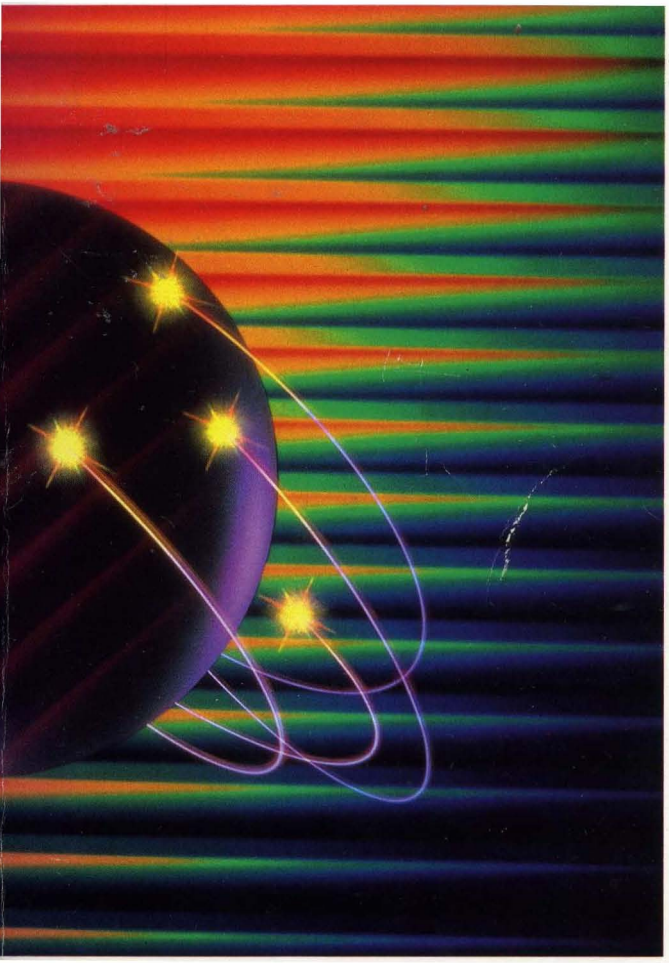
Raytheon



1994 Data Book

ASSP
- Video
- ATE & Instrumentation
- Avionics Communication
- High Speed Communication

Standard Products
- Data Conversion
- Digital Signal Processing
- Linear
- PROMs

ASIC Arrays & Standard Cells
- Analog
- Mixed Analog-Digital

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Advance Information describes products that are not available at the time of printing. Specifications may change in any manner without notice. Contact Raytheon for current information.

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In September 1992, Raytheon Semiconductor Division completed the acquisition of TRW LSI Products, Inc. in La Jolla, California. The TRW products complement Raytheon's growing line of signal processing and multimedia components. The La Jolla operation will continue to develop and introduce leading-edge products for the imaging, graphics, data acquisition and digital signal processing markets.

Contents

Alphanumeric Index

Section 1
Product Innovations

We have accelerated the development of new products at Raytheon Semiconductor, to provide complete, cost-effective solutions to complex problems. We have developed highly integrated solutions for the Multimedia/ Imaging and Automatic Test Equipment markets.

We have highlighted some of the leading products in these areas on the following pages.

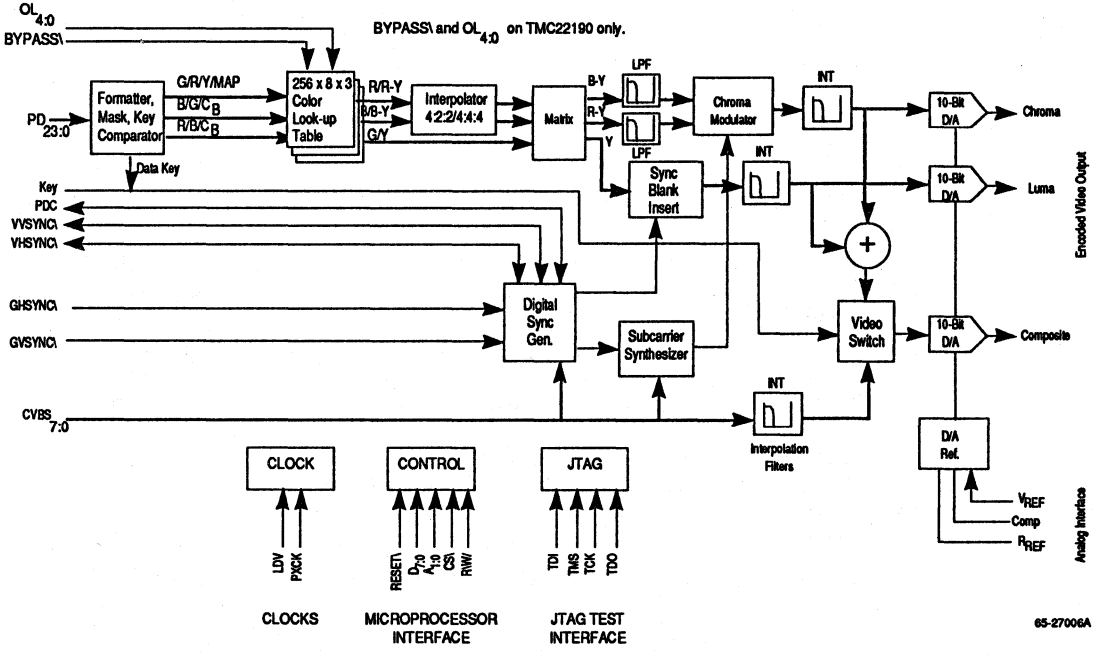
When you have the need for custom mixed-signal ICs, our family of Complementary Bipolar Tile Arrays, CBiCMOS and Standard Cells offer attractive solutions, which are also highlighted.

Contents

TMC22090/22190/TMC22190/22191 Digital Video Encoder and Layering Engine

Features

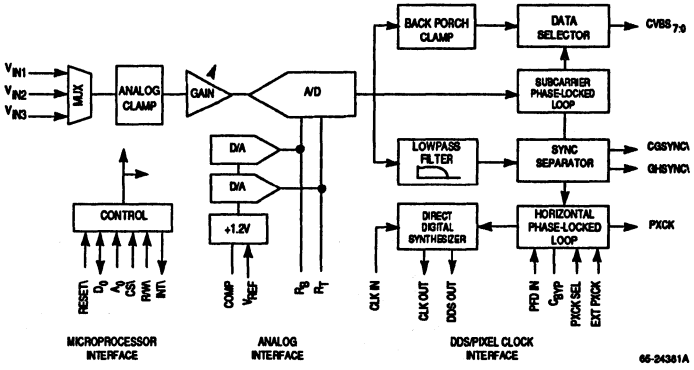
- All digital video encoding
- NTSC-M, PAL-B, G, H, I, M, N formats
- Internal digital oscillators, no crystals required
- Multiple input formats supported:
  - — 24-bit and 15-bit GBR/RGB
  - — YC_BC_R 4:2:2/4:4:4
  - — Color indexed
- 30 overlay colors (TMC22190/TMC22191)
- Fully programmable timing
- Supports pixel rate of 10 to 15 Mpps
- 256 x 8 x 3 color look-up tables (bypassable on TMC2219X)
- 8-bit mask register
- 8-bit composite digital video input
- Hardware and 24-bit data keying
- Synchronizes with TMC22071 Genlocking Video Digitizer
- 8:8:8 video reconstruction
- SMPTE 170M NTSC or CCIR report 624 PAL compatible
- PAL/M
- Simultaneous S-Video (Y/C) NTSC/PAL output
- 10-bit D/A conversion (three channels)
- Controlled edge rates
- Power-down mode
- Built-in color bars and modulated ramp test signals
- JTAG (IEEE Std 1149.1-1990) test interface
- Single +5V power supply
- 84 lead PLCC package



TMC22071 Genlocking Video Digitizer

Features

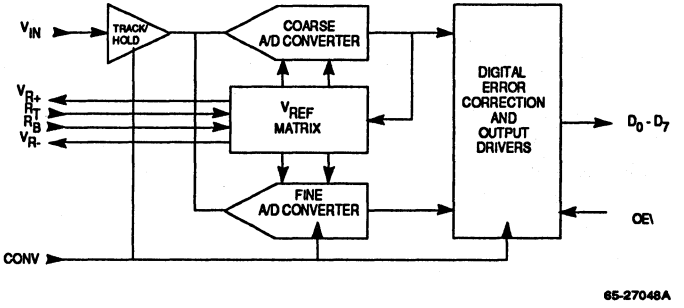
- Fully integrated acquisition
  - 3-Channel video input multiplexer
  - Two-stage video clamp
  - Automatic gain adjustment
  - Sync detection and separation
  - Genlock to NTSC or PAL inputs
  - Clock generation
  - 8-bit video A/D converter
- Microprocessor interface
- Line-locked pixel rates
  - 12.27 MHz NTSC
  - 13.5 MHz NTSC or PAL
  - 14.75 MHz and 1.50 MHz PAL
- Direct interface to TMC22090/TMC22190 encoders
- Built-in circuitry for crystal oscillator
- No tuning or external voltage reference required
- 68 lead PLCC package



TMC1173 2.7 to 3.6 Volt 8-Bit 10 Msps Converter

Features

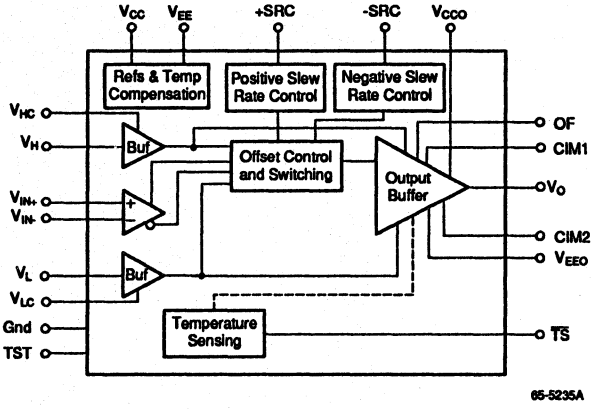
- 8-bit resolution
- 5 and 10 Msps conversion rate
- Integral track/hold
- Differential linearity error <±0.5 LSB
- Single +2.7 to +3.6 volt power supply
- <90 mW power dissipation at 3.6 volts
- Differential phase <0.5°
- Differential gain <1%
- Three-state 3V TTL compatible outputs
- Very low cost



RC7311 250 MHz ATE Pin Electronics Driver

Features

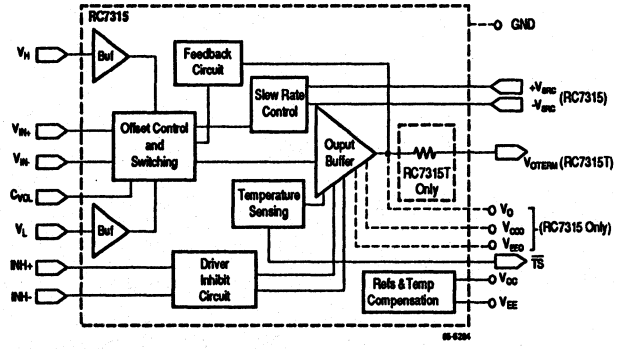
- High output slew rate (2 V/ns minimum)
- Wide output voltage range (-3.0V to +8V), and up to 10 Vp-p swings
- 250 MHz minimum operation for ECL swings
- Wide input common mode range for ease of interface to ECL as well as TTL and CMOS
- Output short-circuit protection with current limiter and thermal shutdown
- 100 mA dynamic switching current drive
- Absolute slew rate control
- Available in 28-pin PLCC
- Low output voltage offset (30 mV) and output offset drift (0.1 mV/°C typ.)
- Low input bias current (1 µA typ.) and current drift (40 nA/°C) for output level program allows direct coupling to a DAC output



RC7315/RC7315T Three-State ATE Pin Electronics Driver

Features

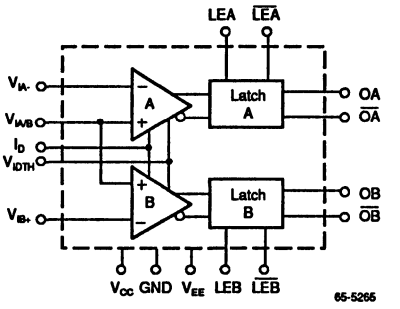
- High output slew rate (1.8 V/ns typ.)
- Wide output voltage range (-2.5V to +7V), and up to 9.5 Vp-p swings
- Three-state/high impedance output
- High repetition rate (250 MHz for ECL swings)
- Low output offset (20 mV typ.) and output offset drift (0.1 mV/°C typ.)
- Low leakage (10 nA typ.) and low output capacitance (3 pF typ.) in high impedance inhibit mode
- RC7315TEL is pin-for-pin compatible with AD1322
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (safe operating area protection with current limiting and thermal shutdown)
- 100 mA typ. dynamic current drive capability
- Absolute slew rate control
- Available in 28-pin PLCC or 16-pin gullwing lead package
- Packaged parts available unterminated (RC7315) or 50Ω series terminated (RC7315T) configurations

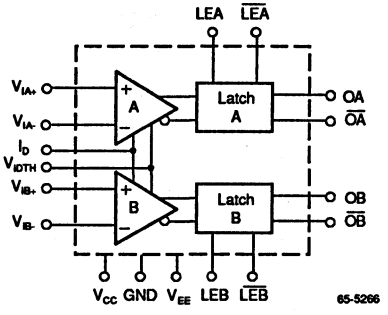


RC7341/RC7342 High Speed Dual Comparator

Features

- 12V max differential input voltage
- Low propagation delays: 2.0 ns maximum
- Low delay dispersion (±50 ps typ.) and drift (4 ps/°C max.)
- ±5 mV maximum input offset and 10 µV/°C max. drift
- 2 µA typical bias current; ±50 pA typ. in disable mode
- Common mode rejection ≥70 dB
- Input disable mode
- 2 pF maximum input capacitance (RC7341)
- Optional latch function
- Available with common threshold input V_{IAB} for lowest input capacitance (RC7341) or two independent comparators (RC7342)
- RC7342 is pin-for-pin compatible with 9687 comparators
- Available in 16-pin SOIC, 20-pin PLCC or 16-pin PDIP

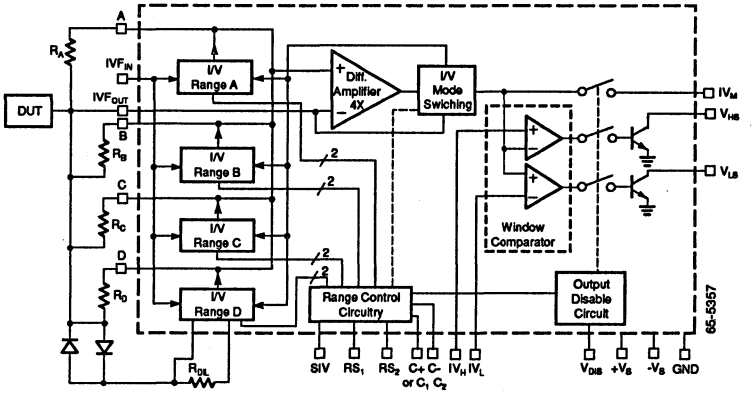




RC7351 Parametric Measurement Unit

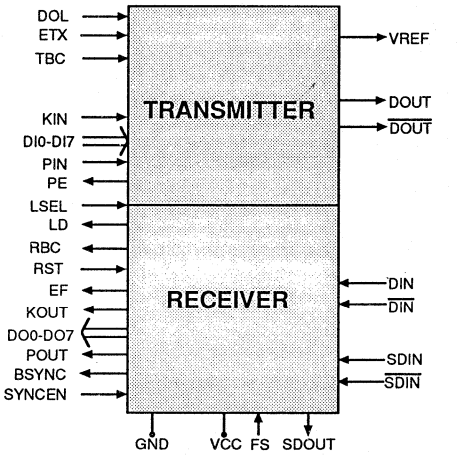
Features

- Force voltage/measure current and force current/ measure voltage functions
- Forced voltage range (-5V to +15V)
- Four programmable measured current ranges: ±500 nA to ± 20 µA, ±2 µA to ±200 µA, ±10 µA to ±1 mA, ±500 µA to ±40 µA
- High resolution current force/measure ±0.05%
- Internal control circuitry for selecting ranges
- High accuracy: 12 bit linearity and 0.5% gain error
- Low current tempco: 5 pA/°C



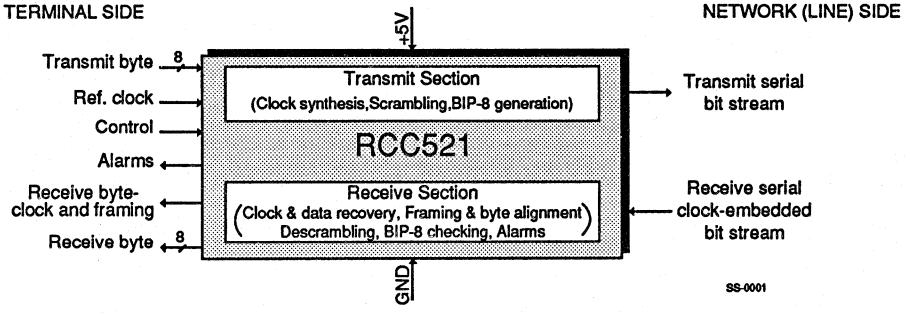
RCC700 ATM/ESCON™/Fibre Channel/SSA™ Transceiver
200 or 265.625 Megabaud

Features
- 200 or 265.625 Megabaud data rates
- Compliant wit the Fibre Channel and ESCON standards
- PLL clock and data recovery
- Clock synthesizer
- On-chip lock detect circuitry
- 8b/10b encode/decode
- Parity generate/check
- Low power dissipation: 600 mW (typ.) @ 200 Mb
- Byte sync on K28.1, K28.5 or K28.7
- Single power supply — +5V
- TTL compatible parallel data inputs/outputs
- PECL compatible serial data inputs/outputs
- Available in 68-pin PLCC and 64-pin PQFP



RCC521 STS-3/STM-1 Synchronizer and Framer

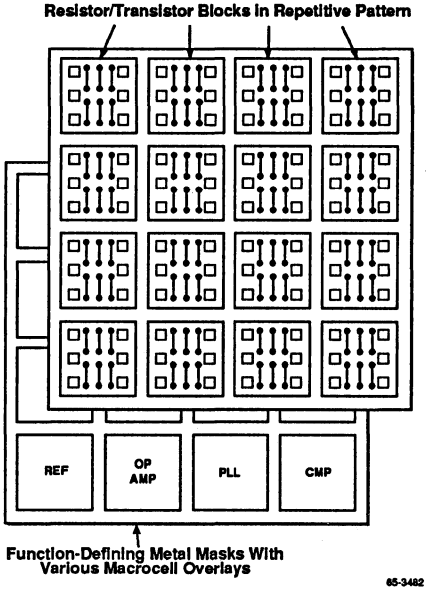
Features
- Transmits/Receives at the STS-3/STM-1 serial data rate of 155.52 Mb/s
- Single supply (+5V) operation
- On-chip clock synthesis and clock and data recovery
- PECL I/O for direct interface to fiber-optic modules
- Detects framing sequence in serial data from network and provides deserialized byte data and 19.44 MHz byte clock to terminal
- Receives 19.44 MHz byte clock and byte data from terminal and provides serial data to network
- Transmit clock may be directly coupled in at 155.52 MHz or synthesized from external 19.44 MHz source
- Receive PLL retains lock even in the absence of transitions in 70 consecutive bit positions
- Scrambling/descrambling and BIP-8 calculation/ checking with optional bypass mode
- Generates LOS (loss of signal), OOF (out of frame), LOF (loss of frame), and RFE (receive frame error) alarms
- Loopback capability at both network and terminal ends
- Test mode allows chip to be tested using an abbreviated frame
- 1.0 W maximum power dissipation
- Fabricated in Raytheon's High Performance CMOS process
- Conforms to ANSI T1.105-1991, CCITT G.708 and Bellcore TR-NWT-000253



VRSA-Tile RPA160 Precision Complementary Tile Array

Features

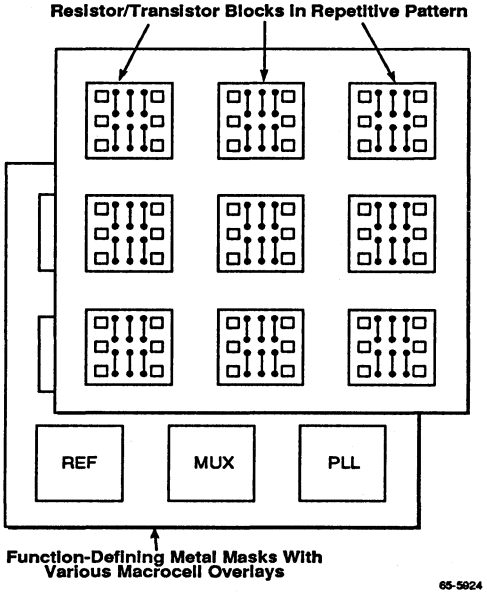
- 16 tiles in a 4 x 4 grid pattern
- 24 NPN and 18 PNPs per tile
- Two high speed Schottky diodes per tile
- Two programmable MOS capacitors per tile
- 13 programmable thin film resistors per tile
- Two metal layer programmability
- Analog pre-designed and characterized macrocells
- SPICE models available for all components and macrofunctions
- Complementary process with f_T of 4 GHz for NPNs and 1.5 GHz for PNPs
- Minimum geometries of 2 micron
- Breakdown voltage BV_{CEO} 13 volts, typical
- Voltage noise for NPN, 2 nV/√Hz
- SiCr thin film resistors:
  - — Sheet resistance 1500 Ω/sq.
  - — Tempco of 50 ppm/°C typical
- PtSi Schottky diodes
- MOS capacitors
  - — Capacitance 0.2 fF/μm²
  - — Temperature stable characteristics



VRSA-Tile RPA90 Precision Complementary Tile Array

Features

- 9 tiles in a 3 x 3 grid pattern
- 24 NPN and 18 PNPs per tile
- Two high speed Schottky diodes per tile
- Two programmable MOS capacitors per tile
- 13 programmable thin film resistors per tile
- Two metal layer programmability
- Analog pre-designed and characterized macrocells
- SPICE models available for all components and macrofunctions
- Complementary process with f_T of 4 GHz for NPNs and 1.5 GHz for PNPs
- Minimum geometries of 2 micron
- Breakdown voltage BV_{CEO} 13 volts, typical
- Voltage noise for NPN, 2 nV/√Hz
- SiCr thin film resistors:
  - — Sheet resistance 1500 Ω/sq.
  - — Tempco of 50 ppm/°C typical
- PtSi Schottky diodes
- MOS capacitors
  - — Capacitance 0.2 fF/μm²
  - — Temperature stable characteristics



RSC4000 CBiCMOS Standard Cells

Features

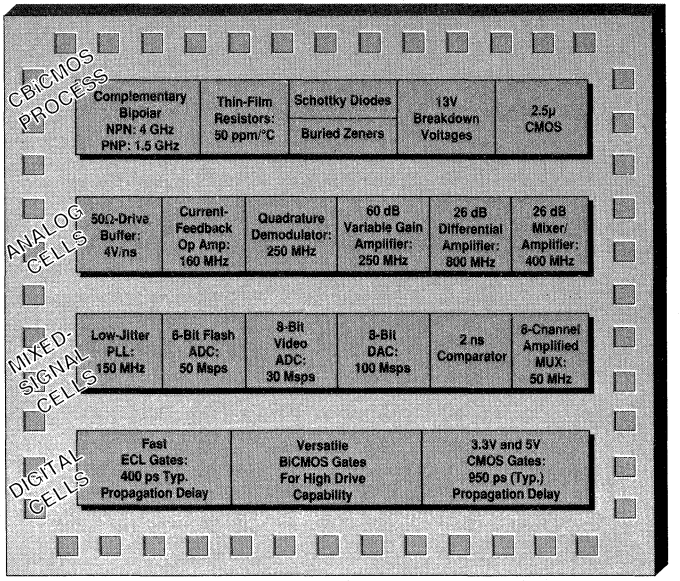
- Complementary process with f_T of 4 GHz for NPNs and 1.5 GHz for PNPs
- Minimum geometries of 2 micron
- Breakdown voltage BV_{CEO} 13 volts, typical
- Voltage noise for NPN, 2 nV/√Hz
- SiCr thin film resistors:
  - — Sheet resistance 1500 Ω/sq.
  - — Tempco of 50 ppm/°C typical
- PtSi Schottky diodes
- MOS capacitors
  - — Capacitance 0.2 fF/μm²
  - — Temperature stable characteristics

Cells Available

- Amplifiers
- Buffers
- Voltage comparators
- Voltage references
- Signal conditioning
- Data recovery
- Data conversion
- Gates, Inverters, Buffers
- Flip-flops, Latches
- Input/Output Translators
- Multiplexer, Decoder, Bandgap References
- CMOS gates

CMOS Features

- Minimum geometry of 2.5 micron with L_{EFF} for PMOS/NMOS transistors of 1.8 microns
- Breakdown voltage BV_{DSS} 13 volts typical
- Internal gate delay <1.5 ns
- 3.3V or 5.0V supply voltage

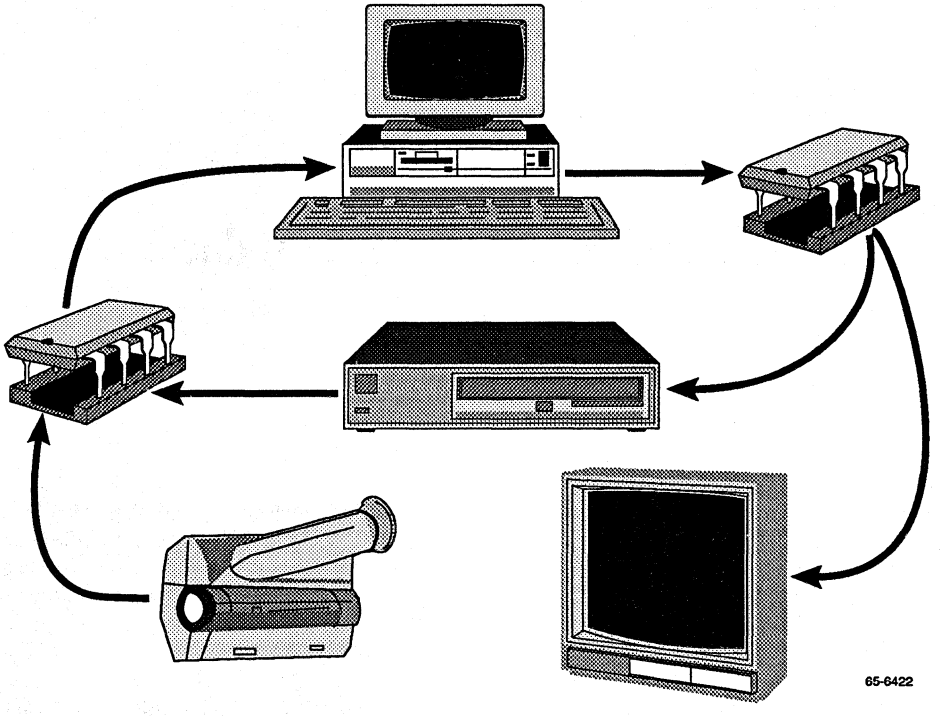


Section 2
Application Specific Standard Products

Modern electronic systems are at once becoming more flexible and more specialized. As a particular systems-level technology develops, key functional elements can be identified that are appropriately tailored to the SPECIFIC demands of that APPLICATION. This provides a higher level of integration than can be employed in a building block approach to system design. Yet these products serve a sufficiently broad market that they can be offered as STANDARD PRODUCTS.

Raytheon Semiconductor has developed families of Application Specific Standard Products (ASSPs) that address the specialized needs in six market areas: Multimedia/Video/Imaging, ATE, Instrumentation, Signal Synthesis, Avionics Communications and High Speed Communications. Through the use of leading-edge mixed-signal design and processing expertise, our families of ASSPs offer a winning combination of high performance, high integration, and low cost.

Contents



Multimedia/Video/Imaging

Raytheon has provided image processing components to the television broadcasting industry since the mid 1970s; many of the products in this selection guide have applications in this area.

The TMC22071 Genlocking Video Digitizer includes everything needed to convert analog NTSC or PAL video into digitized composite video, all on a single CMOS IC. The TMC22X9X and TMC22190 Digital Video Encoders take images in RGB, YC_BC_R, or color-indexed space and converts them to NTSC or PAL in both composite and S-Video formats.

Specifically designed for image processing are the Image Resampling Sequencers (TMC2301 ,TMC2302). These address generators are given an image manipulation transfer function representing a shift, rotate, warp, or zoom. They produce sets of memory pixel addresses that translate to the desired pixel in the output image. High-speed processing elements such as the TMC2249 Mixer and TMC2250 Matrix Multiplier accept these input pixels and compute the values of the output pixels.

The TMC2272 Colorspace Converter is a completely programmable device that can convert between any two color image representations (working in conjunction with the TMC2330 Coordinate Transformer when dealing with HSI-type formats).

The TMC2330 itself is tailored to convert between vector and rectangular coordinate systems — as is necessary to put a radar or ultrasound image on a raster scan display. It is used in general vector image processing, as well as reconstructing CAT and NMR images.

The TMC2311 Fast Cosine Transform is the fundamental element in the common approaches to image compression.

Other products include a Half-Band Filter, Image Convolver, Digital Mixer, and Image Filters — all designed to process images efficiently in real-time.

Video Image Processing Products

Product	Description	Size	Clock Rate[1] (MHz)	Power[1] (Watts)	Package	Grade[2]	Notes	Page
TMC22071	Genlocking Digitizer	8 bit	30		R1	C	Genlocking digitizer with input MUX, clamp, sync separator, clock generator, subcarrier PLL.	2-5
TMC22090	Digital Video Encoder	10 bit	30	1.1	R0	C	All-Digital Encoder, RGB/YC_RC_B/Color Index Input. NTSC/PAL Composite and S-Video Output.	2-27
TMC22091	Digital Video Encoder	10 bit	30	1.1	R0	C	TMC22090 with PAL-M,N and NTSC Japan.	
TMC22190	Digital Video Encoder	10 bit	30	1.1	R0	C	TMC22090 with added layering engine.	2-27
TMC22191	Digital Video Encoder	10 bit	30	1.1	R0	C	TMC22091 with added layering engine.	
TMC2242-1	Half-Band Digital Filter	12/16 bit	40	0.5	R2	C	2:1 interpolate or decimate.	2-95
-			30	0.5	R2	C	Low-pass (-6 dB @ 0.25F).	
TMC2243	Video Filter	10x10x3	20	0.5	G8, H8	C, V	Cascadeable.	2-109
TMC2246-1	Image Filter	10x11 bit	40	0.5	H5, L5	C, V	Four-pixel interpolator.	2-123
-			30	0.5	H5, L5	C, V		
TMC2249-1	Digital Mixer	12x12x2	30	0.5	H5, L5	C, V	Cascadeable.	2-135
-			25	0.5	H5, L5,	C, V	Programmable Delays.	
TMC2250-2	Matrix Multiplier	12x10x9	40	1.2	H5	C	2D convolution 3x3, 2x4.	3-335
-1			36	1.2	H5, G1	C, V	1D convolution, 9 taps.	
-			30	1.2	H5, G1	C, V	3x3 matrix x 3x1 vector	
TMC2255-1	2D Convolver	5x5x8 bit	12.5	0.6	R1	C	3x3, symmetric 5x5.	2-149
-			10	0.6	R1	C	2D convolver.	
TMC2272-2	Color Space Converter	3x12 bit	40	1.2	H5	C	3x3 matrix x 3x1 vector.	2-169
-1			36	1.2	H5	C		
-			30	1.2	H5	C		
TMC2301-2	Image Resampling	4Kx4K pixels	20	0.5	G8, R1	C	Second order.	2-187
-1	Sequencer		18	0.4	G8, R1	C, V, SMD	2-dimension.	
-			15	0.4	G8, R1, L1	C, V		
TMC2302-1	Image Manipulation	65Kx65K	40	0.4	H5	C	Third order.	2-2-213
	Sequencer	pixels	30	0.4	H5	C	3-dimension.	
TMC2311-2	Fast Cosine Transform	12 bit	17.8	0.7	R1	C	Data compression processor.	3-301
-1			14.5	0.7	R1	C	Meets CCITT specification.	
-			17.8	0.7	R1	C	8 x 8, 2-dimension.	
TMC2330-1	Coordinate Transformer	16x16 bit	25	0.7	H5, L5	C, V	Cartesian ↔ polar conversion	3-319
-			20	0.7	H5, L5	C		

Product	Resolution (bits)	Diff. Lin Error[1] (±%)	Conv. Rate[1] (Msps)	Rise Time[1] (ns)	Package	Grade (2)	Notes	Page
Digital Frequency Synthesizers								
TMC2340-1	25	0.006	106	Dual 16 Bit	G1, H5, L5	C, V	AM, FM, PM inputs.	2-315
-	20	0.006	106	Dual 16 Bit	G1, H5, L5	C, V	Quadrature outputs.	
Associated D/A Converters								
TDC1041-1	10	0.048	20	4	R3	C	Low cost 10-bit video D/A TTL interface.	3-195
-	10	0.096	20	4	R3	C		
TDC3310	10	0,.096	40	10	N6, R6	C	Single +5V power supply.	3-239
TDC1141-1	10	0.048	50	4	R3	C	Low cost 10-bit video D/A	3-225
-	10	0.096	50	4	R3	C	ECL interface.	
TDC1012-3	12	0.012	20	4	J7, N7, R3	C	Signal synthesis D/A.	3-153
-2	12	0.024	20	4	J7, N7, R3	C, V, SMD	70 dBc SFDR. Very low glitch.	
-1	12	0.048	20	4	J7, N7, R3	C, V, SMD	Drives 25Ω directly.	
-	12	0.048	20	4	J7, N7, R3	C, V	TTL interface.	

Product	Resolution Bits	Differential Linearity Error [1] (±%)	Conv Rate [1] (Msps)	Rise Time[1]	Package	Grade[2]	Notes	Page
TDC1112-3	12	0.012	50	4	N7, R3	C	Signal synthesis D/A. 70 dBc SFDR. Very low glitch.	3-207
-2	12	0.024	50	4	J7, N7, R3	C, V, SMD	Drives 25Ω directly. ECL interface.	3-35
-1	12	0.048	50	4	J7, N7, R3	C, V, SMD		
-	12	0.048	50	4	J7, N7, R3	C, V		
TDC1044	4	25	—		B9, N9	C, V, SMD		3-35
TDC1046	6	25	33		B8	C, V, SMD		3-45
TDC1047	7	20	39		B7	C, V		3-53
TDC1147	7	15	36		B7	C, V	No pipeline delay. Well suited to subranging converter applications.	3-95
TDC1035	8	—	—		B7	C, V	Peak digitizer. Digitizes peak value of pulses as narrow as 12 ns.	3-17
TDC1038	8	20	45		B6, N6, R3 E1	C, V	Low power version of TDC1048.	3-25
TDC1048	8	20	45		B6, N6 C3, E1	C, V, SMD	Industry standard video A/D.	3-63
TDC1058	8	20	45		B6, N6, R3, E1	C	New industry standard video A/D. Single +5V power supply. TDC1048 performance equivalent.	3-83
TMC1173-10	8	10	45		N2, M7, R3	C	Low power CMOS video A/D w/ integral Track/Hold.	3-105
-05	8	5	45		M7, N2, R3	C	+2.7V to +3.3V power supply.	
TMC1175-20	8	20	45		B2, N2, C3, M7, R3	C, V	Low power CMOS video A/D with integral Track/Hold.	3-121
-30	8	30	45		M7, N2, R3	C, V		
-40	8	40	45		M7, N2, R3, E1	C, V	Includes D/A	
TDC1049	9	30	48		J0, J3, C1, L1, G8, E1	C, V, SMD C, V, SMD	ECL interface	3-73
TDC1020	10	20	55		J1, G0, E1	C, V	Monolithic video A/D, TTL interface. ±2V input range.	3-5
DAC-08	8	0.1	1.0	—	N, D	C, V, SMD, JAN		3-139
TDC1018-1	8	0.20	200	1.7	B7, C3	C	Low cost ECL. Graphics-ready.	3-183
-	8	0.20	125	1.7	B7, C3	C		
TDC1016-10	10	0.05	20	4	N7, N5, B7, B5	C	Industry standard video DAC.	
-9	10	0.10	20	4	N7, N5, B7, B5	C, A	Operates with TTL or ECL logic.	
-8	10	0.20	20	4	N7, N5, B7, B5	C, A		
TDC1041-1	10	0.048	20	4	R3	C	Low cost 10-bit video D/A TTL interface.	3-198
-	10	0.096	20	4	R3	C		
TDC3310	10	0.096	40	10	N6, R6	C	Single +5V power supply	3-239

Notes:

1. Guaranteed. See product specifications for test conditions.
2. A = High reliability, T_C = -55°C to 125°C.
   B = Industrial, T_C = -25°C to 85°C
   C = Commercial, T_A = 0°C to 70°C.
   F = Extended Temperature Range, T_C = -55°C to 125°C
   V = MIL-STD-883 Compliant, T_C = -55°C to 125°C.
   SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C.
3. A = High reliability, T_C = -20°C to 95°C.

TMC22071
Genlocking Video Digitizer

The TMC22071 Genlocking Video Digitizer converts standard baseband composite NTSC or PAL video into 8-bit digital composite video data. It extracts horizontal and vertical sync signals and generates a pixel clock for the on-board 8-bit A/D converter and a 2X clock for the transfer of data to subsequent video processing or encoding with the TMC22X9X Digital Video Encoder family. It also measures the color subcarrier phase and frequency, and provides this data to the Encoder (for genlocked color NTSC or PAL encoding), or a frame buffer (for frame capture) over the digital composite video port.

The TMC22071 includes a three-channel video input multiplexer, analog clamp, variable gain amplifier, and digital back porch clamp. The on-board oscillator circuitry generates the clock from a 20 MHz crystal or the clock source may be an external oscillator. It is programmable over a microprocessor interface for NTSC or PAL operation. No external component changes and no production tuning or service adjustments are ever required.

The TMC22071 is fabricated in an advanced CMOS process, and is packaged in a 68-lead PLCC. Its performance is guaranteed from 0°C to 70°C.

Features

- Fully integrated acquisition
- 3-channel video input multiplexer
- Two-stange video clamp
- Automatic gain adjustment
- Sync detection and separation
- Genlock to NTSC or PAL inputs
- Clock generation
- 8-bit video A/D converter
- Microprocessor interface
- Line-locked pixel rates
  - — 12.27 MHz NTSC
  - — 13.5 MHz NTSC or PAL
  - — 14.75 MHz and 15.0 MHz PAL
- Direct interface to TMC22X9X encoders
- Built-in circuitry for crystal oscillator
- No tuning or external voltage reference required
- 68-lead PLCC package

Applications

- Frame Grabber
- Digital VCR/VTR
- Desktop Video

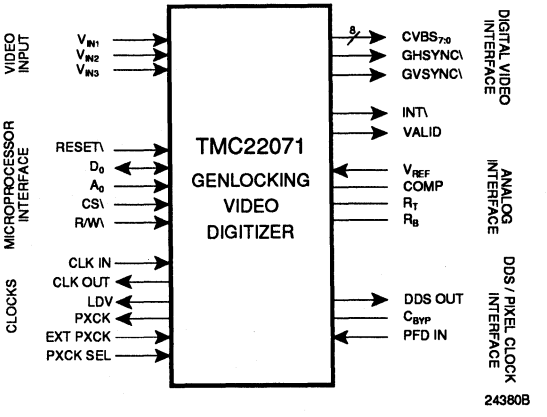
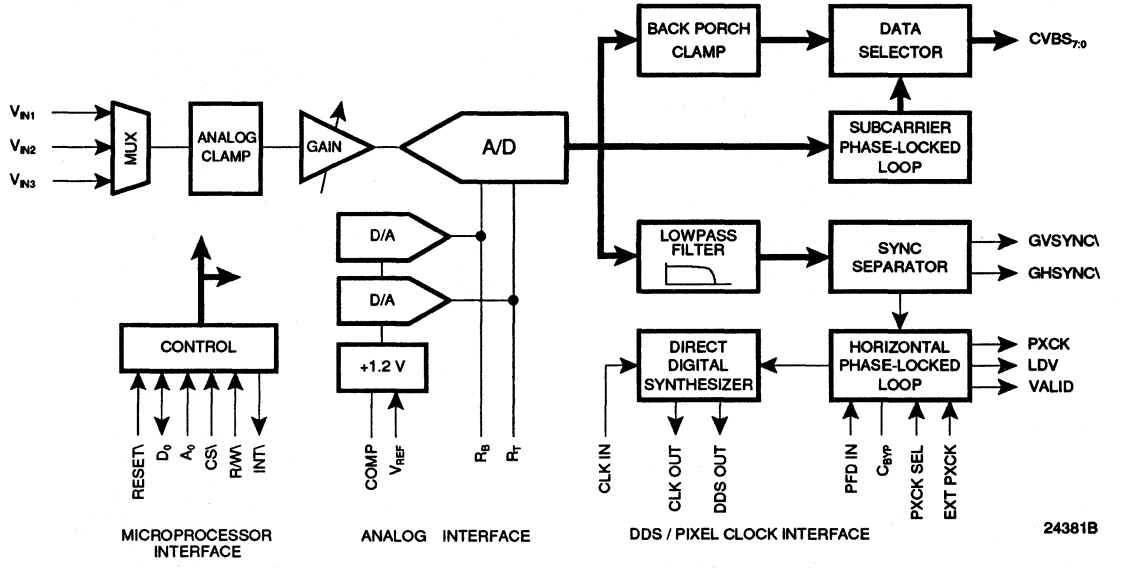


Figure 1. Logic Symbol

Figure 2. Functional Block Diagram



General Description

The TMC22071 is a fully-integrated genlocking video A/D converter which digitizes NTSC or PAL baseband composite video under program control. It accepts video on three selectable input channels, adjusts gain, clamps to the back porch, and digitizes the video at a multiple of the horizontal line frequency. It extracts horizontal and vertical sync, measures the subcarrier frequency and phase (relative to the sampling clock), and provides this data along with digital composite video data over an 8-bit digital video port. Two sync outputs (GHSYNC\ and GVSYNC\) are also provided. It generates 1x (LDV) and 2x (PXCK) pixel clocks (PXCK) for data transfer. PXCK also serves as a master clock for the companion TMC22x9x Encoders.

Operating parameters are set up via a standard microprocessor port. Provisions have been made for internal or external voltage reference operation.

Timing

The TMC22071 operates from an internally-synthesized clock, PXCK, which runs at twice the pixel data rate. The nominal pixel rates may be set to 12.27 Mpps for NTSC, 13.5 Mpps for NTSC and PAL, and 14.75 Mpps or 15.0 Mpps for PAL operation.

Video Input

Three high-impedance video inputs are selected by an internal multiplexer under host processor control. The device accepts industry-standard video levels of 1.23 Volts (sync tip to peak color). Good channel-to-channel isolation allows active video on all three inputs simultaneously. Anti-aliasing filtering (if used) and line termination resistors must be provided externally. The input selection is controlled by two bits in the Control Register.

Analog Clamp

The front-end analog clamp ensures that the input video falls within the active range of the A/D converter. The digitized composite video output is clamped to the back porch by a secondary digital clamp.

Automatic Gain Adjustment

Since video signals may vary substantially from nominal levels, the TMC22071 performs an automatic level setting routine to establish correct signal amplitudes for digitizing.

The TMC22071 relies upon the presence of the sync tip-to-back porch voltage to determine the gain required for the input video signal.

Sync tip compression or clipping is often affected by APL (Average Picture Level) variation. Rather than tracking minor variations in sync tip amplitude and constantly adjusting video gain, the TMC22071 establishes proper signal amplitudes during initial genlock acquisition, and then (optionally) holds the gain constant. This results in a stable picture under variable signal conditions.

Improper termination of video cables (usually double termination) is handled in the TMC22071 by a selectable gain of +1.0 or +1.5. The higher gain is used to amplify a doubly-terminated signal which is reduced in amplitude by 2/3.

If the input signal levels are well controlled, the automatic gain adjustment can be disabled and the gain held at its nominal value (+1.0 or +1.5).

Analog-to-Digital Converter

The TMC22071 contains a high-performance 8-bit A/D converter. Its gain and offset are automatically set as a part of the automatic gain adjustment process during initial signal acquisition, and require no user attention.

The reference voltages to the A/D converter are set up by internal D/A converters under automatic control during genlock acquisition. These voltages determine the gain and offset of the A/D converter with respect to the video level presented at its input.

Low-pass Filter

The digitized composite video stream is digitally low-pass filtered to remove chrominance components from the sync separator. Filtering provides robust operation by optimizing the signal-to-noise ratio of the synchronizing/blanking portion of the video, improving the accuracy of the back porch blanking level detector.

A digital sync separator provides the output sync signals, GHSYNC\ and GVSYNC\, and times internal operations.

Horizontal Phase-Locked Loop

A phase-locked loop generates PXCK, at twice the pixel rate. The reference signal for the horizontal phase-locked loop is generated by the Direct Digital Synthesizer (DDS). The DDS output is constructed with an internal D/A converter and is output from the TMC22071 via the DDS OUT pin. This signal is passed through an external LC filter and input to the horizontal phase-locked loop.

The phase of the DDS output is proportional to the phase difference between PXCK and the horizontal sync of the incoming signal.

A 20 MHz clock is required to drive the DDS. This may be input to the TMC22071 via CMOS levels on the CLK IN pin. Alternately, a 20 MHz crystal may be directly connected between CLK IN and CLK\ OUT with tuning capacitors to activate the internal crystal oscillator circuitry.

Subcarrier Phase-Locked Loop

A fully-digital phase-locked loop is used to extract the phase and frequency of the incoming color burst. These frequency and phase values are output over the CVBS bus during the horizontal sync period.

Back Porch Digital Clamp

A digital back-porch clamp is employed to ensure a constant blanking level. It digitally offsets the data from the A/D converter to set the back porch level to precisely 40_h for PAL and $3C_h$ for NTSC.

Digitized Video Output

The digitized 8-bit video output is provided over an 8-bit wide CVBS data port, synchronous with PXCK and LDV. Subcarrier frequency, and subcarrier phase data are transmitted over $CVBS_{7-0}$ during the horizontal sync tip period.

Microprocessor Interface

Since microprocessor buses are notoriously "noisy" from a wide-band analog point of view, the microprocessor interface bus is only one bit wide, rather than the more customary eight. The operation of this bus is similar to other bus-controlled devices except that the TMC22071 internal Control Register is accessed one bit at a time.

A sequence of 47 bits is written to or read from the LSB of a standard microprocessor port. Writing to or reading from the secondary address results in the transfer of data to or from the internal shift register.

The RESET\ input, when LOW, sets all internal state machines to their initialized conditions. Returning the RESET\ pin HIGH starts the signal acquisition sequence which lasts until locking with the gain-adjusted and clamped video signal is achieved.

Pin Functions

Video Input

V_{IN1-3}	Video inputs, 1.25 Volts peak-to-peak, sync tip to peak color.

Clocks

CLK IN	20 MHz CMOS clock input to DDS. This pin may also be used along with CLK\ OUT for directly connecting crystals.
CLK\ OUT	Inverted DDS clock output. This pin may also be used along with CLK IN for directly connecting a crystal.
LDV	Delayed pixel clock output. LDV runs at 1/2 the rate of PXCK and its rising edge is useful for transferring CVBS digital video from the TMC22071 to the TMC22x9x Digital Video Encoders.
PXCK	2x oversampled line-locked clock output.
EXT PXCK	Input for external PXCK clock source.
PXCK SEL	Select input for internal or external PXCK. When HIGH, the internally generated line-locked PXCK is selected. When LOW, the external PXCK source is enabled.
VALID	This output, when HIGH indicates that incoming horizontal sync has been detected and is within the +/-16 pixel window in time established by previous sync pulses. When LOW, it indicates that incoming horizontal sync has not bee found within the expected time frame.
INT\	This output is LOW if the internal horizontal phase lock loop is unlocked with respect to incoming video for 128 or more lines per field. After lock is established, INT\ goes HIGH.

Digital Video Interface

GHSYNC\ — When the TMC22071 is locked to incoming video, the GHSYNC\ pin provides a negative-going pulse after the falling edge of the horizontal sync pulse. There is a fixed number of PXCK clock cycles between adjacent falling edges of GHSYNC\.

GVSYNC\ — When the TMC22071 is locked to incoming video, the GVSYNC\ pin provides a negative-going edge after the start of a vertical sync pulse.

$CVBS_{7-0}$ — 8-bit composite video data is output on this bus at 1/2 the PXCK rate. During the horizontal blanking interval, field ID, subcarrier frequency, and subcarrier phase are available on this bus.

Microprocessor Interface

D_0 — Microprocessor data port. All control parameters are loaded into and read back from the Control Register over this 1-bit bus.

A_0 — Microprocessor address bus. A LOW on this input loads the I/O Port Shift Register with data from D_0 and CS\. A HIGH transfers the I/O Port Shift Register contents into the Control Register on the last falling edge of CS\.

CS\ — When CS\ is HIGH, D_0 is in a high-impedance state and ignored. When CS\ is LOW, the microprocessor can read or write D_0 data into the Control Register.

RESET\ — Bringing RESET\ LOW forces the internal state machines to their starting states, loads the Control Register with default values, and disables outputs. Bringing RESET\ HIGH restarts the TMC22071.

R/W\ — When R/W\ and A_0 are LOW, the microprocessor can write to the Control Register over D_0. When R/W\ is HIGH and A_0 is LOW, the contents of the Control Register are read over D_0.

Analog Interface

V_{REF} — +1.23 Volt reference. When the internal voltage reference is used, this pin should be decoupled to A_{GND} with a 0.1 µF capacitor. An external +1.2 Volt reference may be connected here, overriding the internal reference source.

COMP — Compensation for DDS D/A converter circuitry. This pin should be decoupled to V_{DDA} with a 0.1 µF capacitor.

R_T, R_B — Decoupling points for A/D converter voltage references. These pins should be decoupled to A_{GND} with a 0.1 µF capacitor.

Loop Filter Interface

DDS OUT — Analog output from the internal Direct Digital Synthesizer D/A converter.

PFD IN — Analog input to the Phase/Frequency Detector of the horizontal phase-locked loop

C_{BYP} — Decoupling point for the internal comparator reference of the Phase/Frequency Detector. This pin should be decoupled to A_{GND} with a 0.1 µF capacitor.

Power Supply

V_{DDA} — Positive power supply to analog section.
V_{DD} — Positive power supply to digital section.
A_{GND} — Ground for analog section.
D_{GND} — Ground for digital section.

Table 1. Package Interconnections

Signal Type	Name	Function	Value	Package Pin
Video Input	V_{IN1-3}	Composite Video Input	1.23Vp-p	34, 31, 29
Clocks	CLK IN	20 MHz DDS clock input	CMOS	51
	CLK\ OUT	Inverted clock output	CMOS	53
	PXCK	2x Pixel clock output	CMOS	19
	LDV	Pixel clock output	CMOS	17
	EXT PXCK	External PXCK input	CMOS	54
	PXCK SEL	PXCK source select	CMOS	46
Digital Video	GHSYNC\	Horizontal sync output	CMOS	12
	GVSYNC\	Vertical sync output	CMOS	13
	$CVBS_{7-0}$	Composite output bus	CMOS	11-9, 6-2
µP I/O	D_0	Data I/O port	TTL	66
	A_0	µP port control	TTL	60
	CS\	Chip select	TTL	62
	RESET\	Master reset input	TTL	64
	R/W\	Bus read/write control	TTL	61
	INT\	Interrupt output	TTL	67
	VALID	HSYNC locked flag	TTL	14
Analog	V_{REF}	V_{REF} input/output	+1.23 V	38
	COMP	Compensation capacitor	0.1 µF	48
	R_T,R_B	A/D V_{ref} decoupling	0.1 µF	36, 28
PLL Filter	DDS OUT	Internal DDS output		45
	PFD IN	Horizontal PLL input		43
	C_{BYP}	Comparator bypass	0.1 µF	42
Power	V_{DDA}	Analog power supply	+5 V	23, 25, 26, 30, 33, 40, 47
	V_{DD}	Digital power supply	+5 V	1, 7, 18, 22, 52, 58, 59, 63
Ground	A_{GND}	Analog ground	0.0 V	24, 27, 32, 35, 37, 39, 41, 44, 49,
	D_{GND}	Digital ground	0.0 V	8, 15, 16, 20, 21, 50, 55-57, 65, 68

Control Register Bit Functions

Bit	Mnemonic	Function
0	SRESET	Software reset. When LOW, resets and holds internal state machines, resets Control Register with previously written values, and disables output drivers. When HIGH, SRESET starts and runs state machines, PXCK, and enables outputs.
1-3	FORMAT	Input signal format select. 000 NTSC at 12.27 Mpps. 001 NTSC at 13.5 Mpps. 010 PAL_A at 14.75 MPPS. 011 PAL_B at 15.0 Mpps. 1xx PAL at 13.5 Mpps.
4-6	TEST	Factory test control bits. These should be set LOW.
7,8	SOURCE	Video source select. 00 V_{IN1} 01 V_{IN2} 1x V_{IN3}
9	VGAIN	Video gain. When LOW, gain is set to +1.0. When HIGH, gain is set to +1.5.
10-16	TEST	Factory test control bits. These should be set LOW.
17-24	LEADLAG	This control word allows the HSYNC to be time-shifted -122 to +132 LDV cycles. When LEADLAG is $7B_h$, HSYNC and incoming video are in alignment. A value of 83_h delays HSYNC eight LDV cycles. A value of 73_h advances HSYNC eight

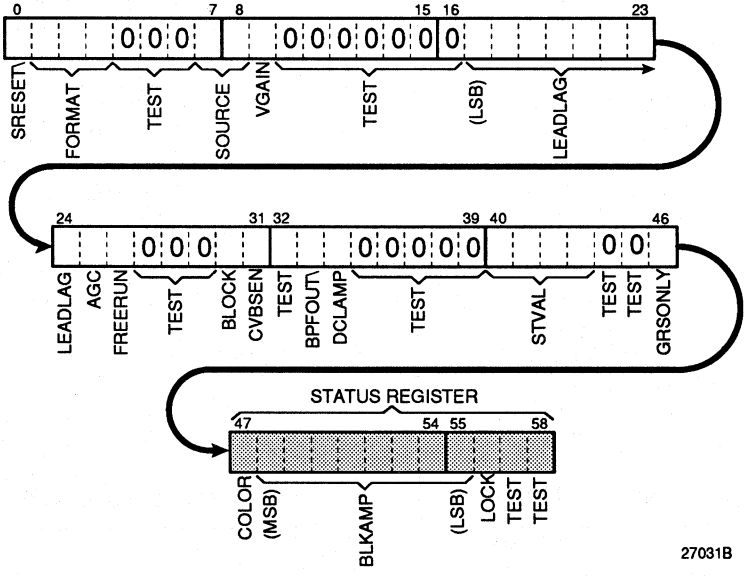
Bit	Mnemonic	Function
		LDV cycles. Bit 24 is the MSB.
25	AGC	AGC operation control. After initial H and V sync acquisition, AGC operation is continuous for two fields and then held when this bit is LOW. When HIGH, AGC is triggered for two fields and then held.
26	FRERUN	When HIGH, a free-running PXCK is generated, independent of incoming video. When LOW, PXCK is locked to incoming video.
27-29	TEST	Factory test control bits. These should be set LOW.
30	BLOCK	Block sync enable. When HIGH, block sync is accepted and sync tip clamping during the vertical interval is disabled.
31	CVBSEN	CVBS bus enable. When LOW, the $CVBS_{7-0}$, GHSYNC\, and GVSYNC\ outputs are in a high-impedance state. When HIGH, they are enables.
32	TEST	Factory test control bit. This should be set LOW.
33	BPFOUT\	Burst phase / frequency output control. When HIGH, GRS is disabled. When LOW, burst phase and frequency information is output on $CVBS_{3-0}$.

Multimedia

Bit	Mnemonic	Function
34	DCLAMP	Digital clamp enable. The digital clamp is enabled when DCLAMP is HIGH and disabled when LOW.
35-39	TEST	Factory test control bits. These should be set LOW.
40-43	STVAL	Sync tip value. When DCLAMP is HIGH and STVAL is set to its default value 3_h, the output sync level is 3_h for NTSC and 7_h for PAL. Bit 43 is the MSB.
44-45	TEST	Factory test control bits. These should be set LOW.
46	GRSONLY	When the horizontal phase lock loop is unlocked and this Control Bit is LOW, all CVBS data is forced LOW except the GRS signals.

Bit	Mnemonic	Function
		The presence of GRS also depends upon bit 33.
		Status Bits (read only)
47	COLOR	Burst present status bit. This bit is LOW when no burst is present on the input video. It is HIGH when burst is present.
48-55	BLKAMP	Blanking amplitude status bits. These eight bits report the actual blanking level.
56	LOCK	Genlocked status bit. When LOW, the TMC22071 is not locked to an input signal. When HIGH, lock has been achieved.
57-58	TEST	These are read-only bits for testing purposes only.

Figure 3. Control Register Map



Control and Status Registers

The TMC22071 is controlled by a single 47-bit long Control Register. Access to the Control Register is via the I/O Port Shift Register arranged as shown in Figure 4. The Control Register can be read and written, permitting software modification and examination of its contents. The 12-bit Status Register is read-only and accessed through the same I/O Port Shift Register. Reading the Status Register yields information about blanking level, subcarrier presence, and whether or not PXCK is locked or unlocked with respect to the line rate.

The host processor writes data into the TMC22071 using only one bit of the microprocessor's data and address bus. Once the shift register has input and positioned the 47 bits of desired data (bit 46 first, bit 0 last), a HIGH on A_0 and a LOW on R/W\ when CS\ falls transfers the I/O Port Shift Register contents to the Control Register. The I/O Port Shift Register, Control Register and Status Register are governed by CS\ , R/W\ , and A_0. R/W\ and A_0 are latched by the TMC22071 on the falling edge of CS\ and data input D_0 is latched on the rising edge of CS\. Data read from D_0 is enabled by the falling edge of CS\ and disabled by the rising edge of CS\.

The full sequence of 47 bits of Control Register data must be written each time a change in that data is desired. All or a few of the Control and Status Register bits may be read, but the sequence always begins with bit 58 of the Status Register.

Figure 4. Control and Shift Register Structure

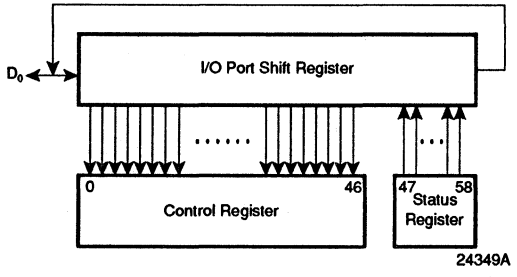


Table 2. Microprocessor Port Control

A_0	R/W\	Action
0	0	Write data from D_0 into I/O Port Shift Register
0	1	Read D_0 data from last stage of I/O Port Shift Register
1	0	Transfer I/O Port Shift Register contents to Control Register
1	1	Enables continuous update of status bits in I/O Port Shift Register

Figure 5. Data Write Sequence

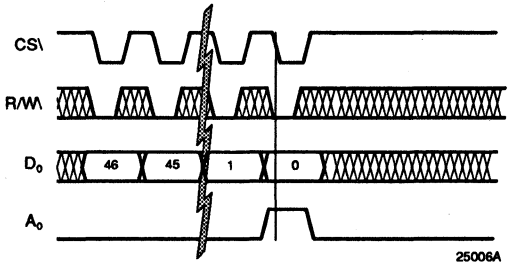
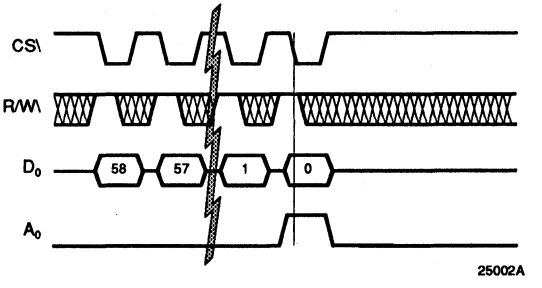


Figure 6. Data Read Sequence



Horizontal Timing

Horizontal line rate is selectable, and is determined by the FORMAT control bits (12.27 Mpps for NTSC, 13.5 Mpps for NTSC and PAL, and either 14.75 or 15.0 Mpps for PAL). Figure 7 illustrates the horizontal blanking interval. Figure 8 completes the definition of timing parameters with vertical blanking interval detail.

Programming the TMC22071

Upon power-up after bringing RESET\ LOW, the TMC22071 Control Register is set to default values as shown in the top entry of Table 4. These default values do not necessarily render the TMC22071 operational in any specific application. Before the TMC22071 is expected to acquire input video, its Control Register must be loaded with data that is specific to its use.

Figure 7. Horizontal Sync Timing

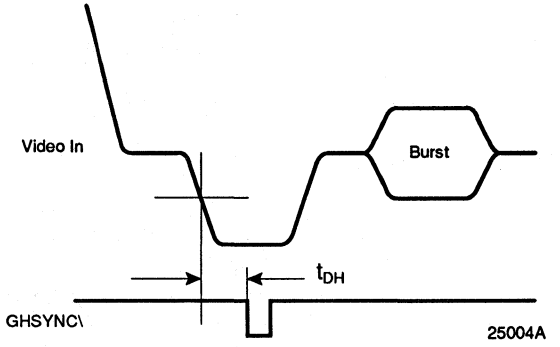


Figure 8. Vertical Sync Timing

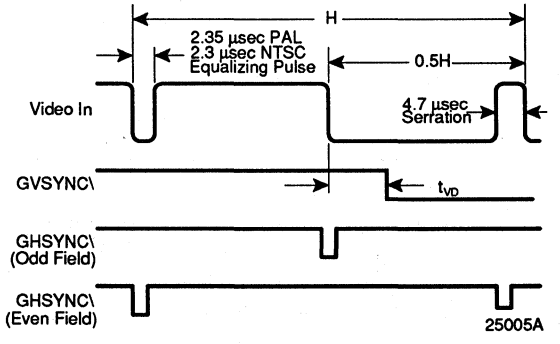


Figure 9. Output Data vs. Input Video Level

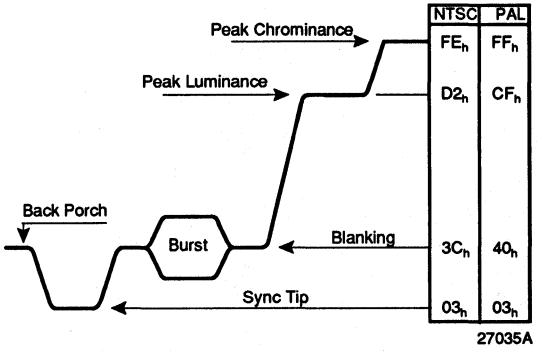


Table 3. TMC22071 Timing Options

Standard	Field Rate (Hz)	Line Rate (kHz)	Pixel Rate (Mpps)	PXCK Frequency (MHz)	Pixels Per Line
NTSC	59.94	15.734264	12.2727+	24.54+	780
NTSC-601	59.94	15.734264	13.50	27.0	858
PAL_A	50.00	15.625	14.75	29.5	944
PAL_B	50.00	15.625	15.00	30.0	960
PAL-601	50.00	15.625	13.50	27.0	864

Table 4. Control Register Example Data

Standard	Control Register Data (Bit 56 ..... Bit 0) 46	42	38	34	30	26	22	18	14	10	6	2
DEFAULT	0000	0110	0000	1001	0000	0010	0000	0000	0000	0000	0000	001
NTSC	0000	0110	0000	1001	0000	0010	0000	0000	0000	00xx	0000	000
NTSC-601	0000	0110	0000	1001	0000	0010	0000	0000	0000	00xx	0000	010
PAL_A	0000	0110	0000	1001	0000	0010	0000	0000	0000	00xx	0000	100
PAL_B	0000	0110	0000	1001	0000	0010	0000	0000	0000	00xx	0000	110
PAL-601	0000	0110	0000	1001	0000	0010	0000	0000	0000	00xx	0001	000

CVBS Bus Data Formats

The CVBS bus outputs a Genlock Reference Signal (GRS) along with the 8-bit digital composite video data. The range of output data versus versus video input voltage is illustrated in Figure 9 where sync tip and blanking levels are controlled by the digital back-porch clamp of the TMC22071. During horizontal sync, the TMC22071 outputs field identification, subcarrier frequency, and subcarrier phase information on the CVBS bus.

Field identification is output on $CVBS_{2-0}$. The LSB, $CVBS_0$, will be LOW during odd fields and HIGH for even fields. When NTSC operation is selected, $CVBS_{1-0}$ count 00,01,10,11 for fields 1 through 4 respectively. When PAL operation is selected, $CVBS_{2-0}$ count 000,001,010, etc. to 111 for fields 1 through 8, respectively.

Subcarrier frequency is sent out in a 24-bit binary representation in six 4-bit nibbles on $CVBS_{3-0}$. Subcarrier frequency data, f_{23-0}, is identical to the pre-programmed BSEED value used in the TMC22071 to lock the subcarrier phase-locked loop to the incoming subcarrier frequency.

Subcarrier phase, Φ_{23-0}, is also sent out in a 24-bit binary representation in six 4-bit nibbles on $CVBS_{3-0}$. Bit Φ_{23} is the MSB.

Figure 10. Genlock Reference Signal (GRS) Format.

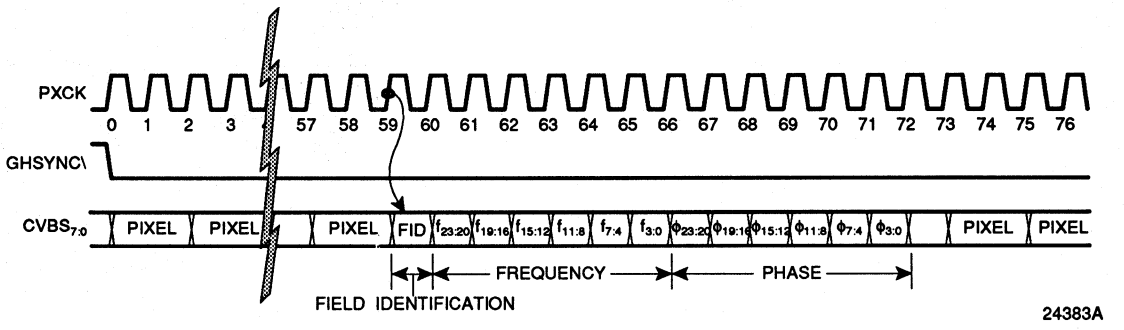


Figure 11. CVBS Bus Video Data Format

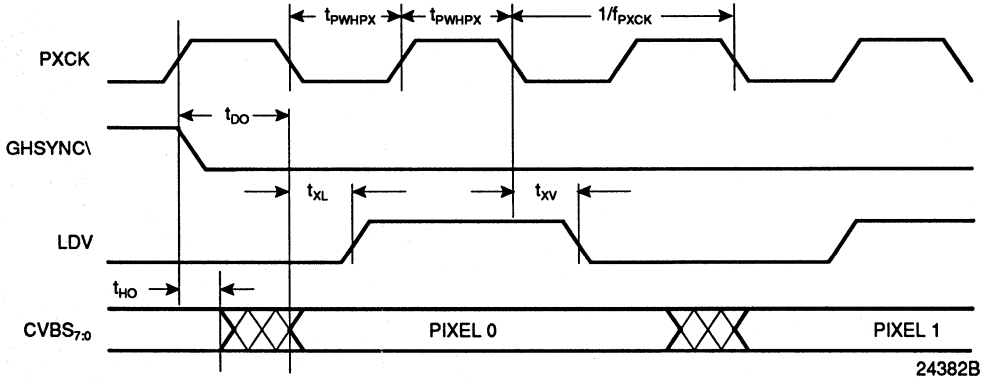


Figure 12. Microprocessor Port - Write Timing

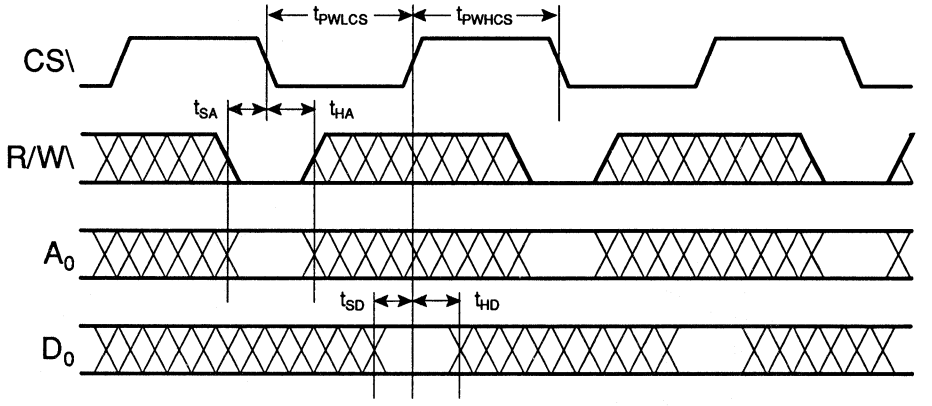


Figure 13. Microprocessor Port - Read Timing

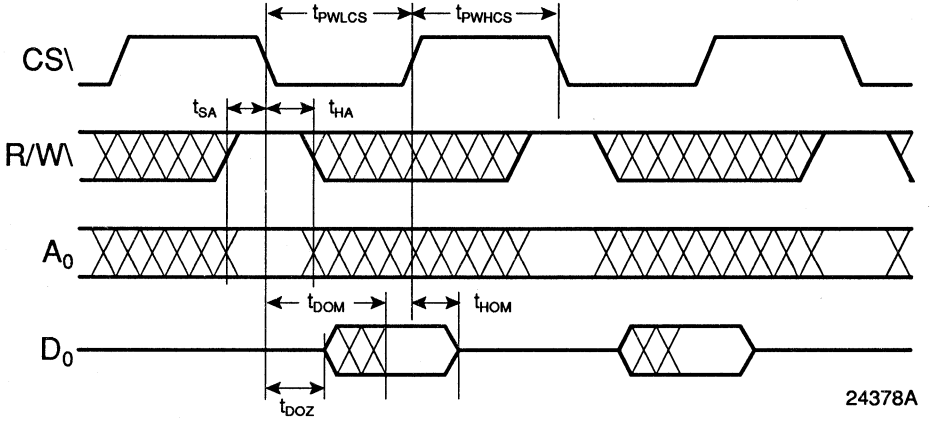


Figure 14. Equivalent PFD IN Circuit

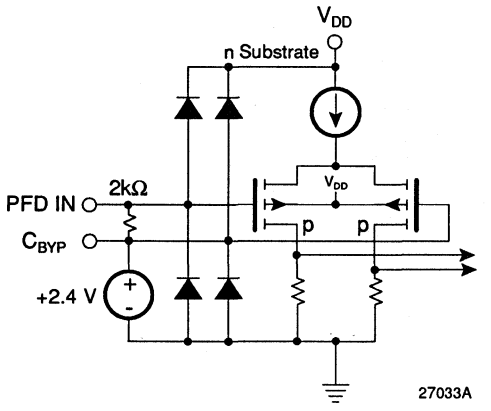


Figure 16. Equivalent DDS OUT Circuit

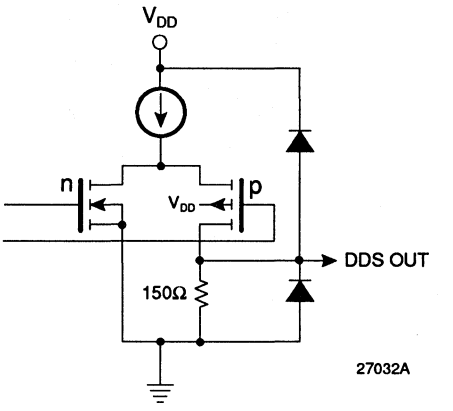


Figure 15. Equivalent Digital Input Circuit

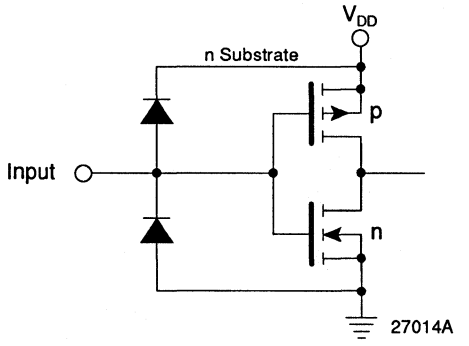


Figure 17. Equivalent Digital Output Circuit

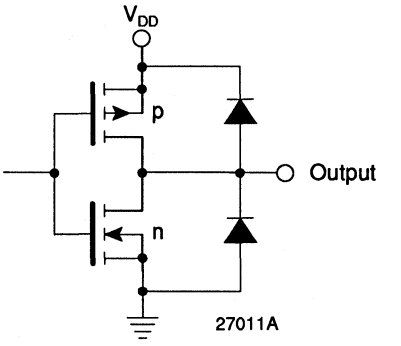
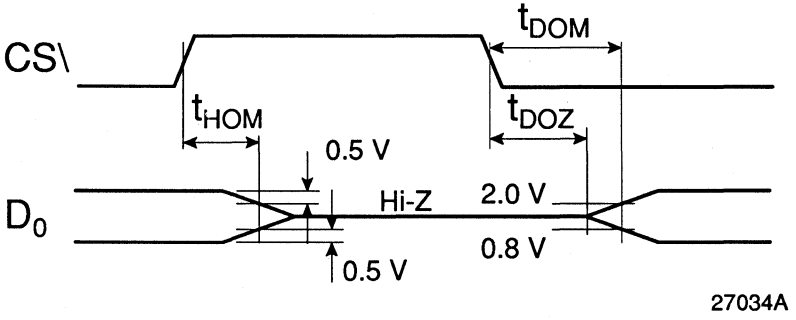


Figure 18. Transition Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged)[1]

Power Supply Voltage ..... -0.5 to +7.0V

Input Voltage ..... -0.5 to V_{DD}+0.5V

Digital Outputs
- Applied Voltage[2] ..... -0.5 to V_{DD}+0.5V
- Forced Current[3,4] ..... -6.0 to 6.0 mA
- Short Circuit Duration
  (Single output in HIGH state to GND) ..... 1 second

Temperature
- Operating, case ..... -60 to +130°C
- Operating, Junction ..... +150°C
- Lead, soldering (10 seconds) ..... +300°C
- Vapor phase soldering (1 minute) ..... +220°C
- Storage ..... -65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Nom	Max	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Inputs	2.0		V_{DD}	V
	CMOS Inputs	2/3 V_{DD}		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				
	TTL Inputs	D_{GND}		0.8	V
	CMOS Inputs	D_{GND}		1/3 V_{DD}	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
V_{IN}	Video Input Signal Level Sync Tip to Peak White		1.0		V
V_{REF}	External Reference Voltage		1.235		V
T_A	Ambient Temperature, Still Air	0		70	°C
Microprocessor Interface					
t_{PWLCS}	CS\ Pulse Width, LOW	35			ns
t_{PWHCS}	CS\ Pulse Width, HIGH	35			ns
t_{SA}	Address Setup Time	4			ns
t_{HA}	Address Hold Time	25			ns
t_{SD}	Data Setup Time	80			ns
t_{HD}	Data Hold Time	2			ns

Note: 1. Timing reference points are at the 50% level.

Electrical Characteristics

Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
I_{DD}	Power Supply Current[1]	Total Current V_{DD}=Max,f_{PXCK}=30MHz		TBD	TBD	mA
I_{REF}	Reference Input Current	V_{REF} = +1.235V			100	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = 4.0V			±10	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0.4V			±10	µA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = -2.0 mA	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = 4.0 mA			0.4	V
I_{OZH}	Hi-Z Output Leakage current, HIGH	V_{DD}=Max, V_{IN}=V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage current, LOW	V_{DD}=Max, V_{IN}=GND			±10	µA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		4	15	pF
C_O	Digital Output Capacitance	T_A = 25°C, f = 1MHz		10		pF
C_V	Input Capacitance, V_{IN1-3}	T_A = 25°C, f = 3.58 MHz			15	pF
R_V	Input Resistance, V_{IN1-3}		50			kΩ

Note 1. Typical I_{DD} with V_{DD}=+5.0 Volts and T_A=25°C, Maximum I_{DD} with V_{DD}=+5.25 Volts and T_A=0°C,

Switching Characteristics

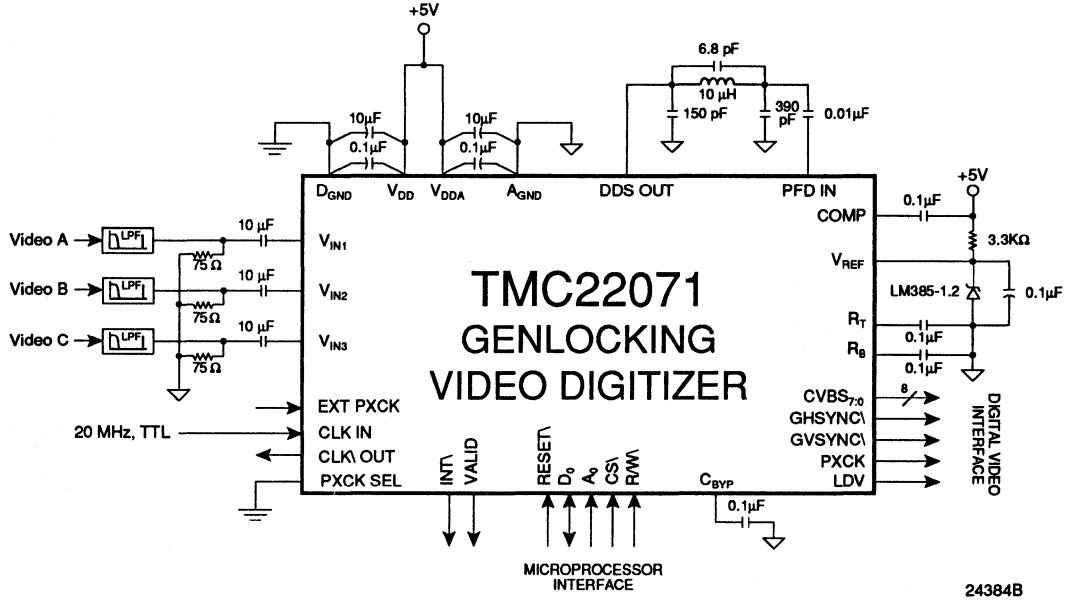
Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 35 pF	2		15	ns
t_{HO}	Output Hold Time		3		8	ns
f_{PCK}	Pixel Rate		12		15.3	MHz
f_{PXCK}	Master Clock Rate		24		30.6	MHz
t_{PWLPX}	PXCK Pulse Width, LOW		12			ns
t_{PWHPX}	PXCK Pulse Width, HIGH		12			ns
t_{DH}	Horizontal Sync to GHSYNC\			4.5		pixels
t_{VD}	Vertical Sync to GVSYNC\			4.5		pixels
t_{XL}	PXCK LOW to LDV HIGH					ns
t_{XV}	PXCK LOW to LDV LOW					ns
t_{DOM}	D_0 enable time					ns
t_{HOM}	D_0 disable time					ns
t_{DOZ}	CS\ LOW to D_0 output driven					ns

System Performance Characteristics

Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
E_{SCH}	Sync time-base variation[1]				±30	ns
E_{SCP}	Subcarrier Phase Error[1]				±5	degrees
t_{AL}	Line-lock Acquisition Time				2	frames
V_{XT}	Channel-to-Channel Crosstalk @3.58 MHz				-35	dB

Notes 1. NTSC/PAL compliant black burst at nominal input level ±10%, frequencies nominal ± 10 ppm.

Figure 19. Typical Interface Circuit



Application Notes

The TMC22071 is a complex mixed-signal VLSI circuit. It produces CMOS digital signals at clock rates of up to 15 MHz while processing analog video inputs with a resolution of less than a few millivolts. To maximize performance it is important to provide an electrically quiet operating environment. The circuit shown in Figure 19 provides an optional external 1.2V reference to the V_{REF} input of the TMC22071. The internal V_{REF} source is adequate for most applications.

Filtering

Inexpensive low-pass anti-aliasing filters are shown in Figures 20 and 20. These filters would normally be inserted in the video signal path just before the 75Ω terminating resistor and AC-coupling capacitor for each of the three video inputs, V_{IN1-3}. The filter of Figure 20 exhibits a 5th-order Chebyshev response with -3dB bandwidth of 6.7MHz and a group delay of 140 nanoseconds at 5MHz. The filter of Figure 21 has been equalized for group delay in the video signal band. Its -3dB passband is 5.5MHz while the group delay is constant at 220 nanoseconds through the DC to 5MHz frequency band.

Figure 20. Simple Anti-aliasing Filter

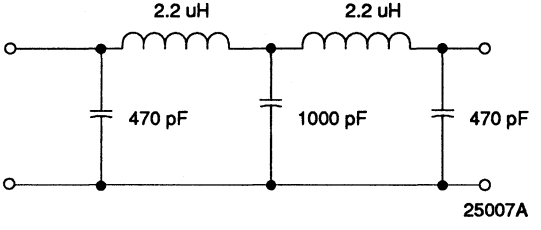
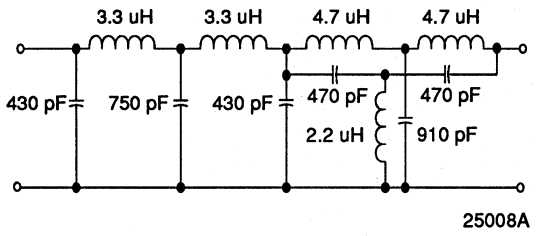


Figure 21. Group Delay Equalized Filter



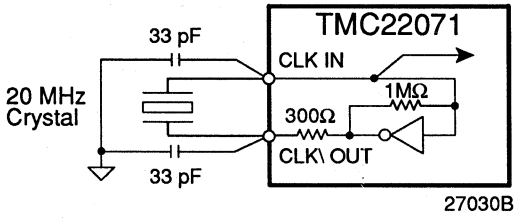
Using a 20 MHz Crystal

In systems where a 20 MHz clock is not available, a crystal may be used to generate the clock to the TMC22071. The crystal must be a 20 MHz "fundamental" type, not overtone." Specific crystal characteristics are listed in Table 5 and the connections are shown in Figure 22.

Table 5. Crystal Parameters

Parameter	Value
Fundamental frequency	20 MHz
Tolerance	±30 ppm @ 25°C
Stability	±50 ppm, 0°C to 70°C
Load Capacitance	20 pF
Shunt Capacitance	7 pF Max.
ESR	50Ω, Max.

Figure 22. Direct Crystal Connections



Grounding

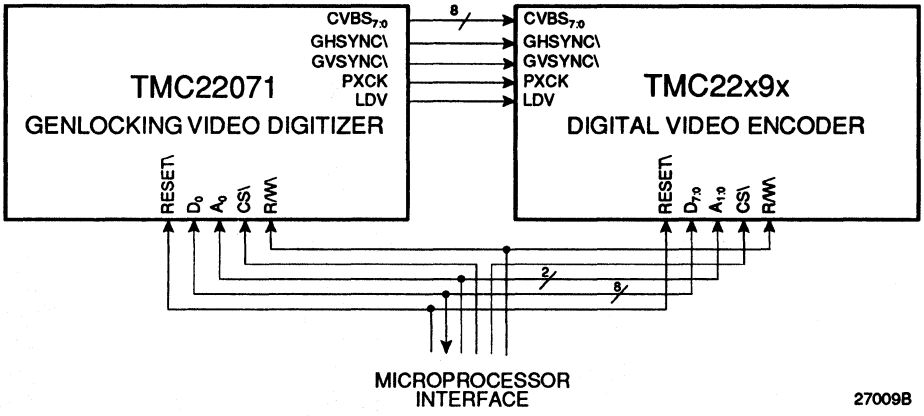
The TMC22071 has separate analog and digital circuits. To minimize digital crosstalk into the analog signals, the power supplies and ground connections are provided over separate pins (V_{DD} and V_{DDA} are digital and analog power supply pins; D_{GND} and A_{GND} are digital and analog ground pins). In general, the best results are obtained by tying all grounds to a solid, low-impedance ground plane. Power supply pins should be individually decoupled at the pin. Power supply noise isolation may be provided between analog and digital supplies via a ferrite bead inductor. Ultimately all +5 Volt power to the TMC22071 should come from the same power source.

Another approach calls for separating analog and digital ground. While some systems may benefit from this strategy, analog and digital grounds must be kept within 0.1V of each other at all times.

Interface to the TMC22x9x Encoder

The TMC22x9x Digital Video Encoders have been designed to directly interface to the TMC22071 Digital Video Genlock. The TMC22071 is the source for TMC22x9x input signals $CVBS_{7-0}$, GHSYNC\, GVSYNC\, LDV, and PXCK as shown in Figure 23. These signals directly connect to the TMC22x9x. The microprocessor interface for TMC22x9x and TMC22071 are identical. All W/R\, RESET\, data and address bus signals from the host microprocessor are shared by the TMC22x9x and TMC22071. Only CS\, VALID, and INT\ signals are separate from the microprocessor bus.

Figure 23. TMC22x9x Interface Circuit



Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor picture quality. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (COMP, V_{REF}, R_T, R_B, DDS OUT, PFD IN, C_{BYP}, and V_{IN1-3}) as short as possible and as far as possible from all digital signals. The TMC22071 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC22071 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC22071 is the same as that of the system's digital circuitry, power to the TMC22071 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

3. the ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

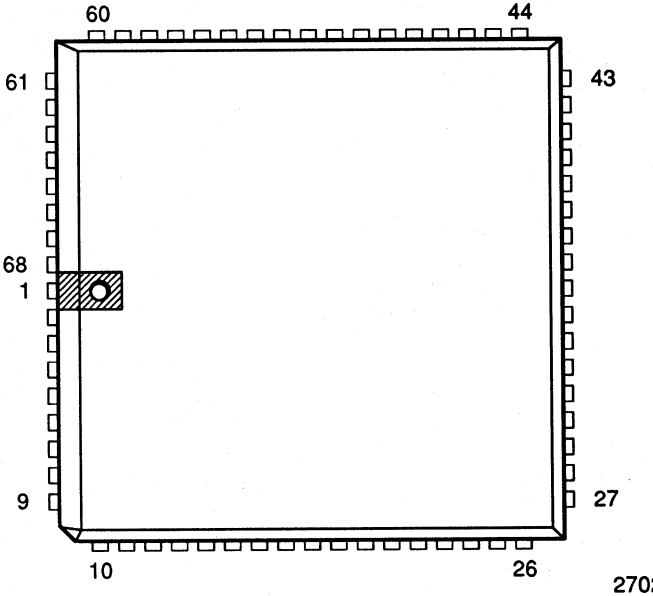
4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They typically supply adjacent circuitry on the device, which generate varying amounts of noise. For best results, use 0.1µF capacitors in parallel with 0.01µF capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC22071, the voltage reference or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC22071 and its related analog circuitry can have an adverse effect on performance.

6. CLK should be handled carefully. Jitter and noise on this clock or its ground reference may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	18	V_{DD}	35	A_{GND}	52	V_{DD}
2	$CVBS_0$	19	PXCK	36	R_T	53	CLK\ OUT
3	$CVBS_1$	20	D_{GND}	37	A_{GND}	54	EXT PXCK
4	$CVBS_2$	21	D_{GND}	38	V_{REF}	55	D_{GND}
5	$CVBS_3$	22	V_{DD}	39	A_{GND}	56	D_{GND}
6	$CVBS_4$	23	V_{DDA}	40	V_{DDA}	57	D_{GND}
7	V_{DD}	24	A_{GND}	41	A_{GND}	58	V_{DD}
8	D_{GND}	25	V_{DDA}	42	C_{BYP}	59	V_{DD}
9	$CVBS_5$	26	V_{DDA}	43	PFD IN	60	A_0
10	$CVBS_6$	27	A_{GND}	44	A_{GND}	61	R/W\
11	$CVBS_7$	28	R_B	45	DDS OUT	62	CS\
12	GHSYNC\	29	V_{IN3}	46	PXCK SEL	63	V_{DD}
13	GVSYNC\	30	V_{DDA}	47	V_{DDA}	64	RESET\
14	VALID	31	V_{IN2}	48	COMP	65	D_{GND}
15	D_{GND}	32	A_{GND}	49	A_{GND}	66	D_0
16	D_{GND}	33	V_{DDA}	50	D_{GND}	67	INT\
17	LDV	34	V_{IN1}	51	CLK IN	68	D_{GND}



27023A

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC22071R1C	T_A = 0°C to 70°C	Commercial	68-Lead PLCC	22071R1C

40GO7281 Rev E 8/93

TMC22090/22091
TMC22190/22191
Digital Video Encoders / Layering Engine

The TMC22X9X digital video encoders convert digital computer image or graphics data (in RGB, YC_BC_R, or color indexed format or a CCIR-601 signal into a standard analog baseband television (NTSC or PAL) signal with a modulated color subcarrier. PAL-M and NTSC without pedestal are also available from the TMC22091/191.

Both composite (single lead) and S-VIDEO (separate chroma and luma) formats are active simultaneously at the three analog output pins, each of which generates a standard video-level signal into doubly-terminated 75Ω load.

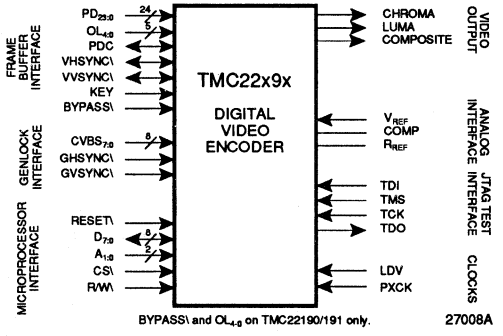
The TMC22X9X accepts digitized video from the companion TMC22070 Genlocking Video Digitizer. Soft switching between video sources is done under either hardware or programmable data level control.

The TMC22190/191 offers a 4-layer keying capability, bypassable CLUTs, and 30 overlay colors.

The TMC22X9X is fabricated in a submicron CMOS process and packaged in 84-lead PLCCs. Performance is guaranteed from 0°C to 70°C.

Features

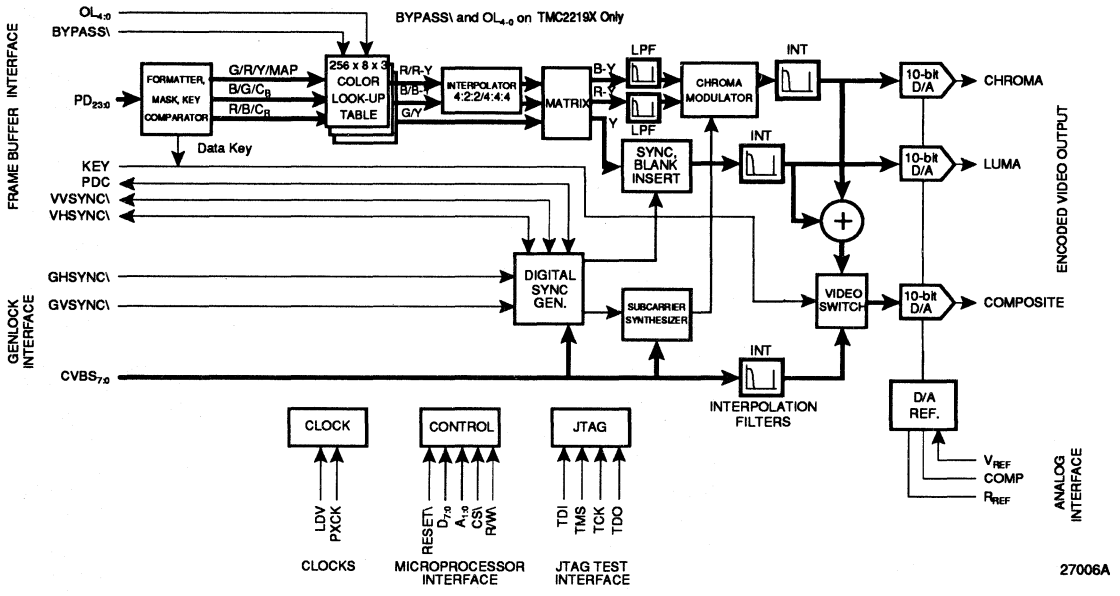
- All digital video encoding
- Internal digital oscillators, no crystals required
- Multiple input formats supported
  - Input formats supported
  - 24-bit and 15-bit GBR/RGB
  - YC_BC_R422 or 444
  - Color indexed
- 30 overlay colors (TMC22190/191)
- Fully programmable timing
- Supports input pixel rates of 10 to 15 Mpps
- 256 x 8 x 3 color look-up tables (bypassable on TMC22190/191)
- 8-bit mask register
- 8-bit composite digital video input
- Hardware and 24-bit data keying
- Synchronizes with TMC22070 genlocking video digitizer
- 8:8:8 video reconstruction
- SMPTE 170M NTSC or CCIR report 624 PAL compatible
- TMC22091/191 also supports PAL-M and NTSC without pedestal
- Simultaneous S-VIDEO (Y/C) NTSC/PAL output
- 10-bit D/A conversion (three channels)
- Controlled edge rates
- 3 power-down modes
- Built-in color bars and modulated ramp test signals
- JTAG (IEEE Std 1149.1-1990) test interface
- Single +5V power supply
- 84-lead PLCC package



Logic Symbol

Contents

Functional Block Diagram



General Description

The TMC22090/091/190/191 are totally-integrated fully-programmable digital video encoders with simultaneous composite and Y/C (S-VIDEO) outputs. The TMC22x9x video outputs are compatible with SMPTE 170M NTSC, CCIR Report 624 PAL, PAL-M, and NTSC without pedestal television standards. No external component selection or tuning is required.

The encoders accept digital image data at the PD port in one of several formats, which are matrixed into luminance and chrominance components. The chrominance signals are modulated onto a digitally synthesized subcarrier. The luminance and chrominance signals are separately interpolated to twice the pixel rate, and converted to analog levels by 10-bit D/A converters. They are also digitally combined and the resulting composite signal is output by a third 10-bit D/A converter. This composite signal may be keyed (pixel rate switching) with a second composite digital video signal presented to the encoder.

The output video frames may be internally timed by the TMC22x9x, synchronized with the external frame buffer, or slaved to the companion Genlocking Video Digitizer (TMC22070). All operational parameters are fully programmable over a standard microprocessor port.

Table 1 shows the key features that distinguish the members of the TMC22x9x family. All of the information presented in this data sheet applies to all of the TMC22x9x unless otherwise noted. Statements, paragraphs, tables, and figures that apply to only one or two of the encoders will have notation specifying the applicable part number.

Timing

The encoder operates from a single clock at twice the system pixel rate. This frequency may be set between 20 MHz and 30 MHz (pixel rates of 10 Mpps to 15 Mpps). Within this range are included CCIR-601, D2 NTSC, and square-pixel formats, as

Multimedia

Table 1. Comparing the TMC22x9x Encoders

Feature	22090	22091	22190	22191
OL_{4-0} pixel inputs for 30 overlay colors	No	No	Yes	Yes
Number of video layers supported	2	2	4	4
BYPASS\ input for bypassing CLUTs	No	No	Yes	Yes
Composite digital video from D_{7-0}	Yes	Yes	Yes	Yes
Luminance data from D_{7-0}	No	Yes	No	Yes
Luminance I/O processing	No	Yes	No	Yes
Extended EH and SL intervals	No	Yes	No	Yes
User-controllable SETUP	No	Yes	No	Yes
Individual D/A power-down mode	No	Yes	No	Yes
NTSC without SETUP	No	Yes	No	Yes
PAL-M	No	Yes	No	Yes

well as a variety of computer-specific pixel rates. An array of programmable timing registers allows the software selection of all pertinent signal parameters to produce NTSC (with or without 7.5 IRE pedestal) and PAL, and PAL-M outputs.

Input Formatting

The input section accepts a variety of video and graphics formats, including 24-bit GBR and RGB, 15-bit GBR and RGB, YC_BC_R422, YC_BC_R444, and 8-bit color-indexed data (Figure 1a and 1b).

The input section of the TMC22x9x includes a key comparator which monitors the pixel data port with three independent 8-bit comparators, and invokes a video key when the selected registers match the incoming data.

Mask Register

A Mask Register is provided which is logically ANDed with incoming color-index data to facilitate pixel animation and other special graphics effects. The Mask Register is ahead of the Data Key comparators and is enabled only when color-index input is selected. Mask Register programming and operation are similar to that of the 171/176 family of graphics RAMDACS.

Color Lookup Table

The Color Lookup Table (CLUT) is a 256 x 8 x 3 random-access memory, and provides means for offset, gain, gamma, and color correction in RGB and YC_BC_R operating modes. It provides a full 24-bit color lookup function for color-index mode and can be loaded in the same manner, with the same data, as a standard VGA RAMDAC.

ColorSpace Conversion Matrix and Interpolator

The matrix converts RGB data (whether from RGB inputs or color-indexed CLUT data) into Y, B-Y, R-Y format for encoding. In input configurations where the pixel input is already in Y, B-Y, R-Y format, the matrix is bypassed. When pixel data is input in YC_BC_R422 format, the interpolation filters produce YC_BC_R444 for encoding.

Sync Generator

The TMC22x9x can operate in Master, Genlock, or Slave modes. In Master and Genlock modes, the encoder internally generates all timing and sync signals, and provides Horizontal Sync, Vertical Sync, and Pixel Data Control (PDC) to the external frame buffer circuitry. PDC is independently selectable to function as an input or an output. In Genlock mode, the TMC22x9x timing is controlled by the TMC22070 Genlocking Video Digitizer over the $CVBS_{7-0}$ bus, GVSYNC\, and GHSYNC\. The

Figure 1a. Pixel Data Format

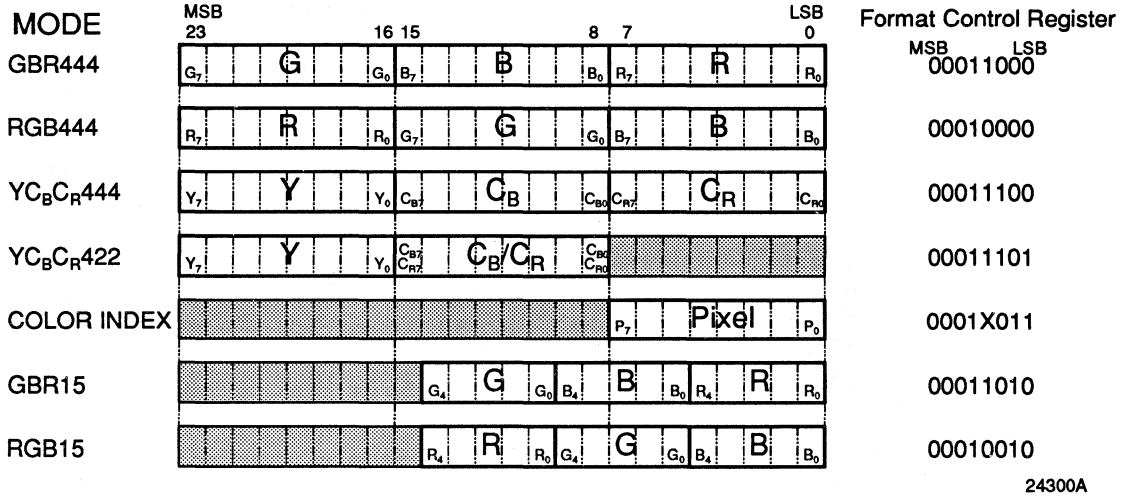
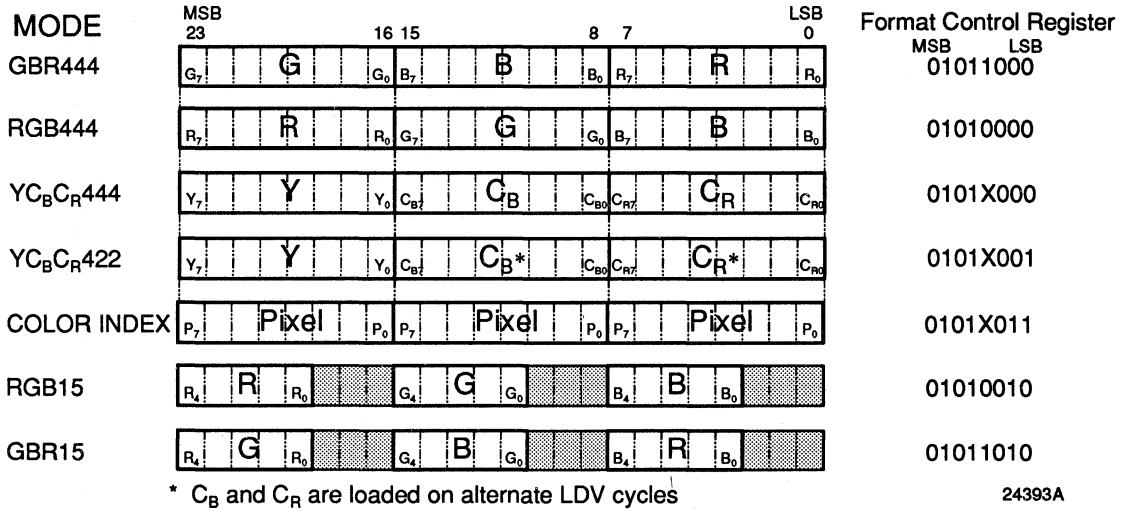


Figure 1b. Pixel Data Format (TMC22190/191 when CLUTs are Bypassed)



encoder, in turn, produces VHSYNC\, VVSYNC\, and PDC for the frame buffer interface.

In Slave mode, VHSYNC\, VVSYNC\, and PDC (optional) are inputs to the TMC22x9x, and determine when new lines, frames, and active picture areas begin. It becomes the responsibility of the external controlling circuitry to establish the correct timing for these signals.

Horizontal and vertical synchronization signals are digitally generated by the TMC22x9x with controlled rise and fall times on all sync edges, the beginning and end of active video, and the burst envelope. All elements of horizontal sync timing are programmable, as are the frequency, phase, and duration of color burst.

Video Input

The TMC22x9x accepts genlocked synchronization data and digital composite video signals from the TMC22070 Genlocking Video Digitizer over the 8-bit CVBS bus. The encoder synchronizes its digital subcarrier oscillator to the video input from the TMC22070 with this data. The composite video data output from the TMC22070 is passed on to the internal video switch for keying with the encoded pixel data.

Chroma Modulator

A 32-bit digital subcarrier synthesizer feeds a quadrature modulator, producing a digital chrominance signal. The relative phases of the burst and active video portions of the subcarrier can be individually adjusted to compensate for external phase errors and to effect a hue control.

Interpolation Filters

Interpolation filters on the luminance and chrominance signals double the pixel rate in preparation for D/A conversion. This band-limited process greatly simplifies the output filtering required following the D/A converters and dramatically reduces sin(x)/x distortion.

An interpolation filter on the CVBS data similarly raises the sample rate of the video signal, for mixing with the encoded pixel data.

Composite Video Switch

The Composite Video Switch selects between the composite video input (CVBS) and the composite encoded pixel data on a pixel-by-pixel basis, under the control of a key function.

Keying may be managed by hardware or software. The hardware key input (KEY pin) directly controls the video switch. The encoder may be programmed to operate with a data key, represented by three 8-bit registers that compare with the 24 input bits. They operate in all input modes and may be individually enabled or disabled.

D/A Converters

The analog outputs of the TMC22x9x are the outputs of three 10-bit D/A converters, operating at twice the pixel clock rate. The outputs are capable of driving standard video levels into a doubly-terminated 75Ω coaxial video cable (37.5Ω total load). An internal voltage reference is provided which can be used to provide reference current for the three D/A converters. For accurate video levels, an external fixed or variable voltage reference source is recommended. The video signal levels from the TMC22x9x may be adjusted to overcome the insertion loss of analog low-pass output filters.

The D/A converters on the TMC22091/191 may be powered-down via Control Register 0E bits 5 and 6. The COMPOSITE D/A is controlled by bit 6 and the LUMA and CHROMA D/A converters are controlled by bit 5.

Microprocessor Interface

The microprocessor interface employs a 13 line format. The RESET\ pin sets all internal state machines to their initialized conditions, disables the analog outputs, sets the internal SRESET\ bit LOW (reset condition), and places the encoder in a power-down mode. All register and CLUT data are

maintained while in power-down mode. Returning the RESET\ pin HIGH synchronizes the internal pixel clock. If the HRESET bit is set HIGH, line 1 field 1 is started when RESET\ goes HIGH, and SRESET\ is ignored. If HRESET is LOW, the encoder remains idle after RESET\ goes HIGH until Control Register bit SRESET\ is set HIGH, which initiates line 1 field 1.

Two address lines are provided and decoded for access to the internal control registers, and CLUT. Controls and CLUT are reached by loading a desired address through the 8-bit D_{7-0} port, followed by the desired data (read or write) for that address. Both the CLUT and the control registers are self-indexing, allowing continuous reads or writes to successive addresses.

JTAG Test Interface

The TMC22x9x includes a standard 4-line JTAG (IEEE Std 1149.1-1990) test interface port, providing access to all digital input/output data pins. This is provided to facilitate component and board-level testing.

Test/Validation Mode

The TMC22x9x may be configured to produce standard color bars or a 40 IRE modulated (or unmodulated) video ramp, independent of any pixel or video data input. Color bars are useful as an idle system output signal. The test signals may be employed to verify proper operation of the analog video signal chain.

Pin Functions

The pins may be divided into nine categories:

1. Clocks
2. Frame Buffer Interface
3. Genlock Interface
4. Microprocessor Interface
5. Video Outputs
6. Analog Interface
7. JTAG Test Interface
8. Power and Ground
9. Factory test (22090/091)

Clocks

PXCK — This 20 to 30 MHz clock is internally divided by 2 to generate the internal pixel clock, PCK, which a LOW on RESET\ forces LOW. PXCK drives the entire TMC22x9x, except the asynchronous microprocessor interface and the semi-synchronous LDV data input clock. All internal registers are strobed on the rising edge of PXCK.

LDV — On each rising edge of LDV, data on PD_{23-0} are latched into the input preload register, for transfer into the input demultiplexer on the next rising edge of PCK.

Frame Buffer Interface

PD_{23-0} — In YC_BC_R, GBR, RGB, and color-indexed pixel data enter the TMC22x9x on PD_{23-0}. The specific format is found in Figures 1a and 1b. LDV is the clock that controls the loading of pixel data.

VHSYNC\ — In Master and Genlock modes, the TMC22x9x outputs horizontal sync on this pin. In Slave modes, the TMC22x9x accepts and locks to horizontal sync input on this pin (with vertical sync on VVSYNC\). VHSYNC\ and VVSYNC\ must be coincident such that they are clocked into the TMC22x9x on the same rising edge of PXCK.

VVSYNC\ — In two-line (separate V and H sync signals) Master and Genlock modes, the TMC22x9x outputs vertical block sync (VVSYNC\ LOW for the 2.5 (PAL) or 3 (NTSC) lines on which vertical sync pulses occur). In composite sync (H and V sync on same signal) Master and Genlock modes, the TMC22x9x outputs horizontal sync, vertical sync, and equalization over this pin. In Slave mode, the TMC22x9x accepts and locks to vertical sync input on this pin (with horizontal sync on VHSYNC\).

VHSYNC\ and VVSYNC\ must be coincident such that they are clocked into the TMC22x9x on the same rising edge of PXCK.

PDC — In Master mode, the TMC22x9x forces PDC HIGH when and only when it wants active video from the frame buffer. During blanking (syncs, equalization, burst, and porches), it forces PDC LOW, signalling that it will ignore any data presented over PD_{23-0}. When PDC is used as an input, forcing it HIGH puts the TMC22x9x into the active video state. Forcing PDC LOW leaves blank and burst unaffected, but forces the TMC22x9x to output black burst.

KEY — When the HKEN control bit is set HIGH and hardware key pin, KEY, is HIGH, video data entering on $CVBS_{7-0}$ are routed to the COMPOSITE output. This control signal is pipelined so the pixel that is presented to the PD port when the KEY signal is invoked is at the midpoint of the soft key transition. When HKEN is LOW, KEY is ignored. Like PD data, KEY is clocked into the TMC22x9x on the rising edge of LDV.

OL_{4-0} (22190) (22190) — 30 of the 256 locations of the CLUTs may be reserved for overlay operation. These CLUT locations are directly accessed by five input pins, OL_{4-0}. OL_{4-0} are entered into the TMC22190 on a pixel-by-pixel basis and select which of the 30 overlay colors is to be encoded. When all five OL_{4-0} inputs are LOW, no overlay occurs.

BYPASS\ (22190) (22191) — When BYPASS\ is HIGH, the CLUTs are in the pixel data path within the TMC22190/191. When BYPASS\ is LOW, pixel data bypasses the CLUTs. BYPASS\ is active only for certain modes of the Layering Control Register (LCR) when the Format Control Register bit 6 is HIGH.

Genlock Interface

GHSYNC\ — In Genlock mode, the TMC22x9x will start a new horizontal line (blank-to-sync-edge transition) with each falling edge of GHSYNC\. In non-genlock modes, the TMC22x9x ignores GHSYNC\. The internal pixel clock, PCK, is aligned with the falling edge of VHSYNC\ or GHSYNC\ (Genlock mode).

GVSYNC\ — In Genlock mode, the TMC22x9x will start a new vertical sync sequence at line 1 field 1 whenever GVSYNC\ and GHSYNC\ are coincident such that they are clocked into the TMC22x9x on the same rising edge of PXCK. If GVSYNC\ falls at any other time, the TMC22x9x will assume that this marks the start of field 2, and will ignore it (in odd-field sync mode) or (in all-field sync mode) respond by generating a single vertical sync pulse, followed by 2 (PAL) or 2.5 (NTSC) lines of vertical sync, keyed to the next falling edge on GHSYNC\. See Interface Control Register bit 0 for odd-field and all-field operation.

$CVBS_{7-0}$ — The encoder receives digitized video, subcarrier phase, and subcarrier frequency over this 8-bit bus at the PCK rate. This data may be provided by the companion TMC22070 Genlocking Video Digitizer. In Genlock mode, the TMC22x9x expects subcarrier phase and frequency data during each line's horizontal sync interval, as well as video data when keying is engaged, transferred at the PCK rate.

Microprocessor Interface

D_{7-0} — All control parameters are loaded into and read back over this 8-bit port. For digital testing, the five lower bits can also serve as a two-cycle 10-bit data output port. For D/A converter testing,

it can be used as a 10-bit two-cycle input port, facilitating, for example, ramp-based D/A converter linearity tests.

A_{1-0} As in a RAMDAC, this control governs whether the microprocessor interface selects a table address or reads/writes table contents. It also governs setting and verification of the TMC22x9x's internal operating modes, also over port D_{7-0}.

CS\ When CS\ is HIGH, the microprocessor interface port, D_{7-0}, is set to HIGH impedance and ignored. When CS\ is LOW, the microprocessor can read or write parameters over D_{7-0}. One additional falling edge of CS\ is needed to move input data to its assigned working registers.

R/W\ When R/W\ and CS\ are LOW, the microprocessor can write to the control registers or CLUT over D_{7-0}. When R/W\ is HIGH and CS\ is LOW, it can read the contents of any CLUT address or control register over D_{7-0}.

RESET\ Bringing RESET\ LOW sets the software reset control bit, SRESET\, LOW, forcing the internal state machines to their starting states and disabling all outputs. Bringing RESET\ HIGH synchronizes the internal pixel clock (PCK = PXCK / 2) to maintain a defined pipeline delay through the TMC22x9x. If HRESET is set HIGH, the encoder is enabled when RESET\ goes HIGH. If HRESET is LOW, the host restarts the TMC22x9x by setting SRESET\ HIGH. RESET\ does not affect the CLUT or the control registers, except SRESET\.

Video Output

COMPOSITE Analog output of composite D/A converter, nominally 1.35 volt peak-to-peak into a 37.5Ω load.

LUMA Analog output of luminance D/A converter, nominally 1.35 volt peak-to-peak into a 37.5Ω load.

CHROMA Analog output of chrominance D/A converter, nominally 1.35 volt peak-to-peak into a 37.5Ω load.

Analog Interface

V_{REF} External voltage reference input, internal voltage reference output, nominally 1.235 V.

COMP Connection point for 0.1uf decoupling capacitor.

R_{REF} Connection point for external current-setting resistor for D/A converters. The resistor (392Ω) is connected between R_{REF} and A_{GND}. Output video levels are inversely proportional to the value of R_{REF}.

JTAG Test Interface

TDI Boundary scan data input port.
TMS Boundary scan (HIGH)/normal operation (LOW) selector.
TCK Boundary scan clock.
TDO Boundary scan data output port.

Power Supply

V_{DD} Positive digital power supply.
V_{DDA} Positive analog power supply.
D_{GND} Digital Ground.
A_{GND} Analog Ground.

Test

TEST (22090) (22091) Reserved for factory testing. These pins have no effect on the operation but do function as JTAG registers. They should be grounded directly or pulled down to ground with 1kΩ or smaller resistors.

Multimedia

Table 2. Package Interconnections

Signal Type	Name	Function	Value	Package Pin
Clocks	PXCK	Master Clock Input	TTL	79
	LDV	Pixel Data Load Clock	TTL	78
Frame Buffer I/O	PD_{23-0}	Pixel Data Inputs	TTL	52-63, 66-77
	VHSYNC\	Horizontal Sync I/O	TTL	12
	VVSYNC\	Vertical Sync I/O	TTL	13
	PDC	Pixel Data Control	TTL	11
	KEY	Hardware Key Input	TTL	4
	OL_{4-0}	Overlay Data Inputs (22190/191)	TTL	29, 48-51
	BYPASS\	CLUT Bypass Control (22190/191)	TTL	28
Genlock I/O	GHSYNC\	Genlock Horizontal Sync	CMOS	83
	GVSYNC\	Genlock Vertical Sync	CMOS	82
	$CVBS_{7-0}$	Composite Video Inputs	TTL	44-47, 84, 1-3
µProc I/O	D_{7-0}	Data I/O Port	TTL	14-21
	A_{1-0}	µProc Port Controls	TTL	8-9
	CS\	Chip Select	TTL	6
	RESET\	Master Reset Input	TTL	5
	R/W\	Bus Read/Write Control	TTL	7
Video Output	COMPOSITE	NTSC/PAL Video	1 V P-P	33
	LUMA	Luminance-only Video	1 V P-P	35
	CHROMA	Chrominance-only Video	1 V P-P	37
Reference	V_{REF}	Voltage Reference Input	+1.23 V	30
	COMP	Compensation Capacitor	0.1 µF	39
	R_{REF}	Current-setting Resistor	392 Ω	31
JTAG I/O	TDI	Data Input Port	TTL	25
	TMS	Scan Select Input	TTL	24
	TCK	Scan Clock Input	TTL	23
	TDO	Data Output Port	TTL	22
Power	V_{DDA}	Analog Power Supply	+5 V	40-43
	V_{DD}	Digital Power Supply	+5 V	27, 64, 81
Ground	A_{GND}	Analog Ground	0.0 V	32, 34, 36, 38
	D_{GND}	Digital Ground	0.0 V	10, 26, 65, 80
Test	TEST	Factory testing (22090/091)	0.0 V	28, 29, 48-51

Control Registers

The TMC22x9x is initialized and controlled by a set of registers which provide a high degree of control over the TMC22x9x's operating parameters. The registers are organized into 13 categories:

1. Global Control
2. Format Control
3. Interface Control
4. Test Control
5. Key Control
6. Misc. Control (22091/191)
7. Standards Control (22091/191)
8. Layering Control (22190/191)
9. Key Value
10. Timing
11. Subcarrier
12. Test I/O
13. Mask Register

An external controller loads the Control Registers through a standard interface port. It also loads the CLUT and verifies (reads) its contents or those of the Control Registers. The port is governed by pins CS\, R/W\, and A_{1-0}.

The Address Register for the CLUT and the Control Register pointer automatically increment to allow successive writes to sequential addresses. In the CLUT, the Address Register has two additional bits which increment in modulo-three to sequentially access the red, green, and blue portions. All three colors must be written when any CLUT address is changed.

The control register autoincrement follows the sequence indicated in the Control Register Map. When it reaches address 40, it stops incrementing, allowing multiple reads or writes of test data from/to the TESTDAT register. To exit the test mode, reset the Control Register pointer by setting A_{1-0}, D_{7-0}, and R/W\ LOW and then bring CS\ LOW. Address 1F is a read-only status register. It is addressed by the autoincrement sequencer. Any data may be written into this port at that time but it will not be stored. When address 50 is accessed, no autoincrement takes place, allowing multiple writes to the Mask Register.

Table 3. Microprocessor Port Control

A_{1-0}	R/W\	Action
00	0	Load D_{7-0} into Control Register pointer.
00	1	Read Control Register pointer on D_{7-0}.
01	0	Load D_{7-0} into CLUT Address Register.
01	1	Read CLUT Address Register on D_{7-0}.
10	0	Write D_{7-0} to addressed Control Register.
10	1	Read addressed Control Register on D_{7-0}.
11	0	Write D_{7-0} to addressed CLUT location.
11	1	Read addressed CLUT location on D_{7-0}.

Table 4. Control Register Map

Reg	Bit	Mnemonic	Function
			Global Control Register
00	7-5		(reserved)
00	4	SRESET\	Software reset
00	3	PAL	Standard select, NTSC or PAL
00	2	LUMDIS	Luminance input disable
00	1	CHRDIS	Chrominance input disable
00	0	HRESET	Software reset disable
			Format Control Register
01	7		(reserved)
01	6	LCREN	Layering Control Register enable (22190/191)
01	5	RAMPEN	Modulated ramp test
01	4	CB\	Color bar test
01	3-2	FORMAT	PD_{23-0} input format select
01	1-0	INMODE	PD_{23-0} input mode select
			Interface Control Register
02	7	VITSEN	VITS lines enable
02	6	SHCY	Short-cycle test mode
02	5-4	TBASE	Time-base source select
02	3	SOUT	Sync output mode select
02	2	FBDIS	Frame buffer signals disable
02	1	PDCDIR	PDC master, slave select
02	0	FLDLK	Field lock select
			Test Control Register
03	7		(reserved)
03	6	LIMEN	Luminance limiter enable
03	5	TESTEN	Test enable
03	4	HOLDEN	MSBs/LSBs hold select
03	3	TSTMSB	LSBs, MSBs in/out select
03	2	LUMTST	LUMA channel test
03	1	8FSUBR	8-field subcarrier reset enable
03	0	CHRTST	CHROMA channel test
			Key Control Register
04	7		(reserved)
04	6	HKEN	Hardware key enable
04	5	BUKEN	Burst key enable
04	4	SKEXT	Data key operation select
04	3	DKDIS	Green/red/Y data key disable
04	2	EKDIS	Blue/green/C_B data key disable
04	1	FKDIS	Red/blue/C_R data key disable
04	0	SKEN	Data key enable
			Layering Control Register (22190/191)
04	7	LAYMODE	MSB of Layer Assignments select
04	6	HKEN	Hardware key enable
04	5	BUKEN	Burst key enable
04	4	SKEXT	Data key operation select
04	3-1	LAYMODE	LSBs of Layer Assignments select
04	0	SKEN	Data key enable
			Key Value Registers
05	7-0	DKEY	Green/red/Y data key value
06	7-0	EKEY	Blue/green/C_B data key value
07	7-0	FKEY	Red/blue/C_R data key value
08-0D			(reserved)
			Misc. Control Register
0E	7	EFEN	Register 0E and 0F enable
0E	6	COMPD/A	COMPOSITE D/A disable
0E	5	SVIDD/A	LUMA/CHROMA D/A disable
0E	4	FKREN	Luminance processing enabled
0E	3	RATIO	Luminance ratio select
0E	2	TFLK	Luminance pass threshold select
0E	1	T512	EH/SL offset select
0E	0	CB100	NTSC/PAL Color Bars
			Standards Control Register
0F	7	EFEN	Same as Reg 0E bit 7 but read-only
0F	6	SIX25	625/525 line per frame select
0F	5	PALID	Phase alternate line select
0F	4	SETUP	7.5 IRE Pedestal Enable
0F	3-2	YGAIN	Luminance gain settings
0F	1-0	CGAIN	Chrominance gain settings
			Timing Registers
10	7-0	SY	Horizontal sync tip length
11	7-0	BR	Breezeway length
12	7-0	BU	Burst length
13	7-0	CBP	Color back porch length
14	7-0	XBP	Extended color back porch 8 LSB
15	7-0	VA	Active video 8 LSB
16	7-0	VC	Active video start 8 LSB
17	7-0	VB	Active video end 8 LSB
18	7-6	XBP	Extended color back porch 2 MSB
18	5-4	VA	Active video 2 MSB
18	3-2	VC	Active video start 2 MSB
18	1-0	VB	Active video end 2 MSB
19	7-0	FP	Front porch length
1A	7-0	EL	Equalization pulse LOW length
1B	7-0	EH	Equalization pulse HIGH length
1C	7-0	SL	Vertical sync LOW length
1D	7-0	SH	Vertical sync HIGH length
1E	7-0	CBL	Color bar length
1F	7-5	FIELD	Field identification
1F	4-0	LTYPE	Line type identification

Notes:
1. Functions are listed in the order used for reading and writing.
2. For each register listed above, all bits not listed are reserved and should be set to zero to ensure proper operation.
3. The meaning of Register 04 (Key Control Register/Layering Control Register) is determined by Format Control Register bit 6 (22190/191)

Table 4. Control Register Map (continued)

Reg	Bit	Mnemonic	Function
			Subcarrier Registers
20	7-0	FREQL	Subcarrier frequency 4th byte (LSBs)
21	7-0	FREQ3	Subcarrier frequency 3rd byte
22	7-0	FREQ2	Subcarrier frequency 2nd byte
23	7-0	FREQM	Subcarrier frequency 1st byte (MSBs)
24	7-0	SYSPHL	Video phase offset LSBs
25	7-0	SYSPHM	Video phase offset MSBs
26	7-0	BURPHL	Burst phase offset LSBs
27	7-0	BURPHM	Burst phase offset MSBs
28-3F			(reserved)
			Test I/O Register
40	7-0	TESTDAT	Test data input/output
			Mask Register
50	7-0	MASK	Mask register
			Y-Component Register
60	7-0	Y	Y-component input/output

Control Register Definitions

Reg	Bit	Mnemonic	Function
			Global Control Register
00	7-5		(reserved)
00	4	SRESET\	Software reset. When LOW, resets and holds internal state machines and disables outputs. When HIGH (normal), starts and runs state machines and enables outputs.
00	3	PAL	Video standard select. When LOW, the NTSC standard is generated with 7.5 IRE pedestal. When HIGH, PAL standard video is generated. In the TMC22091/191, this bit is ignored if Register 0E bit 7 is HIGH, enabling the 0E and 0F registers.
00	2	LUMDIS	Luminance input disable. When LOW (normal), luminance (Y) data from external frame buffer is enabled. When HIGH, luminance (Y) data into the TMC22x9x is forced to 0 IRE but sync pulses continue from the LUMA output.
00	1	CHRDIS	Chrominance input disable. When LOW (normal), burst and frame buffer data into the TMC22x9x are enabled. when HIGH, burst and frame buffer data are suppressed, enabling monochrome operation.
00	0	HRESET	Software reset enable. SRESET is forced LOW when the RESET\ pin is taken LOW. State machines are reset and held. When HRESET is LOW, RESET\ may be taken HIGH at any time. The TMC22x9x is enabled and a new frame is begun with line 1, field 1 on the next PXCK after SRESET is set HIGH. The D/A converters are powered down while RESET\ is LOW. When HRESET is HIGH, a new frame is begun with line 1, field 1 on the next PXCK after RESET\ is taken HIGH. SRESET is ignored. The D/A converters remain active during the reset sequence.
			Format Control Register
01	7		(reserved)
01	6	LCREN (22190) (22191)	Layering Control Register enable. When LOW, the Layering Control Register is not available and Key Control Register functions are enabled. In this mode, the TMC22190/191 functions like the TMC22090/091. When HIGH, the Layering Control Register takes the place of the Key Control Register and enables the layering functions. Data loaded into the Key or Layering Control Registers will remain but have a different meaning if this bit is changed.

Reg	Bit	Mnemonic	Function
01	5	RAMPEN	Modulated ramp test. When LOW (normal), the TMC22x9x encodes and outputs video corresponding to input data. When RAMPEN and CB\ are both HIGH, an internally generated 40 IRE modulated ramp is produced, preempting input data.
01	4	CB\	Color bar test. When HIGH (normal), the TMC22x9x encodes and outputs video corresponding to input data. When CB\, RAMPEN, and Format Control Register bit 0 are LOW, internally generated color bars are produced, preempting input data.
01	3-2	FORMAT	PD_{23-0} input format select. Two bits select RGB, GBR, or YC_BC_R input data. When bits 3 and 2 are: 00, the CLUT output is interpreted as RGB and is converted to YC_BC_R. 10, the CLUT output is interpreted as GBR, and is converted to YC_BC_R. 11, the CLUT output is interpreted as YC_BC_R. 01, is reserved Bits 3 and 2 must be 00 or 10 when the Layering Control Register is enabled (22190/191).
01	1-0	INMODE	PD_{23-0} input mode select. These two bits set up the TMC22x9x for either 444, 422, 15-bit, or 8-bit input modes. 00, 24-bit/pixel GBR, RGB, or YC_BC_R444 data enters from PD_{23-0} 01, YC_BC_R422 data enters from PD_{23-8}; C_R and C_B alternate from PD_{15-8} 10, 15-bit/pixel GBR or RGB data from PD_{14-0} 11, 8-bit/pixel color indexed data enters from PD_{7-0}. Bits 1 and 0 must be 00, 01, or 11 when the Layering Control Register is enabled (22190/191).

Interface Control Register

Reg	Bit	Mnemonic	Function
02	7	VITSEN	VITS lines enable. When LOW, all UBB lines in the vertical interval are black burst regardless of input data. When HIGH, all UBB lines in the vertical interval become UVV active video and are dependent upon input data.
02	6	SHCY	Short-cycle test mode. When LOW, normal operation is enabled. when HIGH, EH (equalization pulse HIGH length) and SL (vertical sync LOW length) are shortened by 256.
02	5-4	TBASE	Time-base source select. These two bits set up the TMC22x9x for either genlock or frame buffer control of timing. When bits 5 and 4 are: 00, the encoder counts out its own time-base from input clock PXCK.

Reg	Bit	Mnemonic	Function
			01, the encoder locks to synchronizing signals from external genlock. 10, the encoder locks to synchronizing signals from frame buffer controller.
02	3	SOUT	Sync output mode select. When LOW, VHSYNC\ and VVSYNC\ output separate horizontal and vertical sync pulses. When HIGH, composite sync (H and V) is output on VVSYNC\ while horizontal sync is output on VHSYNC\.
02	2	FBDIS	Frame buffer signals enable. When LOW, VVSYNC\ and VHSYNC\ outputs to frame buffer are enabled. When HIGH, VVSYNC\ and VHSYNC outputs to frame buffer are disabled.
02	1	PDCDIR	PDC master/slave select. When LOW, PDC is an output where the encoder is requesting data from the frame buffer. When HIGH, PDC is an input, and directs the encoder to accept data from the frame buffer.
02	0	FLDLK	Field lock select. When LOW, (in Slave mode) the encoder locks to each new field. When HIGH, the encoder locks to field 1 only.
			Test Control Register
03	7		(reserved)
03	6	LIMEN	Luminance limiter enable. When LOW, all luminance values are passed to modulator. when HIGH, luminance values are limited to 101 IRE.
03	5	TESTEN	Test enable. When LOW, normal operation is enabled. When HIGH, $TESTDAT_{7-0}$ (Register 40) is connected to the composite output (READ) and D/A converters (WRITE) for test.
03	4	HOLDEN	MSBs/LSBs hold select. When LOW, alternates MSBs and LSBs in test, at PXCK rate. When HIGH, reads/writes only MSBS or LSBS in test (per TSTMSB, bit 3)
03	3	TSTMSB	LSBS,MSBS hold select. When LOW, connects 2 LSBs to $TESTDAT_{1-0}$ for testing when TESTEN is HIGH. When HIGH, connects 8 MSBs to $TESTDAT_{7-0}$ for testing when TESTEN is HIGH.
03	2	LUMTST	LUMA channel test. When LOW (normal), the luminance D/A converter is driven from luminance channel. When HIGH, the luminance D/A converter is driven from TESTDAT for testing when TESTEN is HIGH.
03	1	8FSUBR	8-field subcarrier reset enable. When LOW, the internal subcarrier

Reg	Bit	Mnemonic	Function
			generator is reset with frequency and phase data from FREQ, SYSPH, and BURPH registers every eight fields. When HIGH, the internal subcarrier generator free-runs on the basis of frequency and phase data from the last time it was reset. When RESET\ goes LOW, the subcarrier frequency and phase will be reset from FREQ, SYSPH, and BURPH after field 8.
03	0	CHRTST	CHROMA channel test. When LOW (normal), the chrominance D/A converter is driven from chrominance channel. When HIGH, the chrominance D/A converter is driven from TESTDAT when TESTEN is HIGH.
			Key Control Register
04	7		(reserved)
04	6	HKEN	Hardware key enable. When LOW, the KEY input pin ignored. When HIGH, the KEY input pin is enabled.
04	5	BUKEN	Burst key enable. When LOW, output video burst is generated on TMC22x9x. When HIGH, output burst is taken from genlock input data.
04	4	SKEXT	Data key operation select. When LOW, data keying is allowed only during active video. When HIGH, data keying is allowed during active video and blanking.
04	3	DKDIS	Green/red/Y data key disable. When LOW, green/red/Y input data is enabled for data keying. When HIGH, green/red/Y input data is ignored for data keying. This function is enabled when Layering Control Register is enabled (22190/191).
04	2	EKDIS	Blue/green/C_B data key disable. When LOW, Blue/green/C_B input data is enabled for data keying. When HIGH, Blue/green/C_B input data is ignored for data keying. This function is enabled when Layering Control Register is enabled (22190/191).
04	1	FKDIS	Red/blue/C_R data key disable. When LOW, red/blue/C_R input data is enabled for data keying. When HIGH, red/blue/C_R input data is ignored for data keying. This function is enabled when Layering Control Register is enabled (22190/191).
04	0	SKEN	Data key enable. When LOW, data keying is disabled. When HIGH, data keying is enabled.
			Layering Control Register (22190/191)
04	7	LAYMODE	MSB of Layer Assignments select

Reg	Bit	Mnemonic	Function
04	6	HKEN	Hardware key enable. When LOW, the KEY input pin ignored. When HIGH, the KEY input pin is enabled.
04	5	BUKEN	Burst key enable. When LOW, output video burst is generated on TMC22190/191. When HIGH, output burst is taken from genlock input data.
04	4	SKEXT	Data key operation select. When LOW, data keying is allowed only during active video. When HIGH, data keying is allowed during active video and blanking.
04	3-1	LAYMODE	three LSBs of Layer Assignments select
04	0	SKEN	Data key enable. When LOW, data keying is disabled. When HIGH, data keying is enabled.
			Key Value Registers
05	7-0	DKEY	Green/red/Y data key value. Eight bits hold the match value which triggers keying on red/Y.
06	7-0	EKEY	Blue/green/U data key value. Eight bits hold the match value which triggers keying on green/U.
07	7-0	FKEY	Red/blue/V key value. Eight bits hold the match value which triggers keying on blue/V.

Reg	Bit	Mnemonic	Function
			Misc. Control Register (22091/191)
0E	7	EFEN	Register 0E and 0F enable. When LOW, the functions of Register 0E and 0F are disabled. When HIGH, Registers 0E and 0F are active. When Registers 0E and 0F are enabled, Register 00 bit 3 is ignored. For TMC22091/191, Register 0E bit 7 will read back whatever value was written. For TMC22090/190 Register 0E bit 7 will only read back LOW.
0E	6	COMPD/A	COMPOSITE D/A disable. When HIGH, the COMPOSITE D/A converter is powered-down. When LOW, the D/A is enabled.
0E	5	SVIDD/A	LUMA/CHROMA D/A disable. When HIGH, the LUMA and CHROMA D/A converters are powered-down. When LOW, they are enabled.
0E	4	FKREN	Luminance processing enable. When FKREN is HIGH, the KEY input defines the function of CVBS input data. When the KEY input is HIGH, CVBS data is keyed over PD input data. When KEY is LOW, CVBS data is assumed to be luminance data delayed by one field.

Reg	Bit	Mnemonic	Function
			When FKREN is LOW, the KEY input operates normally, switching between CVBS and PD data.
0E	3	RATIO	Luminance ratio control bit. When LOW, 1/2 of current luminance and 1/2 of field delayed luminance from the CVBS input are added to yield a new combined luminance value. When RATIO is HIGH, 3/4 of current luminance is added to 1/4 of the delayed luminance to produce a new luminance value.
0E	2	TFLK	Luminance-pass threshold. The difference between current luminance and delayed luminance (from the CVBS inputs) is compared against a preset threshold set by TFLK. When TFLK is LOW, the high threshold must be exceeded to trigger the combining of current and delayed luminance (according to RATIO). If the higher threshold is not exceeded, current luminance is passed without modification.
			When TFLK is HIGH, a lower threshold is used to trigger the combining of current and delayed luminance.
0E	1	T512	EH/SL offset control bit. When LOW, the true value of EH and SL is offset by 256. When HIGH, the true value for EH and SL is offset by 512.
0E	0	CB100	NTSC/PAL color bars select. When HIGH, color bars with 100% white level are selected. When LOW, color bars will have 75% white level.

Standards Control Register (22091/191)

Reg	Bit	Mnemonic	Function
0F	7	EFEN	Same as Register 0E bit 7, but read-only.
0F	6	SIX25	Select 625 lines per frame. When HIGH, the encoder assumes 625 line per frame. When LOW, 525 lines per frame are assumed.
0F	5	PALID	PAL select. When HIGH, Phase alternate line (PAL) operation is selected. When LOW, operation conforms to NTSC standards.
0F	4	SETUP	Setup enable. When HIGH, a 7.5 IRE Pedestal is added to the output video. when LOW, no pedestal is added.
0F	3-2	YGAIN	Luminance gain settings are adjusted to conform to the following NTSC and PAL standards: 00 NTSC without SETUP 01 NTSC-A and PAL-M 10 PAL-I and PAL-N 11 (reserved)

Reg	Bit	Mnemonic	Function
0F	1-0	CGAIN	Chrominance gain settings are adjusted to conform to the following NTSC and PAL standards: 00 NTSC without SETUP 01 NTSC-A and PAL-M 10 PAL-I and PAL-N 11 (reserved)
			Timing Registers
10	7-0	SY	Horizontal sync tip length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
11	7-0	BR	Breezeway length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
12	7-0	BU	Burst length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
13	7-0	CBP	Color back porch length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
14	7-0	XBP	Extended color back porch 8 LSBs. This 8-bit register holds the LSBs of a 10-bit value extending from 0 to 1023 PCK cycles. The two MSBs are located in control register 18.
15	7-0	VA	Active video 8 LSBs. This 8-bit register holds the LSBs of a 10-bit value extending from 0 to 1023 PCK cycles. The two MSBs are located in control register 18.
16	7-0	VC	Active video start 8 LSBs. This 8-bit register holds the LSBs of a 10-bit value which is the initial half active video length extending from 0 to 1023 PCK cycles. The two MSBs are located in control register 18.
17	7-0	VB	Active video end 8 LSBs This 8-bit register holds the LSBs of a 10-bit value which is the end half active video length extending from 0 to 1023 PCK cycles. The two MSBs are located in control register 18.
18	7-6	XBP	Extended color back porch 2 MSBs. These two bits hold the MSBs of a 10-bit value extending from 0 to 1023 PCK cycles. The LSBs are located in control register 14.
18	5-4	VA	Active video 2 MSB. These two bits hold the MSBs of a 10-bit value extending from 0 to 1023 PCK cycles. The LSBs are located in control register 15.
18	3-2	VC	Active video start 2 MSBs. These two bits hold the MSBs of a 10-bit value which is the initial half active video length extending from 0 to 1023 PCK cycles. The LSBs are located in control register 16.
18	1-0	VB	Active video end 2 MSBs. These two bits hold the

Reg	Bit	Mnemonic	Function
			MSBs of a 10-bit value which is the end half active video length extending from 0 to 1023 PCK cycles. The LSBs are located in control register 17.
19	7-0	FP	Front porch length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
1A	7-0	EL	Equalization pulse LOW length. This 8-bit register holds a value from 0 to 255 PCK cycles.
1B	7-0	EH	Equalization pulse HIGH length. This 8-bit register holds a value extending from 0 to 255 PCK cycles. This value, when added to 256 (or 512), determines the final pulse length in the range of 256 to 511 (or 767) PCK cycles.
1C	7-0	SL	Vertical sync LOW length. This 8-bit register holds a value from 0 to 255 PCK cycles. This value, when added to 256 (or 512), determines the final pulse length in the range of 256 to 511 (or 767) PCK cycles.
1D	7-0	SH	Vertical sync HIGH length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
1E	7-0	CBL	Color bar length. This 8-bit register holds a value which is the length of each color bar displayed extending from 0 to 255 PCK cycles.

Reg	Bit	Mnemonic	Function
1F	7-5	FIELD	Field identification (read only). These three bits are updated 12 PXCK periods after each VHSYNC\. They allow the user to determine field type on a continuous basis.
1F	4-0	LTYPE	Line type identification (read only). These five bits are updates 5 PXCK periods after each VHSYNC\. They allow the user to determine line type on a continuous basis.
			Subcarrier Registers
20	7-0	FREQL	Subcarrier frequency 4th byte (LSBs). This 8-bit register holds the LSB (bits 7-0) of the 32-bit subcarrier frequency value (non-genlock modes). The next eight most significant bits are held in Register 21.
21	7-0	FREQ3	Subcarrier frequency 3rd byte. This 8-bit register holds bits 15:8 of the subcarrier frequency value (non-genlock modes). The next eight most significant bits are held in Register 22.
22	7-0	FREQ2	Subcarrier frequency 2nd byte. This 8-bit register holds bits 23-16 of the subcarrier frequency value (non-genlock modes). The eight MSBs are held in Register 23.
23	7-0	FREQM	Subcarrier frequency 1st byte (MSBs). This 8-bit register holds the MSBs

Reg	Bit	Mnemonic	Function
			(bits 31-24) of the 32-bit subcarrier frequency value (non-genlock modes).
24	7-0	SYSPHL	Video phase offset LSBs. This 8-bit register holds the 8 LSBs of color subcarrier phase offset during active video.
25	7-0	SYSPHM	Video phase offset MSBs. This 8-bit register holds the 8 MSBs of color subcarrier phase offset during active video.
26	7-0	BURPHL	Burst phase offset LSBs. This 8-bit register holds the 8 LSBs of burst phase offset for color adjustment.
27	7-0	BURPHM	Burst phase offset MSBs. This 8-bit register holds the 8 MSBs of burst phase for color adjustment.
			Test I/O Register
40	7-0	TESTDAT	Test data input/output. This 8-bit register holds MSBs or LSBs, as determined by the Test Control Register. This control address does not autoincrement during read or write operations. To exit the test mode, reset the Control Register pointer by setting A_{1-0} and R/W\ LOW and then bring CS\ LOW.
			Mask Register
50	7-0	MASK	Mask register. This 8-bit register holds an 8-bit word that is logically ANDed with the incoming data presented to the three CLUTs in color-index mode. This register is a write-only register.
			Y-Component Register
60	7-0	Y	Y-component register. This register holds the contents of the luminance value before the Sync and Blank Insert circuitry of the encoder. Loading the Control Register pointer with 60_h brings 8-bit Y values out on the D_{7-0} port.

Color Lookup Table

The CLUT can be used in a variety of ways, depending on the data format and source presented to the PD port.

The CLUT is loaded like a RAMDAC, sequentially writing one byte to each of the three locations associated with the selected CLUT address. These three locations are referred to as Tables D, E, and F (not R,G, and B because they may or may not contain RGB information). and are loaded in that sequence. The address will increment automatically after the three values at one address are written or read.

Color-Index Modes

In color-index (CI) mode, the CLUT is used to store the color look-up data, translating the 8-bit source pixel data into 24-bit RGB colors. Table D holds red data, Table E is green data, and Table F holds blue Data. The incoming data are presented to the three tables in parallel, and a 24-bit output is produced.

When the encoder is connected in parallel with a RAMDAC in a VGA system, the CLUT can be loaded simultaneously with the CLUT in the output RAMDAC. If a 6-bit RAMDAC is employed, 6 bits can be loaded via data pins D_{7-2} (MSB justified). The two LSBs should be set to 00 for optimal black level representation, but the largest error introduced by extraneous data in the LSBs is 3/4 LSB (at 6 bits). The encoder will produce the closest possible translation of the VGA colors in the encoded video environment.

GBR/RGB Modes

The nominal configuration for GBR/RGB modes is unity gain (CLUT data = CLUT address) for PAL and NTSC. Other transfer functions, such as gain adjustment, offset, and gamma correction, are easily loaded. The color data is loaded into the tables in G-B-R sequence in GBR mode, and R-G-B sequence in RGB mode.

Luminance/Color Difference Modes

The TMC22x9x expects Y, B-Y, and R-Y signals at the input to its modulator section. When presenting CCIR-601 YC_BC_R or digitized Y, B-Y, R-Y data to the CLUT, gain and offset factors are needed. Table 5 specifies the recommended transfer functions. CLUTs are loaded in $Y\text{-}C_B\text{-}C_R$ sequence.

Overlay Operation

For the TMC22090/091 and TMC22190/191 (when Format Control Register Bit 6 = LOW), the OL_{4-0} inputs are inactive. In CCIR-601 operation, the nominal data range for Y is from 16 to 235 and for C_B and C_R is from 16 to 240. This means that CLUT locations 0 to 15 and 241 to 255 are available for overlay colors. When the overlay locations are addressed (by forcing CLUT addresses outside the normal CCIR-601 data range), the addressed CLUT data is encoded resulting in the specific color found in that CLUT location. Overlay colors information stored in the unused CLUT locations must be Y, B-Y, R-Y values. Y, B-Y, and R-Y values are found from RGB values by:

$$\begin{aligned} Y &= 0.299\ R + 0.587\ G + 0.114\ B \\ B\text{-}Y &= -0.299\ R - 0.587\ G + 0.886\ B \\ R\text{-}Y &= 0.701\ R - 0.587\ G - 0.114\ B \end{aligned}$$

For the TMC22190/191, when the Format Control Register Bit 6 = HIGH, Overlay is controlled by the OL_{4-9} inputs which directly access CLUT locations, 01 thru 0F and F1 thru FF. The values stored in these CLUT locations are to be in RGB format.

Table 5. CLUT Transfer Functions for NTSC and PAL.

Input Format (CLUT Address) Component	Data Range	Transfer Equations	Output Format (CLUT Data) Component	Data Range
R	0 to 255	1-1	R_O	0 to 255
G	0 to 255	1-1	G_O	0 to 255
B	0 to 255	1-1	B_O	0 to 255
Y	16 to 235	$Y_O = Y * 1.1644 - 18.63$	Y_O	0 to 255
C_B	+/-112	$(B-Y)_O = C_B * 1.0126$	$(B-Y)_O$	+/-113
C_R	+/-112	$(R-Y)_O = C_R * 0.8011$	$(R-Y)_O$	+/-90
Y	0 to 255	1-1	Y_O	0 to 255
B-Y	+/-127	$(B-Y)_O = (B-Y) * 0.893$	$(B-Y)_O$	+/-113
R-Y	+/-127	$(R-Y)_O = (R-Y) * 0.7065$	$(R-Y)_O$	+/-90

Table 6. CLUT Locations Addressed by Overlay Inputs (22190/191)

OL_{4-0}	CLUT location
00	No Overlay
01	01
02	02
....	....
....	....
0E	0E
0F	0F
10	No Overlay
11	F1
12	F2
....	....
....	....
1E	FE
1F	FF

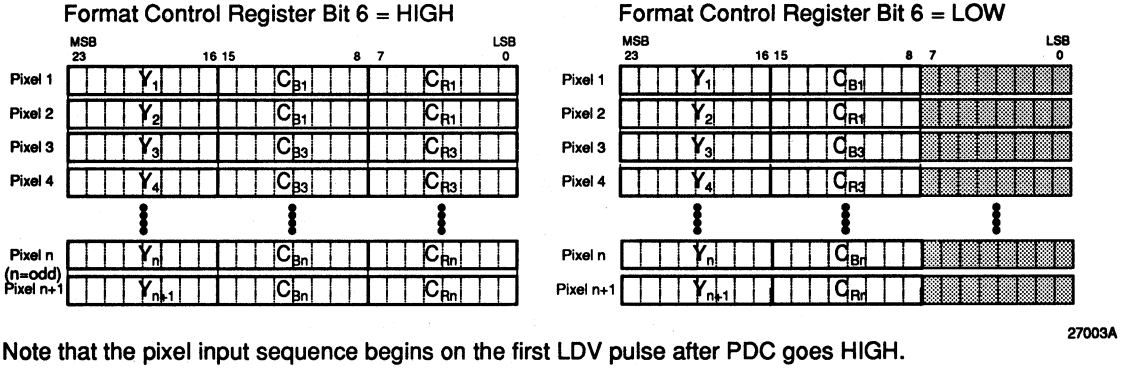
Color-space Conversion in the Matrix

When the input pixels are in RGB, GBR, or color-index format and the CLUTs are bypassed (22190/191), the Matrix remains enabled, converting RGB data to color-difference format. When the input pixels are in 444 format (YC_BC_R444, RGB, GBR, CI), the Interpolator (which converts 422 to 444) is not active. When the input pixels are in YC_BC_R format, the CLUTs are enabled and scale that data to color-difference values, leaving the Matrix inactive. In color-index mode, the Matrix is active, converting the RGB CLUT output data to color-difference values.

Table 7. Pixel Input Operation for Format Control Register bit 6 = HIGH (22190/191)

Format Control Register		Pixel Data Format	
FORMAT Bit 3,2	**INMODE** Bit 1,0	**BYPASS\ = LOW** CLUTs bypassed	**BYPASS\ = HIGH** CLUTs enabled
00 (RGB)	00 (444)	RGB	YC_BC_R444
00	01 (422)	RGB	YC_BC_R422
00	10 (15-bit)	RGB	RGB15
00	11 (CI)	RGB	CI
01	xx	reserved	reserved
10 (GBR)	00 (444)	GBR	YC_BC_R444
10	01 (422)	GBR	YC_BC_R422
10	10 (15-bit)	GBR	GBR15
10	11 (CI)	GBR	CI
11	xx	not allowed	not allowed

Figure 2. Pixel Data (PD_{23-0}) Sequence for YC_BC_R422



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Note that the pixel input sequence begins on the first LDV pulse after PDC goes HIGH.

Gamma Correction

Gamma is built into broadcast television systems as a correction factor for nonlinearity in the signal path. These nonlinearities occur in image acquisition (nonlinear conversion of light into current in a vidicon) and at the display (nonlinear conversion of voltage into beam current in a CRT and phosphor nonlinearity in converting current into light). To minimize the number of nonlinear amplifiers needed, these factors were combined into a single term, Gamma, which is applied to the signal at the camera (there are fewer cameras than receivers).

Gamma is employed in television production to give a particular "feel" to a picture, hence it is not a fixed value, even within a given television system.

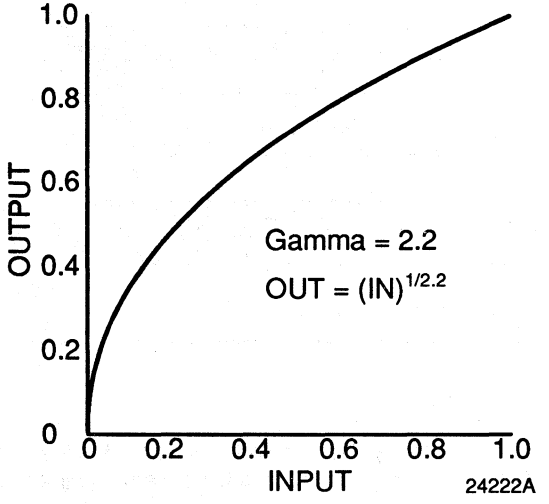
A Gamma corrector transfer function takes the form of
Output = k (Input)$^{1/\gamma}$

where a typical Gamma is 2.2 for NTSC, 2.8 for PAL.

Computer systems usually ignore Gamma in driving a display monitor. Each R, G, and B channel is treated as linear. When encoding a computer display output to video, the user must decide whether to apply a gamma correction factor and, if so, what value. It is a good assumption that, since the digital video input over the CVBS bus is in composite form, it has been Gamma corrected.

Gamma correction is applied in the RGB domain. When operating in YC_BC_R, for example when encoding a CCIR-601 signal, Gamma should have already been applied. Gamma correction is readily added to the RGB transfer equations shown in Table 5.

Figure 3. Typical Gamma Curve for NTSC.



Video Timing

The TMC22x9x can be programmed to accommodate a wide range of system timing requirements. With a line locked pixel rate of 10 to 15 Mpps, the digitally synthesized horizontal waveforms and subcarrier frequency and phase are determined from 24 registers that are loaded by a controller.

Horizontal Programming

Horizontal interval timing is fully programmable, and is established by loading the timing registers with the durations of each horizontal element, the duration expressed in PCK clock cycles. In this way, any pixel clock rate between 10 MHz and 15 MHz can be accommodated, and any desired standard or non-standard horizontal video timing may be produced. Figure 4 illustrates the horizontal blanking interval with timing register identification.

Horizontal timing parameters can be calculated as follows:

t = N x (PCK period)
= N x (2 x PXCK period)

where N is the value loaded into the appropriate timing register, and PCK is the pixel clock period.

Horizontal timing resolution is two PXCK periods. PXCK must be chosen such that it is an even integer multiple of the horizontal line frequency. This ensures that the horizontal line period, H, contains an integer number of pixels. The horizontal line comprises the sum of appropriate elements.

H = FP + SY + BR + BU + CBP + VA

When programming horizontal timing, subtract 5 PCK periods from the calculated values of CBP and add 5 PCK periods to the calculated value for VA.

Figure 4. Horizontal Blanking Interval Timing

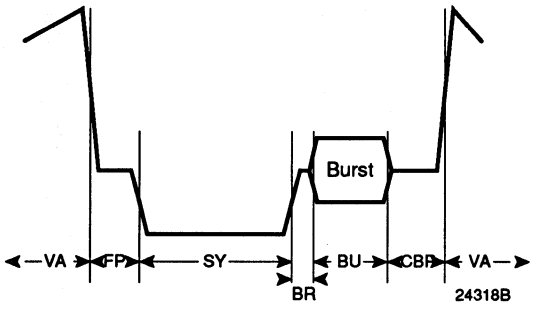


Table 8. Horizontal Timing Specifications

Parameter	NTSC-M (µs)	PAL-I (µs)	PAL-M (µs)
FP	1.5	1.65	1.9
SY	4.7	4.7	4.95
BR	0.6	0.9	0.9
BU	2.5	2.25	2.25
CBP	1.6	2.55	1.8
VA	52.6556	51.95	51.692
H	63.5556	64.0	63.492

Vertical Programming

Vertical interval timing is also fully programmable, and is established by loading the timing registers with the durations of each vertical timing element, the duration expressed in PCK clock cycles. In this way as with horizontal programming, any pixel rate between 10 and 15 Mpps can be accommodated, and any desired standard or non-standard vertical video timing may be produced.

Like horizontal timing parameters, vertical timing parameters are calculated as follows:

t = N x (PCK period)
= N x (2 x PXCK period)

where N is the value loaded into the appropriate timing register, and PCK is the pixel clock period.

The Vertical Interval comprises several different line types based upon H, the Horizontal line time.

H = (2 x SL) + (2 x SH) [Vertical sync pulses]
= (2 x EL) + (2 x EH) [Equalization pulses]

The VB and VC lines are added to produce the half-lines needed in the vertical interval at the beginning and end of some fields. These must properly mate with components of the normal lines.

VB = CBP + VA - XBP = H/2 - CBP
VC = VA - (EL + EH) = VA - H/2

where Equalization HIGH and LOW pulses (EL + EH) = H/2 and the Extended Color Back Porch, XBP = VA + CBP - VB. XBP begins after the end of burst, BU, taking the place of CBP in vertical interval UBV lines.

Figure 5. Vertical Sync and Equalization Pulse Detail

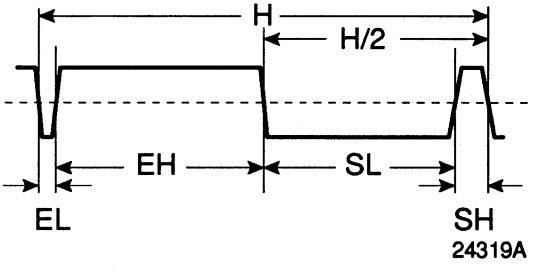


Table 9. Vertical Timing Specifications

Parameter	NTSC-M (µs)	PAL-I (µs)	PAL-M (µs)
H	63.5556	64	63.492
EH	29.4778	29.65	29.45
EL	2.3	2.35	2.3
SH	4.7	4.7	4.65
SL	27.1	27.3	27.1

Figure 6. NTSC Vertical Interval

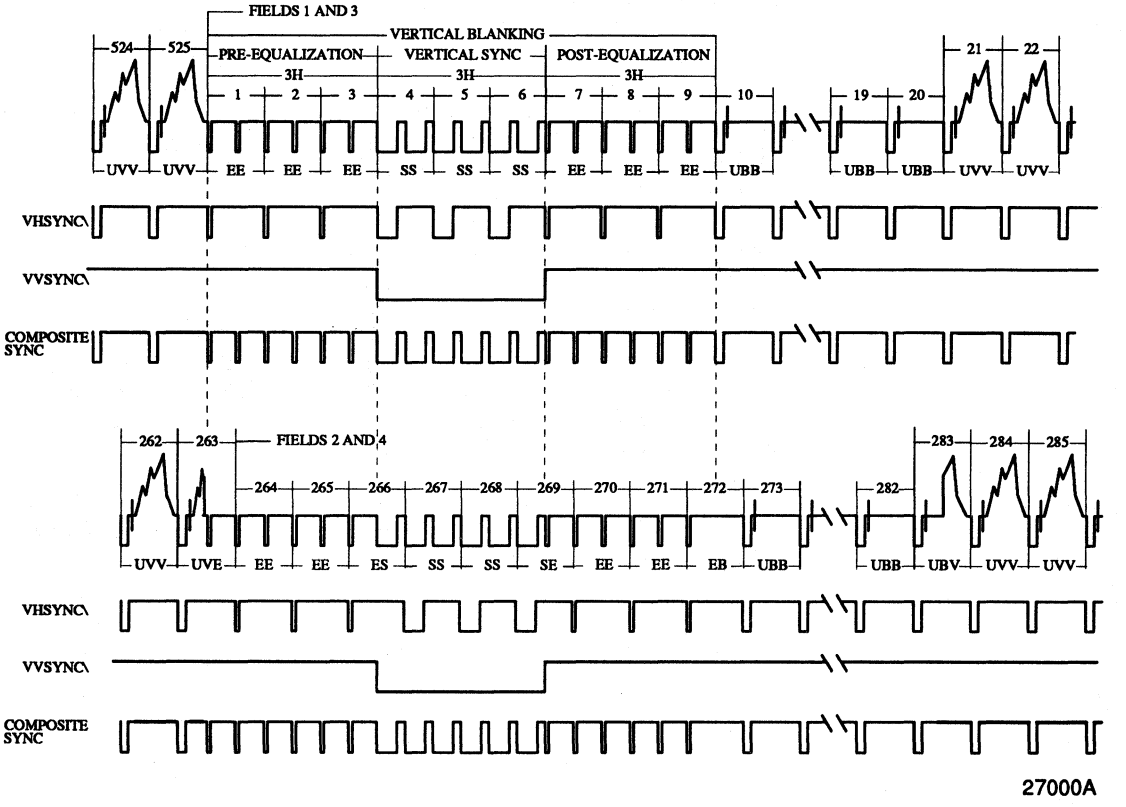


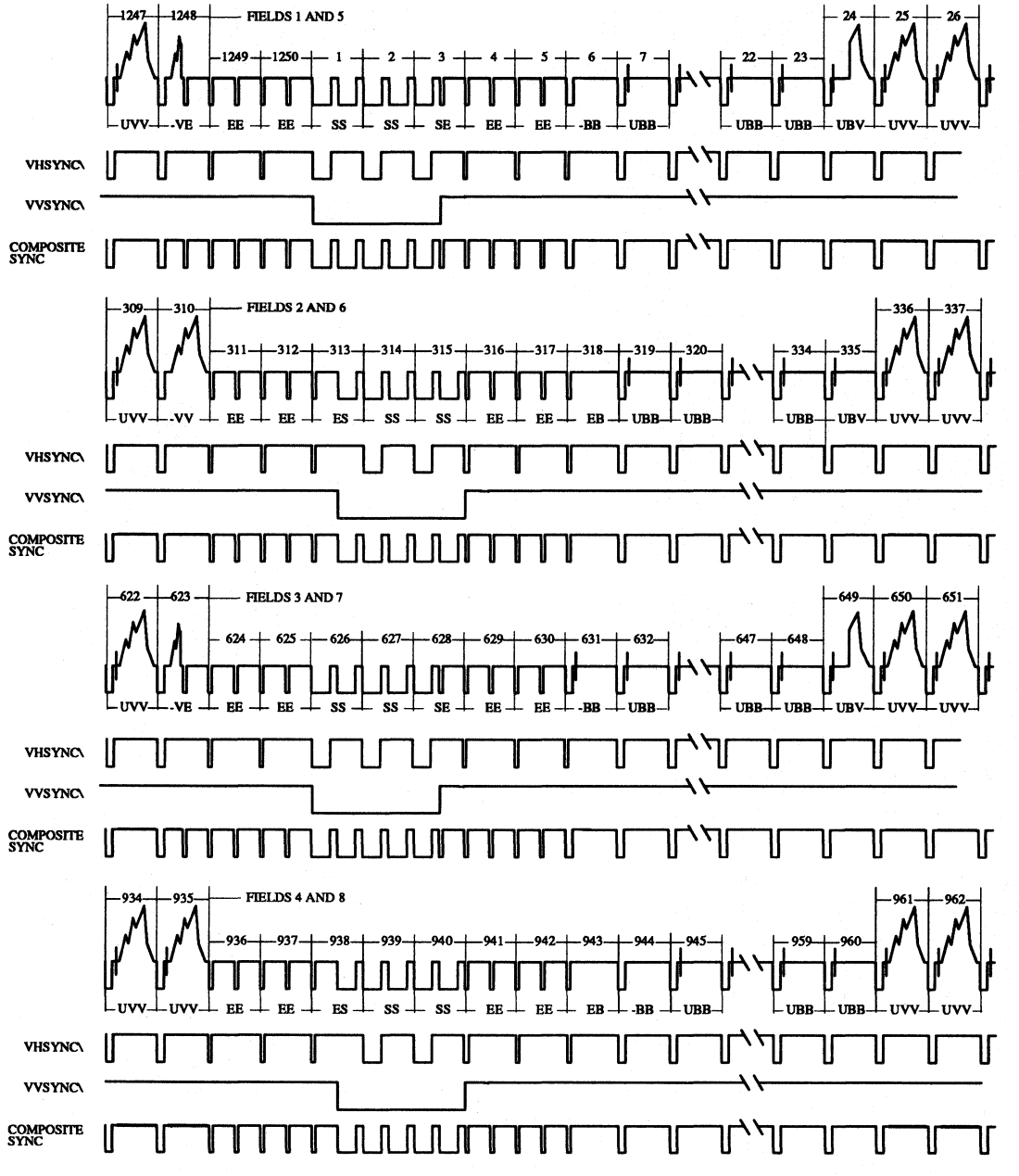
Table 10. NTSC Field / Line Sequence and Identification

Field 1 FIELD ID = x00			Field 2 FIELD ID = x01			Field 3 FIELD ID = x10			Field 4 FIELD ID = x11		
Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE
1	EE	00	264	EE	00	1	EE	00	264	EE	00
2	EE	00	265	EE	00	2	EE	00	265	EE	00
3	EE	00	266	ES	01	3	EE	00	266	ES	01
4	SS	03	267	SS	03	4	SS	03	267	SS	03
5	SS	03	268	SS	03	5	SS	03	268	SS	03
6	SS	03	269	SE	02	6	SS	03	269	SE	02
7	EE	00	270	EE	00	7	EE	00	270	EE	00
8	EE	00	271	EE	00	8	EE	00	271	EE	00
9	EE	00	272	EB	10	9	EE	00	272	EB	10
10	UBB	0D	273	UBB	0D	10	UBB	0D	273	UBB	0D
...	...	...	...	...	...	...	...	...	...	...	...
20	UBB	0D	282	UBB	0D	20	UBB	0D	282	UBB	0D
21	UVV	0F	283	UBV	0E	21	UVV	0F	283	UBV	0E
22	UVV	0F	284	UVV	0F	22	UVV	0F	284	UVV	0F
...	...	...	...	...	...	...	...	...	...	...	...
262	UVV	0F	524	UVV	0F.	262	UVV	0F	524	UVV	0F
263	UVE	0C	525	UVV	0F	263	UVE	0C	525	UVV	0F

EEEqualization pulse
SEHalf-line vertical sync pulse, half-line equalization pulse
SSVertical sync pulse
ESHalf-line equalization pulse, half-line vertical sync pulse
EBEqualization broad pulse
UBB Black burst
UVV Active video
UVEHalf-line video, half-line equalization pulse
UBVhalf-line black, half-line video

Master and Genlock mode details of VHSYNC\, VVSYNC\, and composite VVSYNC\ (SOUT = HIGH) outputs are shown in Figures 6 and 7. When VHSYNC\ and VVSYNC\ are used as inputs (Slave mode), their falling edges mark the beginning of the sync interval and the width of the input pulse is specified under Operating Conditions.

Figure 7. PAL Vertical Interval



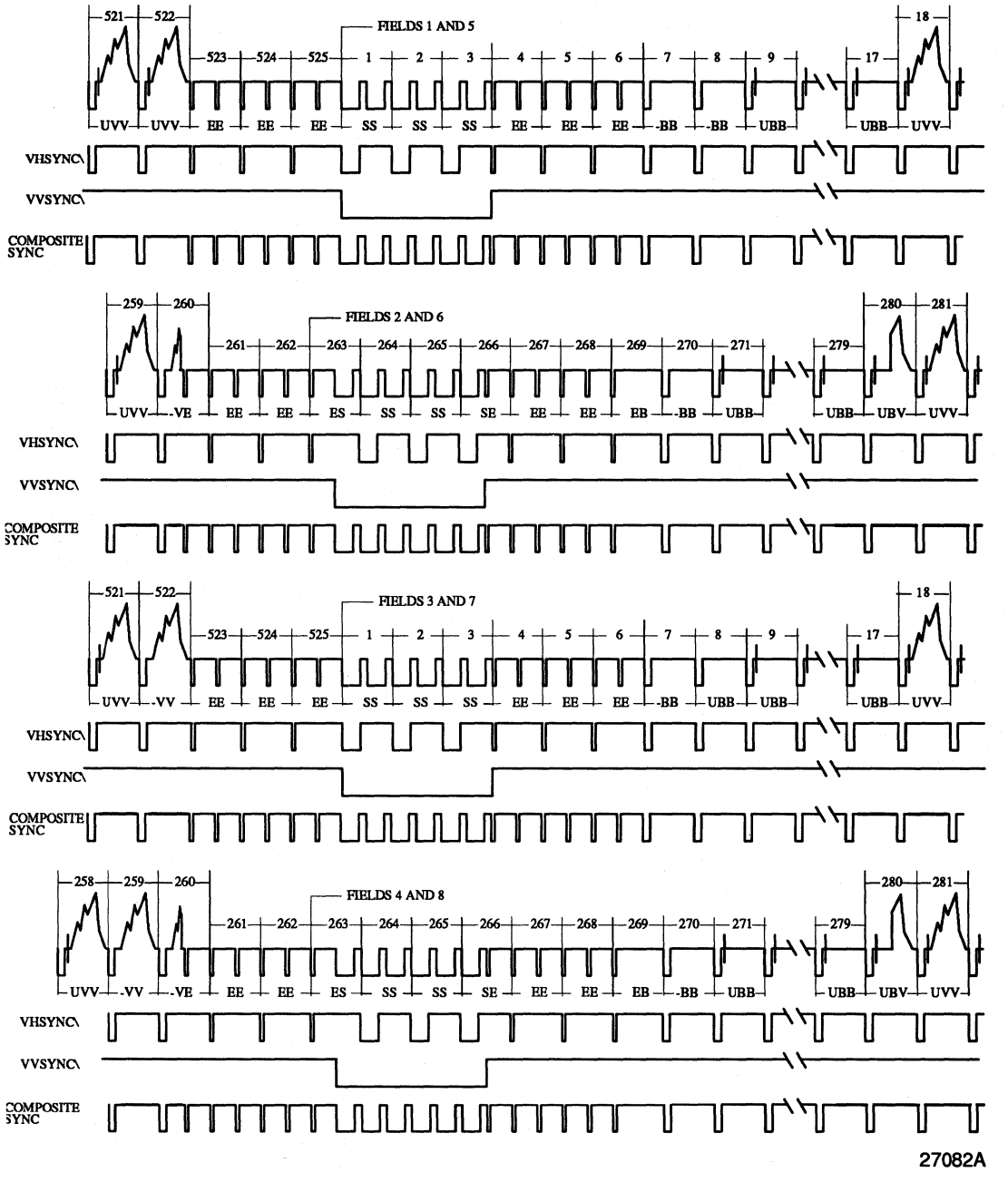
27001A

Table 11. PAL Field / Line Sequence and Identification

Field 1 and 5 FIELD ID = 000, 100			Field 2 and 6 FIELD ID = 001, 101			Field 3 and 7 FIELD ID = 010, 110			Field 4 and 8 FIELD ID = 011, 111		
Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE
1	SS	03	313	ES	01	626	SS	03	938	ES	01
2	SS	03	314	SS	03	627	SS	03	939	SS	03
3	SE	02	315	SS	03	628	SE	02	940	SS	03
4	EE	00	316	EE	00	629	EE	00	941	EE	00
5	EE	00	317	EE	00	630	EE	00	942	EE	00
6	-BB	05	318	EB	10	631	UBB	0D	943	EB	10
7	UBB	0D	319	UBB	0D	632	UBB	0D	944	-BB	05
8	UBB	0D	320	UBB	0D	633	UBB	0D	945	UBB	0D
...	...	...	...	...	...	...	...	...	...	...	...
22	UBB	0D	335	UBB	0D	647	UBB	0D	960	UBB	0D
23	UBV	0E	336	UVV	0F	648	UBV	0E	961	UVV	0F.
24	UVV	0F	337	UVV	0F	649	UVV	0F	962	UVV	0F
...	...	...	...	...	...	...	...	...	...	...	...
308	UVV	0F	621	UVV	0F	933	UVV	0F	1246	UVV	0F
309	UVV	0F	622	-VV	07	934	UVV	0F	1247	UVV	0F
310	-VV	07	623	-VE	04	935	UVV	0F	1248	-VE	04
311	EE	00	624	EE	00	936	EE	00	1249	EE	00
312	EE	00	625	EE	00	937	EE	00	1250	EE	00

EEEqualization pulse
SEHalf-line vertical sync pulse, half-line equalization pulse
SSVertical sync pulse
ESHalf-line equalization pulse, half-line vertical sync pulse
EBEqualization broad pulse
UBB Black burst
-BBBlack burst with color burst suppressed
UVV Active video
-VVActive video with color burst suppressed
UVEHalf-line video, half-line equalization pulse
-VEHalf-line video, half-line equalization pulse, color burst suppressed.
UBVhalf-line black, half-line video

Figure 8. PAL-M Vertical Interval



27082A

Table 12. PAL-M Field / Line Sequence and Identification

Field 1 and 5 FIELD ID = 000, 100			Field 2 and 6 FIELD ID = 001, 101			Field 3 and 7 FIELD ID = 010, 110			Field 4 and 8 FIELD ID = 011, 111		
Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE
1	SS	03	263	ES	01	1	SS	03	263	ES	01
2	SS	03	264	SS	03	2	SS	03	264	SS	03
3	SS	03	265	SS	03	3	SS	03	265	SS	03
4	EE	00	266	SE	02	4	EE	00	266	SE	02
5	EE	00	267	EE	00	5	EE	00	267	EE	00
6	EE	00	268	EE	00	6	EE	00	268	EE	00
7	-BB	05	269	EB	10	7	-BB	05	269	EB	10
8	-BB	05	270	-BB	05	8	UBB	05	270	-BB	05
9	UBB	0D	271	UBB	1D	...	...	...	271	UBB	1D
...	...	...	...	...	...	17	UBB	0D.	...	...	...
17	UBB	0D	279	UBB	0D	18	UVV	0F	279	UBB	0D
18	UVV	0F	280	UBV	0E.	...	...	...	280	UBV	0E.
...	...	...	281	UVV	0F	258	UVV	0F	281	UVV	0F
259	UVV	0F	...	...	..	259	-VV	07	...	...	..
260	-VE	04	521	UVV	0F	260	-VE	04	521	UVV	0F
261	EE	00	522	-VV	07	261	EE	00	522	UVV	0F
262	EE	00	523	EE	00.	262	EE	00	523	EE	00
			524	EE	00				524	EE	00
			525	EE	00				525	EE	00

EEEqualization pulse
SEHalf-line vertical sync pulse, half-line equalization pulse
SSVertical sync pulse
ESHalf-line equalization pulse, half-line vertical sync pulse
EBEqualization broad pulse
UBB Black burst
-BBBlack burst with color burst suppressed
UVV Active video
-VVActive video with color burst suppressed
UVEHalf-line video, half-line equalization pulse
-VEHalf-line video, half-line equalization pulse, color burst suppressed.
UBVhalf-line black, half-line video

Table 13. Standard Timing Parameters

Standard	Field Rate (Hz)	Horizontal Freq. (kHz)	Pixel Rate (Mpps)	PXCK Freq. (MHz)	Timing Register (hex) SY 10	BR 11	BU 12	CBP 13	XBP 14	VA 15	VC 16	VB 17	Note 1 18	FP 19	EL 1A	EH[2] 1B	SL[2] 1C	SH 1D	CBL 1E
NTSC sqr. pixel	59.94	15.734266	12.27	24.54	3A	07	1F	0F	23	8B	05	77	65	12	1C	6A	4D	3A	52
NTSC CCIR-601	59.94	15.734266	13.50	27.00	40	08	22	11	3F	CB	1E	9D	65	14	1F	8E	6E	3F	59
NTSC 4x Fsc	59.94	15.734266	14.32	28.64	43	09	24	12	54	F7	30	B5	65	15	21	A6	84	43	5F
PAL sqr. pixel	50.00	15.625000	14.75	29.50	45	0D	21	21	6D	03	2B	B7	75	19	23	B5	93	45	61
PAL CCIR-601	50.00	15.625000	13.50	27.00	40	0C	1E	1D	4D	C3	13	93	65	16	20	90	71	3F	58
PAL 15 Mpps	50.00	15.625000	15.00	30.00	46	0D	22	21	73	11	31	BF	75	19	23	BD	9A	47	62
PAL-M sqr.pixel	60.00	15.750000	12.50	25.01	3E	0B	1C	13	26	86	FE	8B	61	18	1D	70	53	3A	52
PAL-M CCIR-601	60.00	15,750000	13.50	27.00	44	0C	1E	13	26	Bf	12	99	65	1A	1F	8E	6E	3F	57
PAL-M 4x Fsc	60.00	15,750000	14.30	28.60	47	0D	20	15	4C	E8	22	AC	65	1B	21	A5	84	42	5D

Note:
1. XBP, VA, VC, and VB are 10-bit values. The 2 MSBs for these four variables are in Timing Register 18. See Table 4.
2. EH and SL are 9-bit values. A most significant "1" is forced by the TMC22x9x since EH and SL must range from 256 to 511. Extending the range of EH and SL to 767 is possible in the TMC22091/191. Only the eight LSBs are stored in Timing Registers 1B and 1C.
3. Every calculated timing parameter has a minimum value of 5 except EH and SL which have minimum values of 256.

VITS Signal Insertion

In both NTSC and PAL, the TMC22x9x can be set up to allow VITS signals in the vertical interval in place of normal black burst lines (UBB). This is controlled by the Interface Control Register bit 7. If this bit is LOW, UBB lines are black burst and are independent of TMC22x9x input data. If the bit is HIGH, all vertical interval UBB lines become UVV. UVV lines are active video and depend upon data input to the TMC22x9x. VITS lines may be used for inserting special test signals or for passing captioning data through the encoder.

Edge Control

SMPTE 170M NTSC and Report 624 PAL video standards call for specific rise and fall times on critical portions of the video waveform. The TMC22x9x does this automatically, requiring no user intervention. The TMC22x9x digitally defines slopes compatible with SMPTE 170M NTSC or CCIR Report 624 PAL on all vital edges:

1. H and V Sync leading and trailing edges.
2. Burst envelope.
3. Active video leading and trailing edges.

Subcarrier Programming

The color subcarrier is produced by an internal 32-bit digital frequency synthesizer which is completely programmable in frequency and phase. Separate registers are provided for phase adjustment of the color burst and of the active video, permitting external delay compensation, color adjustment, etc.

In Master or Slave mode, the subcarrier is internally synchronized to establish and maintain a specified relationship between the leading edge of horizontal sync and color burst phase (SCH). In NTSC and PAL, SCH synchronization is performed every eight fields, on field 1 of the eight-field sequence. Proper subcarrier phase is maintained through the entire eight fields, including the 25 Hz offset in PAL systems. See the description of 8FSUBR under Test Control Register bit 1 for the subcarrier reset function.

In Genlock mode, the phase and relative frequency of the incoming video is transmitted by the TMC22070 Genlocking Video Digitizer over the CVBS bus at the beginning of each line, which synchronizes the digital subcarrier synthesizer. When control register bit BUKEN is HIGH and digitized burst from the TMC22070 is passed

through to the reconstruction D/A converter, the reference subcarrier for the chrominance modulator is still synthesized within the encoder.

NTSC Subcarrier

For NTSC encoding, the subcarrier synthesizer frequency has a simple relationship to the pixel clock period, repeating over 2 lines: The decimal value is:

$$FREQ = \frac{(455 / 2)}{(\text{pixels / line})} \times 2^{32}$$

This value must be converted to binary and split into four 8-bit registers, FREQM, FREQ2, FREQ3, and FREQL. The number of pixels / line is:

Pixels / line = (2 / PXCK frequency)(H period)

SYSPH establishes the appropriate phase relationship between the internal synthesizer and the chroma modulator. The nominal value for SYSPH is zero.

Other values for SYSPH must be converted to binary and split into two 8-bit registers, SYSPHM and SYSPHL.

Burst Phase (BURPH) sets up the correct relative NTSC modulation angle. The value for BURPH is:

BURPH = SYSPH + 8,192 = SYSPH + $\pi/4$

This value must be converted to binary and split into two 8-bit registers, BURPHM and BURPHL.

PAL Subcarrier

The PAL relationship is more complex, repeating only once in 8 fields (the well-known 25 Hz offset):

$$FREQ = \frac{(1135 / 4) + (1 / 625)}{(\text{pixels / line})} \times 2^{32}$$

This value must be converted to binary and split as described previously for NTSC. The number of pixels / line is found as in NTSC.

For PAL, the decimal value for SYSPH is found from:

$$SYSPH = FREQ / 2^{17}$$

This value must be converted to binary and split into two 8-bit registers, SYSPHM and SYSPHL. Burst Phase in PAL is identical to SYSPH. Therefore, the same values for SYSPHM and SYSPHL must be used for BURPHM and BURPHL.

PAL-M Subcarrier

$$FREQ = \frac{(909 / 4)}{(\text{pixels / line})} \times 2^{32}$$

$$SYSPH = FREQ / 2^{17} = BURPH$$

Table 14. Standard Subcarrier Parameters

Standard	Field Rate (Hz)	Horizontal Freq. (kHz)	Pixel Rate (MHz)	PXCK Freq. (MHz)	Subcarrier Freq. (MHz)	Subcarrier Register (hex) BURPHM 27	BURPHL 26	SYSPHM 25	SYSPHL 24	FREQM 23	FREQ2 22	FREQ3 21	FREQL 20
NTSC sqr. pixel	59.94	15.734266	12.27	24.54	3.57954500	20	00	00	00	4A	AA	AA	C7
NTSC CCIR-601	59.94	15.734266	13.50	27.00	3.57954500	20	00	00	00	43	E0	F8	3E
NTSC 4x Fsc	59.94	15.734266	14.32	28.64	3.57954500	20	00	00	00	40	00	00	00
PAL sqr. pixel	50.00	15.625000	14.75	29.50	4.43361875	00	00	00	00	4C	F3	18	19
PAL CCIR-601	50.00	15.625000	13.50	27.00	4.43361875	00	00	00	00	54	13	15	96
PAL 15 Mpps	50.00	15.625000	15.00	30.00	4.43361875	00	00	00	00	4B	AA	C6	A1
PAL-M sqr.pixel	60	15.750	12.50	25.01	3.57561149	00	00	00	00	49	45	00	51
PAL-M CCIR-601	60	15,750	13.50	27.00	3.57561149	00	00	00	00	43	DF	3F	D7
PAL-M 4x Fsc	60	15,750	14.30	28.60	3.57561149	00	00	00	00	40	10	66	F5

SCH Phase Error Correction

SCH refers to the timing relationship between the 50% point of the leading edge of horizontal sync and the positive or negative zero-crossing of the color burst subcarrier reference. SCH error is usually expressed in degrees of subcarrier phase. In PAL, SCH is defined for line 1 of field 1, but since there is no color burst on line 1, SCH is usually measured at line 7 of field 1. The need to specify SCH relative to a particular line in PAL is due to the 25 Hz offset of PAL subcarrier frequency. Since NTSC has no such 25 Hz offset, SCH applies to all lines.

The SCH relationship is only important in the TMC22x9x when two video sources are being combined or if the composite video output is externally combined with another video source. In these cases, improper SCH phasing will result in a noticeable horizontal jump of one image with respect to another and/or a change in hue proportional to the SCH error between the two sources.

SCH phasing can be adjusted by modifying BURPH and SYSPH values by equal amounts. SCH is advanced/delayed by one degree by increasing/decreasing the value of BURPH and SYSPH by approximately $B6_h$. An SCH error of 15° is corrected with SYSPH and BURPH offsets of AAA_h.

Video Test Signals

The TMC22x9x has two standard video test waveforms available for evaluating video signal integrity. These are selected and controlled by the Format Control Register.

Setting the Format Control Register bits 0, 4, and 5 LOW generates standard color bars at the COMPOSITE output (Figure 9), the luminance component stair-step signal at the LUMA output, and the chrominance component on the CHROMA output. The six colors are 100% saturated PAL and 75% saturated for NTSC. The exact location of each color vector (subcarrier amplitude, subcarrier phase) can be measured using industry-standard instrumentation (vectorscope).

The percentage color saturation is selectable via Control Register 0E, bit 0 in the TMC22091/191.

The color bar test pattern produced comprises eight equal-width bars during VA, the active video period. The Timing Register value for CBL is found from:

$$CBL = \{ (VA + 7) / 8 \}$$

If CBL is larger than this, the color bars are truncated at the end of VA. If CBL is smaller than VA / 8, the color bar sequence will repeat, starting with another white bar. From left to right color bars 1 to 8 should be white, yellow, cyan, green, magenta, red, blue, and black. See Figures 35, 36, 41, 42, 47, 48.

The modulated ramp waveform is enabled by setting the Format Control Register to 30_h. It comprises constant-amplitude and constant-phase subcarrier modulation superimposed on a linear ramp which slews from black to white during the active video portion of each horizontal line interval (Figure 10). This waveform is useful in making differential gain and differential phase measurements on the video signal. Differential gain is a measure of the variation in saturation of a color as the luminance component is varied from black to white. Differential phase is a measure of the variation in hue of a color as the luminance component is varied from black to white. Differential gain and differential phase are measured with a vectorscope. See Figures 39, 40, 45, 46.

Figure 9. 100% Color Bars With 100% and 75% Chrominance Saturation

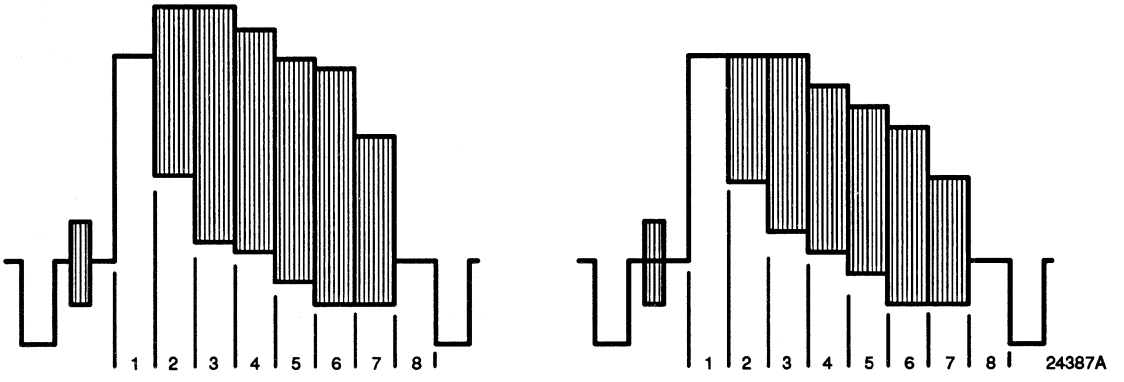
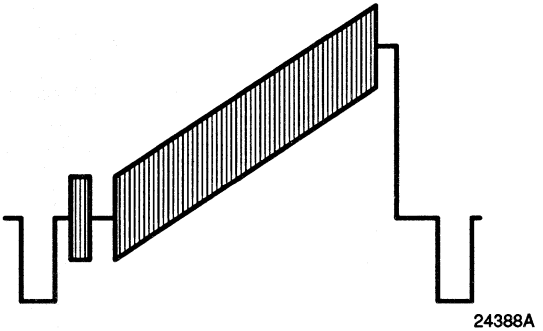


Figure 10. Modulated Ramp Waveform



Microprocessor Interface

The microprocessor interface employs a 13-line interface, with an 8-bit data bus and two address bits: four addresses are required for device programming and CLUT/register management. Address bit 0 selects between control registers and CLUT memory. Address bit 1 selects between reading/writing the register addresses and reading/writing register or CLUT data.

When writing, the address is presented along with a LOW on the R/W\ pin during the falling edge of CS\. Eight bits of data are presented on D_{7-0} during the subsequent rising edge of CS\. One additional falling edge of CS\ is needed to move input data to its assigned working registers.

Figure 11. Microprocessor Port - Write Timing

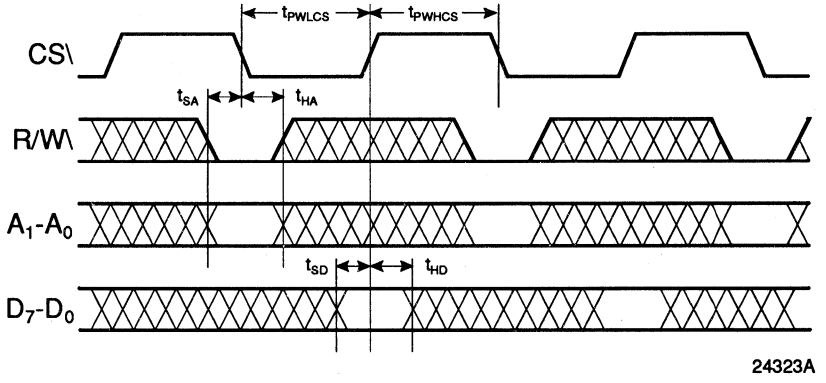
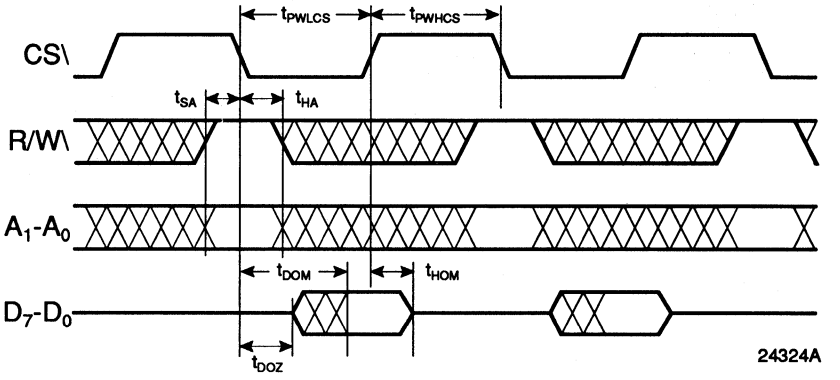


Figure 12. Microprocessor Port - Read Timing



In read mode, the address is accompanied by a HIGH on the R/W\ pin during a falling edge of CS\. The data output pins go to a low-impedance state t_{DOZ} ns after CS\ falls. Valid data is present on D_{7-0} t_{DOM} after the falling edge of CS\. Because this port operates asynchronously with the pixel timing, there is an uncertainty in this data valid output delay of one PXCK period. This uncertainty does not apply to t_{DOZ}.

The RESET\ pin restores the TMC22x9x to field 1 line 1 and places the encoder in a power-down state (if HRESET is LOW). Bit 4 of the Global Control Register (SRESET\) is set LOW. All other control words and CLUT contents are left unchanged. Returning RESET\ HIGH synchronizes the internal clock with PXCK and restores power to the device outputs.

Reading Pixel Data from the D_{7-0} Port

The microprocessor port of the TMC22x9x may be used to extract digital video pixels. The eight MSBs of the up-sampled and interpolated pixel data that go to the COMPOSITE D/A converter can also be sent to the D_{7-0} port and read for subsequent processing. When the Test Control Register is loaded with 28_h and the Control Register pointer is loaded with 40_h, the D_{7-0} port will begin outputting 8-bit composite pixels synchronous with respect to PXCK. To halt the pixel flow from D_{7-0}, simply bring CS\ HIGH.

The TMC22091/191 has an additional feature that allows luminance pixel data to be read from the D_{7-0}. In this case the eight MSBs of luminance found just prior to the Sync and Blank Insert block are routed to the microprocessor port. When the Control Register pointer is loaded with 60_h, the D_{7-0} port will begin outputting 8-bit luminance pixels synchronous with respect to PXCK. To halt the pixel flow from D_{7-0}, simply bring CS\ HIGH.

Operational Timing

The TMC22x9x operates in three distinct modes:

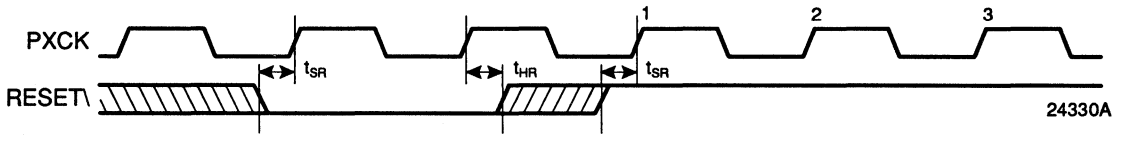
1. Master mode. The encoder independently produces all internal timing and provides digital sync to the host controller.

2. Slave mode. The encoder accepts horizontal and vertical sync from the controller and synthesizes the video output accordingly.

3. Genlock mode. The encoder accepts horizontal and vertical sync from the companion TMC22070 Genlocking Video Digitizer, synchronizes itself to the incoming video, and provides appropriate H Sync and V Sync to the host. It synchronizes Pixel Data input in two ways:

   a. Internal PDC. The encoder internally generates the Pixel Data Control (PDC)

Figure 13. Reset Timing - PCK Synchronization



signal which calls for data input from the external pixel source.

b. External PDC. The encoder receives a PDC signal from the host and accepts Pixel Data based on that input.

Reset Timing

The TMC22x9x operates from a master clock (PXCK) at twice the pixel rate. Some internal circuitry employs a clock at the pixel rate, PXCK / 2. In Master mode, the PCK to PXCK timing relationship is set on the rising edge of RESET\. In Figure 13, PCK is denoted by odd PXCK counts.

When RESET\ is taken LOW with sufficient setup time (t_{SR}) before a rising edge of PXCK, the internal state machines are reset and the device is put into a mode as dictated by the Global Control Register bits 0 and 4. In Master mode, when the RESET\ pin is taken HIGH, the internal clock timing is established. In Slave and Genlock mode, this timing is established by VHSYNC\ and GHSYNC\ respectively. The first PXCK following this RESET\ rising edge is designated as PXCK 1. Where it is significant, reference PXCK timing will be shown with numbered rising edges. A designation of 2N clocks refers to an even number of PXCK rising edges

from device reset. If RESET\ is not shown and clock numbering does not refer to 2N, timing is relative to signals shown in the diagram only.

Pixel Data Input Timing

PXCK is internally divided by 2 to generate an internal pixel clock, PCK which is not accessible from the pins of the TMC22x9x. To ensure the correct relationship between PCK and pixel data, PCK is locked to VHSYNC\ or GHSYNC\ (Slave or Genlock mode, respectively). In Master mode, VHSYNC\ is produced on the rising edge of PCK allowing external circuitry to synchronize the generation of pixel data and LDV which also operates at 1/2 the rate of PXCK.

The rising edge of LDV clocks the 24-bit pixel data into three 8-bit registers while PCK clocks that data through the pixel data path within the TMC22x9x. It is therefore necessary to meet the set-up and hold timing between pixel data and LDV as well as LDV and PCK.

Figure 14. Slave Mode PD Port Interface Timing (Genlock Mode)

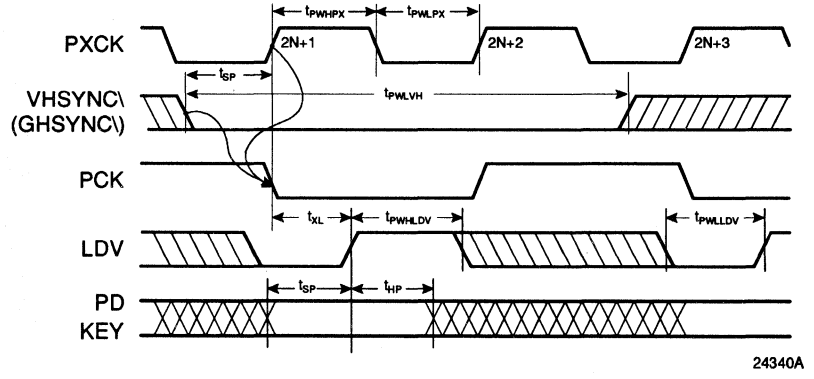
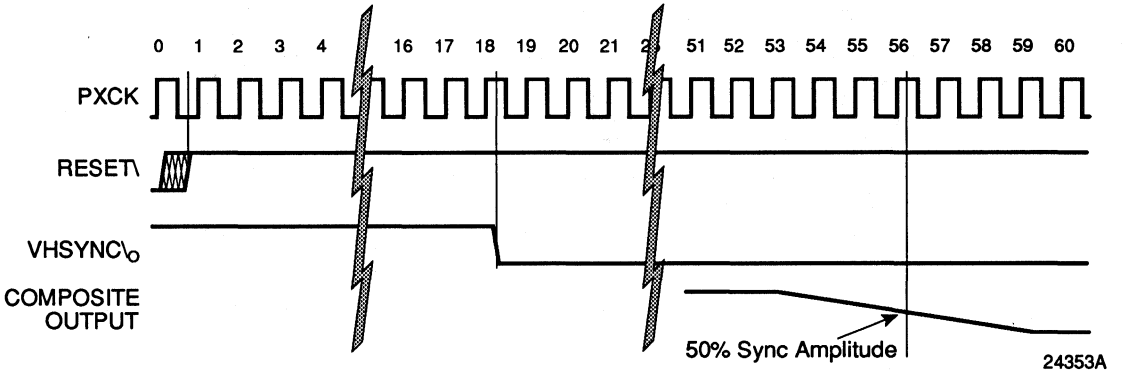


Figure 15. Master Mode Timing



Master Mode

In Master mode, initial timing is determined from the RESET\ input, and subsequent cycles result from programmed values in the Timing Control Registers. The Horizontal Sync output, VHSYNC\, goes LOW 18 PXCK clock cycles after the device is reset. The 50% point of the falling edge of sync LOW on line 4 of field 1 (NTSC) or line 1 of field 1 (PAL) occurs at the COMPOSITE and LUMA outputs 56 clocks after reset, or 38 clocks after VHSYNC\.

Slave Mode

In Slave mode, the 50% point of the falling edge of sync occurs 46 PXCK clocks after the falling edge of VHSYNC\, which is an input signal to the TMC22x9x. This must be provided by the host to begin every line. If it is early, the line will be started early, maintaining the 52 clock delay to output. If it comes late, the front porch portion of the output waveform will be extended as necessary.

Figure 16. Slave Mode Timing

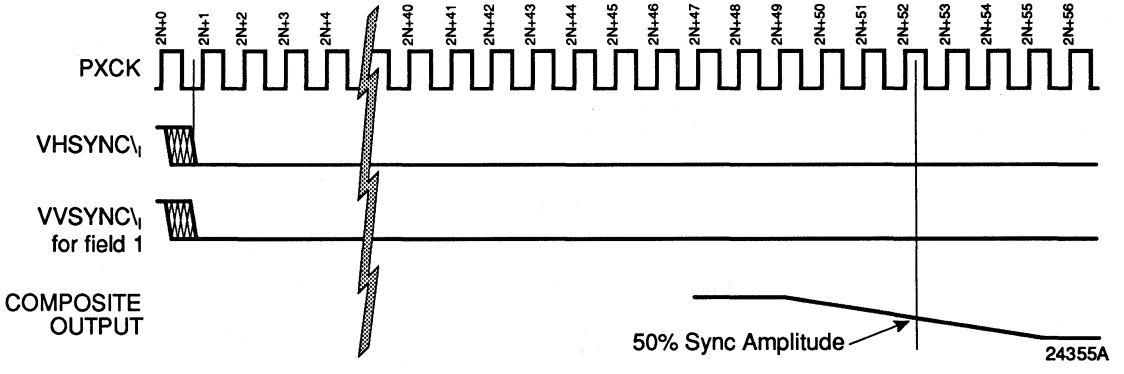
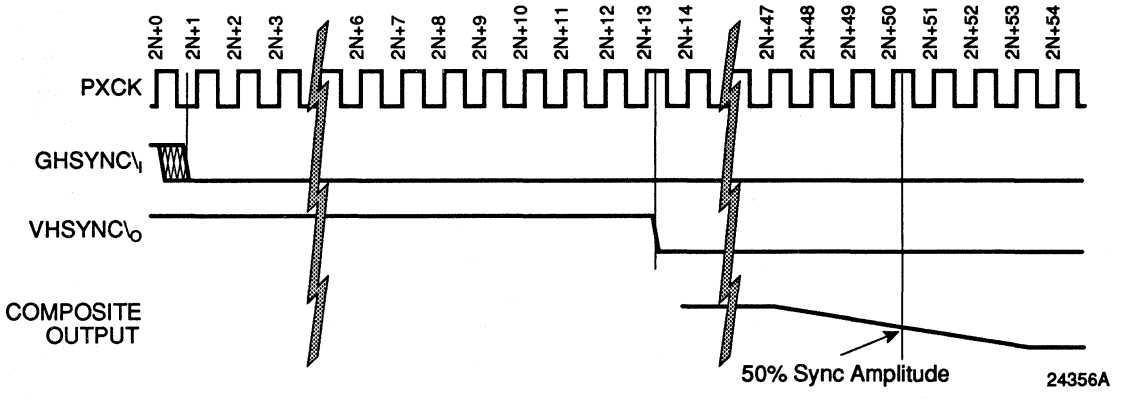


Figure 17. Genlocked Mode Timing



Genlocked Mode

In Genlocked mode, the encoder receives sync signals over the GHSYNC\ and GVSYNC\ inputs, and provides VHSYNC\ and VVSYNC\ to the host. The 50% sync amplitude point occurs 50 PXCK clocks after GHSYNC\ goes LOW, while VHSYNC\ is produced at clock 13. If GHSYNC\ is late, the front porch is lengthened, if is is early, front porch is shortened.

Pixel Data Control

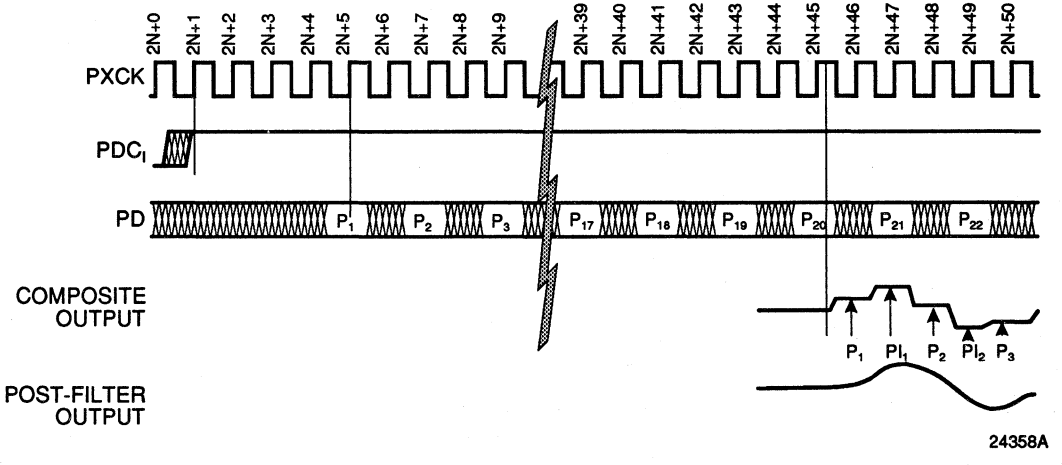
The Pixel Data Control (PDC) signal determines the active picture area. It may be an input or an output, as determined by the Interface Control Register bit 1.

The position (number of PCK cycles) of the rising edge of PDC relative to the falling edge of VHSYNC\ can be found by summing SY, BU, BR, and CBP.

External Pixel Data Control

When used as an input, PDC goes HIGH four PXCK cycles before the first valid pixel of a line is presented to the PD input port. If this signal is late

Figure 18. External Pixel Data Control



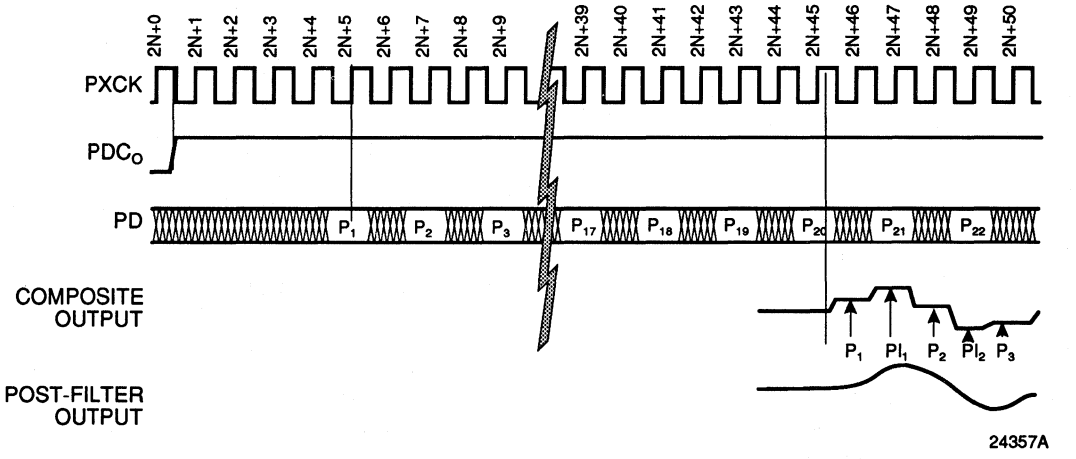
(with respect to the horizontal blanking interval programmed in the timing control registers), the Color Back Porch (CBP) will be extended. If it is early, incoming pixel data will be ignored until the end of the CBP.

Internal Pixel Data Control

When programmed as an output, PDC goes HIGH four PXCK periods prior to the end of CBP (as programmed in the horizontal timing registers) which is also four PXCK cycles prior to required input of the first pixel of a line.

Pixels produced by the encoder appear at the analog outputs (COMPOSITE, LUMA, CHROMA) 40 clocks after they are registered into the PD port. Note that the pixels enter at one-half the PXCK rate. The encoded signal passes through interpolation filters which generate intermediate output values, improving the output frequency response and greatly simplifying the external reconstruction filter. The interpolated pixels are designated PI in the diagram.

Figure 19. Internal Pixel Data Control



Layering with the TMC22190/191

The "layering" capabilities of the TMC22190/191 are powerful and flexible. Layering is a video production concept where various images or patterns are superimposed (keyed) over each other to form a final image that is the layered composite of the input images. Four layers with the following priority are defined for the TMC22190/191:

1. The DOWNSTREAM KEY layer keys over all other layers.
2. The FOREGROUND layer keys over MIDGROUND and BACKGROUND, but not over DOWNSTREAM KEY.
3. The MIDGROUND layer keys over BACKGROUND, but not over FOREGROUND or DOWNSTREAM KEY.
4. The BACKGROUND layer never keys over any other layer.

It is important not to confuse layers with sources. The TMC22190/191 can be programmed to assign any of its input sources (RGB, YC_RC_B, CVBS bus, Overlay bits) to any of the four layers.

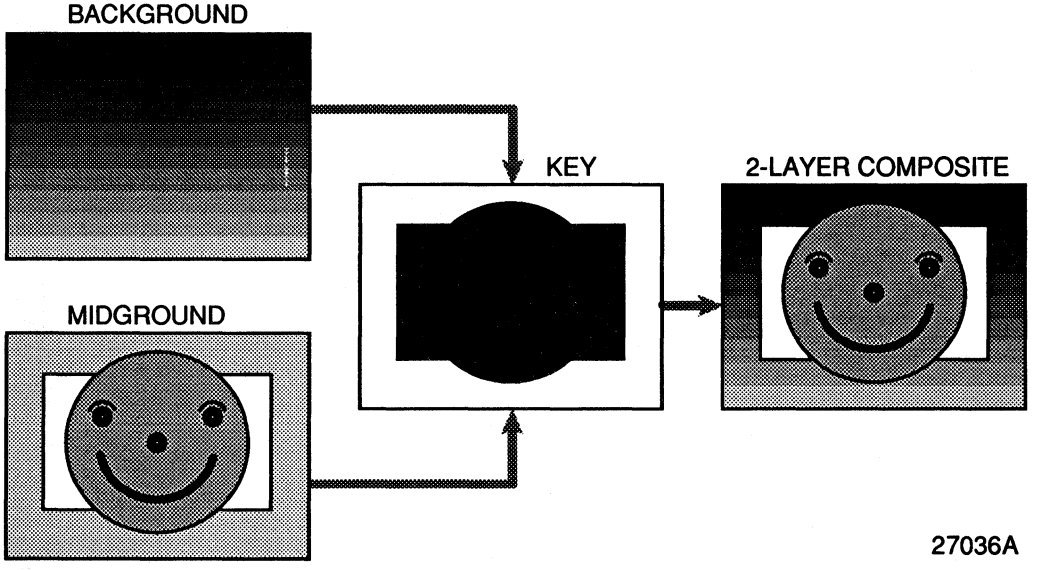
The ability to combine various video sources into a 4-layer composite image is a very powerful tool in the production of computer/live video. The TMC22190/191 performs layering operations entirely in the digital domain, enabling precise digital control.

A 4-Layer Example

For this layering example, a BACKGROUND image (Figure 20) is generated. This image comprises shaded matte levels varying from black at the top of the screen to white at the bottom. This could just as well be a color image which will be seen wherever no other image appears through the layering process.

The MIDGROUND image comprises a happy face superimposed over a white rectangle. Only the happy face and the white rectangle are of interest for this image and therefore, the portion of the image outside that area will be replaced by the BACKGROUND image when MIDGROUND is keyed over BACKGROUND. A key signal is generated on a pixel-by-pixel basis. It indicates

Figure 20. 2-Layer Image Construction



which image is active. The key signal for keying MIDGROUND over BACKGROUND is shown to the right of the MIDGROUND image. This represents a single bit signal mapped over the image. When the signal is black (logic LOW), the MIDGROUND image is active, when it is white (logic HIGH), the BACKGROUND is active.

The results of layering MIDGROUND over BACKGROUND images are shown in the 2-layer composite image Figure 20.

A FOREGROUND image comprises a shaded matte rectangle with "HI KIDS !" alpha characters in its center. This is to be superimposed over the previous 2-layer composite image. The key signal needed for superimposing FOREGROUND over other images is shown to the right of the FOREGROUND image. This represents a single bit signal mapped over the image. When the signal is black (logic LOW), the FOREGROUND image is active, when it is white (logic HIGH), the composite image is active.

A new 3-layer composite image, FOREGROUND over MIDGROUND over BACKGROUND, is shown in Figure 21.

A DOWNSTREAM KEY image comprises the white alpha characters "HAPPY FACE", and black alpha characters "Time". This is to be superimposed over the previous 3-layer composite image. The key signal needed for superimposing DOWNSTREAM KEY image over the other composite images is shown to the right. This represents a single bit signal mapped over the image. When the signal is black (logic LOW), the DOWNSTREAM KEY image is active, when it is white (logic HIGH), the previous composite image is active.

The final 4-layer composite image, DOWNSTREAM KEY over FOREGROUND over MIDGROUND over BACKGROUND, is shown in Figure 22.

In this illustration, all four source images are static (not moving). The images input to the TMC22190/191 can just as well be "live" (from video camera or VCR sources) as long as:

1. Data from those sources is in an input format that the TMC22x9x can accept, and

Figure 21. Adding a 3rd Layer

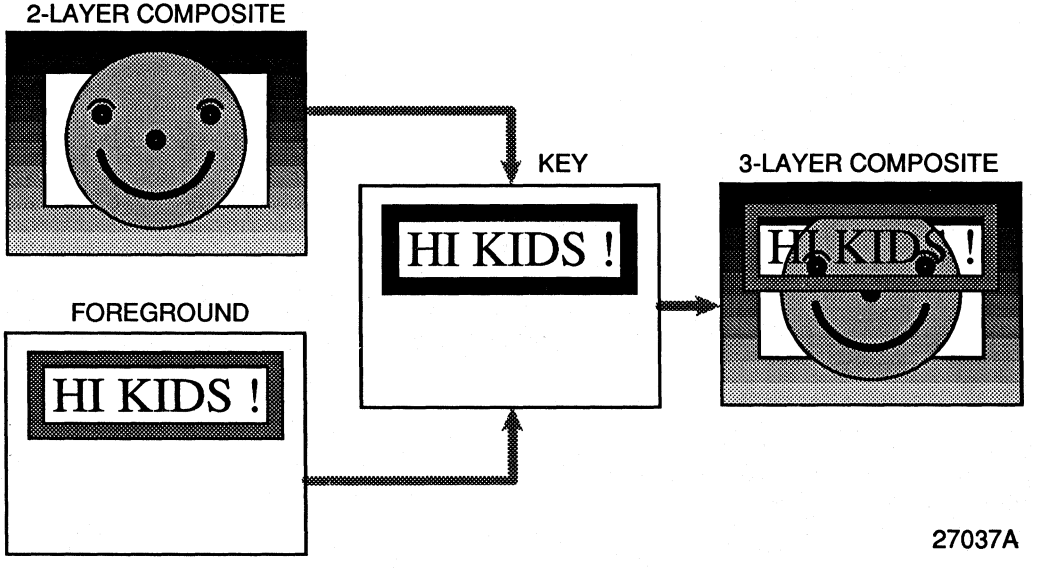
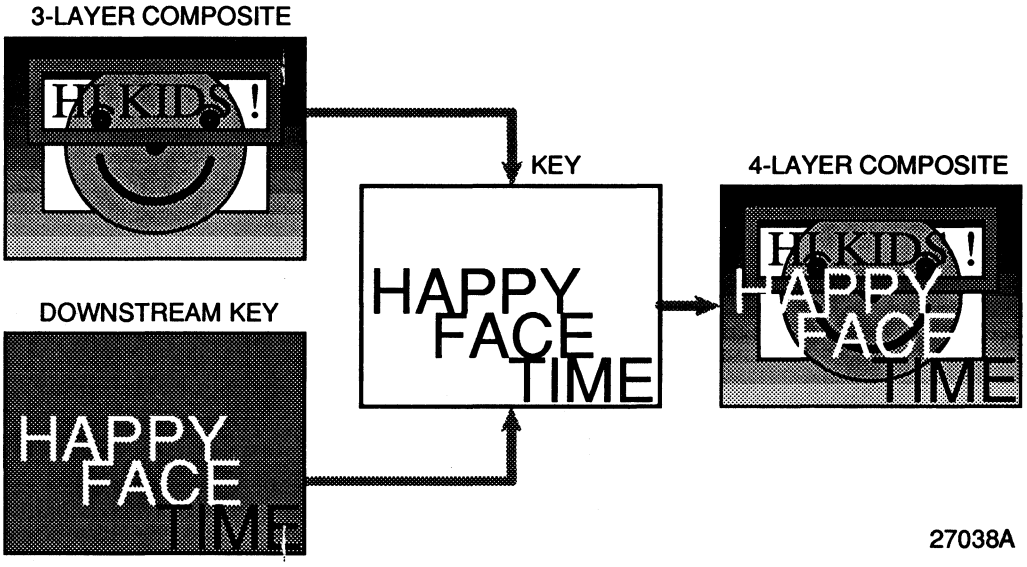


Figure 22. Adding a 4th Layer



2. The sources either synchronize the TMc22x9x (Genlock mode) or are synchronized by the TMC22x9x (Master or Slave mode).

Key signals may be generated external to the TMC22x9x (Hardware Keying) and use the KEY input pin for control. Key signals may also be generated within the TMC22x9x (Data Keying) by the comparison of input color data with color data stored in the TMC22x9x.

2-Layer Keying with the TMC22090/091

The TMC22090/091 facilitates the keying of PD port input data over the CVBS bus input data. Keying is controlled on a pixel-by-pixel basis by either the KEY input pin of the internal Data Key function. The first two layers in the previous **4-Layer Example** apply to the TMC22090/091. The result of keying is an effect where a MIDGROUND source image (i.e. Happy Face from PD data) is superimposed over a BACKGROUND source image (i.e. variable matte color from CVBS data).

Assigning Video Sources to Layers with the TMC22190/191

Digital video inputs to the TMC22190/191 (PD, CVBS, Overlay) are assigned to the four layers by choosing one of 16 modes of the Layering Control Register. OVERLAY is always keyed (switched on a pixel-by-pixel basis from active to transparent) by the OL_{4-0} inputs. OVERLAY can not be programmed to the BACKGROUND layer. The CVBS digital video bus can be assigned to any of the four layers and is keyed by the KEY input signal or internal Data Key comparators. In modes 0 thru 7, the CLUTs are not bypassed and the BYPASS\ input is ignored.

Table 15. Layer Assignments, Image Sources, and Keying Controls (22190/191)

LCR 04	BACKGROUND	MIDGROUND		FOREGROUND		DOWNSTREAM KEY	
LAYMODE	Image Source	Image Source	Keying Control	Image Source:	Keying Control:	Image Source:	Keying Control
0	PD(YC_BC_R, RGB, CI)	CVBS	KEY or Data Key	-	-	-	-
1	PD(YC_BC_R, RGB, CI)	CVBS	KEY or Data Key	OVERLAY	OL_{4-0}	-	-
2	PD(YC_BC_R, RGB, CI)	CVBS	KEY	PD(YC_BC_R, RGB, CI)	Data Key\	OVERLAY	OL_{4-0}
3	PD(YC_BC_R, RGB, CI)	CVBS	KEY	PD(YC_BC_R, RGB, CI)	Data Key	OVERLAY	OL_{4-0}
4	CVBS	OVERLAY	OL_{4-0}	PD(YC_BC_R, RGB, CI)	KEY or Data Key	-	-
5	CVBS	PD(YC_BC_R, RGB, CI)	KEY or Data Key	OVERLAY	OL_{4-0}	-	-
6	PD(YC_BC_R, RGB, CI)	CVBS	KEY	OVERLAY	OL_{4-0}	PD(YC_BC_R, RGB, CI)	Data Key\
7	PD(YC_BC_R, RGB, CI)	CVBS	KEY	OVERLAY	OL_{4-0}	PD(YC_BC_R, RGB, CI)	Data Key
8	PD(YC_BC_R, CI)	CVBS	KEY or Data Key		-	-	-
9	PD(RGB)	PD(YC_BC_R, CI)	BYPASS\	CVBS	KEY or Data Key	OVERLAY	OL_{4-0}
A	PD(RGB)	CVBS	KEY or Data Key	PD(YC_BC_R, CI)	BYPASS\	OVERLAY	OL_{4-0}
B	PD(RGB)	CVBS	KEY or Data Key	OVERLAY	OL_{4-0}	PD(YC_BC_R, CI)	BYPASS\
C	PD(RGB)	PD(YC_BC_R, CI)	BYPASS\	OVERLAY	OL_{4-0}	CVBS	KEY or Data Key
D	CVBS	PD(RGB)	KEY	PD(YC_BC_R, CI)	BYPASS\	OVERLAY	OL_{4-0}
E	CVBS	OVERLAY	OL_{4-0}	PD(RGB)	KEY	PD(YC_BC_R, CI)	BYPASS\
F	PD(RGB)	OVERLAY	OL_{4-0}	CVBS	KEY or Data Key	PD(YC_BC_R, CI)	BYPASS\

Notes:
1. For LAYMODE = 0 to 7, Pixel Data always passes through the CLUTs. FORMAT, INMODE, and the BYPASS\ pin selects the input format for PD_{23-0} according to Table 7.
2. For LAYMODE = 8 to F and BYPASS\ = HIGH, Data Key is disabled.
3. Asserting the signal listed under "Keying Control:" enables the corresponding "Signal Source:". Signals with "\" are asserted by a logic LOW.

Hardware Keying

The KEY input switches the COMPOSITE D/A converter input from the luminance and chrominance combiner output to the CVBS data bus on a pixel-by-pixel basis. This is a "soft" switch, executed over four PXCK periods to minimize out-of-band transients. Keying is accomplished in the digital composite video domain. The video signal from the CVBS bus is only present on the COMPOSITE output. The CHROMA and LUMA outputs continue to present encoded PD port data when CVBS is active.

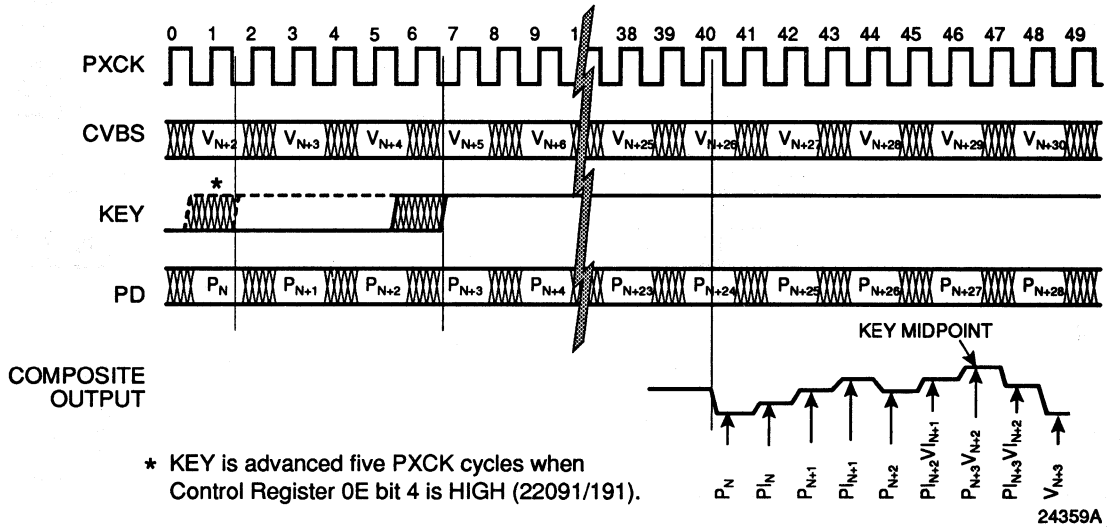
Hardware keying is enabled by the Key Control Register bit 6. Normally, keying is only effective during the Active Video portion of the waveform (as determined by the VA registers 15 and 18. That is, the Horizontal Blanking interval is generated by the encoder state machine even if the KEY signal is held HIGH through Horizontal Blanking. However, it is possible to allow digital Horizontal Blanking to be passed through from the CVBS bus to the COMPOSITE output by setting Key Control Register bit 5 HIGH. In this mode, KEY is always active, and may be exercised at will.

The KEY input is registered into the encoder just like Pixel Data is clocked into the PD port. It may be considered a 25th Pixel Data bit. It is internally pipelined, so the midpoint of the key transition occurs at the output of the pixel that was input at the same time as the KEY signal.

Data Keying

Data Keying internally generates a Key signal that acts exactly as the external KEY signal. There are three Key Value Registers 05, 06, and 07 that are matched against the input data to the three CLUTs. These tables are designated D, E, and F, because they contain different information depending on the input mode selected:

Figure 23. Hardware Keying



The key registers may be individually enabled using bits 3,2,1 of the Key Control Register. Bit 4 of the same register enables/disables data Keying in its entirety. Data Keying and Hardware Keying are logically ORed: when both are enabled, either one will result in a key switch to the CVBS channel.

The key comparison is based on the input data to the CLUTs. When operating in color-index mode, all three CLUTs receive the same input value, so any one of the three registers is sufficient to identify a key value. The outputs of all enabled key registers are ANDed to produce the KEY signal. If more than one key register are enabled and their key values are not identical, no key will be generated.

Table 16. Table D, E, F Contents

Mode	Table D	Table E	Table F
RGB	Red	Green	Blue
GBR	Green	Blue	Red
YC_BC_R	Y	C_B	C_R
CI	CI	CI	CI

Genlock Interface

The TMC22x9x can bring digital composite video into its CVBS port, accompanied by separate horizontal and vertical sync signals. It has been designed to couple tightly with the companion TMC22070 Genlocking Video Digitizer, but other sources may use this port as well.

Digital composite video is in standard 8-bit binary format at a PXCK / 2 rate. Synchronization with the internal PXCK / 2 is established by the phasing of the GHSYNC\ input.

Subcarrier frequency and phase data are received by the encoder over the CVBS bus as 4-bit nibbles on $CVBS_{3-0}$ during the horizontal sync period. Field identification is also required for the TMC22x9x internal sync generator. The 14th nibble of the sequence contains no relevant data. The TMC22070 provides these data - the Genlock Reference Signal (GRS).

Figure 24. Data Keying

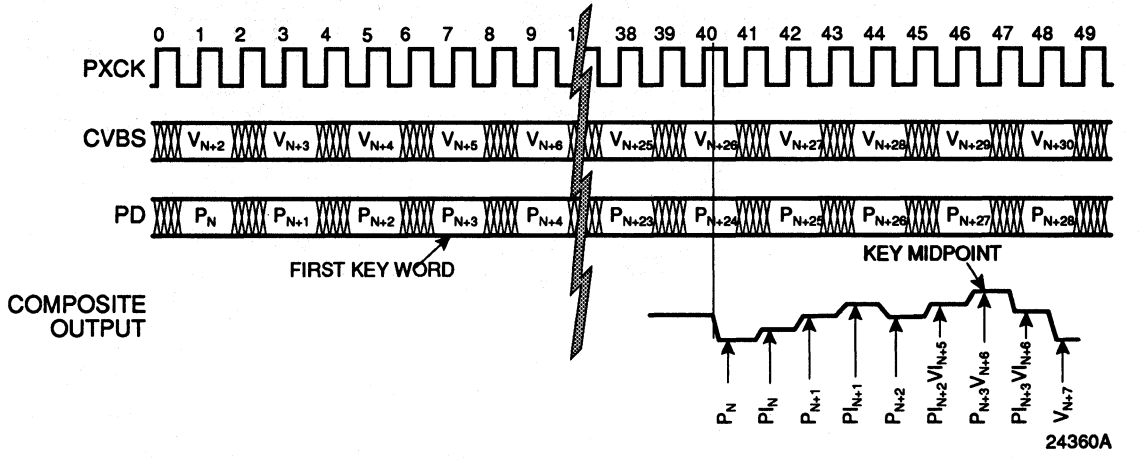


Figure 25. Genlock Interface Timing

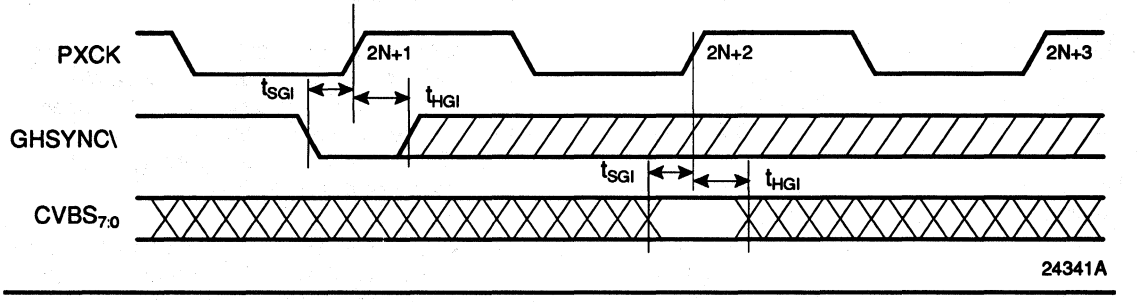
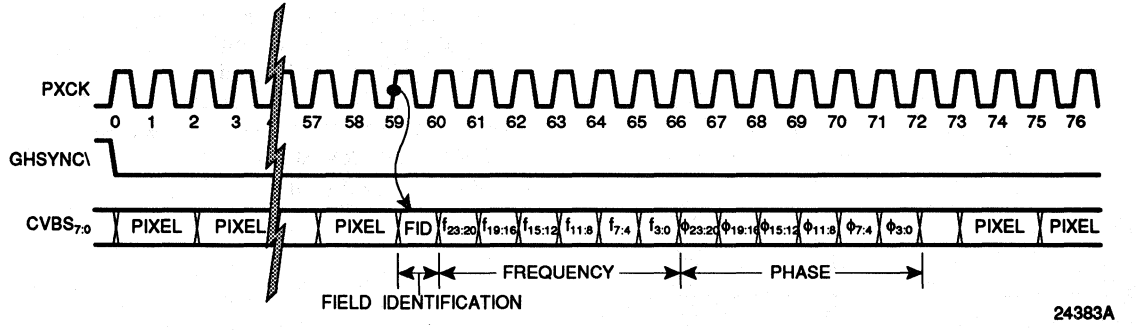


Figure 26. Frequency/Phase Data Transfer



Filtering

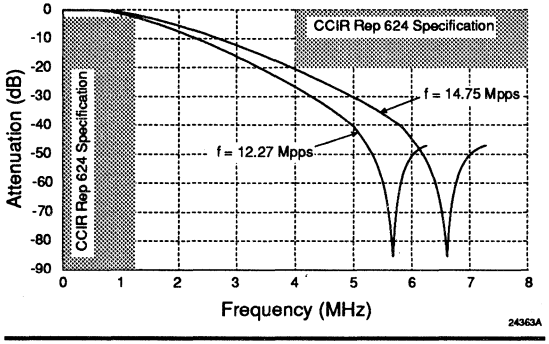
The TMC22x9x incorporates internal digital filters to establish appropriate bandwidths and simplify external analog filter designs.

Color-Difference Low-Pass Filters

The chrominance portion of a composite video signal must be sufficiently bandlimited to avoid cross-color and cross-luminance distortion, and to preclude exceeding the allowable bandwidth of a video channel.

The color-difference low-pass filters on the TMC22x9x establish chrominance bandwidths which meet the specifications outlined in CCIR Report 624-3, Table II, Item 2.6, for system I over a range of pixel rates from 12.27 Mpps to 14.75 Mpps. Equal bandwidth is established for both color-difference channels.

Figure 27. Color-Difference Low-Pass Filter Response



Interpolation Filters

The Chroma Modulator output and the luminance data path are digitally filtered with sharp-cutoff low-pass interpolation filters. These filters ensure that aliased subcarrier, chrominance, and luminance frequencies are sufficiently suppressed in the frequency band above base-band video and below the pixel frequency ($f_S/4$ to $3f_S/4$, where f_S is the PXCK frequency).

Since these are fixed-coefficient digital filters, their filter characteristics depend upon clock rate. Figures 25 and 26 show the frequency response for two pixel rates, 12.27 MHz and 14.75 MHz.

Figure 28. Chroma Modulator and Luminance Interpolation Filter Full Spectrum Response

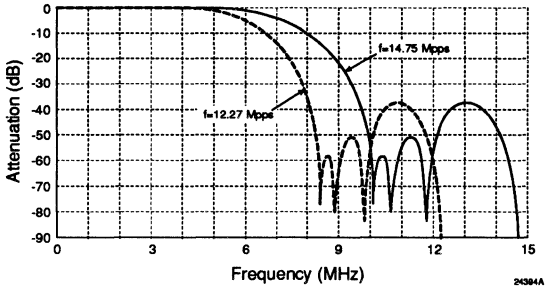
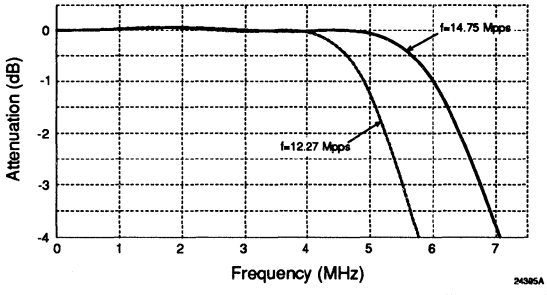


Figure 29. Chroma Modulator and Luminance Interpolation Filter Passband Detail



Virtually all digital-to-analog reconstruction systems exhibit a high frequency roll-off as a result of the zero-order hold characteristic of classic D/A converters. This response is commonly referred to as a sin(x)/x response. It is a function of the sampling rate of the output D/A.

The TMC22x9x's digital interpolation filters convert the data stream to a sample rate of twice the pixel rate. This results in much less high frequency sin(x)/x rolloff and the output spectrum between $f_S/4$ and $3f_S/4$ contains very little energy. Since there is so little signal energy in this frequency band, the demands placed on the output reconstruction filter are greatly reduced. The

output filter needs to be flat to $f_S/4$ and have good rejection at $3f_S/4$. The relaxed requirements greatly simplify the design of a filter with good phase response and low group delay distortion. A small amount of peaking may be used to compensate residual sin(x)/x rolloff.

Figure 30. Sin(x)/x Response At 1x Pixel-Rate Conversion

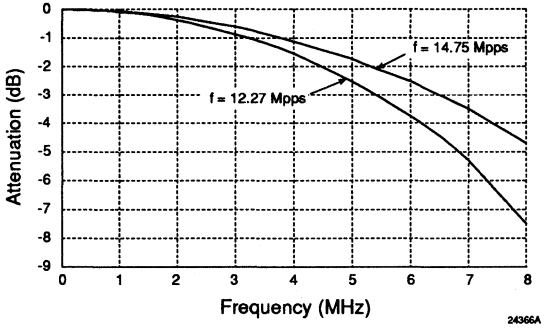
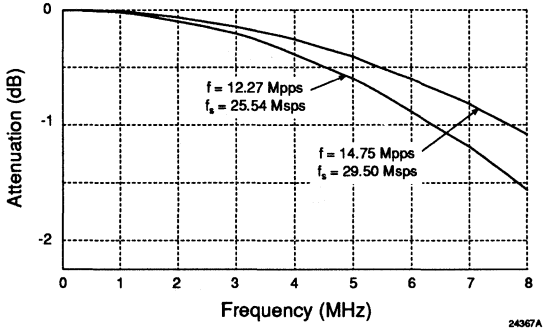


Figure 31. Sin(x)/x Response At 2X Pixel-Rate Conversion



JTAG Test Interface

The JTAG test port accesses registers at every digital I/O pin except the JTAG test port pins. Table 17 shows the sequence of the test registers. The register number (Reg) indicates the order in which the register data is loaded and read (Reg 1 is loaded and read first, therefore it is at the end of the serial path). The scan path is 59 registers long. The six TEST pins of the TMC22090/091 function as JTAG registers.

The JTAG port is a 4-line interface, following IEEE Std. 1149.1-1990 specifications. The Test Data Input (TDI) and Test Mode Select (TMS) inputs are referred to the rising edge of the Test ClocK (TCK) input. The Test Data Output (TDO) is referred to the falling edge of TCK.

Table 17. JTAG Interface Connections

Reg	Pin	Signal	Reg	Pin	Signal	Reg	Pin	Signal
1	28	BYPASS\ (TEST)	21	62	PD_{13}	41	2	$CVBS_1$
2	29	OL_4 (TEST)	22	63	PD_{12}	42	3	$CVBS_0$
3	44	$CVBS_7$	23	66	PD_{11}	43	4	KEY
4	45	$CVBS_6$	24	67	PD_{10}	44	5	RESET\
5	46	$CVBS_5$	25	68	PD_9	45	6	CS\
6	47	$CVBS_4$	26	69	PD_8	46	7	R/W\
7	48	OL_3 (TEST)	27	70	PD_7	47	8	A_1
8	49	OL_2 (TEST)	28	71	PD_6	48	9	A_0
9	50	OL_1 (TEST)	29	72	PD_5	49	11	PDC
10	51	OL_0 (TEST)	30	73	PD_4	50	12	VHSYNC\
11	52	PD_{23}	31	74	PD_3	51	13	VVSYNC\
12	53	PD_{22}	32	75	PD_2	52	14	D_7
13	54	PD_{21}	33	76	PD_1	53	15	D_6
14	55	PD_{20}	34	77	PD_0	54	16	D_5
15	56	PD_{19}	35	78	LDV	55	17	D_4
16	57	PD_{18}	36	79	PXCK	56	18	D_3
17	58	PD_{17}	37	82	GVSYNC\	57	19	D_2
18	59	PD_{16}	38	83	GHSYNC\	58	20	D_1
19	60	PD_{15}	39	84	$CVBS_3$	59	21	D_0
20	61	PD_{14}	40	1	$CVBS_2$			

Figure 32. JTAG Test Port Timing

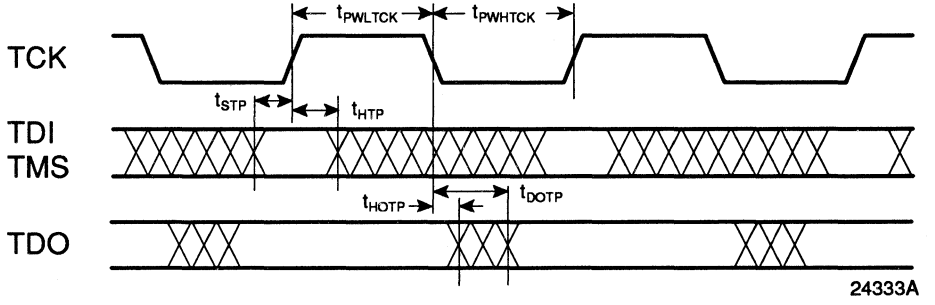


Figure 33. Equivalent Analog Input Circuit

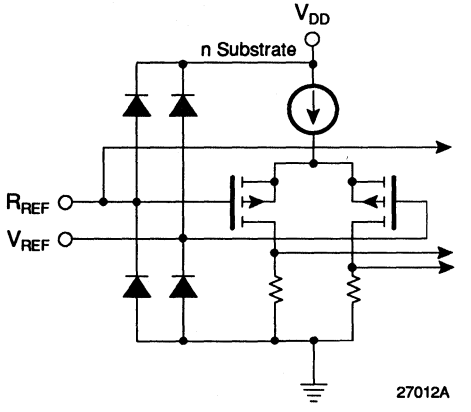


Figure 34. Equivalent Analog Output Circuit

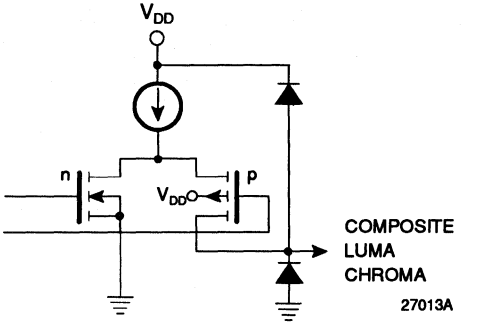


Figure 35. Equivalent Digital Input Circuit

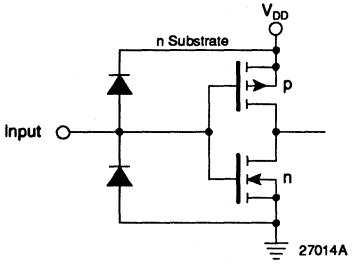


Figure 36. Equivalent Digital Output Circuit

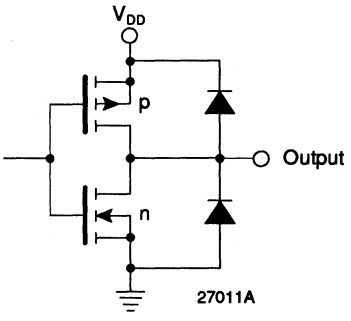
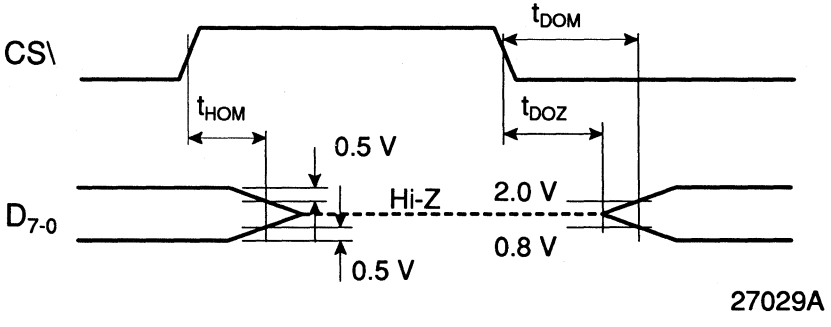


Figure 37. Transition Levels for Three-State Measurements



Absolute Maximum Ratings (beyond which the device may be damaged)

Power Supply Voltage ..... -0.5 to +7.0V

Digital Inputs
- Applied Voltage[2] ..... -0.5 to V_{DD}+0.5V
- Forced Current[3,4] ..... -20.0 to 20.0 mA

Digital Outputs
- Applied Voltage[2] ..... -0.5 to V_{DD}+0.5V
- Forced Current[3,4] ..... -20.0 to 20.0mA
- Short Circuit Duration (Single output in HIGH state to GND) ..... 1 second

Analog Output Short Circuit Duration (Single output to GND) ..... infinite

Temperature
- Operating, case ..... -60 to +130°C
- Operating, Junction, Plastic package ..... +150°C
- Lead, soldering (10 seconds) ..... +300°C
- Vapor phase soldering (1 minute) ..... +220°C
- Storage ..... -65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Compatible Inputs, all but PXCK	2.0		V_{DD}	V
	TTL Compatible Input PXCK	2.5		V_{DD}	V
	CMOS Compatible Inputs	$(2/3)V_{DD}$		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				
	TTL Compatible Inputs	GND		0.8	V
	CMOS Compatible Inputs	GND		$(1/3)V_{DD}$	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current ($I_{REF} = V_{REF} / R_{REF}$, flowing out of the R_{REF} pin)	2.1	3.15	4.4	mA
R_{REF}	Reference Resistor, V_{REF} = Nom.	281	392	588	Ω
R_{OUT}	Total Output Load Resistance		37.5		Ω
T_A	Ambient Temperature, Still Air	0		70	°C
Pixel Interface					
f_{PXL}	Pixel Rate	12.27		15	Mpps
f_{PXCK}	Master Clock Rate, 2x pixel rate	24.54		30	MHz
t_{PWHPX}	PXCK Pulse Width, HIGH	10			ns
t_{PWLPX}	PXCK Pulse Width, LOW	10			ns
	For PD,VVSYNC\,VHSYNC\,PDC,KEY				
t_{SP}	Setup Time	12			ns
t_{HP}	Hold Time, PD and KEY	0			ns
t_{HP}	Hold Time, PDC, VHSYNC\, VVSYNC\	5			ns
t_{XL}	Delay Time, LDV	10			ns
t_{PWHLDV}	LDV Pulse Width, HIGH	15			ns
t_{PWLLDV}	LDV Pulse Width, LOW	10			ns

Operating Conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
t_{PWLVH}	VHSYNC\ Pulse Width, LOW	6		15	PXCK periods
t_{PWHVV}	VVSYNC\ Pulse Width, LOW	0.5		3	H
Genlock Interface					
t_{SGI}	Setup Time, GHSYNC\,GVSYNC\,CVBS	10			ns
t_{HGI}	Hold Time, GHSYNC\, GVSYNC\,CVBS	0			ns
Microprocessor Interface					
t_{PWLCS}	CS\ Pulse Width, LOW, w/ KEY Reg.	95			ns
t_{PWLCS}	CS\ Pulse Width, LOW, w/o KEY Reg.	55			ns
t_{PWHCS}	CS\ Pulse Width, HIGH	30			ns
t_{SA}	Address Setup Time	10			ns
t_{HA}	Address Hold Time	0			ns
t_{SD}	Data Setup Time (write)	15			ns
t_{HD}	Data Hold Time (write)	0			ns
t_{SR}	Reset Setup Time	24			ns
t_{HR}	Reset Hold Time	2			ns
JTAG Interface					
f_{TCK}	Test Clock (TCK) Rate			20	MHz
t_{PWLTCK}	TCK Pulse Width, LOW	25			ns
t_{PWHTCK}	TCK Pulse Width, HIGH	10			ns
t_{STP}	Test Port Setup Time, TDI, TMS	10			ns
t_{HTP}	Test Port Hold Time, TDI, TMS	3			ns

Note: 1. Timing reference points are at the 50% level.

Electrical Characteristics

Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
I_{DD}	Power Supply Current[1]	V_{DD}=Max,f_{PXCK}=30MHz		300	350	mA
I_{DDQ}	Power Supply Current[1] (D/A disabled)	V_{DD}=Max,f_{PXCK}=30MHz			90	mA
V_{RO}	Voltage Reference Output		0.988	1.235	1.482	V
I_{BR}	Input Bias Current, V_{REF}	V_{REF} = Nom		100		µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = 4.0V			10	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0.4V			-10	µA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = Max			0.4	V
I_{OZH}	Hi-Z Leakage current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			10	µA
I_{OZL}	Hi-Z Leakage current, LOW	V_{DD} = Max, V_{IN} = GND			-10	µA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		4	10	pF
C_O	Digital Output Capacitance	T_A = 25°C, f = 1MHz		10		pF
V_{OC}	Video Output Compliance Voltage		-0.3		2.0	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	I_{OUT} = 0 mA, f = 1 MHz		15	25	pF

Note 1. Typical I_{DD} with V_{DD}=+5.0 Volts and T_A=25°C, Maximum I_{DD} with V_{DD}=+5.25 Volts and T_A=0°C.

Switching Characteristics

Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
PIPES	Pipeline Delay[3]	PD to Analog Out	44	44	44	PXCK periods
t_{DOZ}	Output Delay, CS\ to low-Z		8		23	ns
t_{DOM}	Output Delay, CS\ to Data Valid[4]	with KEY Register			125	ns
t_{DOM}	Output Delay, CS\ to Data Valid[4]	without KEY Register			100	ns
t_{HOM}	Output Hold Time, CS\ to hi-Z		10			ns
t_{DOTP}	Output Delay, TCK to TDO Valid				30	ns
t_{HOTP}	Output Hold Time, TCK to TDO Valid			5		ns
t_{DOS}	Output Delay	PXCK to VHSYNC\, VVSYNC\, PDC			25	ns
t_R	D/A Output Current Risetime	10% to 90% of full-scale		2		ns
t_F	D/A Output Current Falltime	90% to 10% of full-scale		2		ns
t_{DOV}	Analog Output Delay			20		ns

Notes:
1. Timing reference points are at the 50% level.
2. Analog C_{LOAD} <10 pF, D_{7-0} load <40 pF.
3. Pipeline delay, with respect to PXCK, is a function of the phase relationship between the internally generated PCK (PXCK/2) and PXCK, as established by the hardware reset).
4. t_{DOM} (without KEY Register) = 1 PXCK + 54 ns = 100 ns worst-case at PXCK=24.54 MHz.

System Performance Characteristics

Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
RES	D/A Converter Resolution		10	10	10	Bits
E_{LI} E_{LD}	Integral Linearity Error Differential Linearity Error				0.25 0.15	% %
E_G	Gain Error				±5	% FS
dp dg	Differential Phase Differential Gain	PXCK = 24.54 MHz,40 IRE Ramp[3] PXCK = 24.54 MHz,40 IRE Ramp[3]		0.5 0.9		degree %
SKEW	CHROMA to LUMA Output Skew			0	1	ns
PSRR	Power Supply Rejection Ratio	C_{COMP}=0.1 µF, f=1kHz		0.5		%/%ΔV_{DD}

Notes
1. TTL input levels are 0.0 and 3.0 Volts, 10%-90% rise and fall times <3 ns.
2. Analog C_{LOAD} <10 pF, D_{7-0} load <40 pF.
3. NTSC

Figure 38. NTSC Vectors

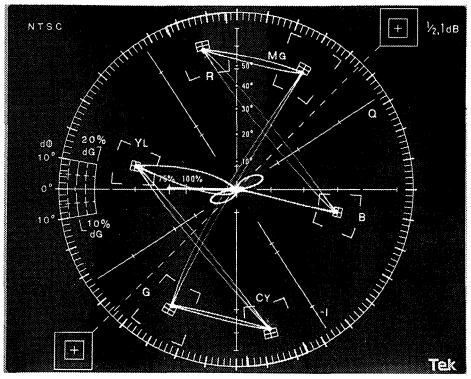


Figure 39. NTSC Color Bars Waveform

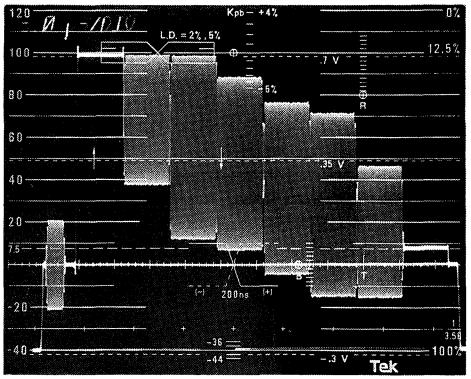


Figure 40. NTSC Horizontal Blanking Interval

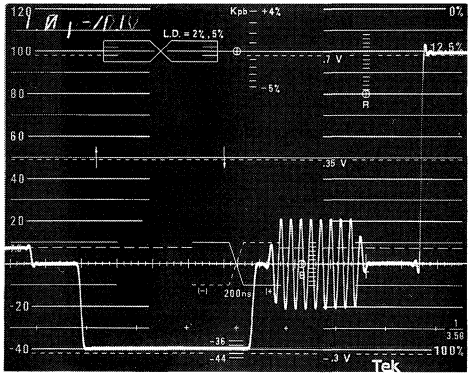


Figure 41. NTSC Vertical Blanking Interval

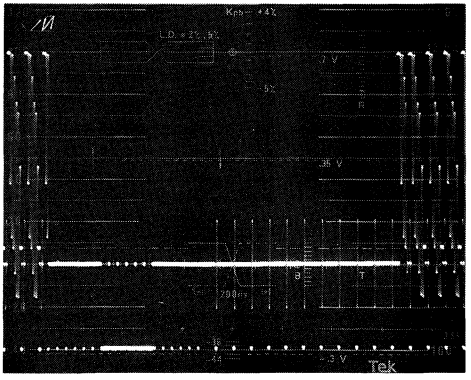


Figure 42. NTSC Differential Gain

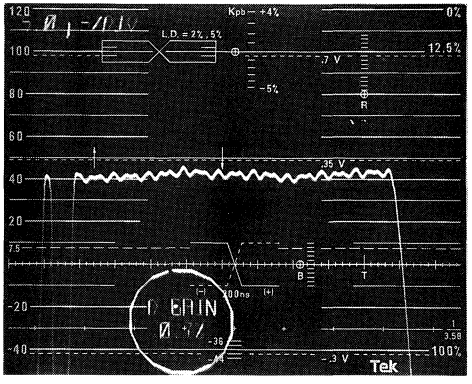
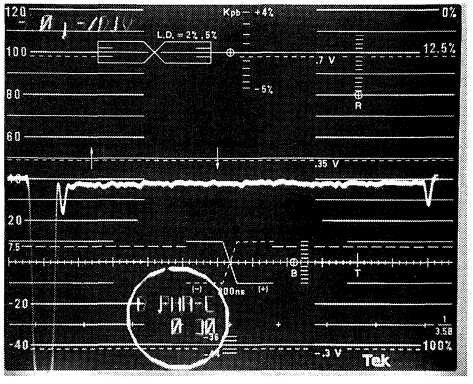


Figure 43. NTSC Differential Phase



Multimedia

Figure 44. PAL Vectors

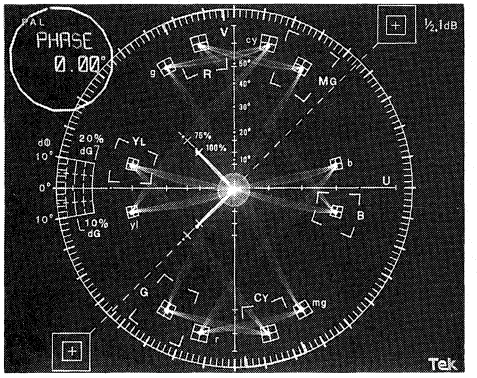


Figure 45. PAL Color Bars Waveform

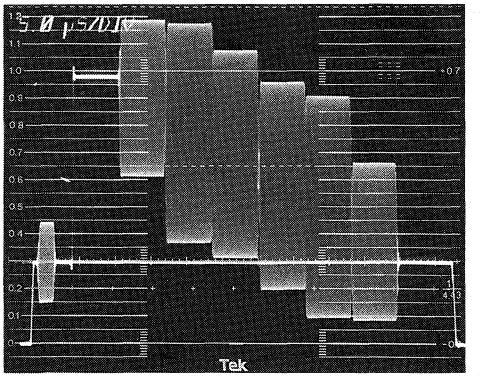


Figure 46. PAL Horizontal Blanking Interval

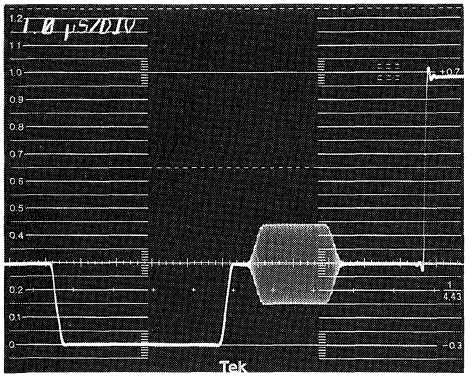


Figure 47. PAL Vertical Blanking Interval

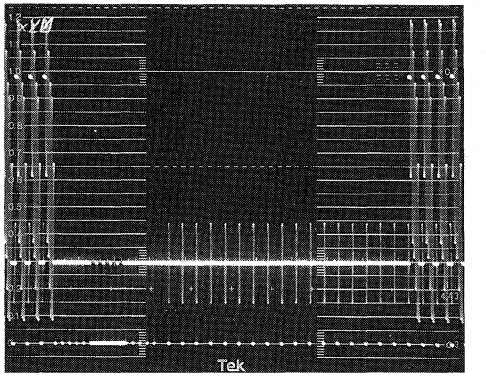


Figure 48. PAL Differential Gain

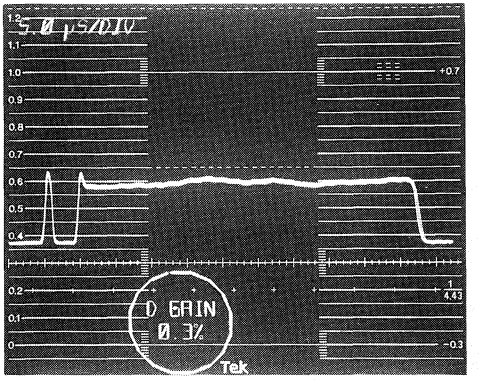


Figure 49. PAL Differential Phase

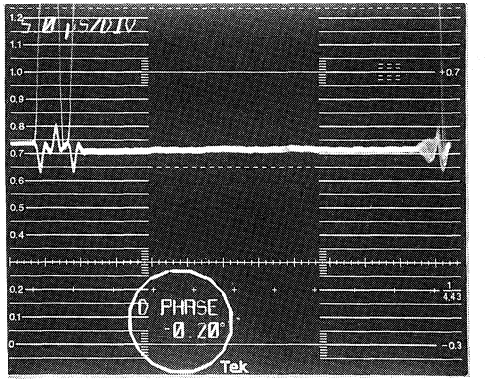


Figure 50. Color Bar Luminance

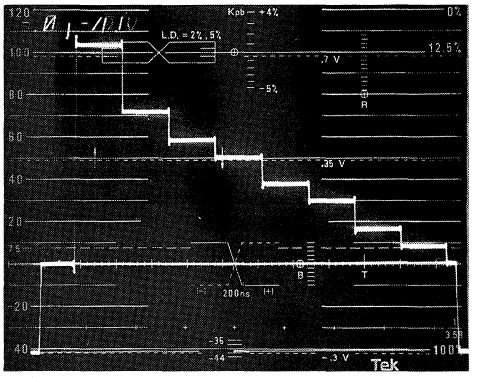


Figure 51. Color Bar Chrominance

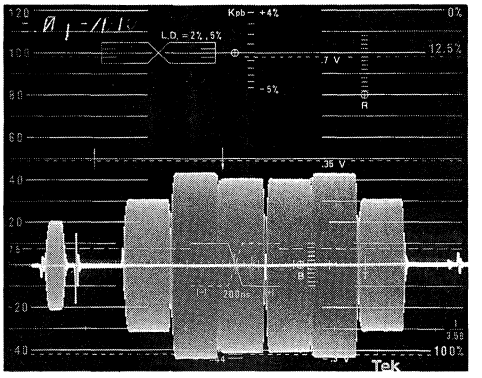


Figure 52. Short Time Distortion

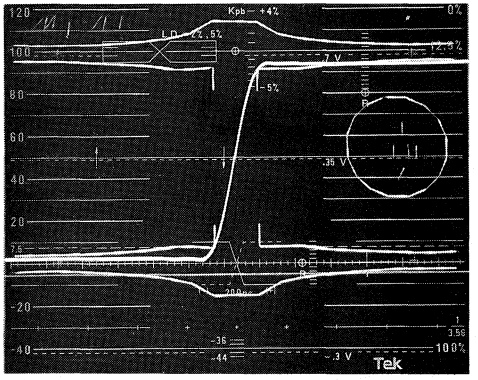


Figure 53. K Factor

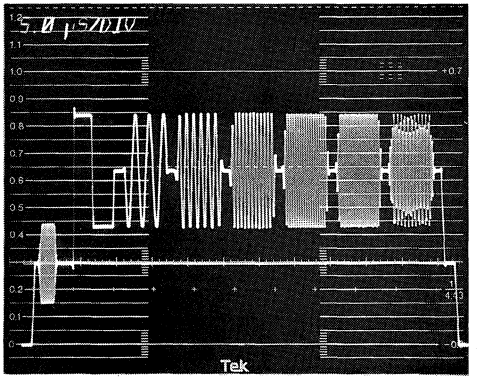


Figure 54. NTSC Multiburst

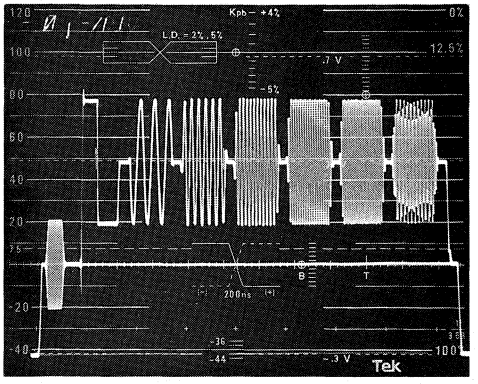


Figure 55. PAL Multiburst

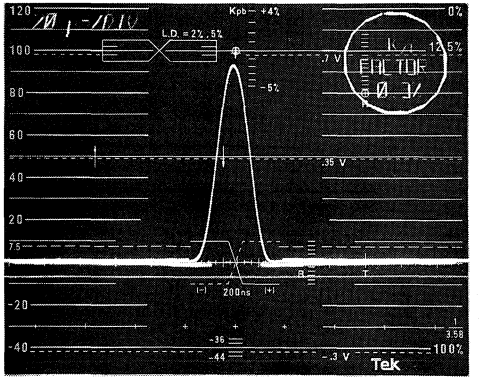
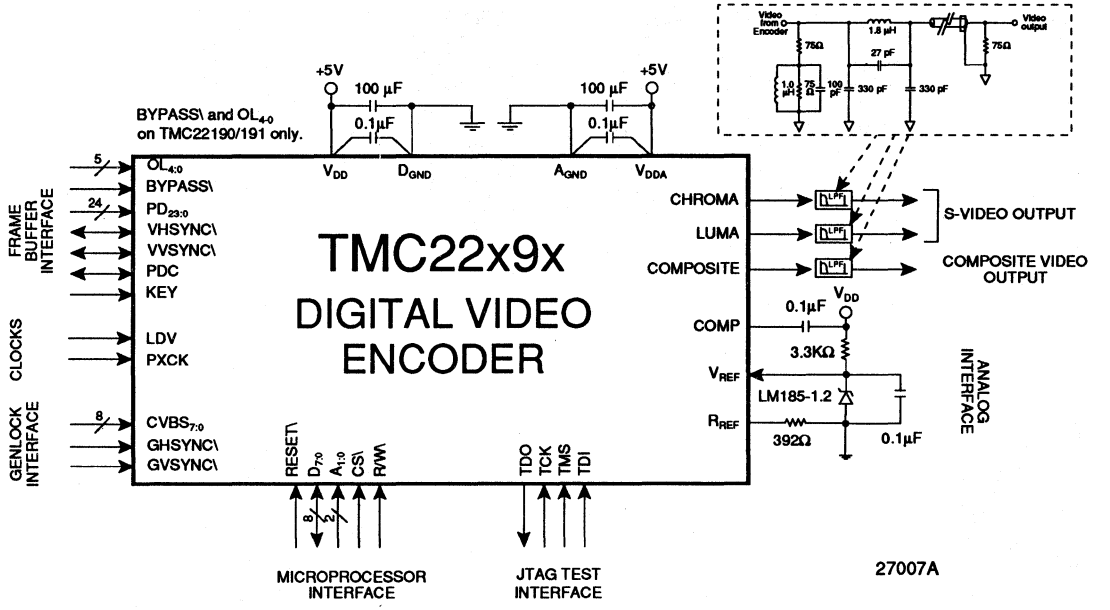


Figure 56. Recommended Interface Circuit



Application Notes

The TMC22x9x is a complex mixed-signal VLSI circuit. It handles TTL digital signals at clock rates of up to 30 MHz while producing analog outputs with a resolution of less than a millivolt. To maximize performance it is important to provide the product with a quiet operating environment.

References

The circuit shown provides a stable external 1.235V voltage reference to the TMC22x9x. To use the internal voltage reference source, simply leave the V_{REF} pin unconnected except for the 0.1 µF capacitor to ground. The accuracy the internal voltage reference is approximately ±20%. This variation can be overcome by varying the R_{REF} resistor to get desired video output levels. It is recommended that a simple voltage divider from the power supply NOT be used, as any variations in power supply voltage would appear directly on the video outputs. The reference bandwidth is limited by the 0.1µF capacitor on the COMP pin, but low frequency signals (eg 60 Hz, 20 KHz power supply noise) will be passed through to the outputs.

Filtering

An inexpensive low-pass output filter is shown in Figure 57. This filter is located in the video signal path just after the COMPOSITE, LUMA, and CHROMA outputs of the TMC22x9x. The TMC22x9x has been designed to output adequate video levels to overcome the insertion loss of output filters. V_{REF} and R_{REF} may be varied to make up for filter loss. Since S-VIDEO comprises separate and simultaneous luminance and chrominance, it is important that the filters used on CHROMA and LUMA have identical group delay.

Figure 57. Recommended Output Reconstruction Filter

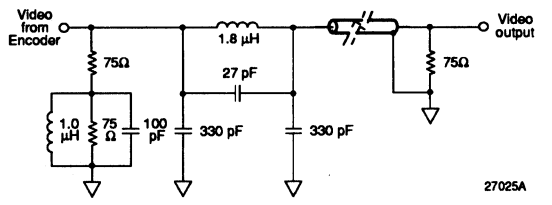
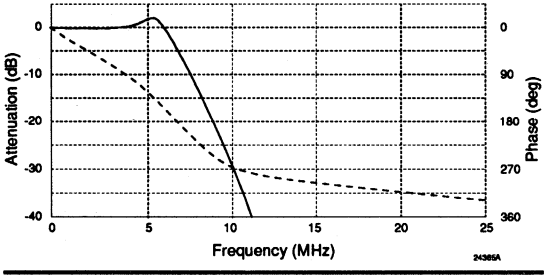


Figure 58. Response of Recommended Output Filter



Interface to the TMC22070 Genlocking Video Digitizer

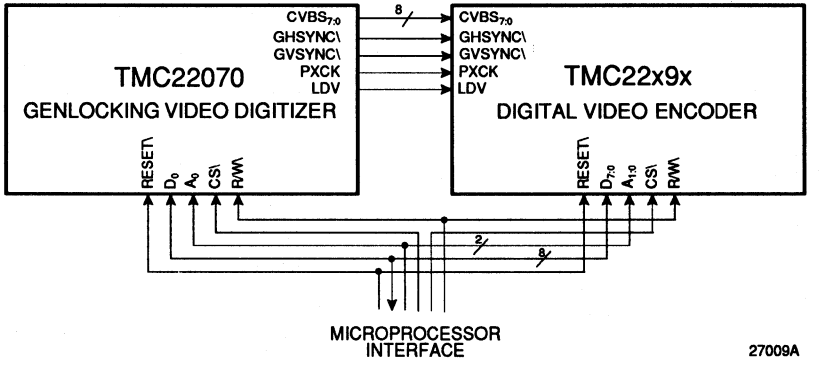
The TMC22x9x Digital Video Encoder has been designed to directly interface to the TMC22070 Genlocking Video Digitizer. The TMC22070 is the source for TMC22070 input signals $CVBS_{7-0}$, GHSYNC\, GVSYNC\, and PXCK as shown in Figure 59. These signals directly connect to the TMC22190/191. The microprocessor interface for TMC22x9x and TMC22070 are identical. All W/R\, RESET\, data and address bus signals from the host microprocessor are shared by the TMC22x9x and TMC22070. Only CS\ and INT\ signals are separately driven from the microprocessor bus.

Grounding Strategy

The TMC22x9x has distinctly separate analog and digital circuits. To minimize digital crosstalk into the analog signals, the power supplies and grounds are provided over separate pins (V_{DD} and D_{GND} are digital power supply pins; V_{DDA} and A_{GND} are analog supplies). In general, the best results are obtained by tying all grounds to a solid, low-impedance ground plane. Power supply pins should be individually decoupled at the pin. Power supply noise isolation may be provided between analog and digital supplies via a series inductor.

Another approach calls for separating analog and digital ground. While some systems may benefit from this strategy, keep in mind that the analog and digital grounds must be kept within 0.5V of each other at all times.

Figure 59. TMC22x9x-to-TMC22070 Interface Circuit



Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor picture quality. Consider the following suggestions when doing the layout:

1. Keep analog traces (COMP, V_{REF}, R_{REF}, CHROMA, LUMA, COMPOSITE) as short and far from all digital signals as possible. The TMC22x9x should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC22x9x should be separate from that which supplies other digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC22x9x is the same for the system's digital circuitry, power to the TMC22x9x should be filtered with ferrite beads and 0.1µF capacitors to reduce noise.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should be very short.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. For best results, use 0.1µF capacitors in parallel with 0.01µF capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If there is dedicated digital power plane, it should not overlap the TMC22x9x footprint, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC22x9x and its related analog circuitry can have an adverse effect on performance.

6. The PXCK should be handled carefully. Jitter and noise on this clock or its ground reference will translate to noise on the video outputs. Terminate the clock line carefully to eliminate overshoot and ringing.

Microprocessor I/O Operations

Various CLUT Read/Write operations are shown in Table 18. Each step in the table requires a CS\ pulse (falling edge followed by a rising edge) to execute.

For Write operations, R/W\ and A_{1-0} must conform to setup and hold timing with respect to the falling edge of CS\. D_{7-0} must meet setup and hold timing with respect to the rising edge of CS\. These timing relationships are illustrated in Figure 11. When writing data into an internal register (i.e. CLUT Address Register) an extra CS\ falling edge is required to transfer the input data to that register. This requirement is usually accomplished by executing the next step in the sequence. If there is no planned next step in the sequence, executing a Control Register Read step will meet the requirement and terminate the sequence.

For Read operations, R/W\ and A_{1-0} must conform to setup and hold timing with respect to the falling edge of CS\. Read data on D_{7-0} is initiated by the falling edge of CS\ and terminated by the rising edge of CS\ as shown in Figure 12. When reading Control Registers, valid data appears t_{DOM} after the falling edge of CS\. When reading CLUT locations, an extra CLUT Read step is needed to set up the CLUT Read sequence. This is accomplished in the table by executing an extra CLUT Read step just before the CLUT Read sequence which returns successive d, e, and f data. CLUT Read sequences must be terminated an extra CS\ falling edge. This requirement is usually accomplished by executing the next I/O step. If there is no planned next step in the sequence, executing a Control Register Read step will meet the requirement and terminate the sequence.

Table 18. CLUT Read/Write Sequences

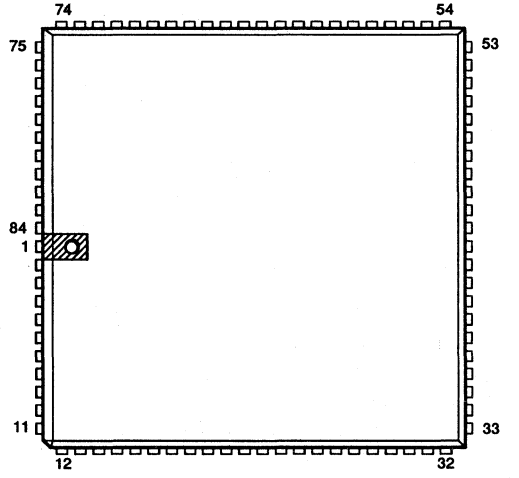
Step	R/W\	A_{1-0}	D_{7-0}	Function
				Write Entire CLUT Starting at Address 00
1	0	01	00	Write 00 into CLUT Address Register.
2	0	11	d1	d1 written into D, CLUT address 00.
3	0	11	e1	e1 written into E, CLUT address 00.
4	0	11	f1	f1 written into F, CLUT address 00.
.	..	..	..	repeat steps 3,4,5 until CLUT is full.
767	0	11	d256	d256 written into D, CLUT address FF.
768	0	11	e256	e256 written into E, CLUT address FF.
769	0	11	f256	f256 written into F, CLUT address FF.
770	1	00	xx	Sequence termination.
				Write CLUT Location addr
1	0	01	addr	Write addr into the CLUT Address Register.
2	0	11	d1	d1 written into D, CLUT address addr.
3	0	11	e1	e1 written into E, CLUT address addr.
4	0	11	f1	f1 written into F, CLUT address addr.
5	1	00	xx	Sequence termination.
				Read CLUT Location addr
1	0	01	addr	Write addr into the CLUT Address Register.
2	1	11	xx	Set up for CLUT Read sequence.
3	1	11	d1	d1 read from D, CLUT address addr.
4	1	11	e1	e1 read from E, CLUT address addr.
5	1	11	f1	f1 read from F, CLUT address addr.
6	1	00	xx	Sequence termination.

Step	R/W\	A_{1-0}	D_{7-0}	Function
				Read CLUT Address Register Then Write
1	1	01	addr	Read CLUT Address Register.
2	0	11	d1	d1 written into D, CLUT address addr.
3	0	11	e1	e1 written into E, CLUT address addr.
4	0	11	f1	f1 written into F, CLUT address addr.
5	1	01	addr+1	Read CLUT Address Register. (terminates Write sequence)
6	0	11	d2	d2 written into D, CLUT address addr+1.
7	0	11	e2	e2 written into E, CLUT address addr+1.
8	0	11	f2	f2 written into F, CLUT address addr+1.
9	1	00	xx	Sequence termination.
				Read/Modify/Write CLUT Location addr
1	0	01	addr	Write addr into the CLUT Address Register.
2	1	11	xx	Set up for CLUT Read.
3	1	11	d1	d1 read from D, CLUT address addr.
4	1	11	e1	e1 read from E, CLUT address addr.
5	1	11	f1	f1 read from F, CLUT address addr.
.	.	..	..	System Modifies d1, e1, f1 to d1', e1', f1'.
6	0	01	addr	Write addr into the CLUT Address Register. (terminates Read sequence)
7	0	11	d1'	d1' written into D, CLUT address addr.
8	0	11	e1'	e1' written into E, CLUT address addr.
9	0	11	f1'	f1' written into F, CLUT address addr.
10	1	00	xx	Sequence termination.

Table 19. Pin Assignments for 84-lead PLCC Package (R0)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	$CVBS_2$	22	TDO	43	V_{DDA}	64	V_{DD}
2	$CVBS_1$	23	TCK	44	$CVBS_7$	65	D_{GND}
3	$CVBS_0$	24	TMS	45	$CVBS_6$	66	PD_{11}
4	KEY	25	TDI	46	$CVBS_5$	67	PD_{10}
5	RESET\	26	D_{GND}	47	$CVBS_4$	68	PD_9
6	CS\	27	V_{DD}	48	OL_3(TEST)	69	PD_8
7	R/W\	28	BYPASS\(TEST)	49	OL_2(TEST)	70	PD_7
8	A_1	29	OL_4(TEST)	50	OL_1(TEST)	71	PD_6
9	A_0	30	V_{REF}	51	OL_0(TEST)	72	PD_5
10	D_{GND}	31	R_{REF}	52	PD_{23}	73	PD_4
11	PDC	32	A_{GND}	53	PD_{22}	74	PD_3
12	VHSYNC\	33	COMPOSITE	54	PD_{21}	75	PD_2
13	VVSYNC\	34	A_{GND}	55	PD_{20}	76	PD_1
14	D_7	35	LUMA	56	PD_{19}	77	PD_0
15	D_6	36	A_{GND}	57	PD_{18}	78	LDV
16	D_5	37	CHROMA	58	PD_{17}	79	PXCK
17	D_4	38	A_{GND}	59	PD_{16}	80	D_{GND}
18	D_3	39	COMP	60	PD_{15}	81	V_{DD}
19	D_2	40	V_{DDA}	61	PD_{14}	82	GVSYNC\
20	D_1	41	V_{DDA}	62	PD_{13}	83	GHSYNC\
21	D_0	42	V_{DDA}	63	PD_{12}	84	$CVBS_3$

Note: Pin names in parentheses apply to TMC22090/091



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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC22090R0C	T_A = 0°C to 70°C	Commercial	84-Lead PLCC	22090R0C
TMC22091R0C	T_A = 0°C to 70°C	Commercial	84-Lead PLCC	22091R0C
TMC22190R0C	T_A = 0°C to 70°C	Commercial	84-Lead PLCC	22190R0C
TMC22191R0C	T_A = 0°C to 70°C	Commercial	84-Lead PLCC	22191R0C

40G07228 Rev D 8/93

TMC2242
Half-Band Interpolating/Decimating Digital Filter
12 Bits, 40 MHz

Description

The TMC2242 is a fixed-coefficient, linear-phase half-band (low-pass) digital filter VLSI circuit which can also be used to halve or double a digital signal's sample rate. When used as a decimating post-filter with a double-speed oversampling video A/D converter, it greatly reduces the cost and complexity of the associated analog antialias pre-filter, such as that required for broadcast video chrominance bandwidth limiting. When used as an interpolating pre-filter, such as that required for broadcast video chrominance bandwidth limiting. When used as an interpolating pre-filter with a double-speed oversampling D/A converter, the TMC2242 can simplify the corresponding analog reconstruction post-filter. The only user "programming" required is selection of mode (interpolate, decimate, or neither) and rounding.

The TMC2242 accepts 12-bit two's complement data at up to 40 million samples per second and outputs saturated, two's complement or inverted offset binary data, rounded to 9 to 16 bits. Within the 40 MHz 1/O limit, the TMC2242's output sample rate can be 1/2, 1, or 2 times its input sample rate.

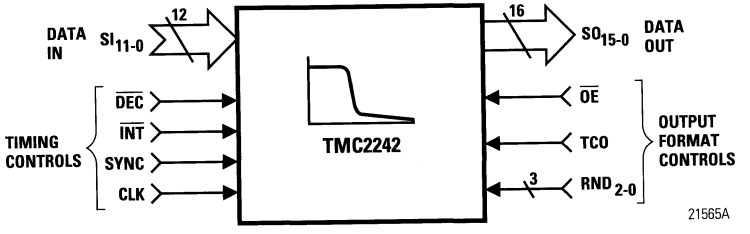
The filter is flat within ±0.02 dB from 0 to 0.22 F_S, with stopband attenuation of greater than 59.4 dB from 0.28 F_S to the Nyquist frequency. The response is 6 dB down at 0.25 F_S. Symmetric-coefficient FIR filters such as the TMC2242 have linear phase response. Although most users will be pleased with the results obtained with one TMC2242 in the system, full compliance with the SMPTE 601 standard of -12 dB at 0.25 F_S requires two devices cascaded serially.

Fabricated using a one-micron CMOS process, the TMC2242 operates at a guaranteed clock rate of 40 MHz over the standard temperature and supply voltage ranges and is available in a 44-lead plastic chip carrier.

Features

- 40 MHz guaranteed maximum clock rate
- User-selectable 2:1 decimation, 1:2 interpolation
- Frequency response ±0.02 dB in passband
- Stopband (0.28 to 0.5 x F_S) rejection 59.4 dB
- Two-device cascade meets CCITT recommendation 601 low-pass filter requirements
- Dedicated 12-bit two's complement input data port and 16-bit output data port with user-selectable rounding to 9 through 16 bits
- Two's complement or inverted offset binary output format
- Built-in limiter prevents overflow
- Single +5V power supply
- Compact 44-lead plastic chip carrier package

Logic Symbol



Applications

- Low-Cost, Industry-Standard Video Chrominance Bandwidth Limiting (Anti- Aliasing)
- Simple, High-Performance Video Reconstruction Post-Filtering
- General Digital-Domain High-Performance Low-Pass Filtering, Requiring:
  - — Passband Below (0.22) x F_S
  - — Stopband Above (0.28) x F_S
- General Digital-Domain Waveform Reconstruction Post-Filtering
- Telecommunications Systems
- Digitally Synthesized Radio
- Radar

Functional Description

The TMC2242 implements a fixed-coefficient linear-phase Finite Impulse Response (FIR) filter of 55 effective taps, with special rate-matching input and output structures to facilitate 1:2 decimation and 2:1 interpolation. In the straight-through mode (equal input and output clock rates), the filter and input and output registers will operate at the guaranteed maximum clock rate of 40MHz. The total internal pipeline latency from the input of an impulse to the corresponding output peak is 33 cycles; the 55-value output response begins after 6 clock cycles and ends after 60 cycles.

To perform interpolation, the chip slows the effective input register clock rate to half the internal and output rates. The TMC2242 internally inserts zeroes between the incoming data samples to "pad" the input data rate to match the output rate.

To perform decimation, the chip sets the output register clock rate to half of the input and internal rates. One output is then obtained for every two inputs.

In interpolation or decimation mode, the SYNC control is first held HIGH, then brought LOW with the first data input value. SYNC is held LOW until resynchronization is desired. For interpolation, input values should be presented at the first rising edge of CLK for which SYNC=0 and at every alternate CLK rising edge thereafter.

Figure 1. Functional Block Diagram

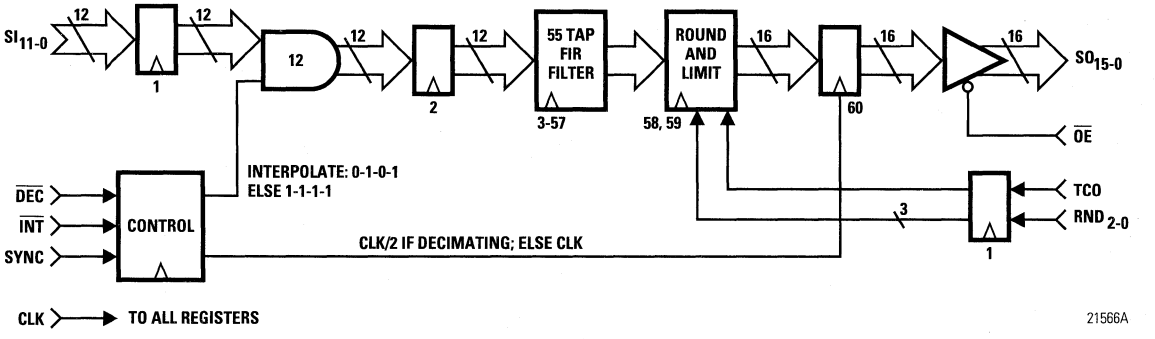


Figure 2A. Transfer Function of TMC2242 Half-Band FIR Filter

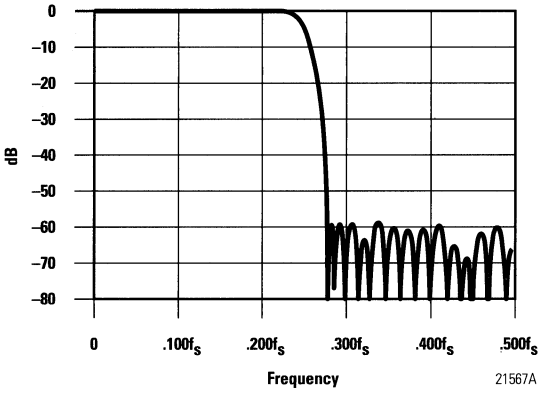
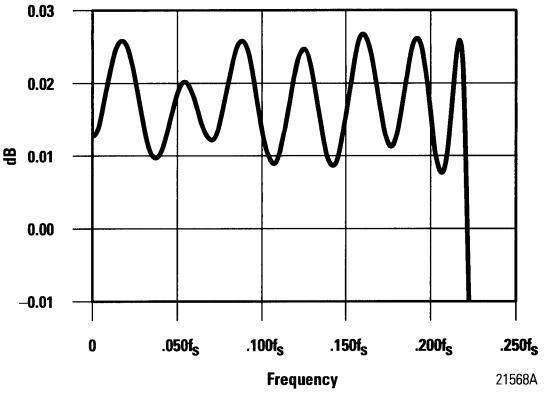


Figure 2B. Passband Detail of TMC2242 Transfer Function



The input data word format is always two's complement. The output data format is two's complement when TCO is HIGH and inverted offset binary when TCO is LOW. The output data can thus be processed further or routed directed to a Digital-to-Analog converter for reconstruction. The user can tailor the output data word width to his system requirements using the Rounding control. As shown in ***Table 1***, the output is half-LSB rounded to the resolution selected by the value of $RND_{2\text{-}0}$. The bits below the LSB are then zero-filled. The asynchronous three-state output enable control simplifies interfacing to a bus.

Signal Definitions

Clock

CLK — The TMC2242 operates from a single master Clock. All internal registers (except output register in decimate mode) are strobed on the rising edge of Clock, and all timing specifications are referenced to the rising edge of Clock.

SYNC — The user synchronizes the incoming data with the TMC2242 by holding SYNC HIGH on Clock N, and then LOW on Clock N+1, when the first data word is presented to the input $SI_{11\text{-}0}$. If $\overline{DEC}$=$\overline{INT}$ (passthrough mode), SYNC is inactive. SYNC may be held LOW until resynchronization is desired, or it may be toggled at 1/2 the clock rate.

Inputs

$SI_{11\text{-}0}$ — Data presented to the registered 12-bit two's complement data input port $SI_{11\text{-}0}$ will be latched internally on the current Clock, or on every other Clock if in INTERPOLATE mode. SI_{11} is the MSB.

Outputs

$SO_{15\text{-}0}$ — The current result is available at the registered 16-bit output port $SO_{15\text{-}0}$, half-LSB rounded as determined by the rounding control word $RND_{2\text{-}0}$. SO_{15} is the MSB.

Note: TMC2242's limiter ensures that an internal overflow will generate a valid full-scale (7FFF positive or 8000 negative) output. The chip's D.C. gain is 1.0015=0.0126dB; 0.5007 = –3.004dB in INTERPOLATE mode.

Controls

TCO — When the Two's Complement format Control TCO is HIGH, all output data are presented in signed two's complement format. When LOW, the output is inverted offset binary, obtained inside the chip by inverting bits SO_{14} through SO_0, leaving SO_{15} unchanged.

$\overline{INT}$ — When the input interpolation control $\overline{INT}$ is LOW, the input register is driven at full clock speed and the chip inserts zeroes between samples, "padding" the input to match the output rate and effectively halving the input data rate and the output amplitude. The TMC2242 then interpolates between these

alternate input data points to achieve a full output data rate.

$\overline{DEC}$ — When the decimation output control $\overline{DEC}$ is LOW, the output register is driven at half clock speed, decimating the output data stream.

Note: When $\overline{INT}$=$\overline{DEC}$, both the input and output registers run at the full clock rate.

$RND_{2\text{-}0}$ — These three pins set the position of the effective least significant bit of the output port by adding a rounding bit to the next lower internal bit and zeroing all outputs below the rounding bit. See *Table 1*.

Note: The above controls, TCO, $\overline{DEC}$, $\overline{INT}$, and $RND_{2\text{-}0}$ determine the device function, numeric format, and rounding of the data. The user must exercise caution when changing them, since they will impact work in progress in the chip's 60 clock internal pipeline.

$\overline{OE}$ — The output data port $SI_{15\text{-}0}$ is in the high-impedance state when the asynchronous output enable is HIGH. When $\overline{OE}$ is LOW, the port is enabled.

Power

V_{DD}, GND — The TMC2242 operates from a single +5V supply. All power and ground pins must be connected.

Table 1. Input and Output Data Formats and Bit Weighting, TCO=1[1]

Bit Weight - Output Port During Interpolation Only[2]

-2^1	2^0	2^{-1}	•••	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}

Bit Weight - All other I/O

-2^0	2^{-1}	2^{-2}	•••	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	Rounding $RND_{2\text{-}0}$

Input SI_{11}	SI_{10}	SI_9	•••	SI_4	SI_3	SI_2	SI_1	SI_0					—
Output													
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_1	SO_0r	000
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_1r	0	001
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2r	0	0	010
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3r	0	0	0	011
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4r	0	0	0	0	100
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5r	0	0	0	0	0	101
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6r	0	0	0	0	0	0	110
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7r	0	0	0	0	0	0	0	111

Note:
1. When TCO=0, most significant bit of output is positive instead of negative.
2. During interpolation, device DC gain is approximately 0.5.
3. Where "r" indicates the half-LSB-rounded bit, 0 the zeroed LSBs, and a minus sign a sign bit.

Table 2. Hexadecimal Impulse Response and Decimal Equivalents of Coefficients

Inpulse Out[1]	Decimal Equivalent	
FFF2	–.000875473	coef #1, 55
0000	.0	coef #2, 54=0
0017	.001390457	
0000	.0	
FFDB	–.002265930	
0000	.0	
0039	.003501892	
0000		
FFA8	–.005355835	
0000		
007D	.007621765	
0000		
FF51	–.01071167	
0000		
00F3	.01483154	
0000		
FEB5	–.02018738	
0000		
01CA	.02796364	
0000		
FD79	–.03949928	
0000		
03CD	.05937767	
0000		
F95E	–.1036148	
0000		
145B	.3180542	coef #27, 29
2010	.5009766	coef #28 (center)

Note: 1. Input=0,0,400,0,0,...
$\overline{INT}$=DEC=1
TCO=1

Table 3. Input Transition Response

	INPUT	OUTPUT				
		$\overline{INT}$=DEC TCO=0	$\overline{INT}$=DEC TCO=1	$\overline{INT}$=0 DEC=1 TCO=1	$\overline{INT}$=1 DEC=0 TCO=1	
	400	XX	XX	XX	XX	
	400	XX	XX	XX	XX	
>55 cycles	•	•	•	•	•	
	•	•	•	•	•	
	•	•	•	•	•	
	400	3FE7	4018	2008	4018	DC gain[1]
	400	3FE7	4018	2010	4018	
	000					
	•					
	•					
	000	3B90	446F	245F	446F	Max ringing
	000	3B90	446F	2010	446F	
	000	4FEB	3014	1004	1004	
	000	6FFB	1004	0000	1004	
	000	846F	FBA9	FBA9	FBA9	Min ringing
	•	•	•			
	•	•	•			
	•	•	•			
	000	7FFF	0000	0000	0000	Steady state

Note: 1. In interpolation, steady-state output will oscillate approximately 0.1%, as here between 2008 and 2010.

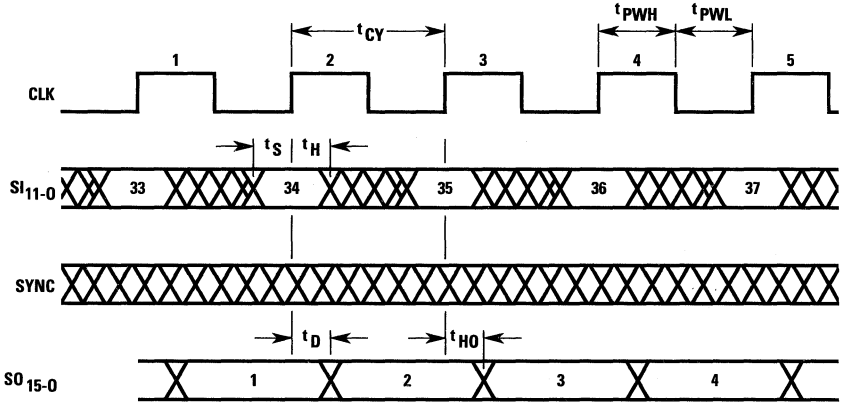
Table 4. Steady-State Output Values and Limiter Triggers (L) versus Input Data

	INT\ = 1 or DEC\ = 0		INT\ = 0 and DEC\ = 1		
Input	TCO = 0	TCO = 1	TCO = 0	TCO = 1	Interpretation
7FF	0000 (L)	7FFF (L)	3FF7 / 3FE7	4008 / 4018	+ full-scale
400	3FE7	4018	5FF7 / 5FEF	2008 / 2010	+ 1/2 scale
001	7FEF	0010	7FF7	0008	+ 1 LSB
000	7FFF	0000	7FFF	0000	Zero
FFF	800F	FFF0	8007	FFF8	- 1 LSB
C00	C017	BFE8	A007 / A00F	DFF8 / DFF0	- 1/2 scale
800	FFFF (L)	8000 (L)	C00F / C01F	BFF1 / BFE0	- Full-scale

Package Interconnections

Signal Type	Name	Function	R2 Package
Timing Controls	$\overline{INT}$	Interpolate	44
	$\overline{DEC}$	Decimate	1
	SYNC	Synchronization	43
	CLK	System Clock	42
Data Inputs	SI_{11-0}	Input Data Port	40, 37, 36, 35, 34, 33, 32, 31, 30, 27, 26, 25
Data Outputs	SO_{15-0}	Output Data Port	4, 5, 6, 7, 8, 9 10, 11, 14, 15, 16, 17, 18, 19, 20, 21
	$\overline{OE}$	Output Enable	3
Output Controls	RND_{2-0}	Rounding	22, 23, 24
Power	V_{DD}	Supply Voltage	13, 29, 38
	GND	Ground	12, 28, 39, 41

Figure 3. Timing Diagram — Equal Rate Mode $\overline{INT}$=$\overline{DEC}$



Note: Values at SO_{15-0} are impulse response centers (peaks) corresponding to inputs bearing the same numbers. Thus, the input-to-center latency is 33 registers (clock cycles).

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Figure 4. Timing Diagram - Decimation $\overline{INT}$=1, $\overline{DEC}$=0

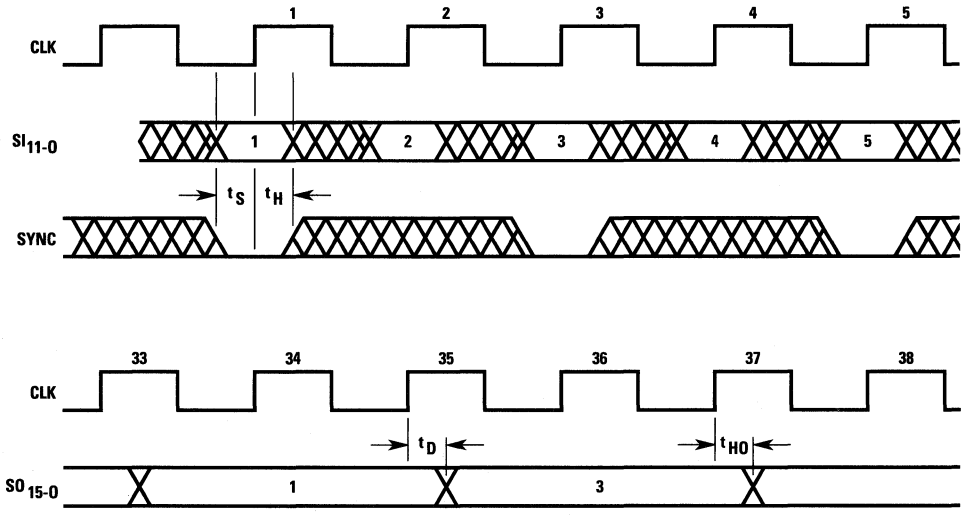

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Figure 5. Timing Diagram - Interpolation $\overline{INT}$=0, $\overline{DEC}$=*1*

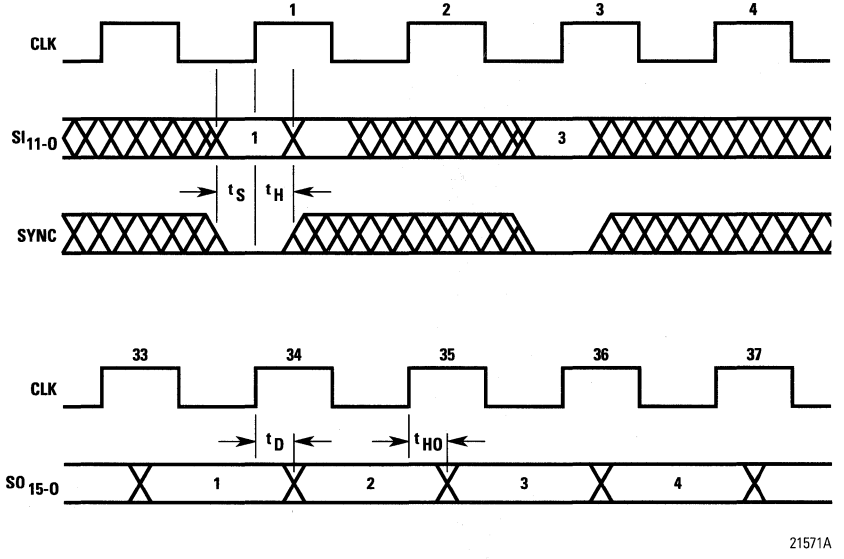

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Figure 6. Impulse Response - Equal I/O Rate Mode $\overline{INT}$=$\overline{DEC}$

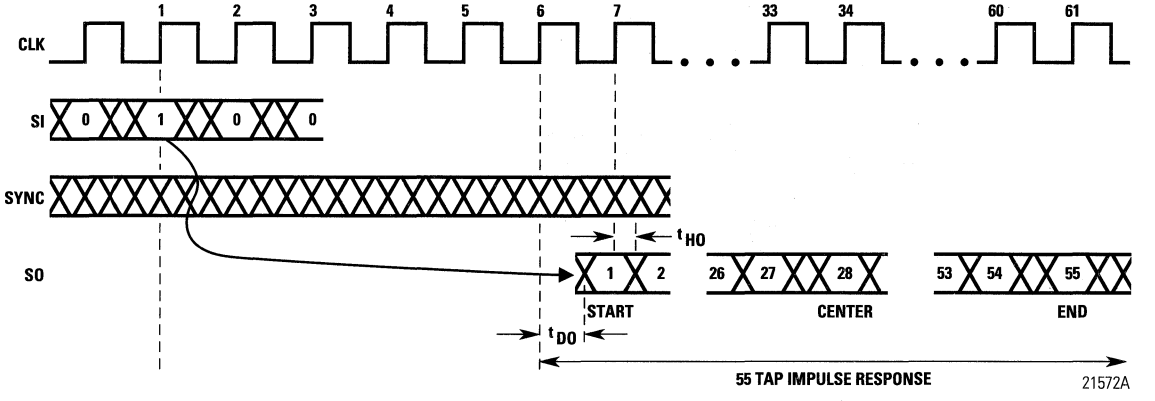


Figure 7. Impulse Response - Interpulate Mode $\overline{DEC}$=1, $\overline{INT}$=0

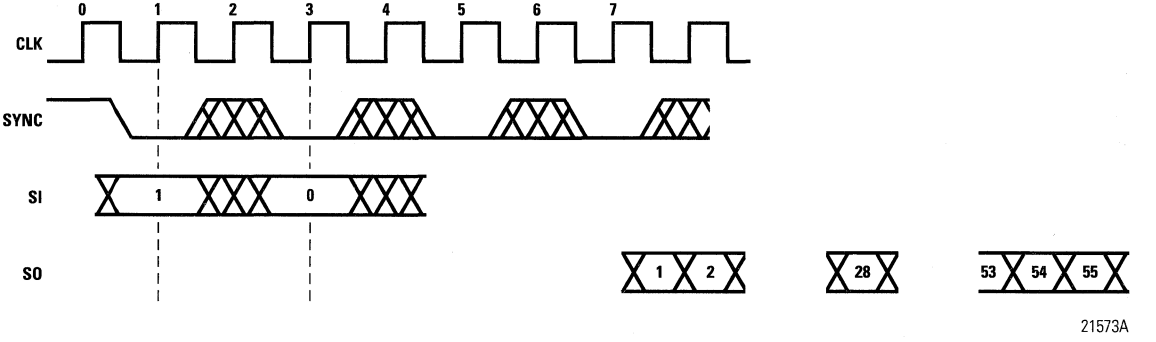


Figure 8. Impulse Response - Decimate Mode $\overline{DEC}$=0, $\overline{INT}$=1

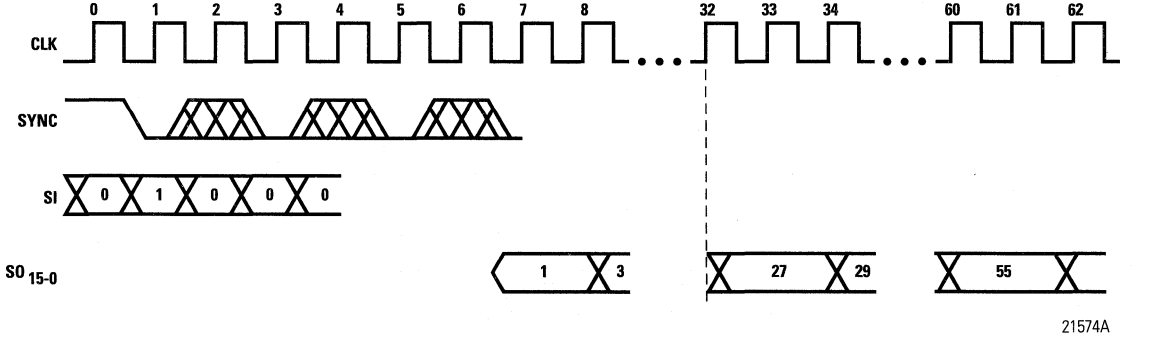


Figure 9. Equivalent Input Circuit

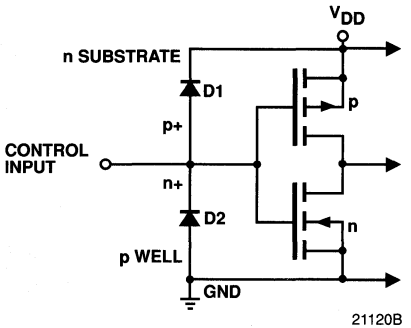


Figure 10. Equivalent Output Circuit

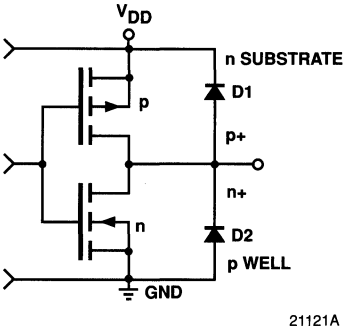
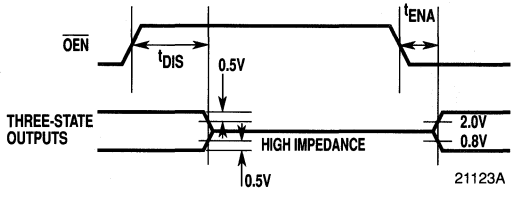


Figure 11. Threshold Levels for Three-State Measurement



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	–0.5 to +7.0V
Input Voltage	–0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage[2]	–0.5 to (V_{DD} + 0.5)V[2]
Forced current[3,4]	–6.0 to 6.0mA[3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating case	–60 to +130°C
junction	175°C
Lead soldering (10 seconds)	300°C
Storage	–65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range Standard Min	Temperature Range Standard Max	Units
V_{DD}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Voltage, Logic LOW		0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0		V
I_{OL}	Output Current, Logic LOW		8.0	mA
I_{OH}	Output Current, Logic HIGH		–4.0	mA
t_{CY}	Cycle Time			
	TMC2242	33		ns
	TMC2242-1	25		ns
t_{PWL}	Clock Pulse Width, LOW	10		ns
t_{PWH}	Clock Pulse Width, HIGH	10		ns
t_S	Input Setup Time			
	TMC2242	10		ns
	TMC2242-1	8		ns
t_H	Input Hold Time	0		ns
T_A	Ambient Temperature, Still Air °C	0	70	°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, $\overline{OE}$=V_{DD},			
		f=10MHz			mA
		f=20MHz		140	mA
I_{IL}	Input Current,Logic LOW	V_{DD}=Max, V_{IN}=0V		±10	µA
I_{IH}	Input Current,Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		±10	µA
V_{OL}	Output Voltage,Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4	V
V_{OH}	Output Voltage,Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V		±40	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		±40	µA
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.	-20	-80	µA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown, but specified operation is guaranteed.

Switching characteristics within specified operating conditions

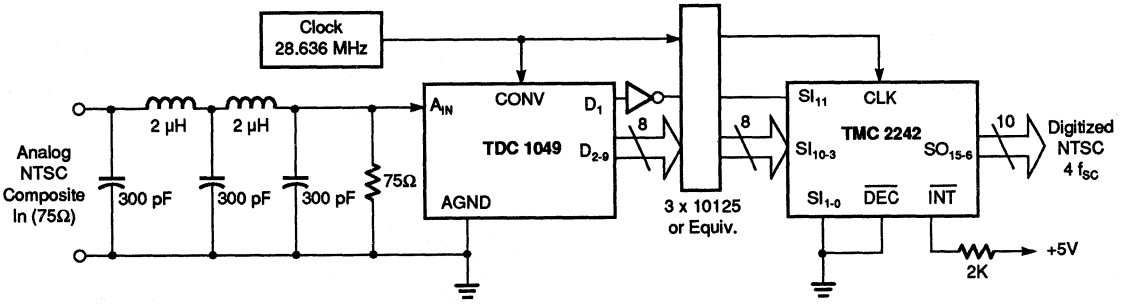
Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_D	Output Delay	V_{DD}=Min, C_L=25pF			
	TMC2242			20	ns
	TMC2242-1			16	ns
t_{HO}	Output Hold	V_{DD}=Max, C_L=25pF	3		ns
t_{ENA}	Output Enable	V_{DD}=Min, C_L=25pF			
	TMC2242			20	ns
	TMC2242-1			15	ns
t_{DIS}	Output Disable	V_{DD}=Min, CL=25pF			
	TMC2242			20	ns
	TMC2242-1			15	ns

Applications Discussion

Digitizing Composite NTSC Video

The TMC2242 is well suited for filtering digitized composite NTSC-encoded analog video. *Figure 12* shows a simple and cost-effective circuit built around the device. The TDC1049 9-bit Analog-to-Digital converter is a popular choice for digitizing high-quality video, offering a 30MHz maximum clock rate and 16MHz input bandwidth at moderate cost. The relative timing of the TDC1049 and TMC2242 clocks must accommodate the delay through the 10125 ECL-to-TTL converter, the TDC1049 output delay, and the TMC2242 input setup and hold times.

Figure 12. Digitizing NTSC Video Using the Decimation Mode



Antialiasing Prefilter

- 0.012 dB @ 5.75 MHz
- 3 dB @ 9.3 MHz
- 48 dB @ 21.5 MHz

TCD 1049 ADC

15 MHz Input BW
28.636 MSPS Clock
D_1 = MSB, D_9 = LSB

TMC 2242 Half-Band Filter

2:1 Decimation Mode
Data in @ 28.636 MSPS
Data Out @ 14.318 MSPS
SI_{11} = MSB. SI_3 = LSB
SI_{15} = MSB, SO_6 = LSB
10 Bits Output Precision
TCO = 1

65-6407

In *Figure 13*, an interpolating TMC2242 drives a fast D/A converter to reconstruct an analog NTSC composite waveform. The TDC1112 12-bit Digital- to-Analog converter features extremely low glitch energy for accurate waveform generation, and settling to ± 1/2 LSB in less than 30nsec. The same *(Figure 12)* 75-ohm analog filter is used, this time after the DAC. The user must maintain the correct timing between the TTL Clock and the ECL Clock, including the delay introduced by the 10124 TTL-ECL converter. See the *Timing Diagram* and the *TDC1012 datasheet*. Lower-speed applications can employ the TTL-input TDC1012 DAC without the level translators *(Figure 14)*.

Figure 13. High Speed Interpolation Application

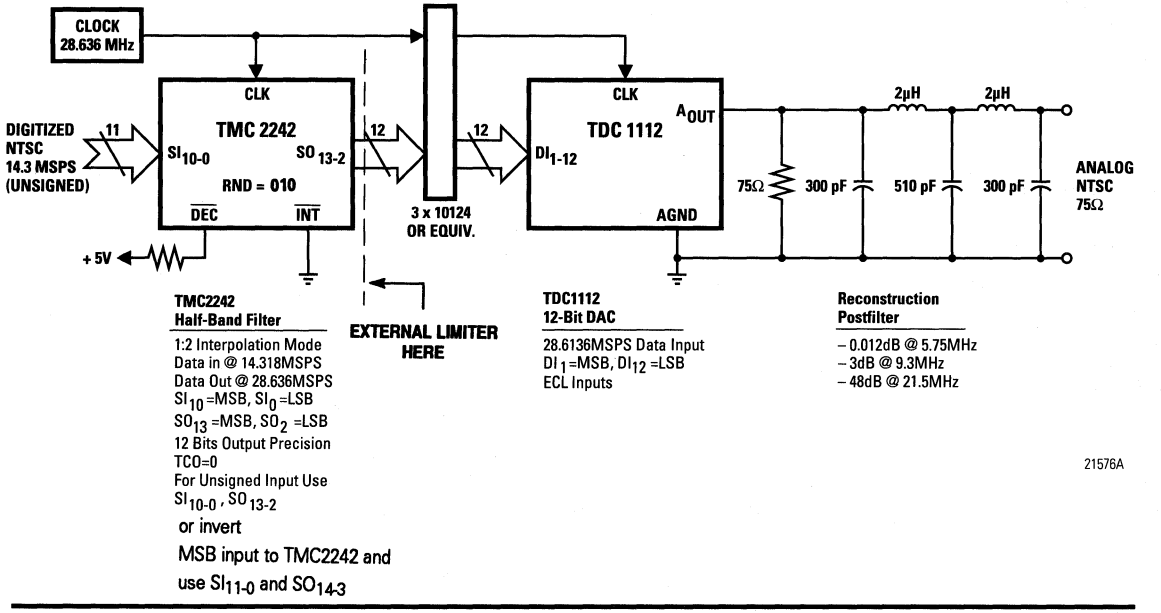
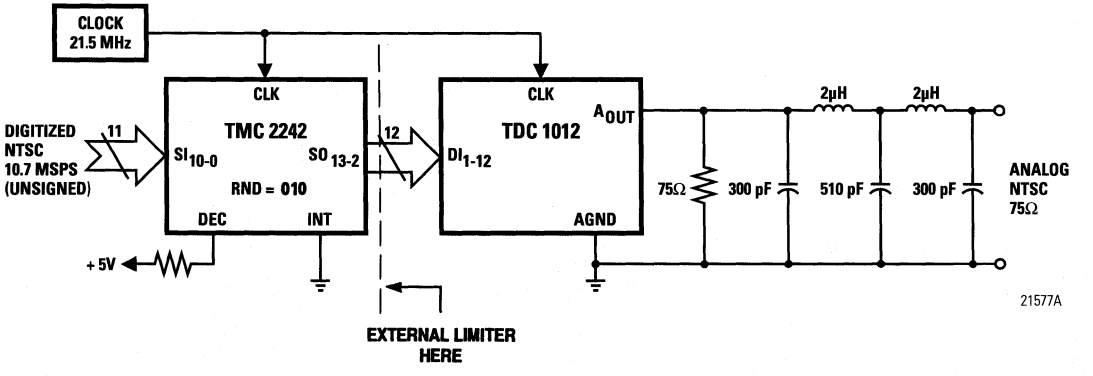
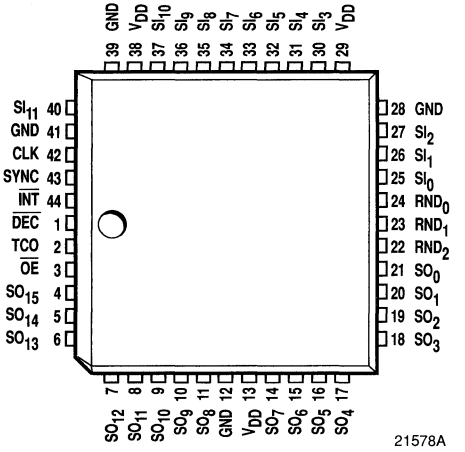


Figure 14. Medium Speed Interpolation Application



Pin Assignments – 44 Lead Plastic Chip Carrier - R2 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	$\overline{DEC}$	12	GND	23	RND_1	34	SI_7
2	TCO	13	V_{DD}	24	RND_0	35	SI_8
3	$\overline{OE}$	14	SO_7	25	SI_0	36	SI_9
4	SO_{15}	15	SO_6	26	SI_1	37	SI_{10}
5	SO_{14}	16	SO_5	27	SI_2	38	V_{DD}
6	SO_{13}	17	SO_4	28	GND	39	GND
7	SO_{12}	18	SO_3	29	V_{DD}	40	SI_{11}
8	SO_{11}	19	SO_2	30	SI_3	41	GND
9	SO_{10}	20	SO_1	31	SI_4	42	CLK
10	SO_9	21	SO_0	32	SI_5	43	SYNC
11	SO_8	22	RND_2	33	SI_6	44	$\overline{INT}$



21578A

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2242R2C	STD-T_A=0°C to 70°C	Commercial	44 Lead Plastic Chip Carrier	2242R2C
TMC2242R2C1	STD-T_A=0°C to 70°C	Commercial	44 Lead Plastic Chip Carrier	2242R2C1

40GO6433 Rev B 8/93

TMC2243
CMOS FIR Filter
10 x 10 Bit, 20 MHz

Description

The TMC2243 is a video speed three stage 10 x 10 bit FIR (Finite Impulse Response) filter integrated circuit composed of three registered multiplier-adders concatenated into a one-dimensional systolic array. Utilizing two's complement representation, the TMC2243 accepts one 10-bit data point, updates one 10-bit coefficient, and produces one 16-bit rounded, filtered output point every 50 nanoseconds.

The TMC2243 has features which facilitate longer FIR filters, a 16-bit Sum-In port and user programmable pipeline registers. Enabling these registers allows the insertion of a zero-coefficient stage before each regular filter stage for up to six stages per TMC2243. Larger FIR filters can be built by cascading Sum-In and Sum-Out.

Coefficients are stored in 3 registers and are addressed via the 2-bit Write Enable control, allowing one coefficient to be changed per clock cycle. All Data, Sum-In, Sum-Out and instruction inputs are registered on the rising edge of clock.

The 16 MSBs of the 23-bit internal summation path are available at the Sum-In and Sum-Out ports. Six bits of cumulative word growth are provided internally. Data Overflow is indicated by an output flag.

Built with Raytheon Semiconductor's one-micron double level metal OMICRON-C™ CMOS process, the TMC2243 is available in a 68-pin grid array.

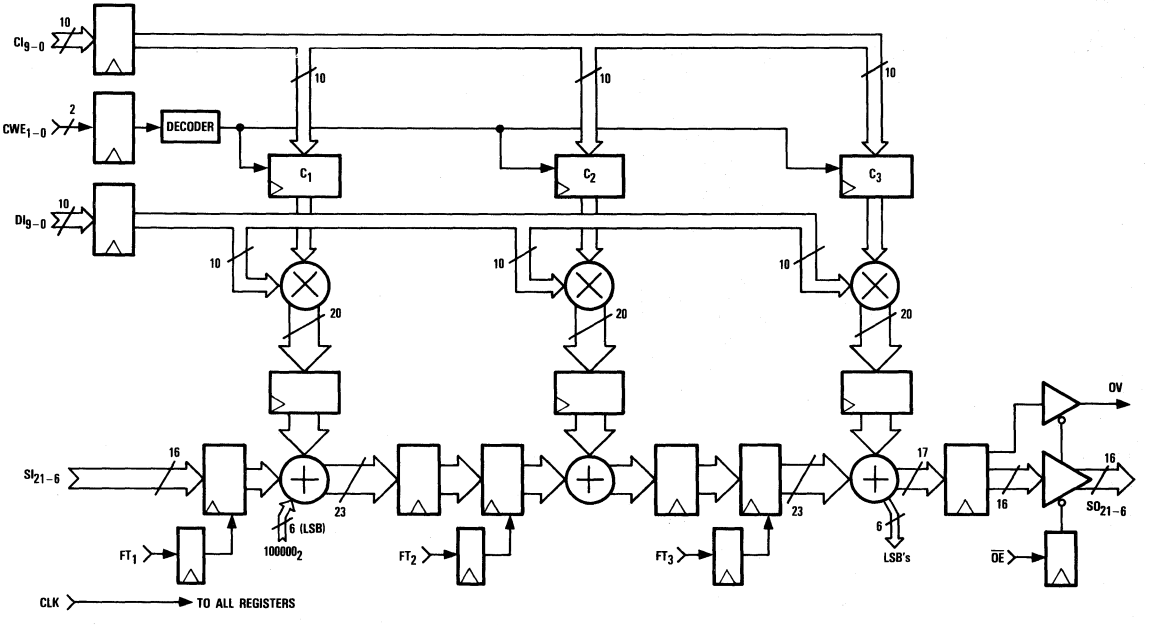
Features

- 20 MHz data input and computation rate
- 10 x 10 bit multiplication with 23-bit extended precision sum of products (overflow, plus 16 output and 6 guard bits)
- Up to 3 zero and 3 non-zero stages per device
- Two's complement arithmetic
- 16-bit Sum-In and Sum-Out ports for cascading
- Internal 1/2 LSB rounding
- All inputs and outputs are registered
- One coefficient update per clock cycle
- Low power consumption CMOS process
- Single +5V supply
- Available in 68-pin grid array and 69-pin plastic PGA packages

Applications

- FIR filters
- Adaptive filters
- Multi-bit correlation
- One and two dimension video filtering
- Radar signal processors
- One and two dimension convolution
- Arithmetic element for systolic array processors

Functional Block Diagram

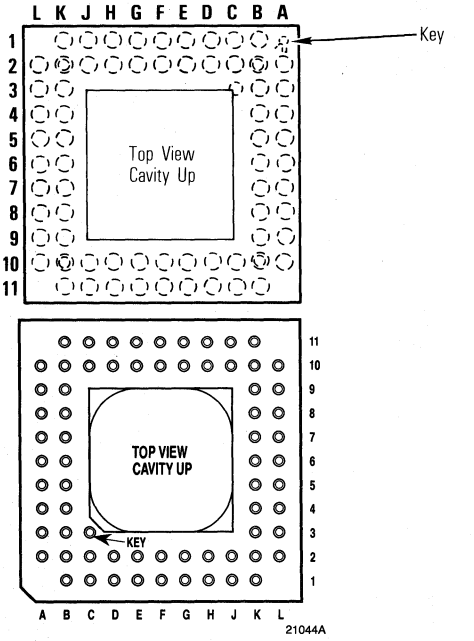


Pin Assignments

63 Pin Grid Array – G8 Package
69 Pin Plastic Pin Grid Array – H8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	GND	K2	DI_1	K10	GND	B10	OV
B1	V_{DD}	L2	DI_0	K11	SI_{18}	A10	SO_{21}
C2	$\overline{OE}$	K3	CI_0	J10	SI_{17}	B9	SO_{20}
C1	FT_0	L3	CI_1	J11	SI_{16}	A9	SO_{19}
D2	FT_1	K4	CI_2	H10	SI_{15}	B8	SO_{18}
D1	FT_2	L4	CI_3	H11	SI_{14}	A8	SO_{17}
E2	CWE_0	K5	CI_4	G10	SI_{13}	B7	SO_{16}
E1	CWE_1	L5	CI_5	G11	SI_{12}	A7	SO_{15}
F2	DI_9	K6	V_{DD}	F10	SI_{11}	B6	SO_{14}
F1	DI_8	L6	CI_6	F11	SI_{10}	A6	SO_{13}
G2	DI_7	K7	CI_7	E10	SI_9	B5	SO_{12}
G1	DI_6	L7	CI_8	E11	SI_8	A5	SO_{11}
H2	DI_5	K8	CI_9	D10	SI_7	B4	SO_{10}
H1	DI_4	L8	SI_{21}	D11	SI_6	A4	SO_9
J2	DI_3	K9	SI_{20}	C10	V_{DD}	B3	SO_8
J1	DI_2	L9	SI_{19}	C11	V_{DD}	A3	SO_7
K1	GND	L10	CLK	B11	GND	A2	SO_6

Note: Pin D4 is a mechanical orientation pin on the H8 package at manufacturer's option.



Functional Description

General Information

The TMC2243 consists of three identical arithmetic cells, each of which contains a 10 x 10 two's complement multiplier and a 23-bit adder. Each cell receives the current data (DI) from the Data input register, multiplies it by a locally stored Coefficient (CI_i), and adds it to the Sum $SI_{(i-1)}$ received from the previous cell. The result,

$$SI_i = DI \times CI_i + SI_{(i-1)},$$

then goes to the next cell via two serial pipeline registers. When only one pipeline register is enabled, stages (i-1) and i are sequential. When both registers are enabled, there is a stage with a zero coefficient between them.

The input arithmetic cell receives $SI_{(i-1)}$ via the 16-bit Sum-In port (registered when FT_1 = LOW), filling the six lower bits with 100 000 (1/2 LSB) for internal rounding. The output cell outputs the 16 MSBs (V_{21} through V_6) of SO_i through a register to the Sum-Out port. The Overflow flag is set when the final output exceeds 16 bits and resets with the output of the next nonoverflowing result. Sum-Out and the Overflow Flag can be forced to high-impedance with the Output Enable control. See Figure 1.

The two-bit Write Enable control specifies the loading of the three coefficient registers (one per arithmetic cell) with data appearing at the Coefficient Input port.

Signal Definitions

Power

V_{DD}, GND — The TMC2243 operates from a single +5V supply.

Clock

CLK — The TMC2243 has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.

Inputs

DI_{9-0} — DI_9 through DI_0 is the 10-bit registered Data Input; DI_9 is the MSB (sign bit) and DI_0 is the LSB. Data is in two's complement representation, and is clocked into the data register on each rising edge of clock. See Figure 1.

SI_{21-6} — SI_{21} through SI_6 is the 16-bit Sum-In port. SI_{21} is the MSB (sign bit). Sum-In is truncated to bit SI_6 (plus the 1/2 LSB rounding bit in SI_5)and is in two's complement representation. See Figure 1. The Sum-In port is registered, on the rising edge of clock, only when FT_1 =LOW. Unique input setup requirements must be observed when operating in the feedthrough mode (FT_1 = HIGH). See text.

CI_{9-0} — CI_9 through CI_0 is the 10-bit registered Coefficient Input; CI_9 is the MSB (sign bit) and CI_0 is the LSB. Each coefficient and its write enable address (CWE_{1-3}) are registered on the same clock. The coefficient is then latched into the indicated register (C_{1-3}) at the rising edge of the next clock. The contents of this bus are ignored if a coefficient register is not selected (CWE = 00). The format of CI_{9-0} is identical to that of DI_{9-0}.

Outputs

SO_{21-6} — SO_{21} through SO_6 is the three-state 16-bit registered Sum-Out port; SO_{21} is the MSB (sign bit). For maximum precision, the internal products and accumulations are 23 bits but Sum-Out is internally truncated to 16 bits, and excludes the overflow bit and the 6 LSBs. The format is identical to that of SI_{21-6}. See Figure 1.

Controls

CWE_{1-0} The two bits of the registered Coefficient Write Enable control indicate which of the coefficient registers is to receive a new coefficient at the beginning of the next clock cycle.

CWE_{1-0}	Coefficient Register Selected
00	Holds all coefficients unchanged.
01	C_1
10	C_2
11	C_3

FT_{3-1} These registered Feed Through controls select clocked (FT_i = LOW) or feedthrough (FT_i = HIGH) operation for each of the pipeline registers. Setting FT_i = LOW inserts a zero coefficient stage, or additional register, before the ith non-zero stage.

$\overline{OE}$ Output Enable is a registered three-state enable control which forces the Sum-Out port and Overflow to the high-impedance state when HIGH. These outputs are enabled when $\overline{OE}$ is LOW.

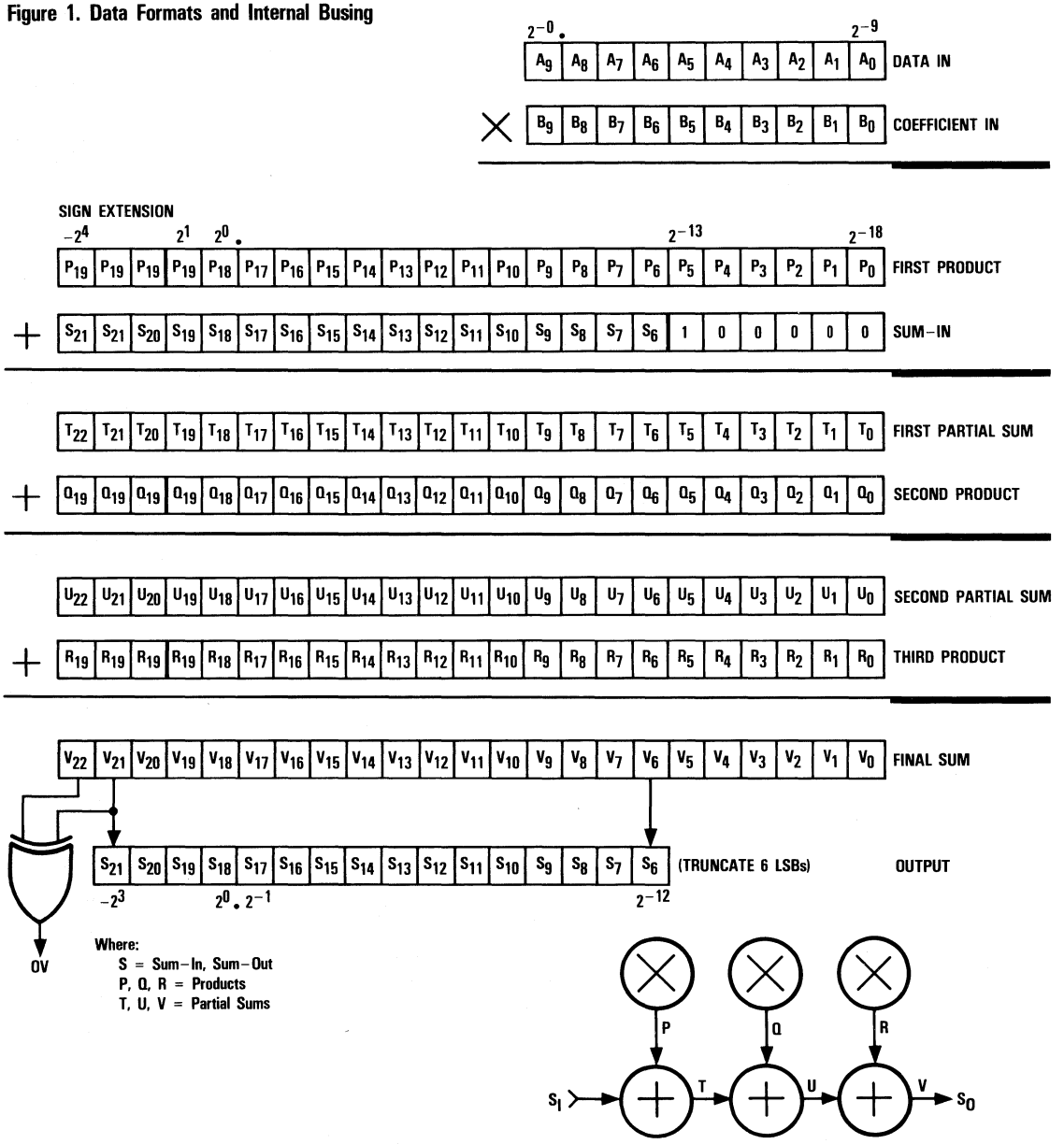
Flags

OV The Overflow Flag is a registered three-state output which goes HIGH whenever the summation result exceeds 16 bits and is reset to LOW on the next nonoverflowing result.

Package Interconnections

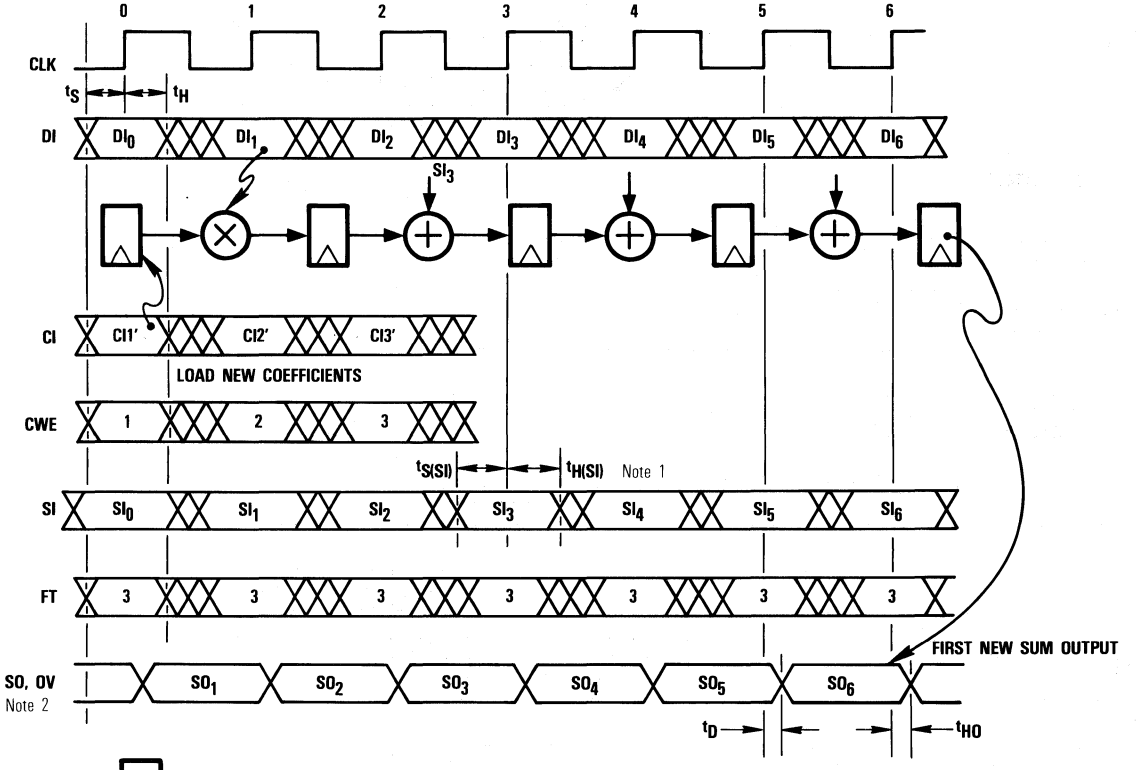
Signal Type	Signal Name	Function	G8, H8 Package Pins
Power	V_{DD}	Supply Voltage	B1, K6, C10, C11
	GND	Ground	B2, K1, K10, B11
Inputs	DI_{9-0}	Data Input	F2, F1, G2, G1, H2, H1, J2, J1, K2, L2
	SI_{21-6}	Sum Input	L8, K9, L9, K11, J10, J11, H10, H11, G10, G11, F10, F11, E10, E11, D10, D11
	CI_{9-0}	Coefficient Input	K8, L7, K7, L6, L5, K5, L4, K4, L3, K3
Outputs	SO_{21-6}	Sum Output	A10, B9, A9, B8, A8, B7, A7, B6, A6, B5, A5, B4, A4, B3, A3, A2
Clock	CLK	Master Clock	L10
Controls	CWE_{1-0}	Coefficient Write Enable	E1, E2
	FT_{3-1}	Feedthrough	D1, D2, C1
	$\overline{OE}$	Output Enable	C2
Flag	OV	Overflow	B10

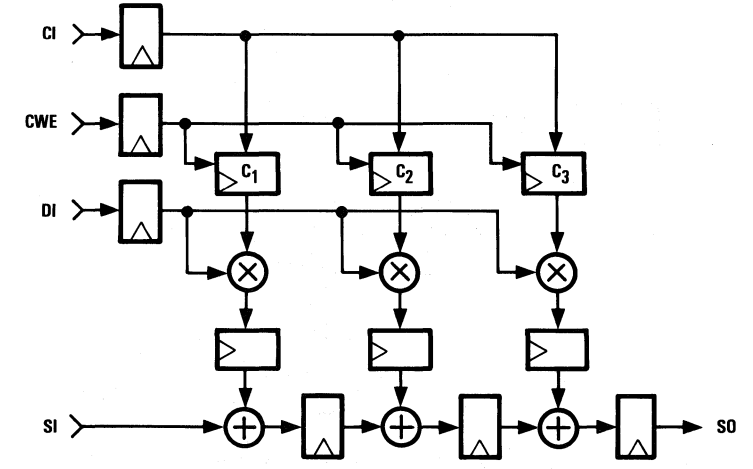
Figure 1. Data Formats and Internal Busing



Because the Sum-In and Sum-Out ports are truncated by 6 bits relative to the external accumulation pipeline, the TMC2243 rounds internally by adding 2^{-13} to each emerging sum of products, effecting half-LSB rounding relative to the output format. The chip internally utilizes all lower-order bits, to 2^{-18}.

Figure 2. Timing Diagram Demonstrating Basic Operation with FT_{1-3} = HIGH (no zero stages)





$$SO_N = SI_{N-3} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$$

Notes:

1. Setup and Hold requirements for the Sum Input are similar to the other registered inputs when when FT_1 = LOW. See text.
2. Sum Out and Overflow timing are shown with $\overline{OE}$ = LOW.

The basic equation describing the function of the TMC2243 operating in a fixed state is:

$$SO(N) = SI_{(N-6+FT1+FT2+FT3)} + C_1 \times DI_{(N-7+FT2+FT3)} + C_2 \times DI_{(N-5+FT3)} + C_3 \times DI_{(N-3)}$$

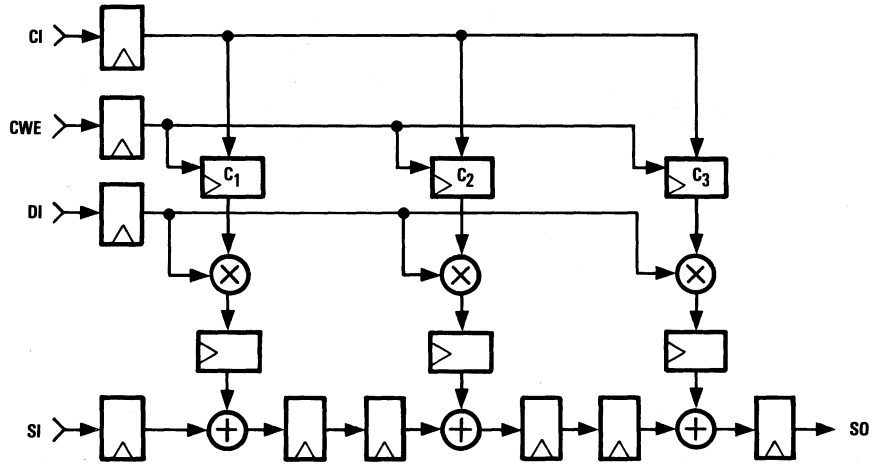
Careful observation of the clock delays shown is basic to construction of a filter algorithm. The operating sequence for the common application with FT_{1-3} = HIGH (no zero stages) is shown in Figure 2. The simplified block diagram demonstrates the clock stages in this configuration. When FT_1 = HIGH, the input feedthrough register is bypassed, and care must be taken to observe the setup requirements on the input of the first adder. Due to the absence of the input register buffer, note that the adder operates on data stable just prior to the arrival of the next clock, and not that setup at the rising edge of the current clock. When FT_1 = LOW the input register latches the input data, and the Sum Input follows setup and hold requirements similar to the other registered inputs of the TMC2243. When FT_1 = HIGH, $t_{S(SI)}$ is guaranteed to allow 20MHz pipelined operation, assuming that input setup is observed, including cascaded operation. See the AC Characteristics table, and Figure 9, Applications Discussion.

Figure 3 shows the effects of the feedthrough registers on filter operation, with two different configurations. The inputs are those presented at the corresponding rising edge of clock, excepting the delayed setup requirements of the Sum Input when FT_1 = HIGH. The outputs are those available up to and including the corresponding edge of clock. Applications utilizing the TMC2243's ability to modify coefficients dynamically are demonstrated in Figure 4, showing the operation of a typical adaptive filter. Note that the Sum Output will be zero in the first few clock cycles of all examples only if the Coefficient Registers are initialized to zero beforehand.

Figure 3. Impulse Response Filter Operation Sequence with $FT_{2,3}$ = LOW

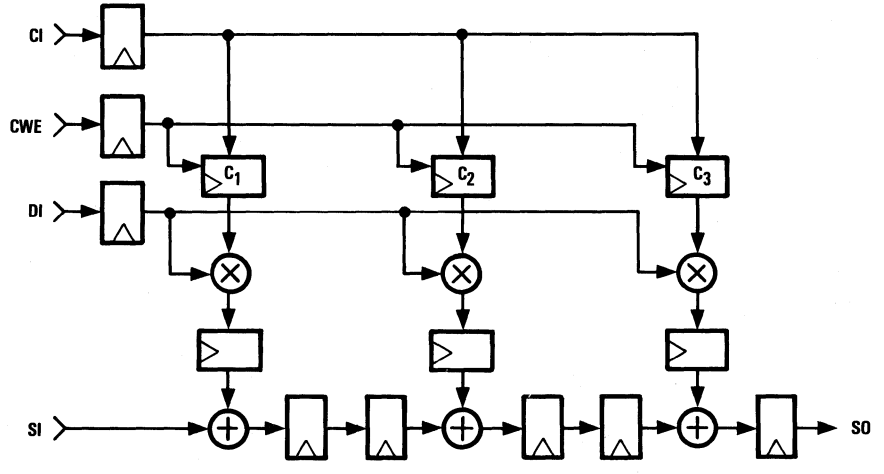
Cycle	SI(A) FT_1 = LOW	SI(B) FT_1 = HIGH	DI	CI	CWE	SO
1	0	0	0	K_0	01	0
2	0	0	0	K_1	10	0
3	0	0	0	K_2	11	0
4	SI_0	0	DI_0	0	00	
5	SI_1	SI_0	DI_1	0	00	0
6	SI_2	SI_1	DI_2	0	00	0
7	SI_3	SI_2	DI_3	0	00	DI_0K_2
8	SI_4	SI_3	DI_4	K_0'	01	DI_1K_2
9	SI_5	SI_4	DI_5	0	00	$DI_0K_1 + DI_2K_2$
10	SI_6	SI_5	DI_6	K_1'	10	$SI_0 + DI_1K_1 + DI_3K_2$
11	SI_7	SI_6	DI_7	0	00	$SI_1 + DI_0K_0 + DI_2K_1 + DI_4K_2$
12	SI_8	SI_7	DI_8	K_2'	11	$SI_2 + DI_1K_0 + DI_3K_1 + DI_5K_2$
13	SI_9	SI_8	DI_9	0	00	$SI_3 + DI_2K_0 + DI_4K_1 + DI_6K_2$
14	0	SI_9	0	0	00	$SI_4 + DI_3K_0 + DI_5K_1 + DI_7K_2$
15	0	0	0	0	00	$SI_5 + DI_4K_0 + DI_6K_1 + DI_8K_2$
16	0	0	0	0	00	$SI_6 + DI_5K_0' + DI_7K_1' + DI_9K_2'$
17	0	0	0	0	00	$SI_7 + DI_6K_0' + DI_8K_1'$
18	0	0	0	0	00	$SI_8 + DI_7K_0' + DI_9K_1'$
19	0	0	0	0	00	$SI_9 + DI_8K_0'$
20	0	0	0	0	00	DI_9K_0'
21	0	0	0	0	00	0

SI(A) is the sequence of Sum Input data with FT_{1-3} = LOW (three zero stages).



$$SO_N = SI_{N-6} + C_1DI_{N-7} + C_2DI_{N-5} + C_3DI_{N-3}$$

SI(B) is the sequence of Sum Input data with FT_1 = HIGH and $FT_{2,3}$ = LOW (two zero stages).

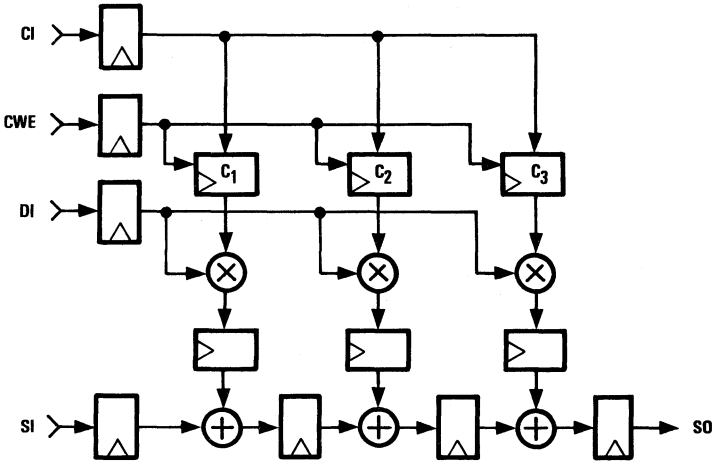


$$SO_N = SI_{N-5} + C_1DI_{N-7} + C_2DI_{N-5} + C_3DI_{N-3}$$

Figure 4. Typical Adaptive Filter Operation Sequence

Cycle	SI	DI	CI	CWE	SO
0	SI_0	DI_0	A_1	01	0
1	SI_1	DI_1	A_2	10	0
2	SI_2	DI_2	A_3	11	0
3	SI_3	DI_3	B_1	01	0
4	SI_4	DI_4	B_2	10	0
5	SI_5	DI_5	B_3	11	0
6	SI_6	DI_6	C_1	01	$SI_2 + A_1DI_1 + A_2DI_2 + A_3DI_3$
7	SI_7	DI_7	C_2	10	$SI_3 + A_1DI_2 + A_2DI_3 + A_3DI_4$
8	SI_8	DI_8	C_3	11	$SI_4 + A_1DI_3 + A_2DI_4 + A_3DI_5$
9	SI_9	DI_9		00	$SI_5 + B_1DI_4 + B_2DI_5 + B_3DI_6$
10	SI_{10}	DI_{10}		00	$SI_6 + B_1DI_5 + B_2DI_6 + B_3DI_7$
11	SI_{11}	DI_{11}		00	$SI_7 + B_1DI_6 + B_2DI_7 + B_3DI_8$
12	SI_{12}	DI_{12}		00	$SI_8 + C_1DI_7 + C_2DI_8 + C_3DI_9$
13	SI_{13}	DI_{13}		00	$SI_9 + C_1DI_8 + C_2DI_9 + C_3DI_{10}$

with FT_1 = LOW and $FT_{2,3}$ = HIGH (one zero stage)



$$SO_N = SI_{N-4} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$$

Figure 5. Equivalent Input Circuit

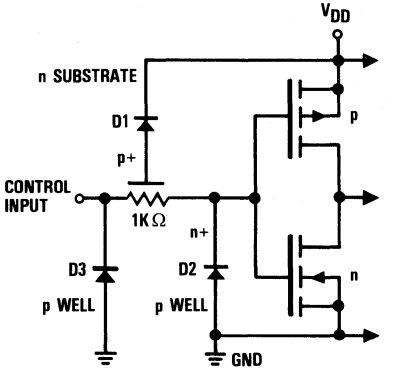


Figure 6. Equivalent Output Circuit

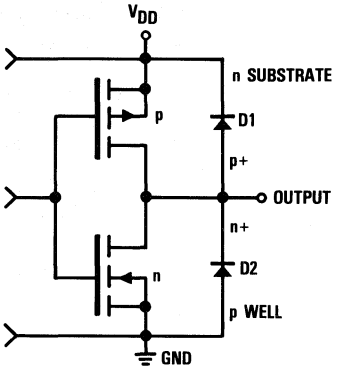


Figure 7. Test Load

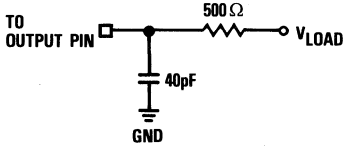
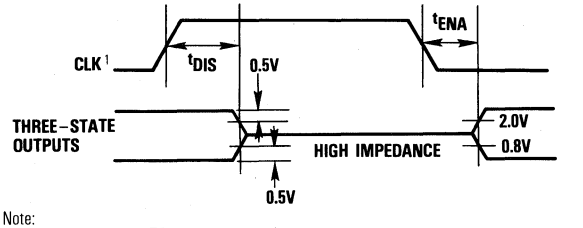


Figure 8. Transition Levels For Three-State Measurements



Note:

1. Assumes $\overline{OE}$ has gone LOW, within the Input Setup requirements.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5V)
Output	
Applied voltage [2]	−0.5 to (V_{DD} +0.5V)
Forced current [3,4]	−1.0 to 6.0mA
Short−circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

		Temperature Range						
		Standard			Extended			
Parameter		**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Units**
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW	2.0			2.0			V
V_{IH}	Input Voltage, Logic HIGH			0.8			0.8	V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OE}$ = HIGH		15		15	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH					
		f = 20MHz		90		90	mA
		f = 10MHz		48		48	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−75	75	−75	75	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}	−75	75	−75	75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	−40	40	−40	40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}	−40	40	−40	40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max		−150		−150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CY}	Cycle Time	V_{DD} = Min	50		50		ns
t_{PWL}	Clock Pulse Width LOW	V_{DD} = Min	20		20		ns
t_{PWH}	Clock Pulse Width HIGH	V_{DD} = Min	20		20		ns
t_S	Input Setup Time		15		20		ns
$t_{S(SI)}$	Input Setup Time, SI_{21-6}, FT_1 = HIGH		25		28		ns
	FT_1 = LOW		18		20		ns
t_H	Input Hold Time		2		3		ns
$t_{H(SI)}$	Input Hold Time, SI_{21-6}		5		5		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		30		30	ns
t_{DC}	Output Delay, Cascaded	V_{DD} = Min, C_{LOAD} = 10pF		20		20	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	5		5		ns
t_{ENA}	Three-State Output, Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		20		25	ns
t_{DIS}	Three-State Output, Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		15		20	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Application Discussion

Loading and Updating of Coefficients

Because of the TMC2243's internal architecture, its impulse response is C_3, C_2, C_1, where C_3 is the rightmost coefficient and C_1 is the leftmost. However, for glitchless performance, coefficients must be updated from left to right: C_1 then C_2 then C_3.

For example, consider an adaptive filter whose first set of coefficients is A_i, second set is B_i and third set is C_i (Figure 4). First, the TMC2243 is initialized with A_i. If these are loaded in numerical (left to right) sequence, two of the first three data points can be loaded with them, as shown in Figure 4. Immediately after the third coefficient is loaded, the first coefficient of the next set can be loaded, if desired, along with the third data point.

Table 1. Impulse Response

FT_{3-1}	Response					
000	C_3	0	C_2	0	C_1	0
001	C_3	0	C_2	0	C_1	
010	C_3	0	C_2	C_1	0	
011	C_3	0	C_2	C_1		
100	C_3	C_2	0	C_1	0	
101	C_3	C_2	0	C_1		
110	C_3	C_2	C_1	0		
111	C_3	C_2	C_1			

Notes:
1. C_3 is the rightmost coefficient, C_1 is the leftmost.
2. FT_1 is relevant only if SUMIN is used. When multiple chips are cascaded, FT_1 = LOW places a zero stage between their concatenated impulse responses.

Building Longer Filters

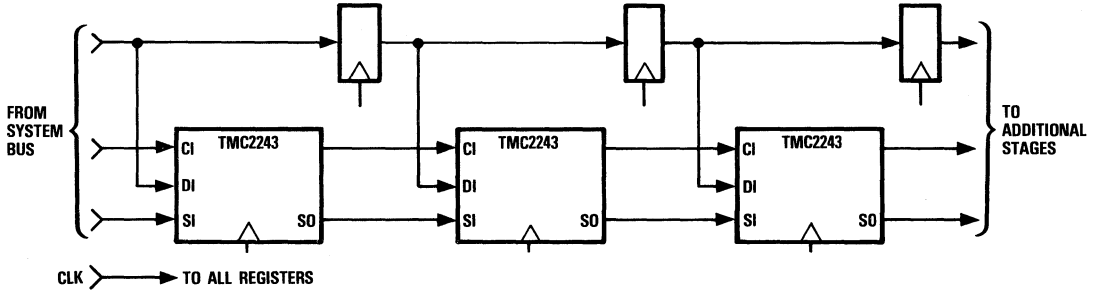
To build a filter of more than three non-zero stages, merely concatenate a series of TMC2243s. The coefficient inputs may be connected to the data bus, a separate common coefficient bus, or separate buses, depending on system architecture, memory and bus resources, and coefficient updating requirements. The data inputs are connected to a common bus. If the first feedthrough register is used (and a zero stage is not desired there), an external register should be inserted in the data input path for proper timing (Figure 9).

The 16-bit Sum-Out port of each TMC2243 is connected to the Sum-In port of the next TMC2243 in the chain; the filter output is the Sum-Out port of the last TMC2243. Since the 6 LSBs of each TMC2243's accumulation pipeline are not output, each TMC2243 incorporates a rounding increment of 1 into the sixth bit, to minimize bias.

When TMC2243s are cascaded in this fashion, the minimum permissible clock period is the sum of the output delay and the Sum-In port's input setup time. When the Input Registers are enabled (that is, FT_1 = LOW), full 20MHz performance can be obtained.

All data and coefficient inputs and outputs are two's complement representation, whose relative scaling is presented in the Data Formats table, Figure 1. Although the data values are shown in fractional format, the user can arbitrarily rescale them, as long as consistency is maintained.

Figure 9. Basic Diagram for Stacking the TMC2243 for High-Speed Operation (no zero tap desired between each TMC2243, all FT_1 = LOW)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2243G8C	STD–T_A=0°C to 70°C	Commercial	68 Pin Grid Array	2243G8C
TMC2243G8V	EXT–T_C=–55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2243G8V
TMC2243H8C	STD–T_A=0°C to 70°C	Commercial	69 Pin Plastic Pin Grid Array	2243H8C

40G02174 Rev D 8/93

TMC2246
CMOS Image Filter
11 x 10 Bit, 40 MHz

Description

The TMC2246 is a video speed The TMC2246 is a video speed convolutional array composed of four 11 x 10 bit registered multipliers followed by a summer and an accumulator. All eight multiplier inputs are accessible to the user and may be updated every clock cycle with integer or fractional two's complement data. A pipelined architecture, fully registered input and output ports, and asynchronous three-state output enable control simplify the design of complex systems.

The data or coefficient inputs to the multipliers may be held over multiple clock cycles, providing storage for mixing and filtering coefficients. The 25-bit accumulator path of the TMC2246 allows two bits of cumulative word growth which may be internally rounded to 16 bits. Output data are updated very 25 ns clock cycle, and may be held under user control. All data inputs, outputs, and controls are TTL compatible and are registered on the rising edge of clock, except the three-state output enable.

The TMC2246 is uniquely suited to performing pixel interpolation in image manipulation and filtering applications. As a companion to the Raytheon Semiconductor TMC2301 Image Resampling Sequencer, the TMC2246 Image Filter can execute a bilinear interpolation of an image (4-pixel kernels) at real-time video rates. Larger kernels or other more complex functions can be realized with no loss in performance by utilizing multiple devices.

With unrestricted access to all data and coefficient input ports, the TMC2246 offers considerable flexibility in applications performing digital filtering, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

Fabricated using Raytheon Semiconductor's proprietary OMICRON-C™ one-micron CMOS process, the TMC2246 operates at a guaranteed clock rate of 40 MHz over the full temperature and supply voltage ranges, and is available in a 120-pin plastic pin grid array.

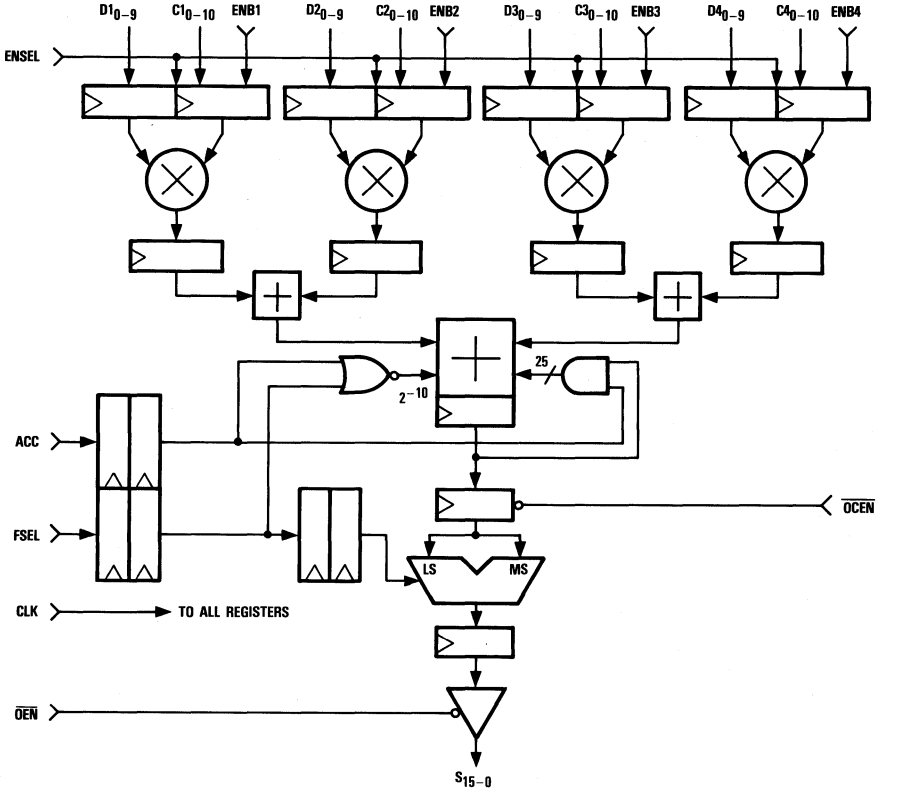
Features

- 40 MHz data and coefficient input and computation rate
- Four 11 x 10 bit multipliers with individual data and coefficient inputs and 25-bit accumulator
- User-selectable fractional or integer two's complement data formats
- Input and output data latches, with user-configurable enables
- User-selectable 16-bit rounded output
- Internal 1/2 LSB rounding
- Fully registered, pipelined architecture
- Low power consumption CMOS process
- Single +5V supply
- Available in 120-pin plastic grid array

Applications

- Fast pixel interpolation
- Fast image manipulation
- Image mixing and keying
- High-performance FIR filters
- Adaptive digital filters
- One and two dimensional image processing

Functional Block Diagram



Functional Description

General Information

The TMC2246 Image Filter is a flexible multiplier-summer array which computes the accumulated sum of four 11 x 10 bit products, allowing word growth up to 25 bits. The inputs are user-configurable, allowing latching of either the 10 or 11-bit input data. The data format is user-selectable between integer or fractional two's complement arithmetic. Total latency from input registers to output data port is five clocks. The output data path is 16 bits wide, providing the lower 16 bits of the accumulator when in integer format or the upper 16 bits of the 25-bit accumulator path when fractional two's complement notation is selected. One-time rounding to 16 bits is performed when accumulating fractional data, which is disabled when operating in integer format to maintain the integrity of the least-significant bits.

Signal Definitions

Power

V_{DD}, GND — The TMC2246 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The TMC2246 operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.

Inputs

D1$_{9-0}$ – D4$_{9-0}$ — D1 through D4 are the 10-bit data input ports. The LSB is Dx$_0$. See *Figure 1*.

Inputs (cont.)

$C1_{10-0}$–$C4_{10-0}$ C1 through C4 are the 11-bit coefficient input ports. The LSB is Cx_0. See *Figure 1*.

Outputs

S_{15-0} The current 16-bit result is available at the Sum output. The LSB is S_0. See *Figure 1*.

Controls

FSEL Data input during the current clock is assumed to be in fractional two's complement format, rounding to 16 bits is performed as determined by the accumulator control ACC, and the upper 16 bits of the accumulator are output when the registered Format Select input is LOW. When FSEL is HIGH, two's complement integer format is assumed, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when operating in integer mode. See *Figure 1* and the *Applications Discussion*.

ENSEL The registered Enable Select determines whether the data or the coefficient input registers may be held on the next rising edge of clock, in conjunction with the individual input enables ENB1–ENB4. See *Figure 2*.

ENB1–ENB4 When ENBi (i=1, 2, 3, or 4) is LOW, registers Ci and Di are both strobed by the next rising edge of CLK. When ENBi is HIGH and ENSEL is LOW, Di is strobed, but Ci is held. When ENBi and ENSEL are both HIGH, Di is held and Ci is strobed. See *Figure 2*. Thus, either or both input registers to each multiplier are updated on each clock cycle.

Figure 2. Input Register Control

ENB1–4	ENSEL	Input Register Held
1	1	Data i
1	0	Coefficient i
0	X	None

Where X denotes a "Don't Care" condition. Any register not explicitly held is updated on the next rising edge of clock.

ACC When the registered Accumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. If operating in fractional two's complement format (FSEL=LOW), one-half LSB rounding to 16 bits is performed on the result. This allows the user to perform summations without propagating roundoff errors. When ACC is HIGH, the internal accumulator adds the emerging product to the sum of previous products, without performing additional rounding.

$\overline{OCEN}$ The output of the accumulator is latched into the output register on the next clock when the registered Clock Enable is LOW. When $\overline{OCEN}$ is HIGH the contents of the output register remain unchanged, however accumulation will continue internally if ACC remains HIGH.

$\overline{OEN}$ Data currently in the output registers is available at the output bus S_{15-0} when the asynchronous Output Enable is LOW. When $\overline{OEN}$ is HIGH, the outputs are in the high-impedance state.

Figure 1. Data Formats

Fractional Two's Complement Format (FSEL = LOW)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						-2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	DATA (D_{1-4})
					-2^1	2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	COEFFICIENT (C_{1-4})
-2^6	2^5	2^4	2^3	2^2	2^1	2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	SUM

Integer Two's Complement Format (FSEL = HIGH)

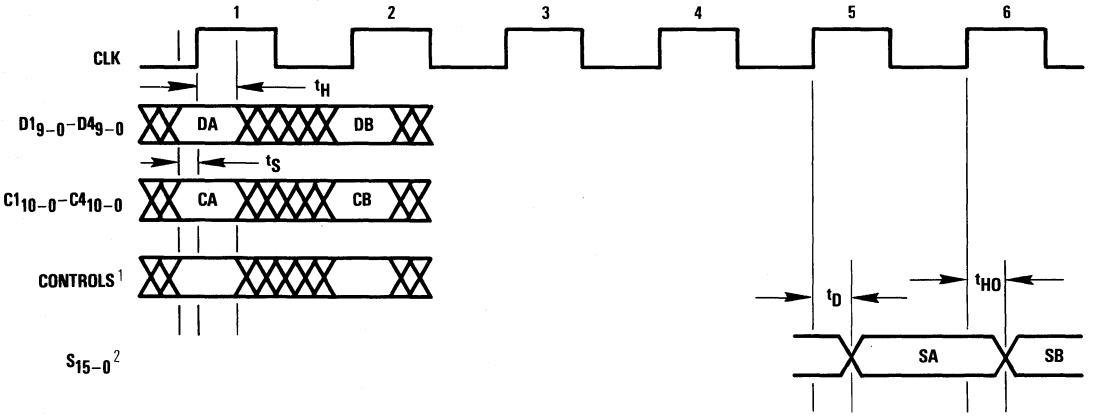
						-2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DATA (D_{1-4})
					-2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	COEFFICIENT (C_{1-4})
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	SUM

Note: A minus sign indicates the sign bit.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8	13, 21, 50, 112
	GND	Ground	E3, G3, J3, L6, H11, C7	9, 17, 25, 46, 79, 116
Clock	CLK	System Clock	C3	2
Inputs	$D1_{9-0}$	D1 Input	M1, K3, L2, N1, L3, M2, N2, L4, M3, N3	28, 29, 30, 31, 35, 36, 37, 38, 39, 40
	$D2_{9-0}$	D2 Input	J12, K13, J11, K12, L13, L12, K11, M13, M12, L11	77, 76, 75, 74, 73, 72, 71, 70, 69, 68
	$D3_{9-0}$	D3 Input	J13, H12, H13, G12, G11, G13, F13, F12, F11, E13	78, 80, 81, 82, 83, 84, 85, 86, 87, 88
	$D4_{9-0}$	D4 Input	B4, C5, A4, B5, A5, C6, B6, A6, A7, B7	125, 124, 123, 122, 121, 120, 119, 118, 117, 115
	$C1_{10-0}$	C1 Input	M4, L5, N4, M5, N5, M6, N6, M7, N7, N8, M8	41, 42, 43, 44, 45, 47, 48, 49, 51, 52, 53
	$C2_{10-0}$	C2 Input	N13, M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54
	$C3_{10-0}$	C3 Input	E12, D13, E11, D12, C13, B13, D11, C12, A13, C11, B12	89, 90, 91, 92, 93, 94, 95, 96, 97, 101, 102
	$C4_{10-0}$	C4 Input	A8, B8, A9, B9, A10, C9, B10, A11, B11, C10, A12	114, 113, 111, 110, 109, 108, 107, 106, 105, 104, 103
Outputs	S_{15-0}	Sum Output	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	7, 8, 10, 11, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 26, 27
Controls	FSEL	Format Select	B2	3
	ENSEL	Enable Select	A1	130
	ENB1 – ENB4	Input Enables	C4, A2, A3, B3	128, 127, 126, 129
	ACC	Accumulate	B1	4
	$\overline{OCEN}$	Output Register Enable	D3	5
	$\overline{OEN}$	Output Enable	C2	6
No Connect		Not Connected	D4 (Index Pin)	1, 32, 33, 34, 65, 66, 67, 98, 99, 100, 131, 132

Figure 3. Timing Diagram



Notes: 1. Except $\overline{OEN}$.
2. Assumes $\overline{OEN}$ = LOW.

Figure 4. Equivalent Input Circuit

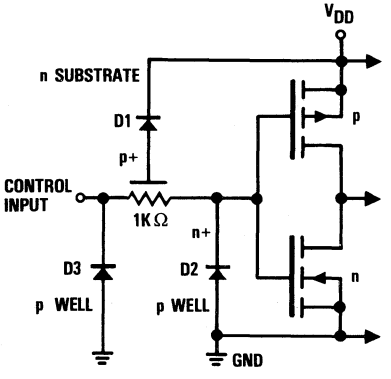


Figure 5. Equivalent Output Circuit

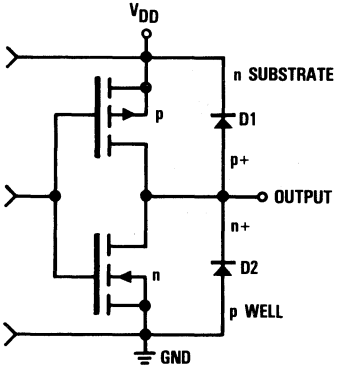
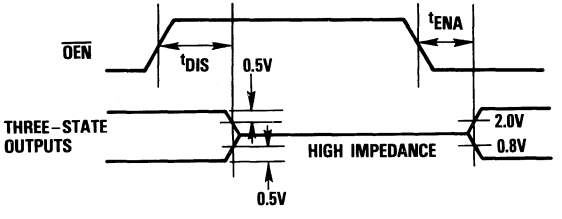


Figure 6. Threshold Levels for Three-State Measurement



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+0.5)V

Output

Applied voltage [2] ..... −0.5 to (V_{DD}+0.5)V

Forced current [3,4] ..... −6.0 to 6.0mA

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH				−2.0			−2.0	mA
t_{CY}	Cycle Time	V_{DD}=Min							
		TMC2246	33						ns
		TMC2246-1	25						ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min							
		TMC2246	15						ns
		TMC2246-1	10						ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	10						ns
t_S	Input Setup Time	TMC2246	10						ns
		TMC2246-1	8						ns
t_H	Input Hold Time		2						ns
T_A	Ambient Temperature, Still Air		0		70				°C
T_C	Case Temperature					−55		125	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		6			mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, $\overline{OEN}$=5V, f=30MHz		100			mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V	−10		−10		µA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		10		10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V	−40		−40		µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		40		40	µA
I_{OS}	Short-Circuit Output	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.		60		60	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but operation is guaranteed as specified.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended [2]		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD}=Min, C_{LOAD}=25pF					
		TMC2246		15			ns
		TMC2246-1		13			ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=25pF	5				ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD}=Min, C_{LOAD}=25pF		15			ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD}=Min, C_{LOAD}=25pF		20			ns

Notes: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.
2. Consult factory for extended temperature specifications.

Applications Discussion

Demonstration of Operation

The versatile input clock enables and unrestricted data and coefficient inputs provided on the TMC2246 allow considerable flexibility in numerous image and signal processing architectures. *Figure 7* shows a typical sequence of operations which clarifies the inherent clock latencies of the device and illustrates fixed coefficient storage, product accumulation, and device reconfiguration prior to beginning a new accumulation. This assumes that the device is set to fractional two's complement mode (FSEL = LOW), with $\overline{OCEN}$ = LOW, $\overline{OEN}$ = LOW, and the input registers configured to hold coefficients only (ENSEL = LOW). X = "don't care."

Figure 7. Typical TMC2246 Operation Sequence

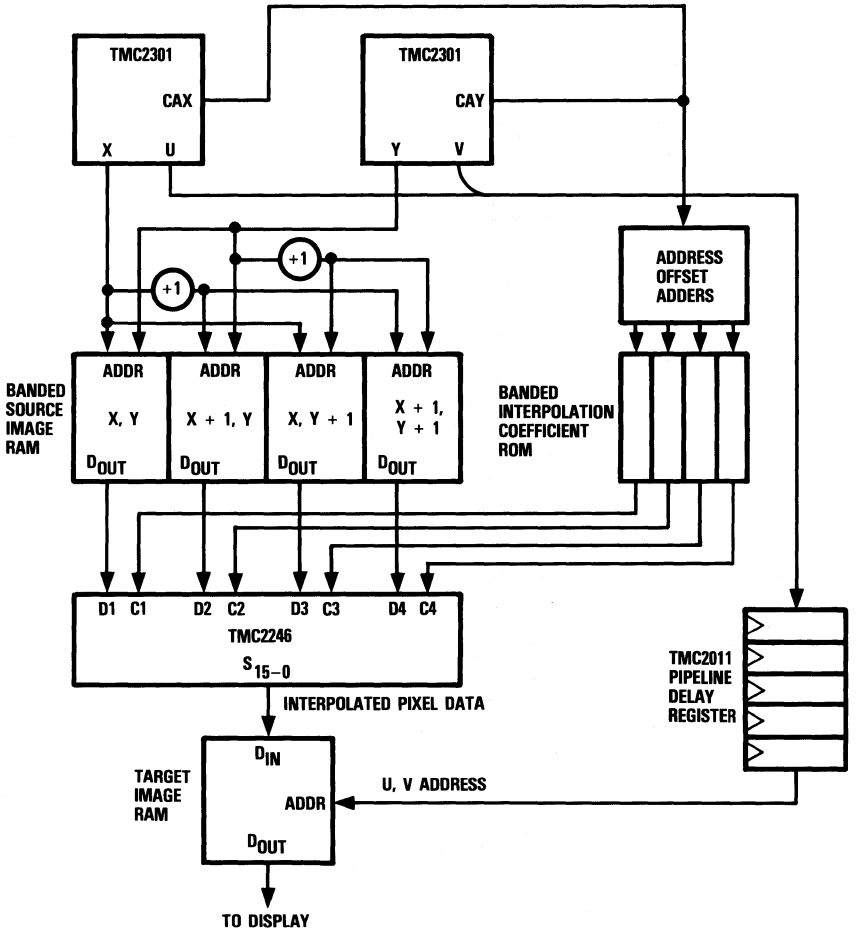
CLK	D1	C1	ENB_1	D2	C2	ENB_2	D3	C3	ENB_3	D4	C4	ENB_4	ACC	Sum
0	–	–	0	–	–	0	–	–	0	–	–	0	–	–
1	D1(1)	C1(1)	1	D2(1)	C2(1)	1	D3(1)	C3(1)	1	D4(1)	C4(1)	1	0	–
2	D1(2)	X	0	D2(2)	X	0	D3(2)	X	1	D4(2)	X	1	1	–
3	D1(3)	C1(3)	0	D2(3)	C2(3)	0	D3(3)	X	0	D4(3)	X	0	1	
4	D1(4)	C1(4)	–	D2(4)	C2(4)	–	D3(4)	C3(4)	–	D4(4)	C4(4)	–	0	
5														$S(5) = D1(1)C1(1) + D2(1)C2(1) + D3(1)C3(1) + D4(1)C4(1) + 2^{-10}$
6														$S(6) = S(5) + D1(2)C1(1) + D2(2)C2(1) + D3(2)C3(1) + D4(2)C4(1)$
7														$S(7) = S(6) + D1(3)C1(3) + D2(3)C2(3) + D3(3)C3(1) + D4(3)C4(1)$
8														$S(8) = D1(4)C1(4) + D2(4)C2(4) + D3(4)C3(4) + D4(4)C4(4) + 2^{-10}$

Notice in this example, operating in fractional two's complement mode, that rounding is imposed on the first cycle only of an accumulation. This avoids the propagation of accumulated roundoff errors.

Using the TMC2246 for Pixel Interpolation

As a companion product to the TMC2301 Image Resampling Sequencer, the TMC2246 offers an excellent tool for performing high-speed pixel interpolation and image filtering. Any pixel resampling operation with multiple-pixel kernels must utilize some parallel-processing technique, such as memory banding, in order to maintain high-speed image throughput rates. Memory Banding utilizes adders to generate parallel offset addresses, allowing the user to access multiple pixel locations simultaneously. Using such techniques, one TMC2246 can perform bilinear interpolation (four-pixel kernel) with no loss in system performance. Larger kernels can be realized in similar systems with additional TMC2246s. See TRW *Application Brief AB-4, "Performing Bilinear Interpolation Using the TMC2301". Figure 8* illustrates a basic pixel interpolation application.

Figure 8. Bilinear Interpolation Using the TMC2246

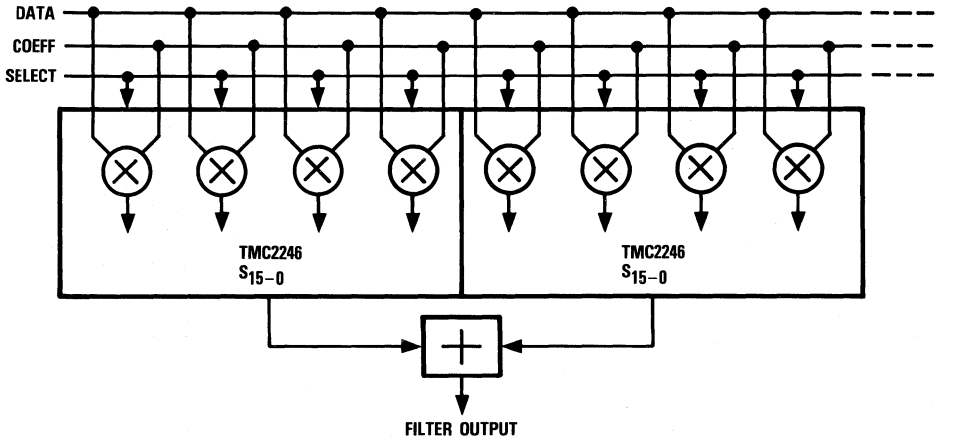


TMC2246 Applications in Digital Filtering

Unrestricted access to all input ports of the TMC2246 allows the user considerable flexiblity in realizing numerous digital filter architectures. *Figure 9* illustrates how the device may be utilized as a flexible high-speed FIR Filter with the ability to modify all of the filter coefficients dynamically or to store a fixed set if desired.

Longer filters, with more taps, are realized by including an external adder (such as the common 74381 type) to cascade multiple TMC2246s. Alternatively, two additional taps and a cascading adder are available in the TRW *TMC2249 Digital Mixer*.

Figure 9. Utilization of the TMC2246 for FIR Filtering

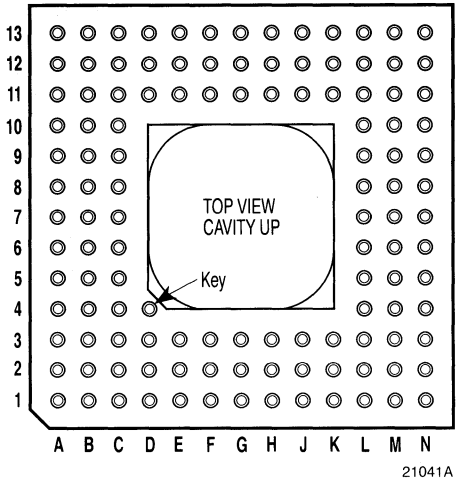


Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package

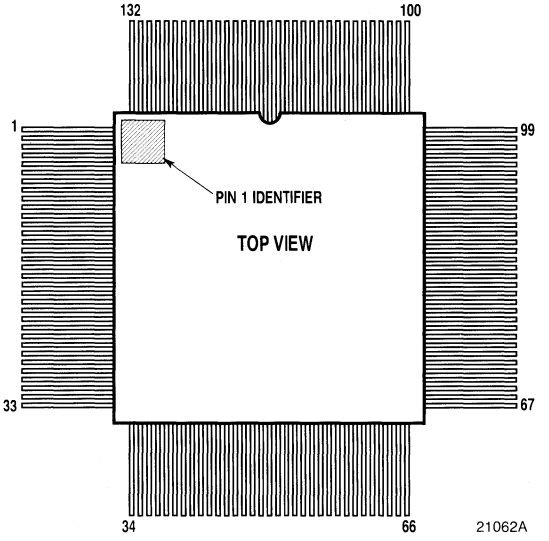
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	CLK	G3	GND	L3	$D1_5$	L7	V_{DD}	L11	$D2_0$	G11	$D3_5$	C11	$C3_1$	C7	GND
B2	FSEL	G1	S_7	M2	$D1_4$	N7	$C1_2$	M12	$D2_1$	G13	$D3_4$	B12	$C3_0$	A7	$D4_1$
B1	ACC	H1	S_6	N2	$D1_3$	N8	$C1_1$	M13	$D2_2$	F13	$D3_3$	A12	$C4_0$	A6	$D4_2$
D3	$\overline{OCEN}$	H2	S_5	L4	$D1_2$	M8	$C1_0$	K11	$D2_3$	F12	$D3_2$	C10	$C4_1$	B6	$D4_3$
C2	$\overline{OEN}$	H3	V_{DD}	M3	$D1_1$	L8	$C2_0$	L12	$D2_4$	F11	$D3_1$	B11	$C4_2$	C6	$D4_4$
C1	S_{15}	J1	S_4	N3	$D1_0$	N9	$C2_1$	L13	$D2_5$	E13	$D3_0$	A11	$C4_3$	A5	$D4_5$
D2	S_{14}	J2	S_3	M4	$C1_{10}$	M9	$C2_2$	K12	$D2_6$	E12	$C3_{10}$	B10	$C4_4$	B5	$D4_6$
E3	GND	K1	S_2	L5	$C1_9$	N10	$C2_3$	J11	$D2_7$	D13	$C3_9$	C9	$C4_5$	A4	$D4_7$
D1	S_{13}	J3	GND	N4	$C1_8$	L9	$C2_4$	K13	$D2_8$	E11	$C3_8$	A10	$C4_6$	C5	$D4_8$
E2	S_{12}	K2	S_1	M5	$C1_7$	M10	$C2_5$	J12	$D2_9$	D12	$C3_7$	B9	$C4_7$	B4	$D4_9$
E1	S_{11}	L1	S_0	N5	$C1_6$	N11	$C2_6$	J13	$D3_9$	C13	$C3_6$	A9	$C4_8$	A3	ENB3
F3	V_{DD}	M1	$D1_9$	L6	GND	N12	$C2_7$	H11	GND	B13	$C3_5$	C8	V_{DD}	A2	ENB2
F2	S_{10}	K3	$D1_8$	M6	$C1_5$	L10	$C2_8$	H12	$D3_8$	D11	$C3_4$	B8	$C4_9$	C4	ENB1
F1	S_9	L2	$D1_7$	N6	$C1_4$	M11	$C2_9$	H13	$D3_7$	C12	$C3_3$	A8	$C4_{10}$	B3	ENB4
G2	S_8	N1	$D1_6$	M7	$C1_3$	N13	$C2_{10}$	G12	$D3_6$	A13	$C3_2$	B7	$D4_0$	A1	ENSEL

Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	23	S_3	45	$C1_6$	67	NC	89	$C3_{10}$	111	$C4_8$
2	CLK	24	S_2	46	GND	68	$D2_0$	90	$C3_9$	112	V_{DD}
3	FSEL	25	GND	47	$C1_5$	69	$D2_1$	91	$C3_8$	113	$C4_9$
4	ACC	26	S_1	48	$C1_4$	70	$D2_2$	92	$C3_7$	114	$C4_{10}$
5	OCENB	27	S_0	49	$C1_3$	71	$D2_3$	93	$C3_6$	115	$D4_0$
6	OENB	28	$D1_9$	50	V_{DD}	72	$D2_4$	94	$C3_5$	116	GND
7	S_{15}	29	$D1_8$	51	$C1_2$	73	$D2_5$	95	$C3_4$	117	$D4_1$
8	S_{14}	30	$D1_7$	52	$C1_1$	74	$D2_6$	96	$C3_3$	118	$D4_2$
9	GND	31	$D1_6$	53	$C1_0$	75	$D2_7$	97	$C3_2$	119	$D4_3$
10	S_{13}	32	NC	54	$C2_0$	76	$D2_8$	98	NC	120	$D4_4$
11	S_{12}	33	NC	55	$C2_1$	77	$D2_9$	99	NC	121	$D4_5$
12	S_{11}	34	NC	56	$C2_2$	78	$D3_9$	100	NC	122	$D4_6$
13	V_{DD}	35	$D1_5$	57	$C2_3$	79	GND	101	$C3_1$	123	$D4_7$
14	S_{10}	36	$D1_4$	58	$C2_4$	80	$D3_8$	102	$C3_0$	124	$D4_8$
15	S_9	37	$D1_3$	59	$C2_5$	81	$D3_7$	103	$C4_0$	125	$D4_9$
16	S_8	38	$D1_2$	60	$C2_6$	82	$D3_6$	104	$C4_1$	126	EN3B
17	GND	39	$D1_1$	61	$C2_7$	83	$D3_5$	105	$C4_2$	127	EN2B
18	S_7	40	$D1_0$	62	$C2_8$	84	$D3_4$	106	$C4_3$	128	EN1B
19	S_6	41	$C1_{10}$	63	$C2_9$	85	$D3_3$	107	$C4_4$	129	EN4B
20	S_5	42	$C1_9$	64	$C2_{10}$	86	$D3_2$	108	$C4_5$	130	ENSEL
21	V_{DD}	43	$C1_8$	65	NC	87	$D3_1$	109	$C4_6$	131	NC
22	S_4	44	$C1_7$	66	NC	88	$D3_0$	110	$C4_7$	132	NC



120 Pin Plastic Pin Grid Array – H5 Package



132 Leaded CERQUAD – L5 Package

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2246H5C	STD – T_A = 0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2246H5C
TMC2246H5C1	STD – T_A = 0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2246H5C1
TMC2246L5V	EXT – T_C = –55°C to 125°C	MIL-STD-883	132 Leaded CERQUAD	2246L5V
TMC2246L5V1	EXT – T_C = –55°C to 125°C	MIL-STD-883	132 Leaded CERQUAD	2246L5V1

40G06126 Rev E 8/93

TMC2249
CMOS Digital Mixer
12 x 12 Bit, 30 MHz

Description

The TMC2249 is a high-speed digital arithmetic circuit consisting of two 12-bit multipliers, an adder and a cascadeable accumulator. All four multiplier inputs are accessible to the user, and each includes a user-programmable pipeline delay of up to 16 clocks in length. The 24-bit adder/subtractor is followed by an accumulator and 16-bit input port which allows the user to cascade multiple TMC2249s. A new 16-bit accumulated output is available every clock, up to the maximum rate of 30 MHz. All inputs and outputs are registered except the three-state output enable, and all are TTL compatible.

The TMC2249 utilizes a pipelined, bus-oriented structure offering significant flexibility. Input register clock enables and programmable input data pipeline delays on each port offer an adaptable input structure for high-speed digital systems. Following the multipliers, the user may perform addition or subtraction of either product, arithmetic rounding to 16-bits, and accumulation and summation of products with a cascading input. The output port allows access to all 24 bits of the internal accumulator by switching between overlapping least and most-significant 16-bit words, and a three-state output enable simplifies a connection to an external system bus.

All programmable features are utilized on a clock-by-clock basis, with internal data and control pipeline registers provided to maintain synchronous operation between incoming data and all available functions within the device.

The TMC2249 has numerous applications in digital processing algorithms, from executing simple image mixing and switching, to performing complex arithmetic functions and complex waveform synthesis. FIR filters, digital quadrature mixers and modulators, and vector arithmetic functions may also be implemented with this device.

Fabricated using a one-micron CMOS process, the TMC2249 operates at a guaranteed clock rate of 30 MHz over the standard commercial temperature and supply voltage ranges, and is available in a low-cost 120 pin plastic pin grid array.

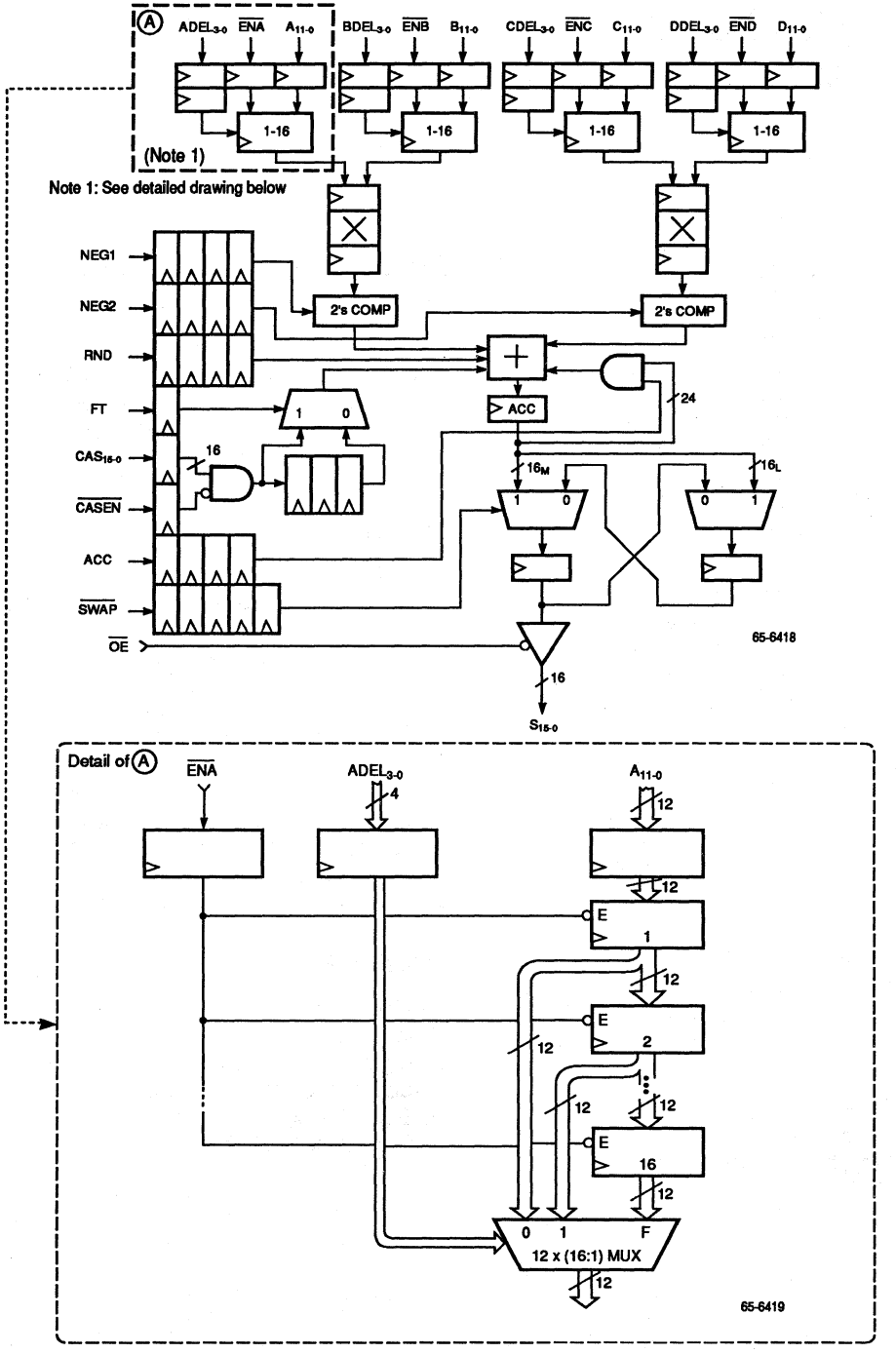
Features

- 30 MHz input and computation rate
- Two 12-bit multipliers with spearate data and coefficient inputs
- Independent, user-selectable pipleline delays of 1 to 16 clocks on all inputs ports
- Separate 16-bit input port allows cascading or addition of a constant
- User-selectable rounded output
- Internal 1/2 LSB rounding og products
- Fully registered, pipelined architecture
- Low power consumption CMOS process
- Single +5V power supply
- Available in 120-pin plastic grid array

Applications

- Video switching
- Image mixing
- Digital signal modulation
- Complex frequency synthesis
- Digital filtering
- Complex arithmetic functions

Functional Block Diagram



Functional Description

General Information

The TMC2249 performs the summation of products described by the formula:

$$S(N+6) = A(N-ADEL) \cdot B(N-BDEL) \cdot (-1^{NEG1(N)})$$
$$+ C(N-CDEL) \cdot D(N-DDEL) \cdot (-1^{NEG2(N)}) + CAS(N+3 \cdot FT)$$

where ADEL through DDEL range from 1 to 16 pipe delays. All inputs and controls utilize pipeline delay registers to maintain synchronicity with the data input during that clock, except when the Cascade data input is routed directly to the accumulator by use of the Feedthrough control. One-half LSB rounding to 16 bits may be performed on the sum of products while summing with the cascade input data. The user may access either the upper or lower 16 bits of the 24-bit accumulator by swapping overlapping registers. The output bus has an asynchronous high-impedance enable, to simplify interfacing to complex systems.

Signal Definitions

Power

V_{DD}, GND — The TMC2249 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK — The TMC2249 operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.

Inputs

A_{11-0} – D_{11-0} A through D are the four 12-bit registered data input ports. A_0-D_0 are the LSBs. See *Table 1*. Data presented to the input ports is clocked in to the top of the 16-stage delay pipeline on the next clock when enabled, "pushing" data down the register stack.

CAS_{15-0} CAS is the 16-bit Cascade data input port. CAS_0 is the LSB. See *Table 1*.

Outputs

S_{15-0} The current 16-bit result is available at the Sum output. The LSB is S_0. The output may be the most or least significant 16 bits of the current accumulator output, as determined by $\overline{SWAP}$. S_0 is the LSB. See *Table 1*.

Controls

$\overline{ENA}$ – $\overline{END}$ Input data presented to port i11-0 (i = A, B, C, or D) are latched into delay pipeline i, and data already in pipeline i advance by one register position, on each rising edge of CLK for which ENi is LOW. When ENi is HIGH, the data in pipeline i do not move and the value at the input port i will be lost before it reaches the multiplier.

$ADEL_{3-0}$ – $DDEL_{3-0}$ ADEL through DDEL are the four-bit registered input data pipe delay select word inputs. Data to be presented to the multipliers is selected from one of sixteen stages in the input data delay pipe registers, as indicated by the delay select word presented to the respective input port during that clock. The minimum delay is one clock (select word = 0000), and the maximum delay is 16 clocks (select word = 1111). Following powerup these values are indeterminate and must be initialized by the user.

NEG1, NEG2 The products of the multipliers are negated, causing a subtraction to be performed during the internal summation of products, when the Negate controls are HIGH. NEG1 negates the product A x B, while NEG2 acts on the output of the multiplier which generates the product C x D. These controls indicate the operation to be performed on data input during the current clock, when the length controls ADEL – DDEL are set to zero.

RND When the rounding control is HIGH, the sum of products resulting from data input during that clock is rounded to 16 bits. Rounding is performed only during the first cycle of each accumulation sequence, to avoid the accumulation of roundoff errors.

FT When the Feedthrough control is HIGH, the pipeline delay through the cascade data path is minimized to simplify the cascading of multiple devices. When FT is LOW and ADEL through DDEL are all set to 0, the data inputs are aligned, such that $S(n+6) = CAS(n) + A(n)B(n) + C(n)D(n)$. See *Table 2*.

$\overline{CASEN}$ Data presented at the cascade data input port are latched and accumulated internally when the input enable $\overline{CASEN}$ during that clock is LOW. When $\overline{CASEN}$ is HIGH, the cascade input port is ignored.

ACC When the registered Accumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. When ACC is HIGH, the internal accumulator adds the emerging product to the sum of previous products.

$\overline{SWAP}$ The user may access both the most and least-significant 16 bits of the 24-bit accumulator by utilizing $\overline{SWAP}$. Normal operation of the device, with $\overline{SWAP}$ = HIGH, outputs the most significant word. Setting $\overline{SWAP}$ = LOW puts a double-register structure into "toggle" mode, allowing the user to examine the LSW on alternate clocks. New output data will not be clocked into the output registers until $\overline{SWAP}$ returns HIGH.

$\overline{OE}$ Data currently in the output registers is available at the output bus S_{15-0} when the asynchronous Output Enable is LOW. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state.

Table 1. Data Formats and Bit Weighting

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
				-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DATA INPUT ($A_{11-0} - D_{11-0}$)
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	CASCADE INPUT (CAS_{15-0})
																SUM (S_{15-0})
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSW
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	MSW

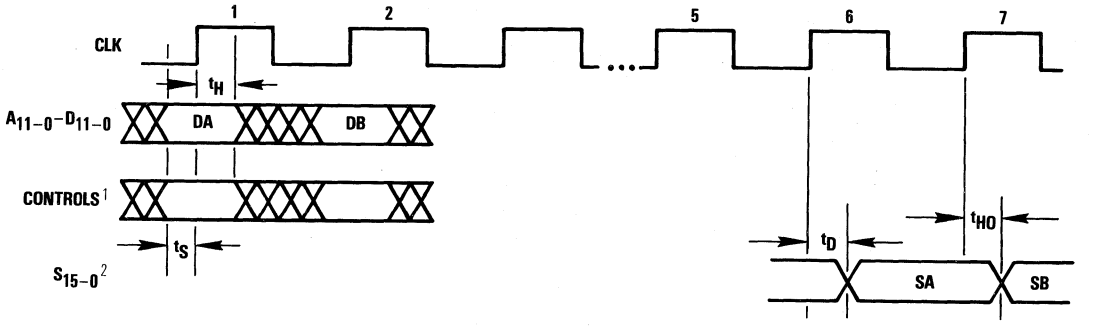
Note: 1. A minus sign indicates the sign bit.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8	13, 21, 50, 112
	GND	Ground	E3, G3, J3, L6, H11, C7	9, 17, 25, 46, 79, 116
Clock	CLK	System Clock	C3	2
Inputs	A_{11-0}	A Input	N8, M8, L8, N9, M9, N10, L9, M10, N11, N12, L10, M11	52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63
	B_{11-0}	B Input	N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, L4	51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 39, 38
	C_{11-0}	C Input	A9, B9, A10, C9, B10, A11, B11, C10, A12, B12, C11, A13	111, 110, 109, 108, 107, 106, 105, 104, 103, 102, 101, 100
	D_{11-0}	D Input	B8, A8, B7, A7, A6, B6, C6, A5, B5, A4, C5, B4	113, 114, 115, 117, 118, 119, 120, 121, 122, 123, 124, 125
	$ADEL_{3-0}$	A Delay	L11, M12, M13, K11	68, 69, 70, 71
	$BDEL_{3-0}$	B Delay	M2, L3, N1, L2	36, 35, 31, 30
	$CDEL_{3-0}$	C Delay	D11, B13, C13, D12	95, 94, 93, 92
	$DDEL_{3-0}$	D Delay	A2, C4, B3, A1	127, 128, 129, 130
	CAS_{15-0}	Cascade Input	L13, K12, J11, K13, J12, J13, H12, H13, G12, G11, G13, F13, F12, F11, E13, E12	73, 74, 75, 76, 77, 78, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89
Outputs	S_{15-0}	Sum Output	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	7, 8, 10, 11, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 26, 27
Controls	$\overline{ENA} - \overline{END}$	Input Enables	N13, N2, C12, A3	64, 37, 96, 126
	NEG1, NEG2	Negate	B1, D3	4, 5
	RND	Round	C2	6
	FT	Feedthrough	E11	91
	$\overline{CASEN}$	Cascade Enable	D13	90
	ACC	Accumulate	B2	3
	$\overline{SWAP}$	Swap Output Words	K3	29
	$\overline{OE}$	Output Enable	M1	28
No Connect	NC	None	L12	1, 32, 33, 34, 65, 66, 67, 72, 98, 99, 100, 131, 132
		Index Pin	D4	

Multimedia

Figure 1. Timing Diagram



Notes: 1. Except $\overline{OE}$.
2. Assumes $\overline{OE}$ = LOW, and ADEL – DDEL set to 0.

Figure 2. Equivalent Input Circuit

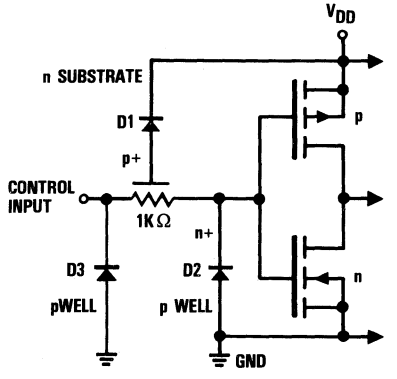


Figure 3. Equivalent Output Circuit

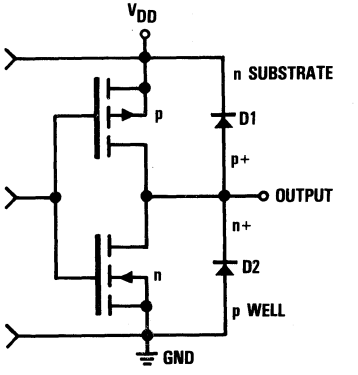
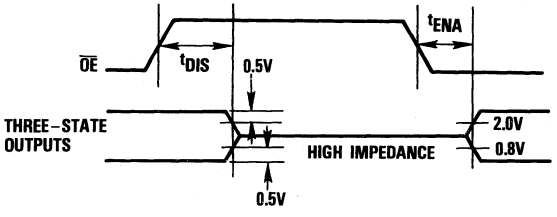


Figure 4. Threshold Levels for Three-State Measurement



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+0.5)V

Output

Applied voltage [2] ..... −0.5 to (V_{DD}+0.5)V

Forced current [3,4] ..... −6.0 to 6.0mA

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended [1]			
			Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH				−2.0			−2.0	mA
t_{CY}	Cycle Time	V_{DD}=Min							
		TMC2249	40						ns
		TMC2249-1	33						ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	15						ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	10						ns
t_S	Input Setup Time		8						ns
t_H	Input Hold Time		4						ns
T_A	Ambient Temperature, Still Air		0		70				°C
T_C	Case Temperature					−55		125	°C

Note: 1. Consult factory for extended temperature specifications.

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		6			mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, $\overline{OEN}$=5V, f=25MHz		100			mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V	−40		−40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.		60		60	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but operation is guaranteed as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD}=Min, C_{LOAD}=25pF					
		TMC2249		17			ns
		TMC2249-1		15			ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=25pF	5				ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD}=Min, C_{LOAD}=25pF		15			ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD}=Min, C_{LOAD}=25pF		20			ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Applications Discussion

Basic Operation

The TMC2249 is a flexible signal and image processing building block with numerous user-selectable functions which expand it's usefulness. *Table 2* clarifies the operation of the device, demonstrating the various features available to the user and the timing delays incurred.

Table 2. TMC2249 Operation Sequence

CLK	ADEL	A_{11-0}	BDEL	B_{11-0}	CDEL	C_{11-0}	DDEL	D_{11-0}	NEG1	NEG2	CAS_{15-0}	FT	ACC	RND	$\overline{SWAP}$	S_{15-0}
1	0	A(1)	0	B(1)	0	C(1)	0	D(1)	L	L	—	L	L	L	H	—
2	0	A(2)	0	B(2)	0	C(2)	0	D(2)	L	H	—	L	L	L	H	—
3	0	A(3)	0	B(3)	0	C(3)	0	D(3)	H	L	—	L	L	L	H	—
4	0	A(4)	0	B(4)	0	C(4)	0	D(4)	L	L	CAS(4)	L	L	L	H	—
5	0	A(5)	0	B(5)	0	C(5)	0	D(5)	L	L	—	L	L	L	H	—
6	0	A(6)	0	B(6)	0	C(6)	0	D(6)	L	L	—	L	L	H	H	$(A(1)\cdot B(1)+C(1)\cdot D(1))_{ms}$
7	0	A(7)	0	B(7)	0	C(7)	0	D(7)	L	L	—	L	H	H	H	$(A(2)\cdot B(2)-C(2)\cdot D(2))_{ms}$
8	0	A(8)	0	B(8)	0	C(8)	0	D(8)	L	L	CAS(8)	H	L	L	L	$(-A(3)\cdot B(3)+C(3)\cdot D(3))_{ms}$
9	0	A(9)	0	B(9)	0	C(9)	0	D(9)	L	L	—	L	L	L	H	$(A(4)\cdot B(4)+C(4)\cdot D(4)+CAS(4))_{ms}$
10																$(A(5)\cdot B(5)+C(5)\cdot D(5)+CAS(8))_{ms}$
11																$(A(6)\cdot B(6)+C(6)\cdot D(6)+2^7)_{ms}$
12																$(A(7)\cdot B(7)+C(7)\cdot D(7)+S(11))_{ms}$
13																$(S(12))_{ls}$
14																$(A(9)\cdot B(8)+C(7)\cdot D(6))_{ms}$

Where H=HIGH, L=LOW. "ms" indicates most significant output word (bits 23–8), "ls" indicates least significant word (bits 15–0). The appropriates enables for the indicated data are assumed, otherwise '–' indicates that port not enabled. Note that the output data summation including A(8)–D(8) is lost, since the output on cycle 13 is swapped to the LSW of S(12) on cycle 8.

Digital Filtering

The input structure of the TMC2249 demonstrates great versatility when all four multiplier inputs and the programmable delay registers are utilized. *Tables 3* and *4* demonstrate how a direct-form symmetric FIR filter of up to 32 taps can be implemented. By utilizing the four input delay registers as pipelined storage banks, the user can store up to 32 coefficient-data word pairs, split into alternate "even" and "odd" halves. Two taps of the filter are calculated on each clock, and the user then increments/decrements the delay words (ADEL–DDEL). The sums of products are successively added to the global sum in the internal accumulator. Once all of the products of the desired taps have been summed, the resultant is available at the output. The user then "pushes" a new time-data sample on to the appropriate even or odd data register "stack" and reiterates the summation. Note that the coefficient bank "pointers", the BDEL and DDEL delay words, are alternately incremented and decremented on successive filter passes to maintain alignment between the incoming data samples and their respective coefficients. The effective filter speed is calculated by dividing the clock rate by one-half the number of taps implemented.

Table 3. Using the TMC2249 to Perform FIR Filtering — Initial Data Loading

Register Position (Hex)	Even Data A	Odd Data C	Coefficient B	Storage D
0	x(31)	x(30)	h(0)	h(1)
1	x(29)	x(28)	h(2)	h(3)
2	x(27)	x(26)	h(4)	h(5)
3	x(25)	x(24)	h(6)	h(7)
4	x(23)	x(22)	h(8)	h(9)
5	x(21)	x(20)	h(10)	h(11)
6	x(19)	x(18)	h(12)	h(13)
7	x(17)	x(16)	h(14)	h(15)
8	x(15)	x(14)	h(15)	h(14)
9	x(13)	x(12)	h(13)	h(12)
A	x(11)	x(10)	h(11)	h(10)
B	x(9)	x(8)	h(9)	h(8)
C	x(7)	x(6)	h(7)	h(6)
D	x(5)	x(4)	h(5)	h(4)
E	x(3)	x(2)	h(3)	h(2)
F	x(1)	x(0)	h(1)	h(0)

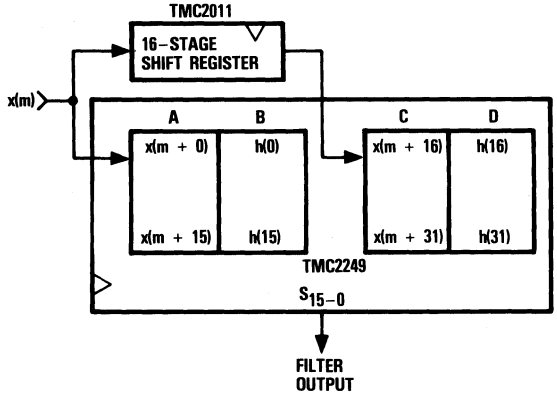
Table 4. FIR Filtering — Operation Sequence

Cycle	Push A	B	Push C	D	ADEL	CDEL	BDEL	DDEL	ACC	ENA	ENC	ENB	END	Convolution Sum	Resultant Output
1	–	–	–	–	0	0	0	0	H	H	H	H	H	x(31)•h(0)+x(30)•h(1)	
2	–	–	–	–	1	1	1	1	H	H	H	H	H	+x(29)•h(2)+x(28)•h(3)	
3	–	–	–	–	2	2	2	2	H	H	H	H	H	+x(27)•h(4)+x(26)•h(5)	
4	–	–	–	–	3	3	3	3	H	H	H	H	H	+x(25)•h(6)+x(24)•h(7)	
5	–	–	–	–	4	4	4	4	H	H	H	H	H	+x(23)•h(8)+(22)•h(9)	
6	–	–	–	–	5	5	5	5	H	H	H	H	H	+x(21)•h(10)+x(20)•h(11)	
7	–	–	–	–	6	6	6	6	H	H	H	H	H	+x(19)•h(12)+x(18)•(13)	
8	–	–	–	–	7	7	7	7	H	H	H	H	H	+x(17)•h(14)+x(16)•h(15)	
9	–	–	–	–	8	8	8	8	H	H	H	H	H	+x(15)•h(15)+(14)•h(14)	
10	–	–	–	–	9	9	9	9	H	H	H	H	H	+x(13)•h(13)+x(12)•h(12)	
11	–	–	–	–	A	A	A	A	H	H	H	H	H	+x(11)•h(11)+x(10)•h(10)	
12	–	–	–	–	B	B	B	B	H	H	H	H	H	+X(9)•h(9)+x(8)•h(8)	
13	–	–	–	–	C	C	C	C	H	H	H	H	H	+x(7)•h(7)+x(6)•h(6)	
14	–	–	–	–	D	D	D	D	H	H	H	H	H	+x(5)•h(5)+x(4)•h(4)	
15	–	–	–	–	E	E	E	E	H	H	H	H	H	+x(3)•h(3)+x(2)•h(2)	
16	–	–	x(32)	–	F	F	F	F	H	H	L	H	H	+x(1)•h(1)+x(0)•h(0)	
17	–	–	–	–	0	0	F	F	H	H	H	H	H	x(31)•h(1)+x(32)•h(0)	
18	–	–	–	–	1	1	E	E	H	H	H	H	H	+x(29)•h(3)+x(30)•h(2)	
19	–	–	–	–	2	2	D	D	H	H	H	H	H	+x(27)•h(5)+x(28)•h(4)	
20	–	–	–	–	3	3	C	C	H	H	H	H	H	+x(25)•h(7)+x(26)•h(6)	31
21	–	–	–	–	4	4	B	B	H	H	H	H	H	+x(23)•h(9)+x(24)•h(8)	$S=\sum_{k=0} h(k)x(n-k)$
.															
.															
.															

Digital Filtering (cont.)

Alternatively, non-symmetric FIR Filters can be implemented using the TMC2249 in a similar fashion. Here, a shift register is used to delay the incoming data fed to the A input by an amount equal to one-half the length of the filter (the length of the A delay register). As shown in *Figure 5*, the data is then sent to the C input, thus "stacking" the A and C delay registers to create a single N-tap FIR filter. The incremented delay words (ADEL – DDEL) for all four inputs are identical. Again, the filter throughput is equal to the clock speed divided by one-half the number of taps implemented.

Figure 5. Non-Symmetric 32-Tap FIR Filtering Using the TMC2249



Complex Arithmetic Functions

The TMC2249 can also be used to perform complex arithmetic functions. The basic function performed by the device, ignoring the delay controls,

$$SUM = (\pm A \cdot B) + (\pm C \cdot D),$$

can realize in two steps the familiar summation:

$$(P + jR)(S + jT) = \underbrace{(PS - RT)}_{(1)} + j\underbrace{(PT + SR)}_{(2)}$$

by loading the TMC2249 as follows:

Step	TMC2249 Inputs						Resultant Output
	A	B	C	D	NEG1	NEG2	
1	P	S	R	T	L	H	(PS – RT)
2	P	T	R	S	L	L	(PT + SR)

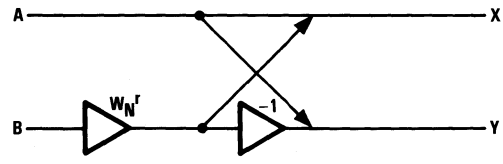
where H and L indicate a logic HIGH and LOW.

Thus we can perform a complex multiplication in two clock cycles. Notice that the user must switch the two components of the second input vector between the B and D inputs to obtain the second complex summation.

Calculating a Butterfly

Taking advantage of the complex multiply which we implemented above using the TMC2249, we can expand slightly to calculate a Radix-2 Butterfly, the core of the Fast Fourier Transform algorithm. To review, the Butterfly is calculated as shown in *Figure 6*.

Figure 6. Signal Flow Diagram of Radix-2 Butterfly



Where $X = A + B(W_N^r)$

$Y = A - B(W_N^r)$,

and W_N^r is the complex phase coefficient, or "twiddle factor" for the N-point transform, which is:

$$\begin{aligned} W_N^r &= e^{-j(2\pi/N)} \\ &= \cos(2\pi/N) + j(\sin(2\pi/N)) \\ &= Re(W) + jIm(W), \end{aligned}$$

with Re and Im indicating the real and imaginary parts of the vector.

Expanding the complex vectors A and B to calculate X and Y, we get:

$$\begin{aligned} X &= (Re(A) + jIm(A)) + (Re(B)Re(W) - Im(B)Im(W) + j(Re(B)Im(W) + Im(B)Re(W)) \\ &= (Re(A) + Re(B)Re(W) - Im(B)Im(W)) + j(Im(A) + Re(B)Im(W) + Im(B)Re(W)) \\ &= Re(X) + jIm(X) \end{aligned}$$

and,

$$\begin{aligned} Y &= (Re(A) + jIm(A)) - (Re(B)Re(W) - Im(B)Im(W) + j(Re(B)Im(W) + Im(B)Re(W)) \\ &= (Re(A) - Re(B)Re(W) + Im(B)Im(W)) + j(Im(A) - Re(B)Im(W) - Im(B)Re(W)) \\ &= Re(Y) + jIm(Y) \end{aligned}$$

Multimedia

Calculating a Butterfly (cont.)

The butterfly is then neatly implemented in four clocks, as follows:

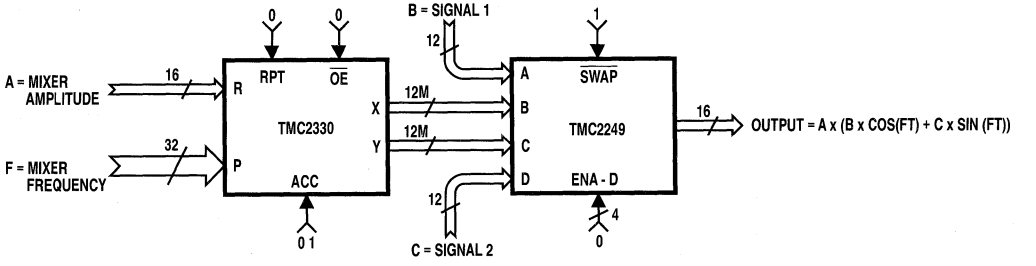
Step	TMC2249 Inputs A	B	C	D	CAS Input	NEG1	NEG2	Resultant Output
1	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	L	H	Re(X)
2	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	H	L	Re(Y)
3	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	L	L	Im(X)
4	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	H	H	Im(Y)

Notice again that the components of the second vector must be switched by the user on the second half of the computation, as well as the parts of the vector presented to the cascade input.

Quadrature Modulation

The TMC2249 can also be used to advantage as a digital-domain complex frequency synthesizer, as demonstrated in *Figure 7*. Here, orthogonal sinusoidal waveforms are generated digitally by sequentially addressing Sine and Cosine ROMS. These quadrature phase coefficients can then be multiplied with two input signals, such as digitized analog data. The TMC2249 then adds these products, which could be output directly to a high-speed digital-to-analog converter such as the TRW TDC1012 for direct waveform synthesis. This 12-bit, 20MHz DAC is ideally suited to waveform generation, featuring extremely low glitch energy for low spurious harmonics.

Figure 7. Direct Quadrature Waveform Synthesizer Using the TMC2249

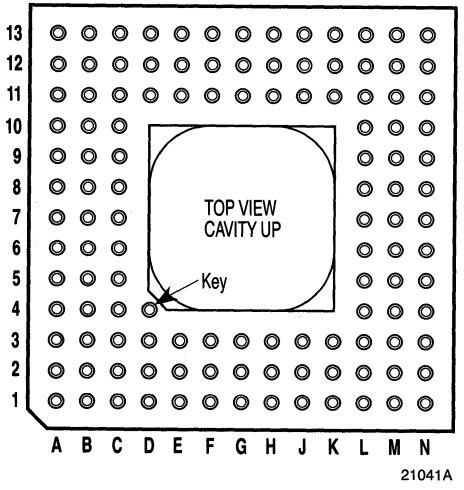


Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package

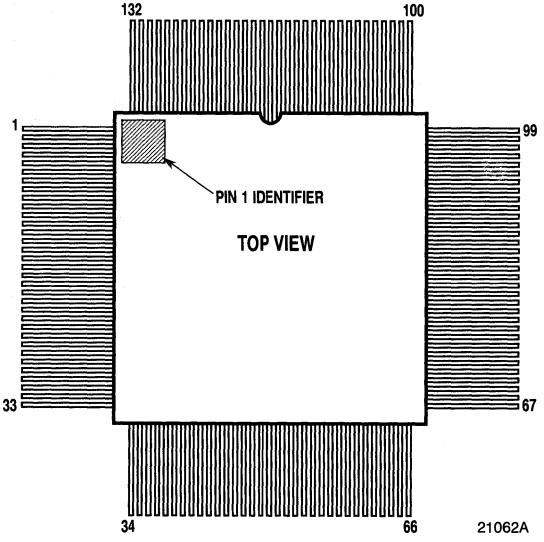
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	CLK	G3	GND	L3	$BDEL_2$	L7	V_{DD}	L11	$ADEL_3$	G11	CAS_6	C11	C_1	C7	GND
B2	ACC	G1	S_7	M2	$BDEL_3$	N7	B_{11}	M12	$ADEL_2$	G13	CAS_5	B12	C_2	A7	D_8
B1	NEG1	H1	S_6	N2	$\overline{ENB}$	N8	A_{11}	M13	$ADEL_1$	F13	CAS_4	A12	C_3	A6	D_7
D3	NEG2	H2	S_5	L4	B_0	M8	A_{10}	K11	$ADEL_0$	F12	CAS_3	C10	C_4	B6	D_6
C2	RND	H3	V_{DD}	M3	B_1	L8	A_9	L12	NC	F11	CAS_2	B11	C_5	C6	D_5
C1	S_{15}	J1	S_4	N3	B_2	N9	A_8	L13	CAS_{15}	E13	CAS_1	A11	C_6	A5	D_4
D2	S_{14}	J2	S_3	M4	B_3	M9	A_7	K12	CAS_{14}	E12	CAS_0	B10	C_7	B5	D_3
E3	GND	K1	S_2	L5	B_4	N10	A_6	J11	CAS_{13}	D13	$\overline{CASEN}$	C9	C_8	A4	D_2
D1	S_{13}	J3	GND	N4	B_5	L9	A_5	K13	CAS_{12}	E11	FT	A10	C_9	C5	D_1
E2	S_{12}	K2	S_1	M5	B_6	M10	A_4	J12	CAS_{11}	D12	$CDEL_0$	B9	C_{10}	B4	D_0
E1	S_{11}	L1	S_0	N5	B_7	N11	A_3	J13	CAS_{10}	C13	$CDEL_1$	A9	C_{11}	A3	$\overline{END}$
F3	V_{DD}	M1	$\overline{OE}$	L6	GND	N12	A_2	H11	GND	B13	$CDEL_2$	C8	V_{DD}	A2	$DDEL_3$
F2	S_{10}	K3	$\overline{SWAP}$	M6	B_8	L10	A_1	H12	CAS_9	D11	$CDEL_3$	B8	D_{11}	C4	$DDEL_2$
F1	S_9	L2	$BDEL_0$	N6	B_9	M11	A_0	H13	CAS_8	C12	$\overline{ENC}$	A8	D_{10}	B3	$DDEL_1$
G2	S_8	N1	$BDEL_1$	M7	B_{10}	N13	$\overline{ENA}$	G12	CAS_7	A13	C_0	B7	D_9	A1	$DDEL_0$

Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	23	S_3	45	B_7	67	NC	89	$\overline{CAS_0}$	111	C_{11}
2	CLK	24	S_2	46	GND	68	$ADEL_3$	90	$\overline{CASEN}$	112	V_{DD}
3	ACC	25	GND	47	B_8	69	$ADEL_2$	91	FT	113	D_{11}
4	NEG1	26	S_1	48	B_9	70	$ADEL_1$	92	$CDEL_0$	114	D_{10}
5	NEG2	27	S_0	49	B_{10}	71	$ADEL_0$	93	$CDEL_1$	115	D_9
6	RND	28	$\overline{OE}$	50	V_{DD}	72	NC	94	$CDEL_2$	116	GND
7	S_{15}	29	$\overline{SWAP}$	51	B_{11}	73	CAS_{15}	95	$\overline{CDEL_3}$	117	D_8
8	S_{14}	30	$BDEL_0$	52	A_{11}	74	CAS_{14}	96	$\overline{ENC}$	118	D_7
9	GND	31	$BDEL_1$	53	A_{10}	75	CAS_{13}	97	C_0	119	D_6
10	S_{13}	32	NC	54	A_9	76	CAS_{12}	98	NC	120	D_5
11	S_{12}	33	NC	55	A_8	77	CAS_{11}	99	NC	121	D_4
12	S_{11}	34	NC	56	A_7	78	CAS_{10}	100	NC	122	D_3
13	V_{DD}	35	$BDEL_2$	57	A_6	79	GND	101	C_1	123	D_2
14	S_{10}	36	$BDEL_3$	58	A_5	80	CAS_9	102	C_2	124	D_1
15	S_9	37	$\overline{ENB}$	59	A_4	81	CAS_8	103	C_3	125	D_0
16	S_8	38	B_0	60	A_3	82	CAS_7	104	C_4	126	$\overline{END}$
17	GND	39	B_1	61	A_2	83	CAS_6	105	C_5	127	$DDEL_3$
18	S_7	40	B_2	62	A_1	84	CAS_5	106	C_6	128	$DDEL_2$
19	S_6	41	B_3	63	A_0	85	CAS_4	107	C_7	129	$DDEL_1$
20	S_5	42	B_4	64	$\overline{ENA}$	86	CAS_3	108	C_8	130	$DDEL_0$
21	V_{DD}	43	B_5	65	NC	87	CAS_2	109	C_9	131	NC
22	S_4	44	B_6	66	NC	88	CAS_1	110	C_{10}	132	NC



120 Pin Plastic Pin Grid Array – H5 Package



132 Leaded CERQUAD – L5 Package

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2249H5C	STD–T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2249H5C
TMC2249H5C1	STD–T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2249H5C1
TMC2249L5V	EXT–T_C= –55°C to 125°C	MIL-STD-883	132 Leaded CERQUAD	2249L5V
TMC2249L5V1	EXT–T_C= –55°C to 125°C	MIL-STD-883	132 Leaded CERQUAD	2249L5V1

40G06125 Rev D 8/93

TMC2255
CMOS 3 x 3, 5 x 5 Image Convolver
8 x 8 Bits, 12 MHz Data Rate

Description

Like the faster TMC2250, the low cost TMC2255 can perform a triple 3x1 matrix-vector multiplication or a 3x3 convolution. It can also perform a 5x5 convolution with bidimensionally symmetrical coefficients. The on-chip coefficient memory stores four sets of nine 8-bit two's complement coefficients. Two of the TMC2255's five 8-bit coefficients, which can be updated during operation. The device accepts the unsigned and/or two's complement data at 1/3 of the applied clock rate.

The 3 (3x1) matrix multiply mode supports various 3-space numerical operations, such as video standards conversion (e.g. YIQ to RGB) or three-dimensional perspective transformation. Three input ports accept the 8-bit two's complement and/or unsigned magnitude data. The two remaining input ports can be loaded with coefficients and/or device control parameters "on-the-fly." In this mode, an output is generated on every clock cycle.

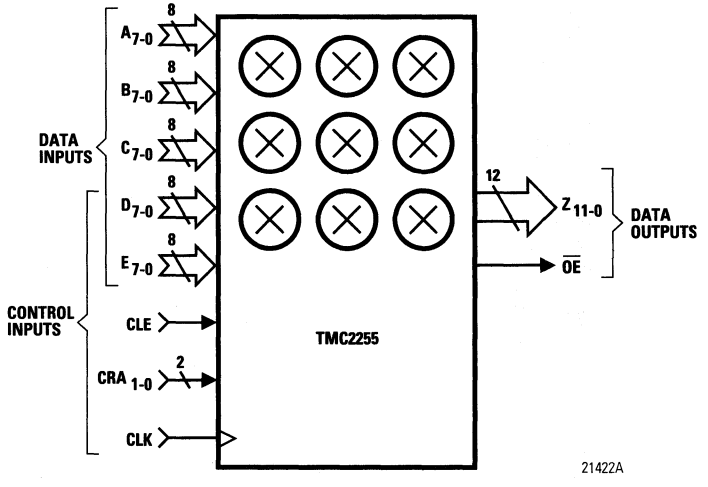
The 3x3 and 5x5 pixel image convolver modes support numerous functions, including static filtering and edge detection. On every third clock cycle, the TMC2255 accepts three (3x3 mode) or five (5x5 mode) data inputs. In the 5x5 mode, the coefficient kernel must be symmetric both horizontally and vertically. Outputs from the device are generated on every third clock cycle, matching the input pixel data rate, and can be limited ("clipped") to 8, 9 or 12 bits.

Fabricated in Raytheon Semiconductor's OMICRON-CTM one-micron CMOS process, the TMC2255 will operate at clock rates of 0 to 30 MHz over the full commercial temperature (0°C to 70°C) and supply voltage ranges.

Features

- 8-bit data and coefficient input precision
- Triple 3x1 matrix-vector multiplication mode
- 3x3 and 5x5 two dimensional convolution modes
- TTL-compatible I/O with three-state output bus
- Offered in 68-contact plastic chip carrier (PLCC)
- Built-in 8-, 9-, or 12-bit arithmetic limiter
- Two's complement, unsigned, or mixed data formats

Logic Symbol



Applications

- RGB To/From YUV/YIQ Color Space Conversion
- 3x3 Or 5x5 Two Dimensional FIR Filtering
- Edge Enhancement And General Image Processing
- Robotics And Image Recognition
- Electronic Darkroom
- Desktop Publishing

Associated Products

- TMC2011 Variable Length Shift Register
- TMC2302 Image Manipulation Sequencer

Functional Description

The TMC2255 contains an array of multipliers and adders, four 9x8-bit coefficient "pages" and a global control block, all of which can be initialized or reconfigured through ports D and E when $\overline{CLE}$ is LOW. Device parameters include matrix coefficients, internal device configuration (mode), rounding precision, and input/output data formats (two's complement, unsigned, or mixed). After the control parameters have been loaded, device operation commences with the next clock rising edge on which $\overline{CLE}$ returns HIGH. Depending on the mode selected, three or five data are input in parallel and proceed through a sequence of operations: Input, Preaddition, Multiply-Accumulation, Rounding, Limiting and Output (*Figures 1-4*).

Input Stage

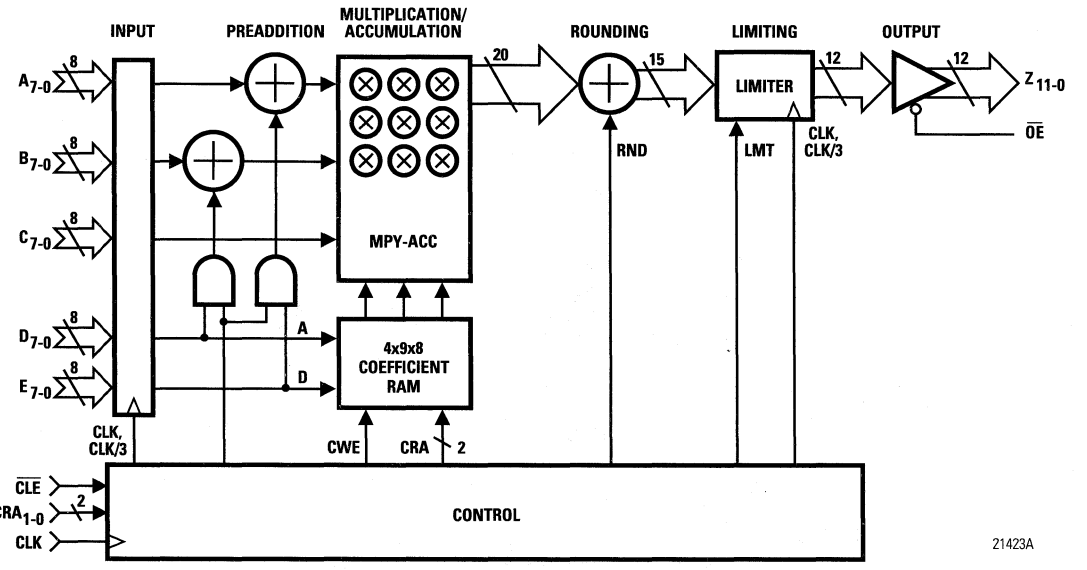
Inputs are supplied to ports A through C in all operating modes on every third clock cycle, beginning with the clock rising edge that contains the most recent $\overline{CLE}$ LOW to HIGH transition. Control and/or coefficient parameters can be input through ports D and E during any of the three master clock cycles that make up each data cycle. In the 5x5 convolution mode data enter the device through ports A-E. Control and/or coefficients may be updated through ports D and E on the remaining two cycles of each clock triplet.

Input data formats may be unsigned and/or two's complement, as identified in the mode select field of port E.

Preaddition

In and only in 5x5 convolution, the horizontal and vertical symmetry of the coefficients permits nine multipliers to do the work of 25. To facilitate this, the data input to ports A and E are pre-added before multiplication, as are the B and D inputs (*Figure 4*, the *5x5 Block Diagram*).

Figure 1. Structural Block Diagram



Coefficient Memory

The TMC2255 contains enough memory to store four "pages" of nine 8-bit two's complement coefficients each. When $\overline{CLE}$ is LOW, a new coefficient is written through port E to the page and location address identified on port D. On every third clock cycle, the coefficient page to be read and used in the immediate 3-cycle computation set is selected by CRA_0 and CRA_1. Of the nine coefficients per page, K1, i (i=1 to 3) process the port A (and E) data; K2, i, the port B (and D) data; and K3, i, the port C data.

Multiplication and Accumulation

The device computes nine products during every three clock cycles, accumulating them internally to full precision.

Rounding

Accumulated sums of products are rounded before the last 5 or 6 bits are truncated. Rounding is performed by adding "010000" or "100000" to the emerging data stream, according to the desired precision of the output results. When $\overline{CLE}$=0 and D=0XXX1111, pin E_6 sets the chip's rounding position, viz: E_6=0: add .010000 and use Z_0 as least significant bit; E_6=1: add .100000 and use Z_1 as least significant bit, ignoring Z_0.

Output Limiting

The device provides programmable output limiting in unsigned (UN) and/or two's complement (TC) format and for 8, 9, or 12 bits of output precision (including Z_0). In 3(3x1) mode, for an RGB to YIQ transformation, the device can limit Z_1 (Y) to 9 bits unsigned while limiting Z_3 (I) and Z_3 (Q) to 9 bits two's complement.

Outputs

Output is through the 12-bit Z port, which provides 1/2 or 1 LSB precision, relative to the input format. In the 3(3x1) mode three outputs will appear consecutively at the Z port during each triple clock cycle; for data input on clock rising edge 0, these results will emerge t_{D0} after clock rising edges 7, 8, and 9. In both convolution modes the results are output at 1/3 the device master clock rate, with the first point of the impulse response emerging after clock rising edge 9. To facilitate connection to a bus, the output buffers are enabled and disabled (placed in high-impedance state) by asynchronous control $\overline{OE}$.

Figure 2. Functional Block Diagram, 3(3x1) Mode

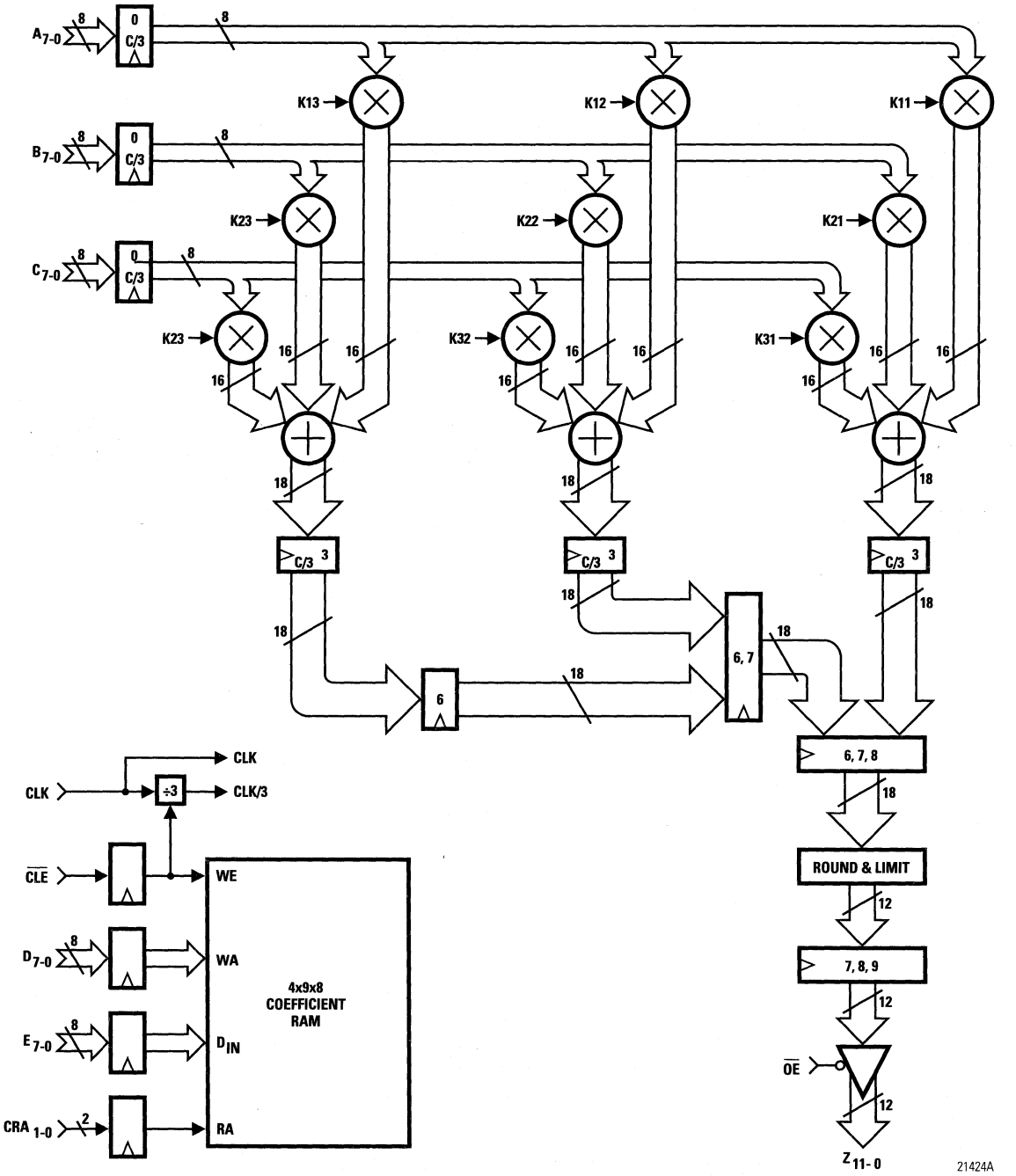


Figure 3. Functional Block Diagram, 3x3 Mode

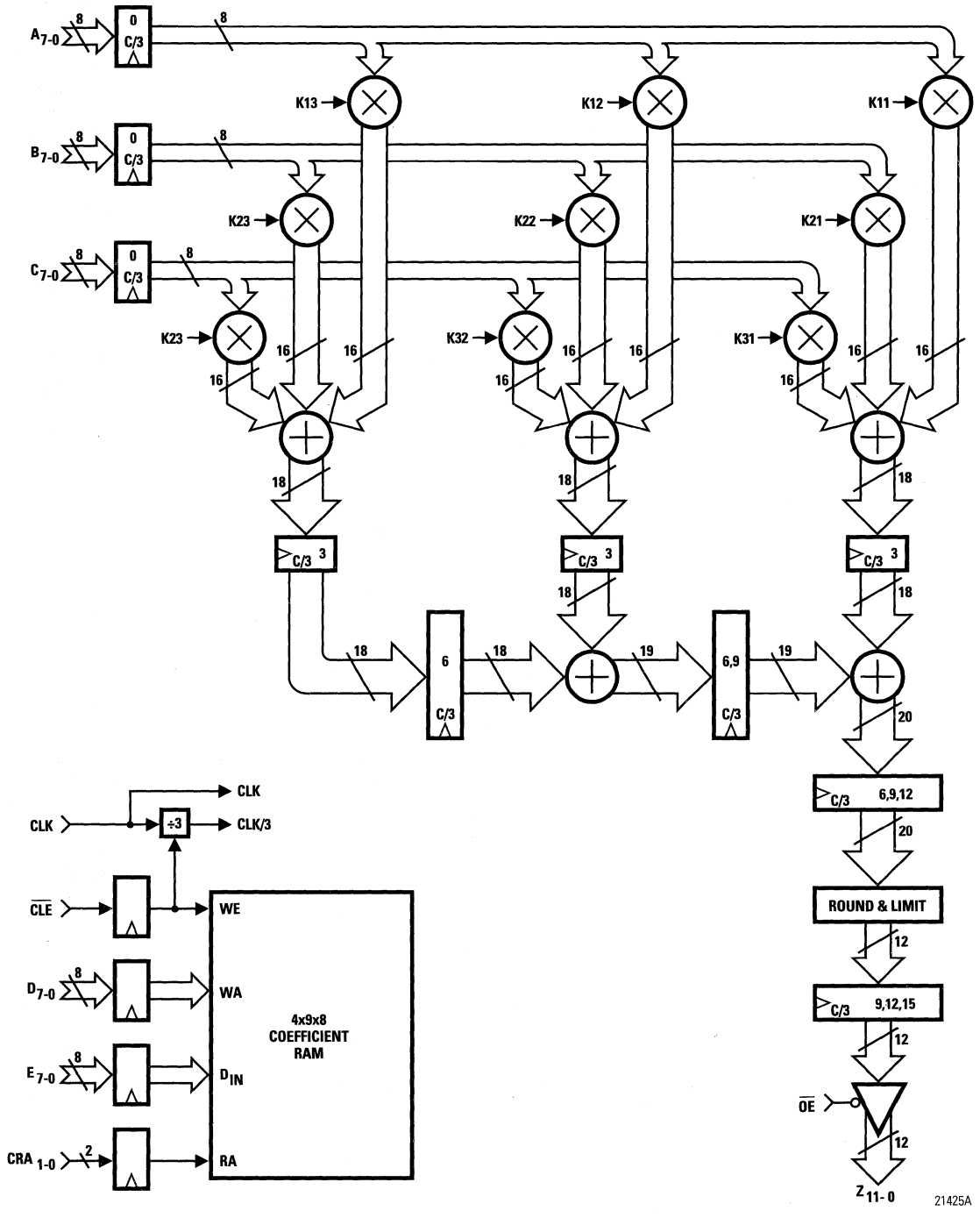
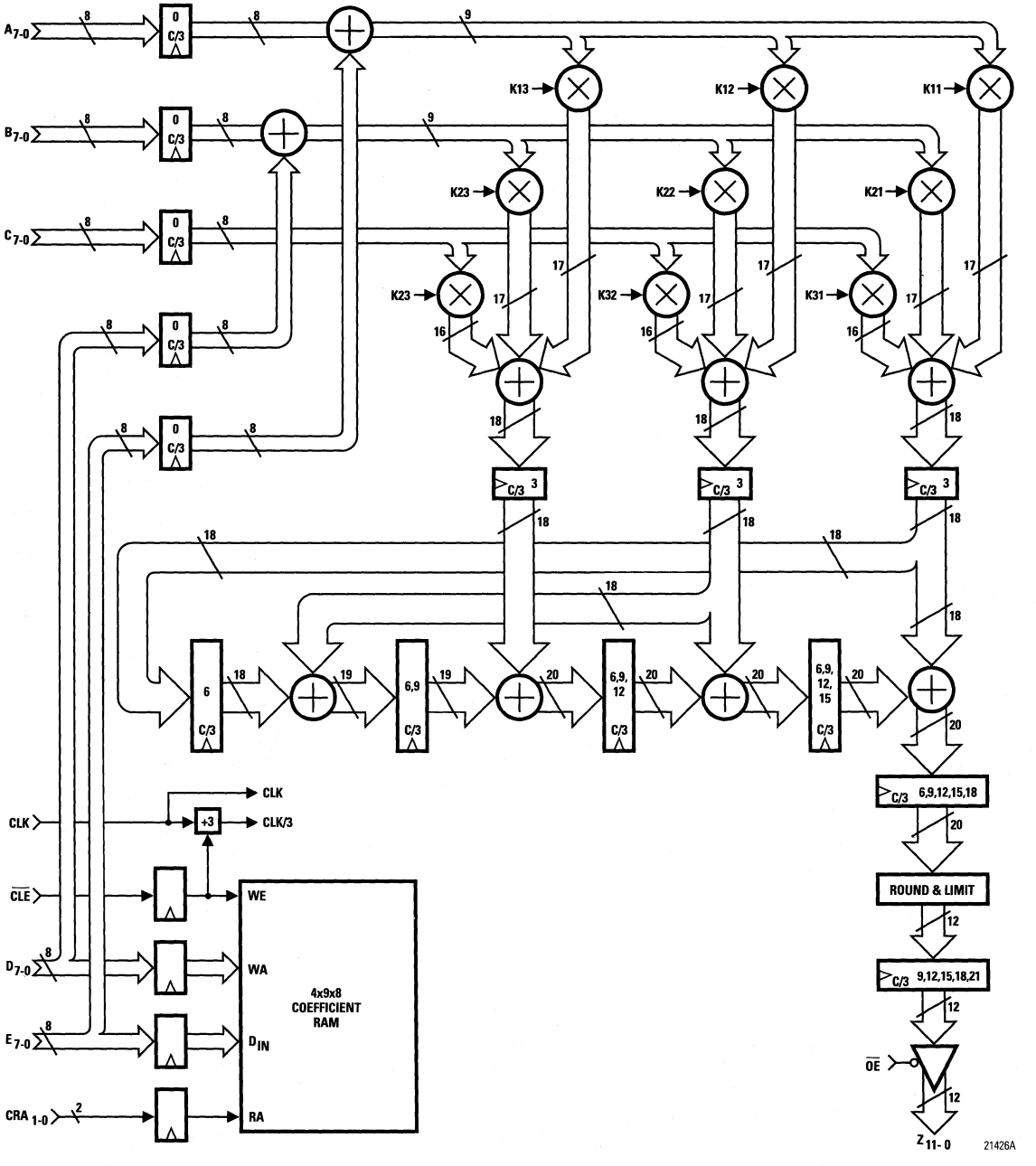


Figure 4. Functional Block Diagram, 5x5 Mode



Signal Definitions

Inputs

CLK — Master chip clock, 0 to 30MHz. All operations are referenced to the rising edges of CLK.

DATA INPUTS — Of the device's five 8-bit data input ports, A, B, and C are used exclusively as data inputs, whereas D and E are also used to program the device (see description of $\overline{CLE}$ pin). For 5x5 convolution, all five ports accept incoming data. In the other modes, only Ports A-C accept incoming data, leaving D and E dedicated to control and coefficient values, which may be updated at any time. In all modes, data are loaded on every third rising edge of CLOCK, beginning on a clock rising edge for which $\overline{CLE}$ makes a 0-to-1 transition. Bits A7, B7, ... are the two's complement sign bits or most significant unsigned bits; bits A_0, B_0, ... are the least significant bits (LSBs).

$\overline{CLE}$ — Active-LOW coefficient and control load enable. When $\overline{CLE}$ is LOW, E becomes the input port for the coefficients, and D becomes the coefficient write address and control port. When $\overline{CLE}$ is HIGH, all coefficients are held unchanged. A LOW to HIGH transition at $\overline{CLE}$ also synchronizes the TMC2255, ushering in a new data input.

CRA_0, CRA_1 — Coefficient read address. The chip can hold four "pages" of nine coefficients each. These two pins determine which of the four coefficient sets is to be used with the data entering during that cycle.

The timing of coefficient selection by CRA is mode dependent. In the 3(3x1) mode, CRA influences all coefficients simultaneously. In the 3x3 and 5x5 convolution modes, however, CRA selects the coefficients for each multiplier column individually, i.e., three per clock cycle from left to right (Block Diagram - 3x3 Mode). CRA should be changed only on "data input" clock cycles to avoid corrupting 3x3 or 3x(3x1) work in progress. CRA should not be updated during a 5x5 operation whose result is needed.

When updating coefficients on-the-fly the user should not set CRA_{1-0} and D5:4 to the same page, but should read from one page while writing to another.

$\overline{OE}$ — Asynchronous, active-LOW output enable. When $\overline{OE}$ is LOW, the output drivers are enabled. When $\overline{OE}$ is HIGH, they are disabled (high-impedance).

Outputs

DATA OUTPUTS — Outputs available on the Z Port are enabled by $\overline{OE}$. Z_{11} is the unsigned MSB or two's complement MSB/sign bit; Z_1 is the integer LSB ("ones' digit"). Z_0 is the 1/2 (fractional) digit. In the 3(3x1) mode (E=XXXXX0XX), a new valid result will emerge t_{DO} after every rising edge of CLOCK. In the other modes (E=XXXXX1XX), a result emerges after every third rising edge of CLOCK. When 9-bit limiting is used, bits Z_{11} through Z_8 will be identical.

Operation and Timing

Before operation, the TMC2255 must be initialized, i.e. loaded with coefficients and set to the desired operating mode, data format, and rounding precision. The chip is programmed via ports D and E, which double as data input ports in 5X5 mode.

Initialization

Chip Select

This control is accessed through bit 7 of port D. When $\overline{CLE}$ is LOW, D_7 must be LOW to allow the coefficient/control information to be updated. If D_7 is HIGH when $\overline{CLE}$ is forced LOW, the device will not allow the coefficient or control information to be updated, and device execution will begin or continue as commanded on the previous LOW to HIGH transition of $\overline{CLE}$. Holding D_7 HIGH (at least when $\overline{CLE}$ is LOW) permits the system to resynchronize the chip without changing any coefficients or configuration parameters.

Coefficient Loading

When $\overline{CLE}$ and D_7 are LOW, the coefficient values presented to port 6 are loaded into the coefficient position and page registers selected by port D, as shown below.

When D_{7-0} =	Update From E_{7-0}: Coef	Page
0XYY0000	1, 1	YY
0XYY0001	1, 2	YY
0XYY0010	1, 3	YY
0XYY0100	2, 1	YY
0XYY0101	2, 2	YY
0XYY0110	2, 3	YY
0XYY1000	3, 1	YY
0XYY1001	3, 2	YY
0XYY1010	3, 3	YY
0XXX0X11	Hold all Coefficients	
0XXXX011	Hold all Coefficients	
0XXX110X	Hold all Coefficients	
0XXX11X0	Hold all Coefficients	
0XXX1111	Control Information	
1XXXXXX	Hold all Coefficients	

X = Don't Care

Each of the four "pages" YY comprises a full set of nine coefficients (one per filter tap).

Mode Selection

When $\overline{CLE}$=0 and D=0XXX1111, pins E_{2-0} select the chip's operating MODE and input data formats, viz:

When E_{7-0} =	Mode =	Data Formats= A B C
0XXXX000	3(3x1)mat mpy	TC TC TC
0XXXX001	3(3x1)mat mpy	UN TC TC
0XXXX010	<Reserved – DO NOT USE>	
0XXXX011	3(3x1)mat mpy	UN UN UN
Z1 = A*K1,1 + B*K2,1 + C*K3,1		first of 3 results
Z2 = A*K1,2 + B*K2,2 + C*K3,2		
Z3 = A*K1,3 + B*K2,3 + C*K3,3		last of 3 results
0XXXX100	3x3 convolution	TC TC TC
0XXXX101	3x3 convolution	UN UN UN
Z = A1*K1,1 + B1*K2,1 + C1*K3,1 + A2*K1,2 + B2*K2,2 + C2*K3,2 + A3*K1,3 + B3*K2,3 + C3*K3,3		
0XXXX110	5x5 convolution	TC TC TC
0XXXX111	5x5 convolution	UN UN UN
Z = A1*K1,3 + B1*K2,3 + C1*K3,3 + D1*K2,3 + E1*K1,3 + A2*K1,2 + B2*K2,2 + C2*K3,2 + D2*K2,2 + E2*K1,2 + A3*K1,1 + B3*K2,1 + C3*K3,1 + D3*K2,1 + E3*K1,1 + A4*K1,2 + B4*K2,2 + C4*K3,2 + D4*K2,2 + E4*K1,2 + A5*K1,3 + B5*K2,3 + C5*K3,3 + D5*K2,3 + E5*K1,3		
1XXXXXXX	[Unchanged from previous setting]	

[Coefficients are always 8-bit two's complement.]

Rounding

All computuations are rounded internally following the final accumulation of products. Rounding position depends on the output format. If the user desires outputs with 1/2 LSB precision (relative to the inputs) then rounding is performed into Z_{-1}, just to the right of the LSB of the output port, Z_0. For 1 LSB precision, rounding is into Z_0, and the output is on pins Z_{11-1} only.

When E_{7-0} =	Outputs are,	Rounded at:
00XXXXXX	Z_{11}-Z_0 (12 bits)	Z_{-1}
01XXXXXX	Z_{11}-Z_1 (11 bits)	Z_{-0}
1XXXXXXX	Unchanged from previous setting	

Output Limiting

When $\overline{CLE}$=0 and D=0XXX1111, pins E_{5-3} tell the chip to which numerical format(s) to limit the emerging results. Unsigned (UN), two's complement (TC), and mixed data formats of 8, 9, or 12 bits (including Z_0) are supported, as follows. Limit "Z" applies to 3x3 and 5x5 convolutional modes; limits Z1, Z2, Z3 apply to 3(3x1) mode.

E_{7-0} =	Limit Z1 or Z	Limit Z2	Limit Z3	Range (RND=0)
0X000XXX	<Limiter Disabled>			
0X001XXX	UN9	UN9	UN9	0,255.5
0X010XXX	TC12	TC12	TC12	–1024,1023.5
0X011XXX	UN12	UN12	UN12	0,2047.5
0X100XXX	TC9	TC9	TC9	–128,127.5
0X101XXX	UN9	TC9	TC9	(mixed)
0X110XXX	<Reserved; Do Not Use>			
0X111XXX	UN8	UN8	UN8	0,127.5
1XXXXXX	Unchanged from previous setting			

Prior to output, the limiter (if enabled) tests the leading bits of the emerging result. In the unsigned limit modes, if the MSB=1, denoting a negative value, the output is forced to 0; if the MSB=0 but any other bit above the 8, 9 or 12 bit output field = 1, the output is forced to 11111111111.1 In the TC9 limit mode, values above 127.5 (00001111111.1) are forced to 00001111111.1 and values below –128 become 11110000000.0. In the TC12 limit mode, values above 1023.5 (01111111111.1) are forced to 01111111111.1, and values below –1024 become 10000000000.0. If full LSB rounding (E_6=1) is used, output bit Z_0 is ignored, each data format is correspondingly 1 bit narrower than shown in the table, and the .5 fractions disappear from the range limits.

Timing

Result Latency

Device operating mode affects when valid results will be available at the output port $Z_{11:0}$. The three results of a 3x1 triple dot product whose inputs enter on clock rising edge 0 will be available t_{D0} after clock rising edges 7, 8, and 9. In a 3 x 3 and 5 x 5 convolution, the first three impulse response points will emerge after clock rising edges 9, 12, and 15. The last two points of a 5-point response (5x5 mode) will follow after rising edges 18 and 21.

Instructions, Inputs, and Synchronization

Each rising edge of CLK which bears a $\overline{CLE}$ LOW to HIGH transistion resynchronizes the device. If $\overline{CLE}$ goes from LOW to HIGH on clock rising edge N, then the chip will resynchronize, starting a new 3-cycle sequence on that edge. It will look for incoming data at clock rising edges N+3i, where i = 1, 2, ... (*Timing Diagrams, Figures 5* through *11*). If $\overline{CLE}$ is brought LOW while an operation is already in progress (e.g., to update coefficients), it should be brought HIGH only on a regular data input clock cycle (N+3i), to avoid corrupting pending results.

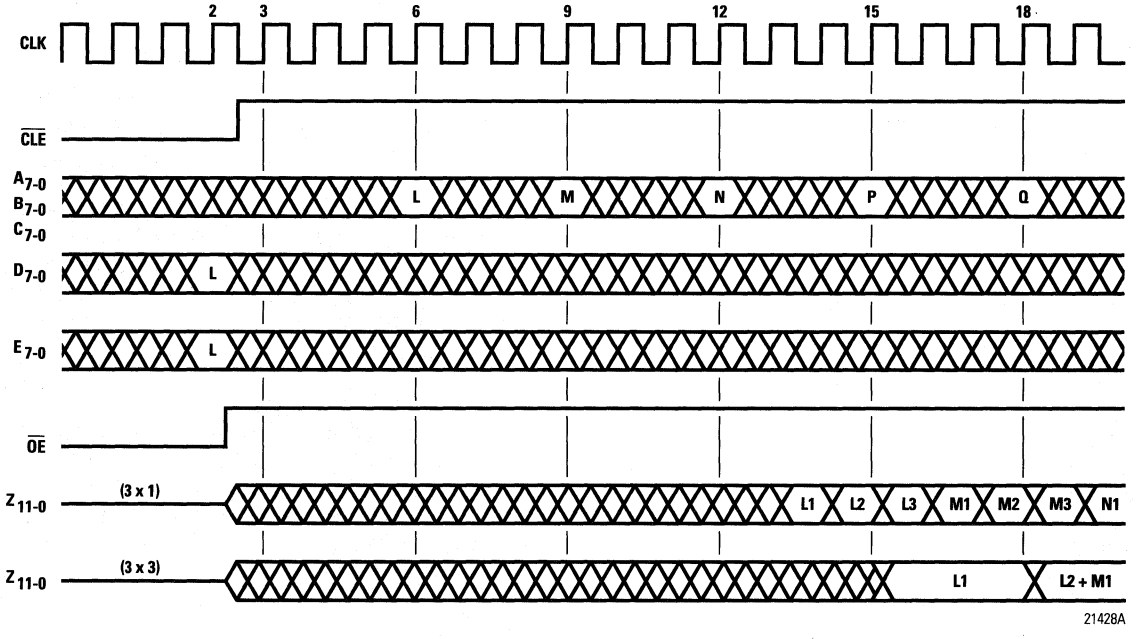
If $\overline{CLE}$ is LOW, control and/or coefficient information entering on a rising edge of CLK will affect all subsequent data inputs until the control parameters are again updated. Internal pipelining of the controls ensures that "in progress" operations on data previously input to the device will continue unaffected, as long as $\overline{CLE}$ is brought HIGH only on data input clock edges.

System Timing

Because the TMC2255's data throughput rate is 1/3 of its incoming clock rate, the user must synchronize the data inputs with the chip's control inputs and internal operation. *Figures 5* through *8* illustrate four ways to use rising edges of $\overline{CLE}$ to align data inputs in the 3(3x1) and 3x3 modes, whereas *Figures 9* through *11* show how to use $\overline{CLE}$ in the 5x5 mode.

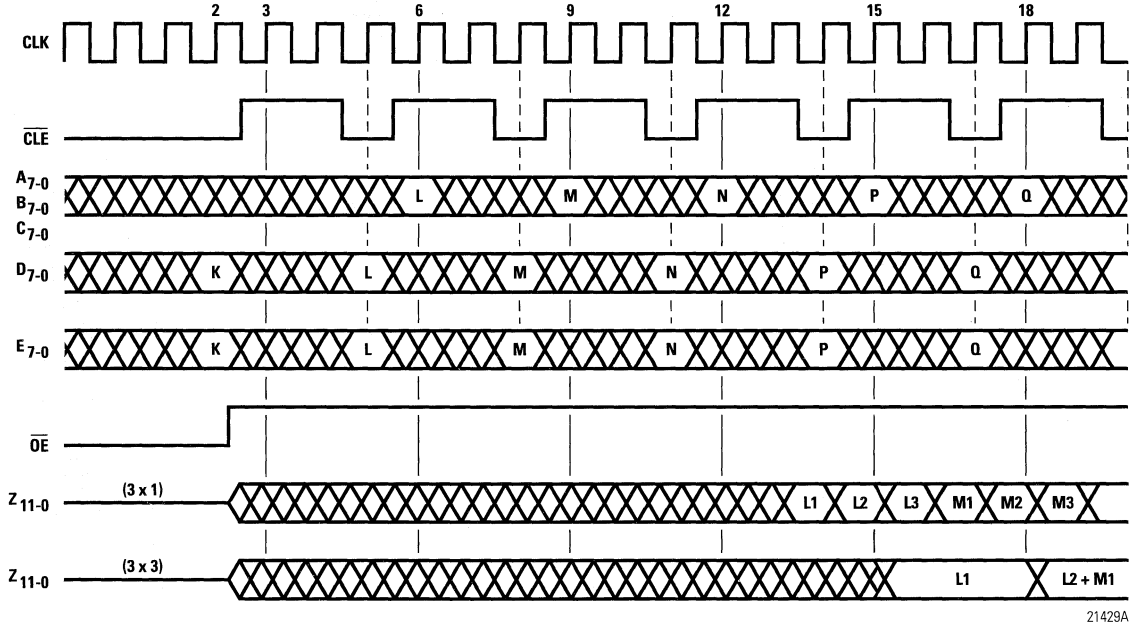
In *Figure 5*, the $\overline{CLE}$ 0 to 1 transition on CLK rising edge 3("t = 3") initializes the chip. The final configuration and coefficient values are loaded through ports D and E at t = 2 and the first incoming data enter ports A, B, and C on rising edge 6. In 3(3x1) mode, the three results from the t = 6 input data emerge after t = 13, 14, and 15. In 3x3 mode, the first result from the edge 6 input data appears after edge 15 and remains until t = 18, when the second result using t = 6 inputs (which is the first result using t = 9 inputs) emerges. After t = 18, the convolution of the t = 6, t = 9, and t = 12 inputs, the last output involving the t = 6 input, appears. The part operates continuousy, with inputs read on every third rising clock edge and a new output available t_{DO} after each rising clock edge (3(3x1) mode) or every third rising edge (3x3 mode).

Figure 5. 3(3x1), 3x3 Timing Diagram, Single $\overline{CLE}$ Rising Edge



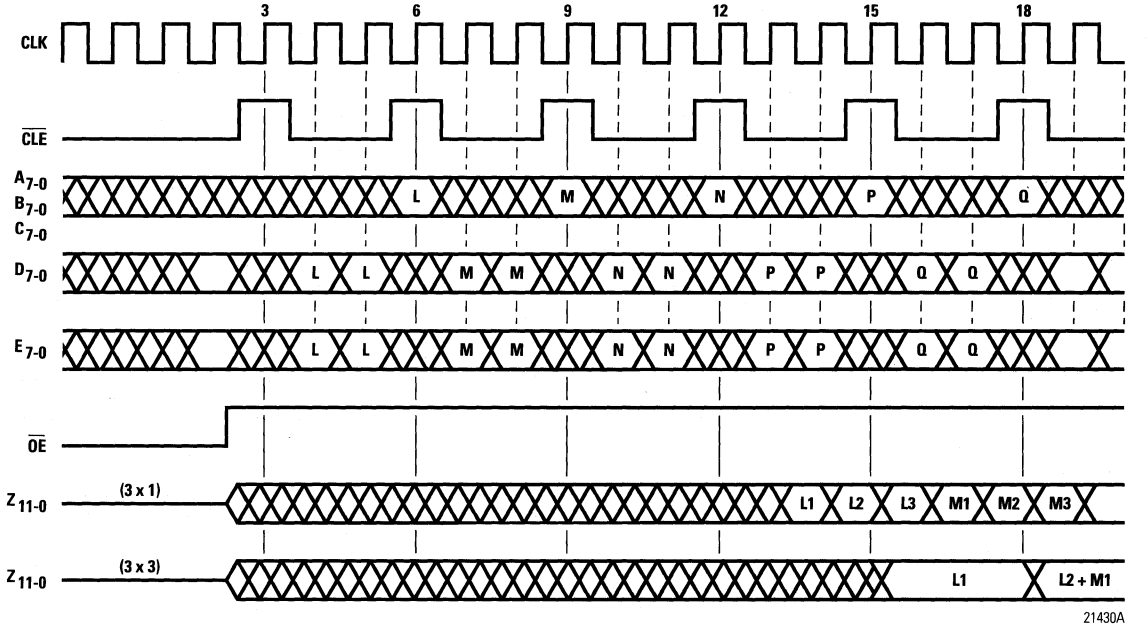
In *Figure 6*, CLK rising edges at t = 3, 6, 9, ... resynchronize the chip, with configuration or coefficient updates at t = 2, 5, 8, ... Data input/output timing is unchanged from *Figure 4*.

Figure 6. 3xX Modes, Periodic Long $\overline{CLE}$ Pulses



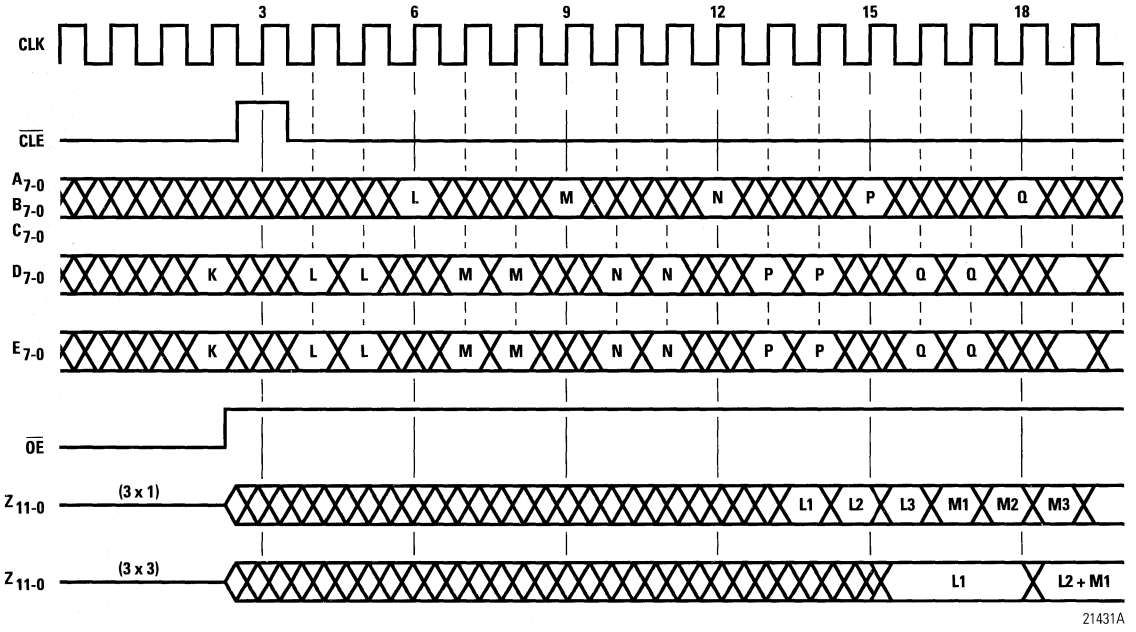
In *Figure 7*, CLK rising edges at t = 3, 6, 9, ... again resynchronize the chip, but configuration and coefficients may be changed twice as often, at t = 1, 2, 4, 5, 7, 8, ...

Figure 7. 3xX Modes, Periodic Short $\overline{CLE}$ Pulses



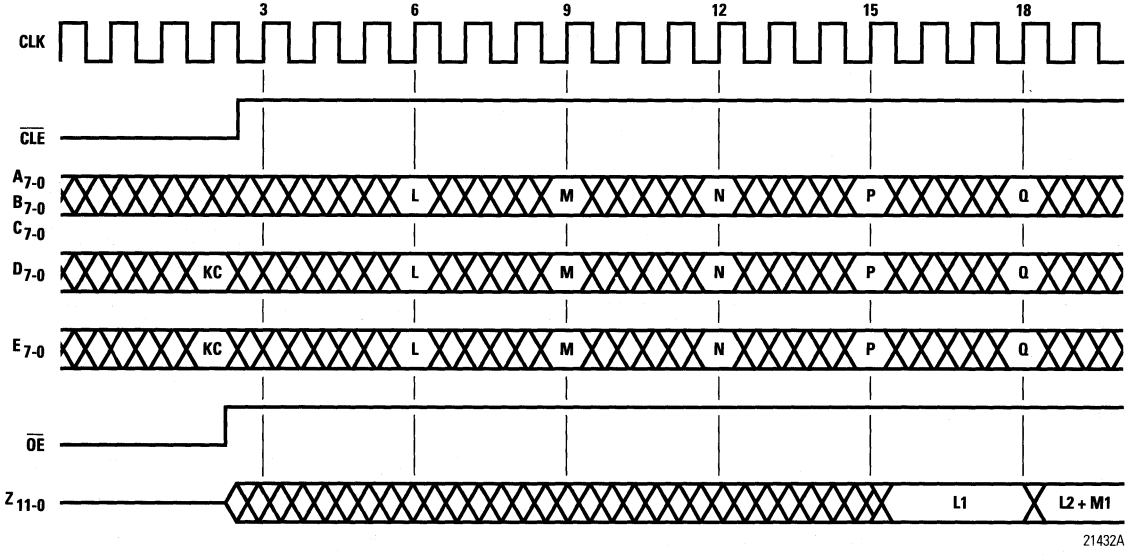
In *Figure 8*, data timing is the same as that of *Figure 5*. However, since $\overline{CLE}$ is left LOW after the one-cycle initialization pulse, instructions and coefficients may be updated on every clock cycle, or three times per data input. Instructions entering between data values, e.g. at t = 4 or t = 5, affect the next data value (i.e., that entering at t = 6). Instructions entering with a given data value (e.g., t = 6) affect the next data input (i.e., at t = 9).

Figure 8. 3xX Modes, Single $\overline{CLE}$ Rising Edge



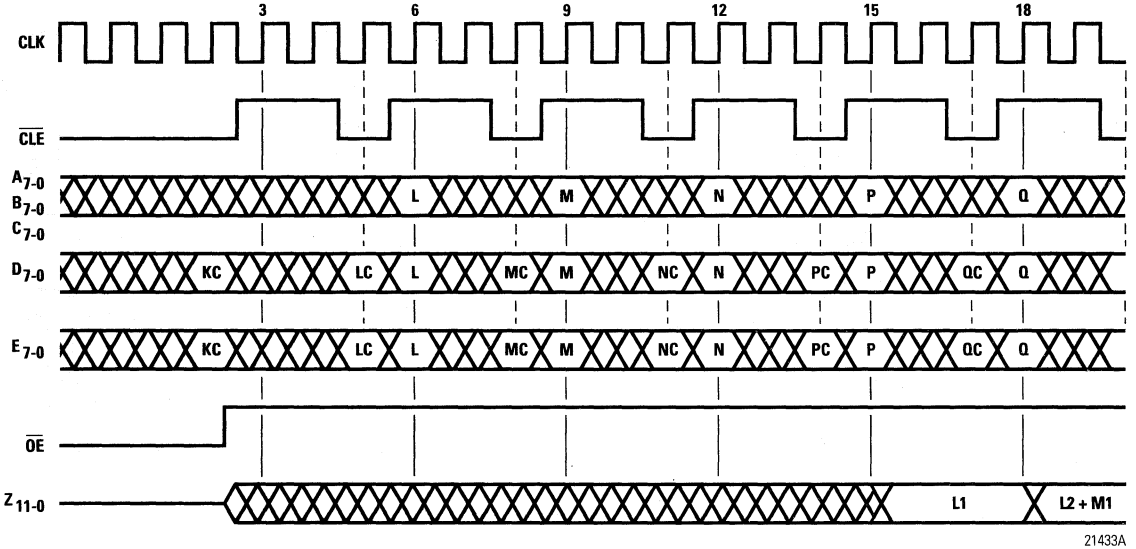
In *Figure 9*, the CLK rising edge at t = 3 synchronizes the operation. The final configuration and coefficient values are loaded through ports D and E at t = 2 and the first incoming data enter ports A through E at t = 6. The first result using the t = 6 input appears after t = 15 and remains until t = 18. The last result using the t = 6 input emerges after t = 27 and remains until t = 30. The part operates continuously, with data inputs read on every third rising edge of CLK and a new output available t_{DO} after every third rising edge of CLK.

Figure 9. 5x5 Convolution, Single $\overline{CLE}$ Rising Edge



In *Figure 10*, one new coefficient or configuration value can be input for every data input, at t = 5, 8, 11, ...

Figure 10. 5x5 Convolution, Periodic Long $\overline{CLE}$ Pulse



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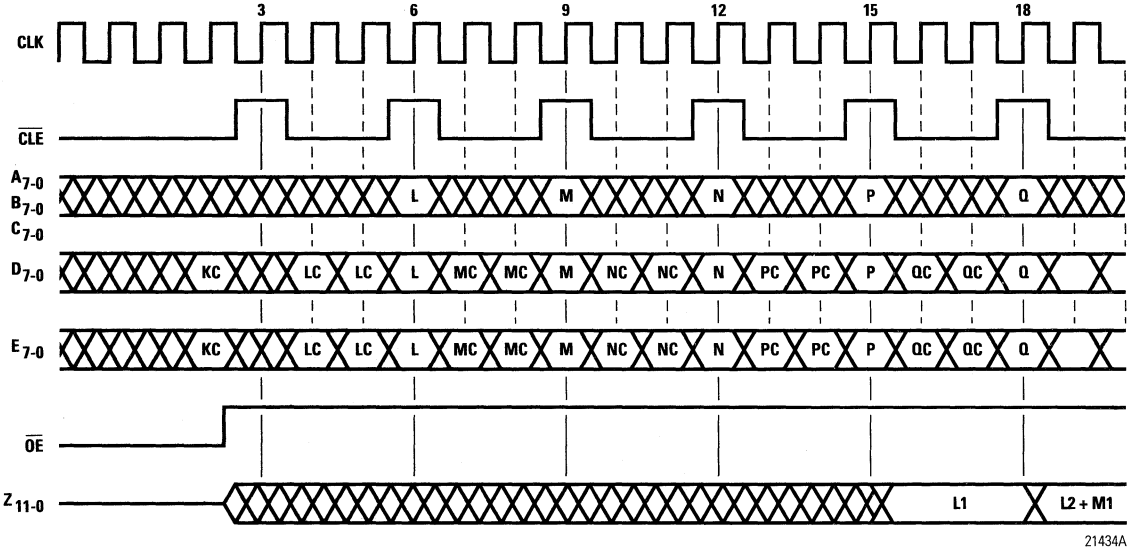
In *Figure 11*, two new coefficients or configuration values can be loaded for every incoming data point, at t = 4, 5, 7, 8, 10, 11, ...

Figure 11. 5x5 Convolution, Periodic Short $\overline{CLE}$ Pulse



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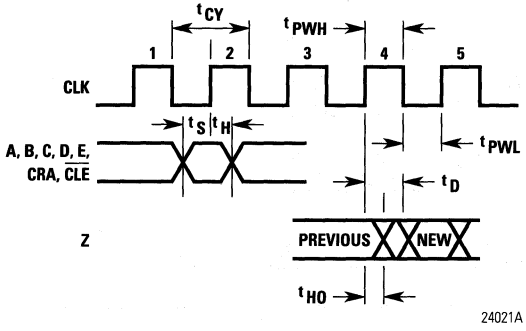
In 5x5 mode, $\overline{CLE}$ should not be left LOW continuously, since ports D and E must serve as data inputs on every third clock cycle. If $\overline{CLE}$ is LOW on a data input cycle, the chip will interpret the current D and E inputs as both data and instructrions/coefficients.

Figure 12. I/O Timing Diagram



Power-Up Sequence

To ensure proper operation, the TMC2255 should receive at least two clock rising edges soon after power-up, with $\overline{CLE}$ making a 0-to-1 transition on edge 4, 5, or 6. Otherwise, some of the internal multiplexers will power up in disallowed states and draw excessive power.

Data Formats

Figure 13 summarizes the TMC2255's data and coefficient formats for all operating modes. Although integer weighting of input data is shown, the binary point may be moved anywhere to the left, as long as the binary point of the output is moved the same distance. Likewise, the coefficient binary point can be moved, as long as the output binary point is moved equally or the data input binary point is moved in the opposite direction. In all coefficients and in all two's complement data, the most significant bit carries a negative weighting.

Figure 13. Data Formats and Bit Alignment

	2^{10}	...	2^{7}	...	2^{2}	2^{1}	2^{0} .	2^{-1}	2^{-2}	...	2^{-6}
Data at Input Ports:			A_7	...	A_2	A_1	A_0 .				
Coefficients:						K_7	K_6 .	K_5	K_4	...	K_0
Internally Accumulated Products:	P_{16}	...	P_{13}	...	P_8	P_7	P_6 .	P_5	P_4	...	P_0
Data at Output Port (Round = 0):	Z_{11}	...	Z_8	...	Z_3	Z_2	Z_1 .	Z_0			
Data at Output Port (Round = 1):	Z_{11}	...	Z_8	...	Z_3	Z_2	Z_1 .	(Ignore Z_0)			

Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	–0.5 to +7.0V
Input Voltage	–0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage	–0.5 to (V_{DD} + 0.5)V[2]
Forced current	–6.0 to 6.0mA[3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating case	–60 to +130°C
junction	175°C
Lead soldering (10 seconds)	300°C
Storage	–65 to 150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
V_{IL}	Input Voltage LOW			0.8	V
V_{IH}	Input Voltage HIGH	2.0			V
I_{OL}	Output Current LOW			4.0	mA
I_{OH}	Output Current HIGH			–2.0	mA
t_{CY}	Cycle Time				
	TMC2255	33			ns
	TMC2255-1	27			ns
t_{PWL}	Clock Pulse Width LOW				
	TMC2255	16			ns
	TMC2255-1	14			ns
t_{PWH}	Clock Pulse With HIGH				
	TMC2255	13			ns
	TMC2255-1	10			ns
t_S	Input Setup Time				
	TMC2255	8			ns
	TMC2255-1	6			ns
t_H	Input Hold Time	0			ns
t_A	Ambient Temperature	0	25	70	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
I_{DDQ}	Supply Current, Quiesc	V_{DD}=Max, V_{IN}=0	15	mA	
I_{DDU}	Supply Current, No Load	V_{DD}=Max, t_{CY}=50ns	100	mA	
I_{IL}	Input Current, LOW		–10	µA	
I_{IH}	Input Current, HIGH		10	µA	
V_{OL}	Output Voltage, LOW		0.4	V	
V_{OH}	Output Voltage, HIGH		2.0		V
I_{OS}	Short-Circuit Out Current		–100	uA	
C_I	Input Capacitance		10	pF	
C_O	Output Capacitance		10	pF	

Note: Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
t_D	Output Delay	V_{DD}=Min, C_L=25pF			
	TMC2255			22	ns
	TMC2255-1			19	ns
t_{HO}	Output Hold	V_{DD}=Max, C_L=25pF		6	ns
t_{ENA}	Output Enable	V_{DD}=Min, C_L=25pF			
	TMC2255			18	ns
	TMC2255-1			15	ns
t_{DIS}	Output Disable	V_{DD}=min, C_L=25pF			
	TMC2255			21	ns
	TMC2255-1			20	ns

Figure 14. Equivalent Input Circuit

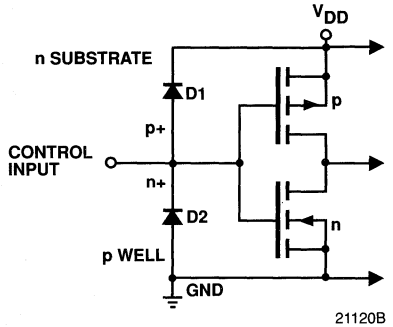


Figure 15. Equivalent Output Circuit

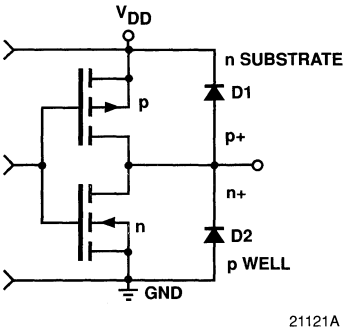
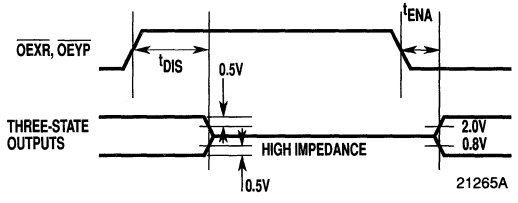


Figure 16. Transition Levels for Three-State Measurements

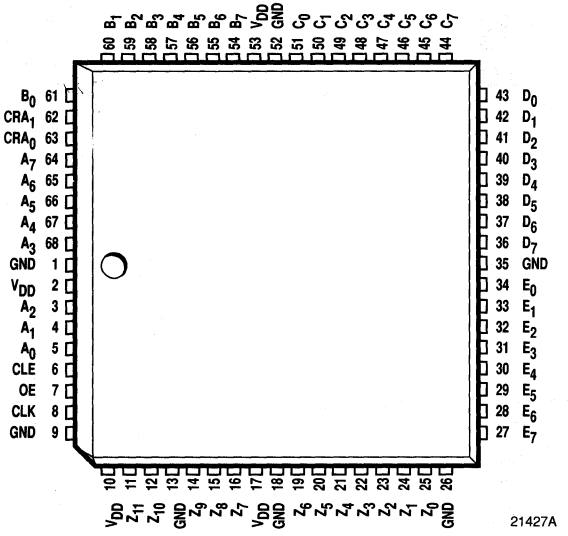


Package Interconnections

Signal Type	Signal Name	Function	R1 Package
Power	V_{DD}	Supply Voltage (+5)	2,10,17,53
	GND	Ground	1,9,18,26,35,52
Clock	CLK	System Clock	8
Control	$\overline{CLE}$	Coefficient Load Enable	6
	$\overline{OE}$	Output Enable	7
	CRA_{1-0}	Coefficient Read Address	62,63
Inputs	A_{7-0}	Data Input Port A	64,65,66,67,68,3,4, 5
	B_{7-0}	Data B	54,55,56,57,58,59,60,61
	C_{7-0}	Data C	44,45,46,47,48,49,50,51
	D_{7-0}	Control/Data D	36,37,38,39,40,41,42,43
	E_{7-0}	Coefficient/Data E	27,28,29,30,31,32,33,34
Outputs	Z_{11-0}	Data Outputs	11,12,14,15,16,19,20,21,22,23,24,25

Pin Assignments – 68-Lead Plastic Chip Carrier – R1 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	18	GND	35	GND	52	GND
2	V_{DD}	19	Z_6	36	D_7	53	V_{DD}
3	A_2	20	Z_5	37	D_6	54	B_7
4	A_1	21	Z_4	38	D_5	55	B_6
5	A_0	22	Z_3	39	D_4	56	B_5
6	$\overline{CLE}$	23	Z_2	40	D_3	57	B_4
7	$\overline{OE}$	24	Z_1	41	D_2	58	B_3
8	CLK	25	Z_0	42	D_1	59	B_2
9	GND	26	GND	43	D_0	60	B_1
10	V_{DD}	27	E_7	44	C_7	61	B_0
11	Z_{11}	28	E_6	45	C_6	62	CRA_1
12	Z_{10}	29	E_5	46	C_5	63	CRA_0
13	GND	30	E_4	47	C_4	64	A_7
14	Z_9	31	E_3	48	C_3	65	A_6
15	Z_8	32	E_2	49	C_2	66	A_5
16	Z_7	33	E_1	50	C_1	67	A_4
17	V_{DD}	34	E_0	51	C_0	68	A_3



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Ordering Information

Product Number	Data Rate MHz	Temperature Range	Screening	Package	Package Marking
TMC2255R1C	10	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2255R1C
TMC2255R1C1	12.5	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2255R1C1

40G06713 Rev B 8/93

TMC2272
Digital Colorspace Converter/Corrector
36-Bit Color (12 Bits x 3 Components) 40 MHz

Description

A 40 MHz, three-channel, 36 bit (three 12-bit components) colorspace converter and color corrector, the TMC2272 uses 9 parallel multipliers to process high-resolution imagery in real time.

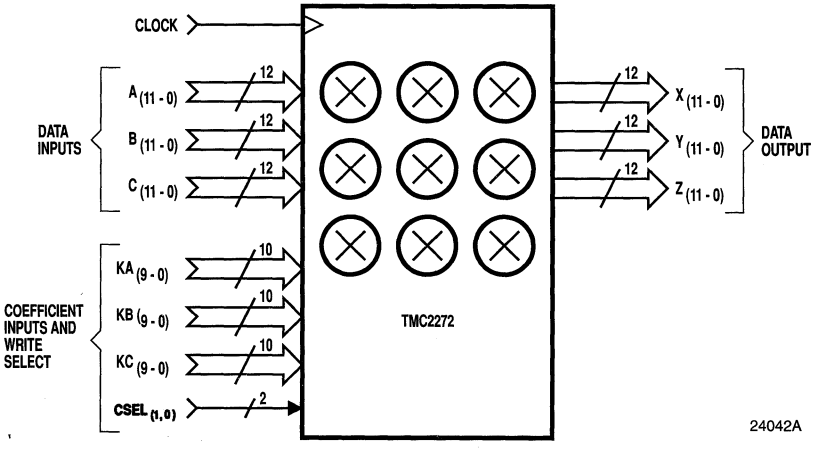
The TMC2272 also operates at any slower clock rate and with any smaller data path width, allowing it to handle all broadcast and consumer camera, frame-grabber, encoder/decoder, recorder and monitor applications as well as most electronic imaging applications.

The TMC2272's processing ability allows colorspaces to be optimized for every input or output device; camera, monitor, transmission or storage medium in real time, regardless of the signal format required by each stage in a system. For instance, a frame buffer may be operated in any desired colorspace in an otherwise RGB system with the use of two TMC2272s for translation to and from the desired frame-buffer colorspace.

A complete set of three 12-bit samples is processed on every clock cycle, with a five-cycle pipeline latency. Full 23-bit (for each of three components) internal precision is provided with 10-bit user-defined coefficients. The coefficients may be varied dynamically, with three new coefficients loaded every clock cycle. (The full set of nine can be replaced in three clock cycles.) Rounding to 12 bits per component is performed only at the final output. This allows full accuracy with correct rounding and overflow headroom for applications that require less than 12 bits per component. All inputs and outputs are registered on the rising edges of the clock.

The TMC2272 is fabricated in a one-micron CMOS process and has fully guaranteed performance over the full commercial temperature range of 0 to 70°C, and all other operational conditions specified in the ***Operating Conditions*** table. The TMC2272 is available in a 121-pin plastic pin-grid array (PPGA) package in three speed grades.

Logic Symbol



TMC2272

Features

- 40 MHz (25 ns) pipelined throughput
- 3 Simultaneous 12-bit input and output channels (64 Giga [2^{36}] colors)
- Two's complement inputs and outputs
- Overflow headroom available in lower resolution
- 10-bit user-defined coefficients
- TTL-compatible input and output signals
- Full precision internal calculation
- Output rounding
- On-board coefficient memory
- OMICRON-C™ 1μ CMOS process

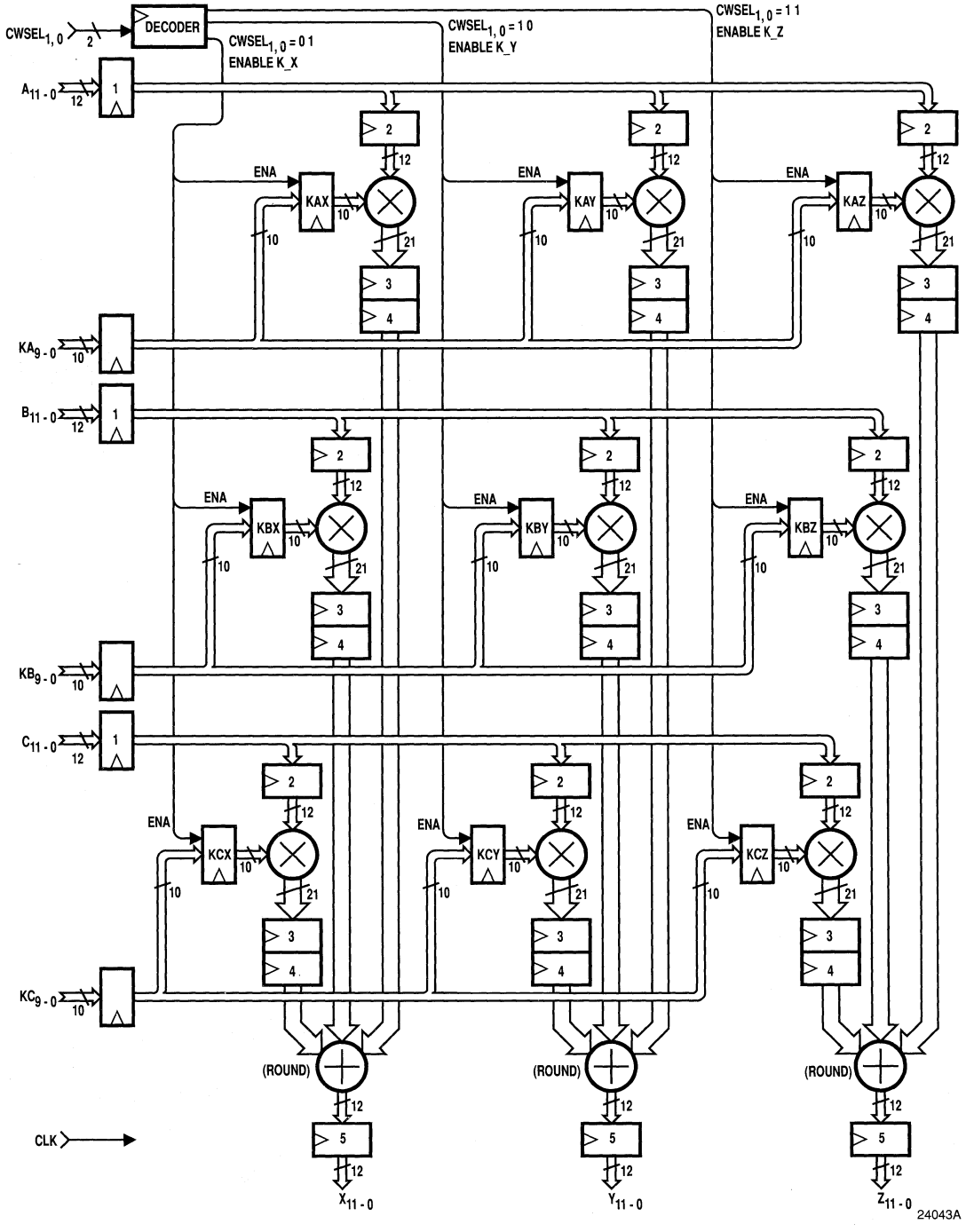
Applications

- Translation between component color standards (RGB, YIQ, YUV, etc.)
- Broadcast composite color encoding and decoding (all standards)
- Broadcast composite color standards conversion and transcoding
- Camera tube and monitor phosphor colorimetry correction
- White balancing and color-temperature conversion
- Image capture, processing and storage
- Color matching between systems, cameras and monitors
- Three-dimensional perspective translation

Associated Products

- TDC1058 A/D Converter
- TDC1049 A/D Converter
- TMC2242 Interpolator/Decimator
- TMC2230 Rectangular/Polar Converter
- TMC22X9X Digital Video Encoder
- TMC22071 Genlocking Video Digitizer

Figure 1. Functional Block Diagram



Multimedia

Functional Description

General Information

The TMC2272 is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product). With a 40MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A_{11-0}, B_{11-0}, C_{11-0}) accept 12-bit two's complement integer data, which is also the format for the output ports (X_{11-0}, Y_{11-0}, and Z_{11-0}). Other format and path width options are discussed in the numeric format and overflow section. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. ***Table 2*** details the bit weighting.

Full precision is maintained throughout the TMC2272. Each output is accurately rounded to 12 bits from the 23 bits entering the final adder.

Signal Definitions

A(n), B(n), C(n) — Indicates the data word presented to that input port during the specified clock rising edge (n). Applies to input ports A_{11-0}, B_{11-0}, and C_{11-0}.

KAX(n) thru KCZ(n) — Indicates coefficient value stored in the specified one of the nine onboard coefficient registers KAX through KCZ, input during or before the specified clock rising edge (n).

X(n), Y(n), Z(n) — Indicates data available at that output port t_{DO} after the specified clock rising edge (n). Applies to output ports X_{11-0}, Y_{11-0}, and Z_{11-0}.

The TMC2272 utilizes six input and output ports to realize a "triple dot product," in which each output is the sum of all three input words in multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words rounded to 12-bits are then available every clock cycle. See the *Applications Discussion* regarding encoded video standard conversion matrices.

X(5) = A(1)KAX(1) + B(1)KBX(1) + C(1)KCX(1)
Y(5) = A(1)KAY(1) + B(1)KBY(1) + C(1)KCY(1)
Z(5) = A(1)KAZ(1) + B(1)KBZ(1) + C(1)KCZ(1)

Pin Definitions

Power

V_{DD}, GND — The TMC2272 operates from a single +5V supply. All pins must be connected.

Control

$CWSEL_{1-0}$ — This input selects which three of the 9 coefficient registers, if any, will be updated on the next clock cycle from the KA_{9-0}, KB_{9-0} and KC_{9-0} inputs. See ***Table 4*** and the ***Functional Block Diagram***.

Clock

CLK — The TMC2272 operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.

Data and Coefficient Inputs

A_{11-0}, B_{11-0}, C_{11-0} — These are the three 12-bit wide data input ports.

KA_{9-0}, KB_{9-0}, KC_{9-0} — These are the 10-bit wide coefficient input ports. The value at each of these three inputs will update one coefficient register as selected by the coefficient write select ($CWSEL_{1-0}$) on the next clock. See ***Table 1*** and the ***Functional Block Diagram***.

Outputs

X_{11-0}, Y_{11-0}, Z_{11-0} — These are the data outputs. Data are available at the 12-bit registered Output Ports X, Y, and Z t_{DO} after every clock rising edge.

Table 1. Coefficient Loading

		$CWSEL_{1,0}$			
		00	01	10	11
Input	KA_{9-0}	Hold All	Load KAX	Load KAY	Load KAZ
Input	KB_{9-0}	Hold All	Load KBX	Load KBY	Load KBZ
Input	KC_{9-0}	Hold All	Load KCX	Load KCY	Load KCZ

Package Interconnections

Signal Type	Signal Name	Function	H5 Package
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8, C4
	GND	Ground	E3, G3, J3, L4, L6, H11, C7, C5, A4, B5
Clock	CLK	System Clock	D11
Controls	$CWSEL_{1,0}$	Coefficient Write Select	J12, J13
Inputs	A_{11-0}	Data Input A	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12
	B_{11-0}	Data Input B	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12
	C_{11-0}	Data Input C	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9
	KA_{9-0}	Coefficient Input KAX, KAY, or KAZ (See Pin Definitions and Table 1)	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13
	KB_{9-0}	Coefficient Input KBX, KBY, or KBZ (See Pin Definitions and Table 1)	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8
	KC_{9-0}	Coefficient Input KCX, KCY, or KCZ (See Pin Definitions and Table 1)	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5
Outputs	X_{11-0}	Output X	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2
	Y_{11-0}	Output Y	D1, E2, E1, F2, F1, G2, G1, H1, K1, J2, J1, H2
	Z_{11-0}	Output Z	M4, N3, M3, N2, M2, L3 N1, L2, K3, M1, L1, K2

Figure 2. Impulse Response

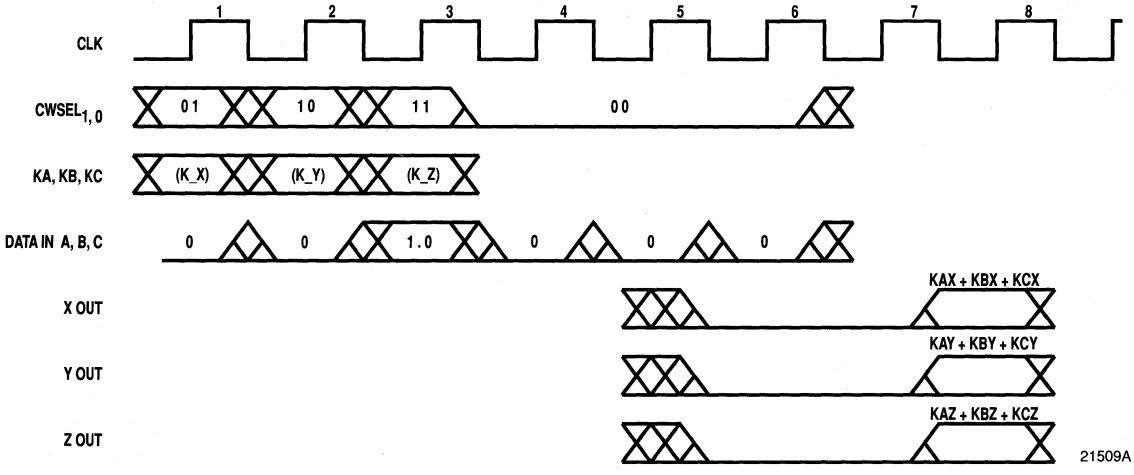
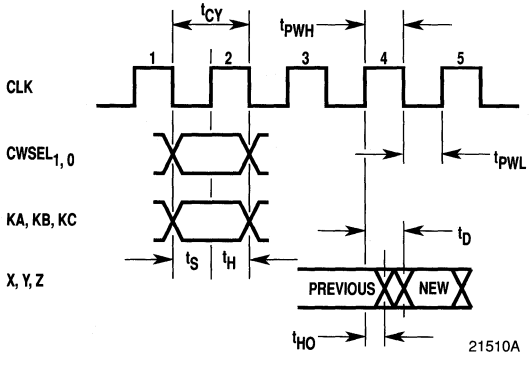


Figure 3. Input/Output Timing Diagram



Numeric Format and Overflow

Table 2 shows the binary weightings of the input and output ports of the TMC2272. Although the internal sums of products could grow to 23-bits, the outputs X, Y, and Z are rounded to yield 12-bit integer words. Thus the output format is identical to the input data format. Bit weighting is easily adjusted by applying the same scaling correction factor to both input and output data words.

As shown in *Table 2*, the TMC2272's matched input and output data formats accommodate 0dB (unity) gain. Therefore the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific translation performed to ensure that no overflow occurs.

Use with Fewer Than 12 Bits

The TMC2272 can be configured to provide several format and overflow options when used in systems with fewer than 12-bits of resolution. An 8-bit system will be used as an example, however these concepts apply to any other word width.

The most apparent mode of operation is to left justify the incoming data and to ground the unused input LSBs. However, the outputs will still be rounded to the least significant bit of the TMC2272, having little if any effect on the top 8 bits actually used. Because the TMC2272 carries out all calculations to full precision, the preferred mode of operation is to right justify and sign extend the data as shown in *Figure 4*. Since all the LSBs are used, the desired output will be rounded correctly, and overflow will be accommodated by bits 7 through 10.

The TMC2272 may also be used in unsigned binary 8-bit systems as shown in *Figure 5*. Bits 11 through 8 will handle overflow.

In all applications, a digital zero (ground) should be connected to all unused inputs.

Table 2. Bit Weightings for Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
INPUTS																						
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	.									
Coefficients KA, KB, KC												$-K_9$	.	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Internal Sum	$-X_{20}$	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	.	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
OUTPUTS																						
X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	.									

Note: A minus sign indicates a two's complement sign bit.

Figure 4. Two's Complement 8-Bit Application

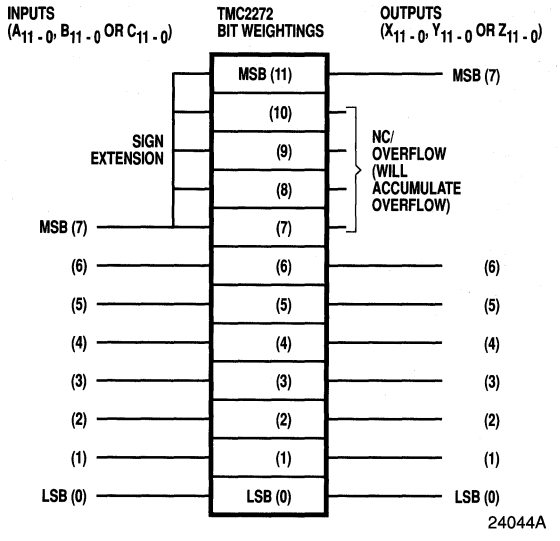
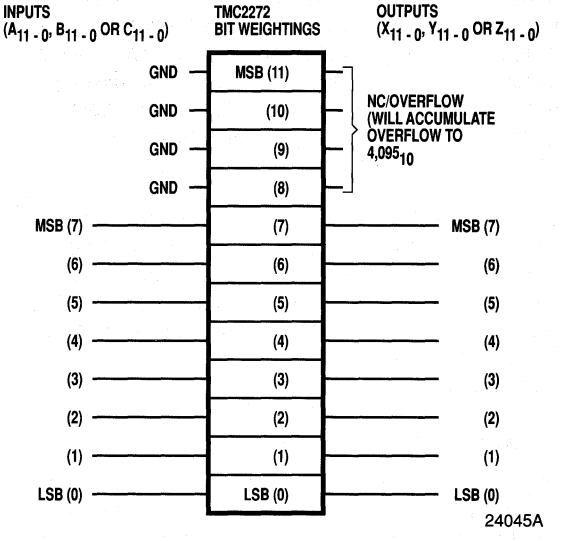


Figure 5. Binary 8-Bit Application



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage	−0.5 to (V_{DD} + 0.5)V[2]
Forced current	−6.0 to 6.0mA[3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating case	−60 to +130°C
junction	175°C
Lead soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Nom	Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
V_{IL}	Input Voltage,Logic LOW			0.8	V
V_{IH}	Input Voltage,Logic HIGH	2.0			V
I_{OL}	Output Current,Logic LOW			4.0	mA
I_{OH}	Output Current,Logic HIGH			–2.0	mA
t_{CY}	Cycle Time				
	TMC2272	33			ns
	TMC2272-1	27.7			ns
	TMC2272-2	25			ns
t_{PWL}	Clock Pulse Width,LOW				
	TMC2272	15			ns
	TMC2272-1	12			ns
	TMC2272-2	10			ns
t_{PWH}	Clock Pulse Width,HIGH	10			ns
t_S	Input Setup Time				
	TMC2272	8			ns
	TMC2272-1	7			ns
	TMC2272-2	6			ns
t_H	Input Hold Time				
	TMC2272	3			ns
	TMC2272-1	3			ns
	TMC2272-2	2			ns
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		12	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=20MHz		160	mA
I_{IL}	Input Current,Logic LOW[2]	V_{DD}=Max, V_{IN}=0V		±10	uA
I_{IH}	Input Current,Logic HIGH[2]	V_{DD}=Max, V_{IN}=V_{DD}		±10	uA
I_{OZL}	Leakage Current, Logic LOW[3]	V_{DD}=Max, V_{IN}=0V		±40	uA
I_{OZH}	Leakage Current, Logic HIGH[3]	V_{DD}=Max, V_{IN}=V_{DD}		±40	uA
V_{OL}	Output Voltage,Logic LOW	V_{DD}=Min, I_{OL}=4mA		0.4	V
V_{OH}	Output Voltage,Logic HIGH	V_{DD}=Min, I_{OH}=-2mA	2.4		V
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, One Pin to Ground, One Second Duration Max.	–20	–80	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10	pF

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Except pins X_{11-0}, Y_{11-0}
3. Pins X_{11-0}, Y_{11-8} only.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_D	Output Delay	V_{DD}=Min, C_{LOAD}=25pF			
	TMC2272			18	ns
	TMC2272-1			17	ns
	TMC2272-2			16	ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=25pF			
	TMC2272		3		ns
	TMC2272-1		3		ns
	TMC2272-2		3		ns

Figure 6. Equivalent Input Circuit

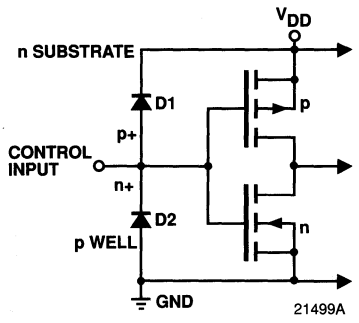
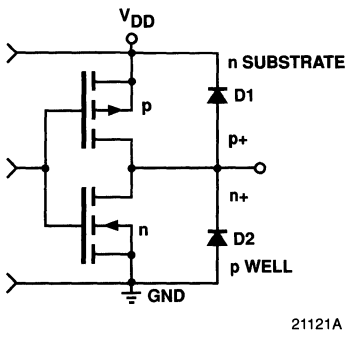


Figure 7. Equivalent Output Circuit



Applications Discussion

The TMC2272 can convert between any two three-coordinate colorspaces with the selection of the proper coefficients. Sets of coefficients for some popular colorspace conversions are presented below.

By concatenating coefficient matrices of single transformations, the user can program the TMC2272 to perform compound transforms efficiently. For example, given an RGB input, correction of the relative values of R and B, for color temperature, conversion to YIQ, modification of contrast by changing Y, and conversion back to RGB can be performed as quickly and easily as any simple transformation. To calculate the final set of coefficients from the coefficients of the individual transformations, the procedure in ***Figure 8*** (concatenation) is used. If more than two matrices are to be combined, the result from the concatenation of the first two matrices is concatenated with the third. If more matrices must be incorporated in the final function, the last step is repeated.

Figure 8. Concatenation

$$\begin{vmatrix} A & B & C \\ D & E & F \\ G & H & I \end{vmatrix} \begin{vmatrix} J & K & L \\ M & N & O \\ P & Q & R \end{vmatrix} = \begin{vmatrix} AJ+BM+CP & AK+BN+CQ & AL+BO+CR \\ DJ+EM+FP & DK+EN+FQ & DL+EO+FR \\ GJ+HM+IP & GK+HN+IQ & GL+HO+IR \end{vmatrix}$$

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Converting From GBR to YC_BC_R

With the right coefficients, two external NOT gates, and an external 4-bit half-addder, the TMC2272 can convert video data from 8-bit full-scale (e.g., VGA) GBR components to 10-bit YC_BC_R components.

Table 1. 10-bit component formats and inclusive ranges.

Color Space Term		Data Range	Format
Y	Luminance	64-940	magnitude
Y'	Y - 64	0-876	magnitud
C_B	Color difference, Blue	64-960	magnitude
U'	C_B - 512	+/-448	2's comp
C_R	Color difference, Red	64-960	magnitude
V'	C_R - 512	+/-448	2s comp
GBR	Green, Blue, Red components	0-255	magnitude, 8-bits

The analog defining equations for 1 Volt luminance and +/-0.5 Volt color difference components are:

$$\begin{aligned} Y &= 0.5870\,(G) + 0.1140\,(B) + 0.2990\,(R) \\ B - Y &= -0.3313\,(G) + 0.5000\,(B) - 0.1687\,(R) \\ R - Y &= -0.4187\,(G) - 0.0813\,(B) + 0.5000\,(R) \end{aligned}$$

To translate these equations into the digital domain, note that the ranges of R, G, and B are 0 to 255 instead of 0 to 1, the range of Y is 64 to 940 instead of 0 to 1, and the ranges of U and V are 64 to 960, instead of +/- 0.5:

$$\begin{aligned} Y &= (876/255)(0.587(G)+0.114(B)+0.299(R))+64 \\ &= 2.01652\,(G) + 0.39162\,(B) + 1.02715\,(R) + 64 \end{aligned}$$

$$\begin{aligned} C_B &= (896/255)(-0.3313(G)+0.5(B)-0.1687(R))+512 \\ &= -1.16397(G) + 1.75686(B) - 0.59289(R) + 512 \end{aligned}$$

$$\begin{aligned} C_R &= (896/255)(-0.4187(G)-0.0813(B)+0.5(R))+512 \\ &= -1.47115(G) - 0.28571(B) + 1.75686(B)) + 512 \end{aligned}$$

Let Y' = Y - 64, U' = C_B - 512, and V' = C_R - 512. The TMC2272 will compute Y', U', and V'. Adding 64 (040_h) externally to Y' will then yield Y, whereas inverting the most significant bits of U' and V', U'9 and V'9, will yield C_B and C_R, respectively. Multiplying the equations immediately above by 128 and rounding each coefficient to the nearest integer yields the recommended set of coefficients for GBR to YUV conversion.

128 (Y') = 258 (G)	+50 (B)	+131 (R) dec.
102	032	083 hex
128 (U') = -149 (G)	+225 (B)	-76 (R) dec.
36B	0E1	3B4 hex
128 (V') = -188 (G)	-37 (B)	+225 (R) dec.
344	3DB	0E1 hex

If the TMC2272 input data alignment for 8-bit GBR is:

0	0	G7	G6	G5	G4	G3	G2	G1	G0	0	0
0	0	B7	B6	B5	B4	B3	B2	B1	B0	0	0
0	0	R7	R6	R5	R4	R3	R2	R1	R0	0	0

then the output data alignment for 10-bit Y'U'V' is:

0	0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
U9	U9	U9	U8	U7	U6	U5	U4	U3	U2	U1	U0
V9	V9	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

where the tripled U9 and V9 sign bits denote two's complement sign extensions. The factors of 4 in the input data format and 128 in the equations are absorbed by the internal 9-bit (factor of 512) right-shifting of the emerging results.

At the output of the TMC2272, invert the most significant bits, U9 and V9, of the chrominance components, and add 1 at Y6 of the luminance to obtain the true CCIR Rec. 601 values.

Converting from GBR to 8-bit Full-Scale YUV

With the right coefficients and two external NOT gates, the TMC2272 can convert video data from 8-bit full-scale (e.g., VGA) GBR components to 8-bit full-scale YUV components.

Table 2. 8-bit component formats and inclusive ranges:

Color Space Term		Range	Format
Y	Luminance	0-255	magnitude
U	Color difference, Blue	128 to -127	2's comp
U'	U + 128	0-255	magnitude
V	Color difference, Red	128 to -127	2s comp
V'	V + 128	0-255	magnitude
G,B,R	Green, Blue, Red components	0-255	magnitude

As in the previous RGB to YC_BC_R case, begin with the defining equations, but without the range compensation factors of 255 / 876 and 255 / 896:

Y = 0.5870 (G) +0.1140 (B) +0.2990 (R)
U = -0.3313 (G) +0.5000 (B) -0.1687 (R)
V = -0.4187 (G) -0.0813 (B) +0.5000 (R)

The TMC2272 will compute Y, U, and V directly, whereas inverting the most significant bits of U and V (U7 and V7 will yield U' and V', respectively. Multiplying the equations immediately above by 512 and rounding each coefficient to the nearest integer yields the recommended set of coefficients for GBR to YUV conversion.

512 (Y) = 301 (G) +58 (B) +153 (R)		dec.
12D 03A 099		hex
512 (U) = -170 (G) +256 (B) -86 (R)		dec.
356 100 3AA		hex
512 (V) = -214 (G) -42 (B) +256 (R)		dec.
32A 3D6 100		hex

If the TMC2272 input data alignment for 8-bit GBR is:

0	0	0	0	G7	G6	G5	G4	G3	G2	G1	G0
0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

then the output data alignment for 8-bit YUV is:

0	0	0	0	y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
U7	U7	U7	U7	U7	U6	U5	U4	U3	U2	U1	U0
V7	V7	V7	V7	V7	V6	V5	V4	V3	V2	V1	V0

where the quintupled U9 and V9 sign bits denote two's complement sign extensions. The factor of 512 in the equations above is absorbed by the internal 9-bit right shift of each emerging result.

At the output of the TMC2272, invert the most significant bits, U7 and V7, of the chrominance components, to obtain the 8-bit offset format.

Converting From YC_BC_R to GBR

Following the notation employed earlier, the TMC2272 will be used to convert data in Y'U'V' format into GBR format.

Since Y' = 876, U' = V' = 0, and G = B = R = 255 for saturated white output, every "Y'" coefficient will be 255 / 876 = 0.29110. The full analog matrix for Y'U'V' to GBR conversion is:

G = 0.29110 (Y') -0.09794 (U') -0.20324 (V')
B = 0.29110 (Y') +0.50431 (U')
R = 0.29110 (Y') +0.39901 (V')

Since the largest element is just over 0.5 and the largest permissible coefficient is 511, multiply all elements of the matrix by 512 to obtain the values to load into the TMC2272:

G = 149 (Y') -50 (U') -04 (V')		dec.
095 3CE 398		hex
B = 149 (Y') +258 (U')		dec.
095 100		hex
R = 149 (Y') +204 (V')		dec.
095 0CC		hex

Decrease the incoming luminance at the input to the TMc2272 by 64 by adding 1's at positions Y9, Y8, Y7, and Y6. Invert U9 and V9 and their sign extensions, to accommodate CCIR Rec. 601 data. Instead of reducing Y by 64, an alternate is to reduce each of the G. B. and R outputs by (255) (64 / 876) = 19.

For the Y'U'V' to RGB conversion, the TMC2272 input data alignment for 10-bit Y'U'V' is:

0	0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
U9	U9	U9	U8	U7	U6	U5	U4	U3	U2	U1	U0
V9	V9	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

where the tripled U9 and V9 sign bits denote two's complement sign extensions. The TMC2272 output data alignment for 8-bit GBR is then:

0	0	0	0	G7	G6	G5	G4	G3	G2	G1	G0
0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

Converting From 8-bit Full Scale YUV to GBR

Following the notation employed earlier, the TMC2272 will be used to convert data in 8-bit YUV format into 8-bit GBR format.

Since Y = 256, U = V = 0, and G = B = R = 255 for saturated white output, every "Y" coefficient will be 255 / 255=1.0. The full matrix for YUV to GBR conversion is:

G = 1.0 (Y) -0.3443 (U) -0.7142 (V)
B = 1.0 (Y) +1.7727 (U)
R = 1.0 (Y) +1.3965 (V)

Since the largest element is over 1.0 and the largest permissible coefficient is 511, multiply all elements of the matrix by 256 to obtain the values to load into the TMC2272:

G = 256 (Y') -88 (U') -83 (V')	dec.
100 3A8 349	hex
B = 256 (Y') +454 (U')	dec.
100 1C6	hex
R = 256 (Y') +359 (V')	dec.
100 167	hex

For the YUV to RGB conversion, the TMC2272 input data alignment for 10-bit Y'U'V' is:

0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	0
U9	U9	U8	U7	U6	U5	U4	U3	U2	U1	U0	0
V9	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0	0

where the doubled U9 and V9 sign bits denote two's complement sign extensions. The TMC2272 output data alignment for 8-bit GBR is then:

0	0	0	0	G7	G6	G5	G4	G3	G2	G1	G0
0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

Note that the inputs have to be doubled because the coefficient gain is 256, whereas the internal gain is 1 / 512, for a net gain of 1/2.

Table 3. Summary of Colorspace Conversion Coefficients

Conversion	KAX KAY KAZ	KBX KBY KBZ	KCX KCY KCZ
RGB to YUV	099 3AA 100	12D 356 32A	03A 100 3D6
RGB to YC_BC_R	083 3B4 0E1	102 36B 344	032 0E1 3DB
YUV to RGB	100 100 100	000 3A8 1C6	167 349 000
YC_BC_R to RGB	149 149 149	000 3CE 102	0CC 398 000

Table 4. Conversion Port Assignments and Alignments

Port	AIN	BIN	CIN	XOUT	YOUT	ZOUT
RGB to YUV	R_{7-0}	G_{7-0}	B_{7-0}	Y_{7-0}	U_{7-0} (e)	V_{7-0} (e)
RGB to YC_BC_R	R_{7-0}	G_{7-0}	B_{7-0}	Y_{9-0}	U_{9-0} (e)	V_{9-0} (e)
YUV to RGB	Y_{8-1} (e)	U_{8-1} (e)	V_{8-1} (e)	R_{7-0}	G_{7-0}	B_{7-0}
YC_BC_R to RGB	Y_{9-0}	C_{B9-0} (e)	C_{R9-0} (e)	R_{7-0}	G_{7-0}	B_{7-0}

where X_{Y-0} denotes right-justified, (e) denotes sign extension, and X_{Y-1} denotes shifted ome bit leftward from right-justified position.

HSV (HSI) Format Conversions

HSV (or HSI) refers to Hue (color) Saturation (vividness) and Value (intensity or brightness), quantities which are directly related to the human perception of light and color. The V (or I) levels are simply the Y (or luminance) levels. Hue and Saturation are derived from the R-Y and B-Y color difference values of a signal.

HSV Calculations:

Value (V) = Intensity (I) = Y

Hue (H) = Arctan (B-Y/R-Y)

Saturation (S) = $\sqrt{(R\text{-}Y)^2 + (B\text{-}Y)^2}$

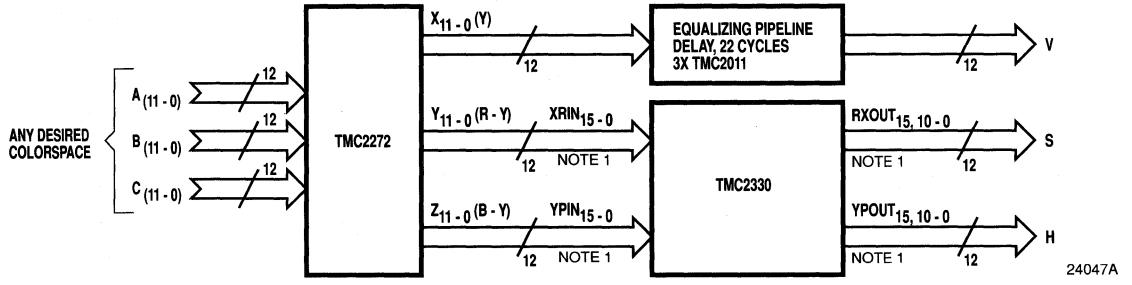
R-Y = S * cos(H)

B-Y = S * sin(H)

One may use two 64Kx8 ROM look-up-tables to calculate Hue and Saturation from R-Y and B-Y in an 8-bit system. However, the finite size of this LUT may limit performance, especially if the TMC2272's full precision is used. The TMC2330, developed to translate between rectangular and polar coordinates, can perform the trigonometric transformations to 16 bit precision at 25MHz. These calculations are the the same as required in HSV calculations. A 4 Giga-byte x 32 bit LUT can achieve the same accuracy and precision as the TMC2330, if it is programmed correctly.

To convert between Y, R-Y, B-Y and HSV, the the TMC2272 isn't needed at all; simply use the TMC2330. To convert between HSV and any other format, use the TMC2330 to translate between HSV and Y, R-Y, B-Y, and use the TMC2272 to translate between Y, R-Y, B-Y and the other format. See ***Figures 9*** and ***10***.

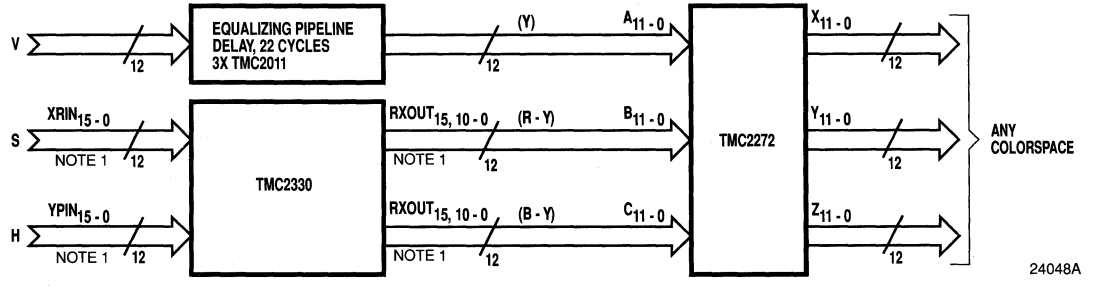
Figure 9. Conversion to HSV



Notes: 1. Connect TMC2272 MSBs (Bits 11) to TMC 2330 MSBs (Bits 15) and also to TMC2330 Bits 14-11. Connect TMC2272 LSBs (Bits 10-0) to TMC2330 LSBs (Bits 10-0). TMC2330 output bits 14-11 are overflow.

2. TMC2272 $Y_{11\text{-}0}$ outputs should not be confused with the designation "Y" used to signify the intensity components. The assignment of components to TMC2272 inputs and outputs may be altered through the selection of appropriate coefficients.

Figure 10. Conversion from HSV



Notes: 1. Connect input MSBs (Bits 11) to TMC2330 MSBs (Bits 15(and also to TMC2330 Bits 14-11. Connect input LSBs (Bits 10-0) to TMC2330 LSBs (Bits 10-0).

2. TMC2272 $Y_{11\text{-}0}$ outputs should not be confused with the designation 'Y' used for an intensity component. Component assignment depends on the coefficients used.

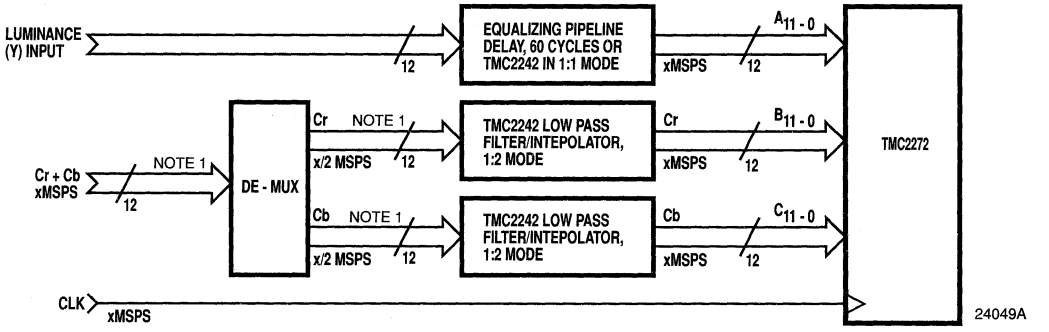
Input Interpolation/Output Decimation and Filtering

In some applications the two color-difference signals (R-Y/B-Y or Cr/Cb, for example,) are transmitted at one-half the rate of the luminance (Y) signal. These two color-difference signals are often multiplexed to one signal which is at the same sample rate as the luminance signal. In many applications, if the color difference signals are already band-limited, it is satisfactory to use the same color difference sample for each two luminance samples. Little improvement is obtained with a simple averaging ([A+B]/2) interpolation filter. If the color difference signal is not band-limited, either of these two methods may yield unsatisfactory results due to aliasing. In this case, a TRW TMC2242 digital low-pass ("half-band") interpolating filter will correctly band-limit each color difference signal as it is interpolated. See *Figure 11.*

The same methods are used to decimate the color difference outputs. Simple decimation by removing every other sample of color information may yield unsatisfactory results due to aliasing. This is a problem because the color difference signals have now been transformed with the higher-bandwidth luminance signals and therefore have higher bandwidths than they had before the transform. The best performance is obtained by using a precise low-pass ("half-band") decimation filter such as the TDC2242 to remove aliasing components. See *Figure 12.*

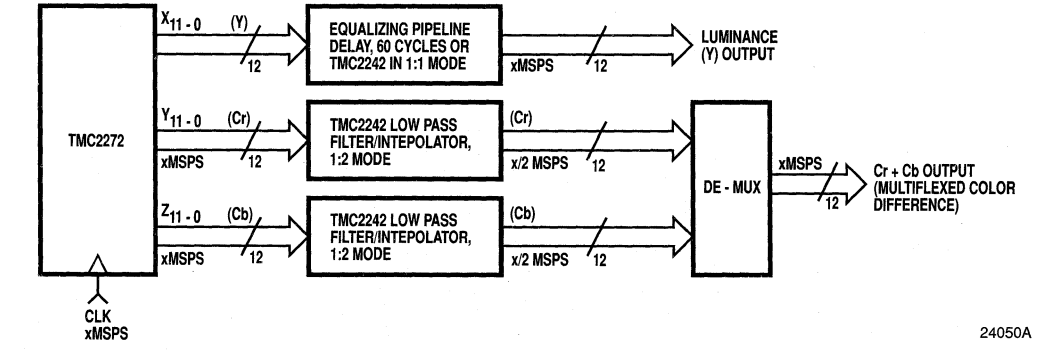
The TMC2242 is a bi-directional, selectable rate filter/ interpolator/decimator

Figure 11. Input Interpolation and Filtering



Notes: 1. Width of input paths will vary with source.
2. See TMC2242 Datasheet for further information.

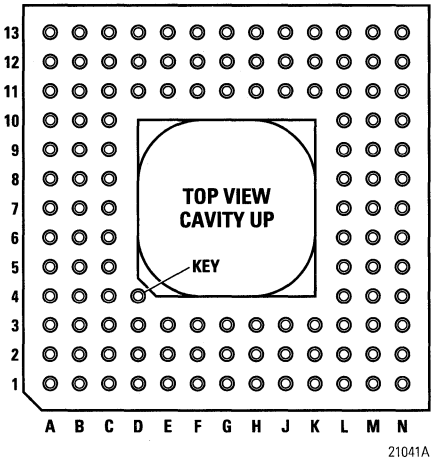
Figure 12. Output Decimation and Filtering



Pin Assignments – 121-Pin Plastic Pin Grid Array H5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	X7	B5	GND	C9	C_0	F1	Y_7	H13	A_1	L5	KC_0	M9	KB_2
A2	X_9	B6	C_9	C10	B_8	F2	Y_8	J1	Y_1	L6	GND	M10	KB_5
A3	X_{10}	B7	C_6	C11	B_5	F3	V_{DD}	J2	Y_2	L7	V_{DD}	M11	KB_9
A4	GND	B8	C_4	C12	B_3	F11	A_7	J3	GND	L8	KB_0	M12	KA_2
A5	C_{11}	B9	C_2	C13	B_1	F12	A_6	J11	KA_8	L9	KB_4	M13	KA_3
A6	C_8	B10	B_{11}	D1	Y_{11}	F13	A_5	J12	$CWSEL_1$	L10	KB_8	N1	Z_5
A7	C_7	B11	B_9	D2	X_0	G1	Y_5	J13	$CWSEL_0$	L11	KA_1	N2	Z_8
A8	C_5	B12	B_6	D3	X_3	G2	Y_6	K1	Y_3	L12	KA_5	N3	Z_{10}
A9	C_3	B13	B_2	D11	CLK	G3	GND	K2	Z_0	L13	KA_6	N4	KC_1
A10	C_1	C1	X_1	D12	B_0	G11	A_3	K3	Z_3	M1	Z_2	N5	KC_3
A11	B_10	C2	X_2	D13	A_{10}	G12	A_2	K11	KA_4	M2	Z_7	N6	KC_5
A12	B_7	C3	X_6	E1	Y_9	G13	A_4	K12	KA_7	M3	Z_9	N7	KC_7
A13	B_4	C4	V_{DD}	E2	Y_{10}	H1	Y_4	K13	KA_9	M4	Z_{11}	N8	KC_8
B1	X_4	C5	GND	E3	GND	H2	Y_0	L1	Z_1	M5	KC_2	N9	KB_1
B2	X_5	C6	C_{10}	E11	A_{11}	H3	V_{DD}	L2	Z_4	M6	KC_4	N10	KB_3
B3	X_8	C7	GND	E12	A_9	H11	GND	L3	Z_6	M7	KC_6	N11	KB_6
B4	X_{11}	C8	V_{DD}	E13	A_8	H12	A_0	L4	GND	M8	KC_9	N12	KB_7
												N13	KA_0

Note: Pin D4 has no electrical connection. It is a mechanical orientation pin.



Ordering Information

Product Number	Speed MHz	Temperature Range	Screening	Package	Package Marking
TMC2272H5C	30	STD-TA = 0°C to 70°C	Commercial	121 Pin Plastic PGA	2272H5C
TMC2272H5C-1	36	STD-TA = 0°C to 70°C	Commercial	121 Pin Plastic PGA	2272H5C-1
TMC2272H5C-2	40	STD-T_A = 0°C to 70°C	Commercial	121 Pin Plastic PGA	2272H5C-2

40G06753 Rev B 8/93

TMC2301
CMOS Image Resampling Sequencer
15, 18 MHz

Description

The TMC2301 is a VLSI circuit which supports image resampling, rotation, rescaling and filtering by generating input bit plane, interpolation coefficient lookup table, and output bit plane memory addresses along with external multiplier-accumulator control signals. The TMC2301 can process data fields of up to 4096 x 4096 multibit words at a clock rate of up to 18 MHz. An IRS-based system can nearest-neighbor resample a 512 x 512 image in 15 milliseconds, translating, zooming, rotating, or warping it, depending on the transform parameter set loaded. A complete bilinear interpolation of the same image can be completed in 60 milliseconds. Image resampling speed is independent of the angle of rotation, degree of warp, or amount of zoom specified.

A high performance, TMC2301-based system can execute bilinear and cubic convolution algorithms that rotate images accurately and in real time. Keystone or other perspective correction, image plane distortion, and numerous other second order polynomial transformations can be programmed and executed under direct user control. Direct access to the interpolation coefficient lookup table allows dynamic modification of the algorithm.

Following an initialization with the transform parameters and control bits defining the operation to be executed, the IRS assumes control of the input and output data fields and executes unattended. Data word size is user selectable. All inputs except INTER and all outputs are registered on the rising edge of clock. All outputs are three-state controlled except ACC, CZERO, END, and DONE.

Fabricated in a 1 micron CMOS process, the TMC2301 operates at clock rates of up to 18 MHz over the full commercial (0 to 70°C) temnperature at 15 MHz over the extended (-55 to +125°C) temperature and supply voltage ranges. All signals are TTL compatible.

Features

- Rotation, warping, panning, zooming, and compression of images in real time
- 18 MHz clock rate
- 4096 x 4096 image field addressing capability
- User-selectable nearest-neighbor, bilinear interpolation, and cubic convolution resampling algorithms
- Static convolutional filtering of up to 16 x 16 pixel windows
- Single-pass or two-pass convolution operations
- Low power consumption CMOS process
- Single 5V power supply
- Available in a 68-pin grid array and low-cost plastic leaded chip carrier (J-bend)

Applications

- Video special-effects generators
- Image recognition systems, robotics
- Artificial intelligence
- High-precision image registration (LANDSAT processing)
- High-speed data encoding/decoding
- General purpose image processing
- Image data compression

Logic Symbol

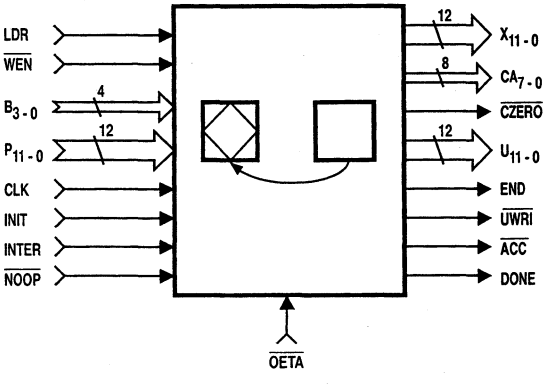


Table 3. Parameter Registers Binary Format (Row or Column Sequencer)

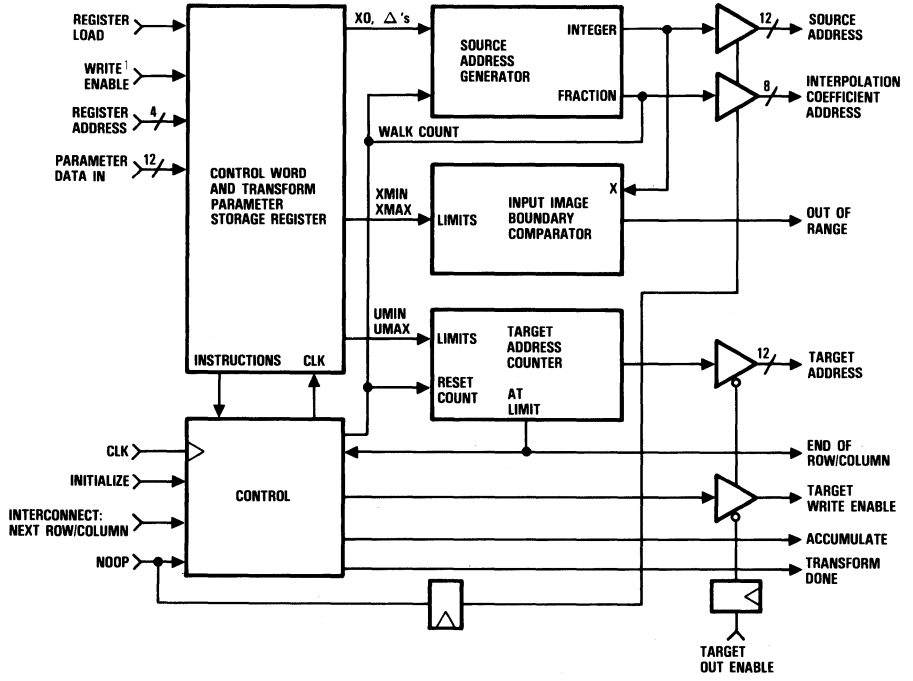
Addr.	Format MSB											LSB	Limits Dec	Limits Hex	Name
0000*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000	XMIN
0001*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000	XMAX
0010	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	$4096-2^{-5}$ -4096	0FFF.F8 F000.00	X_O
							2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}			
0011 (Control)	ALR	AIN	PIPE	R/C	M_1	M_0									
0100	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	$128-2^{-12}$ -128	007F.FFF FF80.000	DX/DU_0
0101					-2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}			
0101* (TM, FOV)	TM	2^{2}	2^{1}	2^{0}											
0110	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	$128-2^{-12}$ -128	007F.FFF FF80.000	DX/DV_0
0111					-2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}			
0111* (Kernel)	2^{3}	2^{2}	2^{1}	2^{0}											Kernel
1000	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-10}	$8-2^{-20}$ -8	0007.FFFFF FFF8.00000	$D^2X/DU2V$
1001	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}			
1010	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-10}	$8-2^{-20}$ -8	0007.FFFFF FFF8.00000	D^2X/DU^2
1011	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}			
1100	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$8-2^{-20}$ -8	0007.FFFFF FFF8.00000	D^2X/DV^2
1101	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}			
1110*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000	UMIN
1111*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000	UMAX

* unsigned binary notation
A "-" indicates MSB is sign bit

Internal Bit Mapping TMC2301 (For parametric inputs, integers in table are bits of P, the input point)

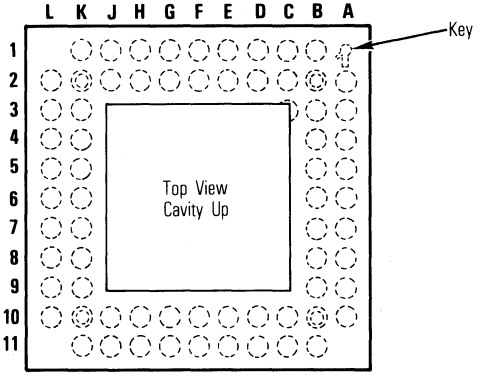
	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}
X_{OUT} [11:0]		11	10	9	8	7	6	5	4	3	2	1	0																			
C_{ADN} [7:4]														7	6	5	4															
XMAX, XMIN		11	10	9	8	7	6	5	4	3	2	1	0																			
X_O 5		4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0														
DX/DU, DX/DV						7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0							
$D^2X/DUDV$, $D^2X/DU2$ $D^2X/DV2$										11	10	9	8	7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0

Functional Block Diagram

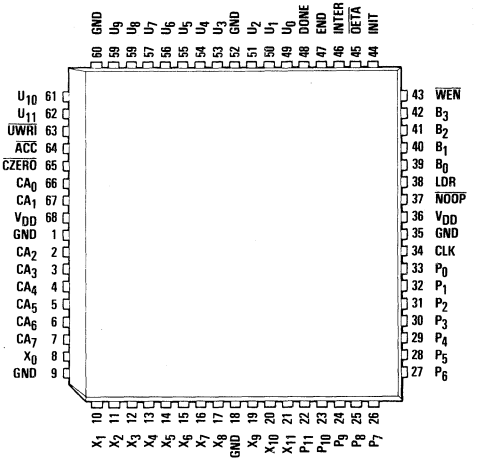


Pin Assignments – 68 Pin Grid Array, G8 or H8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	INIT	K2	U_{10}	K10	X_1	B10	P_6
B1	$\overline{OETA}$	L2	U_{11}	K11	X_2	A10	P_5
C2	INTER	K3	$\overline{UWRI}$	J10	X_3	B9	P_4
C1	END	L3	$\overline{ACC}$	J11	X_4	A9	P_3
D2	DONE	K4	$\overline{CZERO}$	H10	X_5	B8	P_2
D1	U_0	L4	CA_0	H11	X_6	A8	P_1
E2	U_1	K5	CA_1	G10	X_7	B7	P_0
E1	U_2	L5	V_{DD}	G11	X_8	A7	CLK
F2	GND	K6	GND	F10	GND	B6	GND
F1	U_3	L6	CA_2	F11	X_9	A6	V_{DD}
G2	U_4	K7	CA_3	E10	X_{10}	B5	$\overline{NOOP}$
G1	U_5	L7	CA_4	E11	X_{11}	A5	LDR
H2	U_6	K8	CA_5	D10	P_{11}	B4	B_0
H1	U_7	L8	CA_6	D11	P_{10}	A4	B_1
J2	U_8	K9	CA_7	C10	P_9	B3	B_2
J1	U_9	L9	X_0	C11	P_8	A3	B_3
K1	GND	L10	GND	B11	P_7	A2	$\overline{WEN}$



Pin Assignments



68 Leaded (J Bend) Plastic Chip Carrier – L1 or R1 Package

Functional Description

General Information

The IRS is a versatile self–sequencing address generator designed primarily to filter a two–dimensional image or to remap and resample it from one set of Cartesian coordinates (x, y) into a new, transformed set (u, v). Most applications use two identical devices in tandem, one generating the row coordinates (X and U), the other generating the column coordinates (Y and V). The algorithm performed by the TMC2301 consists of two steps: a coordinate system transformation, followed by pixel interpolation. Interpolation is necessary when the transformed pixel positions (U, V) do not coincide with the original pixel positions (X, Y). The new pixel intensity values are obtained by interpolating the original pixels in the neighborhood of the transformed pixel positions. See Figure 1.

The IRS executes a general second order coordinate transformation of the form:

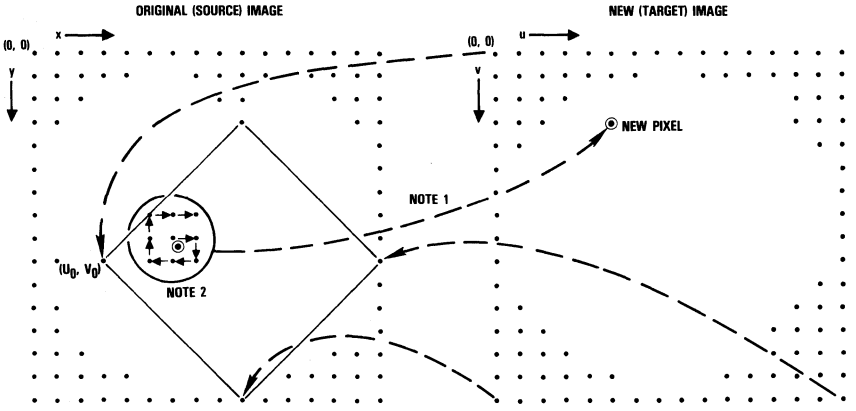
$$X(u, v) = Au^2 + Bu + Cuv + Dv^2 + Ev + F$$
$$Y(u, v) = Gu^2 + Hu + Kuv + Lv^2 + Mv + N$$

where A through N are user–defined parameters. It steps sequentially through the pixels of a user–defined rectangle in the new set of coordinates, computing the "old" address (X, Y) corresponding to each "new" location (U, V).

The TMC2301 uses the external multiplier–accumulator, connected to the system clock, to calculate the interpolated pixel value by summing the products of the original pixel values stored in the source buffer RAM and the appropriate weights from the polynomial transform lookup table. The new interpolated image value is then stored in the corresponding (U, V) memory location. Finally, the new image address is incremented by one pixel in the "U" direction or reset to the start of the next line (with "V" incremented), proceeding line–by–line through the entire destination image.

The TMC2301 can support any nearest neighbor, bilinear, or cubic resampling, according to the user's requirements. The bilinear and cubic kernels require a coefficient lookup table and multiplier–accumulator. Both one–pass and two–pass algorithms are supported. Sophisticated "walkaround" algorithms implementing static filters are also easily realized, utilizing convolutional kernels of up to 16 x 16 pixels. Both one and two–pass algorithms are supported. For each output point in a typical static single–pass filter, the IRS will generate a series of addresses, "walking" around that point in two dimensions. At the end of each walk, it will advance one pixel along the output scan line, then begin the walk for the next pixel.

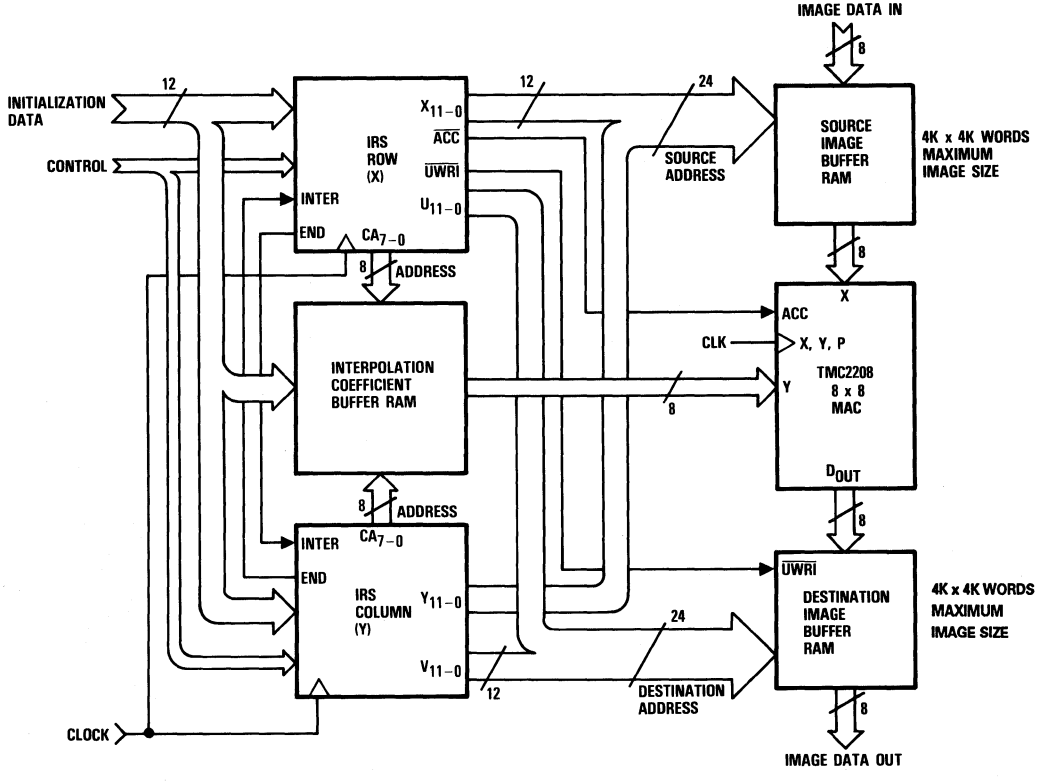
Figure 1. Image Resampling Geometry Showing Image Rotation and Expansion



Notes:
1. Coordinate transformation U, V pixel mapped into X, Y coordinates.
2. Pixel interpolation walk new U, V pixel intensity calculated from surrounding X, Y pixel neighborhood.

A basic TMC2301-based system is shown in Figure 2. In this typical system, two Image Resampling Sequencers process the image. The only other external parts needed are a multiplier-accumulator, external interpolation coefficient lookup table RAM, and the user-specified Source and Destination Image Memory.

Figure 2. Basic 2-D Image Convolver Using TMC2301 Image Resampling Sequencer Utilizing Typical 8-Bit Data Path



Signal Definitions

Power

V_{DD}, GND — The TMC2301 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The TMC2301 has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

P_{11-0} — The coordinate transformation parameters are loaded through the registered 12-bit P input port. P_{11} is the Most Significant Bit.

B_{3-0} — The write addresses for the individual coordinate transform parameters are presented at the registered 4-bit B input port. B_3 is the Most Significant Bit.

Outputs

X_{11-0} — The current X (or Y) source pixel address of the image being resampled is indicated by the registered 12-bit X_{11-0} output bus. This output is forced to the high impedance state when $\overline{NOOP}$ is LOW. X_{11} is the Most Significant Bit.

CA_{7-0} — The current interpolation kernel coefficient lookup table address is indicated by the registered 8-bit CA_{7-0} output bus. This output is forced to the high impedance state when $\overline{NOOP}$ is LOW. CA_7 is the Most Significant Bit.

U_{11-0} — The U (or V) target address of the image being generated is indicated by the registered 12-bit U_{11-0} output bus. This output is forced to the high impedance state when $\overline{OETA}$ is HIGH. U_{11} is the Most Significant Bit.

Controls

INIT — The control logic is cleared and initialized for the start of a new image transformation when the registered INIT input is HIGH for a minimum of two clock cycles. Normal operation begins after INIT goes LOW.

$\overline{WEN}$ — The registered Write Enable input allows the transformation parameters to be written into the preload register indicated by the address at the B input port when LOW. See Figure 4.

LDR — The data held in all transformation parameter preload registers is latched into the storage registers when the registered input LDR is HIGH. When LDR is LOW, the parameters remain unchanged. See Figure 4.

$\overline{ACC}$ — The accumulation register of the external multiplier-accumulator is initialized by the registered $\overline{ACC}$ output. $\overline{ACC}$ goes LOW for one cycle at the start of each interpolation "walk," effectively clearing the storage register by loading in only the new first product. See Figure 9.

$\overline{UWRI}$ — After the end of each interpolation "walk," the Target Memory (U or V) Write Enable goes LOW for one clock cycle. See Figure 9. This registered output is forced to the high impedance state when $\overline{OETA}$ is HIGH.

INTER — In the common two-device system configuration, the Interconnect inputs are connected to the END flag outputs. The END flag from the row (X) sequencer thus indicates an "end of line" to the column (Y) device, while the column sequencer in turn sends a "bottom of frame" signal to the row device, forcing a reset of the address counter.

$\overline{NOOP}$ — The Clock is overidden when the registered input $\overline{NOOP}$ is LOW, holding all address generators in their current state. Also, the output buffers for the address busses X_{11-0} and CA_{7-0} are forced to the high impedance state. This allows the user access to all external memory. When $\overline{NOOP}$ goes HIGH, normal operation resumes on the next clock cycle.

$\overline{OETA}$ — The target memory outputs $\overline{UWRI}$ and address bus U_{11-0} are in the high-impedance state when the registered Output Enable input is HIGH. When $\overline{OETA}$ is LOW, they are enabled on the next clock cycle.

Flags

$\overline{\text{CZERO}}$ — The registered $\overline{\text{CZERO}}$ flag of a horizontal dimension TMC2301 goes HIGH if $X < 0$, $XMIN \leq X \leq XMAX$, or $X \geq 4096$ (1000 hex). It goes LOW if $0 \leq X < XMIN$ or $XMAX < X < 4096$. The logical AND of the $\overline{\text{CZERO}}$ flags of a two-dimensional pair of TMC2301s will go LOW when the source address falls outside a rectangle with vertices (XMIN, YMIN), (XMAX, YMIN), (XMIN, YMAX), and (XMAX, YMAX), denoting an invalid address. The external data path can be wired to substitute a selected background value whenever this AND = 0.

END — The registered END flag goes HIGH during the last pixel of the last walk in a row in the case of the row chip, and the last pixel of the last walk in a column in the column chip, in the two-device architecture. This output is used as the end-of-line and end-of-frame indicator in conjunction with the INTER inputs of both TMC2301s.

DONE — In the standard two-device system, a row sequencer DONE flag HIGH after the last walk at the end of the last row of an image (during $\overline{\text{UWRI}}$ LOW) indicates the end of the transform. This registered output is usually ignored on the column device. See the Transformation Control Parameters, AUTOINIT.

Package Interconnections

Signal Type	Signal Name	Function	G8, H8 Package Pins	L1, R1 Package Pins
Power	V_{DD}	Supply Voltage	L5, A6	36, 68
	GND	Ground	F2, K1, K6, L10, F10, B6	1, 9, 18, 35, 52, 60
Clock	CLK	System Clock	A7	34
Inputs	P_{11-0}	Parameter Register Data	D10, D11, C10, C11, B11, B10, A10, B9, A9, B8, A8, B7	22, 23, 24, 25, 26, 27 28, 29, 30, 31, 32, 33
	B_{3-0}	Parameter Register Address	A3, B3, A4, B4	42, 41, 40, 39
Outputs	X_{11-0}	Source Address	E11, E10, F11, G11, G10, H11 H10, J11, J10, K11, K10, L9	21, 20, 19, 17, 16, 15, 14, 13, 12, 11, 10, 8
	CA_{7-0}	Coefficient Address	K9, L8, K8, L7, K7, L6, K5, L4	7, 6, 5, 4, 3, 2, 67, 66
	U_{11-0}	Target Address	L2, K2, J1, J2, H1, H2, G1, G2, F1, E1, E2, D1	62, 61, 59, 58, 57, 56, 55, 54, 53, 51, 50, 49
Controls	INIT	Initialize	B2	44
	$\overline{\text{NOOP}}$	No Operation	B5	37
	$\overline{\text{WEN}}$	Parameter Write Enable	A2	43
	LDR	Lead Parameter Data Registers	A5	38
	$\overline{\text{ACC}}$	Accumulate	L3	64
	$\overline{\text{OETA}}$	Target Memory Output Enable	B1	45
	$\overline{\text{UWRI}}$	Target Memory Write Enable	K3	63
	INTER	Interconnect	C2	46
Flags	$\overline{\text{CZERO}}$	Coefficient Zero	K4	65
	END	End of Row/Page	C1	47
	DONE	End of Transform	D2	48

Transformation Control Parameters

The TMC2301 is a self-sequencing device which requires no cycle-to-cycle intervention from the host system. To program the device, the user loads the 16 operating parameters, which define the transformation to be performed, which sections of the original and resampled image spaces are to be utilized, and various control words. Filtering operations are further defined by the values the user loads into the external coefficient memory. The transform parameters are described below. See also Tables 1 through 3.

XMIN, XMAX, YMIN, YMAX — These four parameters outline the "source" rectangular region of the original image. Whenever the IRS pair generates an (X, Y) address within this boundary the $\overline{CZERO}$ flags will denote a valid memory read. In the most common case, XMIN < XMAX, YMIN < YMAX, 000h < X < FFFh <, and 000h < Y < FFFh. In this case, addresses out-of-bounds cause one or both $\overline{CZEROs}$ to go LOW. Refer to Application Note TP-38 for further information on other boundary violation cases. Each parameter is expressed in 12-bit unsigned binary integer notation. See Figure 12.

UMIN, UMAX, VMIN, VMAX — These four parameters outline the "target" region of the (u, v) plane, into which the resampled image will be written. The IRS will generate, line by line, a scan that fills only this portion of the plane, permitting the user to assemble a mosaic of multiple rectangular subimages. Care must be taken to ensure that UMAX > UMIN and VMAX > VMIN. Each parameter is expressed in 12-bit unsigned binary integer notation. See Figure 12.

(X_0, Y_0) — These are the coordinates of the first pixel to be read from the original image. In many applications, this point will be one of the four corners of the original image to be resampled. The pixels near (X_0, Y_0) in the original image will be used to compute the upper left pixel of the transformed image. In non-inverting, non-reversing applications (X_0, Y_0) will be the upper left corner of the original subimage. Each coordinate is expressed in 13-bit integer plus 5-bit fraction, two's complement notation.

dX/dU_0 — Is the initial horizontal partial first derivative indicating the displacement along the X axis which corresponds to each one-pixel movement along the U axis. Usually, $0 < dX/dU_0 < 1$ corresponds to magnification, whereas $dX/dU_0 > 1$ represents reduction and $dX/dU_0 < 0$ denotes reflection about a vertical axis. The first derivatives are expressed in 8-bit integer, 12-bit fraction two's complement notation.

dX/dV_0 — Is the initial horizontal-vertical partial first derivative. It indicates the displacement along the X axis corresponding to each one-pixel movement along the V axis. The coefficients dX/dV_0 and dY/dU_0 define image rotation and shear.

dY/dU_0 — Is the initial vertical-horizontal partial first derivative. It indicates the displacement along the Y axis corresponding to each one-pixel movement along the U axis.

dY/dV_0 — Is the initial vertical partial first derivative. It indicates the displacement along the Y axis corresponding to each one-pixel step along the V axis. Since dX/dU_0 and dY/dV_0 are separate parameters, vertical magnification and reflection need not match their horizontal counterparts.

NOTE: For each incremental move along the U axis, the starting point of the new "walk around spiral" is indexed to the ENDING point of the previous walk around spiral, rather than to its center. Therefore, the terms dX/dU_0 and dY/dU_0 must be adjusted accordingly. Since each new line is referenced back to the previous line's initial spiral starting point, no similar dX/dV_0 or dY/dV_0 correction is needed.

d^2X/dU^2 — Is the second order horizontal derivative. It indicates the rate of change of the horizontal-horizontal first derivative with each step along a line in the output image space. All six second-order derivatives are 4-bit integer, 20-bit fractional two's complement parameters.

d^2X/dV^2 Is the second order horizontal-vertical-vertical derivative. It indicates the rate of change of the horizontal-vertical first derivative with each step down a column in the output image space.

d^2Y/dU^2 Is the second order vertical-horizontal-horizontal derivative. It indicates the rate of change of the the vertical-horizontal first derivative with each step along a line of the output image space.

d^2Y/dV^2 Is the second order vertical derivative. It indicates the rate of change of the vertical-vertical first derivative with each step down a column of the output image space.

$d^2X/dUdV$ Is the mixed second order derivative indicating the rate of change of the first order horizontal derivative as one proceeds downwards through the output image space. This is also the rate of change of the first order horizontal-vertical derivative during horizontal sweeps in the output image space.

$d^2Y/dUdV$ Is the mixed second order derivative indicating the rate of change of the first order vertical derivative as one moves horizontally across the output space, or, equivalently, the rate of change of the first order vertical-horizontal derivative as one moves vertically in the output image space.

Row/Column Select Sets the mode to either Row (0) or Column (1) operation.

Mode This 2-bit control word defines three unique instructions:

Code	Instruction
00, 01	single-pass operation
10	pass 1 of two-pass operation
11	pass 2 of two-pass operation

In single-pass operation, the device walks through the entire (k + 1) x (k + 1) kernel for each output pixel, where k is the value written into the Kernel section (see below) of the parameter register. Two-pass operation, which requires a dimensionally separable kernel, is executed first for a (k + 1) element kernel in one direction, then for a (k + 1) element kernel in the other direction. For kernel sizes exceeding 2 x 2, the two-pass algorithm is obviously beneficial, requiring 2n samples per output point instead of n x n. In this case, the intermediate image data stored in the destination image memory following the first pass is used as the source image data on the second pass. The user may design his system to switch source and destination memory bank addresses in place, or could utilize a second TMC2301 pair in a pipelined architecture. This would require a third image buffer for the final destination image. Both devices of a system pair are usually set to the same mode.

Kernel The effective kernel width (height) exceeds this 4-bit unsigned number by 1, thereby providing kernels of 1 x 1 to 16 x 16 source pixels per output, for either resampling or filtering. Simple static filters can be implemented with kernels of up to 16 x 16 pixels (Kernel = 15), while resampling interpolation kernels are limited to 4 x 4 pixels (Kernel = 3), due to the four bits of fractional X (or Y) address generated by the TMC2301. See the Applications Discussion, below. Again, both devices in a pair are generally initialized with equal Kernel values.

Field of View (FOV) As the device walks through its kernel coefficients, each corresponding step in (x, y) space is normally one pixel length or height; this is a field of view of 1. However, the user can subsample the original space before filtering or resampling, by applying the coefficient kernel over a view field of up to 7 units. At a field of view of F, the pixels selected for each kernel operation are F pixels apart. This is useful in oversampled pictures, whose intensity changes only slowly from pixel to pixel.

Autoload (ALR) When set to 1 (HIGH), the LDR control is automatically asserted when INIT is strobed, loading the coefficient set currently stored in the preload registers.

Autoinit (AIN) At the end of an image, if the AIN bit is 1 (HIGH) the DONE flag goes HIGH for one clock cycle and a new transform begins. If 0 (LOW), $\overline{\text{UWRT}}$ and the DONE flag remain HIGH during the sequence until the user strobes the INIT control to begin a new image transformation.

Pipe (PIPE)

Adjusts the timing of the target memory write controls, to compensate for buffered source image RAM. If the PIPE bit is 1 (HIGH), outputs $\overline{ACC}$ and $\overline{UWRI}$ will be delayed one clock cycle relative to the generation of the target address (U or V). See Figure 9.

Test Mode (TM)

This mode is available for user inspection of the coefficient data. The source image and coefficient addresses are calculated by an internal 28-bit accumulator. When TM is 1 (HIGH), the sign bit, normally discarded, and the lower 11 bits of internal data are substituted for the upper 12 bits appearing at the source address port (X) during a standard transform cycle. This allows user verification of algorithm mathematics during debug. Since the TM bit is registered and cannot be changed during a single clock cycle, two distinct clock cycles are required to access both the MSW and LSW of the internal accumulator. See Figure 3.

Figure 3. Test Mode Data Routing

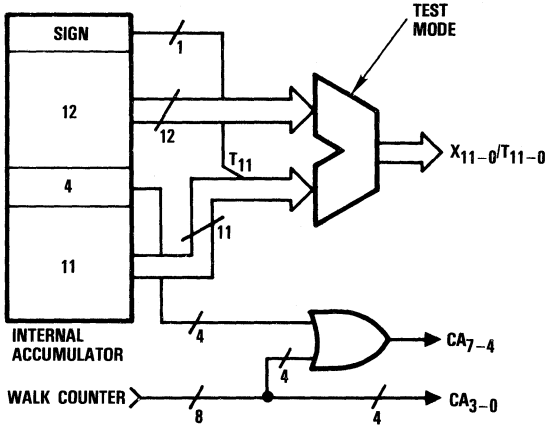


Table 1. Parameter Registers – Row Sequencer

Address	Name	Description
0000	XMIN	Left side of Source Window
0001	XMAX	Right side of Source Window
0010	X_0 (LSW)	Source starting point – X coordinate
0011	X_0 (MSW)	Source starting point – X coordinate
0011	Controls	Mode Select Bits
0100	dX/dU_0 (LSW)	Row/Row first differential
0101	dX/dU_0 (MSW)	Row/Row first differential
0101	TM, FOV	Test Mode, Field of View
0110	dX/dV_0 (LSW)	Row/Column first differential
0111	dX/dV_0 (MSW)	Row/Column first differential
0111	Kernel	Resampling/Filtering Kernel
1000	$d^2X/dUdV$ (LSW)	Mixed second differential
1001	$d^2X/dUdV$ (MSW)	Mixed second differential
1010	d^2X/dU^2 (LSW)	Row second differential
1011	d^2X/dU^2 (MSW)	Row second differential
1100	d^2X/dV^2 (LSW)	Row/Column second differential
1101	d^2X/dV^2 (MSW)	Row/Column second differential
1110	UMIN	Left edge of Final Image
1111	UMAX	Right edge of Final Image

Table 2. Parameter Registers – Column Sequencer

Address	Name	Description
0000	YMIN	Top of Source Window
0001	YMAX	Bottom of Source Window
0010	Y_0 (LSW)	Source starting point – Y coordinate
0011	Y_0 (MSW)	Source starting point – Y coordinate
0011	Controls	Mode Select Bits
0100	dY/dU_0 (LSW)	Column/Row first differential
0101	dY/dU_0 (MSW)	Column/Row first differential
0101	TM, FOV	Test Mode, Field of View
0110	dY/dV_0 (LSW)	Column/Column first differential
0111	dY/dV_0 (MSW)	Column/Column first differential
0111	Kernel	Resampling/Filtering Kernel Size
1000	$d^2Y/dUdV$ (LSW)	Mixed second differential
1001	$d^2Y/dUdV$ (MSW)	Mixed second differential
1010	d^2Y/dU^2 (LSW)	Column/Row second differential
1011	d^2Y/dU^2 (MSW)	Column/Row second differential
1100	d^2Y/dV^2 (LSW)	Column second differential
1101	d^2Y/dV^2 (MSW)	Column second differential
1110	VMIN	Top edge of Final Image
1111	VMAX	Bottom edge of Final Image

Table 3. Parameter Registers Binary Format (Row Or Column Sequencer)

Addr	Format												Limits	
	MSB											LSB	Dec	Hex
0000*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
0001*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
0010 0011	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0} -2^{12}	2^{-1} 2^{11}	2^{-2} 2^{10}	2^{-3} 2^{9}	2^{-4} 2^{8}	2^{-5} 2^{7}	$4096-2^{-5}$ -4096	0FFF.F8 F000.00
0011 (Control)	ALR	AIN	PIPE	R/C	M_1	M_0								
0100 0101	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5} -2^{7}	2^{-6} 2^{6}	2^{-7} 2^{5}	2^{-8} 2^{4}	2^{-9} 2^{3}	2^{-10} 2^{2}	2^{-11} 2^{1}	2^{-12} 2^{0}	$128-2^{-12}$ -128	007F.FFF FF80.000
0101* (TM, FOV)	TM	2^{2}	2^{1}	2^{0}										
0110 0111	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5} -2^{7}	2^{-6} 2^{6}	2^{-7} 2^{5}	2^{-8} 2^{4}	2^{-9} 2^{3}	2^{-10} 2^{2}	2^{-11} 2^{1}	2^{-12} 2^{0}	$128-2^{-12}$ -128	007F.FFF FF80.000
0111* (Kernel)	2^{3}	2^{2}	2^{1}	2^{0}										
1000 1001	2^{-9} -2^{3}	2^{-10} 2^{2}	2^{-11} 2^{1}	2^{-12} 2^{0}	2^{-13} 2^{-1}	2^{-14} 2^{-2}	2^{-15} 2^{-3}	2^{-16} 2^{-4}	2^{-17} 2^{-5}	2^{-18} 2^{-6}	2^{-19} 2^{-7}	2^{-20} 2^{-8}	$8-2^{-20}$ -8	0007.FFFFF FFF8.00000
1010 1011	2^{-9} -2^{3}	2^{-10} 2^{2}	2^{-11} 2^{1}	2^{-12} 2^{0}	2^{-13} 2^{-1}	2^{-14} 2^{-2}	2^{-15} 2^{-3}	2^{-16} 2^{-4}	2^{-17} 2^{-5}	2^{-18} 2^{-6}	2^{-19} 2^{-7}	2^{-20} 2^{-8}	$8-2^{-20}$ -8	0007.FFFFF FFF8.00000
1100 1101	2^{-9} -2^{3}	2^{-10} 2^{2}	2^{-11} 2^{1}	2^{-12} 2^{0}	2^{-13} 2^{-1}	2^{-14} 2^{-2}	2^{-15} 2^{-3}	2^{-16} 2^{-4}	2^{-17} 2^{-5}	2^{-18} 2^{-6}	2^{-19} 2^{-7}	2^{-20} 2^{-8}	$8-2^{-20}$ -8	0007.FFFFF FFF8.00000
1110*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
1111*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000

* unsigned binary notation

A "-" indicates MSB is sign bit

Operation of the Transformation Parameter Registers

Numerous applications require the ability to update the coordinate transformation parameters "on the fly." Because the parameters are double-buffered, the user can load any or all of them into the preload registers without upsetting the operation in progress. Then LDR (load data registers) will update all transform parameters to the new values simultaneously. This feature is particularly valuable for "pin cushion" and "fish eye" transformations, or polar-to-rectangular conversions, which cannot be performed with constant second derivatives. The Autoload function updates the preload registers at the beginning of a new image automatically. See the Transformation Control Parameters section. Note also that data can be loaded in to the registers while $\overline{\text{NOOP}}$ is active (LOW).

Figure 4. Operation of LDR Control for Parameter Update

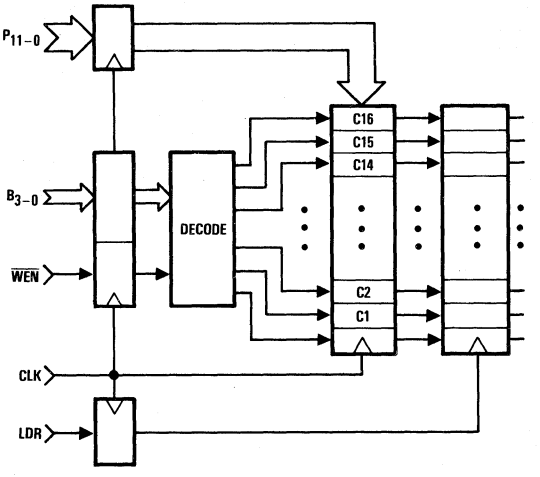
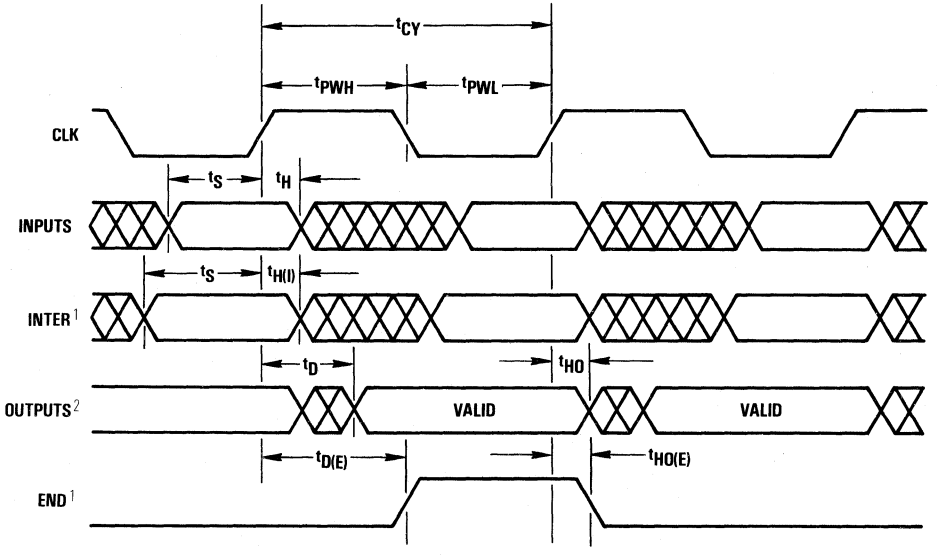


Figure 5. Timing Diagram



Notes:

1. t_S and $t_{D(E)}$ are guaranteed to allow full speed operation in the standard two-device architecture. See text.
2. All outputs except END. See text.

Figure 6. Equivalent Input Circuit

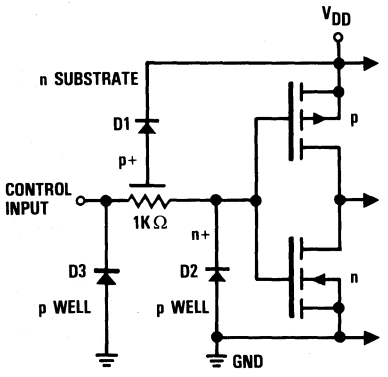


Figure 7. Equivalent Output Circuit

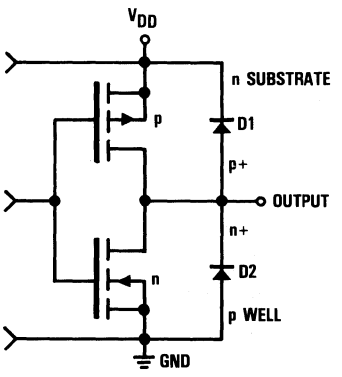
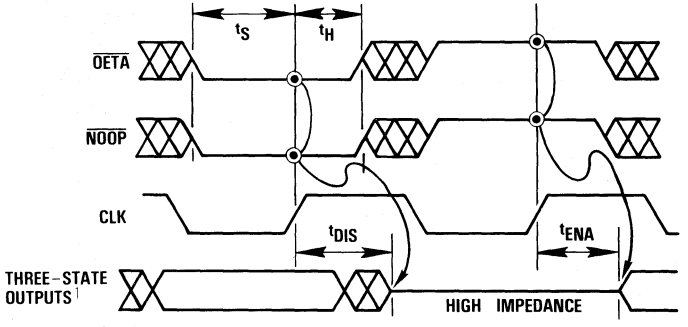


Figure 8. Transition Level for Three-State Measurement



Note:
1. All outputs except $\overline{CZERO}$, $\overline{ACC}$, END and DONE.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	**−0.5 to +7.0V**
Input Voltage	**−0.5 to (V_{DD} +0.5)V**
Output	
Applied voltage [2]	−0.5 to (V_{DD} +0.5)V
Forced current [3,4]	−1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			8.0			8.0	mA
I_{OH}	Output Current, Logic HIGH			−4.0			−4.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 15MHz		75		75	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10	+10	−75	+75	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Min, V_{IN} = V_{DD}	−10	+10	−75	+75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Min, V_{IN} = 0V	−40	+ 40	−40	+ 40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Min, V_{IN} = V_{DD}	−40	+ 40	−40	+ 40	μA
I_{OS}	Short-Circuit Output Current [2]	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Notes:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Guaranteed but not tested.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard –1 Min	Standard –1 Max	Standard Min	Standard Max	Extended Min	Extended Max	Units
t_{CY}	Cycle Time	V_{DD} = Min	55		66		66		ns
t_{PWL}	Clock Pulse Width LOW	V_{DD} = Min	25		30		30		ns
t_{PWH}	Clock Pulse Width HIGH	V_{DD} = Min	25		30		30		ns
t_S	Input Setup Time[1]		18		20		20		ns
t_H	Input Hold Time		2		2		2		ns
$t_{H(I)}$	Input Hold Time, INTER		10		10		10		ns
t_D	Output Delay[2]	V_{DD} = Min, C_{LOAD} = 40pF		27		35		35	ns
$t_{D(E)}$	Output Delay, END[1]	V_{DD} = Min, C_{LOAD} = 10pF		37		45		45	ns
t_{HO}	Output Hold Time[2]	V_{DD} = Max, C_{LOAD} = 40pF	5		5		5		ns
$t_{HO(E)}$	Output Hold Time, END	V_{DD} = Max, C_{LOAD} = 10pF	10		10		10		ns
t_{DIS}	Three-State Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		18		20		20	ns
t_{ENA}	Three-State Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF	27		35		35		ns

Notes:
1. $t_S + t_{D(E)} = t_{CY}$ max.
2. Excluding output pin END.

Applications Discussion

Basic Operation

Each TMC2301 pair contains address controllers which execute patterns much like the following FORTRAN 3-level nested DO loop:

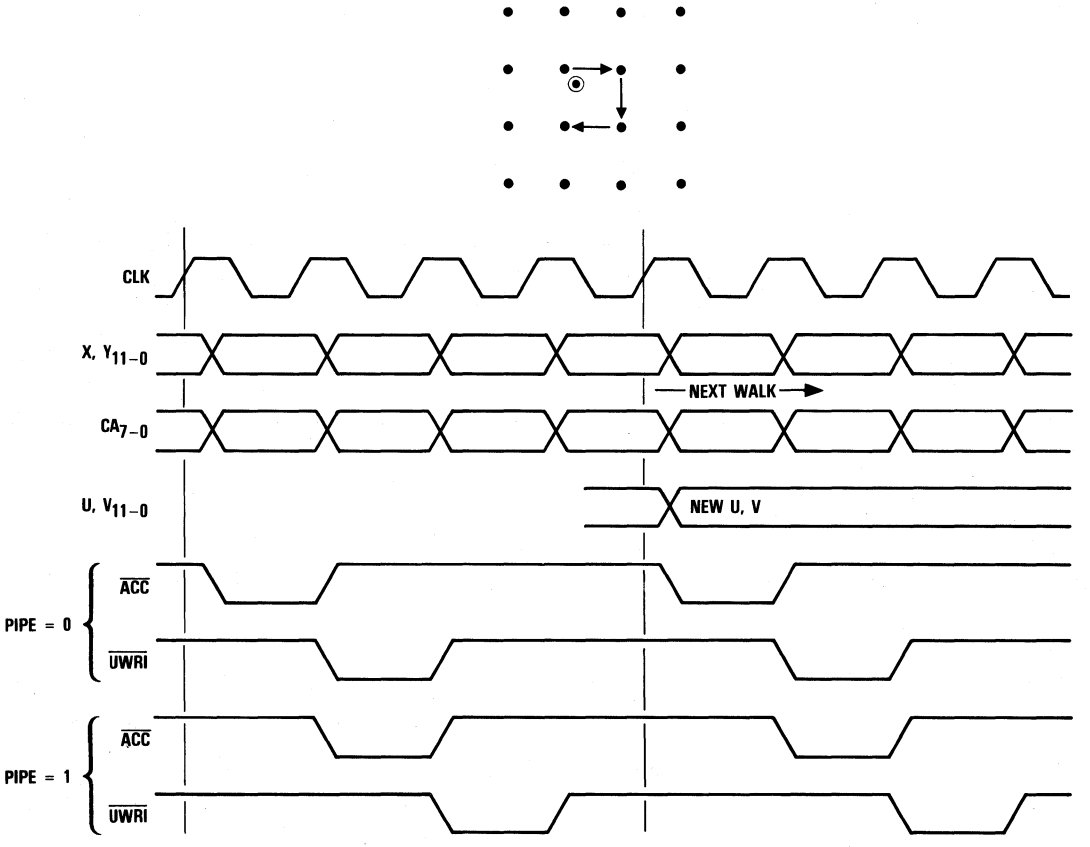
1. The inner loop is a clockwise outgoing spiral "walk" through the N-element coefficient kernel.
2. The middle loop is a left-to-right "scan" along each row of the output image space.
3. Finally, the outer loop is a top-to-bottom "scan" down each column of the output image space.

A typical one-pass image transformation proceeds as follows:

1. The device pair outputs the addresses (X_0, Y_0), which is the first point in the source image, and (CAX, CAY), the interpolation lookup table address for the first pixel in the kernel. The output $\overline{ACC}$ goes LOW, causing the external accumulator to load the first product without summation, clearing the accumulator.
2. For the next N cycles, the IRS walks through an outward clockwise spiral in (x, y) space, accumulating pixel-interpolation coefficient products. The spiral sequence is depicted in Figure 9.
3. After the completion of the first spiral walk, the IRS outputs the target address of the first pixel, (UMIN, VMIN) and the control $\overline{UWRI}$, along with the initial (X, Y) values of the next spiral walk. $\overline{ACC}$ and $\overline{UWRI}$ can be delayed by one clock cycle by setting the control bit PIPE to 1 (HIGH), simplifying the task of interfacing the TMC2301 to buffered source image memory.
4. After the last cycle of the next spiral, $\overline{UWRI}$ again goes LOW for one clock, and the target address outputs are updated, pointing to the location of the pixel calculation just completed, (UMIN + 1, VMIN).

5. The third spiral walk begins with $\overline{ACC}$ going LOW, and ends with (UMIN + 2, VMIN) output and $\overline{UWRI}$ going LOW.
6. he procedure continues until (UMAX + 1, VMIN) is reached, at which point the device resets to U (position within row) and increments V (number of row). Thus, the next (U, V) set after (UMAX + 1, VMIN) will be (UMIN, VMIN + 1), followed by (UMIN + 1, VMIN + 1), etc.
7. Upon completion of the walk corresponding to (UMAX + 1, VMAX + 1), the TMC2301 will generate a DONE flag with the final UWRI, and begin a new sequence.

Figure 9. Timing Diagram and Pixel Map Showing Outward Clockwise Spiral Walk Generated by TMC2301 (2 x 2 Kernel Shown)



Notes:

1. Assumes that $\overline{OETA}$ is LOW and $\overline{NOOP}$ is HIGH.
2. Timing Parameters are not shown on this diagram.

On any given clock cycle, the actual (X, Y) and (U, V) outputs of the IRS are given by the following equations:

$$x = X_0 + dX/dU_0 * m + dX/dV_0 * n + d^2X/dUdV * m * n + d^2X/dU^2 * (m^2 - m)/2 + d^2X/dV^2 * (n^2 - n)/2^0 + FOV * CAX(w) + FOV * m * CAX(Ker)$$

$$y = Y_0 + dY/dU_0 * m + dX/dV_0 * n + d^2Y/dUdV * m * n + d^2Y/dU^2 * (m^2 - m)/2 + d^2Y/dV^2 * (n^2 - n)/2^0 + FOV * CAY(w) + FOV * m * CAY(Ker)$$

$$u = UMIN + m$$

$$v = VMIN + n$$

where FOV is the 4-bit field of view parameter, normally set to 1 so that the spiral walk proceeds in single-pixel steps. Setting FOV to 4 would expand the spiral walk, allowing the user to trade two bits of image size for two bits of additional interpixel positioning resolution. CAX(w) and CAY(w) are the current value of the coefficient address outputs, and CAX(KER) and CAY(KER) are the terminal values of each pixel walk. The CA(KER) terms arise because the IRS computes each new walk's starting point from the previous spiral walk's end point, rather than its starting point.

Interpolation Coefficient Lookup Table Addressing

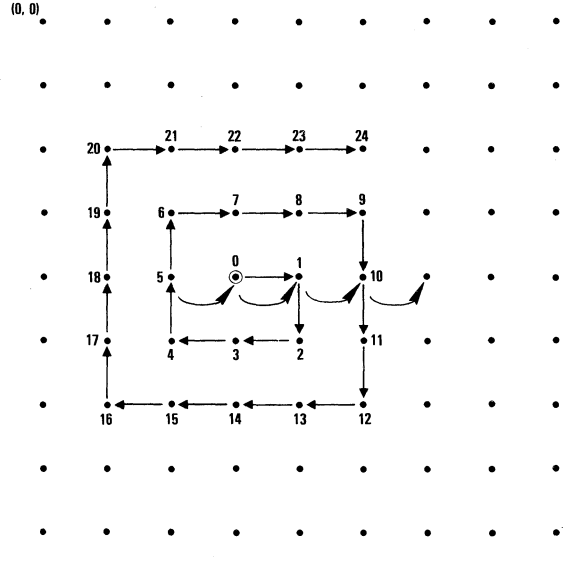
The external coefficient lookup table RAM stores the interpolation values used to calculate the value of the new pixel. These values are selected by the user, allowing maximum filtering flexibility. In simple filtering applications, all 8 bits of coefficient address are available to access up to 256 interpolation coefficients, for kernels of 16 x 16 pixels. This address is generated by the internal walk counter of the TMC2301. In most applications, the same Kernel parameter value is selected in both IRS devices; thus, the Coefficent Address outputs CA_{7-0} for the X and Y devices are identical, and the user needs only one of the 8-bit buses for memory access.

Applications executing a coordinate transformation, however, will almost always generate non-integer source pixel addresses; that is, the U (or V) locations will not map to the X (or Y) addresses exactly, and fractional address components are generated. The user then must account for this spatial offset in both dimensions by storing the appropriate corrected interpolation kernel values in the lookup table. The 8-bit address bus is broken up into two parts: the fractional portion (upper 4 bits), and the walk counter (lower 4 bits). Thus, in resampling applications, the maximum kernel size is 4 x 4 pixels, or 16 locations. As in the filtering example, assuming that the user has selected the same kernel size for both IRS devices, the 4 bits of least-significant address generated by both devices will be identical, and redundant. The four most significant address bits, however, will reflect the current fractional offsets of the resampled pixel from the nearest X (Y) location, to a spatial resolution of 4 bits, in the X (or Y) directions. Utilization of the 12 bits (total) of lookup table address is left to the user, to be arranged as desired for memory access. See Figure 3.

Application Examples

One of the more common applications for the TMC2301 is simple static filtering. In this case the source and target memories locations are identical and no coordinate transformation is performed. The (X, Y) and (U, V) outputs listed in Table 4 show the address sequencing generated by the TMC2301 to execute the walk of a 5 x 5 pixel interpolation kernel. The normalized coefficients shown implement a first-order Butterworth Low Pass Filter with cutoff radius of $1/\sqrt{2}$. Note that the (U, V) output address is updated following the completion of the walk for that location.

Figure 10. Pixel Map Showing Walk Sequence for 5 x 5 Static Filter



Multimedia

Table 4. IRS Outputs for Static Filter Illustrated in Figure 10

Cycle	X	Y	Index (CA)	Coefficient	U	V
1	3	4	0	0.2176	2	4
2	4	4	1	0.0725	2	4
3	4	5	2	0.0435	2	4
4	3	5	3	0.0725	2	4
5	2	5	4	0.0435	2	4
6	2	4	5	0.0725	2	4
7	2	3	6	0.0435	2	4
8	3	3	7	0.0725	2	4
9	4	3	8	0.0435	2	4
10	5	3	9	0.0198	2	4
11	5	4	10	0.0272	2	4
12	5	5	11	0.0198	2	4
13	5	6	12	0.0128	2	4
14	4	6	13	0.0198	2	4
15	3	6	14	0.0272	2	4
16	2	6	15	0.0198	2	4
17	1	6	16	0.0128	2	4
18	1	5	17	0.0198	2	4
19	1	4	18	0.0272	2	4
20	1	3	19	0.0198	2	4
21	1	2	20	0.0128	2	4
22	2	2	21	0.0198	2	4
23	3	2	22	0.0272	2	4
24	4	2	23	0.0198	2	4
25	5	2	24	0.0128	2	4
26	4	4	0	0.2175	3	4

Figure 11 illustrates the sequence for a bilinear resampling of a 63° rotation. The starting point is translated +1 in the Y-direction. A common rotation matrix might be:

$dX/dU_0 = \cos(a) = .6$ $\quad dY/dU_0 = \sin(a) = .8$

$dX/dV_0 = -\sin(a) = -.8$ $\quad dY/dV_0 = \cos(a) = .6$

However, we have included a linear compression factor of 5:1, and must accommodate the fact that each time u is incremented, the start of the new walk is referenced to the END of the previous walk. Given these corrections, the rotation matrix becomes:

$dX/dU_0 = 5\cos(a) = 3$ $\quad dY/dU_0 = 5\sin(a) - FOV = 3$

$dX/dV_0 = -5\sin(a) = -4$ $\quad dY/dV_0 = 5\cos(a) = 3$

Kernel = 1

Figure 11. Pixel Map Showing Parameters for 63° Rotation and 5:1 Compression Listed in Table 5

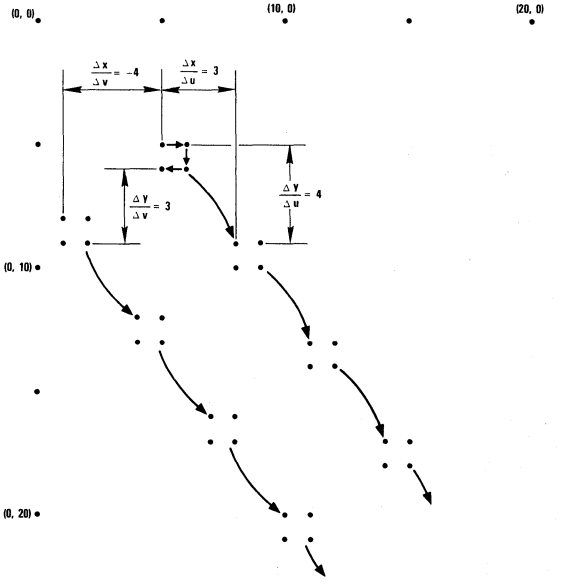
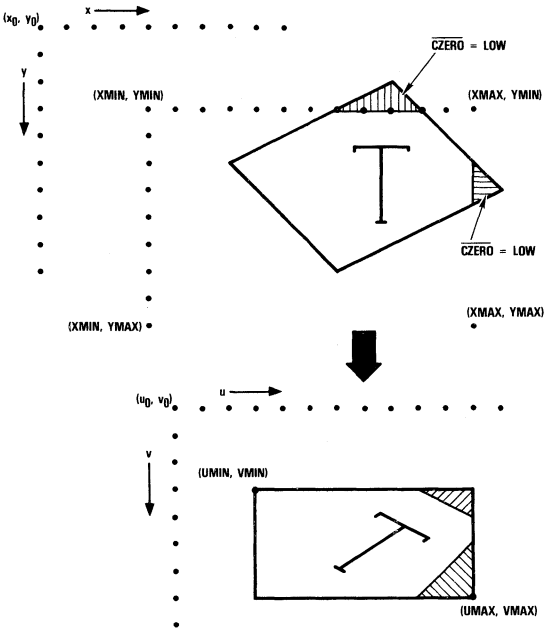


Table 5. IRS Outputs for Operation Illustrated in Figure 11

Cycle	X	Y	Index	U	V
1	5	5	0	4	5
2	6	5	1	4	5
3	6	6	2	4	5
4	5	6	3	4	5
5	8	9	0	5	5
6	9	9	1	5	5
7	9	10	2	5	5
8	8	10	3	5	5
9	11	13	0	6	5
10	12	13	1	6	5
11	12	14	2	6	5
12	11	14	3	6	5
13	14	17	0	7	5
14	15	17	1	7	5
15	15	18	2	7	5
16	14	18	3	7	5
17	1	8	0	8	5
18	2	8	1	8	5
19	2	9	2	8	5
20	1	9	3	8	5
21	4	12	0	5	6
22	5	12	1	5	6
23	5	13	2	5	6
24	4	13	3	5	6
25	7	16	0	6	6
26	8	16	1	6	6
27	8	17	2	6	6
28	7	17	3	6	6
29	10	20	0	7	6
30	11	20	1	7	6
31	11	21	2	7	6
32	10	21	3	7	6
33	0	15	0	8	6

Figure 12 may help clarify the relationships among (X_0, Y_0), (XMIN, YMIN), (XMAX, YMAX), (UMIN, VMIN), and (UMAX, VMAX). With positive first derivatives, (X_0, Y_0) and (UMIN, VMIN) represent the upper left corners of the original image and the new destination field, respectively. The lower right corner of the transformed image is located at (UMAX + 1, VMAX + 1); the location of the corresponding corner of the original image depends on the values of the derivatives. Not to be confused with (X_0, Y_0), the points (XMIN, YMIN) and (XMAX, YMAX) define the "usable" rectangular portion of the original image; points (X, Y) lying outside this region are ignored in most resampling and filtering applications. This feature permits one to construct a mosaic of several abutting subimages in the (x, y) plane, without danger of edge effect interference between adjacent subimages. Note in the figure that the upper left and lower left corners of the original image lie outside the admissible region; in practice, the values fetched at these locations will not be included in the convolutional sums.

Figure 12. Pixel Maps Demonstrating Source and Destination Image Boundaries and Image Clipping (Note Shaded Area)



Note: Assume 000h < X < FFFh
000h < Y < FFFh

Multimedia

Application Note

Nearest Neighbor Operation — Additional Timing Details

Example A, PIPE = 0

Inspecting Figure 201:
PIPE = 0, KER = 0 (near neighbor), AUTOIN = 1 (on),
UMN = 0, UMX = 5, VMN = 0, VMX = 5,
DX/DU = 1, DY/DV = 1, XO = 0
First rising edge of CLK after INIT falling edge is #0.
Rable entries are events after listed clock rising edge.
END, DONE flags = 0, except where shown as 1.
UWRI goes low and remains low with CLK #2.

CLK	X	U	V	END		DON	Comments
				R	C		
0				0	0		first clock after INIT falling edge
1				0	0		
2	0			0	0		first valid X addresses = XO
3	1	0	0	0	0		second X; first valid U, V = UMN, VMN
4	2	1	0	0	0		
5	3	2	0	1	0		END ROW flag 3 cycles before last X
6	4	3	0	0	0		
7	5	4	0	0	0		
8	6	5	0	0	0		last X of first row
9	0	6	0	0	0		last U, V or first row; first X of 2nd row
10	1	0	1	0	0		First U, V of second row
11	2	1	1	0	0		
12	3	2	1	1	0		END ROW flag 4 cycles before last U, V
13	4	3	1	0	0		
14	5	4	1	0	0		
15	6	5	1	0	0		last X of second row
16	0	6	1	0	0		last U, V of second row U = UMX + 1
35	5	4	4	0	1		END COL goes high before last X
36	6	5	4	0	1		last X of V = VMX - 1row
37	0	6	4	0	1		first X of Last (V = VMX) row
38	1	0	5	0	1		first U, V = UMN, VMX of last row
39	2	1	5	0	1		
40	3	2	5	1	1		last END ROW flag of frame
41	4	3	5	0	1		END COL goes low when DONE goes high
42	5	4	5	0	0	1	DONE immediately before last X
43	6	5	5	0	0		last X of frame
44	0	6	5	0	0		last U, V = UMX + 1, VMX
45	1	0	0	0	0		first U, V = UMN, VMN of new frame
46	2	1	0	0	0		
47	3	2	0	1	0		first END ROW flag of new frame

Example B. PIPE = 1

Now, referring to Figure 202:
PIPE = 1, KER - 0 (near neighbor), AUTOIN = 1 (on),
UMN = 0, UMX = 5, VMN = 0, VMX = 5,
DX/DU = 1, DY/DV - 1, XO = 0
First rising edge of CLK after INIT falling edge is #0.
Table entries are events after listed clock rising edges.
END, DONE, flags = 0, except where shown as 1.
UWRI goes low with CLK #3, stays low. Otherwise, the timing is the same as Figure 201, i.e., pipeline delays UWRI and ACC by one clock cycle.

Bilinear Interpolation

Example C. PIPE = 0

From Figure 203, we can see the following:
PIPE = 0, KER - 1 (bilinear), AUTOIN = 1 (on),
UMN = 0, UMX = 5, VMN = 0, VMX = 5,
DX/DU = 1, DY/DV = 1, YO = 0, XO = 0
First rising edge of CLK after INIT falling edge is #0.
Table entries are events after listed clock rising edges.
END, DONE flags = 0, except where shown as 1.

CLK	X	U	V	END ROW	UWR	ACC	DON	Comments
0					1	0		1st CLK after INIT falling edge
1					0	0		
2	0				1	0		1st valid X address = XO: start 1st ACCum
3	1				0	1		
4	1				1	1		
5	0				1	1		end 1st 2x2 kernel; end 1st ACCum
6	1	0	0		1	0		1st valid u, v = UMN, VMN; 2nd ACCum start
7	2	0	0		0	1		
8	2	0	0		1	1		
9	1	0	0		1	1		
10	2	1	0		1	0		2nd valid u, v = UMN + 1, VMN
11	3	1	0		0	1		
12	3	1	0		1	1		
13	2	1	0		1	1		
14	3	2	0		1	0		3rd valid u, v = UMN + 2, VMN
15	4	2	0		0	1		
16	4	2	0		1	1		
17	3	2	0		1	1		end 4th 2x2 kernel
160	5	3	5	1	1	1		
161	4	3	5	1	1	1		
162	5	4	5	1	1	0		begin next-to-last x-walk
163	6	5	4	1	0	1		

CLK	X	U	V	END ROW	UWR	ACC	DON	Comments
164	6	5	4		1	1		
165	5	4	5		1	1		
166	6	5	5		1	0		begin last x-walk
167	7	5	5		0	1		
168	7	5	5		1	1	1	
169	6	5	5		1	1		last x of frame
170	0	6	5		1	0		
171	1	6	5		0	1		
172	1	6	5		1	1		
173	0	6	5		1	1		last u, v = UMX + 1, VMX
174	1	0	0		1	0		first u, v of new frame
175	2	0	0		0	1		
176	2	0	0		1	1		
177	1	0	0		1	1		

Performing Larger Interpolation Kernels

With PIPE = 0, AUTOINIT = 1, and the following definitions:

T_{xdone} = Clock cycle of final X address of a transform.
T_{xend} = Clock cycle of final X address along a row.
KER = (K + 1)(K + 1), where K is the value in the "kernel size" parameter register.

The following relationships hold true:

First X address - valid 3 rising clock edges after INIT's failing edge.

END FLAG - goes HIGH for KER cycles at clock cycle T_{xend} -1-2*KER. Otherwise stated, END is active for one walkaround starting two walkarounds and one cycle prior to the final source address of a row.

DONE FLAG -goes HIGH for one cycle at clock cycle T_{xdone} -1. Otherwise stated, DONE is active for one clock cycle one cycle prior to the last source address of the final walkaround.

Examples:

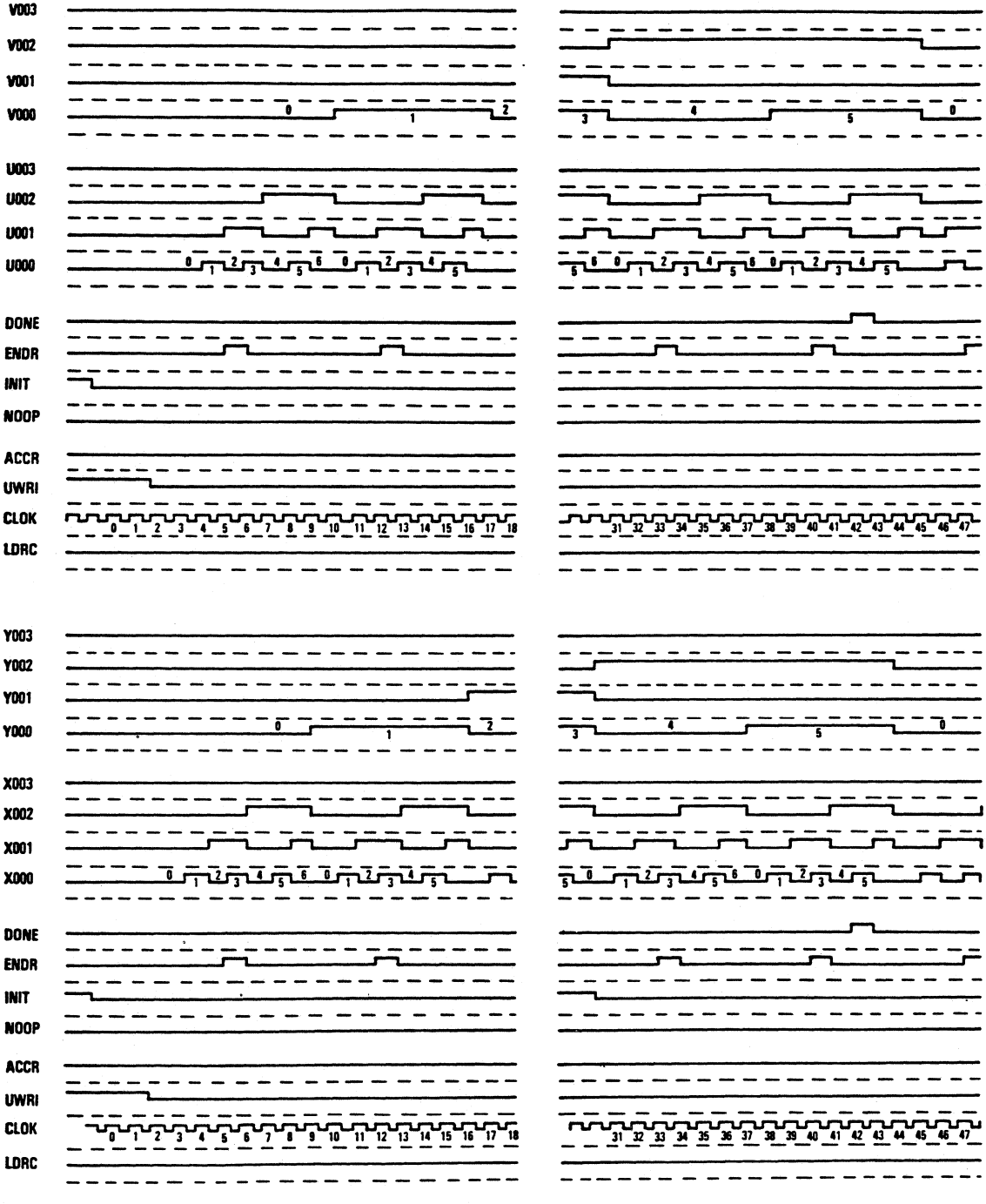
D. KER = 0 (nearest neighbor), UMIN = 0, UMAX = 3, UMIN = 0, VMAX = 2

If first CLOCK edge after INIT goes low is 0, then:
First x, y out (= XO, YO) appears after CLOCK edge 2.
First u, v out (= 0, 0) appears after CLOCK edge 3.
END is high after CLOCK edge 13 only.
DONE is high after CLOCK edge 16.
Last x out appears after CLOCK edge 16.
Last u, v out (= 4, 2) appears after CLOCK edge 17.

E. KER = 1, (1 pass bilinear), UMIN = 0, UMAX = 4, VMIN = 1, VMAX = 3

If first CLOCK edge after INIT goes low is 0, then:
First x, y out (= XO, YO) appears after CLOCK edge 2.
First u, v out (= 0, 1) appears after CLOCK edge 6 and remains through edges 7, 8 and 9.
END is high after CLOCK edge 92, goes low after 96.
DONE is high after CLOCK edge 100 only.
Last x out appears CLOCK edge 101.
Last u, v out (= 5, 3) appears after CLOCK edge 102 and remains through edges 103, 104 and 105.

Figure 20

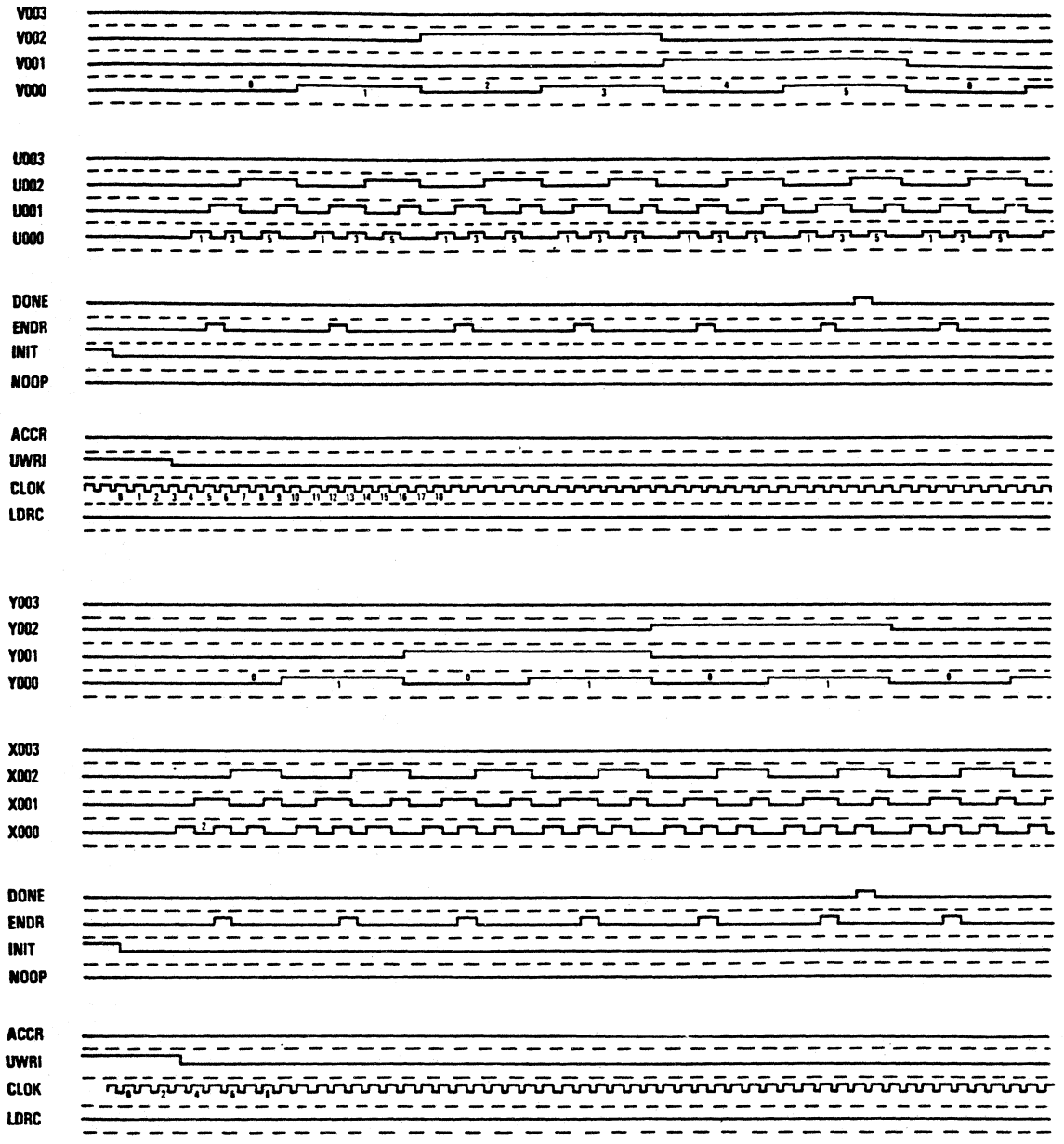


KER = 0
PIPE = 0

UMIN = 0
UMAX = 5

VMIN = 0
VMAX = 5

Figure 202

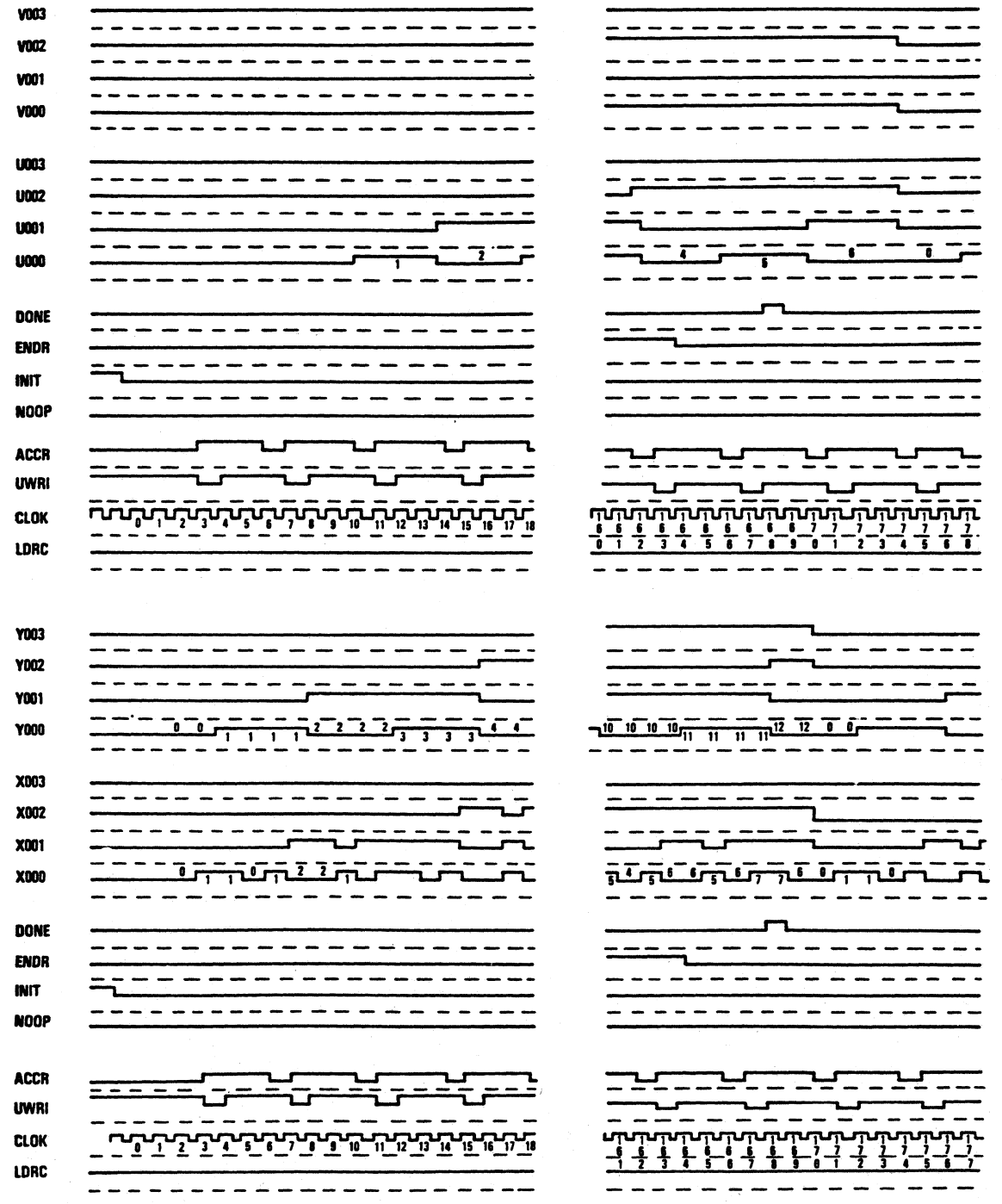


KER = 0
PIPE = 1

UMIN = 0
UMAX = 5

VMIN = 0
VMAX = 5

Figure 203



KER = 1
PIPE = 0

UMIN = 0
UMAX = 5

VMIN = 0
VMAX = 5

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2301G8C2	STD–T_A=0°C to 70°C	Commercial	68 Pin Grid Array	2301G8C2
TMC2301G8V	EXT–T_C=–55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2301G8V
TMC2301G8V1	EXT–T_C=–55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2301G8V1
TMC2301H8C	STD–T_A=0°C to 70°C	Commercial	68 Pin Grid Array	2301H8C
TMC2301H8C1	STD–T_A=0°C to 70°C	Commercial	68 Pin Grid Array	2301H8C1
TMC2301L1V	EXT–T_C=–55°C to 125°C	MIL-STD-883	68 Leaded Hermetic Ceramic Chip Carrier	2301L1V
TMC2301L1V1	EXT–T_C=–55°C to 125°C	MIL-STD-883	68 Leaded Hermetic Ceramic Chip Carrier	2301L1V1
TMC2301R1C	STD–T_A=0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C
TMC2301R1C1	STD–T_A=0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C1
TMC2301R1C2	STD–T_A=0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C2

40G05061 Rev G 8/93

TMC2302
Image Manipulation Sequencer
40 MHz

Description

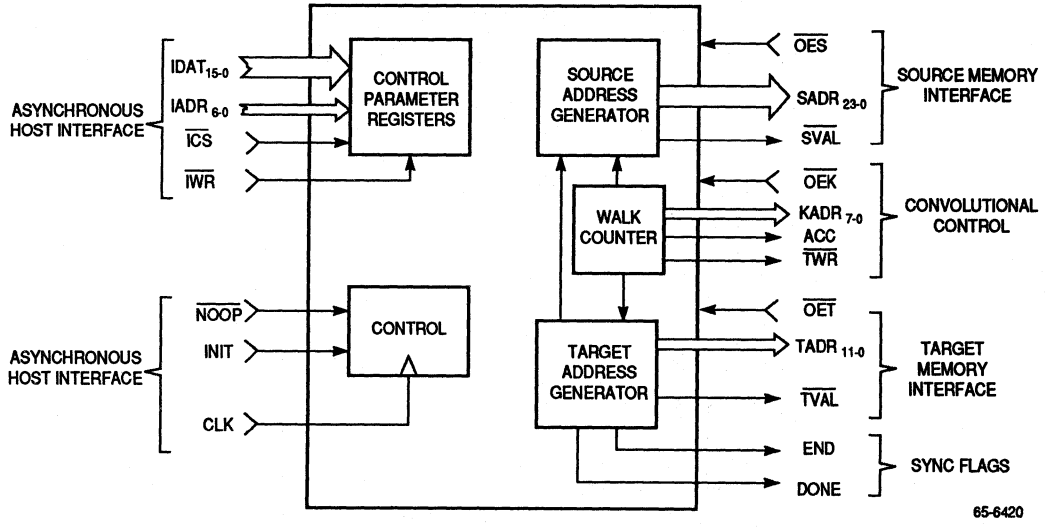
The TMC2302 is a high-speed self-sequencing VLSI circuit address generator which supports image resampling, rotation, rescaling, warping, and filtering. It generates input bit plane, interpolation coefficient lookup table, and output bit plane memory addresses along with pixel interpolator control signals.

Similar in architecture to the TMC2301 Image Resampling Sequencer, the TMC2302 features numerous enhancements. In addition to an increase in the maximum clock rate to 40 MHz, the device offers three-dimensional address generation and implements two-dimensional image transformation polynomials of up to third order.

The TMC2302 can process image data fields with up to 24 bits of binary resolution (224 pixels) per dimension, with 0 to 16-bit subpixel resolution.

A system based on two TMC2302s can nearest-neighbor resample a two-dimensional 512 x 512 pixel image in 6.5 milliseconds, translating, rotating, or warping it, depending on the user-selected transformation parameters. A complete bilinear interpolation of the sample image can be completed in 26 milliseconds, while a nearest-neighbor resampling of a 3D image 128 pixels on a side takes only 53 milliseconds with three TMC2302s. Image resampling speed is independent of angle of rotation, degree of warp, or amount of zoom specified.

Simplified Block Diagram



TMC2302

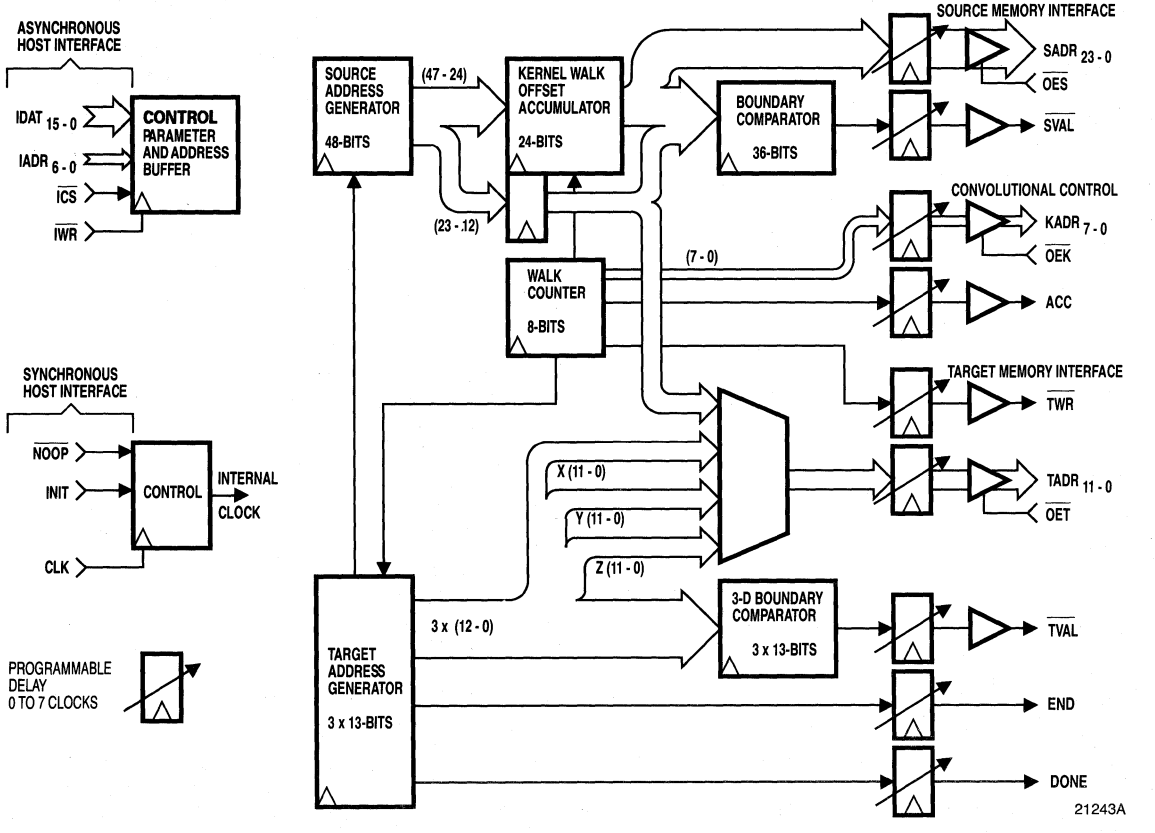
Features

- Asynchronous Loading Of Control Parameters
- Rapid (25ns Per Pixel) Rotation, Warping, Panning, And Scaling Of Images
- Three-Dimensional Image Addressing Capability
- General Third-Order Polynomial Transformations In Two Dimensions Implemented On-Chip; Three-Dimensional Transformation Of Up To Order 1.5 Also Supported
- Flexible, User-Configurable Pixel Datapath Timing Structure
- Static Convolutional Filtering Of Up To 16 x 16 Pixel (One-Pass), 256 x 256 Pixel (Two-Pass) Or 256 x 256 x 256 Pixel (Three-Pass) Windows
- User-Selectable Source Image Subpixel Resolution of 2^{-8} to 2^{-16}
- 24-Bit (Optional 36-Bit) Positioning Precision Within The Source Image Space, 48-Bit Internal Precision
- Low Power CMOS Process
- Available In A 120 Pin Plastic Pin Grid Array

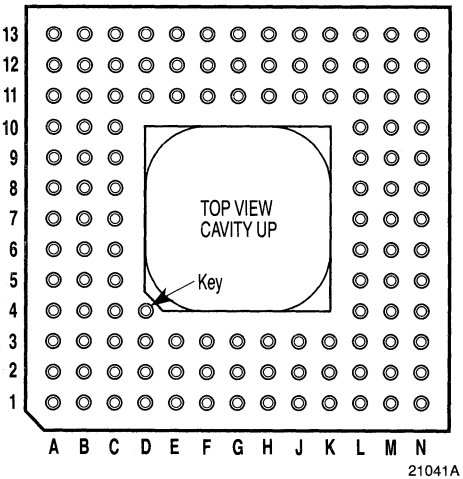
Applications

- High-Performance Video Special-Effects Generators
- Guidance Systems
- Image Recognition, Robotics
- High-Precision Image Registration (LANDSAT Processing)

Functional Block Diagram



Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	V_{DD}	G3	V_{DD}	L3	NC	L7	V_{DD}	L11	V_{DD}	G11	GND	C11	GND	C7	$IADR_5$
B2	$SADR_{15}$	G1	$SADR_6$	M2	$\overline{OEK}$	N7	$TADR_1$	M12	GND	G13	$IDAT_0$	B12	$IDAT_8$	A7	$IADR_6$
B1	$SADR_{14}$	H1	$SADR_5$	N2	$KADR_7$	N8	$TADR_2$	M13	$\overline{TVAL}$	F13	$IDAT_1$	A12	$IDAT_9$	A6	$\overline{OES}$
D3	GND	H2	$SADR_4$	L4	V_{DD}	M8	$TADR_3$	K11	V_{DD}	F12	GND	C10	$IDAT_{10}$	B6	$SADR_{23}$
C2	V_{DD}	H3	GND	M3	$KADR_6$	L8	$TADR_4$	L12	GND	F11	V_{DD}	B11	$IDAT_{11}$	C6	$SADR_{22}$
C1	$SADR_{13}$	J1	$SADR_3$	N3	$KADR_5$	N9	$TADR_5$	L13	$\overline{NOOP}$	E13	$IDAT_2$	A11	$IDAT_{12}$	A5	$SADR_{21}$
D2	$SADR_{12}$	J2	$SADR_2$	M4	$KADR_4$	M9	$TADR_6$	K12	INIT	E12	$IDAT_3$	B10	$IDAT_{13}$	B5	$SADR_{20}$
E3	GND	K1	$SADR_1$	L5	GND	N10	$TADR_7$	J11	V_{DD}	D13	$IDAT_4$	C9	$IDAT_{14}$	A4	V_{DD}
D1	$SADR_{11}$	J3	V_{DD}	N4	$KADR_3$	L9	$TADR_8$	K13	GND	E11	GND	A10	$IDAT_{15}$	C5	$SADR_{19}$
E2	$SADR_{10}$	K2	$SADR_0$	M5	$KADR_2$	M10	$TADR_9$	J12	CLK	D12	$IDAT_5$	B9	$\overline{ICS}$	B4	$SADR_{18}$
E1	$SADR_9$	L1	$\overline{SVAL}$	N5	$KADR_1$	N11	$TADR_{10}$	J13	$\overline{IWR}$	C13	$IDAT_6$	A9	$IADR_0$	A3	$SADR_{17}$
F3	V_{DD}	M1	ACC	L6	$KADR_0$	N12	$TADR_{11}$	H11	GND	B13	$IDAT_7$	C8	$IADR_1$	A2	$SADR_{16}$
F2	$SADR_8$	K3	GND	M6	$\overline{OET}$	L10	DONE	H12	V_{DD}	D11	V_{DD}	B8	$IADR_2$	C4	GND
F1	$SADR_7$	L2	V_{DD}	N6	$\overline{TWR}$	M11	GND	H13	SYNC	C12	GND	A8	$IADR_3$	B3	V_{DD}
G2	GND	N1	GND	M7	$TADR_0$	N13	ENDD	G12	V_{DD}	A13	V_{DD}	B7	$IADR_4$	A1	GND

Functional Description

General Information

The TMC2302 is a versatile, high-performance address generator which can control, under user direction, filtering or remapping of two or three-dimensional images by resampling them from one set of Cartesian coordinates (x, y, z) into a new, transformed set (u, v, w). Most applications utilize two identical devices for two-dimensional, or three devices for three-dimensional, image processing. The host CPU initializes the system by loading the input image buffer RAM with the source image pixel data and the TMC2302s with the image transformation and system configuration control parameters. These parameters are loaded by a separate, asynchronous input clock. The IMS-based system then executes the entire transformation as programmed, generating a DONE flag upon completion of the transform. The user can program the chip to repeat the transform continuously or to halt at the end.

General Information (cont.)

The IMSs continuously compute the target bit plane (u, v) or bit space addresses (u, v, w) in typical line-by-line, raster-scan serial sequence. For each output pixel address, they compute the corresponding remapped source image coordinates, each of whose upper 24 bits become the source bit plane addresses (x, y). An additional lower twelve bits are available through the target address port in the optional extended address mode. Source image addresses may be generated at up to 40MHz, with the corresponding target image addresses then appearing at up to (40/k)MHz, where "k" is the size of the interpolation kernel implemented. In the two-device system, one TMC2302 computes the horizontal coordinates x and u while the other generates the y and v (vertical) addresses. In a three-dimensional system, one additional device would provide the z and w (depth or time) coordinates.

To support a wide range of image transformations, the "row" or x/u device implements a 16-term polynomial of the form:

$$x = a + bu + cu^2 + du^3 + ev + fvu + gvu^2 + hvu^3 + iv^2 + jv^2u + kv^2u^2 + lv^2u^3 + mv^3 + nv^3u + ov^3u^2 + pv^3u^3$$

where a through p are the user-defined image transformation parameters. The TMC2302 steps sequentially through the pixels within a user-defined rectangle in the target image space, computing the "old" source image address (x, y, z) corresponding to each "new" target image pixel (u, v, w). User-programmable flags are available to indicate when the source and target image addresses have fallen outside of a defined rectangular area, simplifying the generation of complex images or image windows.

In the three-dimensional mode, the x/u transformation equation is:

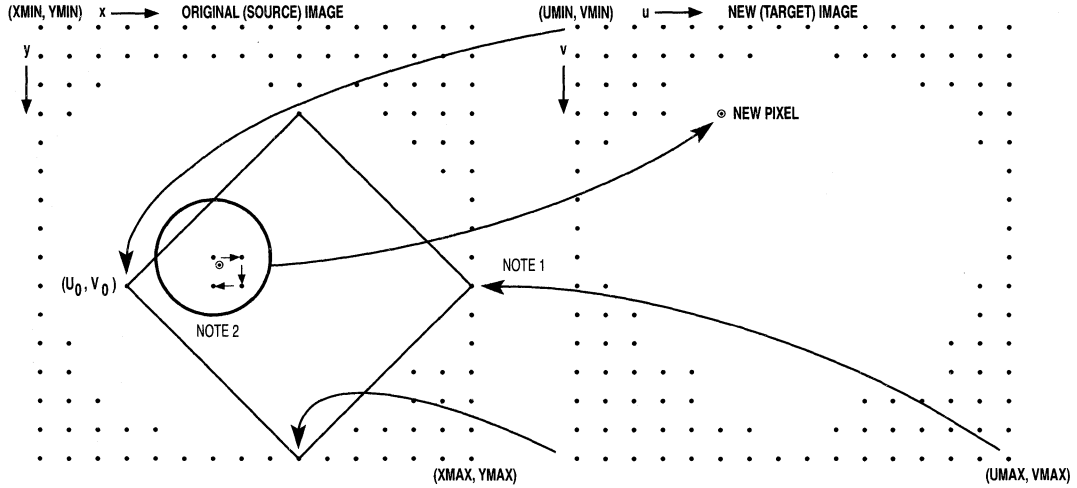
$$x = a + bu + ev + kw + fuv + ivw + luw + juvw$$

See "The Image Transformation Polynomial" section of the *Applications Discussion* .

The TMC2302 utilizes an external multiplier-accumulator or interpolator, connected to the system clock, to calculate the interpolated pixel value for each color. The products of the original source image pixel values surrounding the remapped pixel location (interpolation kernel) and the appropriate weights stored in the coefficient lookup table are summed. The resulting new interpolated image pixel value is then stored in the corresponding (U, V, W) memory location in the target image memory buffer. Next, the target image address is incremented by one in the "u" direction until UMAX is reached (end of line), when U is reset to UMIN, and the V counter is incremented to give the first pixel location in the next line. The process is repeated, proceeding line-by-line through the image, until VMAX is reached. In the case of three-dimensional images, the IMS system also steps through each page in the image, incrementing in the "w" direction with the completion of each image plane until WMAX is reached, and the transformation is complete.

The Image Manipulation Sequencer can support any nearest-neighbor, bilinear interpolation, or cubic convolution resampling, according to the user's requirements. Interpolation kernels of more than one pixel require an external interpolation coefficient lookup table and multiplier-accumulator. One, two, and three-pass algorithms are supported. For each output point in a typical two-dimensional single-pass static image filter, the TMC2302 implements a spiralling pixel resampling algorithm, "walking" around the resampling neighborhood in two dimensions and generating the appropriate coefficient table addresses to sum up the interpolated pixel value in the external pixel interpolator. At the end of each walk, the TMC2302 will advance one pixel along the output scan line and then execute the walk for that next pixel. When performing multiple-pass interpolation, the TMC2302 system proceeds along only one dimension per pass, which requires dimensionally separable, preferably orthogonal, coefficients.

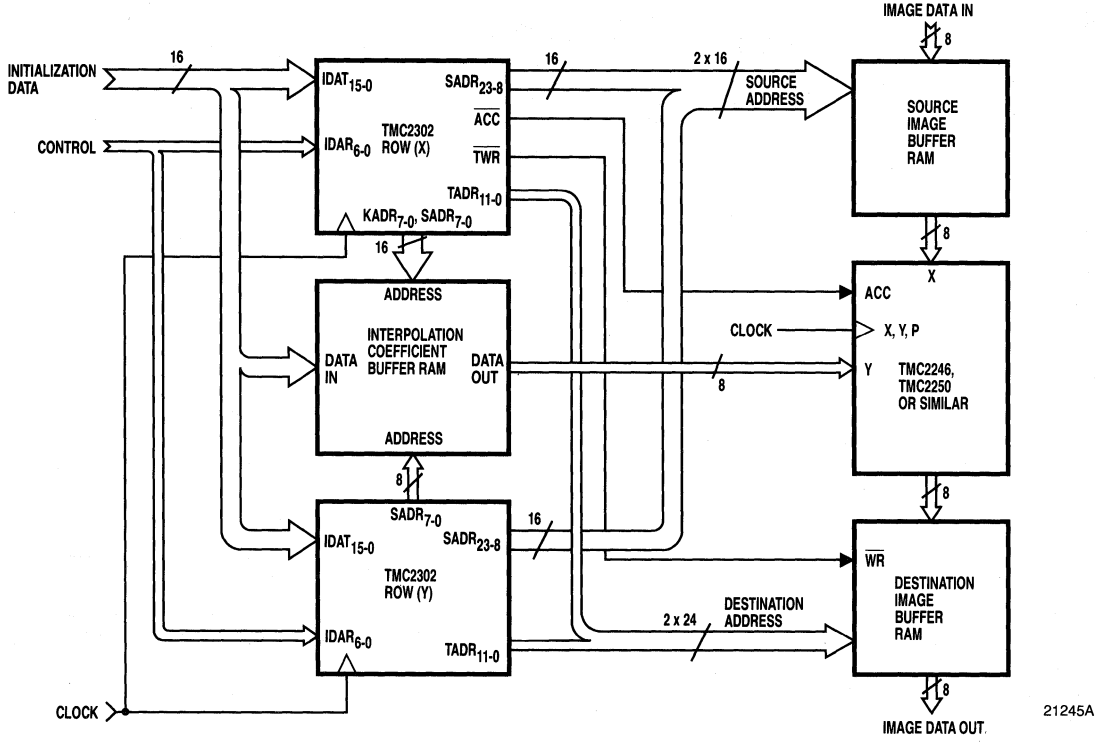
Figure 1. Image Resampling Geometry Showing Two-Dimensional Image Rotation and Expansion



NOTES: 1. Coordinate transformation U, V pixel mapped into X, Y coordinates. 2. Bilinear pixel interpolation walk. New U, V pixel intensity calculated from surrounding X, Y pixel neighborhood. 21244A

A basic, two-dimensional TMC2302-based system is shown in *Figure 2*. In this typical arrangement, two Image Manipulation Sequencers process the image. The only other components needed beyond the source and target image buffer memories are a multiplier-accumulator or pixel interpolator such as the TRW TMC2246 Image Mixer or TMC2250 Matrix Multiplier, and the Interpolation Coefficient Lookup Table RAM or ROM.

Figure 2. Basic Two-Dimensional Image Convolver Using TMC2302 IMS with Typical 8-Bit Data Path



Signal Definitions

Power

VDD, GND — The TMC2302 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The pixel clock of the TMC2302 strobes all internal registers except the control parameter preload registers. All timing specifications except those are referenced to the rising edge of CLK.

$\overline{IWR}$ — The internal image transformation and configuration control parameter registers are double buffered to simplify interfacing with system controllers. Depending on the state of the chip selects $\overline{ICS}$, control words input to $IDAT_{15-0}$ and the corresponding addresses presented to $IADR_{6-0}$ are strobed into the outer preload registers on the rising edge of the Input parameter Write clock $\overline{IWR}$. The last parameter must be loaded twice on two consecutive rising edges of IWR \.

Inputs

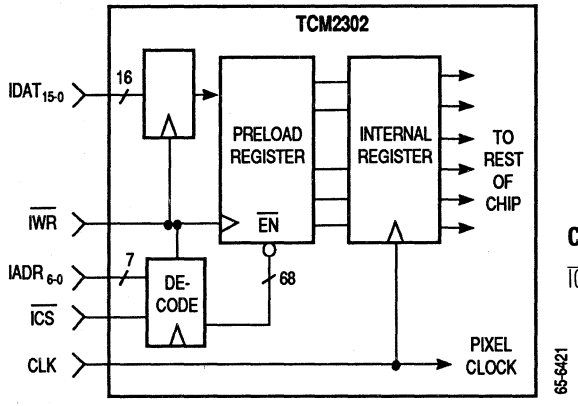
IADR6-0 — The input parameter preload register currently indicated by the Input parameter register Address $IADR_{6-0}$ is loaded with the data presented to input port IDAT on the rising edge of $\overline{IWR}$, as demonstrated in Figure 3.

IDAT15-0 — Configuration and transformation parameter Input Data is presented, along with the appropriate input register address word $IADR_{6-0}$, to the parameter Input Data port.

Inputs (cont.)

$IDAT_{15-0}$ (cont.) $IDAT_{15-0}$ and is latched into the preload registers on the next rising edge of $\overline{IWR}$. Preload register updates are disabled by the chip select control $\overline{ICS}$. See *Figure 3*.

Figure 3. Image Transformation and Configuration Control Parameters Register Structure



Outputs

$SADR_{23-0}$ The 24-bit address of one dimension (X, Y, Z) of the source image pixel value currently being resampled is output through the Source Address port $SADR_{23-0}$. This port can be forced to the high-impedance state by the enable control $\overline{OES}$.

$KADR_{7-0}$ The integer address steps for each dimension of the spiral interpolation walk performed by the TMC2302, as determined by the transform parameter KERNEL, are generated by the internal walk counter and output at the Coefficient Address output port $KADR_{7-0}$. This port can be forced to the high-impedance state by the enable control $\overline{OEK}$.

$TADR_{11-0}$ The 12-bit address of one dimension (U, V, W) of the target image pixel value just resampled is output through the Target Address Port $TADR_{11-0}$. This port is forced into the high-impedance state by the enable control $\overline{OET}$. $TADR_{11-0}$ can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by utilization of the pipeline delay parameter PIPTAD. For systems requiring greater spatial resolution in the source image than that offered by the $SADR_{23-0}$ alone, the Target Address Port can be reconfigured to output 12 additional LSBs of the source address by placing the device into the Extended mode, in which case the pipeline delay parameter must be set to 0 to maintain alignment with the current source address port output. See the *Device Configuration and Control Parameters* section.

Controls

$\overline{ICS}$ The input parameter preload register write clock $\overline{IWR}$, and thus the preloading of all configuration and transformation parameters, is disabled on the next clock when the registered Input parameter Chip Select input is HIGH. When $\overline{ICS}$ returns LOW, they are enabled on the next clock. See *Figure 3*.

INIT The TMC2302 control logic is cleared and initialized for the start of a new image transformation, and the internal working registers are updated with the contents of the current control parameter preload registers when the registered control input INIT is HIGH. The image transformation then commences with the first source image pixel address nine clocks later.

SYNC The user can select between continuous or one-frame operation with the registered input control SYNC. Assuming that INIT remains LOW and $\overline{NOOP}$ remains HIGH, if SYNC remains HIGH at the end of a transform the TMC2302 will begin the next image transformation without interruption. This assumes either that the user is not changing the parameter set, or that a new set of parameters has already been loaded into the preload registers midframe, prior to the beginning of the last line in the transform.

Controls (cont.)

SYNC (cont.) If SYNC is LOW during the last clock cycle of a transform, the device will complete the image, having loaded the new transform parameter set during the first clock of the final line of the transform, and halt in the state set on the first clock cycle of the next transform. These outputs are held until SYNC is again brought HIGH, and operation resumes on the next clock. See *Figure 5*.

ACC The external pixel interpolator or multiplier-accumlator is initialized for a new accumulation of products by the registered Accumulator Control output ACC. On the first cycle of each interpolation walk, this output goes LOW for one cycle, effectively clearing the register by loading in only the first new resampled pixel value. When performing nearest-neighbor resampling, this control will remain LOW throughout the entire transform. This output can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPACC. See the *Device Configuration and Control Parameters* section.

$\overline{TWR}$ On the last cycle of each interpolation walk, the Target Write Enable goes LOW for one clock cycle, returning HIGH for all but the last cycle of the next walk. When performing nearest-neighbor resampling, this control will remain LOW throughout the entire transform. This output can be forced to the high-impedance state by the enable control $\overline{OET}$, and can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPTWR. See the *Device Configuration and Control Parameters* section.

$\overline{NOOP}$ Assuming that INIT remains LOW, the internal system clock of the TMC2302 will be disabled on the next clock, halting the current transform, when the registered control input $\overline{NOOP}$ goes LOW. When $\overline{NOOP}$ returns HIGH, normal operation resumes on the next clock. This control does not affect the loading of the configuration and transformation parameter preload registers.

$\overline{OES}$ The source address port $SADR_{23-0}$ is enabled when the asynchronous output enable $\overline{OES}$ is LOW. When $\overline{OES}$ is HIGH, the port is in the high-impedance state.

$\overline{OEK}$ The interpolation coefficient address port $KADR_{7-0}$ is enabled when the asynchronous output enable $\overline{OEK}$ is LOW. When $\overline{OEK}$ is HIGH, the port is in the high-impedance state.

$\overline{OET}$ The target address port $TADR_{11-0}$ and target write enable $\overline{TWR}$ are enabled when the asynchronous Target Output Enable $\overline{OET}$ is LOW. When $\overline{OET}$ is HIGH, these outputs are in the high-impedance state. This control functions in both the normal and extended addressing modes.

Flags

$\overline{SVAL}$ When the current source image address component output is within the working space defined by the parameters XMIN and XMAX (or YMIN, YMAX for the column (Y/V) device or ZMIN, ZMAX for the page (Z/W) device), the Source Address Valid flag $\overline{SVAL}$ for that device is LOW. This flag will go HIGH on the clock in which the corresponding component address falls outside the defined region. In a typical system, the $\overline{SVAL}$ outputs of all IMS devices are OR'ed together to generate a global boundary violation flag. The user might then insert zeroes into the pixel interpolator to ignore that portion of the image outside the defined space, or insert a background color or image. This output can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPSVA. See the *Device Configuration and Control Parameters* section.

Flags (cont.)

$\overline{\text{TVAL}}$ When the current target image addresses are within the working space defined by the parameters UMINI and UMAXI, and VMINI and VMAXI (and WMINI and WMAXI for systems processing three-dimensional images), the Target Address Valid flag $\overline{\text{TVAL}}$ for that device is LOW. This flag will go HIGH on the clock in which the current target address outputs fall outside the defined region. Since each TMC2302 device is programmed with distinct MINI/MAXI parameters and generates a separate $\overline{\text{TVAL}}$ flag, the user may define separate two or three-dimensional target space windows for each device. $\overline{\text{TVAL}}$ can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPTVA. See the ***Device Configuration and Control Parameters*** section.

ENDD During the last pixel interpolation walk of a row (X/U device), the last row in a page (Y/V device), or the last page in a three-dimensional transform (Z/W device), the flag ENDD goes HIGH for the entire walk, indicating End of the transform in that dimension. It remains LOW otherwise. This output can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPEND. See the ***Device Configuration and Control Parameters*** section.

DONE On the last clock cycle of the current image transform, the DONE flags on all TMC2302s go HIGH for one clock cycle. On the next clock cycle, all devices output the first addresses and control signals for the next image transform. If SYNC is LOW, the IMS system halts. If SYNC is HIGH, operation continues without interruption. See "SYNC," in the ***Controls*** section. This flag can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPDON. Also see "PFLS," in the ***Device Configuration and Control Parameters*** section.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins
Power	V_{DD}	Supply Voltage	C3, C2, F3, G3, J3, L2, L4, L7, L11, K11, J11, H12, G12, F11, D11, A13, A4, B3
	GND	Ground	D3, E3, G2, H3, K3, N1, L5, M11, M12, L12, K13, H11, G11, F12, E11, C12, C11, C4, A1
Clocks	CLK	System Clock	J12
	$\overline{IWR}$	Input Parameter Write Clock	J13
Inputs	$IDAT_{15-0}$	Input Parameter Data	A10, C9, B10, A11, B11, C10, A12, B12, B13, C13, D12, D13, E12, E13, F13, G13
	$IADR_{6-0}$	Input Parameter Address	A7, C7, B7, A8, B8, C8, A9
Outputs	$SADR_{23-0}$	Source Address	B6, C6, A5, B5, C5, B4, A3, A2, B2, B1, C1, D2, D1, E2, E1, F2, F1, G1, H1, H2, J1, J2, K1, K2
	$KADR_{7-0}$	Coefficient Address	N2, M3, N3, M4, N4, M5, N5, L6
	$TADR_{11-0}$	Target Address	N12, N11, M10, L9, N10, M9, N9, L8, M8, N8, N7, M7
Controls	INIT	Initialize	K12
	SYNC	Run/Halt	H13
	$\overline{ICS}$	Input Parameter Chip Select	B9
	ACC	Accumulate	M1
	$\overline{TWR}$	Target Memory Write Enable	N6
	$\overline{NOOP}$	No Operation	L13
	$\overline{OES}$	Source Address Output Enable	A6
	$\overline{OEK}$	Coefficient Address Output Enable	M2
	$\overline{OET}$	Target Address Output Enable	M6
Flags	$\overline{SVAL}$	Source Address Valid	L1
	$\overline{TVAL}$	Target Address Valid	M13
	ENDD	End of Dimension	N13
	DONE	Done	L10
No Connects	NC	No Connect	L3
		Index Pin	D4

Table 1. Nominal Output Signal Timing

$SADR_{23-0}$ [1]	ACC	$TADR_{11-0}$	$\overline{TWR}$	END	DONE
$X_{I-1,J,0}$	0	$U_{L-1,M}$	1	0	0
$X_{I-1,J,1}$	1	$U_{L-1,M}$	1	0	0
$X_{I-1,J,2}$	1	$U_{L-1,M}$	1	0	0
•					
•					
•					
$X_{I-1,J,K}$	1	$U_{L-1,M}$	0	1	0
$X_{I,J,0}$	0	$U_{L,M}$	1	1	0
$X_{I,J,1}$	1	$U_{L,M}$	1	1	0
$X_{I,J,2}$	1	$U_{L,M}$	1	1	0
•					
•					
•					
$X_{I,J,K}$	1	$U_{L,M}$	0	1	1

Note: 1. $KADR_{7-0}$ timing identical.

The nominal sequence of address and control signals of a two-dimensional, single-pass-programmed TMC2302 system, with all PIPE parameters set to 0, is shown in *Table 1*. Here, the values of the last two new target image pixels $U_{L-1,M}$ and $U_{L,M}$ are being calculated, and the beginning and end of the interpolation walks of length K which sample source image pixels in the neighborhod of locations ($X_{I-1,J}$, $X_{I,J}$) can be seen. Utilizing the arrival of the source image address ($SADR_{31-0}$) as a reference point, the other signals shown can be delayed up to seven clock cycles from the nominal timing shown here, allowing the user to configure these outputs to match the timing latencies of his pixel data path structure. Considerable speed and timing variations in image buffer memory, data register, and pixel interpolator structure can thus be accomodated, with minimal corresponding support hardware. Also see "PFLS," in the ***Device Configuration and Control Parameters*** section.

Transformation Coefficient and Configuration and Control Parameters

The TMC2302 is intended to act as a co-processor, requiring only that the user program the device to perform the image transformation desired by loading in the appropriate device configuration and transformation control parameters discussed in this section. The user then issues an "Init" command, allowing his system to run unattended until the completion of the image when a "Done" flag is generated to inform the host system.

The capabilities and flexibility of the TMC2302 Image Manipulation Sequencer are apparent when reviewing the following tables which define the transformation coefficient and configuration and control parameters. These tables are broken up into two separate groups. The first parameters discussed are the control words which select the dimension calculated, the functional configuration of each device, the working space in which they will operate, the size of the interpolation kernel desired, and the timing of the various address and control signals involved in handling the pixel data pipeline. The second parameters are the polynomial transform coefficients used in performing image manipulation. The TMC2302 utilizes three levels of internal 48-bit accumulators to calculate these values by forward difference accumulation, generating no significant cumulative spatial error for most applications. The user must be aware that all internal parameter and coefficient registers must be set by the user, including resetting after powerup any unused control words or coefficients.

A major difference between the TMC2302 and the TMC2301 is that elimination of the device interconnects. Instead, the user programs all X, U, V, and W boundaries into all TMC2302 devices. The system's progress through the image is monitored by each device independently and in parallel.

Transformation Coefficient and Configuration and Control Parameters (cont.)

The boundary values are usually identical in all devices in order to maintain synchronous operation.

As mentioned above, the TMC2302 also features user-programmable image data pipeline configuration controls. All output signals except the source and coefficient address outputs can be individually delayed by the user up to seven clocks after the nominal system timing illustrated in ***Table 1***. This allows the user to software-configure the TMC2302s in his system to match his pixel interpolator, image buffer, and interpolation coefficient RAM structure timing.

The user can also program the device to continue into the next image for a set number of clock cycles after the Done flag has appeared. First, this "flushes" the final resampled pixel data word through the interpolation pipeline, all the way to the target image RAM. Also, valid pixel data will then appear on the first clock of the next transform independent of the length of the pixel pipeline, incurring no lost clock cycles.

Device Configuration and Control Parameters

UMIN, VMIN, WMIN — The memory addresses of the target image boundaries corresponding to the top, left side, and front page of the new image being generated are defined in all devices of the user's system by the parameters UMIN, VMIN, and WMIN, respectively. At the beginning of the transformation, the initial source image coordinate (X_0, Y_0, Z_0) will be mapped to this coordinate set. The numeric format assumed is 12-bit unsigned binary integer.

UMAX, VMAX, WMAX — The memory addresses of the target image boundaries corresponding to the bottom, right side, and last page of the image being generated are defined in all devices by the parameters UMAX, VMAX, and WMAX, respectively. These values should be greater than the UMIN/VMIN/WMIN values defined above. Numeric format assumed is unsigned 12-bit binary integer.

Note: The parameter UMAX must exceed UMIN so as to ensure that a minimum of 5 system clock cycles in two-dimensional operation, or 15 clock cycles in three-dimensional operation, pass between the periods in which these two target address values are generated. Thus in 2D nearest neighbor operation UMAX must be 5 greater than UMIN. In 2D bilinear interpolation mode (4-pixel two-dimensional kernel), the distance must be two pixels in the target image (actually enforcing a spacing of 8 system clocks).

UMINI, VMINI, WMINI — The target image addresses corresponding to those of the top, left side, and front page of the 2 or 3 dimensional region indicated by the valid target address flag $\overline{\text{TVAL}}$ are UMINI, VMINI, and WMINI, respectively. Thus, to define a valid region beginning at "m," the MINI parameter value is "m." These parameters are assumed to be in 12-bit unsigned binary integer format.

UMAXI, VMAXI, WMAXI — The target image addresses one more than those of the right side, bottom and back page of the region indicated by the valid target address flag $\overline{\text{TVAL}}$ are UMAXI, VMAXI, and WMAXI, respectively. Thus, to define a valid region ending at "n," the MAXI parameter value is "n+1". These parameters are assumed to be in 12-bit unsigned integer format.

XMIN, XMAX — The source image boundaries are defined for each device by the parameters XMIN and XMAX, in the case of the row device. The column device then contains YMIN and YMAX, and the page device (in systems performing three-dimensional operations) ZMIN and ZMAX. The value of XMAX should be greater than XMIN if the boundary violation flag $\overline{\text{SVAL}}$ is to operate correctly. These values are assumed to be in 32-bit unsigned binary integer format.

PFLS — The user can set the number of clock cycles that the TMC2302 continues in to the next image following the DONE flag, allowing his system to Flush all control and data pipeline paths and halt after a maximum of seven cycles. The numeric format assumed is three-bit unsigned binary integer.

Device Configuration and Control Parameters (cont.)

PTAD, PDON, PEND, PTVA, PSVA, PTWR, PACC — As mentioned above, the control signals and target image pixel addresses generated by the TMC2302 can be delayed up to seven clock cycles after the nominal timing shown in ***Table 1*** by setting the appropriate Pipeline delay word. The numeric format assumed for all delay words is three-bit unsigned binary integer.

XTND — When the user sets the control bit XTND to 1, the TMC2302 operates in an extended-resolution source address bus configuration. Assuming that the user has his own raster scan generator available elsewhere to manage the flow of output pixels from the TMC2302 system, the target address output bus $TADR_{11-0}$ is reconfigured internally into an extension of the source address bus, as $SADR_{11-0}$. The original source address bus $SADR_{23-0}$ is then $SADR_{35-12}$, providing 36 bits of spatial resolution in the source address space. An XTND of 0 puts the device in the standard 24-bit source, 12-bit target address configuration.

E3D — Setting this control bit to 0 indicates a two-dimensional image transform is to be performed. When the E3D is set to 1, a three-dimensional image is assumed, using three TMC2302 devices.

DIM — The user sets each TMC2302 to operate in a specific dimension as follows:

$DIM_{1,0}$	Dimension
00	X/U (Row) Device
01	Y/V (Column) Device
10	Z/W (Page) Device
11	No Operation

MODE — In systems performing the standard two-dimensional spiral interpolation walk, MODE is set to 11, indicating single-pass operation. When performing multiple-pass resampling, the user must set this two-bit control word pass-by-pass in all IMSs, to implement each pass direction. For instance, setting MODE to 00 causes the TMC2302 system to increment only in the X-direction, holding the Y (and Z) addresses constant until the end of that pixel walk. On the next pass through the image, the user sets MODE=01, with the kernel increment in Y only. In 3D, the IMS system then proceeds again through the (U, V) target image space, walking kernels only along the Z direction.

$MODE_{1,0}$	Resampling Performed
00	X-Pass
01	Y-Pass
10	Z-Pass
11	Two-Dimension Spiral Walk

KERNEL — This parameter determines the size of the interpolation walk performed. To implement a convolutional sum of K+1 pixels, the parameter KERNEL is set to K, up to a maximum of 255. In single-pass operation, this value must be identical in all devices, giving a square interpolation kernel. In multiple-pass operation, however, non-square kernels may be implemented, with different K values in each dimension. Or, the user could utilize a banded memory architecture in two-pass mode to access an entire row or column of a kernel in one clock, completing the entire sum in a single pass through the other dimension of the kernel. Numeric format is 8-bit unsigned integer.

FOV — The user determines the size of each step in an interpolation walk, in terms of the number of source image pixels, by setting the Field Of View control. The binary weighting of the image transformation parameters and source address must be taken into account when determining this value. See ***Table 6*** and the ***Applications Discussion*** section. The numeric format assumed is unsigned 16-bit integer.

Table 2. Control Parameter Registers Binary Format (Row, Column or Page Device)

Name	Addr Hex	Format MSB														LSB	Limits Dec	Limits Hex
UMIN	30					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
UMAX	31					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
UMINI	32					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
UMAXI	33					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
VMIN	34					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
VMAX	35					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
VMINI	36					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
VMAXI	37					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
WMIN	38					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
WMAX	39					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
WMINI	3A					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
WMAXI	3B					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
XMINL	3C	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	00000000
XMINM	3D	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	$2^{32}-1$	FFFFFFFF
XMAXL	3E	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	00000000
XMAXM	3F	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	$2^{32}-1$	FFFFFFFF
PFLS	40		2^{2}	2^{1}	2^{0}													7 0	7 0
PTAD	40					2^{2}	2^{1}	2^{0}										7 0	7 0
PDON	40								2^{2}	2^{1}	2^{0}							7 0	7 0
PEND	40											2^{2}	2^{1}	2^{0}				7 0	7 0
PTVA	40														2^{2}	2^{1}	2^{0}	7 0	7 0
PSVA	41		2^{2}	2^{1}	2^{0}													7 0	7 0
PTWR	41					2^{2}	2^{1}	2^{0}										7 0	7 0

Note: Table 1 continues on the following page.

Table 2. Control Parameter Registers Binary Format (cont.)

Name	Addr Hex	Format MSB															LSB	Limits Dec	Hex
PACC	41									2^2	2^1	2^0						7 0	7 0
XTND	41												XTND						
E3D	41													E3D					
DIM	41														DIM_1	DIM_0			
MODE	41																$MODE_1$	$MODE_0$	
KERNEL	42									2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	255 0	FF 00
FOV	43	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	$2^{16}-1$ 0	FFFF 0000

Transformation Parameter Registers

The Transformation Parameter Word storage register addresses for the X/U device are listed in ***Table 3***, along with the differential terms for each polynomial coefficient for both two and three-dimensional transforms. The polynomial terms for the other IMS device(s) are found by replacing every "X" in the table with a Y (or Z). A TMC2302-based system can perform image manipulations of up to third order in two dimensions, and three-dimensional transforms of up to order 1.5 ("first-and-a-half order"). Also, see "The Image Transformation Polynomial", in the *Applications Discussion* section.

The notation used to define each polynomial coefficient term in ***Table 3*** is easily interpreted. Each differential is of course defined by a differential in X, followed by the corresponding dependent U, V, or W terms. Thus,

DXUV is equivalent to $d^2X/dUdV$

and

DXUUUV to d^4X/dU^3dV.

Table 3. Transformation Polynomial Coefficient Register Addresses

Name	Parameter 2D Term	Parameter 3D Term	Coefficient Word Addresses (hex) MSW	CSW	LSW
A	X_0	X_0	00	01	02
B	DXU	DXU	03	04	05
C	DXUU		06	07	08
D	DXUUU		09	0A	0B
E	DXV	DXV	0C	0D	0E
F	DXUV	DXUV	0F	10	11
G	DXUUV	X_0	12	13	14
H	DXUUUV	DXU	15	16	17
I	DXVV	DXVW	18	19	1A
J	DXUVV	DXUVW	1B	1C	1D
K	DXUUVV	DXW	1E	1F	20
L	DXUUUVV	DXUW	21	22	23
M	DXVVV		24	25	26
N	DXUVVV		27	28	29
O	DXUUVVV		2A	2B	2C
P	DXUUUVVV		2D	2E	2F

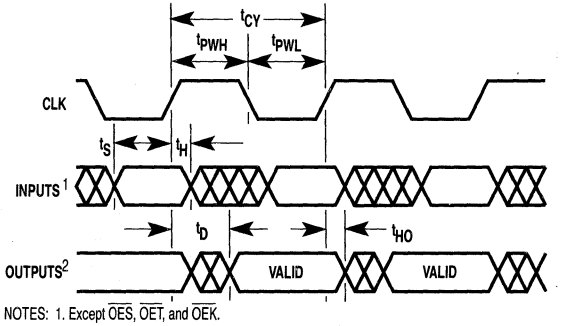
Note: The X_0 and DXU terms must each be loaded into two different registers when performing 3D transforms. Table 3 shows the binary weighting of all of the Transformation Parameter words, which are 48-bit signed fractional binary.

Table 4. Integer Binary Weighting of Transformation Parameters

	Format																Limits	
	MSB															LSB	Dec	Hex
MSW	-2^{47}	2^{46}	2^{45}	2^{44}	2^{43}	2^{42}	2^{41}	2^{40}	2^{39}	2^{38}	2^{37}	2^{36}	2^{35}	2^{34}	2^{33}	2^{32}	$2^{48}-1$	FFFFFFFFFFFF
CSW	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}		
LSW	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	000000000000

Note: A minus sign indicates a sign bit.

Figure 4a. Timing Diagram, Pixel Clock, Control, and Outputs



NOTES: 1. Except $\overline{OES}$, $\overline{OET}$, and $\overline{OEK}$.
2. Assumes $\overline{OES}$, $\overline{OET}$, and $\overline{OEK}$ = LOW. All pipeline latency parameters set to 0.

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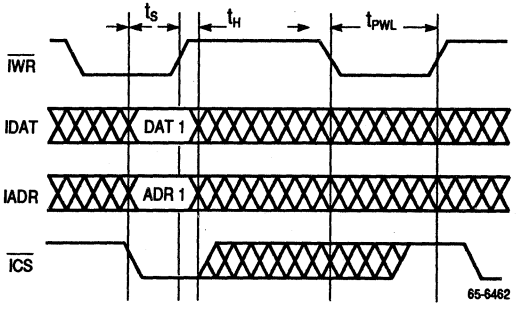
Figure 4b. Timing Diagram, Preload Parameters



Value "DAT 1" is loaded into address "ADR 1" on the second rising edge of IWR, since ICS = 0, having been acquired by the input register on the first edge.

Figure 5. Equivalent Input Circuit

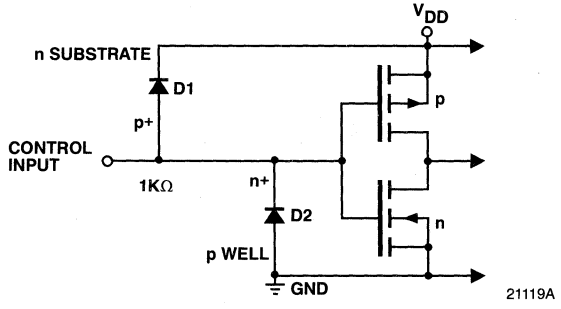


Figure 6. Equivalent Output Circuit

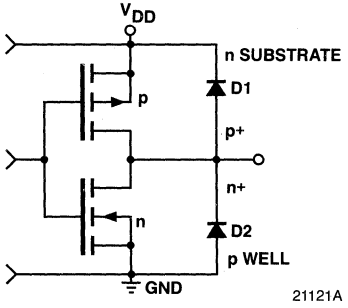
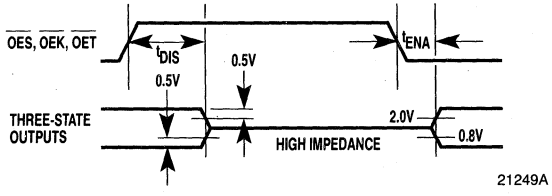


Figure 7. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+0.5)V

Output

Applied voltage [2] ..... −0.5 to (V_{DD}+0.5)V

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.

Operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Standard						
						−1			
			Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				8.0			8.0	mA
I_{OH}	Output Current, Logic HIGH				−4.0			−4.0	mA
t_{CY}	Cycle Time	V_{DD}=Min	33			25			ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	15			12.5			ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	15			10			ns
t_S	Input Setup Time		10			8			ns
t_H	Input Hold Time		2			2			ns
T_A	Ambient Temperature, Still Air		0		70	0		70	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	−1 Min	−1 Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=20MHz, $\overline{OES}=\overline{OEK}=\overline{OET}$=5V		70		70	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V	−40		−40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.	−20	−70	−20	−70	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	−1 Min	−1 Max	Units
t_{DO}	Output Delay	V_{DD}=Min, C_{LOAD}=25pF		15		12	ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=25pF	4		4		ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD}=Min, C_{LOAD}=25pF		12		12	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD}=Min, C_{LOAD}=25pF		15		15	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Applications Discussion

The Image Transformation Polynomial

On any given clock cycle, when performing a two-dimensional geometric transformation the addresses output by the row (X/U) TMC2302 are generated by forward difference accumulation according to the following third-order polynomial:

$$x(u,v) = a + bu + cu^2 + du^3 + ev + fvu + gvu^2 + hvu^3 + iv^2 + jv^2u + kv^2u^2 + lv^2u^3 + mv^3 + nv^3u + ov^3u^2 + pv^3u^3 + FOV \cdot CAX(ca)$$

The polynomial utilized for three-dimensional transforms is:

$$x(u,v,w) = a + bu + ev + kw + fuv + ivw + luw + juvw + FOV \cdot CAX(ca)$$

where $UMIN \leq u \leq UMAX$, $VMIN \leq v \leq VMAX$, $WMIN \leq w \leq WMAX$, and the polynomials for the column or page devices are obtained by replacing the x by a y or z, as appropriate.

The Image Transformation Polynomial (cont.)

FOV is the 16-bit field-of-view parameter, normally set so that the spiral walk proceeds in single-pixel steps. FOV can be increased to expand the step size and thus the spiral walk, subsampling the image. See *Table 2* and *Table 6*. Also, CAX(ca) is the current value of the coefficient address, and CAX(Ker) is the terminal value of each pixel walk in that dimension. See the *Interpolation Coefficient Lookup Table Addressing*. The CAX(Ker) term arises because the IRS computes each new walk's starting point from the previous spiral walk's end point, rather than its starting point.

We can reform the two-dimensional polynomial as:

$$x(u,v) = (a + ev + iv^2 + mv^3) + (b + fv + jv^2 + nv^3)u + (c + gv + kv^2 + ov^3)u^2 + (d + hv + lv^2 + pv^3)u^3,$$

and retain the simpler three-dimensional form:

$$x(u,v,w) = a + bu + ev + kw + fuv + ivw + luw + juvw$$

and define each of the polynomial coefficients in arithmetic terms, as shown in *Table 5*.

Table 5. Transformation Polynomial Coefficients

	Parameter			
	Two-Dimensional		Three-Dimensional	
Name	Term	Coefficient	Term	Coefficient
A	X_0	a	X_0	a
B	DXU	b+c+d	DXU	b
C	DXUU	2c+6d	—	0
D	DXUUU	6d	—	0
E	DXV	e+i+m	DXV	e
F	DXUV	f+g+h+j+k+l+n+o+p	DXUV	f
G	DXUUV	2(g+k+o)+6(h+l+p)	X_0	a
H	DXUUUV	6(h+l+p)	DXU	b
I	DXVV	2i+6m	DXVW	i
J	DXUVV	2(j+k+l)+6(n+o+p)	DXUVW	j
K	DXUUVV	4k+12l+12o+36p	DXW	k
L	DXUUUVV	12l+36p	DXUW	l
M	DXVVV	6m	—	0
N	DXUVVV	6(n+o+p)	—	0
O	DXUUVVV	12o+36p	—	0
P	DXUUUVVV	36p	—	0

Understanding The Polynomial Coefficients An Overview

As the formulae indicate, the source address is a polynomial function of the two (or three) dimensions of the target address. Each of the 16 terms of the equation is of the form:

$$\frac{d^{m+n+p}X}{du^m\,dv^n\,dw^p},$$

and may be treated approximately as a mixed partial difference of order m, n, and p.

The simplest term, X_0, is a zeroeth (non-) function of the target addresses; it specifies the source address point corresponding to the upper left point in the target space. X_0 generates image translation or "pan."

The next-simplest terms, dX/dU and dY/dV, govern the relative scales of the source and target images, i.e., how large a step in source space corresponds to a unit step in the corresponding direction in the target space. As long as the cross-terms, dX/dV and dY/dU, are zero, this is a straight scale ("zoom") operation, without rotation or shear.

Multimedia

Understanding The Polynomial Coefficients (cont.)

The first-order cross terms, dX/dV and dY/dU, generate source space displacements perpendicular to unit displacements in the target space, thereby causing shearing of the image. In conjunction with the parallel source terms described above, they govern rotation, shear, and scaling of the image.

Although the actions of the higher-order terms become progressively difficult to describe, all terms behave essentially as partial differences of various orders, and a little thought and common sense will generally lead the user to the proper conclusions. For example, the term dXUU (using the notation of ***Table 3***) is a horizontal scale factor which increases as one progresses across each row, causing a quadratic horizontal warp. In fact, all terms of the form dmX/dUm or dnY/dVn cause only stretching of the image, never rotation.

Interpolation Coefficient Lookup Table Addressing

The external coefficient lookup table RAM stores the interpolation coefficient values used to calculate the value of the new pixel. These values are selected by the user, allowing maximum filtering flexibility. In simple filtering applications, the source and target pixel addresses map one-to-one, and only one interpolation coefficient set is required. These integer addresses are generated for each dimension by the internal walk counters of each TMC2302.

However, applications performing a coordinate transformation will almost always generate non-integer source pixel addresses; that is, the U (or V) locations will not map to the X (or Y) addresses exactly, and a fractional source address components are generated. The user must then expand the interpolation coefficient lookup table to include spatially-corrected values, as determined by the subpixel resolution of the system.

The TMC2301 Image Resampling Sequencer allows the user to trade subpixel resolution against interpolation step size by obtaining the interpolation coefficient addresses directly from the fractional part of the source address. The TMC2302 gives the user 16 different interpolation bit weighting positions. The complete Interpolation Coefficient Address for that dimension then consists of both the 8-bit interpolation walk address $KADR_{7-0}$, weighted to match the source address binary point by the parameter FOV, and the fractional portion of the source pixel address $SADR_{23-0}$, to the desired subpixel resolution. See Table 6.

Internal and External Data Formats

The source address value output by the TMC2302 is a 24-bit two's complement number, with binary point assignable by the user anywhere in the 16 lower bits. The Extended mode appends 12 additional fractional bits for greater output precision. All internal computations include these 24 plus 12 bits, plus an additional 12 lower bits, for 48-bit precision. See ***Table 6***.

Internally, each TMC2302's source address (X, Y, or Z) generator computes a 48-bit address through a mode-specific accumulation of the sixteen 48-bit user-specified resampling parameters. The 24 most significant bits of the final accumulation emerge via the source address port, whereas the "extend" mode makes the 12 next-most-significant bits available at the target address port. The 12 least significant bits are truncated internally.

Source Address Bit Weighting and Setting the Binary Point

When performing nearest-neighbor resampling, the user may arbitrarily trade source image size against subpixel resolution merely by adhering to a single binary point position for all resampling parameters. For example, if the binary point follows the 16 most significant bits in each resampling parameter, then it will appear following the source address' 16 most significant bits, leaving 8 (20 in extended mode) bits of subpixel resolution on $SADR_n$.

Since the TMC2302 has no internal limiter, the user should select the source address weighting appropriately. Moving the source address connections to the right, and reducing the resampling parameters accordingly, reduces the chance or arithmetic overflow while increasing arithmetic round-off error.

In any filtering or resampling operation performing an interpolation walk, the user should set the Field or View (FOV) parameter according to the desired binary point position determined above, as follows. To provide 2^{24} integral pixel positions per dimension, with no subpixel resolution, set FOV = 001 (hex). For 2^{23} positions with 1-bit (0,5) subpixel resolution, FOV = 0010 (hex). Similarly, for 2^9 positions and 15-bit subpixel resolution. FOV = 8000 (hex). As shown in ***Table 6***, using the parameter FOV the user effectively "shifts" the bit weight of the coefficient address word $KADR_{7-0}$ to match the established location of his source address binary point. In each case, the EXTEND mode provides 12 additional bits of subpixel resolution but eliminates the separate target or raster address, which must then be generated elsewhere in the user's system.

Table 6. Relative Bit Weighting – Source Address

Word \ Weight	2^{47}	$2^{46}...2^{40}$	2^{39}	2^{32}	$2^{31}...2^{25}$	2^{24}	$2^{23}...2^{16}$	$2^{15}...2^{12}...2^{8}$	$2^{7}...2^{0}$
Transform Parameters	–47	46							0
Internal Source Address Generator	–47	46							0
Source Address Output $SADR_{23-0}$	–23	22 ... 16	15	8	7 ... 1	0			
Extended Mode Only $TADR_{11-0}$							11 ... 4	3 ... 0	
$KADR_{7-0}$									
FOV = 0001					2^7 ... ... 2^0				
FOV = 0002				2^7	2^6 ... 2^0				
•									
•									
•									
FOV = 8000		2^7 ... 2^1	2^0						

Note: A minus sign indicates a sign bit.

Utilization of the Image Boundary Flags $\overline{SVAL}$ and $\overline{TVAL}$

As mentioned above, the TMC2302 provides two programmable valid address, or boundary flags. The source valid flag $\overline{SVAL}$ is asserted when the current source image address output for that device's source image dimension is within the space defined by the configuration parameters XMIN and XMAX, or YMIN and YMAX, or ZMIN and ZMAX, as appropriate. Also, the target valid flag $\overline{TVAL}$ is available to indicate when the current target image address values fall within the space defined by the configuration parameters UMINI, UMAXI, VMINI, VMAXI, and also WMINI and WMAXI in three-dimensional systems. Note that all of these parameters are each programmed into each individual TMC2302. Thus, the user could define two (or three) different working spaces, one indicated by each IMS device.

Figure 8 may help clarify the relationships among (X_0, Y_0, Z_0), (UMIN, VMIN, WMIN), and (UMAX, VMAX, WMAX), for the two-dimensional case. With positive first derivatives, (X_0, Y_0) and (UMIN, VMIN) represent the upper left corners of the original image and the new destination field, respectively. The lower right corner of the new transformed image is located at (UMAX, VMAX); the location of the corresponding corner of the original image depends on the values of the derivatives.

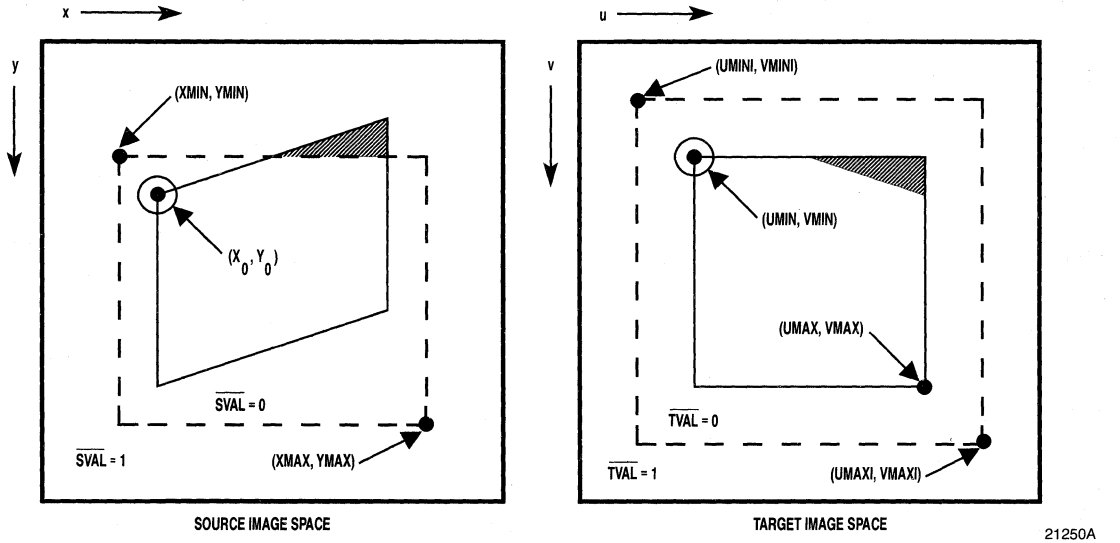
Not to be confused with (X_0, Y_0), the points (XMIN, YMIN) and (XMAX, YMAX) define the "usable" rectangular portion of the original image which is indicated by the valid address flag $\overline{SVAL}$; points (X, Y) lying outside this region are ignored in most resampling and filtering applications. Specifically, the point (X_0, Y_0) is the location from which the TMC2302 system begins the image resampling sequence. Every step beyond that point in the source image space is defined by the address generators implementing the image transformation polynomials.

The valid source address flag feature permits one to construct a mosaic of several abutting subimages in the (X, Y) plane, without danger of edge effect interference between adjacent subimages. Note in the figure that the upper right corner of the resampled source image lies outside the admissible region; in practice, the values fetched at these locations will not be included in the convolutional sums. One might, for instance, program these boundary values to alert the system that an edge is being approached and to modify the interpolation coefficients appropriately, or simply to ignore pixel values outside the defined space.

Utilization of the Image Boundary Flags $\overline{SVAL}$ and $\overline{TVAL}$ (con't.)

The flag $\overline{TVAL}$ however is utilized somewhat differently. Working in unison with the target address working space defined by UMIN/UMAX, etc., the target address valid flag could be programmed to delineate image areas other than the immediate working space, and the flag of each TMC2302 to indicate the unique regions anywhere within the target image. With this flexibility, the user can generate windows, "picture-in-picture" composite multiple images, or simply switch to a background image or border color.

Figure 8. Pixel Maps Demonstrating Source and Destination Image Boundaries, Violation Flags, and Image Clipping (Note Shaded Areas)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2302H5C [1]	STD – T_A = 0°C to 70°C	Commercial, 30MHz	120 Pin Plastic PGA	2302H5C
TMC2302H5C1 [1]	STD – T_A = 0°C to 70°C	Commercial, 40MHz	120 Pin Plastic PGA	2302H5C1

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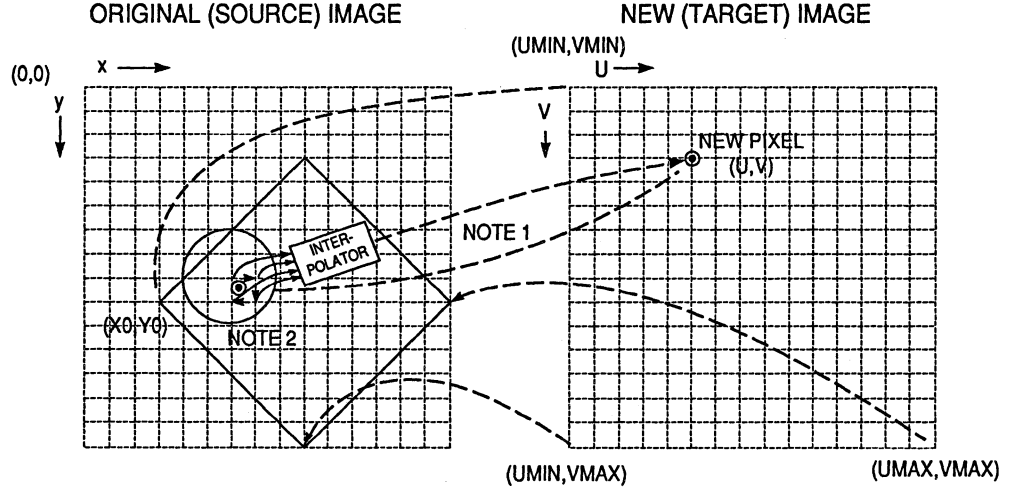
Real-Time Bilinear Interpolation Using the TMC2302 or TMC2301

Image transformations and translations in bit mapped systems are done by taking an original (source) image, performing coordinate remapping and interpolation, then restoring the image into a new (destination) image space. The coordinates are remapped according to a transformation polynomial. The polynomial, evaluated at destination pixel addresses, maps the transformed pixel addresses (U,V) to pixel addresses in the original image (X,Y), i.e., (X,Y) is a polynomial function of (U,V).



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Notes:

1. Coordinate transformation: Each pixel in (U,V) space is mapped to a location in (X,Y) space.
2. Interpolation: Unless the pixel in (U, V) space coincides with one in (X,Y) space, its amplitude must be estimated as a weighted average of these of the surrounding pixels in (X,Y) space. If the interpolation is done serially, throughput suffers in proportion to the size of the interpolation kernel. However, the interpolation can also be performed in parallel to preserve throughput, as discussed here.

The TMC2302 Image Manipulation Sequencer

The TMC2302 is a controller/address generator, around which an image filtering and resampling system can be built. Under limited supervision from an external controller, the TMC2302 will generate the sequence of memory read and write addresses to transform, resample, and/or filter an image. In all cases, it fetches data from one image buffer, governs its convolution with a user-specified kernel of coefficients, and directs the results to another image memory space. With 24-bit source address buses the device and operate from a source frame size of, for example, 64K X 64K pixels with spatial resolution of 1/256th pixel. A simplified block diagram of the TMC2302 is shown in Figure 2. Although the 24 source addresses bits of each TMC2302 can be designed arbitrarily with the source image address bus, assume for the current discussion that bits SADR (19:8) will correspond to the source image address and that SADR (7:4) therefore denote subpixel positioning to 1/16 pixel resolution.

The basic 2-D system, shown in Figure 3, consists of data source and destination memories, coefficient lookup table, multiplier-accumulator, TMC2302 parameters to define the transform and starts the operation. It may also control the loading of the source image into RAM and provide the screen refresh, if needed.

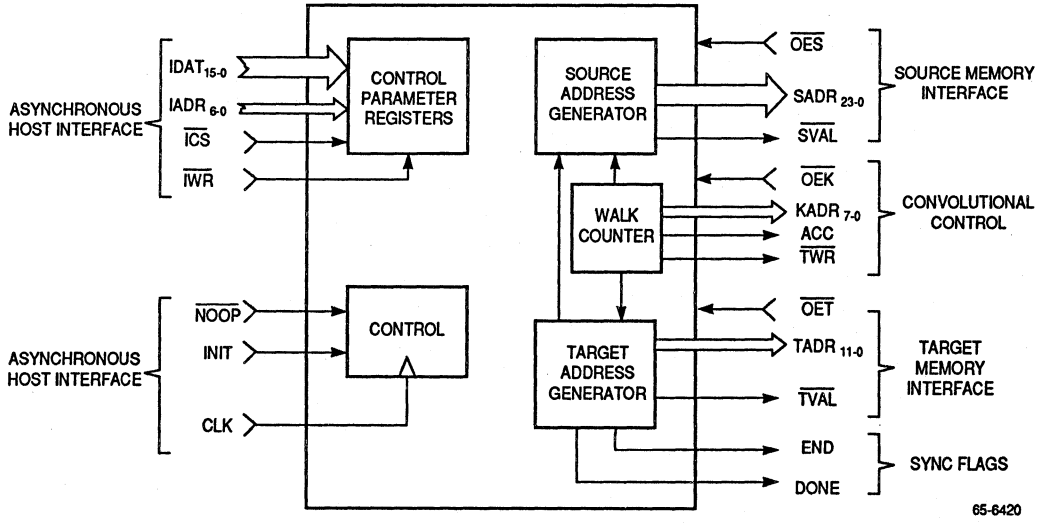


Figure 2. TMC2302 Block Diagram

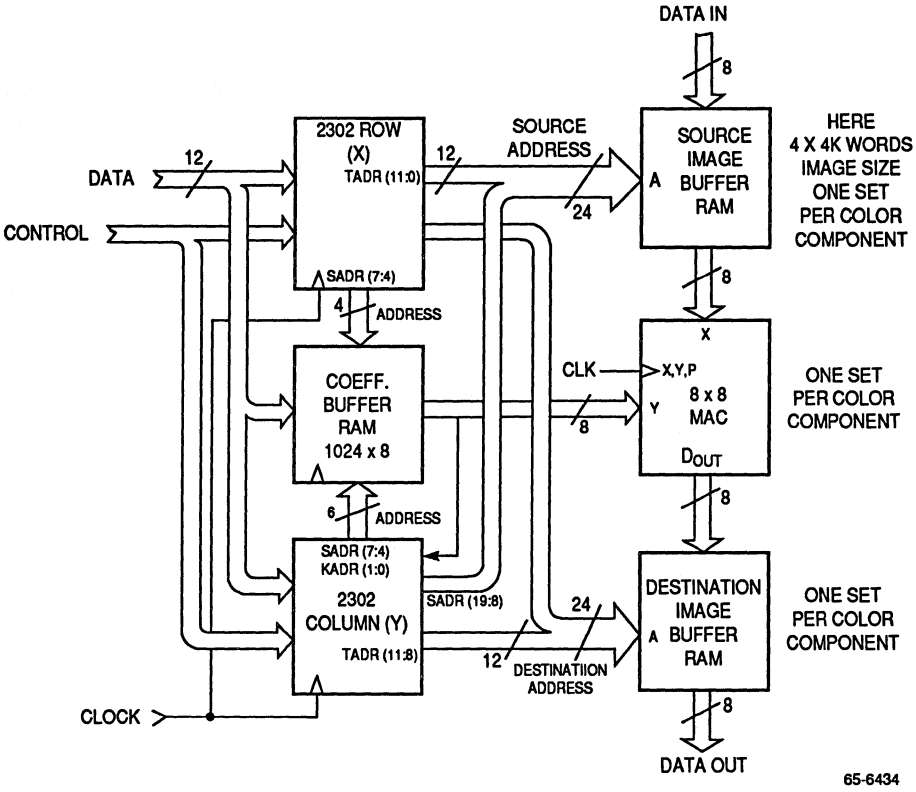


Figure 3. Basic 2-D Image Transformation Systems

Inexact Transformations

In many cases, evaluation of the transformation polynomial results in a non-integer result (non-integer address in the X, Y image space). In such cases, the mapping from original image to transformed image will be inexact. When this occurs, the user has the option of accepting the pixel "nearest" to the address generated, or performing interpolation, a weighted average of nearby pixel values. Using the pixel nearest the address generated is the fastest method since one transformed pixel can be generated on every cycle. The resulting image will include jagged biasing artifacts, however. Performing several transformations on the same image will further degrade the resulting image.

One Cycle Bilinear Interpolation

A better image can be obtained by finding the four pixels nearest the address generated and performing a weighted averaging to determine the new pixel value. This is known as bilinear interpolation. The TMC 2302 eases the control logic required for such a function by performing a "walk" around the four closest pixels in the source image space. Essentially, the TMC2302 generates the addresses of the four walk cycles, and the current source pixel is multiplied by a weighting factor and accumulated by the external multiplier accumulator. At the end of the walk, the accumulated result from the four nearest pixels is written into the destination image RAM and the TMC2302 proceeds to the next group. The obvious disadvantage to using bilinear interpolation is that one new destination pixel is generated only on every fourth cycle, reducing the output bandwidth by a factor of four.

One method of "real-time" bilinear interpolation consists of using four memories, each containing the entire source image. The storage arrangement of the pixels within each bank is staggered so that a single address fed to the memories will result in the access of the proper four pixel group. The TMC2302 is programmed to generate the nearest neighbor address and the four nearest pixels are accessed simultaneously and input to the four independent multipliers of a TMC2246 quad multiplier chip. The four pixels are multiplied by their associated weighting factors and added to determine the destination pixel sum. The major drawback of this method is the prohibitive cost for additional memory required to store four copies of the entire source image. For large images, the memory cost and additional board space makes this method unattractive.

A more efficient method is to divide the original source image into a "four-color checker board" and to store it into four separate pixel memory banks, each containing 14th of the source image. Since the image is separated into four memories rather than duplicated, no additional image memory is required. The goal is to separate the image so that any square of four adjacent pixel locations can be accessed simultaneously. Thus, the user must organize the memory such that the four pixels of any cluster will reside in separate memory banks. With this method, only one set of address generators (TMC2302s) is necessary, and only a slight address modification is necessary to guarantee that the correct group of pixels is accessed and output to the multipliers. Since all pixels are accessed simultaneously, no "walk" is performed, and the TMC2302 system is able to generate one destination pixel on each clock cycle. For example, a 1024 X 768 image can be generated every 20ms for a frame refresh rate of 50Hz. This method which will be described below.

Using "Banded" Pixel Memory

The TMC2302 should be programmed to do "nearest-neighbor" transformations (Kernel, K = 0 and the X_0 and Y_0 start boundaries programmed without 1/2-LSB truncation debiasing to force address truncation when evaluating the transformation polynomial for the nearest-pixel address). The biased X_0 and Y_0 guarantee that when the exact pixel address falls within the region of four pixels, the upper leftmost pixel will always be selected as "nearest-neighbor."

The key to performing real-time bilinear interpolation is to arrange the pixels in memory so that the four pixels of every grouping will be stored in separate memories. The four nearest pixels will form a square. Figure four shows a sample 512 X 512 pixel image and the arrangement into four separate memory banks designated A, B, C, and D. It can be seen from the figure that any (square) grouping of four pixels will have one pixel located in each bank. Thus, one memory sector will hold even row-even column pixels, another, even-row-add column pixels, etc.

$A_{0,0}$ (0,0)	$B_{0,0}$ (1,0)	$A_{1,0}$ (2,0)	$B_{1,0}$ (3,0)	$A_{2,0}$ (4,0)	$B_{2,0}$ (5,0)	$A_{3,0}$ ..... $A_{255,0}$ (6,0) .....(510,0)	$B_{255,0}$ (511,0)
$C_{0,0}$ (0,1)	$D_{0,0}$ (1,1)	$C_{1,0}$ (2,1)	$D_{1,0}$ (3,1)	$C_{2,0}$ (4,1)	$D_{2,0}$ (5,1)	$C_{3,0}$ ..... $C_{255,0}$ (6,1) .....(510,1)	$D_{255,0}$ (511,1)
$A_{0,1}$ (0,2)	$B_{0,1}$ (1,1)	$A_{1,1}$ (2,1)	$B_{1,1}$ (3,2)	$A_{2,1}$ (4,2)	$B_{2,1}$ (5,2)	$A_{3,1}$ ..... $A_{255,1}$ (6,2) .....(510,2)	$B_{255,1}$ (511,2)
$C_{0,1}$ (0,3)	$D_{0,1}$ (1,3)	$C_{1,1}$ (2,3)	$D_{1,1}$ (3,3)	$C_{2,1}$ (4,3)	$D_{2,1}$ (5,3)	$C_{3,1}$ ..... $C_{255,1}$ (6,3) .....(510,3)	$D_{255,1}$ (511,3)
$A_{0,2}$ (0,4)	$B_{0,2}$ (1,4)	$A_{1,2}$ (2,4)	$B_{1,2}$ (3,4)	$A_{2,2}$ (4,4)	$B_{2,2}$ (5,4)	$A_{3,2}$ ..... $A_{255,2}$ (6,4) .....(510,4)	$B_{255,2}$ (511,4)
$C_{0,2}$ (0,5)	$D_{0,2}$ (1,5)	$C_{1,2}$ (2,5)	$D_{1,2}$ (3,5)	$C_{2,2}$ (4,5)	$D_{2,2}$ (5,5)	$C_{3,2}$ ..... $C_{255,2}$ (6,5) .....(510,5)	$D_{255,2}$ (511,5)
$A0_{0,255}$ (0,510)	$B_{0,255}$ (1,510)	$A_{1,255}$ (2,510)	$B_{1,255}$ (3,510)	$A_{2,255}$ (4,510)	$B_{2,255}$ (5,510)	$A_{3,255}$ ..... $A_{255,2}$ 55 (6,510) .....(510,510)	$B_{255,255}$ (511,510)
$C_{0,255}$ (0,511)	$D_{0,255}$ (1,511)	$C_{1,255}$ (2,511)	$D_{1,255}$ (3,511)	$C_{2,255}$ (4,511)	$D_{2,255}$ (5,511)	$C_{3,255}$ ..... $C_{255,255}$ (6,511) .....(510,511)	$D_{255,255}$ (511,511)

Figure 4. Source Image Pixel Arrangement

Subscripts i,j for A, B, C, and D denote relative addresses in memory respectively.

The ordered pairs (a, b) denote the physical (X,Y) pixel locations and the TMC2302 SAPR(X) and SADR(Y) address outputs.

The pixels of the original image should be stored in the source RAM banks as shown in Figure 5. The original source image can be loaded by decoding the TMC2302 least significant address bits ($SADR_X(8)$. $SADR_Y(8)$ to determine the memory bank for the pixel while the most-significant address bits ($SADR_X(19:9)$, $SADR_Y(19:9)$) are used as common address lines to all four memory banks.

In the following discussion, the TMC2302 address outputs $SADR_X$ and $SADR_Y$ will be designated as:

Horizontal Source

XA_0 Least-Significant Horizontal Source X-Address Bit $SADR_X$ (8)
XA_μ Upper Horizontal Source Address Bits $SADR_X$ (19:9)

YA_0 Least-Significant Vertical Source Y-Address Bit $SADR_X(8)$
YA_μ Upper Vertical-Source Address Bits $SADR_Y$ (19:9)

TMC2302 Address		Bank A	Bank B	Bank C	Bank D
XA_μ	YA_μ	XA_0YA_0=00	XA_0YA_0=01	XA_0YA_0=10	XA_0YA_0=11
0	0	$A_{0,0}$	$B_{0,0}$	$C_{0,0}$	$D_{0,0}$
0	1	$A_{0,1}$	$B_{0,1}$	$C_{0,1}$	$D_{0,1}$
0	2	$A_{0,2}$	$B_{0,2}$	$C_{0,2}$	$D_{0,2}$
0	255	$A_{0,255}$	$B_{0,255}$	$C_{0,255}$	$D_{0,255}$
1	0	$A_{1,0}$	$B_{1,0}$	$C_{1,0}$	$D_{1,0}$
1	1	$A_{1,1}$	$B_{1,1}$	$C_{1,1}$	$D_{1,1}$
1	2	$A_{1,2}$	$B_{1,2}$	$C_{1,2}$	$D_{1,2}$
255	254	$A_{255,254}$	$B_{255,254}$	$C_{255,254}$	$D_{255,254}$
255	255	$A_{255,254}$	$B_{255,254}$	$C_{255,254}$	$D_{255,254}$

Figure 5. Memory-Pixel Arrangement

Interpolation Kernal

$P_{i,j}$ $P_{i,j+1}$

* - actual Pixel

Figure 6. TMC2302 Serial Walk Sequence
In real time bilinear resampling, this is executed in parallel.

$P_{i+1,j}$ $P_{i+1,j+1}$

When the transformation polynomial is evaluated and the resulting pixel address falls within a group of four nearby pixels (non-integer result), the TMC2302 will always choose the upper leftmost pixel (P_{jj}) as the nearest neighbor (due to the fractional address truncation in the X and Y directions). Since the four pixels will reside in independent banks, the upper leftmost pixel might be located in any of the four memory banks (A,B,C, or D). The bank which contains the nearest neighbor must be known, since in each case, different memory address modification is required to select the correct pixel from each bank.

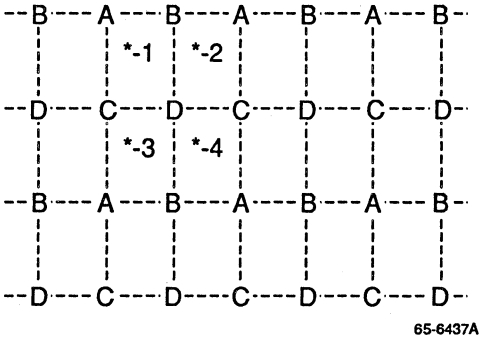


Figure 7. Possible Selections for Nearest Neighbor

Memory Address Modification

Using the address LSBs (XA_0, YA_0) from each TMC2302 external logic can determine which bank contains the nearest neighbor. (This same decoding is used when loading the original image into the source image RAMs.)

Case*	XA_0	YA_0	Nearest Neighbor (Upper Leftmost) Pixel
1	0	0	A Memory Bank contains Nearest Neighbor
2	0	1	B Memory Bank contains Nearest Neighbor
3	1	0	C Memory Bank contains Nearest Neighbor
4	1	1	D Memory Bank contains Nearest Neighbor

*from Figure 7 above

Addressing for each memory bank (A, B, C, D) is done using the uppermost address bits (XA_μ) of the TMC2302s. The LSB of each TMC2302 is used to determine both the upper leftmost pixel and the address modification required. In the following paragraphs, the lower case subscripts (i,j) denote the address of a pixel within a given memory bank (A, B, C, or D), and XA, YA are used to denote physical address outputs of the TMC2302 pairs.

Pixel address modification use to access the correct four pixel group is determined as follows:

Case A: $A_{i,j}$ is nearest upperleft neighbor,
(No address modifications)
($XA_0 = YA_0 = 0$)

$A_{i,j}$ $B_{i,j}$

*

$C_{i,J}$ $D_{i,j}$

Figure 8. Pixel Memory Mapping for A = Upper Leftmost

Memory Addressing Becomes:
A address = XA_μ, YA_μ
B address = XA_μ, YA_μ
C address = XA_μ, YA_μ
D address = XA_μ, YA_μ
i.e., no modification is required.

Case B: $B_{i,j}$ is upperleft neighbor,
(Modify X component of A & C memory addresses)
($XA_0 = 1$, $YA_0 = 0$)

$B_{i,j}$ $A_{i+1,j}$

*

$D_{i,j}$ $C_{i+1,j}$

Figure 9. Pixel Memory Pattern for B = Upper Leftmost

Memory Addressing Becomes:
A address = ($XA_\mu + 1$, YA_μ)
B address = (XA_μ, YA_μ)
C address = ($XA_\mu + 1$, YA_μ)
D address = (XA_μ, YA_μ)

Case C: $C_{i,j}$ is upperleft neighbor,
(Modify Y component of A & B memory addresses)
($XA_0 = 0$, $YA_0 = 1$)

$C_{i,j}$ $D_{i,j}$

*

$A_{i,j+1}$ $B_{i,j+1}$

Figure 10. Pixel Pattern for C = Upper Leftmost

Memory Addressing Becomes:
A address = XA_μ, $YA_\mu + 1$
B address = XA_μ, $YA_\mu + 1$
C address = XA_μ, YA_μ
D address = XA_μ, YA_μ

Case D: $D_{i,j}$ is nearest neighbor,
(Modify A, B & C addresses, X and Y components)
($XA_0 = 1$, $YA_0 = 1$)

$D_{i,j}$ $C_{i+1,j}$

*

$B_{i,j+1}$ $A_{i+1,j+1}$

Figure 11. Pixel Pattern for D = Upper Leftmost

Memory Addressing Becomes:
A address = $XA_\mu + 1$, $YA_\mu + 1$
B address = XA_μ, $YA_\mu + 1$
C address = $XA_\mu + 1_\mu$, YA_μ
D address = XA_μ, YA_μ

Taking a close look at the address modifications required for each case above, a simple pattern can be seen. This pattern leads to a set of address modification "rules" based on the values of the least-significant address bits from the TMC2301s (XA_0 and YA_0). These rules are:

When $YA_0 = 0$, (Case A & B)
No modification to the Y address component (YA_μ) is necessary.

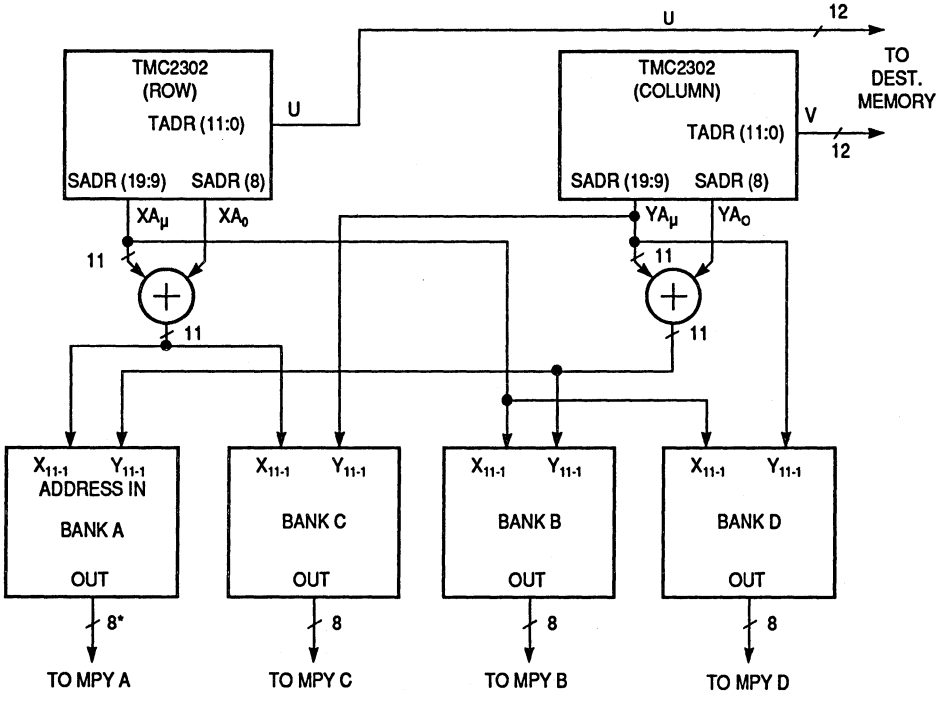
When $YA_0 = 1$, (Case C & D)
The Y component (YA_μ) of addresses to the A & B memory banks must be incremented by 1.

When $XA_0 = O$, (Case A & C)
No modification to the X address component (XA_μ) is necessary.

When $XA_0 = 1$, (Case B & D)
The X component (XA_μ) of addresses to the A & C memory banks must be incremented by 1.

A system can easily be designed to modify the pixel memory addresses according to the above criteria, to select the correct four pixels to be interpolated. Rather than actually performing a "conditional" address increment as discussed above, it requires less logic simply to add the LSB address bit to the memory bank addresses (XA_μ, YA_μ). Figure 12 shows the logic to perform the required address modifications. The addition ($XA_\mu + XA_0$, $YA_\mu + YA_0$) can be done using half-adders with the XA_0 (YA_0) address output of the TMC2302 connected to the carry-in of each adder. It can also be done using high-speed programmable logic.

Note: Only modifications to the source image memory are necessary. The destination image memory may be arranged in a linear or other type array as required by the refresh circuitry.



*Number of bits of intensity per pixel, per column component, typically 8 to 12.

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Figure 12. Memory Address Modification

Coefficient Memory

Typically, the 4 highest fractional source address bits from each TMC2302 (SADR (7:4) in the example) are used to reflect the offset from the nearest XA (YA) pixel location. With spatial resolution of 4 bits in both the X and Y directions, there can be as many as 256 unique coefficient values. This requires a coefficient memory of at least 256 bytes.However, as shown below, each of the four different cases requires its own set of 256 coefficients.

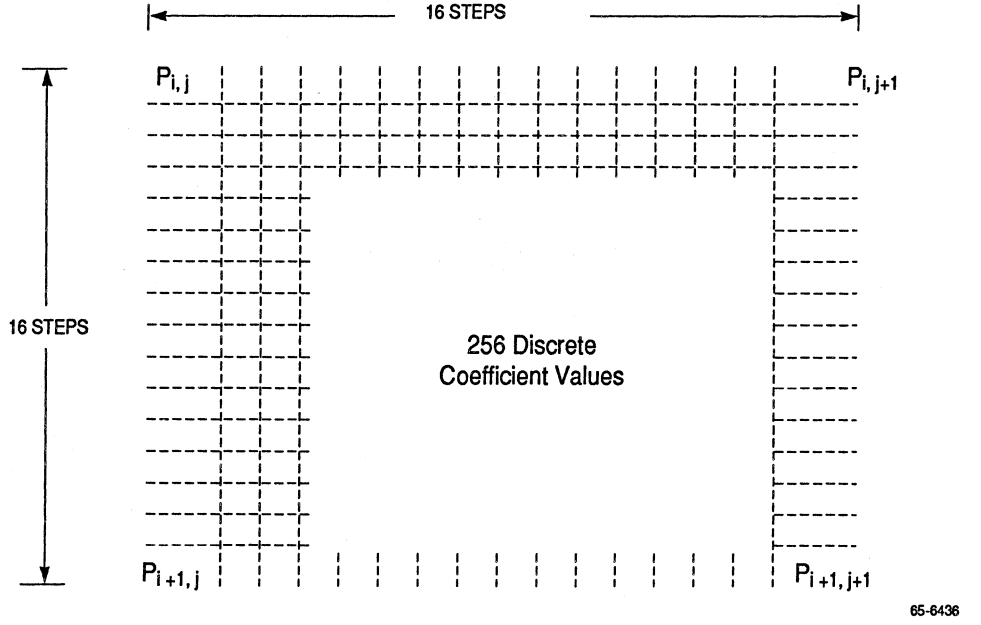


Figure 13. Interpixel Resoultion

One-cycle bilinear interpolation requires four independent coefficient memories, so that a parallel multiplication can be performed with the four pixel values.

Similar to determining the correct four pixel group, the coefficients must take into account the memory bank (A, B, C or D) that contains the upper leftmost pixel, and adjust the coefficients accordingly. These adjustments are necessary since the fractional address outputs ($SADR_X$ (7:4), $SADR_Y$ (7,4) from the TMC2302s reflect the spatial distance only from the upper leftmost pixel within the pixel group. Assuming that the fractional addresses $SADR_X$ (7:4) and $SADR_Y$ (7:4) plus the integer LSBs SADRX (8) and $SADR_Y$ (8) are to be used directly to address the 1024-byte coefficient memory, the loading of the coefficients is shown on the next page with F_X = $SADR_X$ (7:4) and F_Y = $SADR_Y$ (7:4) Case A through D are the same as discussed previously for the pixel address modifications.

Case A: A is nearest neighbor ($XA_0 = 0$, $YA_0 = 0$)

Coeff A = $(1- f_X) * (1 - f_Y)$
Coeff B = $(f_X) * (1-f_Y)$
Coeff C = $(1 -f_X) * (f_Y)$
Coeff D = $f_X * f_Y$

Case B: B is nearest neighbor ($XA_0 = 0$, $YA_0 = 1$)

Coeff A = $f_X * (1- f_Y)$
Coeff B = $(1- f_X) * (1- f_Y)$
Coeff C = $f_X * f_Y$
Coeff D = $(1-f_X)f_Y$

Case C: C is nearest neighbor ($XA_0 = 1$, $YA_0 = 0$)

Coeff A = $(1- f_X) f_y$
Coeff B = $f_X f_y$
Coeff C = $(1- f_X) (1- f_y)$
Coeff D = $f_X * (1-f_y)$

Case D: D is nearest neighbor ($XA_0 = 1$, $YA_0 = 1$)

Coeff A = $f_X f_y$
Coeff B = $(1 - f_X) f_y$
Coeff C = $f_X * (1- f_y)$
Coeff D = $(1- f_X) (1 - f_y)$

Incorporating the concepts outlined in this discussion, the final system for one-cycle bilinear interpolation is shown in figure 14. This figure shows a small increase in logic over the basic 2-D system shown in figure 3. The additional logic required includes: TMC2246 (rather than a single multiply/accumulate), and three additional coefficient memories. Some additional decoding logic is required to load the four pixel memory banks as well as some data and address pipelining (registering) to meet timing requirements. The solution, however, provides an increased pixel bandwidth, by a factor of four, and only a small increase in part count.

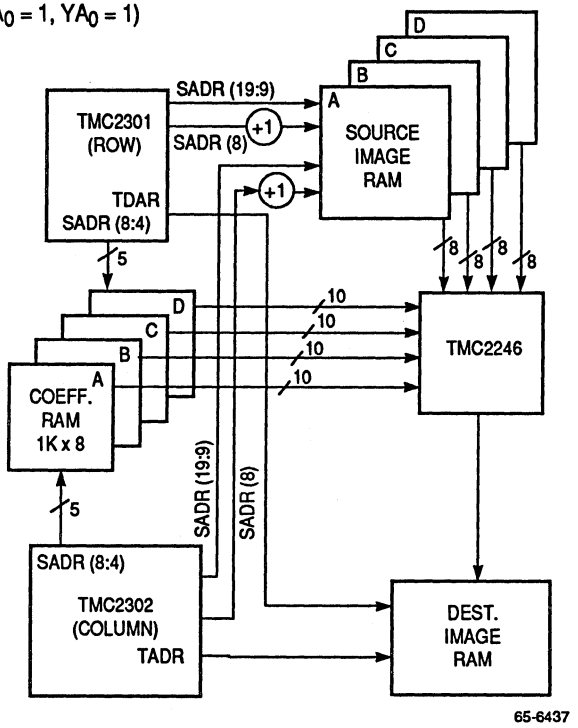
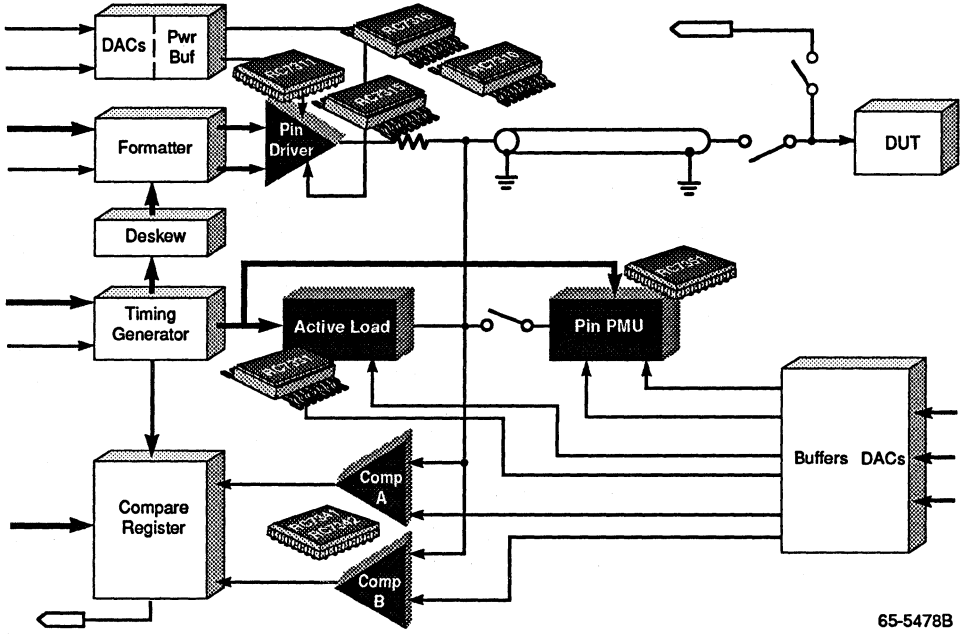


Figure 14. One-Cycle Bilinear Interpolation System

ATE Products



Raytheon offers a family of ASSPs designed to meet the needs of the ATE pin electronics system designer. The product family provides the end user with the capability of realizing a complete pin electronics card as shown above.

The RC7310, RC7311 and RC7315 250 MHz Pin Drivers offer a high output slew rate of 2 V/ns and wide output voltage ranges of -3.0V to +8.0V and up to 10 Vp-p output swings. The RC7311 is a cost effective pin driver primarily targeted for Memory ATE, while the RC7315 is a three-state output driver ideally suited for VLSI and Logic ATE. The RC7316 Pin Driver is designed for use in ultra high speed ATE systems. The RC7316 has the ability to drive a 50Ω transmission line of up to two feet in length with a slew rate of 3.2 V/ns and a repetition rate of over 550 MHz for ECL output levels. The device also features a maximum output swing of 9.5 Vp-p over the range of -3.0V to +7.0V. All products can be used as high performance line drivers for Instrumentation and Communications applications.

The RC7331 Active Current Load provides a ±50 mA of voltage-programmable current sourcing or sinking. The device features ±0.1% of output current resolution and ±0.2% of accuracy, while still maintaining 10 µA°C of drift.

The Raytheon ATE family includes a selection of comparators with both dual and window comparator configurations. The RC7341 and RC7342 are window and dual comparators respectively. They provide users with propagation delays of less than 2.5 ns, while attempting to keep input bias currents and input capacitance to a minimum.

Raytheon's ATE products are rounded out by the RC7351 Precision Measurement Unit (PMU) which is the only such standard device on the market today. This device allows users to force voltages and measure currents and vice versa, with precision and flexibility. The device supports four programmable voltage, and current ranges.

ATE Products

Pin Drivers	Slew Rate	Voltage Range	Output Swing (p-p)	Output Three State	Package	Page
RC7310	1.2 V/ns	-3.0 to +8V	10 Vp-p	No	28 PLCC	2-249
RC7311	2 V/ns	-3.0 to +8.0V	10V	No	28 PLCC, 16 LDCC	2-257
RC7315	1.8 V/ns	-2.5 to 7.5V	9.5V	Yes	28 EPLCC, 16 LDCC	2-265
RC7316	3.2 V/ns	-3.0 to 7.0V	9.5V	Yes	28 EPLCC, 16 LDCC	2-273

Active Load	Current Range	Current Resolution	Accuracy	Drift	Package	
RC7331/32	±50 mA	±0.1%	±0.2%	10 µA/°C	16 LDCC 20 PLCC	2-281

Comparators	Propagation Delay	Voltage Range	Input Bias Current	Input Capacitance	Package	
RC7341 (Window)	2.0 ns	-4V to +8V	10 µA (over -4 to +8V)	2 pF	16 SOIC	2-287
RC7342 (Dual)	2.0 ns	-4V to +8V	10 µA (over -4 to +8V)	1.25 pF	16 SOIC	2-287

Precision Measurement Unit	Force Voltage Range	Force Current Ranges	Force Current Resolution	Accuracy	Package	
RC7351	-5V to +15V	(4 Ranges) ±500 nA to ±20 µA ±2 µA to ±200 µA ±10 µA to ±1 mA ±500 µA to ±40 mA	±0.05%	12 bits, 0.5% gain error	28 PLCC	2-293
RC73687						2-303

Notes:
1. Both the RC7342 and the RC73687 are pin-for-pin compatible with 9687 standard comparators.

RC7310
High Speed Driver

Features

- High output slew rate (1.2 V/ns minimum)
- Wide output voltage range (-3.0V to +8V), and up to 10 Vp-p swings
- 250 MHz minimum operation for ECL swings
- Wide input common mode range for ease of interface to ECL as well as TTL and CMOS
- Output short-circuit protection with current limiter and thermal shutdown
- 100 mA dynamic switching current drive
- Absolute slew rate control
- Low output voltage offset (30 mV typ.) and output offset drift (0.1 mV/°C typ.)
- Low input bias current (1 µA typ.) and current drift (40 nA/°C typ.) for output level program voltage allows direct coupling to a DAC output
- Available in 28-pin PLCC

Applications

- Differential line driver/receiver
- Precision waveform generator
- Level translator
- Switch driver
- Laser driver
- CRT preamplifier

General Product Description

The RC7310 is a low cost High Speed Driver capable of over 250 MHz operation at ECL levels and greater than 1.2 V/ns slew rate for 5 Vp-p output. The driver offers programmable output levels between -3.0V and +8V and an output amplitude up to 10 Vp-p. It is therefore capable of driving any logic family such as ECL, TTL and CMOS. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with low offset (30 mV typical) and offset drift (0.1 mV/°C typical). The V_H and V_L inputs have been buffered to operate with low bias currents (1.0 µA typical) allowing direct coupling to the output of a DAC.

The RC7310 is normally driven by ECL levels. However, the input common mode range, -2V to +6V, is wide enough to accommodate TTL or CMOS input signals. When driven with a single ended signal the other input of the RC7310 must tied to the appropriate threshold voltage.

The RC7310 is specified at nominal power supply values of 10V and -5.2V, and commensurate output voltage swing limits of -3.0V and +8V.

The supply rails may be raised by 2V to achieve an output high level (V_{OH}) of +10V, or lowered by 2V to achieve an output low level (V_{OL}) of -5V. At all times there must be at least a 2V margin between the positive supply and the maximum value of V_{OH}, and between the negative supply and the minimum value of V_{OL}.

The RC7310 is implemented using Raytheon's high performance precision Complementary Bipolar Process (CBiP).

Pin Definitions

Name	Function
V_{CC}	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +8V, V_{CC} should be raised 2V above the maximum V_{OH} value. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
V_{EE}	Quiet negative supply. The nominal value is -5.2V to ±5%. For output low voltage levels (V_{OL}) less than -3V, V_{EE} should be lowered 2V below the minimum V_{OL} value. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{CCO}	Positive supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EEO}	Negative supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
GND	Chip ground. These pins should be connected to the printed circuit board's ground plane at the pins.
TST	Pin used for factory testing the thermal characteristics of the device. The pin should be left unconnected or tied to GND.
V_H	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_L	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from V_L to V_{OL} is nominally unity gain.
V_{HC}	Bypass for analog program input high, V_H. V_{HC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_{LC}	Bypass for analog program input low, V_L. V_{LC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_{IN+} V_{IN-}	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs will normally be driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_O	Driver output of RC7310. The output impedance is 12.6Ω ±1.5Ω. The output is usually back-terminated in the characteristic impedance of the driven transmission line. For a 50Ω line, a 37.4Ω ±1% or better resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short-circuit current of the output.
OF	On chip filter to improve output waveform (optional). This pin connection is optional and should be left unconnected if not used. When used OF pin should be tied to the termination node that is directly connected to the DUT.
SRCA	Absolute slew rate control. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin affects both positive and negative edge rates. If this slew rate control is not desired this pin should be left open.
CIM1 CIM2	**Optional:** A 10,000 pF chip capacitor could be placed between CIM1 and CIM2 to improve impedance matching across different voltage swings. With this capacitor, output impedance stays more constant with changes in voltage swings. If not used, leave pins CIM1 and CIM2 open.
SRCM	Slew rate control matching. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin adjusts the match between positive and negative edges . If this slew rate control is not desired this pin should be left open.

Pin Definitions (continued)

Name	Function
$\overline{TS}$	Active low output notifies thermal shutdown has occurred. In the event of a short-circuit or other fault that causes the die temperature to rise between 115°C and 160°C, the thermal shutdown will activate. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wired together and input to a latch to indicate an alarm condition.
NC	No connection.

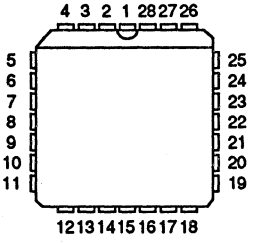
Absolute Maximum Ratings (1)

Positive power supply, V_{CC} 13V
Negative power supply, V_{EE} ..... -8.2V
Difference between V_{CC} and V_{EE} 16V
Input voltage at V_{IN+}, V_{IN-} ..... V_{CC} -12V
V_{EE} +12V
Input voltage at $V_{H, L}$ ..... V_{CC} -13V
V_{EE} +13V
Differential input voltage, $|V_{IN+} - V_{IN-}|$ 6V
Difference between V_H & V_L, $(|V_H - V_L|)$ 13V
Driver output voltage ..... V_{CC} -13V
V_{EE} +13V
Output voltage at $\overline{TS}$ 7V
Duration of short-circuit to ground ..... Indefinite
Operating temperature range ..... 0°C to 70°C
Storage temperature range ..... -65°C to +125°C
Lead temperature range
(Soldering 10 seconds) ..... 300°C

Notes:
1. "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Connection Information

28-pin PLCC Package
(Top View)



65-5741

Pin	Function	Pin	Function
1	V_O	15	V_{IN+}
2	OF	16	GND
3	CIM1	17	NC
4	CIM2	18	V_H
5	TST	19	V_L
6	NC	20	NC
7	V_{CCO}	21	NC
8	V_{CC}	22	V_{EE}
9	V_{HC}	23	V_{EEO}
10	V_{LC}	24	$\overline{NC}$
11	SRCM	25	TS
12	SRCA	26	NC
13	NC	27	NC
14	V_{IN-}	28	GND

Ordering Information

Part Number	Package	Operating Temperature Range
RC7310QA	QA	0°C to +70°C

Notes:
QA = 28-pin PLCC

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case operating temperature(1)	0		70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	V_{EE} +2V		V_{CC} - 2V	V
$\|V_{OH}$-$V_{OL}\|$	Output amplitude	0.4		10.0	V
R_T	Output back-termination resistor for RC7310		37.4		Ω

Notes
1. With air flow >300 lfpm

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air), no load, unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Differential Inputs: V_{IN+}, V_{IN-}					
V_{IN+}, V_{IN-}	Absolute Input Voltage		-2.0		+6.0	V
V_{ID}	Differential Input Range	$\|V_{IN+} - V_{IN-}\|$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Bias Current	-2V≤ $V_{IN\pm}$ ≤+6V		-100	-250	µA
	Absolute SLR Control, SRCA					
V_{SRCA}	Compliance Voltage Range	V_H = +5V, V_L = 0V	-2.3	-1.6	-0.9	V
I_{SRCA}	Control Current Range		-1.0		+1.0	mA
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = - 2.0		-20		%
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = - 2.4		-40/+25		%
	Matching SLR Control, SRCM					
V_{SRCM}	Compliance Voltage Range	V_H = +5V, V_L = -0V	0.4	0.6	0.9	V
I_{SRCM}	Control Current Range		-0.5		+0.5	mA
$\%_{SLR}$	Max % SLR Matching Change			30		%
	Voltage Program Inputs $V_{H,L}$					
V_H	V_H Range	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_L	V_L Range	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	-1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
V_A	$\|V_{OH} - V_{OL}\|$	Output Voltage Amplitude	0.40		10	V
I_H	Bias Current @ V_H	-1.0V ≤ V_H ≤ +8V; V_L = -3.0V		-1.0	-5.0	µA
I_L	Bias Current @ V_L	-3V ≤ V_L ≤ +5.5V; V_H = +8.0V		-1.0	-5.0	µA
TCI_H	Max Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_A ≤ 70°C; (output not switching)			40	nA/°C
TCI_L	Max Temperature Drift in I_L	V_L = -2.0; 25°C ≤ TC ≤ 70°C (output not switching)			40	nA/°C
ΔIBDC	Variation in I_H, I_L with Power Supply and DC Voltage at V_H or V_L	V_H = - 1.0V to +8V V_L = -3V to +5.5V	-2.0		+2.0	µA
$V_{H,L}$BW	$V_{H,L}$ BW	-3 dB point from $V_{H,L}$BW to V_{OUT}		50		kHz

DC Electrical Characteristics (continued)

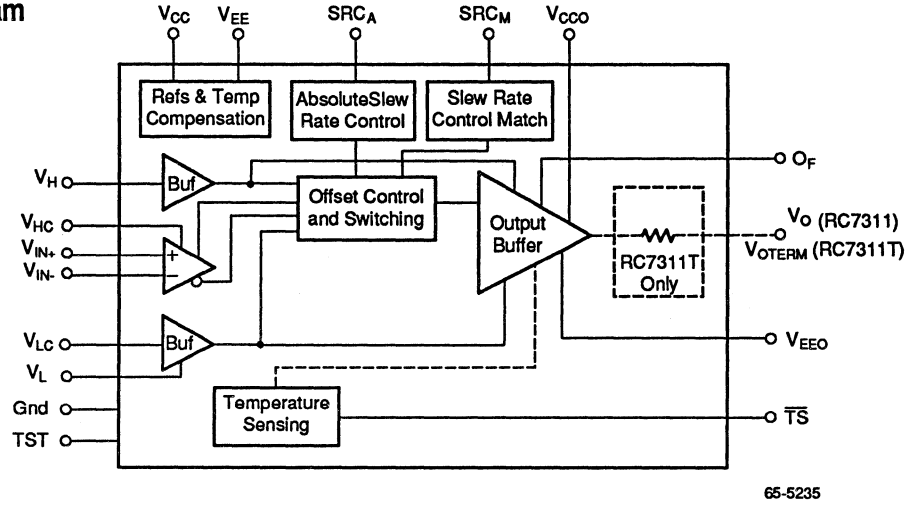
Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Signal Output V_O, V_{OTERM}					
V_{OH}	Range for High Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_{OL}	Range for Low Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
δV_{OH}	Offset to Output High Level	$\delta V_{OH} = \lvert V_H - VOH \rvert$, VH = 0V, VL = -3V $-1.0V \le V_H \le +8V$; V_L = -2V		30	100	mV
δV_{OL}	Offset to Output Low Level	$\delta V_{OL} = \lvert V_L - VOL \rvert$, VH = 8V, VL = 0V $-3V \le VL \le +5.5V$; V_H = +7V		30	100	mV
VTC	Output Voltage Drift	$-3V \le V_L \le +5.5V$, $-1.0V \le V_H \le +8V$		0.1	0.5	mV/°C
ε_G	Gain Error	$-3.0V \le V_L \le +5.5V$, V_H= +8V $-1.0V \le V_H \le +7.5V$, V_L = -3V	-1.0		+1.0	$\%V_{SET}$
ε_L	Linearity Error	$0V \le V_L \le +5V$, V_H= +8V $0V \le V_H \le +5V$, V_L = -3V	-0.3		+0.3	$\%V_{SET}$
		$-3.0V \le V_L \le +5.5V$, V_H= +8V $-1.0V \le V_H \le +7.5V$, V_L = -3V	-0.5		+0.5	$\%V_{SET}$
Z_{OUT}	Output Impedance	V_O (RC7310)		12.6		Ω
I_{AC}	AC Current Drive		70	100		mA
I_{DC}	DC Current Drive		50			mA
	Thermal Shutdown Output (TS)					
V_{OL}	Output Low Level	I_{OL} = 4 mA			0.5	V
I_{CL}	DC Current Limit		70	110	130	mA
TS	Shutdown Die Temperature		115	130	160	°C
	Other					
I_{CC}	Positive Supply Current			60		mA
I_{EE}	Negative Supply Current			60		mA
$PSRV_O$	Output Level to Power Supply	V_{CC}; ΔV_{CC} = ±2.5%	40			dB
	Rejection Ratio	V_{EE}; ΔV_{EE} = ±2.5%	40			dB
$PSRV_{SL}$	Output Slew Rate to Power Supply	V_{CC}; ΔV_{CC} = ±200 mV			4	%
	Rejection Ratio	V_{EE}; ΔV_{EE} = ±200 mV			4	%
T_A	Operating Temperature	Still Air	0	25	50	°C
	Range	Air Flow > 300 lfpm	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line should be back-terminated in 50Ω (±1%) using an external resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 6 pF and resistance no smaller than 10 kΩ.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
SLR	Slew Rate	V_H-V_L = 5V; measured between				
	(SRCM and SRCA	20% and 80% points.				
	Adjusted)	With probe only as load	1.2	1.6		V/ns
		With probe and transmission line	1.1	1.5		V/ns
SLR	Slew Rate	V_H-V_L = 5V; measured between				
	(No SRCM and SRCA	20% and 80% points.				
	Adjustment)	With probe only as load	1.0	1.4		V/ns
		With probe and transmission line	1.0	1.4		V/ns
t_R	Rise Time and	Load is Probe Only				
t_F	Fall Time	Amplitude = 0.8V (20% to 80%)		0.6	0.8	ns
	(SRCM and SRCA	3V (10% to 90%)		1.7	2.0	ns
	Adjusted)	5V (10% to 90%)		2.4	2.9	ns
		9V (10% to 90%)		4. 0	4.8	ns
t_R	Rise Time and	Load is Probe Only				
t_F	Fall Time	Amplitude = 0.8V (20% to 80%)		0.7	1.0	ns
	(No SRCM and SRCA	3V (10% to 90%)		2.0	2.4	ns
	Adjustment)	5V (10% to 90%)		2.8	3.6	ns
		9V (10% to 90%)		4.8		ns
f	Toggle Rate	Amplitude = 0.8V	250	270		MHz
		Amplitude = 5.0V	105	110		MHz
	Propagation Delay					
t_{PLH}	Low to High	f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		1.6	2.0	ns
t_{PHL}	High to Low			1.6	2.0	ns
Δt_P	Matching $\lvert t_{PLH} - t_{PHL} \rvert$			150	175	ps
t_PTC	Temperature Coefficient			2		ps/°C
tPW_{MIN}	Minimum Pulse Width	V_H - V_L = 2.0V; Pulse Width at which amplitude drops by 50 mV, measured between 50% points	2.0			ns
$\Delta t_P PW$	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V	-75		+75	ps
PS	Preshoot	0.5V < $\lvert V_{OH}$-$V_{OL} \rvert$ < 5V		15 mV + 3% of VA		mV
OS	Overshoot	0.5V < $\lvert V_{OH}$-$V_{OL} \rvert$ < 5V		50 mV + 4% of VA		mV
t_S	Output Settling Time	$\lvert V_{OH}$-$V_{OL} \rvert$ = 5V;				
		To Within 3% of $\lvert V_{OH}$-$V_{OL} \rvert$		5		ns
		To Within 1% of $\lvert V_{OH}$-$V_{OL} \rvert$		10		ns

Block Diagram



RC7311
250 MHz ATE Pin Electronics Driver

Features

- High output slew rate (1.8 V/ns typical)
- Wide output voltage range (-3.0V to +8V), and up to 10 Vp-p swings
- 250 MHz minimum operation for ECL swings
- Wide input common mode range for ease of interface to ECL as well as TTL and CMOS
- Output short-circuit protection with current limiter and thermal shutdown
- 100 mA dynamic switching current drive
- Absolute slew rate control
- Available in 28-pin PLCC
- Low output voltage offset (30 mV) and output offset drift (0.1 mV/°C typ.)
- Low input bias current (1 µA typical) and current drift (40 nA/°C) for output level program allows direct coupling to a DAC output.

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Switch driver
- Laser driver
- CRT preamplifier

General Product Description

The RC7311 Pin Electronics Driver is an economical alternative to standard pin electronics drivers in applications that do not require three state capability in the driver. An example of such an application would be the large number of input address pins found in memory testers.

The driver output levels are programmable between -3.0V and +8V to drive ECL, TTL and CMOS logic families. The peak to peak output swing can vary from values lower than 300 mV to values as high as 10V. With toggle rates greater than 250 MHz for ECL signals and typical slew rates of 2 V/ns for 5 Vp-p signal amplitudes, the RC7311 is compatible with the requirements of state-of-the-art testers. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with low offset (30mV) and offset drift (0.1mV/°C typical). The V_H and V_L inputs have been buffered to operate with low bias currents (1.0 µA typical) allowing direct coupling to the output of a DAC.

The RC7311 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a wide voltage range, -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is tied to the appropriate threshold value.

The RC7311 is specified at nominal power supply values of 10V and -5.2V, and commensurate output voltage swing limits of -3.0V and +8V. The supply rails may be raised by 2V to achieve an output high level (V_{OH}) of +10V, or lowered by 2V to achieve an output low level (V_{OL}) of -5V. At all times there must be at least a 2V margin between the positive supply and the maximum value of V_{OH}, and between the negative supply and the minimum value of V_{OL}.

The RC7311 is implemented using Raytheon's high performance precision complementary bipolar process.

Pin Definitions

Name	Function
V_{CC}	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +8V, V_{CC} should be raised 2V above the maximum V_{OH} value. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
V_{EE}	Quiet negative supply. The nominal value is -5.2V to ±5%. For output low voltage levels (V_{OL}) less than -3V, V_{EE} should be lowered 2V below the minimum V_{OL} value. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{CCO}	Positive supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EEO}	Negative supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
GND	Chip ground. These pins should be connected to the printed circuit board's ground plane at the pins.
TST	Pin used for factory testing the thermal characteristics of the device. The pin should be left unconnected or tied to GND.
V_H	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_L	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from V_L to V_{OL} is nominally unity gain.
V_{HC}	Bypass for analog program input high, V_H. V_{HC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_{LC}	Bypass for analog program input low, V_L. V_{LC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_{IN+} V_{IN-}	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs will normally be driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_O	Driver output of RC7311. The output impedance is 12.6Ω±1.5Ω. The output is usually back-terminated in the characteristic impedance of the driven transmission line. For a 50Ω line, a 37.4Ω±1% or better resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short-circuit current of the output.
OF	On chip filter to improve output waveform (optional). This pin connection is optional and should be left unconnected if not used. When used OF pin should be tied to the termination node that is directly connected to the DUT.
SRCA	Absolute slew rate control. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin affects both positive and negative edge rates. If this slew rate control is not desired this pin should be left open.
CIM1 CIM2	**Optional**: A 10,000 pF chip capacitor could be placed between CIM1 and CIM2 to improve impedance matching across different voltage swings. With this capacitor, output impedance stays more constant with changes in voltage swings. If not used, leave pins CIM1 and CIM2 open.
SRCM	Slew rate control matching. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin adjusts the match between positive and negative edges . If this slew rate control is not desired this pin should be left open.

Pin Definitions (continued)

Name	Function
$\overline{TS}$	Active low output notifies thermal shutdown has occurred. In the event of a short-circuit or other fault that causes the die temperature to rise between 115°C and 160°C, the thermal shutdown will activate. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wired together and input to a latch to indicate an alarm condition.
NC	No connection.

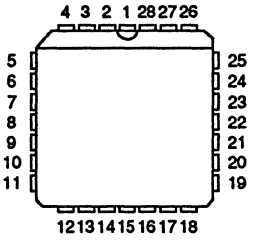
Absolute Maximum Ratings (1)

Positive power supply, V_{CC} 13V
Negative power supply, V_{EE} ..... -8.2V
Difference between V_{CC} and V_{EE} 16V
Input voltage at V_{IN+}, V_{IN-} ..... V_{CC} -12V
V_{EE} +12V
Input voltage at $V_{H, L}$ ..... V_{CC} -13V
V_{EE} +13V
Differential input voltage, $|V_{IN+} - V_{IN-}|$ 6V
Difference between V_H & V_L, $(|V_H - V_L|)$ 13V
Driver output voltage ..... V_{CC} -13V
V_{EE} +13V
Output voltage at TS 7V
Duration of short-circuit to ground ..... Indefinite
Operating temperature range ..... 0°C to 70°C
Storage temperature range ..... -65°C to +125°C
Lead temperature range
(Soldering 10 seconds) ..... 300°C

Notes:
1. "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Connection Information

28-pin PLCC Package
(Top View)



65-5741

Pin	Function	Pin	Function
1	V_O	15	V_{IN+}
2	OF	16	GND
3	CIM1	17	NC
4	CIM2	18	V_H
5	TST	19	V_L
6	NC	20	NC
7	V_{CCO}	21	NC
8	V_{CC}	22	V_{EE}
9	V_{HC}	23	V_{EEO}
10	V_{LC}	24	$\overline{NC}$
11	SRCM	25	TS
12	SRCA	26	NC
13	NC	27	NC
14	V_{IN-}	28	GND

Ordering Information

Part Number	Package	Operating Temperature Range
RC7311QA	QA	0°C to +70°C

Notes:
QA = 28-pin PLCC

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case operating temperature(1)	0		70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	V_{EE} +2V		V_{CC} - 2V	V
$\|V_{OH}$-$V_{OL}\|$	Output amplitude	0.4		10.0	V
R_T	Output back-termination resistor for RC7311		37.4		Ω

Notes
1. With air flow >300 lfpm

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5% T_A = 25°C (still air), no load, unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Differential Inputs V_{IN+}, V_{IN-}					
V_{IN+}, V_{IN-}	Absolute Input Voltage		-2.0		+6.0	V
V_{ID}	Differential Input Range	$\|V_{IN+} - V_{IN-}\|$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Bias Current	-2V≤ $V_{IN\pm}$ ≤ +6V		-100	-250	µA
	Absolute SLR Control, SRCA					
V_{SRCA}	Compliance Voltage Range	V_H = +5V, V_L = 0V	-2.3	-1.6	-0.9	V
I_{SRCA}	Control Current Range		-1.5		+1.5	mA
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = - 2.0		-20		%
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = - 2.4		-40/+25		%
	Matching SLR Control, SRCM					
V_{SRCM}	Compliance Voltage Range	V_H = +5V, V_L = -0V	0.3	0.6	0.9	V
I_{SRCM}	Control Current Range		-0.5		+0.5	mA
$\%_{SLR}$	Max % SLR Matching Change			30		%
	Voltage Program Inputs $V_{H,L}$					
V_H	V_H Range	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_L	V_L Range	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	-1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
V_A	$\|V_{OH} - V_{OL}\|$	Output Voltage Amplitude	0.30		10	V
I_H	Bias Current @ V_H	-1.0V ≤ V_H ≤ +8V; V_L = -3.0V		-1.0	-5.0	µA
I_L	Bias Current @ V_L	-3V ≤ V_L ≤ +5.5V; V_H = +8.0V		-1.0	-5.0	µA
TCI_H	Max Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_A ≤ 70°C; (output not switching)			40	nA/°C
TCI_L	Max Temperature Drift in I_L	V_L = -2.0; 25°C ≤ TC ≤ 70°C (output not switching)			40	nA/°C

DC Electrical Characteristics (continued)

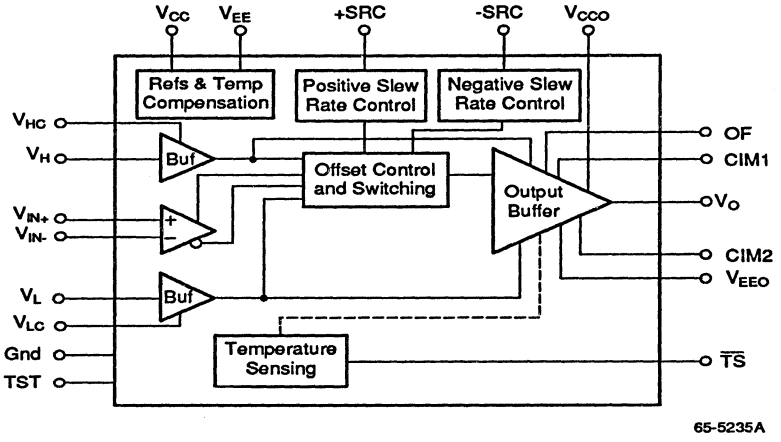
Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
$\Delta IBDC$	Variation in I_H, I_L with Power Supply and DC Voltage at V_H or V_L	V_H= - 1.0V to +8V V_L= -3V to +5.5V	-1.8		+1.8	µA
$V_{H,L}BW$	$V_{H,L}$ BW	-3 dB point from $V_{H,L}BW$ to V_{OUT}		50		kHz
	Signal Output V_O, V_{OTERM}					
V_{OH}	Range for High Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_{OL}	Range for Low Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
δV_{OH}	Offset to Output High Level	$\delta V_{OH} = \lvert V_H - V_{OH}\rvert$, V_H = 0V, VL = -3V -1.0V ≤ V_H ≤ +8V; V_L = -2V		30	50	mV
δV_{OL}	Offset to Output Low Level	$\delta V_{OL} = \lvert V_L$ - VOL$\rvert$, VH = 8V, VL = 0V -3V ≤ V_L ≤ +5.5V; V_H = +7V		30	50	mV
VTC	Output Voltage Drift	-3V ≤ V_L ≤ +5.5V -1.0V ≤ V_H ≤ +8V		0.1	0.5	mV/°C
ε_G	Gain Error	-3.0V ≤ V_L ≤ +5.5V, V_H= +8V -1.0V ≤ V_H ≤ +7.5V, V_L= -3V	-1.0		+1.0	$\%V_{SET}$
ε_L	Linearity Error	0V ≤ V_H ≤ +5V, V_H= +8V 0V ≤ V_H ≤ +5V, V_L= -3V	-0.3		+0.3	$\%V_{SET}$
		-3.0V ≤ V_H ≤ +5.5V, V_H= +8V -1.0V ≤ V_H ≤ +7.5V, V_L= -3V	-0.5		+0.5	$\%V_{SET}$
Z_{OUT}	Output Impedance	V_O (RC7311)		12.6		Ω
I_{AC}	AC Current Drive		70	100		mA
I_{DC}	DC Current Drive		50			mA
	Thermal Shutdown Output (TS)					
V_{OL}	Output Low Level	I_{OL} = 4 mA			0.5	V
I_{CL}	DC Current Limit		70	110	130	mA
TS	Shutdown Die Temperature		115	130	160	°C
	Other					
I_{CC}	Positive Supply Current			60		mA
I_{EE}	Negative Supply Current			60		mA
$PSRV_O$	Output Level to Power Supply Rejection Ratio	V_{CC}; ΔV_{CC} = ±2.5%	40			dB
		V_{EE}; ΔV_{EE} = ±2.5%	40			dB
$PSRV_{SL}$	Output Slew Rate to Power Supply Rejection Ratio	V_{CC}; ΔV_{CC} = ±200 mV			4	%
		V_{EE}; ΔV_{EE} = ±200 mV			4	%
T_A	Operating Temperature Range	Still Air	0	25	50	°C
		Air Flow > 300 lfpm	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line should be back-terminated in 50Ω (±1%) using an external resistor (RC7311). The measurement probe is a high impedance FET probe with capacitance no greater than 6 pF and resistance no smaller than 10 kΩ.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
SLR	Slew Rate (Adjust both SRCM & SRCA)	V_H-V_L = 5V; measured between 20% and 80% points.				
		With probe only as load	1.6	1.8		V/ns
		With probe and transmission line	1.5	1.7		V/ns
SLR	Slew Rate (No SRCM & SRCA Adjustment)	V_H-V_L = 5V; measured between 20% and 80% points.				
		With probe only as load	1.4	1.6		V/ns
		With probe and transmission line	1.35	1.5		V/ns
t_R	Rise Time and	Load is Probe Only				
t_F	Fall Time	Amplitude = 0.8V (20% to 80%)		0.60	0.5	ns
	(SRCM &	3V (10% to 90%)		1.7	1.9	ns
	SRCA Adjusted)	5V (10% to 90%)		2.4	2.8	ns
		9V (10% to 90%)		4. 0	4.5	ns
t_R	Rise Time and	Load is Probe Only				
t_F	Fall Time	Amplitude = 0.8V (20% to 80%)		0.7	0.9	ns
	(No SRCM &	3V (10% to 90%)		1.8	2.2	ns
	SRCA Adjustment)	5V (10% to 90%)		2.6	3.2	ns
		9V (10% to 90%)		4.5	5.2	ns
f	Toggle Rate	Amplitude = 0.8V	250	270		MHz
		Amplitude = 5.0V	105	110		MHz
	Propagation Delay					
t_{PLH}	Low to High	f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		1.6	1.9	ns
t_{PHL}	High to Low		1.6	1.9	ns	
Δt_P	Matching $\lvert t_{PLH} - t_{PHL} \rvert$			150	ps	
t_PTC	Temperature Coefficient			2		ps/°C
tPW_{MIN}	Minimum Pulse Width	V_H - V_L = 2.0V; pulse Width at which amplitude drops by 50 mV, measured between 50% points	2.0			ns
$\Delta t_P PW$	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V	-75		+75	ps
PS	Preshoot	0.5V < $\lvert V_{OH}$-$V_{OL} \rvert$ < 5V			15 mV + 3% of VA	mV
OS	Overshoot	0.5V < $\lvert V_{OH}$-$V_{OL} \rvert$ < 5V			50 mV + 4% of VA	mV
t_S	Output Settling Time	$\lvert V_{OH}$-$V_{OL} \rvert$ = 5V;				
		To Within 3% of $\lvert V_{OH}$-$V_{OL} \rvert$		5		ns
		To Within 1% of $\lvert V_{OH}$-$V_{OL} \rvert$		10		ns

Block Diagram



RC7315/RC7315T
Three-State ATE Pin Electronics Driver

Features

- High output slew rate (1.8 V/ns typical)
- Wide output voltage range (-2.5V to +7V), and up to 9.5 Vp-p swings
- Three-state/high impedance output
- High repetition rate (250 MHz for ECL swings)
- Low output offset (20 mV typ.) and output offset drift (0.1 mV/°C typ.).
- Low leakage (10 nA typ.) and low output capacitance (3 pF typ.) in high impedance inhibit mode
- RC7315TEL is pin-for-pin compatible with AD1322
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (Safe Operating Area protection with current limiting and thermal shutdown)
- 100 mA typ. dynamic current drive capability
- Absolute slew rate control
- Available in 28-pin PLCC, or 16-pin gullwing lead package
- Packaged parts available in unterminated (RC7315) or 50Ω series terminated (RC7315T) configurations

Applications

- ATE Pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Laser driver
- CRT preamplifier

General Product Description

The RC7315 Pin Electronics Driver is designed for use in all high speed ATE systems which require pin drivers with three state capability and high slew rates. The RC7315 has the ability to drive a 50Ω transmission line of up to 2 feet in length with a slew rate of 1.8 V/ns and repetition rate of over 250 MHz for ECL output levels. These features, combined with a maximum output swing of 9.5 Vp-p over the range of -2.5V to +7V, provide this circuit with the ability to test TTL, CMOS, ECL and GaAs devices. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with very low offset drift. The VH and V_L inputs have been buffered to operate with low bias currents (1 μA typical) allowing direct coupling to the output of a DAC.

When the RC7315 is used on an I/O pin, it may be forced into the high impedance state through the INH+ and INH- differential inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin by virtue of low driver output capacitance (3 pF typical) and low output leakage (10 nA typical).

The RC7315 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is tied to the appropriate threshold value. The pin driver is available in unterminated RC7315 or 50Ω series terminated RC7315T configurations. The RC7315TEL is pin-for-pin compatible with the Analog Devices AD1322 driver.

The RC7315 is implemented using Raytheon's high frequency complementary bipolar process.

Pin Definitions

Name	Function
V_{CC}	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +7V, V_{CC} should be raised 3V above the maximum value of V_{OH}. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EE}	Quiet negative supply. The nominal value is -5.2V ±5%. For output low voltage levels (V_{OL}) less than the nominal value of -2.2V, V_{EE} should be lowered 3V below the minimum value of V_{OL}. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should also be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{CCO}	Positive supply for the RC7315 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EEO}	Negative supply for the RC7315 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
CI+	Output stage positive supply decouple for TC7315TEL only. C_{I+} should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
CI+	Output stage negative supply decouple for TC7315TEL only. C_{I-} should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
GND	Chip ground. Should be connected to the printed circuit board's ground plane at the pin.

Name	Function
V_H	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_L	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from V_L to V_{OL} is nominally unity gain.
C_{VOL} C_{VOH}	Bypass capacitor for V_{OH} and V_{OL} respectively. Pins C_{VOL} and C_{VOH} should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
V_{IN+} V_{IN-}	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_O	Driver output on RC7315. The output impedance is 8Ω ±2Ω. The output is usually back terminated in the characteristic impedance of the transmission line it drives. For a 50Ω line, a 40Ω ±1% resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.
V_{OTERM}	Driver output on RC7315T. This version is packaged with an internal back termination resistor. The output impedance is 50Ω ±2.5Ω.
INH+ INH-	Differential digital inputs. When INH is true (i.e. IHN+ > INH-), the driver is forced into the high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
SRCA	Slew rate control for both edges. Slew rate of both rising and falling edges decreases as the control current is changed from 0 mA to -0.5 mA. SRC can be programmed with a current DAC or set to a fixed value using a resistor.

Pin Definitions (continued)

Name	Function
SRCM	Increases the speed of the falling edge to match the rising edge
$\overline{TS}$	Active low output notifies thermal shutdown has occurred. In the event of a short circuit or other fault that causes the die temperature to become excessively large, the thermal shutdown will kick in at a die temperature between 115°C and 160°C. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wire-ORed together and input to a latch to indicate an alarm condition.
NC	No connection.

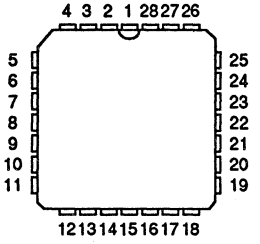
Ordering Information

Part Number	Package	Operating Temperature Range
RC7315QA	QA	0°C to +70°C
RC7315TEL	EL	0°C to +70°C
RC7315TAEL	EL	0°C to +70°C

Notes:
QA = 28-pin PLCC
TEL = 16-pin Gullwing, 50Ω termination (AD1322 pinout)
TAEL = 16-pin Gullwing, 50Ω termination

Connection Information

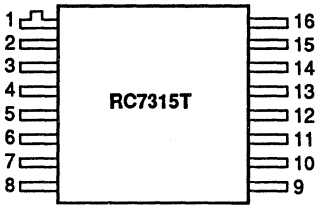
28-pin PLCC
(Top View)



65-5741

Pin	Function	Pin	Function
1	GND	15	TS
2	V_{CC}	16	V_H
3	SRCM	17	C_{VOL}
4	V_{EE}	18	V_{EE}
5	V_{EE}	19	V_{EE}
6	V_{OUT}	20	C_{VOH}
7	SRCA	21	V_{IN-}
8	NC	22	V_{IN+}
9	V_{CCO}	23	INH-
10	V_{EEO}	24	INH+
11	V_{EE}	25	V_{EE}
12	V_{EE}	26	V_{EE}
13	V_L	27	NC
14	NC	28	NC

16-pin Ceramic Leaded Chip Carrier
with Gullwing Leads
(Top View)



65-5313

RC7315TEL

Pin	Function
1	GND
2	NC
3	V_{OTERM}
4	NC
5	C_{I+}
6	C_{I-}
7	V_L
8	DNC*
9	GND
10	V_H
11	V_{IN-}
12	V_{IN+}
13	INH-
14	INH+
15	V_{EE}
16	V_{CC}

RC7315TAEL

Pin	Function
1	GND
2	SRCM
3	V_{OTERM}
4	SRCA
5	DNC*
6	DNC*
7	$\overline{V_L}$
8	TS
9	GND
10	V_H
11	V_{IN-}
12	V_{IN+}
13	INH-
14	INH+
15	V_{EE}
16	V_{CC}

*DNC = Do Not Connect

ATE & Instrumentation

Absolute Maximum Ratings (1)

Positive power supply, V_{CC} 13V
Negative power supply, V_{EE} ..... -8.2V
Difference between V_{CC} and V_{EE} 17V
Input voltage at V_{IN+}, V_{IN-}, INH+, INH- ..... V_{CC} -12V, V_{EE} +12V
Input Voltage at V_H, V_L ..... V_{CC} -13V, V_{EE} +13V
Differential input voltage, $|V_{IN+} - V_{IN-}|$, $|V_{INH+} - V_{INH-}|$ 6V
Difference between V_H & V_L ($|V_H - V_L|$) 11V
Input voltage at SRCA ..... -3V/+7V
Slew rate control current ..... -2.0 mA
Driver Output Voltage ..... V_{CC} -13V, V_{EE} +13V
Output voltage at $\overline{TS}$ 5V
Duration of short-circuit to ground ..... Indefinite
Operating temperature range ..... 0°C to +70°C
Storage temperature range ..... -65°C to +125°C
Lead temperature range
(Soldering 10 seconds) ..... 300°C

Notes:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case operating temperature		25		°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	°C
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	-2		7.0	V
V_{OH}-V_{OL}	Output amplitude	0.3		10.0	V
R_T	Output back-termination resistor (RC7315 only)	38	41	42	Ω

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50 Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using either the internal termination resistor (RC7315T) or an external resistor (RC7315).

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Differential Inputs V_{IN+}, V_{IN-}, V_{INH+}, V_{INH-}					
V_{IN+}, V_{IN-}	Absolute Voltage @ Data Inputs		-2.0		+6.0	V
V_{INH+}, V_{INH-}	Absolute Voltage @ Inhibit Inputs INH+, INH-		-2.0		+6.0	V
V_{ID}	Differential Input Range	$\|V_{IN+} - V_{IN-}\|$	0.4	ECL	5.0	V
V_{DINH}	Differential Inhibit Input Range	$\|V_{INH+} - V_{INH-}\|$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Input Bias Current @ Data Inputs	$-2V \le V_{IN+}, V_{IN-} \le +6V$		-100		µA
I_{INH+}, I_{INH-}	Input Bias Current @ Inhibit Inputs	$-2V \le V_{INH+}, V_{INH-} \le +5V$		-100		µA
	Absolute Slew Rate Control Input SRCA					
V_{SRCA}	Compliance Voltage Range		-2.0		+2.0	V
I_{SRCA}	Control Current Range		-0.5		+0.5	mA
	Matching Slew Rate Control Input SRCM					
V_{SRCM}	Compliance Voltage Range		-2.0		+2.0	V
I_{SRCM}	Control Current Range		-0.5		+0.5	mA
	Voltage Program Inputs V_H, V_L					
V_H	V_H Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+5.0	V
V_L	V_L Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.5		+6.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	-0.5		+8.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.5		+4.0	V
I_H	Bias Current @ V_H	$-1V \le V_H \le +7V$; V_L = -2.0V	-5	-1		µA
I_L	Bias Current @ V_L	$-2V \le V_L \le +5V$; V_H = 6.0V	-5	-1		µA
TCI_H	Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
TCI_L	Temperature Drift in I_L	V_L = -2.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
ΔIBDC	Variation in I_H, I_L with DC voltage at V_H or V_L	$-1V \le V_H \le +7V$ $-2V \le V_L \le +6V$	-1		1	µA
$V_{H,L}BW$	-3 dB bandwidth from V_H or V_L to the output	$-1V \le V_H \le +7V$; $-2V \le V_L \le +6V$; $V_H - V_L$ = 2.0V			50	kHz

DC Electrical Characteristics (cont'd)

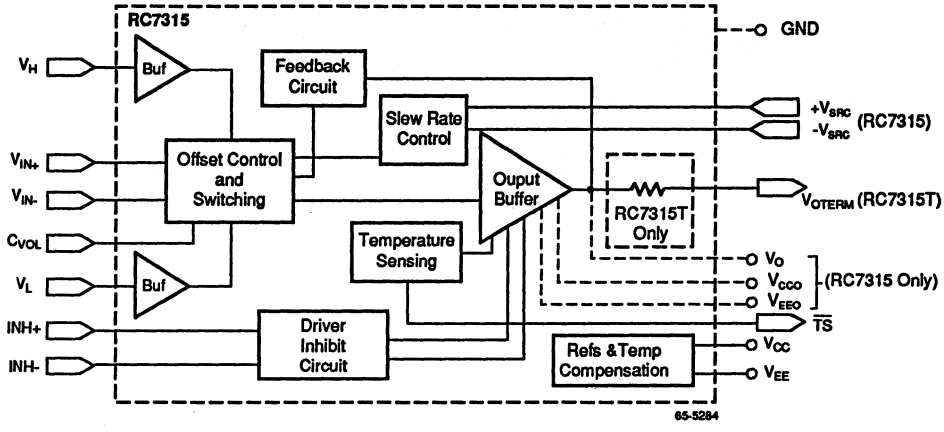
Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Signal Output					
	V_O, V_{OTERM}					
V_O	Output Voltage Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.5		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	-0.5		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.5		+5.0	V
V_A	Amplitude	$\|V_{OH} - V_{OL}\|$	0.3		9.5	V
δV_{OH}	Offset to Output High Level	V_H=0, no load; V_L = -2V		40		mV
		$\delta V_{OH} = \|V_H - V_{OH}\|$				
δV_{OL}	Offset to Output Low Level	V_H=0, no load; V_H = +7V		20		mV
		$\delta V_{OL} = \|V_L - V_{OL}\|$				
VTC	Output Voltage Drift	-1V ≤ V_{OH} ≤ +7V;		0.1		mV/°C
		-2V ≤ V_{OL} ≤ +6V				
ε_G	Gain Error	-1V ≤ V_{OH} ≤ +7V;		1	2	$\%V_{SET}$
		-2V ≤ V_{OL} ≤ +6V				
ε_L	Linearity Error	0 ≤ V_{OUTPUT} ≤ +5V		0.5		$\%V_{SET}$
		-2V ≤ V_{OUTPUT} ≤ +7V		1.0		$\%V_{SET}$
Z_{OUT}	Output Impedance, I_{OUT} 50 mA	V_O (RC7315 only)		8		Ω
		V_{OTERM} (RC7315T only)		47.5		Ω
I_{ZL}	Output Leakage Current in	-1.0V ≤ V_O ≤ +5V			10	nA
	Inhibit Mode	+5.0V ≤ V_O ≤ +7V		0.5	1	µA
I_{DC}	DC Current Drive		50			mA
I_{AC}	AC Current Drive		70	100		mA
	Thermal Shutdown Output (TS)					
I_{CL}	Short Circuit Current Limit		145		mA	
VTS	TS Flag Output Level	I_{OL} = 4 mA			0.5	V
T_{TS}	Shutdown Die Temperature			145	°C	
	Other					
$V_{S\ MAX}$	Maximum Rail to Rail Supply Voltage	V_{CC} - V_{EE}		17		V
V_{CC}	Positive Supply	+8.0	+10.0	+12.0	V	
V_{EE}	Negative Supply	-7.2	-5.2	-3.2	V	
I_{CC}	Positive Supply Current		85		mA	
I_{EE}	Negative Supply Current		90		mA	
$PSRV_O$	Output Level Power Supply	V_{CC}; ΔV_{CC} = ±2.5%	40			dB
	Rejection Ratio	V_{EE}; ΔV_{EE} = ±2.5%	40			dB
$PSRV_{SL}$	Output Slew Rate Power Supply Rejection Ratio @ V_{CC}	V_H = 5V and V_L = 0V; ΔV_{CC} = ±200 mV		4		%
	@V_{EE}	V_H = 5V and V_L = 0V; ΔV_{EE} = ±200 mV		4		%
T_A	Operating Temperature Range	Still Air	0	25	40	°C
		Air Flow > 300 l_{fpm}	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using either the internal termination resistor (RC7315T) or an external resistor (RC7315). The measurement probe is a high impedance FET probe with capacitance no greater than 6 pF and resistance no smaller than 10 kΩ.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
SLR	Slew Rate (Slew rate not adjusted)	V_H - V_L = 5V; Measured between 20% and 80% points.				
		With probe only as load	1.6	1.8		V/ns
		With probe and transmission line	1.5	1.7		V/ns
t_R, t_F	Rise Time, and Fall Time (Slew rate not adjusted)	Load is Probe Only;				
		V_A = 1V (20% to 80%)		0.6		ns
		V_A = 2V (10% to 90%)		1.2		ns
		V_A = 3V (10% to 90%)		1.6		ns
		V_A = 5 V (10% to 90%)		2.5		ns
f	Toggle Rate	Amplitude = 0.8V	300	350		MHz
		Amplitude = 5.0V	150	175		MHz
t_{PLH}	Low to High Propagation Delay	f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		1.6		ns
t_{PHL}	High to Low Propagation Delay	f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		1.4		ns
Δt_P	Propagation Delay Match	$\lvert t_{PLH} - t_{PHL} \rvert$		200		ps
t_PTC	Propagation Delay Temperature Coefficient			2		ps/°C
tPW_{min}	Minimum Pulse Width	V_H - V_L = 2.0V; pulse Width at which amplitude drops by 50 mV, measured between 50% points.			2.0	ns
$\Delta t_P PW$	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		±75		ps
t_{PS}	Preshoot	0.5V < V_A < 5.0V			15 mV + 3% of V_A	
t_{OS}	Overshoot	0.5V < V_A < 5.0V			50 mV + 4% of V_A	
t_S	Output Settling Time	V_A = 5V;				
		To within 3% of V_A		8		ns
		To within 1% of V_A		10		ns
t_{PHZ}	Propagation Delay from Logic High to Inhibit Mode	V_{OH} = 1V; V_{OL} = -1V Load = 100 Ω || 15 pF; Propagation delay is measured to the point at which voltage has changed by 200 mV.		2.9		ns
t_{PLZ}	Propagation Delay from Logic Low to Inhibit Mode			2.9		ns
t_{PZH}	Propagation Delay from Inhibit Mode to Logic High			2.9		ns
t_{PZL}	Propagation Delay from Inhibit Mode to Logic Low			2.9		ns
C_Z	Output capacitance in Inhibit Mode			3		pF

Block Diagram



RC7316
Three-State ATE Pin Electronics Driver

Features

- High output slew rate (3.2 V/ns) typical driving coax
- Wide output voltage range (-3.0V to +7V), and up to 9.5 Vp-p swings
- Three-state/high impedance output
- High repetition rate (550 MHz for ECL swings)
- Low output offset (20 mV typ.) and output offset drift (0.1 mV/°C typ.).
- Low leakage (10 nA typ.) and low output capacitance (3.0 pF typ.) in high impedance inhibit mode
- 100 mA typ. dynamic current drive capability
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (Safe Operating Area protection with current limiting and thermal shutdown)
- Independently adjustable slew rate control available on RC7316QA and RC7316TAEL package versions
- Available in 28-pin PLCC and 16-pin gullwing packages
- RC7316TEL is pin-for-pin compatible with AD1321, AD1322, and AD1324

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Laser driver
- CRT preamplifier

General Product Description

The RC7316 Pin Electronics Driver is designed for use in ultra high speed ATE systems which require pin drivers with three state capability and high slew rates. The RC7316 has the ability to drive a 50Ω transmission line of up to 2 feet in length with a slew rate of 3.2 V/ns and repetition rate of over 550 MHz for ECL output levels. These features, combined with a maximum output swing of 9.5 Vp-p over the range of -3.0V to +7V, provide this circuit with the ability to test TTL, CMOS, ECL and GaAs devices. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with very low offset drift. The V_H and V_L inputs have been buffered to operate with low bias currents (1 µA typical) allowing direct coupling to the output of a DAC.

When the RC7316 is used on an I/O pin, it may be forced into the high impedance state through the INH+ and INH- differential inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin by virtue of low driver output capacitance (3.0 pF typical) and low output leakage (10 nA typical).

The RC7316 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is tied to the appropriate threshold value.

The pin driver is available in unterminated RC7316QA, or 50Ω series terminated RC7316 (TAEL or TEL) configurations. The RC7316TEL is pin-for-pin compatible with Analog Devices' AD1321, AD1322 and AD1324 drivers.

Independent control of the positive and negative slew rates by an external voltage, current or resistors available on RC7316QA and RC7316TAEL package versions. The RC7316QA is packaged in a thermal enhanced 28 PLCC.

The RC7316 is implemented using Raytheon's high frequency BiCMOS process.

Pin Description

Name	Function
V_{CC}	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +7V, V_{CC} should be raised 3V above the maximum value of V_{OH}. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EE}	Quiet negative supply. The nominal value is -5.2V ±5%. For output low voltage levels (V_{OL}) less than the nominal value of -2.5V, V_{EE} should be lowered 3V below the minimum value of V_{OL}. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should also be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{CCO}	Positive supply for the RC7316 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EEO}	Negative supply for the RC7316 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
GND	Chip ground. Should be connected to the printed circuit board's ground plane at the pin.
V_H	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_L	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from V_L to V_{OL} is nominally unity gain.
C_{VOL} C_{VOH}	Bypass capacitor for V_{OH} and V_{OL} respectively. Pins C_{VOL} and C_{VOH} should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
V_{IN+} V_{IN-}	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_O	Driver output on RC7316. The output impedance is 10Ω±2Ω. The output is usually back terminated in the characteristic impedance of the transmission line it drives. For a 50Ω line, a 40Ω±1% resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.
INH+ INH-	Differential digital inputs. When INH is true (i.e. IHN+ > INH-), the driver is forced into the high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
+SRC	Slew rate control for the positive edge. Slew rate of the positive edge changes as the control voltage is changed from -2.0V to +2.0V. +SRC can also be programmed with a current DAC or set to a fixed value using a resistor.
-SRC	Slew Rate Control for the negative edge. Slew rate of the negative edge changes as the control voltage is changed from -2.0V to +2.0V. -SRC can also be programmed with a current DAC or set to a fixed value using a resistor.
TS	Active low output notifies thermal shutdown has occurred. In the event of a short circuit or other fault that causes the die temperature to become excessively large, the thermal shutdown will kick in at a die temperature between 115°C and 160°C. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. TS is an open collector output capable of driving two standard TTL loads. The TS pins of several drivers may be wire-ORed together and input to a latch to indicate an alarm condition.
NC	No connection.

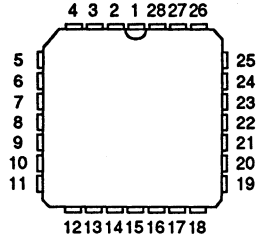
Ordering Information

Part Number	Package	Operating Temperature Range
RC7316QA	QA	0°C to +70°C
RC7316TEL	EL	0°C to +70°C
RC7316TAEL	EL	0°C to +70°C

Notes:
QA = 28-pin PLCC, unterminated
TEL = 16-pin Gullwing, 50Ω termination (AD1322 pinout)
TAEL = 16-pin Gullwing, 50Ω termination

Connection Information

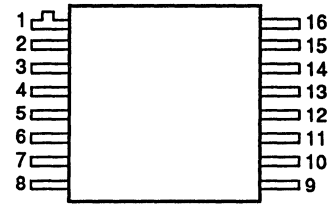
28-pin PLCC
(Top View)



65-5741

Pin	Function	Pin	Function
1	GND	15	$\overline{TS}$
2	V_{CC}	16	V_H
3	-SRC	17	C_{VOL}
4	V_{EE}	18	V_{EE}
5	V_{EE}	19	V_{EE}
6	V_{OUT}	20	C_{VOH}
7	+SRC	21	V_{IN-}
8	NC	22	V_{IN+}
9	V_{CCO}	23	INH-
10	V_{EEO}	24	INH+
11	V_{EE}	25	V_{EE}
12	V_{EE}	26	V_{EE}
13	V_L	27	NC
14	NC	28	NC

16-pin Ceramic Leaded Chip Carrier
with Gullwing Leads
(Top View)



65-5313

RC7315TEL Pin	RC7315TEL Function	RC7315TAEL Pin	RC7315TAEL Function
1	GND	1	GND
2	NC	2	-SRC
3	V_{OTERM}	3	V_{OTERM}
4	NC	4	+SRC
5	C_{I+}	5	DNC*
6	C_{I-}	6	DNC*
7	V_L	7	V_L
8	DNC*	8	$\overline{TS}$
9	GND	9	GND
10	V_H	10	V_H
11	V_{IN-}	11	V_{IN-}
12	V_{IN+}	12	V_{IN+}
13	INH-	13	INH-
14	INH+	14	INH+
15	V_{EE}	15	V_{EE}
16	V_{CC}	16	V_{CC}

*DNC = Do Not Connect NC= No Connection

Absolute Maximum Ratings (1)

Positive power supply, V_{CC} 13V
Negative power supply, V_{EE} ..... -8.2V
Difference between V_{CC} and V_{EE} 16V
Input voltage at V_{IN+}, V_{IN-}, INH+, INH- ..... V_{CC} -12V, V_{EE} +12V
Input Voltage at V_H, V_L ..... V_{CC} -13V, V_{EE} +13V
Differential input voltage, $|V_{IN+} - V_{IN-}|$, $|V_{INH+} - V_{INH-}|$ 6V
Difference between V_H & V_L ($|V_H - V_L|$) 11V
Input voltage at +SRC,-SRC ..... -3V/+7V
Slew rate control current ..... -2.0 mA
Driver Output Voltage ..... V_{CC} -13V, V_{EE} +13V
Output voltage at TS 5V
Duration of short-circuit to ground ..... Indefinite
Operating temperature range ..... 0°C to +70°C
Storage temperature range ..... -65°C to +125°C
Lead temperature range
(Soldering 10 seconds) ..... 300°C

Notes:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case operating temperature	0	25	+70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	°C
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	-3.0		7.0	V
V_{OH}-V_{OL}	Output amplitude	0.1		9.5	V
R_T	Output back-termination resistor (RC7316 only)		41		Ω

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor (RC7316).

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Differential Inputs V_{IN+}, V_{IN-}, V_{INH+}, V_{INH-}					
V_{IN+}, V_{IN-}	Absolute Voltage @ Data Inputs		-2.0		+6.0	V
V_{INH+}	Absolute Voltage @ Inhibit					
V_{INH-}	Inputs INH+, INH-		-2.0		+5.0	V
V_{ID}	Differential Input Range	$\lvert V_{IN+} - V_{IN-} \rvert$	0.4	ECL	5.0	V
V_{DINH}	Differential Inhibit Input Range	$\lvert V_{INH+} - V_{INH-} \rvert$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Input Bias Current @ Data Inputs	$-2V \le V_{IN+}, V_{IN-} \le +6V$		-35	-100	µA
I_{INH+}, I_{INH-}	Input Bias Current @ Inhibit Inputs	$-2V \le V_{INH+}, V_{INH-} \le +5V$		-50	-150	µA
	Positive Edge Slew Rate Control Input +SRC (Available on RC7316QA and RC7316TAEL only)					
V_{+SRC}	Compliance Voltage Range		-2.0V		+2.0	V
	Negative Edge Slew Rate Control Input -SRC (Available on RC7316QA and RC7316TAEL only)					
V_{-SRC}	Compliance Voltage Range		-2.0		+2.0	V
	Voltage Program Inputs V_H, V_L					
V_H	V_H Range	V_{CC} = 10V; V_{EE} = -5.2V	-3.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	-1.0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-5.0		+5.0	V
V_L	V_L Range	V_{CC} = 10V; V_{EE} = -5.2V	-3.0		+6.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	-1.0		+8.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-5.0		+4.0	V
I_H	Bias Current @ V_H	$-1V \le V_H \le +7V$; V_L = -3.0V		1.0	5.0	µA
I_L	Bias Current @ V_L	$-3V \le V_L \le +5V$; V_H = 6.0V		-1.0	-5.0	µA
TCI_H	Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
TCI_L	Temperature Drift in I_L	V_L = -3.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
ΔIBDC	Variation in I_H, I_L with power supply and DC voltage at V_H or V_L	$-1V \le V_H \le +7V$ $-2V \le V_L \le +6V$	-1		1	µA
$V_{H,L}$BW	-3 dB bandwidth from V_H or V_L to the output	$-1V \le V_H \le +7V$; $-2V \le V_L \le +6V$; V_H-V_L = 2.0V			50	kHz

DC Electrical Characteristics (cont'd)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Signal Output V_O, V_{OTERM}					
V_O	Output Voltage Range	V_{CC} = 10V; V_{EE} = -5.2V	-3.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	-1.0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-5.0		+5.0	V
V_A	Amplitude	$\|V_{OH} - V_{OL}\|$	0.1		9.5	V
δV_{OH}	Offset to Output High Level	$-1V \le V_H \le +6V$; V_L = -2V $\delta V_{OH} = \|V_H - V_{OH}\|$		20	40	mV
δV_{OL}	Offset to Output Low Level	$-2V \le V_L \le +6V$; V_H = +7V $\delta V_{OL} = \|V_L - V_{OL}\|$		20	40	mV
VTC	Output Voltage Drift	$-1V \le V_{OH} \le +7V$;		0.1		mV/°C
ε_G	Gain Error	$-2V \le V_{OL} \le +7V$	-1.0	±0.5	+1.0	$\%V_{SET}$
ε_L	Linearity Error	$0V \le V_{OUTPUT} \le +5V$	-0.5	±0.2	+0.5	$\%V_{SET}$
		$-2V \le V_{OUTPUT} \le +7V$	-1.0	±0.6	+1.0	$\%V_{SET}$
Z_{OUT}	Output Impedance		8.0	10	12	Ω
I_{ZL}	Output Leakage Current in Inhibit Mode	$-2.0V \le V_O \le +6.5V$	-10	±1.0	+10	nA
I_{DC}	DC Current Drive		50			mA
I_{AC}	AC Current Drive		70	100		mA
	Thermal Shutdown Output (TS)	**(Open Collector Output)**				
I_{CL}	DC Current Limit		70	110	130	mA
V_{OL}	Output Low Level	I_{OL} = 4 mA			0.5	V
T_{TS}	Shutdown Die Temperature		115	135	160	°C
	Other					
V_S	Rail to Rail Supply Voltage	$V_{CC} - V_{EE}$			17	V
V_{CC}	Positive Supply		+8.0	+10.0	+12.0	V
V_{EE}	Negative Supply		-7.2	-5.2	-3.2	V
I_{CC}	Positive Supply Current		70	95	mA	
I_{EE}	Negative Supply Current		75	95	mA	
$PSRV_O$	Output Level Power Supply	V_{CC}; ΔV_{CC} = ±2.5%	40			dB
	Rejection Ratio	V_{EE}; ΔV_{EE} = ±2.5%	40			dB
$PSRV_{SL}$	Output Slew Rate Power Supply	V_H = 5V |				
	Rejection Ratio @ V_{CC}	and $\|\Delta V_{CC}$ = ±200 mV			4	%
	@ V_{EE}	V_L = 0V $\|\Delta V_{EE}$ = ±200 mV			4	%
T_A	Operating Temperature	Still Air	0	25	50	°C
	Range	Air Flow > 300 l_{fpm}	0	25	75	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using both internal and external termination resistance. The measurement probe is a high impedance FET probe with capacitance no greater than 3 pF and resistance no smaller than 10 kΩ.

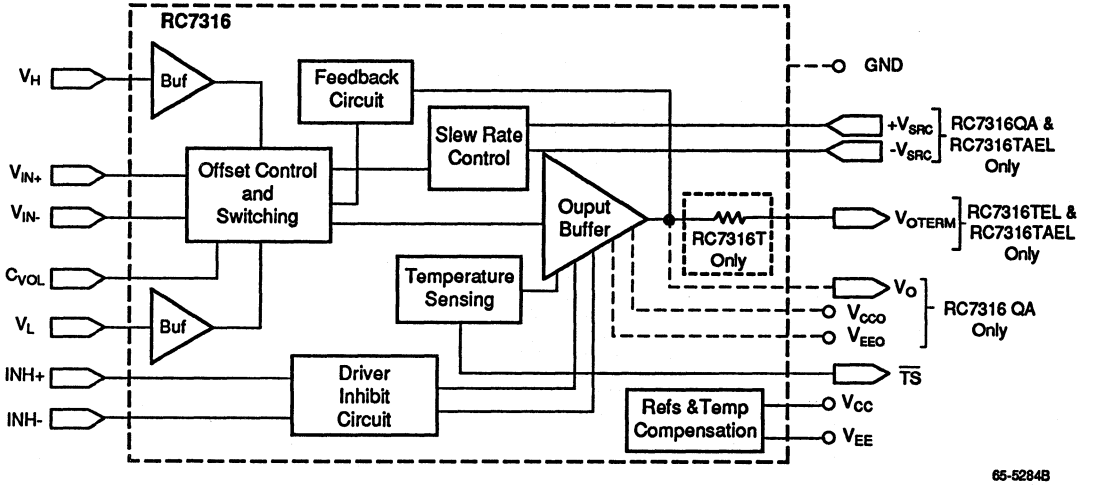
Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
SLR	Slew Rate	V_H - V_L = 5V; Measured between 20% and 80% points.				
		With probe only as load	3.2	3.5		V/ns
		With probe and transmission line	3.0	3.2		V/ns
V+SRC	Positive SLR Control + SRC	RC7316QA & RC7316TAEL				
	Control Voltage Range	VH = +5V, VL = 0V	-2.0		+2.0	V
	Slew Rate Change		0.5		+3.5	V/ns
V-SRC	Negative SLR Control -SRC	RC7316QA & RC7316TAEL				
	Control Voltage Range	VH = +5V, VL = 0V	-2.0		+2.0	V
	Slew Rate Change		0.5		+3.5	V/ns
t_R, t_F	Rise Time, and Fall Time	C_L = 5.0 pF				
		V_A = 0.8V (20% to 80%)		0.5	0.6	ns
		V_A = 3V (10% to 90%)		0.95	1.1	ns
		V_A = 5V (10% to 90%)		1.4	1.6	ns
f	Toggle Rate (Probe only)	Amplitude = 0.8 Vp-p	500	550		MHz
		Amplitude = 3.0 Vp-p	275	300		MHz
		Amplitude = 5.0 Vp-p	200	220		MHz
t_{PHL}	High to Low Propagation Delay	f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		1.8	20	ns
Δt_P	Propagation Delay Match	$\lvert t_{PLH} - t_{PHL} \rvert$		70	100	ps
$t_P TC$	Propagation Delay Temperature Coefficient			2		ps/°C
tPW_{min}	Minimum Pulse Width	V_H - V_L = 2.0V; pulse Width at which amplitude drops by 50 mV, measured between 50% points. C_L = 5.0 pF		1.1	1.2	ns
$\Delta t_P PW$	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		70	100	ps
t_{PS}	Preshoot	0.5V < V_A < 5.0V			15 mV + 3% of V_A	
t_{OS}	Overshoot	0.5V < V_A < 5.0V			50 mV + 4% of V_A	
t_S	Output Settling Time	V_A = 5V;				
		To within 3% of V_A		5.0	7.0	ns
		To within 1% of V_A		10.0	12.0	ns

AC Electrical Characteristics (continued)

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using both internal and external termination resistance. The measurement probe is a high impedance FET probe with capacitance no greater than 3 pF and resistance no smaller than 10 kΩ.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
t_{PHZ}	Propagation Delay from Logic High to Inhibit Mode	VOH = 1V; VOL = -1V Load = 100Ω		1.5	2.0	ns
t_{PLZ}	Propagation Delay from Logic Low to Inhibit Mode	to 2.5V; Propagation delay is measured		2.0	2.5	ns
t_{PZH}	Propagation Delay from Inhibit Mode from Logic High	to the point at which voltage has changed by		2.0	2.5	ns
t_{PZL}	Propagation Delay from Inhibit Mode to Logic Low	200 mV.		2.0	2.5	ns
C_Z	Output capacitance in Inhibit Mode			2.5	3.0	pF

Block Diagram



RC7331/32
Active Load

General Product Description

The RC7331/32 Active Load IC's are designed for use in high speed ATE systems. Both are fully monolithic devices capable of loading the device under test with independently programmable sink and source currents. Independent sink (I_{SINK}) and source (I_{SOURCE}) currents are set by the voltage applied to control inputs VI_{SINK} and VI_{SOURCE}, respectively. The control voltage inputs (VI_{SINK} and VI_{SOURCE}) to output current conversion is 10 mA per volt with R_{SR} and R_{SK} equal to 1 kΩ.

This voltage to current conversion is performed within the RC7331/32 Active Loads and the low bias current required (5.0 µA typ.) allows for the setting of output current levels using a standard voltage output D/A Converter.

The RC7331 and RC7332 Active Loads feature typical linearity error of ±0.1% linearity errors. The transition between the output sink (I_{SINK}) and source (I_{SOURCE}) current is controlled by a wide input range commutation voltage (VCOM) (-3.0V to +7.0V). Switching occurs when the device under test output V_{DUT} slews above or below the programmed V_{COM}.

When the RC7331/32 are used on an ATE pin, they may be forced into a high impedance state through the high speed differential INH+ and INH- inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin of the DUT, by virtue of the low output capacitance (2 pF typ.) and low output leakage current (100 nA typ.).

The INH+ and INH- differential inputs are normally driven by ECL signals. However they have a wide common mode voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS input levels provided that the other input is tied to the appropriate threshold value. The switching speed between I_{OH}, I_{OL} and the inhibit mode is 1.5 ns typ. enabling the RC7331/32 to be compatible with Raytheon's 250 MHz RC7311 and RC7315 Pin Drivers.

The RC7331EL is pin-for-pin compatible with the Analog Devices' AD1315 Active Load. The RC7331QA comes in a thermally enhanced 28 PLCC package.

The RC7332 Active Load is a lower cost version and provides the capability to set maximum I_{SINK} and I_{SOURCE} current with two external resistors, RSR and RSK.

Features

- ±50 mA voltage programmable current (RC7331)
- Independent programmable control of sink and source current values
- ±0.1% Output current resolution, ±1.5% typical gain error, and ±0.1% typical linearity error
- 2 pF typical output capacitance
- Low current leakage in inhibit mode (100 nA)
- Low output current temperature drift 2.0 µA/°C
- Wide commutation voltage range (-3.0V to +7V)
- Fully monolithic device (including Schottky diodes)
- 1.5 ns typical propagation delay
- Operates on -5.2V and +10V supplies
- Inhibit control digital inputs have wide voltage range for ECL, TTL or CMOS compatibility
- RC7331 is available in 16-pin Gullwing, pin-for-pin compatible with Analog Devices' AD1315
- RC7332 is available in 28-pin PLCC thermal enhanced package
- Fast settling time of 12 ns typical at ±50 mA.

Applications

- ATE pin measurement electronics
- Instrumentation

Pin Definitions

Name	Function
V_{CC}	Quiet positive supply. The nominal value is 10V ±5%. V_+ should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EE}	Quiet negative supply. The nominal value is -5.2V ±5%. V_- should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
GND	Device ground. This pin should be connected to the printed circuit board's ground plane at the pins.
VI_{SINK}	Analog DC voltage input which sets the sink current value. VI_{SINK} control voltage to output current conversion is $\frac{10}{R_{SK}}$ A/V (e.g., VI_{SINK} = 5V, I_{OUT} = -50 mA, RSK = 1kΩ).
VI_{SOURCE}	Analog DC voltage input which sets the source current limit. VI_{SOURCE} control voltage to output current conversion is $\frac{10}{R_{SK}}$ A/V (e.g., VISOURCE = 5V, I_{OUT} = 50 mA, RSR = 1kΩ).
V_{COM}	Commutation analog DC voltage input which sets the transition point voltage where switching between forced sink or source current occurs.
INH+ INH-	Differential digital inputs. When INH+ is true (i.e. INH+ > INH-), VDUT input is forced into a high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
I_{SOURCE}	In the inhibit mode the programmed source current is steered to this pin. I_{SOURCE} may be connected to any potential voltage between -3V and +7V. It is typically connected to the V_{COM} programming voltage point. A connection to GND is possible although not recommended in order to keep ground transient currents to a minimum.
I_{SINK}	In the inhibit mode programmed sink current is steered to this pin. I_{SINK} may be connected to any potential voltage between -3V and +7V. It is typically connected to the V_{COM} programming voltage point. A connection to GND is possible although not recommended in order to keep ground transient currents to a minimum.
I_{OUT}	This pin is connected to the DUT.
R_{SR}	This pin is used to connect an external resistor which establishes the I_{SOURCE} maximum current range. It is recommended to use 0.1% or better maximum tolerance resistors to achieve ±2.5% or better accuracy. The other end of this resistor is tied to ground.
R_{SK-} R_{SK+}	This pin is used to connect an external resistor which establishes the I_{SINK} maximum current range. It is recommended to use 0.1% or better maximum tolerance resistors to achieve ±2.5% or better accuracy.
NC	No connect.

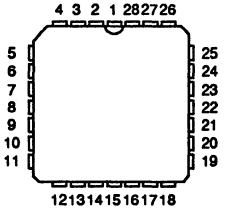
Ordering Information

Part Number	Package	Operating Temperature Range
RC7332QA	QA	0°C to 70°C
RC7331EL	EL	0°C to 70°C

Notes:
QA = 28-pin PLCC
EL = 16-pin Gullwing

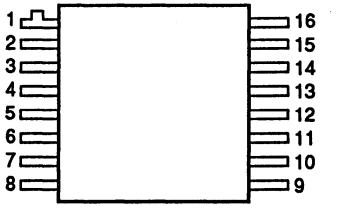
Connection Information

28-pin PLCC
(Top View)



65-5741A

16-pin Ceramic Leaded Chip Carrier
with Gullwing Leads
(Top View)



65-5313

RC7332QA[1]

Pin	Function	Pin	Function
1	GND	15	$\overline{TS}$
2	V_{CC}	16	V_H
3	-SRC	17	C_{VOL}
4	V_{EE}	18	V_{EE}
5	V_{EE}	19	V_{EE}
6	V_{OUT}	20	C_{VOH}
7	+SRC	21	V_{IN-}
8	NC	22	V_{IN+}
9	V_{CCO}	23	INH-
10	V_{EEO}	24	INH+
11	V_{EE}	25	V_{EE}
12	V_{EE}	26	V_{EE}
13	V_L	27	NC
14	NC	28	NC

RC7331EL

Pin	Function
1	I_{SOURCE}
2	V_{COM}
3	I_{OUT}
4	V_{EE}
5	I_{SINK}
6	VI_{SOURCE}
7	GND[2]
8	GND
9	VI_{SINK}
10	NC
11	NC
12	NC
13	VCC
14	INH+
15	INH-
16	NC

Notes:
1. On RC7332QA package, VI_{SINK} input is tied to the other end of the limiting resistor tied to RSK_{LIMIT} pin.
2. Internally connected to package LID and GND.

ATE & Instrumentation

Absolute Maximum Ratings (1)

Positive power supply, V_{CC} 13V
Negative power supply, V_{EE} ..... -11V
Difference between V_{CC} and V_{EE} 18V
VI_{SINK} control voltage 6V
VI_{SOURCE} control voltage 6V
Input voltage at INH+ , INH- ..... -3V to +7V
Differential input voltage, |INH+, INH- ..... 0.4 to +5.5V
Input voltage at V_{COM} ..... -3.5V to +7.5V

Notes:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case operating temperature	0		70	°C
V_{CC}	Positive supply voltage	9.5	10.0	10.5	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{COM}	Commutation input voltage	-3.0	+7.0	V	
VINH+ VINH_	Absolute input voltage	-2.0	+6.0	V	
I_{SOURCE}/I_{SINK}	Sink/ source maximum current (RC7331)			±50	mA
I_{SOURCE}/I_{SINK}	Sink/ source maximum current (RC7332)			±40	mA
R_{OUT}	Load output resistance (VCOM to I_{OUT})			7.0	Ω

DC Electrical Characteristics

V_{CC} = 10V ±5%, V_{EE} = -5.2V ±5%, T_A = 25°C, unless otherwise specified.

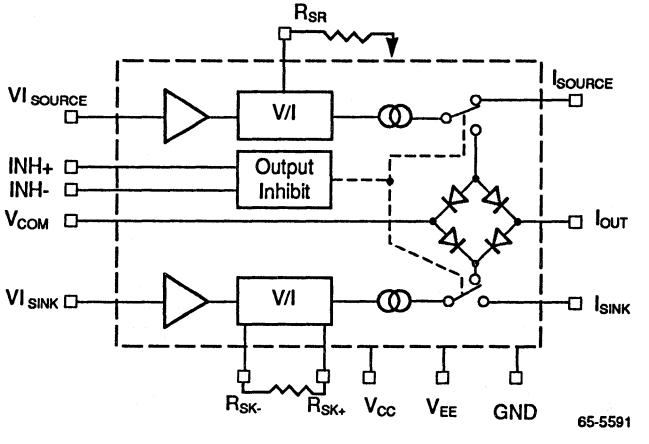
Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	V_{SINK}/V_{SOURCE} Program Inputs					
V_{SOURCE}/ V_{SINK}	Control Voltage Range		0		+5.0	V
I_S	V_{SINK}/V_{SOURCE} Input Bias Current			5.0	10.0	µA
V_{ITC}	Max Temp. Drift in V_{SINK}/V_{SOURCE} Bias Current	(25°C ≤ TA ≤ 70°C)			0.1	µA/°C
	Commutation Voltage Input					
V_{COM}	Control Voltage Range		-3.0		+7.0	V
	Differential Inputs INH+, INH-					
V_{INH+} V_{INH-}	Absolute Input Voltage		-2.0		+6.0	V
V_{ID}	Differential Input Range	| VIN+ - VIN- |	0.4		5.0	V
I_{INH+} I_{INH-}	Bias Current	(-2.0V ≤ VIN± ≤ +6V)	-100	±35	+100	µA
	Load Output Current/Voltage/Resistance					
I_{SINK}	Load Output Sink Current	V_{SINK} = 5V, R_{SK}=1kΩ	-50		0	mA
I_{SOURCE}	Load Output Source Current	V_{SOURCE}= 5V, RSR = 1kΩ	0		+50	mA
V_{OUT}	Load Output Voltage Range		-3.0		+7.0	V
R_{OUT}	Load Output Resistance	(V_{COM} to I_{OUT})		7.0		Ω
	Forcing Current Parameters					
VI_{TF}	Transfer Function (10 mA output per Volt)	R= 1.0K		10		mA/V
ε_L	Linearity Error			±0.1	±0.12	%
ε_G	Gain Error	(V_{DUT} = -3V to +7V)		±1.5	±2.0	%
I_{OS}	Offset Error		-0.5	±0.2	+0.5	mA
ITC	Output Current Drift			2.0	5.0	µA/°C
	Inhibit Mode	(V_{DUT} = -3V to +7V)				
C_Z	Output Capacitance in inhibit mode			2.0	3.0	pF
I_L	Leakage Current		-200	±100	+200	nA
	Other (P_D = 1.53W max)					
I_{CC}	Positive Supply Current	I_{OUT} = 50 mA		+75	+85	mA
I_{EE}	Negative Supply Current	I_{OUT} = - 50 mA		-75	-130	mA
PSSR	Power Supply Rejection Ratio		70	80		dB
	I_{SOURCE} Settling Time (Settled to ±1.0%)	I_{SINK} = + 50 mA V_{COM} = +2.0V Load = 10Ω to GND		12		ns
	I_{SINK} Settling Time (Settled to ±1.0%)	I_{SOURCE} = - 50 mA V_{COM} = - 2.0V Load = 10Ω to GND		12		ns

AC Electrical Characteristics

V_{CC} = 10V ±5%, V_{EE} = -5.2V ±5%, T_A = 25°C.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Propagation Delay					
t_{PD1}	$\pm I_{MAX}$ to INHIBIT	From ECL crossing to IMAX ±10%		1.5	2.5	ns
t_{PD2}	INHIBIT to $\pm I_{MAX}$	From ECL crossing to IMAX ±10%		1.5	2.5	ns
		V_{DUT} = - 2V to 7V				
		C_{DUT} = 10 pF				
		R_{DUT} = 10Ω				

Block Diagram



Notes:
1. RSR and RSK are required only for the RC7332.
2. The RSR, RSK-, and RSK+ pins are not provided on the RC7331. RSR and RSK are 1 K and provided internally.

RC7341/RC7342
High Speed Dual Comparator
2.0 ns Propagation Delay

Description

The RC7341/42 is a very high speed dual comparator with latched input option and ECL compatible outputs capable of driving 50Ω terminated lines. The RC7341 is configured as a windows comparator whereas the RC7342 is configured as two independent comparators and is pin for pin compatible with the industry standard 9687 comparators. The RC7341/42's low propagation delay (2.0 ns maximum), wide input common range (-4V to +8V) and low bias current (±10 µA maximum) makes it ideal to for monitoring outputs from TTL, CMOS, ECL and even GaAs devices in ATE applications.

The propagation delay dispersion is only ±100 ps (typical). The RC7341/42 features a high impedance input mode (I_D) that reduces the bias current to ±50 pA (typical), effectively removing the DC electrical load of the comparator inputs. The RC7341/42 also has a latch function to sample the input waveforms. Latches A and B are controlled by differential latch enable (LEA and LEB) ECL signals.

The RC7341/42 is fabricated using Raytheon's high performance complementary bipolar process.

Features

- 12 V max differential input voltage
- Low propagation delays: 2.0 ns maximum
- Low delay dispersion (±100 ps typical) and drift (4 ps/°C typical)
- ±5 mV maximum input offset and 10 µV/°C max. drift
- ±2 µA typical bias current; ±50 pA typ. in disable mode
- Common mode rejection ≥ 60 dB
- Input disable mode (transparent to user)
- 2 pF maximum input capacitance (RC7341)
- Latch function
- Available with common threshold input $V_{IA/B}$ window comparator (RC7341) or two independent comparators (RC7342)
- RC7342 is pin for pin compatible with 9687 comparators
- Available in 16-pin SOIC, 20-pin PLCC or 16-pin P-DIP

Applications

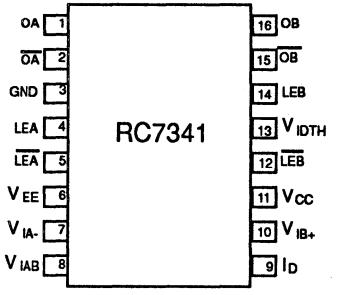
- ATE Pin Electronics
- Threshold/Peak Voltage Detector
- Level Line Receiver
- Limiting Amplifier

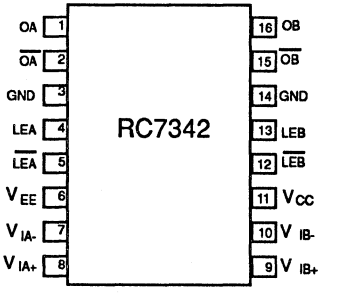
Ordering Information

Part Number	Package	Operating Temperature Range
RC7341PN	PN	0°C to +70°C
RC7341QC	QC	0°C to +70°C
RC7341QCA	QCA	0°C to +70°C
RC7341KM	KM	0°C to +70°C
RC7342PN	PN	0°C to +70°C
RC7342QC	QC	0°C to +70°C
RC7342KM	KM	0°C to +70°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
PN = 16-lead SOIC
QC = 20-lead PLCC
QCA = 28-lead PLCC
KM = 16-lead PDIP

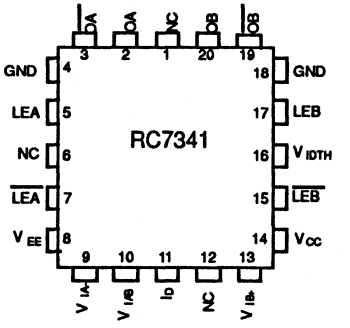
Connection Information for DIP and SO

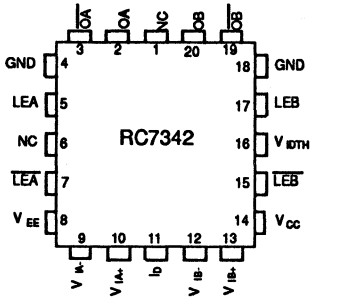


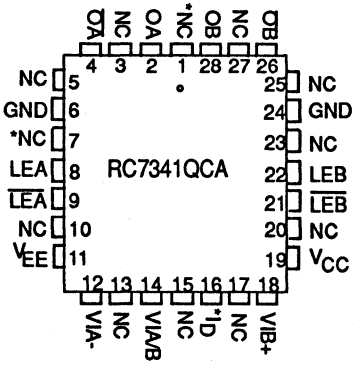


Notes:
1. Input disable mode not available on RC7342 SOIC and P-DIP package.
2. RC7341QCA is pin-for-pin compatible with BT681 except for * pins.

Connection Information for PLCC







Absolute Maximum Ratings(1)

Positive power supply, V_{CC} ..... +12V
Negative power supply, V_{EE} ..... -7V
Difference between V_{CC} and V_{EE} 19V
Input voltage at V_{IA+}, V_{IB+} ..... V_{CC} +0.7V
Input voltage at V_{IA-}, V_{IB-} ..... V_{EE} -0.7V
Differential input voltage |VIA+ - VIA-|, |VIB+ - VIB-|, 16V
Input voltage at LEA, LEB ..... V_{CC}
Input voltage at $\overline{LEA}$, $\overline{LEB}$ ..... V_{EE}
Input voltage at I_{D+}, I_{D-} ..... VCC, VEE
Differential input voltage ..... |LEA - $\overline{LEA}$|, 7V
..... |LEB - $\overline{LEB}$|, 7V
..... |ID - V_{IDTH}|, 7V
Operating temperature range ..... -40°C to +85°C
Storage temperature range ..... -65°C to +125°C
Lead temperature range (solder 10 sec.) ..... 260°C

Notes:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Pin Definitions

Pin No.	Function
V_{CC}	Quiet positive supply. The nominal voltage is 10V ±3%. V_{CC} should be bypassed to ground with a 0.01 µF chip ceramic capacitor placed as close to the pins as possible.
V_{EE}	Quiet negative supply. The nominal voltage is -5.2 ±5%. V_{EE} should be bypassed to ground with a 0.01 µF chip capacitor placed as close to the pins as possible
GND	Chip ground. This pin should be connected to the printed circuit board's ground plane at the pin.
V_{IA+}, V_{IB+} RC7342 ONLY	Differential non-inverting inputs for RC7342 comparators.
V_{IA-}, V_{IB-} RC7342 ONLY	Differential inverting inputs for RC7342 comparators.
V_{IA+}, V_{IB-} RC7341 ONLY	Single ended inputs for RC7341 window comparator.
V_{IAB} RC7341 ONLY	RC7341 window comparator threshold input.
LEA, LEB $\overline{LEA}$, $\overline{LEB}$	Differential digital enable inputs for latches A and B. Although these inputs will be normally driven by ECL signals, they will have a wide enough common mode range that they may be driven by a TTL or CMOS signal provided the other input is tied to the appropriate threshold. If LEA or LEB inputs are tied to a logic high, then latches A and B are transparent and output A or B, will track changes to comparator A or B respectively. A logic low on LEA or LEB will disable the latch, and the outputs will reflect the input state just prior to the latch disable command.
I_D, V_{IDTH}	I_D is the differential non-inverting input and V_{IDTH} is the inverting input for enabling/disabling the comparator. Although the inputs will normally be driven by ECL signals, they have a wide enough common mode range that they may be driven by a TTL or CMOS signal provided the other input is tied to the appropriate threshold. When I_D and V_{IDTH} pins are left open they remain internally biased a +2.5 volt and -1.3 volts respectively and the circuit defaults to a comparator input enable state. A differential voltage of 400 mV must be exceeded to disable the comparator input. The disabled inputs will have a typical bias current of ±50 pA.
OA, $\overline{OA}$	Differential outputs for comparator A.
OB, $\overline{OB}$	Differential outputs for comparator B. Each comparator can drive 50Ω terminated lines to V_{TT}.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case operating temperature	0		70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
R_T	Output termination load resistance	45	50	100	Ω
V_{TT}	Load termination supply voltage	-3.0	-2.0	-2.0	V
V_H	Latch input threshold voltage	-1.25	-1.3	-1.35	V

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Differential Analog Inputs V_{IA+}, V_{IA-}, V_{IB+}, V_{IB-}					
V_{IA+}, V_{IA-}	Absolute Input Voltage		-4.0		+8.0	V
V_{IB+}, V_{IB-}	(Input Common Mode Range)					
V_{IAD}, V_{IBD}	Differential Input Range	$\|V_{IX+} - V_{IX-}\|$			12	V
V_O	Input Voltage Offset			±2	±5	mV
TCV_O	Input Voltage Offset Drift				10	µV/°C
IIX+, IIX-	Input Bias Current [1] (per input)	Enabled Mode, $0 \le V_I \le +5V$		±2	±10	µA
		Enabled Mode, $-2V \le V_I \le +8V$		±2	±10	µA
I_{DIB}	Input Bias Current	Disabled Mode		±50		pA
$I_{BOFFSET}$	Input Bias Current Offset	Enabled Mode		1		µA
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Analog Input Capacitance			1	1.25	pF
$V_{IA/B}$	Analog Input Capacitance			1.5	2	pF
Z_I	Input Impedance			10		MΩ
CMRR	Common Mode Rejection Ratio	-2V to +2V	70	80		dB
	Digital Inputs (Latch & Disable)					
V_{IA+}, V_{IA-}	Absolute Input Voltage		-2.0		+5.0	V
V_{ID}	Differential Range	$\|V_{ID+} - V_{ID-}\|$	0.4	ECL	+5.0	V
I_D	Digital Input Current				20	µA
	Digital Outputs					
V_{OH}	Output Voltage High		-1.0			V
V_{OL}	Output Voltage Low				-1.6	V
	Power Supply					
I_{CC}	Positive Supply Current			25		mA
I_{EE}	Negative Supply Current			45		mA
PSRR	Power Supply Rejection Ratio	V_{CC} ±2.5%, V_{EE} ± 2.5%	60	70		dB

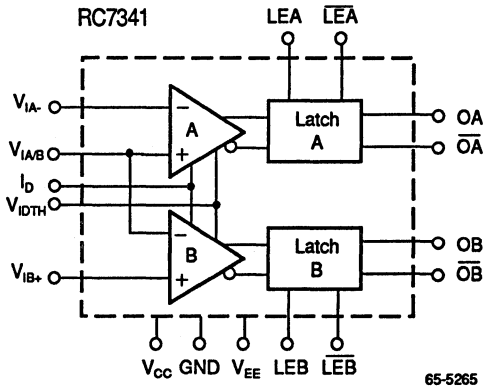
Note 1 Tested at extremes: V_{IN} = -2V, -2V to +3V, 5 Vp-p and V_{IN} = +7V, +2V to +7V, 5 Vp-p
RC7341 window comparator $V_{IA/B}$ input bias current will be 2 times the per input value.

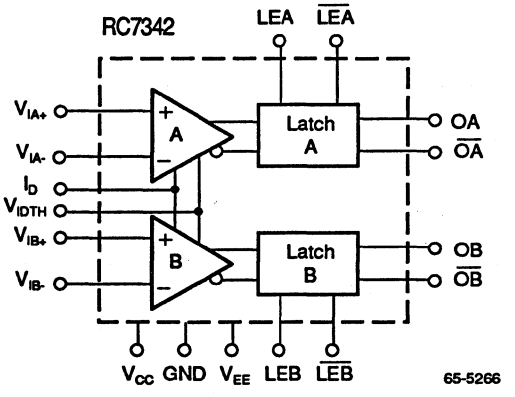
AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
t_{PD}	Propagation Delay H to L and L to H			1.8	2.0	ns
t_S	Delay Slew Between A and B Sides			100	200	ps
t_D	Delay Dispersion	(0.2 V/ns≤ Input slew rate≤ 2.0 V/ns)				
		ECL: V_{TH} = -1V, +0.2V overdrive; V_{TL} = -1.6V, -0.2V underdrive rising and falling edges		±100		ps
		TTL: V_{TH} = 4.5V, +0.5V overdrive; VTL = 0.5V; -0.5V underdrive rising and falling edges		±100		ps
Δt_{PDTC}	Prop. Delay Temp. Drift.			4		ps/°C
Δt_{PDTC}	Delta Prop. Delay with Duty Cycle	0.01% and 99.99% duty cycle 50 kHz, V_{lp-p} = 5V, V_{TH} = 2.5V (10 ns between measurements)		50		ps
tPW_{MIN}	Minimum pulse Width	$0 \le V_S \le 3V$; V_{THA} = 2.8V, V_{THB} = 0.2V; t_{IS} = 2.5 V/ns, $\lvert V_{OH} - V_{OL} \rvert \ge 600\ mV_{p-p}$			1.0	ns
t_S	Data to latch enable set up time		1.0			ns
t_H	Latch enable to data in hold time		TBD			ns
t_{IPD}	Latch enable to output high or low			1.5	2.0	ns
t_{ID}	Active to Inhibit			5.0		ns
t_{IE}	Inhibit to Active			10.0		ns

Block Diagram





RC7351
Parametric Measurement Unit

General Product Description

The RC7351 "Per-Pin" Parametric Measurement Unit (PMU) provides both Forcing Voltage/Measure Current and Forcing Current/Measure Voltage functions. The functions can be selected by applying a TTL input voltage on the SI/V pin. The RC7351 forces voltages between -5V and +15V or currents up to ±40 mA, and measures resulting current or voltage, respectively. The RC7351 circuitry supports four current ranges. Each range is selected by applying TTL input voltage to the RS_1 and RS_2 range select pins. In the Force Voltage/Measure Current mode the force voltage presented to the DUT at I/VF_{OUT} is set by the voltage applied to the I/VF_{IN} pin. The resulting DUT current (I_{DUT}) is converted into a voltage V_R via an external resistor: $V_R = R \times I_{DUT}$, where R is the external resistor (typically ±0.05% maximum tolerance) corresponding to current range A, B, C or D. Resistor tolerance directly affects gain error that usually can be calibrated out. The resulting voltage V_R is sensed by the difference amplifier, multiplied by 4 to increase resolution and then compared against the set upper and lower current limits (I/V_H, I/V_L) of the on-chip window comparator. I/V_H and I/V_L current limits are set by applying a voltage equal to 4 x I x R where R is the external resistor of the selected current range (A, B, C or D) and I is the current limit high (I_H) or current limit low (I_L). The outputs of current high and current low comparators, V_{HS} and V_{LS}, respectively, are open collector outputs and can drive TTL or CMOS inputs depending on the pull up resistor and voltage. The difference amplifier output voltage equal to 4 V_R (4 x R x I_{DUT}) is also provided at the $(I/V)_M$ pin for reading the exact current value via an A/D conversion or for a high/low status using an external window comparator. The full scale measured current for each range is set by corresponding external resistors (R_A, R_B, R_C, R_D) and the ±8V maximum $(I/V)_M$ output range:

$$(I/V)_M = 4V_R = 4 \times I \times R = \pm 8V, \text{ i.e., } I = \frac{\pm 8V}{4R} = \pm \frac{2V}{R}$$

In the Force Current/Measure Voltage mode the force current (IF) present at I/VF_{OUT} is set by applying 4 x R x IF at the I/VF_{IN} input, where R is the external resistor of the selected current range (A, B, C, or D). The values of

Features

- Force voltage/measure current and force current/measure voltage functions
- Forced voltage range (-5V to +15V)
- Four programmable measured current ranges:
  Range A = ±20 µA max
  Range B = ±200 µA max
  Range C = ±1.0 mA max
  Range D = ±40 mA max
- High resolution current force/measure ±0.05%
- Internal control circuitry for selecting ranges.
- High accuracy: 12 bit linearity and 0.5% gain error
- High current range D current limit protection set externally by the value of resistor R_{DIL}
- Measurement output voltage can be disabled
- Forced current ranges:
  Range A = ±20 µA max
  Range B = ±200 µA max
  Range C = ±1.0 mA max
  Range D = ±40 mA max
- Measured voltage range: -5V to +15V
- High resolution voltage measurement (±0.05%) and accuracy: (±10 mV max. offset) and 0.5% gain error.
- Internal current limit for ranges (A, B,& C)
- Available in 28 pin PLCC and 24 pin side brazed ceramic packages.

Applications

- ATE pin electronics measurement
- Instrumentation

internal full scale voltage which is nominally 2V and the output full scale voltage ±8V are related to selected I/VF_{IN} range and power supply values.

The measured voltage is compared against the upper and lower voltage limits (I/V_H,I/V_L) of the on-chip window comparator. The outputs of voltage high and voltage low comparator, V_{HS} and V_{LS}, respectively, are open collector outputs and can drive either TTL or CMOS depending on the pull up resistor and voltage. The resulting DUT voltage when IF is forced is also provided at the $(I/V)_M$ pin for reading the exact value via an A/D converter or for a high/low status using an external window comparator. All three voltage outputs ($(I/V)_M$, V_{HS}, and V_{LS}) can be disabled by applying a TTL voltage on the V_{DIS} pin to allow for a common bus connection between multiple PMUs. V_{HS} and V_{LS} can be wire-ORed. When wire-ORing more than two outputs an external resistor tied to V_{CC} must be added at the input of the circuit driven by the multiple PMUs.

The Force Voltage/Measure Current and Force Current/Measure Voltage modes are selected by applying a TTL input voltage at the SI/V input. All input control pins SI/V, RS_1, RS_2, V_{DIS} can interface with TTL logic levels. The threshold of the control inputs is set at level (VITH = 1.4V)

The RC7351 PMU is fabricated using Raytheon's precision, high voltage process.

Pin Definitions

Pin	Definition
$+V_S$	Quiet positive supply. The nominal value is 20V ±3%. V+ should be bypassed to ground with a 10.0 µF tantalum capacitor placed as close to the pin as possible.
$-V_S$	Quiet negative supply. The nominal value is -10V ±5%. V- should be bypassed to ground with a 10.0 µF tantalum capacitor placed as close to the pins as possible.
V_{EE}	Quiet negative supply for Range D. This pin should be bypassed to ground with a 0.1 µF ceramic capacitor and tied directly to $-V_S$.
GND	Chip ground. This pin should be connected to the printed circuit board's ground plane at the pin.
I/VF_{IN}	I/VF_{IN} input voltage sets the DUT force voltage at I/VF_{OUT} in the Force Voltage/Measure Current mode or sets the DUT Force current at I/VF_{OUT} ($I_F = \frac{I/VF_{IN}}{4R}$) in the Force Current/Measure Voltage Mode.
I/VF_{OUT}	The output voltage/current applied to the Device Under Test (DUT). Forces voltage set on I/VF_{IN} in the Force Voltage/Measure Current mode. Forces a current, I_F, proportional to I/VF_{IN} at the DUT ($I_F = \frac{I/VF_{IN}}{4R}$) in the Force Current/Measure Voltage Mode.
SI/V	A TTL/CMOS signal applied to this pin selects either Force Voltage/Measure Current or Force Current/Measure Voltage mode. A TTL/CMOS low level will select Force Voltage/Measure Current function. A TTL/CMOS high level selects Force Current/Measure Voltage mode.
R_A	Resistor R_A should be placed between pin A and I/VF_{OUT} to set current range A (I_A). R_A tolerance should be better than ±0.05% to improve gain error. Maximum current for a given R_A is $I_A = \frac{2V}{R_A}$. The ±2 volts represents the maximum voltage V_A across R_A since full scale $(I/V)_M = 4 \times V_A = \pm 8V$. For Range A, I_A should not exceed ±20 µA, i.e., R_A should be higher than or equal to 100 kΩ with ±0.1% tolerance. A metal film resistor should be used to reduce inherent resistor noise (schott and popcorn noise) and improve resolution. For

Pin Definitions (continued)

Pin **Definition**

maximum stability, a 300 pF capacitor should be connected across R_A.

R_B Same as A but for current range B (I_B). For Range B, I_B should not exceed ±200 µA, i.e., R_B should be higher than or equal to 10 kΩ with ±0.05% tolerance. For maximum stability, a 1,000 pF capacitor should be connected across R_B.

R_C Same as A but for current range C (I_C). For Range C, I_c should not exceed ±1 mA, i.e., R_C should be higher than or equal to 2 kΩ with ±0.05% tolerance.

R_D Same as A but for current range D (I_D). For Range D, I_D should not exceed ±40 mA, i.e., R_D should be higher than or equal to 50Ω with ±0.05% tolerance

D_1 High current range D output. Two diodes must be connected between D_1 and D_2 as shown in the block diagram.

C+/C- A 30 pF capacitor should be placed between C+ and C- to improve stability.

R_{DIL} Range D output for current limiting. An external resistor is connected between this output pin and D_2 to limit current to a value

$$I_{LIM} = \frac{0.8V}{R_L}$$

RS_1 RS_2 A TTL /CMOS signal applied to these pins selects which current range is activated.

RS_1	RS_2	Range Selected
L	L	A
L	H	B
H	H	C
H	L	D

I/V_H Analog voltage input which sets the upper current/voltage limit measurement threshold. To set desired current limit for current measurement, a voltage equal to 4 x I_H x R must be applied on this pin. R is the external resistor of the selected range (A, B, C, or D). For voltage measurement, the voltage applied to this pin is the limit high voltage.

I/V_L Analog DC voltage input which sets the lower current/voltage limit measurement threshold. To set desired current limit for current measurement, a voltage equalling (4 x I_L x R) must be applied on this pin. R is the external resistor of the selected range (A, B, C, or D). For voltage measurement, the voltage applied to this pin is the limit low voltage.

Pin **Definition**

V_{HS} Output for upper current limit status. If measured current/voltage is less than set upper limit, V_{HS} will be at a logic high state. The V_{HS} output is TTL and CMOS compatible. For wire-ORing multiple PMU's V_{HS} is an open collector output and the multiple PMU wired-ORed line must be pulled up by an external resistor tied to V_{CC} at the input of the driven circuit. The output can be disabled by applying a TTL voltage on the V_{DIS} pin. When disabled the output transistor is turned off and the output voltage is set high by an external resistor tied to V_{CC}. Connect a 3,000 pF capacitor to GND to minimize oscillation at the cross-over point.

V_{LS} Output for upper current limit status. If measured current/voltage is greater than set lower limit, V_{LS} will be at a logic high state. The V_{LS} output is TTL and CMOS compatible. For wire-ORing multiple PMU's V_{LS} is an open collector output and the multiple PMU wired-ORed line must be pulled up by an external resistor tied to V_{CC} at the input of the driven circuit. The output can be disabled by applying a TTL voltage on the V_{DIS} pin. When disabled the output transistor is turned off and the output voltage is set high by an external resistor tied to V_{CC}. Connect a 3,000 pF capacitor to GND to minimize oscillation at the cross-over point.

V_{DIS} V_{HS}, VLS, and $(I/V)_M$ outputs are disabled when a high level TTL signal is applied to this pin. When in disabled state, V_{HS}, V_{LS} and $(I/V)_M$ pins remain in a high impedance state. When V_{DIS} is tied to ground, VHS, V_{LS}, and $(I/V)_M$ are enabled.

$(I/V)_M$ In the Force Voltage/Measure Current mode this output voltage is equal to four times the voltage across external resistor R of selected range A, B, C or D through which the measured current is flowing ($(I/V)_M$ = 4.0 x I_M x R). In the Force Current/Measure Voltage mode this output is equal to the voltage measured. This output can be disabled by applying a TTL voltage on the V_{DIS} pin.

V_D DUT buffered output voltage, I/V F_{out}.

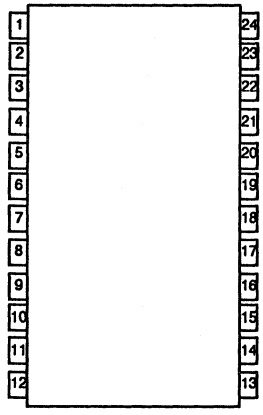
Ordering Information

Part Number	Package	Operating Temperature Range
RC7351QA	QA	0°C to +70°C
RC7351S	S	0°C to +70°C

Notes:
QA = 28-pin PLCC
S = 24-pin Side Brazed Ceramic DIP

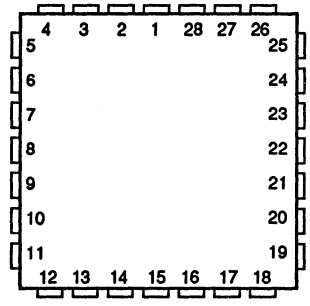
Connection Information

24-pin Side-Brazed Ceramic DIP
(Top View)



Pin	Function	Pin	Function
1	$(I/V)_M$	13	D_2
2	$-V_S$	14	R_{DIL}
3	R_B	15	V_{EE}
4	V_D	16	V/I_H
5	V_{DIS}	17	VH_S
6	R_C	18	C-
7	I/VF_{IN}	19	I/VF_{OUT}
8	D_1	20	GND
9	C+	21	R_A
10	V/I_L	22	RS_1
11	V_{LS}	23	$SI/_V$
12	$+V_S$	24	RS_2

28-pin PLCC
(Top View)



65-5594A

Pin	Function	Pin	Function
1	D_2	15	$(V/I)_M$
2	R_{DIL}	16	$-V_S$
3	V_{EE}	17	NC
4	V/I_H	18	NC
5	V_{HS}	19	R_B
6	C-	20	V_D
7	I/VF_{OUT}	21	V_{DIS}
8	GND	22	R_C
9	R_A	23	I/V_{FIN}
10	NC	24	D_1
11	NC	25	C+
12	RS_1	26	V/I_L
13	SI/V	27	V_{LS}
14	RS_2	28	$+V_S$

Absolute Maximum Ratings (1)

Positive power supply, $+V_S$ 21V
Negative power supply, $-V_S$ ..... -11V
Absolute Difference, |+Vs -(-Vs)| 32V
Digital Control Inputs SIV, RS1, RS2, VDIS ..... -2V/+6V
Comparator Inputs, V_{VH}, V_{VL} ..... $-VS \leq IVH, IVL < +VS$
$V_{VF_{IN}}$ ..... $-V_S \leq IVF_{IN} \leq +V_S$

Notes:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case operating temperature	0		70	°C
V+	Positive supply voltage	10.4	20.0	20.6	V
V-	Negative supply voltage	-9.5	-10.0	-10.5	V
V_{CCO}	Positive supply voltage		5.0	5.5	V
R_A	Resistor for I_A current range	100		100	kΩ
R_B	Resistor for I_B current range	10		100	kΩ
R_C	Resistor for I_C current range	2		100	kΩ
R_D	Resistor for I_D current range	50		100	KΩ

DC Electrical Characteristics

$+V_S$ = 20V ±3%, $-V_S$ = -10V ±5%, T_A = 25°C, and external ±0.05% tolerance resistors R_A = 100 kΩ, RB = 10 kΩ, RC = 2 kΩ, and R_D = 50Ω, unless otherwise specified.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Forced Current/Measure Voltage					
I/VF_{IN}	Input Voltage Range For Setting Forced Current (I_F)	$I/VF_{IN} = 4 \times I_F \times R$	-8		+8	V
$(I/V)_M$	Measured Voltage Output	All ranges, full scale current	-5		+15	V
$(I/V)_M$	$(I/V)_M$ Output Sink/Source Current	$(I/V)_M$= -5V, +15V	-200		+200	µA
V_{MR}	Voltage Measurement Resolution		-0.05	±0.025	+0.05	% FSR
	Voltage Measurement Accuracy					
V_{OS}	Voltage Measurement Offset	I/VF_{IN}= 0V, I/VF_{OUT}= 0V	-6.0	±2	+6.0	mV
V_{GE}	Voltage Gain Error		-1.0	±0.5	+1.0	%
CMRR	CMRR[1]	$-5V \le I/VF_{OUT} \le +15V$		60		dB
	Forced Voltage/Measure Current					
I/VF_{IN}	Force Input Voltage Range	All ranges, full scale current	-5		+15	V
I/VF_{VOS}	Forced Voltage Offset	I/VF_{IN}= 0V, measure I/VF_{OUT} and V_D	-6.0	±2	+6.0	mV
	Forced Voltage Linearity Error			±0.025	±0.05	%
CMRR	CMRR[2]	$-5V \le I/VF_{OUT} \le +15V$		60		dB
I/VF_{OUT}	Forced Output Voltage Range	All ranges, full scale current	-5		+15	V
$(I/V)_M$	Voltage Output Equivalent to Measured	All ranges, full scale voltage				
	Current: $(I/V)_M = 4 \times I_F \times R$		-8		+8	V
$(I/V)_M$	$(I/V)_M$ Output Sink/Source Current	$(I/V)_M$=- 8.0V, +8.0V	-200		+200	µA
	Force Or Measure Current Ranges					
	Range A					
I_A	Maximum Full Scale Current	R_A= 100 kΩ			±20	µA
I_{AMR}	Current Measurement Resolution		-0.05	±0.025	+0.05	%
I_{MA}	Current Measurement Accuracy				%	
I_{LIN}	Linearity[3]		-0.05	±0.025	+0.05	
I_{GE}	Current Gain Error[4]		-10	±0.5	+1.0	%
I_{FIOS}	Force Current Offset[5]	I/VF_{IN}= 0V	-25	±10	+25	nA
I_{MIOS}	Measure Current Offset[6]	I/VF_{IN}= 0V	-25	±10	+25	nA
	Range B					
I_B	Maximum Full Scale Current	R_B= 10 kΩ			±200	µA
I_{BMR}	Current Measurement Resolution		-0.05	±0.025	+0.05	%
I_{BMA}	**Current Measurement Accuracy**					
I_{LIN}	Linearity[3]		-0.05	±0.025	+0.05	
I_{GE}	Current Gain Error[4]		-1.0	±0.5	+1.0	%
I_{FIOS}	Force Current Offset[5]		-250	±100	+250	nA
I_{MIOS}	Measure Current Offset[6]		-250	±100	+250	nA

DC Electrical Characteristics (continued)

$+V_S$ = 20V ±3%, $-V_S$ = -10V ±5%, T_A = 25°C, and external ±0.05% tolerance resistors R_A = 100 kΩ, RB = 10 kΩ, RC = 2 kΩ, and R_D = 50Ω, unless otherwise specified.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Range C	R_C= 2 kΩ				
I_C	Maximum Full Scale Current				±1	mA
I_{CMR}	Current Measurement Resolution		-0.05	±0.025	+0.05	%
I_{CMA}	**Current Measurement Accuracy**					
I_{LIN}	Linearity[3]		-0.05	±0.025	+0.05	%
GE	Current Gain Error[4]		-1.0	±0.5	+1.0	%
I_{FIOS}	Force Current Offset[5]		-1.5	±0.5	+1.5	µA
I_{MIOS}	Measure Current Offset[6]		-1.5	±0.5	+1.5	µA
	Range D	R_B= 50Ω				
I_C	Maximum Full Scale Current				±40	mA
I_{DMR}	Current Measurement Resolution		-0.05	±0.025	+0.05	%
I_{DMA}	**Current Measurement Accuracy**					
I_{LIN}	Linearity[3]		-0.05	±0.025	+0.05	%
I_{GE}	Current Gain Error[4]		-1.0	±0.5	+1.0	%
I_{FIOS}	Force Current Offset[5]		-50	±20	+50	µA
I_{MIOS}	Measure Current Offset[6]		-50	±20	+50	µA
	Digital Control Inputs (SI/V, RS_1, RS_2,)					
V_{IH}	Internal Threshold Voltage		0.8	1.4	2.0	V
I_{LH}	Logic High Bias Current	VH = 2.0V		200		nA
I_{LL}	Logic Low Bias Current	VL = 0.8V		2.0		nA
	Digital Control Input V_{DIS}					
V_{IH}	Internal Threshold Voltage		0.8	1.4	2.0	V
I_{LH}	Logic High Bias Current	VH = 2.0V		1.0		µA
I_{LL}	Logic Low Bias Current	VL = 0.8V		2.0		nA
	Comparator Inputs; I/V_H,I/V_L					
$I/V_{H,L}$	Input Voltage Range		-8.0		+15	V
I_H	Input Bias Current (Logic High)	VH = +15V		0.4		µA
I_L	Input Bias Current (Logic Low)	VL = -8.0V		0.4		µA
	Comparator Status Outputs ;VHS, VLS					
V_{OH}	Output Voltage (Logic High)	R_{PULLUP} = 10 kΩ	3.5			V
V_{OL}	Output Voltage (Logic Low)	$R_{PULLDOWN}$ = 10 kΩ			0.8	V
I_{OH}	Output Current High	V_{OUT} = 5.0V		0.1		µA
I_{OL}	Output Current Low				1.0	mA
I_Z	Output Leakage Current Disabled State	V_{OUT} = 5.0V		0.1		µA
	Other					
I+	Positive Supply Current	no load		4.0		mA
I-	Negative Supply Current	no load		4.0		mA

ATE & Instrumentation

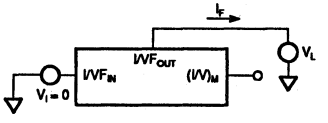
AC Electrical Characteristics

$+V_S$ = 20V ±3%, $-V_S$ = -10V ±5% , T_A = 25°C, and external ±0.05% tolerance resistors R_A = 100 kΩ, RB =10 kΩ, RC = 2 kΩ, and R_D = 50Ω, unless otherwise specified.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Comparator					
t_{HL}	Response Time High to Low	R_{LOAD} = 10 KΩ, 5 mV Overdrive		1.1		µs
t_{LH}	Response Time Low to High	R_{LOAD} = 10 kΩ, 5 mV Overdrive		450		ns
	Differential Amplifier					
t_{MZF}	Response Time (settling time)[7]	Range A		2.4		ms
	Force Current/Measure Voltage	Range B		2.3		
		Range C		2.6		
		Range D		2.6		
		V_M = -5.0V to 15V				
		I_F = Max				
t_{MZF}	Response Time (settling time)	Ranges A		2.4		ms
	Force Voltage/Measure Current	Ranges B		2.5		
		Ranges C		2.6		
		Ranges D		2.7		
		V_F = 5.0V to +15V				
		I_M = Max				
t_{MZF}	Response Time (Settling time)	Ranges A, B, C, & D		0.8	1.0	ms
		V_F = -2.0V to +6.0V				
		C_+ & C_- = 30 pF				
		No Load				
t_{DS}	Output Disable to Enable Time			20		µs

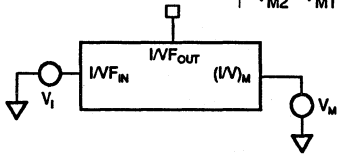
Notes:

1. CMRR is measured with V_{L2} = +15V, V_{L1} = -5, I_{F2} = IF (V_{L2}) $I_{F1} = I_F(V_{L1})$, and $CMRR = 20 \log \left| \frac{V_{L2} - V_{L1}}{R(I_{F2} - I_{F1})} \right|$



65-6362

2. CMRR is measured with V_{I2}= +15V, V_{I1}= -5V, VM2 = VM(VI_2), VM_1 = VM(VI_1), and $CMRR = 20 \log \left| \frac{(V_{I2} - V_{I1}) \times 4}{V_{M2} - V_{M1}} \right|$



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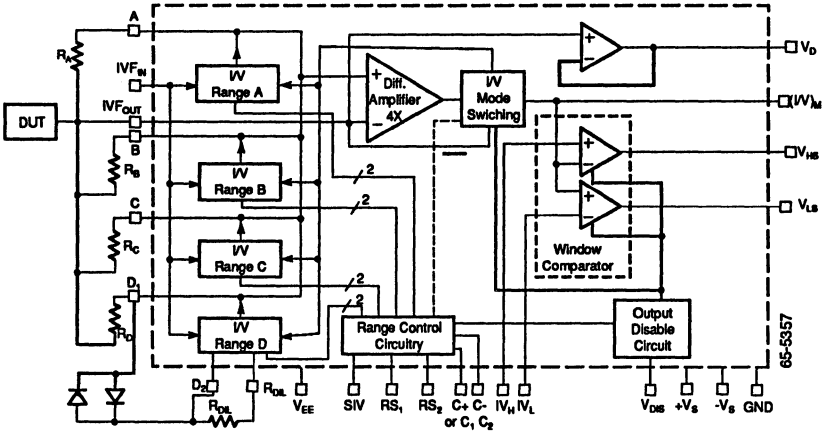
3. Linearity is measured against two point straight line calibration with five measurement points.
4. Current Gain Error is measured with RIL2 = +2V, RIL1 = 2V, VM_2 = VM(IL2), VM1 = (IL_1), and Current Gain Error = $VM_2 - VM_1 R(IL_2 - IL_1)$
5. Forced current offset is measured with I/VF_{IN} = 0V. It is measured at I/VF_{OUT} to ground.
6. Measured current offset is measured with I/VF_{IN}= 0V, $IV/_{FOUT}$ = open. Offset = I/VM where R is R_A, R_B, R_C or R_D.
7. Response Time (settling time) for Force Current/Measure Voltage mode is measured with C+ and C_ = 30 pF, and IV/F_{IN} Voltage Swings from -8.0V to +8.0V, and RL value for Range placed between I/VF_{OUT} and 5V.

500 Ω	A
50 Ω	B
10 kΩ	C
250 Ω	D

Block Diagram



RC73687
High Speed Dual Comparator
2.2 ns Propagation Delay

Product Description

The RC73687 is a very high speed dual comparator with latched input option and ECL compatible outputs capable of driving 50Ω terminated lines. The RC73687 is configured as two independent comparators and is pin for pin compatible with the industry standard 9687 comparators. The RC73687 low propagation delay (2.2 ns maximum), wide input common range (-4V to +8V) and low bias current (±5 µA maximum) makes it ideal to for monitoring outputs from TTL, CMOS, ECL and even GaAs devices in ATE applications. The propagation delay dispersion is only ±80 ps (typical).

The RC73687 features a high impedance input mode (I_D) that reduces the bias current to ±50 pA (typical), effectively removing the DC electrical load of the comparator inputs. The RC73687 also has a latch function to sample the input waveforms. Latches A and B are controlled by differential latch enable (LEA and LEB) ECL signals.

The RC73687 is designed to operate with VCC supply voltages of +5.0V to +10V.

Operation at +10V will provide a wider input common mode voltage range, (-4V to +8V) versus (-4V to +3V). It also provides a lower input capacitance (1.0 pF) versus (1.5 pF)

The RC73687 is fabricated using Raytheon's high performance complementary bipolar process.

Features

- 12 V max differential input voltage (for V_{CC} = +10V, V_{EE} = - 5.2V)
- Low propagation delays: - 1.8 ns typical
- Low delay dispersion (±65 ps typical) and drift (4 ps/°C typical)
- ±5 mV maximum input offset and 10 µV/°C max. drift
- ±3 µA typical bias current; 50 pA typ. in **disable mode**
- Common mode rejection ≥ 70 dB
- Input disable mode (transparent to user)
- Latch function
- RC73687 is pin for pin compatible with 9687 comparators
- Available in 16-pin SOIC, 20-pin PLCC or 16-pin P-DIP

Applications

- ATE Pin Electronics
- Threshold/Peak Voltage Detector
- Level Line Receiver
- Limiting Amplifier

Absolute Maximum Ratings(1)

Positive power supply, V_{CC} ..... +12V
Negative power supply, V_{EE} ..... -7V
Difference between V_{CC} and V_{EE} 19V
Input voltage at V_{IA+}, V_{IB+} ..... V_{CC} +0.7V
Input voltage at V_{IA-}, V_{IB-} ..... V_{EE} -0.7V
Differential input voltage $|V_{IA+} - V_{IA-}|$, $|V_{IB+} - V_{IB-}|$, 16V
Input voltage at LEA, LEB ..... V_{CC}
Input voltage at $\overline{LEA}$, $\overline{LEB}$ ..... V_{EE}
Input voltage at I_{D+}, I_{D-} ..... V_{CC}, V_{EE}
Differential input voltage ..... |LEA - $\overline{LEA}$|, 7V
|LEB - $\overline{LEB}$|, 7V
$|I_D - V_{IDTH}|$, 7V
Operating temperature range ..... -40°C to +85°C
Storage temperature range ..... -65°C to +125°C
Lead temperature range (solder 10 sec.) ..... 260°C

Notes:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

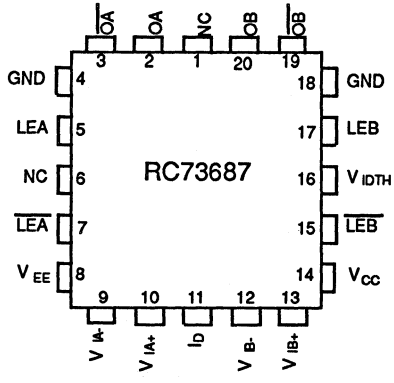
Ordering Information

Part Number	Package	Operating Temperature Range
RC73687PN	PN	0°C to +70°C
RC73687QC	QC	0°C to +70°C
RC73687KM	KM	0°C to +70°C

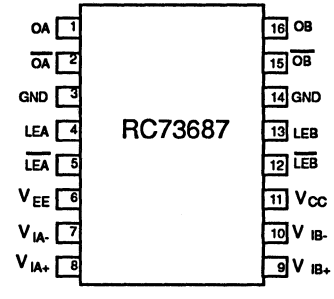
Notes:
PN = 16-lead SOIC
QC = 20-lead PLCC
KM = 16-lead PDIP

Connection Information

PLCC



SO and P-DIP (300 mil wide)



Note: Input disable mode not available on RC73687 SOIC package.

Pin Definitions

Pin No.	Function
V_{CC}	Quiet positive supply. The nominal voltage is 10V ±3%. V_{CC} should be bypassed to ground with a 0.01 µF chip ceramic capacitor placed as close to the pins as possible.
V_{EE}	Quiet negative supply. The nominal voltage is -5.2 ±5%. V_{EE} should be bypassed to ground with a 0.01 µF chip capacitor placed as close to the pins as possible
GND	Chip ground. This pin should be connected to the printed circuit board's ground plane at the pin.
V_{IA+}, V_{IB+}	Differential non-inverting inputs
V_{IA-}, V_{IB-}	Differential inverting inputs
$\overline{LEA}$, LEB LEA, $\overline{LEB}$	Differential digital enable inputs for latches A and B. Although these inputs will be normally driven by ECL signals, they have a wide enough common and that they may be driven by a TTL or CMOS signal provided the other input is tied to the appropriate threshold. If LEA or LEB inputs are tied to a logic high, then latches A and B are transparent and output A or B, will track changes to comparator A or B respectively. A logic low on LEA or LEB will disable the latch, and the outputs will reflect the input state just prior to the latch disable command.
I_D, V_{IDTH}	I_D is the differential non-inverting input and V_{IDTH} is the inverting input for enabling/disabling the comparator. Although the inputs will normally be driven by ECL signals, they have a wide enough common mode range that they may be driven by a TTL or CMOS signal provided the other input is tied to the appropriate threshold. When I_D and V_{IDTH} pins are left open they remain internally biased a +2.5 volt and -1.3 volts respectively and the circuit defaults to a comparator input enable state. A differential voltage of 400 mV must be exceeded to disable the comparator input. The disabled inputs will have a typical bias current of ±50 pA.
OA, $\overline{OA}$	Differential outputs for comparator A.
OB, $\overline{OB}$	Differential outputs for comparator B. Each comparator can drive 50Ω terminated lines to 2 V_{TT}.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case operating temperature	0		70	°C
V_{CC}	Positive supply voltage	4.75	5.0	5.25	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
R_T	Output termination load resistance	45	50	100	Ω
V_{TT}	Load termination supply voltage	-3.0	-2.0	-2.0	V
V_H	Latch input threshold voltage	-1.25	-1.3	-1.35	V

DC Electrical Characteristics (Normal Operating Conditions)

V_{CC} = +5V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C.

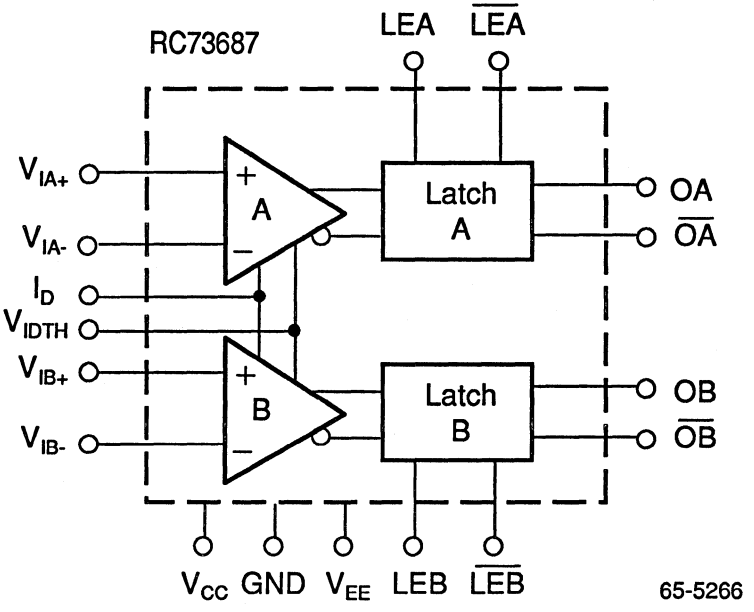
Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Differential Analog Inputs V_{IA+}, V_{IA-}, V_{IB+}, V_{IB-}					
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Absolute Input Voltage (Input Common Mode Range)		-4.0		+3.0	V
V_{IAD}, V_{IBD}	Differential Input Range	$\|V_{IX+} - V_{IX-}\|$			±7.0	V
V_O	Input Voltage Offset			±2	±5	mV
TCV_O	Input Voltage Offset Drift				10	µV/°C
IIX+, IIX- µA	Input Bias Current	Enabled Mode		±5.0	±10	µA
I_{DIB}	Input Bias Current	Disabled Mode		±50		pA
$I_{BOFFSET}$	Input Bias Current Offset	Enabled Mode		1.0		µA
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Analog Input Capacitance			1.0	2.0	pF
Z_I	Input Impedance			500		KΩ
CMRR	Common Mode Rejection Ratio	-2V to +2V	70	80		dB
	Digital Inputs (Latch & Disable)					
V_{IA+}, V_{IA-}	Absolute Input Voltage		-2.0		+5.0	V
V_{ID}	Differential Range	$\|V_{ID+} - V_{ID-}\|$	0.4	ECL	+5.0	V
I_D	Digital Input Current				20	µA
	Digital Outputs					
V_{OH}	Output Voltage High		-1.0			V
V_{OL}	Output Voltage Low				-1.6	V
	Power Supply					
I_{CC}	Positive Supply Current			24		mA
I_{EE}	Negative Supply Current			40		mA
PSRR	Power Supply Rejection Ratio	V_{CC} ±2.5%, V_{EE} ± 2.5%	60	70		dB

AC Electrical Characteristics

V_{CC} = +5.0V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
t_{PD}	Propagation Delay H to L and L to H			1.8	2.2	ns
t_S	Delay Slew Between A and B Sides			100	200	ps
t_D	Delay Dispersion	(0.2 V/ns ≤ Input slew rate ≤ 2.0 V/ns) ECL: V_{TH} = -1V, +0.2V overdrive; V_{TL} = -1.6V, -0.2V underdrive rising and falling edges TTL: V_{TH} = +2.5V, +0.5V overdrive; VTL = 0.5V; -0.5V underdrive rising and falling edges		 ±150 ±150		 ps ps
Δt_{PDTC}	Prop. Delay Temp. Drift			4		ps/°C
Δt_{PDTC}	Delta Prop. Delay with Duty Cycle	0.01% and 99.99% duty cycle 50 kHz, V_{lp-p} = 5V, V_{TH} = 2.5V (10 ns between measurements)		50		ps
tPW_{MIN}	Minimum Pulse Width	$0 \le V_S \le 3V$; V_{THA} = 2.8V, V_{THB} = 0.2V; t_{IS} = 2.5 V/ns, $\lvert V_{OH} - V_{OL} \rvert \ge 600\ mV_{p-p}$			1.0	ns
t_S	Data to latch enable set up time		1.0			ns
t_H	Latch enable to data in hold time		TBD			ns
t_{IPD}	Latch enable to output high or low			1.5	2.0	ns
t_{ID}	Active to Inhibit			5.0		ns
t_{IE}	Inhibit to Active			10.0		ns

Block Diagram



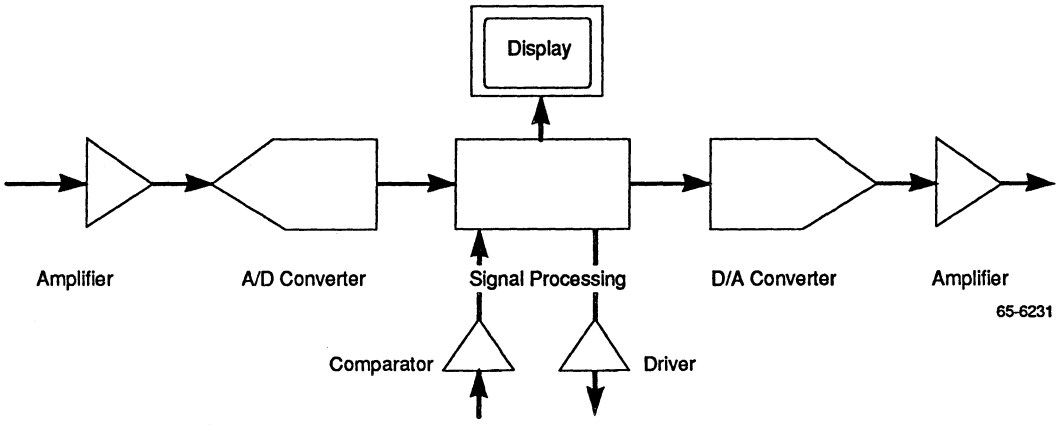
Addendum

DC Electrical Characteristics (High Supply Voltage Conditions)

V_{CC} = +10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Differential Analog Inputs VIA+, VIA-, VIB+, VIB-					
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Absolute Input Voltage (Input Common Mode Range)		-4.0		+8.0	V
V_{IAD}, V_{IBD}	Differential Input Range	$\lvert V_{IX+} - V_{IX-} \rvert$			12	V
V_O	Input Voltage Offset			±3.0	±10	mV
TCV_O	Input Voltage Offset Drift				10	µV/°C
I_{IX+}, I_{IX-}	Input Bias Current	Enabled Mode		±7.0	±15	µA
I_{DIB}	Input Bias Current	Disabled Mode		±50		pA
$I_{BOFFSET}$	Input Bias Current Offset	Enabled Mode		1.0		µA
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Analog Input Capacitance			1.0	2.0	pF
Z_I	Input Impedance			500		K
CMRR	Common Mode Rejection Ratio	-2V to +2V	70	80		dB
	Digital Inputs (Latch & Disable)					
V_{IA+}, V_{IA-}	Absolute Input Voltage		-2.0		+5.0	V
V_{ID}	Differential Range	$\lvert V_{ID+} - V_{ID-} \rvert$	0.4	ECL	+5.0	V
I_D	Digital Input Current				20	µA
	Digital Outputs					
V_{OH}	Output Voltage High		-1.0			V
V_{OL}	Output Voltage Low				1.6	V
	Power Supply					
I_{CC}	Positive Supply Current			24		mA
I_{EE}	Negative Supply Current			40		mA
PSRR	Power Supply Rejection Ratio	V_{CC} ±2.5%, V_{EE} ±2.5%	60	70		dB

Instrumentation Products



Modern instrumentation calls for a wide variety of high-performance signal conditioning, acquisition, processing, and synthesis components. Raytheon offers a wide variety of standard products in all of these categories. Moreover, the ASIC RPA160 tile arrays and RSC4000 Standard Cells enable you to tailor ICs to your system specific requirements. Here are a few highlights from our broad line of products.

In signal conditioning our amplifiers and amplifier cells cover the spectrum up to 800 MHz, with very low noise options as well. For acquisition, we have both high-speed A/D converters and blazing fast comparators. If low-power or battery operation is important, look at the TMC1173 3V 10 Msps A/D converter. It's perfect for handheld applications such as digital scopes. Our Parametric Measurement Unit makes it easy to assemble a low-cost DC measure.

Once the signal is acquired, we have the DSP functions to analyze it, from Fast Fourier Transforms (FFTs) to complex digital filters and mixers. If your instrument needs to generate signals, either for output or for demodulation of acquired signals, the TMC2340 is a great digital quadrature oscillator. For analog signal generation, use our Signal Synthesis DACs, followed again by high-performance amplifiers. For digital signal generation, use our high-speed, high current Pin Drivers to drive ECL, Positive shifted ECL, TTL or CMOS levels.

Instrumentation Products

Product	Resolution Bits	Conv. Rate[1] (Msps)	RMS/RMS SNR[1] (dB)	Package	Grade[2]	Notes
TDC1035	8	—	—	B7, R3	C, V	Peak digitizer. Digitizes peak value of pulses as narrow as 12 ns.
TDC1038	8	20	45	B6, N6, R3, C3, E1	C, V	Low power version of TDC1048.
TDC1048	8	20	45	B6, N6, C3, E1	C, V, SMD	Industry standard video A/D.
TDC1058	8	20	45	B6, N6, R3, E1	C	New industry standard video A/D. Single +5V power supply. TDC1048 performance equivalent.
TMC1173-10	8	10	45	N2, M7, R3	C	Low power CMOS video A/D with integral Track/
-05	8	5	45	M7, N2, R3	C	Hold. +2.7V to +3.3V power supply.
TMC1175-20	8	20	45	B2, N2, C3, M7, R3	C, V	Low power CMOS video A/D with integral Track/ Hold. Includes D/A
-30	8	30	45	M7, N2, R3	C, V	
-40	8	40	45	M7, N2, R3, E1	C, V	
TDC1049	9	30	48	J0, J3, C1, L1, G8, E1	C, V, SMD	ECL interface
TDC1020	10	20	55	J1, G0, E1	C, V	Monolithic video A/D, TTL interface. ±2V input range.

Notes:
1. Guaranteed. See product specifications for test conditions.
2. A = High reliability, T_C = -55°C to 125°C. C = Commercial, T_A = 0°C to 70°C. V = MIL-STD-883 Compliant, T_C = -55°C to 125°C. SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C.
3. A = High reliability, T_C = -20°C to 95°C.

Product	Clock Rate[1] (MHz)	Frequency Resolution (Hz)	SFDR (dB)	Output	Package	Grade	Notes
Digital Frequency Synthesizers							
TMC2340-1	25	0.006	106	Dual 16 Bit	G1, H5, L5	C, V	AM, FM, PM inputs.
	20	0.006	106	Dual 16 Bit	G1, H5, L5	C, V	Quadrature outputs.

Pin Drivers	Slew Rate	Voltage Range	Output Swing (p-p)	Output Three State	Package
RC7310	1.2 V/ns	-3.0 to +8V	10 Vp-p	No	28 PLCC
RC7311	2 V/ns	-3.0 to +8.0V	10V	No	28 PLCC, 16 LDCC
RC7315	1.8 V/ns	-2.5 to 7.5V	9.5V	Yes	28 EPLCC
RC7316	3.2 V/ns	-3.0 to 7.0V	9.5V	Yes	28 EPLCC, 16 LDCC

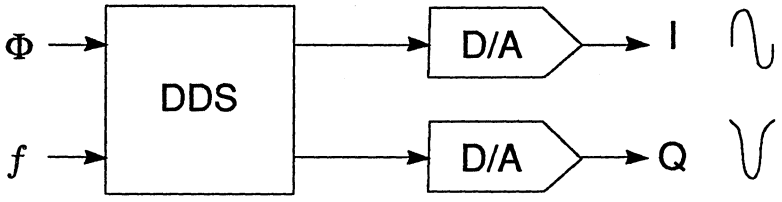
Comparators	Propagation Delay	Voltage Range	Input Bias Current	Input Capacitance	Package
RC7341 (Window)	2.0 ns	-4V to +8V	10 µA (over -4 to +8V)	2 pF	All are
RC7342 (Dual)	2.0 ns	-4V to +8V	10 µA (over -4 to +8V)	1.25 pF	available in
RC73687 (Dual)	2.2 ns	-4V to +8V	5 µA	2 pF	

Precision Measurement Unit	Force Voltage Range	Force Current Ranges	Force Current Resolution	Accuracy	Package
RC7351	-5V to +15V	(4 Ranges) ±500 nA to ±20 µA ±2 µA to ±200 µA ±10 µA to ±1 mA ±500 µA to ±40 mA	±0.05%	12 bits, 0.5% gain error	28 PLCC

Notes:
1. Both the RC7342 and the RC73687 are pin-for-pin compatible with 9687 standard comparators.

For Applications Information, call (619) 457-1000.
For Technical Literature, call 1-800-722-7074.

Signal Synthesis



65-6223

Direct Digital Frequency Synthesis (DDFS) offers signal flexibility and stability that is unattainable with analog techniques. DDFS is the process whereby the digital samples representing a desired analog signal are computed. These samples are then fed to a D/A converter for the construction of the analog signal. The TMC2340 produces data representing baseband signals up to 12.5 MHz (higher with aliasing or multiplexing techniques) with a 0.006 Hz frequency resolution and can change frequencies cleanly in 25 ns. It produces a pair of 16-bit quadrature outputs.

The synthesizer can produce frequency modulation (FM) or phase modulation (PM) simultaneously with amplitude modulation (AM). It is carefully designed to drive the TDC1012 signal synthesis D/A converter, creating the lowest-distortion digital synthesizer subsystem available today.

Raytheon's new TMC22X9X Digital Video Encoders are complete programmable video waveform synthesizers. Incorporating DDFS to digitally generate a subcarrier, with fully programmable horizontal timing, and three high-precision output D/A converters on board, these encoders are outstanding integrated test signal generators. Built-in colorbars and a modulated ramp are also included.

Signal Synthesis Products

Product	Clock Rate [1] (MHz)	Frequency Resolution (Hz)	SFDR (dB)	Output	Package	Grade	Notes
Digital Frequency Synthesizers							
TMC2340-1	25	0.006	106	Dual 16 Bit	G1, H5, L5	C, V	AM, FM, PM inputs.
-	20	0.006	106	Dual 16 Bit	G1, H5, L5	C, V	Quadrature outputs.

Product	Resolution (bits)	Diff. Lin Error[1] (±%)	Conv. Rate[1] (Msps)	Rise Time[1] (ns)	Package	Grade (2)	Notes
Associated D/A Converters							
TDC1041-1	10	0.048	20	4	R3	C	Low cost 10-bit video D/A TTL interface.
-	10	0.096	20	4	R3	C	
TDC3310	10	0,.096	40	10	N6, R6	C	Single +5V power supply.
TDC1141-1	10	0.048	50	4	R3	C	Low cost 10-bit video D/A
-	10	0.096	50	4	R3	C	ECL interface.
TDC1012-3	12	0.012	20	4	J7, N7, R3	C	Signal synthesis D/A.
-2	12	0.024	20	4	J7, N7, R3	C, V, SMD	70 dBc SFDR. Very low glitch.
-1	12	0.048	20	4	J7, N7, R3	C, V, SMD	Drives 25Ω directly.
-	12	0.048	20	4	J7, N7, R3	C, V	TTL interface.
TDC1112-3	12	0.012	50	4	N7, R3	C	Signal synthesis D/A.. 70 dBc SFDR. Very low glitch.
-2	12	0.024	50	4	J7, N7, R3	C, V, SMD	Drives 25Ω directly. ECL interface.
-1	12	0.048	50	4	J7, N7, R3	C, V, SMD	
-	12	0.048	50	4	J7, N7, R3	C, V	

Product	Description	Size	Clock Rate[1] (MHz)	Power[1] (Watts)	Package	Grade[2]	Notes
Digital Video Generators							
TMC22X9X	Digital Video Encoder	10 bit	30	1.1	R0	C	All-Digital Encoder, RGB/YC_RC_B/Color Index Input. NTSC/PAL Composite and S-Video Output.

Notes:
1. Guaranteed. See product specifications for test conditions.
2. C = Commercial, T_A = 0°C to 70°C. V = MIL-STD-883 compliant, T_C = -55°C to 125°C.
   SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C

TMC2340
Digital Synthesizer
Dual 16-Bit, 25 MOPS

Description

The TMC2340 performs waveform synthesis, modulation, and demodulation. When presented with a TTL clock signal and user-selected 15-bit amplitude and 32-bit phase increment values, the TMC2340 automatically generates quadrature-matched pairs of 16-bit sine and cosine waves in DAC-compatible 16-bit offset binary format. If desired, these waveforms are easily phase or frequency-modulated on-chip, and the amplitude input facilitates gain adjustment or amplitude modulation. Digital output frequencies are restricted only by the Nyquist limit of clock rate/2, with frequency resolution of 0.006 Hz at the guaranteed maximum 25 MHz clock rate.

A new data word pair is available at the output every clock cycle. All input and output data ports are registered, with a user-configurable phase accumulator structure and input clock enables to simplify interfacing. The phase data range over a full 2Π radians. All signals are TTL compatible.

Fabricated in Raytheon Semiconductor's OMICRON-C™ one-micron CMOS process, the TMC2340 operates at the 25 MHz maximum clock rate over the full commercial temperature (0 to 70°C) and supply (4.75 to 5.25V) voltage ranges, and is available in a low-cost 120 pin plastic pin grid array. The MIL-STD-883 version, the TMC2340L5V, is housed in a ceramic chip carrier and is specified over the full extended (-55°C to 125°C) case temperature range.

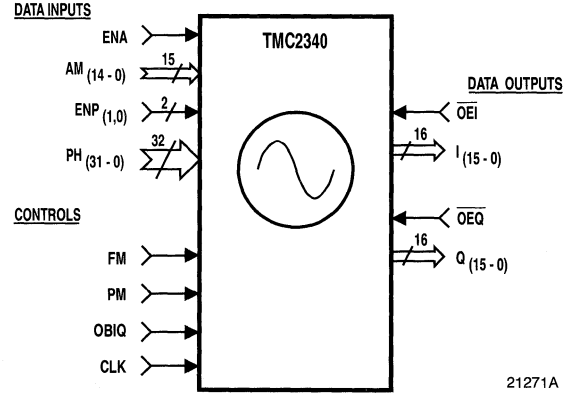
Features

- User-configurable phase accumulator for waveform synthesis, frequency modulation or phase modulation
- Amplitude input for gain adjustment and amplitude modulation
- Guaranteed 25 Msps pipelined data throughput rate
- 15-bit magnitude, 32-bit phase data input precision
- 16-bit offset binary or 15-bit unsigned magnitude output data format
- Input register clock enables simplify interfacing
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 120-pin plastic pin grid array package
- Compliant with MIL-STD-883B in a 132-leaded CERQUAD

Applications

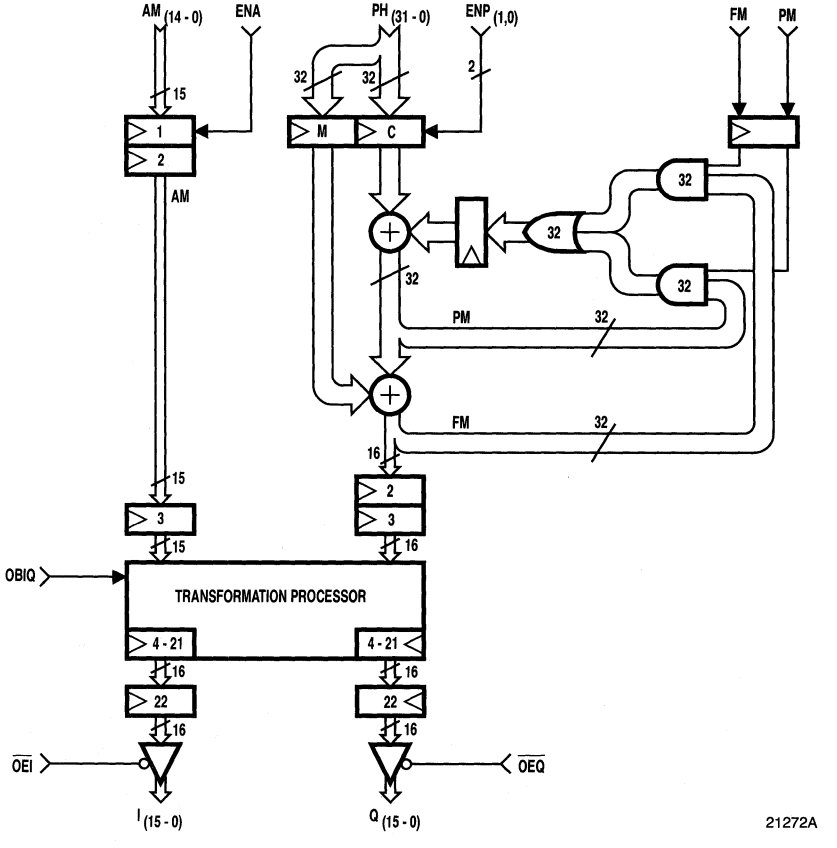
- Digital waveform synthesis, including quadrature functions
- Digital modulation and demodulation

TMC2340 Logic Symbol



Signal Synthesis

Functional Block Diagram



Functional Description

General Information

The TMC2340 converts Polar (Phase and Magnitude) data into Rectangular (Cartesian) format. The first transformed result is available at the outputs 22 clock cycles after startup, with new output data available every 40ns. All input and output data ports are registered, with input clock enables to simplify system bus connections.

The input ports accept 15-bit amplitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words in either 16-bit offset binary or 15-bit unsigned magnitude format. The 32-bit phase accumulator handles high-accuracy (0.006Hz at the maximum clock rate) phase increment values with minimal accumulation error. The flexible input phase accumulator structure supports frequency or phase modulation, as determined by the input register clock enable $ENYP_{1,0}$ and accumulator controls FM and PM. The 16 MSBs (Most Significant Bits) of phase data are used in the transformation itself.

Signal Definitions

Power

V_{DD}, GND — The TMC2340 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK — The TMC2340 operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Inputs/Outputs

AM_{14-0} — AM_{14-0} is the registered peak amplitude 15-bit input data port. AM_{14} is the MSB.

PH_{31-0} — PH_{31-0} is the registered Phase angle increment 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENP_{1,\ 0}$. PH_{31} is the MSB.

I_{15-0} — I_{15-0} is the registered X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OEI}$=HIGH. I_0 is the LSB. I_{15} will be "stuck at" logic HIGH if OBIQ=0.

Q_{15-0} — Q_{15-0} is the registered Cartesian Y-coordinate 16-bit output data port. This output is forced to the high-impedance state when $\overline{OEQ}$=HIGH. Q_0 is the LSB. Q_{15} will remain at logic HIGH if OBIQ=0.

Controls

ENA — Data presented to the input port AM are latched into the input registers on the current clock when ENA is HIGH. When ENA is LOW, the data stored in the register remains unchanged.

$ENP_{1,\ 0}$ — The value presented to the PH input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENP_{1,\ 0}$, as shown below:

$ENP_{1,0}$	Instruction
00	No registers enabled, current data held
01	M register input enabled, C data held
10	C register input enabled, M data held
11	M register set to 0, C register input enabled

where C is the Carrier register and M is the Modulation register, and 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

FM, PM — The user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word FM, PM, as shown below:

FM, PM	Instruction
00	No accumulation performed
01	PM accumulator path enabled
10	FM accumulator path enabled
11	(Nonsensical) logical OR of PM and FM

where 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees.

OBIQ — The format select control sets the numeric format of the Rectangular data: offset binary format when HIGH, and unsigned when LOW. This is a static input. See the *Timing Diagram*.

$\overline{OEI}$, $\overline{OEQ}$ — Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OEX}$ or $\overline{OEY}$ is HIGH, the respective output port is in the high-impedance state.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 9, 21, 37, 45, 53, 67, 87, 91, 99, 112, 120
	GND	Ground	D3, E2, E1, F2, G3, K3, L3, L7, K11, J11, G11, F12, E12, D11, C10, C9, B7, C7, C5, C4	5, 11, 12, 14, 17, 29, 33, 49, 75, 83, 86, 89, 95, 104, 108, 115, 116, 124, 129
Clock	CLK	System Clock	F3	13
Inputs	AM_{14-0}	Radius Data	F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	85, 84, 82, 81, 80, 79, 78, 77, 76, 74, 73, 71, 69, 68, 66
	PH_{31-0}	Phase Data	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	61, 60, 59, 58, 57, 56, 55, 54, 52, 51, 50, 48, 47, 46, 44, 43, 42, 41, 40, 39, 38, 36, 34, 31, 30, 28, 27, 26, 25, 24, 23, 22
Outputs	I_{15-0}	I Data	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	90, 92, 93, 94, 96, 97, 100, 102, 105, 106, 107, 109, 110, 111, 113, 114
	Q_{15-0}	Q Data	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	117, 118, 119, 121, 122, 123, 125, 126, 127, 130, 132, 3, 4, 6, 7, 8
Controls	ENR	Radius In Enable	M11	63
	$ENP_{1,0}$	Phase In Enable	G1, G2	18, 16
	FM, PM	Modulation	H2, H1	20, 19
	OBIQ	Cartesian Data Format	F1	15
	$\overline{OEI}$	I Out Enable	E13	88
	$\overline{OEQ}$	Q Out Enable	D1	10
No Connect	NC	No Connect Pins	–	2, 32, 35, 62, 64, 65, 72, 98, 101, 103, 128, 131
		Index Pin	D4	–

Static Control Input

OBIQ determines the numeric format of the output data: offset binary if HIGH and unsigned magnitude if LOW. This control acts with 2-cycle latency on the chip's 22-cycle data path and is normally hardwired to a system-specific state.

Table 1. Data Input/Output Formats – Integer Format

Port	OBIQ	Bit # 31	30	29	. . .	16	15	14	. . .	0	Format
AM	X							2^{14}	. . .	2^{0}	U
PH	X	$\pm 2^{0}$	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	($\times\pi$) T/U
I	0							2^{14}	. . .	2^{0}	U
I	1						2^{15}	2^{14}	. . .	2^{0}	B
Q	0							2^{14}	. . .	2^{0}	U
Q	1						2^{15}	2^{14}	. . .	2^{0}	B

Notes:

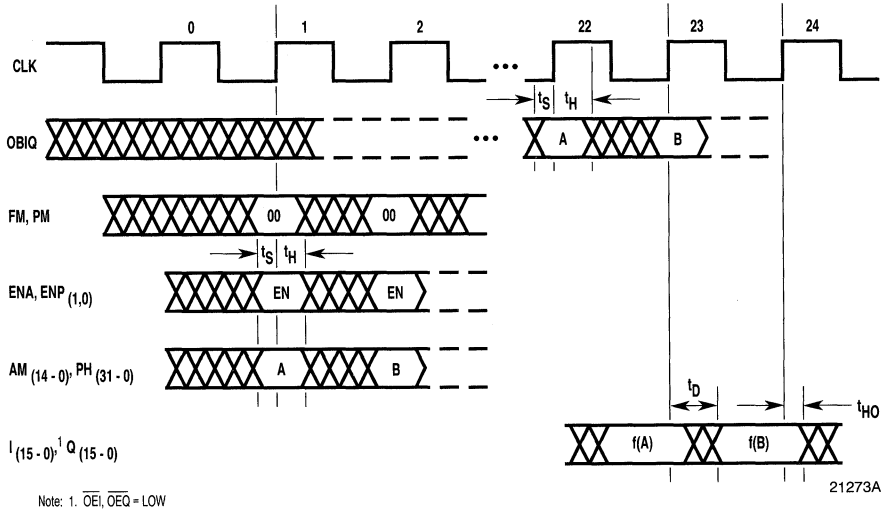
1. $\pm 2^{0}$ denotes two's complement sign or highest magnitude bit - since phase angles are module 2π and phase accumulator is module 2^{32}, this bit may be regarded as $\pm\pi$.
2. All phase angles are in terms of π radians, hence notation "$\times\pi$."
3. A sign-and-magnitude "Q" output is obtained by appending the input bit PH_{31} as a sign bit to the corresponding (i.e., delayed 22 cycles) $Q_{14\text{-}0}$.
4. A sign-and-magnitude "I" output is obtained by appending the exclusive OR of PH_{31} and PH_{30} as a sign bit to the corresponding $I_{14\text{-}0}$.
5. When OBIQ=0, outputs I_{15} and Q_{15} become "do not connects" and will stay logic HIGH. (They may be wired to V_{DD}, left open, or connected to any logic input without damage to the part or excessive power consumption.)
6. Formats:

   T/U = Two's Complement/Unsigned Magnitude 32 Bits
   U = Unsigned Magnitude 15 Bits
   B = Offset Binary 16 Bits

AM, I, Q			PH	
HEX	U	B	T	U
FFFF		32767	$-\pi \cdot 2^{-15}$	$\pi(2-2^{-15})$
– –	– –	– –		
8001		1	$-\pi(1-2^{-15})$	$\pi(1+2^{-15})$
8000		0	$-\pi$	π
7FFF	32767	–1	$\pi(1-2^{-15})$	$\pi(1-2^{-15})$
– –	– –	– –		
0001	1	–32767	$\pi \cdot 2^{-15}$	$\pi \cdot 2^{-15}$
0000	0	–32768	0	0

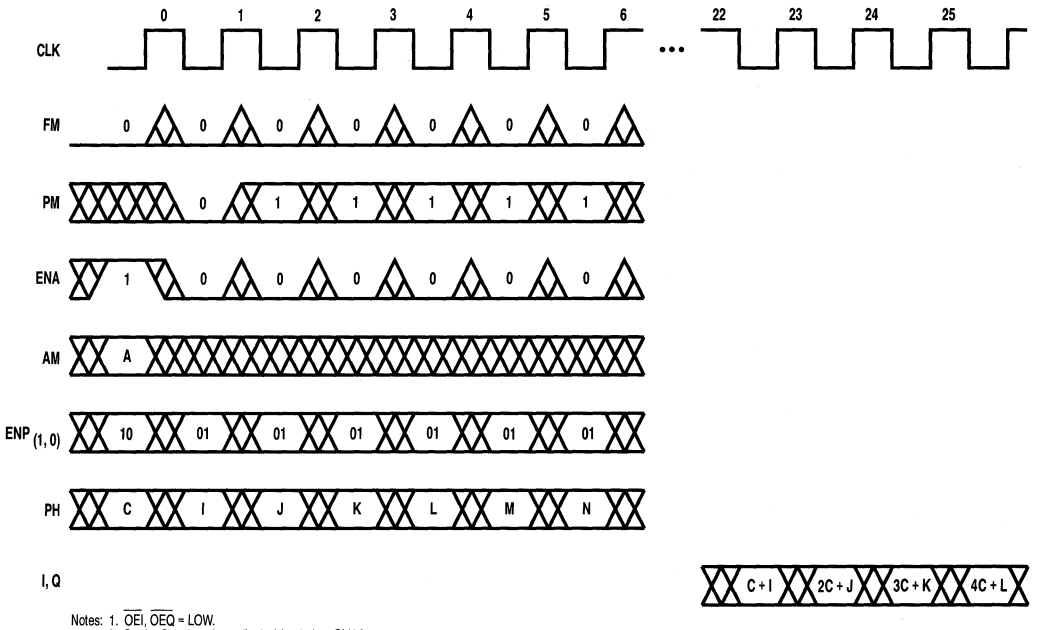
"Hex" column contains the 16 MSBs of the 32-bit phase input (16 LSBs are 0), the 15 bits of the amplitude input or the 16 bits of the offset binary output.

Figure 1. Timing Diagram, Operating Conditions



Note: 1. $\overline{OEI}$, $\overline{OEQ}$ = LOW

Figure 2. Timing Diagram, Phase Modulation



Notes: 1. $\overline{OEI}$, $\overline{OEQ}$ = LOW.
2. Carrier C and peak amplitude A loaded on CLK 0.
3. Modulation values I, J, K, L, . . . loaded on CLK 1, CLK 2, etc.
4. Output corresponding to modulation loaded at CLK i emerged t_{DO} after CLK i + 21.
5. To modulate amplitude, vary AM with ENA = 1.

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Figure 3. Equivalent Input Circuit

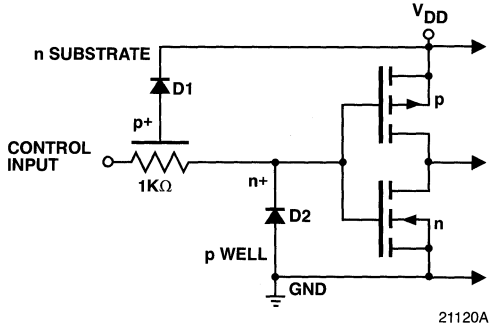

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Figure 4. Equivalent Output Circuit

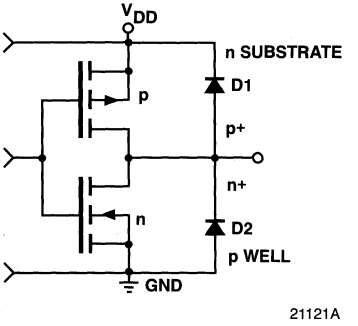

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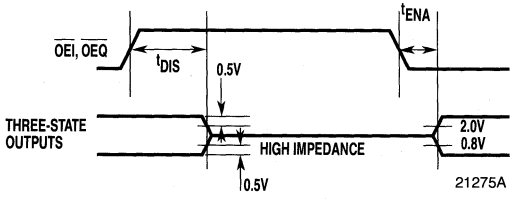
Figure 5. Transition Levels for Three-State Measurements



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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+0.5)V

Output Voltage

Applied voltage ..... −0.5 to (V_{DD}+0.5)V [2]

Forced current ..... −6.0 to 6.0mA [3,4]

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
V_{DD}	Supply Voltage		4.75	5.25	4.5	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8		0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		V
I_{OL}	Output Current, Logic LOW			8.0		8.0	mA
I_{OH}	Output Current, Logic HIGH			-4.0		-4.0	mA
t_{CY}	Cycle Time	V_{DD}=Min		50		55	ns
		TMC2340-1		40		45	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	10		11		ns
		TMC2340-1	8		8		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	8		8		ns
		TMC2340-1	6		6		ns
t_S	Input Setup Time		12		13		ns
		TMC2340-1	10		11		ns
t_H	Input Hold Time		1		2		ns
		TMC2340-1	1		2		ns
T_A	Ambient Temperature, Still Air		0	70			°C
T_C	Case Temperature				-55	125	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz $\overline{OEI}$ and $\overline{OEQ}$ = V_{DD}		160		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.	−20	−100	−20	−100	μA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but specified operation is guaranteed.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		22		25	ns
		TMC2340-1		20		23	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF		4		4	ns
		TMC2340-1		4		4	ns
t_{ENA}	Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF		13		17	ns
		TMC2340-1		12		15	ns
t_{DIS}	Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		14		14	ns
		TMC2340-1		13		13	ns

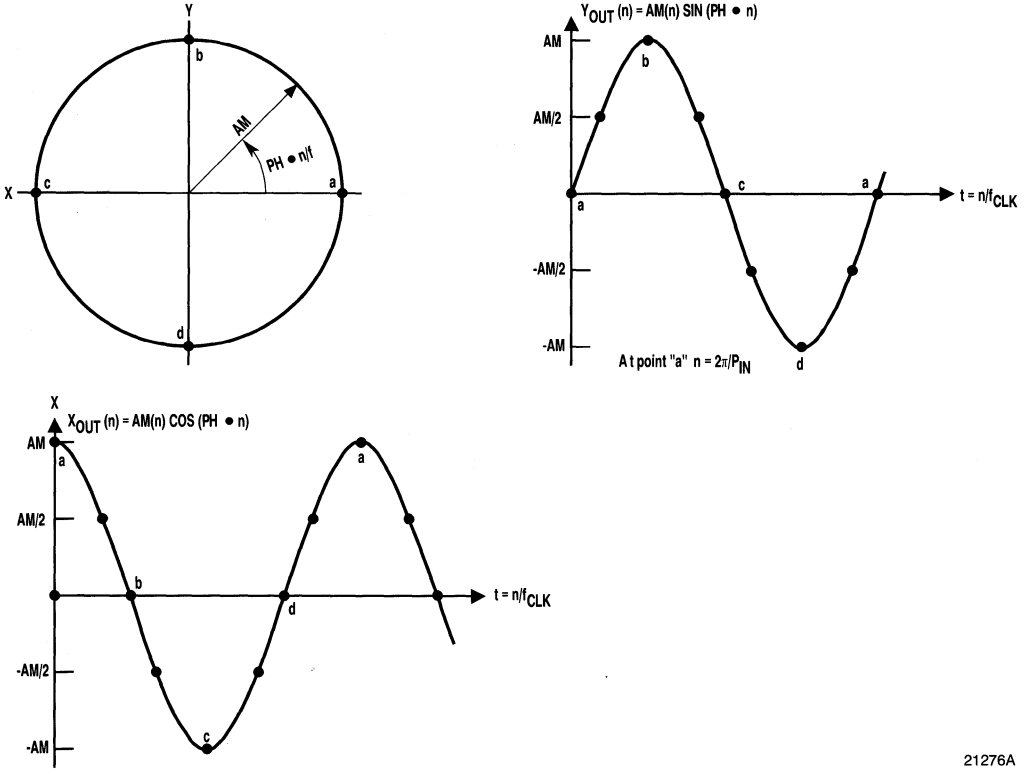
Phase/Amplitude to Sine/Cosine Conversion Geometry

Polar-To-Rectangular Conversion Geometry

The TMC2340 performs a coordinate-space transformation according to the familiar trigonometic relationships shown in *Figure 6*.

With constant amplitude and phase increment values and either FM or PM HIGH, the TMC2340 will output a series of complex number pairs representing the horizontal and vertical projections of a vector rotating about the origin, i.e., a cosine wave and a sine wave.

Figure 6. Input to Output Relationship for Sinusoid Generation



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Digital Waveform Synthesis

Waveform Generation and Modulation

Utilizing the internal phase accumlators in a TMC2340, users can easily generate high-accuracy digital quadrature sinusoidal waveforms with minimal support. The 32-bit data path ensures negligible cumulative error in most applications, and the accuracy of the transform is limited only by the truncation of the result to 16 bits prior to the Transform Processor and the ±1 LSB maximum error of the transform algorithm. Amplitude Modulation is of course performed simply by varying the amplitude input. Either Frequency (phase angle shifted by the cumulative sum of the modulation input) or Phase (phase angle shifted by the instantaneous modulation input) Modulation can be realized by configuring the TMC2340 as shown in *Figures 7 and 8*.

In *Figure 7*, the output valid during clock rising edge m+22 is:

$$I_{m+22} = AM_m \cos(PH_m + mPC)$$
$$Q_{m+22} = AM_m \sin(PH_m + mPC)$$

where PH_m and AM_m are the chip inputs at rising edge m, PC is the (constant) carrier phase increment, $PM_1 = 0$, $PM_{2,...m} = 1$, and $FM_{1\text{-}m} = 0$.

Expressed in terms of time instead of clock cycles,

$$I_{((m+22)/f_{clk})} = AM_m/f_{clk} \cos(PH_m/f_{clk})$$

where f_{clk} is the frequency of the square wave applied to CLK.

Figure 7. Performing Phase Modulation

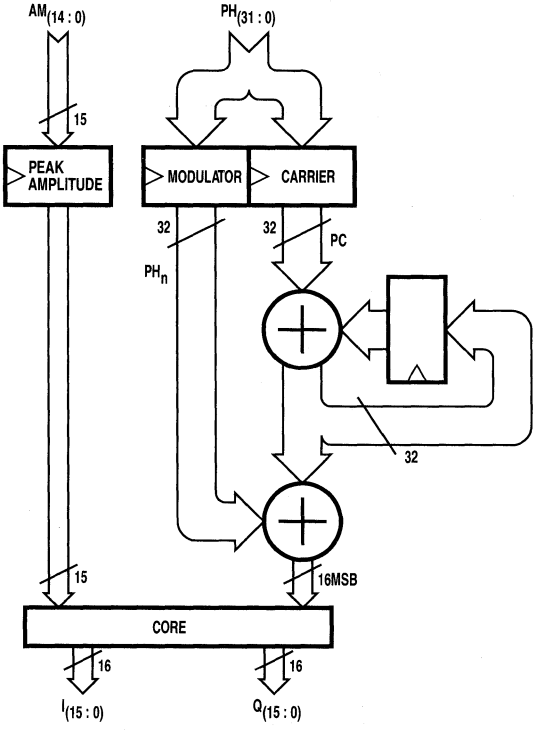

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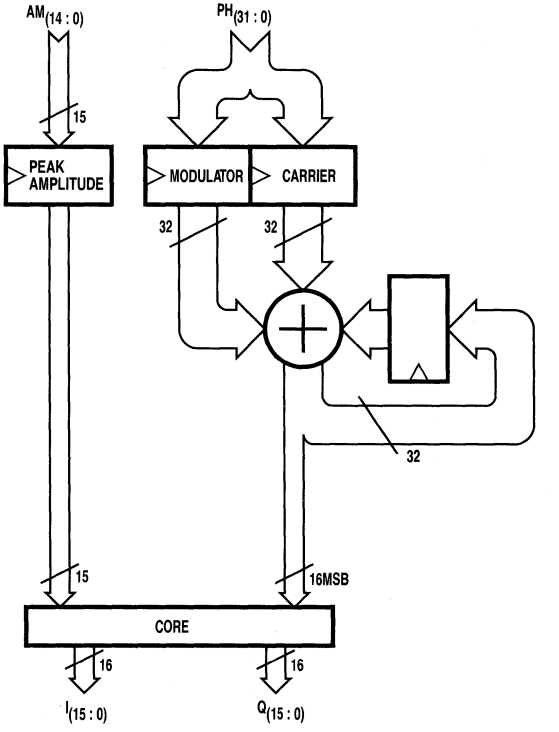
Figure 8. Performing Frequency Modulation



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In *Figure 8*, the output valid during clock rising edge n+22 is:

$$I_{m+22} = AM_m \cos\left(\sum_{m=1}^{n} PH_m + nPC\right)$$

$$Q_{n+22} = AM_m \sin\left(\sum_{m=1}^{n} PH_m + nPC\right)$$

where PH_m and AM_m are the chip inputs at rising edge AM, PC is the (constant) carrier phase increment, $FM_1 = 0$, $FM_{2...n} = 1$, and $PM = 0$.

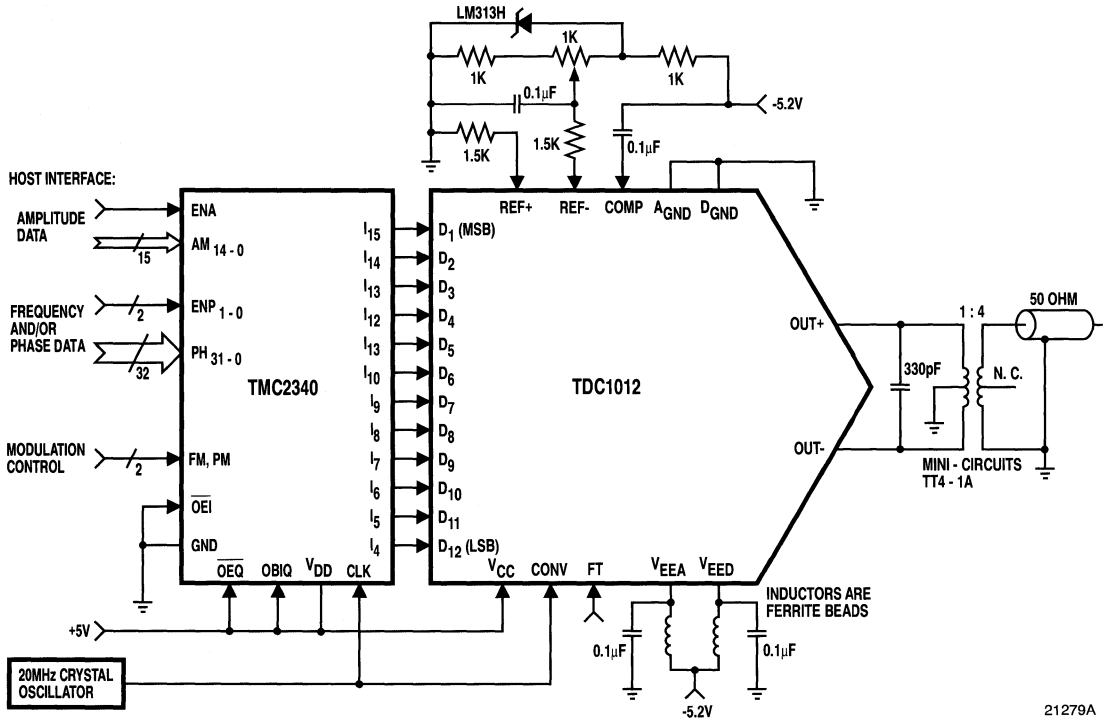
Expressed in terms of time instead of clock cycles,

$$I_{(n+22)/fclk} = AM_{m/fclk} \cos\left(\sum_{m-1}^{n} PH_{m/fclk} + PC \bullet m/fclk\right)$$

Digital Synthesizer with TDC1012 D/A Converter

Connection of the TMC2340 to the TDC1012 D/A converter is straightforward. As shown in *Figure 9*, the TDC1012 data lines are connected to either the I or Q outputs. Both outputs may be used, with two TDC1012's for quadrature synthesis.

Figure 9. Frequency Synthesizer



Note: To use two TDC1012's in quadrature, connect second TDC1012 to Q_{15} (MSB) to Q_4 and ground $\overline{OEQ}$.

Control of the TMC2340

The TMC2340 needs to be initialized to tell it what frequency and amplitude sinusoid to generate. To initialize amplitude, apply the desired full-scale amplitude to the AM input port of the TMC2340 (AM_{14} through AM_0) and pull ENA HIGH for one clock cycle. This will load the amplitude. If ENA is held HIGH, then the amplitude will follow the inputs on the AM port. If the user assumes an implied binary point before the MSB of the AM port, the input range will be 0 to just under 1, and the outputs will fall between 0 and 2, with binary points after I_{15} and Q_{15}.

To set the frequency, the C register must be loaded with a value which is the phase increment per clock cycle. If the binary point is considered to be just left of the MSB (input range is 0 to almost 1) then the output frequency is the TMC2340 clock frequency multiplied by the number loaded into C. Since C is 32 bits wide, with a 20MHz clock, one LSB represents a frequency increment of 0.005Hz.

To load the C register, set $ENYP_1=1$ and $ENYP_0=0$; the data presented at the PH port will be loaded on the next clock rising edge.

At this point the TMC2340 has been initialized and can be put into one of three modes depending upon the states of FM and PM:

Mode 0 — FM=0, PM=0
In this mode the chip is in standby. The unchanging output corresponds to AM cos(PM) on the I outputs with PM being the phase increment.

Mode 1 — FM=1, PM=0
Frequency Modulation Mode. The chip generates an output signal of peak amplitude AM and frequency determined by accumulating the sum of the phase increment values in the C and M registers (more about the M register in a later section).

Mode 2 — FM=0, PM=1
Phase Modulation Mode. The TMC2340 generates a sinusoid of the frequency represented in the C register and the peak amplitude in the AM register. On each clock cycle, the phase of the signal is offset by the value in the M register.

Modulation

The output of the TMC2340 can be phase (Mode 2) or frequency (Mode 1) modulated. An unmodulated sinusoid results if the contents of registers C and M are held constant. Its frequency is set by C (Mode 2) or C+M (Mode 1). Since the state of the M register is not defined at power up, the M register should be loaded or cleared to begin operation.

If the signal is to be frequency modulated then the modulation signal is loaded into the M register. The format for the frequency is the same as that for the C register. If $ENYP_{1,0}=0$, 1 then the data that is presented at the PH port is automatically loaded on each clock rising edge.

For phase modulation, the phase deviation is loaded into the M register (same manner as for frequency modulation). The units of the phase offset are cycles and full-scale is just under one output cycle per TMC2340 clock cycle. The MSB represents a phase of 180°, and the LSB a phase of about $8x10^{-8}$ degrees (eight one-hundred-millionths of a degree), or $\pi/2^{31}$ radians.

To synchronize two TMC2340s, first load them with their respective data in mode 0, then switch them simultaneously to either Mode 1 or Mode 2.

Calculating Frequency, Amplitude, and Phase Input Values for the TMC2340

This Application Brief discusses equations which simplify the calculation of register values which control the TMC2340. These values allow the generation of output carrier frequency, frequency or phase modulation, and output amplitude.

The results of the equations are converted to binary register values and should be rounded to the resolution of the applicable register (32 or 15-bits). For negative values of phase or frequency modulation, use these equations for positive values and see Table 1 of the TMC2340 data sheet to convert them to negative values.

The TMC2340 operates by continuously incrementing a register (phase accumulator) that rolls over when it becomes full. For example, if the next increment to the phase accumulator causes it to overflow by 47 LSBs, the phase accumulator retains the value 47. The value present in the carrier register (C) is the amount by which the phase accumulator is incremented each system clock cycle. As the value of the carrier register is increased, the value with which the the phase accumulator is incremented each clock cycle is increased, resulting in an increased carrier frequency.

The magnitude of the carrier is determined or modulated by the value loaded in the AM register. Phase modulation is accomplished by adding the value of the phase accumulator to the value of the modulation (M) register. This adds an offset to the phase of the carrier. This does not affect the increment value of the phase accumulator and therefore only effects the phase of the carrier, leaving the frequency constant.

Adding the value of the modulation register to the phase accumulator along with the value of the carrier register on each clock cycle results in a shift in frequency. This is because the phase accumulator is incremented by a different amount each clock cycle.

Frequency or phase modulation is selected with the FM and PM input pins which configure the TMC2340. The equations presented herein are useful for setting carrier frequency and phase, output amplitude, and frequency and phase modulation. To modulate the carrier with an external signal, the signal must be digitized and those values loaded into the modulation inputs of the TMC2340.

The carrier and modulation registers are loaded through the PH_{31-0} inputs. The $ENP_{1,0}$ inputs select the desired register. The amplitude register is loaded through the AM_{14-0} inputs.

CARRIER FREQUENCY:

$$\text{Carrier Register (C) Value} = \frac{\text{Desired Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

AMPLITUDE AND AMPLITUDE MODULATION:

$$\text{AM Register Value} = \frac{\text{Desired Output Amplitude}}{\text{Full-Scale Output Amplitude}} \times (2^{15} - 1)$$

FREQUENCY MODULATION:

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

PHASE MODULATION:

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Phase in radians (degrees)}}{2\pi\ (360°)} \times 2^{32}$$

EXAMPLE 1: Set carrier frequency to 3.579545 MHz with a system clock of 20MHz.

$$\text{Carrier Register (C) Value} = \frac{\text{Desired Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32} = \frac{3.579545 \times 10^6}{20 \times 10^6} \times 2^{32}$$

C = 0.17897725 X 4,294,967,296 = 768,701,436 = 2DD1 73FBh
= 0010 1101 1101 0001 0111 0011 1111 1011 = $PH_{31\text{-}0}$

EXAMPLE 2: Set output amplitude to be 12.2% of full-scale.

$$\text{AM Register Value} = \frac{\text{Desired Output Amplitude}}{\text{Full-Scale Output Amplitude}} \times (2^{15}\text{-}1) = \frac{0.122}{1.000} \times 32767$$

AM = 3,998 = 0F9Eh = 0001 1111 0011 1100 = $AM_{14\text{-}0}$

EXAMPLE 3: Change carrier frequency by 10kHz with a system clock of 3 MHz.

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

$$M = \frac{10 \times 10^3}{3 \times 10^6} \times 2^{32} = 14{,}316{,}558 = 00DA\ 740Eh$$

M = 0000 0000 1101 1010 0111 0100 0000 1110 = $PH_{31\text{-}0}$

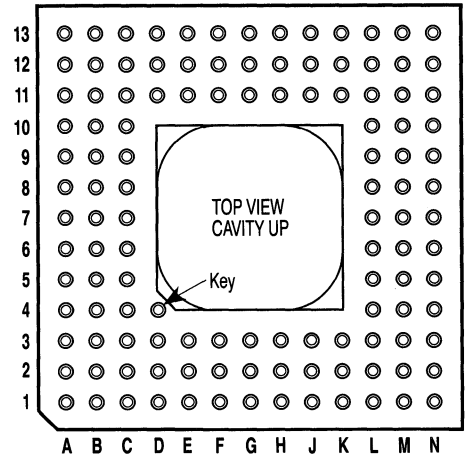
EXAMPLE 4: Shift the phase of any carrier frequency by 12°.

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Phase}}{360°} \times 2^{32} = \frac{12}{360} \times 2^{32}$$

M = 0.033333 X 2^{32} = 143,165,577 = 0888 8889h
= 0000 1000 1000 1000 1000 1000 1000 1001 = $PH_{31\text{-}0}$

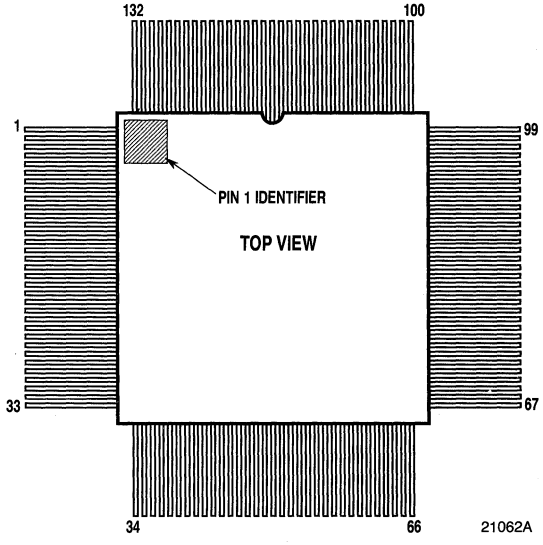
Pin Assignments — 121-Pin Plastic Pin Grid Array, H5 Package; 120-Pin Ceramic PGA, G1 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	Q_5	B3	Q_6	C5	GND	E1	GND	G11	GND	K1	PH_2	L10	PH_{31}	M12	AM_1
A2	Q_7	B4	Q_9	C6	V_{DD}	E2	GND	G12	AM_{12}	K2	PH_4	L11	V_{DD}	M13	AM_2
A3	Q_8	B5	Q_{11}	C7	GND	E3	V_{DD}	G13	AM_{13}	K3	GND	L12	AM_3	N1	PH_8
A4	Q_{10}	B6	Q_{13}	C8	V_{DD}	E11	V_{DD}	H1	PM	K11	GND	L13	AM_4	N2	PH_{10}
A5	Q_{12}	B7	GND	C9	GND	E12	GND	H2	FM	K12	AM_5	M1	PH_6	N3	PH_{12}
A6	Q_{14}	B8	I_1	C10	GND	E13	$\overline{OEI}$	H3	V_{DD}	K13	AM_6	M2	PH_9	N4	PH_{15}
A7	Q_{15}	B9	I_3	C11	V_{DD}	F1	OBIQ	H11	AM_9	L1	PH_5	M3	PH_{11}	N5	PH_{17}
A8	I_0	B10	I_5	C12	I_{11}	F2	GND	H12	AM_{10}	L2	PH_7	M4	PH_{13}	N6	PH_{19}
A9	I_2	B11	I_7	C13	I_{13}	F3	CLK	H13	AM_{11}	L3	GND	M5	PH_{16}	N7	PH_{21}
A10	I_4	B12	I_9	D1	$\overline{OEQ}$	F11	V_{DD}	J1	PH_0	L4	V_{DD}	M6	PH_{18}	N8	PH_{22}
A11	I_6	B13	I_{12}	D2	Q_0	F12	GND	J2	PH_1	L5	PH_{14}	M7	PH_{20}	N9	PH_{24}
A12	I_8	C1	Q_1	D3	GND	F13	AM_{14}	J3	PH_3	L6	V_{DD}	M8	PH_{23}	N10	PH_{26}
A13	I_{10}	C2	Q_2	D11	GND	G1	ENP_1	J11	GND	L7	GND	M9	PH_{25}	N11	PH_{29}
B1	Q_3	C3	V_{DD}	D12	I_{14}	G2	ENP_0	J12	AM_7	L8	V_{DD}	M10	PH_{28}	N12	PH_{30}
B2	Q_4	C4	GND	D13	I_{15}	G3	GND	J13	AM_8	L9	PH_{27}	M11	ENA	N13	AM_0



Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	23	PH_1	45	V_{DD}	67	V_{DD}	89	GND	111	I_2
2	NC	24	PH_2	46	PH_{18}	68	AM1	90	I_{15}	112	VDD
3	Q_4	25	PH_3	47	PH_{19}	69	AM2	91	V_{DD}	113	I_1
4	Q_3	26	PH_4	48	PH_{20}	70	GND	92	I_{14}	114	I_0
5	GND	27	PH_5	49	GND	71	AM_3	93	I_{13}	115	GND
6	Q_2	28	PH_6	50	PH_{21}	72	NC	94	I_{12}	116	GND
7	Q_1	29	GND	51	PH_{22}	73	AM_4	95	GND	117	Q_{15}
8	Q_0	30	PH_7	52	PH_{23}	74	AM_5	96	I_{11}	118	Q_{14}
9	V_{DD}	31	PH_8	53	V_{DD}	75	GND	97	I_{10}	119	Q_{13}
10	$\overline{OEQ}$	32	NC	54	PH_{24}	76	AM_6	98	NC	120	V_{DD}
11	GND	33	GND	55	PH_{25}	77	AM_7	99	V_{DD}	121	Q_{12}
12	GND	34	PH_9	56	PH_{26}	78	AM_8	100	I_9	122	Q_{11}
13	CLK	35	NC	57	PH_{27}	79	AM_9	101	NC	123	Q_{10}
14	GND	36	PH_{10}	58	PH_{28}	80	AM_{10}	102	I_8	124	GND
15	OBIQ	37	V_{DD}	59	PH_{29}	81	AM_{11}	103	NC	125	Q_9
16	ENP_0	38	PH_{11}	60	PH_{30}	82	AM_{12}	104	GND	126	Q_8
17	GND	39	PH_{12}	61	PH_{31}	83	GND	105	I_7	127	Q_7
18	ENP_1	40	PH_{13}	62	NC	84	AM_{13}	106	I_6	128	NC
19	PM	41	PH_{14}	63	ENA	85	AM_{14}	107	I_5	129	GND
20	FM	42	PH_{15}	64	NC	86	GND	108	GND	130	Q_6
21	V_{DD}	43	PH_{16}	65	NC	87	V_{DD}	109	I_4	131	NC
22	PH_0	44	PH_{17}	66	AM_0	88	$\overline{OEI}$	110	I_3	132	Q_5

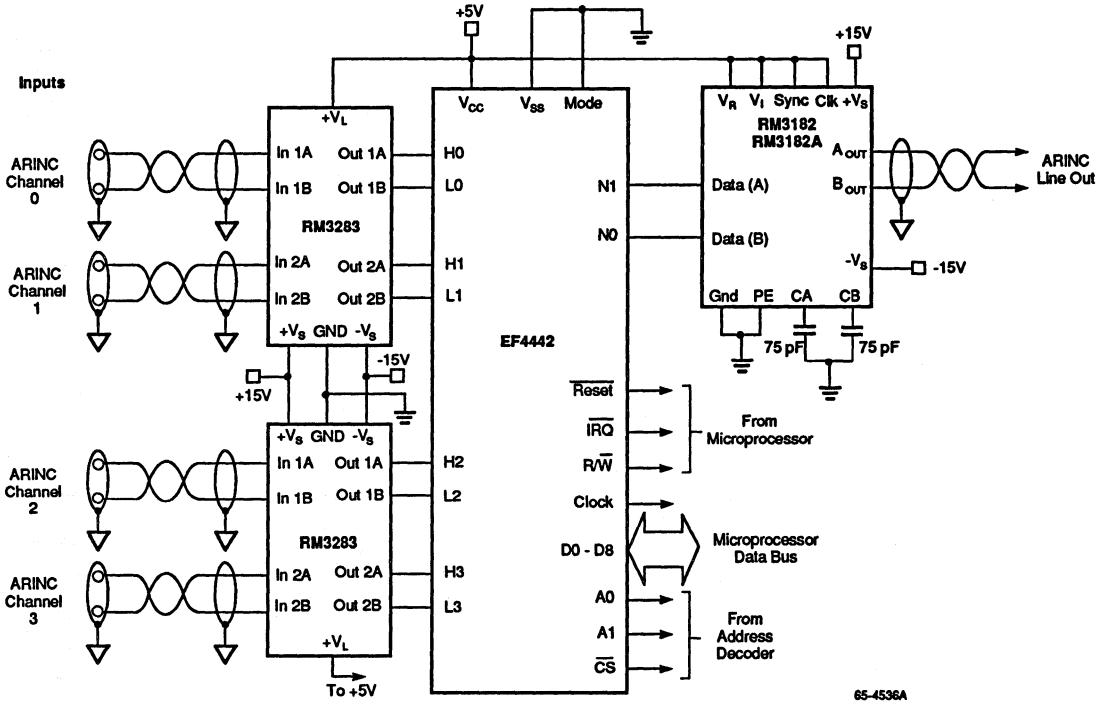


Ordering Information

Product Number	Temperature Range	Screening	Package	Pakcage Marking
TMC2340H5C1	STD: T_A = 0 to 70°C	Commercial	121-Pin Plastic Pin Grid Array	2340H5C1
TMC2340H5C	STD: T_A = 0 to 70°C	Commercial	121-Pin Plastic Pin Grid Array	2340H5C
TMC2340L5V1	EXT: T_C = -55°C to 125°C	MIL-STD-883B	132-Leaded CERQUAD	2340L5V1
TMC2340L5V	EXT: T_C = -55°C to 125°C	MIL-STD-883B	132-Leaded CERQUAD	2340L5V
TMC2340G1V1	EXT: T_C = -55°C to 125°C	MIL-STD-883B	120-Pin Ceramic PGA	2340G1V1
TMC2340G1V	EXT: T_C = -55°C to 125°C	MIL-STD-883B	120-Pin Ceramic PGA	2340G1V

40G06720 Rev B 8/93

ARINC Products



ARINC429 defines an air transport industry standard for the transfer of digital data between avionic system elements. It specifies the basic system configuration and communication protocols. Any avionics element, having information to transmit, will do so from a designated output port over a single twisted and shielded pair of wires to all other elements that have a need for such information. The information flow is uni-directional. The typical ARINC429 system consists of a Controller, which oversees the gathering and time multiplexing of data in accordance with the protocol, a Line Driver, capable of driving the twisted pair, and one or more Receivers, which process the data transmitting over the twisted pair.

Dual Receiver

Features

- Converts ARINC429 levels to serial data
- Two separate analog receiving channels
- Built in TTL compatible test inputs
- TTL and CMOS compatible inputs
- Short-circuit protected
- 3183 and 3283 are pin compatible

Line Drivers

Features

- Adjustable rise and fall times
- Adjustable output voltage swing
- Short circuit protection
- Output over-voltage protected
- TTL and CMOS compatible inputs
- Drives 400Ω/ /30 nF loads
- MIL-STD-883B screening available

ARINC Receivers

	Bandgap References	Hysteresis	Matched Prop. Delays	MIL-STD-883	Voltages	Packages
RM3183	No	No	No	No	+15, -15, +5V	20 pin CDIP 20 pad LCC
RM3183/883B	No	No	No	Yes	+15, -15, +5V	20 pin CDIP 20 pad LCC
RM3283	Yes	Yes	Yes	No	+15, -15, +5V	20 pin CDIP 20 pin SOL 20 pad LCC
RM3283/883B	Yes	Yes	Yes	No	+15, -15, +5V	20 pin CDIP 20 pad LCC

ARINC Line Drivers

	Digitally Sel Transmission Rate	Output Impedance 75Ω Nominal	75Ω Controlled	2Ω	MIL-STD-883	Voltages	Packages
RM3182	No	Yes	No	No	No	+15, -15, +5V	20 pin CDIP 20 pad LCC
RM3182/883B	No	Yes	No	No	Yes	+15, -15, +5V	20 pin CDIP 20 pad LCC
RM3182A	Yes	No	Yes	Yes	No	+15, -15, +5V	20 pin CDIP 20 pin SOL 20 pad LCC
RM3182A/883B	Yes	No	Yes	Yes	Yes	+15, -15, +5V	20 pin CDIP 20 pad LCC

RM3182
ARINC 429 Differential Line Driver

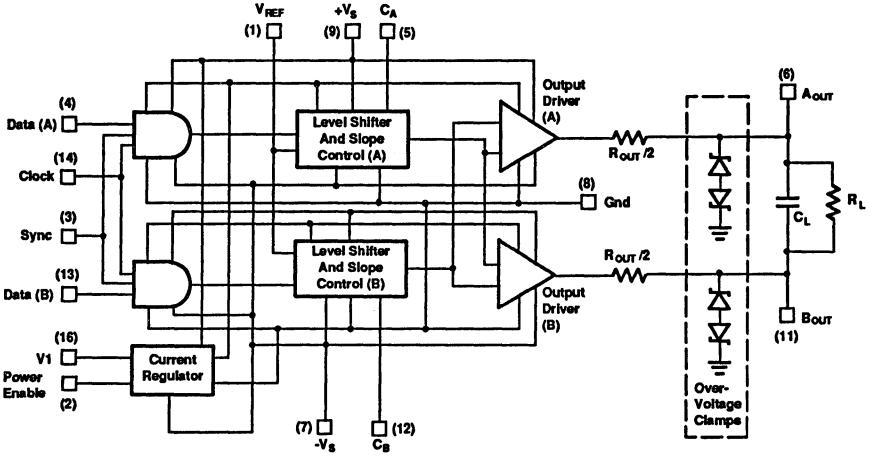
Description

The RM3182 consists of a bus interface line driver circuit plus auxiliary gating and synchronization circuitry. Designed to address the ARINC 429 standard, the RM3182 has output rise and fall times adjustable by the selection of two external capacitor values, and the output voltage swing range can be adjusted through an externally applied V_{REF} signal. The logic inputs as well as the sync control inputs are TTL/CMOS compatible. The device is constructed on a monolithic IC using a junction-isolated bipolar process. Sputtered SiCr resistors are used in the internal bias circuitry, providing stable internal bias currents. The RM3182 is available in 16-lead ceramic DIP and 28-pad LCC, and can be ordered with MIL-STD-883B high reliability screening.

Features

- Adjustable rise and fall times
- Adjustable output voltage swing
- Short circuit protected
- Output overvoltage protected
- Sync and clock enable inputs
- TTL and CMOS compatible inputs
- MIL-STD-883B types available
- 100 Kbits/second data rate

Functional Block Diagram



Notes:
1. R_L and C_L are external. Full load values are: R_L = 400 Ω, C_L = 0.03 µF.
2. Pin numbers are for 16-lead DIP.

Absolute Maximum Ratings

Supply Voltage ($+V_S$ to $-V_S$) 36V
V1 Voltage ..... +7V
V_{REF} Voltage ..... +6V
Logic Input Voltage ..... -0.3V to $+V_S$ +0.3V
Output Short Circuit Duration ..... See Note 1
Output Overvoltage ..... ±6.5V
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -55°C to +125°C
See Note 2
Lead Soldering Temperature (60 sec.) ..... +300°C

Notes:
1. Heatsinking may be required for output short circuit at +125°C.
2. Heatsinking may be required depending on load and signal frequencies

Thermal Characteristics

(Still air, soldered into PC board)

	16-Lead Sidebrazed DIP	28-Pad LCC
Max. Junction Temp.	+175°C	+175°C
Max. P_D T_A < 50°C	1470 mW	1040 mW
Therm. Res. θ_{JC}	25°C/W	25°C/W
Therm. Res. θ_{JA}	85°C/W	120°C/W
For T_A > 50°C Derate at	11.7 mW/°C	8.3 mW/°C

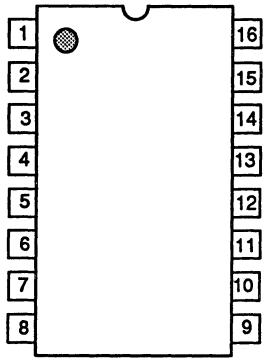
Ordering Information

Part Number	Package	Operating Temperature Range
RM3182S	S	-55°C to +125°C
RM3182S/883B	S	-55°C to +125°C
RM3182L	L	-55°C to +125°C
RM3182L/883B	L	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S = 16-lead sidebraze ceramic DIP
L = 28-pad leadless chip carrier

Connection Information

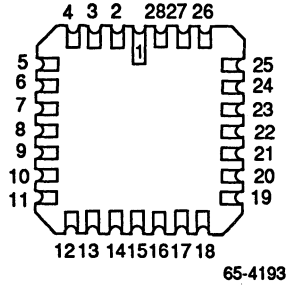
16-Lead Sidebraze DIP (Top View)



65-04192

Pin	Function
1	V_{REF}
2	Pwr Enable
3	Sync
4	Data (A)
5	C_A
6	A_{OUT}
7	$-V_S$
8	GND
9	$+V_S$
10	NC
11	V_{OUT}
12	C_B
13	Data (B)
14	Clock
15	NC
16	V1

28-Pad LCC (Top View)



65-4193

Pin	Function	Pin	Function
1	V_{REF}	15	GND
2	NC	16	$+V_S$
3	Pwer Enable	17	B_{OUT}
4	Sync	18	NC
5	NC	19	NC
6	Data (A)	20	NC
7	NC	21	NC
8	NC	22	C_B
9	C_A	23	Data(B)
10	NC	24	NC
11	NC	25	Clock
12	NC	26	NC
13	A_{OUT}	27	NC
14	$-V_S$	28	V1

Electrical Characteristics

(V_S = ±15V, V_{REF} = V1 = +5V, Pwr Enable = 0V, R_L = open circuit, -55°C ≤ T_A ≤ +125°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Positive Supply Current	Data Rate = 0 to 100 Kbits/sec		11	16	mA
Negative Supply Current	Data Rate = 0 to 100 Kbits/sec	-16	-10		mA
V1 Supply Current	Data Rate = 0 to 100 Kbits/sec		200	975	µA
V_{REF} Supply Current	Data Rate = 0 to 100 Kbits/sec	-1.0	-0.4	-0.15	mA
Input Logic Level High		2.0			V
Input Logic Level Low				0.5	V
Output Voltage High	With Respect to Ground	4.75	5.0	5.25	V
Output Voltage Low	With Respect to Ground	-5.25	-5.0	-4.75	V
Output Voltage Null	Both Data Input = Logic 0	-250	0	+250	mV
Input Current High	V_{IN} = 2.0V		1	10	µA
Input Current Low	V_{IN} = 0.5V	-20	-1		µA
Output Short Circuit Current	Output in High State, to Gnd		-133	-80	mA
Output Short Circuit Current	Output in Low State, to Gnd	80	133		mA
Positive Supply Current	Output High and Shorted to Gnd			150	mA
Negative Supply Current	Output Low and Shorted to Gnd	-150			mA
Input Capacitance*			5	15	pF

*Guaranteed by design.

Typical Power Dissipation Characteristics

(V_S = ±15V, V1 = V_{REF} = +5V, Pwr Enable = 0V, T_A = +25°C)

Data Rate (Kbits/sec)	Load	Positive Supply Current	Negative Supply Current	Pin V1 Supply Current	Internal Power Dissipation	Load Power Dissipation
0 to 100	Open Circuit	11 mA	-10 mA	200 µA	325 mW	0
12.5 to 14	Full Load**	24 mA	-24 mA	200 µA	660 mW	60 mW
100	Full Load**	46 mA	-46 mA	200 µA	1000 mW	325 mW

**R_L = 400Ω, C_L = 0.03 µF (see Functional Block Diagram).

Principles of Operation

Each device consists of one differential driver and associated gating circuitry. The gating circuitry consists of clock and sync signal inputs which are ANDed with the two data inputs. See the block diagram and truth table. Three power supplies are required to operate the RM3182 in a typical ARINC 429 bus application: +15V, -15V, and +5V. The +5V supply, in addition to powering the internal bus current regulator, provides a reference voltage that determines the output voltage swing. The differential output swing will equal 2 V_{REF}. If a value of V_{REF} other than +5V is used, then a separate +5V supply is required for pin V1.

Figure 1 depicts connections for the ARINC 429 application. The driver output impedance is nominally 75Ω. With the Data(A) input at a logic high and Data (B) input at a logic low, A_{OUT} will swing to $+V_{REF}$ and B_{OUT} will swing to $-V_{REF}$ (constituting a logic high state). Reversing the data input states will cause A_{OUT} to swing to $-V_{REF}$ and B_{OUT} to $+V_{REF}$. With both data input signals at a logic low state, the outputs will both swing to 0V (output in null state).

The slew rate of the outputs, and consequently rise and fall times, can be adjusted through the selection of two external capacitor values. Typical values are $C_A = C_B = 75$ pF for high-speed operation (100 Kbits/sec) and $C_A = C_B = 500$ pF for low-speed operation (12.5 to 14 Kbits/sec).

The device can be powered down by applying a logic high signal to the Power Enable pin. If the power down feature is not used, then the Power Enable pin should be tied directly to ground.

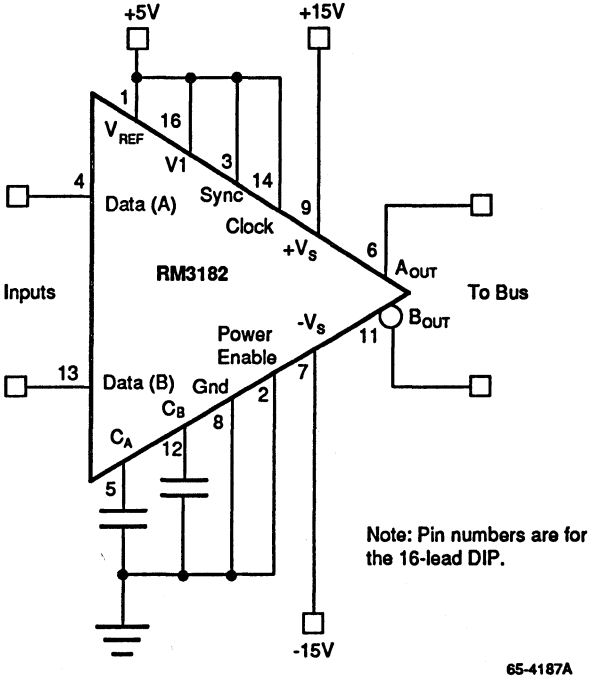


Figure 1. ARINC 429 Bus Application

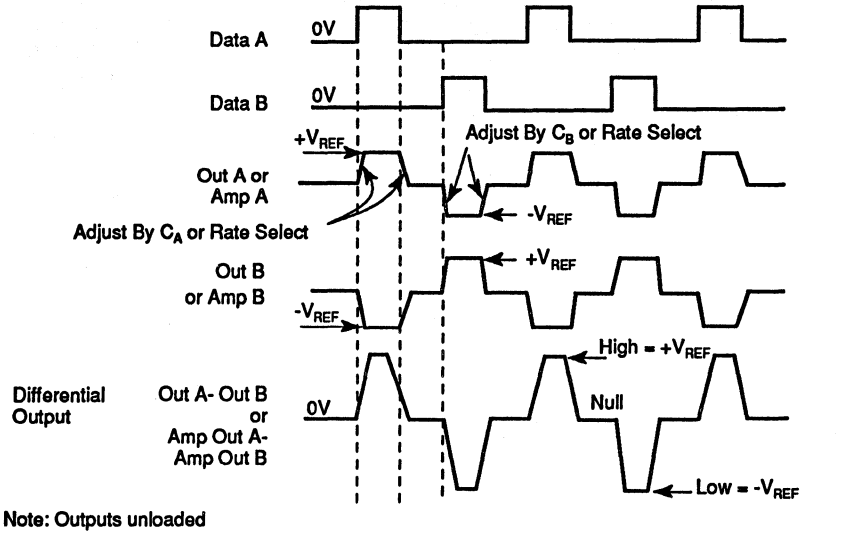
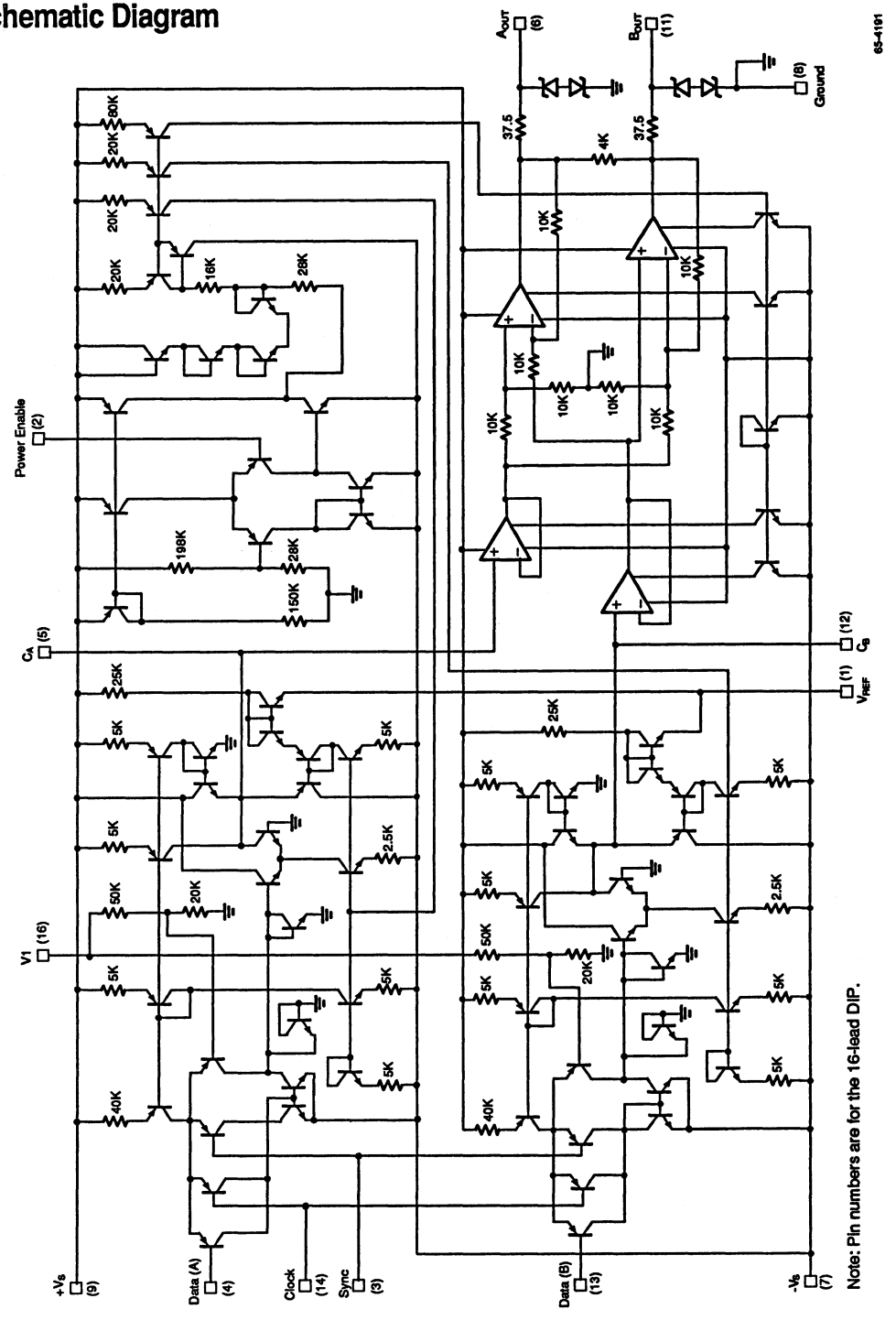


Figure 1. Switching Waveforms

Truth Table

Sync	Clock	Data (A)	Data (B)	AOUT	BOUT	Comments
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	$-V_{REF}$	$+V_{REF}$	Low
H	H	H	L	$+V_{REF}$	$-V_{REF}$	High
H	H	H	H	0V	0V	Null

Schematic Diagram



RM3182A
ARINC 429 Differential Line Driver

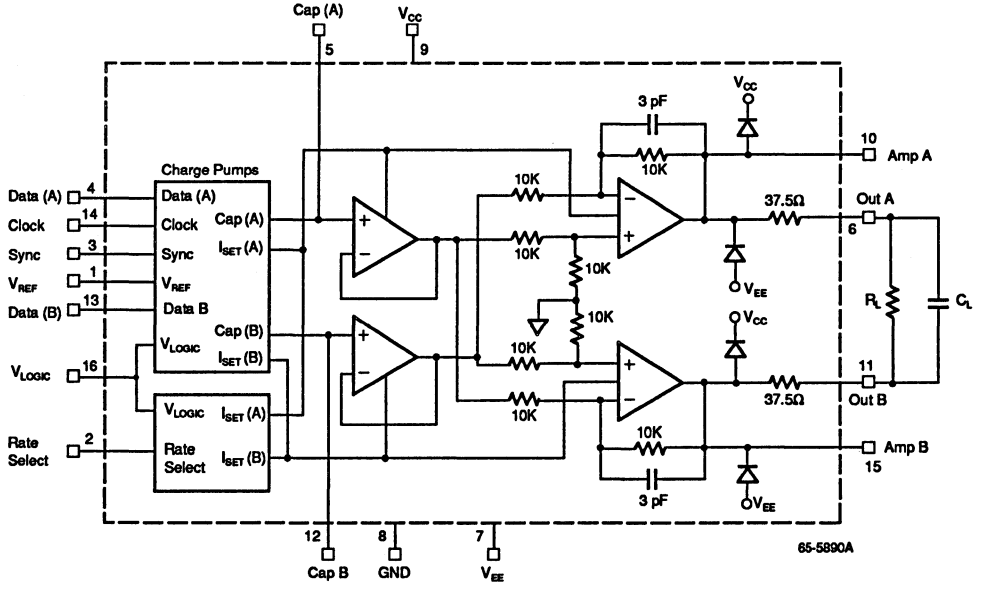
Description

The RM3182A is a complete differential line driver IC. When Data A = Data B or Sync or Clock Signal is low, the driver forces the output to a Voltage Null level (0V ± 250 mV). Designed to address the ARINC 429 standard, the RM3182A has output rise and fall times that can be adjusted by the selection of an external capacitor (C_A or C_B) and an output voltage range adjustable through an externally applied V_{REF} signal. All logic inputs and sync control inputs are TTL/CMOS compatible. The device is constructed on a monolithic IC using a junction-isolated bipolar process. Sputtered SiCr resistors in the internal bias circuitry provide for stable bias currents and a tighter tolerance of output impedance. The RM3182 is available in 16-lead ceramic side-brazed DIP, 28-pad LCC and can be ordered with MIL-STD-883B high reliability screening.

Features

- Adjustable rise and fall times
- Low supply current
- Capable of driving 30 nF || 400Ω
- Digitally selectable 12.5 or 100 kbit/sec data rate
- Adjustable output voltage swing
- Output overvoltage protected
- Short circuit protected
- TTL and CMOS compatible inputs
- MIL-STD-883B screening available
- Available in 16-lead ceramic side-brazed DIP and 28-pad LCC

Functional Block Diagram



Note: Pin numbers are for the DIP package.

Absolute Maximum Ratings

Supply Voltage (V_{CC} to V_{EE}) ..... +36V
V_{LOGIC} Threshold Voltage ..... +7V
V_{REF} Voltage ..... $+V_{CC}$
Logic Input Voltage ..... -0.3V to V_{LOGIC} +0.3V
Temperature Range
Storage ..... -65°C to +150°C
Operating ..... -55°C to +125°C
Junction Temperature ..... -55°C to +175°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Thermal Characteristics

(Still air, soldered on a PC board)

Parameter	16-Lead Side-brazed DIP	28-Pad LCC
Max. Junction Temp.	+175°C	+175°C
Therm. Res. θ_{JA}	70°C/W	60°C/W
Therm. Res. θ_{JC}	28°C/W(1)	25°C/W
For T_A > 50°C Derate at	14.3 mW/°C	13.3 mW/°C

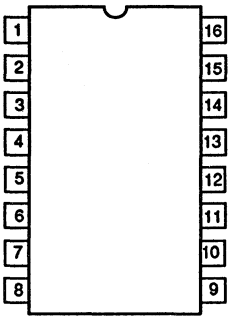
Ordering Information

Part Number	Package	Operating Temperature Range
RM3182AS	S	-55°C to +125°C
RM3182AL	L	-55°C to +125°C

Notes:
S = 16-lead ceramic DIP
L = 28-pad ceramic leadless chip carrier

Connection Information

Top View

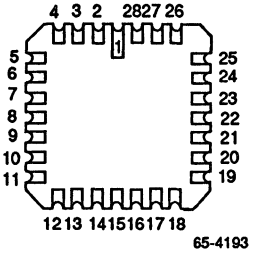


65-04192

Pin Definition 16-lead DIP

Pin	Function	Pin	Function
1	V_{REF}	9	V_{CC}
2	Rate Select	10	Amp A
3	Sync	11	Out B
4	Data A	12	C_B
5	C_A	13	Data B
6	Out A	14	Clock
7	V_{EE}	15	Amp B
8	GND	16	V_{LOGIC}

Top View



65-4193

Pin Definition 28-terminal LCC

Pin	Function	Pin	Function
1	V_{REF}	15	GND
2	NC	16	V_{CC}
3	Rate Select	17	Out B
4	Sync	18	NC
5	NC	19	NC
6	Data A	20	Amp A
7	NC	21	NC
8	NC	22	C_B
9	C_A	23	Data B
10	NC	24	NC
11	NC	25	Clock
12	NC	26	Amp B
13	Out A	27	NC
14	V_{EE}	28	V_{LOGIC}

Electrical Characteristics

(V_{CC} = +15V, V_{EE} = -15V, V_{REF} = +5V, V_{LOGIC} = +5V, Rate Select = 0V, R_L = Open Circuit, C_L = 0 pF, -55°C < T_A < +125°C)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Positive Supply Current	I_{CC}	Data Rate = 0 to 100 kb/s	4.0	5.7	6.9	mA
Negative Supply Current	I_{EE}	Data Rate = 0 to 100 kb/s	4.0	4.9	6.9	mA
V_{LOGIC} Supply Current	I_{LOGIC}	Data Rate = 0 to 100 kb/s	150	214	300	µA
V_{REF} Supply Current	I_{REF}	Data Rate = 0 to 100 kb/s	-500	-294	-100	µA
Input Logic Level High	V_{IH}	Dependent on V_{LOGIC}	2.0		Vlogic	V
Input Logic Level Low	V_{IL}				0.5	V
Output Voltage High	V_{OH}	With Respect to Ground	4.75	5.0	5.25	V
Output Voltage Low	V_{OL}	With Respect to Ground	-5.25	-5.0	-4.75	V
Output Voltage Null	V_{NULL}	Both Data Inputs = Logic 0	-250	0	+250	mV
Input Current High	I_{IH}	V_{IN} = 2.0V			1	µA
Input Current Low	I_{IL}	V_{IN} = 0.5V	-645	-161	-50	nA
Input Capacitance	C_I(1)				15	pF
Output Short Circuit Current	I_{SC}	A_{OUT} and/or B_{OUT} shorted line to line or to GND	100	133	156	mA
V_{CC} Short Circuit Current	I_{SCVCC}	A_{OUT} and/or B_{OUT} shorted line to line or to GND		140	165	mA
V_{EE} Short Circuit Current	I_{SCVEE}	A_{OUT} and/or B_{OUT} shorted line to line or to GND		140	165	mA

Note: 1. Guaranteed by design

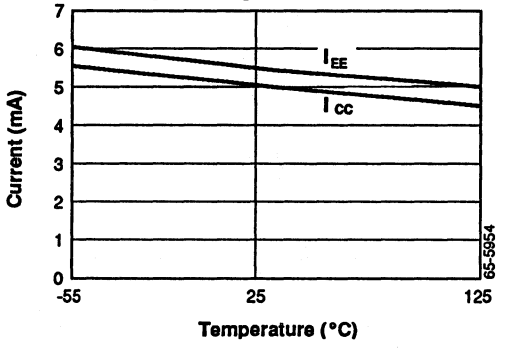
Typical Power Dissipation Characteristics

(V_{CC} = +15V, V_{EE} = -15V, V_{REF} = +5V, T_A = +25°C, C_A = C_B = 56 pF)

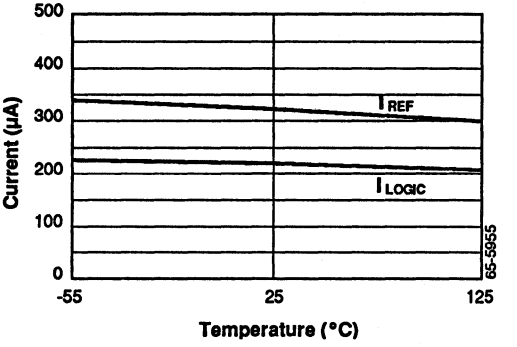
Data Rate (Kbits/sec)	Load	Rate Select	Positive Supply Current	Negative Supply Current	Pin V_{LOGIC} Supply Current	Total Power Dissipation
0-100	Open Circuit	Logic 1,0	5.7 mA	4.9 mA	214 µA	160 mW
12.5-14	Full Load*	Logic 1	19.6 mA	22.7 mA	200 µA	655 mW
100	Full Load*	Logic 0	39.1 mA	38.4 mA	200 µA	1165 mW

*R_L = 400Ω, C_L = 0.03 µF (See Functional Block Diagram)

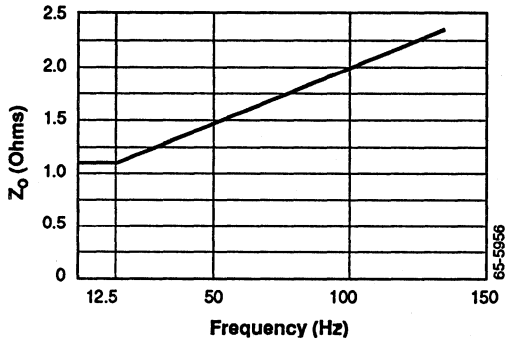
Supply Current vs. Temperature
(C_L = 0 pF, R_L = Open Circuit)



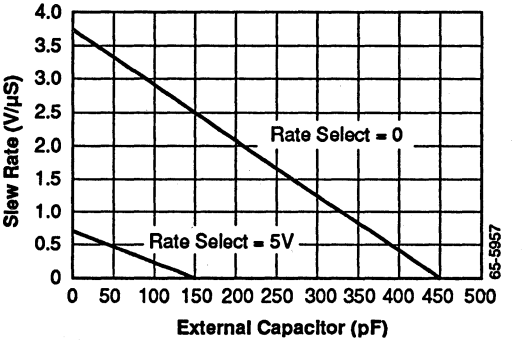
I_{REF} , I_{LOGIC} vs. Temperature



AmpA, AmpB Output Impedance Typical



Slew Rate vs. C_A, C_B



Principles of Operation

The device contains three main functional blocks. The first block is a digital section used to decode the ARINC Clock, Synchronization, and Data inputs as shown in Functional Block Diagram. This block takes these inputs and channels the data to the charge pump circuits. The logical relationship for these pins is presented below.

I/O Truth Table

Sync	Clock	Data A	Data B	Out A	Out B	Comments
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	$-V_{REF}$	$+V_{REF}$	Low
H	H	H	L	$+V_{REF}$	$-V_{REF}$	High
H	H	H	H	0V	0V	Null

The second functional block is a charge pump circuit that is used to control the output waveform and its timing characteristics. This is achieved through charging and discharging a capacitor with a known current. The capacitor is user selectable, and is connected between C_A or C_B pins and ground. A Rate Select pin (digital input) enables to set the rise and fall time. If this pin is tied to ground, the device functions in the high rate. This mode is recommended if the user does not have an application requiring data rate switching. In the table below, recommended capacitor values are given for each possible data combination.

Rate Select Pin Truth Table

Rate Select	C_A C_B (pF)	10% to 90% Rise/Fall Time (µs)	Data Rate (Kbits/sec)	Comments
Logic 0	56	1.5	100	High Rate
Logic 1	56	10	12-14.5	Low Rate
Logic 0	390	10	12-14.5	Low Rate
Logic 1	390	N/A	N/A	Not Used

The last functional block of the device consists of a voltage follower and a high power output differential amplifier. The voltage follower buffers the signals presented at the charge caps and presents the mirrored signal to the difference amplifier to drive the ARINC line. Two different outputs are available from the differential amplifiers: Amp A, Amp B, and Out A , Out B. The outputs Amp A and Amp B are the direct outputs of the power amplifier. The outputs Out A and Out B include 37.5Ω series resistors added to minimize bus reflections by matching the power amplifier's output impedance to the cable's impedance of 75Ω. Amp A and Amp B may be used to customize the output impedance of the device. These outputs can also be used to enhance the device's drive capability. For example, driving the standard 30 nF || 400Ω load defined in the ARINC specifications (see output drive capability and capacitive loads for more details). All outputs are protected from voltage spikes with diodes connected between the output pins and the supply lines.

Output Drive Capability and Capacitive Loads

The Traditional Approach

The RM3182A is capable of driving a high capacitive/ resistive load. If complete ARINC compliance is required then Out A and Out B pins are recommended to maintain the output impedance. In this configuration, driving the full ARINC load of 30 nF || 400Ω the output characteristic takes on the transfer function of a low pass filter due to the internal 37.5Ω resistor, the line resistance and the capacitance associated with the cable. This will result in a lower rise/fall time of the device. Equation 1.1 relates the output voltage at Out A and Out B to the voltage at the power amplifier's output. Output A is taken for this example:

1.1

$$\text{Out A} = \frac{\text{AmpA } Z_L/2}{(Z_L/2) + R_{OUT}}$$

Where: $R_{OUT} = 37.5\Omega$ and $Z_L = R_L \parallel C_L$

The output as a function of frequency is given by equation 1.2.

1.2

$$A_{OUT}(j\omega) = \text{Amp } A(j\omega)\left[\frac{R_L}{R_L + 2R_{OUT}\ (1 + j\omega C_L R_L)}\right]$$

Using equation 1.2, a time constant can be determined for the given application which is shown in equation 1.3.

1.3

$$\tau = (R_{OUT} \| R_L) C_L$$

So, for the maximum loading condition of 30 nf || 400Ω the resulting time constant is 1.9 µs. This shows that with a maximum load, the output waveform is greatly affected by the low pass filter combination of the $R_{OUT} \parallel R_L$ resistor and the load capacitance.

A New Option: Amp A/Amp B

The RM3182A also provides the user the option of connecting the data line directly to the power output amplifiers thus bypassing the internal 37.5Ω resistance of the device and matching the line more precisely. For example, using a 1% 37.5Ω resistor allows better control of the output impedance. By applying the load directly to the power amplifiers output pins, the resulting waveform is virtually unchanged when driving other loads. There may be applications where these pins present a more desirable result. For instance, if the line that the chip is driving is short, then the parasitic components of the line can be neglected, and power amplifier can be tied directly to the lines. This option can be utilized to achieve a greater noise immunity through bypassing the internal resistors.

Applications

Heat Sinking /Air Flow and Short Circuit Protection

The user application will determine if and how much heat sinking/air flow will be required for the RM3182A. Consideration must be given to ambient temperature, load conditions and output voltage swing. In addition, power consumption increases with increased operating frequency. Use the numbers given in the Thermal Characteristics Table to determine that the maximum allowable junction temperature of 175°C is not exceeded.

Outputs Out A and Out B are short circuit protected by the internal 37.5Ω back termination resistors. During a short circuit of the output to either power supply or ground, the device must be able to dissipate the generated heat. For example, if the output is shorted to ground and V_{CC} = +15V, the device must dissipate 15V x 0.165A = 2.5W. An appropriate heat sink is required in this situation.

Note that the Amp A and Amp B outputs are not short circuit protected. Shorting these pins to either power supply or ground will cause failure of the device. An added external resistor will protect the circuit by limiting the current.

Power Supply Considerations

Three power supplies are required to operate the RM3182A in a typical ARINC 429 bus application: +15V for V_{CC}, -15V for V_{EE}, and +5V for both V_{REF} and V_{LOGIC}. The differential output swing of the RM3182A is equal to 2 x V_{REF}. Using +5V gives a differential output swing of 10V. If a different output voltage swing is required, an additional power supply is needed to set V_{LOGIC}.

Each power supply pin should be decoupled to ground using a high quality 10 µF tantalum capacitor. This is especially true when driving a large capacitive or resistive loads. The decoupling capacitors should be located as close to the device pins as possible to eliminate the wiring inductance.

Typical ARINC 429 Application

Figure 1 shows typical switching waveform for the RM3182A in any configuration.

Figure 2 depicts connections for a ARINC 429 high speed bus driver application. This circuit shows the complete configuration for a 100 Kbits/sec, 10V differential output swing using the terminated output pins.

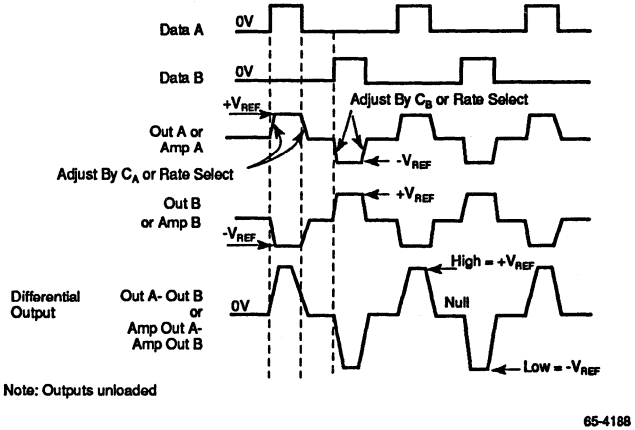


Figure 1. Switching Waveforms

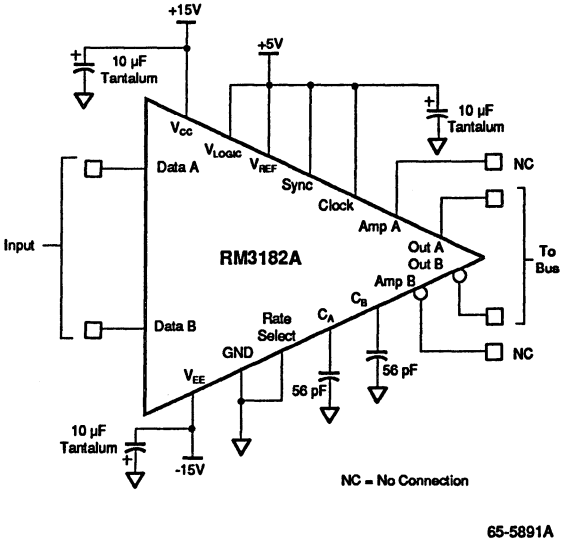


Figure 2. ARINC 429 Bus Driver Application (100 kb/s Mode)

RM3183
Dual ARINC 429 Line Receiver

Description

The RM3183 is a dual line receiver designed to meet all requirements of the ARINC 429 interface specification. It contains two independent receiver channels which accept differential input signals and converts then to serial TTL data.

Input overvoltage protection is provided by special circuitry including dielectrically-isolated thin-film resistors and clamping diodes. Self-test logic inputs are provided for internal system tests. These inputs force the outputs to either a high, a low or a null state for off-line system tests.

Input noise filtering is accomplished with external capacitors. Two are required for each channel and can be adjusted for best noise immunity at a specific data rate.

Three power supplies are needed plus ground. The input thresholds depend only on the logic supply, so a wide range of dual supplies can be accommodated.

The Raytheon RM3183 line receiver is the companion chip to the RM3182 line driver. Together they provide all the analog functions needed for the ARINC 429 interface. Digital data processing involving serial-to-parallel conversion and clock recovery can be accomplished using one of the ARINC interface ICs available or by discrete or gate array implementations.

Features

- Converts ARINC levels to serial data
- Adjustable noise filters
- TTL and CMOS compatible outputs
- Built-in test inputs
- Input protection circuitry
- Mil-Std-883B screening available
- 20-pin DIP and LCC packages available
- Dice with Mil visual screening available

Absolute Maximum Ratings

Supply Voltage $+V_S$ ..... +20VDC
$-V_S$ ..... -20VDC
$+V_L$ ..... +7VDC
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Input Voltage Range ..... ±50V
Output Short Circuit Duration ..... Not Protected
Internal Power Dissipation ..... 900 mW
Lead Soldering Temperature
(DIP, LCC; 60 sec.) ..... +300°C

Thermal Characteristics

(Still air, soldered into PC board)

	20-Lead Ceramic DIP	20-Pad LCC
Max. Junction Temp.	+175°C	+175°C
Max. P_D T_A < 50°C	1042 mW	925 mW
Therm. Res. θJ_C	60°C/W	37°C/W
Therm. Res. θJ_A	120°C/W	105°C/W

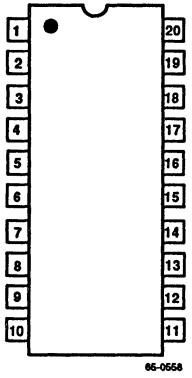
Ordering Information

Part Number	Package	Operating Temperature Range
RM3183S	D	-55°C to +125°C
RM3183L	L	-55°C to +125°C

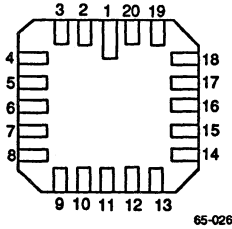
Notes:
D = 20-lead ceramic DIP
L = 28-pad leadless chip carrier

Connection Information

Top View



20-Pad LCC
(Top View)



Pin Definition 20-Lead DIP/20-Terminal LCC

Pin	Function	Pin	Function
1	$-V_S$	11	$+V_S$
2	TestA	12	OUT1B
3	CAP2B	13	NC
4	IN2B	14	GND
5	OUT2B	15	OUT1A
6	IN2A	16	IN1B
7	CAP2A	17	CAP1B
8	OUT2A	18	IN1A
9	$+V_L$	19	CAP1A
10	NC	20	TESTB

DC Electrical Characteristics

T_A = -55°C to +125°C, ±12V ≤ V_S ≤ ±15V, V_L = +5V, unless otherwise noted

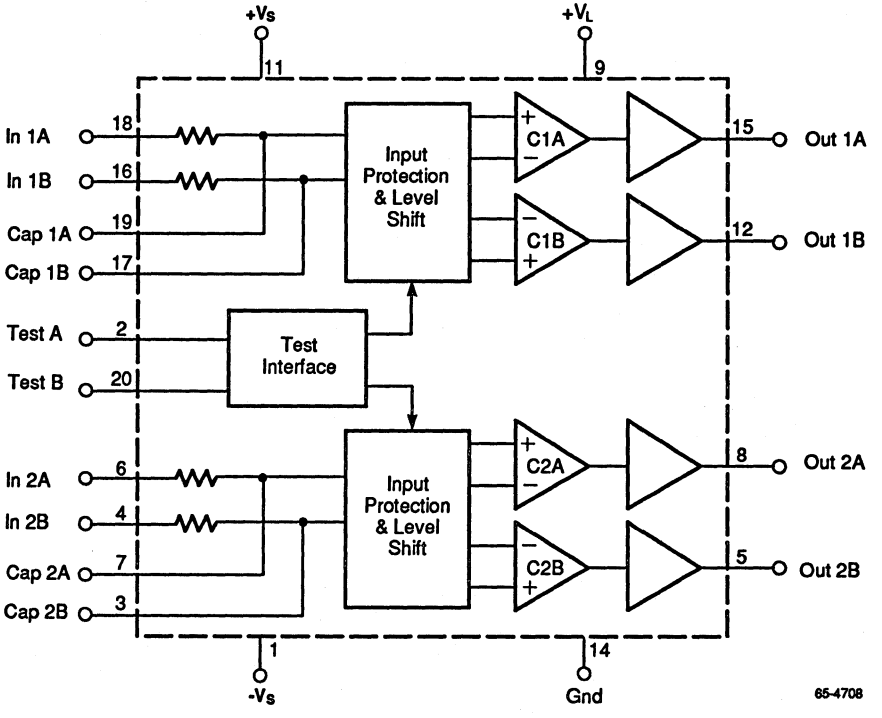
Symbol	Parameter	Conditions		Specifications			
				Min	Typ	Max	Units
V_{IH}	V(A)-V(B)	OUTA = 1		6.5	10	13	V
V_{IL}	V(A)-V(B)	OUTB = 1		-6.5	-10	-13	V
V_{IN}	V(A)-V(B)	OUTA and OUTB = 0		-2.5	0	+2.5	V
V_{IC} (2)	V(A) and V(B)-GND	Max common mode			±5		V
		frequency = 80 kHz					
R_I	Input resistance, Input A to Input B			30	50		kΩ
R_H	Input resistance, Input A to Gnd			19	25		kΩ
R_G	Input resistance, B to Gnd			19	25		kΩ
C_I (1, 2)	Input capacitance, A to B	Filter caps disconnected			3	10	pF
C_H (1, 2)	Input capacitance, A to Gnd	Filter caps disconnected			3	10	pF
C_G (1, 2)	Input capacitance B to Gnd	Filter caps disconnected			3	10	pF
Test Inputs (Test A, Test B)							
V_{IH}	Logic 1 input voltage		V(A) = 0V V(B) = 0V	2.7			V
V_{IL}	Logic 0 input voltage					0.0	V
I_{IH}	Logic 1 input current	V_{IH} = 2.7V			5	15	µA
I_{IL}	Logic 0 input voltage	V_{IL} = 0.0V			0.5	1.0	µA
Outputs							
V_{OH}	I_{OH} = 100 µA	T_A = 25°C		4.0	4.3		V
	I_{OH} = 2.8 mA	Full temp. range		3.5	4.0		V
V_{OL}	I_{OL} = 100 µA	T_A = 25°C			0.02	0.08	V
	I_{OL} = 2.0 mA	Full temp. range			0.3	0.8	V
Tr	Rise Time	C_L = 50 pF, T_A = 25°C			40	70	ns
Tf(6)	Fall Time	C_L = 50 pF T_A = 25°C			30	70	ns
T_{PLH}	Propagation delay Output low to high	C_L = 50 pF, f_O = 400 kHz Filter caps = 39 pF			800		ns
T_{PHL}	Output high to low	T_A = 25°C			320		ns
Supply Current							
I_{CC} (+V_S)	Test inputs = 0V	±V_S = 15V, T_A = 15°C			3.7	7.0	mA
		±V_S = 12V, T_A = 15°C			3.0	6.0	mA
I_{EE} (-V_S)	Test inputs = 0V	±V_S = 15V, T_A = 15°C			8.7	15.0	mA
		±V_S = 12V, T_A = 15°C			7.4	14.0	mA
I_{DD} (+V_L)	Test inputs = 0V	±V_S = 15V, T_A = 15°C			9.0	20.0	mA
		±V_S = 12V, T_A = 15°C			8.6	18.0	mA

Notes:
1. With noise filter capacitors disconnected.
2. Guaranteed by design.

Truth Table

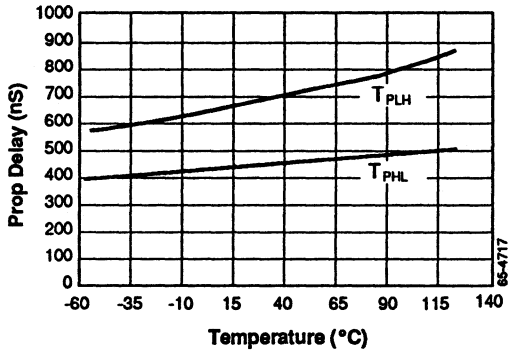
ARINC nputs V(A) - V(B)	Test Inputs TESTA	TESTB	Outputs OUTA	OUTB
Null	0	0	0	0
Low	0	0	0	1
High	0	0	1	0
V(A) = 0V, V(B) = 0V	0	1	0	1
V(A) = 0V, V(B) = 0V	1	0	1	0
V(A) = 0V, V(B) = 0V	1	1	0	0

Functional Block Diagram

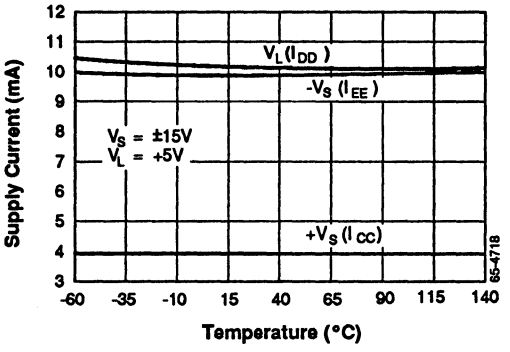


Typical Performance Characteristics

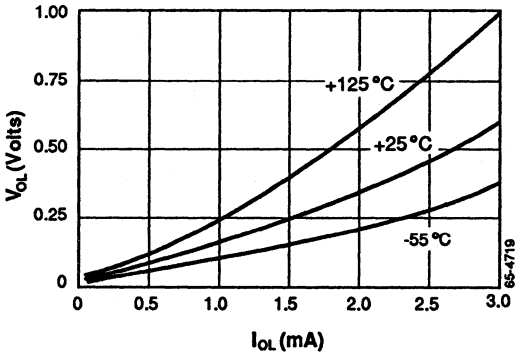
Propagation Delay vs. Temperature
C_L = 50 pF, C_{FILTER} = 39 pF



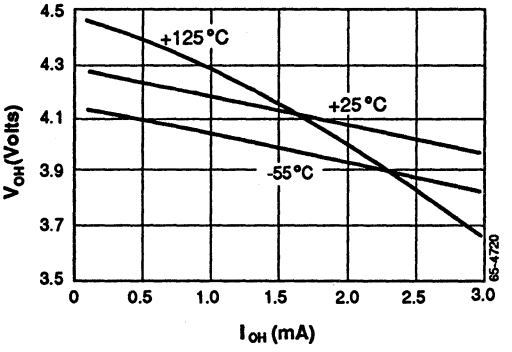
Supply Current vs. Temperature



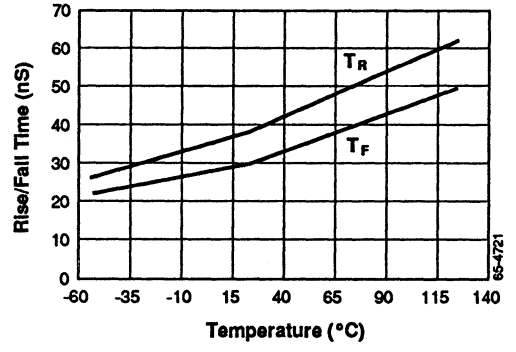
Output Voltage Low vs. Output Current



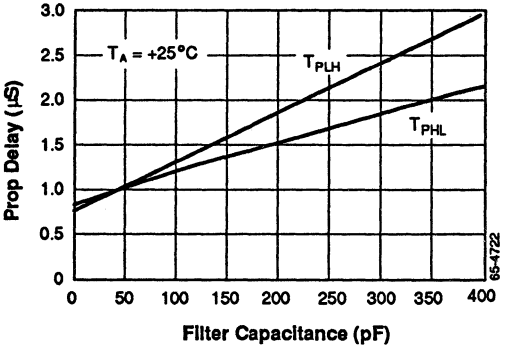
Output Voltage High vs. Output Current

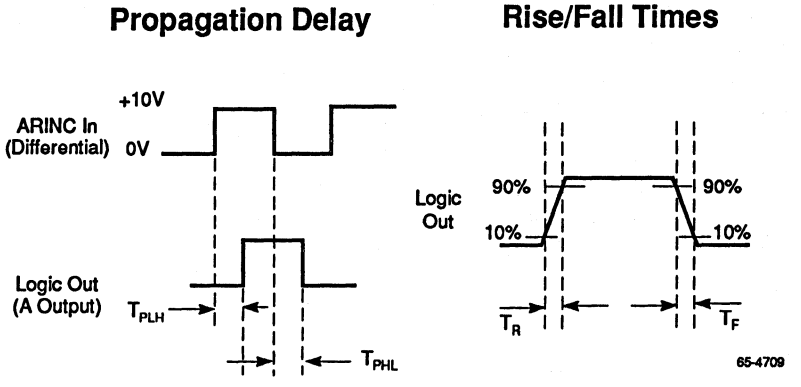


T_R and T_F vs. Temperature

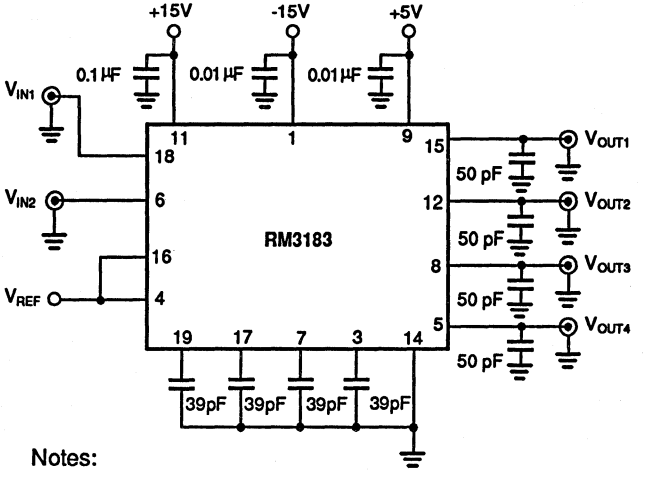


Propagation Delay vs. Filter Capacitance
T_A = 25°C





AC Test Waveforms



Notes:

1. V_{IN} = 400 kHz square wave, -3.5V to +3.5V.
2. Set V_{REF} = +3.5 V to test V_{OUT1} and V_{OUT3}.
   Set V_{REF} = -3.5 V to test V_{OUT2} and V_{OUT4}.
3. 50 pF load capacitance includes probe and wiring capacitance.

65-4706

AC Test Schematic Diagram

Circuit Description

The RM3183 contains two discrete ARINC 429 receiver channels. Each channel contains three main sections: a resistor-diode input network, a window comparator, and a logic output buffer stage. The first stage provides overvoltage protection and biases the signal using voltage dividers and current sources which are internally connected to the $+V_L$ logic supply. This configuration provides excellent input common mode rejection and a stable reference voltage for the window comparators. Because the threshold for switching is determined by this circuitry, ±5% tolerance is recommended for the $+V_L$ supply. The test inputs will set the outputs to a predetermined state for built-in test capability. The ARINC inputs must be forced to 0V when using the test inputs. If the test inputs are not used, they should be grounded.

The window comparator stage generates two serial data streams, one having logic 1 states corresponding to ARINC "high" states (OUTA), and the other having logic 1 states corresponding to ARINC "low" states (OUTB). An ARINC "null" state at the inputs forces both outputs to logic 0. thus, the ARINC clock signal is recovered by applying a NOR function to OUTA and OUTB.

The output stage generates a TTL compatible logic output capable of driving several gate inputs.

Applications Information

The standard connections for the RM3183 are shown in Figure 1. Dual supplies from ±12 to ±15 VDC are recommended for the $\pm V_S$ supplies. Decoupling of all supplies should be done near the IC to avoid propagation of noise spikes due to switching transients. The ground connections should be sturdy and isolated from large switching currents to provide as quiet a ground reference as possible.

The noise filter capacitors are optional and are added to provide extra noise immunity by limiting the noise bandwidth of the input signal before it reaches the comparator. Two capacitors are required for each channel and they must all be the same value. The suggested capacitor value for 100 KHz operation is 39 pF, which will give a noise bandwidth of approximately 800 KHz. For lower data rates, larger values of capacitance may be used to yield better noise performance. To get optimum performance, the following equation should be used to calculate capacitor value for a specific data rate:

$$C = \frac{3.95 \times 10^{-6}}{F_O}$$

F_O = Data rate, bits/sec

The RM3183 can be used with the Raytheon RM3182 Line Driver to provide a complete analog ARINC 429 interface. A simple application which can be used for systems requiring a repeater-type circuit for long transmissions or test interfaces is given in Figure 2. More RM3182 drivers may be added to test multiple ARINC channels, as shown.

An all digital IC is available which forms a complete receiver system when combined with the RM3183. The Thomson EF4442 is a four channel ARINC 429 receiver IC which contains all the digital circuitry required to interface with an 8-bit processor. Each channel consists of a 32-bit register, an 8-bit status word comparator, and a 24-bit latch. A multiplexer and 8-bit data bus buffer form the interface to the system microprocessor. Figure 3 shows a typical ARINC application having both transmit and receive functions using four ICs: the RF4442, plus the RM3182 driver and two RM3183 dual receivers. Fore more information on the EF4442, contact Thomson Military Semiconductors at (714) 957-6018.

Typical Applications

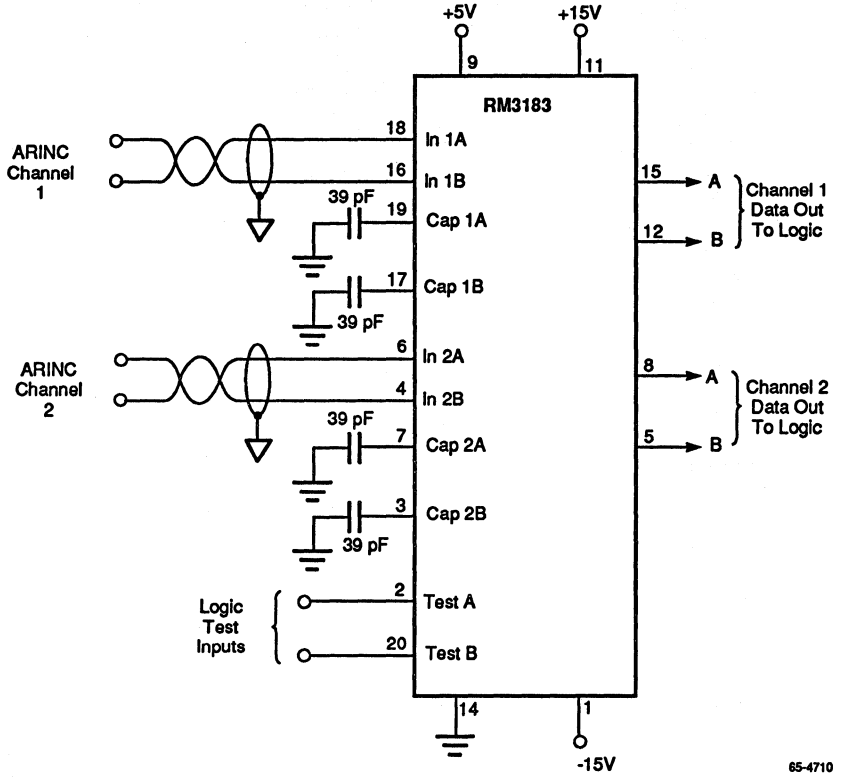


Figure 1. ARINC Receiver Standard Connections

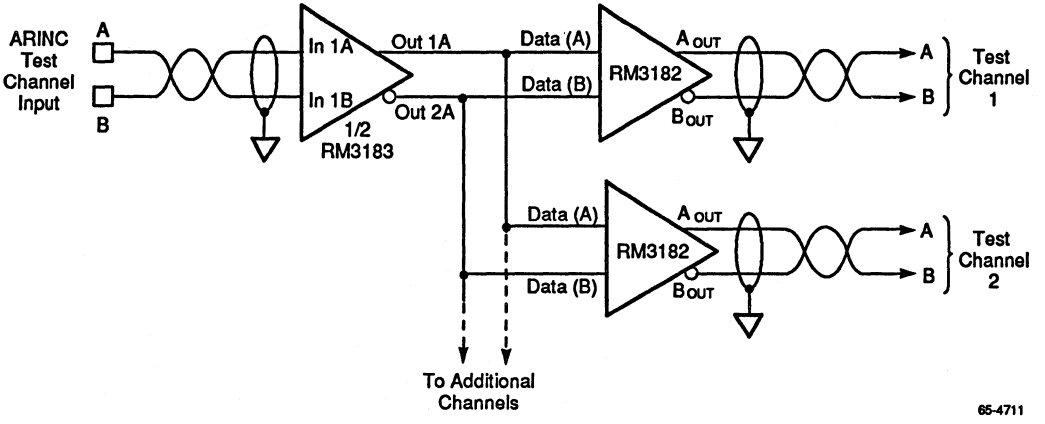


Figure 2. Repeater Circuit

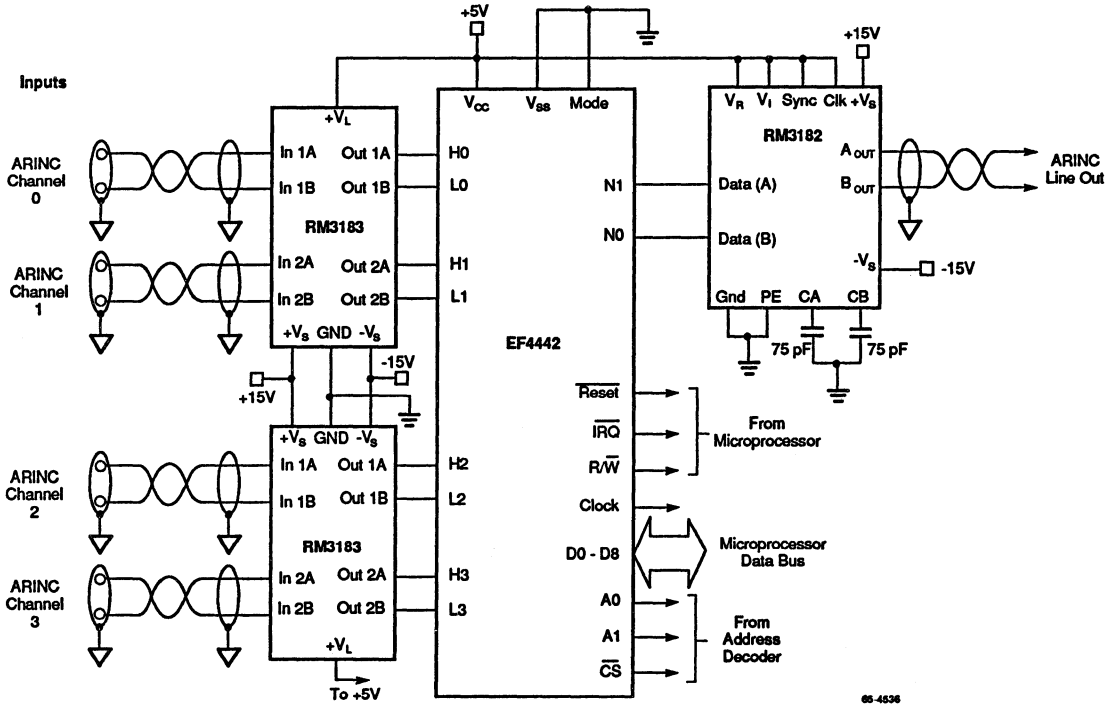
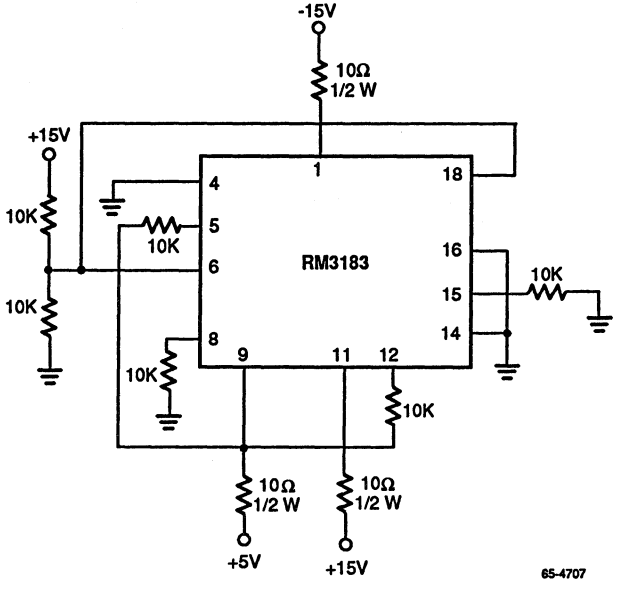
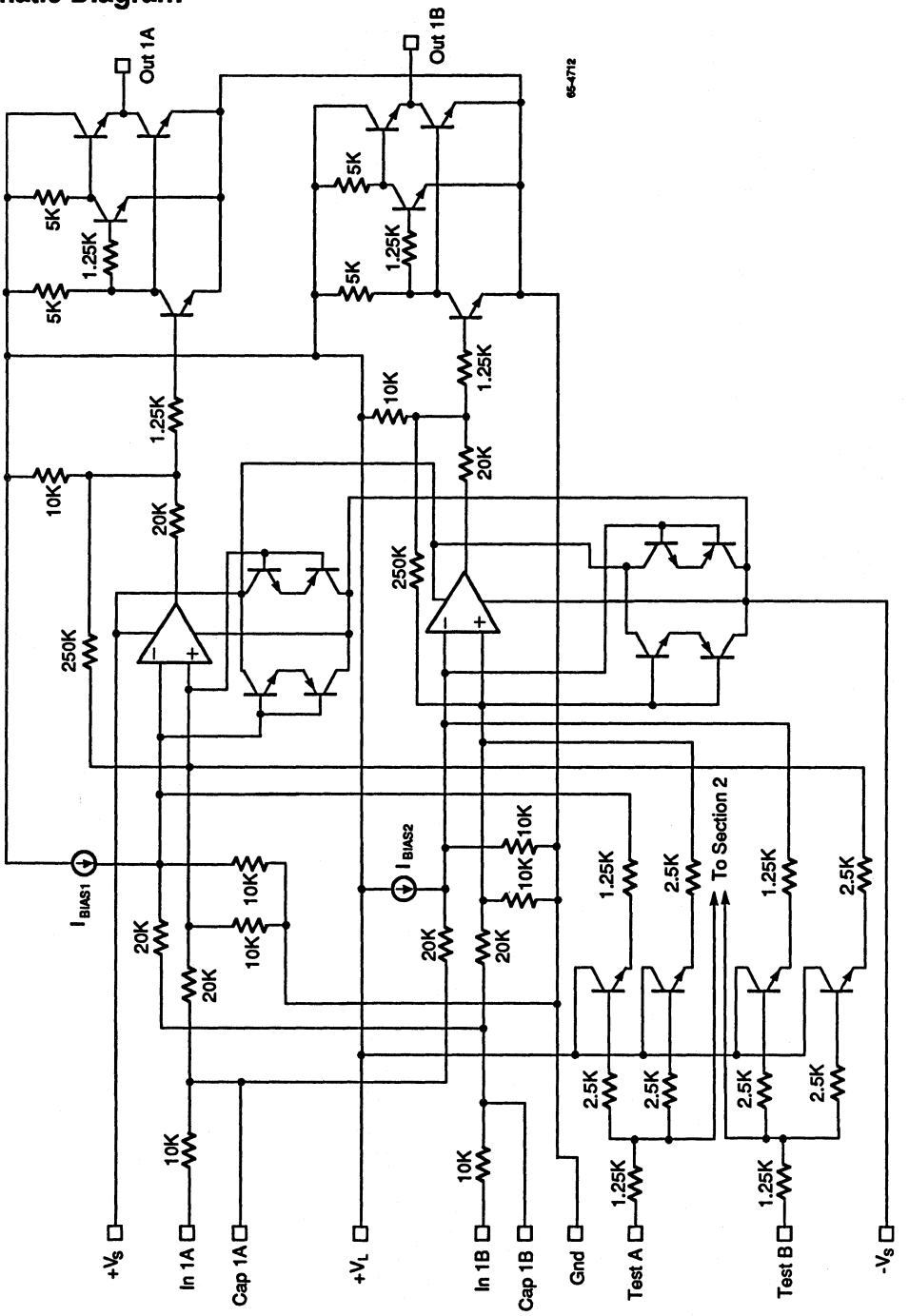


Figure 3. Four-Channel ARINC Receiver Circuit



Burn-In Circuit

Schematic Diagram



RM3283
Dual ARINC 429 Line Receiver

Description

The RM3283 consists of two analog ARINC 429 receivers which take differentially encoded ARINC level data and convert it to serial TTL level data. The RM3283 provides two complete analog ARINC receivers and no external components are required.

Input level shifting thin film resistors and bipolar technology allow ARINC input voltage transients up to ±100V without damage to the RM3283.

Each channel is identical, featuring symmetrical propagation delays for better high speed performance. Input common mode rejection is excellent and threshold voltage is stable, independent of supply voltage. Data outputs are TTL and CMOS compatible.

Two TTL compatible test inputs used to test the ARINC channels are available. They can be used to override the ARINC input data and set the channel outputs to a known state.

The Raytheon RM3182/RM3182A line driver is the companion chip to the RM3283 line receiver. Together they provide the analog functions needed for the ARINC 429 interface. Digital data processing involving serial-to-parallel conversion and clock recovery can be accomplished using one of the ARINC interface IC's available or by an equivalent gate array implementation.

Features

- Two separate analog receiver channels
- Converts ARINC 429 levels to serial data
- Built-in TTL compatible complete channel test inputs
- TTL and CMOS compatible outputs
- Low power dissipation
- Internal bandgap
- Short circuit protected
- MIL-STD-883B screening available for ceramic packages
- Available in 20-lead ceramic DIP, 20-pad LCC, and 20-lead SOL

Absolute Maximum Ratings

Supply Voltage (V_{CC} to V_{EE}) ..... +36V
V_{LOGIC} Voltage ..... +7V
Logic Input Voltage ..... -0.3V to V_{LOGIC} +0.3V
Temperature Range
  Storage ..... -65°C to +150°C
  Operating ..... -55°C to +125°C
Junction Temperature ..... -55°C to +175°C
Lead Soldering Temperature
  (60 sec., DIP, LCC) ..... +300°C
  (10 sec., SOL) ..... +260°C

Ordering Information

Part Number	Package	Operating Temperature Range
RV3283M	M	-40°C to + 85°C
RM3283D	D	-55°C to +125°C
RM3283L	L	-55°C to +125°C

Notes:
D = 20-lead ceramic DIP
L = 20-pad LCC
M = 20-lead SOL (Wide Body SOIC)

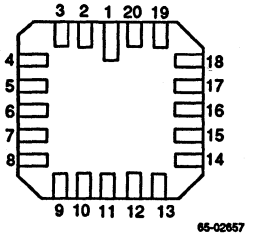
Thermal Characteristics (Still air, soldered on a PC board)

Parameter	20-Pad LCC	20-Lead CDIP	20-Lead SOL
Max Junction Temp.	175°C	175°C	125°C
Therm. Res. θ_{JA}	85°C/W	70°C/W	85°C/W
Therm. Res. θ_{JC}	20°C/W(1)	28°C/W(1)	30 °C/W

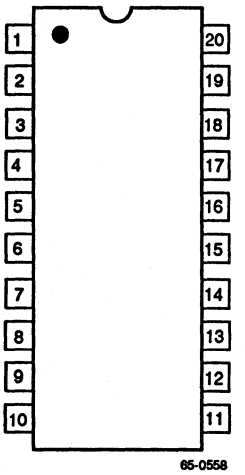
Notes:
1. MIL-STD-1835

Connection Information

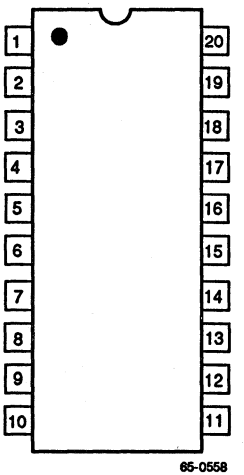
Top View



Top View



Top View



Pin	Function
1	-Vs
2	TestA
3	Cap2B
4	In2B
5	Out2B
6	In2A
7	Cap2A
8	Out2A
9	$+V_L$
10	NC
11	+Vs
12	Out1B
13	NC
14	Gnd
15	Out1A
16	In1B
17	Cap1B
18	In1A
19	C1A
20	TestB

DC Electrical Characteristics

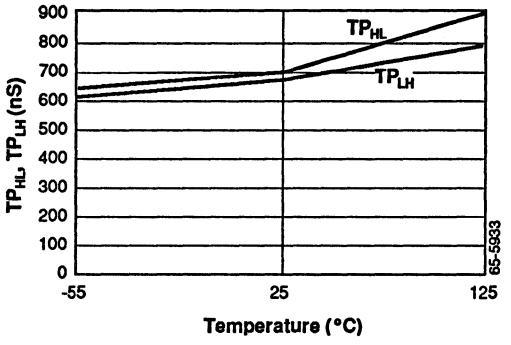
T_A = -55°C to +125°C, ±12V ≤ V_S ≤ ±15V, V_L = +5V, unless otherwise noted

Symbol	Parameter	Conditions	Specifications			
			Min	Typ	Max	Units
I_{CC} ($+V_S$)	Test inputs = 0V			4.3	6.0	mA
I_{EE} ($-V_S$)	Test inputs = 0V			10.1	12.0	mA
I_L (V_L)	Test inputs = 5V			14.0	17.5	mA
V_{TL} (2)	V(A)-V(B)	Low threshold	4.7	5.0	5.3	V
V_{TH} (2)	V(A)-V(B)	High threshold	5.7	6.0	6.3	V
V_{IN}	V(A)-V(B)	OUTA and OUTB = 0	-2.5	0	2.5	V
V_{IC} (3)	V(A) and V(B)-GND	Max common mode frequency = 80 kHz		±5		V
R_I	Input resistance, Input A to Input B		35	50		kΩ
R_H	Input resistance, Input A to Gnd		20	25		kΩ
R_G	Input resistance, B to Gnd	Filter caps disconnected	20	25		kΩ
C_I (1, 4)	Input capacitance, A to B				10	pF
C_H (1, 4)	Input capacitance, A to Gnd	Filter caps disconnected			10	pF
C_G (1, 4)	Input capacitance B to Gnd	Filter caps disconnected			10	pF
Test Inputs (Test A, Test B)						
V_{IH} (5)	Logic 1 input voltage		2.7			V
V_{IL} (5)	Logic 0 input voltage		0		0.8	V
I_{IH}	Logic 1 input current	V_{IH} = 5V		120	300	µA
I_{IL}	Logic 0 input voltage	V_{IL} = 0.8V		15	40	µA
Outputs						
V_{OH}	I_{OH} = 100 µA	T_A = 25°C	4.0	4.3		V
	I_{OH} = 2.8 mA	Full temp. range	3.5	4.0		V
V_{OL}	I_{OL} = 100 µA	T_A = 25°C		0.02	0.1	V
	I_{OL} = 2.0 mA	Full temp. range		0	0.8	V
Tr(6)	Rise Time	C_L = 50 pF @ 25°C		50	70	ns
Tf(6)	Fall Time	C_L = 50 pF @ 25°C		40	70	ns
T_{PLH}	Propagation delay	C_L = 50 pF, f = 400 kHz				
	Output low to high	Filter caps = 0 pF		700		ns
T_{PHL}	Output high to low	T_A = 25°C		700		ns

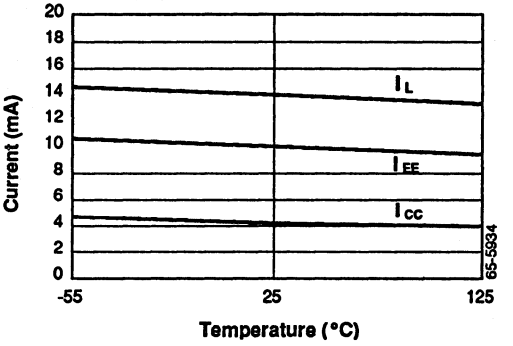
Notes
1. As stated in ARINC429
2. V_T refers to the threshold voltage at which the channels output switches from low to high or from high to low
3. Common mode voltage present at both ARINC inputs
4. Guaranteed by design
5. Test inputs should be connected to ground if not used
6. Sample tested

Typical Performance Curves

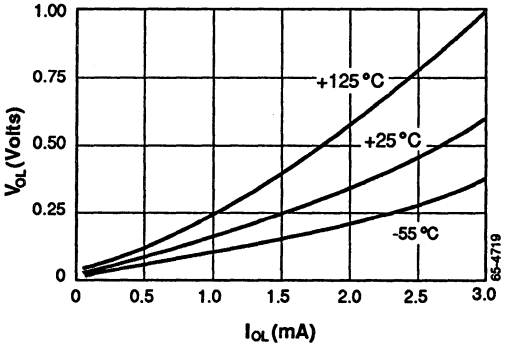
Propagation Delay vs. Temperature
C_L = 50 pF, C_{FILTER} = 0 pF



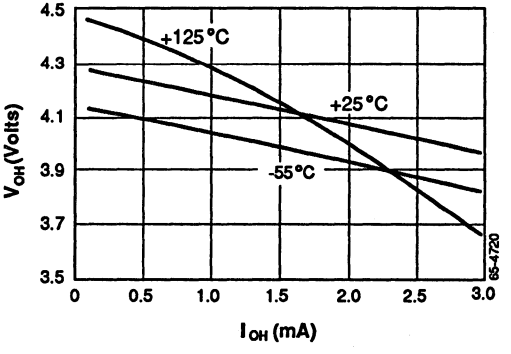
Supply Current vs. Temperature



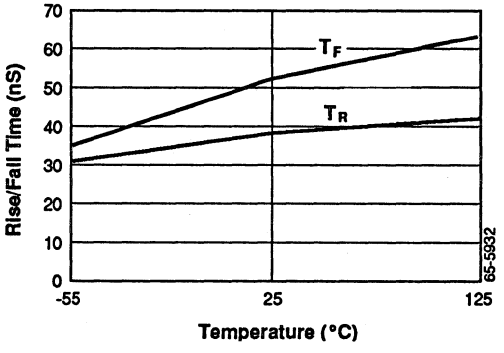
Output Voltage Low vs. Output Current



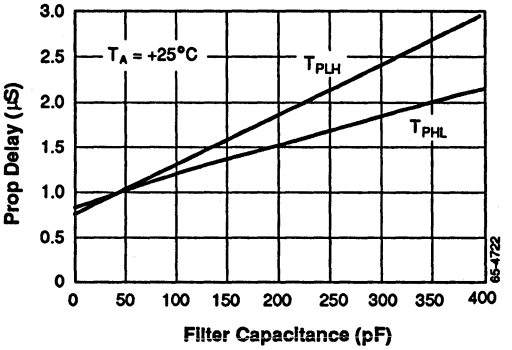
Output Voltage High vs. Output Current

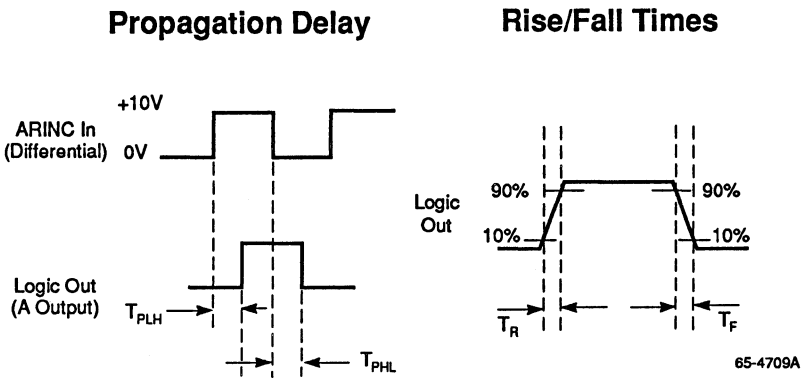


T_R and T_F vs. Temperature

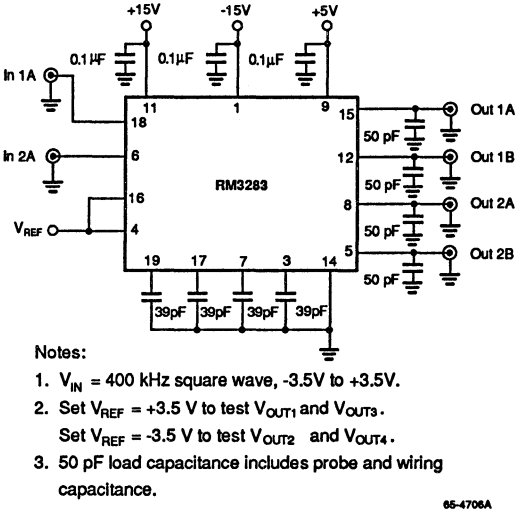


Propagation Delay vs. Filter Capacitance
T_A = 25°C





AC Test Waveforms

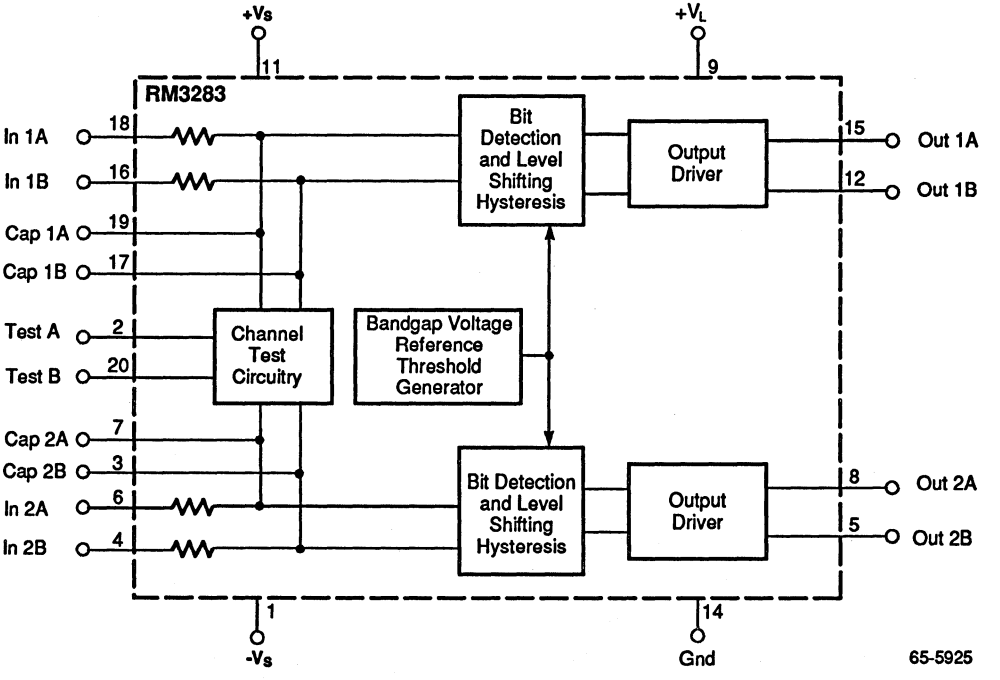


AC Test Schematic Diagram

RM3283 Test Input Truth Table

ARINC Inputs	Test Inputs		Outputs		Output
V(A)-V(B)	TESTA	TESTB	OUTA	OUTB	State
Null	0	0	0	0	Null
Low	0	0	0	1	Low
High	0	0	1	0	High
X	0	1	0	1	Low
X	1	0	1	0	High
X	1	1	0	0	Null

Functional Block Diagram



Circuit Description

The RM3283 contains two discrete ARINC 429 receiver channels. Each channel contains three main sections: a resistor input network, a window comparator, and a logic output buffer stage. The first stage provides overvoltage protection and biases the signal using voltage dividers and current sources, providing excellent input common mode rejection. The test inputs are provided to set the outputs to a predetermined state for built-in channel test capability. If the test inputs are not used, they should be grounded.

The window comparator section detects data from the resistor input network. A Logic 1 corresponds to ARINC "high" state (OUTA) and a Logic 0, to ARINC "low" state (OUTB). An ARINC "null" state at the inputs forces both outputs to Logic 0. Threshold and hysteresis voltages are generated by a bandgap voltage reference to maintain stable switching characteristics over temperature and power supply variations.

The output stage generates a TTL compatible logic output capable of driving 3 mA of load.

Applications Information

The standard connections for the RM3283 are shown in Figure 1. Dual supplies from ±12 to ±15 VDC are recommended for the $\pm V_S$ supplies. Decoupling of all supplies should be done near the IC to avoid propagation of noise spikes due to switching transients. The ground connection should be sturdy and isolated from large switching currents to provide as quiet a ground reference as possible.

The noise filter capacitors are optional and are added to provide extra noise immunity by limiting bandwidth of the input signal before it reaches the window comparator stage. Two capacitors are required for each channel and they must all be the same value. The suggested capacitor value for 100 kHz operation is 39 pF. For lower data rates, larger values of capacitance may be used to yield better noise performance. To get optimum performance, the following equation can be used to calculate capacitor value for a specific date rate:

$$C_{FILTER} = \frac{3.95 \times 10^6}{F_O}$$

Where:

C_{FILTER} is the capacitor value in pF

F_O is the input frequency 10 kHz ≤ F_O ≤ 150 kHz.

The RM3283 can be used with the Raytheon RM3182/RM3182A line driver to provide a complete analog ARINC 429 interface. A simple application which can be used for systems requiring a repeater-type circuit for long transmissions is given in Figure 2. More RM3182 drivers may be added to test multiple ARINC channels, as shown.

Typical Applications

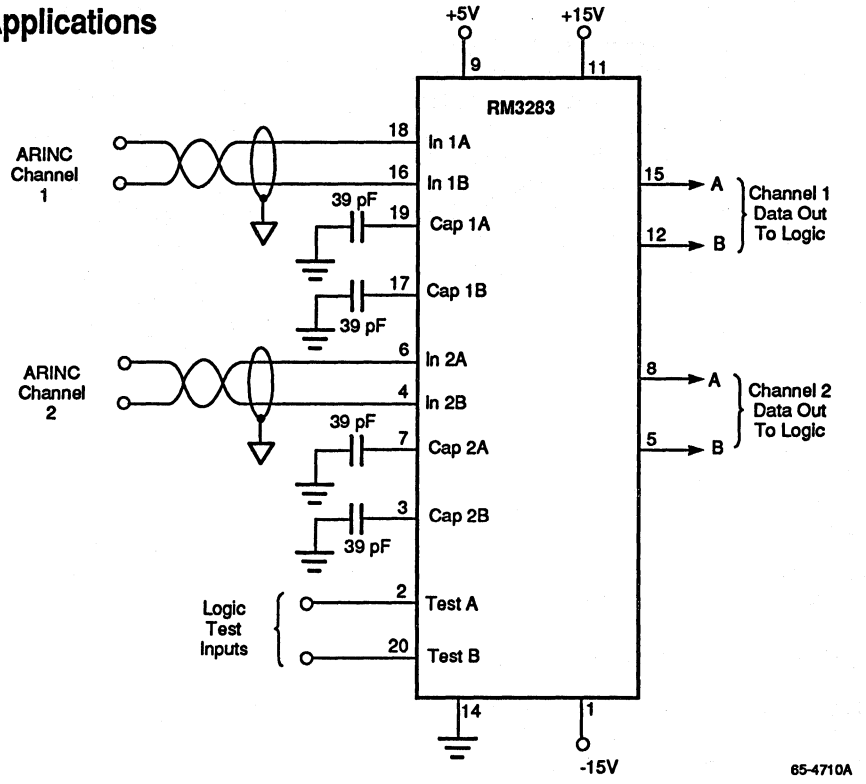


Figure 1. ARINC Receiver Standard Connection

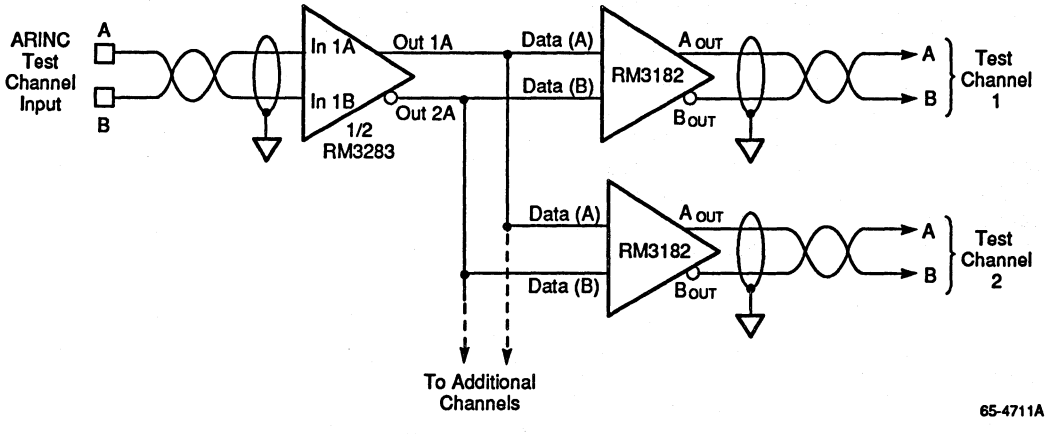


Figure 2. Repeater Circuit

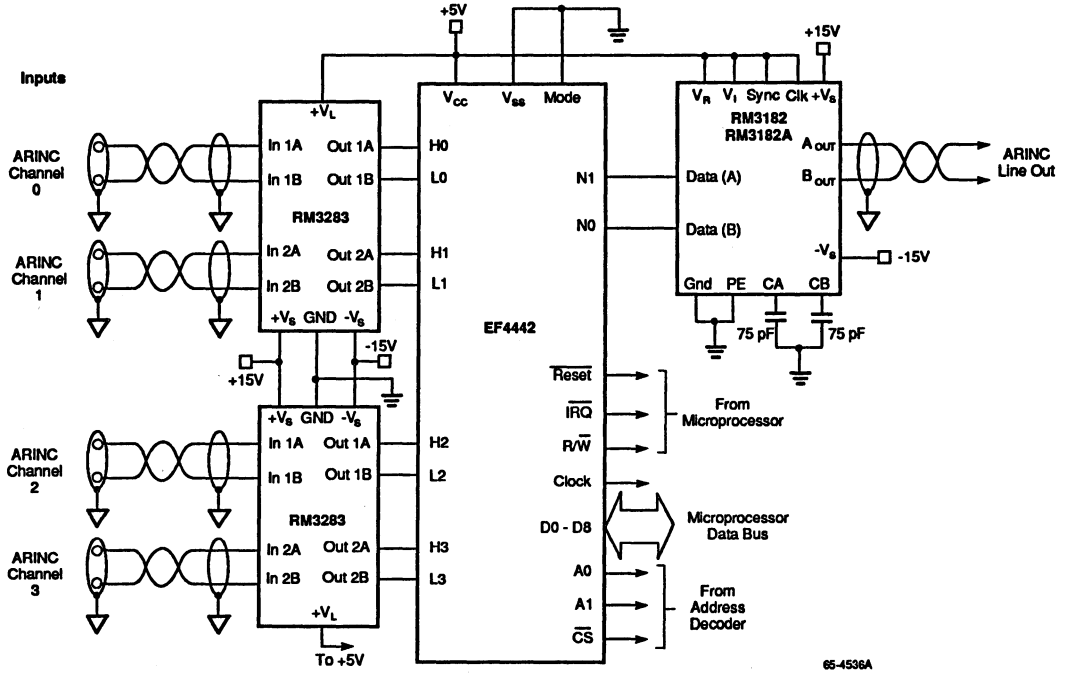
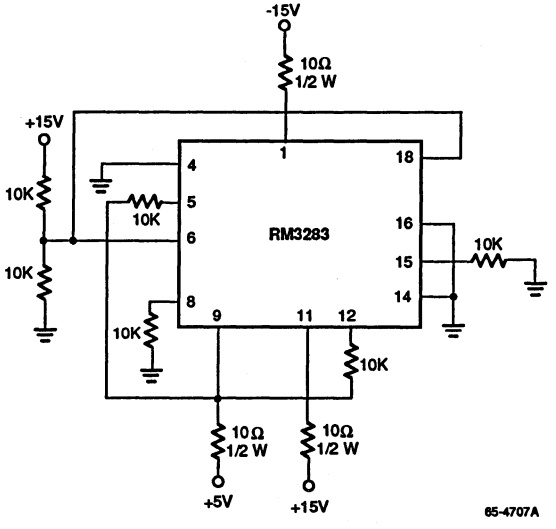
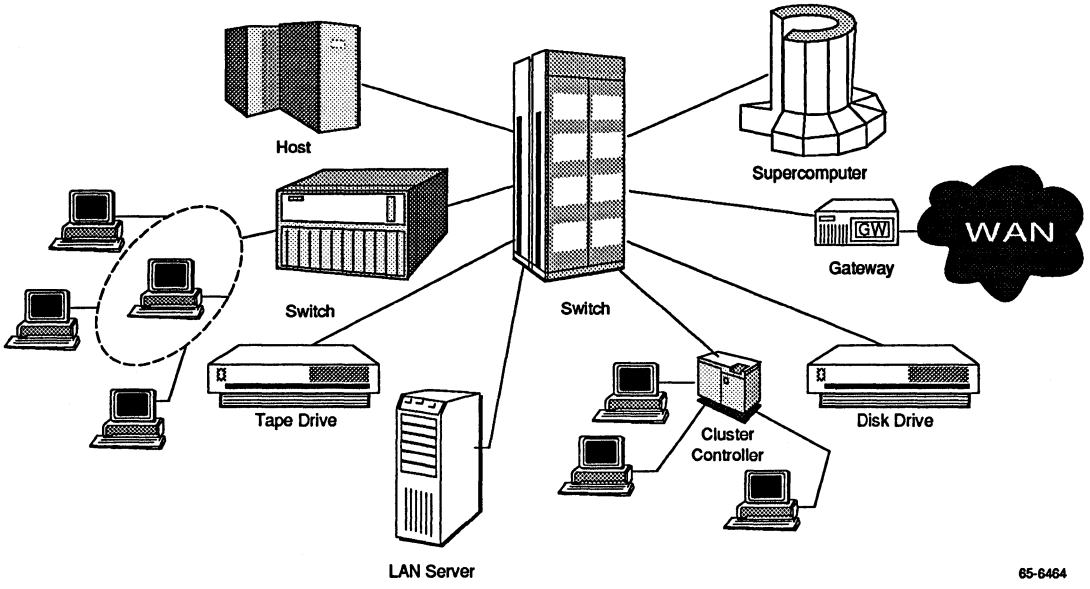


Figure 3. Four-Channel ARINC Receiver Circuit



Burn-In Schematic Diagram

Communications



The RCC700 is a high speed transmitter, receiver (transceiver) for serial fiber optic or copper communications. It can operate at data rates of 194.40, 200.00, 265.625 Mbaud. this device together with circuitry driving a coax or a fiber optic line, forms the complete physical layer of a communication system and as such is fully compliant with the Fiber Channel Physical Layer Standard (FC-PH), Enterprise Systems Connection Architecture (ESCON) and Serial Storage Architecture (SSA). The device can also be used as the physical transport for an Asynchronous Transport Mode LAN, operating at 194.4 Mbaud. The RCC700 integrates a complete phase-locked loop clock recovery and data retiming/generation subsystem, a phase-locked loop clock synthesizer, a 10:1 MUX and a 1:10 DeMUX, and an 8B/10B encoder/decoder. The device is implemented in a submicron CMOS process which offers the possibility of back integrating the protocol circuitry for the network as well.

The RCC521 is a Synchronizer/Framer that will find its applications primarily in a Synchronous Optical Network (SONET) and ATM 155.52 Mb/s physical transport. SONET is an international, digital standard for fiber optic communications and is expected to become the transport backbone of the broadband network of the future. It defines a multiplexing hierarchy that starts with a data rate of 51.84 Mb/s (OC1) and goes to 2488.2 Mb/s (OC48) in multiples of OC1. The RCC521 provides the frame recognition and synchronization functions required of a SONET line interface at 155.52 Mb/s (OC3). The device has on chip phase-locked loops for clock generation and clock and data recovery. It provides frame recognition, byte alignment, scrambling/descrambling, bit interleaved parity generation/checking and alarm generation in accordance with CCITT and ANSI standards. The device also satisfies the requirements in Bellcore TR-NWT-000253.

RCC700
ATM/ESCON™/Fibre Channel/SSA™ Transceiver
200 or 265.625 Megabaud

Description

The RCC700 is a monolithic transmitter/receiver IC integrating a complete phase-locked loop clock recovery and data retiming/regeneration subsystem, a phase locked loop clock synthesizer, a 10:1 Mux, a 1:10 Demux, an 8b/10b Encoder and a 10b/8b Decoder. It operates with a single +5V power supply. The RCC700 provides a complete physical interface in compliance with the Fibre Channel Physical Layer Standard (FC-PH), Enterprise Systems Connection Architecture (ESCON) and Serial Storage Architecture (SSA) specifications. It can also be used for the transport of Asynchronous Transfer Mode (ATM) LAN operating at 194.4 Mbaud (155.52 Mb/s OC-3 data rate with 8b/10b overhead).

The RCC operates at 194.4/200 Megabaud when FS is at a level high and at 265.625 Megabaud when FS is low (i.e. Gnd).

Features

- 200 or 265.625 Megabaud data rates
- Compliant with the Fibre Channel and ESCON standards
- PLL clock and data recovery
- Clock synthesizer
- On-chip lock detect circuitry
- 8b/10b Encode/Decode
- Parity generate/check
- Low power dissipation: 600 mW (typ) @ 200 Mbaud
- Byte sync on K28:1, K28.5 or K28.7
- Single power supply: +5V
- TTL compatible parallel data inputs/outputs
- PECL compatible serial data inputs/outputs
- Available in 68-pin PLCC and 64-pin PQFP

Applications

- Fibre Channel, ESCON, and SSA transceiver
- ATM transceiver
- High-speed fiber optics or coax links
- High-resolution graphic display terminal
- High-speed test equipment
- Video data transmission

Ordering Information

Part Number	Package	Operating Temperature Range
RCC700 PL	PL	0°C to +70°C
RCC700PQ	PQ	0°C to +70°C

Notes:
PL = 68-Pin PLCC package
PQ = 64-Pin PQFP package

Absolute Maximum Ratings[1]

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature Range ..... -55°C to +150°C
Lead Temperature Range (Soldering 10 sec.) ..... 300°C
Positive Power Supply, V_{CC} ..... 0 to 6V
Voltage Applied to Any TTL Inputs ..... -1 to 6V
Voltage Applied to Any PECL Inputs ..... -1 to 6V
Voltage Applied to Any CMOS Outputs ..... -1 to 6V
Voltage Applied to Any PECL Outputs ..... -1 to 6V
Current from Any CMOS Outputs ..... -50 to 50 mA
Current from Any PECL Outputs ..... -50 to 50 mA
Voltage Applied to V_{REF} Output Voltage ..... -1 to +6V

Notes:
1. "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

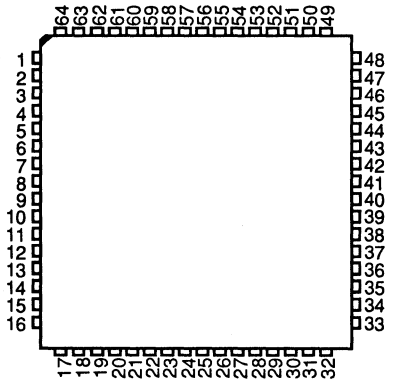
Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_A	**Ambient operating temperature**	**0**		**70**	**°C**
V_{CC}	**Positive supply voltage (DVCC and AVCC)**	**4.75**	**5.0**	**5.25**	**V**
R_l	**PECL differential load resistance [2]**	**80**	**100**	**150**	**Ω**

Notes
2. Differential load resistance of 100Ω equals connection of 50Ω to AC ground on each of DOUT, $\overline{DOUT}$.

Connection Information

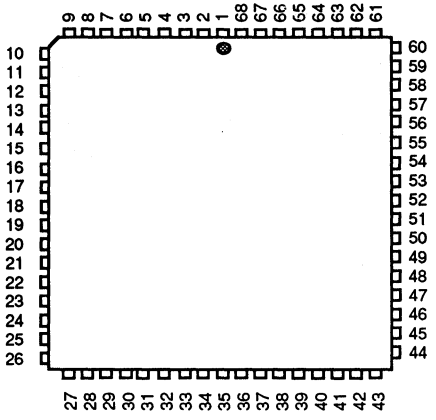
64-Pin PQFP Package
(Top View)



Note: Contact factory for 64-pin PQFP dimensions

Pin	Function	Pin	Function	Pin	Function
1	DO2	23	DI1	45	SDIN
2	DO1	24	DI0	46	SDIN
3	DO0	25	NC	47	FI
4	DVCC	26	TBC	48	FIN
5	DVCC	27	DVCC	49	FS
6	DGND	28	DOL	50	LD
7	DGND	29	DGND	51	SYNCEN
8	POUT	30	DVCC	52	BSYNC
9	KOUT	31	DOL	53	DVCC
10	EF	32	DGND	54	DVCC
11	RBC	33	DOUT	55	DVCC
12	PE	34	DOUT	56	DGND
13	NC	35	LSEL	57	DGND
14	PIN	36	AVGND	58	DGND
15	PIN	37	AVCC	59	D07
16	ETX	38	AVCC	60	D06
17	DI7	39	AGND	61	D05
18	DI6	40	AGND	62	DO4
19	DI5	41	AVCC	63	DO3
20	DI4	42	AVCC	64	DGND
21	DI3	43	AGND		
22	DI2	44	SDOUT		

68-Pin PLCC Package
(Top View)



Pin	Function	Pin	Function	Pin	Function
1	DGND	24	PIN	47	LSEL
2	DGND	25	KIN	48	AGND
3	DGND	26	ETX	49	AVCC
4	DO7	27	NC	50	AVCC
5	DO6	28	DI7	51	AGND
6	DO5	29	DI6	52	AGND
7	DO4	30	DI5	53	AVCC
8	DO3	31	DI4	54	AVCC
9	NC	32	DI3	55	AGND
10	NC	33	DI2	56	SDOUT
11	DO2	34	DI1	57	SDIN
12	DO1	35	DI0	58	SDIN
13	DO0	36	GND	59	DIN
14	DVCC	37	TBC	60	DIN
15	DVCC	38	DVCC	61	NC
16	DGND	39	RST	62	FS
17	DGND	40	DGND	63	LD
18	POUT	41	DVCC	64	SYNCEN
19	KOUT	42	DOL	65	BSYNC
20	EF	43	NC	66	DVCC
21	RBC	44	DOUT	67	DVCC
22	PE	45	DOUT	68	DVCC
23	NC	46	VREF		

Pin Definitions

Name	Function
DVCC	Positive supply for digital circuitry. The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
AVCC	Positive supply for analog circuitry. The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
DGND	Chip ground for digital circuitry. DGND should be connected to the printed circuit board's ground plane at the pins.
AGND	Chip ground for analog circuitry. AGND pins should be connected to the printed circuit board's ground plane at the pins.
DI0-DI7	Transmitter input data (TTL levels).
TBC	Transmit Byte Clock (TTL levels). Input reference frequency for the internal high speed clock generator: 20 MHz or 26.5625 MHz.
KIN	K character indicator input (TTL levels).
PIN	Odd parity input (TTL levels).
PE	Parity Error indicator output (TTL levels). PE will stay low when the on-chip calculated odd parity matches the incoming parity PIN. If there is a parity error, the PE flag is raised to a level high.
$\overline{\text{DOUT}}$ DOUT	Transmitter differential output data (PECL levels). The output is a current mode driver with a nominal current driver of 12 mA. To generate a 1.2V swing, use a 100Ω resistor across DOUT, $\overline{\text{DOUT}}$.
DOL	Data Output Low controls inputs (TTL levels). When high, it forces the output to a logic low state (DOUT = LOW and $\overline{\text{DOUT}}$ = HIGH) to protect the fiber optic source. Connect to GND or leave open when not used.
VREF	Data output threshold reference to provide ease of interfacing to a single-ended input.
LSEL	(TTL levels) Internal differential loopback for "on-board" diagnostic of the device. When loop select (LSEL) is high, the receiver accepts the output data from the transmitter section (DOUT/$\overline{\text{DOUT}}$). When LESL is low, i.e., tied to GND, the receiver accepts the incoming input data (DIN/$\overline{\text{DIN}}$). Connect to GND or leave open when not used.
$\overline{\text{DIN}}$/DIN	Receiver differential input data (PECL levels).
SYNCEN	Byte Synchronization Enable (TTL levels). When SYNCEN is high, the RCC700 will automatically resynchronize the demultiplexer to byte align with the received K28.1, K28.5 or K28.7 for both negative and positive running disparities (RD- and RD+). Connect to GND or leave open when not used.
BSYNC	Byte Synchronized output flag (CMOS levels). BYSNC goes to a HIGH level for one byte clock when SYNCEN is high and the RCC700 detects and resynchronizes on K28.1, K28.5 or K28.7.
$\overline{\text{SDIN}}$, SDIN	PECL input of the PECL to CMOS converter for the signal detect flag of the fiber optics receiver module. Leave open when not used.
SDOUT	CMOS output of the PECL to CMOS converter for the signal detect flag of the fiber optics receiver module.
DO0...7	Receiver output data (CMOS levels).
KOUT	K character indicator output (CMOS level).
POUT	Odd parity output (CMOS level). POUT is high when the parity of the DO0/D07 byte is odd.
RBC	Receive Byte Clock (CMOS levels): 20 MHz or 26.5625 MHz.
LD	Lock Detect output flag (CMOS levels). It is HIGH on powerup. It goes LOW on loss of lock. It remains LOW for 50 µs and cycles HIGH/LOW for every 50 µs until lock is established. In the locked state, LD remains HIGH.
EF	Error Flat output (CMOS levels). EF goes high to flag running disparity and coding violations detected during the 10B/8B decoding.
FS	Frequency Select (CMOS levels). The RCC700 operates at 200 Mb/s when FS is at a level high and at 265.625 Mb/s when FS is low (i.e., GND).
RST	Asynchronous Chip reset input. Chip is reset when RST is brought to a level high (CMOS levels).

DC Electrical Characteristics

V_{CC} = 5V ±5%, GND = 0V unless otherswise indicated)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Transmitter Section					
Vih	TTL Input Voltage High		2.0		+5.5	V
Vil	TTL Input Voltage Low		0		0.8	V
Iin	TTL Input Current		-1	±0.1	1	µA
Ci	Input Capacitance			3	10	pF
Vohp	PECL Output Voltage High	Rdiff = 100Ω	4.1	4.3	4.5	V
Volp	PECL Output Voltage Low	Rdiff = 100Ω	2.9	3.1	3.3	V
Io	PECL Output Current			12		mA
VREF	Output Threshold Reference		.45 (Vohp +Volp)		.55 (Vhp +volp)	V
IREF	VREF Output Current		1			mA
	Receiver Section					
Vih	TTL Input Voltag High		2.0		+5.5	V
Vil	TTL Input Voltage Low		0		0.8	V
Iin	TTL Input Current		-1		1	µA
Vcm	Com. Mode Range (DIN, $\overline{DIN}$)		2		5	
Vdiff	Diff. Input Voltge (DIN, $\overline{DIN}$)		0.2		5.5	V
Iip	PECL Input Current		-100			1
µA						
Vohc	CMOS Output Voltge High		3.5		VCC	V
Volc	CMOS Output Voltage Low		0		0.5	V
Iolc	Output Current		1			mA
ICC	Supply Current (200 Mb)			120		mA
	(265 Mb)			140		mA
PD	Power Dissipation (200 Mb)	Note 3		600		mW
	(265 Mb)			700		mW

Notes:
3. Under both transmit and receive output switching conditions.

AC Electrical Characteristics

(V_{CC} = 5V ±5%, GND = 0V unless otherwise indicated)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	Transmitter Section					
Fref	Input Clock reference frequency	FS = 0 (GND)		26.5625		MHz
		FS = 1		20		MHz
tacq	Acquisition time	Note 2			1	ms
tids	DIN0..7, KIN, PIN valid to TBC↑ setup		4			ns
tidh	TBC↑ to DIN0..7, KIN invalid hold		4			ns
Fout	Output data rate	FS = 0 (GND)		265.625		Mb/s
		FS = 1		200		Mb/s
tr, tf	DOUT, $\overline{\text{DOUT}}$ rise and fall times	20% to 80% points			500	ps
trj	DOUT, $\overline{\text{DOUT}}$ pk-pk random jitter	Note 3		300		ps
tdj	DOUT, $\overline{\text{DOUT}}$ pk-pk deterministic jitter	Note 4		100		ps
	Receiver Section					
fcc	Input data rate variation				±1000	ppm
D	Input data transition density to acquire and maintain lock		0.2			
tacq	Loop acquisition time for 10E-12 BER				2500	bits
fc	Loop capture range		±1000			ppm
tri, tfi	DIN, $\overline{\text{DIN}}$ input rise and fall time	20% to 80% points			1	ns
tj	DIN, $\overline{\text{DIN}}$ input peak to peak jitter	Note 5			0.07T	ns
tH	RBC pulse width high		0.45T	0.5T	0.55T	ns
tL	RBC pulse width low		0.45T	0.5T	0.55T	ns
tld1	LD assert delay			60		µs
tld2	LD pulse width			50		µs
tod	RBC↑ to DO0..7, KOUT, POUT delay					
	200 Mbaud		20		35	ns
	265.5625 Mbaud		13.8		23.8	ns
T	RBC period	FS = 0		37.7		ns
f		FS = 1		50.0		ns

Notes:

1. Test conditions (unless otherwise indicated): PECL input rise and fall times ≤2 ns, RLOAD = 100Ω across DOUT, $\overline{\text{DOUT}}$ VBB = 3.7V; TTL input rise and fall times ≤15 ns. Receiver input data rate = 200 or 256.625 Mb/s ±1000 ppm; transition density ≥0.25.
2. Acqusition time is the time to establish lock once the device is pwoered up to the operating VCC range.
3. Input test patter K28.7. Jitter measured at 50% amplitude, for a BER of 10E-12.
4. Input test pattern K28.5. Jitter measured at 50% amplitude.
5. Guaranteed by design.

Transmitter Section

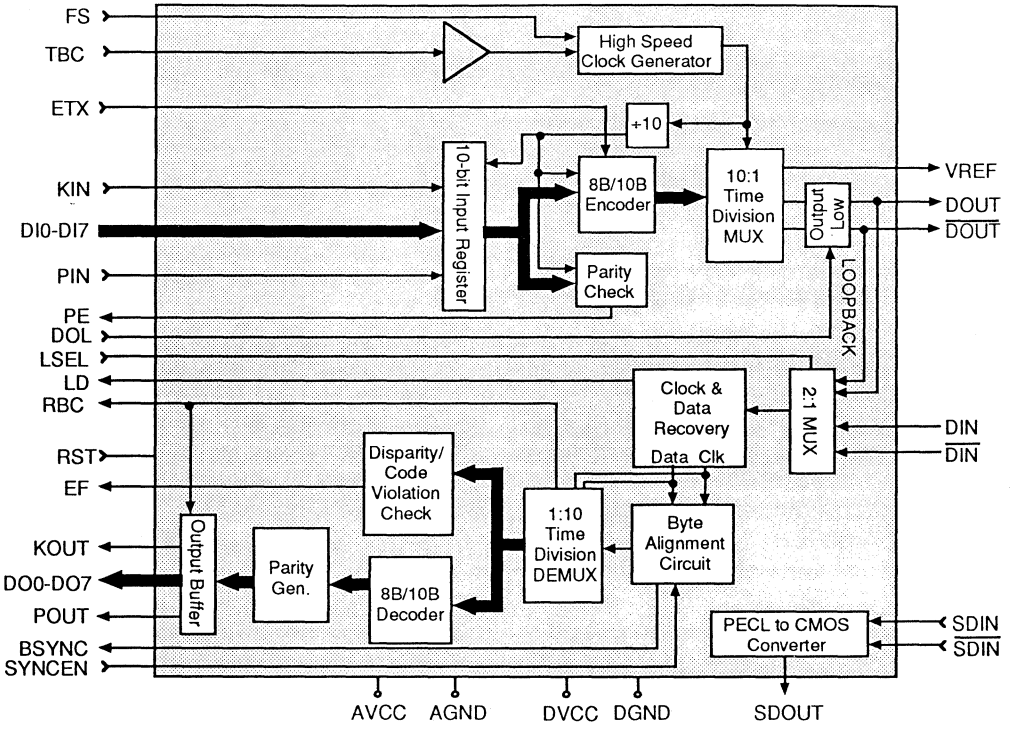
The RCC700 transmitter section includes a phase-locked loop synthesizer, an 8B/10B encoder, an input parity checker and a 10:1 multiplexer. The RCC700 accepts a CMOS data byte (DI0-DI7) along with the K character indicator (KIN) and parity bit (PIN).

The Parity Check circuitry calculates the odd parity of the input data byte and compares it with PIN. If the calculated parity differs from PIN, the transmitter flags the error by bringing the parity error bit, PE, to a HIGH level. For example, for DI0-DI7 = 00000101, PIN should be 1. If PIN is not equal to 1, PE = 1.

The RCC700 transmitter section encodes the CMOS input data byte DI0 to DI7) into a 10-bit word using IBM's 8B/10B coding (see Table 1) The encoded word is then converted to a serial high speed data stream (DOUT/DOUT) at 200 or 265.625 Mbauds via a 10:1 Time Division Mux. The serial data stream (DOUT/DOUT) is transmitted at PECL levels (positive shifted ECL levels, Vth = +3.7V). in 68-pin PLCC package, a data output threshold reference, VREF, is provided for ease of interfacing to single-ended inputs. However, differential connections are recommended.

The RCC700 features a Data Output Low function (DOL) that can force the data output (DOUT) to LOW for protection of the fiber optic module transmitter diode. DOL is controlled by the Protocol IC or the fiber optic transmitter module. The RCC700 also incorporates an Error Transmit input (ETX). The RCC700 sends a violating code when ETX is brought to a logic HIGH. If ETX stays HIGH for more than one word clock cycle, the transmitter will send error bytes of alternate running disparities in order to maintain the DC balance of the line (100111 1011 or 011000 0100).

The 200 or 265.625 MHz clock used for the serial stream is generated using a PLL clock generator which multiplies the input frequency, 20 or 26.5625 MHz, by a factor of 10. A Frequency Select pin (FS) is used to set the VCO center frequency. The VCO is set for 200 MHz operation when FS is at a CMOS logic HIGH and 2675.625 MHz when FS is at a CMOS logic LOW. The input clock reference for the PLL clock generator, Transmit Byte Clock (TBC), typically comes from a crystal oscillator or from the system.



Receiver Section

The RCC700 receiver section includes a complete phase-locked loop clock recovery and data retiming/ regeneration subsystem, a byte alignment circuit, a 1:10 demultiplexer, an 8B/10B decoder, a disparity/code violation checker and a parity generator. The RCC700 accepts a differential PECL (positive shifted ECL levels, VH = 3.7V) data stream (DIN/DIN) at 200 Mbauds or 265.625 Mbauds, recovers the clock and regenerates the encoded serial data. The recovered encoded data is then converted to 10 parallel data lines via 1:10 time division demultiplexer and decoded into an -bit byte via the 8B/10B decoder. K Command characters are also detected and indicated by bringing the KOUT pin to a HIGH level. The odd parity of the output 8-bit byte (DO0-DO7) is calculated and available at pin POUT. For example, for DO0-DO7 = 00000101, POUT should be 1. The RCC700 also generates a Receive Byte Clock (RBC) for driving the CMOS protocol layer IC. All the outputs to the protocol layer IC are at CMOS levels.

Running disparity and coding is checked during the 10B/ 8B decoding and violations are flagged by bringing the Error Flag (EF) to a HIGH level. If consecutive bytes have more 1s or more 0s, or if running disparity is different from expected for the received code, or the transmission character s not part of Table 1, EF goes HIGH. If 100111 1011 or 011000 0100 is received, EF=1, KOUT=1, DO0-DO7=00000000.

The RCC700 contains a byte synchronization circuitry. When enabled (SYNCEN high), the RCC700 will automatically resynchronize the demultiplexer to align with the leading seven bits (00111 11 or 11000 00) of the transmission character, corresponding to reception of K28.1, K28.5 or K28.7).

SYNCEN pin gives the protocol layer IC the flexibility to request the RCC700 to align only when required, e.g. at power up or after loss of word synchronization.

The RCC700 also incorporates a Lock Detect (LD) output to alert the protocol layer circuit when the incoming data is phase-locked to the VCO frequency. The LD output is normally HIGH on powerup. In the event of loss of lock, the lock detect (LD) flag changes to a LOW state and stays LOW for about 50 µs. It then cycles HIGH and LOW approximately every 50 µs until the Clock and Data Recover circuit is phase-locked to the incoming data. In the locked state, LD remains HIGH. The RCC700 also incorporates a PECL to CMOS converter to translate the PECL output signal from an optical receiver module SDIN/SDIN to a CMOS output signal. This allows for direct interfacing with the CMOS protocol layer circuit. SDIN is active high. Therefore, SDOUT will be at a CMOS level high when an optical signal is present at the input of the fiber optics receiver module.

Loopback Test Mode

The RCC700 features an internal differential loopback for "on-board" diagnostic of the device. When loop select (LSEL) is high, the receiver accepts the output data from the transmitter section (DOUT/DOUT). When LSEL is low, i.e., tied to GND, the receiver accepts the incoming input data (DIN/DIN).

Use of Table 1 for Encoding/Decoding

The following information describes how Table 1 can be used for generating valid transmission characters (encoding) and checking the validity of received transmission characters (decoding).

The transmission character s labelled "abckefghj." The transmission order is a,b,c,...j in that order. HGFEDCBA corresponds to the data inputs DI7...DI0 in that order. In the table, each valid data byte and special code byte has two columns representing two transmission characters. The two columns correspond to the current value of the running disparity (CURRENT RD- or CURRENT RD+). Running disparity is a binary parameter with either the value + or -.

The transmitter calculates the new running disparity based on the contents of the transmitted character. Similarly, the receiver calculates the new running disparity based on the contents of the received character.

The first 6 bits of the character, "abcdei," form one sub-block and "fghj" form another sub-block for computing running disparity. Running disparity (CURRENT RD+ or CURRENT RD-) at the beginning of the six-bit sub-block is the running disparity at the end of the last transmission character. Running disparity at the beginning of the four-bit sub-block is the running disparity at the end of the six-bit sub-block. Running disparity at the end of the transmission character is the running disparity at the end of the four-bit sub-block.

Running disparity at the end of sub-block is positive, if it contains more 1s than 0s. It is also positive if it is 00111 for the six-bit sub-block and 0011 for the four-bit sub-block. Otherwise, the running disparity is the same as at the beginning of the sub-block.

CURRENT RD is used to select the transmission

character for the data byte or special code.

While decoding the received character, the column corresponding to the current value of the receiver's running disparity shall be searched for the received transmission character. If the received transmission character is found in the proper column, the transmission character is considered valid and the associated data or special code byte decoded. Otherwise, the character is considered invalid and EF pin is held HIGH for that byte. Independent of the transmission character's validity, the received transmission character shall be used to calculate a new value of running disparity.

Detection of a code violation (EF=HIGH), does not necessarily indicate that the transmission character in which the code violation was detected is inerror. Code violation may occur due to the prior error which altered the running disparity of the bit stream, but it did not result in a detectable error at the transmission character in which it occurred. An example of an error scenario where the error is flagged after it happens is shown in the figure below.

	RD	Character	RD	Character	RD	Character	RD
Transmitted character stream	-	D21.1	-	D10.2	-	D23.5	+
Transmitted bit stream	-	101010 1001	-	010101 0101	-	111010 1010	+
Bit stream after error	-	101010 1011	+	010101 0101	+	111010 1010	+
Decoded character stream	-	D21.0	+	D10.2	+	Error	+

Block Diagram

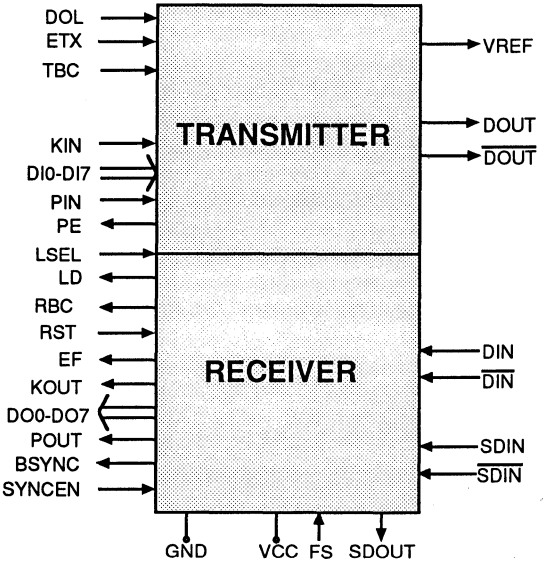


Table 1. 8B/10B Encoding

DATA[3] BYTE NAME	BITS HGF	BITS EDCBA[1]	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001

DATA[3] BYTE NAME	BITS HGF	BITS EDCBA[1]	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.3	010	11111	101011	0101	010100	0101

Table 1. 8B/10B Encoding (continued)

DATA[3] BYTE NAME	BITS HGF	BITS EDCBA[1]	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.5	100	00110	011001	1101	011001	0010
D7.5	100	00111	111000	1101	000111	0010
D8.5	100	01000	111001	0010	000110	1101
D9.5	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010

Table 1. 8B/10B Encoding (continued)

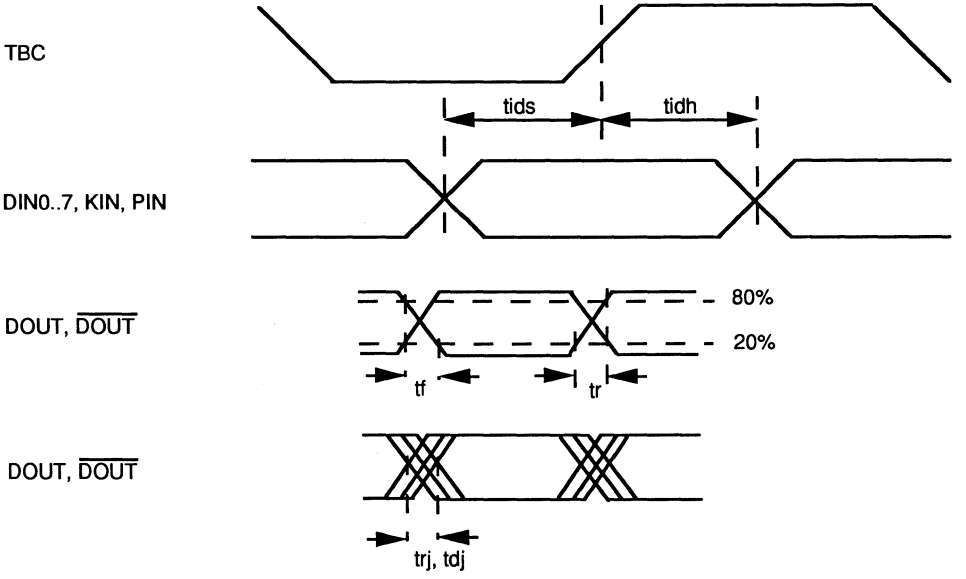
DATA[3] BYTE	BITS		CURRENT RD-		CURRENT RD+	
			abcdei	fghj[2]	abcdei	fghj[2]
D0.6	110	00000	100111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	010111	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	001100	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101011	0110	010100	0110

DATA[3] BYTE	BITS		CURRENT RD-		CURRENT RD+	
NAME	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
D0.7	111	00000	100111	0001	011000	1110
D1.7	111	00001	011101	0001	100010	1110
D2.7	111	00010	101101	0001	010010	1110
D3.7	111	00011	110001	1110	110001	0001
D4.7	111	00100	110101	0001	001010	1110
D5.7	111	00101	101001	1110	101001	0001
D6.7	111	00110	011001	1110	011001	0001
D7.7	111	00111	111000	1110	000111	0001
D8.7	111	01000	111001	0001	000110	1110
D9.7	111	01001	100101	1110	100101	0001
D10.7	111	01010	010101	1110	010101	0001
D11.7	111	01011	110100	1110	110100	1000
D12.7	111	01100	001101	1110	001101	0001
D13.7	111	01101	101100	1110	101100	1000
D14.7	111	01110	011100	1110	011100	1000
D15.7	111	01111	010111	0001	101000	1110
D16.7	111	10000	011011	0001	100100	1110
D17.7	111	10001	100011	0111	100011	0001
D18.7	111	10010	010011	0111	010011	0001
D19.7	111	10011	110010	1110	110010	0001
D20.7	111	10100	001011	0111	001011	0001
D21.7	111	10101	101010	1110	101010	0001
D22.7	111	10110	011010	1110	011010	0001
D23.7	111	10111	111010	0001	000101	1110
D24.7	111	11000	110011	0001	001100	1110
D25.7	111	11001	100110	1110	100110	0001
D26.7	111	11010	010110	1110	010110	0001
D27.7	111	11011	110110	0001	001001	1110
D28.7	111	11100	001110	1110	001110	0001
D29.7	111	11101	101110	0001	010001	1110
D30.7	111	11110	011110	0001	100001	1110
D31.7	111	11111	101011	0001	010100	1110

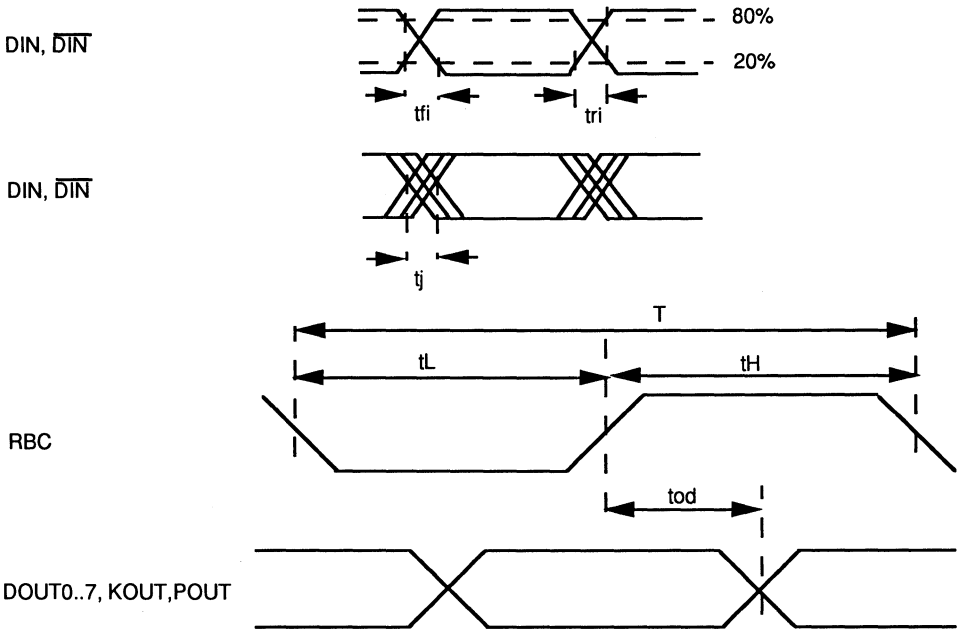
SPECIAL[4] CODE	BITS		CURRENT RD-		CURRENT RD+	
NAME	HGF	EDCBA[1]	abcdei	fghi[2]	abcdei	fghi[2]
K28.0	000	11100	001111	0100	110000	1011
K28.1	001	11100	001111	1001	110000	0110
K28.2	010	11100	001111	0101	110000	1010
K28.3	011	11100	001111	0011	110000	1100
K28.4	100	11100	001111	0010	110000	1101
K28.5	101	11100	001111	1010	110000	0101
K28.6	110	11100	001111	0110	110000	1001
K28.7	111	11100	001111	1000	110000	0111
K23.7	111	10111	111010	1000	000101	0111
K27.7	111	11011	110110	1000	001001	0111
K29.7	111	11101	101110	1000	010001	0111
K30.7	111	11110	011110	1000	100001	0111

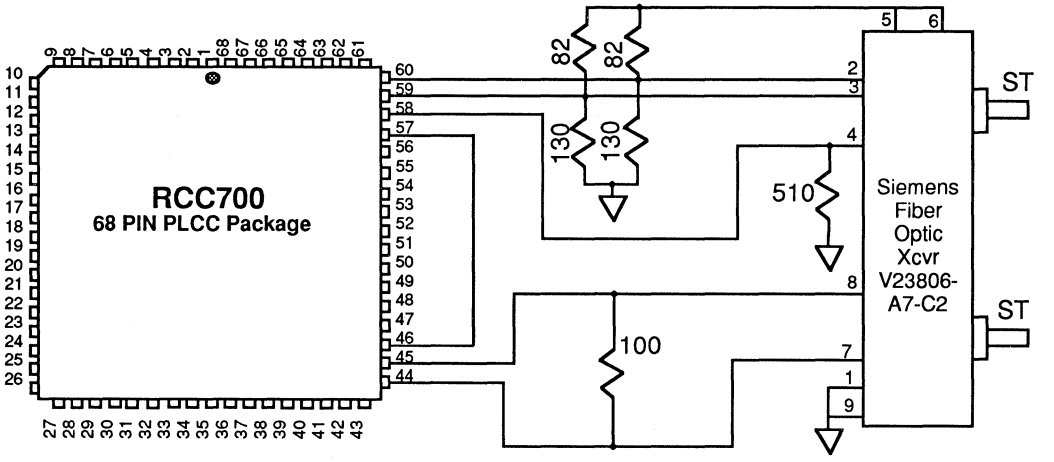
Notes:
1. "HGF EDC BA" corresponds to DI7 ...0 in that order
2. a is to be transmitted first, followed by b, c, d ....i in that order
3. Kin=0
4. Kin=1

TRANSMITTER TIMING



RECEIVER TIMING





Interconnection of RCC700 to a Fiber Optic Transceiver

RCC521
STS-3/STM-1 Synchronizer and Framer

General Description

The RCC521 STS-3/STM-1 Synchronizer and Framer provides all the frame recognition and synchronization functions required of a SONET/SDH line interface at the 155.52 Mb/s data rate. On-chip phase-locked loops facilitate clock generation and clock and data recovery. The chip provides frame recognition, byte alignment, scrambling/descrambling, bit interleaved parity (BIP-8) generation/checking, and alarm generation according to the applicable CCITT and ANSI standards. The chip also satisfies the requirements in Bellcore TR-NWT-000253.

The high speed serial line signals are provided with positive-shifted ECL (PECL) interfaces, operating off a single +5V supply, to interface directly with standard fiber-optic modules.

The RCC521 is implemented using Raytheon's high performance CMOS-D process.

In a typical SONET OC-3/SDH-1 link, the RCC521 will interface with standard fiber optic modules on the line side and with CMOS circuitry on the terminal side. The differential PECL I/O on the RCC521 permits a direct interface to standard fiber optic modules without recourse to intervening level translators. In most applications, the only high speed board traces will be two pairs of short stubs carrying serial data differentially: one from the transmit section of the RCC521 to the fiber optic transmitter module, the other from the fiber optic receiver module to the receive section of the RCC521. A list of SONET/SDH compliant fiber optic modules that are compatible with the RCC521 are given in the Application Information section.

Features

- Transmits/Receives at the STS-3/STM-1 serial data rate of 155.52 Mb/s
- Single supply (+5V) operation
- On-chip clock synthesis and clock and data recovery
- PECL I/O for direct interface to fiber-optic modules
- Detects framing sequence in serial data from network and provides deserialized byte data and 19.44 MHz byte clock to terminal
- Receives 19.44 MHz byte clock and byte data from terminal and provides serial data to network
- Transmit clock may be directly coupled in at 155.52 MHz or synthesized from external 19.44 MHz source
- Receive PLL retains lock even in the absence of transitions in 70 consecutive bit positions
- Scrambling/descrambling and BIP-8 calculation/checking with optional bypass mode
- Generates LOS(loss of signal), OOF(out of frame), LOF(loss of frame), and RFE(receive frame error) alarms
- Loopback capability at both network and terminal ends
- Test mode allows chip to be tested using an abbreviated frame
- 1.0 W maximum power dissipation
- Fabricated in Raytheon's High Performance CMOS process
- Conforms to ANSI T1.105-1991,CCITT G.708 and Bellcore TR-NWT-000253

Applications

- SONET STS-3 or SDH STM-1 line interface
- OC-3/SDH-1 Regenerators, Add/Drop Multiplexers
- ATM using SONET transport
- SONET/SDH Test Equipment

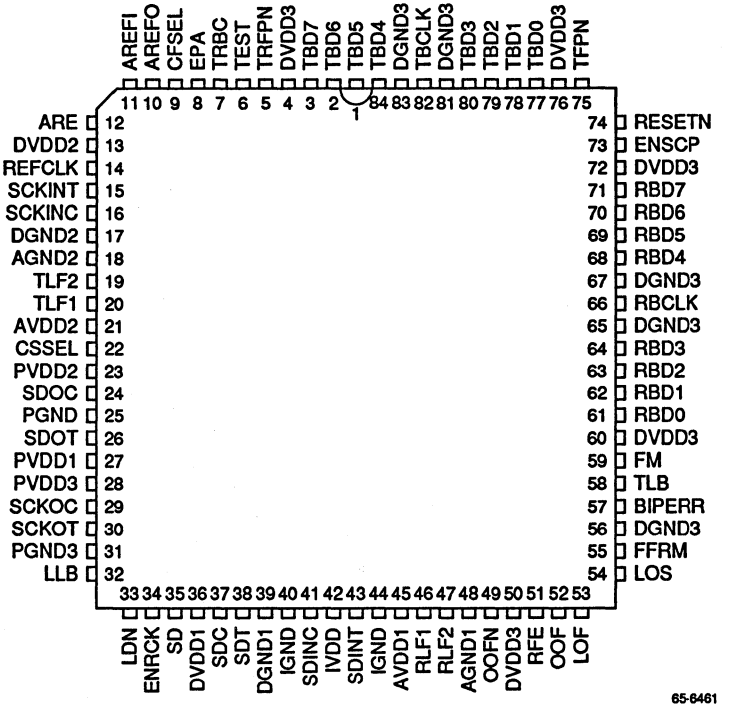
Pin No.	Signal Name	Type	Pin No.	Signal Name	Type
1	TBD5	TTL Input	43	SDINT	PECL Input
2	TBD6	TTL Input	44	IGND	PECL Ground
3	TBD7	TTL Input	45	AVDD1	Analog Power
4	DVDD3	Digital Power	46	RLF1	Analog Curent O/P
5	TRFPN	TTL Output	47	RLF2	Analog Current O/P
6	TEST	TTL Input	48	AGND1	Analog Ground
7	TRBC	TTL Output	49	OOFN	TTL Input
8	EPA	TTL Input	50	DVDD3	Digital Power
9	CFSEL	TTL Input	51	RFE	TTL Output
10	AREFO	Analog Output	52	OOF	TTL Output
11	AREFI	Analog Input	53	LOF	TTL Output
12	ARE	TTL Input	54	LOS	TTL Output
13	DVDD2	Digital Power	55	FFRM	TTL Input
14	REFCLK	TTL Input	56	DGND3	Digital Ground
15	SCKINT	PECL Input	57	BIPERR	TTL Output
16	SCKINC	PECL Input	58	TLB	TTL Input
17	DGND2	Digital Ground	59	FM	TTL Output
18	AGND2	Analog Ground	60	DVDD3	Digital Power
19	TLF2	Analog Current O/P	61	RBD0	TTLOutput
20	TLF1	Analog Current O/P	62	RBD1	TTL Output
21	AVDD2	Analog Power	63	RBD2	TTL Output
22	CSSEL	TTL Input	64	RBD3	TTL Output
23	PVDD2	Digital Power	65	DGND3	Digital Ground
24	SDOC	PECL Output	66	RBCLK	TTL Output
25	PGND	PECL Ground	67	DGND3	Digital Ground
26	SDOT	PECL Output	68	RBD4	TTL Output
27	PVDD1	PECL Power	69	RBD5	TTL Output
28	PVDD3	PECL Power	70	RBD6	TTL Output
29	SCKOC	PECL Output	71	RBD7	TTL Output
30	SCKOT	PECL Output	72	DVDD3	Digital Power
31	PGND3	PECL Ground	73	ENSCP	TTL Input
32	LLB	TTL Input	74	RESETN	TTL Input
33	LDN	TTL Output	75	TFPN	TTL Input
34	ENRCK	TTL Input	76	DVDD3	Digital Power
35	SD	TTL Output	77	TBD0	TTL Input
36	DVDD1	Digital Power	78	TBD1	TTL Input
37	SDC	PECL Input	79	TBD2	TTL Input
38	SDT	PECL Input	80	TBD3	TTL Input
39	DGND1	Digital Ground	81	DGND3	Digital Ground
40	IGND	PECL Ground	82	TBCLK	TTL Intput
41	SDINC	PECL Input	83	DGND3	Digital Ground
42	IVDD	PECL Power	84	TBD4	TTL Input

Ordering Information

Part Number	Package	Operating Temperature Range
RCC521XX	XX	0°C to 70°C
RCC521YY	YY	0°C to 70°C

Package	Order Number
84 Pin PLCC	RCC521xx
84 Pin CLDCC	RCC521yy

Pinout



65-6461

Absolute Maximum Ratings (1)

Supply voltage, AVDD,DVDD,IVDD,PVDD 7V
Voltage at any input 6V
Ambient operating temperature range ..... -40°C to 85°C
Power dissipation 1.2W
Storage temperature range ..... -65°C to +150°C
Lead temperature range
(Soldering 10 seconds) ..... 300°C

Notes:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_C	Case Oerating Temprature	-40		85	°C
V_{DD}	Positive Supply Voltage	4.75	5.0	5.25	V
P_D	Power Dissipation			1.0	W

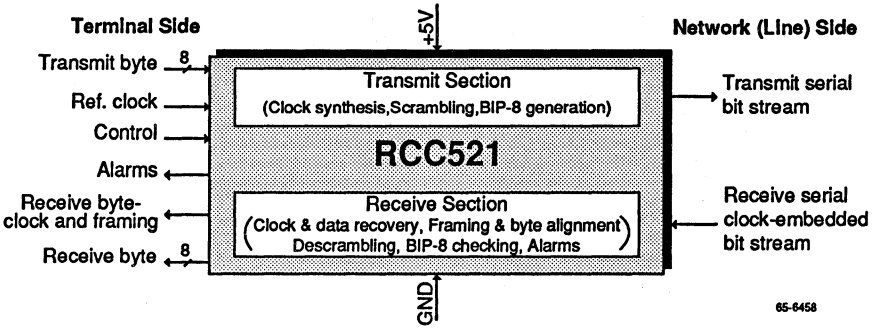


Figure 1. Simplified Block Diagram

Detailed Description

The simple block diagram of Figure 1 is shown in more detail in Figure 3. The transmit section is expanded into a Clock Generation block, a Transmit State Machine block and a Parallel-to-Serial Conversion block. The receive section consists of a Clock and Data Recovery block, a Framer block and a Receive State Machine block.

The RCC521 can operate in two modes: a "Full Framing mode" (FFRM=0) and a "Recognition Only mode" (FFRM=1). In the Full Framing mode, the RCC521 recognizes the STS-3/STM-1 framing sequence in the bit stream received from the line and then anticipates and tracks subsequent occurrences of the framing sequence in conformance with the CCITT and ANSI standards. Most applications will use the chip in this mode. In the Recognition Only mode, the RCC521 will look for the framing sequence, output a Frame Mark (FM) pulse at every occurrence of the framing sequence, and provide byte alignment based on the detected framing. It will not execute the tracking algorithm required of the ANSI and CCITT standards. This mode will only be used in when the tracking is done by a separate upstream device.

Clock Generation

The Clock Generation block generates and distributes the 155.52 MHz clock used for serial transmission. This clock may be derived in one of two ways, determined by Clock Frequency Select (CFSEL) : it may be synthesized from a reference at the byte frequency of 19.44 MHz using an on-chip phase-locked loop, or it may be coupled in externally at 155.52 MHz. If CFSEL is 1, the Clock Generation block expects a 19.44 MHz clock that conforms to the ANSI/CCITT standards to be presented at the Reference Clock (REFCLK) input pin. The on-chip PLL will synthesize the transmit clock using this reference. If CFSEL is 0, the Clock Generation block expects to receive an ANSI/CCITT compliant 155.52 MHz clock at the SCKINT (Serial Clock In True) and SCKINC (Serial Clock In Complement) pins. In this case, the on-

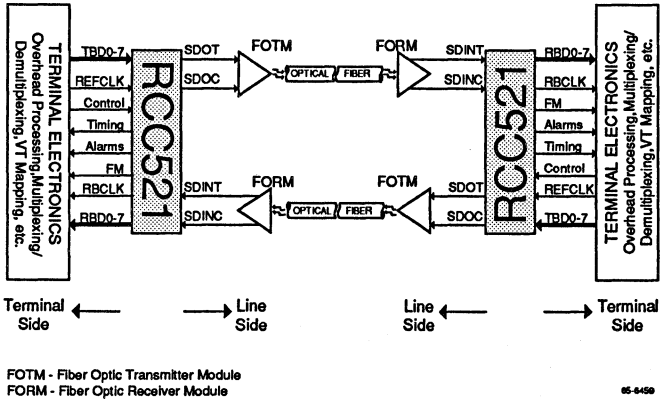


Figure 2. The RCC521 in a Typical Link

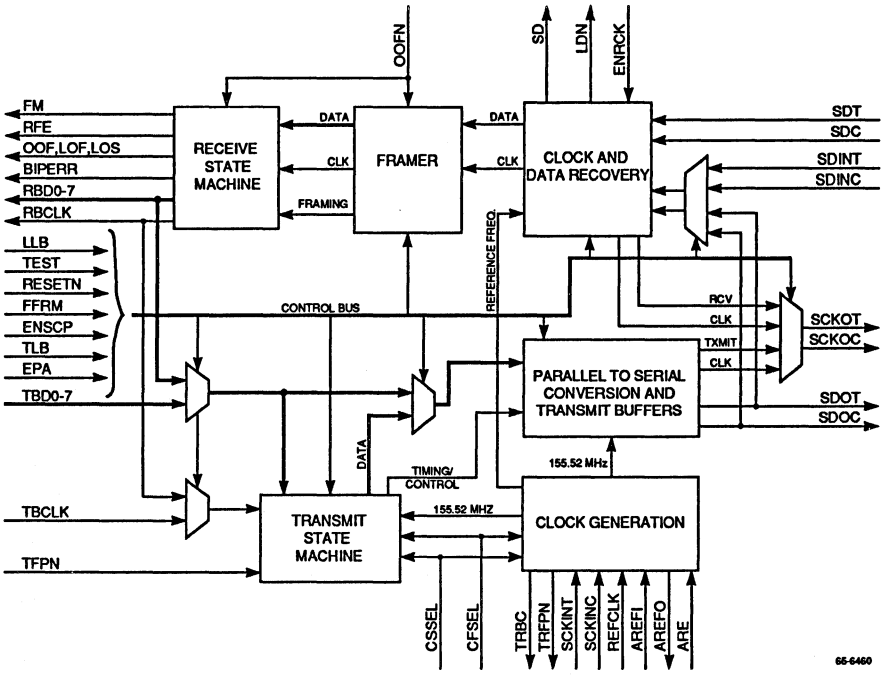


Figure 3. Detailed Block Diagram

chip PLL is bypassed and the external clock is buffered and distributed within the device. SCKINT and SCKINC are differential PECL (positive-shifted ECL) inputs.

The Clock Generation block also generates two timing reference signals, TRBC and TRFPN, based on REFCLK, which may be used by the terminal to frame and clock out the byte-wide data to the RCC521 from the transmit FIFO in the terminal. TRFPN (Transmit Reference Frame Pulse Negative) has width equal to one byte and occurs at the frame rate of 8 kHz. TRBC (Transmit Reference Byte Clock) is a symmetrical clock signal at 19.44 MHz.

The Clock Generation block also has an alternate reference circuit. The alternate reference may be used to insert a secondary timing reference, or provide a stable clock for start-up in the event the primary reference cannot be relied upon. The alternate reference may be generated in one of two ways: the first, by connecting the output from a 19.44 MHz external crystal oscillator/clock source to AREFI (Alternate Reference In), the second, by connecting a 19.44 MHz fundamental mode crystal between pins AREFI and AREFO (Alternate Reference Out). If the Alternate Reference Enable (ARE) input pin is asserted, the Clock Generation block synthesizes the serial transmit clock from the alternate reference instead of synthesizing it from REFCLK or using SCKINT/SCKINC. The ANSI/CCITT standards require Network Equipment (NEs) to provide a secondary clock source in case the primary source becomes unsuitable. The secondary clock source may be connected to AREFI and switched in using ARE. It is unlikely that an alternate reference generated using the on-chip crystal oscillator will be suitable as the secondary clock source in NEs, unless each device is individually tuned, because the frequency cannot be guaranteed to be within ±20 ppm from device to device owing to variations in semiconductor process and parasitic capacitance. However, the crystal will have to be provided, to ensure proper initialization, in Line, Loop and Through timing applications where the principal clock is derived from the SONET/SDH input to the device and a guaranteed standby clock is unavailable. The crystal provides a permanent, free-running, clock source that assures proper start-up on Power Up and Reset. This is explained below in the description of the Clock and Data Recovery block. Note, in all applications where the transmit reference is not related to the received clock, a crystal or an alternate external reference is not necessary for proper operation of the RCC521.

More information on clock generation, which includes Raytheon's solutions for clock synthesis from other reference frequencies (1.544, 2.048 and 51.84 MHz), is available in the Application Information section

Transmit State Machine

The Transmit State Machine provides the timing marks for the scrambler and the B1 parity generation circuitry. It receives the Transmit Byte Clock (TBCLK), the Transmit Frame Pulse Negative (TFPN) and the Transmit Byte Data (TBD0-7) from the terminal. TBCLK is the 19.44 MHz byte clock with which the data byte TBD0-7 is clocked into the RCC521 for subsequent serialization and transmission. TFPN provides the framing reference for the transmit section of the RCC521; it should be a pulse synchronous with the third A2 byte of the framing sequence. The terminal may derive TBCLK and TFPN from TRBC and TRFPN, respectively.

Parallel to Serial Conversion

This block serializes the TBD0-7 data byte, scrambles it, and transmits it at 155.52 Mb/s using the serial transmit clock from the Clock Generation block. Although the serial transmit clock will be exactly eight times the frequency of TBCLK, thereby obviating the need for an on-chip FIFO, the phase relationship between the two clock signals will be arbitrary. This can lead to setup and hold problems when the data byte is loaded into the Parallel to Serial Conversion block for serialization. A phase alignment circuit is used to establish adequate phase separation between TBCLK and the internal load clock which loads the data byte into the Parallel to Serial Conversion block. Once the phase relationship is established, the circuit will operate properly even if the active edge of TBCLK shifts ±6 ns relative to its initial reference position. If the Enable Phase Adjustment (EPA) pin is logic "1", the phase alignment circuit will re-establish the load clock if the active edge of TBCLK shifts outside the permitted window. If EPA is "0", the internal load clock, once established, remains fixed until a Reset is applied, no matter what TBCLK does subsequently.

Note, if EPA="1", clock wander will not cause phase realignment because TBCLK and the internal bit clock track the reference clock. A phase realignment will be necessary only if there is extreme variation in the propagation delay of TRBC through the terminal electronics to TBCLK, or if protection switching is activated. The operation of the phase alignment circuit is discussed fully in the Application Information section.

The Serial Data Output to the line side is differential (SDOT and SDOC). The output has PECL voltage levels allowing the RCC521 to drive standard opto-electronic transmitters directly.

The Enable Scrambling and Parity (ENSCP) control pin determines whether the data bytes should be scrambled and the B1 parity byte calculated and inserted, or whether the data bytes should simply be relayed through without scrambling or B1 insertion. If ENSCP="1", the scrambler is enabled three octets after the trailing edge of TFPN (i.e., after the third C1 byte). The Bit Interleaved Parity (BIP-8) is also calculated, to give even parity, for all octets in the current frame after scrambling. When the bytes of the next frame are clocked into the RCC521 from the terminal, the first B1 byte in the new frame is replaced by the BIP-8 value that was last calculated (note, BIP-8 is inserted before scrambling but calculated after scrambling). The scrambler is disabled after 2421 bytes have been transmitted. The TFPN pulse should, therefore, be synchronous with the last A2 byte of the framing pattern. This ensures that the first nine bytes of the frame (the framing pattern and the C1 bytes) are not scrambled.

If ENSCP="0", TBD0-7 is simply serialized and transmitted without scrambling or parity insertion.

The behavior of the Transmit Section immediately after Reset and Power Up are explained in detail in the Application Information section.

Clock and Data Recovery

The Clock and Data Recovery block extracts the serial bit clock from the input bit stream. This clock is the basis for all timing in the Receive Section. The Clock and Data Recovery block receives the high speed serial bit stream from the opto-electronic receiver on differential PECL inputs - Serial Data In True and Serial Data In Complement (SDINT & SDINC). It also receives the differential inputs, Signal Detect True and Signal Detect Complement (SDT and SDC), from the opto-electronic receiver. Signal Detect is a low speed PECL signal which is asserted by the opto-electronic receiver when it receives optical power above a specified threshold value.

The Clock and Data Recovery block consists of a low-jitter phase-locked loop which extracts the clock information and the data from the serial input on pins SDINT and SDINC. This phase-locked loop, which will be referred to as the Receive PLL, is separate from the phase-locked loop in the Clock Generation block. The latter, which will be referred to as the Transmit PLL, is well isolated from the Receive PLL to minimize jitter from any cross-coupling between the two and to avoid false lock. Upon power up or Reset, the Receive PLL aligns itself to the Transmit PLL using a phase-frequency comparison

scheme which allows the Receive PLL to pull-in and achieve lock even if the initial frequency discrepancy is relatively large. After the Receive PLL is locked to the transmit frequency, it will immediately re-align itself to the incoming data stream if and when Signal Detect is TRUE and transitions are detected at the SDINT and SDINC inputs. When the Receive PLL locks onto the serial input, it employs a phase-only comparison scheme along with a proprietary pulse discrimination technique to minimize jitter generation and improve jitter tolerance. By initially aligning the Receive PLL to the transmit frequency, the Receive PLL is tuned very close to the input frequency. This permits the Receive PLL to maintain a low bandwidth for jitter performance, and yet, reliably lock onto the serial input data.

The recovered 155.52 MHz Receive clock is output on differential PECL outputs SCKOT and SCKOC (Serial Clock Out True and Complement) where it may be buffered out to other devices in Line, Loop, and Through timing applications. Because the PECL buffers dissipate a fair amount of power and inject some noise into the substrate of the integrated circuit, the Enable Receive Clock (ENRCK) control pin may be de-asserted to disable the PECL buffers if the Serial Receive Clock output is not needed. If the board designer prefers not to route high speed clocks on the board, the Receive Byte Clock may be connected externally to other devices and the serial clock synthesized from the byte clock. In this case, however, the jitter will be the composite jitter from two phase-locked loops. The Receive PLL also generates a Lock Detect Negative (LDN) output which is asserted when the Receive PLL is locked to the serial input.

Because the Receive PLL needs the Transmit PLL for initialization, a circularity problem may arise in timing applications where the serial transmit clock is derived from the clock recovered on the same chip. On Power Up or Reset, the Receive PLL will look to the Transmit PLL to provide initial frequency alignment. But, the Transmit PLL cannot provide a stable clock because it derives its reference from the clock recovered by the Receive PLL. Even if the transmit reference is derived from a SONET/SDH input received on a different chip, failure of that source would again prevent initialization of the Receive PLL. To overcome this problem, the Clock Source Select (CSSEL) input is provided. If CSSEL is 0, the Serial Transmit Clock is derived in the usual manner: it is synthesized from REFCLK or derived from SCKINT/C as determined by CFSEL. If CSSEL is 1, the Serial Transmit Clock is synthesized from AREFI. If a SONET compliant clock source is not provided to AREFI as the secondary clock, a crystal will have to be provided. A clock source accurate to ±200 ppm is adequate for initialization. If LDN is connected to CSSEL, the transmitter will initialize using the secondary reference and then switch to the primary reference after the Receive PLL has successfully locked to the input bit stream. The Application Information section provides details on how the RCC521 should be hooked up in various timing configurations.

Framer

The Framer block identifies the frame boundaries and correctly demarcates the incoming serial bit stream into octets. The Receive Section of the RCC521 will enter the Seek Framing (SF) condition whenever RESETN or Out Of Frame Negative (OOFN) is asserted. More details on the operation of the RCC521 after RESETN or OOFN is asserted is given below in the Reset and Receive State Machine sections, respectively. Once in the Seek Framing condition, if FFRM="1", the Framer block will initiate the ANSI/CCITT procedure to acquire frame alignment. It will begin a serial search for the STS-3 framing pattern: three A1 (hex F6) octets followed by three A2 (hex 28) octets. When the framing pattern is recognized, the RCC521 sets the timing mark for the byte boundary and begins counting octets. If the framing pattern is accurately repeated exactly one frame later, the RCC521 enters the In Frame (IF) condition. Otherwise, the circuit resumes the search for two framing patterns which are exactly one frame interval apart. A new frame search may be initiated at an arbitrary point within the incoming data stream by simply asserting OOFN. As soon as the RCC521 enters the In Frame condition, it outputs a Frame Mark (FM) pulse and enables the byte aligned data onto RBD0-7. This is explained further in the Receive State Machine section.

In the Recognition Only Mode (FFRM="0"), when the Framer block is in the Seek Framing condition, it will search for the framing pattern and determine the frame and byte boundaries from the first framing pattern detected. The circuit will not attempt to verify framing or modify the established frame and byte boundaries based on subsequent occurrences of the framing pattern. A new search for the framing pattern must be initiated by the terminal electronics by re-asserting OOFN.

If ENSCP="1", the BIP-8 is generated for each frame of the received data before the data is descrambled. The value obtained for one frame is compared for errors with the first B1 byte of the descrambled data of the next frame. If ENSCP="0", the received data is deserialized and passed through to the terminal without descrambling.

Receive State Machine

The Receive State Machine provides the timing marks for the descrambler, the parity checker, and the other circuits in the Receive Section. It also generates the alarm signals according to the ANSI/CCITT standards and outputs the status of the B1 parity check.

The Receive State Machine divides down the recovered bit clock to generate the Receive Byte Clock (RBCLK) and synchronizes the Received Byte Data (RBD0-7) to RBCLK. The terminal clocks in the deserialized data using RBCLK. When the RCC521 enters the In Frame condition, the Receive State Machine outputs a Frame Mark (FM) pulse. This pulse is one byte wide and in phase with the third A2 byte of the framing pattern relayed on RBD0-7. If FFRM="1", the first FM pulse is output with the third A2 byte in the second of the two consecutive frames needed to take the RCC521 into the In Frame condition. If FFRM="0", the FM pulse is output with the third A2 byte of the very first frame pattern recognized.

In the Full Framing Mode, once the RCC521 is in the In Frame condition, the Receive State Machine will output FM pulses regularly, every 2430 bytes, until RESETN or OOFN is asserted. The occurrence of a spurious framing pattern within the frame will not cause re-framing or the output of an FM pulse. If the RCC521 goes Out of Frame (OOF) from an In Frame condition (OOF is described below), the Receive State Machine retains the current frame boundary until OOFN is asserted. It retains the current byte boundary until a subsequent frame acquisition is successful. Therefore, on detecting an Out of Frame condition, the OOF alarm is set, but the FM pulses, RBD0-7 and RBCLK continue based on the existing timing. As soon as OOFN is asserted to initiate a new frame search, the FM pulses stop until the new frame acquisition is successful, whereupon they resume based on the newly established frame boundary. RBD0-7 and RBCLK will continue to be output based on the old byte boundaries while the frame search is in progress, although the data may well be invalid. After frame acquisition, RBD0-7 and RBCLK will reflect the new byte boundaries when the first FM pulse corresponding to the new frame boundary is output. A pulse stretching circuit is employed to ensure that no runt pulse is output on RBCLK when it changes alignment as a result of reframing.

In the Recognition Only Mode, once the RCC521 is in the In Frame condition, the Receive State Machine will output an FM pulse every time a framing pattern is recognized. The occurrence of framing patterns will not cause realignment of byte and frame boundaries unless OOFN is asserted.

The Receive State Machine also generates the following alarm signals: Receive Frame Error (RFE), Out Of Frame (OOF), Loss Of Frame (LOF), and Loss Of Signal (LOS). The RFE and LOS alarms are generated in both the Full Frame and the Recognition Only modes. The OOF and LOF alarms are generated only if FFRM="1".

RFE: Once the RCC521 is in the In Frame condition, the Receive State Machine expects the Framer to identify the six byte framing pattern beginning 2424 bytes after the last Frame Mark. If the Framer does not recognize a correct framing pattern, a one byte wide RFE pulse is generated. RFE is output in phase with the FM pulse.

OOF: The Receive State Machine asserts the OOF alarm output as long as the RCC521 is in the OOF condition. The RCC521 will be in the OOF condition on power up, Reset, and when OOFN is asserted. It is also possible to enter the OOF condition from the In Frame condition if the incoming data is corrupt. In the Full Frame mode, the RCC521 will autonomously enter the OOF condition from the In Frame condition if erroneous framing patterns are detected in four consecutive frames. The RCC521 will re-enter the In Frame condition when two successive error free framing patterns are detected. In the Recognition Only mode, the RCC521 cannot autonomously enter the OOF condition from the In Frame condition. It can only do so if OOFN is explicitly asserted. In this case, the RCC521 enters the In Frame condition as soon as the first framing pattern is encountered.

LOF: If the OOF condition persists for 3 ms (24 frames), the LOF alarm is asserted. The LOF is de-asserted when eight consecutive error free framing patterns are received (i.e., the circuit has remained In Frame for 1 ms).

LOS: The Receive State Machine asserts the LOS alarm if Signal Detect is de-asserted or if an uninterrupted series of all ones or all zeros is received for an interval exceeding 25±5µs. The LOS is de-asserted when two consecutive error free framing patterns are detected.

If FFRM="1", the Receive State Machine will output the results of the B1 parity check on the BIP Error (BIPERR) output pin. The B1 byte that was generated for the prior frame is exclusive OR-ed with the B1 byte in the present frame to yield an error byte which has a logic 1 at every bit position that is in error. The error byte is clocked out in byte-wide pulses in phase with RBD0-7. The first pulse will be in phase with the B1 byte on RBD0-7.

Loopback

The RCC521 has loopback capability at both the terminal

and the network ends. If Terminal Loopback (TLB) is asserted, TBD0-7 is serialized as usual. However, the Clock and Data Recovery block will internally select the serial transmit data instead of the serial receive data on SDINT and SDINC. Consequently, RBD0-7 will output a delayed replication of TBD0-7. If Line Loopback (LLB) is asserted, the serial input data on SDINT and SDINC is deserialized and presented to RBD0-7. The data is also multiplexed internally, along with the receive clock, into the Transmit State Machine. The signal on SDOT and SDOC will therefore be a delayed replication of SDINT and SDINC.

Test Mode

The Test Mode is used to factory-test the chip expeditiously. If TEST is asserted, the RCC521 operates with a short frame of 16 bytes. The first six bytes constitute the framing pattern. The first nine bytes are not scrambled. The 13th byte is treated as the B1 byte. The remaining six bytes may be packed with arbitrary data. In the Test mode, the serial transmit clock is output on SCKOT/SCKOC instead of the recovered clock.

Reset

A general reset is performed by asserting RESETN (Reset Negative) for at least two byte periods. The RCC521 will automatically perform a Reset on power up. On Reset, the Transmit PLL and the Receive PLL will enter the out of lock condition and begin a new acquisition cycle. The byte counter and the scrambler in the Transmit Section will reset themselves and await TBCLK and the next TFPN pulse. Once the Transmit PLL has achieved lock, TRBC and TRFPN will be issued. The serial output will be all zeroes until transitions are present on TBCLK. The first negative going transition on TBCLK will trigger the phase alignment circuit and establish the position of the internal load clock which loads the parallel to serial converter. If ENSCP="0", valid data is presented to the serial output with the very first byte. If ENSCP="1", valid data is presented at the serial output from the beginning of the next frame (the B1 byte in the very first frame will be incorrect).

On Reset, The Receive Section will enter the Out Of Frame condition and follow the standard procedure to go In Frame. All preset alarms will be cleared. As soon as the Receive PLL commences the lock-in procedure to acquire the serial receive input, a timer is set. An OOF condition is declared when this timer expires if framing is not achieved prior to expiry. New alarms will be generated depending on how long the OOF condition persists.

Power Up

On power up, all CMOS outputs are held low until the positive supply reaches 4V(±0.5V) and then released. This assures glitch free operation on power up. A Reset is issued internally when the positive supply reaches the release voltage. The ensuing operation is identical to that described above in the Reset section.

Pin Definitions

Power and Ground

Power and ground feeds to the various functional blocks on the chip are kept separate to prevent switching noise from one block from affecting another. Many of the functional blocks have distinct power and ground pins which, at a minimum, have to be interconnected on the power and ground planes, respectively, on the printed circuit board. The Application Information section has guidelines on how optimal power distribution and supply decoupling should be done.

Symbol	Pin	Signal Name / Function
AVDD1 AGND1	45 48	**Analog VDD** and **GND** for the Clock and Data Recovery block. For optimal supply decoupling, an RF quality 0.01 µF capacitor should be connected between the pins as close as possible to the pins.
DVDD1 DGND1	36 39	**Digital VDD** and **GND** for the Clock and Data Recovery block. For optimal supply decoupling, an RF quality 0.01 µF capacitor should be connected between the pins as close as possible to the pins.
IVDD IGND	42 40,44	**VDD** and **GND** for the **PECL Inputs**. For optimal supply decoupling, an RF quality 0.01 µF capacitor should be connected between the pins as close as possible to the pins. Good isolation from supply noise should be provided on the printed circuit board. Otherwise, the jitter tolerance of the Clock and Data Recovery block will be impaired.
AVDD2 AGND2	21 18	**Analog VDD** and **GND** for the Clock Generation block. For optimal supply decoupling, an RF quality 0.01 µF capacitor should be connected between the pins as close as possible to the pins.
DVDD2 DGND2	13 17	**Digital VDD** and **GND** for the Clock Generation block. For optimal supply decoupling, an RF quality 0.01 µF capacitor should be connected between the pins as close as possible to the pins.
PVDD1 PVDD2 PVDD3 PGND PGND3	27 23 28 25 31	**VDD** and **GND for** the **PECL Outputs**. For optimal supply decoupling, an RF quality 0.01 µF capacitor should be connected between PVDD1 and PGND as close as possible to the pins. Another should be connected, likewise, between PVDD2 and PGND. PVDD3 should be decoupled to PGND3.
DVDD3	4,50 60,72 76	**VDD** for the **Digital** logic. If there is no VDD plane, each pin should be decoupled to the ground plane on the printed circuit board using RF quality 0.01 µF capacitors.
DGND3	56,65 67,81 83	**Ground** for the **Digital** logic. These pins should be connected to the ground plane of the printed circuit board.

Line (Network) Side I/O

Symbol	Pin	Signal Name / Function
SDINT SDINC	43 41	**Serial Data In True** and **Complement**. These differential PECL inputs receive the serial bit stream at 155.52 Mb/s from the line side.
SDT SDC	38 37	**Signal Detect True** and **Complement**. This low speed differential signal is received from the fiber optic receiver module. If the signal is TRUE, it indicates optical power is received by the module. If the signal is FALSE, the Clock and Data Recovery unit will not attempt to extract the timing information from the input bit stream. It will, instead, synchronize its voltage controlled oscillator (VCO) to the serial transmit frequency. If 'Signal Detect' is issued as a single-ended output by the fiber optic module, this output should be connected to SDT and the appropriate threshold should be provided to SDC (see Application Information). Note, if the user does not wish to engage the Signal Detect function, the RCC521 will operate properly if SDT and SDC are hardwired to a TRUE state. However, the standard implementation, which employs the Signal Detect, is more robust in that it offers greater immunity to false lock.
SDOT SDOC	26 24	**Serial Data Out True** and **Complement**. These differential PECL outputs transmit the serial bit stream at 155.52 Mb/s to the fiber optic transmitter module.

Pin Definitions (continued)

Line (Network) Side I/O (continued)

Symbol	Pin	Signal Name / Function
SCKOT SCKOC	30 29	**Serial Clock Out True** and **Complement.** In normal operation, these differential PECL outputs provide the serial receive clock recovered from SDINT and SDINC. In the TEST mode, these outputs provide the serial transmit clock corresponding to SDOT and SDOC. SCKOT and SCKOC should be disabled by deasserting ENRCK if the serial clock is not required for off-chip timing.

Terminal Side I/O

Symbol	Pin	Signal Name / Function
RBD0 RBD1 RBD2 RBD3 RBD4 RBD5 RBD6 RBD7	61 62 63 64 68 69 70 71	**Receive Byte Data 0-7.** The deserialized data from the line is output to the terminal on this bus. RBD7 is the MSB. It is received first.
RBCLK	66	**Receive Byte Clock.** This is a 19.44 MHz clock signal corresponding to RBD0-7. It is used by the terminal electronics to clock in RBD0-7. RBD0-7 is clocked in by the falling edge of RBCLK.
FM	59	**Frame Mark.** This is a byte-wide pulse output at the frame frequency (8 KHz) of the received signal. The pulse is active high. It lasts for the duration of the third A2 byte of the framing pattern transmitted on RBD0-7.
TBD0 TBD1 TBD2 TBD3 TBD4 TBD5 TBD6 TBD7	77 78 79 80 84 1 2 3	**Transmit Byte Data 0-7.** The octets meant for serialization are input to the RCC521 from the terminal on this bus. Transmission is big-endian, i.e., TBD7, which is the MSB, is transmitted first.
TBCLK	82	**Transmit Byte Clock.** This is a 19.44 MHz clock signal corresponding to TBD0-7. The RCC521 clocks in TBD0-7 on the falling edge of TBCLK.
TFPN	75	**Transmit Frame Pulse Negative.** This active low signal should be one byte wide and repeat at the transmit frame frequency. The RCC521 derives framing information from this signal. TFPN must be in phase with the third A2 byte of the framing pattern on TBD0-7.

Timing

Symbol	Pin	Signal Name / Function
REFCLK	14	**Reference Clock.** A reference clock at 19.44 MHz should be provided on this pin. This clock should conform to the ANSI/CCITT requirements for clocks because the Clock Generation block uses REFCLK to synthesize the serial transmit clock. In external timing applications, REFCLK will normally be a derivative of the BITS clock. In Line, Loop and Through timing applications, where the transmit clock must be extracted from the received bit stream, RBCLK may be connected externally to REFCLK.
SCKINT SCKINC	15 16	**Serial Clock In True** and **Complement.** If a compliant serial clock is available and the on-chip synthesizer is not desired, the 155.52 MHz transmit clock can be directly provided through these PECL inputs. The CFSEL control input should specify whether REFCLK or SCKINT/SCKINC is used.

Pin Definitions (continued)

Timing (continued)

Symbol	Pin	Signal Name / Function
TRBC	7	**Transmit Reference Byte Clock.** The serial transmit clock is divided down to provide a clock output at 19.44 MHz. The terminal may derive TBCLK from this output.
TRFPN	5	**Transmit Reference Frame Pulse Negative.** An inverted pulse one byte wide is output at the frame frequency by dividing down the serial transmit clock. This signal may be used by the terminal to derive TFPN.
AREFI AREFO	11 10	**Alternate Reference In** and **Out.** In External timing applications, an optional 19.44 MHz timing reference that is an alternate to REFCLK may be applied to AREFI and switched in using the ARE control pin. In timing applications where REFCLK or SCKINT/SCKINC is derived from the received data stream, an alternate reference is compulsory because the primary reference will be invalid until the Receive PLL establishes lock. If a reliable source is unavailable for AREFI, a fundamental mode crystal that will provide a 19.44 MHz ±200ppm frequency must be connected between AREFI and AREFO and the CSSEL control input must be set to a logic "1". The LDN control pin may be used to determine if the Receive PLL has established lock and then switch over to the primary reference.

Alarm Signals

Symbol	Pin	Signal Name / Function
OOFN	49	**Out Of Frame Negative.** This positive edge triggered signal is asserted by holding OOFN low for at least two byte periods (105 ns). The RCC521 acts on the rising edge of OOFN after it has been low for the requisite two byte periods. OOFN resets the Receive Section with the exception of the Clock and Data Recovery block. When OOFN is asserted, the RCC521 initiates a new frame search. Until the RCC521 gets back in frame, RBD0-7 and RBCLK will continue to be output based on the previous demarcation of byte boundaries.
RFE	51	**Receive Frame Error.** This is a one byte wide pulse output in phase with the third A2 byte of the framing pattern on RBD0-7. RFE is output only if a framing pattern is not detected where one is expected.
OOF	52	**Out Of Frame.** This active high output is asserted for as long as the RCC521 is in the Out Of Frame condition. The RCC521 will enter the OOF condition from the In Frame condition if four consecutive frames have framing pattern errors. To re-enter the In Frame condition, two consecutive error-free framing patterns must be detected. OOF is disabled if FFRM="0".
LOF	53	**Loss Of Frame.** This active high output is asserted if OOF is high for 24 frames (3 ms). OOF is de-asserted when eight consecutive error free framing patterns are detected. LOF is disabled if FFRM="0".
LOS	54	**Loss Of Signal.** This active high output is asserted if the serial input bit stream is stuck high or stuck low for more than 25±5 µS. It is de-asserted when two consecutive error-free framing patterns are detected.
BIPERR	57	**Bit Interleaved Parity Error.** If ENSCP="1", the result of the B1 parity check is output on this pin as a series of byte wide pulses in phase with RBCLK. The first BIPERR pulse denotes an error in the Bit-7 positon. This pulse is output synchronously with the B1 byte on RBD0-7. BIPERR pulses that occur in any of the subsequent seven byte intervals indicate errors in the corresponding B1 bit positions.

Pin Definitions (continued)

Control Signals

Symbol	Pin	Signal Name / Function
FFRM	55	**Full Framing Mode.** This input is active high. When FFRM is "1", the Framer block executes the full ANSI/CCITT procedure to establish framing and enter the In Frame condition. If FFRM="0", the part operates in the Recognition Only mode. In the latter case, the RCC521 establishes byte boundaries based on the first framing pattern recognized. The part then enters the In Frame condition and ceases verification of frame boundaries until OOFN is asserted.
TLB	58	**Terminal Loopback.** This input is active high. When TLB is asserted, the serial transmit data is passed through to SDOT and SDOC and also looped back internally into the Clock and Data Recovery block. The result is identical to what would be achieved if SDOT and SDOC were tied externally to SDINT and SDINC, respectively.
LLB	32	**Line Loopback.** This input is active high. When LLB is asserted, the received byte data is passed through to RBD0-7 and also looped back internally into the Transmit Section. The recovered clock is passed through and TBCLK is ignored. The result is identical to that achieved if RBD0-7 were connected externally to TBD0-7 and the receive timing substituted for the transmit timing.
ENSCP	73	**Enable Scrambling and Parity .** This input is active high. If ENSCP="1", the scramblers and the parity circuits are enabled in the Transmit and the Receive sections. On the transmit side, the BIP-8 byte that was generated for the previous frame is substituted into the B1 position of the present frame. The data is scrambled and then transmitted serially. On the receive side, the serial input data is descrambled and the B1 byte is checked against the BIP-8 byte generated from the previous frame. Any errors are reported on BIPERR. If ENSCP="0", the transmit data is serialized and passed through without scrambling and B1 substitution. The receive data is simply deserialized without descrambling. The BIP-8 circuitry is disabled and no errors are reported on BIPERR.
ARE	12	**Alternate Reference Enable.** This input is active high. If ARE="1", the Clock Generation block will internally switch its reference from REFCLK to AREFI.
TEST	6	**Test Mode.** This input is active high. If the TEST input is held high for at least one byte interval, the RCC521 will enter the TEST mode. The Test mode is incorporated in the RCC521 to ease chip test in the factory. In the Test mode, the part operates assuming an implied frame length of 16 bytes. As in normal operation, the first six bytes comprise the framing pattern and the first nine bytes are not scrambled. However, the thirteenth byte is the implied B1 byte. The other six bytes may carry random data. In the Test mode, the serial transmit clock implied by SDOT/SDOC is output on SCKOT/SCKOC instead of the clock recovered from SDINT/SDINC.
RESETN	74	**Reset Negative.** This input is positive edge triggered. RESETN must be held low for at least two byte intervals to be recognized. After this interval, the RCC521 executes a general reset on the ensuing rising edge of RESETN. On Reset, the Transmit PLL and the Receive PLL re-synchronize themselves. The Framer block enters the Seek Framing condition after giving the PLLs enough time to lock. All alarms are cleared. The transmit reference clocks are generated after the transmit PLL achieves lock. The transmit byte counter is reset and transmission resumes based on the first trailing edge of TBCLK received after the Transmit PLL has locked.
ENRCK	34	**Enable Receive Clock.** This is an active high output. When it is asserted, the serial receive clock is output on SCKOT/SCKOC in normal operation, and the serial transmit clock is output on the same pins in the Test mode. In normal operation, if the recovered serial clock is not needed for off-chip timing, ENRCK should remain deasserted to conserve power and reduce switching noise.
LDN	33	**Lock Detect Negative.** This is an active low output. LDN goes low when the Receive PLL locks onto the input bit stream on SDINT and SDINC. LDN is not asserted when the Receive PLL locks onto the transmit frequency during initial frequency alignment.

Pin Definitions (continued)

Control Signals (continued)

Symbol	Pin	Signal Name / Function
EPA	8	**Enable Phase Alignment.** This input is active high. The phase alignment circuit maintains the necessary interval between TBCLK and the internal clock which loads the parallel to serial converter in the Transmit section. If EPA="1", the phase alignment circuit will re-align the internal load clock should TBCLK drift by more than ±6ns with respect to the initial reference timing. If EPA="0", the phase alignment is established just once.
CFSEL	9	**Clock Frequency Select.** This input specifies which of two primary references are used to generate the serial transmit clock. If CFSEL="1", the Clock Generation block expects a 19.44 MHz reference on REFCLK. If CFSEL="0", the Clock Generation block expects a 155.52 MHz differential clock on SCKINT and SCKINC.
CSSEL	22	**Clock Source Select.** If CSSEL="0", the serial transmit clock is derived from the primary reference: either REFCLK or SCKINT/SCKINC. If CSSEL="1", the serial transmit clock is synthesized from AREFI.

Other

Symbol	Pin	Signal Name / Function
SD	35	**Signal Detect.** This is an active high output. The signal received on the differential PECL inputs SDT and SDC is translated to TTL levels and output on this pin.
TLF1 TLF2	20 19	**Transmit Loop Filter 1** and **2.** The passive components that comprise the loop filter for the Transmit PLL are connected to these pins. See the Application Information section for component values and their effect on loop performance.
RLF1 RLF2	46 47	**Receive Loop Filter 1** and **2.** The passive components that comprise the loop filter for the Receive PLL are connected to these pins. See the Application Information section for component values and their effect on loop performance.

DC Electrical Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	TTL Inputs					
V_{IH}	High level input voltage	DV_{DD}=4.75V	2.0			V
V_{IL}	Low level input voltage	DV_{DD}=5.25V			0.8	V
I_{IL}	Input leakage current	DV_{DD}=5.25V			10	µA
C_I	Input capacitance				3.0	pF
	Positive-shifted ECL Inputs					
V_{IH}	High level input voltage	IV_{DD}=5.0V	3.7		4.0	V
V_{IL}	Low level input voltage	IV_{DD}=5.0V	3.0		3.3	V
I_{IL}	Input leakage current	IV_{DD}=5.25V			1.0	µA
C_I	Input capacitance				8	pF
	TTL Outputs					
V_{OH}	High level output voltage	DV_{DD}=4.75V,I_{OH}=-2mA	4.25			V
V_{OL}	Low level output voltage	DV_{DD}=5.25V,I_{OL}=4mA			0.4	V
I_{OL}	High level output current				4.0	mA
I_{OH}	Low level output current				-2.0	mA
	Positive-shifted ECL Outputs					
V_{OH}	High level output voltage	PV_{DD}=5.0V,R_{DIFF}=50Ω	3.7	4.1	4.4	V
V_{OL}	Low level output voltage	PV_{DD}=5.0V,R_{DIFF}=50Ω	2.7	3.3	3.8	V
V_{OD}	Differential output voltage	PV_{DD}=5.0V,R_{DIFF}=50Ω	0.6	0.8	1.0	V
I_{OL}	High level output current	PV_{DD}=5.0V,R_{DIFF}=50Ω	13	16	19	mA
I_{OH}	Low level output current	PV_{DD}=5.0V,R_{DIFF}=50Ω	13	16	19	mA

AC Electrical Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
	TTL Outputs					
t_{RISE}	Rise time	DV_{DD}=5.0V,C_L=15pF	1.0		8.0	ns
t_{FALL}	Fall time	DV_{DD}=5.0V,C_L=15pF	1.0		8.0	ns
	Positive-shifted ECL Outputs[2]					
t_{RISE}	Rise time	PV_{DD}=5.0V,R_{DIFF}=50Ω,C_L=20pF			1.1	ns
t_{FALL}	Fall time	PV_{DD}=5.0V,R_{DIFF}=50Ω,C_L=20pF			1.1	ns
	Clock Jitter (r.m.s.)					
J_{GEN}	Jitter Generation:					
	Total jitter in the differential output (SDOT-SDOC)	f=155.52MHz,(2^{15}-1) PRBS[3] R_{DIFF}=50Ω,C_L=20pF			45	ps
	Random jitter in TRBC	REFCLK=19.44 MHz[4]			22	ps
J_{TRANSF}	Jitter Transfer:					
	Serial Receive Input to Serial Receive Clock (SDINT-SDINC) to(SCKOT-SCKOC)	(Fig. 4), Serial I/p is freq. modulated with sinusoid that generates jitter to the mask in Fig.5				
	Jitter Gain	10Hz ≤ f ≤130 kHz			0.1	dB
	Jitter Gain Rolloff	f >130 kHz	-20			dB/dec
	REFCLK/AREFI to TRBC					
	Jitter Gain	10Hz ≤ f ≤ 80 kHz			0.1	dB
	Jitter Gain Rolloff	f > 80 kHz	-20			dB/dec
J_{TOL}	Jitter Tolerance:					
	Serial Receive Input (SDINT-SDINC) amplitude penalty	Input jitter conforms to the mask in Figure 5. BER=10^{-10}			1	dB

Notes:

2. The PECL outputs are current mode outputs with a nominal current drive of 16 mA. The outputs are designed to give a nominal swing of 800 mV when used in conjunction with a differential load of 50Ω.
3. Jitter number includes data dependent and random jitter. Data dependent jitter is measured by inserting a 2^{15}-1 pseudo-random bit sequence in byte-organized fashion at TBD0-7 with the chip in the bypass mode.
4. Random jitter on TRBC is measured by applying a low-jitter (<10 ps rms) square wave to REFCLK, measuring the random jitter in TRBC on a high speed digital sampling oscilloscope, and subtracting out the trigger jitter in rms fashion.

Jitter Transfer Characteristic from the Serial Receive Input to the Serial Receive Clock

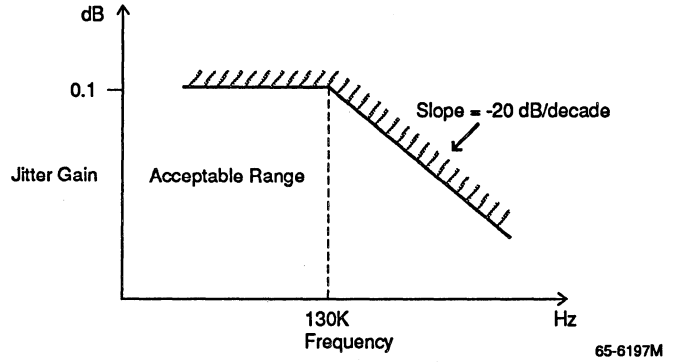


Figure 4

Jitter Tolerance Mask for the Serial Receive Input

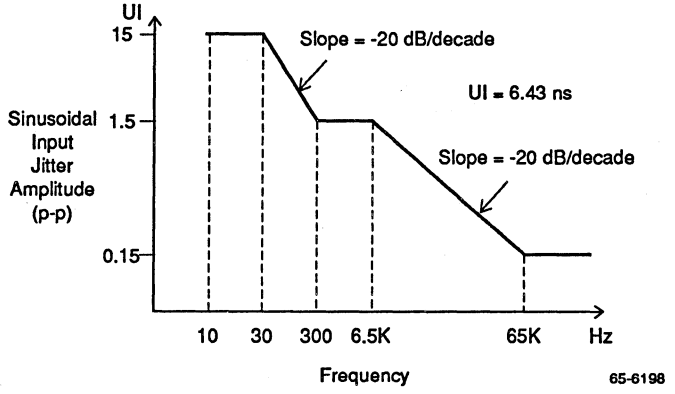


Figure 5

Timing Relationships

Symbol	Parameter Description	Min	Typ	Max	Units
T1	TBD0-7 setup time to falling edge of TBCLK	5.0			ns
T2	TBD0-7 hold time after falling edge of TBCLK	5.0			ns
T3	TFPN setup time to falling edge of TBCLK	5.0			ns
T4	TFPN hold time after falling edge of TBCLK	5.0			ns
T5	TBCLK clock period	-20 ppm	51.4403	+20 ppm	ns
T6	TBCLK pulsewidth high	18			ns
T7	TBCLK pulsewidth low	18			ns
T8	RBD0-7 output delay after the falling edge of RBCLK	0		10	ns
T9	FM output delay after falling edge of RBCLK	0		10	ns
T10	RBCLK clock period	-20 ppm	51.4403	+20 ppm	ns
T11	RBCLK pulsewidth high	22			ns
T12	RBCLK pulsewidth low	22			ns
T13	FM pulsewidth	47	51.44	56	ns
T14	Offset of rising edge of Serial Clock Out (SCKOT-SCKOC) from centre of bit cell of Serial Data Out (SDOT-SDOC) in Test Mode	-0.5		0.5	ns
T15	(SCKOT-SCKOC) pulse period	-20 ppm	6.43	+20 ppm	ns
T16	(SCKOT-SCKOC) pulsewidth low	3.0	3.215		ns
T17	(SCKOT-SCKOC) pulsewidth high	3.0	3.215		ns
T18	Delay from falling edge of TBCLK to centre of bit cell of MSB of byte output on (SDOT-SDOC)			40	ns
T19	Delay from falling edge of LSB on (SDINT-SDINC) to falling edge of RBCLK for the corresponding byte			40	ns
T20	TRFPN falling edge output delay after rising edge of TRBC	0		10	ns
T21	TRFPN pulsewidth	47	51.44	56	ns
T22	TRBC period	-20 ppm	51.4403	+20 ppm	ns
T23	TRBC pulsewidth high	22			ns
T24	TRBC pulsewidth low	22			ns
T25	RESETN pulsewidth	105			ns
T26	Delay from rising edge of RESETN to rising edge of valid TRBC			500	µs
T27	Delay from first valid rising edge of TRBC to first valid falling edge of TRFPN	0		10	ns
T28	Delay from rising edge of RESETN to leading edge of valid (SCKOT-SCKOC) when serial input is present			1.2	ms
T29	Delay from falling edge of RBCLK to leading edge of BIPERR output bit	0		10	ns

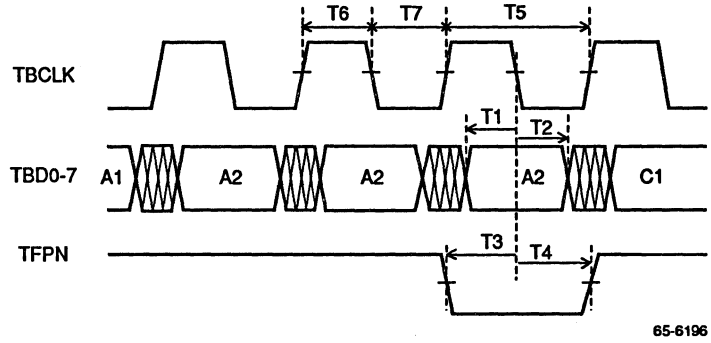


Figure 6

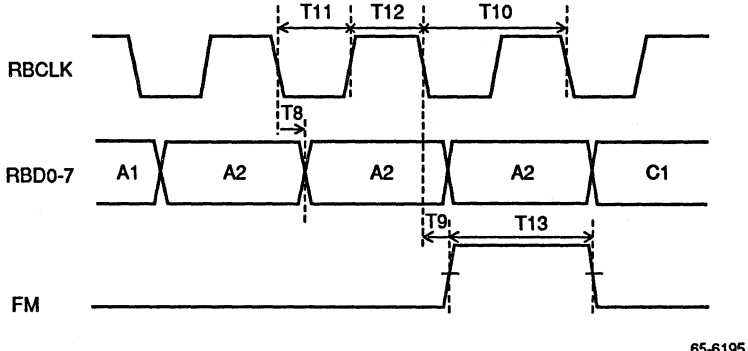


Figure 7

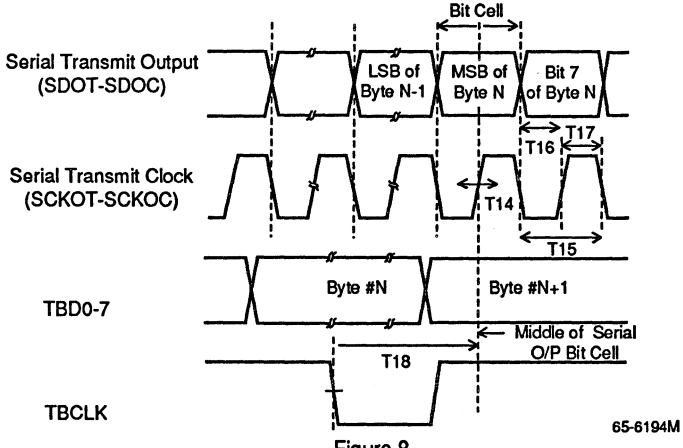


Figure 8

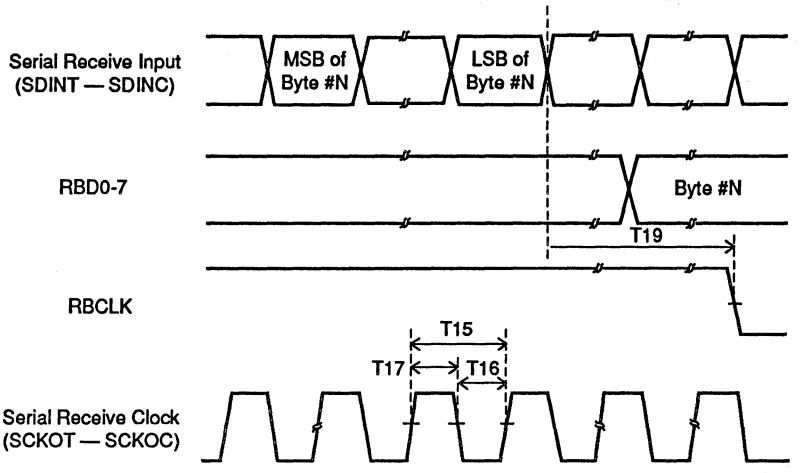
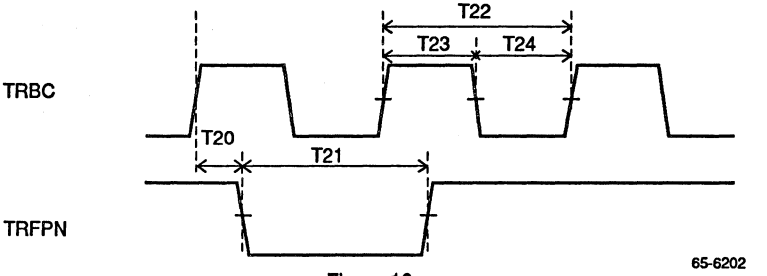


Figure 9

65-6201



65-6202

Figure 10

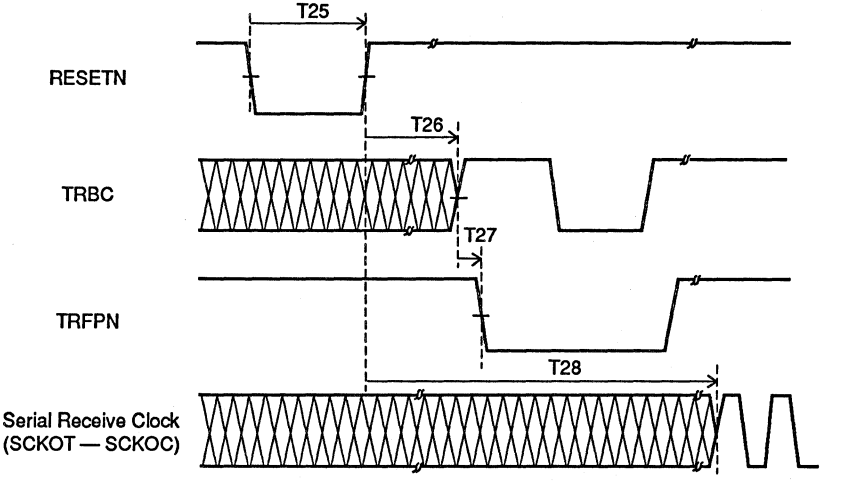


Figure 11

65-6203M

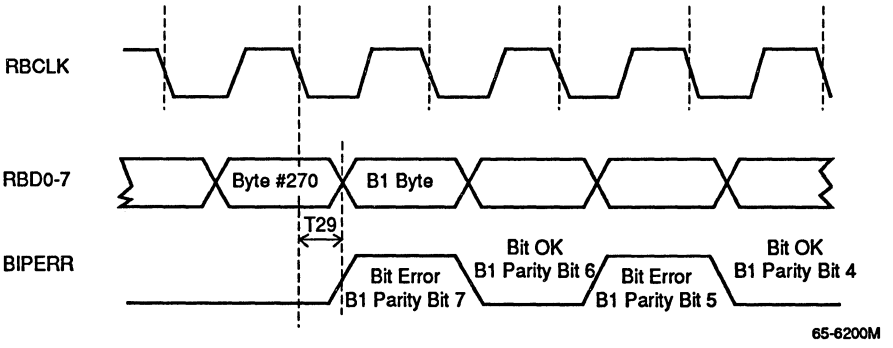

RBCLK
RBD0-7
Byte #270
B1 Byte
T29
BIPERR
Bit Error
B1 Parity Bit 7
Bit OK
B1 Parity Bit 6
Bit Error
B1 Parity Bit 5
Bit OK
B1 Parity Bit 4
65-6200M

Figure 12

Section 3
Standard Products

Raytheon Semiconductor offers a comprehensive line of standard products serving a wide variety of applications in diverse commercial, industrial and military markets. Applications that include video processing, medical imaging, data acquisition, instrumentation, guidance control systems, radar and many others.

Addressing video signal synthesis and graphics applications, to name a few, are Raytheon's A/D and D/A converters, ranging from 4-bits at 200 Msps up to 12-bits at 50 Msps.

Signal processing functions are performed by our Transform and Vector Processing, Correlator, Fixed-Point Arithmetic and Memory/Storage products.

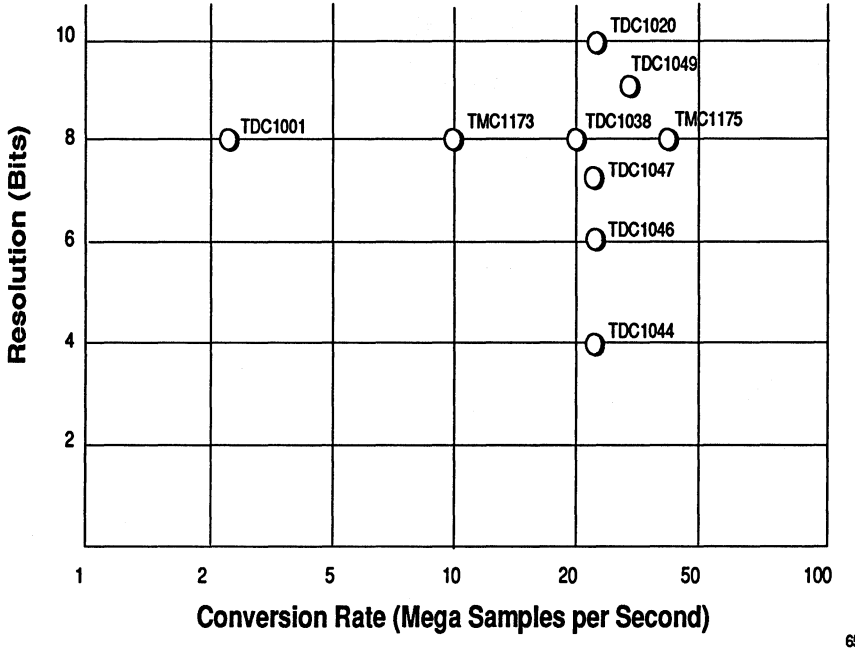
Standard Linear products have provided solutions for designers since the early 1960s. Products such as precision op amps, comparators, voltage references, DACs and regulators are manufactured using the company's own bipolar junction isolated process, and can be screened to JAN Class B.

Raytheon's PROMs include standard and power-switched versions in many different speeds and packages and have high immunity to total dose radiation, making these products especially suitable for military applications.

Small signal transistors round out Raytheon's Standard Products offering. Both sole source and industry-standard types are available, and support many existing commercial and military applications.

Contents

A/D Converters



Raytheon Semiconductor offers a line of high performance A/D converters that addresses applications requiring conversion rates from less than 1 Msps to 40 Msps. We pioneered the monolithic video A/D converter in 1977, and in 1989 received an Emmy Award for our contributions to the field of video conversion. The current offerings are the fourth generation products of Raytheon Semiconductor's commitment to quality video conversion.

For standard video bandwidth conversion, you can't beat the TMC1175 8-bit 40 Msps CMOS A/D, which is available in a 24 lead SOIC package, and consumes less than 150 mW. For low voltage applications, the new TMC1173 operates at 10 Msps with a supply voltage of 2.7 to 3.3V and only requires 90 mW.

New to the family of video converters is the TMC22070 Genlocking Video Digitizer. This fully-integrated acquisition system includes everything needed to convert analog NTSC or PAL video into a composite digital video signal. The digitizers generate a line-locked sampling clock, adjust the gain and offset of the incoming video, digitize it, and measure the phase and frequency of the color burst for further processing.

The TDC1035 is an innovative new product that digitizes the peak value of a pulse (as narrow as 12 ns) that occurs any time during a user-defined "window". It is ideal for high-energy physics experiments, electronic warfare and general purpose instrumentation.

Product	Resolution Bits	Conv. Rate [1] (Msps)	RMS/RMS SNR[1] (dB)	Package	Grade[2]	Notes
TDC1044	4	25	—	B9, N9	C, V, SMD	
TDC1046	6	25	33	B8	C, V, SMD	
TDC1047	7	20	39	B7	C, V	
TDC1147	7	15	36	B7	C, V	No pipeline delay. Well suited to subranging converter applications.
TDC1035	8	—	—	B7	C, V	Peak digitizer. Digitizes peak value of pulses as narrow as 12 ns.
TMC22071	8	15		R1	C	Genlocking digitizer with input MUX, clamp, sync separator, clock generator, subcarrier PLL
TDC1038	8	20	45	B6, N6, R3 E1	C, V	Low power version of TDC1048.
TDC1048	8	20	45	B6, N6 C3, E1	C, V, SMD	Industry standard video A/D.
TDC1058	8	20	45	B6, N6, R3, E1	C	New industry standard video A/D. Single +5V power supply. TDC1048 performance equivalent.
TMC1173-10	8	10	45	M7,N2, R3	C	Low power CMOS video A/D with integral Track/Hold. +2.7V to +3.3V power supply.
-05	8	5	45	M7, N2, R3	C	
TMC1175-20	8	20	45	B2, N2, C3, M7, R3	C, V	Low power CMOS video A/D with integral Track/Hold.
-30	8	30	45	M7, N2, R3	C, V	
-40	8	40	45	M7, N2, R3	C, V	
				E1	C	Includes TDC3310 D/A
TDC1049	9	30	48	J0, J3, C1, L1, G8, E1	C, V, SMD	ECL interface
TDC1020	10	20	55	J1, G0, E1	C, V	Monolithic video A/D, TTL interface. ±2V input range.

Notes:

1. Guaranteed. See product specifications for test conditions.
2. A = High reliability, T_C = -55°C to 125°C.
   B = Industrial, T_C = -25°C to 85°C
   C = Commercial, T_A = 0°C to 70°C.
   F = Extended Temperature Range, T_C = -55°C to 125°C
   V = MIL-STD-883 Compliant, T_C = -55°C to 125°C.
   SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C.
3. A = High reliability, T_C = -20°C to 95°C.

TDC1020
High-Speed Monolithic A/D Converter
10-Bit, 20 Msps

Description

The TDC1020 is a 20 Msps (Megasample per second) full-parallel (flash) analog-to-digital converter, capable of converting a video signal into a stream of 10-bit digital words.

All outputs of the device are TTL compatible, and will provide the conversion in unsigned magnitude, or two's complement format, and either inverted or noninverted. An output signal indicating overflow condition is also provided for added flexibility. All digital inputs to the device are TTL compatible.

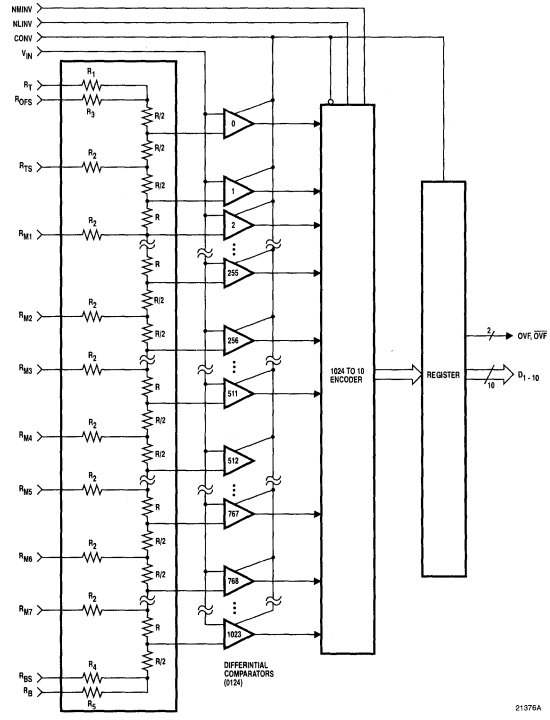
Features

- 10-bit resolution
- 20 Msps conversion rate
- Overflow flag
- Sample-and-hold circuit not required
- TTL digital interface
- Selectable output format

Applications

- Medical imaging systems
- Video data conversion
- Radar data conversion
- High-speed data acquisition
- Process control

Functional Block Diagram



Functional Description

General Information

The TDC1020 is a flash analog-to-digital (A/D) converter in which each of the 1024 comparators has one input biased at one of the transition points of the transfer function and all of the other comparator inputs are connected to the analog input signal. The output of the comparator array is sometimes referred to as a "thermometer" code as all of comparators biased at voltages more positive than the input voltage will be off and the rest will be on. The thermometer code from the comparator array is encoded into an 11-bit code (10 data bits plus an overflow bit). The format of the code that is encoded is determined by the format controls NMINV and NLINV so that the data presented to the output latches is in binary, two's complement or inverted data format.

Power and Thermal Management

The TDC1020 operates from two supply voltages, +5.0V and −5.2V. The bulk of the current drawn by the positive supply is returned through the negative supply, however, the positive supply should be referenced to digital ground (D_{GND}) and the negative supply to analog ground (A_{GND}). All power and ground pins must be connected. The maximum power is drawn at the lower limit of the operating temperature range. When the device is being operated at elevated temperatures, the power dissipation drops, however, thermal management will then be a consideration. The TDC1020 is rated for operation in a 70°C ambient temperature in still air.

The power dissipation decreases with increasing temperature. TRW specifies the absolute maximum I_{EE} and I_{CC} specifications in the *Electrical Characteristics Table*. The worst case conditions are V_{CC}=5.25V, V_{EE}=−5.5V and the case temperature equal to 0°C. The case temperature of 0°C is, however, a transient condition since the device immediately warms up and decreases its power dissipation, upon power up. For typical steady state power dissipation as a function of ambient temperature, please see *Figure 7*.

It is possible to relax the temperature requirements of the device by providing adequate heat sinking.

Reference

The bias voltages for the comparator array are provided by use of a serial chain of 1024 equal-valued resistors across which the reference voltage is applied. Seven equally separated mid-point adjustment taps are provided to allow the user to optimize the integral linearity of the device. In addition, there are sense leads on the top and bottom of the resistor chain which allow the user to minimize the offset and gain errors of the device. It is recommended that the user drive R_{M2}, R_{M4} and R_{M6} in order to obtain optimal device performance. One method for driving the references is shown in the *Typical Interface Circuit*. The reference top and reference bottom sources must be able to source or sink the reference current and since noise on these leads will lead to inaccurate conversions, they should be bypassed with a capacitor to A_{GND}. There are in addition 4 more reference taps, the use of which is not required to obtain 0.1% integral linearity. It is recommended that these pins be left open (no connection).

Format Control

There are two inputs provided on the TDC1020 which control the output format of the device. When NMINV is connected to a logic LOW, the MSB is inverted. When NLINV is connected to a logic LOW D_2 through D_{10} will be inverted. By using various combinations of these commands the user can select any of the following output data formats: binary, inverted binary, two's complement, inverted two's complement. The *Output Coding Table* shows the output formats generated for each of the control states.

Convert

The analog input to the TDC1020 is sampled at a time t_{STO} after the rising edge of the CONV signal. The output data from the 1024 comparators is encoded into the proper format and the final result is transferred to the output latches on the next rising edge. This timing is shown in the *Timing Diagram (Figure 1)*. Note that there are minimum LOW and HIGH requirements of the CONV signal (t_{PWH}, t_{PWL}) which must be met for proper device operation. In addition, the performance is generally improved if the CONV signal is LOW for as long as possible. A circuit which provides an optimized waveshape CONV signal to the TDC1020 is shown on the *Typical Interface Circuit*.

Analog Input

The analog input to the TDC1020 has an equivalent circuit shown in *Figure 2*. It should be noted that the major component of the input impedance is capacitance, and the input range is 4Vp-p. A low-impedance driving circuit is recommended for the TDC1020 to obtain good dynamic performance. All analog inputs to the TDC1020 must be connected to insure proper operation of the A/D converter.

Outputs

The data and overflow outputs of the TDC1020 are TTL compatible, capable of driving four low power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time t_{HO} after the rising edge of the CONV signal. New data becomes valid after a maximum delay time, t_D.

No Connects

There are several pins labelled No Connect (NC) which have no electrical connection to the chip. These pins should be connected to A_{GND} for best noise performance.

TDC1020 Package Interconnections

Signal Type	Signal Name	Function	Value	J1 Package Pins	G0 Package Pins
Power	V_{CC}	Positive Supply Voltage	5.0V	13, 14, 19, 20, 40, 58	K4, K5, L7, K8, C11, B1
	V_{EE}	Negative Supply Voltage	−5.2V	12, 15, 16, 17, 18, 21	L3, L5, K6, L6, K7, L8
	D_{GND}	Digital Ground	0.0V	10, 11, 22, 23	L2, K3, L10, K10
	A_{GND}	Analog Ground	0.0V	43, 55	A10, A3
Reference	R_T	Reference Resistor, Top	2.0V	59	C2
	R_{OFS}	Overflow Sense	2.0V	57	B2
	R_{TS}	Reference Resistor, Top Sense	2.0V	60	C1
	R_{M1}	Reference Resistor, 1/8 Tap	1.5V [1]	54	B3
	R_{M2}	Reference Resistor, 2/8 Tap	1.0V [1]	53	A4
	R_{M3}	Reference Resistor, 3/8 Tap	0.5V [1]	51	A5
	R_{M4}	Reference Resistor, 4/8 Tap	0.0V [1]	49	B6
	R_{M5}	Reference Resistor, 5/8 Tap	−0.5V [1]	47	A8
	R_{M6}	Reference Resistor, 6/8 Tap	−1.0V [1]	45	A9
	R_{M7}	Reference Resistor, 7/8 Tap	−1.5V [1]	44	B9
	R_B	Reference Resistor, Bottom	−2.0V	39	C10
	R_{BS}	Reference Resistor, Bottom Sense	−2.0V	41	B11
Format Control	NMINV	Not MSB Invert	TTL	63	E2
	NLINV	Not LSB Invert	TTL	28	J11
Convert	CONV	Convert	TTL	36	D11
Analog Input	V_{IN}	Analog Signal Input	+2 to −2V	46, 48, 50, 52	B8, B7, B5, B4
Outputs	OVF	Overflow	TTL	1	E1
	$\overline{OVF}$	Overflow Complement	TTL	2	F2
	D_1 MSB	Most Significant Bit	TTL	3	F1
	D_2		TTL	4	G2
	D_3		TTL	5	G1
	D_4		TTL	29	H10
	D_5		TTL	30	H11
	D_6		TTL	31	G11

Note: 1. Measured values.

TDC1020 Package Interconnections (cont.)

Signal Type	Signal Name	Function	Value	J1 Package Pins	G0 Package Pins
Outputs	D_7		TTL	32	F10
	D_8		TTL	33	F11
	D_9		TTL	34	E11
	D_{10} LSB	Least Significant Bit	TTL	35	D10
No Connects	NC	No Connection	Open	6, 7, 8, 9, 24, 25, 26, 27, 37, 38, 42, 56, 61, 62, 64	H2, H1, J2, J1, K1, K2, L4, K9, L9, K11, J10, G10, E10, B10, A7, A6, A2, D2, D1

Output Coding Table

	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
Input	NMINV=1 NLINV=1	NMINV=0 NLINV=0	NMINV=0 NLINV=1	NMINV=1 NLINV=0
	MSB–LSB (OVF)			
>2.000V	0000000000(1)	1111111111(1)	1000000000(1)	0111111111(1)
2.000V	0000000000(0)	1111111111(0)	1000000000(0)	0111111111(0)
1.996V	0000000001(0)	1111111110(0)	1000000001(0)	0111111110(0)
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
0.004V	0111111111(0)	1000000000(0)	1111111111(0)	0000000000(0)
0.000V	1000000000(0)	0111111111(0)	0000000000(0)	1111111111(0)
–0.004V	1000000001(0)	0111111110(0)	0000000001(0)	1111111110(0)
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
–1.996V	1111111110(0)	0000000001(0)	0111111110(0)	1000000001(0)
–2.000V	1111111111(0)	0000000000(0)	0111111111(0)	1000000000(0)

Note: Input voltages are at code centers.

Figure 1. Timing Diagram

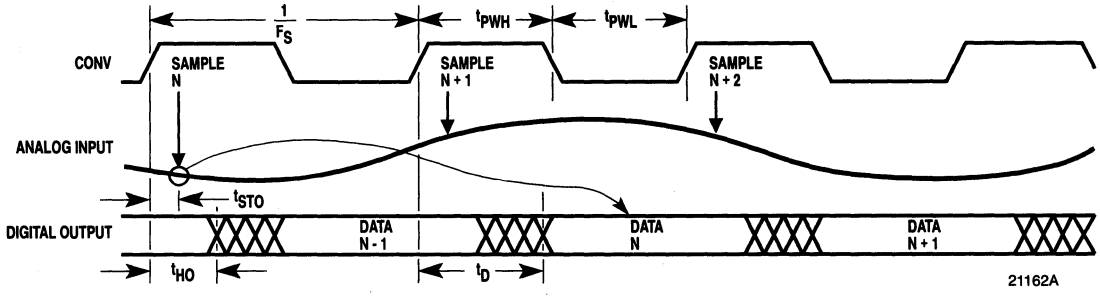
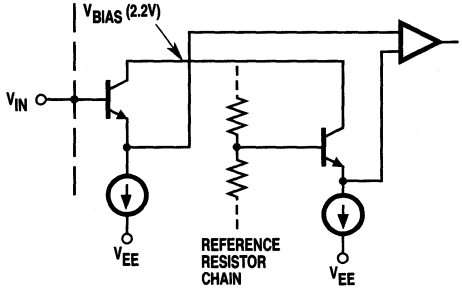
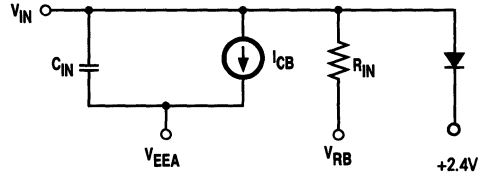


Figure 2. Simplified Analog Input Equivalent Circuits





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

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Figure 3. Equivalent Input Circuits Convert, NMINV, and NLINV

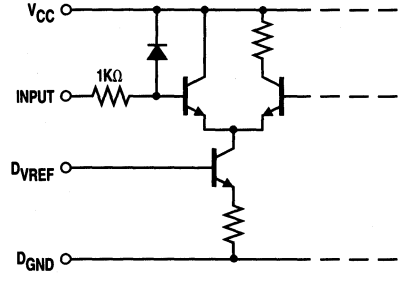

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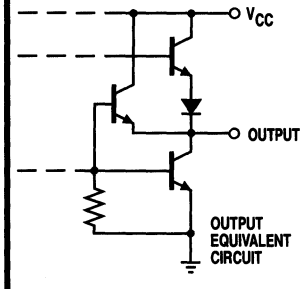
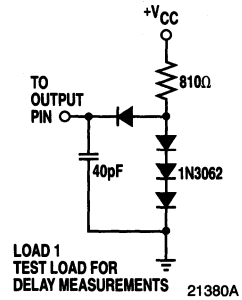
Figure 4. Output Circuits





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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +6.0V
V_{EE} (measured to A_{GND}) ..... +5.0 to −6.0V
A_{GND} (measured to D_{GND}) ..... −1.0 to +1.0V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN} (measured to A_{GND}) ..... V_{CC} to V_{EE}V
Any reference (measured to A_{GND}) ..... V_{CC} to V_{EE}V
V_{RT} (measured to V_{RB}) ..... −1.0 to +4.4V

Output

Applied voltage measured to D_{GND} [2] ..... −0.5 to +5.5V
Applied current, externally forced [3,4] ..... −1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground) ..... 1 Second
Sense lead current ..... −1.0 to 1.0mA

Temperature

Operating, ambient ..... −55 to +90°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Commercial			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{EE}	Negative Power Supply Voltage	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	22			22			ns
t_{PWH}	CONV Pulse Width, HIGH	18			20			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RM2}	Reference Tap, 1/4-Scale	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{RM4}	Reference Tap, 1/2-Scale	−0.2	0.0	0.2	−0.2	0.0	0.2	V
V_{RM6}	Reference Tap, 3/4-Scale	−0.8	−1.0	−1.2	−0.8	−1.0	−1.2	V
V_{RT}	Most Positive Reference Voltage	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{RB}	Most Negative Reference Voltage	−1.8	−2.0	−2.2	−1.8	−2.0	−2.2	V
$V_{RT}-V_{RB}$	Reference Voltage Differential	3.6	4.0	4.4	3.6	4.0	4.4	V

Operating conditions (cont.)

Parameter		Temperature Range						Units
		Commercial			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{IN}	Input Voltage Range	V_{RB}	±2.0	V_{RT}	V_{RB}	±2.0	V_{RT}	V
T_A	Ambient Temperature, C-Grade	0		70				°C
T_C	Case Temperature, V-Grade				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Commercial		Extended		
			Min	Max	Min	Max	
I_{CC}	Total Positive Supply Current	$V_{CC}=V_{EE}=$ Max		850		850	mA
I_{EE}	Total Negative Supply Current	$V_{EE}=$ Max		−500		−500	mA
I_{REF}	Reference Current	V_{RT}, $V_{RB}=$ Nom		50		50	mA
R_{REF}	Reference Chain Resistance	V_{RT}, $V_{RB}=$ Nom	80		80		Ohms
R_{IN}	Analog Input Resistance	V_{RT}, $V_{RB}=$ Nom, $V_{IN}=V_{RB}$	3000		2000		Ohms
C_{IN}	Analog Input Capacitance	V_{RT}, $V_{RB}=$ Nom, $V_{IN}=V_{RB}$		300		300	pF
I_{CB}	Input Constant Bias	$V_{EE}=$ Max		2		3	mA
I_{IL}	Input Current, Logic LOW	$V_{CC}=$ Max, $V_I=0.5V$		50		50	μA
I_{IH}	Input Current, Logic HIGH	$V_{CC}=$ Max, $V_I=2.4V$		100		100	μA
I_I	Input Current, Maximum	$V_{CC}=$ Max, $V_I=5.25V$		100		100	μA
V_{OL}	Output Voltage, Logic LOW	$V_{CC}=$ Min, $I_{OL}=$ Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	$V_{CC}=$ Min, $I_{OL}=$ Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	$V_{CC}=$ Max, output HIGH, one pin to ground, one second duration max.		−35		−35	mA
C_I	Digital Input Capacitance	$T_A=25°C$, f=1MHz		15		15	pF

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Commercial		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	$V_{EE}=$ Min, $V_{CC}=$ Min	20		20		Msps
t_{STO}	Sampling Time Offset	$V_{EE}=$ Max, $V_{CC}=$ Max	3	17	3	17	ns
t_D	Output Delay	$V_{EE}=$ Max, $V_{CC}=$ Max		37		43	ns
t_{HO}	Output Hold Time	$V_{EE}=$ Max, $V_{CC}=$ Max	5		5		ns

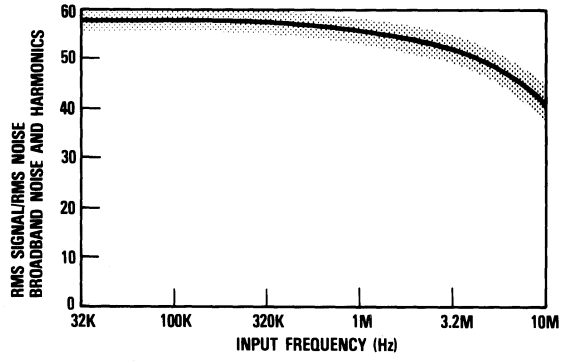
System performance characteristics within specified operating conditions

Parameter		Test Conditions	Typ	Temperature Range				Units
				Commercial		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity Error, Integral	Reference Taps Open	±0.1		±0.2		±0.2	%
E_{LI}	Linearity Error, Integral	Reference Taps Adjusted	±0.05		±0.1		±0.1	%
E_{LD}	Linearity Error, Differential	Reference Taps Open	±0.05		±0.1		±0.1	%
CS	Code Size			5	225	5	225	% Nominal
E_{OT}	Offset Error, Top				25		30	mV
E_{OB}	Offset Error, Bottom				−30		−35	mV
T_{CO}	Offset Error Tempco				±10		±20	μA/°C
t_{TR}	Transient Response	Full-Scale Input Step, Settling to ±32 LSBs	20		30		30	ns
BW	Full-Power Bandwidth	Full-Scale Input	10	5				MHz
SNR	Signal-to-Noise Ratio	Note 1						
		F_{IN}=1.0MHz	60	58		58		dB
		F_{IN}=2.0MHz	59	56		56		dB
		F_{IN}=5.0MHz	56	52		52		dB
		F_{IN}=8.0MHz	54	47				dB
		F_{IN}=10.0MHz	52	43				dB
SINAD	Signal-to-Noise And Distortion	Note 1						
		F_{IN}=1.0MHz	59	55		52		dB
		F_{IN}=2.0MHz	58	52		52		dB
		F_{IN}=5.0MHz	54	48		45		dB
		F_{IN}=8.0MHz	48	41				dB
		F_{IN}=10.0MHz	43	39				dB
THD	Total Harmonic Distortion	Note 1						
		F_{IN}=1.0MHz	−66	−58		−53		dBc
		F_{IN}=2.0MHz	−64	−56		−53		dBc
		F_{IN}=5.0MHz	−58	−52		−46		dBc
		F_{IN}=8.0MHz	−50	−43				dBc
		F_{IN}=10.0MHz	−44	−41				dBc
SFDR	Spurious-Free Dynamic Range	Note 1						
		F_{IN}=1.0MHz	70	53		53		dB
		F_{IN}=2.0MHz	68	54		54		dB
		F_{IN}=5.0MHz	63	48		48		dB
		F_{IN}=8.0MHz	55	40				dB
		F_{IN}=10.0MHz	48	35				dB
E_{AP}	Aperture Error				50		50	ps
DP	Differential Phase	F_S=4 x NTSC Subcarrier, Reference Taps Adjusted	0.3		0.5			Degree
DG	Differential Gain	F_S=4 x NTSC Subcarrier, Reference Taps Adjusted	0.8		1.0			%

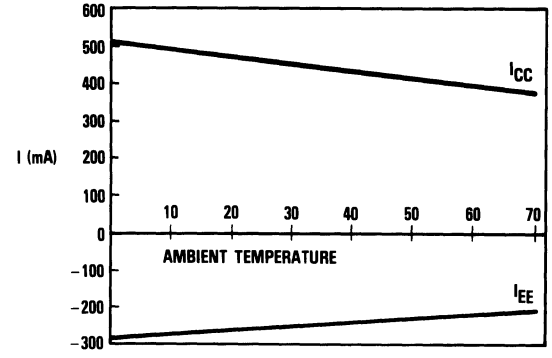
Note: 1. F_S=20Msps, Reference Taps Adjusted, V_{CC}=V_{EE}=Nom, T_A=25°C.

Typical Performance Curves

A. Typical SNR vs. Input Frequency



B. Typical Supply Current vs. Temperature



Calibration

Calibration of the TDC1020 consists of adjusting the reference taps so that the converters integral linearity, gain and offset errors are minimized. To minimize the offset errors the sense leads must be used properly. The sense leads are not designed to carry very much current (<1mA) and should therefore be used in a feedback loop to a high-impedance input such as that shown in the ***Typical Interface Circuit***. When a circuit similar to that in the ***Typical Interface Circuit*** is used for generating the reference voltages, calibration can be achieved with the following procedure:

1. Apply an input to the input amplifier which is 1/2 LSB less than full-scale (A/D input=1.998V) and adjust the gain so that the output of the A/D is toggling between full-scale and one LSB below full-scale (1111111111 and 1111111110 for binary conversions).
2. Apply an input to the input amplifier which is 1/2 LSB greater than zero-scale (A/D input= −1.998V) and adjust V_{RB} via the V_{RB} pot so that the output of the A/D is toggling between 0 and 1 (0000000000 and 0000000001 for binary conversions).

The A/D converter will now be calibrated to provide accurate conversions throughout its input range. To optimize the integral linearity of the device set up the "Subtractive Ramp Test" described on ***page 6*** of the ***TRW Applications Note TP-30, "Understanding Flash A/D Converter Terminology,"*** then adjust the mid-point taps to minimize the bow in the error curve.

Typical Interface

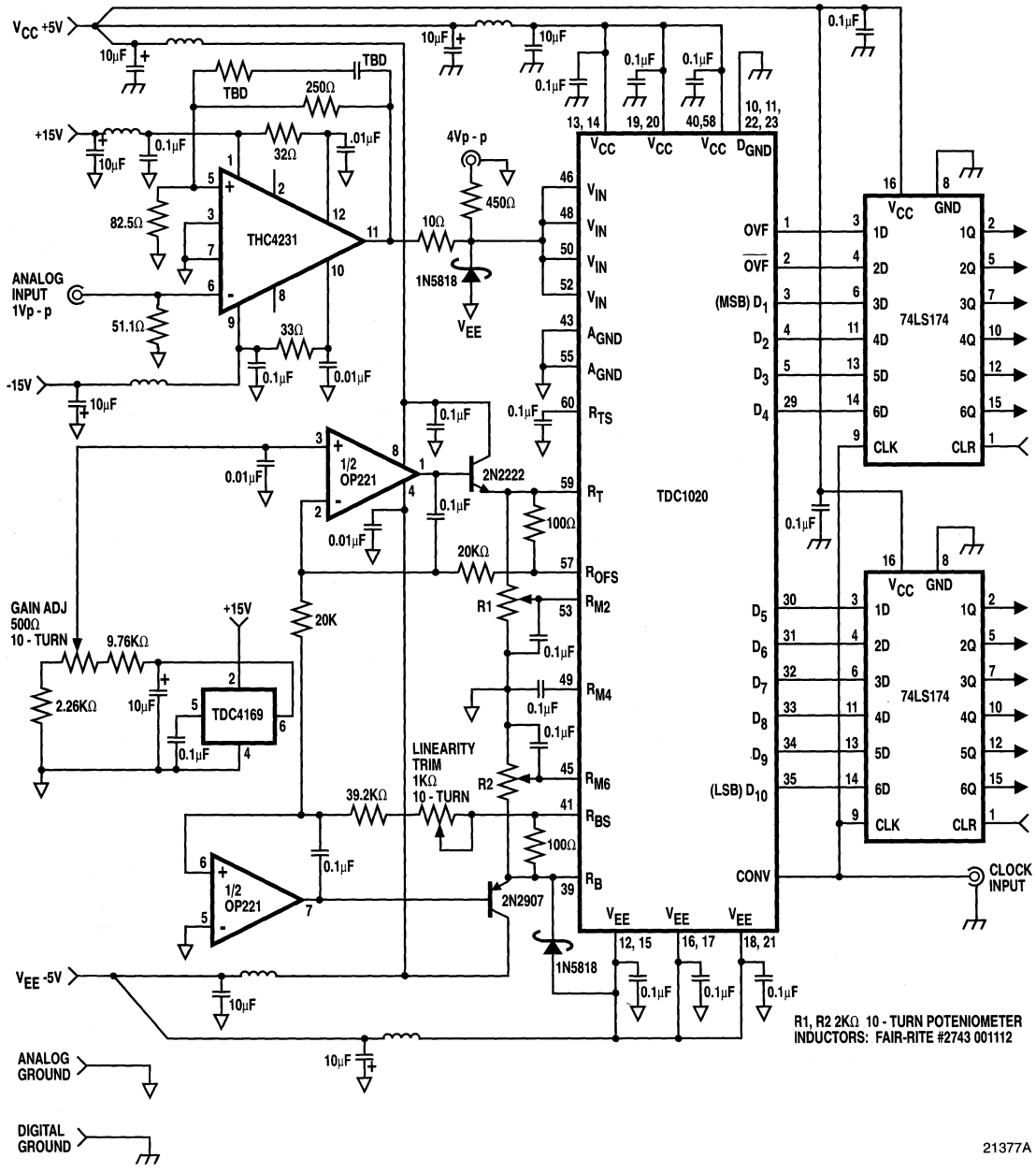
A Typical Interface Circuit is shown of the TDC1020. The analog input amplifier, a THC4231, is used to directly drive the A/D converter. This amplifier is set up to have a gain of four and will provide the recommended +2 to −2V input signal to the TDC1020 when it has a 1Vp-p input signal. All four analog input pins are connected in parallel to decrease the parasitic inductance. An LM313 is used to provide a stable reference voltage which is buffered by a dual op-amp, generating V_{RT} and V_{RB}. Both op-amps have their outputs buffered by an emitter follower to decrease the output impedance seen by the reference resistor chain. To minimize noise coupling into the reference resistor chain, bypass capacitors have been added, bypassing the reference taps to ground.

Since capacitive coupling from the digital signals to the analog input will adversely affect the converter performance, careful attention to board layout is recommended.

As is true with most bipolar integrated circuits, the substrate of the TDC1020 (V_{EE}) must be the most negative potential applied. This rule applies for all conditions of temperature, signal level and power supply sequencing. In many systems, the voltage reference generators and input driving amplifier are powered from voltages greater than the +5 and −5.2V of the TDC1020. Whenever this situation occurs, it is always possible for the V_{EE} inputs of the TDC1020 to be positive with respect to the V_{IN} or V_{RB} inputs when power supplies are cycled ON and OFF.

To protect the TDC1020 from latch-up due to substrate bias, TRW recommends the use of a 1N5818 Schottky diode connected between V_{EE} and V_{IN} and another between V_{EE} and V_{RB} with the anode of each diode connected to V_{EE}. The diodes prevent V_{IN} and V_{RT} from going more than 0.4V more negative than V_{EE}. This protection circuit is shown in ***Figure 5***.

Figure 5. Typical Interface Circuit



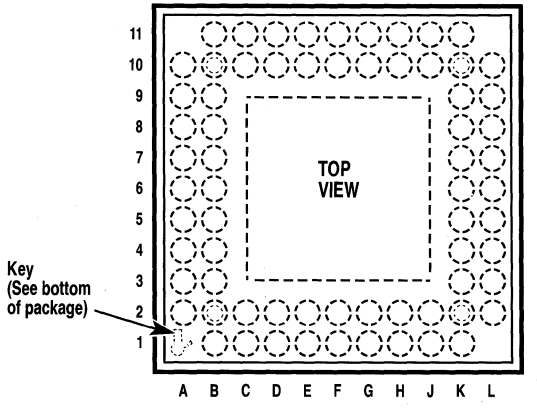
Ordering Information

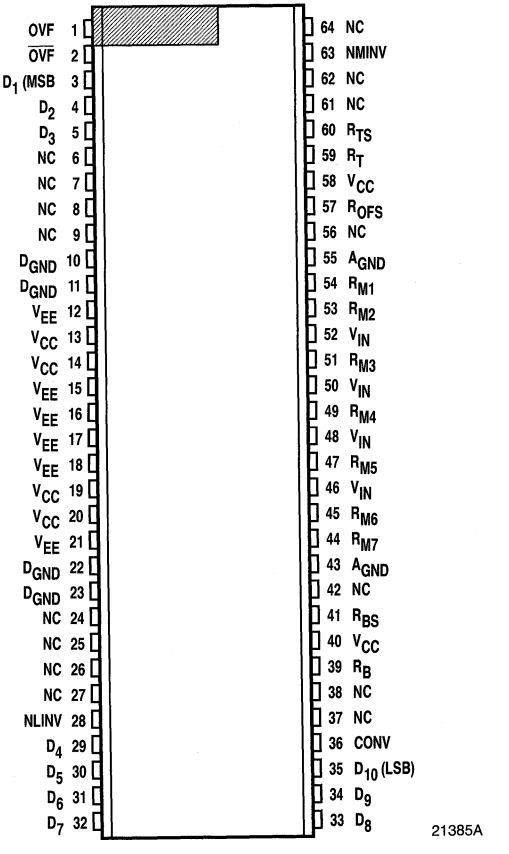
Product Number	Temperature Range	Screening	Package	Package Marking
TDC1020J1C	STD–T_A=0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	1020J1C
TDC1020J1V	EXT–T_C=–55°C to 125°C	Military	64 Pin Hermetic Ceramic DIP	1020J1V
TDC1020G0C	STD–T_A=0°C to 70°C	Commercial	68 Pin PGA	1020G0C
TDC1020G0V	EXT–T_C=–55°C to 125°C	Military	68 Pin PGA	1020G0V

Pin Assignments

68 Pin Grid Array – G0 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	R_{M7}	F10	D_7	K4	V_{CC}
A3	A_{GND}	B10	NC	F11	D_8	K5	V_{CC}
A4	R_{M2}	B11	R_{BS}	G1	D_3	K6	V_{EE}
A5	R_{M3}	C1	R_{TS}	G2	D_2	K7	V_{EE}
A6	NC	C2	R_T	G10	NC	K8	V_{CC}
A7	NC	C10	R_B	G11	D_6	K9	NC
A8	R_{M5}	C11	V_{CC}	H1	NC	K10	D_{GND}
A9	R_{M6}	D1	NC	H2	NC	K11	NC
A10	A_{GND}	D2	NC	H10	D_4	L2	D_{GND}
B1	V_{CC}	D10	D_{10} LSB	H11	D_5	L3	V_{EE}
B2	R_{OFS}	D11	CONV	J1	NC	L4	NC
B3	R_{M1}	E1	OVF	J2	NC	L5	V_{EE}
B4	V_{IN}	E2	NMINV	J10	NC	L6	V_{EE}
B5	V_{IN}	E10	NC	J11	NLINV	L7	V_{CC}
B6	R_{M4}	E11	D_9	K1	NC	L8	V_{EE}
B7	V_{IN}	F1	D_1 MSB	K2	NC	L9	NC
B8	V_{IN}	F2	$\overline{OVF}$	K3	D_{GND}	L10	D_{GND}





64 Pin Hermetic Ceramic DIP – J1 Package

40G05371 Rev D 8/93

TDC1035
Monolithic Peak Digitizer
8-Bit, 30 ns Full Response Peak Width

Description

The TDC1035 is a unique variant of the full-parallel ("flash") analog-to-digital converter, capable of capturing the maximum peak amplitude of one or more pulses applied to its input between asynchronous reset pulses. Multiple "peak read" operations can be performed between resets. Peaks are detected digitally, so operation is stable and predictable. Packaged in a 24-pin CERDIP, the TDC1035 features lower power consumption and smaller size than an analog peak detector/ADC combination. All digital inputs and outputs are TTL compatible, and all outputs are registered and three-state.

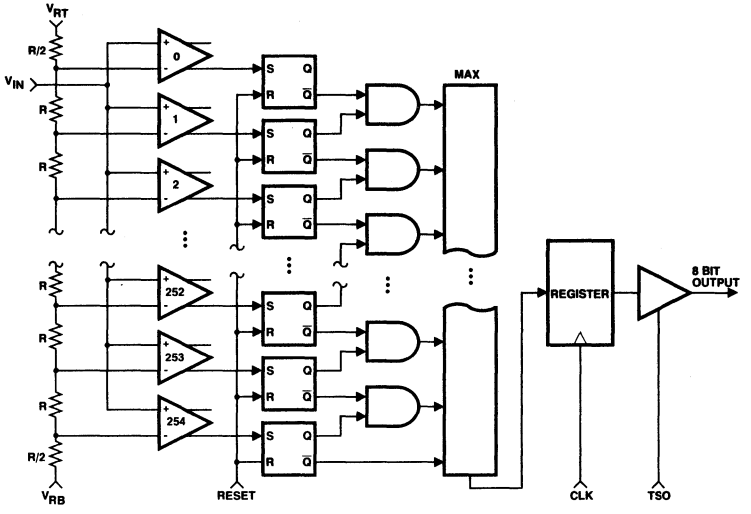
Features

- 8-bit resolution
- Full DC linearity for pulses — 30 ns wide
- Does not require analog peak-hold circuit
- Continuous peak capture between resets
- Multiple read operations between resets
- 1/2 LSB linearity
- Narrow ambiguity region around reset
- Detects pulses as small as 12 ns wide
- Guaranteed monotonic
- Selectable data format
- Available in 24-pin CERDIP and 28-lead PLCC packages
- 1.0W power consumption
- Three-state registered outputs

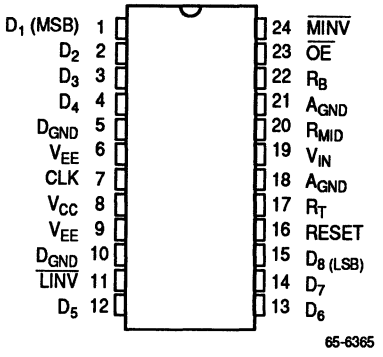
Applications

- Radar pulse classification
- Electronic countermeasures
- Radiation measurement
- Instrumentation

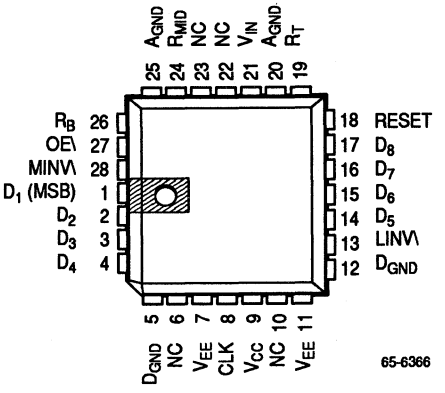
Functional Block Diagram



Pin Assignments



24 Pin CERDIP — B7 Package



28 Lead PLCC — R3 Package

Functional Description

General Information

The TDC1035 peak detector operates on ground-referenced negative-going signals. Within t_{RP} nanoseconds after the rising edge of the clock signal CLK, it outputs the most negative value reached since the previous RESET pulse. The active-HIGH RESET control is independent of CLK, but may be connected to CLK to provide a single-control peak detector. Multiple output cycles are permitted between reset operations.

The TDC1035 contains parallel array of comparators, an array of latches, and an encoder which outputs the location of the highest-valued latch which is set. The TDC1035's response characteristics are determined by its comparator array. A comparator's response time is determined by the degree of overdrive, since the output changes only when the area above threshold reaches a characteristic value. Therefore, the digitization accuracy of a pulse's peak value depends on the shape of the pulse.

To permit accurate, repeatable characterization, the TDC1035 is tested with a slew-rate limited "square" pulse. It will digitize (to its DC accuracy) the peak value of a square pulse having a minimum duration of 30ns. The accuracy degrades gracefully as the duration decreases from 30 down to 12ns, where it understates the applied amplitude by 15% (***Figure 7***). Production characterization of the TDC1035 uses "square" pulses with controlled rise and fall times of 8ns.

Performance of the TDC1035 with other pulse shapes (such as Gaussian or bandwidth-limited square pulse) can be estimated by applying an energy above threshold model, with area of 120 picoVolt-seconds.

The operation of all asynchronous sequential logic circuits involves some temporal ambiguity. The most common form of this ambiguity, metastability, occurs in data synchronizers. In a peak digitizer such as the TDC1035, this ambiguity comes in the form of periods during which the accuracy of the measurement of a pulse may be affected, or the pulse may not even be detected. There is a 10ns (t_{RP}) ambiguity period after the falling edge of the RESET signal, during which detection or accuracy of detection of any pulse is not guaranteed. There is also a region of 40ns (t_{PC}) before the rising edge of the (output) clock (CLK) where a pulse may be missed or detected inaccurately. These regions are shown in the timing diagrams, ***Figures 1 and 2***. During the latter period, if the input signal increases to a new peak larger than the previously-latched value, the value loaded into the output register may be incorrect (and will most likely be zero); nonetheless, the peak detection latches will hold the (correct) new peak value.

As shown in ***Figure 3***, the TDC1035's comparator inputs have emitter-follower buffers, which limit the permissible input signal slew rate to 250V/μs. This corresponds to a full-scale transition time of 8ns.

Power

The TDC1035 operates from two supply voltages: +5.0V and −5.2V. The current return for the positive supply is D_{GND}, and the return for the negative (analog) supply is A_{GND}. All power and ground pins MUST be connected.

Reference

The reference for the TDC1035 is a negative voltage applied across a chain of 255 resistors. The top of this chain is connected to the RT pin, and the voltage applied to the R_T pin (V_{RT}) should be within 0.1V of the analog ground. Note that the difference between the voltage applied to the pin and the voltage at the reference chain is the offset specification (E_{OT} and E_{OB}). The bottom of the reference resistor chain is connected to the RB pin, and the voltage applied to the R_B pin (V_{RB}) should be between 1.8 and 2.2V negative with respect to the R_T pin for full-specification operation. Reduced reference voltage operation is possible at reduced accuracy (for example, for generating a non-linear transfer function). The $R_T - R_B$ reference source should be able to deliver at least 45mA.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be connected to circuit nodes with a low impedance to ground. For circuits in which the reference is not varied at a high rate, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (e.g., for AGC or nonlinear operation), a low-impedance reference source is required. The reference voltages may be varied dynamically; contact the factory for information on limitations when the device is used in this mode. The performance of the TDC1035 is specified with DC references of $V_{RT} = 0.0V$ and $V_{RB} = -2.0V$.

Control

Two function control pins, $\overline{\text{MINV}}$ and $\overline{\text{LINV}}$, are provided. These names stand for active-LOW Most significant bit INVert and active-LOW Least significant bits INVert, respectively. These controls are for DC (i.e., steady-state), not dynamic, use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. A single output state control pin, $\overline{\text{OE}}$, is provided. The three-state outputs may be placed in a high-impedance state by applying a logic HIGH to the $\overline{\text{OE}}$ control pin, and enabled by driving $\overline{\text{OE}}$ LOW.

The function control pins may be tied to V_{CC} for a logic HIGH, and D_{GND} for a logic LOW; however, a 2.2 kOhm pull-up resistor is preferred over direct connection to V_{CC}. If a pull-up resistor is not used, the absolute maximum voltage rating for the part becomes that of the TTL input, 5.5V, rather than the higher value for the V_{CC} terminal.

Command

Two pins, RESET and CLK, control the TDC1035. When brought HIGH, the level-sensitive RESET control resets the peak-storing latches. The edge-sensitive CLK control causes the peak value to be loaded into the output register when a rising-edge (LOW-to-HIGH) signal is applied. As noted above, there is a data ambiguity period associated with the operation of each of these inputs.

Analog Input

Although the TDC1035's 255 comparators have emitter-follower isolated inputs, the input impedance can vary up to 25 percent with the signal level, as comparator input transistors switch on or off. As a result, for optimal performance, the source impedance of the driving device must be less than 25 Ohms. The input signal will not damage the TDC1035 if it remains in the range $V_{EE} - 0.5V$ to $V_{AGND} + 0.5V$. If the input signal stays between the V_{RT} and V_{RB} reference voltages, the 8-bit digital equivalent of the most negative voltage reached will be latched into the array of latches, subject to the dynamic effects mentioned above. A transient more negative than V_{RB} will cause a full-scale output t_{DO} after the CLK line rises.

Outputs

The outputs of the TDC1035 are TTL compatible, capable of driving four low-power Schottky TTL (54LS/74LS) unit loads or the equivalent. The outputs hold the previous data a minimum time t_{HO} after the rising edge of the CLK input, and are guaranteed to have the new output value after a maximum time t_{DO}. Under light DC load conditions (such as driving CMOS loads or base-input low-power Schottky such as the 74L5374) 2.2k pull-up resistors to +5.0V are recommended.

Package Interconnections

Name	Function	Value	B7 Package Pins	R3 Package Pins
V_{CC}	Positive Supply Voltage	+5.0V	8	9
V_{EE}	Negative Supply Voltage	-5.2V	6, 9	7, 11
D_{GND}	Digital Ground	0.0V	5, 10	5, 12
A_{GND}	Analog Ground	0.0V	18, 21	20, 25
R_T	Reference Resistor, Top	0.0V	17	19
R_{MD}	Reference Resistor, Middle	-1.0V	20	24
R_B	Reference Resistor, Bottom	-2.0V	22	26
MINV	MSB Invert	TTL (Active LOW)	24	28
LINV	LSB Invert	TTL (Active LOW)	11	13
OE	Output Enable	TTL (Active LOW)	23	27
RESET	Resets Peak Value to Zero	TTL (Active HIGH)	16	18
CLK	Loads Output Register	TTL (Rising Edge)	7	8
V_{IN}	Analog Input Signal	0.0V to -2.0V	19	21
D_1	MSB Output	TTL	1	1
D_2		TTL	2	2
D_3		TTL	3	3
D_4		TTL	4	4
D_5		TTL	12	14
D_6		TTL	13	15
D_7		TTL	14	16
D_8	LSB Output	TTL	15	17

Figure 1. Timing with Separate RESET and CLK

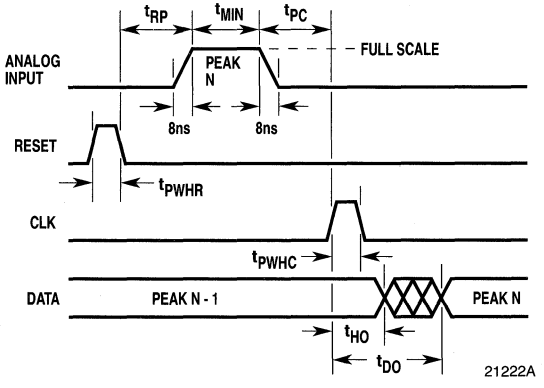


Figure 2. Timing with Common RESET and CLK

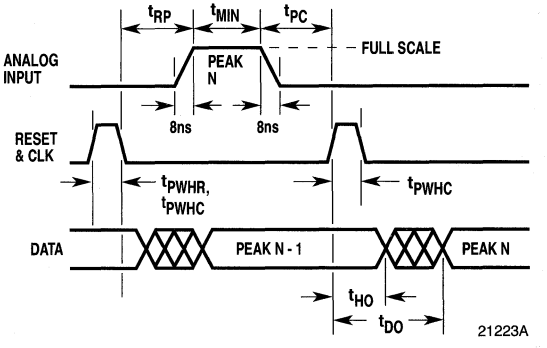
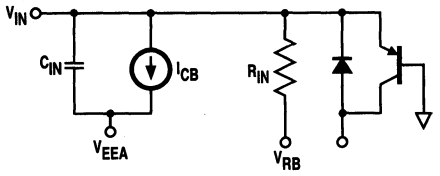


Figure 3. Simplified Analog Input Equivalent Circuits



C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

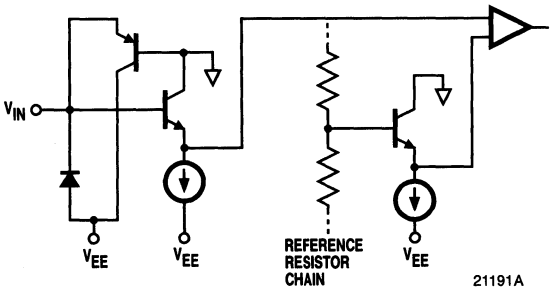


Figure 4. Digital Input Equivalent Circuit

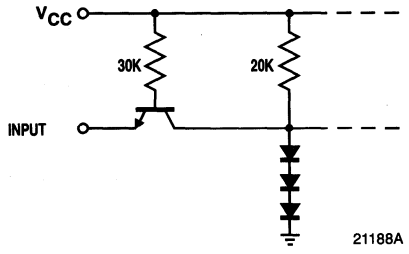


Figure 5. Output Circuits

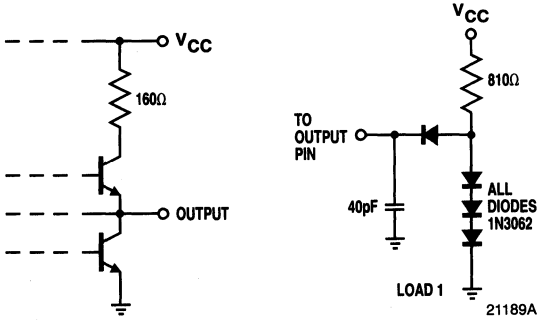


Figure 6. Recommended Input Circuit

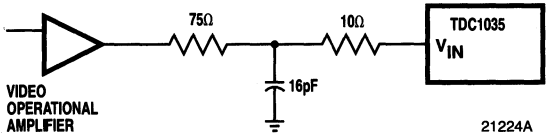
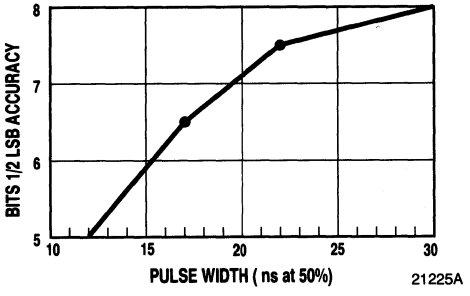


Figure 7. Variation of Accuracy as a Function of Width, "Square" Input Pulse



Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2.0000V FS	−2.0480V FS	$\overline{MINV}$ = 1	0	0	1
	7.8431mV Step	8.000mV Step	$\overline{LINV}$ = 1	0	1	0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	−0.0078V	−0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9922V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0000V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0078V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9844V	−2.0240V	11111110	00000001	01111110	10000001
255	−1.9922V	−2.0320V	11111111	00000000	01111111	10000000

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to D_{GND})	−7.0 to +0.5V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

RESET, CLK, $\overline{OE}$, $\overline{MINV}$, $\overline{LINV}$ (measured to A_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	(V_{EE} − 0.5) to +0.5V
V_{RT} (measured to V_{RB})	−2.2 to +2.2V

Outputs

Applied voltage (measured to D_{GND})	−0.5 to +0.5V [2]
Applied current (externally forced)	−1.0 to 6.0mA [3,4]
Short-circuit duration (single output HIGH to shorted to ground)	1 Second

Temperature

Operating, ambient	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance is guaranteed only if specified operating conditions are met.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.5	V
V_{EE}	Negative Supply Voltage	−4.90	−5.2	−5.5	−4.90	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWHR}	Reset Minimum Pulse Width, HIGH	20			20			ns
t_{PWLC}	CLK Minimum Pulse Width, LOW	20			20			ns
t_{PWHC}	CLK Minimum Pulse Width, HIGH	20			20			ns
S_R	Input Signal Slew Rate			250			250	V/μS
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Reference Voltage, Top	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Reference Voltage, Bottom	−1.8	−2.0	−2.2	−1.8	−2.0	−2.2	V
$V_{RT}-V_{RB}$	Reference Voltage Span	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage Range	V_{RT}		V_{RB}	V_{RT}		V_{RB}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, Static		35		35	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, Static		−160		−160	mA
I_{REF}	Reference Current	$V_{RT}-V_{RB}$ = Nom		35		35	mA
R_{REF}	Reference Resistance	Total, R_T to R_B	57		57		Ohms
R_{IN}	Input Equivalent Resistance (DC)	V_{RT}, V_{RB} = Nom, $V_{IN}=V_{RB}$	50		50		kOhms
C_{IN}	Input Capacitance, Analog	V_{RT}, V_{RB} = Nom, $V_{IN}=V_{RB}$		50		50	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		250		350	μA
I_{IL}	Input Current Logic LOW	V_{CC} = Max, V_{IL} = 0.4V		−500		−500	μA
I_{IH}	Input Current Logic HIGH	V_{CC} = Max, V_{IH} = 2.4V		50		50	μA
I_{IM}	Input Current, V_{IN} = Max	V_{CC} = Max, V_{IH} = 5.5V		1		1	mA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = Max, V_O = 0V	−30	30	−30	30	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = Max, V_O = 5V	−30	30	−30	30	μA
I_{OS}	Short-Circuit Output [1]	V_{CC} = Max, Output HIGH, one output tied to D_{GND} for 1 second.		−50		−50	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Max, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
C_{IN}	Input Capacitance, Digital			10		10	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{PC}	CLK Setup Time	V_{CC}=Min, V_{EE}=Min, Load 1		30		30	ns
t_{RP}	RESET Delay	V_{CC}=Min, V_{EE}=Min, Load 1		5		5	ns
t_{DO}	Output Delay	V_{CC}=Min, V_{EE}=Min, Load 1		35		35	ns
t_{HO}	Output Hold Time	V_{CC}=Min, V_{EE}=Min, Load 1	5		5		ns
t_{DIS}	Output Disable Time	V_{CC}=Min, V_{EE}=Min, Load 1		20		20	ns
t_{ENA}	Output Enable Time	V_{CC}=Min, V_{EE}=Min, Load 1		70		90	ns

Note: 1. t_{RP} and t_{PC} are the guaranteed maximum lengths of the ambiguity periods.

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error, Integral, Independent	V_{RT}, V_{RB}=Nom		0.2		0.2	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB}=Nom		0.2		0.2	%FS
CS	Code Size	V_{RT}, V_{RB}=Nom	30	170	30	170	% Nominal
t_{MIN}	Analog Input Pulse Width	Square Pulse,					
		15% Accuracy	12		12		ns
		DC Accuracy	30		30		ns
E_{OT}	Offset Error, Top	V_{IN}=V_{RT}		±8		±8	mV
E_{OB}	Offset Error, Bottom	V_{IN}=V_{RB}		±15		±15	mV
T_{CO}	Offset Error, Temperature Coefficent	V_{RT}, V_{RB}, V_{CC}, V_{EE}=Nom		±20		±20	μV/°C

Applications Discussion

Under certain conditions, the real component of the input impedance may go negative at frequencies near 100MHz. To prevent oscillation at the input signal port, TRW recommends connecting the input signal to the TDC1035 via a series-connected resistor of at least 10 Ohms located close to the device. Further, if the signal bandwidth is not already limited so that the input slew rate limit is not exceeded, external circuitry is also recommended. The circuit shown in *Figure 6* accomplishes both goals.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1035B7C	STD - T_A = 0°C to 70°C	Commercial	24-Pin CERDIP	1035B7C
TDC1035B7V	EXT - T_C = -55°C to 125°C	MIL-STD-883	24-Pin CERDIP	1035B7V
TDC1035R3C	T_A = 0°C to 70°C	Commercial	28-Lead PLCC	1035R3C

40G06460 Rev B 8/93

TDC1038
Monolithic Video A/D Converter
8-Bit, 20 Msps, Low Power

Description

The TDC1038 is a flash analog-to-digital converter capable of converting a video-speed signal into a stream of 8-bit digital words at 20 Msps (MegaSamples Per Second). It is pin-for-pin compatible with the industry standard TDC1048 but uses half the power. Since the TDC1038 is a flash converter, a sample-and-hold circuit is not required.

The TDC1038 consists of 255 clocked latching comparators, combining logic, and an output register. A single convert clock controls the conversion operation. The unit can be configured to give either true or inverted outputs, in binary or offset two's complement coding. All digital I/O is TTL compatible.

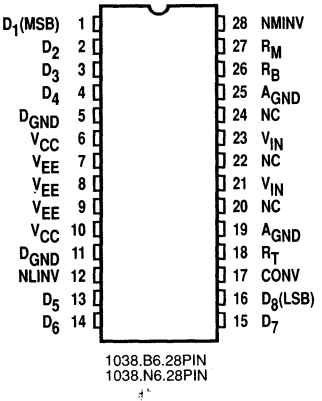
Features

- 8-bit resolution
- DC to 20 Msps conversion rate
- 7 MHz full-power bandwidth
- 30 MHz small signal -3 dB bandwidth
- 1/2 LSB linearity
- 700 mW power dissipation
- +5V, -5V (or -5.2V) supply operation
- Low cost
- Drop-in replacement for TDC1048
- Sample-and-hold circuit not required
- Analog input range 0 to -2V
- Differential phase 0.3°
- Differential gain 0.7%
- Selectable data format
- Available in plastic DIP, CERDIP, and PLCC

Applications

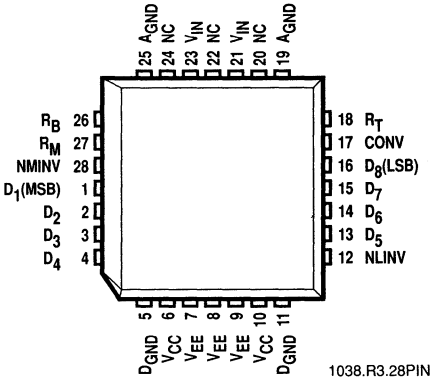
- Digital television
- Electronic warfare
- Low power upgrade for TDC1048
- Video digitizing
- Medical imaging
- High energy physics
- Low cost, low power, high-speed data conversion

Pin Assignments



1038.B6.28PIN
1038.N6.28PIN

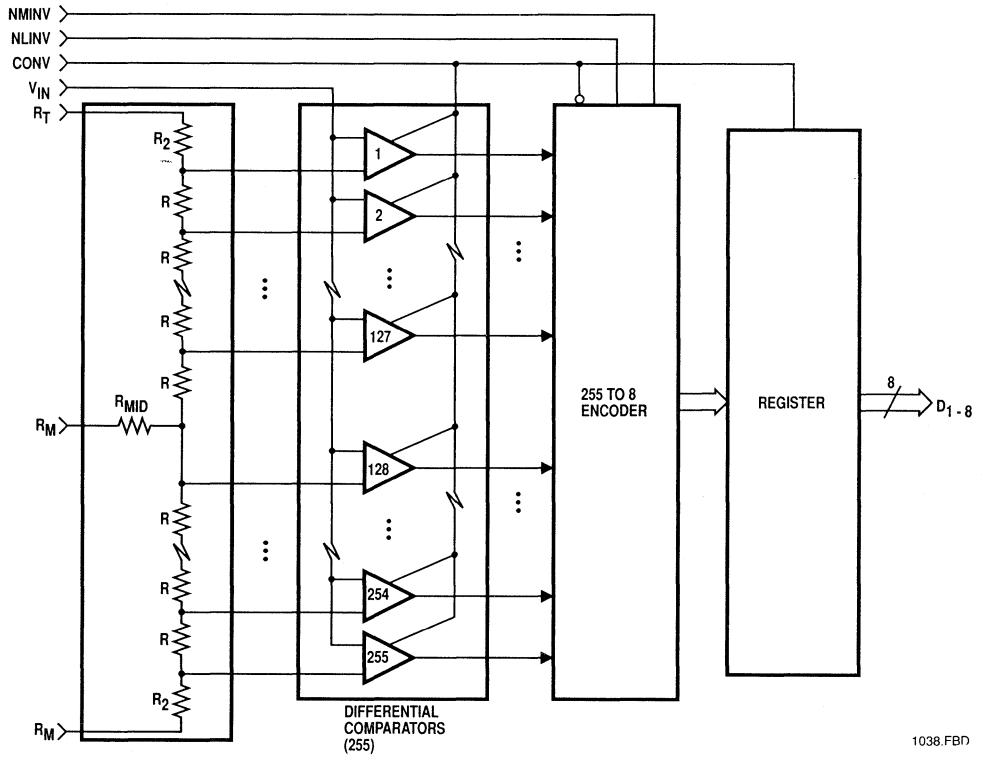
28 Pin CERDIP - B6 Package
28 Pin Plastic DIP - N6 Package



1038.R3.28PIN

28 Lead Plastic J-Leaded Chip Carrier - R3 Package

Functional Block Diagram



Functional Description

General Information

The TDC1038 has three functional sections: a comparator array, encoding logic, and output registers. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (or thermometer code, since all the comparators whose reference is more negative than the input signal will be on, and all those whose reference is more positive will be off). The encoding logic converts the N-of-255 code into the user's choice of coding. The output register holds the output constant between updates.

Power

The TDC1038 operates from two supply voltages: +5.0V and -5.0V. -5.2V may be used with a slight increase in power dissipation. The return path for I_{CC}, the current from the +5.0V supply is D_{GND}. The return for path I_{EE}, the current from the -5.0V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1038 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. The specifications of the TDC1038 are guaranteed with V_{RT}, (the voltage applied to the top of the reference resistor chain) at 0.0±0.1V and V_{RB} (the voltage applied to the bottom of the reference resistor chain) at -2.0±0.1V.

Linearity is guaranteed with no adjustment; however, a midpoint tap, R_M, allows trimming of converter integral linearity as well as the creation of a nonlinear transfer function. This is explained in the Application Note ***TP-19 "Non-Linear A/D Conversion."*** The circuit shown in ***Figure 6*** will provide approximately a 1/2 LSB adjustment of the linearity at midscale. The characteristic impedance seen at this node is approximately 200 ohms and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and any noise introduced at this point will degrade the overall quantization SNR. Due to the slight variation in the reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor (0.0 to 0.1 µF) to ground is recommended. If the reference inputs are exercised dynamically (as in an automatic gain control circuit) a low-impedance reference source is required. The reference voltages may be varied dynamically up to 5 MHz; however, device performance is specified with fixed reference voltages as defined in the ***Operating Conditions Table.***

Analog Input

For precise quantization, the TDC1038 uses latching comparators. For optimum overall system performance the source impedance of the driving circuit must be less than 25 ohms. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number from 0 to 255. When a signal outside the recommended input voltage range (0 to -2V) is applied, the output will remain at either full-scale value. The input signal will not damage the TDC1038 if it remains within the range specified in the ***Absolute Maximum Ratings Table***. Both analog input pins are connected together internally and therefore either one or both may be used.

Convert

The TDC1038 requires external convert (CONV) signal. Because the TDC1038 is a flash converter it does not require a track-and-hold circuit. A sample is taken (the outputs of the comparators are latched) within t_{STO} (Sampling Time Offset) after a rising edge on the CONV pin. The result is encoded and then transferred to the output registers on the next rising edge. The digital output for sample N becomes valid t_D after the rising edge of clock N+1 and remains valid until t_{HO} after the rising edge of clock N+2. (See ***Figure 1, Timing Diagram.***)

Output Format Control

Two output format control pins, NMINV and NLINV, are provided. These controls are for DC (i.e., steady state) uses. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These active LOW pins may be tied to V_{CC} (through a 4.7 kOhm resistor) for a logic 1 or D_{GND} for a logic 0.

Outputs

The outputs of the TDC1038 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) loads or equivalent. The outputs hold the previous data for a minimum of tHO after the rising edge of the CONVert signal.

Not Connected

There are several pins that have no internal connection to the chip. They should be left open.

Package Interconnections

Signal Type	Signal Name	Function	Value	B6, N6, R3 Package Pins
Power	VCC	Digital Supply Voltage	+5.0V	6,10
	VEE	Analog Supply Voltate	-5.0V	7, 8, 9
	AGND	Analog Ground	0.0V	19, 25
	DGND	Digital Ground	0.0V	5, 11
Reference	RT	Reference Resistor (Top)	0.0V	18
	RM	Reference Resistor (Middle)	-1.0V	27
	RB	Reference Resistor (Bottom)	-2.0V	26
Analog Input	VIN	Analog Signal Input	0V to -2V	21, 23
Convert	CONV	Convert	TTL	17
Format Control	NMINV	Not Most Signficant Bit Invert	TTL	28
	NLINV	Not Least Significant Bit Invert	TTL	12
Data Output	D1	Most Significant Bit Output	TTL	1
	D2		TTL	2
	D3		TTL	3
	D4		TTL	4
	D5		TTL	13
	D6		TTL	14
	D7		TTL	15
	D8	Least Significant Bit Output	TTL	16
Not Connected	NC	Not Connected	Open	20, 22, 24

Figure 1. Timing Diagram

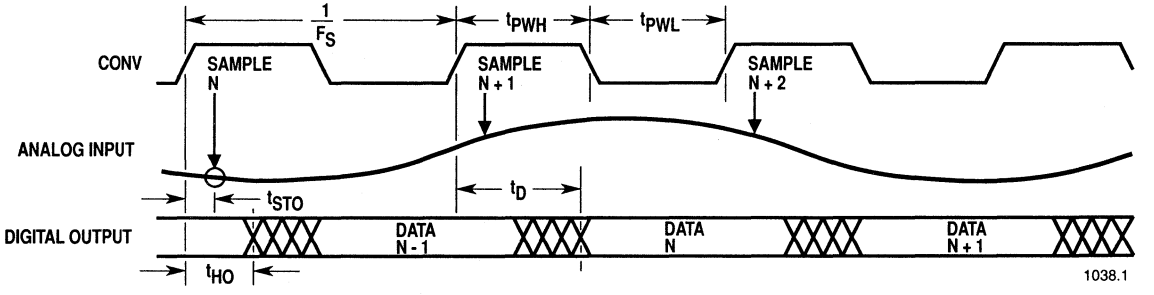
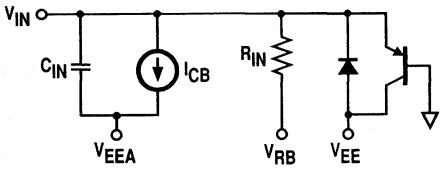
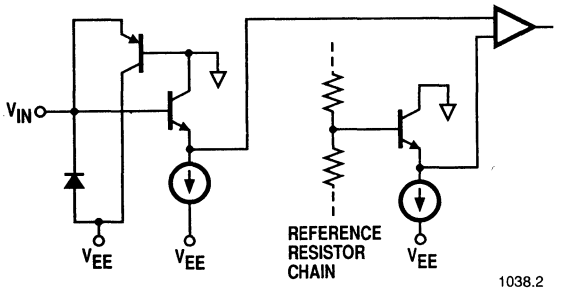


Figure 2. Simplified Input Circuits

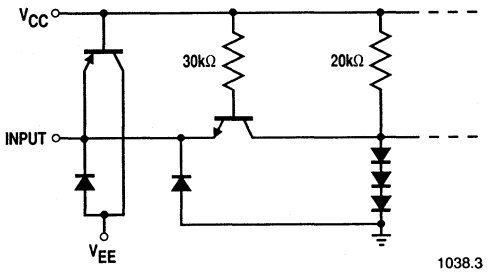


C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B



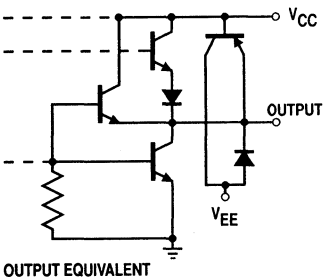
1038.2

Figure 3. Convert Input Equivalent Circuit

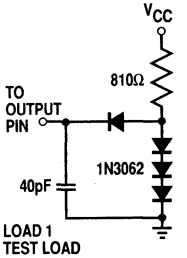


1038.3

Figure 4. Output Circuit



OUTPUT EQUIVALENT CIRCUIT



1038.4

Output Coding Table

	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
Input Voltage	NMINV=HIGH NLINV=HIGH	NMINV=LOW NLINV=LOW	NMINV=LOW NLINV=HIGH	NMINV=HIGH NLINV=LOW
0.0000V	0000 0000	1111 1111	1000 0000	0111 1111
-0.0078V	0000 0001	1111 1110	1000 0001	0111 1110
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
-0.9922V	0111 1111	1000 0000	1111 1111	0000 0000
-1.0000V	1000 0000	0111 1111	0000 0000	1111 1111
-1.0078V	1000 0001	0111 1110	0000 0001	1111 1110
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
-1.9844V	1111 1110	0000 0001	0111 1110	1000 0001
-1.9922V	1111 1111	0000 0000	0111 1111	1000 0000

Notes:
1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V for a logic 1 or tied to ground for a logic 0.
2. Voltages are code midpoints.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	-0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to -7.0V
A_{GND} (measured to D_{GND})	-0.5 to +0.5V

Input Voltages [2]

CONV, NMINV, NLINV	-0.5 to (V_{CC}+0.5V)
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	V_{EE} to +0.5V
V_{RT} (measured to V_{RB})	-2.2 to +2.2V

Input Currents [3]

CONV, NMINV, NLINV	-50 to +50 mA
V_{IN}, V_{RT}, V_{RB}	-100 to +100 mA

Output

Applied voltage (measured to D_{GND})	-0.5 to (V_{CC}+0.5V) [2]
Applied current, externally forced	-20 to +20 mA [3]
Short-circuit duration (single output in HIGH state to ground)	

Temperature

Operating, ambient (all packages except N6 and R3	-55 to +125°C
(N6 and R3 packages only)	-20 to +90°C
junction (all packages)	+175°C
Lead, soldering, all packages (10 seconds)	+300°C
Storage, all packages	-65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. A condition applied individually that exceeds the Operating Conditions specification but is less than the Absolute Maximum Ratings will not cause immediate device failure.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.

Operating Conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Digital Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{EE}	Analog Supply Voltage	-4.9	-5.0	-5.50	-4.9	-5.2	-5.50	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	-0.1	0.0	0.1	-0.1	0.0	0.1	V
t_{PWL}	CONVert Pulse Width, LOW	18			18			ns
t_{PWH}	CONVert Pulse Width, HIGH	22			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-400			-400	µA
V_{RT}	Most Positive Reference Input [1]	-0.1	0.0	0.1	-0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	-1.9	-2.0	-2.1	-1.9	-2.0	-2.1	V
V_{RT}-V_{RB}	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70	-55		125	°C

Note: 1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Thermal characteristics (approximate)

Parameter		Nom	Max	Min
θja	Thermal Resistance, Junction to Ambient	B6	50	°C/W
		N6	45	°C/W
		R3	65	°C/W
θjc	Thermal Resistance, Junction to Case	B6	12	°C/W
		N6	17	°C/W
		R3	14	°C/W

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC}=Max[1]		35		35	mA
I_{EE}	Negative Supply Current	V_{EE}=Max [1]		-170		-170	mA
I_{REF}	Reference Current	V_{RT}, V_{RB}=Nom		30		50	mA
R_{REF}	Total Reference Resistance		67		40		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB}=Nom, V_{IN}=V_{RB}	80		40		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB}=Nom, V_{IN}=V_{RB}		50		50	pF
I_{CB}	Input Constant Bias Current	V_{CCA}=Max		250		500	µA
I_{IL}	Input Current, Logic LOW	V_{CC}=Max, V_I=0.4V		-0.6		-0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC}=Max, V_I=2.4V	-200	50	-400	50	µA
I_I	Input Current, Max Input Voltage	VCC=Min, I_{OL}=Max		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC}=Min, I_{OL}=Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC}=Min, I_{OH}=Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC}=Max, Output HIGH, one pin to ground, one second duration max		-40		-40	mA
C_I	Digital Input Capacitance	T_A=25°C, F=1 MHz		15		15	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate		20		20		Msps
t_{STO}	Sampling Time Offset		-2	10	-2	10	ns
t_D	Output Delay	V_{CC}=Min, Load 1, Figure 4		30		35	ns
t_{HO}	Output Hold Time	V_{CC}=Min, Load 1, Figure 4	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB}=Nom		0.2		0.2	%
E_{LD}	Linearity Error Differential			0.2		0.2	%
C_S	Code Size		25	175	25	175	% Nom
E_{OT}	Offset Error, Top	V_{IN}=V_{RT}		+15		+15	mV
E_{OB}	Offset Error, Bottom	V_{IN}=V_{RB}		-15		-15	mV
T_{CO}	Offset Error, Temperature Coefficient			±20		±20	µV/°C
BW	Bandwidth, Full-Scale Input	No Spurious or Missing Codes	7		7		Mhz
BW_{SS}	-3 dB Bandwidth, Small Signal	-20 dBFS Input	30		30		MHz
t_{TR}	Transient Response, Full Scale		40		40		ns
SNR	Signal-to-Noise Ratio	10 MHz Bandwidth,					
		20 Msps Conversion Rate					
	Peak Signal/RMS Noise	1.248 MHz Input	54		53		dB
		2.438 MHz Input	53		52		dB
	RMS Signal/RMS Noise	1.248 MHz Input	45		44		dB
		2.438 MHz Input	44		43		dB
E_{AP}	Aperture Error			60		60	ps
DP	Differential Phase Error	F_S=4 x NTSC		1.0		1,0	Degree
DG	Differential Gain Error	F_S=4 x NTSC		2.0		2.0	%

Figure 5. Typical Interface Circuit

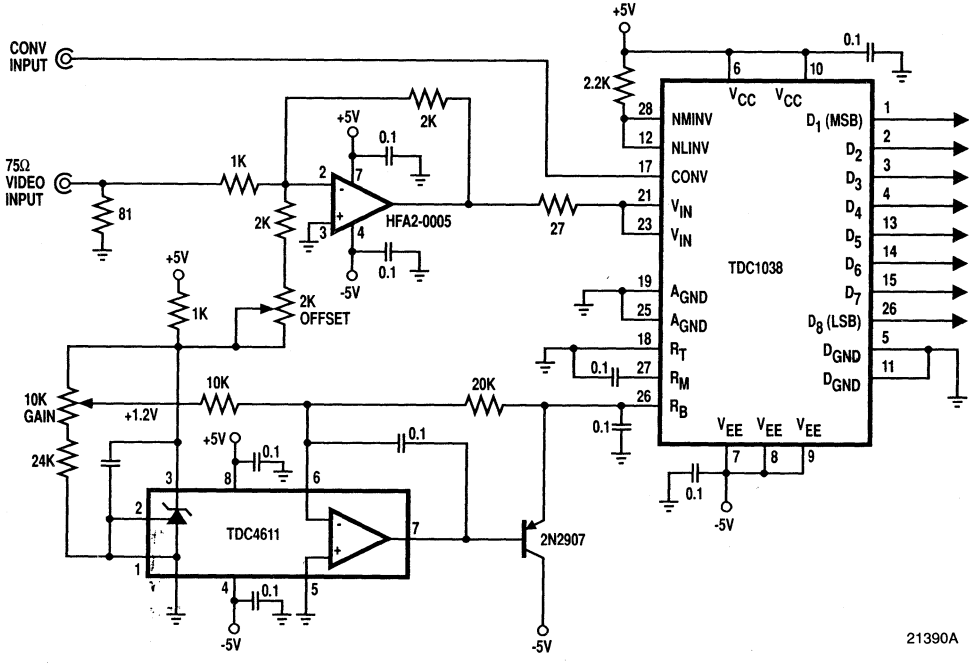


Figure 6. Optional Midscale Linearity Adjust

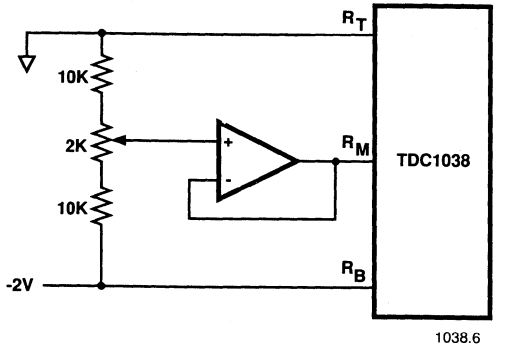
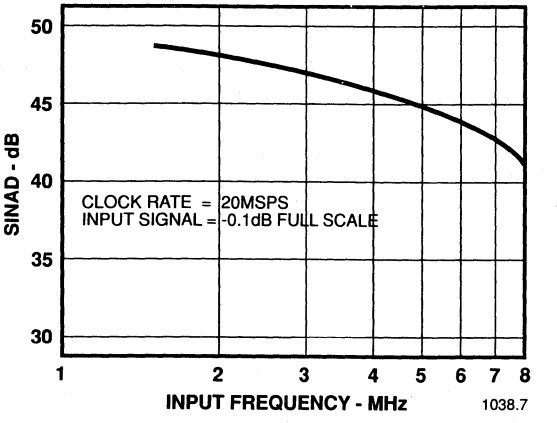


Figure 7. Typical SINAD vs. Input Frequency



Typical Interface Circuit

The Typical Interface Circuit (Figure 5) shows a wideband operational amplifier driving the A/D converter directly. Bipolar inputs to the op amp can be accommodated by adjusting the offset control. Raytheon Semiconductor's TDC4611 provides a stable reference for the offset and gain controls. All V_{IN} pins are connected close to the device package and the input amplifier's feedback loop should be closed at that point.

The buffer has an inverting gain of two, increasing a 1Vp-p video input signal to the recommended 2Vp-p input for the TDC1038. Proper decoupling is recommended for all systems.

The bottom reference voltage (V_{RB}) is supplied by an inverting amplifier or the TDC4611, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1038B6C	STD - T_A = 0°C to 70°C	Commercial	28-Pin CERDIP	1038B6C
TDC1038B6V	EXT - T_C = -55°C to 125°C	MIL-STD-883	28-Pin CERDIP	1038B6V
TDC1038N6C	STD - T_A = 0°C to 70°C	Commercial	28-Pin Plastic DIP	1038N6C
TDC1038R3C	STD - T_A = 0°C to 70°C	Commercial	28-Lead Plastic J-Leaded Chip Carrier	1038R3C

40G06121 Rev D 8/93

TDC1044
Monolithic Video A/D Converter
4-Bit, 25 Msps

Description

The TDC1044 is a 25 Msps (Megasample per second) full-parallel analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5 MHz into 4-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1044. All digital inputs and outputs are TTL compatible.

The TDC1044 consists of 15 latching comparators, encoding logic, and an output register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

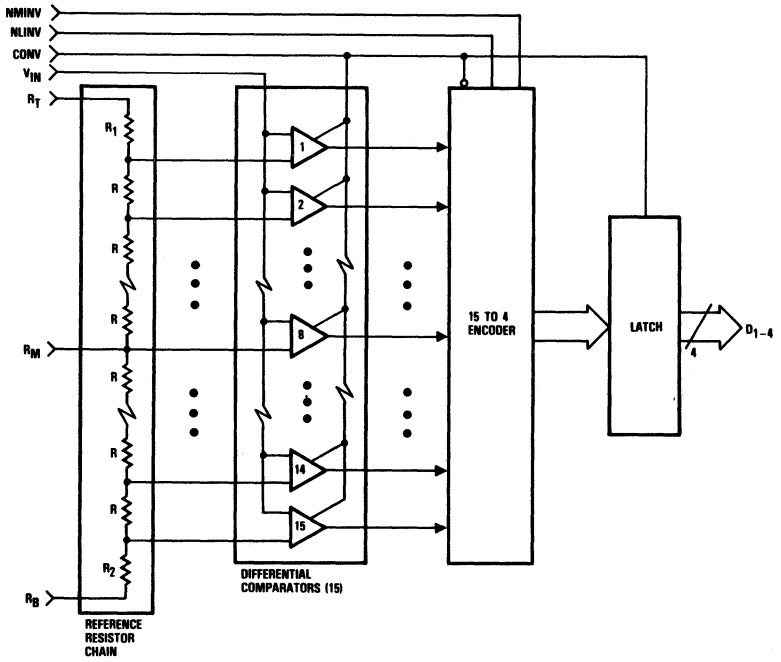
Features

- 4-bit resolution
- 1/4 LSB non-linearity
- Sample-and-hold circuit not required
- 25 Msps conversion rate
- Selectable output format
- Available in a 16-pin DIP and a 20-lead PLCC

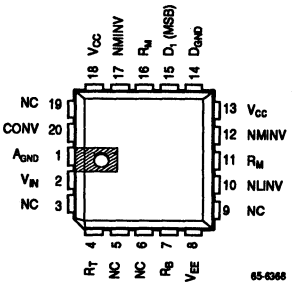
Applications

- Video special effects
- Radar data conversion
- Medical imaging
- Medical processing

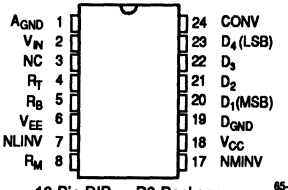
Functional Block Diagram



Pin Assignments



20 Lead PLCC — R4 Package



16 Pin DIP — B9 Package
16 Pin Plastic DIP — N9 Package

Functional Description

General Information

The TDC1044 has three functional sections: a comparator array, encoding logic, and an output register. The comparator array compares the input signal with 15 reference voltages to produce an N-of-15 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-15 code into binary or two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output register holds the output constant between updates.

Power

The TDC1044 operates from two power supply voltages, +5.0V and −5.2V. The return for I_{CC} (the current drawn from the +5.0V supply) is D_{GND}. The return for I_{EE} (the current drawn from the −5.2V supply) is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1044 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RB}$ into digital form. V_{RB} (the voltage applied to R_B at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to R_T at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.4V and 1.3V. The nominal voltages are V_{RT}=0.00V and V_{RB}=−1.00V. These voltages may be varied dynamically up to 10MHz. Due to slight variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required. A reference middle, R_M, is also provided; this may be used as an input to adjust the mid-scale point in order to improve integral linearity. This point may also be used as a tap to supply a mid-scale voltage to offset the analog input. If V_{RM} is used as an output, it must be connected to a high input impedance device which has small input current. Noise at this point may adversely affect the performance of the device.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1044 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within t_{STO} after a rising edge of CONV. The coded result is translated to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. New data becomes valid after a maximum delay time, t_D.

Analog Input

The TDC1044 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, the source impedance of the driving circuit must be less than 25 Ohms. The input signal will not damage the device if it remains within the range of V_{EE} to +0.5V. If the input signal is at a voltage between V_{RT} and V_{RB}, the output will be a binary code between 0 and 15 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1044 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. Data becomes valid after a maximum delay time (t_D) after the rising edge of CONV. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

No Connects

Pin 3 of the TDC1044 is labeled No Connect (NC), and has no connection to the chip. Connect this pin to A_{GND} for best noise performance.

Package Interconnections

Signal Type	Signal Name	Function	Value	B9, N9 Package Pins	R4 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	10	13
	V_{EE}	Negative Supply Voltage	-5.2V	6	8
	D_{GND}	Digital Ground	0.0V	11	14
	A_{GND}	Analog Ground	0.0V	1	1
Reference	R_T	Reference Resistor, Top	0.0V	4	4
	R_M	Reference Resistor, Middle	-0.5V	8	11
	R_B	Reference Resistor, Bottom	-1.0V	5	7
Controls	NMINV	Not MSB Invert	TTL	9	12
	NLINV	Not LSB Invert	TTL	7	10
Convert	CONV	Convert	TTL	16	20
Analog Input	V_{IN}	Analog Input Signal	0V to -1V	2	2
Outputs	D_1	MSB Output	TTL	12	15
	D_2		TTL	13	16
	D_3		TTL	14	17
	D_4	LSB Output	TTL	15	18
No Connects	NC	No Connect	A_{GND}	3	3, 5, 6, 9, 19

Figure 1. Timing Diagram

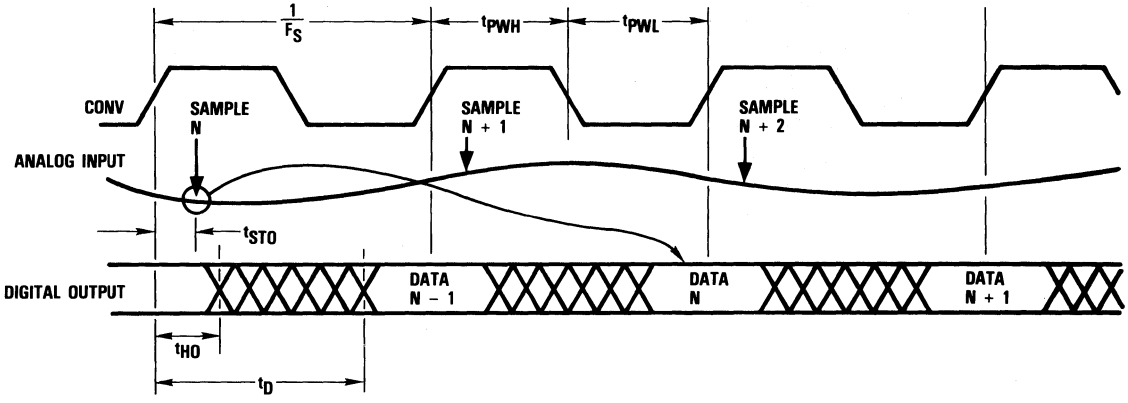


Figure 2. Simplified Analog Input Equivalent Circuit

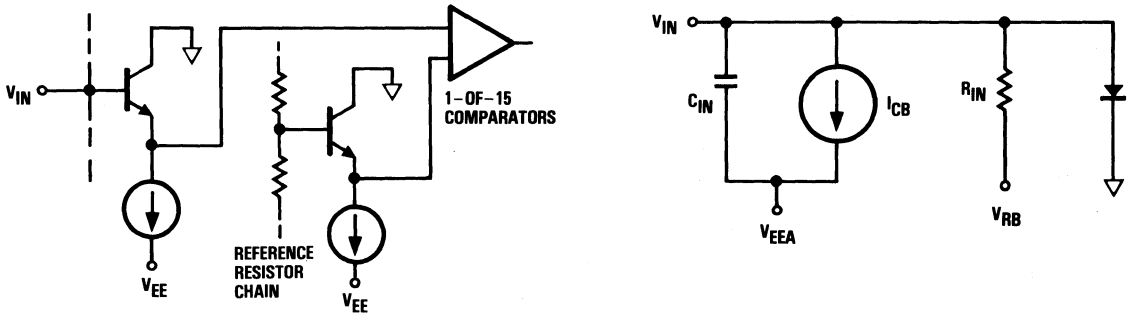


Figure 3. Digital Input Equivalent Circuit

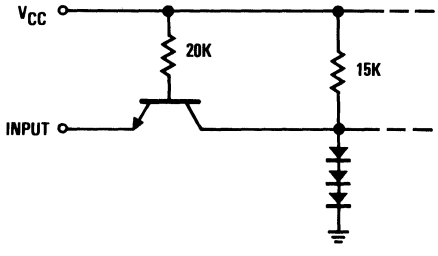
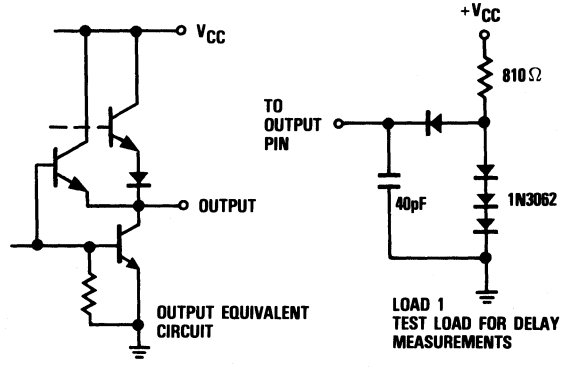


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +7.0V
V_{EE} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... −0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}V
V_{RT} (measured to V_{RB}) ..... −2.2 to +2.2V

Output

Applied voltage (measured to D_{GND}) ..... −0.5 to +5.5V [2]
Applied current, externally forced ..... −1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground) ..... 1 sec

Temperature

Operating, ambient ..... −55 to +125°C
junction ..... +150°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (Measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	17			17			ns
t_{PWH}	CONV Pulse Width, HIGH	17			17			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference	−1.9	0.0	0.1	−1.9	0.0	0.1	V
V_{RB}	Most Negative Reference	−2.1	−1.0	−0.1	−2.1	−1.0	−0.1	V
$V_{RT}-V_{RB}$	Reference Differential	0.2	1.0	2.0	0.2	1.0	2.0	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		15		20	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]					
		T_A = 0°C to 70°C		-50			mA
		T_A = 70°C		-40			mA
		T_C = -55°C to 125°C				-65	mA
		T_C = -125°C				-35	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		2		2	mA
R_{REF}	Total Reference Resistance		500		500		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	300		100		kOhms
C_{IN}	Input Capacitance			25		25	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		25		50	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, Output HIGH.		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case: all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		10		15	ns
t_D	Digital Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30		35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RB} = NOM		1.6		1.6	%
E_{LD}	Linearity Error Differential			1.6		1.6	%
CS	Code Size	V_{RT}, V_{RB} = NOM	75	125	75	125	% Nominal
E_{OT}	Offset Error Top	V_{IN} = V_{RT}		+30		+30	mV
E_{OB}	Offset Error Bottom	V_{IN} = V_{RB}		+40		+40	mV
T_{CO}	Offset Error Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		12.5		12.5		MHz
t_{TR}	Transient Response, Full Scale			10		10	ns
E_{AP}	Aperture Error			30		30	ps

Output Coding Table[1]

Range	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
-1.00V FS	NMINV = 1 NLINV = 1	0 0	0 1	1 0
0.000V	0000	1111	1000	0111
-0.067V	0001	1110	1001	0110
-0.133V	0010	1101	1010	0101
-0.200V	0011	1100	1011	0100
-0.267V	0100	1011	1100	0011
-0.333V	0101	1010	1101	0010
-0.400V	0110	1001	1110	0001
-0.467V	0111	1000	1111	0000
-0.533V	1000	0111	0000	1111
-0.600V	1001	0110	0001	1110
-0.667V	1010	0101	0010	1101
-0.733V	1011	0100	0011	1100
-0.800V	1100	0011	0100	1011
-0.867V	1101	0010	0101	1010
-0.933V	1110	0001	0110	1001
-1.000V	1111	0000	0111	1000

Note:

1. Input voltages are at code centers.

Calibration

To calibrate the TDC1044, adjust V_{RT} and V_{RB} to set the 1st and 15th thresholds to the desired voltages. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0033V (1/2 LSB from 0.000V) on the analog input, and adjust V_{RT} for output toggling between codes 0000 and 0001. Then apply −0.967V (1/2 LSB from −1.000V) and adjust V_{RB} for toggling between codes 1110 and 1111. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with an amplifier offset control. R_B is a convenient point for gain adjustment that is not in the analog signal path.

Typical Interface Circuit

The TDC1044 does not require a special input buffer amplifier to drive the analog input because of its low input capacitance. A terminated low-impedance transmission line (<100 Ohms) connected to the V_{IN} terminal of the device is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain stability. The ***Typical Interface Circuit*** in ***Figure 5*** shows a simple amplifier and voltage reference circuit that may be used with the device. U2 is a wide-band operational amplifier with a gain factor of −1. A small value resistor, R12, serves to isolate the small input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the amplifier are optimized by variable capacitor C12. The reference voltage for the TDC1044 is generated by amplifier U3. System gain is adjusted by varying R9 which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors R1 and R2. Formulas for calculating values for these input resistors are:

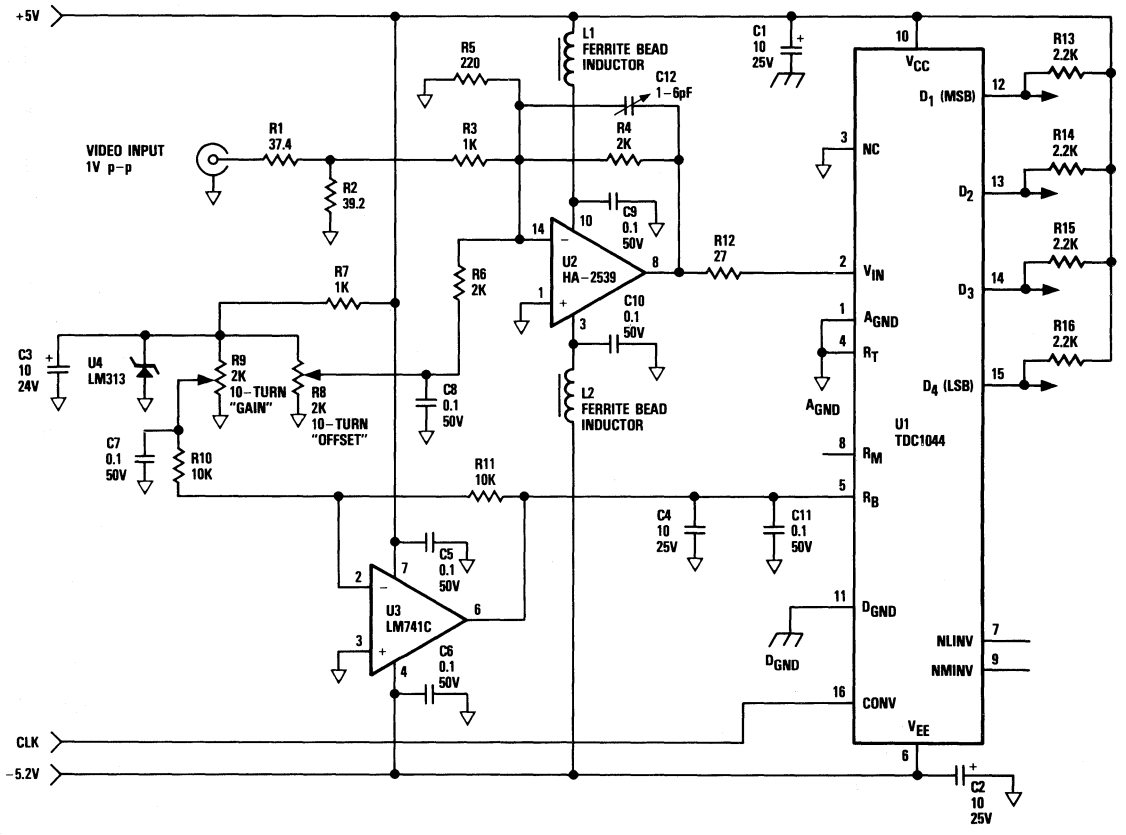
$$R1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

and

$$R2 = Z_{IN} - \left(\frac{1000\ R1}{1000 + R1}\right)$$

where VR is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R3. As shown, the circuit is set up for 1Vp-p 75 Ohm video input.

Figure 5. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1044B9C	STD - T_A = 0°C to 70°C	Commercial	16-Pin DIP	1044B9C
TDC1044B9V	EXT - T_C = -55°C to 125°C	MIL-STD-883	16-Pin DIP	1044B9V
TDC1044N9C	STD - T_A = 0°C to 70°C	Commercial	16-Pin Plastic DIP	1044N9C
TDC1044R4C	STD - T_A = 0°C to 70°C	Commercial	20-Lead PLCC	1044R4C

40G01899 Rev E 8/93

TDC1046
Monolithic Video A/D Converter
6-Bit, 25 Msps

Description

The TDC1046 is a 25 Msps (Megasample per second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5 MHz into 6-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1046. All digital inputs and outputs are TTL compatible.

The TDC1046 consists of 63 clocked latching comparators, encoding logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

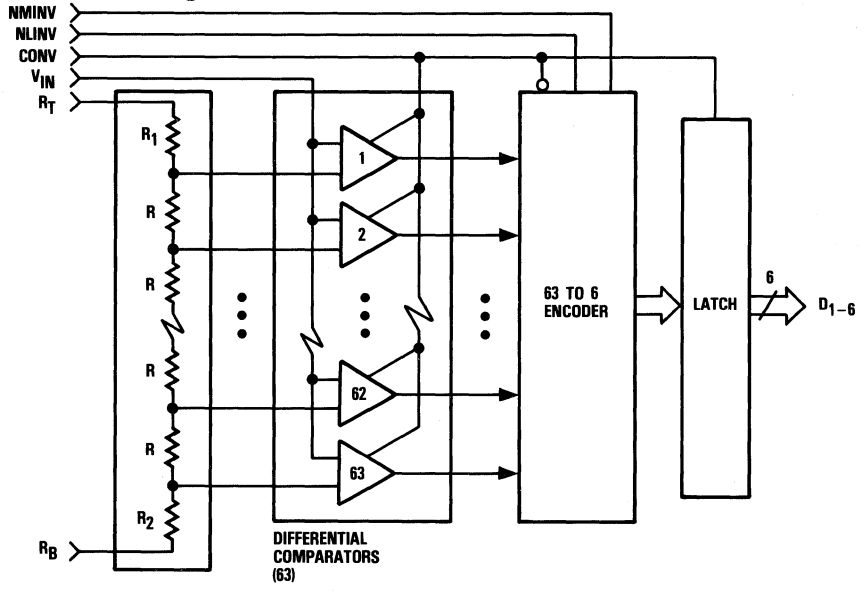
Features

- 6-bit resolution
- 1/4 LSB linearity
- Sample-and-hold circuit not required
- TTL compatible
- 25 Msps conversion rate
- Selectable output format
- Available in an 18-pin CERDIP
- Low cost
- Low analog inut capacitance
- Available per Standard Military Drawing

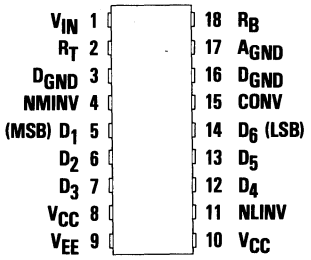
Applications

- Low-cost video digitizing
- Medical imaging
- Data acquisition
- TV special effects
- Video simulators
- Radar data conversion

Functional Block Diagram



Pin Assignments



18 Pin CERDIP – B8 Package

Functional Description

General Information

The TDC1046 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 63 reference voltages to produce an N-of-63 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-63 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1046 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1046 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to R_B at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to R_T at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT} - V_{RB}$) must be between 0.8V and 1.2V. The nominal voltages are $V_{RT} = 0.00V$ and $V_{RB} = -1.00V$. These voltages may be varied dynamically up to 12.5MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1046 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within 5ns (t_{STO}) after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. The 63 to 6 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Analog Input

The TDC1046 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, the source impedance of the driving circuit must be less than 50 Ohms. The input signal will not damage the TDC1046 if it remains within the range of V_{EE} to +0.5V. If the input signal is at a voltage between V_{RT} and V_{RB}, the output will be a binary number between 0 and 63 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1046 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. Data is guaranteed to be valid after a maximum delay time (t_D) after the rising edge of CONV. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Package Interconnections

Signal Type	Signal Name	Function	Value	B8 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	8, 10
	V_{EE}	Negative Supply Voltage	−5.2V	9
	D_{GND}	Digital Ground	0.0V	3, 16
	A_{GND}	Analog Ground	0.0V	17
Reference	V_{RT}	Reference Resistor (Top)	0.0V	2
	V_{RB}	Reference Resistor (Bottom)	−1.0V	18
Controls	NMINV	Not Most Significant Bit INVert	TTL	4
	NLINV	Not Least Significant Bit INVert	TTL	11
Convert	CONV	Convert	TTL	15
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	1
Outputs	D_1	MSB Output	TTL	5
	D_2		TTL	6
	D_3		TTL	7
	D_4		TTL	12
	D_5		TTL	13
	D_6	LSB Output	TTL	14

Output Coding Table [1]

Range	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV = 1	0	0	1
15.8730mV Step	NLINV = 1	0	1	0
0.0000V	000000	111111	100000	011111
−0.0159V	000001	111110	100001	011110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.4921V	011111	100000	111111	000000
−0.5079V	100000	011111	000000	111111
−0.5238V	100001	011110	000001	111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9841V	111110	000001	011110	100001
−1.0000V	111111	000000	011111	100000

Note: 1. Voltages are code midpoints when calibrated (see *Calibration* section).

Figure 1. Timing Diagram

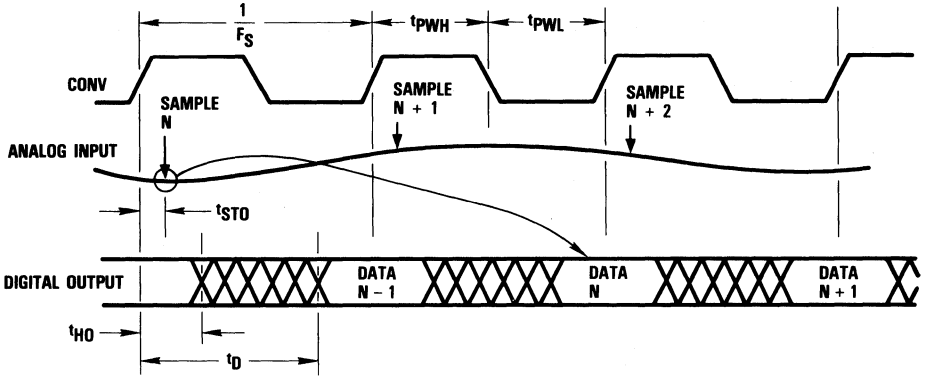


Figure 2. Simplified Analog Input Equivalent Circuit

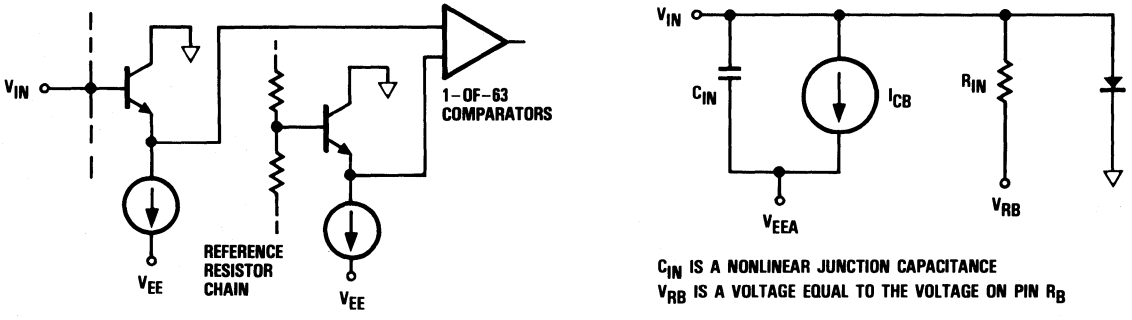


Figure 3. Digital Input Equivalent Circuit

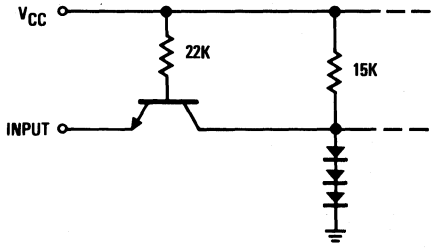
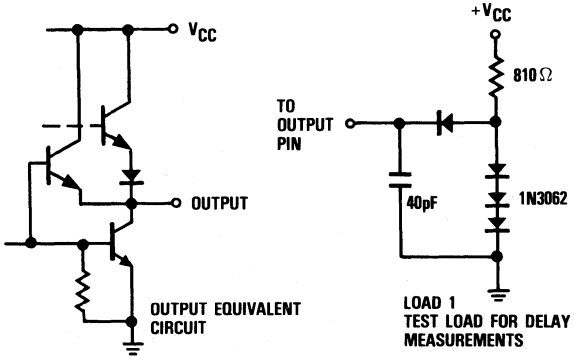


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+1.2 to −1.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V [2]
Applied current, externally forced	−1.0 to 6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width (LOW)	15			15			ns
t_{PWH}	CONV Pulse Width (HIGH)	17			17			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4			−0.4	mA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−1.0	−1.1	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8		1.2	0.8		1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		20		25	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]					
		T_A = 0°C to 70°C		-95			mA
		T_A = 70°C		-75			mA
		T_C = -55°C to 125°C				-150	mA
		T_C = 125°C				-75	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		10		15	mA
R_{REF}	Total Reference Resistance	V_{RT} - V_{RB} = MAX	100		66		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	40		40		kOhms
C_{IN}	Input Capacitance			30		30	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		105		180	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = 2 mA		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		5		10	ns
t_D	Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30		35	ns
t_{HO}	Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB}=Nom		0.4		0.4	%
E_{LD}	Linearity Error Differential			0.4		0.4	%
CS	Code Size	V_{RT}, V_{RB}=Nom	50	150	50	150	% Nominal
E_{OT}	Offset Error, Top	$V_{IN}=V_{RT}$		+50		+50	mV
E_{OB}	Offset Error, Bottom	$V_{IN}=V_{RB}$		−30		−30	mV
T_{CO}	Temperature Coefficient (Offset Voltage)			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		12.5		12.5		MHz
t_{TR}	Transient Response, Full-Scale			10		10	ns
SNR	Signal-to-Noise Ratio	12.5MHz Bandwidth, 25Msps Conversion Rate					
	Peak Signal/RMS Noise	1MHz Input	42		36		dB
		12.5MHz Input	40		32		dB
	RMS Signal/RMS Noise	1MHz Input	33		33		dB
		12.5MHz Input	31		29		dB
E_{AP}	Aperture Error			30		30	ps

Calibration

To calibrate the TDC1046, adjust V_{RT} and V_{RB} to set the 1st and 63rd thresholds to the desired voltages. In the ***Functional Block Diagram***, note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0079V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9921V and adjust V_{RB} for toggling between codes 62 and 63. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in *Figure 5*.

Typical Interface Circuit

The TDC1046 does not require a special input buffer amplifier to drive the analog input because of its low analog input capacitance. A terminated low-impedance transmission line (<100 Ohms) connected to the V_{IN} terminals of the TDC1046 is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain control. The *Typical Interface Circuit (Figure 5)* shows a simple buffer amplifier and voltage reference circuit that may be used with the TDC1046. U2 is a wide-band operational amplifier with a gain factor of −2. A small value resistor, R12, serves to help isolate the input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the buffer amplifier are optimized by variable capacitor C12.

The reference voltage for the TDC1046 is generated by amplifier U3 and PNP transistor Q1 which supplies the reference current. System gain is adjusted by varying R9 which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors R1 and R2. Formulas for calculating values for these input resistors are:

$$R1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

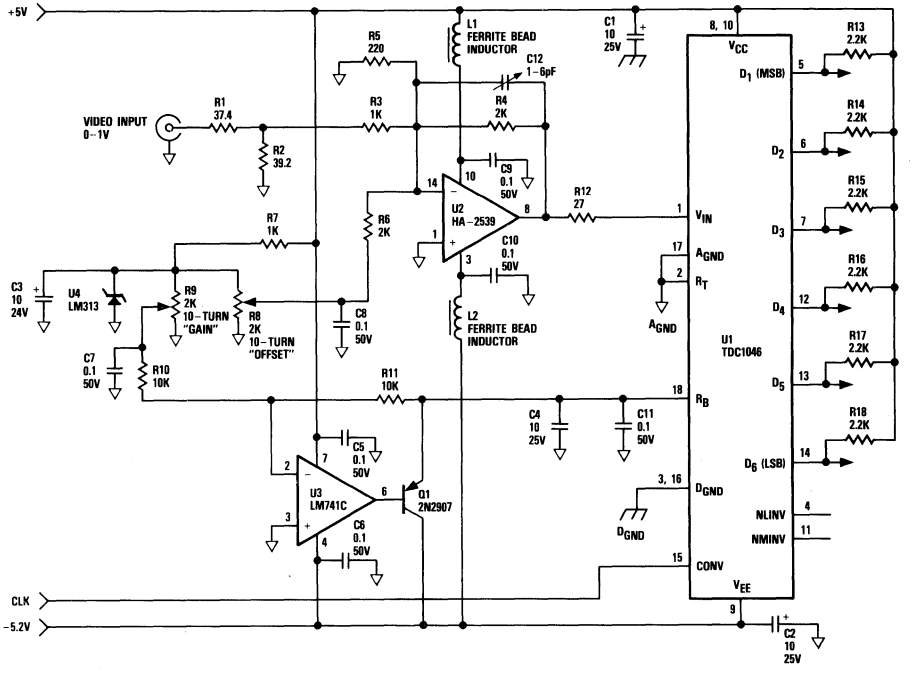
Typical Interface Circuit (cont.)

and

$$R2 = Z_{IN} - \left(\frac{1000\ R1}{1000 + R1}\right)$$

where VR is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R3. As shown, the circuit is set up for 1Vp-p 75 Ohm video input.

Figure 5. Typical Interface Circuit



Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

Standard Military Drawing	Nearest Equivalent TRW Product No.	Package
5962-87786-01VA	TDC1046B8V	18 Pin CERDIP

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1046B8C	STD–T_A=0°C to 70°C	Commercial	18 Pin CERDIP	1046B8C
TDC1046B8V	EXT–T_C=–55°C to 125°C	MIL-STD-883	18 Pin CERDIP	1046B8V
5962-87786 01VA	EXT–T_C=–55°C to 125°C	Per Standard Military Drawing	18 Pin CERDIP	5962-87786 01VA

40G01719 Rev F 8/93

TDC1047
Monolithic Video A/D Converter
7-Bit, 20 Msps

Description

The TDC1047 is a 20 Msps (Megasample per second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7 MHz into 7-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are TTL compatible.

The TDC1047 consists of 127 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

The TDC1047 is pin and function compatible with Raytheon Semiconductor La Jolla's TDC1027, and offers increased performance with lower power dissipation.

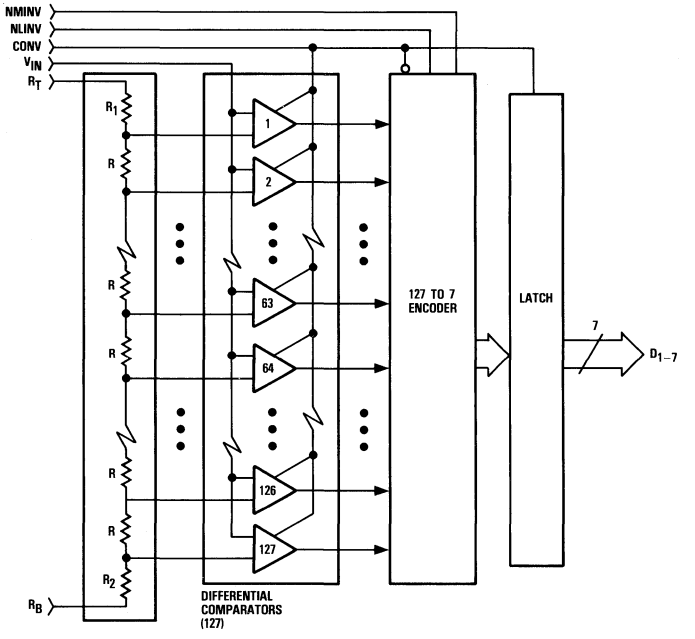
Features

- 7-bit resolution
- 1/2 LSB linearity
- Sample-and-hold circuit not required
- 20 Msps conversion rate
- Selectable output format
- Available in 24-pin CERDIP

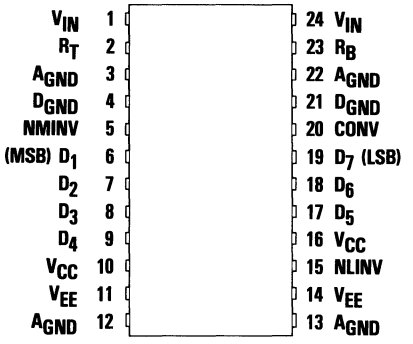
Applications

- Low-cost video digitizing
- Medical imaging
- TV special effects
- Video simulators
- Radar data conversion

Functional Block Diagram



Pin Assignments



24 Pin CERDIP – B7 Package

Functional Description

General Information

The TDC1047 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1047 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1047 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.8V and 1.2V. The nominal voltages are V_{RT}=0.00V and V_{RB}=−1.00V. These voltages may be varied dynamically up to 7MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically as in an Automatic Gain Control (AGC) circuit, a low-impedance reference source is recommended.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table.*** These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1047 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within the Sampling Time Offset (t_{STO}) of a rising edge on the CONV pin. The 127 to 7 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e., data for sample N is acquired by the external circuitry while the TDC1047 is taking input sample N+2.

Analog Input

The TDC1047 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, both V_{IN} pins must be used and the source impedance of the driving circuit must be less than 30 Ohms. The input signal will not damage the TDC1047 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1047 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	10, 16
	V_{EE}	Negative Supply Voltage	−5.2V	11, 14
	D_{GND}	Digital Ground	0.0V	4, 21
	A_{GND}	Analog Ground	0.0V	3, 12, 13, 22
Reference	R_T	Reference Resistor (Top)	0.00V	2
	R_B	Reference Resistor (Bottom)	−1.00V	23
Controls	NMINV	Not Most Significant Bit INVert	TTL	5
	NLINV	Not Least Significant Bit INVert	TTL	15
Convert	CONV	Convert	TTL	20
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	1, 24
Outputs	D_1	MSB Output	TTL	6
	D_2		TTL	7
	D_3		TTL	8
	D_4		TTL	9
	D_5		TTL	17
	D_6		TTL	18
	D_7	LSB Output	TTL	19

Figure 1. Timing Diagram

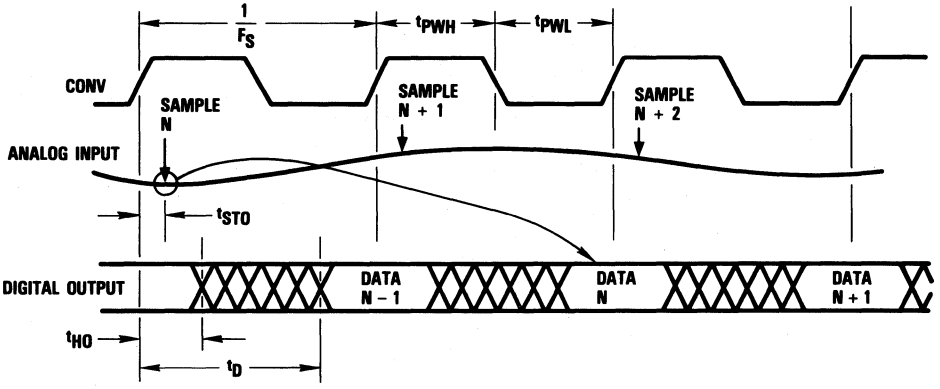
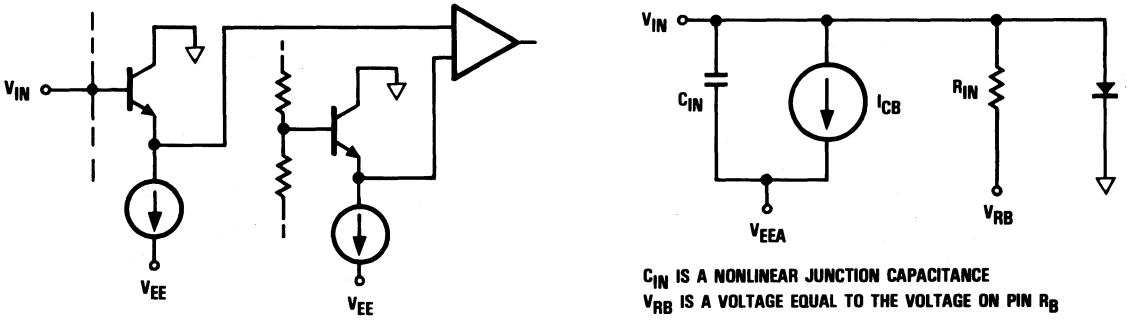


Figure 2. Simplified Analog Input Equivalent Circuit



C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

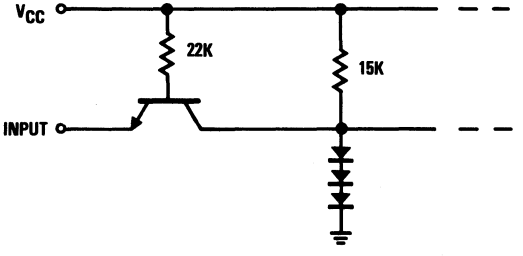
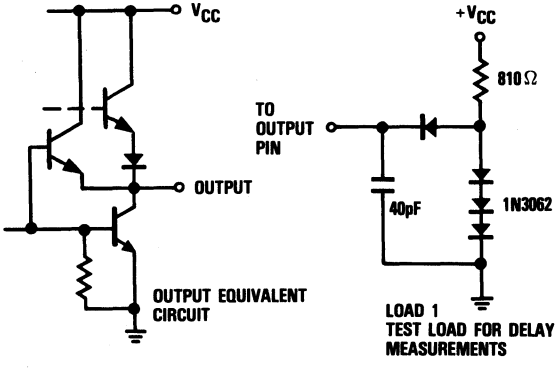


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V[2]
Applied current, externally forced	−1.0 to 6.0mA[3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to + 125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter	Test Conditions	Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	14			14			ns
t_{PWH}	CONV Pulse Width, HIGH	16			16			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4			−0.4	mA
V_{RT}	Most Positive Reference Input[1]	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input[1]	−0.9	−1.0	−1.1	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, static[1]		25		30	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, static[1]					
		T_A = 0°C to 70°C		-170			mA
		T_A = 70°C		-135			mA
		T_C = -55°C to 125°C				-220	mA
		T_C = 125°C				-130	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		35		50	mA
R_{REF}	Total Reference Resistance		28		20		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	100		40		kOhms
C_{IN}	Input Capacitance			60		60	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		150		300	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = Max, one pin to ground, one second duration.		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = Min, V_{EE} = Min	20		20		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = Min, V_{EE} = Min		7		10	ns
t_D	Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		30		35	ns
t_{HO}	Output Hold Time	V_{CC} = Max, V_{EE} = Max, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.4		0.4	%
E_{LD}	Linearity Error Differential			0.4		0.4	%
CS	Code Size	V_{RT}, V_{RB} = Nom	30	170	30	170	% Nominal
V_{OT}	Offset Voltage Top	V_{IN} = V_{RT}		+50		+50	mV
V_{OB}	Offset Voltage Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		7		7		MHz
t_{TR}	Transient Response, Full Scale			10		10	ns
SNR	Signal-to-Noise Ratio	7MHz Bandwidth,					
		20MSPS Conversion Rate					
	Peak Signal/RMS Noise	1MHz Input	48		46		dB
		7MHz Input	46		44		dB
	RMS Signal/RMS Noise	1MHz Input	39		37		dB
		7MHz Input	37		35		dB
E_{AP}	Aperture Error			50		50	ps
DP	Differential Phase Error[1]	F_S = 4 x NTSC		1.5		1.5	Degree
DG	Differential Gain Error[1]	F_S = 4 x NTSC		2.5		2.5	%

Note:
1. In excess of quantization.

Output Coding

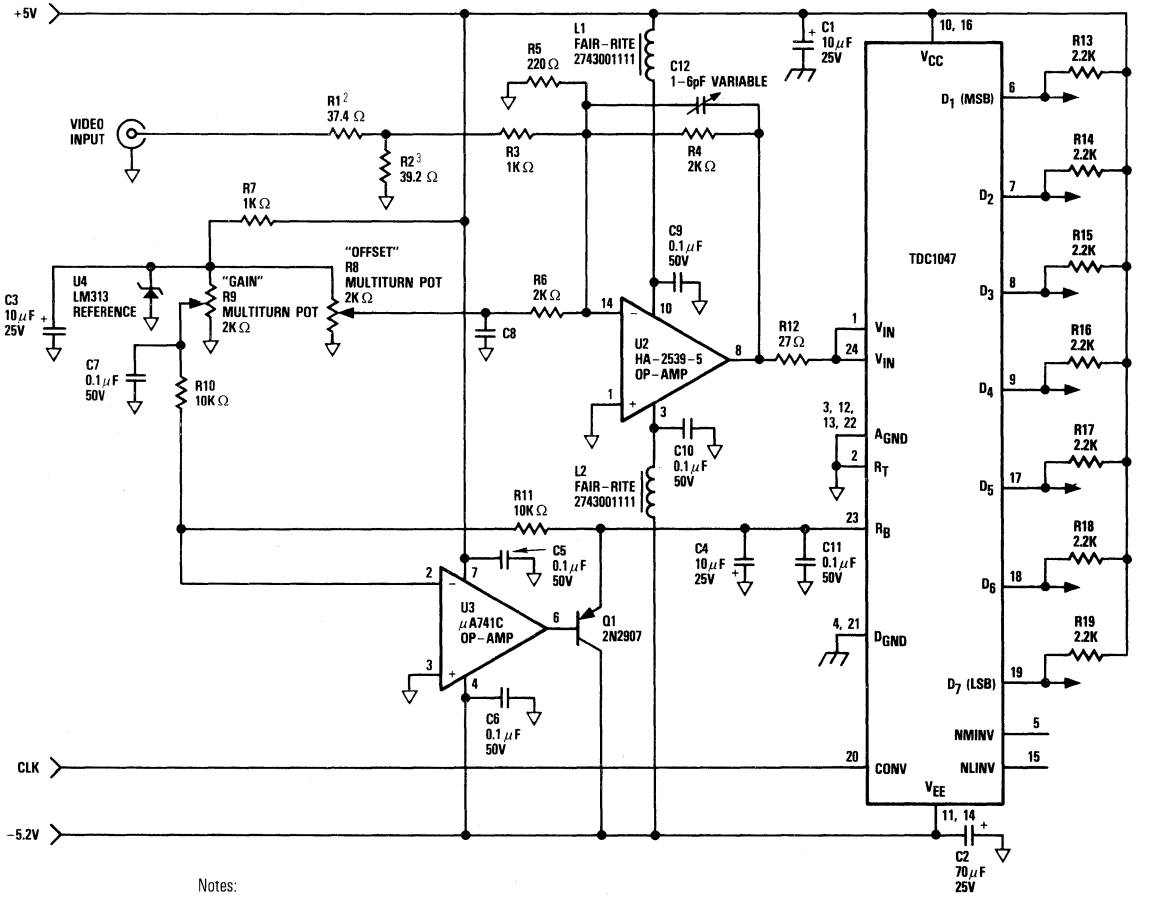
Step		Binary		Offset Two's Complement	
	Range	True	Inverted	True	Inverted
	−1.0000V FS 7.874mV STEP	NMINV = 1 NLINV = 1	0 0	0 1	1 0
000	0.0000V	0000000	1111111	1000000	0111111
001	−0.0078V	0000001	1111110	1000001	0111110
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
063	−0.4960V	0111111	1000000	1111111	0000000
064	−0.5039V	1000000	0111111	0000000	1111111
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
126	−1.9921V	1111110	0000001	0111110	1000001
127	−1.0000V	1111111	0000000	0111111	1000000

Note:
1. Voltages are code midpoints when calibrated (see Calibration Section).

Calibration

To calibrate the TDC1047, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages in the block diagram. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0039V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9961V and adjust V_{RB} for toggling between codes 126 and 127. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Figure 5. Typical Interface Circuit



Notes:

1. Unless otherwise specified, all resistors are 1/4W, 2%.

2. $R1 = Z_{IN} - \left(\frac{1000\ R2}{1000 + R2}\right)$

3. $R2 = \frac{1}{\left(\frac{2V_{Range}}{V_{REF}\ Z_{IN}}\right) - 0.001}$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1047B7C	STD–T_A=0°C to 70°C	Commercial	24 Pin CERDIP	1047B7C
TDC1047B7V	EXT–T_C= –55°C to 125°C	MIL-STD-883	24 Pin CERDIP	1047B7V

40G01393 Rev F 8/93

TDC1048
Monolithic Video A/D Converter
8-Bit, 20 Msps

Description

The TDC1048 is a 20 Msps (Megasample per second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7 MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. Low power consumption eases thermal considerations, and board space is minimized with a 28-pin package. All digital inputs and outputs are TTL compatible.

The TDC1048 consists of 255 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

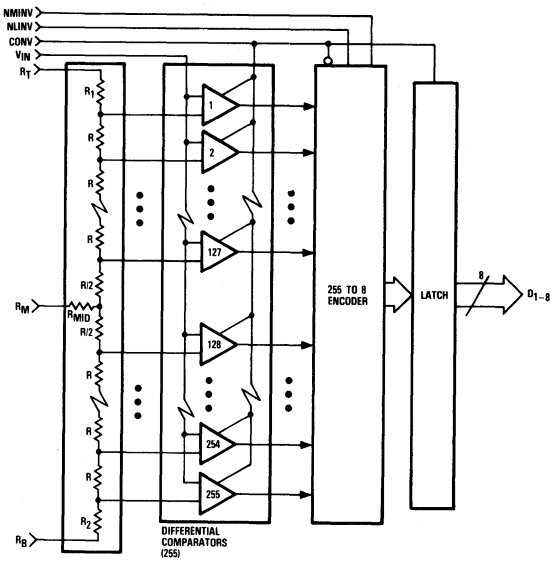
Features

- 8-bit resolution
- 20 Msps conversion rate
- Sample-and-hold circuit not required
- Differential phase 1 degree
- Differential gain 2.0%
- 1/2 LSB linearity
- Guaranteed monotonic
- TTL compatible outputs
- Selected data format
- Available in 28-pin plastic DIP, CERDIP, or LCC
- Mil-Std-883 compliant screening available
- Available per standard military drawing

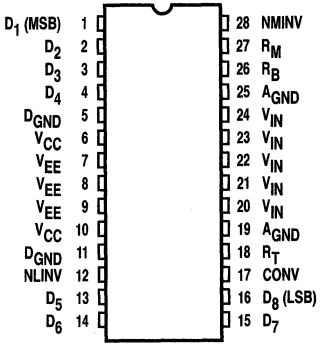
Applications

- Low-cost video digitizing
- Radar data conversion
- Data acquisition
- Medical imaging

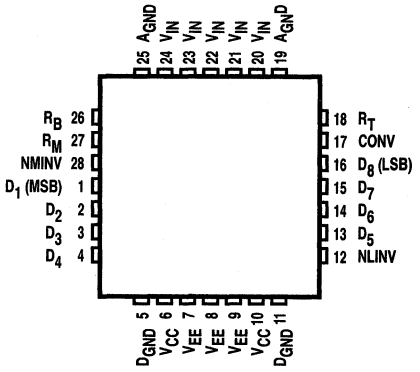
Functional Block Diagram



Pin Assignments



28 Pin CERDIP – B6 Package
28 Pin Plastic DIP – N6 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1048 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-255 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1048 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1048 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and −2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 1.8V and 2.2V. The nominal voltages are V_{RT}=0.0V, V_{RB}=−2.0V.

A midpoint tap, R_M, allows the converter to be adjusted for optimum linearity, although adjustment is not necessary to meet the linearity specification. It can also be used to achieve a nonlinear transfer function. The circuit shown in ***Figure 5*** will provide approximately 1/2 LSB adjustment of the linearity midpoint. The characteristic impedance seen at this node is approximately 220Ω, and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and noise introduced at this point will degrade the quantization process.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically, (as in an automatic gain control circuit), a low-impedance reference source is required. The reference voltages may be varied dynamically up to 5MHz.

Control

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW, as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1048 requires a convert (CONV) signal. A sample is taken (the comparators are latched) within 15ns after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short-term uncertainty (jitter) in sampling offset time is less than 100 picoseconds. The 255 to 8 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. New data becomes valid after a Digital Output Delay, t_D, time. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e., data for sample N is acquired by the external circuitry while the TDC1048 is taking input sample N+2.

Analog Input

The TDC1048 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance of the driving device must be less than 25Ω. The input signal will not damage the TDC1048 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 255 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. All five analog input pins must be connected together.

Outputs

The outputs of the TDC1048 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal. For optimum performance, 2.2 kΩ pull-up resistors are recommended.

Package Interconnections

Signal Type	Signal Name	Function	Value	B6, N6, C3 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	6, 10
	V_{EE}	Negative Supply Voltage	−5.2V	7, 8, 9
	D_{GND}	Digital Ground	0.0V	5, 11
	A_{GND}	Analog Ground	0.0V	19, 25
Reference	R_T	Reference Resistor (Top)	0.0V	18
	R_M	Reference Resistor (Middle)	−0.996V	27
	R_B	Reference Resistor (Bottom)	−2.0V	26
Controls	NMINV	Not Most Significant Bit INVert	TTL	28
	NLINV	Not Least Significant Bit INVert	TTL	12
Convert	CONV	Convert	TTL	17
Analog Input	V_{IN}	Analog Signal Input	0V to −2V	20, 21, 22, 23, 24

Package Interconnections (cont.)

Signal Type	Signal Name	Function	Value	B6, N6, C3, R3 Package Pins
Outputs	D_1	MSB Output	TTL	1
	D_2		TTL	2
	D_3		TTL	3
	D_4		TTL	4
	D_5		TTL	13
	D_6		TTL	14
	D_7		TTL	15
	D_8	LSB Output	TTL	16

Figure 1. Timing Diagram

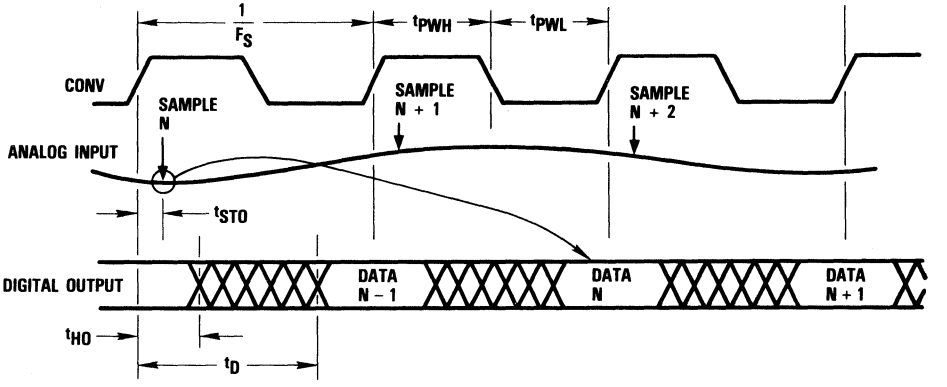
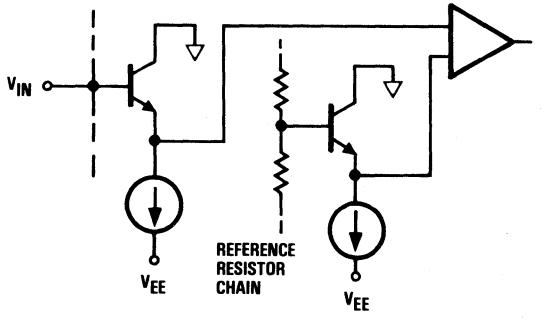
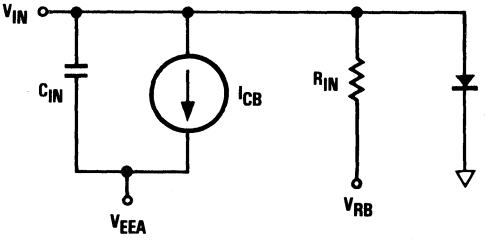


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Convert Input Equivalent Circuit

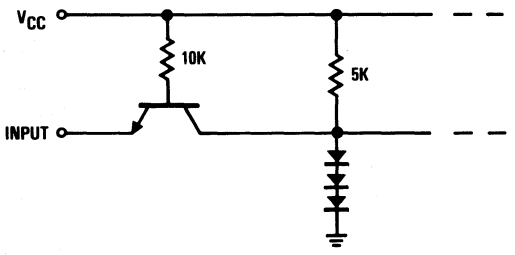
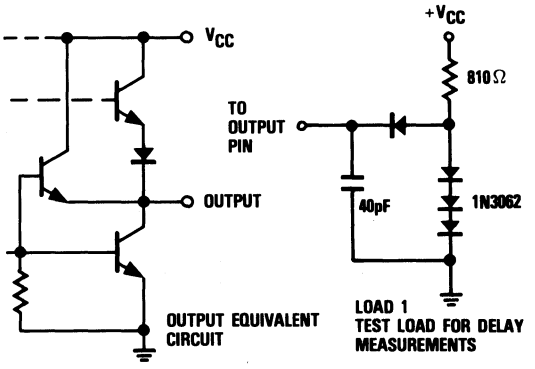


Figure 4. Output Circuits



Output Coding Table

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2.0000V FS 7.8431mV Step	−2.0480V FS 8.000mV Step	NMINV=1 NLINV=1	0 0	0 1	1 0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	−0.0078V	−0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0039V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0118V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0320V	11111110	00000001	01111110	10000001
255	−2.0000V	−2.0400V	11111111	00000000	01111111	10000000

Notes: 1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V for a logical "1" and tied to ground for a logical "0."
2. Voltages are code midpoints when calibrated by the procedure given below.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in HIGH state to ground)	1 Second

Temperature

Operating, ambient	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

		Temperature Range						
		Standard			Extended			
Parameter		**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Units**
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{EE}	Negative Supply Voltage	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0	+0.1	−0.1	0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	18			18			ns
t_{PWH}	CONV Pulse Width, HIGH	22			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	−1.9	−2.0	−2.1	−1.9	−2.0	−2.1	V
V_{RT}-V_{RB}	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note: 1 V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC}=Max, static [1]		35		40	mA
I_{EE}	Negative Supply Current	V_{EE}=Max, static [1]					
		T_A=0°C to 70°C		−260			mA
		T_A=70°C		−185			mA
		T_C=−55°C to 125°C				−320	mA
		T_C=125°C				−180	mA
I_{REF}	Reference Current	V_{RT}, V_{RB}=Nom		40		50	mA
R_{REF}	Total Reference Resistance		50		40		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB}=Nom, V_{IN}=V_{RB}	10		10		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB}=Nom, V_{IN}=V_{RB}		100		100	pF
I_{CB}	Input Constant Bias Current	V_{EE}=Max		200		550	μA
I_{IL}	Input Current, Logic LOW	V_{CC}=Max, V_I=0.5V					
		CONV		−0.4		−0.4	mA
		NMINV, NLINV		−0.6		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC}=Max, V_I=2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC}=Max, V_I=5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC}=Min, I_{OL}=Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC}=Min, I_{OH}=Max	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC}=Max, Output HIGH, one pin to ground, one second duration max.		−30		−30	mA
C_I	Digital Input Capacitance	T_A=25°C, F=1MHz		15		15	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC}=Min, V_{EE}=Min	20		20		Msps
t_{STO}	Sampling Time Offset	V_{CC}=Min, V_{EE}=Min	0	10	0	15	ns
t_D	Digital Output Delay	V_{CC}=Min, V_{EE}=Min, Load 1		30		35	ns
t_{HO}	Digital Output Hold Time	V_{CC}=Max, V_{EE}=Max, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB}=Nom		0.2		0.2	%
E_{LD}	Linearity Error Differential			0.2		0.2	%
CS	Code Size		25	175	25	175	% Nominal
E_{OT}	Offset Error, Top	$V_{IN}=V_{RT}$		+40		+40	mV
E_{OB}	Offset Error, Bottom	$V_{IN}=V_{RB}$		−30		−30	mV
T_{CO}	Offset Error, Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		7		5		MHz
t_{TR}	Transient Response, Full-Scale			20		20	ns
SNR	Signal-to-Noise Ratio	20Msps Conversion Rate, 10MHz Bandwidth					
	Peak Signal/RMS Noise	1.248MHz Input	54		53		dB
		2.438MHz Input	53		52		dB
	RMS Signal/RMS Noise	1.248MHz Input	45		44		dB
		2.438MHz Input	44		43		dB
E_{AP}	Aperture Error			60		60	ps
DP	Differential Phase Error	F_S=4 x NTSC		1.0		1.0	Degree
DG	Differential Gain Error	F_S=4 x NTSC		2.0		2.0	%
NPR	Noise Power Ratio	DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 20Msps Conversion Rate	36.5		36.5		dB

Calibration

To calibrate the TDC1048, adjust V_{RT} and V_{RB} to set the 1st and 255th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −2V desired range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.996V (1/2 LSB from −2V) and adjust V_{RB} for toggling between codes 62 and 63.

The degree of required adjustment is indicated by the offset error, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the *Functional Block Diagram*. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method of calibration requires that both ends of the resistor chain, R_T and R_B, are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in *Figure 6*.

Typical Interface

Figure 6 shows an example of a typical interface circuit for the TDC1048. The analog input amplifier is a bipolar wideband operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. TRW's TDC4611 provides a stable reference for both the offset and gain control. All five V_{IN} pins are connected close to the device package, and the buffer amplifier feedback loop should be closed at that point. The buffer has a gain of minus two, increasing a 1Vp-p video input signal to the recommended 2Vp-p input for the A/D converter. Proper decoupling is recommended for all systems.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier on the **LM611**, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the ***Calibration*** section.

Figure 5. Typical Reference Midpoint Adjust Circuit

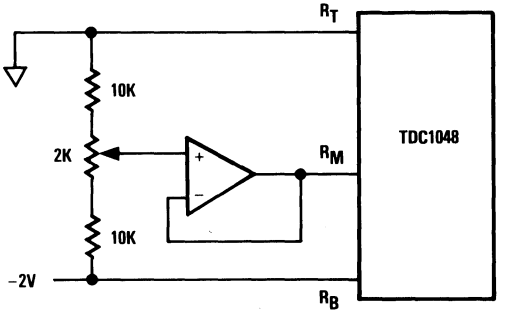
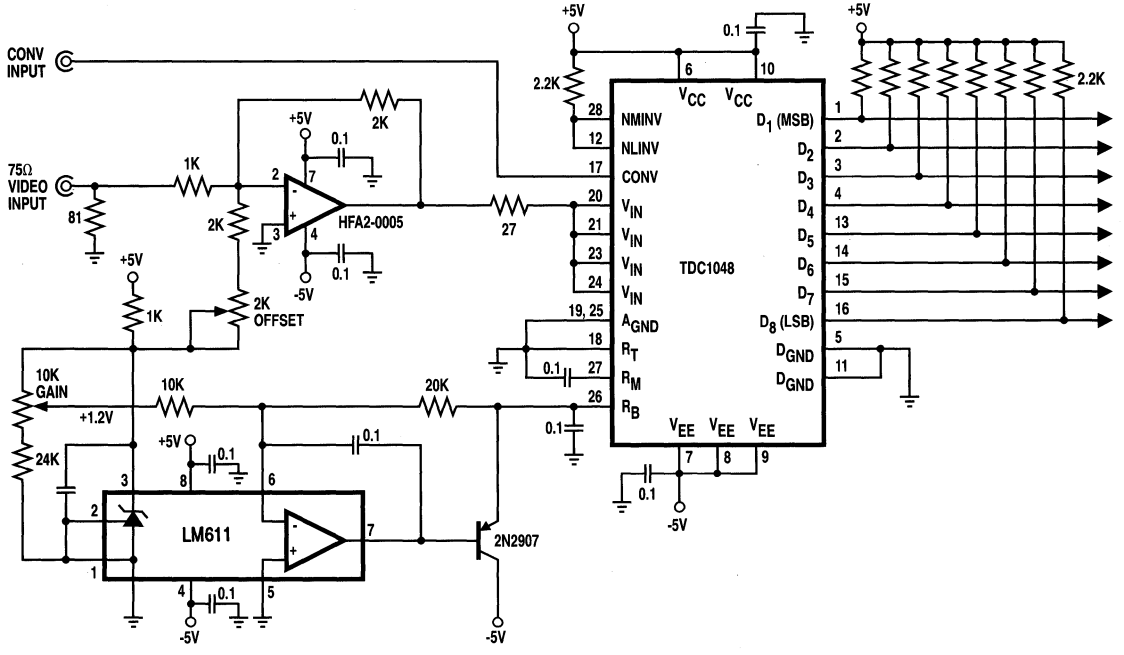


Figure 6. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
5962-8760001XA	EXT - T_C = -55°C to 125°C	Per Standard Mil Drawing	28-Pin Ceramic DIP	5962-8760001XA
TDC1048C3C	STD - T_A = 0°C to 70°C	Commercial	28-Contact LCC	1048C3C
TDC1048C3V	EXT - T_C = -55°C to 125°C	MIL-STD-883	28-Contact LCC	1048C3V
5962-87600013A	EXT - T_C = -55°C to 125°C	Per Standard Mil Drawing	28-Contact LCC	5962-87600013A
TDC1048B6C	STD - T_A = 0°C to 70°C	Commercial	28-Pin CERDIP	1048B6C
TDC1048B6V	EXT - T_C = -55°C to 125°C	MIL-STD-883	28-Contact LCC	1048B6V
TDC1048C3C	STD - T_A = 0°C to 70°C	Commercial	28-Contact LCC	1048C3C

40G01216 Rev I 8/93

TDC1049
High-Speed A/D Converter
9-Bit, 30 Msps

Description

The TDC1049 is a flash (full-parallel) analog-to-digital converter capable of converting analog signals with full-power frequency components up to 15 MHz into 9-bit words at rates up to 30 Msps (Megasamples Per Second). A sample-and-hold circuit is not required. All digital inputs and outputs are differential ECL.

The TDC1049 consists of 512 latching comparators, encoding logic and an output register. A differential convert signal controls the conversion operation. The outputs can be connected to give either true or inverted binary or offset two's complement formats.

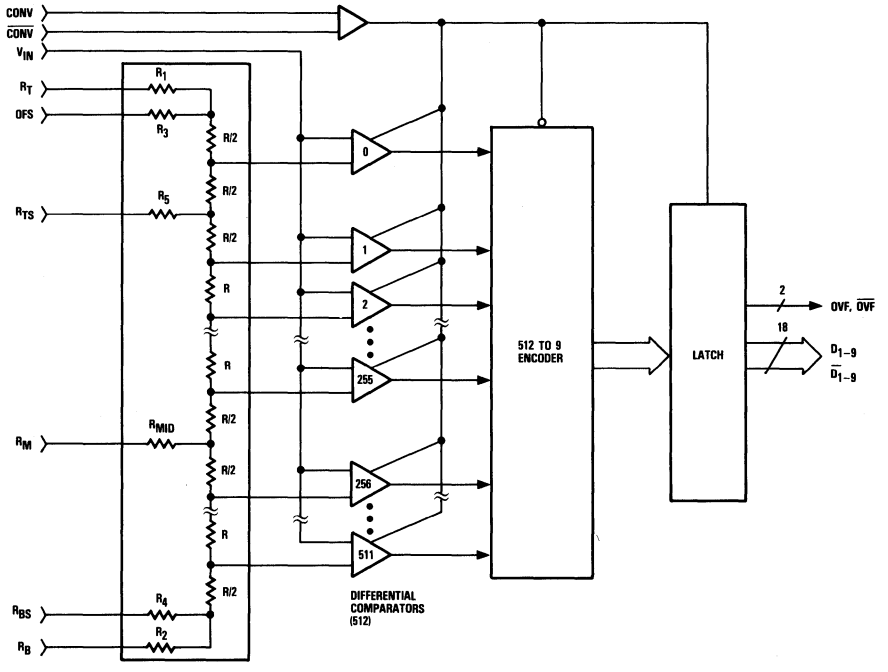
Features

- 30 Msps conversion rate, 15 MHz analog bandwidth
- 9-Bit resolution and linearity
- Sample-and-hold circuit not required
- Differential phase 0.5 degrees
- Differential gain 1.0%
- Overflow flag
- Single -5.2V power supply
- Differential ECL outputs
- Available in a 64-pin DIP, 68-contact LCC and 68-pin ceramic pin grid array

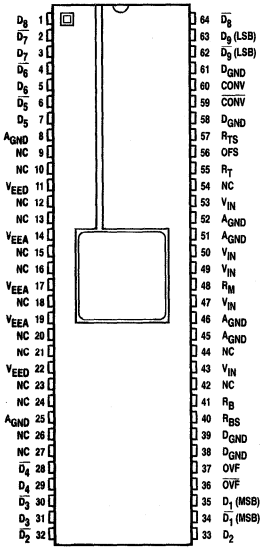
Applications

- Video data conversion
- Radar data conversion
- High-speed data acquisition

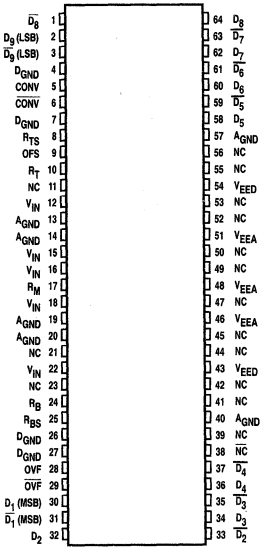
Functional Block Diagram



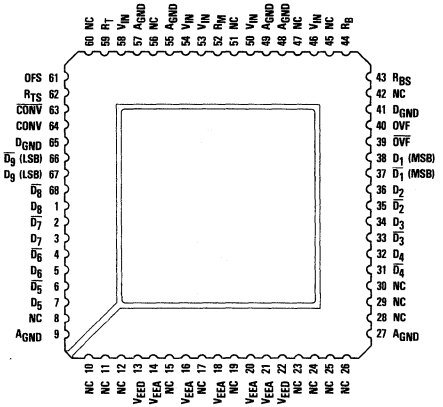
Pin Assignments



64 Pin DIP – J0 Package



64 Pin DIP – J3 Package

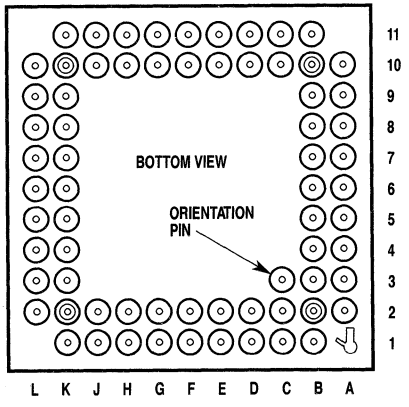


68 Contact LCC – C1 Package

Pin Assignments

68 Pin Ceramic Pin Grid Array, G8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	V_{EEA}	F10	D_8	K4	A_{GND}
A3	V_{EED}	B10	NC	F11	$\overline{D_7}$	K5	V_{IN}
A4	NC	B11	A_{GND}	G1	D_1	K6	V_{IN}
A5	NC	C1	NC	G2	$\overline{D_1}$	K7	NC
A6	NC	C2	NC	G10	D_9	K8	A_{GND}
A7	NC	C10	D_5	G11	$\overline{D_8}$	K9	V_{IN}
A8	NC	C11	NC	H1	$\overline{OVF}$	K10	R_{TS}
A9	NC	D1	D_4	H2	OVF	K11	$\overline{CONV}$
A10	V_{EED}	D2	$\overline{D_4}$	H10	D_{GND}	L2	NC
B1	NC	D10	D_6	H11	$\overline{D_9}$	L3	NC
B2	A_{GND}	D11	$\overline{D_5}$	J1	NC	L4	A_{GND}
B3	V_{EEA}	E1	D_3	J2	D_{GND}	L5	R_M
B4	NC	E2	$\overline{D_3}$	J10	CONV	L6	NC
B5	V_{EEA}	E10	D_7	J11	D_{GND}	L7	V_{IN}
B6	V_{EEA}	E11	$\overline{D_6}$	K1	R_{BS}	L8	A_{GND}
B7	V_{EEA}	F1	D_2	K2	R_B	L9	R_T
B8	NC	F2	$\overline{D_2}$	K3	V_{IN}	L10	OFS



Functional Description

General Information

The TDC1049 has three functional sections: a comparator array, encoding logic and output register. The comparator array compares the input signal with 512 reference voltages to produce an N-of-512 code or "thermometer" code. The comparators referenced to voltages less than the input signal will be on and those referenced to voltages greater than the input signal will be off. The encoding logic converts the N-of-512 code into 9-bit binary data. The output register holds the output between updates.

Power

For optimum performance, separate analog and digital power, V_{EEA} and V_{EED} should be supplied to the TDC1049. Separate analog and digital power supplies or a common supply with separate analog and digital paths and high-frequency decoupling can be used. The return path for the current drawn from V_{EEA} and V_{EED} is A_{GND} and D_{GND}, respectively. The returns A_{GND} and D_{GND} should also be kept separate and connected together at the power supply terminals. It is recommended that provisions be made on the printed circuit board for shorting jumpers between analog and digital ground as close to the A/D converter as possible. The installation of the jumpers depends upon the printed circuit board layout and overall system performance once the system is in operation. The voltage difference between V_{EEA} and V_{EED} must be less than $\pm 0.1V$. The same voltage difference limit applies to the difference between A_{GND} and D_{GND}. All power and ground inputs to the converter must be connected.

Reference

The TDC1049 converts analog signals in the range $V_{RB} < V_{IN} < V_{RT}$ into digital form. V_{RB} (the voltage applied to R_B) at the bottom of the reference resistor chain, and V_{RT} (the voltage applied to R_T) at the top of the reference resistor chain, should both be between $+0.1V$ and $-2.1V$. Within that range, V_{RT} must be more positive than V_{RB}. The linearity specification is based upon a 2.0V difference between V_{RT} and V_{RB}. The nominal voltages are $V_{RT} = 0.0V$ and $V_{RB} = -2.0V$. To avoid damage to the converter, the voltage across V_{RT} and V_{RB} must not exceed 2.2V. A decoupling capacitor is recommended between R_B and A_{GND}. Noise introduced at this point, as well as the other reference inputs (R_T, R_{TS}, R_M, R_{BS}, OFS), may result in encoding errors.

A midpoint tap, R_M, allows the converter to be adjusted for optimum integral linearity. It can also be used to achieve a nonlinear transfer function, but adjustment of R_M is not required to meet 9-bit linearity. If this node is driven by external circuitry, it should be driven from a low-impedance source; if not used, it must be left open.

Parasitic resistances, R1 and R2, introduce offset errors at the top and bottom of the reference resistor chain. Sense points, R_{TS}, R_{BS} and OFS, may be used to reduce the effect of these offset errors. Overflow Sense (OFS) may be used to reduce the effect of the offset at the overflow (most positive) comparator whenever the Overflow (OVF, $\overline{OVF}$) flags are used. Sense points are not required for 9-bit linearity and, if not used, they must be left open.

Convert

The TDC1049 requires a differential ECL clock (CONV and $\overline{CONV}$) signal. The conversion occurs (the comparators are latched) within t_{STO} (Sampling Time Offset) of the rising edge of CONV. The 512 to 9 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output register on the next rising edge of CONV. Data for sample N is available at the output t_D (Output Delay Time) after the rising edge of sample N+1.

Analog Input

The TDC1049 uses latching comparators which are connected to the analog inputs V_{IN}. For optimal performance, the source impedance of the driver amplifier should be less than 25Ω. The input signal will not damage the TDC1049 if it remains within the range of V_{EEA} to $+0.5V$. If the input signal is between the V_{RT} and V_{RB}, the output will be a binary number between 0 and 511 inclusive. All five analog inputs must be connected.

Outputs

The outputs of the TDC1049 are differential ECL. The recommended pull-down resistance is 500Ω to $-2V$, or a 220/330Ω termination between D_{GND} and V_{EED}. The OVF signal indicates that the analog input has exceeded the threshold of the most positive comparator. Data is held valid at the output register for at least t_{HO} (Output Hold Time) after the rising edge of CONV. New data becomes valid t_D after the rising edge of CONV.

No Connects

There are several pins labeled NC (No Connect). These pins are not connected internally and may be either left open or connected to analog ground to aid heat transfer from the package and to reduce electrical noise.

Package Interconnections

Signal Name	Function	Value	J3 Package Pins	J0 Package Pins	C1 Package Pins	G8 Package Pins
V_{EEA}	Analog Supply Voltage	−5.2V	46, 48, 51	14, 17, 19	14, 16, 18, 20, 21	B9, B7, B6, B5
V_{EED}	Digital Supply Voltage	−5.2V	43, 54	11, 22	13, 22	A3, A10
D_{GND}	Digital Ground	0.0V	4, 7, 26, 27	38, 39, 58, 61	41, 65	J2, J11, H10
A_{GND}	Analog Ground	0.0V	13, 14, 19, 20, 40, 57	8, 25, 45, 46, 51, 52	9, 27, 48, 49, 55, 57	B2, K4, L4, K8, L8, B11
R_T	Reference Resistor, Top	0.0V	10	55	59	L9
R_{TS}	Reference Resistor, Top Sense	0.0V	8	57	62	K10
R_B	Reference Resistor, Bottom	−2.0V	24	41	44	K2
R_{BS}	Reference Resistor, Bottom Sense	−2.0V	25	40	43	K1
R_M	Reference Resistor, Midpoint	−1.0V	17	48	52	L5
OFS	Overflow Sense	0.0V	9	56	61	L10
CONV	Convert	ECL	5	60	64	J10
$\overline{CONV}$	Convert, Complement	ECL	6	59	63	K11
V_{IN}	Analog Signal Input	0V to −2V	12, 15, 16, 18, 22	43, 47, 49, 50, 53	46, 50, 53, 54, 58	K3, K5, K6, L7, K9
D_1 MSB	Most Significant Bit	ECL	30	35	38	G1
$\overline{D_1}$ $\overline{MSB}$	Most Significant Bit Complement	ECL	31	34	37	G2
D_2		ECL	32	33	36	F1
$\overline{D_2}$		ECL	33	32	35	F2
D_3		ECL	34	31	34	E1
$\overline{D_3}$		ECL	35	30	33	E2
D_4		ECL	36	29	32	D1
$\overline{D_4}$		ECL	37	28	31	D2
D_5		ECL	58	7	7	C10
$\overline{D_5}$		ECL	59	6	6	D11
D_6		ECL	60	5	5	D10
$\overline{D_6}$		ECL	61	4	4	E11
D_7		ECL	62	3	3	E10
$\overline{D_7}$		ECL	63	2	2	F11
D_8		ECL	64	1	1	F10
$\overline{D_8}$		ECL	1	64	68	G11
D_9 LSB	Least Significant Bit	ECL	2	63	67	G10
$\overline{D_9}$ $\overline{LSB}$	Least Significant Bit Complement	ECL	3	62	66	H11
OVF	Overflow Output	ECL	28	37	40	H2
$\overline{OVF}$	Overflow Output Complement	ECL	29	36	39	H1
NC	No Connect	Open	11, 21, 23, 38, 39, 41, 42, 44, 45, 47, 49, 50, 52, 53, 55, 56	9, 10, 12, 13, 15, 16, 18, 20, 21, 23, 24, 26, 27, 42, 44, 54	8, 10, 11, 12, 15, 17, 19, 23, 24, 25, 26, 28, 29, 30, 42, 45, 47, 51, 56, 60	B1, C2, C1, J1, L2, L3, L6, K7, C11, B10, A9, B8, A8, A7, A6, A5, B4, A4, A2

Output Coding Table [1]

V_{IN}	OVF	D_1 MSB ... D_9 LSB
+0.0039V	1	000000000
0.0000V	0	000000000
−0.0039V	0	000000001
•	•	•
•	•	•
•	•	•
−0.9980V	0	011111111
−1.0020V	0	100000000
−1.0059V	0	100000001
•	•	•
•	•	•
•	•	•
−1.9961V	0	111111110
−2.0000V	0	111111111

Note: 1. Voltages are code midpoints.

Figure 1. Timing Diagram

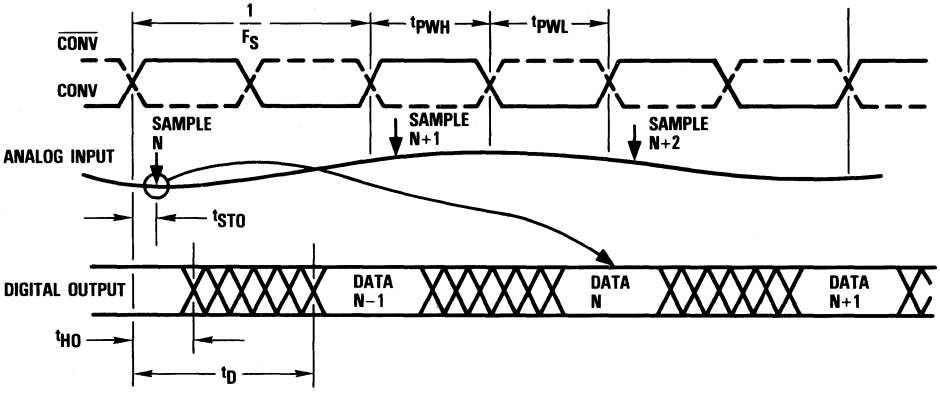
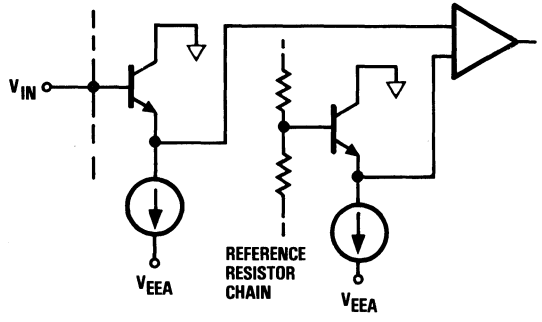
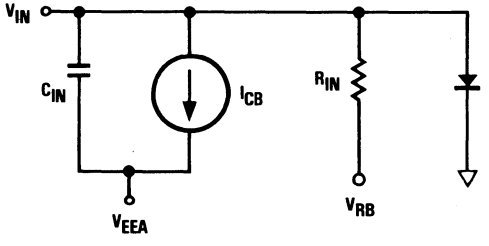


Figure 2. Simplified Analog Input Equivalent Circuits





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

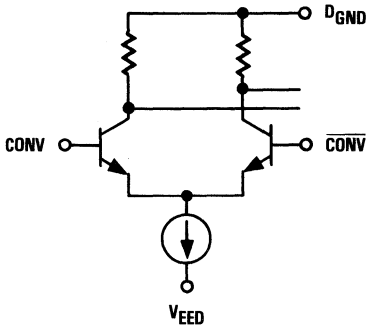


Figure 4. Output Circuits

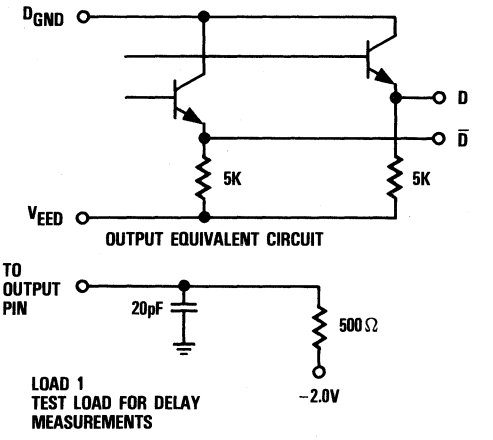
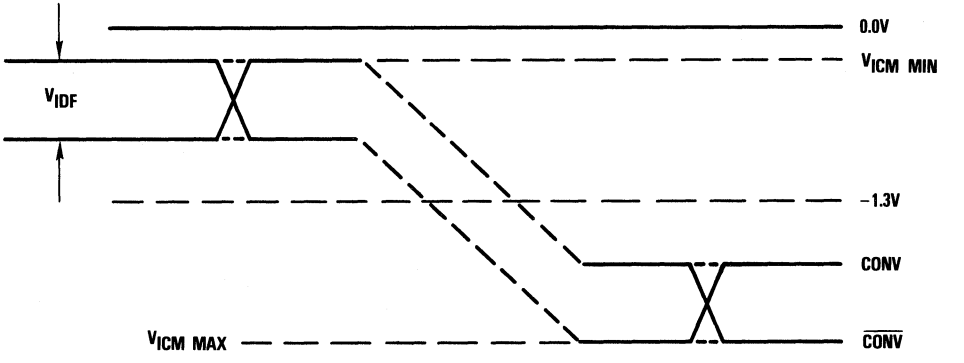


Figure 5. CONVert, CONVert Switching Levels



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND}) ..... +0.5 to −7.0V
V_{EEA} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... +1.0 to −1.0V
V_{EEA} (measured to V_{EED}) ..... +0.5 to −0.5V

Input Voltages [2]

CONV, $\overline{CONV}$ (measured to D_{GND}) ..... +0.5 to V_{EE}
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}
V_{RT} (measured to V_{RB}) ..... +2.5 to −2.5V

Output

Short-circuit duration (single output in HIGH state to ground) ..... Infinite

Temperature

Operating, case ..... −60 to +140°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{EED}	Digital Supply Voltage (measured to D_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	12			12			ns
t_{PWH}	CONV Pulse Width, HIGH	15			15			ns
V_{ICM}	Input Voltage, Common Mode	−0.5		−2.5	−0.5		−2.5	V
V_{IDF}	Input Voltage, Differential	0.3		1.2	0.3		1.2	V
V_{IN}	Input Voltage Range	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	−1.9	−2.0	−2.1	−1.9	−2.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note: 1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{EE}	Supply Current	V_{EED}, V_{EEA} = Max					
		T_A = 0°C to 70°C		−950			mA
		T_A = 70°C		−750			mA
		T_C = −55°C to 125°C				−1090	mA
		T_C = 125°C				−750	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom	10	36	10	36	mA
R_{REF}	Total Reference Resistance		56	200	56	200	Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	16		16		kOhms
C_{IN}	Analog Input Capacitance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		160		160	pF
I_{CB}	Input Constant Bias Current	V_{EEA} = Max, V_{IN} = 0V		500		750	μA
I_I	Input Current, CONV, $\overline{CONV}$	V_{EED} = Max, V_I = −0.7V		150		180	μA
V_{OL}	Output Voltage, Logic LOW [1]	V_{EED} = Nom		−1.6		−1.5	V
V_{OH}	Output Voltage, Logic HIGH [1]	V_{EED} = Nom	−0.95		−1.1		V
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		20		20	pF

Note: 1. Test Load = 500Ω to −2V on each output.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{EED}, V_{EEA} = Min	30		30		Msps
t_{STO}	Sampling Time Offset	V_{EED}, V_{EEA} = Min	−2	6	−2	6	ns
t_D	Output Delay [1]	V_{EED}, V_{EEA} = Min		27		27	ns
t_{HO}	Output Hold Time [1]	V_{EED}, V_{EEA} = Min	3		3		ns

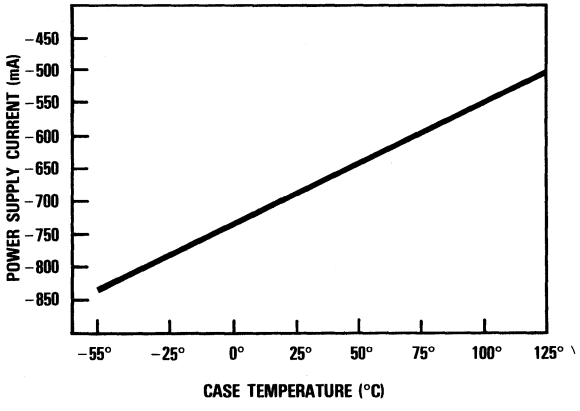
Note: 1. Test Load = 500Ω to −2V on each output, C_{LOAD} = 20pF.

System performance characteristics within specified operating conditions

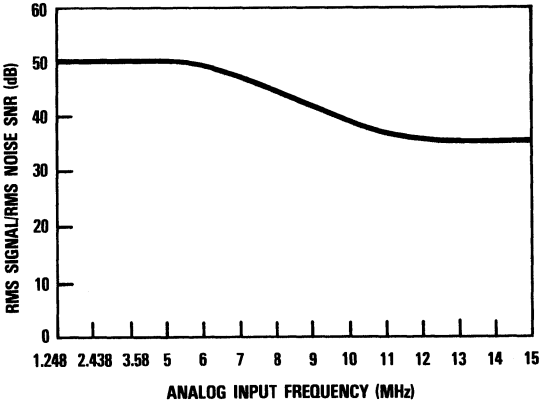
Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB}=Nom		0.15		0.20	%
		V_{RT}, V_{RB}=Nom, V_{RM} Adjusted		0.10		0.10	%
E_{LD}	Linearity Error Differential	V_{RT}, V_{RB}=Nom		0.1		0.1	%
Q	Code Size	V_{RT}, V_{RB}=Nom	15	185	15	185	% Nominal
E_{OTS}	Offset Error, Top	V_{IN}=V_{RT}, R_{TS} Connected		±4		±4	mV
E_{OT}	Offset Error, Top	V_{IN}=V_{RT}		30		30	mV
E_{OBS}	Offset Error, Bottom	V_{IN}=V_{RB}, R_{BS} Connected		±4		±4	mV
E_{OB}	Offset Error, Bottom	V_{IN}=V_{RB}		−30		−30	mV
T_{CO}	Offset Error, Temperature Coefficient			20		20	µV/°C
t_{TR}	Transient Response, Full-Scale			20		20	ns
BW	Bandwidth, Full Power Input	±0.9dB Frequency Response	15		15		MHz
SNR	Signal-to-Noise Ratio	30Msps Conversion Rate, 10MHz Bandwidth					
	Peak Signal/RMS Noise	1.25MHz Input	57		57		dB
		5.0MHz Input	53		53		dB
	RMS Signal/RMS Noise	1.25MHz Input	48		48		dB
		5.0MHz Input	44		44		dB
E_{AP}	Aperture Error			50		50	ps
DP	Differential Phase Error	F_S=4 x NTSC		0.5		0.5	Degree
DG	Differential Gain Error	F_S=4 x NTSC		1.5		1.5	%

Typical Performance Curves

A. Power Supply Current vs. Temperature



B. SNR vs. Analog Input Frequency



Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1049J0C	STD - T_A = 0°C to 70°C	Commercial	64-Pin Ceramic DIP	049J0C
TDC1049J0V	EXT - T_C = -55°C to 125°C	MIL-STD-883	64-Pin Ceramic DIP	1049J0V
5962-8853201XA	EXT - T_C = -55°C to 125°C	Per Standard Mil Drawing	64-Pin Ceramic DIP	5962-8853201XA
TDC1049C1C	STD - T_A = 0°C to 70°C	Commercial	68-Contact Ceramic LCC	1049C1C
TDC1049C1V	EXT - T_C = -55°C to 125°C	MIL-STD-883	68-Contact Ceramic LCC	1049C1V
5962-8853201ZA	EXT - T_C = -55°C to 125°C	Per Standard Mil Drawing	68-Contact Ceramic LCC	5962-8853201ZA
TDC1049G8C	STD - T_A = 0°C to 70°C	Commercial	68-Pin Ceramic PGA	1049G8C
TDC1049G8V	EXT - T_C = -55°C to 125°C	MIL-STD-883	68-Pin Ceramic PGA	1049G8V

Standard Military Drawing	Nearest Equivalent Raytheon Product No.	Package
5962-8853201XA	TDC1049J0V	64-Pin Ceramic DIP
5962-8853201YA	TDC1049J3V	64-Pin Ceramic DIP
5962-8853201ZA	TDC1049C1V	68-Contact Chip Carrier
5962-8853201UA	TDC1049L1V	68-Contact Chip Carrier

40G03657 Rev E 8/93

TDC1058
Monolithic Video A/D Converter
8-Bit, 20 Msps, Low Power

Description

The TDC1058 is a flash analog-to-digital converter capable of converting a video-speed signal into a stream of 8-bit digital words at 20 Msps (MegaSamples Per Second). Since the TDC1058 is a flash converter, a sample-and-hold circuit is not required.

The TDC1058 consists of 255 clocked latching comparators, combining logic, and an output register. A single convert clock controls the conversion operation. The unit can be configured to give either true or inverted outputs in binary or offset two's complement coding. All digital I/Os are TTL compatible.

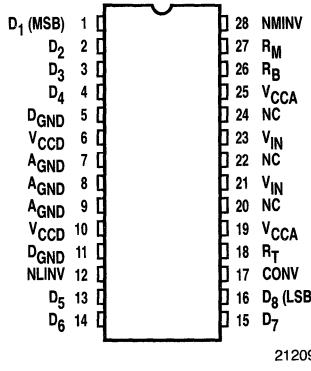
Features

- 8-bit resolution
- DC to 20 Msps conversion rate
- 7 MHz full-power bandwidth
- 60 MHz small signal -3 dB bandwidth
- 1/2 LSB linearity
- 600 mW power dissipation
- +5V single supply operation
- Lowest cost
- Pin compatible with CXA1096P, ADC-304
- Sample-and-hold circuit not required
- Analog input range +3V to +5V
- Differential phase 0.5°
- Differential gain 1%
- Selectable data format
- Available in plastic DIP, CERDIP, and PLCC

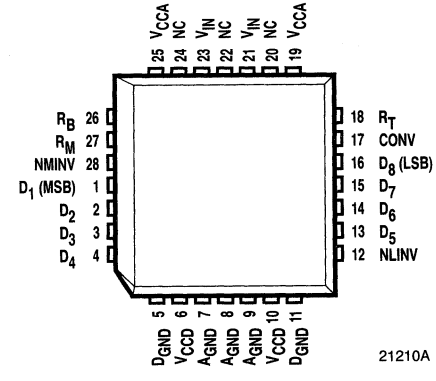
Applications

- Digital television
- PC-based data acquisition
- Video digitizing
- Medical imaging
- High energy physics
- Low cost, low power, high-speed data conversion

Pin Assignments

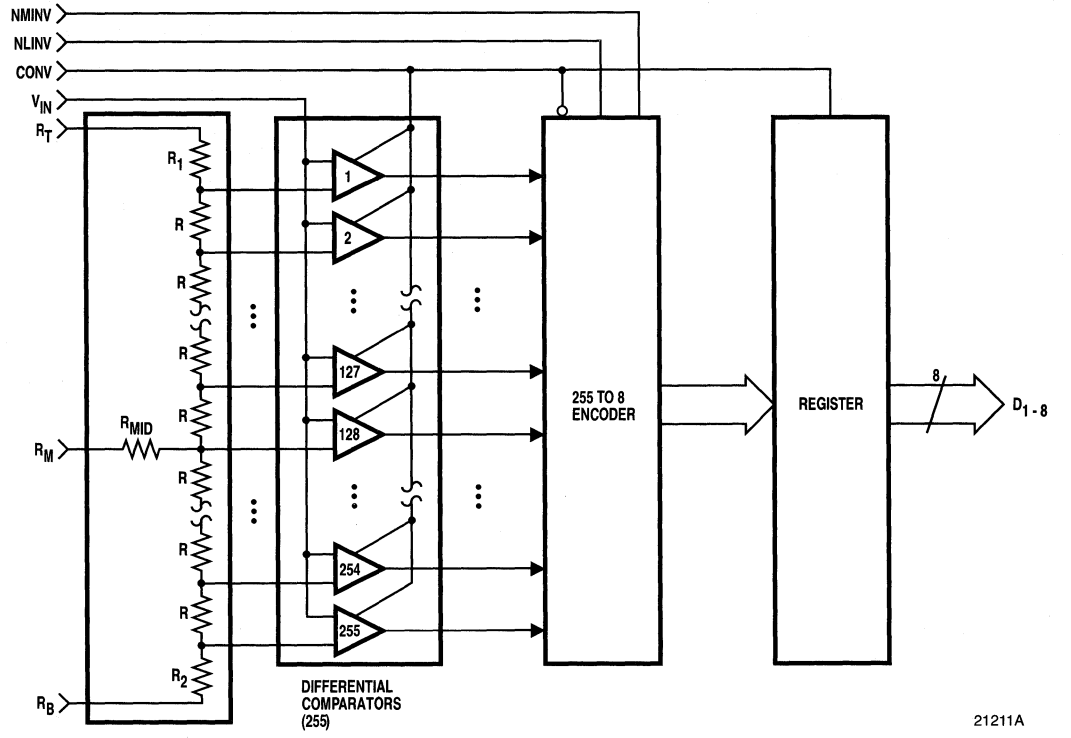


28 Pin CERDIP – B6 Package
28 Pin Plastic DIP – N6 Package



28 Leaded Plastic Chip Carrier – R3 Package

Functional Block Diagram



Functional Description

General Information

The TDC1058 has three functional sections: a comparator array, encoding logic, and output registers. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (or thermometer code, since all the comparators whose reference is more negative than the input signal will be on, and all those whose reference is more positive will be off). The encoding logic converts the N-of-255 code into the user's choice of coding. The output register holds the output constant between updates.

Power

The TDC1058 operates from a single supply voltage: +5.0V. All power and ground pins must be connected.

Reference

The TDC1058 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. Nominally, V_{RB} is set to 3V and V_{RT} is set to 5V. However, the specifications of the TDC1058 are guaranteed as long as the following three reference operating conditions are met: 1.) the voltage applied across the reference resistor

Reference (cont.)

chain (V_{RT}-V_{RB}) is within the range of 1.8 to 2.2V, 2.) $V_{RT} \leq (V_{CCA}+0.1V)$ and 3.) $V_{RB} \geq 2.65V$. Therefore, if the supply voltage is expected to drop below 4.9V, the reference voltages should be lowered accordingly. For instance, if the system design allows the supply voltage to drop to the minimum recommended value of 4.75V, V_{RT} should be set to 4.65V and V_{RB} should be set to 2.65V. These reference voltages will allow the TDC1058 to give fully guaranteed performance over the full supply voltage range. See the ***Operating Conditions Table*** for further information.

Linearity is guaranteed with no adjustment; however, a midpoint tap, R_M, allows for the optional trimming of converter integral linearity as well as the creation of a nonlinear transfer function. This is explained in the ***Application Note TP-19 "Non-Linear A/D Conversion."*** The circuit shown in ***Figure 7*** will provide approximately a 1/2 LSB adjustment of the linearity at midscale. The characteristic impedance seen at this node is approximately 220 Ohms and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity and any noise introduced at this point will degrade the overall SNR. Due to the slight variation in the reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor (0.01 to 0.1μF) to ground is recommended. If the reference inputs are exercised dynamically (as in an automatic gain control circuit) a low-impedance reference source is required. The reference voltages may be varied dynamically at up to 5MHz; however, device performance is specified with fixed reference voltages as defined in the ***Operating Conditions Table***.

Analog Input

For precise quantization, the TDC1058 uses latching comparators. The source impedance of the driving circuit must be less than 25 Ohms, for optimum overall system performance. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number from 0 to 255. When a signal outside the recommended input voltage range (V_{RB} to V_{RT}) is applied, the output will remain at either full-scale value. The input signal will not damage the TDC1058 if it remains within the range specified in the ***Absolute Maximum Ratings Table***. Both analog input pins are connected together internally and therefore either one or both may be used.

Convert

The TDC1058 requires an external convert (CONV) signal. Because the TDC1058 is a flash converter it does not require a track-and-hold circuit. A sample is taken (the outputs of the comparators are latched) within t_{STO} (Sampling Time Offset) after a rising edge on the CONV pin. The result is encoded on the falling edge, and then transferred to the output registers on the next rising edge. The output becomes valid t_D (Output Delay Time) after the rising edge of CONVert and remains valid for at least t_{HO} (Output Hold Time) after the rising edge of CONVert. Therefore, the value of sample N becomes valid t_D after the rising edge of clock N+1 and remains valid until t_{HO} after the rising edge of clock N+2. (See ***Figure 1, Timing Diagram***.)

Output Format Control

Two output format control pins, NMINV and NLINV, are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW, as signified by the N prefix in the signal name. They may be tied to V_{CC} (through a 4.7 kOhm resistor) for a logic HIGH or D_{GND} for a logic LOW.

Outputs

The outputs of the TDC1058 are TTL compatible and capable of driving four low-power Schottky TTL (54/74 LS) loads or the equivalent. The outputs hold the previous data for a minimum of t_{HO} after the rising edge of the CONVert signal.

Not Connected

There are several pins that have no internal connection to the chip. They should be left open.

Package Interconnections

Signal Type	Signal Name	Function	Value	B6, N6, R3 Package Pins
Power	V_{CCD}	Digital Supply Voltage	+5.0V	6, 10
	V_{CCA}	Analog Supply Voltage	+5.0V	19, 25
	A_{GND}	Analog Ground	0.0V	7, 8, 9
	D_{GND}	Digital Ground	0.0V	5, 11
Reference	R_T	Reference Resistor (Top)	5.0V	18
	R_M	Reference Resistor (Middle)	4.0V	27
	R_B	Reference Resistor (Bottom)	3.0V	26
Analog Input	V_{IN}	Analog Signal Input	See Text	21, 23
Convert	CONV	Convert	TTL	17
Format Control	NMINV	Not Most Significant Bit Invert	TTL	28
	NLINV	Not Least Significant Bit Invert	TTL	12
Data Output	D_1	Most Significant Bit Output	TTL	1
	D_2		TTL	2
	D_3		TTL	3
	D_4		TTL	4
	D_5		TTL	13
	D_6		TTL	14
	D_7		TTL	15
	D_8	Least Significant Bit Output	TTL	16
Not Connected	NC	Not Connected	Open	20, 22, 24

Figure 1. Timing Diagram

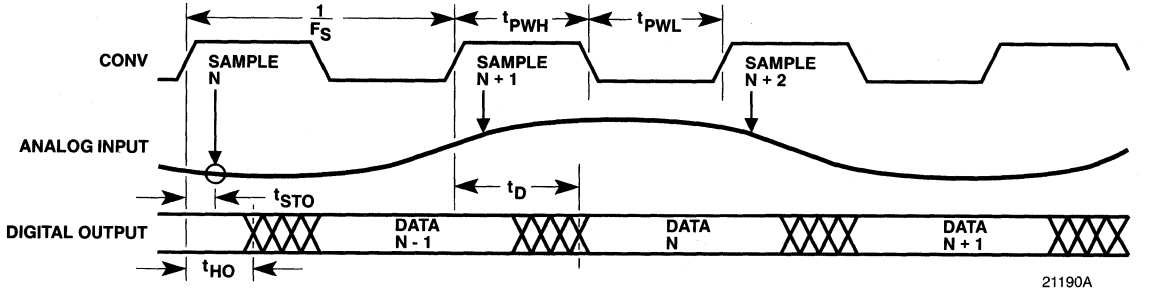
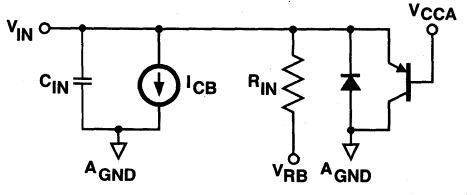


Figure 2. Simplified Analog Input Equivalent Circuit



C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

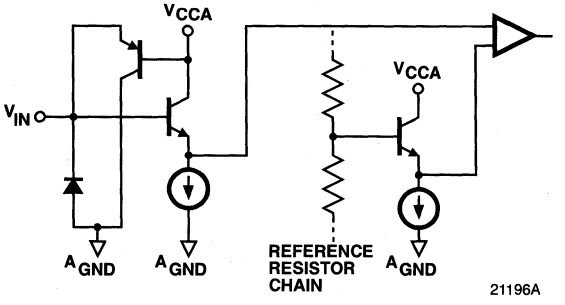


Figure 3. Convert Input Equivalent Circuit

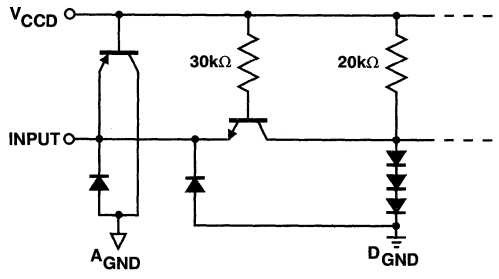
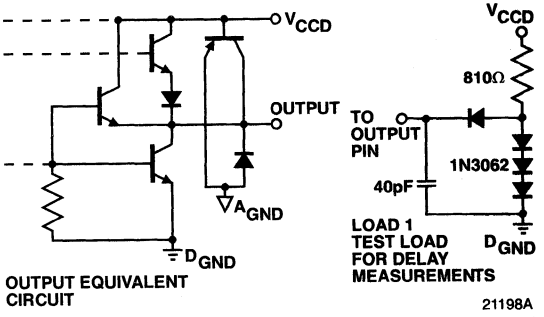


Figure 4. Output Circuit



Output Coding Table

Input Voltage	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = HIGH NLINV = HIGH	NMINV = LOW NLINV = LOW	NMINV = LOW NLINV = HIGH	NMINV = HIGH NLINV = LOW
5.0000V	0000 0000	1111 1111	1000 0000	0111 1111
4.9922V	0000 0001	11111110	1000 0001	0111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
4.0078V	0111 1111	1000 0000	1111 1111	0000 0000
4.0000V	1000 0000	0111 1111	0000 0000	1111 1111
3.9922V	1000 0001	0111 1110	0000 0001	1111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3.0156V	1111 1110	0000 0001	0111 1110	1000 0001
3.0078V	1111 1111	0000 0000	0111 1111	1000 0000

Notes:
1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V through a 4.7 kOhm resistor for a logic HIGH or tied to ground for a logic LOW.
2. Voltages are code midpoints.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Power Supply Voltages

V_{CCA} (measured to A_{GND})	-0.5 to +7.0V
V_{CCD} (measured to D_{GND})	-0.5 to +7.0V
A_{GND} (measured to D_{GND})	-0.5 to +0.5V

Input Voltages

CONV, NLINV, NMINV	-0.5 to V_{CC}+0.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	-0.5 to +5.5V
V_{RT} (measured to V_{RB})	-2.2 to +2.2V

Input Currents

CONV, NLINV, NMINV	-50 to +50 mA
V_{IN}, V_{RT}, V_{RB}	-100 to +100 mA

Digital Outputs

Applied voltage[2]	-0.5 to V_{CC}+0.5V
Applied current[3,4]	-50 to +50 mA
Short-circuit duration (single output in HIGH state to GND)	1 second.

Temperature

Operating, ambient (all packages except N6 and R3)	-55 to +125°C
(N6 and R3 packages only)	-20 to 90°C
junction (all packages)	+175°C
Lead, soldering, all packages (10 seconds)	+300°C
Storage	-65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CCA}	Analog Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{CCD}	Digital Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	-0.1	0.0	0	+0.1	0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	19			18			ns
t_{PWH}	CONV Pulse Width, HIGH	27			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-400			-400	µA
V_{RT}	Most Positive Reference Input [1]		5.0	V_{CCA} = 0.1	4.9	5.0	5.1	V
V_{RB}	Most Negative Reference Input [1]	2.65	3.0		2.9	3.0	3.1	V
V_{RT}-V_{RB}	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
TA	Case Temperature				-55		125	°C

Note: 1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Thermal characteristics (approximate)

Parameter		Package	Typical	Units
Θ_{ja}	Thermal Resistance, Junction to Ambient	N6	45	°C/W
		R3	65	°C/W
		B6	50	°C/W
Θ_{jc}	Thermal Resistance, Junction to Case	N6	17	°C/W
		R3	14	°C/W
		B6	TBD	°C/W

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
$I_{CCA} + I_{CCD}$	Total Supply Current	V_{CC}=Max[1]		160		160	mA
I_{REF}	Reference Current	V_{RT}, V_{RB}=Nom		30		50	mA
R_{REF}	Total Reference Resistance		67		40		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB}=Nom, V_{IN}=V_{RB}	80		40		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB}=Nom, V_{IN}=V_{RB}		50		50	pF
I_{CB}	Input Constant Bias Current	V_{CCA}=Max		250		500	µA
I_{IL}	Input Current, Logic LOW	V_{CC}=Max, V_I=0.4V		-0.6		-0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC}=Max, V_I=2.4V	-200	50	-400	50	µA
I_I	Input Current, Max Input Voltage	VCC=Min, I_{OL}=Max		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC}=Min, I_{OL}=Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC}=Min, I_{OH}=Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC}=Max, Output HIGH, one pin to ground, one second duration max		-40		-40	mA
C_I	Digital Input Capacitance	T_A=25°C, F=1 MHz		15		15	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate		20		20		Msps
t_{STO}	Sampling Time Offset		-2	10	-2	10	ns
t_D	Output Delay	V_{CC}=Min, Load 1, Figure 4		35		35	ns
t_{HO}	Output Hold Time	V_{CC}=Min, Load 1, Figure 4	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB}=Nom		0.2		±0.2	%
E_{LD}	Linearity Error Differential			0.2		±0.2	%
C_S	Code Size		25	175	25	175	% Nom
E_{OT}	Offset Error, Top	V_{IN}=V_{RT}	-10	+10		+15	mV
E_{OB}	Offset Error, Bottom	V_{IN}=V_{RB}		-15		-15	mV
T_{CO}	Offset Error, Temperature Coefficient		-20	±20		±20	µV/°C
BW	Bandwidth, Full-Scale Input	No Spurious or Missing Codes	7		7		Mhz
BW_{SS}	-3 dB Bandwidth, Small Signal	-20 dBFS Input	60		60		MHz
t_{TR}	Transient Response, Full Scale		70		70		ns
SNR	Signal-to-Noise Ratio	10 MHz Bandwidth, 20 Msps Conversion Rate					
	Peak Signal/RMS Noise	1.248 MHz Input	54		53		dB
		2.438 MHz Input	53		52		dB
	RMS Signal/RMS Noise	1.248 MHz Input	45		44		dB
		2.438 MHz Input	44		43		dB
E_{AP}	Aperture Error			60		60	ps
DG	Differential Gain Error	F_S=4 x NTSC		2.0		2.0	%

Figure 5. Typical Interface Circuit

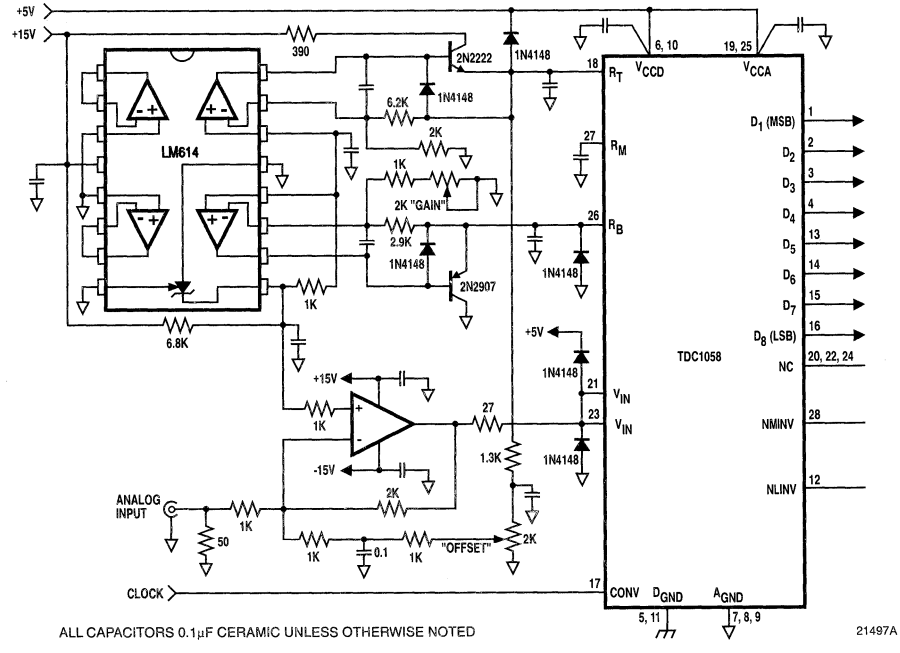
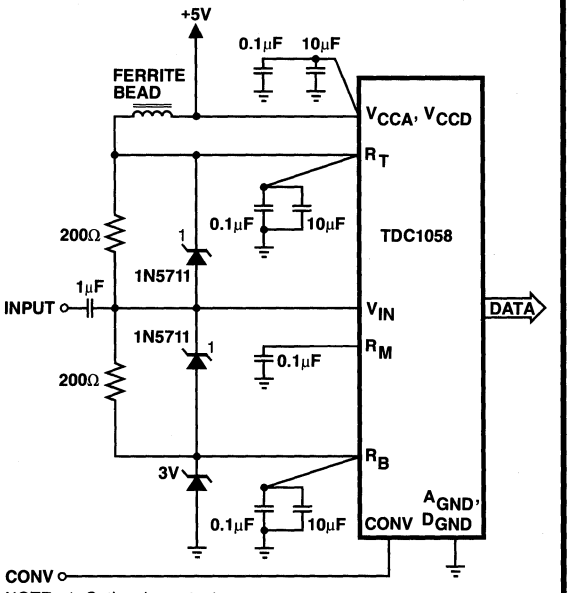
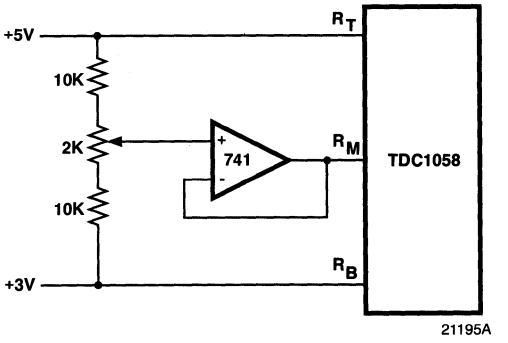


Figure 6. Inexpensive Interface Circuit



NOTE: 1. Optional, see text

Figure 7. Optional Midscale Linearity Adjust



Typical Interface Circuit

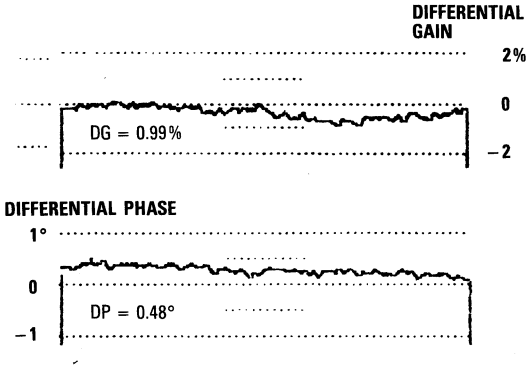
The *Typical Interface Circuit (Figure 5)* shows an example of a high-performance application circuit for the TDC1058. The wideband analog input amplifier drives the A/D converter directly. Bipolar inputs to the amplifier can be accommodated by adjusting the offset control. TRW's TDC4614 provides a stable reference for both the offset and gain control. All V_{IN} pins are con-nected close to the device package and the input ampli-fier's feedback loop should be closed at that point. The buffer has an inverting gain of two, increasing a 1Vp-p video input signal to the recommended 2Vp-p input for the TDC1058. Proper decoupling is recommended for all systems.

The bottom reference voltage (V_{RB}) is supplied by an inverting amplifier or the TDC4614, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain.

The *Inexpensive Interface Circuit* shown in *Figure 6* offers considerable parts reduction for cost-sensitive applications where DC response is not required and loss of some power supply rejection is tolerable. The 200 Ohm resistors bias the input to +4V and provide the current to the zener diode to provide the reference bottom voltage. The 1μF capacitor decouples the input signal from the DC voltage present at the input of the TDC1058. The 10μF and 0.1μF capacitors, as well as the ferrite bead, provide power supply decoupling. The 1N5711 Schottky diodes are for protection against overvoltages at the input and are not required if these precautions are taken elsewhere in the circuit.

Typical Performance Curves

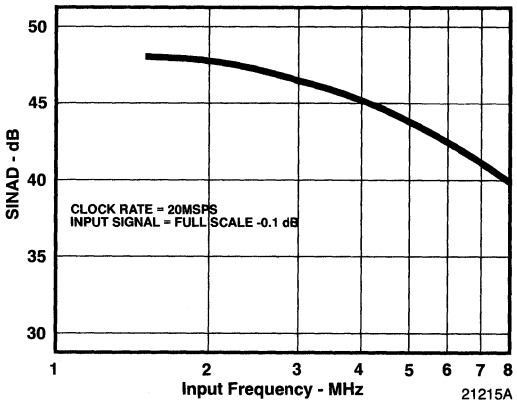
A. Typical Differential Phase and Gain



Convert Frequency = 14.3181800MHz
Analog Input = 3.57954550MHz

21214A

B. Typical SINAD (SNR + Distortion) vs. Input Frequency



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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1058B6C	STD - T_A = 0°C to 70°C	Commercial	28-Pin CERDIP	1058B6C
TDC1058B6V	EXT - T_C = -55°C to 125°C	MIL-STD-883	28-Pin CERDIP	1058B6V
TDC1058N6C	STD - T_A = 0°C to 70°C	Commercial	28-Pin Plastic DIP	1058N6C
TDC1058R3C	STD - T_A = 0°C to 70°C	Commercial	28-Lead Plastic J-Leaded Chip Carrier	1058R3C

40G05738 Rev E 8/93

TDC1147
Monolithic Video A/D Converter
7-Bit, 15 Msps

Description

The TDC1147 is a 7-bit "flash" analog-to-digital converter which has no pipeline delay between sampling and valid data. The output data register normally found on flash A/D converters has been bypassed, allowing data to transfer directly to output drivers from the encoding logic section of the circuit. The converter requires only one clock pulse to perform the complete conversion operation. The conversion time is guaranteed to be less than 60 nanoseconds.

The TDC1147 is function and pin-compatible with Raytheon Semiconductor La Jolla's TDC1047 7-bit flash A/D converter which has an output data register. The TDC1147 will operate accurately at sampling rates up to 15 Msps and has an analog bandwidth of 7 MHz. Linearity errors are guaranteed to be less than 0.4% over the operating temperature range.

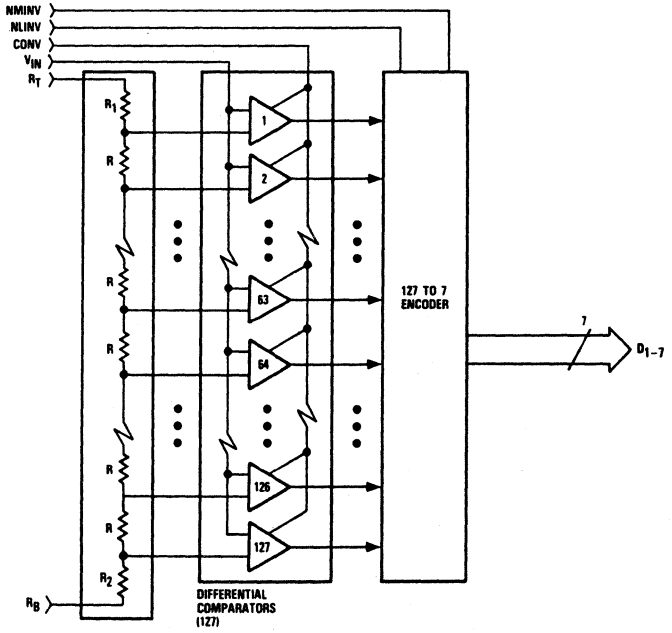
Features

- 20 Msps conversion rate
- No digital pipeline delay
- 7-bit resolution
- 1/2 LSB linearity
- Sample-and-hold circuit not required
- TTL compatible
- Selectable output format
- Available in 24 pin CERDIP

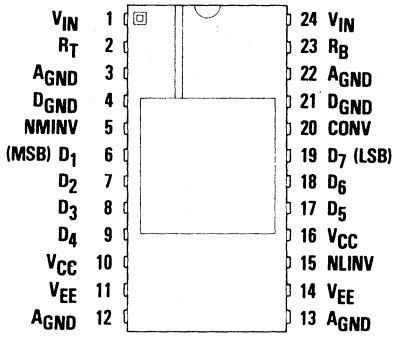
Applications

- Low-cost video digitizing
- Medical imaging
- Data acquisition
- High resolution A/D converters
- Telecommunications systems
- Radar data conversion

Functional Block Diagram



Pin Assignments



24 Pin CERDIP – B7 Package

Functional Description

General Information

The TDC1147 has two functional sections: a comparator array and encoding logic. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV.

Power

The TDC1147 operates from two supply voltages, +5.0V and −5.2V. The return path for I_{CC} (the current drawn from the +5.0V supply) is D_{GND}. The return path for I_{EE} (the current drawn from the −5.2V supply) is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1147 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.8V and 1.2V. The nominal voltages are V_{RT}=0.00V and V_{RB}=−1.00V. These voltages may be varied dynamically up to 7MHz. Due to slight variations in the reference current with clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically as in an Automatic Gain Control (AGC) circuit, a low-impedance reference source is recommended.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***.

Convert

The TDC1147 uses a CONVert (CONV) input signal to initiate the A/D conversion process. Unlike other flash A/D converters which have a one-clock-cycle pipeline delay between sampling and output data, the TDC1147 requires only a single pulse to perform the entire conversion operation. The analog input is sampled (comparators are latched) within the maximum Sampling Time Offset (t_{STO}, see ***Figure 1***). Data from that sample becomes valid after a maximum Output Delay Time (t_D) while data from the previous sample is held at the outputs for a minimum Output Hold Time (t_{HO}). This allows data from the TDC1147 to be acquired by an external register or other circuitry. Note that there are minimum time requirements for the HIGH and LOW portions (t_{PWH}, t_{PWL}) of the CONV waveform and all output timing specifications are measured with respect to the rising edge of CONV.

Analog Input

The TDC1147 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, both V_{IN} pins must be used and the source impedance of the driving circuit must be less than 30 Ohms. The input signal will not damage the TDC1147 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1147 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. New data becomes valid after a maximum time (t_D) after the rising edge of the CONV signal. The use of 2.2 kOhm pull-up resistors is recommended.

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	10, 16
	V_{EE}	Negative Supply Voltage	−5.2V	11, 14
	D_{GND}	Digital Ground	0.0V	4, 21
	A_{GND}	Analog Ground	0.0V	3, 12, 13, 22
Reference	R_T	Reference Resistor (Top)	0.00V	2
	R_B	Reference Resistor (Bottom)	−1.00V	23
Controls	NMINV	Not Most Significant Bit INVert	TTL	5
	NLINV	Not Least Significant Bit INVert	TTL	15
Convert	CONV	Convert	TTL	20
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	1, 24
Outputs	D_1	MSB Output	TTL	6
	D_2		TTL	7
	D_3		TTL	8
	D_4		TTL	9
	D_5		TTL	17
	D_6		TTL	18
	D_7	LSB Output	TTL	19

Figure 1. Timing Diagram

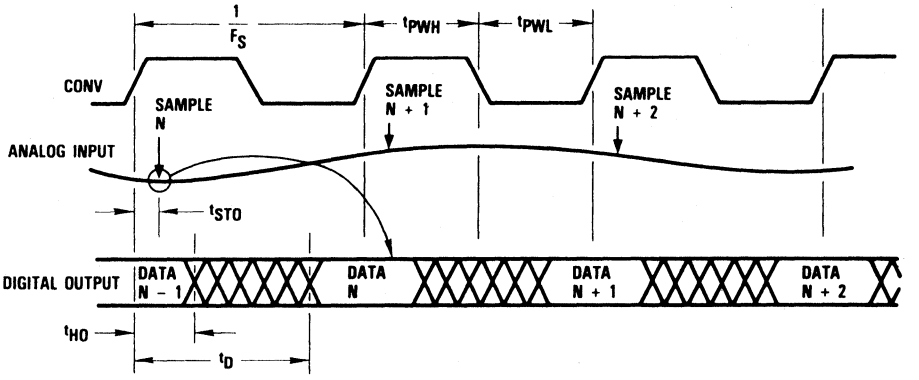


Figure 2. Simplified Analog Input Equivalent Circuit

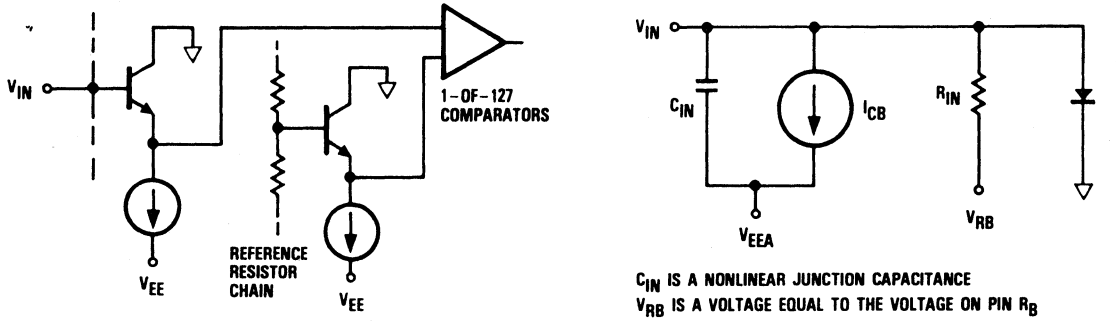


Figure 3. Digital Input Equivalent Circuit

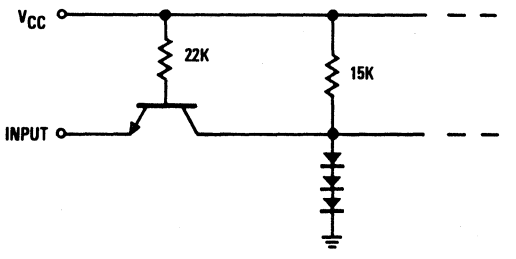
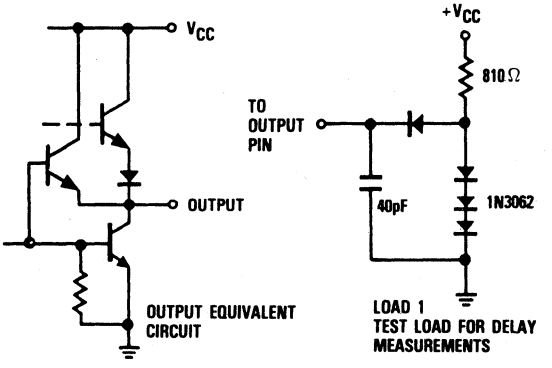


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V [2]
Applied current, externally forced	−1.0 to 6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter	Test Conditions	Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	22			22			ns
t_{PWH}	CONV Pulse Width, HIGH	18			18			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4			−0.4	mA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−1.0	−1.1	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note: 1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, static [1]		25		30	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, static [1]					
		T_A = 0°C to 70°C		-170			mA
		T_A = 70°C		-135			mA
		T_C = -55°C to 125°C				-220	mA
		T_C = 125°C				-130	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		35		50	mA
R_{REF}	Total Reference Resistance		34		20		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	100		40		kOhms
C_{IN}	Input Capacitance			60		60	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		160		300	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V CONV		-0.4		-0.6	mA
		$\overline{\text{NMINV, NLINV}}$		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = Max, one pin to ground, one second duration.		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = Min, V_{EE} = Min	15		15		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = Min, V_{EE} = Min		7		10	ns
t_D	Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		60		70	ns
t_{HO}	Output Hold Time	V_{CC} = Max, V_{EE} = Max, Load 1	15		15		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error, Integral Independent	V_{RT}, V_{RB} = Nom		0.4		0.4	%
E_{LD}	Linearity Error, Differential			0.4		0.4	%
CS	Code Size	V_{RT}, V_{RB} = Nom	30	170	30	170	% Nominal
V_{OT}	Offset Voltage, Top	V_{IN} = V_{RT}		+50		+50	mV
V_{OB}	Offset Voltage, Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		7		7		MHz
t_{TR}	Transient Response, Full Scale			10		10	ns
SNR	Signal-to-Noise Ratio	7MHz Bandwidth,					
		20MSPS Conversion Rate					
	Peak Signal/RMS Noise	1MHz Input	45		46		dB
		7MHz Input	43		44		dB
	RMS Signal/RMS Noise	1MHz Input	36		37		dB
		7MHz Input	34		35		dB
E_{AP}	Aperture Error			50		50	ps
DP	Differential Phase Error[1]	F_S = 4 x NTSC		1.5		1.5	Degree
DG	Differential Gain Error[1]	F_S = 4 x NTSC		2.5		2.5	%

Note:
1. In excess of quantization.

Output Coding

Range	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
−1.00V FS	NMINV = 1	0	0	1
	NLINV = 1	0	1	0
0.0000V	0000000	1111111	1000000	0111111
−0.0078V	0000001	1111110	1000001	0111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.4960V	0111111	1000000	1111111	0000000
−0.5039V	1000000	0111111	0000000	1111111
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9921V	1111110	0000001	0111110	1000001
−1.0000V	1111111	0000000	0111111	1000000

Note:
1. Voltages are code midpoints.

Calibration

To calibrate the TDC1147, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages. Assuming a 0V to −1V input range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.996V (1/2 LSB from −1V) and adjust V_{RB} for toggling between codes 126 and 127.

The degree of required adjustment is indicated by the offset voltages, V_{OT} and V_{OB}. Offset voltages are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the *Functional Block Diagram*. Calibration will cancel all offset voltages, eliminating offset and gain errors.

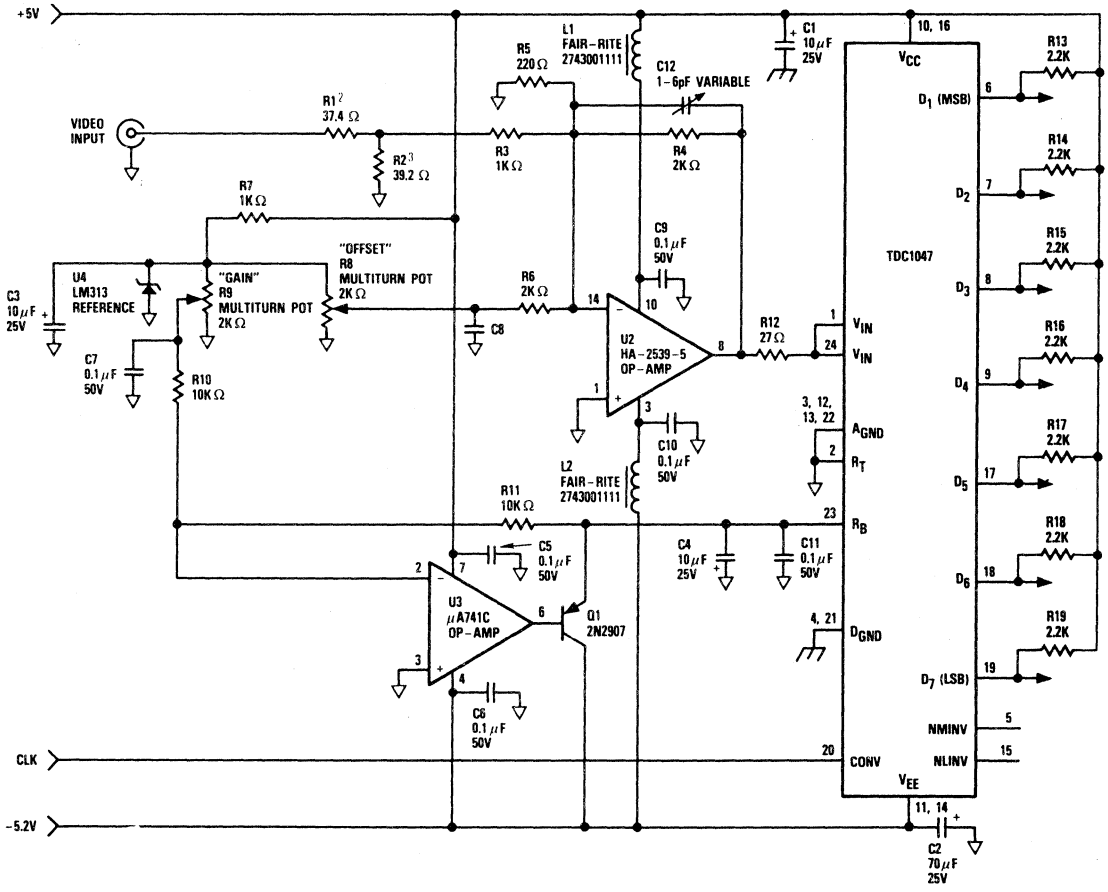
The above method for calibration requires that both ends of the resistor chain, R_T and R_B, are driven by variable voltage sources. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with an input amplifier offset control. The offset error at the bottom of the resistor chain causes a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path.

Typical Interface Circuit

Figure 5 shows an example of a typical interface circuit for the TDC1147. The analog input amplifier is a bipolar wideband operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. A zener diode provides a stable reference for both the offset and gain control. The amplifier has a gain of −1 providing the recommended 1Vp-p input for the A/D converter. Proper decoupling is recommended for all supplies, although the degree of decoupling shown may not be needed. A variable capacitor permits either step response or frequency response optimization. This may be replaced with a fixed capacitor, whose value depends upon the circuit board layout and desired optimization.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier, followed with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, V_{OB}, as discussed in the ***Calibration*** section.

Figure 5. Typical Interface Circuit



Notes:

1. Unless otherwise specified, all resistors are 1/4W, 2%.

2. $R1 = Z_{IN} - \left(\frac{1000\ R2}{1000 + R2}\right)$

3. $R2 = \frac{1}{\left(\frac{2V_{Range}}{V_{REF}\ Z_{IN}}\right) - 0.001}$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1147B7C	STD–T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1147B7C
TDC1147B7V	EXT–T_C = –55°C to 125°C	MIL-STD-883	24 Pin CERDIP	1147B7V

40G01900 Rev F 8/93

TMC1173
2.7 to 3.6 Volt 8-Bit 10 Msps A/D Converter

Description

The TMC1173 analog-to-digital (A/D) converter employs a two-step architecture with integral track/hold. The device converts analog signals into 8-bit digital words at rates up to 10 Msps (Megasamples per second). The architecture and CMOS technology reduce typical power dissipation to less than 90 mW.

The TMC1173 operates from a single power supply as low as 2.7 Volts and has internal voltage reference resistors which allow self-bias operation. The input capacitance is very low, simplifying the design of, or eliminating, the need for video driving amplifiers. All digital inputs and three-state outputs are 3V TTL-compatible.

The TMC1173 is available in 24-pin plastic DIP, 24-Lead plastic SOIC, and 28-lead J-lead PLCC packages. Performance specifications are guaranteed from 0 to 70°C.

Features

- 8-bit resolution
- 5 and 10 Msps conversion rate
- Integral track/hold
- Differential linearity error <±0.5 LSB
- Single +2.7 to +3.6 Volt Power Supply
- <90 mW power dissipation at 3.6 volts
- Differential phase <0.5°
- Differential gain <1%
- Three-state 3V TTL-compatible outputs
- Very low cost

Applications

- Battery operated digital video
- Hand-held digital oscilloscopes
- Low cost, low power data conversion
- Portable image scanners
- Laptop / Notebook computer video boards
- Multimedia

Related Products

- TMC1175 20, 30, and 40 Msps 8-Bit Video A/D Converter
- TMC22070 Genlocking Video Digitizer
- TDC3310 10-Bit Video D/A Converter
- TMC22090/TMC22190 Digital Video Encoder
- TMC2242/TMC2243/TMC2246 Video Filter
- TMC2302 Image Manipulation Sequencer

Figure 1. Block Diagram

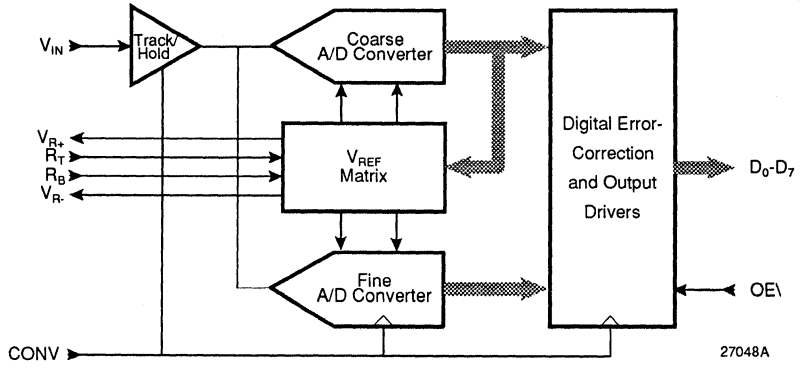
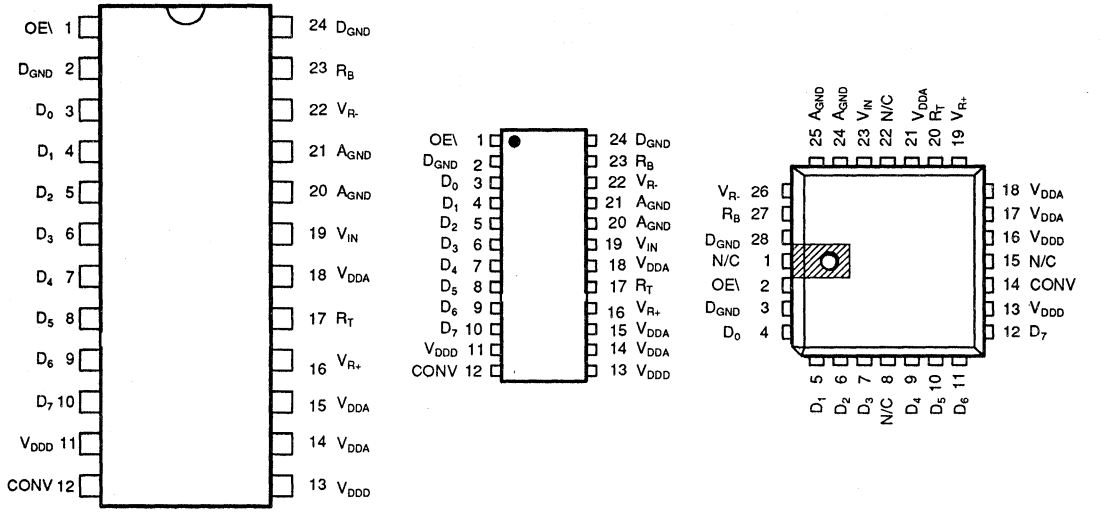


Figure 2. Pin Assignments and Packages



N2 Package
24-pin Plastic DIP

M7 Package
24-Lead SOIC

R3 Package
28-lead J-lead PLCC

27049A

General Description

The TMC1173 is an 8-bit A/D converter which uses a two-step architecture to perform analog-to-digital conversion at rates up to 10 Msps. The input signal is held in an integral track/hold stage during the conversion process. Pipelined operation is achieved with one input sample taken and one output word provided for each convert cycle. The first step in the conversion process is a coarse 4-bit conversion. The coarse 4-bit result determines the range of the subsequent fine 4-bit A/D conversion step. To eliminate spurious codes, the fine 4-bit A/D converter output is gray-coded and converted to binary before combining with the coarse result to form the complete 8-bit result.

The TMC1173 is characterized and specified for use in "3 Volt" applications where the power supply voltage can be as low as 2.7 Volts.

Analog Input and Voltage References

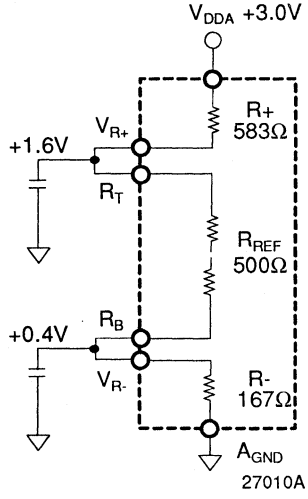
The TMC1173 converts analog signals in the range $R_T \leq V_{IN} \leq R_B$ into digital data. The A/D converter input range is very flexible and extends from the +3 Volt power supply to ground. Normally, external voltage reference sources are connected to the R_T and R_B pins or R_B is grounded.

Two reference pull-up and pull-down resistors connected to V_{R+} and V_{R-} are provided for operation without external voltage reference circuitry. These voltages applied to R_T and R_B may be generated externally, or are self-generated by connecting V_{R+} to R_T and V_{R-} to R_B. In the latter case the power supply voltage is divided by on-chip resistors to bias the R_T and R_B points.

The self-bias reference voltages are useful in applications where overall circuit cost is important and absolute accuracy and stability of the A/D converter gain is not critical.

The V_{IN} input range is from R_B to R_T. The device will not be damaged by signals within the range A_{GND} to V_{DD}.

Figure 3. Reference Resistors



Digital Inputs and Outputs

The sampling of the applied input signal takes place on the falling edge of the CONV signal. The output word is available after the rising edge of CONV, delayed by 2 1/2 CONV cycles. The output remains valid for t_{HO} (Output Hold Time) and new data becomes valid t_D (Output Delay Time) after the rising edge of CONV.

The outputs of the TMC1173 are 3V TTL-compatible and are capable of driving four low-power Schottky TTL (54/74LS) loads. An output enable control, OE\, places the outputs in a high-impedance state when HIGH. The outputs are enabled when OE\ is LOW.

Power and Ground

The TMC1173 operates from a single +2.7 to +3.6 Volt power supply. For optimum performance, it is recommended that A_{GND} and D_{GND} pins of the TMC1173 be connected to the system analog ground plane.

Table 1. Output Coding Table

Input Voltage	Output Code MSB LSB
$>R_T$	11111111
R_T	11111111
R_T - 1 LSB	11111110
•	•
•	•
$(R_T + R_B)/2$ + 1 LSB	10000000
$(R_T + R_B)/2$	01111111
•	•
•	•
R_B + 1 LSB	00000001
R_B	00000000
$<R_B$	00000000

Note: 1 LSB = $(R_T - R_B)/255$

Pin Functions

V_{IN}	The input voltage conversion range extends from the voltage applied to the $R_T$and R_B pins.
R_T, R_B	The top and bottom inputs to the reference resistor ladder. DC voltages applied to R_T and R_B define the V_{IN} conversion range.
V_{R+},V_{R-}	Internal pull-up and pull-down reference resistors used in self-bias operation.
CONV	A/D converter clock input. V_{IN} is sampled on the falling edge of CONV.

OE\ Output Enable. When LOW, D_0-D_7 are enabled. When HIGH, D_0-D_7 are in a high-impedance state.

D_0-D_7 Eight-bit 3V TTL-compatible digital outputs. Valid data is output on the rising edge of CONV.

V_{DDA},V_{DDD} +3 Volt power inputs. These should come from the same power source and be decoupled to A_{GND}.

A_{GND},D_{GND} Ground inputs should be connected to the system analog ground plane.

Table 2. Package Interconnections

Signal Type	Name	Function	Value	N2, M7 Pin	R3, C3 Pin
Inputs	V_{IN}	Analog Input	R_B-R_T	19	23
	R_T	Reference Voltage Top Input	2.6V	17	20
	R_B	Reference Voltage Bottom Input	0.6V	23	27
	V_{R+}	Reference Voltage Top Source	2.6V	16	19
	V_{R-}	Reference Voltage Bottom Source	0.6V	22	26
	OE\	Output enable	TTL	1	2
	CONV	Convert (Clock) input	TTL	12	14
Outputs	D_0	Least Significant Bit	TTL	3	4
	D_1		TTL	4	5
	D_2		TTL	5	6
	D_3		TTL	6	7
	D_4		TTL	7	9
	D_5		TTL	8	10
	D_6		TTL	9	11
	D_7	Most Significant Bit	TTL	10	12
Power	V_{DDA}	Analog Supply Voltage	+5V	14, 15, 18	17, 18, 21
	V_{DDD}	Digital Supply Voltage	+5V	11, 13	13, 16
	A_{GND}	Analog Ground	0.0V	20, 21	24, 25
	D_{GND}	Digital Ground	0.0V	2, 24	3, 28
No Connect	N/C	Not Connected	open		1, 8, 15, 22

Figure 4. Timing Diagram

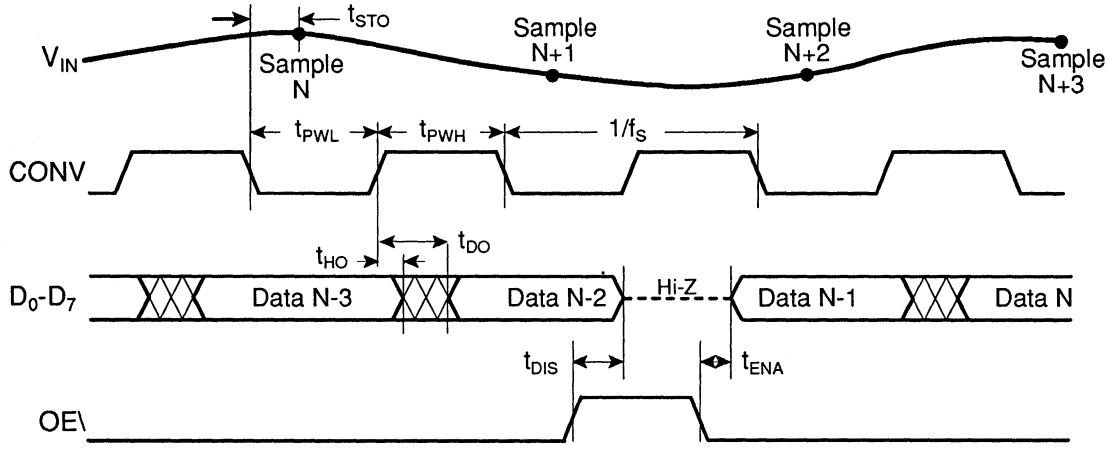


Figure 5. Equivalent Digital Input Circuit

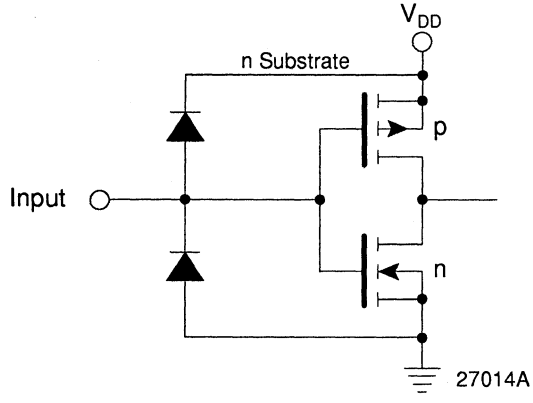


Figure 6. Equivalent Analog Input Circuit

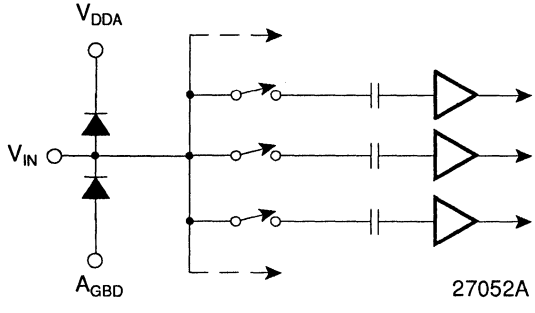


Figure 7. Equivalent Digital Output Circuit

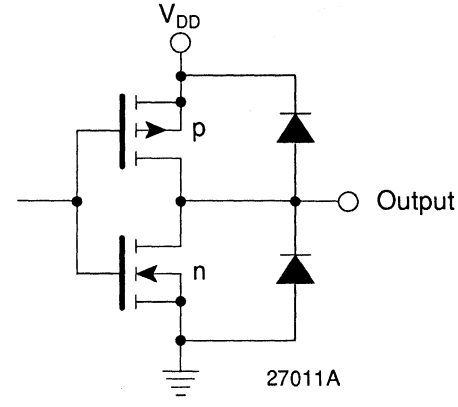
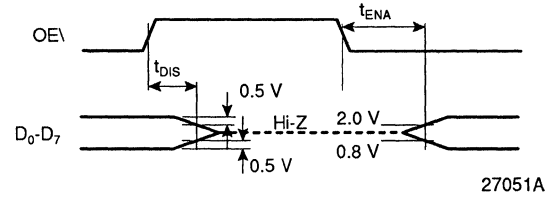


Figure 8. Transition Levels for Three-State Measurements



Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{DDA} (measured to A_{GND}) ..... -0.5 to +7.0V
V_{DDD} (measured to D_{GND}) ..... -0.5 to +7.0V
V_{DDA} (measured to V_{DDD}) ..... -0.5 to +0.5V
D_{GND} (measured to A_{GND}) ..... -0.5 to +0.5V

Inputs

Applied voltage[2] CONV, OE\ ..... -0.5 to V_{DDD} V
Applied voltage[2] R_T, R_B, V_{IN} ..... A_{GND} to V_{DDA} V

Outputs

Applied Voltage[2] ..... -0.5 to (V_{DD}+0.5) V
Forced Current[3,4] ..... -6.0 to 6.0 mA
Short Circuit Duration
(Single output in HIGH state to GND) ..... 1 second

Temperature

Operating, ambient ..... -20 to +90°C
Junction ..... +140°C
Lead, soldering (10 seconds) ..... +300°C
Vapor phase soldering (1 minute) ..... +220°C
Storage ..... -65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating conditions

Parameter		Standard Temperature Range			Units
		Min	Nom	Max	
V_{DDA}	Analog Supply Voltage	2.7	3.0	3.6	V
V_{DDD}	Digital Supply Voltage	2.7	3.0	3.6	V
A_{GND}	Analog Ground Voltage (Measured to D_{GND})	-0.1	0	0.1	V
f_S	Conversion Rate				
	TMC1173-5	5			Msps
	TMC1173-10	10			Msps
t_{PWH}	CONV pulse width, HIGH				
	TMC1173-5	20			ns
	TMC1173-10	20			ns
t_{PWL}	CONV pulse width, LOW				
	TMC1173-5	20			ns
	TMC1173-10	20			ns
R_T	Reference, Top	0		V_{DD}	V
R_B	Reference, Bottom	0		1.3	V
$R_T - R_B$	Reference Voltage Differential	1.2		3.3	V
V_{IN}	Analog Input Range	R_B		R_T	V
V_{IH}	Input Voltage, Logic HIGH	0.85			x V_{DD}
V_{IL}	Input Voltage, Logic LOW			0.2	x V_{DD}
I_{OH}	Output Current, Logic HIGH			-1.0	mA
I_{OL}	Output Current, Logic LOW			2.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical characteristics

Parameter		Conditions	Standard Temperature Range			Units
			Min	Typ	Max	
I_{DD}	Total Power Supply Current	V_{DDA}=V_{DDD}= 3.6V, C_{LOAD} = 35pF				
		TMC1173-5, f_S = 5 Msps		17	25	mA
		TMC1173-10, f_S = 10 Msps		21	30	mA
I_{DDQ}	Quiescent Power Supply Current	V_{DDA}=V_{DDD}=Max,CONV=LOW		15		mA
		V_{DDA}=V_{DDD}=Max,CONV=HIGH		20		mA
P_D	Total Power Dissipation	V_{DDA} = V_{DDD} = 3.6V, C_{LOAD} = 35pF				
		TMC1173-5, f_S = 5 Msps		61		mW
		TMC1173-10, f_S = 10 Msps		76		mW
C_{IN}	Input Capacitance	CONV = HIGH		16	18	pF
R_{IN}	Input Resistance		100			kΩ
I_{CB}	Analog Input Current				±10	µA
I_{REF}	Reference Current	R_T = 1.2 V, R_B = 0.0 V		2.4		mA
R_{REF}	Reference Resistance		400	500		Ω
V_{RT}	Ref. Voltage, Top	R_B = V_{R-}, R_T = V_{R+}		1.6		V
V_{RB}	Ref. Voltage, Bottom	R_B = V_{R-}, R_T = V_{R+}		0.4		V
V_{RT}-V_{RB}	Ref.Voltage Diff.	R_B = V_{R-}, R_T = V_{R+}		1.2		V
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Leakage Current, HIGH	OE\ = HIGH, V_{OUT} = V_{DD}			±10	µA
I_{OZL}	Leakage Current, LOW	OE\ = HIGH, V_{OUT} = D_{GND}			±10	µA
I_{OS}	Short-Circuit Current				30	mA
V_{OH}	Output Voltage, HIGH	D_{0-7}, I_{OH} = Max	2.2			V
V_{OL}	Output Voltage, LOW	D_{0-7}, I_{OH} = Max			0.3	V

Note: Values shown in Typ column are typical for V_{DD} = +3.0 V and T_A = 25°C.

Switching Characteristics

Parameter		Conditions	Standard Temperature Range			Units
			Min	Typ	Max	
t_{STO}	Sampling Time Offset		0	3	10	ns
t_{DO}	Output Delay Time	C_{LOAD} = 15pF			44	ns
t_{HO}	Output Hold Time	C_{LOAD} = 15pF	5			ns
t_{ENA}	Output Enable Time				65	ns
t_{DIS}	Output Disable Time				65	ns

System Performance Characteristics

Parameter		Conditions	Standard Temperature Range			Units
			Min	Typ	Max	
E_{LI}	Integral Linearity Error	$R_B = V_{R-}$, $R_T = V_{R+}$		±0.3	±0.5	LSB
		$R_B = A_{GND}$, R_T = +1.2 V		±0.3	±0.5	LSB
		$R_B = A_{GND}$, R_T = +2.7 V		±0.3	±0.5	LSB
		$R_B = A_{GND}$, $R_T = V_{DDA}$		±0.3	±0.5	LSB
E_{LD}	Differential Linearity Error	$R_B = V_{R-}$, $R_T = V_{R+}$		±0.3	±0.5	LSB
		$R_B = A_{GND}$, R_T = +1.2 V		±0.3	±0.5	LSB
		$R_B = A_{GND}$, R_T = +2.7 V		±0.3	±0.5	LSB
		$R_B = A_{GND}$, $R_T = V_{DDA}$		±0.3	±0.5	LSB
CS	Code Size		5		195	%nom
BW	Bandwidth				5	MHz
E_{ap}	Aperture Error			30		ps
E_{OT}	Offset Voltage, Top	$R_T - V_{IN}$ for most positive code transition			±75	mV
E_{OB}	Offset Voltage, Bottom	$R_B - V_{IN}$ for most negative code transition			±40	mV
DG	Differential Gain	f_S = 14.3 Msps, NTSC 40 IRE ramp, for $R_B = V_{R-}$, $R_T = V_{R+}$ and $R_B = A_{GND}$, R_T = +1.2 V V_{DD} = +3.0 V, T_A = 25°C		2		%
DP	Differential Phase	f_S = 14.3 Msps, NTSC 40 IRE ramp, for $R_B = V_{R-}$, $R_T = V_{R+}$ and $R_B = A_{GND}$, R_T = +1.2 V V_{DD} = +3.0 V, T_A = 25°C		1		°

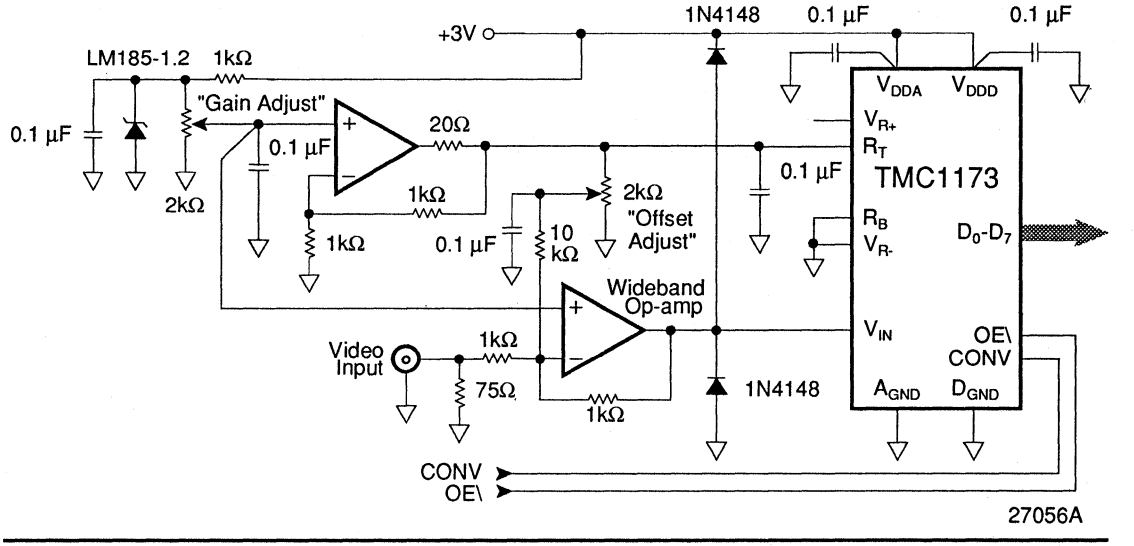
Note: Values shown in Typ column are typical for V_{DD} = +3.0 V and T_A = 25°C. Bandwidth is the frequency band in which a full-scale sinewave can be digitized without spurious codes.

System Performance Characteristics

Parameter		Conditions	Standard Temperature Range			Units
			Min	Typ	Max	
SNR	Signal-to-Noise Ratio	TMC1173-5, f_S = 5 Msps,				
		f_{IN} = 1.24 MHz	43	46		dB
		f_{IN} = 2.48 MHz	42	45		dB
		TMC1173-10, f_S = 10 Msps,				
		f_{IN} = 1.24 MHz	43	45		dB
		f_{IN} = 2.48 MHz	42	44		dB
		f_{IN} = 4.96 MHz	40	42		dB
SFDR	Spurious Free Dynamic Range	TMC1173-5, f_S = 5 Msps,				
		f_{IN} = 1.24 MHz	37	43		dB
		f_{IN} = 2.48 MHz	32	40		dB
		TMC1173-10, f_S = 10 Msps,				
		f_{IN} = 1.24 MHz	37	43		dB
		f_{IN} = 2.48 MHz	31	40		dB
		f_{IN} = 4.96 MHz	26	32		dB

Note: SNR values do not include the harmonics of the fundamental frequency.
SFDR is the ratio in dB of fundamental amplitude to the harmonic with highest amplitude.
Values shown in Typ column are typical for V_{DD} = +3.0 V and T_A = 25°C.

Figure 9. Typical Interface Circuit



Application Notes

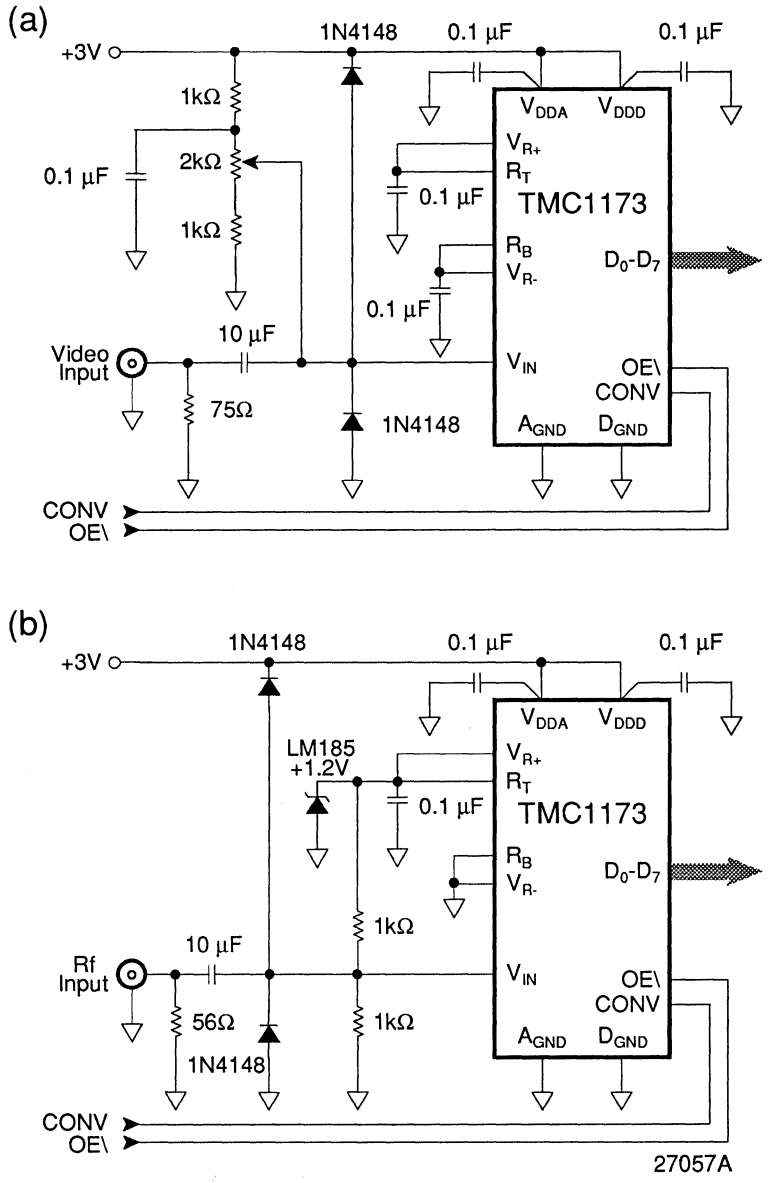
The circuit in Figure 9 uses a band-gap reference to generate a variable R_T reference voltages for the TMC1173 as well as a bias voltage to offset the wideband input amplifier to mid-range. An "offset adjust" is also shown for varying the mid-range voltage level. The operational amplifier in the reference circuitry is a standard general-purpose 741-type.

The voltage reference is variable from 0.0 to 2.4 volts on R_T while R_B is grounded. Note the diode clamps on the wideband op-amp output. These prevent the A/D input from being driven beyond the power supply. Diode protection is advised as good practice to prevent analog input signals from being driven beyond the power supply.

The circuit in Figure 10a shows the self-bias of R_T and R_B by connection to V_{R+} and V_{R-}. This sets up a 0.4 to 1.5 Volt input range for V_{IN}. The input range is susceptible to power supply variation since the voltages on R_T and R_B are directly derived from V_{DDA}. The video input is AC-coupled and biased at a variable midpoint of the A/D input range. This circuit offers the advantage of minimum support circuitry for the most cost-sensitive applications.

In Figure 10b, an external band-gap reference sets R_T to +1.2 Volts while R_B is grounded. The internal pull-up resistor, R+, provides the bias current for the band-gap diode. The input impedance of the Rf input is approximately 50Ω and the A/D converter input is biased at the mid-point of the input range.

Figure 10. Typical Interface Circuits



Grounding

The TMC1173 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DDD} and V_{DDA}) come from the same source and ground connections (D_{GND} and A_{GND}) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.
The digital circuitry that gets its input from the TMC1173 should be referred on the system digital ground plane.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option...even for breadboarding. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{IN}, R_T, R_B, V_{R+}, V_{R-}) as short as possible and as far as possible from all digital signals. The TMC1173 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC1173 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1173 is the same as that of the system's digital circuitry, power to the TMC1173 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

3. the ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

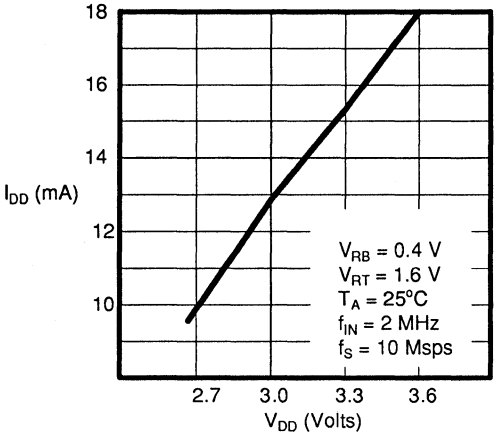
4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They typically supply adjacent circuitry on the device, which generate varying amounts of noise. For best results, use 0.1µF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC1173, the voltage reference or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1173 and its related analog circuitry can have an adverse effect on performance.

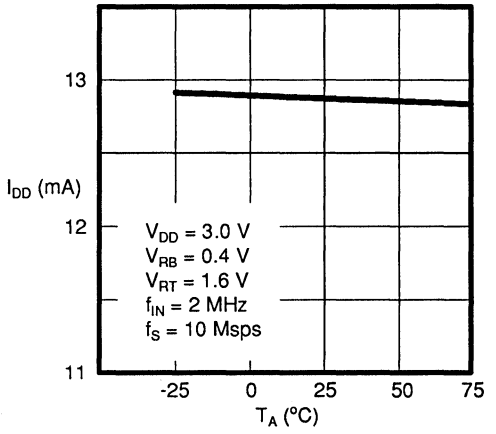
6. CONV should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Typical Performance Curves

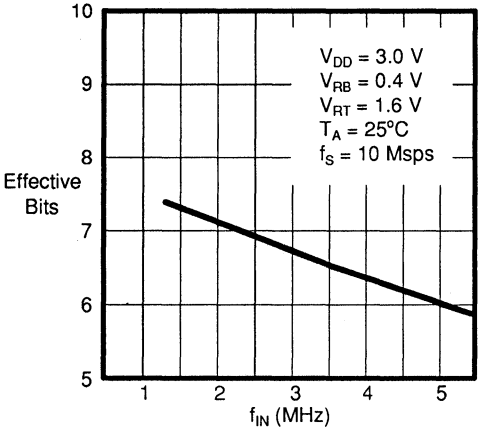
A. I_{DD} vs. V_{DD} at 25°C



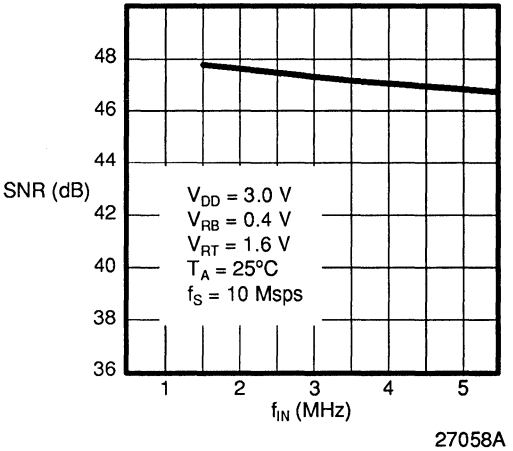
B. I_{DD} vs. T_A at f_S = 10 Msps



C. EFB vs. f_{IN}



D. SNR vs. f_{IN}



27058A

Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC1173M7C5	5	T_A: 0°C to 70°C	Commercial	24-Lead SOIC	1173M7C5
TMC1173M7C10	10	T_A: 0°C to 70°C	Commercial	24-Lead SOIC	1173M7C10
TMC1173N2C5	5	T_A: 0°C to 70°C	Commercial	24-Pin Plastic DIP	1173N2C5
TMC1173N2C10	10	T_A: 0°C to 70°C	Commercial	24-Pin Plastic DIP	1173N2C10
TMC1173R3C5	5	T_A: 0°C to 70°C	Commercial	28-Lead Plastic PLCC	1173R3C5
TMC1173R3C10	10	T_A: 0°C to 70°C	Commercial	28-Lead Plastic PLCC	1173R3C10
TMC1175E1C	30	T_A: 00°C to 70°C	Commercial	Eurocard PC Board	TMC1175E1C

40GO7280 Rev B 8/93

TMC1175
CMOS 8-Bit Video A/D Converter

Description

The TMC1175 analog-to-digital (A/D) converter employs a two-step architecture with integral track/hold. The device converts analog signals into 8-bit digital words at rates up to 40 Msps (Megasamples per second). The architecture and CMOS technology reduce typical power dissipation to less than 150 mW.

The TMC1175 operates from a single +5 Volt power supply and has internal voltage reference resistors which allow self-bias operation. The input capacitance is very low, simplifying the design of, or eliminating, the need for video driving amplifiers. All digital inputs and three-state outputs are TTL-compatible.

The TMC1175 is available in 24-pin plastic DIP, 24-Lead plastic SOIC, and 28-lead J-lead PLCC packages. Mil-temperature versions are available in CERDIP or ceramic LCC packages. Performance specifications are guaranteed over the -20 to 75°C and -55 to 125°C temperature ranges.

Features

- 8-bit resolution
- 10, 20, and 40 Msps conversion rate
- Integral track/hold
- Differential linearity error <±0.5 LSB
- Single +5V Power Supply
- <150 mW power dissipation
- Differential phase <0.5°
- Differential gain <1%
- Three-state 3V TTL-compatible outputs
- Very low cost

Applications

- Digital television
- Video digitizing
- Low cost, high speed data conversion
- Image scanners
- Personal computer video boards
- Multimedia

Related Products

- TMC1173 Low-Voltage, Low-Power 8-Bit Video A/D Converter
- TMC22070 Genlocking Video Digitizer
- TDC3310 10-Bit Video D/A Converter
- TMC22090/TMC22190 Digital Video Encoder
- TMC2242/TMC2243/TMC2246 Video Filter
- TMC2302 Image Manipulation Sequencer

Block Diagram

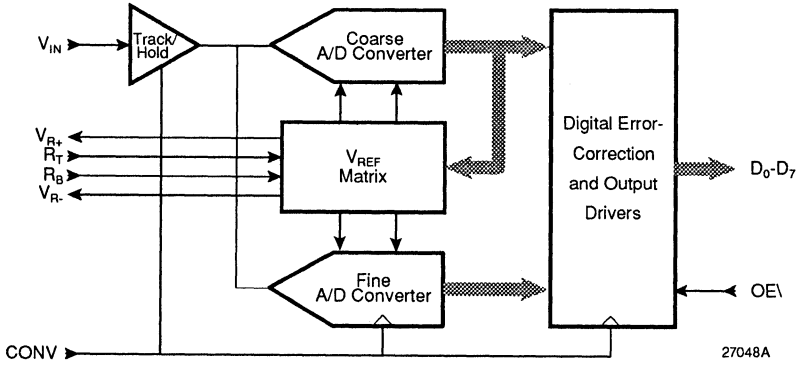
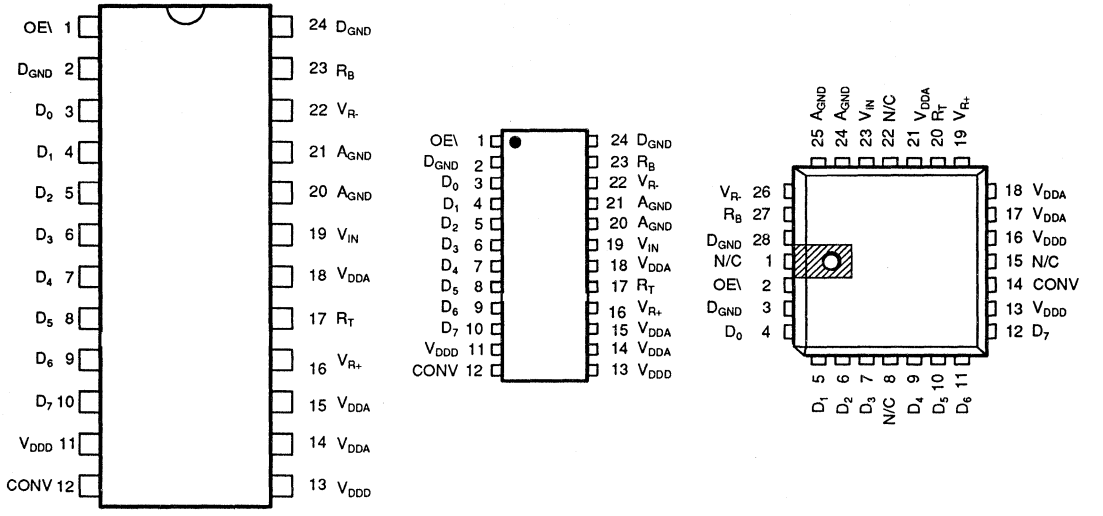


Figure 2. Pin Assignments and Packages



N2 Package
24-pin Plastic DIP

M7 Package
24-Lead SOIC

R3 Package
28-lead J-lead PLCC

27049A

General Description

The TMC1175 is an 8-bit A/D converter which uses a two-step architecture to perform analog-to-digital conversion at rates up to 40 Msps. The input signal is held in an integral track/hold stage during the conversion process. Pipelined operation is achieved with one input sample taken and one output word provided for each convert cycle. The first step in the conversion process is a coarse 4-bit conversion. The coarse 4-bit result determines the range of the subsequent fine 4-bit A/D conversion step. To eliminate spurious codes, the fine 4-bit A/D converter output is gray-coded and converted to binary before combining with the coarse result to form the complete 8-bit result.

Analog Input and Voltage References

The TMC1175 converts analog signals in the range $R_T \leq V_{IN} \leq R_B$ into digital data. The A/D converter input range is very flexible and extends from the +5 Volt power supply to ground. Normally, external voltage reference sources are connected to the R_T and R_B pins or R_B is grounded.

Two reference pull-up and pull-down resistors connected to V_{R+} and V_{R-}, are provided for operation without external voltage reference circuitry. These voltages applied to R_T and R_B may be generated externally, or are self-generated by connecting V_{R+} to R_T and V_{R-} to R_B. In the latter case the power supply voltage is divided by on-chip resistors to bias the R_T and R_B points.

The self-bias reference voltages are useful in applications where overall circuit cost is important and absolute accuracy and stability of the A/D converter gain is not critical.

The V_{IN} input range is from R_B to R_T. The device will not be damaged by signals within the range A_{GND} to V_{DD}.

Figure 3. Reference Resistors

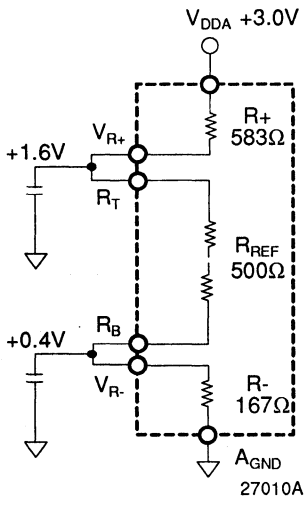


Table 1. Output Coding Table

Input Voltage	Output Code MSB LSB
$<R_B$	00000000
R_B	00000000
R_B + 1 LSB	00000001
•	•
•	•
$(R_T + R_B)/2$	01111111
$(R_T + R_B)/2$ + 1 LSB	10000000
•	•
•	•
R_T - 1 LSB	11111110
R_T	11111111
$>R_T$	11111111

Note: 1 LSB = $(R_T - R_B)/255$

Digital Inputs and Outputs

The sampling of the applied input signal takes place on the falling edge of the CONV signal. The output word is available after the rising edge of CONV, delayed by 2 1/2 CONV cycles. The output remains valid for t_{HO} (Output Hold Time) and new data becomes valid t_D (Output Delay Time) after the rising edge of CONV.

The outputs of the TMC1175 are TTL-compatible and are capable of driving four low-power Schottky TTL (54/74LS) loads. An output enable control, OE\, places the outputs in a high-impedance state when HIGH. The outputs are enabled when OE\ is LOW.

Power and Ground

The TMC1175 operates from a single +5 Volt power supply. For optimum performance, it is recommended that A_{GND} and D_{GND} pins of the TMC1175 be connected to the system analog ground plane.

Pin Functions

V_{IN} — The input voltage conversion range extends from the voltage applied to the R_T and R_B pins.

R_T, R_B — The top and bottom inputs to the reference resistor ladder. DC voltages applied to R_T and R_B define the V_{IN} conversion range.

V_{R+},V_{R-} — Internal pull-up and pull-down reference resistors used in self-bias operation.

CONV — A/D converter clock input. V_{IN} is sampled on the falling edge of CONV.

OE\ — Output Enable. When LOW, D_0-D_7 are enabled. When HIGH, D_0-D_7 are in a high-impedance state.

D_0-D_7 — Eight-bit TTL-compatible digital outputs. Valid data is output on the rising edge of CONV.

V_{DDA},V_{DDD} +5 Volt power inputs. These should come from the same power source and be decoupled to A_{GND}.

A_{GND},D_{GND} Ground inputs should be connected to the system analog ground plane.

Table 2. Package Interconnections

Signal Type	Name	Function	Value	N2, M7 Pin	R3, C3 Pin
Inputs	V_{IN}	Analog Input	R_B-R_T	19	23
	R_T	Reference Voltage Top Input	2.6V	17	20
	R_B	Reference Voltage Bottom Input	0.6V	23	27
	V_{R+}	Reference Voltage Top Source	2.6V	16	19
	V_{R-}	Reference Voltage Bottom Source	0.6V	22	26
	OE\	Output enable	TTL	1	2
	CONV	Convert (Clock) input	TTL	12	14
Outputs	D_0	Least Significant Bit	TTL	3	4
	D_1		TTL	4	5
	D_2		TTL	5	6
	D_3		TTL	6	7
	D_4		TTL	7	9
	D_5		TTL	8	10
	D_6		TTL	9	11
	D_7	Most Significant Bit	TTL	10	12
Power	V_{DDA}	Analog Supply Voltage	+5V	14, 15, 18	17, 18, 21
	V_{DDD}	Digital Supply Voltage	+5V	11, 13	13, 16
	A_{GND}	Analog Ground	0.0V	20, 21	24, 25
	D_{GND}	Digital Ground	0.0V	2, 24	3, 28
No Connect	N/C	Not Connected	open		1, 8, 15, 22

Figure 4. Timing Diagram

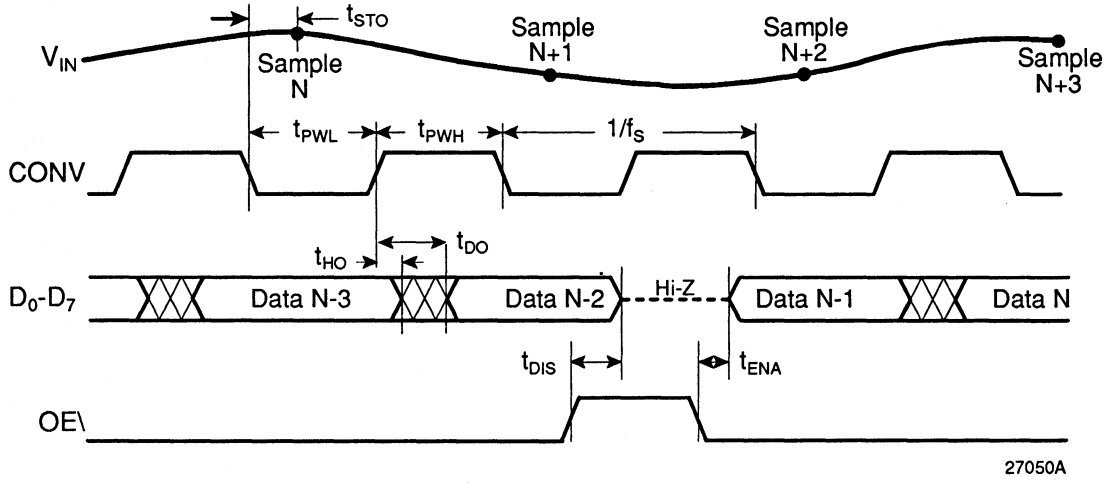


Figure 5. Equivalent Digital Input Circuit

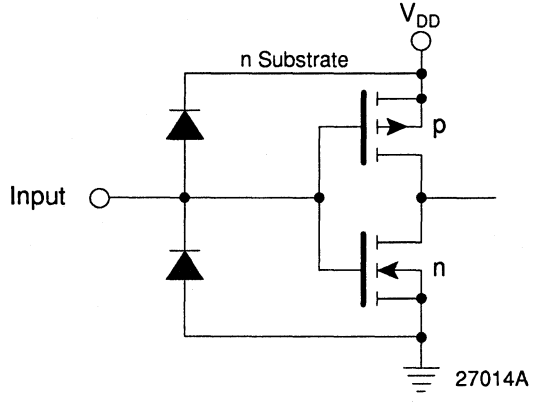


Figure 6. Equivalent Analog Input Circuit

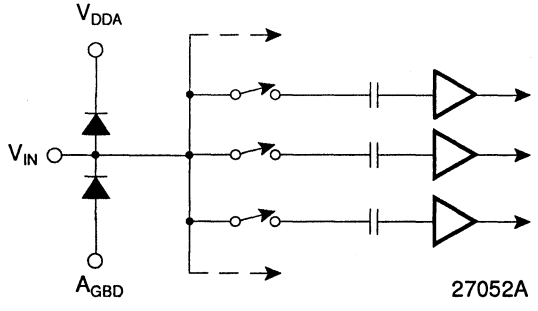


Figure 7. Equivalent Digital Output Circuit

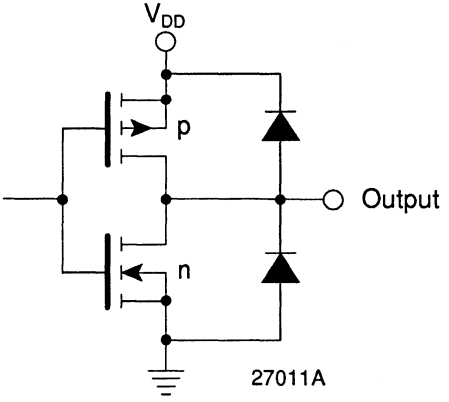
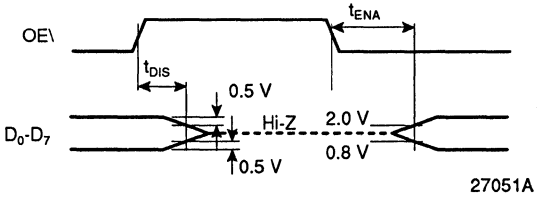


Figure 8. Transition Levels for Three-State Measurements



Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Supply Voltages
- V_{DDA} (measured to A_{GND}) ..... -0.5 to +7.0V
- V_{DDD} (measured to D_{GND}) ..... -0.5 to +7.0V
- V_{DDA} (measured to V_{DDD}) ..... -0.5 to +0.5V
- D_{GND} (measured to A_{GND}) ..... -0.5 to +0.5V

Inputs
- Applied voltage[2] CONV, OE\ ..... -0.5 to V_{DDD} V
- Applied voltage[2] R_T, R_B, V_{IN} [2] ..... A_{GND} to V_{DDA} V

Outputs
- Applied Voltage[2] ..... -0.5 to (V_{DD}+0.5) V
- Forced Current[3,4] ..... -6.0 to 6.0 mA
- Short Circuit Duration
- (Single output in HIGH state to GND) ..... 1 second

Temperature
- Operating, ambient ..... -55 to +125°C
- Junction ..... +140°C
- Lead, soldering (10 seconds) ..... +300°C
- Vapor phase soldering (1 minute) ..... +220°C
- Storage ..... -65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
T_A	Ambient Temperature, Still Air	-20		75				°C
T_C	Case Temperature, Still Air				-55		125	°C
V_{DDA}	Analog Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{DDD}	Digital Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
A_{GND}	Analog Ground Voltage (Measured to D_{GND})	-0.1	0	0.1	-0.1	0.0	0.1	V
f_S	Conversion Rate							
	TMC1175-20	20			20			Msps
	TMC1175-30	30						Msps
	TMC1175-40	40						Msps
t_{PWH}	CONV pulse width, HIGH							
	TMC1175-20	15			17			ns
	TMC1175-30	13						ns
	TMC1175-40	12						ns
t_{PWL}	CONV pulse width, LOW							
	TMC1175-20	15			17			ns
	TMC1175-30	15						ns
	TMC1175-40	12						ns
R_T	Reference, Top	0		V_{DD}	0		V_{DD}	V
R_B	Reference, Bottom	0		2.7	0		2.7	V
$R_T - R_B$	Reference Voltage Differential	1.8		5	1.8		5	V
V_{IN}	Analog Input Range	R_B		R_T	R_B		R_T	V
V_{IH}	Input Voltage, Logic HIGH	4.0			4.0			V
V_{IL}	Input Voltage, Logic LOW			1.0			1.0	V
I_{OH}	Output Current, Logic HIGH			-1.5			-1.0	mA
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA

Electrical characteristics

Parameter		Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
I_{DD}	Total Power Supply Current	V_{DDA}=V_{DDD}=Max, worst-case, C_{LOAD} = 35pF							
		TMC1175-20, f_S = 20 Msps		35	60		35	65	mA
		TMC1175-30, f_S = 30 Msps		43	70				mA
		TMC1175-40, f_S = 40 Msps		50	80				mA
I_{DDQ}	Quiescent Power Supply Current	V_{DDA}=V_{DDD}=Max,CONV=LOW		13			13		mA
		V_{DDA}=V_{DDD}=Max,CONV=HIGH		24			24		mA
P_D	Total Power Dissipation	V_{DDA} = V_{DDD} = Nom, C_{LOAD} = 35pF							
		TMC1175-20, f_S = 20 Msps		175			175		mW
		TMC1175-30, f_S = 30 Msps		215					mW
		TMC1175-40, f_S = 40 Msps		250					mW
C_{IN}	Input Capacitance	CONV = HIGH		16	18		16	18	pF
R_{IN}	Input Resistance		100			100			kΩ
I_{CB}	Analog Input Current				±5			±10	µA
I_{REF}	Reference Current			7.5	10.5		7.5	10.5	mA
R_{REF}	Reference Resistance		190	270		190	270		Ω
V_{RT}	Ref. Voltage, Top	R_B = V_{R-}, R_T = V_{R+}		2.6			2.6		V
V_{RB}	Ref. Voltage, Bottom	R_B = V_{R-}, R_T = V_{R+}		0.6			0.6		V
V_{RT} -V_{RB}	Ref.Voltage Diff.	R_B = V_{R-}, R_T = V_{R+}		2.0			2.0		V
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±5			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±5			±10	µA
I_{OZH}	Leakage Current, HIGH	OE\ = HIGH, V_{OUT} = V_{DD}			±5			±10	µA
I_{OZL}	Leakage Current, LOW	OE\ = HIGH, V_{OUT} = D_{GND}			±5			±10	µA
I_{OS}	Short-Circuit Current				30			30	mA
V_{OH}	Output Voltage, HIGH	D_{0-7}, I_{OH} = Max	4.0			4.0			V
V_{OL}	Output Voltage, LOW	D_{0-7}, I_{OH} = Max			0.4			0.4	V

Note: Values shown in Typ column are typical for V_{DD} = +5.0 V and T_A = 25°C.

Switching Characteristics

Parameter		Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
t_{STO}	Sampling Time Offset	TMC1175-20	0	3	8	0	5	10	ns
		TMC1175-30	0	3	8				ns
		TMC1175-40	0	3	8				ns
t_{DO}	Output Delay Time	C_{LOAD} = 15pF							
		TMC1175-20			30			38	ns
		TMC1175-30			30				ns
		TMC1175-40			20				ns
t_{HO}	Output Hold Time	C_{LOAD} = 15pF							
		TMC1175-20	5			5			ns
		TMC1175-30	5						ns
		TMC1175-40	5						ns
t_{ENA}	Output Enable Time				65			65	ns
t_{DIS}	Output Disable Time				65			65	ns

System Performance Characteristics

Parameter		Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
E_{LI}	Integral Linearity Error	$R_B = V_{R-}$, $R_T = V_{R+}$		±0.75	±1.0			±1.0	LSB
		$R_B = A_{GND}$, R_T = +2.5 V		±0.75	±1.0		±0.75		LSB
		$R_B = A_{GND}$, $R_T = V_{DDA}$		±0.75			±0.75		LSB
E_{LD}	Differential Linearity Error	$R_B = V_{R-}$, $R_T = V_{R+}$		±0.3	±0.5			±0.5	LSB
		$R_B = A_{GND}$, R_T = +2.5 V		±0.3	±0.5		±0.3		LSB
		$R_B = A_{GND}$, $R_T = V_{DDA}$		±0.3			±0.3		LSB
CS	Code Size		10		190	5		195	%nom
BW	Bandwidth	TMC1175-20			10			10	MHz
		TMC1175-30			12				MHz
		TMC1175-40, V_{DD} = 5.0V, T_A = 0°C to 70°C			12				MHz
E_{ap}	Aperture Error			30			30		ps
E_{OT}	Offset Voltage, Top	$R_T - V_{IN}$ for most positive code transition			-75			-75	mV
E_{OB}	Offset Voltage, Bottom	$R_B - V_{IN}$ for most negative code transition			±40			±40	mV
DG	Differential Gain	f_S = 14.3 Msps, NTSC 40 IRE ramp, for $R_B = V_{R-}$, $R_T = V_{R+}$ and $R_B = A_{GND}$, R_T = +2.5 V, V_{DD} = +5.0 V, T_A = 25°C			2.0			2.0	%
DP	Differential Phase	f_S = 14.3 Msps, NTSC 40 IRE ramp, for $R_B = V_{R-}$, $R_T = V_{R+}$ and $R_B = A_{GND}$, R_T = +2.5 V, V_{DD} = +5.0 V, T_A = 25°C			1.0			1.0	°

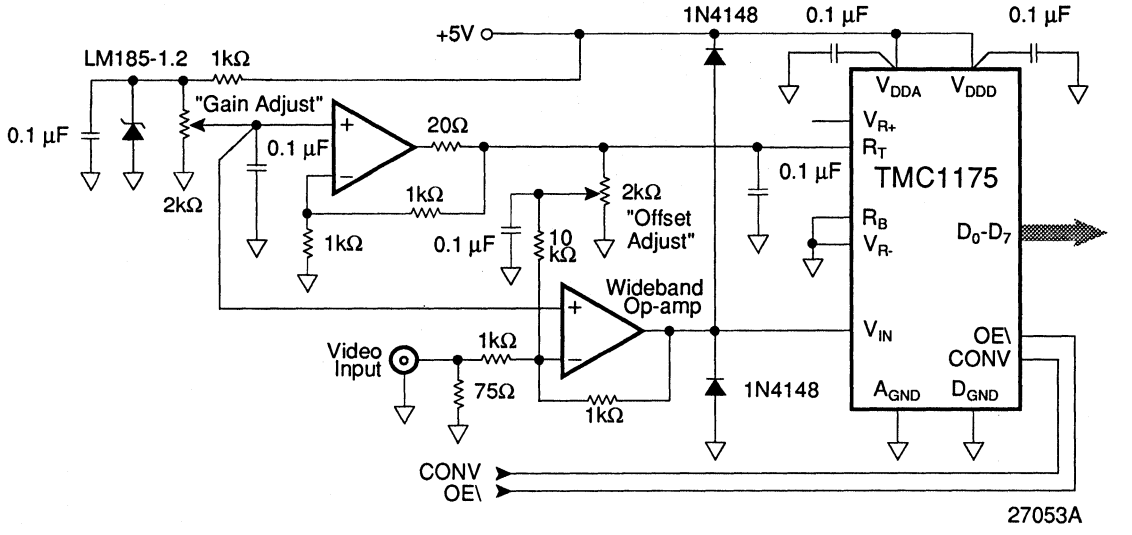
Note: Values shown in Typ column are typical for V_{DD} = +5.0 V and T_A = 25°C. Bandwidth is the frequency band in which a full-scale sinewave can be digitized without spurious codes.

System Performance Characteristics

Parameter		Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
SNR	Signal-to-Noise Ratio	TMC1175-20, f_S = 20 Msps,							
		f_{IN} = 1.24 MHz	44	46		43	46		dB
		f_{IN} = 2.48 MHz	43	45		42	45		dB
		f_{IN} = 6.98 MHz	42	45		40	45		dB
		f_{IN} = 10.0 MHz	42	45		40	45		dB
		TMC1175-30, f_S = 30 Msps, t_{PWH} = 13 ns							
		f_{IN} = 1.24 MHz	42	44					dB
		f_{IN} = 6.98 MHz	41	43					dB
		f_{IN} = 10.0 MHz	40	43					dB
		f_{IN} = 12.0 MHz	39	42					dB
		TMC1175-40, f_S = 40 Msps, T_A = 0°C to 70°C							
		f_{IN} = 1.24 MHz	40	43					dB
		f_{IN} = 6.98 MHz	39	42					dB
		f_{IN} = 10.0 MHz	38	41					dB
		f_{IN} = 12.0 MHz	38	41					dB
SFDR	Spurious Free Dynamic Range	TMC1175-20, f_S = 20 Msps,							
		f_{IN} = 1.24 MHz	44	51		41	51		dB
		f_{IN} = 2.48 MHz	43	47		39	47		dB
		f_{IN} = 6.98 MHz	32	38		30	38		dB
		f_{IN} = 10.0 MHz	30	35		27	35		dB
		TMC1175-30, f_S = 30 Msps,							
		f_{IN} = 1.24 MHz	42	48					dB
		f_{IN} = 6.98 MHz	32	36					dB
		f_{IN} = 10.0 MHz	30	34					dB
		f_{IN} = 12.0 MHz	28	32					dB
		TMC1175-40, f_S = 40 Msps, T_A = 0°C to 70°C							
		f_{IN} = 1.24 MHz	41	44					dB
		f_{IN} = 6.98 MHz	31	34					dB
		f_{IN} = 10.0 MHz	30	33					dB
		f_{IN} = 12.0 MHz	30	32					dB

Note: SNR values do not include the harmonics of the fundamental frequency.
SFDR is the ratio in dB of fundamental amplitude to the harmonic with highest amplitude.
Values shown in Typ column are typical for V_{DD} = +5.0 V and T_A = 25°C.

Figure 9. Typical Interface Circuit



Application Notes

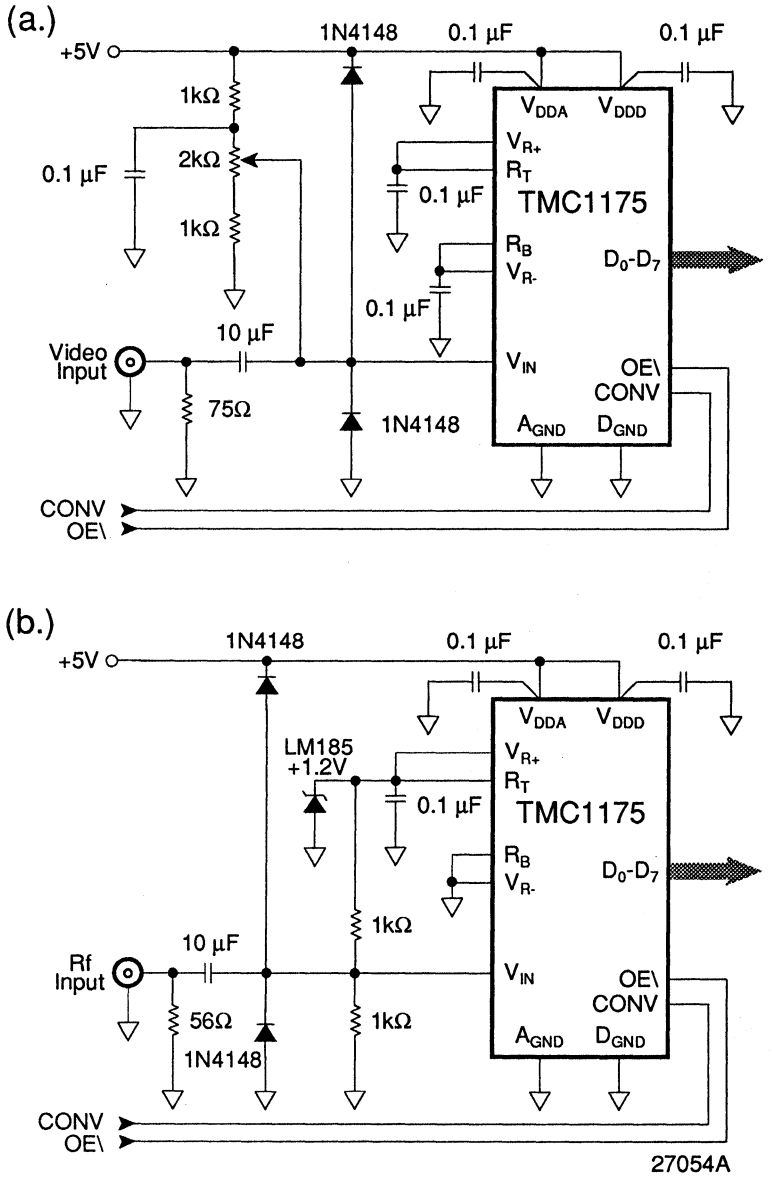
The circuit in Figure 9 uses a band-gap reference to generate a variable R_T reference voltages for the TMC1175 as well as a bias voltage to offset the wideband input amplifier to mid-range. An "offset adjust" is also shown for varying the mid-range voltage level. The operational amplifier in the reference circuitry is a standard general-purpose 741-type.

The voltage reference is variable from 0.0 to 2.4 volts on R_T while R_B is grounded. Note the diode clamps on the wideband op-amp output. These prevent the A/D input from being driven beyond the power supply. Diode protection is advised as good practice to limit analog input voltages to within the power supply range.

The circuit in Figure 10a shows the self-bias of R_T and R_B by connection to V_{R+} and V_{R-}. This sets up a 0.6 to 2.6 Volt input range for V_{IN}. The input range is susceptible to power supply variation since the voltages on R_T and R_B are directly derived from V_{DDA}. The video input is AC-coupled and biased at a variable midpoint of the A/D input range. This circuit offers the advantage of minimum support circuitry for the most cost-sensitive applications.

In Figure 10b, an external band-gap reference sets R_T to +1.2 Volts while R_B is grounded. The internal pull-up resistor, R+, provides the bias current for the band-gap diode. The input impedance of the Rf input is approximately 50Ω and the A/D converter input is biased at the mid-point of the input range.

Figure 10. Typical Interface Circuit



Grounding

The TMC1175 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DDD} and V_{DDA}) come from the same source and ground connections (D_{GND} and A_{GND}) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

The digital circuitry that gets its input from the TMC1175 should be referred on the system digital ground plane.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option, even for breadboarding. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{IN}, R_T, R_B, V_{R+}, V_{R-}) as short as possible and as far as possible from all digital signals. The TMC1175 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC1175 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1175 is the same as that of the system's digital circuitry, power to the TMC1175 should be decoupled with ferrite beads and 0.1μF capacitors to reduce noise.

3. the ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

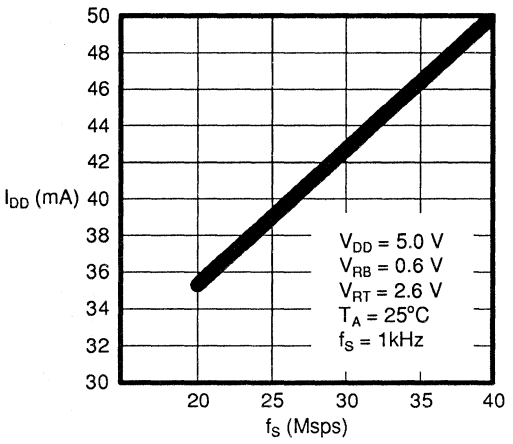
4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They typically supply adjacent circuitry on the device, which generate varying amounts of noise. For best results, use 0.1μF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC1175, the voltage reference or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1175 and its related analog circuitry can have an adverse effect on performance.

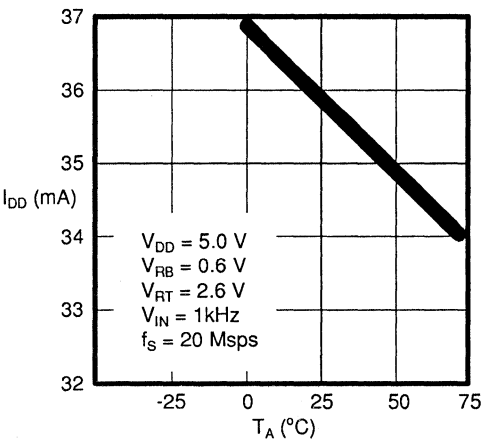
6. CONV should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Typical Performance Curves

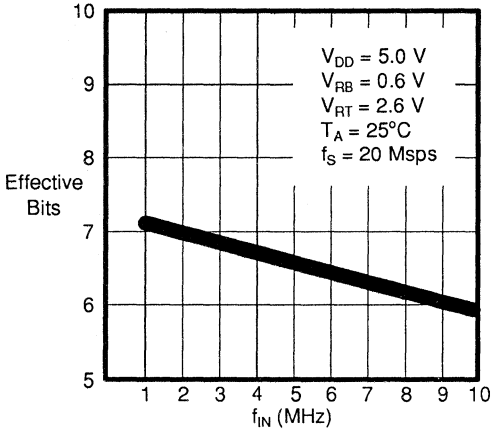
A. I_{DD} vs. f_S at 25°C



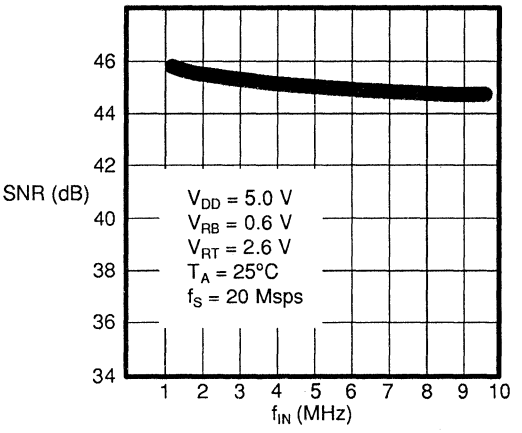
B. I_{DD} vs. T_A at f_S = 20 Msps



C. EFB vs. f_{IN}



D. SNR vs. f_{IN}



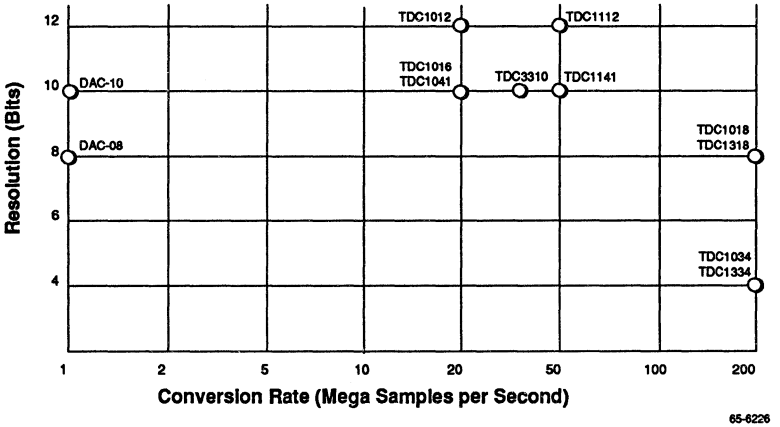
27055A

Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC1175M7C20	20	T_A: -20°C to 75°C	Commercial	24-Lead SOIC	1175M7C20
TMC1175M7C30	30	T_A: -20°C to 75°C	Commercial	24-Lead SOIC	1175M7C30
TMC1175M7C40	40	T_A: -20°C to 75°C	Commercial	24-Lead SOIC	1175M7C40
TMC1175N2C20	20	T_A: -20°C to 75°C	Commercial	24-Pin Plastic DIP	1175N2C20
TMC1175N2C30	30	T_A: -20°C to 75°C	Commercial	24-Pin Plastic DIP	1175N2C30
TMC1175N2C40	40	T_A: -20°C to 75°C	Commercial	24-Pin Plastic DIP	1175N2C40
TMC1175R3C20	20	T_A: -20°C to 75°C	Commercial	28-Lead Plastic PLCC	1175R3C20
TMC1175R3C30	30	T_A: -20°C to 75°C	Commercial	28-Lead Plastic PLCC	1175R3C30
TMC1175R3C40	40	T_A: -20°C to 75°C	Commercial	28-Lead Plastic PLCC	1175R3C40
TMC1175B2F20	20	T_A: -55°C to 125°C	Commercial	24-Pin CERDIP	1175B2F20
TMC1175C3F20	20	T_A: -55°C to 125°C	Commercial	28-lead Ceramic LCC	1175C3F20
TMC1175E1C	30	T_A: -20°C to 75°C	Commercial	Eurocard PC Board	TMC1175E1C

40G06715 Rev B 8/93

D/A Converters



Raytheon's D/A converters address video, signal synthesis and graphics applications.

To the industry standard TDC1016 10-bit video D/A (75Ω voltage output) we have recently added the smaller, less expensive, and lower-power TDC1041 (TTL) and TDC1141 (ECL) DACs. The new devices are available in 28 lead PLCCs as well as DIPs, and have been optimized to produce quality video signals. The TDC3310 provides high-performance 10-bit video with TTL interfaces from a single +5V power supply.

The TDC1012 (20 Msps) and TDC1112 (50 Msps) have become the standard for signal synthesis applications. The 12-bit D/As have a Spurious-Free Dynamic Range (SFDR) of more than 70 dBc. They can directly drive a double-terminated 50Ω line (25Ω) to 1 Vp-p without an amplifier, simplifying interfacing and reducing overall system distortion.

Raytheon's line of high-speed graphics D/As addresses the needs of today's high-resolution display systems. Palette D/As with 6- or 8-bit resolution meet industry-standard pinouts and exceed competitors' performance. The single and triple 4- and 8-bit 200 Msps D/As are ideal for systems not requiring a palette function.

Product	Resolution Bits	Differential Linearity Error [1] (±%)	Conv Rate [1] (Msps)	Rise Time[1]	Package	Grade[2]	Notes
DAC-08	8	0.1	1.0	—	N, D	C, V, SMD, JAN	
TDC1018-1	8	0.20	200	1.7	B7, C3	C	Low cost ECL. Graphics-ready.
-	8	0.20	125	1.7	B7, C3	C	
TDC1318	8 (triple)	0.20	200	2	B5	C	Low Cost ECL. Graphics-ready.
TDC1016-10	10	0.05	20	4	N7, N5, B7, B5	C	Industry standard video DAC.
-9	10	0.10	20	4	N7, N5, B7, B5	C, A	Operates with TTL or ECL logic.
-8	10	0.20	20	4	N7, N5, B7, B5	C, A	
TDC1041-1	10	0.048	20	4	R3	C	Low cost 10-bit video D/A TTL interface.
-	10	0.096	20	4	R3	C	
TDC3310	10	0.096	40	10	N6, R6	C	Single +5V power supply
TDC1141-1	10	0.048	50	4	R3	C	Low cost 10-bit video D/A ECL interface.
-	10	0.096	50	4	R3	C	
TDC1012-3	12	0.012	20	4	N7, R3	C	Signal synthesis D/A. 70 dBc SFDR. Very
-2	12	0.024	20	4	J7, N7, R3	C, V, SMD	low glitch. Drives 25Ω directly. TTL Interface.
-1	12	0.048	20	4	J7, N7, R3	C, V, SMD	
-	12	0.048	20	4	J7, N7, R3	C, V	
TDC1112-3	12	0.012	50	4	J7, N7, R3	C	Signal synthesis D/A.
-2	12	0.024	50	4	J7, N7, R3	C, V, SMD	70 dBc SFDR. Very low glitch.
-1	12	0.048	50	4	J7, N7, R3	C, V, SMD	Drives 25Ω directly.
-	12	0.048	50	4	J7, N7, R3	C, V	ECL Interface.

Notes:
1. Guaranteed. See product specifications for test conditions.
2. A = High Reliability, T_C = -55°C to 125°C.
   C = Commercial, T_A = 0°C to 70°C.
   V = MIL-STD-883 Compliant, T_C = -55°C to 125°C.
   SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C.

DAC-08
8-Bit High Speed Multiplying D/A Converter

Description

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 ns settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications.

Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33 mW power consumption attainable at ±5.0V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications. Devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1.0 µs A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

Features

- Fast settling output current — 85 ns
- Full scale current pre-matched to ±1.0 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% max. over temperature range
- High output impedance and compliance — -10V to +18V
- Differential current outputs
- Wide range multiplying capability — 1.0 MHz bandwidth
- Low FS current drift — ±10 ppm/°C
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33 mW @ ±5.0V
- Low cost

Ordering Information

Part Number	Package	Operating Temperature Range	Non-linearity
DAC-08EN	N	0°C to +70°C	±0.19%
DAC-08CN	N	0°C to +70°C	±0.39%
DAC-08AD	D	-55°C to +125°C	±0.1%
DAC-08D	D	-55°C to +125°C	±0.19%
DAC-08D/883B	D	-55°C to +125°C	±0.19%
DAC-08AD/883B	D	-55°C to +125°C	±0.1%

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
N = 16-lead plastic DIP
D = 16- lead ceramic DIP

Absolute Maximum Ratings

(T_A = +25°C unless otherwise noted)

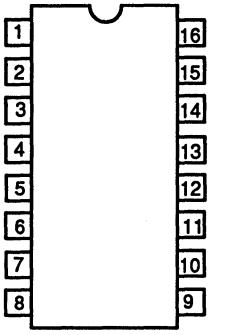
Supply Voltage (between $+V_S$ and $-V_S$) 36V
Logic Inputs ..... $-V_S$ to ($-V_S$ plus 36V)
Analog Current Outputs ..... 4 mA
Reference Inputs (V_{14} to V_{15}) ..... $-V_S$ to $+V_S$
Reference Input Differential
Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) ..... 5.0 mA
Operating Temperature Range
DAC-08AD, D ..... -55°C to +125°C
DAC-08EN, CN ..... 0°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Thermal Characteristics

	16-Lead Ceramic DIP	16-Lead Plastic DIP
Max. Junction Temp.	+175°C	+125°C
Max. P_D T_A <50°C	1042 mW	555 mW
Therm. Res θ_{JC}	60°C/W	—
Therm. Res. θ_{JA}	120°C/W	135°C/W
For T_A >50°C Derate at	8.38 mW/°C	7.41 mW/°C

Connection Information

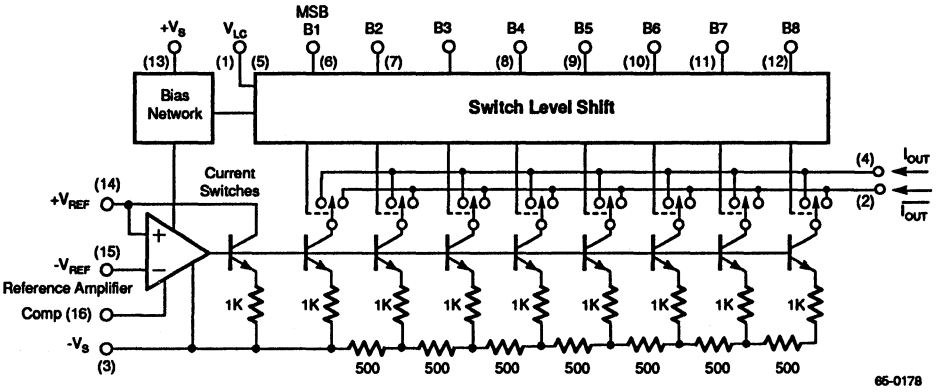
16-Lead
Dual-In-Line
(Top View)



65-0177

Pin	Function	Pin	Function
1	VLC Threshold Control	9	B5
2	I_{OUT}	10	B6
3	$-V_S$	11	B7
4	I_{OUT}	12	B8 (LSB)
5	B1 (MSB)	13	$+V_S$
6	B2	14	V_{REF} (+)
7	B3	15	V_{REF} (-)
8	B4	16	Compensation

Functional Block Diagram



Electrical Characteristics

(V_S = ±15V, I_{REF} = 2.0 mA, T_A = -55°C to +125°C for DAC-08 and DAC-08A; T_A = 0°C to +70°C for DAC-08C and DAC-08E unless otherwise specified. Output characteristics refer to both I_{OUT} and $I_{\overline{OUT}}$.)

Parameters	Test Conditions	DAC-08A			DAC-08			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Nonlinearity	Full Temperature Range			+0.1			+0.19	%FS
Settling Time	To +1/2LSB, All Bits Switched ON or OFF T_A = +25°C[1]		85	135		85	150	ns
Propagation Delay								
Each Bit	T_A = +25°C[1]		35	60		35	60	ns
All Bits Switched			35	60		35	60	
Full Scale Tempco			±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < 1/2 LSB R_{OUT} > 20 MΩ Typical	-10		+18	-10		+18	V
Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Scale Symmetry	$I_{FS} - I_{\overline{FS}}$		±0.5	±4.0		±1.0	±8.0	µA
Zero Scale Current			0.1	1.0		0.2	2.0	
Output Current Range	V_{REF} = +15V, $-V_S$ = -10V	2.1			2.1			mA
R_{14}, R_{15} = 5.000kΩ	V_{REF} = +25V, $-V_S$ = 12V	4.2			4.2			
Logic Input Levels								
Logic "0"	V_{LC} = 0V			0.8			0.8	V
Logic "1"		2.0			2.0			
Logic Input Current	V_{LC} = 0V							
Logic "0"	V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	µA
Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	
Logic Input Swing	$-V_S$ = -15V	-10		+18	-10		+18	V
Logic Threshold Range[1]	V_S = ±15V	-10		+13.5	-10		+13.5	
Reference Bias Current			-1.0	-3.0		-1.0	-3.0	µA
Reference Input Slew Rate[1]		4.0	8.0		4.0	8.0		mA/µs

Note:

1. Guaranteed by design, but not tested.

Electrical Characteristics (continued)

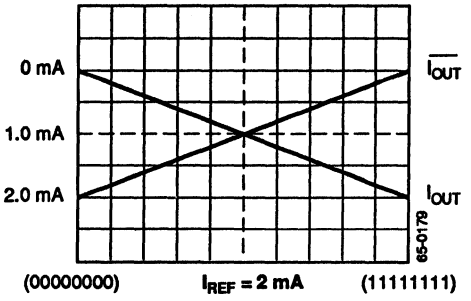
Parameters	Test Conditions	DAC-08A Min	DAC-08A Typ	DAC-08A Max	DAC-08 Min	DAC-08 Typ	DAC-08 Max	Units
Power Supply Sensitivity	$+V_S$ = 4.5V to 18V,							%ΔFS
Positive	$-V_S$ = -4.5V to -18V,		±0.0003	±0.01		±0.0003	±0.01	%ΔV
Negative	I_{REF} = 1.0 mA		±0.002	±0.01		±0.002	±0.01	%/%
Power Supply Current								
Positive	V_S = ±5.0V,		2.3	3.8		2.3	3.8	mA
Negative	I_{REF} = 1.0 mA		-4.3	-5.8		-4.3	-5.8	mA
Positive	V_S = +5.0V, -15V,		2.4	3.8		2.4	3.8	mA
Negative	I_{REF} = 2.0 mA		-6.4	-7.8		-6.4	-7.8	mA
Positive	V_S = ±15V		2.5	3.8		2.5	3.8	mA
Negative	I_{REF} = 2.0 mA		-6.5	-7.8		-6.5	-7.8	mA
Power Consumption	V_S = ±5.0V I_{REF} = 1.0 mA		33	48		33	48	mW
	V_S = +5.0V, -15V, I_{REF} = 2.0 mA		108	136		108	136	
	V_S = ±15V I_{REF} = 2.0 mA		135	174		135	174	

Parameters	Test Conditions	DAC-08E Min	DAC-08E Typ	DAC-08E Max	DAC-08C Min	DAC-08C Typ	DAC-08C Max	Units
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Nonlinearity	Full Temperature Range			+0.19			+0.39	%FS
Settling Time	To +1/2LSB, All Bits Switched ON or OFF T_A = +25°C[1]		85	150		85	150	ns
Propagation Delay								
Each Bit	T_A = +25°C[1]		35	60		35	60	ns
All Bits Switched			35	60		35	60	
Full Scale Tempco			±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < 1/2 LSB R_{OUT} > 20 MΩ Typical	-10		+18	-10		+18	V
Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FS4}-I_{FS2}		±1.0	±8.0		±2.0	±16.0	µA

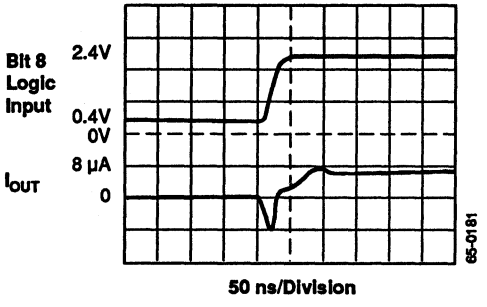
Electrical Characteristics (continued)

Parameters	Test Conditions	DAC-08E			DAC-08C			Units
		Min	Typ	Max	Min	Typ	Max	
Zero Scale Current			0.2	2.0		0.2	4.0	µA
Output Current Range	V_{REF} = +15V, $-V_S$ = -10V	2.1			2.1			mA
R_{14}, R_{15} = 5,000kΩ	V_{REF} = +25V, $-V_S$ = -12V	4.2			4.2			mA
Logic Input Levels								
Logic "0"	V_{LC} = 0V			0.8			0.8	V
Logic "1"		2.0			2.0			
Logic Input Current	V_{LC} = 0V							
Logic "0"	V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	µA
Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	
Logic Input Swing	$-V_S$ = -15V	-10		+18	-10		+18	V
Logic Threshold Range[1]	V_S = ±15V	-10		+13.5	-10		+13.5	V
Reference Bias Current			-1.0	-3.0		-1.0	-3.0	µA
Reference Input Slew Rate[1]		4.0	8.0		4.0	8.0		mA/µs
Power Supply Sensitivity	$+V_S$ = 4.5V to 18V							
Positive	$-V_S$ = -4.5V to -18V		±0.0003	±0.01		±0.0003	±0.01	%ΔFS
Negative	I_{REF} = 1.0 mA		±0.002	±0.01		±0.002	±0.01	%ΔV
Power Supply Current								
Positive	V_S = ±5.0V,		2.3	3.8		2.3	3.8	mA
Negative	I_{REF} = 1.0 mA		-4.3	-5.8		-4.3	-5.8	
Positive	V_S = +5.0V, -15V,		2.4	3.8		2.4	3.8	mA
Negative	I_{REF} = 2.0 mA		-6.4	-7.8		-6.4	-7.8	
Positive	V_S = ±15V		2.5	3.8		2.5	3.8	mA
Negative	I_{REF} = 2.0 mA		-6.5	-7.8		-6.5	-7.8	
Power Consumption	V_S = ±5.0V, I_{REF} = 1.0 mA		33	48		33	48	mW
	V_S = +5.0V, -15V, I_{REF} = 2.0 mA		103	136		108	136	mW
	V_S = ±15V, I_{REF} = 2.0 mA		135	174		135	174	mW

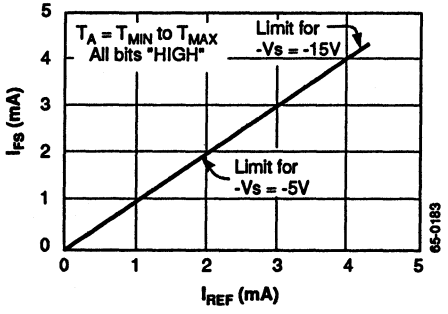
Typical Performance Characteristics



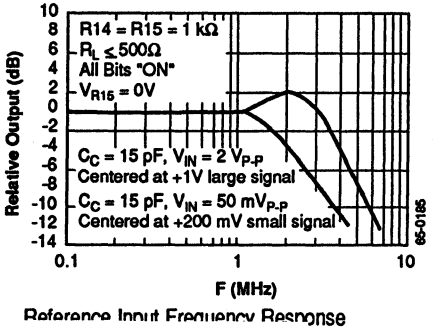
True and Complementary Output Operation



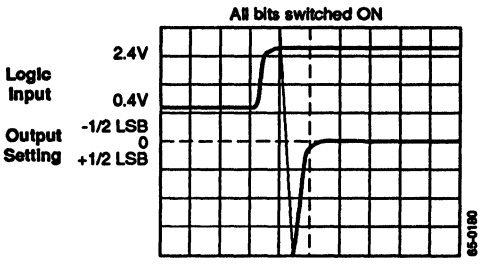
LSB Switching



Full Scale Output Current vs. Reference Current

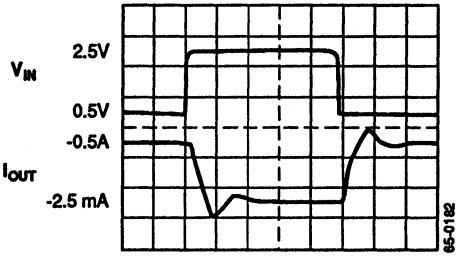


Reference Input Frequency Response



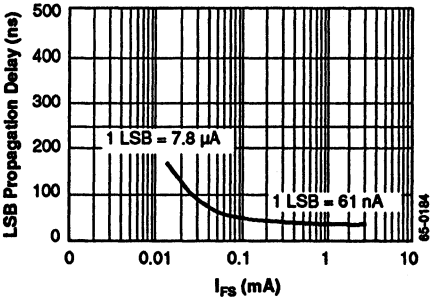
I_{FS} = 2 mA
R_L = 1 kΩ
1/2 LSB = 4 µA

Full Scale Settling Time



R_{EQ} (Input) = 200Ω
R_L = 100Ω
C_C = 0
R_{IN} = 5K
$+V_{IN}$ = 10V

Fast Pulsed Reference Operation



LSB Propagation Delay vs. Full Scale Output Current

Applications Information

Reference Amplifier Set-up

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or vary from nearly zero to +4.0 mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \quad X\ I_{REF} \text{ where } I_{REF} = I_{14}$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to VREF(-) at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (normally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common mode range of the reference amplifier is given by: $V_{CM^-} = -V_S$ plus (I_{REF} x 1 kΩ) plus 2.5V. The positive common mode range is $+V_S$ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1 µF capacitor.

For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2 mA to +4.0 mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to $-V_S$. For fixed reference operation, a 0.01 µF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

Multiplying Operation

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4.0 µA to 4.0 mA. Monotonic operation is maintained over a typical range of I_{REF} from 100 µA to 4.0 mA.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to $-V_S$. The value of this capacitor depends on the impedance presented to pin 14; for R_{14} values of 1.0, 2.5, and 5.0 kΩ, minimum values of C_C are 15, 37, and 75 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1.0 kΩ and C_C = 15 pF, the reference amplifier slews at 4.0 mA/µs enabling a transition from I_{REF} = 0 to I_{REF} = 2.0 mA in 500 ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2.0 mA) occurs in 120 ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16 mA/µs which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2.0 µA logic input current and completely adjustable logic threshold voltage. For $-V_S$ = -15V, the logic inputs may swing between -10V and +18V. This enables direct interface with +5V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: $-V_S$ plus (I_{REF} x 1.0 kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range

by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). V_{TH} is nominally 1.4V above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL an I_{REF} = 1.0 mA is recommended. For general setup of the logic control circuit, it should be noted that pin 1 will source or sink 100 µA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1.0 kΩ divider, for example, it should be bypassed to ground by a 0.01 µF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided where $I_{OUT} + \overline{I_{OUT}} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_{OUT}}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above $-V_S$ and is independent of the positive supply. Negative compliance is given by $-V_S$ plus (I_{REF} x 1.0 kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection, and other balanced applications such as driving center-tapping coils and transformers.

Power Supplies

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5.0V or less, $I_{REF} \leq 1.0$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required. However, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows: $Pd = (I+)(+V_S) + (I-)(-V_S) + (2\ I_{REF})(-V_S)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power bypass capacitors.

Temperature Performance

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is typically ±10 ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at -55°C; at +125°C an increase of about 15% is typical.

Typical Applications

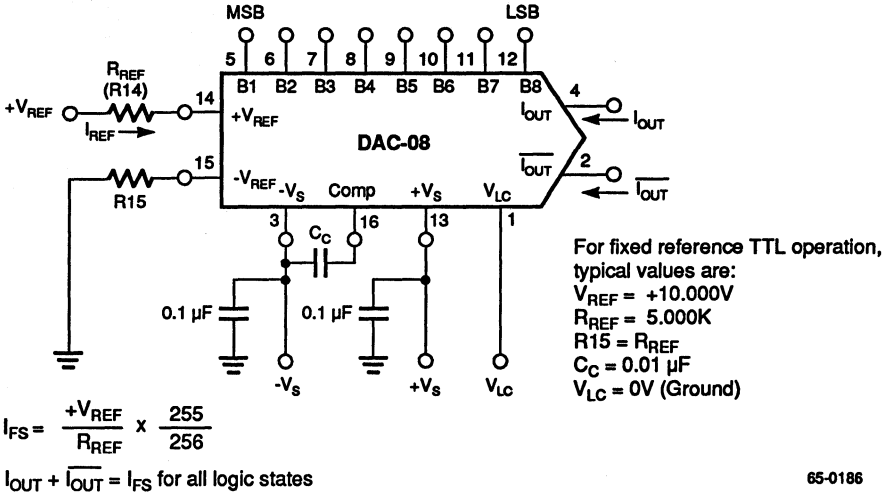


Figure 1. Basic Positive Reference Operation

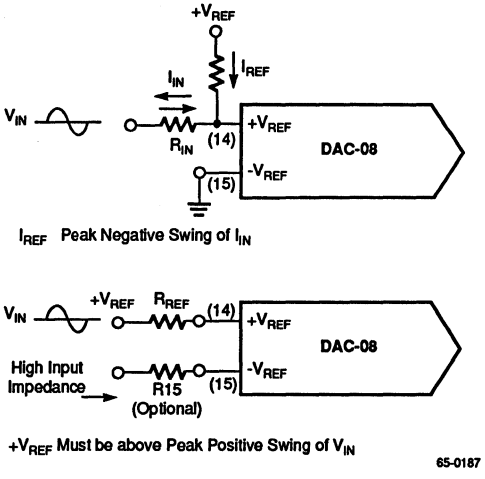


Figure 2. Accommodating Bipolar References

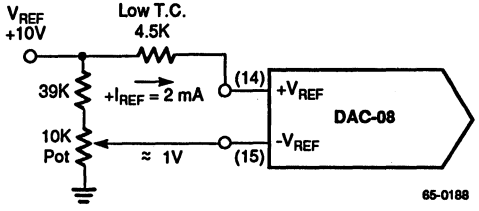


Figure 3. Recommended Full Scale Adjustment Circuit

Typical Applications (Continued)

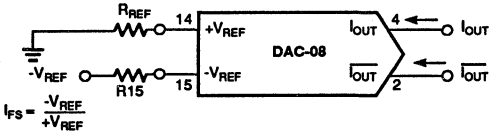
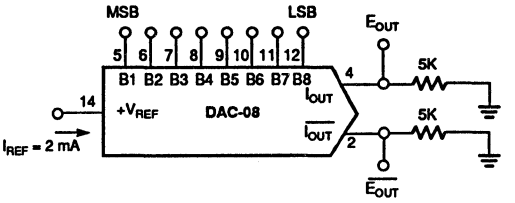


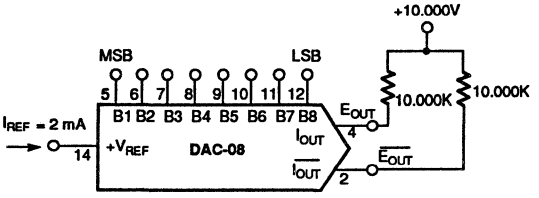
Figure 4. Basic Negative Reference Operation



Scale	B1	B2	B3	B4	B5	B6	B7	B8	I_{OUT}mA	$\overline{I_{OUT}}$mA	E_{OUT}	$\overline{E_{OUT}}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	-9.660	-0.000
Half Scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

65-0190

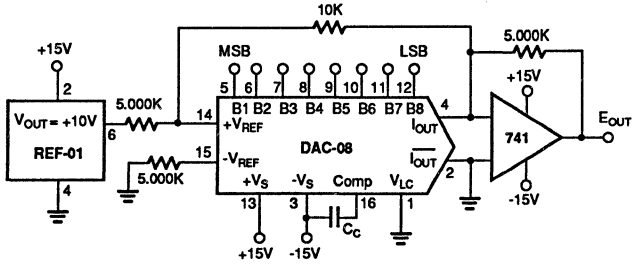
Figure 5. Basic Unipolar Negative Operation



Scale	B1	B2	B3	B4	B5	B6	B7	B8	E_{OUT}	$\overline{E_{OUT}}$
Pos Full Scale	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos Full Scale - LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale - LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920

65-0191

Figure 6. Basic Bipolar Output Operation

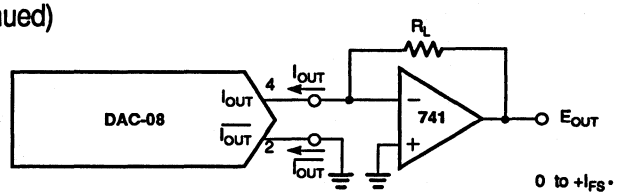


Scale	B1	B2	B3	B4	B5	B6	B7	B8	E_{OUT}
Pos Full Scale	1	1	1	1	1	1	1	1	+4.960
Zero Scale	1	0	0	0	0	0	0	0	0.000
Neg Full Scale + 1 LSB	0	0	0	0	0	0	0	1	-4.960
Neg Full Scale	0	0	0	0	0	0	0	0	-5.000

65-0192

Figure 7. Offset Binary Operation

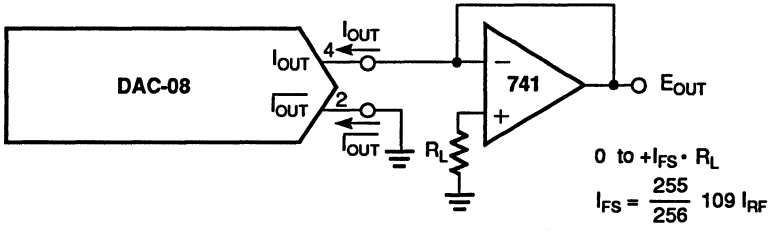
Typical Applications (Continued)



For complementary output (operation as a negative logic (DAC) connect inverting input of op amp to $\overline{I_{OUT}}$ (pin 2) ; connect I_{OUT} (pin 4) to ground.

65-0193

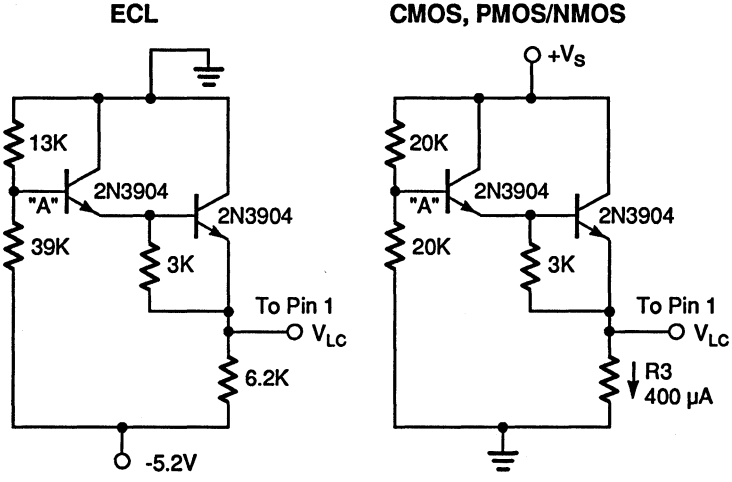
Figure 8. Positive Low Impedance Output Operation



For complementary output (operation as a negative logic (DAC) connect inverting input of op amp to $\overline{I_{OUT}}$ (pin 2) ; connect I_{OUT} (pin 4) to ground.

65-0194

Figure 9. Negative Low Impedance Output Operation



Temperature Compensating V_{LC} Circuits

65-0195

Figure 10. Interfacing With Various Logic Families

Settling Time

The DAC-08 is capable of extremely fast settling times, typically 85 ns at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 ns for each of the 8 bits. Settling time to within 1/2 LSB is therefore 35 ns, with each progressively larger bit taking successively longer. The MSB settles in 85 ns, thus determining the overall settling time of 85 ns. Settling to 6-bit accuracy requires about 65 to 70 ns. The output capacitance of the DAC-08 including the package is approximately 15 pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0 mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output R_C time constant.

Measurement of settling time requires the ability to accurately resolve ±4.0 µA, therefore a 1.0 kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture uses a cascade design to permit driving a 1.0 kΩ load with less than 5.0 pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0 mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}..

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic state: 0.1 µF capacitors at the supply pins provide full transient protection.

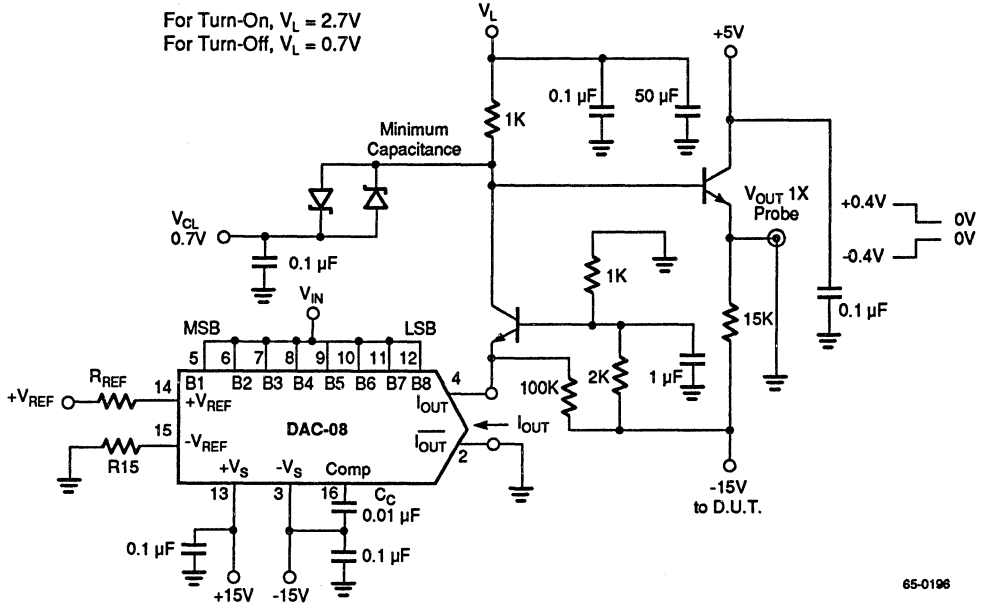


Figure 11. Settling Time Test Fixture

TDC1012
Monolithic Digital-to-Analog Converter
12-Bit, 20 Msps

Description

The TDC1012 is a TTL compatible, 12-bit monolithic D/A converter capable of converting digital data into an analog current or voltage at data rates in excess of 20 Megasamples per second (Msps).

The analog performance has been optimized for dynamic performance, with very low glitch energy. The dual outputs are able to drive 50Ω load with 1 Volt output levels while keeping a spurious-free-dynamic range greater than 70 dB.

Data registers are incorporated on the TDC1012. This eliminates the temporal data skew encountered with external registers and latches and minimizes the glitches that can adversely affect performance in many applications.

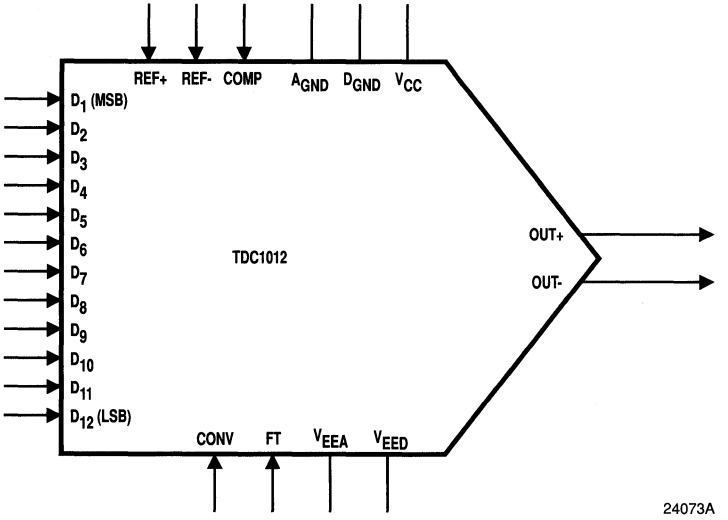
Features

- 12-bit resolution
- 20 Msps data rate
- TTL inputs
- Very low glitch with no Track-and-Hold circuit needed
- Dual +4 dBm (1V into 50Ω) outputs make output amplifiers unnecessary in many applications
- 70 dB typical spurious-free dynamic range
- Available compliant to MIL-STD-883

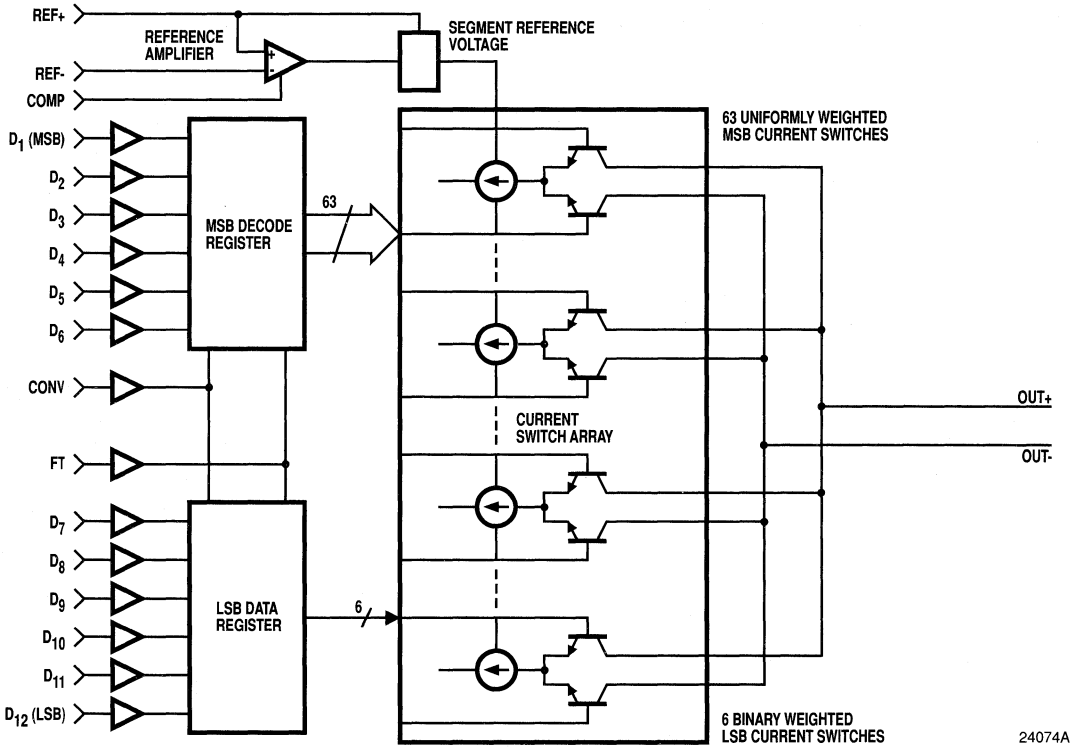
Applications

- Direct digital RF signal generation
- Test signal generation
- Arbitrary waveform synthesis
- Broadcast and studio video
- High-resolution A/D converters

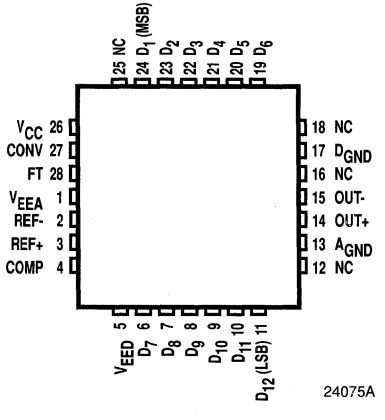
Interface Circuit



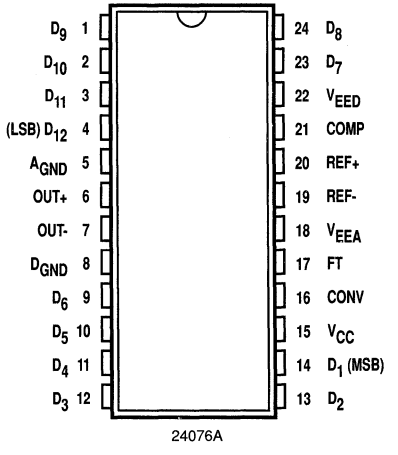
Functional Block Diagram



Pin Assignments



28 Contact Chip Carrier-C3 Package
28 Leaded Plastic Chip Carrier-R3 Package



24 Pin Hermetic Ceramic DIP-J7 Package
24 Pin Plastic DIP-N7 Package

Functional Description

General Information

The TDC1012 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

There are three major D/A architectures: segmentated, weighted current sources, and R-2R. In segmentated converters there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N-1 current sources. A weighted current source D/A has one current source for each input bit, and a binary weighting for the current sources. In an R-2R D/A, there is one current source per bit and a resistor network which scales the current sources to have a binary weighting. When transitioning from a code of 011111111111 to 100000000000, both the R-2R D/A and Binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where too many current sources are either on or off, resulting in a glitch. In a segmented architecture, 2047 of the current sources remain on, and one more is turned on to increment the output - no possibility of a glitch.

The TDC1012 uses an architecture with the 6 MSBs segmented and the 6 LSBs form a R-2R network. The result is a D/A converter which has very low-glitch energy, and a moderate die size.

Power, Grounds

The TDC1012 requires a –5.2V power supply and a +5.0V power supply. The analog (V_{EEA}) and digital (V_{EED}) supply voltages should be decoupled from each other, as shown in the ***Typical Interface Circuits***. The V_{CC} pin should be considered a digital power supply. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The inductors are simple ferrite beads and are neither critical in value nor always required.

Reference

The TDC1012 has two reference inputs: REF+ and REF–. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF– pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT} = N \times \frac{I_{REF}}{64}$$

Where N is the value of the input code

This means that with an I_{REF} that is nominally 625µA, the full scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω total load) with a 1V peak to peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so the effect of amplifier input bias current is minimized. The TDC1012 has been optimized to operate with a reference current of 625µA. Significantly increasing or decreasing this current may degrade the performance of the device.

The minimum and maximum values for V_{REF} and I_{REF} are listed in the table of ***Operating conditions***. The internal reference amplifier is externally compensated to assure stability. To compensate this amplifier, a 0.1µF capacitor should be connected between the COMP pin and V_{EEA}. The amplifier has been optimized to minimize the settling time, and as a result should be considered a DC amplifier. Performance of the TDC1012 operating in a multiplying D/A mode is not guaranteed.

Stable, adjustable reference circuits are shown in the *Typical Interface Circuits*, *5*, *6* and *7*.

Digital Inputs

The data inputs are TTL compatible. The TDC1012 is specified with two sets of setup and hold times. One of these pairs of specifications guarantees the performance of the TDC1012 to specifications listed in the ***Minimum*** and ***Maximum*** columns of the ***System performance characteristics*** table.

The second more rigid specification is recommended for applications where lowest possible glitch and highest SFDR are desired. The more stringent t_S and t_H ensure that the data will not be slewing during times critical to the TDC1012, and will minimize the effects of capacitively coupled data feedthrough and optimize SFDR performance.

Another method for reducing the effect of capacitive coupling is to slow down the slew rates of the digital inputs. This has been done in the circuit shown in the *Typical Interface Circuits* by the addition of 50Ω series resistors to the data lines.

Clock and Feedthrough Control

The TDC1012 requires a TTL clock signal (CONV) Data is synchronously entered on the rising edge of CONV. The CONV input is ignored in the Feedthrough (FT = HIGH) mode. The Feedthrough (FT) pin is normally held LOW, where the TDC1012 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided,and this pin may be left open for clocked operation.

For certain applications, such as high-precision successive approximation A/D converters, throughput delay may be more important then glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronously in response to the digital inputs.

Since skew in the bits of the input word will result in glitches, and will affect settling time, it is recommended that the TDC1012 be operated in clocked mode for most applications.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By driving the current source outputs into a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to –40mA output current (0 to –1V when terminated in 25Ω) as the input code varies from 0000 0000 0000 to 1111 1111 1111. OUT– varies in a complementary manner from –40 to 0mA (–1 to 0V when terminated with 25Ω) over the same code range. (See the *Input Coding Table*.)

The output current is proportional to the reference current and the input code. The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a terminated 50Ω transmission line. With this load, the output voltage range of the converter is 0 to –1.0V.

If a load is capacitively coupled to the TDC1012, it is recommended that a 25Ω load at DC, as seen by the TDC1012, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the *Electrical characteristics table*, or the accuracy may be impaired.

Package Interconnections

Signal Type	Signal Name	Function	Value	J7 & N7 Package Pins	C3 & R3 Package Pins
Power	V_{CC}	Digital Supply Voltage	+5.0V	15	26
	A_{GND}	Analog Ground	0.0V	5	13
	D_{GND}	Digital Ground	0.0V	8	17
	V_{EEA}	Analog Supply Voltage	–5.2V	18	1
	V_{EED}	Digital Supply Voltage	–5.2V	22	5
Reference	REF–	Reference Voltage Input	–1.0V	19	2
	REF+	Reference Current Input	625µA	20	3
	COMP	Compensation Capacitor	0.1µF, see text	21	4
Data Inputs	D_1 (MSB)	Most Significant Bit	TTL	14	24
	D_2		TTL	13	23
	D_3		TTL	12	22
	D_4		TTL	11	21
	D_5		TTL	10	20
	D_6		TTL	9	19
	D_7		TTL	23	6
	D_8		TTL	24	7
	D_9		TTL	1	8
	D_{10}		TTL	2	9
	D_{11}		TTL	3	10
	D_{12} (LSB)	Least Significant Bit	TTL	4	11
Feedthrough	FT	Feedthrough Mode Control	TTL	17	28
Convert	CONV	Convert (Clock) Input	TTL	16	27
Analog Output	OUT+	Analog Output	0 to 40mA	6	14
	OUT–	Analog Output	40 to 0mA	7	15

Input Coding Table[1]

Input Data MSB LSB	OUT+ (mA)	V_{OUT+}(mV)	OUT– (mA)	V_{OUT-}(mV)
0000 0000 0000	0.000	0.00	40.000	–1000.00
0000 0000 0001	0.009	–0.24	39.990	–999.75
0000 0000 0010	0.019	–0.49	39.980	–999.52
	•	•	•	•
	•	•	•	•
	•	•	•	•
	•	•	•	•
0111 1111 1111	19.995	–499.88	20.005	–500.12
1000 0000 0000	20.005	–500.12	19.995	–499.88
	•	•	•	•
	•	•	•	•
	•	•	•	•
1111 1111 1101	39.980	–999.52	0.019	–0.49
1111 1111 1110	39.990	–999.75	0.009	–0.24
1111 1111 1111	40.000	–1000.00	0.000	0.0

Note: 1. I_{REF} = 625µA, R_{LOAD} = 25Ω

Figure 1. Timing Diagram

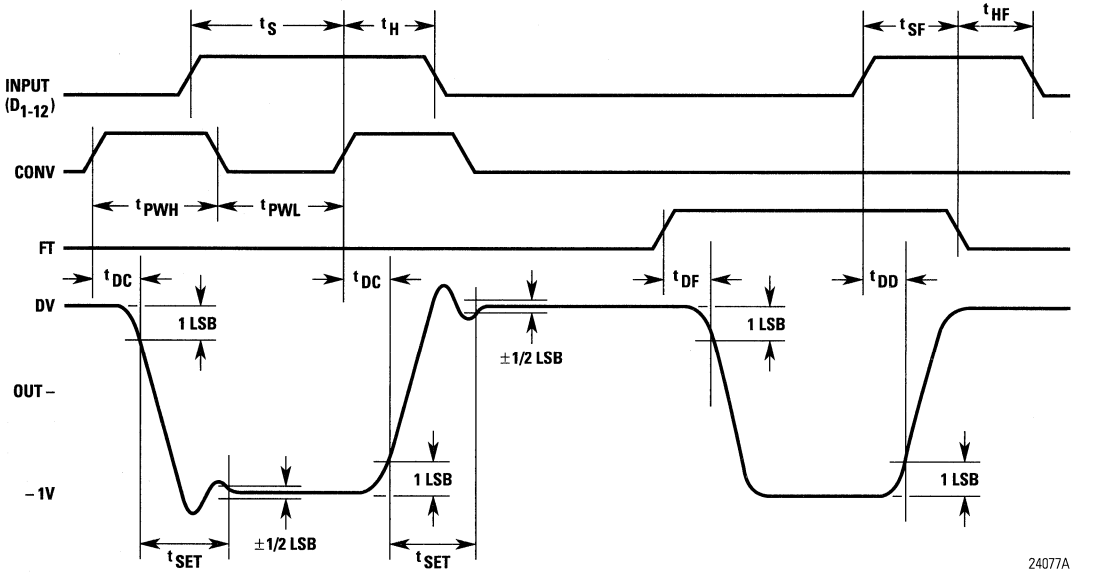


Figure 2. Equivalent Input Circuits

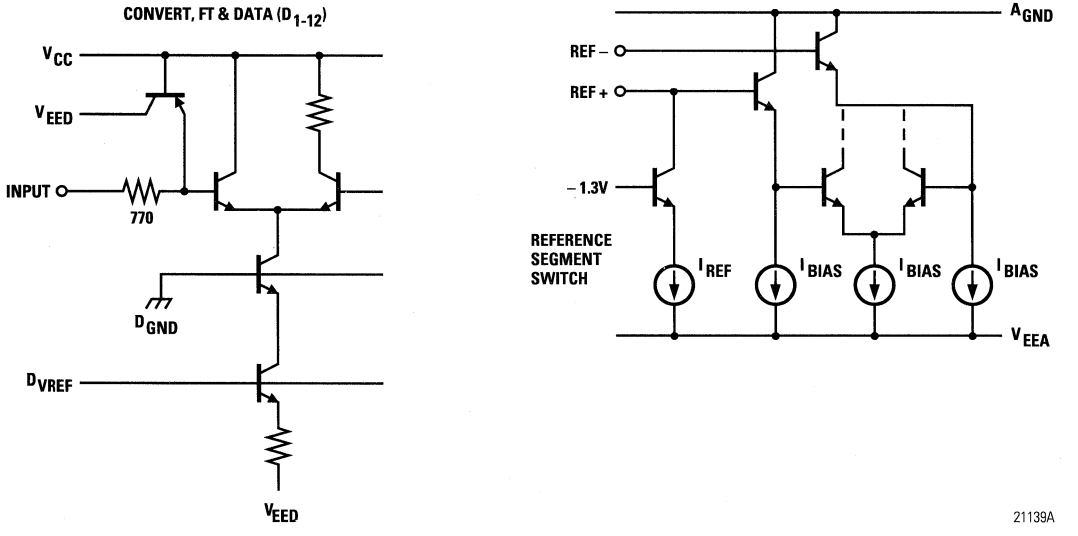


Figure 3. Equivalent Reference and Output Circuits

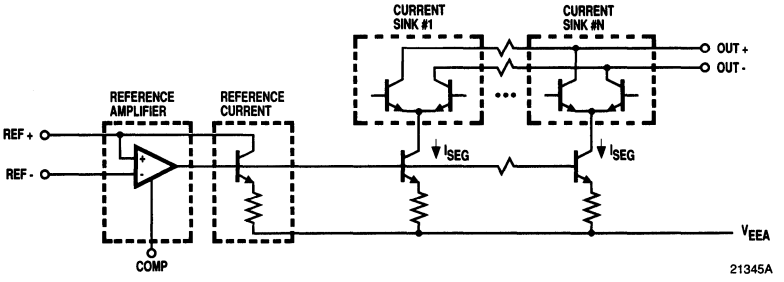
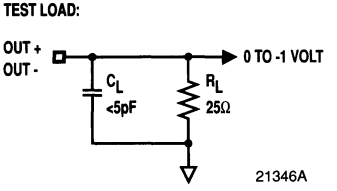


Figure 4. Output Test Load



D/A

Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{CC}	(Measured to D_{GND})	–0.5 to +7.0V
V_{EEA}	(Measured to A_{GND})	–7.0 to +0.5V
V_{EEA}	(Measured to V_{EED})	–50 to +50mV
V_{EED}	(Measured to D_{GND})	–7.0 to +0.5V
A_{GND}	(Measured to D_{GND})	–0.5 to +0.5V

Inputs

CONV, FT, D_{1-12} (Measured to D_{GND})[2]	V_{CC} +0.5 to –0.5V
CONV, FT, D_{1-12} Current, Externally Forced[3]	±3mA
REF+, REF–, Applied Voltage (Measured to A_{GND})[3]	V_{EEA} to +0V
REF+, REF–, Current, Externally Forced[3]	±3mA

Outputs

OUT+, OUT–, Applied Voltage (Measured to A_{GND})[2]	–2.0 to +2.0V
OUT+, OUT–, Current, Externally Forced[3]	+50mA
Short-Circuit Duration (Single Output to GND)	unlimited

Temperature

Operating, Ambient	
(Plastic Package)	–20 to +90°C
(Ceramic Package)	–60 to +150°C
Junction	
(Plastic Package)	+140°C
(Ceramic Package)	+200°C
Lead, soldering (10 seconds)	+300°C
Storage	–65 to +150°C

Note: 1. Absolute maximum ratings are limited values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.

2. Applied voltage must be current limited to specified range.

3. Forcing voltage must be limited to specified range. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EED}	Negative Supply Voltage (Measured to D_{GND})	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{EEA}	Negative Supply Voltage (Measured to A_{GND})	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{EEA}	Negative Supply Voltage (Measured to V_{EED})	–20	0	20	–20	0	20	mV
t_{PWL}	CONV Pulse Width LOW (to Meet Specification)	20			20			ns
t_{PWL}	CONV Pulse Width LOW (to Optimize SFDR)	20			20			ns
t_{PWH}	CONV Pulse Width HIGH (to Meet Specifications)	20			20			ns
t_{PWH}	CONV Pulse Width HIGH (to Optimize SFDR)	20			20			ns
t_S	Setup Time, Data to CONV (to Meet Specification)	25			25			ns
t_S	Setup Time, Data to CONV (to Optimize SFDR)	32			36			ns
t_H	Hold Time (to Meet Specifications)	1			1			ns
t_H	Hold Time (to Optimize SFDR)	4			6			ns
t_{SF}	Setup Time, Data to FT	5			7			ns
t_{HF}	Hold Time, Data to FT	28			32			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
V_{REF}	Reference Voltage (REF–)	–0.7	–1.0	–1.3	–0.7	–1.0	–1.3	V
I_{REF}	Reference Current (REF+)	550	625	700	575	625	675	µA
C_C	Compensation Capacitor	0.01	0.1		0.01	0.1		µF
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				–55		125	°C

Notes: 1. A common power supply isolated with ferrite bead inductors is recommended for V_{EEA} and V_{EED}. This is shown in the *Typical Interface Circuits*.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
$I_{EEA}+I_{EED}$		$V_{EEA}=V_{EED}$=Max,static					
		T_A=0 to 70°C		–180			mA
		T_A=70°C		–150			mA
		T_C=–55 to 125°C				–200	mA
		T_C=125°C				–150	mA
I_{CC}		V_{CC}=Max, Static		25			mA
		T_A=0 to 70°C					
		T_A=70°C		20			mA
		T_C=–55 to 125°C				35	mA
		T_C=125°C				24	mA
C_{REF}	Reference Input Capacitance			15		15	pF
C_I	Digital Input Capacitance			15		15	pF
V_{OC}	Compliance Voltage		–1.2	1.2	–1.2	1.2	V
R_O	Output Resistance		12		12		kΩ
C_O	Output Capacitance			45		45	pF
I_O	Full Scale Output Current	I_{REF}=Nominal	40		40		mA
I_{IL}	Input Current, Logic LOW	V_{CC}, V_{EE}=Max , V_I=0.4V	–10	50	–10	50	µA
I_{IH}	Input Current, Logic HIGH	V_{CC}, V_{EE}=Max, V_I=2.4V	–10	100	–10	100	µA
I_{IM}	Input Current, Max Input Voltage	V_{CC}, V_{EE}=Max, V_I=V_{CC} Max	–10	100	–10	100	µA
V_{TH}	Logic Input Threshold Voltage,Typical	V_{CC}, V_{EE}=Nom, T_A=25°C	1.25	1.55	1.25	1.55	V

Switching characteristics

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
F_D	Maximum Data Rate	V_{EEA}, V_{EED}, V_{CC} = Min	20	25		20	23		MHz
t_{DC}	Clock to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min, F T =LOW			17			20	ns
t_{DD}	Data to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min, FT = HIGH			35			40	ns
t_{DF}	FT to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min			35			40	ns
t_R	Risetime	90% to 10% of FSR, FT = LOW			4			4	ns
t_F	Falltime	10% to 90% of FSR, FT = LOW			4			4	ns
t_{SET}	Settling Time, Voltage	FT = LOW, Full-Scale Voltage Transition on I_{OUT} to ±0.0188% FSR		20	30		20	35	ns

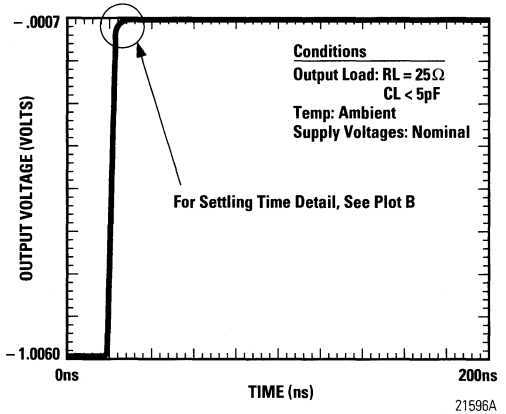
System performance characteristics

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
E_{LD}	Differential Linearity Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[1]							
		TDC1012XXY3			±0.012			±0.012	%
		TDC1012XXY2			±0.024			±0.024	%
		TDC1012XXY1			±0.048			±0.048	%
E_{LI}	Integral Linearity Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[1]							
		TDC1012XXY3			±0.024			±0.024	%
		TDC1012XXY2			±0.048			±0.048	%
		TDC1012XXY1			±0.048			±0.048	%
V_{OS}	REF+ to REF– Offset Voltage		–10		+10	–10		+10	mV
I_B	REF– Input Bias Current				5			10	µA
E_G	Absolute Gain Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom	–5		5	–5		5	%
I_{OF}	Output Offset Current	V_{EEA}, V_{EED}, V_{CC}= Min, D_{1-12}=LOW	–5		+5	–5		+5	µA
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[2]			–50			–48	dB
PSS	Power Supply Sensitivity	V_{CC}, V_{EEA}, V_{EED}=4%, I_{REF}=Nom			–140			–140	µA/V
G_A	Peak Glitch Area			25	45		25	45	pV–sec
SFDR	Spurious Free Dynamic Range	I_{REF}=Nom, 20Msps, 10MHz bandwidth	60			60			dBc
		F_{out}=6MHz							
		F_{out}=5MHz		70					dBc
		F_{out}=2MHz		75					dBc
		F_{out}=1MHz		78					dBc

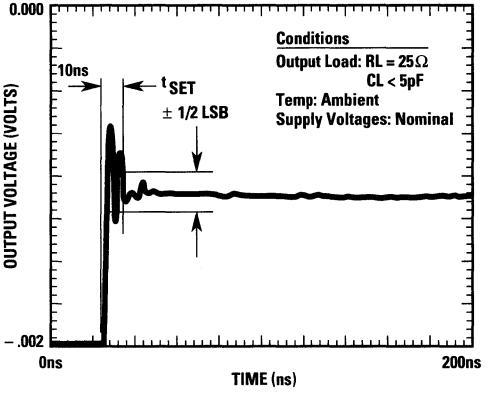
Notes: 1. OUT– connected to A_{GND}, OUT+ driving virtual ground.
2. 120 Hz, 600 mV p-p ripple on V_{EE} and V_{CC}.

Typical Performance Curves (Typical Settling Time Characteristics)

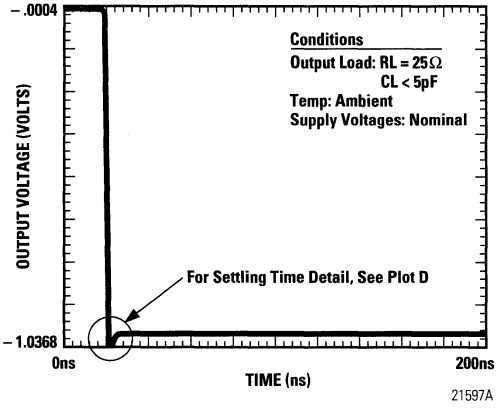
A. Full-Scale Output Transition, Rising Edge



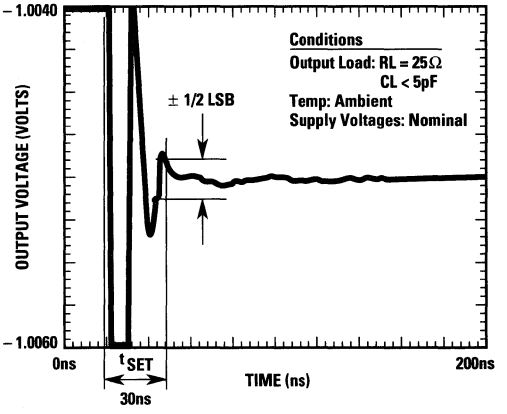
B. Settling Time, Full-Scale Output, Rising Edge



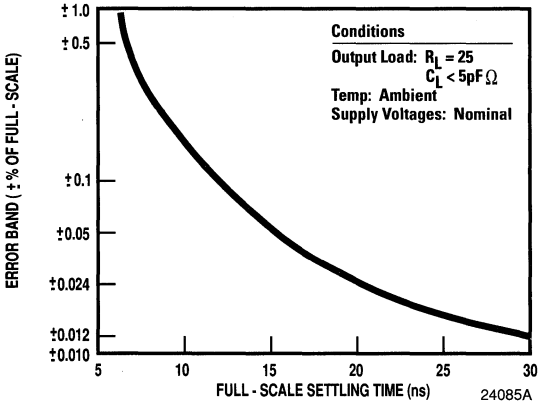
C. Full-Scale Output Transition, Falling Edge



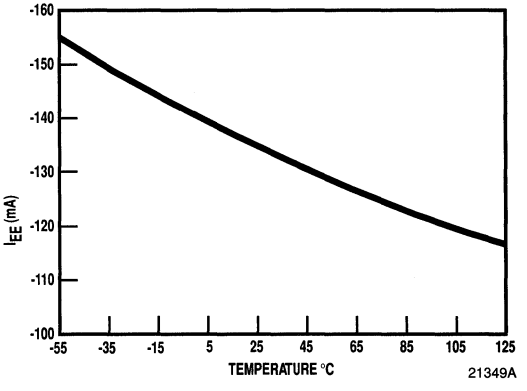
D. Settling Time, Full-Scale Output, Falling Edge



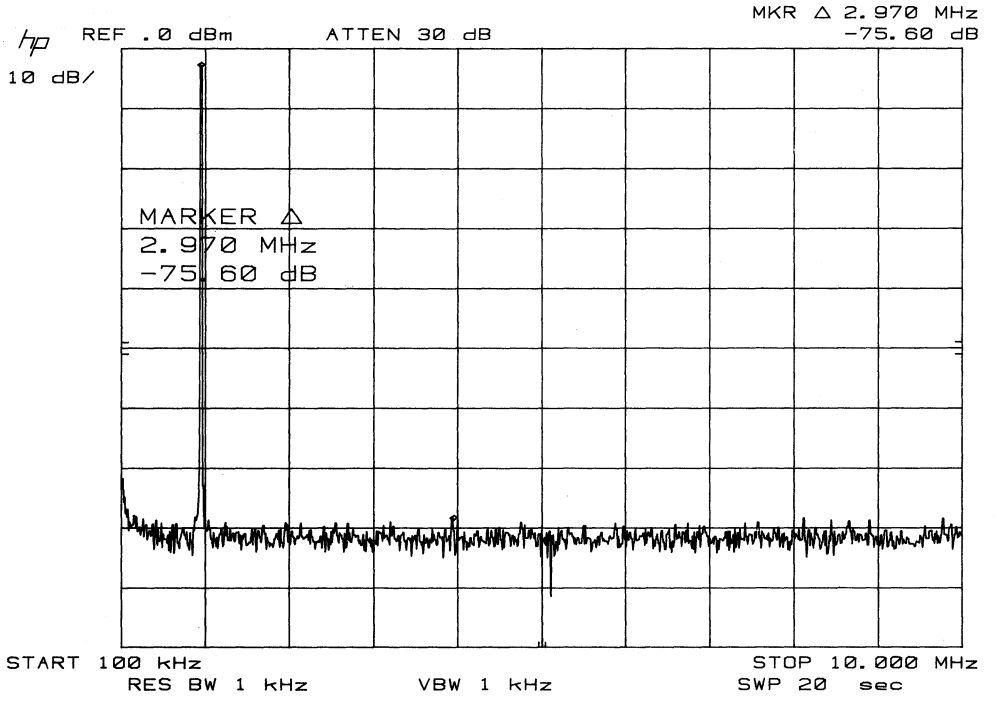
E. Typical Settling Time vs. Settling Accuracy



F. Typical Supply Current vs. Temperature



G. Typical Output Spectrum 20Msps 1MHz F_{OUT}



Applications Discussion

The TDC1012 is a high performance D/A converter. To get the best possible performance requires careful attention to the details of circuit design and layout.

Layout

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided at the TDC1012. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1012 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1 Volts.

The high slew-rates of digital data make capacitive coupling with the D/A output a potential problem. Since the digital signals contain high-frequency harmonics of the clock, as well as the signal that is being provided to the TDC1012, the result of data feedthrough often looks like harmonic distortion which degrades the Spurious-Free-Dynamic-Range (SFDR) performance of the D/A. Capacitive coupling can be minimized by keeping digital lines physically away from the analog output and reference. Another technique that can reduce capacitive data coupling is to use low slew rate digital drive circuits or slowing the driving edges with series resistors.

Direct Digital Synthesis Applications

For most synthesis applications, optimum signal purity is obtained with the use of a balun (a simple RF transformer made by wrapping a few turns of wire around a ferrite core) as shown in ***Figure 5***. This configuration has the benefit of canceling common mode distortion. An output

amplifier is not recommended because any amplifier will add distortion, which is likely to be much greater than that present from the outputs of the TDC1012.

The strict adherence to at least the minimum input data setup and hold times is important for the realization of the optimal performance. Spur levels may decrease as setup and hold times are increased. It is possible to achieve even higher performance in some instances by carefully "tuning" the input data setup and hold times (slightly delaying or advancing the CONV signal in relation to the data) provided to the TDC1012. The ***Operating conditions*** table has two sets of data for t_S and t_H, one which guarantees performance of the device in most applications, and one, more conservative specification, which has been found to be optimal for DDS applications.

The actual digital-data waveform which represents a sinewave contains strong harmonics of that fundamental frequency. This can be seen by connecting a digital data line to the input of a spectrum analyzer. Data feedthrough to the analog output of a system due to improper board layout or system shielding and grounding will appear as additional harmonic distortion, adversely affecting SFDR.

Harmonic distortion may improve even further with reduced AC termination impedance values, at the expense of lowered output voltage. This is achieved by a balun used as an impedance transformer as shown in ***Figure 5***.

The purity of the output of the TDC1012 is greater than that which can be measured by many spectrum analyzers. The spectral plots shown in this data sheet were generated with an HP8568B, which has a noise floor just below that of the TDC1012. When making spectral measurements it is important to remember that the TDC1012 output power is +4dBm, which is greater power than many analyzers are equipped to handle without adding distortion of their own. Accordingly, it may be necessary to introduce an attenuator to the input of the spectrum analyzer.

The CONV signal provided to the TDC1012 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory.

The TMC2340 direct digital synthesizer is ideal for generating a digital sinusoid for the D/A converter. The TMC2340 automatically generates a carrier frequency which may then be digitally phase, frequency or amplitude modulated. Two outputs are provided which are 90° out of phase (quadrature outputs). For more information on direct digital synthesis, and other applications of the TDC1012, please see application note ***TP46*** and ***AB-8*** from TRW LSI Products.

Bipolar Output

See ***Figure 6*** for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output, either with a balun or an operational amplifier in the differential mode. If it is desired that the TDC1012 be operated in a single-ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 7***.

Figure 5. Typical Interface Circuit with Balun Output

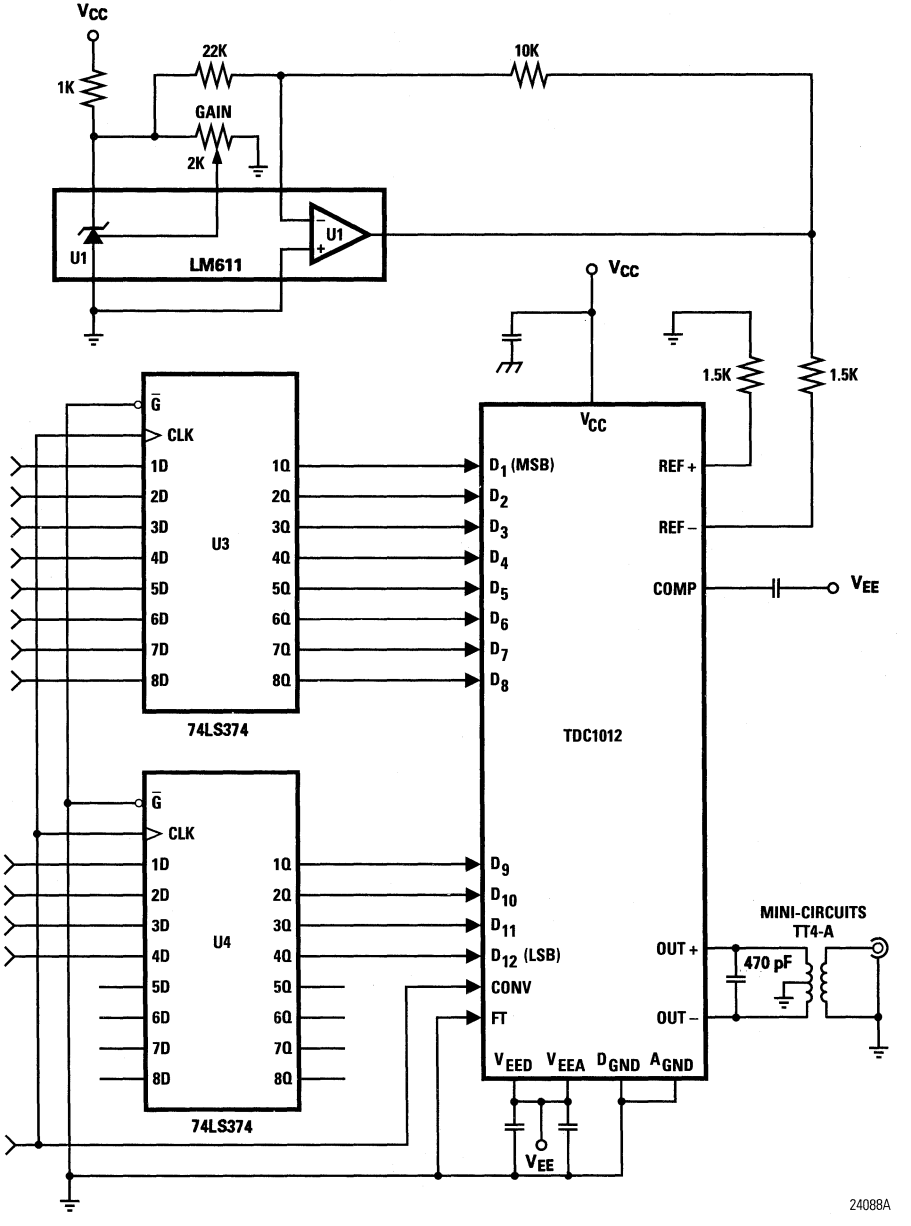


Figure 6. Typical Interface Circuit with Differential Amplifier Output

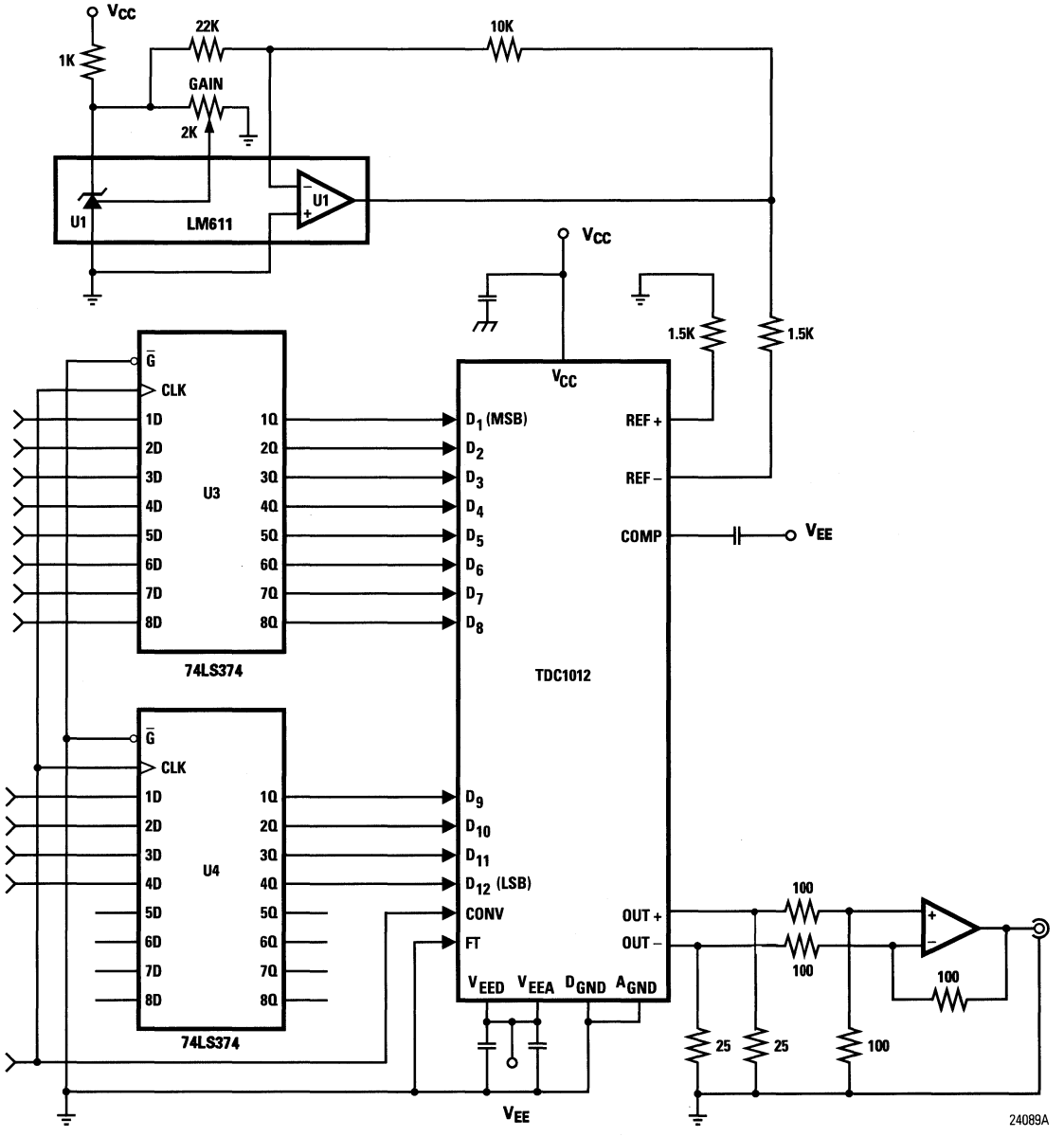
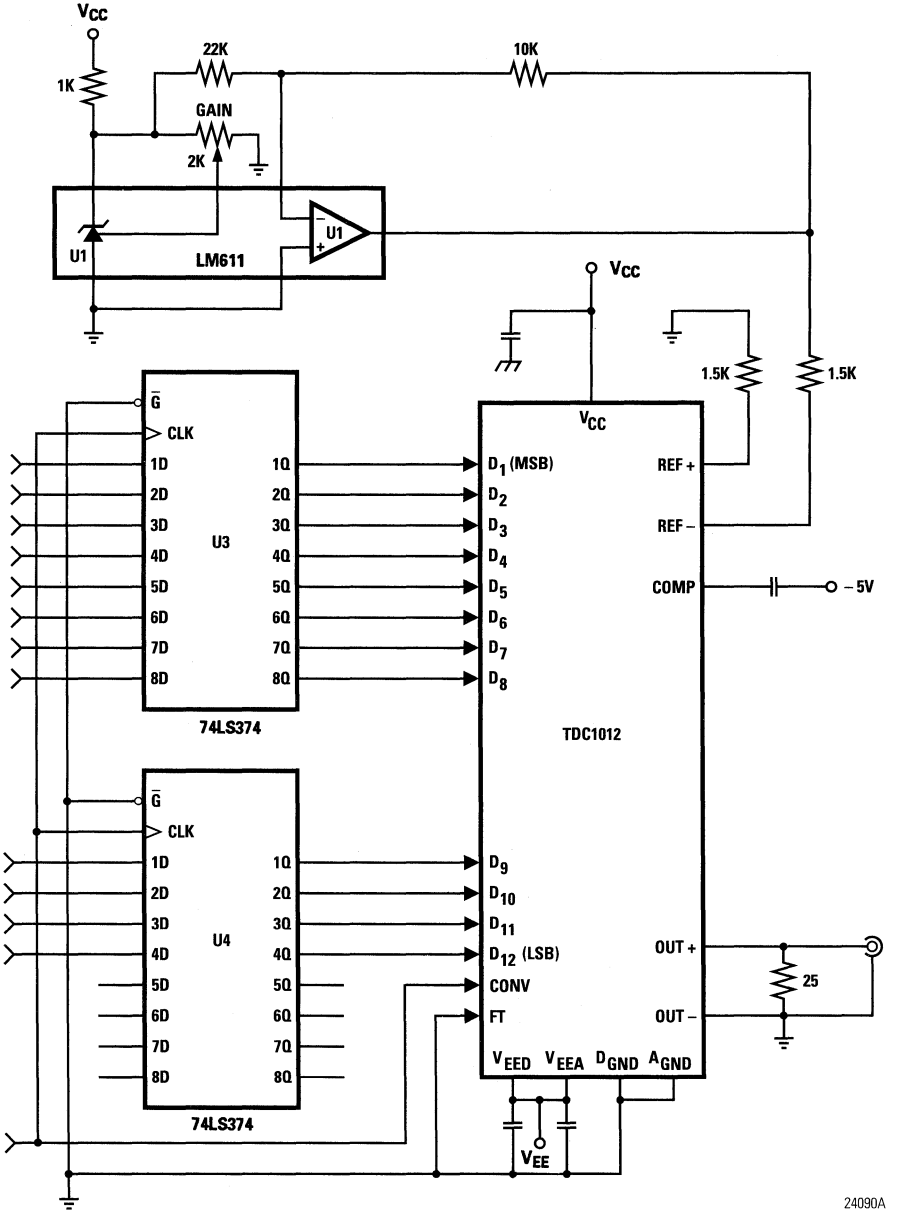


Figure 7. Typical Interface Circuit with Resistive Load Output



Using the TDC1012 and TDC1112 in Sinusoidal Synthesis Applications

In the past, most waveform synthesis was performed using analog oscillators, with their problems of drift, limited versatility, and design complexity. However, as the cost of high-performance digital circuits and digital-to-analog converters continues to fall, digital waveform synthesis is becoming increasingly popular. Direct digital synthesis (DDS) offers unprecedented levels of signal stability. Potential signal complexity for numerous applications including communications, instrumentation, radar, and medical imaging is also enhanced by DDS. This application note describes how exceptional spectral purity can be achieved with the TDC1012 and TDC1112 in sinewave synthesis applications. Board design techniques which optimize the performance of these D/A converters is also discussed.

In most applications, the performance of a digital synthesizer is limited by the digital-to-analog converter (D/A) employed. Specifications of interest include maximum allowable sampling (digital clock) rate, signal-to- [random] noise ratio, total harmonic distortion, and spurious-free dynamic range (SFDR).

With their high linearity and low glitch energy, the TRW TDC1012 and TDC1112 12-bit and TDC1018 8-bit D/A converters are particularly well suited to DDS applications. When used with the TRW TMC2340 Direct Digital Frequency Synthesizer, the TDC1012 becomes the output stage of a high-performance, low part count digital frequency synthesizer. The TDC1012 offers a 20MSPS clock rate and is TTL-compatible. The TDC1112 operates at up to 50MSPS and is ECL-compatible. Both parts offer 70dB SFDR for 8 MHz signals sampled at 20MSPS.

The circuit in Figure 10 can perform with spurs as low as -70dBc. To maintain a clean clock signal, a buffer should drive the clock to the direct digital synthesis circuitry. The clock oscillator should be powered from the same decoupled V_{CC} as the D/A converter.

Grounding is extremely important. A solid copper ground plane should be used and connected to digital ground at only one point to prevent the formation of ground loops. This minimizes the flow of digital switching current across the D/A ground plane.

The use of a balun across the D/A outputs significantly improves spectral purity, since it effectively cancels distortion due to the Early voltage and data feedthrough characteristics of the D/A converter. In some applications, a 470 picofarad capacitor connected between pin 6 and pin 7 as close to those pins as possible will be effective in reducing spurs.

The primary sources of 2nd-harmonic distortion are insufficient input setup and hold times (t_S and t_H) and data feedthrough. Minimum setup and hold times for the SFDR specification are shown in the "System Performance Characteristics" section of the data sheets for the TDC1012 and TDC1112.

Figure 10 shows a 74ALS374 8-bit register with a 2ns R-C delay (200 Ohm, 10 pF in the clock input line) that is designed to help meet setup and hold times for the TDC1012 (when it is operated at 20MSPS) while reducing output slew rates. For military applications, a 54F374 with a 3ns R-C delay will meet the extended temperature range setup and hold time specifications while maintaining reasonable output slew rates. Note that the military versions of the TDC1012 and TDC1112 are available in a 24-pin side brazed ceramic dual-in-line package which has been specifically designed to minimize data feedthrough. For optimum performance, the D/A converter should be soldered directly to the board. If a socket must be used, a low profile gold-insert socket such as Robinson-Nugent part number ICT-246-S-TG is recommended.

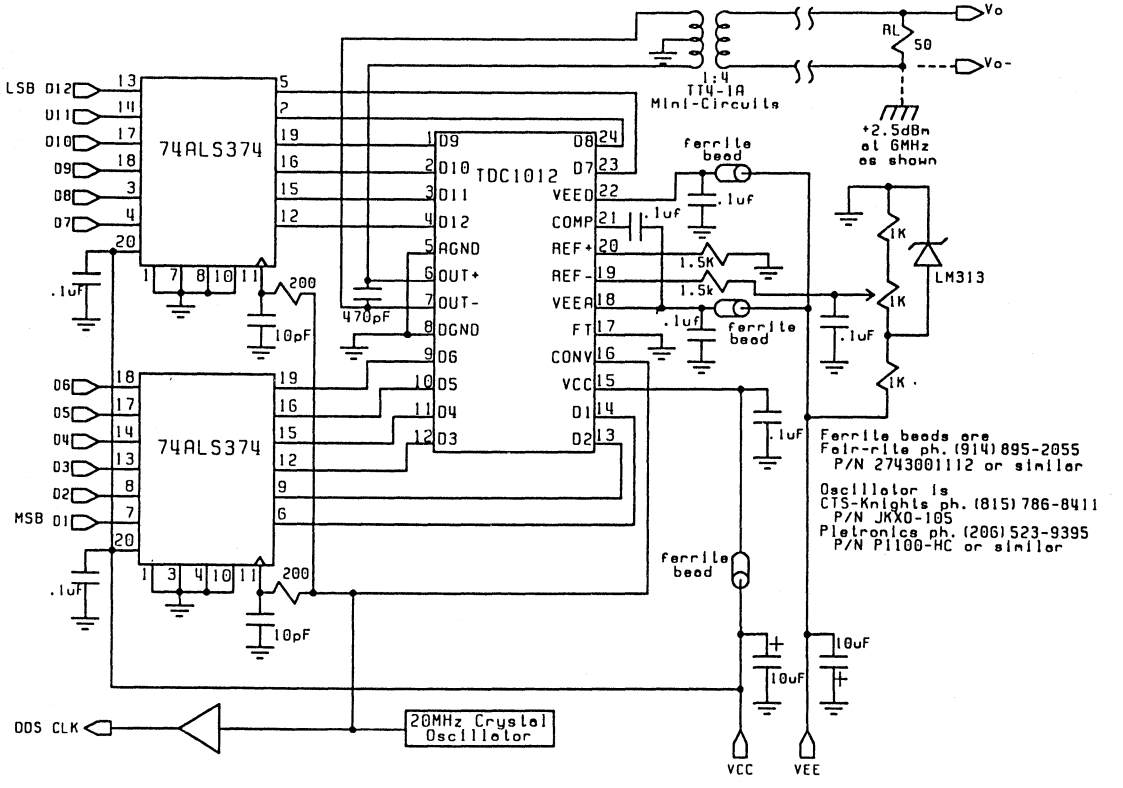
The primary source of 3rd-harmonic distortion is the small non-linear component of output capacitance of the D/A. This can be minimized by reducing the amplitude of the output voltage swing, e.g. with the 1:4 impedance ratio balun as shown in Figure 10. The center tap of the balun can be tied to a positive voltage generated by two diodes in series to ground. This will improve the 3rd-

harmonic distortion by around 2dB at the expense of the power dissipated by the diode biasing circuit. The D/A output voltage excursions should be limited to less than +1.2V.

The true harmonic distortion of these circuits can be masked by the spectrum analyzer under certain conditions. In particular, the circuit of Figure 10 generates a relatively high output power which can cause distortion in the internal circuitry of some spectrum analyzers. This can be avoided by setting the input attenuation to a higher level, typically 40dB.

The TDC1012 and TDC1112 D/A converters and TMC2340 Direct Digital Frequency Synthesizer make high-performance digital frequency synthesis cost-effective in applications requiring stability, spectral purity, and versatility.

Figure 8. The TDC1012 In a DDS Application



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1012N7CX	T_A=0°C to 70°C	Commercial	Plastic DIP	1012N7C-X
TDC1012J7CX	T_A=0°C to 70°C	Commercial	Ceramic DIP	1012J7C-X
TDC1012J7VX	T_C=–55°C to 125°C	MIL-STD-883	Ceramic DIP	1012J7V-X
TDC1012R3CX	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1012R3C-X
TDC1012C3VX	T_C–55°C to 125°C	MIL-STD-883	Ceramic Chip Carrier	1012C3V-X

Linearity Grade (X)		None	1	2	3
E_{LD}	Linearity Error, Differential	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)	±0.012% (1/2 LSB)
E_{LI}	Linearity Error, Integral	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)

40G02291 Rev E 8/93

TDC1016
Video Speed D/A Converter
10-Bit, 20 Msps

Description

The TDC1016 is a bipolar monolithic digital-to-analog converter which can convert digital data into an analog voltage at rates up to 20 Msps (Megasamples Per Second). The device includes an input data register and operates without an external deglitcher or amplifier.

Operating the TDC1016 from a single -5.2V power supply will bias the digital inputs for ECL levels, while operating from a dual ±5V power supply will bias the digital inputs for TTL levels.

All version of the TDC1016 are 10-bit digital-to-analog converters, but are available with linearity specifications of either 8. 9, or 10 bits. The TDC1016 is patented under U.S. patent number 3283120 with other patents pending.

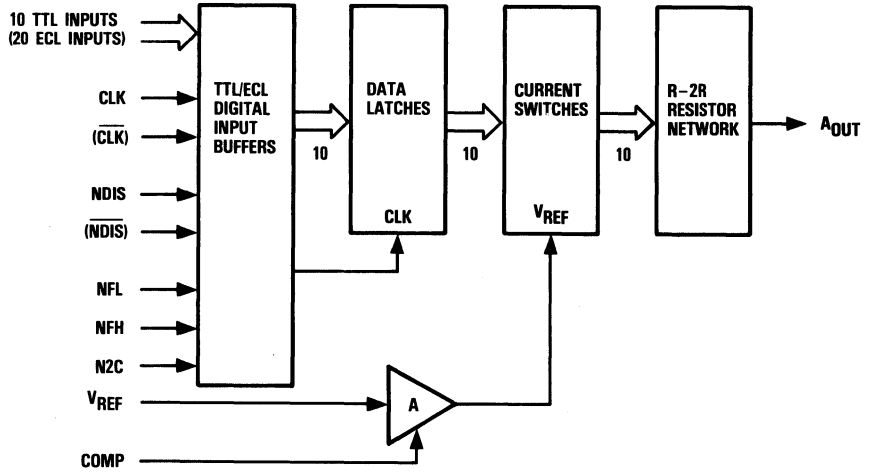
Features

- 20 Msps conversion rate
- 8, 9, or 10-bit linearity
- Voltage output, no amplifier required
- Single supply operation (-5.2V, ECL compatible)
- Dual supply operation (±5.0V, TTL compatible)
- Internal 10-bit latched data register
- Low glitch energy
- Disabling controls, forcing full-scale, zero, and inverting input data
- Binary or two's complement input data formats
- Differential gain = 1.5%, differential phase = 1.0°

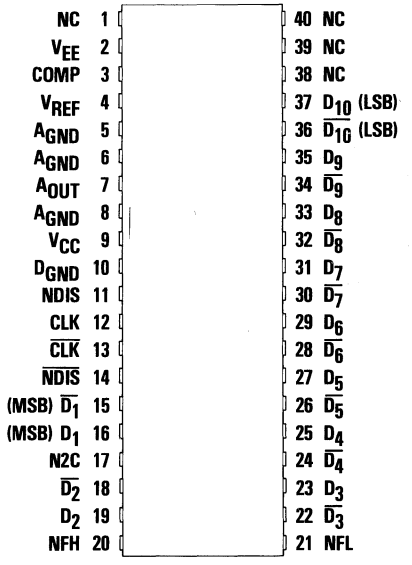
Applications

- Construction of video signals from digital data 3x or 4x NTSC or PAL color subcarrier frequency
- CRT graphics displays, RGB, Raster, Vector
- Waveform synthesis

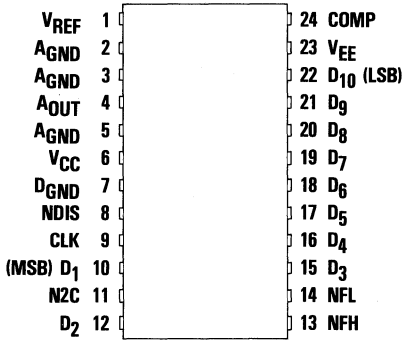
Functional Block Diagram



Pin Assignments



40 Pin Ceramic J5 Package



24 Pin Ceramic J7 Package

Functional Description

General Information

TTL/ECL buffers are used for all digital inputs to the TDC1016. Logic family compatibility depends upon the connection of power supplies. When single power supply (−5.2V) operation is employed, all data, clock, and disable inputs are compatible with differential ECL logic levels. All digital inputs become compatible with TTL levels when dual power supply (±5.0V) operation is used.

The internal 10-bit register latches data on the rising edge of the clock (CLK) pulse. Currents from the current sources are switched accordingly and combined in the resistor network to give an analog output voltage. The magnitude of the output voltage is directly proportional to the magnitude of the digital input word.

The NFL and NFH inputs can be used to simplify system calibration by forcing the analog output voltage to either its zero-scale or full-scale value. The TDC1016 can be operated in binary, inverse binary, two's complement, or inverse two's complement input data formats.

Power

The TDC1016 can be operated from a single −5.2V power supply or from a dual ±5.0V power supply. For single power supply operation, V_{CC} is connected to D_{GND} and all inputs to the device become ECL compatible. When V_{CC} is tied to +5.0V, the inputs are TTL compatible.

The return path for the output from the 10 current sources is A_{GND}. The current return path for the digital section is D_{GND}. D_{GND} and A_{GND} should be returned to system power supply ground by way of separate conductive paths to prevent digital ground noise from disturbing the analog circuitry of the TDC1016. All A_{GND} pins must be connected to system analog ground.

Reference

The reference input is normally set to −1.0V with respect to A_{GND}. Adjusting this voltage is equivalent to adjusting system gain. The temperature stability of the TDC1016 analog output (A_{OUT}) depends primarily upon the temperature stability of the applied reference voltage.

Reference (cont.)

The internal operational amplifier of the TDC1016 is frequency stabilized by an external 1 microfarad tantalum capacitor connected between the COMP pin and V_{EE}. A minimum of 1 microfarad is adequate for most applications, but 10 microfarads or more is recommended for optimum performance. The negative side of this capacitor should be connected to V_{EE}.

Controls

The NDIS inputs are used to disable the TDC1016 by forcing its output to the zero-scale value (current sources off). The NDIS inputs are asynchronous, active without regard to the CLK inputs. The other digital control inputs are synchronous, latched on the rising edge of the CLK pulse.

The rising edge of the CLK pulse transfers data from the input lines to the internal 10-bit register. In TTL mode, the inverted inputs for CLK, DATA, and NDIS are inactive and should be left open.

The *Input Coding Table* illustrates the function of the digital control inputs. A two's complement mode is created by activating N2C with a logic "0." When NFH and NFL are both activated with a logic "0," the input data to the 10-bit register is inverted.

Data Inputs

Data inputs are ECL compatible when single power supply operation is employed. The J5 and C2 packages allow for differential ECL inputs while the J7 and B7 packages have only single-ended inputs. When differential ECL data is used, any data input can be inverted simply by reversing the connections to the true and inverted data input pins. All inverted input pins should be left open if single-ended ECL or TTL modes are used. All data inputs have an internal 40 kOhm pull-up resistor to V_{CC}.

Analog Output

The analog output voltage is negative with respect to A_{GND} and varies proportionally with the magnitude of the input data word. The output resistance at this point is 80 Ohms, nominally.

No Connects

There are several pins labeled no connect (NC) on the TDC1016 J5 and C2 packages, which have no connections to the chip. These pins should be left open.

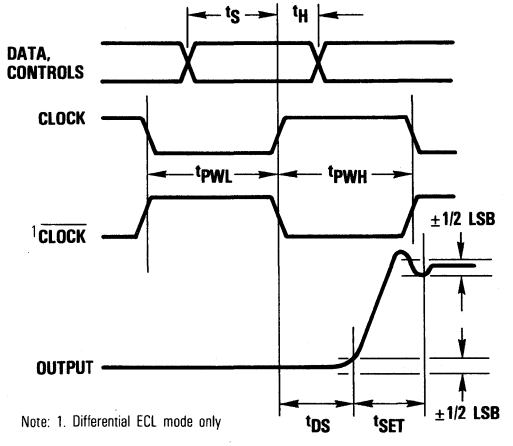
Package Interconnections

Signal Type	Signal Name	Function	Value	B5 Package Pins	B7 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	9	6
	V_{EE}	Negative Supply Voltage	−5.0V	2	23
	A_{GND}	Analog Ground	0.0V	5, 6, 8	2, 3, 5
	D_{GND}	Digital Ground	0.0V	10	7
Reference	V_{REF}	Reference Voltage In	−1.0V	4	1
	COMP	Compensation	1μF	3	24
Controls	NDIS	Not Disable	TTL/ECL	11	8
	$\overline{\text{NDIS}}$	Not Disable (Inv)	ECL	14	
	CLK	Clock	TTL/ECL	12	9
	$\overline{\text{CLK}}$	Clock (Inv)	ECL	13	
	N2C	Not Two's Complement	TTL/ECL	17	11
	NFH	Not Force HIGH	TTL/ECL	20	13
	NFL	Not Force LOW	TTL/ECL	21	14

Package Interconnections (cont.)

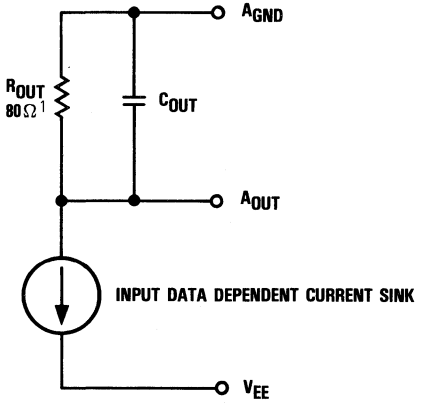
Signal Type	Signal Name	Function	Value	B5 Package Pins	B7 Package Pins
Data Inputs	D_1	Data Bit 1 (MSB)	TTL/ECL	16	10
	$\overline{D_1}$	Data Bit 1 (MSB Inv)	ECL	15	
	D_2		TTL/ECL	19	12
	$\overline{D_2}$		ECL	18	
	D_3		TTL/ECL	23	15
	$\overline{D_3}$		ECL	22	
	D_4		TTL/ECL	25	16
	$\overline{D_4}$		ECL	24	
	D_5		TTL/ECL	27	17
	$\overline{D_5}$		ECL	26	
	D_6		TTL/ECL	29	18
	$\overline{D_6}$		ECL	28	
	D_7		TTL/ECL	31	19
	$\overline{D_7}$		ECL	30	
	D_8		TTL/ECL	33	20
	$\overline{D_8}$		ECL	32	
	D_9		TTL/ECL	35	21
	$\overline{D_9}$		ECL	34	
	D_{10}	Data Bit 10 (LSB)	TTL/ECL	37	22
	$\overline{D_{10}}$	Data Bit 10 (LSB Inv)	ECL	36	
Analog Output	A_{OUT}	Analog Output Voltage	0V to −1V	7	4
No Connects	NC	No Connect	Open	1, 38, 39, 40	– –

Figure 1. Timing Diagram



Note: 1. Differential ECL mode only

Figure 2. Analog Output Equivalent Circuit, TTL and ECL Mode



Note: 1. 75Ω requires outside trim

Figure 3. Digital Input Equivalent Circuit, TTL Mode

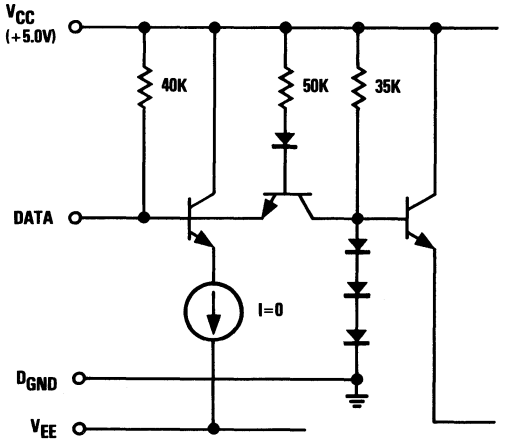
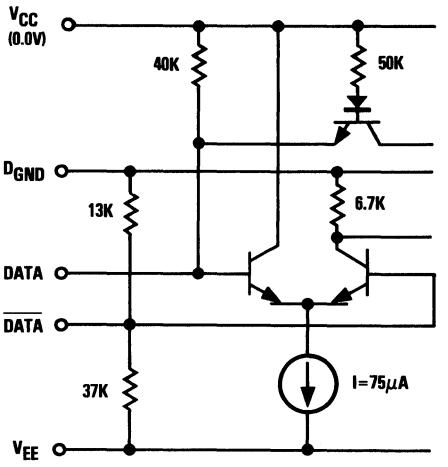


Figure 4. Digital Input Equivalent Circuit, ECL Mode



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured To D_{GND})	−0.5 to +7.0V
V_{EE} (measured To A_{GND})	+0.5 to −7.0V
A_{GND} (measured To D_{GND})	+0.5 to −0.5V

Input Voltages

Digital (measured To D_{GND})	+7.0 to −7.0V
Reference (measured To A_{GND})	−1.5 to +0.5V

Output

Applied voltage (measured To A_{GND})	+2.0 to −2.0V [2]
Short-circuit duration	indefinite

Temperature

Operating ambient	+125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.

Operating conditions

Parameter			Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Positive Supply Voltage	TTL Mode	4.75	5.0	5.25	4.50	5.0	5.50	V
		ECL Mode	−0.25	0.0	0.25	−0.25	0.0	0.25	V
V_{EE}	Negative Supply Voltage		−4.5	−5.0	−5.5	−4.5	−5.0	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})		−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CLK Pulse Width, LOW		15			20			ns
t_{PWH}	CLK Pulse Width, HIGH		15			20			ns
t_S	Input Register Set-up Time	TTL Mode	20			22			ns
		ECL Mode	25			27			ns
t_H	Input Register Hold Time		2			2			ns
V_{IL}	Logic "0"	TTL Mode	D_{GND}		0.8	D_{GND}		0.8	V
		ECL Mode			−1.67			−1.67	V
V_{IH}	Logic "1"	TTL Mode	2.0		V_{CC}	2.0[1]		V_{CC}	V
		ECL Mode	−1.0			−1.0			V
V_{REF}	Reference Voltage		−0.8	−1.0	−1.2	−0.8	−1.0	−1.2	V
C_{COMP}	Compensation Capacitor		1.0			1.0			μF
T_A	Ambient Temperature		0		70				°C
T_C	Case Temperature					−55		125	°C

Note:
1. V_{IH}/NDIS = 2.2 Min.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Power Supply Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		20		20	mA
I_{EE}	Power Supply Current	TTL Mode, V_{CC} = Max, V_{EE} = Max[1]		−130		−150	mA
I_{REF}	Reference Input Current	V_{EE} = Max, V_{REF} = −1.0V		10		10	μA
I_{IL}	Logic "0" Input Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		−1.0		−1.0	mA
		ECL Mode, V_{CC} = 0.0, V_{EE} = Max		−300		−300	μA
I_{IH}	Logic "1" Input Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		75		75	μA
		ECL Mode, V_{CC} = 0.0, V_{EE} = Max		350		350	μA
C_{OUT}	Output Capacitance	A_{OUT} to A_{GND} (Figure 2)		10		10	pF
C_{IN}	Digital Input Capacitance	Any Digital Input to D_{GND}		35		35	pF
R_{OUT}	Output Resistance	A_{OUT} to A_{GND} (Figure 2)	70	95	70	95	Ohms

Note:
1. Return current from V_{EE} flows through A_{GND}.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Maximum Data Rate	TTL Mode Full-Scale Output Step	20		20		MSPS
		ECL Mode Full-Scale Output Step	17.8		17.8		MSPS
t_{DS}	Data Turn-on Delay	RL = 75 Ohms		30		30	ns
t_{SET}	Settling Time	TDC1016-8 to 0.2%		30		30	ns
		TDC1016-9 to 0.1%		35		35	ns
		TDC1016-10 to .05%		40		40	ns
t_{RV}	Output 10% to 90% Risetime	V_{EE} = Nom, RL = 75 Ohms, Full-Scale Step		5.5		5.5	ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
RES	Resolution	All TDC1016 Devices		10		10	Bits
ELI, ELD	Linearity Error Integral and Differential Independent Based	TDC1016-8		0.2		0.2	% FS
		TDC1016-9		0.1		0.1	% FS
		TDC1016-10		0.075			% FS
V_{OFS}	Full-Scale Output Voltage	V_{EE} = Nom, RL $\geq$ 10 kOhms	-0.95	-1.05	-0.95	-1.05	V
		V_{REF} = -1.000V					
V_{OZS}	Zero-Scale Output Voltage	V_{EE} = Nom, RL $\geq$ 10 kOhms		±15		±15	mV
		V_{REF} = -1.000V					
DP	Differential Phase	NTSC 4x subcarrier[1]		1.0		1.0	Degree
DG	Differential Gain	NTSC 4x subcarrier[1]		1.5		1.5	%
GE	Glitch "Energy" (Area)	RL = 50 Ohms, Midscale		125		125	pV-sec
GV	Glitch Voltage	RL = 50 Ohms, Midscale		35		35	mV

Note:

1. In excess of theoretical DP and DG due to quantizing error.

Input Coding Table

NDIS	N2C	NFH	NFL	Data	Output	Description
0	x	x	x	xxxxxxxxxx	0.0	Output Disabled
1	1	1	1	1111111111	0.0	Binary (Default State for TTL
1	1	1	1	0000000000	−1.0	Mode Control) Inputs Open
1	1	0	0	1111111111	−1.0	Inverse Binary
1	1	0	0	0000000000	0.0	
1	0	1	1	0111111111	0.0	Two's Complement
1	0	1	1	1000000000	−1.0	
1	0	0	0	0111111111	−1.0	Inverse Two's Complement
1	0	0	0	1000000000	0.0	
1	x	0	1	xxxxxxxxxx	0.0	Force HIGH
1	x	1	0	xxxxxxxxxx	−1.0	Force LOW

Notes:
1. For TTL, $0.0 < V_{IL} < +0.8V$ is logic "0".
2. For TTL, $+2.0 < V_{IH} < +5.0V$ is logic "1".
3. For ECL, $-1.85 < V_{IL} < -1.67V$ is logic "0".
4. For ECL, $-1.0 < V_{IH} < -0.8V$ is logic "1".
5. x="don't care".

Calibration

The TDC1016 is calibrated by adjusting the voltage reference to give the desired full-scale output voltage. The current switches can be turned on either by loading the data register with full-scale data or by bringing the NFH input to a logic zero. Note that all 10 current switches are activated by the NFH input and the resulting full-scale output voltage will be greater than if the system used only eight or nine bits for full-scale data.

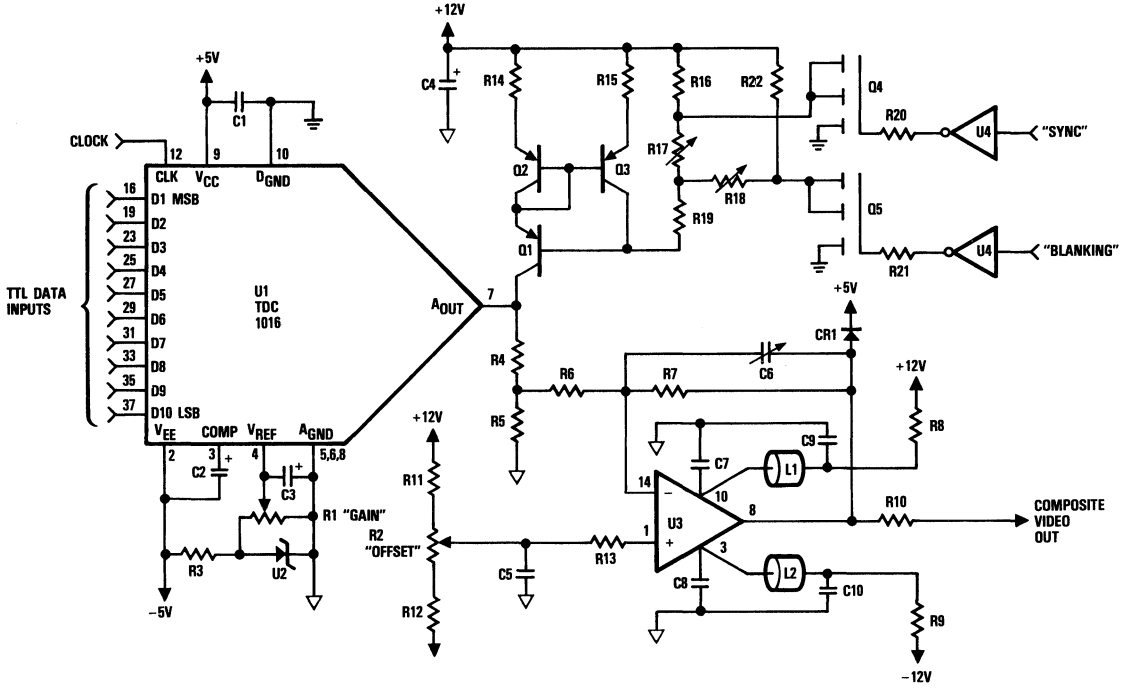
Typical Application

The *Typical Interface Circuit (Figure 5)* shows the TDC1016 in a typical application, reconstructing video signals from digital data. Television timing signals, SYNC and BLANKING, are added by injecting current from the Wilson current source into a resistor divider circuit at the output of the TDC1016.

The TDC1016 output and currents from the SYNC and BLANKING inputs are summed and amplified by the HA2539 wide-band operational amplifier. Note the careful power supply decoupling at the power input pins of the amplifier. The output of the circuit is a composite video signal with SYNC and BLANKING levels coming from external sources. This technique allows the TDC1016 to use its entire dynamic range for the video information while pulses are added by other means.

The reference for the TDC1016 is generated by dividing the output voltage from a two-terminal band-gap voltage reference. System gain is calibrated by adjusting variable resistor R1. Analog and digital grounds should be routed back to system power supply ground by separate paths.

Figure 5. Typical Interface Circuit



Parts List

Resistors

R1	5K	1/4W	10-turn
R2	1K	1/4W	10-turn
R3	1K	1/4W	5%
R4	43	1/4W	5%
R5	33	1/4W	5%
R6	330	1/4W	5%
R7	750	1/4W	5%
R8,R9	10	1/4W	5%
R10	75	1/4W	2%
R11,R12	10K	1/4W	5%
R13	220	1/4W	5%
R14,R15	100	1/4W	5%
R16,R22	390	1/4W	5%
R17,R18	2K	1/4W	10-turn
R19	1K	1/4W	5%
R20,R21	1K	1/4W	5%

Capacitors

C1	0.01μF	50V
C2	1.0μF	10V
C3	1.0μF	10V
C4	2.2μF	25V
C5	0.1μF	50V
C6	2-5 pF	50V
C7	0.1μF	50V
C8	0.1μF	50V
C9	0.1μF	50V
C10	0.1μF	50V

RF Chokes

L1,L2	Ferrite beads

Diodes

CR1	1N4001

Transistors

Q1	2N2907
Q2	2N2907
Q3	2N2907
Q4	2N6660
Q5	2N6660

Integrated Circuits

U1	TRW TDC1016
U2	LM113
U3	HA2539
U4	SN7404

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1016J5CX	STD - T_A = 0°C to 70°C	Commercial	40 Pin Ceramic	1016J5CX
TDC1016J5AX	EXT - T_C = -55°C to 125°C	High Reliability	40 Pin Ceramic	1016J5AX
TDC1016J7CX	STD - T_A = 0°C to 70°C	Commercial	24 Pin Ceramic	1016J7CX
TDC1016J7AX	EXT - T_C = -55°C to 125°C	High Reliability	24 Pin Ceramic	1016J7AX

40G00280 Rev H 8/93

TDC1018
Digital-to-Analog Converter
8-Bit, 200 MHz

Description

The TDC1018 is an 8-bit digital-to-analog converter, designed for 200 MHz operation and capable of directly driving a 75 Ohm load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Four special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

The TDC1018 is built with Raytheon Semiconductor's OMICRON-B™ 1-micron bipolar process. On-chip data registers and precise matching of propagation delays make the TDC1018 inherently low-glitching. The TDC1018 offers high performance, low power consumption, and video compatibility in a 24-pin DIP or a 28-contact chip carrier.

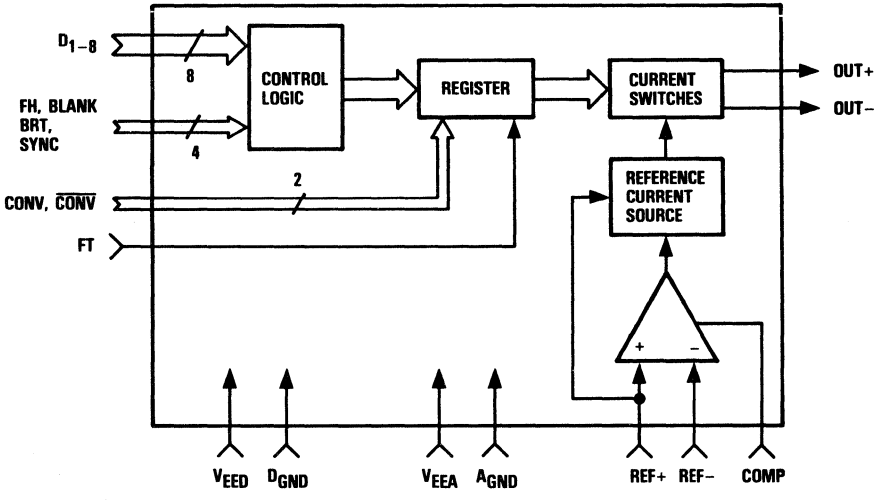
Features

- Monolithic "Graphics-Ready"
- 125 MHz digital update rate, TDC1018
- 200 MHz digital update rate, TDC1018-1
- 8-bit resolution
- 1/2 LSB linearity
- Registered data and video controls
- Complementary current outputs
- Video controls: SYNC, BLANK, BRighT, force high
- Inherently low glitch energy
- ECL compatible inputs
- Multiplying mode capability
- Can be operated in TTL systems
- Available in a 24-pin DIP and 28-contact chip carrier
- Single -5.2V power supply

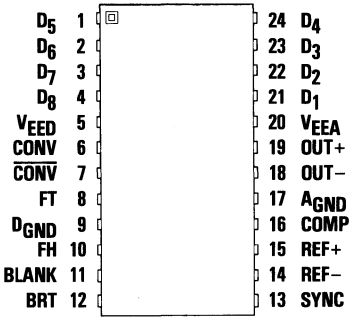
Applications

- RGB graphics
- High resolution video
- Raster graphic displays
- Digital synthesizers
- Automated test equipment
- Digital transmitters/modulators

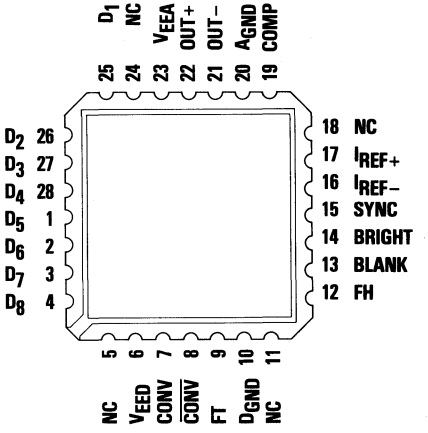
Functional Block Diagram



Pin Assignments



24 Pin CERDIP – B7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1018 develops complementary analog output currents proportional to the product of the digital input data and analog reference current. All data and control inputs are compatible with standard ECL logic levels. FeedThrough control (FT) determines whether data and control inputs are synchronous or asynchronous. If FT is LOW, each rising edge of the CONVert clock (CONV) latches decoded data and control values into an internal D-type register. The registered values are then converted into the appropriate analog output by switched current sinks. When FT is HIGH, data and control inputs are not registered, and the analog output asynchronously tracks the input values. FT is the only asynchronous input, and is normally used as a DC control.

The TDC1018 uses a segmented approach in which the four MSBs of the input data are decoded into a parallel "Thermometer" code, which drives fifteen identical current sinks to produce sixteen coarse output levels. The LSBs of the input drive four binary-weighted current switches, with a total contribution of one-sixteenth of full-scale. The LSB and MSB currents are summed to provide 256 analog output levels.

Special control inputs, SYNC, BLANK, Force High (FH) and BRight (BRT), drive appropriately weighted current sinks which add to the output current to produce specific output levels especially useful in video applications.

Power

To provide highest noise immunity, the TDC1018 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}, respectively. Since the required voltage for both V_{EEA} and V_{EED} is $-5.2V$, these may ultimately be connected to the same power source, but individual high-frequency decoupling for each supply is recommended. A typical decoupling network is shown in *Figure 7*. The return for I_{EED}, the current drawn from the V_{EED} supply, is D_{GND}. The return for I_{EEA} is A_{GND}. All power and ground pins MUST be connected.

Although the TDC1018 is specified for a nominal supply of $-5.2V$, operation from a $+5.0V$ supply is possible provided that the relative polarities of all voltages are maintained.

For additional information concerning the use of ECL D/A converters in a $+5V$ system, refer to ***TRW Application Note TP-33 "Using the TDC1018 and TDC1034 in a TTL Environment."***

Reference

The TDC1018 has two reference inputs: REF+ and REF−, which are noninverting and inverting inputs of an internal reference buffer amplifier. The output of this operational amplifier serves as a reference for the current sinks. The feedback loop is internally connected around one of the current sinks to achieve high accuracy (see *Figure 4*).

The analog output currents are proportional to the digital data and reference current, I_{REF}. The full-scale output value may be adjusted over a limited range by varying the reference current. Accordingly, the stability of the analog output depends primarily upon the stability of the reference. A method of achieving a stable reference is shown in *Figure 7*.

The reference current is fed into the REF+ input, while REF− is typically connected to a negative reference voltage through a resistor chosen to minimize input offset bias current effects.

A COMPensation input (COMP), is provided for external compensation of the TDC1018's reference amplifier. A capacitor (C_C) should be connected between COMP and the V_{EEA} supply, keeping lead lengths as short as possible. The value of the compensation capacitor determines the effective bandwidth of the amplifier. In general, decreasing C_C increases bandwidth and decreases amplifier stability. For applications in which the reference is constant, C_C should be large, while smaller values of C_C may be chosen if dynamic modulation of the reference is required.

Controls

The TDC1018 has four special video control inputs: SYNC, BLANK, Force High (FH), and BRighT (BRT), in addition to a clock FeedThrough control (FT). All controls are standard ECL level compatible, and include internal pulldown resistors to force unused controls to a logic LOW (inactive) state.

Typically the TDC1018 is operated in the synchronous mode, which assures the highest conversion rate and lowest spurious output noise. By asserting FT, the input registers are disabled, allowing data and control changes to asynchronously feed-through to the analog output. Propagation delay from input change (control or data) to analog output is minimized in the asynchronous mode of operation.

In the synchronous mode, the video control inputs are registered by the rising edge of the CONV clock in a manner similar to the data inputs. The controls, like data, must be present at the inputs for a setup time of t_S (ns) before, and a hold time of t_H (ns) after the rising edge of CONV in order to be registered. In the asynchronous mode, the setup and hold times are irrelevant and minimum pulse widths HIGH and LOW become the limiting factor.

Asserting the video controls produces various output levels which are used for frame synchronization, horizontal blanking, etc., as described in video system standards such as RS-170 and RS-343A. The effect of the video controls on the analog outputs is shown in *Table 1*. Special internal logic governs the interaction of these controls to simplify their use in video applications. BLANK, SYNC, and Force High override the data inputs. SYNC overrides all other inputs, and produces full negative video output. Force High drives the internal digital data to full-scale, giving a reference white video level output. The BRT control creates a "whiter than white" level by adding 10% of the full-scale value to the present output level, and is especially useful in graphics displays for highlighting cursors, warning messages, or menus. For non-video applications, the special controls can be left unconnected.

Data Inputs

Data inputs to the TDC1018 are standard single-ended ECL level compatible. Internal pulldown resistors force unconnected data inputs to logic LOW. Input registers are provided for synchronous data entry and lowest differential data propagation delay (skew), which minimizes glitching.

In the registered mode, valid data must be present at the input a setup time t_S (ns) before, and a hold time t_H (ns) after the rising edge of CONV. When FT is HIGH, data input is asynchronous and the input registers are disabled. In this case the analog output changes asynchronously in direct response to the input data.

Convert

CONVert (CONV) is a differential ECL compatible clock input whose rising edge synchronizes data and control entry into the TDC1018. Within the constraints shown in ***Figure 2***, the actual switching threshold of CONV is determined by $\overline{CONV}$. CONV may be driven single-ended by connecting $\overline{CONV}$ to a suitable bias voltage (V_{BB}). The bias voltage chosen will determine the switching threshold of CONV. However, for best performance, CONV must be driven differentially. This will minimize clock noise and power supply/output intermodulation. Both clock inputs must normally be connected, with $\overline{CONV}$ being the complement of CONV.

Analog Outputs

The two analog outputs of the TDC1018 are high-impedance complementary current sinks which vary in proportion to the input data, controls, and reference current values. The outputs are capable of directly driving a dual 75 Ohm load to standard video levels. The output voltage will be the product of the output current and effective load impedance, and will usually be between 0V and −1.07V in the standard configuration (see ***Figure 5***). In this case, the OUT− output gives a DC shifted video output with "sync down." The corresponding output from OUT+ is also DC shifted and inverted, or "sync up."

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins	C3 Package Pins
Power	V_{EEA}	Analog Supply Voltage	−5.2V	20	23
	V_{EED}	Digital Supply Voltage	−5.2V	5	6
	A_{GND}	Analog Ground	0.0V	17	20
	D_{GND}	Digital Ground	0.0V	9	10
Reference	REF−	Reference Current− Input	Op-Amp Virtual Ground	14	16
	REF+	Reference Current+ Input	Op-Amp Virtual Ground	15	17
	COMP	COMPensation Input	C_C	16	19
Controls	FT	Register FeedThrough Control	ECL	8	9
	FH	Data Force High Control	ECL	10	12
	BLANK	Video BLANK Input	ECL	11	13
	BRT	Video BRighT Input	ECL	12	14
	SYNC	Video SYNC Input	ECL	13	15
Data Inputs	D_1	Data Bit 1 (MSB)	ECL	21	25
	D_2		ECL	22	26
	D_3		ECL	23	27
	D_4		ECL	24	28
	D_5		ECL	1	1
	D_6		ECL	2	2
	D_7		ECL	3	3
	D_8	Data Bit 8 (LSB)	ECL	4	4
Convert	CONV	CONVert Clock Input	ECL	6	7
	$\overline{CONV}$	CONVert Clock Input, Complement	ECL	7	8
Analog Outputs	OUT−	Output Current−	Current Sink	18	21
	OUT+	Output Current+	Current Sink	19	22

Figure 1. Timing Diagram

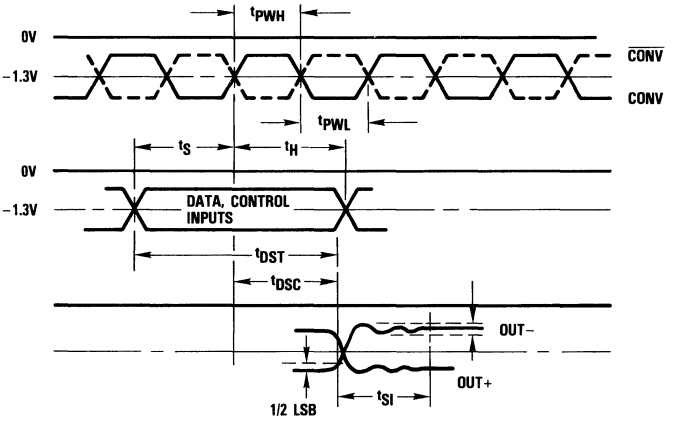


Figure 2. CONVert, CONVert Switching Levels

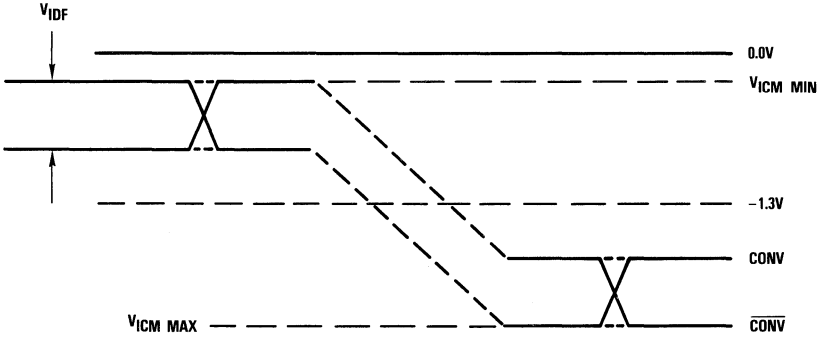


Figure 3. Equivalent Input Circuits

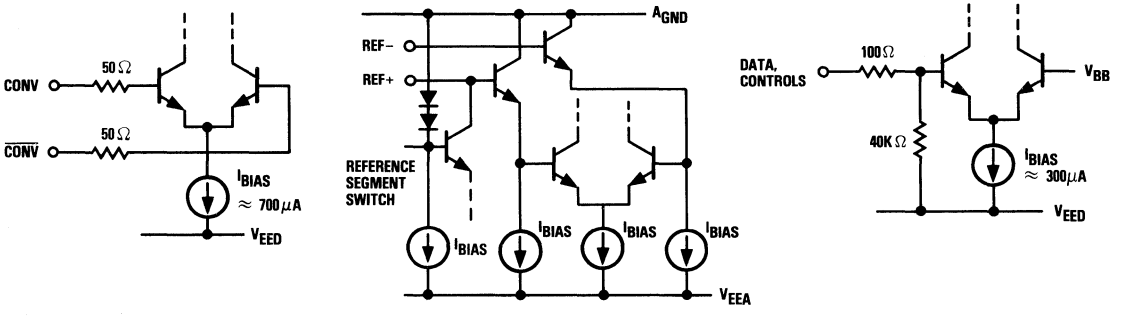


Figure 4. Equivalent Output Circuit

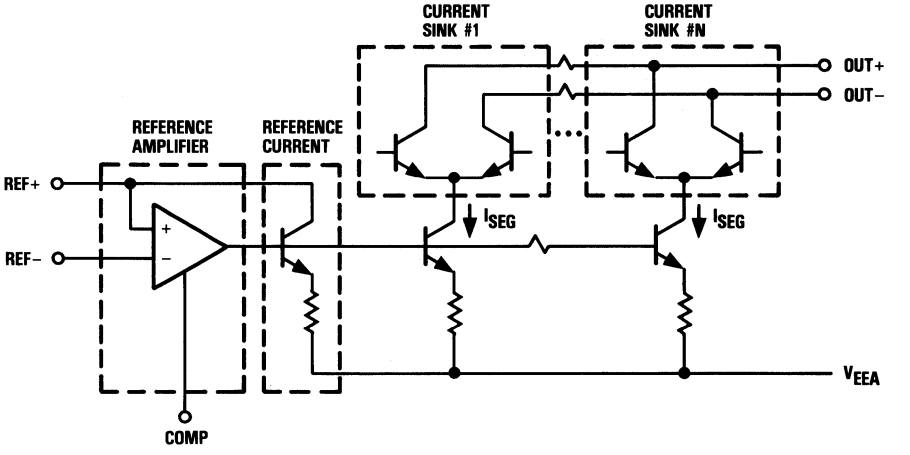
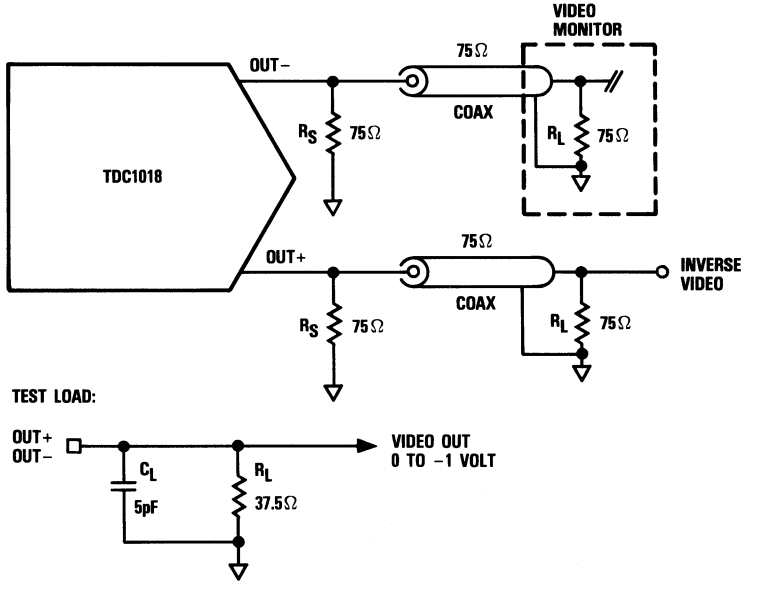


Figure 5. Standard Load Configuration



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND})	−7.0 to 0.5V
V_{EEA} (measured to A_{GND})	−7.0 to 0.5V
A_{GND} (measured to D_{GND})	−0.5 to 0.5V

Input Voltages

CONV, Data, and Controls (measured to D_{GND})	V_{EED} to 0.5V
Reference input, applied voltage (measured to A_{GND}) [2]	
REF+	V_{EEA} to 0.5V
REF−	V_{EEA} to 0.5V
Reference input, applied current, externally forced [3,4]	
REF+	6.0mA
REF−	0.5mA

Output

Analog output, applied voltage (measured to A_{GND})	
OUT+	−2.0 to +2.0V
OUT−	−2.0 to +2.0V
Analog output, applied current, externally forced [3,4]	
OUT+	50mA
OUT−	50mA
Short circuit duration	Unlimited sec

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions

Parameter			Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage (measured to D_{GND})		-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})		-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})		-0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential		-0.1	0.0	+0.1	V
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 2)		-0.5		-2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 2)		0.4		1.2	V
t_{PWL}	CONV Pulse Width, LOW		4			ns
t_{PWH}	CONV Pulse Width, HIGH		4			ns
t_S	Setup Time, Data and Controls		3.5			ns
t_H	Hold Time, Data and Controls		0			ns
V_{IL}	Input Voltage, Logic LOW				-1.49	V
V_{IH}	Input Voltage, Logic HIGH		-1.045			V
I_{REF}	Reference Current	Video standard output levels[1]	1.059	1.115	1.171	mA
		8-bit linearity	1.0		1.3	mA
C_C	Compensation Capacitor		2000	3900		pF
T_A	Ambient Temperature, Still Air		0		70	°C

Note:

1. Minimum and Maximum values allowed by ±5% variation given in RS343A and RS170 after initial gain correction of device.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{EED}$	Supply Current	$V_{EEA} = V_{EED}$ = MAX, static[1]			
		T_A = 0°C to 70°C		170	mA
		T_A = 70°C		130	mA
C_{REF}	Equivalent Input Capacitance, REF+, REF-			5	pF
C_I	Input Capacitance, Data and Controls			5	pF
V_{OCP}	Compliance Voltage, + Output		-1.2	+1.5	V
V_{OCN}	Compliance Voltage, - Output		-1.2	+1.5	V
R_O	Equivalent Output Resistance		20		KOhms
C_O	Equivalent Output Capacitance			20	pF
I_{OP}	Max Current, + Output	V_{EEA} = NOM, SYNC = BLANK = 0, FH = BRT = 1		30	mA
I_{ON}	Max Current, - Output	V_{EEA} = NOM, SYNC = 1		30	mA
I_{IL}	Input Current, Logic LOW, Data and Controls	V_{EED} = MAX, V_I = -1.49V		200	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls	V_{EED} = MAX, V_I = -1.045V		200	μA
I_{IC}	Input Current, Convert	V_{EED} = MAX, $-1.49V < V_I < -1.045V$		50	μA

Note:

1. Worst case over all data and control states.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Data Rate	V_{EEA}, V_{EED} = MIN			
		TDC1018	125		MSPS
		TDC1018-1	200		MSPS
t_{DSC}	Clock to Output Delay, Clocked Mode	V_{EEA}, V_{EED} = MIN, FT = 0		8	ns
t_{DST}	Data to Output Delay, Transparent Mode	V_{EEA}, V_{EED} = MIN, FT = 1		13	ns
t_{SI}	Current Settling Time, Clocked Mode	V_{EEA}, V_{EED} = MIN, FT = 0			
		0.2%		10	ns
		0.8%		8	ns
		3.2%		5	ns
t_{RI}	Risetime, Current	10% to 90% of Gray Scale		1.7	ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Terminal Based	V_{EEA}, V_{EED}, I_{REF} = NOM		0.2	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = NOM		0.2	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = MAX, SYNC = BLANK = 0, FH = BRT = 1		10	μA
E_G	Absolute Gain Error	V_{EEA}, V_{EED} = MIN, I_{REF} = NOM		±5	% of Gray Scale
TC_G	Gain Error Tempco			±0.024	% of Gray Scale/°C
BWR	Reference Bandwidth, -3dB	C_C = MIN, ΔV_{REF} = 1mV p-p	1		MHz
DP	Differential Phase	4 x NTSC		1.0	Degrees
DG	Differential Gain	4 x NTSC		2.0	%
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = NOM[1]		45	dB
		V_{EEA}, V_{EED}, I_{REF} = NOM[2]		55	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = NOM		120	μA/V
G_C	Peak Glitch Charge	Registered Mode[3,4]		800	fCoulomb
G_I	Peak Glitch Current	Registered Mode		1.2	mA
G_E	Peak Glitch "Energy" (Area)	Registered Mode[4]		30	pV-Sec
FT_C	Feedthrough Clock	Data = Constant[5]		-50	dB
FT_D	Feedthrough Data	Clock = Constant[5]		-50	dB

Notes:

1. 20KHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. fCoulombs = microamps x nanoseconds
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch area approaches zero.
5. dB relative to full gray scale, 250MHz bandwidth limit.

Table 1 Video Control Truth Table

Sync	Blank	Force High	Bright	Data Input	Out– (mA)[1]	Out– (V)[2]	Out– (IRE)[3]	Description[4]
1	X	X	X	X	28.57	–1.071	–40	Sync Level
0	1	X	X	X	20.83	–0.781	0	Blank Level
0	0	1	1	X	0.00	0.00	110	Enhanced High Level
0	0	1	0	X	1.95	–0.073	100	Normal High Level
0	0	0	0	000...	19.40	–0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	–0.073	100	Normal High Level
0	0	0	1	000...	17.44	–0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.00	110	Enhanced High Level

Notes:

1. Out+ is complementary to Out–. Current is specified as conventional current when flowing into the device.
2. Voltage produced when driving the standard load configuration (37.5 Ohms). See Figure 5.
3. 140 IRE units = 1.00V.
4. RS–343–A tolerance on all control values is assumed.

Figure 6. Video Output Waveforms for Out– and Out+ with Standard Load Configuration

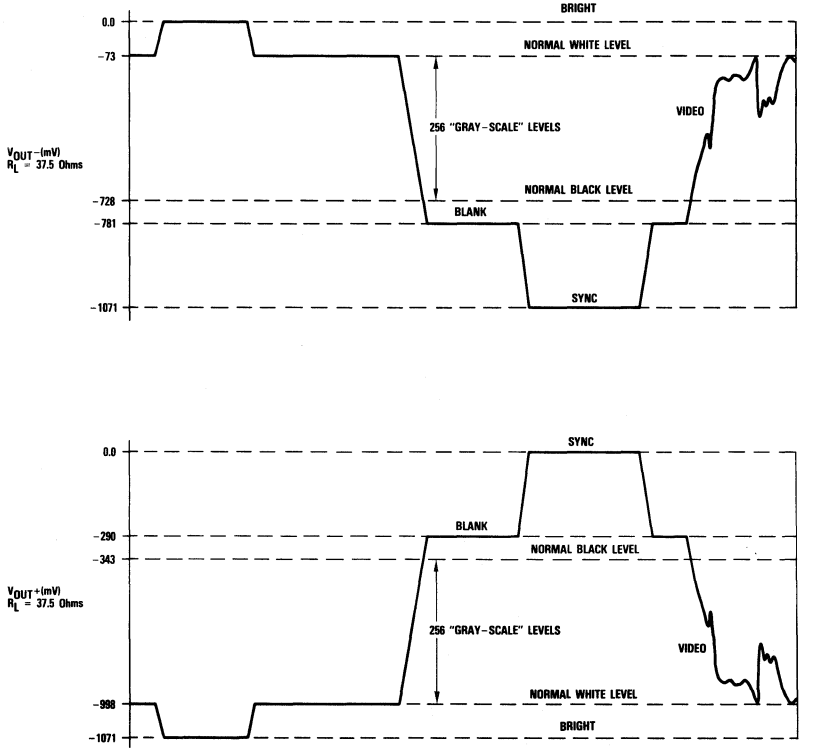
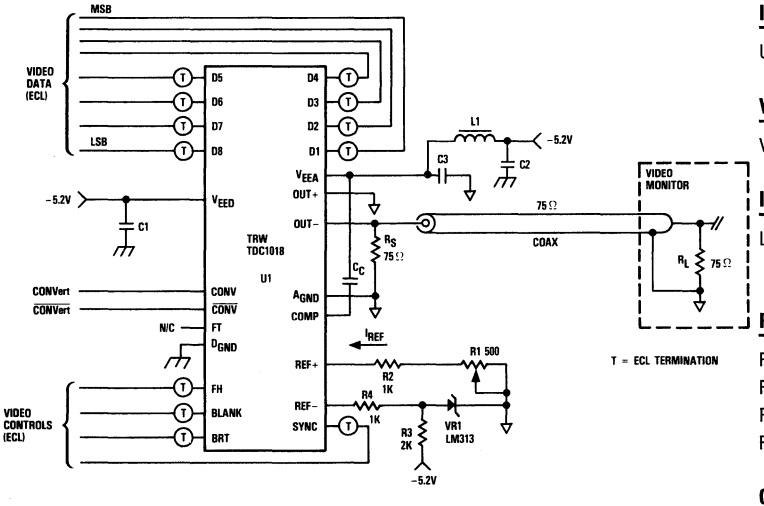


Figure 7. Typical Interface Circuit



Parts List

Integrated Circuits

U1 TDC1018 D/A Converter

Voltage References

VR1 LM113 or LM313 Bandgap Reference

Inductors

L1 Ferrite Bead Shield Inductor
Fair-Rite P/N 2743001112 or Similar

Resistors

R1	1KΩ	Pot	10 Turn
R2	1.00KΩ	1/8W	1% Metal Film
R3	2.00KΩ	1/8W	1% Metal Film
R4	1.00KΩ	1/8W	1% Metal Film

Capacitors

C1 – C3	0.1μF	50V	Ceramic Disc
C_C	0.01μF	50V	Ceramic Disc

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1018B7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1018B7C
TDC1018B7C1	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1018B7C1
TDC1018C3C	STD – T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1018C3C
TDC1018C3C1	STD – T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1018C3C1

40G01211 Rev H 8/93

TDC1041
Monolithic Digital-to-Analog Converter
10-Bit, 20 Msps, 12 ns Settling Time

Description

The TDC1041 is a TTL compatible, 10-bit monolithic D/A converter capable of converting digital data into an analog current or voltage at data rates in excess of 20 Megasamples-per second (Msps).

The analog circuitry has been optimized for dynamic performance, with very low glitch energy. The output is able to drive a 50Ω load with a 1 Volt output level while maintaining low harmonic distortion.

Data registers are incorporated on the TDC1041. This eliminates data skew encountered with external registers and latches and minimizes the glitches that can adversely affect many applications.

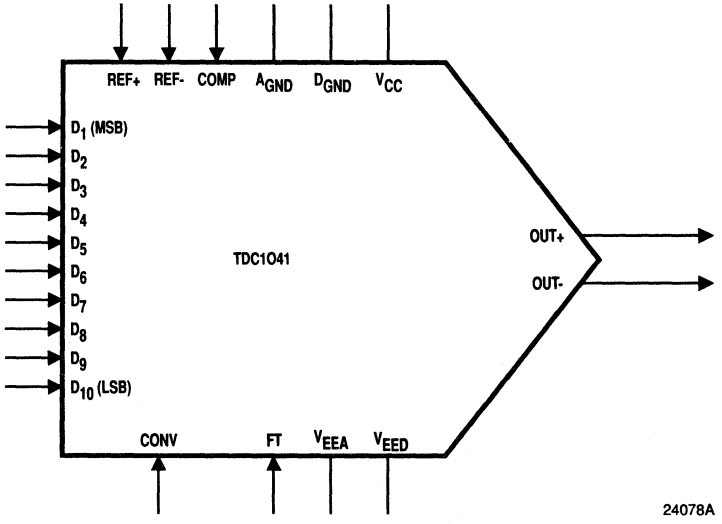
Features

- 10-bit resolution
- 20 Msps data rate
- TTL inputs
- Very low-glitch with no track and hold circuit needed
- Dual +4 dBm (1V into 50Ω) outputs make output amplifiers unnecessary in many application

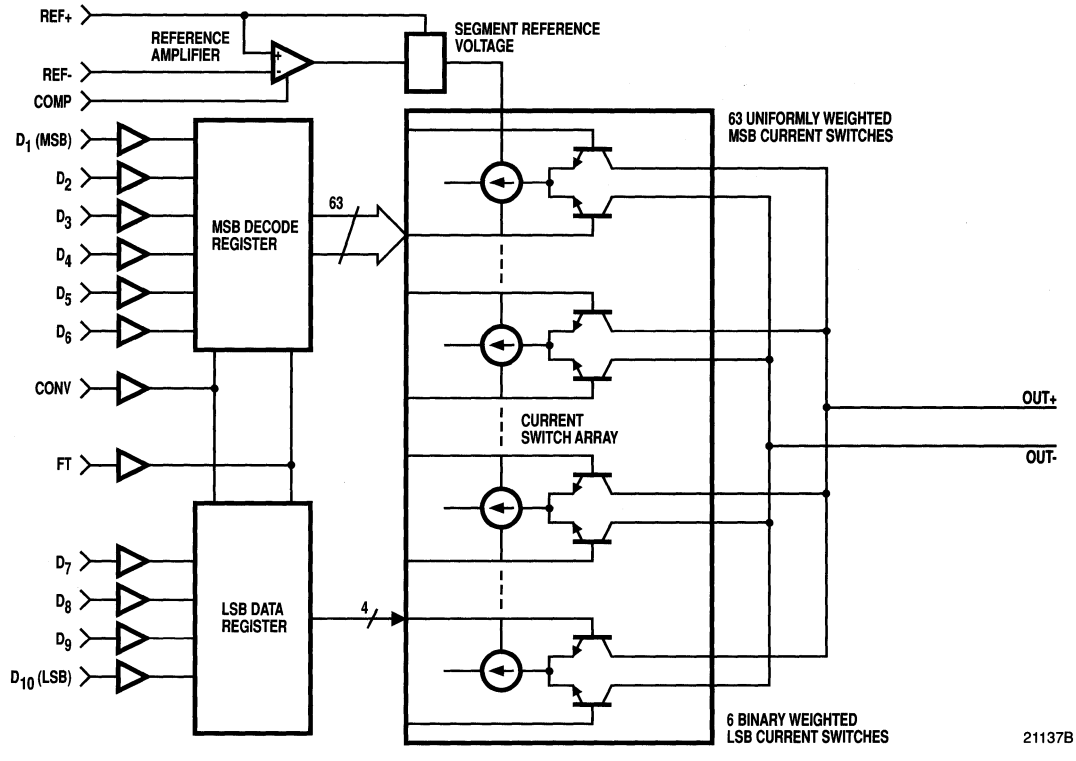
Applications

- Test signal generation
- Arbitrary waveform synthesis
- Broadcast and studio video
- High-resolution A/D converters

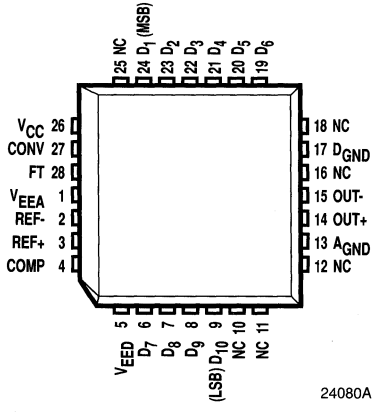
Interface Diagram



Functional Block Diagram



Pin Assignments



28 Leaded Plastic Chip Carrier – R3 Package

Functional Description

General Description

The TDC1041 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

Power, Grounds

The TDC1041 requires a –5.2V power supply and a +5.0V power supply. The analog (V_{EEA}) and digital (V_{EED}) supply voltages should be decoupled from each other, as shown in the *Typical Interface Circuit*. The V_{CC} pin should be considered a digital power supply. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The inductors are simple ferrite beads and are neither critical in value nor always required.

Reference and Compensation

The TDC1041 has two reference inputs: REF+ and REF–. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF- pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT} = N \times \frac{I_{REF}}{16}$$

Where N is the value of the input code.

This means that with an I_{REF} that is nominally 625μA, the full-scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω total load) with a 1V peak to peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so that the effect of amplifier input bias current is minimized. When driving a 75Ω load, the reference current must be reduced. This can be done by increasing the value of the resistor from REF+ to ground.

The internal reference amplifier is externally compensated to ensure stability. A 0.1μF capacitor should be connected between the COMP pin and V_{EEA}.

Digital Inputs

The data inputs are TTL compatible. One of the effects that leads to degradation of the dynamic performance of the device is the capacitive feedthrough from the digital inputs to the analog output of the device. One method of reducing the effect of capacitive coupling is to slow down the slew rates of the digital inputs. This can be done in many ways, starting with the selection of a logic family that is no faster than what is needed, and can include the addition of 50Ω series resistors to the data lines.

Clock and Feedthrough Control

The TDC1041 requires a TTL clock signal (CONV). Data is synchronously entered on the rising edge of CONV. The CONV input is ignored in the Feedthrough (FT = HIGH) mode. The Feedthrough (FT) pin is normally held LOW, where the TDC1041 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided, and this pin may be left open for clocked operation.

For certain applications, such as high-precision successive approximation A/D converters, throughput delay may be more important than glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronously in response to the digital inputs.

Since skew in the bits of the input word will result in glitches, and will affect settling time, it is recommended that the TDC1041 be operated in clocked mode for most applications.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By loading the current source outputs with a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to –40mA output current (0 to –1V when terminated in 25Ω) as the input code varies from 00 0000 0000 to 11 1111 1111. OUT– varies in a complementary manner from –40 to 0mA (–1 to 0V when terminated with 25Ω) over the same code range. (See the *Input Coding Table*.) The output current is proportional to the reference current and the input code.

No Connect

These pins have no internal connection and should be left open for optimal performance.

Package Interconnections

Signal Type	Signal Name	Function	Value	R3 Package Pins
Power	A_{GND}	Analog Ground	0.0V	13
	D_{GND}	Digital Ground	0.0V	17
	V_{EEA}	Analog Supply Voltage	–5.2V	1
	V_{EED}	Digital Supply Voltage	–5.2V	5
	V_{EED}	Digital Supply Voltage	–5.2V	26
Reference	REF–	Reference Voltage Input	–1.0V	2
	REF+	Reference Current Input	625µA	3
	COMP	Compensation Capacitor	0.1µF, see text	4
Data Inputs	D_1 (MSB)	Most Significant Bit	TTL	24
	D_2		TTL	23
	D_3		TTL	22
	D_4		TTL	21
	D_5		TTL	20
	D_6		TTL	19
	D_7		TTL	6
	D_8		TTL	7
	D_9		TTL	8
	D_{10} (LSB)	Least Significant Bit	TTL	9
Feedthrough	FT	Feedthrough Mode Control	TTL	28
Convert	CONV	Convert (Clock) Input	TTL	27
Analog Output	OUT+	Analog Output	0 to 40mA	14
	OUT–	Analog Output	40 to 0mA	15
No Connect	NC	No Internal Connection	Open	10,11,12,16,18,25

Input Coding Table[1]

Input Data MSB LSB	OUT+ (mA)	V_{OUT+}(mV)	OUT– (mA)	V_{OUT-}(mV)
00 0000 0000	0.000	0.00	40.000	–1000.00
00 0000 0001	0.039	–0.97	39.961	–998.05
00 0000 0010	0.078	–1.95	39.922	–998.05
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
0111 1111 11	19.961	–499.03	20.000	–500.00
1000 0000 00	20.000	–500.00	19.961	–499.03
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1111 1111 01	39.922	–998.05	0.078	–1.95
1111 1111 10	39.961	–999.03	0.039	–0.97
1111 1111 11	40.000	–1000.00	0.000	0.0

Note: 1. I_{REF} = 625µA, R_{LOAD} = 25Ω

Figure 1. Timing Diagram

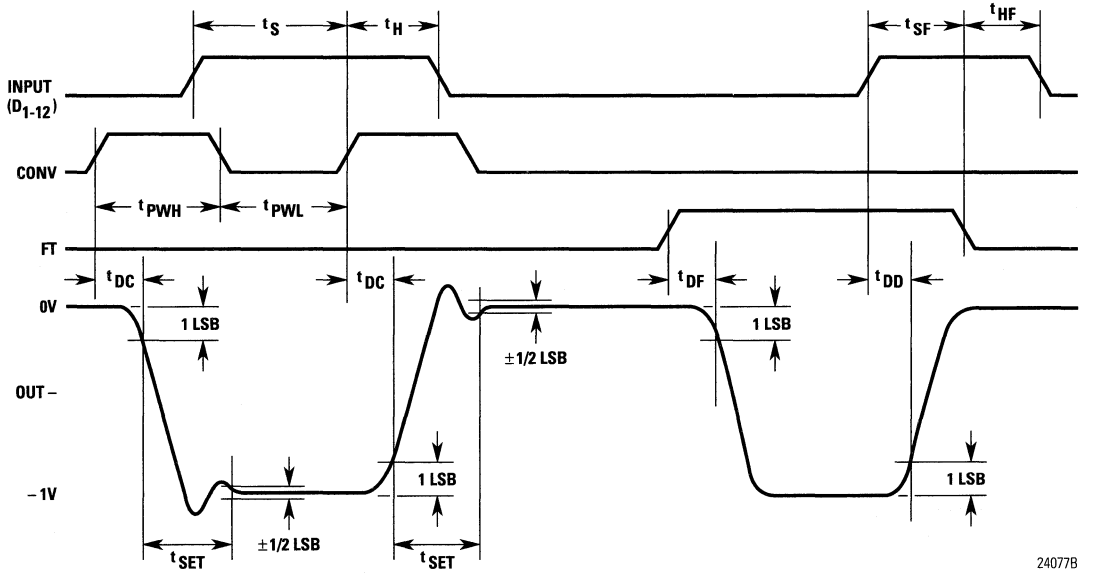
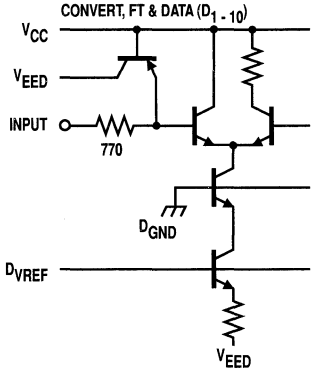


Figure 2. Equivalent Reference and Output Circuits



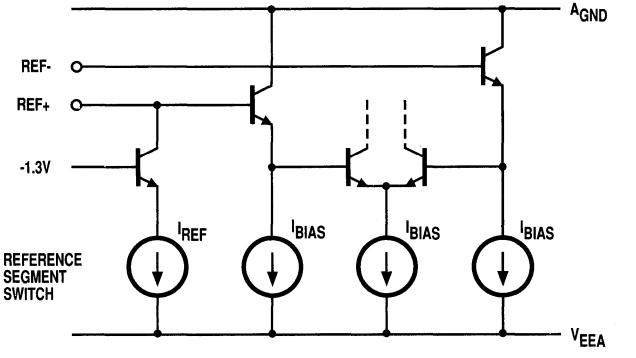


Figure 3. Simplified Reference and Output Circuits

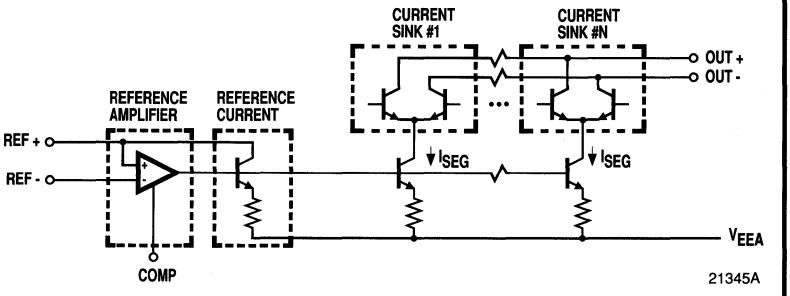
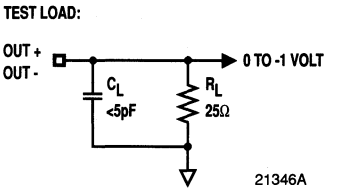


Figure 4. Output Test Load



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{CC}	(measured to D_{GND})	–0.5 to +7.0V
V_{EEA}	(measured to A_{GND})	–7.0 to +0.5V
V_{EEA}	(measured to V_{EED})	–50 to +50mV
V_{EED}	(measured to D_{GND})	–7.0 to +0.5V
A_{GND}	(measured to D_{GND})	–0.5 to +0.5V

Inputs

CONV, FT, $D_{1\text{-}10}$ (measured to D_{GND})[2]	V_{CC} +0.5 to –0.5V
CONV, FT, $D_{1\text{-}10}$ Current, externally forced[3]	±3mA
REF+, REF-,applied voltage (measured to A_{GND})[3]	V_{EEA} to +0.5V
REF+, REF-, current, externally forced[3]	±3mA

Outputs

OUT+, OUT–, applied voltage (measured to A_{GND})[2]	–2.0 to +2.0V
OUT+, OUT–, current, externally forced[3]	+50mA
Short-circuit duration (single output to GND)	unlimited

Temperature

Operating, ambient	
(Plastic Package)	–20 to +90°C
(Ceramic Package)	–60 to +150°C
Junction	
(Plastic Package)	+140°C
(Ceramic Package)	+200°C
Lead, soldering (10 seconds)	+300°C
Storage	–65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range (Standard) Min	Nom	Max	Units
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	V
V_{EED}	Negative Supply Voltage (Measured to D_{GND})	–4.9	–5.2	–5.5	V
V_{EEA}	Negative Supply Voltage (measured to A_{GND})	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	V
V_{EEA}	Negative Supply Voltage (Measured to V_{EED})[1]	–20	0	20	mV
t_{PWL}	CONV Pulse Width LOW (to Meet Specification)	20			ns
t_{PWH}	CONV Pulse Width HIGH (to Meet Specifications)	20			ns
t_S	Setup Time, Data to CONV (to Meet Specification)	25			ns
t_H	Hold Time (to Meet Specifications)	1			ns
t_{SF}	Setup Time, Data to FT	5			ns
t_{HF}	Hold Time, Data to FT	28			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
V_{REF}	Reference Voltage (REF–)	–0.7	–1.0	–1.3	V
I_{REF}	Reference Current (REF+)	400	625	700	µA
C_C	Compensation Capacitor	0.01	0.1		µF
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. A common power supply isolated with ferrite bead inductors is recommended for V_{EEA} and V_{EED}. This is shown in the *Typical Interface Circuit*.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range (Standard) Min	Max	Units
$I_{EEA}+I_{EED}$		$V_{EEA}=V_{EED}$=Max, static T_A=0 to 70°C		–180	mA
		T_A=70°C		–150	mA
I_{CC}		V_{CC}=Max, Static T_A=0 to 70°C		25	mA
		T_A=70°C		20	mA
C_{REF}	Reference Input Capacitance			15	pF
C_I	Digital Input Capacitance			15	pF
V_{OC}	Compliance Voltage		–1.2	1.2	V
R_O	Output Resistance		12		kΩ
C_O	Output Capacitance			45	pF
I_O	Full-Scale Output Current	I_{REF}=Nominal	40		mA
I_{IL}	Input Current, Logic LOW	V_{CC},V_{EE}=Max , V_I=0.4V	–10	50	µA
I_{IH}	Input Current, Logic HIGH	V_{CC},V_{EE}=Max, V_I=2.4V	–10	100	µA
I_{IM}	Input Current, Max Input Voltage	V_{CC},V_{EE}=Max, V_I=V_{CC} Max	–10	100	µA
V_{TH}	Logic Input Threshold Voltage,Typical	V_{CC},V_{EE}=Nom, T_A=25°C	1.25	1.55	V

Switching characteristics

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
F_D	Maximum Data Rate	V_{EEA}, V_{EED}, V_{CC}=Min	20	25		MHz
t_{DC}	Clock to Output Delay	V_{EEA}, V_{EED}, V_{CC}=Min, FT=LOW			17	ns
t_{DD}	Data to Output Delay	V_{EEA}, V_{EED}, V_{CC}=Min, FT=HIGH			35	ns
t_{DF}	FT to Output Delay	V_{EEA}, V_{EED}, V_{CC}=Min			35	ns
t_R	Risetime	90% to 10% of FSR, FT=LOW			4	ns
t_F	Falltime	10% to 90% of FSR, FT=LOW			4	ns
t_{SET}	Settling Time, Voltage	FT=LOW, Full-Scale Voltage transition on I_{OUT} to ±0.0188%FSR		20	30	ns

System performance characteristics

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
E_{LD}	Differential Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1041			±0.1	%
		TDC1041-1			±0.05	%
E_{LI}	Integral Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1041			±0.1	%
		TDC1041-1			±0.05	%
V_{OS}	REF+ to REF- Offset Voltage		–10		+10	mV
I_B	REF- Input Bias Current				5	µA
E_G	Absolute Gain Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom	–5		5	%
I_{OF}	Output Offset Current	V_{EEA}, V_{EED}, V_{CC}= Min, $D_{1\text{-}10}$=LOW			±40	µA
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[2]			–50	dB
PSS	Power Supply Sensitivity	V_{CC}, V_{EEA}, V_{EED}=4%, I_{REF}= Nom			–140	µA/V
G_A	Peak Glitch Area			25	45	pV-sec
SFDR	Spurious Free Dynamic Range	I_{REF}=Nom, 20 Msps, 10MHz bandwidth F_{out}=6MHz	60			dBc
		F_{out}=5MHz		70		dBc
		F_{out}=2MHz		75		dBc
		F_{out}=1MHz		78		dBc

Notes: 1. OUT- connected to A_{GND}, OUT+ driving virtual ground.

2 120 Hz, 0.6Vp-p ripple on V_{EEA} and V_{EED}. dB relative to 0.6Vp-p ripple input.

Applications Information

There are three major D/A architectures: segmented, weighted current sources, and R-2R. In segmented there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N current sources. A weighted current source D/A has one current source for each bit of input with a binary weighting for the current sources. In an R-2R D/A, there is one current source per bit, and a resistor network which scales the current sources to have a binary weighting.

When transitioning from a code of 0111111111 to 100000000000, both the R-2R D/A and Binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where all current sources are either on or off, resulting in a glitch. In a segmented architecture, 511 of the current sources remain on, and one more is turned on to increment the output no possibility of a glitch.

The TDC1041 uses a hybrid architecture with the 6 MSBs segmented, and the 4 LSBs from a R-2R network. The result is a converter which has very low-glitch energy, and a moderate die size.

Layout, Power and Grounding

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided at the TDC1041. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1041 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected (typically through a ferrite bead inductor) to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1 Volts.

Direct Digital Synthesis Applications

There are many factors that can influence the system performance of a direct digital synthesizer. The following comments are directed at getting the best possible performance from the TDC1041, as measured by Spurrious Free Dynamic Range (SFDR).

The termination of the output pins has an effect on DAC performance. For most synthesis applications, optimum signal purity is obtained with the use of a balun (a simple RF transformer made by wrapping a few turns of wire around a ferrite core). This configuration has the benefit of cancelling common mode distortion.

Harmonic distortion may improve even further with reduced AC termination impedance values, at the expense of lowered output voltage.

An output amplifier is not recommended because any amplifier will add extra distortion of its own, which is likely to be much greater than that present from the direct outputs of the TDC1041.

One detrimental effect in DAC performance is capacitive coupling of the digital data into the output terminal. The actual digital-data waveform which represents a sine wave contains strong harmonics of that sine wave. This can be seen by connecting a digital data line to the input of an analog spectrum analyzer. Therefore data feedthrough to the analog output of a system due to improper board layout or system shielding and grounding will appear as additional harmonic distortion, adversely affecting SFDR.

The strict adherence to at least the minimum input data setup and hold times is important for the realization of the optimal performance. Spur levels may decrease as setup and hold times are increased. It is possible to achieve even higher performance in some instances by carefully "tuning" the input data setup and hold times (slightly delaying or advancing the CONV signal in relation to the data) fed to the TDC1041. The ***Operating conditions*** table has two sets of data for t_S and t_H, one which guarantees performance of the device in most applications, and one, more conservative specification which has been found to be optimal for DDS applications.

The purity of the output of the TDC1041 is greater than that which can be measured by many spectrum analyzers. The spectral plots shown in this data sheet were generated with an HP8568B, which has a noise floor barely below that of the TDC1041, once the TDC1041 performance has been optimized. When making spectral measurements it is important to remember that the TDC1041 output power is +4dBm, which is greater power than many analyzers are

equipped to handle without adding distortion of their own. Accordingly, it may be necessary to introduce an attenuator to the input of the spectrum analyzer to see the true DAC performance.

Output Termination

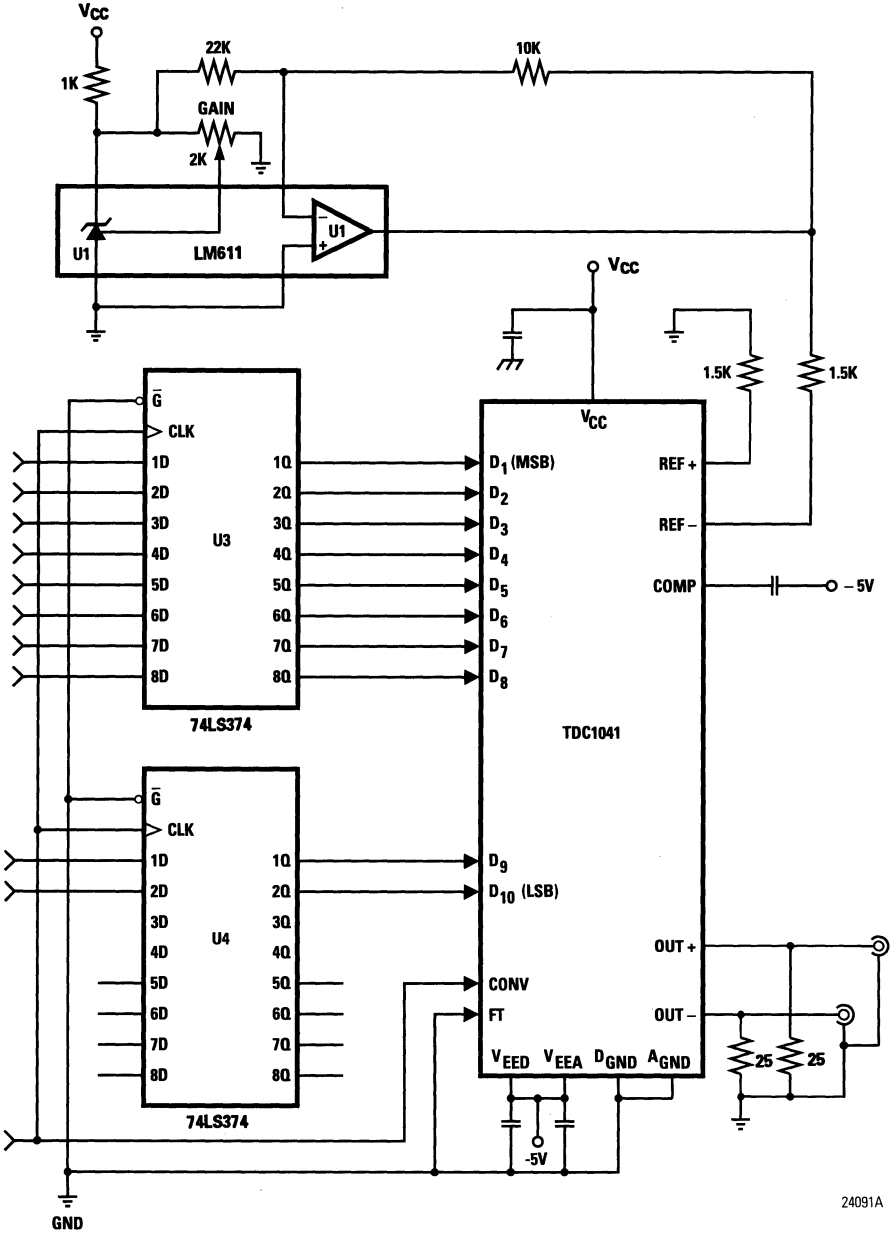
The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a 50Ω transmission line. With this load, the output voltage range of the converter is 0 to –1.0V. If a load is capacitively coupled to the TDC1041, it is recommended that a 25Ω load at DC, as seen by the TDC1041, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the ***Electrical Characteristics*** table, or the accuracy may be impaired.

Optimum DC linearity is obtained by using a differential output either with a balun, or an operational amplifier in the differential mode. If it is desired that the TDC1041 be operated in a single ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 5***. The CONV signal provided to the TDC1041 must be as free from clock jitter as possible. Clock jitter is the random cycle-to- cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory, although not as jitter free as a crystal oscillator.

Driving a 75Ω Transmission line

The TDC1041 has been optimized to operate with a reference current of 625μA. Significantly increasing or decreasing this current may degrade the performance of the device. If it is desired that the device drive a 37.5Ω load (75Ω source termination driving 75Ω transmission line) rather than the 25Ω suggested load, then V_{REF} should be held at 1V and I_{REF} reduced to 417μA. This will result in a 1V p-p voltage being generated at the DAC output.

Figure 5. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1041R3C	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1041R3C
TDC1041R3C1	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1041R3C1

40G06718 Rev C 8/93

TDC1112
Monolithic Digital-to-Analog Converter
12-Bit, 50 Msps, 12 ns Settling Time to 0.1%, 70 dB SFDR

Description

The TDC1112 is a ECL compatible, 12-bit monolithic D/A converter capable of converting digital data into an analog current at data rates in excess of 50 Megasamples-per second (Msps).

The analog circuitry has been optimized for dynamic performance, with very low glitch energy. The output is able to drive a 50Ω load with 1 Volt outputs while keeping a spurious-free-dynamic range greater than 70 dB.

Data registers are incorporated on the chip. This eliminates the temporal data skew encountered with external registers and latches and minimizes the glitches that can adversely affect many applications.

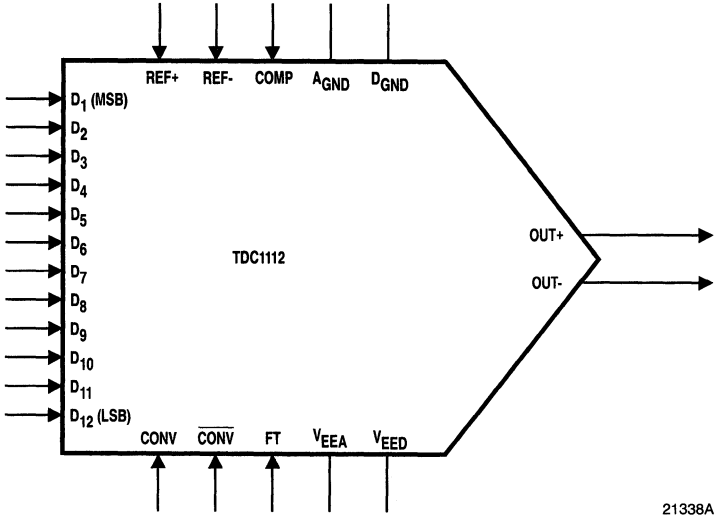
Features

- 12-bit resolution
- 50 Msps data rate
- ECL inputs
- Very low-glitch with no track and hold circuit needed
- Dual +4 dBm (1V into 50Ω) outputs make output amplifiers unnecessary in many applications
- 70 dB typical spurious-free-dynamic-range
- Available compliant to MIL-STD-883C

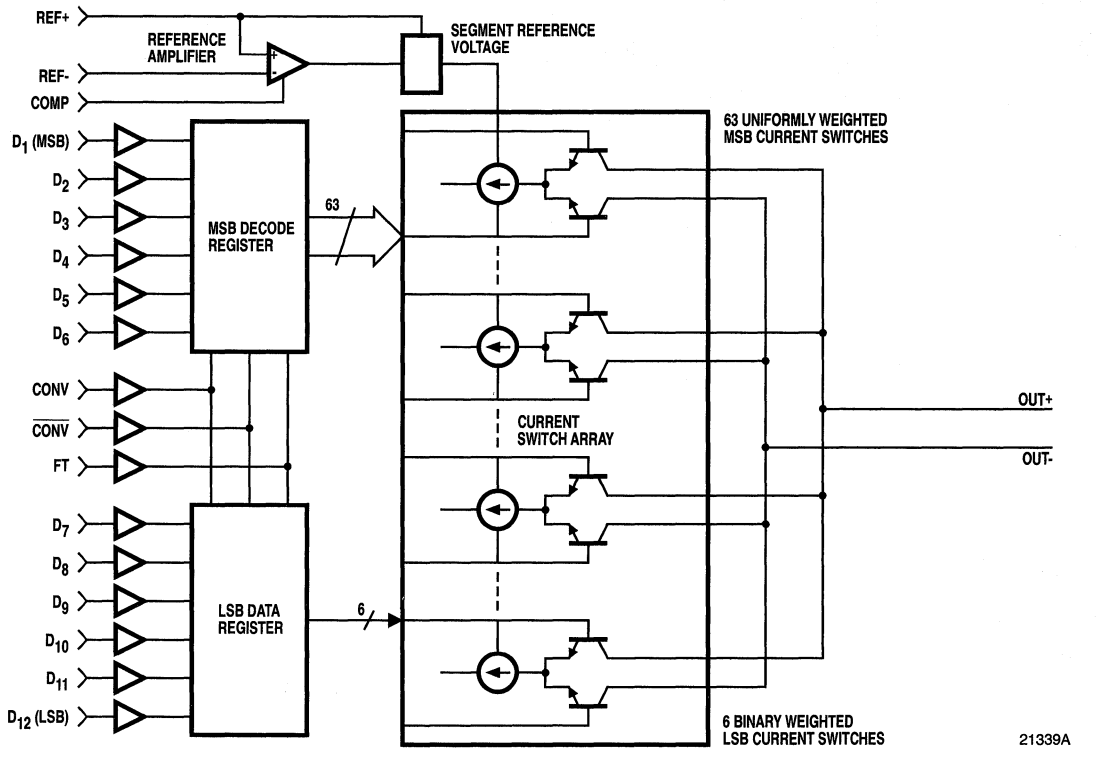
Applications

- Direct digital RF signal generation
- Test signal generation
- Arbitrary waveform synthesis
- Broadcast and studio video
- High-resolution A/D converters

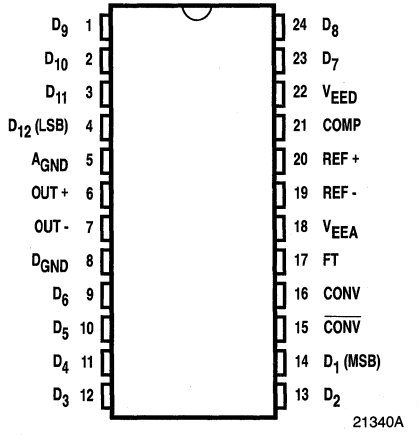
Interface Diagram



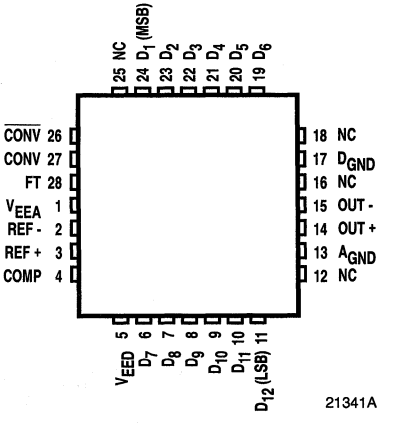
Functional Block Diagram



Pin Assignments



24 Pin Hermetic Ceramic DIP – J7 Package
24 Pin Plastic DIP – N7 Package



28 Contact Chip Carrier – C3 Package
28 Leaded Plastic Chip Carrier – R3 Package

Functional Description

General Information

The TDC1112 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

There are three major D/A architectures: thermometer code segmentation, weighted current sources, and R–2R. In thermometer code segmentation there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N current sources. A weighted current source D/A has one current source for each bit of input with a binary weighting for the current sources. In an R–2R D/A, there is one current source per bit, and a resistor network which scales the current sources to have a binary weighting.

When transitioning from a code of 011111111111 to 100000000000, both the R–2R D/A and binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where all current sources are either on or off, resulting in a glitch. In a segmented architecture, 2047 of the current sources remain on, and one more is turned on to increment the output-no possibility of a glitch.

The TDC1112 uses a hybrid architecture with the 6 MSBs segmented, and the 6 LSBs from a R–2R network. The result is a converter which has very low glitch energy, and a moderate die size.

Power, Grounds, and Layout

The TDC1112 requires a single –5.2V power supply. The analog (V_{EEA}) and digital (V_{EED}) supply voltages should be decoupled from each other, as shown in the ***Typical Interface Circuits***, to provide the highest noise immunity. The 0.1μF decoupling capacitors should be placed as close as possible to the power pins. The inductors are simple ferrite beads and are neither critical in value nor always required.

The high slew-rates of digital data make capacitive coupling with the D/A output a real problem. Since the digital signals contain high-frequency harmonics of the clock, as well as the signal that is being provided to the DAC, the result of data feedthrough often looks like harmonic distortion which degrades the Spurious-Free-Dynamic-Range (SFDR) performance of the D/A.

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided at the TDC1112. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1112 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected (typically through a ferrite bead inductor) to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1V.

Reference

The TDC1112 has two reference inputs: REF+ and REF–. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF– pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT}\,(\text{Input Code N}) = N \times \frac{I_{REF}}{64}$$

This means that with an I_{REF} that is nominally 625μA, the full scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω load total) with a 1V peak-to-peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so that the effect of amplifier input bias current is minimized.

Reference (cont.)

The TDC1112 has been optimized to operate with a reference current of 625μA. Significantly increasing or decreasing this current may degrade the performance of the device. The minimum and maximum values for V_{REF} and I_{REF} are listed in the ***Operating Conditions Table***.

The internal reference amplifier is externally compensated to assure stability. To compensate this amplifier, a 0.1μF capacitor should be connected between the COMP pin and V_{EEA}. The amplifier has been optimized to minimize the TDC1112 settling time, and as a result should be considered a DC amplifier. Performance of the TDC1112 operating in a multiplying D/A mode is not guaranteed.

A typical interface circuit that includes a stable, adjustable reference circuit is shown in ***Figures 9a-c***.

Digital Inputs

The data inputs are single-ended ECL compatible. The TDC1112 is specified with two sets of setup and hold times. One of these pairs of specifications guarantees the performance of the TDC1112 to specifications listed in the minimum and maximum columns of the ***System Performance Characteristics Table***. The second more rigid specification is recommended for applications where lowest possible glitch and highest SFDR are desired. The more stringent t_S and t_H insure that the data will not be slewing during times critical to the TDC1112, and will hence minimize the effects of capacitively coupled data feedthrough and optimize SFDR performance. Another method reducing the effect of capacitive coupling is to slow down the slew rates of the digital inputs. This has been done in the circuit shown in ***Figures 9a-c*** by the addition of 50Ω series resistors to the data lines.

Clock and Feedthrough Control

The TDC1112 requires an ECL clock signal (CONVert and $\overline{\text{CONVert}}$). Even though complementary operation is preferred, a single-ended signal may be used if either unused CONV input is biased at a DC voltage midway between the active input's V_{IH} and V_{IL} levels.

Data is synchronously entered on the rising edge of CONV (the falling edge of $\overline{\text{CONV}}$). The CONV input is ignored in the Feedthrough (FT=HIGH) mode.

The Feedthrough (FT) pin is normally held LOW, in which case the TDC1112 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided, and this pin may be left open for clocked operation. For certain applications, such as high-precision successive approximation A/D converters, speed may be more important then glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronous in response to the digital input, without the need for a clock.

Since skew in the bits of the input word will result in glitches, and may affect settling time, it is recommended that the TDC1112 be operated in clocked mode for most applications.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By loading the current source outputs with a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to −40mA output current (0 to −1V when terminated in 25Ω) as the input code varies from 0000 0000 0000 to 1111 1111 1111. OUT− varies in a complementary manner from −40 to 0mA (−1 to 0V when terminated with 25Ω) over the same code range. (See the ***Output Coding Table***.) The output current is proportional to the reference current and the input code.

The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a 50Ω transmission line. With this load, the output voltage range of the converter is 0 to −1.0V. If a load is capacitively coupled to the TDC1112, it is recommended that a 25Ω load at DC, as seen by the TDC1112, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the ***Electrical Characteristics Table***, or the accuracy may be impaired.

See ***Figure 9b*** for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output either with a balun, or an operational amplifier in the differential mode. If it is desired that the TDC1112 be operated in a single ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 9c***.

Package Interconnections

Signal Type	Signal Name	Function	Value	J7, N7 Package Pins	C3, R3 Package Pins
Power	V_{EEA}	Analog Supply Voltage	−5.2V	18	1
	V_{EED}	Digital Supply Voltage	−5.2V	22	5
	A_{GND}	Analog Ground	0.0V	5	13
	D_{GND}	Digital Ground	0.0V	8	17
Reference	REF−	Reference Voltage Input	−1.0V	19	2
	REF+	Reference Current Output	0.625mA	20	3
	COMP	Compensation Capacitor	0.1μF, See Text	21	4
Data Input	D_1 (MSB)	Most Significant Bit Input	ECL	14	24
	D_2		ECL	13	23
	D_3		ECL	12	22
	D_4		ECL	11	21
	D_5		ECL	10	20
	D_6		ECL	9	19
	D_7		ECL	23	6
	D_8		ECL	24	7
	D_9		ECL	1	8
	D_{10}		ECL	2	9
	D_{11}		ECL	3	10
	D_{12} (LSB)	Least Significant Bit Input	ECL	4	11
Feedthrough	FT	Feedthrough Mode Control	ECL	17	28
Convert (Clock)	CONV	Convert (Clock) Input	ECL	16	27
	$\overline{\text{CONV}}$	Convert (Clock) Input	ECL	15	26
Analog Output	OUT+	Analog Output	0 to −40mA	6	14
	OUT−	Analog Output	−40 to 0mA	7	15

Output Coding Table [1]

Input Data MSB		D_{1-12} LSB	OUT+ (mA)	V_{OUT+} (mV)	OUT− (mA)	V_{OUT-} (mV)
0000	0000	0000	0.000	0.00	40.000	−1000.00
0000	0000	0001	0.009	−0.24	39.990	−999.75
0000	0000	0010	0.019	−0.49	39.980	−999.52
	•		•	•	•	•
	•		•	•	•	•
	•		•	•	•	•
0111	1111	1111	19.995	−499.88	20.005	−500.12
1000	0000	0000	20.005	−500.12	19.995	−499.88
	•		•	•	•	•
	•		•	•	•	•
	•		•	•	•	•
1111	1111	1101	39.980	−999.52	0.019	−0.49
1111	1111	1110	39.990	−999.75	0.009	−0.24
1111	1111	1111	40.000	−1000.00	0.000	0.00

Note: 1. $I_{REF}=625\mu A$, $R_{LOAD}=25\Omega$.

Figure 1. Timing Diagram

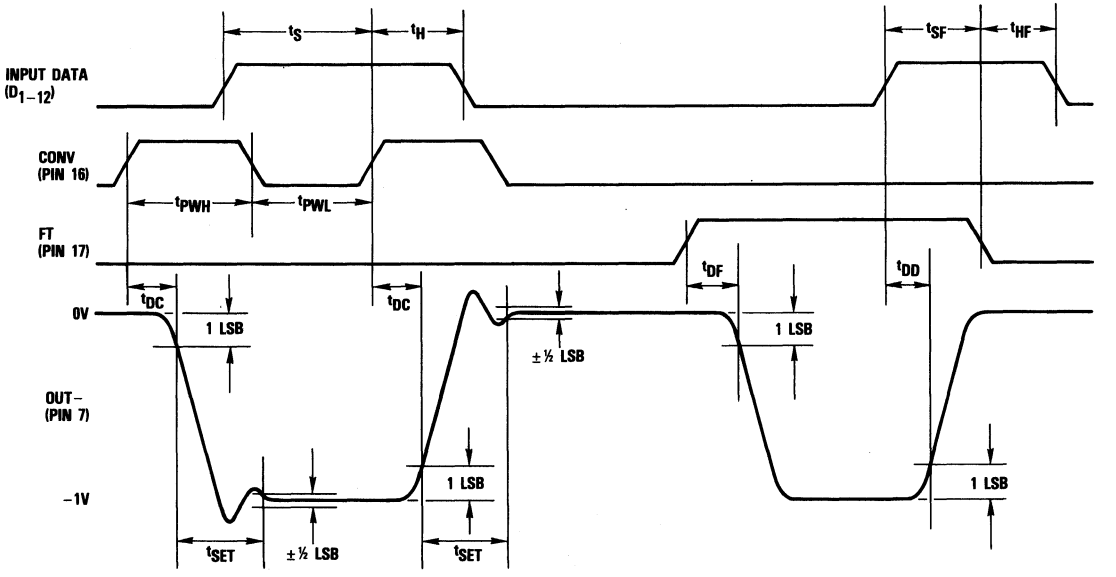


Figure 2a. Equivalent Input Circuit (Data and FT)

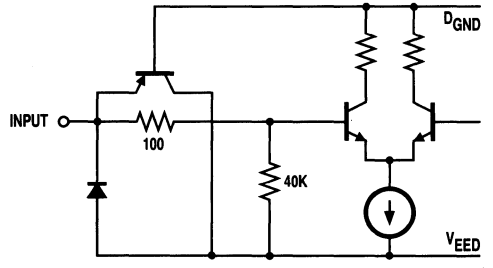


Figure 2b. Equivalent Input Circuit (CONV and $\overline{CONV}$)

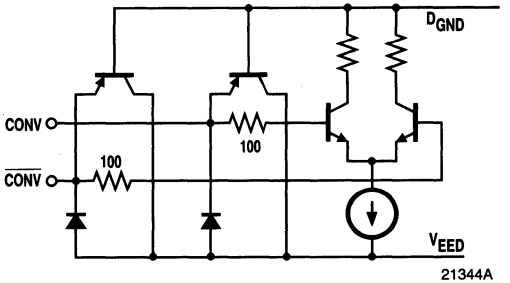


Figure 3. Equivalent Reference and Output Circuits

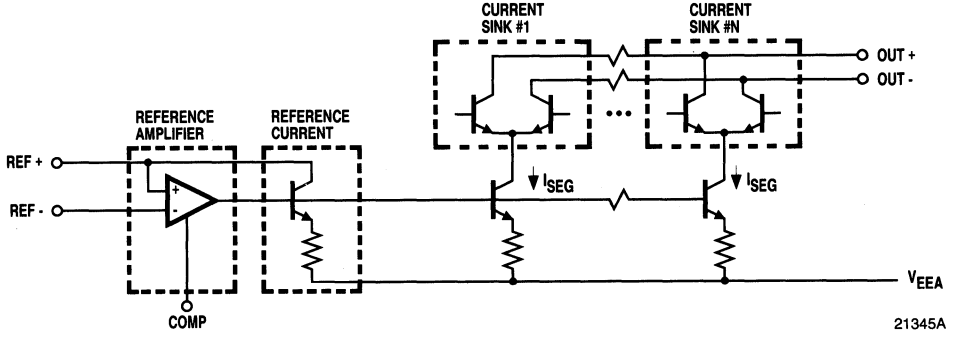


Figure 4. Standard Test Load

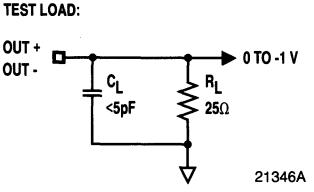
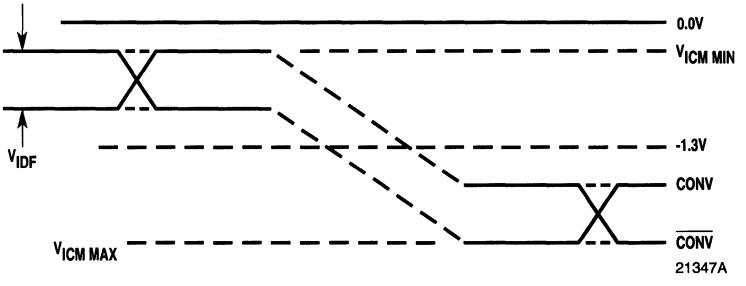


Figure 5. CONV and $\overline{CONV}$ Switching Levels



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EEA} (measured to A_{GND})	−7.0 to +0.5V
V_{EEA} (measured to V_{EED})	−50 to +50mV
V_{EED} (measured to D_{GND})	−7.0 to +0.5V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Inputs

Applied voltage	
CONV, $\overline{\text{CONV}}$, FT, $D_{1\text{-}12}$ (measured to D_{GND}) [2]	V_{EED} to +0.0V
REF+, REF− (measured to A_{GND}) [2]	V_{EEA} to +0.0V
Applied current	
REF+, REF−, externally forced (measured to A_{GND}) [3,4]	±3mA
Digital inputs	±3mA

Outputs

Applied voltage	
OUT+, OUT− (measured to A_{GND}) [2]	−2.0 to +2.0V
Applied current	
OUT+, OUT−, externally forced (measured to A_{GND}) [3,4]	+50mA
Short-circuit duration (single output to GND)	Unlimited

Temperature

Operating, ambient (plastic package)	−20 to +90°C
(ceramic package)	−60 to +150°C
junction (plastic package)	+140°C
(ceramic package)	+200°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Commercial			Military			
		Min	Nom	Max	Min	Nom	Max	
F_S	Clock Frequency	0		50	0		50	MHz
V_{EEA}	Analog Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to V_{EED}) [1]	−20	0.0	+20	−20	0.0	+20	mV
V_{EED}	Digital Supply Voltage (measured to D_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{REF}	Reference Voltage, REF−	−0.7	−1.0	−1.3	−0.7	−1.0	−1.3	V
I_{REF}	Reference Current, REF+	0.550	0.625	0.700	0.575	0.625	0.675	mA
C_C	Compensation Capacitor	0.01	0.1		0.01	0.1		μF
V_{IL}	Digital Input Voltage, Logic LOW			−1.55			−1.60	V
V_{IH}	Digital Input Voltage, Logic HIGH	−1.05			−1.00			V
t_S	Input Data Setup Time	17			18			ns
t_S	Input Data Setup Time [2]	24			24			ns
t_H	Input Data Hold Time	0			0			ns
t_H	Input Data Hold Time [2]	4			4			ns
t_{SF}	Setup Time, Data to FT			7			7	ns
t_{HF}	Hold Time, Data to FT			24			24	ns
V_{ICM}	CONV Input Voltage, Common Mode Range [3]	−0.5		−2.0	−0.5		−2.0	V
V_{IDF}	CONV Input Voltage, Differential [3]	0.4		1.2	0.4		1.2	V
t_{PWL}	CONV Pulse Width LOW							
	⩾ 40Msps	10.5			10.5			ns
	< 40Msps	11			11			ns
t_{PWL}	CONV Pulse Width LOW [2]	18			18			ns
t_{PWH}	CONV Pulse Width HIGH							
	⩾ 40Msps	8.0			8.5			ns
	< 40Msps	9.0			9.0			ns
t_{PWH}	CONV Pulse Width HIGH [2]	11			11			ns
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Notes:
1. A common power supply, isolated simply with ferrite bead inductors, is recommended for V_{EEA} and V_{EED}. See the Typical Interface Circuits, Figures 9a-c.
2. SFDR sensitive applications.
3. See Figure 5., CONV, CONV Switching Levels.

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Commercial		Military		
			Min	Max	Min	Max	
I_{EE}	Supply Current ($I_{EEA}+I_{EED}$) [2]	V_{EEA}=Max [3]		−180		−195	mA
		T_A=70 °C		−150			mA
		T_C=125°C				−145	mA
C_{REF}	Reference Input Capacitance	REF+, REF−		15		15	pF
C_I	Digital Input Capacitance	D_{1-12}, FT, CONV, $\overline{CONV}$		15		15	pF
I_{IL}	Digital Input Current, Logic LOW	V_{EED}=Max, V_I=−1.85V	−10	200	−10	250	μA
I_{IH}	Digital Input Current, Logic HIGH	V_{EED}=Max, V_I=−0.8V	−10	200	−10	250	μA
I_{IC}	CONV Input Current	V_{EED}=Max, −1.85V<V_I<−0.8V		50		50	μA
R_O	Output Resistance	OUT+, OUT−	12		12		kOhms
C_O	Output Capacitance	OUT+, OUT−		45		45	pF
V_{OC}	Output Compliance Voltage	OUT+, OUT−	−1.2	+1.2	−1.2	+1.2	V
I_O	Full-Scale Output Current	OUT+, OUT−	40		40		mA

Notes:
1. Worst case over all data and control states.
2. See the Typical Supply Current vs. Temperature graph (Figure 6) for typical values.
3. Standard test load, Figure 4.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Commercial			Military			
			Min	Typ	Max	Min	Typ	Max	
F_S	Maximum Clock Rate [1,2,3]	V_{EEA}, V_{EED}=Min, FT=LOW	50			50			Msps
t_{DC}	Clock to Output Delay [2,3]	V_{EEA}, V_{EED}=Min, FT=LOW			20			20	ns
t_{DD}	Data to Output Delay [2,4]	V_{EEA}, V_{EED}=Min, FT=HIGH			25			25	ns
t_{DF}	FT to Output Delay [2]	V_{EEA}, V_{EED}=Min			30			30	ns
t_R	Output Risetime [3]	90% to 10% of FSR, FT=LOW		2	4		2	4	ns
t_F	Output Falltime [3]	10% to 90% of FSR, FT=LOW		2	4		2	4	ns
t_{SET}	Output Voltage Settling Time [2,5,6]	FT=LOW, Worst Case Full-Scale Voltage Transition on OUT−							
		to 0.1% FS (4 LSB or 10 Bits)		12	20		13		ns
		to 0.05% FS (2 LSB)		17			14		ns
		to 0.0188% FS (3/4 LSB)		20	30		18	35	ns
		to 0.0125% FS (1/2 LSB)		25	35		25		ns

Notes:
1. F_S is limited only by t_{PWL}, t_{PWH}, t_S and t_H requirements.
2. See Figure 1., Timing Diagram.
3. Clock Mode.
4. Feedthrough Mode.
5. Standard test load, Figure 4.
6. See the Typical Output Voltage Settling Time vs. Settling Accuracy curve.

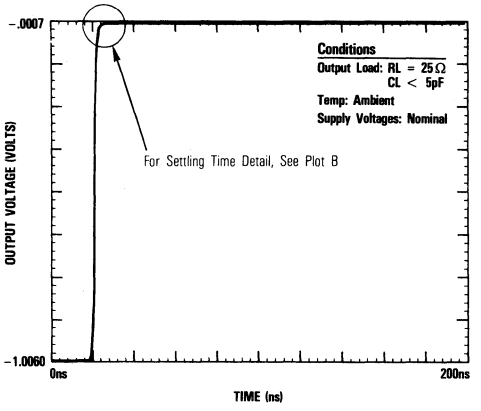
System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Commercial			Military			
			Min	Typ	Max	Min	Typ	Max	
E_{LI}	Linearity Error, Integral (Terminal Based)	Note 1,							
		TDC1112			±0.096			±0.096	%
		TDC1112-1			±0.048			±0.048	%
		TDC1112-2			±0.048			±0.048	%
		TDC1112-3			±0.024			±0.024	%
E_{LD}	Linearity Error, Differential	Note 1,							
		TDC1112			±0.096			±0.096	%
		TDC1112-1			±0.048			±0.048	%
		TDC1112-2			±0.024			±0.024	%
		TDC1112-3			±0.012			±0.012	%
SFDR	Spurious-Free Dynamic Range [2]	32Msps,							
		F_{OUT}=12MHz	55	67			67		dB
		F_{OUT}=10MHz		68		54	68		dB
		40Msps,							
		F_{OUT}=16MHz		63			63		dB
		F_{OUT}=5MHz		70			70		dB
		F_{OUT}=1MHz		72			72		dB
E_G	Absolute Gain Error	Note 3		±1	±5		±1	±5	%
TC_{EG}	Gain Error Temperature Coefficient	Note 3		±30			±30		ppm/°C
I_{OF}	Output Offset Current	Note 4		±0.1	±5		±0.1	±5	μA
TC_{OF}	Offset Temperature Coefficient	Note 5		±2			±2		μV/°C
V_{OS}	REF+ to REF- Offset Voltage			±1.5	±10		±1.5	±10	mV
I_B	REF- Input Bias Current				5			10	μA
PSRR	Power Supply Rejection Ratio	Note 6			-50			-48	dB
PSS	Power Supply Sensitivity	Note 7			-140			-140	μA/V
DP	Differential Phase	Note 8		0.2					Degree
DG	Differential Gain	Note 8		0.3					%
G_A	Peak Glitch Area [9]	FT=LOW		20	35		20	45	pV-sec

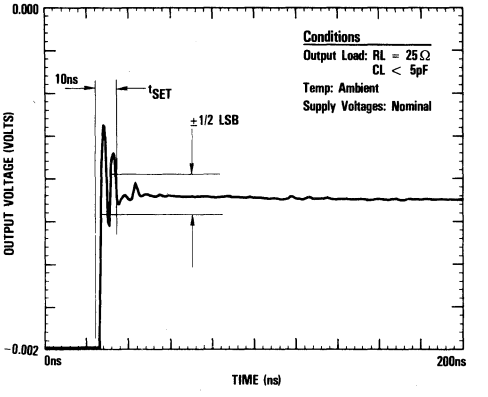
Notes:
1. OUT-connected to A_{GND}, OUT+driving virtual ground.
2. Circuit as shown in Figure 9a., I_{REF}=Nom.
3. V_{EED}, V_{EEA}, V_{REF}=Nom.
4. V_{EEA}, V_{EED}=Min, D1-12=LOW.
5. V_{EEA}, V_{EED}=Max, D1-12=LOW.
6. 120 Hz, 0.6Vp-p ripple on V_{EEA} and V_{EED}. dB relative to 0.6Vp-p ripple input. V_{EEA}, V_{EED}, I_{REF}=Nom.
7. V_{EEA}, V_{EED}=±4%, I_{REF}=Nom.
8. F_S=4xNTSC Subcarrier.
9. Worst case 1 LSB transition

Typical Performance Curves (Typical Settling Time Characteristics)

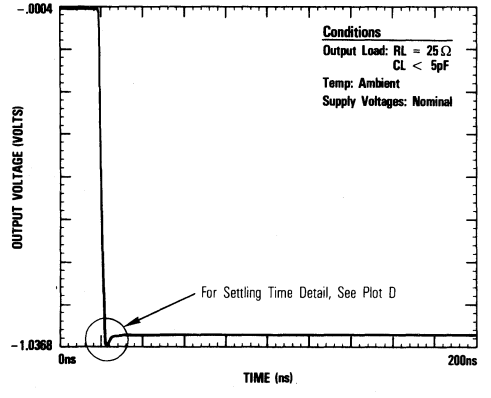
A. Full-Scale Output Transition, Rising Edge



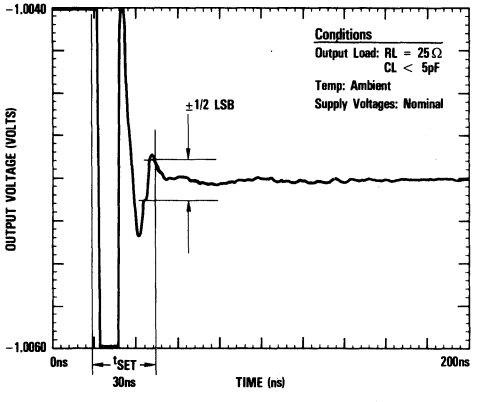
B. Settling Time, Full-Scale Output, Rising Edge



C. Full-Scale Output Transition, Falling Edge



D. Settling Time, Full-Scale Output, Falling Edge



E. Typical Settling Time vs. Settling Accuracy

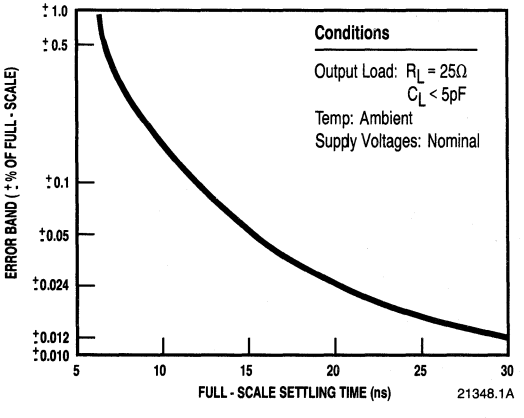


Figure 6. Typical Supply Current vs. Temperature

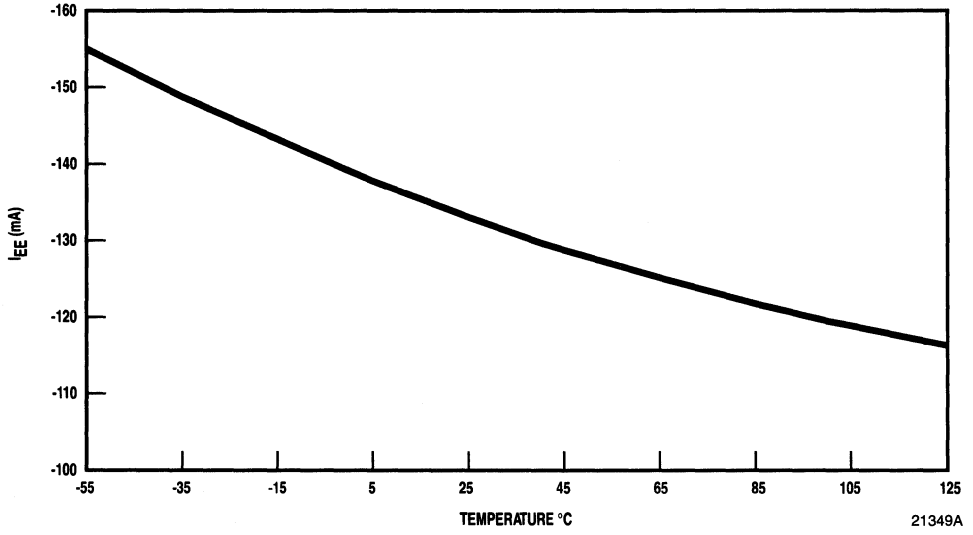


Figure 7. Typical Output Spectrum, 40MSPS, 13.336MHz F_{OUT}

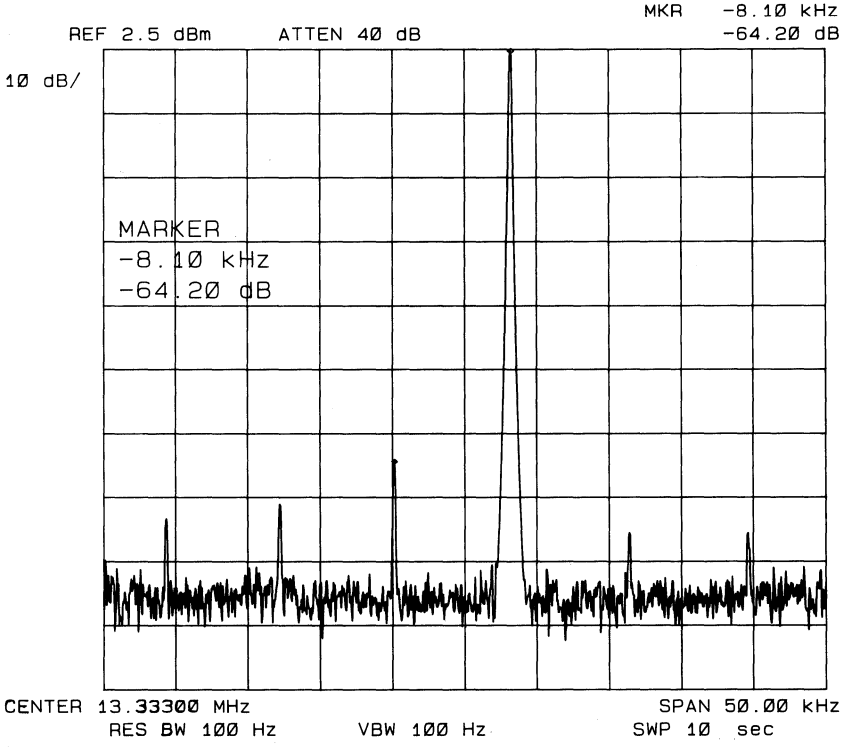
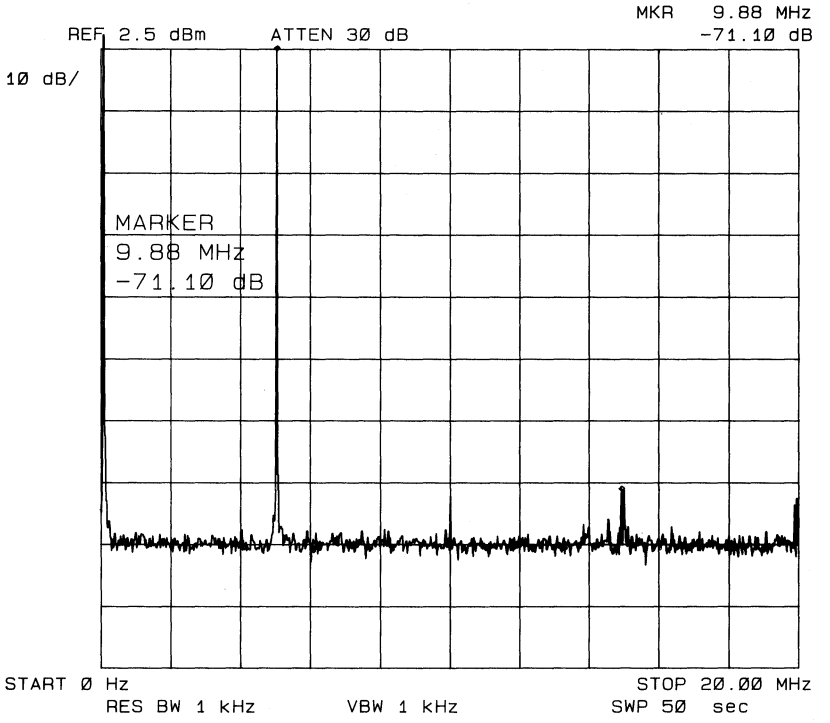


Figure 8. Typical Output Spectrum, 40Msps, 5MHz F_{OUT}



Application Discussion

Direct Digital Synthesis Applications

For most synthesis applications, optimum signal purity is obtained with the use of a balun (a simple RF transformer made by wrapping a few turns of wire around a ferrite core) as shown in ***Figure 9a***. This configuration has the benefit of cancelling common mode distortion.

An output amplifier is not recommended because any amplifier will add extra distortion of its own, which is likely to be much greater than that present from the direct outputs of the TDC1112.

The strict adherence to at least the minimum input data setup and hold times is important for the realization of the optimal performance. Spur levels may decrease as setup and hold times are increased. It is possible to achieve even higher performance in some instances by carefully "tuning" the input data setup and hold times (slightly delaying or advancing the CONV signal in relation to the data) fed to the TDC1112. The ***Operating Conditions Table*** has two sets of data for t_S and t_H, one which guarantees performance of the device in most applications, and one, more conservative specification which has been found to be optimal for DDS applications.

The actual digital-data waveform which represents a sine wave contains strong harmonics of that sinewave. This can be seen by connecting a digital data line to the input of an analog spectrum analyzer. Therefore, data feedthrough to the analog output of a system due to improper board layout or system shielding and grounding will appear as additional harmonic distortion, adversely affecting SFDR.

Harmonic distortion may improve even further with reduced AC termination impedance values, at the expense of lowered output voltage.

The purity of the output of the TDC1112 is greater than that which can be measured by many spectrum analyzers.

Direct Digital Synthesis Applications (cont.)

The spectral plots shown in *Figures 7 and 8* were generated with an HP8568B, which has a noise floor barely below that of the TDC1112, once the TDC1112 performance has been optimized. When making spectral measurements it is important to remember that the TDC1112 output power is +4dBm, which is greater power than many analyzers are equipped to handle without adding distortion of their own. Accordingly, it may be necessary to introduce an attenuator to the input of the spectrum analyzer to see the true DAC performance.

The CONV signal provided to the TDC1112 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory, although not as jitter free as a crystal oscillator.

Figure 9a. Typical Interface Circuit with Balun Output

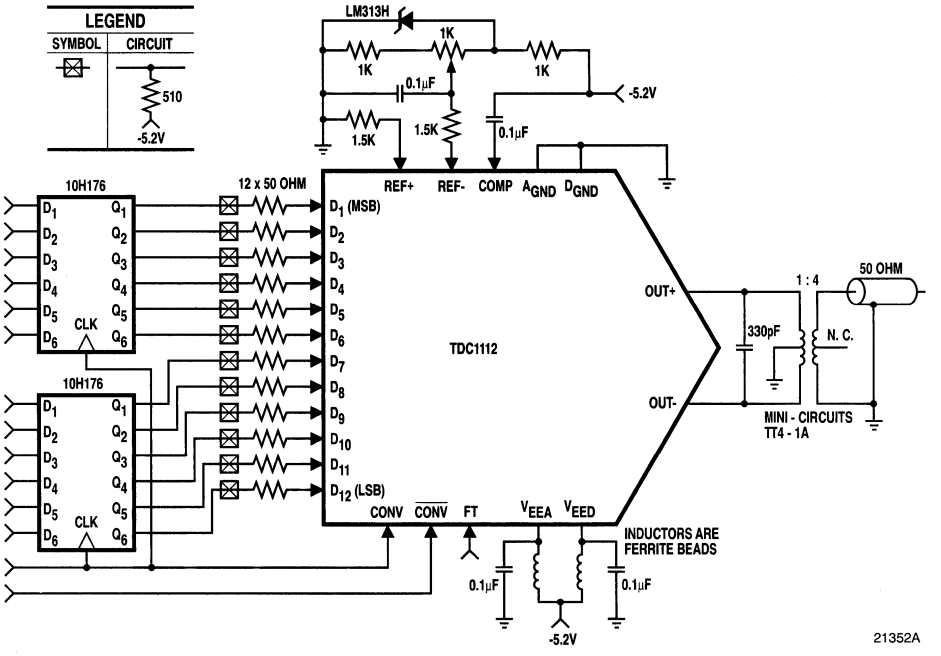


Figure 9b. Typical Interface Circuit with Bipolar, Differential Mode Operational Amplifier Output

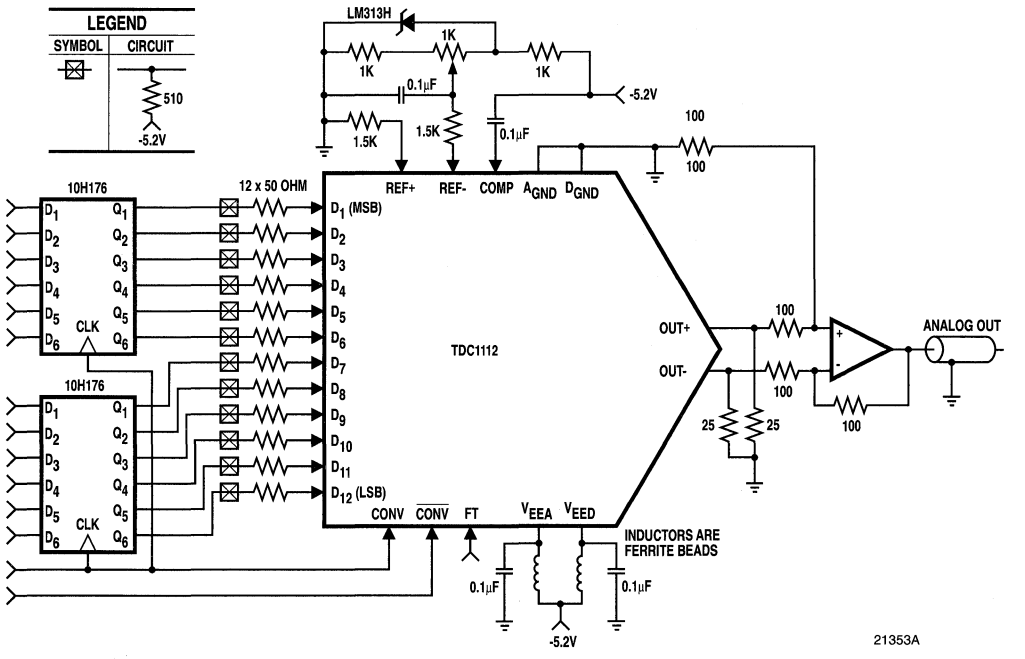
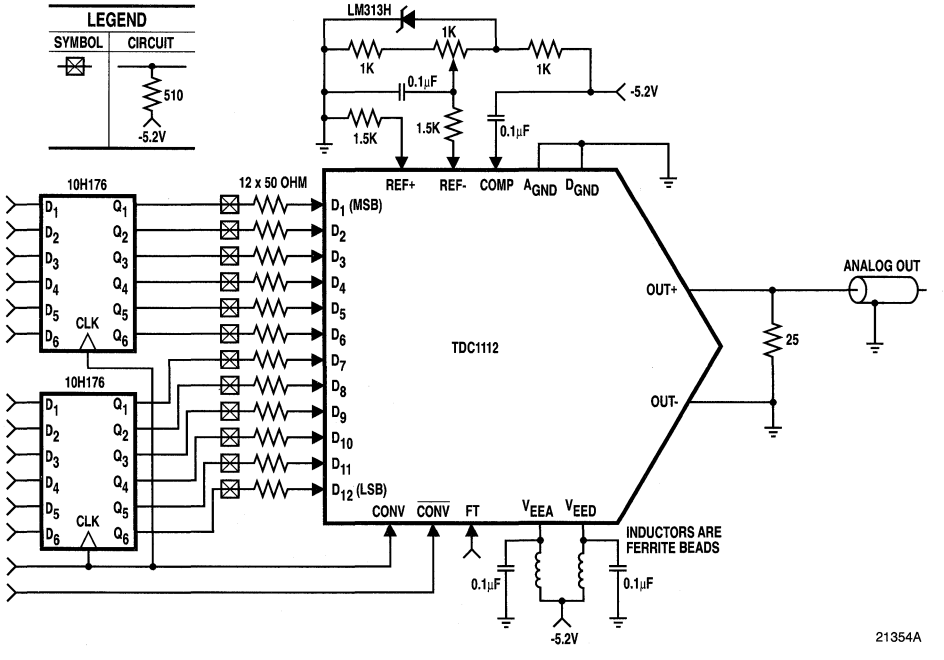


Figure 9c. Typical Interface Circuit with Resistive Load Output



Ordering Information

Product [1] Number	Temperature Range	Screening	Package	Package [1] Marking
TDC1112J7CX	STD – T_A = 0°C to 70°C	Commercial	24 Pin Hermetic Ceramic DIP	1112J7C-X
TDC1112J7VX	EXT – T_C = –55°C to 125°C	MIL-STD-883	24 Pin Hermetic Ceramic DIP	1112J7V-X
TDC1112N7CX	STD – T_A = 0°C to 70°C	Commercial	24 Pin Plastic DIP	1112N7C-X
TDC1112C3VX	EXT – T_C = –55°C to 125°C	MIL-STD-883	28 Contact Chip Carrier	1112C3V-X
TDC1112R3CX	STD – T_A = 0°C to 70°C	Commercial	28 Leaded Plastic Chip Carrier	1112R3C-X

Note: 1. The "X" in the product designation denotes the linearity grade, guaranteed over the operating temperature range, per the following table:

Linearity Grade (X)	None	1	2	3
E_{LD} Linearity Error, Differential	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)	±0.012% (1/2 LSB)
E_{LI} Linearity Error, Integral	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)

Not every grade is available in every package/screening/temperature range combination. Consult factory for availability.

40G02322 Rev D 8/93

TDC1141
Monolithic Digital-to-Analog Converter
10-Bit, 50 Msps, 12 ns Settling Time

Description

The TDC1141 is a ECL compatible, 10-bit monolithic D/A converter capable of converting digital data into an analog current or voltage at data rates in excess of 50 Megasamples-per second (Msps).

The analog circuitry has been optimized for dynamic performance, with very low glitch energy. The output is able to drive a 50Ω load with 1 Volt output levels while maintaining large spurious-free-dynamic range.

Data registers are incorporated on the TDC1141. This eliminates data skew encountered with external registers and latches and minimizes the glitches that can adversely affect many applications.

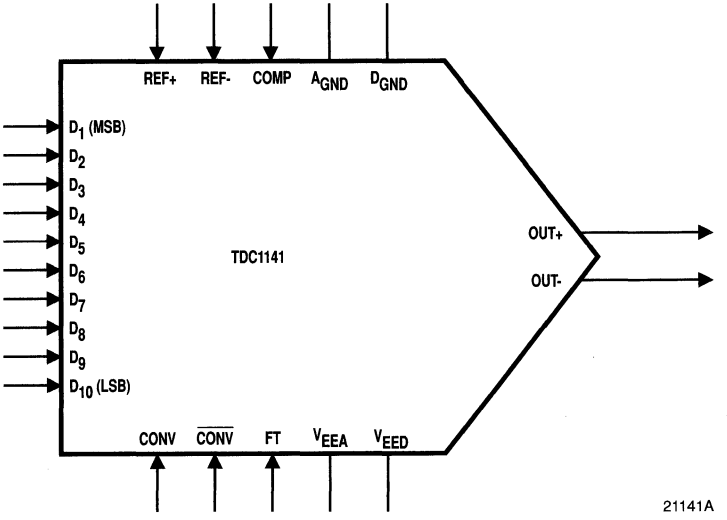
Features

- 10-bit resolution
- 50 Msps data rate
- ECL inputs
- Very low-glitch with no track and hold circuit needed
- Dual +4 dBm (1V into 50Ω) outputs make output amplifiers unnecessary in many application

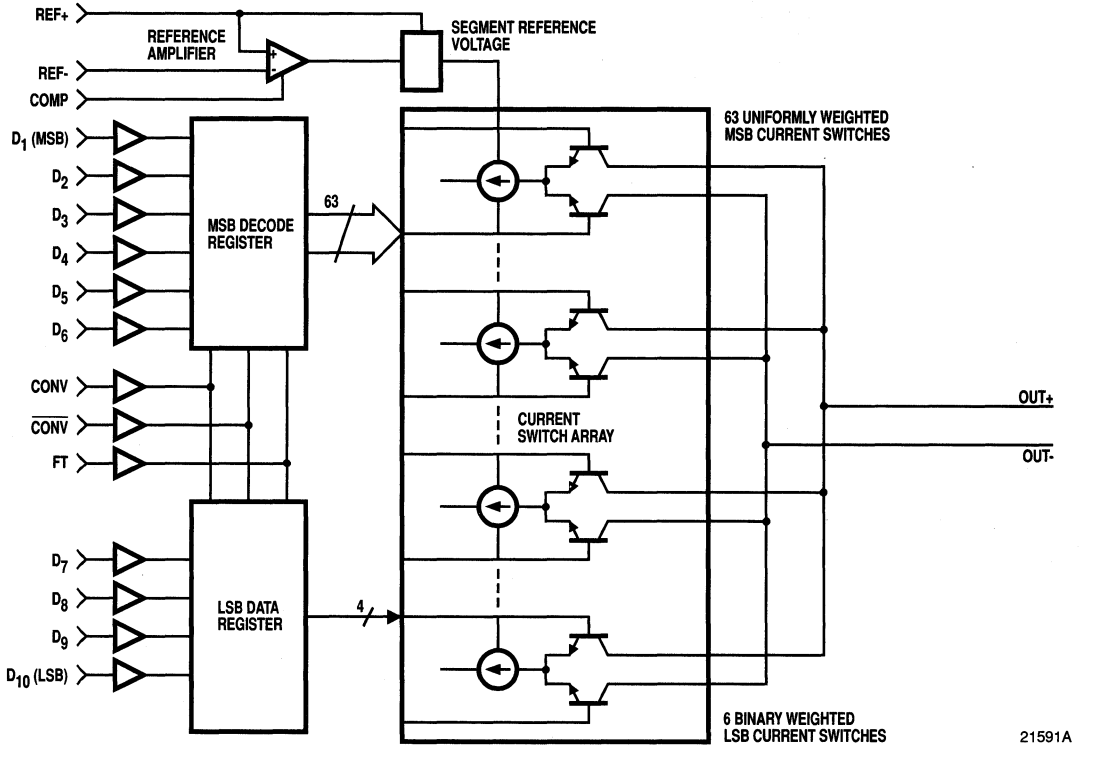
Applications

- Direct digital RF signal generation
- Test signal generation
- Arbitrary waveform synthesis
- Broadcast and studio video
- High-resolution A/D converters

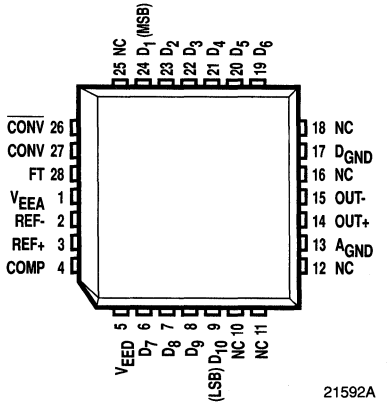
Interface Diagram



Functional Block Diagram



Pin Assignments



28 Leaded Plastic Chip Carrier – R3

Functional Description

General Description

The TDC1141 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

Power and Grounds

The TDC1141 requires a single –5.2V power supply. This supply is divided into analog (V_{EEA}) and digital (V_{EED}) supply pins which should be decoupled from each other. An example of this decoupling is shown in the ***Typical Interface Circuit***. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The

inductors are simple ferrite beads and are neither critical in value nor always required.

Reference and Compensation

The TDC1141 has two reference inputs: REF+ and REF–. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF– pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT} = N \times \frac{I_{REF}}{16}$$

Where N is the input code to the D/A converter

This means that with an I_{REF} that is nominally 625μA, the full-scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω load total) with a 1V peak to peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so that the effect of amplifier input bias current is minimized.

The internal reference amplifier is externally compensated to ensure stability. A 0.1μF capacitor should be connected between the COMP pin and V_{EEA}.

Digital Inputs

All digital inputs including the FT, CONV and Data Inputs are compatible with ECL logic. Input registers are provided on the data input lines to minimize the effect of glitching caused by data skew.

Clock and Feedthrough Control

The TDC1141 requires a differential ECL clock signal (CONVert and $\overline{\text{CONV}}$ert). Even though complementary operation is preferred, a single-ended signal may be used if either unused CONV input is biased at a DC voltage midway between the active input's V_{IH} and V_{IL} levels.

Data is synchronously entered on the rising edge of CONV (the falling edge of $\overline{\text{CONV}}$). The CONV input is ignored in the Feedthrough (FT = HIGH) mode.

The Feedthrough (FT) pin is normally held LOW, in which case the TDC1141 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided, and this pin may be left open for clocked operation. For certain applications, such as high-precision successive approximation A/D converters, output delay may be more important than glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronously in response to the digital input, without the need for a clock.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By loading the current source outputs with a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to –40mA output current (0 to –1V when terminated in 25Ω) as the input code varies from 00 0000 0000 to 11 1111 1111. OUT– varies in a complementary manner from –40 to 0mA (–1 to 0V when terminated with 25Ω) over the same code range. (See the *Input Coding Table*.) The output current is proportional to the reference current and the input code.

No Connect

These pins have no internal connection and should be left open for optimal performance.

Package Interconnections

Signal Type	Signal Name	Function	Value	R3 Package Pins
Power	A_{GND}	Analog Ground	0.0V	13
	D_{GND}	Digital Ground	0.0V	17
	V_{EEA}	Analog Supply Voltage	–5.2V	1
	V_{EED}	Digital Supply Voltage	–5.2V	5
Reference	REF–	Reference Voltage Input	–1.0V	2
	REF+	Reference Current Input	625µA	3
	COMP	Compensation Capacitor	0.1µF, see text	4
Data Inputs	D_1 (MSB)	Most Significant Bit	ECL	24
	D_2		ECL	23
	D_3		ECL	22
	D_4		ECL	21
	D_5		ECL	20
	D_6		ECL	19
	D_7		ECL	6
	D_8		ECL	7
	D_9		ECL	8
	D_{10} (LSB)	Least Significant Bit	ECL	9
Feedthrough	FT	Feedthrough Mode control	ECL	28
Convert	CONV	Convert (Clock) Input	ECL	27
	$\overline{CONV}$	Convert Complement	ECL	26
Analog Output	OUT+	Analog Output	0 to 40mA	14
	OUT–	Analog Output	40 to 0mA	15
No Connect	NC	No Internal Connection	Open	10,11,12,16,18,25

Input Coding Table[1]

Input Data MSB LSB	OUT+ (mA)	V_{OUT+}(mV)	OUT– (mA)	V_{OUT-}(mV)
00 0000 0000	0.000	0.00	40.000	–1000.00
00 0000 0001	0.039	–0.97	39.961	–998.05
00 0000 0010	0.078	–1.95	39.922	–998.05
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
0111 1111 11	19.961	–499.03	20.000	–500.00
1000 0000 00	20.000	–500.00	19.961	–499.03
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1111 1111 01	39.922	–998.05	0.078	–1.95
1111 1111 10	39.961	–999.03	0.039	–0.97
1111 1111 11	40.000	–1000.00	0.000	0.0

Note: 1. I_{REF} = 625µA, R_{LOAD} = 25Ω

Figure 1. Timing Diagram

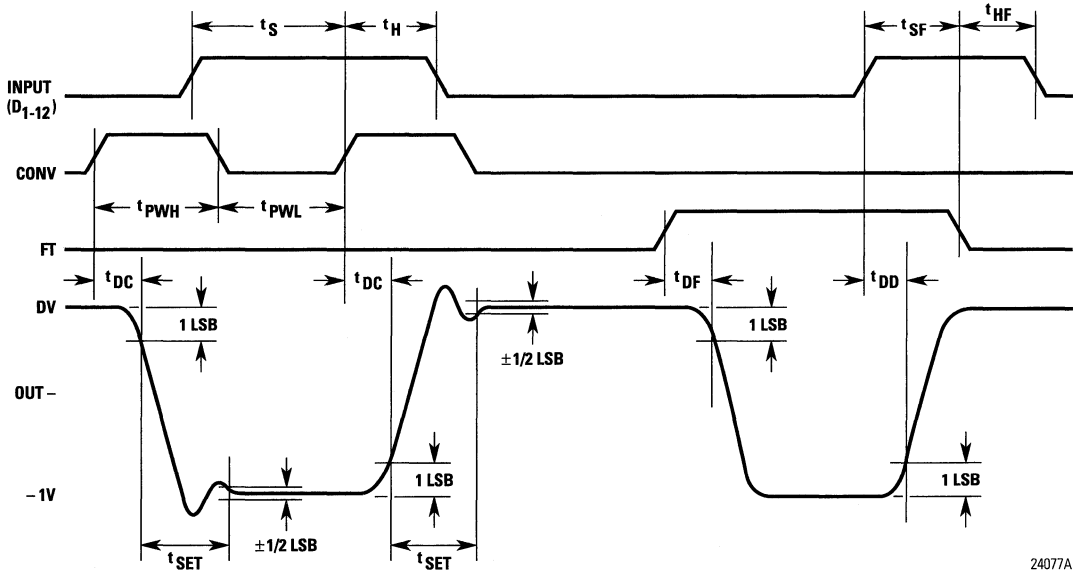


Figure 2. Equivalent Input Circuit (Data and FT)

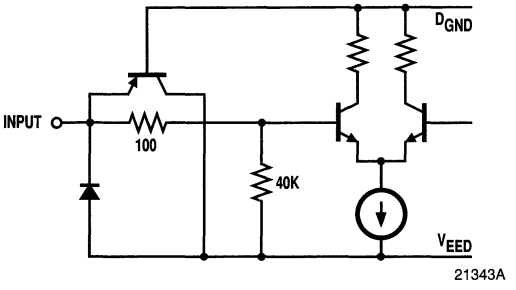


Figure 3. Equivalent Input Circuit (CONV and $\overline{\text{CONV}}$)

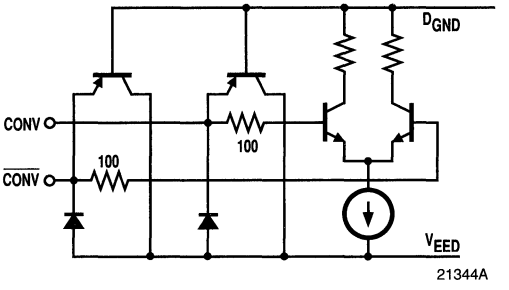


Figure 4. Equivalent Reference and Output Circuits

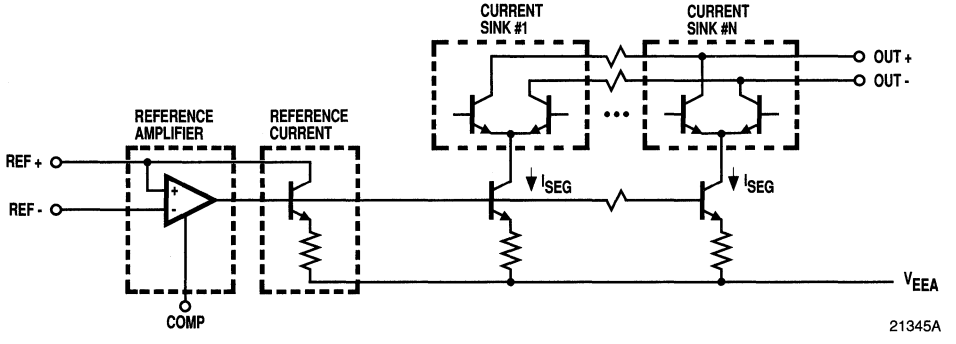


Figure 5. Standard Test Load

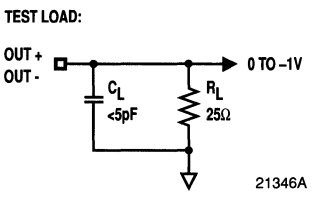
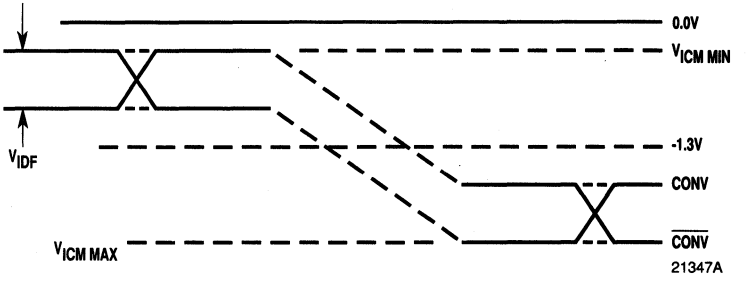


Figure 6. CONV and $\overline{CONV}$ Switching Levels



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{EEA}	(Measured to A_{GND})	–7.0 to +0.5V
V_{EEA}	(Measured to V_{EED})	–50 to +50mV
V_{EED}	(Measured to D_{GND})	–7.0 to +0.5V
A_{GND}	(Measured to D_{GND})	–0.5 to +0.5V

Inputs

CONV, $\overline{CONV}$, FT, $D_{1\text{-}12}$ (Measured to D_{GND})[2]	V_{EED} to +0.5V
REF+, REF-, Applied Voltage (Measured to A_{GND})[2]	V_{EEA} to +0.5V
REF+, REF–, Current, Externally Forced[3,4]	±3mA

Outputs

OUT+, OUT–, Applied Voltage (Measured to A_{GND})[2]	–2.0 to +2.0V
OUT+, OUT–, Current, Externally Forced[3,4]	+50mA
Short-Circuit Duration (Single Output to GND)	unlimited

Temperature

Operating, ambient (Plastic Package)	–20 to +90°C
Operating, ambient (Ceramic Package)	–60 to +150°C
Junction (Plastic Package)	+140°C
Junction (Ceramic Package)	+200°C
Lead, Soldering (10 Seconds)	+300°C
Storage	–65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
F_S	Clock Frequency	0		50	Msps
V_{EED}	Negative Supply Voltage (Measured to D_{GND})	–4.9	–5.2	–5.5	V
V_{EEA}	Negative Supply Voltage (Measured to A_{GND})	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	V
V_{EEA}	Negative Supply Voltage (Measured to V_{EED})[1]	–20	0	20	mV
t_{PWL}	CONV Pulse Width LOW ($F_S \geq 40$ Msps)	10.5			ns
	CONV Pulse Width LOW ($F_S < 40$ Msps)	11			ns
t_{PWH}	CONV Pulse Width HIGH ($F_S \geq 40$ Msps)	8			ns
	CONV Pulse Width HIGH ($F_S < 40$ Msps)	9			ns
t_S	Setup Time, Data to CONV	17			ns
t_H	Hold Time	0			ns
t_{SF}	Setup Time, Data to FT	7			ns
t_{HF}	Hold Time, Data to FT	24			ns
V_{IL}	Input Voltage, Logic LOW			–1.55	V
V_{IH}	Input Voltage, Logic HIGH	–1.05			V
V_{REF}	Reference Voltage (REF–)	–0.7	–1.0	–1.3	V
I_{REF}	Reference Current (REF+)	400	625	700	µA
C_C	Compensation Capacitor	0.01	0.1		µF
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. A common power supply isolated with ferrite bead inductors is recommended for V_{EEA} and V_{EED}. This is shown in the *Typical Interface Circuits*.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{IEED}$		$V_{EEA}=V_{EED}$=Max,static T_A=0 to 70°C		–180	mA
		T_A=70°C		–150	mA
C_{REF}	Reference Input Capacitance			15	pF
C_I	Digital Input Capacitance			15	pF
V_{OC}	Compliance Voltage		–1.2	1.2	V
R_O	Output Resistance		12		kΩ
C_O	Output Capacitance			45	pF
I_O	Full-Scale Output Current	I_{REF}=625µA	40		mA
I_{IL}	Input Current, Logic LOW	V_{EE}=Max, V_I=0.4V	–10	200	µA
I_{IH}	Input Current, Logic HIGH	V_{EE}=Max, V_I=2.4V	–10	200	µµA

Switching characteristics

Parameter		Test Conditions	Temperature Range (Standard) Min	Typ	Max	Units
t_{DC}	Clock to Output Delay	V_{EEA}, V_{EED}=Min, FT=LOW			20	ns
t_{DD}	Data to Output Delay	V_{EEA}, V_{EED}=Min, FT=HIGH			25	ns
t_{DF}	FT to Output Delay	V_{EEA}, V_{EED}=Min			30	ns
t_R	Risetime[1]	90% to 10% of FSR, FT=LOW		2	4	ns
t_F	Falltime[1]	10% to 90% of FSR, FT=LOW		2	4	ns
t_{SET}	Settling Time, Voltage	FT=LOW, Full-Scale Voltage transition on I_{OUT} to 0.1% FSR		12	20	ns

Note: 1. Clocked Mode

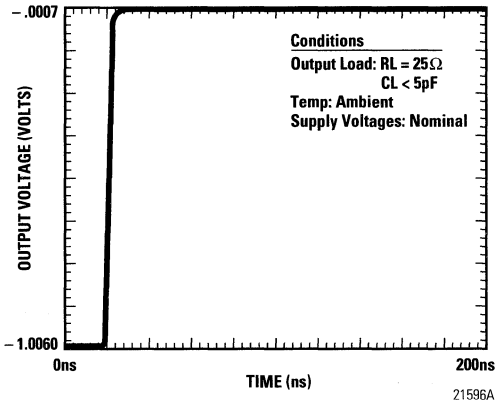
System performance characteristics

Parameter		Test Conditions	Temperature Range (Standard) Min	Typ	Max	Units
E_{LD}	Differential Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1141			±0.1	%
		TDC1141-1			±0.05	%
E_{LI}	Integral Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1141			±0.1	%
		TDC1141-1			±0.05	%
V_{OS}	REF+ to REF– Offset Voltage		–10		+10	mV
I_B	REF- Input Bias Current			5	µA	
E_G	Absolute Gain Error	V_{EEA}, V_{EED}, I_{REF} = Nom	–5		5	%
I_{OF}	Output Offset Current	V_{EEA}, V_{EED}= Max, $D_{1\text{-}12}$ = LOW			±40	µA
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = Nom[2]			–50	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED} = ±4%, I_{REF} = Nom			–140	µA/V
G_A	Peak Glitch Area				40	pV– sec

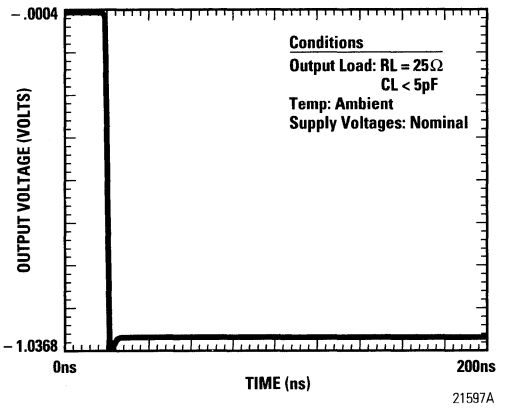
Notes: 1. OUT-connected to A_{GND}, OUT+driving virtual ground.
2 120 Hz, 600 mVp-p ripple on V_{EE} and V_{CC}.

Typical Performance Curves (Typical Settling Time Charactersitics)

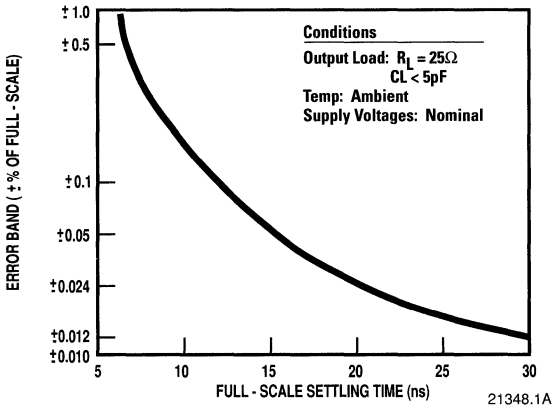
A. Full-Scale Output Transition, Rising Edge



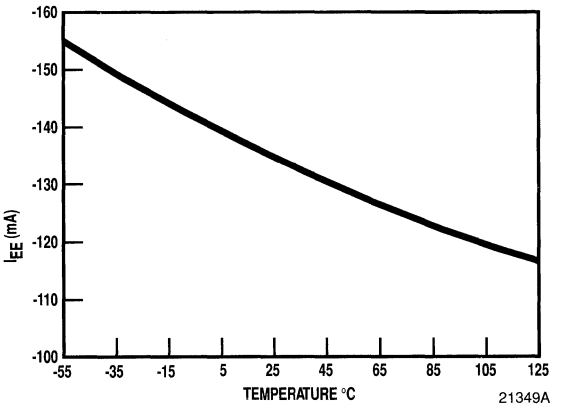
B. Full-Scale Output Transition, Falling Edge



C. Typical Settling Time vs. Settling Accuracy



D. Typical Supply Current vs. Temperature



Applications Information

There are three major D/A architectures: segmented, weighted current sources, and R-2R. In segmentated D/A converters there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N current sources. A weighted current source D/A has one current source for each bit of input with a binary weighting for the current sources. In an R-2R D/A, there is one current source per bit, and a resistor network which scales the current sources to have a binary weighting.

When transitioning from a code of 0111111111 to 1000000000, both the R-2R D/A and Binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where all current sources are either on or off, resulting in a glitch. In a segmented architecture, 511 of the current sources remain on, and one more is turned on to increment the output with no possibility of a glitch.

The TDC1141 uses a hybrid architecture with the 6 MSBs segmented, and the 4 LSBs from a R-2R network. The result is a converter which has very low glitch energy, and a moderate die size.

Layout, Power and Grounding

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided on the TDC1141. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1141 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected (typically through a ferrite bead inductor) to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1 Volt.

Output Termination

The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a 50Ω transmission line. With this load, the output voltage range of the converter is 0 to –1.0V. If a load is capacitively coupled to the TDC1141, it is recommended that a 25Ω load at DC, as seen by the TDC1141, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the ***Electrical Characteristics Table***, or the accuracy may be impaired.

See ***Figure 8*** for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output either with a balun, or an operational amplifier in the differential mode. If it is desired that the TDC1141 be operated in a single ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 9***. The CONV signal provided to the TDC1141 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory, although not as jitter free as a crystal oscillator.

Driving a 75Ω Transmission line

The TDC1141 has been optimized to operate with a reference current of 625μA. Significantly increasing or decreasing this current may degrade the performance of the device. If it is desired that the device drive a 37.5Ω load (75Ω source termination driving 75Ω transmission line) rather than the 25Ω suggested load, then V_{REF} should be held at 1V and I_{REF} reduced to 417μA. This will result in a 1V p-p voltage being generated at the DAC output.

Figure 7. Typical Interface Circuit with Balun Output

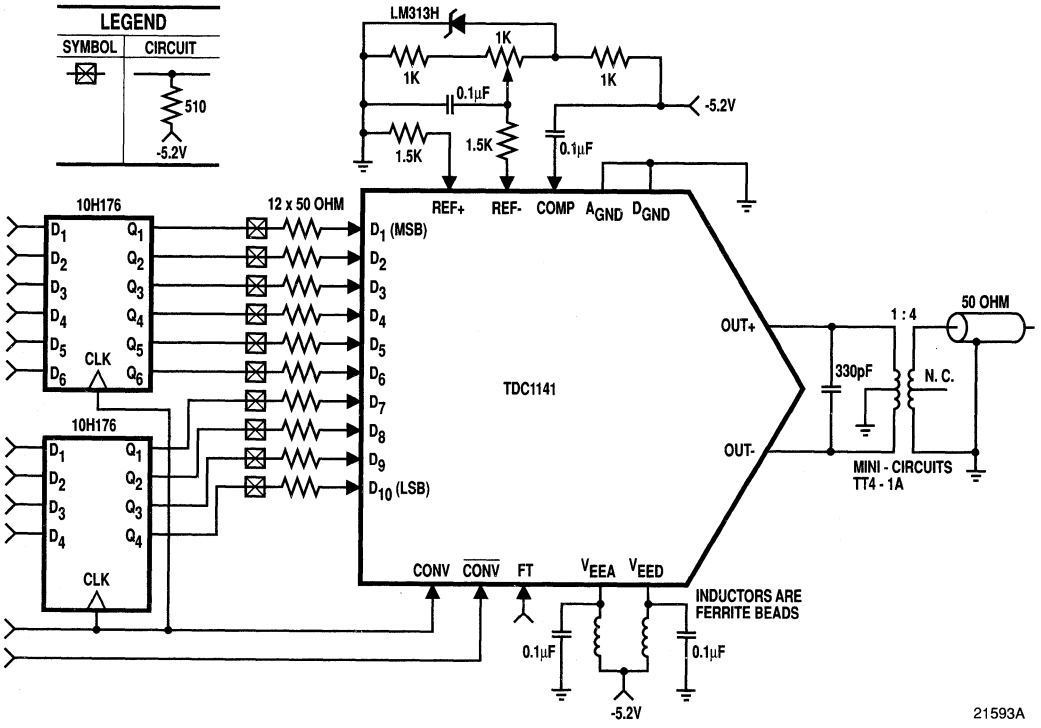


Figure 8. Typical Interface Circuit with Bipolar, Differential Mode Operational Amplifier Output

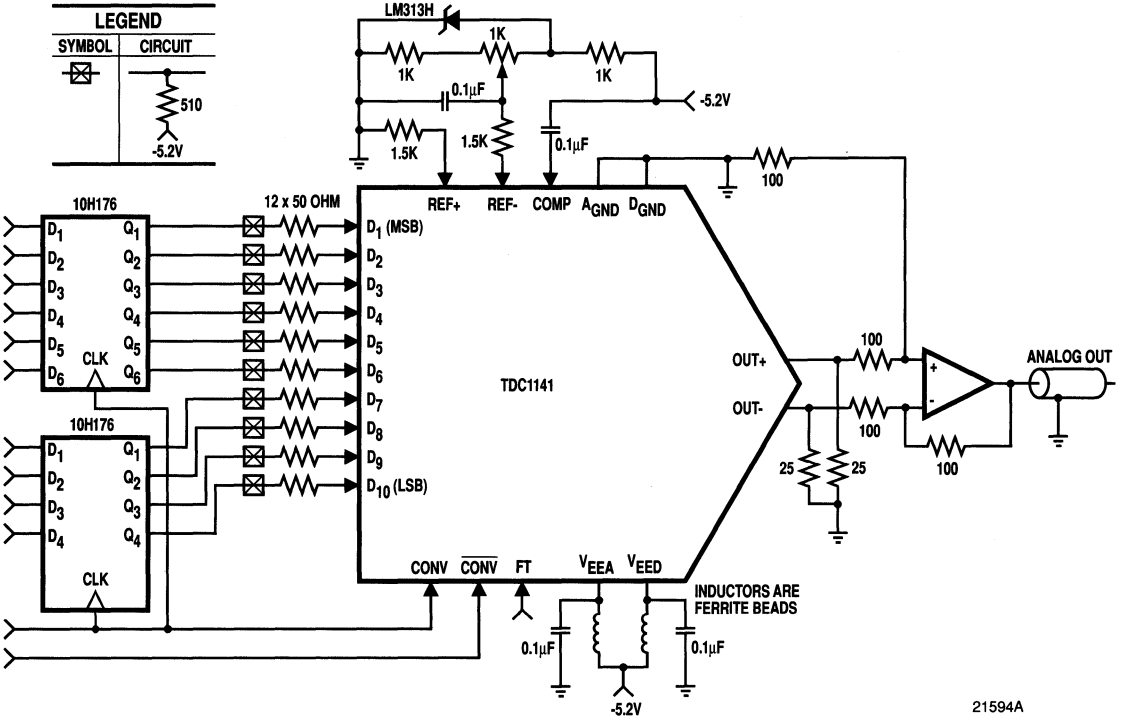
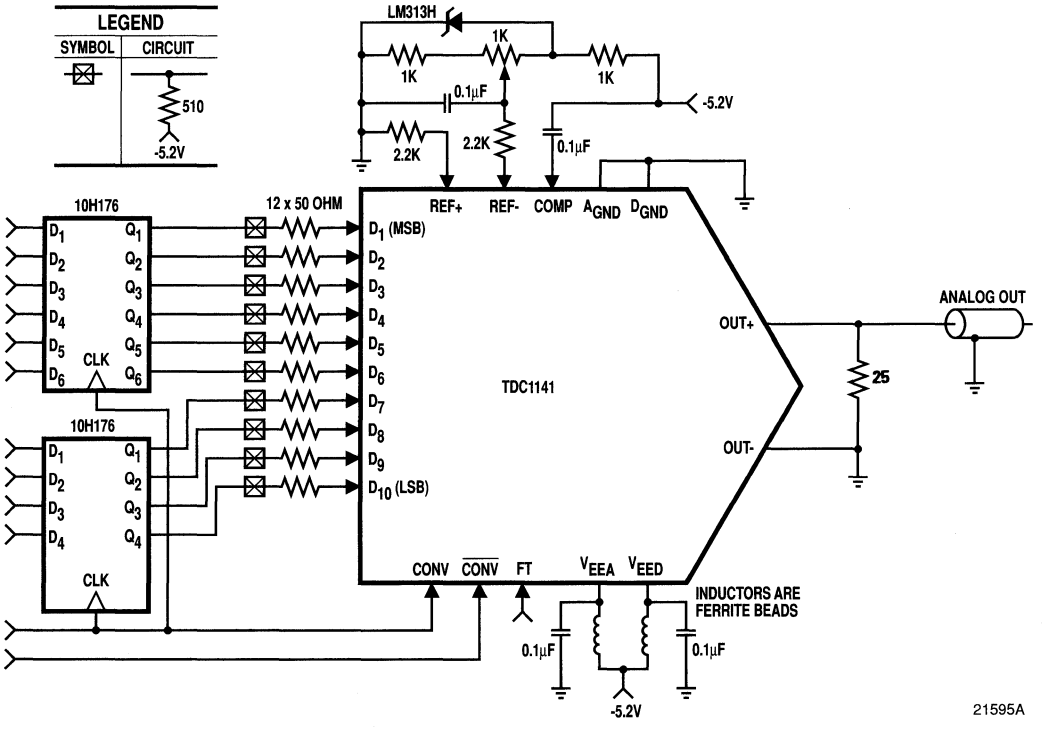


Figure 9. Typical Interface Circuit with Resistive Load Output



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1141R3C	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1141R3C
TDC1141R3C1	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1141R3C-1

40G06718 Rev B 8/93

TDC3310
Video D/A Converter 10-Bit, 40 Msps

Description

The TDC3310 is a very high-speed 10-bit D/A converter especially suited for low-cost video applications. The TDC3310 offers 10-bit resolution, TTL-compatible inputs, and requires only a single +5 volt power supply. It has a single-ended voltage output, SYNC and BLANKing control inputs and an INVERT input that reverses video levels without altering either SYNC or BLANKing.

Operating at data rates up to 40 Msps, the TDC3310 is ideal for reconstructing composite NTSC, PAL and RS-343A video waveforms. Data is decoded and registered ahead of the current switch array, resulting in outstanding low-glitch characteristics.

The TDC3310 is available in a 32-lead plastic J-Leaded PLCC and 28-pin plastic packages and is guaranteed from 0°C to 70°C.

Features

- 10-Bit resolution
- Single +5 volt power supply operation
- DC to 40 Msps, guaranteed
- ±1.0 LSB linearity error
- TTL-compatible inputs
- 1 Vp-p video output
- Sync and Blank controls
- Video invert control
- Very low glitch energy
- Very low cost

Applications

- Reconstruction of composite video
- High-resolution video
- Low-cost video systems
- Set-top RF converter boxes
- Satellite receivers
- Direct digital synthesis
- Multimedia

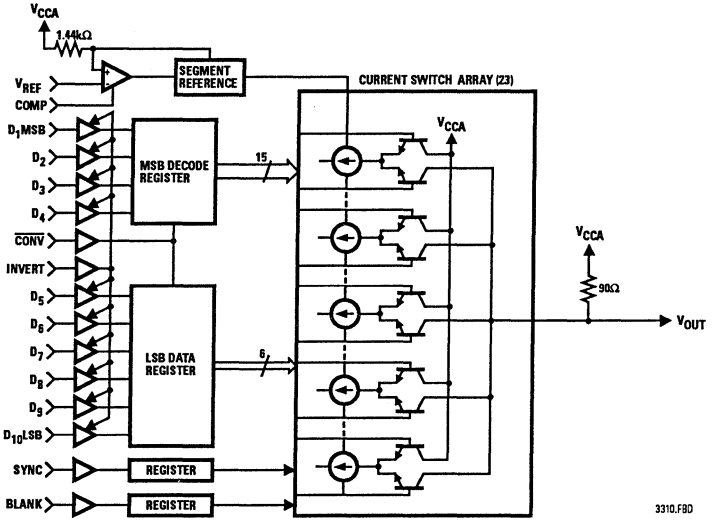
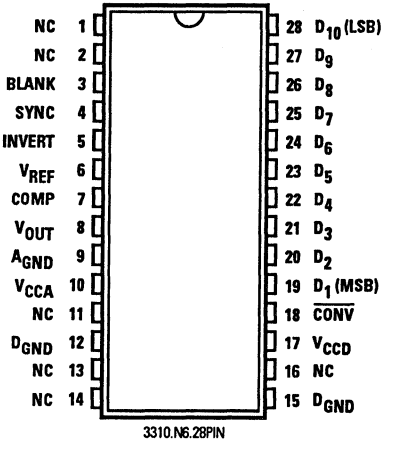
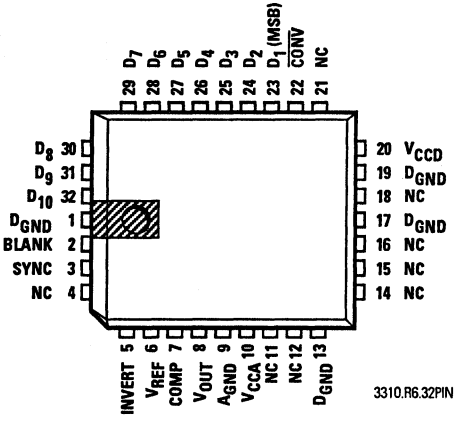


Figure 1. Block Diagram

Connection Information



28-Pin Plastic DIP — N6 Package



32-Lead Plastic J-Leaded Chip Carrier — R6 Package

Ordering Information

Product Number	Linearity Error (LSB)	Temperature Range	Screening	Package	Package Marking
TDC331N6C	±1.0	T_A = 0°C to 70°C	Commercial	28-pin Plastic DIP	3310N6C
TDC3310R6C	±1.0	T_A = 0°C to 70°C	Commercial	32-Lead J-Lead PLCC	3310R6C
TMC1175E1C	30	T_A = 0°C to 70°C	Commercial	Eurocard PC Board	TMC1175E1C

Functional Description

The TDC3310 consists of five major circuit sections: the data and control registers, the MSB decode block, the MSB current switch array, the binary weighted LSB array and the reference amplifier. All inputs are registered just before the current switch array to minimize the temporal skew that generates glitches.

The TDC3310 uses an architectures that combines segmentation and binary weighted techniques. With the four MSBs segmented into 15 equal-value current switches, and the six LSBs using binary weighting, an optimal trade-off between glitch performance and die size (cost to the user) is made. The result is a very low cost, high performance D/A converter.

Power and Ground

The TDC3310 requires a single +5.0 volt power supply. The analog (V_{CCA}) and digital (V_{CCD}) power supply voltages should be separately decoupled, as shown in the Typical Interface Circuits, to reduce power supply induced noise. 0.1 µF decoupling capacitors should be placed as close as possible to the TDC3310 power pins. Ferrite beads are neither critical in value nor always required.

The high slew rate of digital data make capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high frequency harmonics of the CONV

signal, as well as the video output signal, the result of data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance Separate analog and digital grounds are provided on the TDC3310, but all ground pins should be connected to a common solid ground plane for best performance.

V_{REF}

The TDC3310 is designed to operate with a voltage reference referred to V_{CCA} (a 1V difference between V_{REF} and V_{CCA}). The TDC3310 uses this voltage differential to generate an internal reference current for the current switch array. Since the DC voltage provided to V_{REF} must be referred to V_{CCA} (and not A_{GND}), the output voltage of the D/A converter is referred to V_{CCA} (and not to A_{GND}). This allows the gain of the TDC3310 to be immune from variations of V_{CCA}. V_{REF} should be decoupled to V_{CCA}.

The internal reference amplifier has a high-impedance input and is externally frequency-compensated to ensure stability. A 0.1 µF capacitor should be connected between the COMP pin and A_{GND}. The Typical Interface Circuits include an adjustable reference circuit.

Data Inputs $D_{1\text{-}10}$

The data inputs are TTL-compatible. For applications involving fewer than 10 bits, connect the unused LSBs to D_{GND}.

CONV\

The TDC3310 requires a TTL-compatible clock signal, CONV\. All inputs are registered on and the analog output changes t_{CO} after the falling edge of CONV\.

SYNC and BLANK

SYNC and BLANK inputs control the output level of the TDC3310 during CRT retrace intervals. When BLANK is HIGH, data to D1-10 is ignored and VOUT is forced to a fixed blanking level, nominally 81 mV below the video "black" level. When SYNC is HIGH, data to $D_{1\text{-}10}$ and BLANK are ignored and VOUT is forced to a fixed sync level, nominally 433 mV below the level corresponding to BLANK. SYNC and BLANK are registered within the TDC3310 on the falling edge of CONV\.

INVERT

INVERT controls the polarity of $D_{1\text{-}10}$ without affecting the SYNC or BLANK inputs. This input functions as a system data format selector, allowing the reversal of black and white in a video image. See the Input Coding Table. INVERT is registered within the TDC3310 on the falling edge of CONV\.

V_{OUT}

The voltage output of the TDC3310 is referred to V_{CCA} and varies from V_{CCA} to V_{CCA} - V_{REF}. The V_{OUT} terminal of the TDC3310 has an internal 90Ω resistor to provide a voltage output from the current switch array. The close thermal coupling and matched temperature coefficients of the internal reference current generator and this V_{OUT} load resistor provide an output that is stable over temperature. Operation with an external load resistor will reduce output voltage range as well as temperature stability. Current may be driven into or out of the V_{OUT} terminal as long as the output compliance voltage limit of the TDC3310 is not violated.

Not Connected

There are several pins with no internal connection to the TDC3310. They should be left open.

Table 1. Package Interconnections

Signal Type	*Name*	*Function*	*Value*	*N6 Pin*	*R6 Pin*
Power	V_{CCA}	Analog supply voltage	5.0V	10	10
	V_{CCD}	Digital supply voltage	5.0V	17	20
Ground	A_{GND}	Analog ground	0.0V	9	9
	D_{GND}	Digital ground	0.0V	12, 15	1, 13, 17, 19
Reference	V_{REF}	Reference voltage input	V_{CCA}-1	6	6
	COMP	Compensation capacitor	0.1 µF	7	7
Data Input	D_1 (MSB)	Most Significant Bit Input	TTL	19	23
	D_2		TTL	20	24
	D_3		TTL	21	25
	D_4		TTL	22	26
	D_5		TTL	23	27
	D_6		TTL	24	28
	D_7		TTL	25	29
	D_8		TTL	26	30
	D_9		TTL	27	31
	D_{10} (LSB)	Least Significant Bit Input	TTL	28	32
	INVERT	Invert D1-D10	TTL	5	5
	SYNC	SYNC input	TTL	4	3
	BLANK	BLANK input	TTL	3	2
Clock	CONV\	Clock input	TTL	18	22
Output	V_{OUT}	Analog output	+4 to +5	8	8
Not Used	NC	Not connected	Open	1, 2, 11	4, 11, 12, 14
				13, 14, 16	15, 16, 18, 21

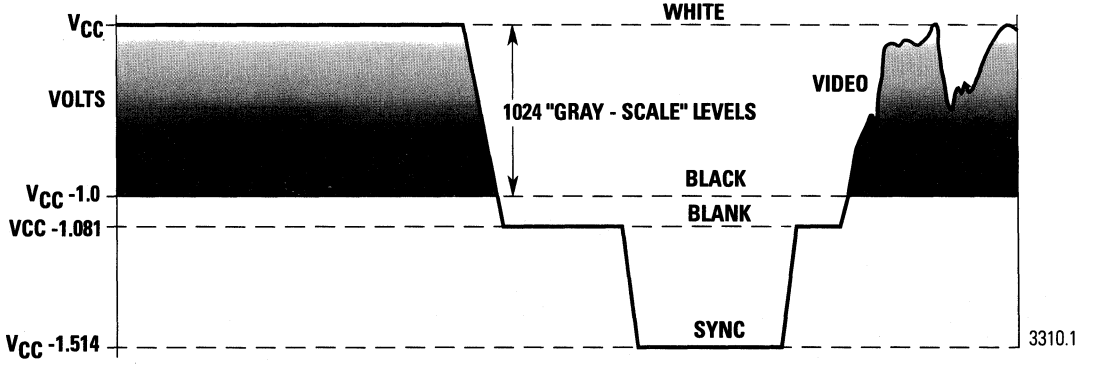


Figure 3. Video Output Waveforms

Table 2. Input Coding Table

D1.....D10 (MSB LSB)	BLANK	SYNC	INVERT = LOW V_{OUT} w/r V_{CCA}	V_{OUT} w/r A_{GND}	INVERT = HIGH V_{OUT} w/r V_{CCA}	V_{OUT} w/r A_{GND}
11 1111 1111	0	0	0.000	5.000	-1.000	4.000
11 1111 1110	0	0	-0.001	4.999	-0.999	4.001
11 1111 1101	0	0	-0.002	4.998	-0.998	4.002
.	.	.	.	.	.	.
.	.	.	.	.	.	.
10 0000 0000	0	0	-0.500	4.500	-0.501	4.499
01 1111 1111	0	0	-0.501	4.499	-0.500	4.500
.	.	.	.	.	.	.
.	.	.	.	.	.	.
00 0000 0010	0	0	-0.998	4.002	-0.002	4.998
00 0000 0001	0	0	-0.999	4.001	-0.001	4.999
00 0000 0000	0	0	-1.000	4.000	0.000	5.000
xx xxxx xxxx	1	0	-1.081	3.919	-1.081	3.919
xx xxxx xxxx	x	1	-1.514	3.486	-1.514	3.486

Note: $V_{REF} = V_{CCA}$ - 1.000 volts, V_{CCA} = 5.0 volts, no external

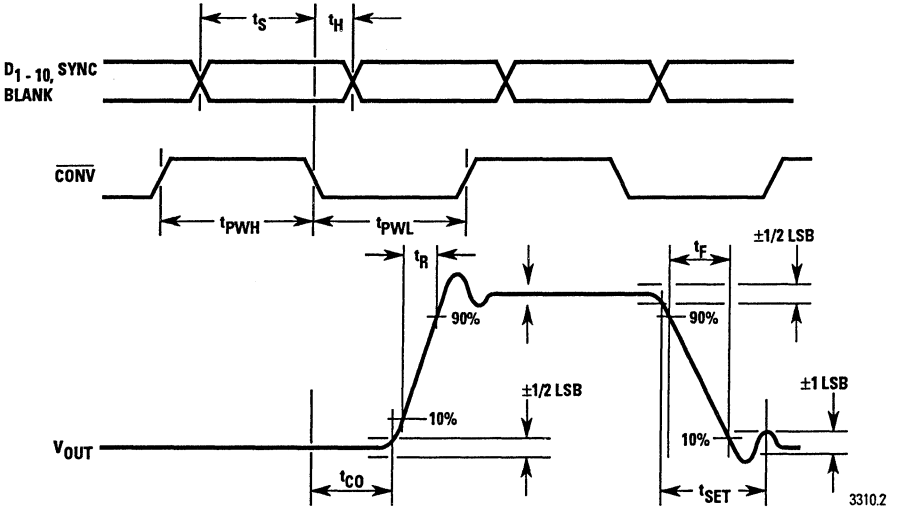


Figure 4. Timing Diagram

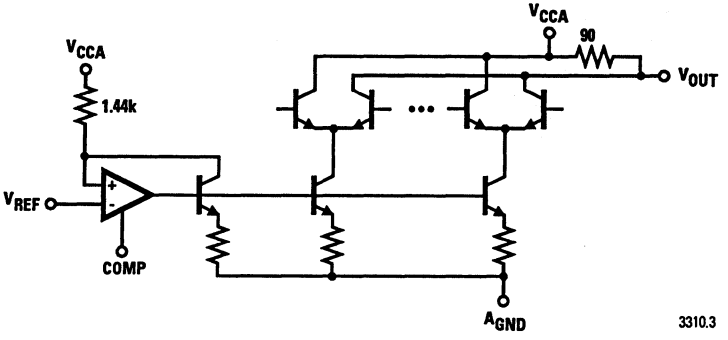


Figure 5. Equivalent Reference and Output Circuit

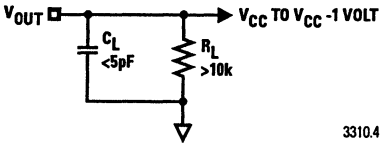


Figure 6. Output Test Load

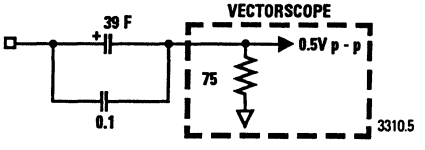


Figure 7. Output Load for DP and DG

Absolute Maximum Ratings [1]

Supply Voltages

V_{CCA} (measured to A_{GND})	-0.5 to +7.0V
V_{CCD} (measured to D_{GND})	-0.5 to +7.0V
V_{CCA} (measured to V_{CCD})	-0.5 to +0.5V
A_{GND} (measured to D_{GND})	-0.5 to +0.5V

Inputs

CONV\, $D_{1\text{-}10}$, SYNC, BLANK, INVERT

Applied voltage measured to D_{GND} [2]	-0.5 to +7.0V
Externally forced current [3]	±10 mA

V_{REF}

Applied voltage (measured to A_{GND}) [2]	-0.5 to (V_{CCA} +2)V
Externally forced current [3]	±10 mA

Output

V_{OUT}

Applied voltage (measured to A_{GND}) [2]	+3.0 to +7.0V
Externally forced current [3]	±20 mA

Temperature

R6 Package	
Operating, ambient	-25 to +90°C
Junction	+140°C
B6 Package	
Operating, ambient	-60 to +150°C
Junction	+200°C
Lead, soldering (10 sec.)	+300°C
Storage	-65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied to individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.

Operating Conditions

Parameter	Description	Standard Temperature Range			Units
		Min	Nom	Max	
V_{CCA}	Analog Power Supply Voltage	4.75	5.00	5.25	V
V_{DDC}	Digital Power Supply Voltage	4.75	5.00	5.25	V
V_{CCA}-V_{CCD}	Power Supply Voltage Differential	-0.1	0.0	0.1	V
A_{GND}-D_{GND}	Ground Voltage Differential	-0.1	0.0	0.1	V
V_{REF}	Reference Voltage	V_{CCA} - 1.5	V_{CCA} - 1.0	V_{CCA} - 0.5	V
C_C	Compensation Capacitor	0.01	0.1		µF
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
t_S	Input Data Setup Time	20			ns
t_H	Input Data Hold Time	2			ns
t_{PWL}	CONV\ Pulse Width, LOW	10			ns
t_{PWH}	CONV\ Pulse Width, HIGH	10			ns
T_A	Temperature Range, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Standard Temperature Range			Units
			Min	Typ	Max	
I_{CC}	Supply current	V_{CCD} = V_{CCA} = Max		70	115	mA
C_{IN}	Input Capacitance	CONV\, D_{1-10}, SYNC, BLANK, INVERT, V_{REF}		5	10	pF
I_{IL}	Input Current, Logic LOW	V_{CCD} = Max, V_I = 0.4V		-200	-400	µA
I_{IH}	Input Current, Logic HIGH	V_{DDC} = Max, V_I= 2.4V		10	100	µA
R_O	Output Resistance	V_{OUT} to V_{CCA}, T_A = +25°C	80	90	100	Ω
C_O	Output Capacitance	V_{OUT} Terminal			20	pF
V_{OC}	Output Compliance	Referred to V_{CCA}	-1.5	0	+0.4	V
V_{FS}	Full-Scale Output	Referred to V_{CCA}, V_{REF} = Nom	-0.95	-1.0	-1.05	V
V_{BLANK}	Blank Output Voltage	Referred to V_{FS}, V_{REF} = Nom	-71	-81	-91	mV
V_{SYNC}	Sync Output Voltage	Referred to V_{BLANK}, V_{REF} = Nom	-380	-433	-480	mV

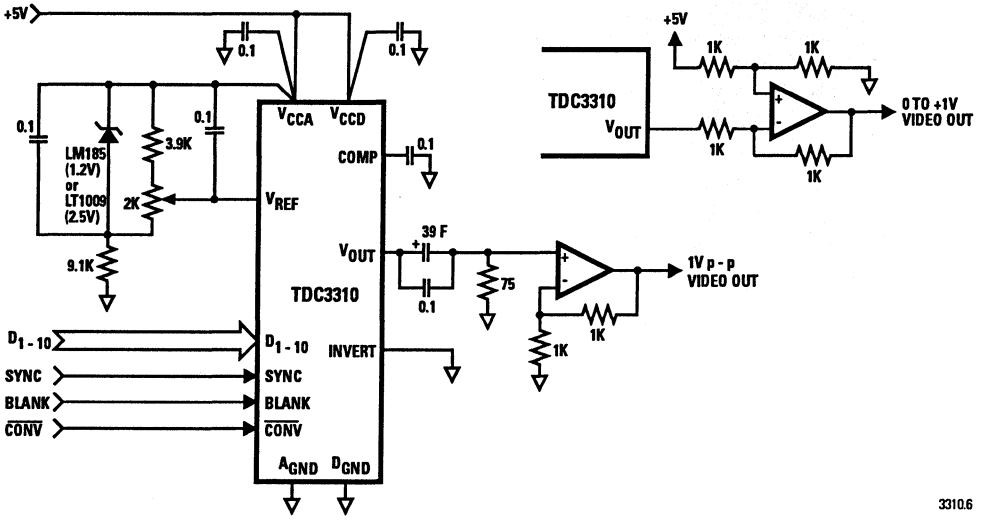
Switching Characteristics

Parameter		Conditions	Standard Temperature Range Min	Typ	Max	Units
f_S	Maximum Clock Rate	V_{CCA}, V_{CCD} = Min	40			MHz
t_{CO}	Clock to Output Delay[1, 2]	V_{CCA}, V_{DDC} = Min		8	15	ns
t_R	Output Risetime [1, 2]	90% to 10% of Full Scale		5	10	ns
t_F	Output Falltime[1,2]	10 to 90% of Full Scale		5	10	ns
t_{SET}	Output Settling Time [1, 2, 3]	to 1%		10	18	ns
		to ±1LSB		25	40	ns
G_A	Peak Glitch Area[2, 3]			50		pV-sec

Notes:
1. See Timing Diagram.
2. Standard Test Load, Figure 4.
3. Worst-case transition.

System Performance Characteristics

Parameter		Conditions	Standard Temperature Range Min	Typ	Max	Units
E_{LD}	Differential Linearity Error	V_{CCA}, V_{CCD}, V_{REF} = Nom		±0.5	±1.0	LSB
E_{LI}	Integral Linearity Error	V_{CCA}, V_{CCD}, V_{REF} = Nom		±0.5	±1.0	LSB
E_G	Absolute Gain Error	V_{CCD}, V_{CCA}, V_{REF} = Nom		±1	±5	%
TC_{EG}	Gain Error Tempco	V_{CCD}, V_{CCA}, V_{REF} = Nom		±30		ppm/°C
V_{OF}	Output Offset Voltage	V_{CCA}, V_{CCD} = Max, $D_{1\text{-}10}$ = HIGH		-10	-25	mV
TC_{OF}	Offset Tempco	V_{CCA}, V_{CCD}, = Max, $D_{1\text{-}10}$ = HIGH		-50		µV/°C
I_{REF}	V_{REF} Input Bias Current			1	5	µA
D_P	Differential Phase	f_S = 4 x NTSC Subcarrier		0.2		Degrees
D_G	Differential Gain	f_S = 4 x NTSC Subcarrier		0.3		%



Application Notes

Since the internal reference and output circuits of the TDC3310 are referred to the power supply, V_{CC}, the external voltage reference shown in the Typical Interface Circuit is also referred to V_{CC}. A simple 1.2 volt Bandgap reference diode is voltage-divided to provide 1.0 volts between the V_{REF} and V_{CC} inputs. The output of the TDC3310 is AC coupled into a 75Ω resistor which divides the output video level by a factor of two. The video amplifier gain is +2, restoring the 1 Vp-p video level and referring the video signal to A_{GND}. It is important to ensure the power supply for the TDC3310 is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit.

Grounding

The TDC3310 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages (V_{DDD} and V_{DDA}) come from the same source and ground connections (D_{GND} and A_{GND}) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

The digital circuitry that gets its input from the TMC1173 should be referred on the system digital ground plane.

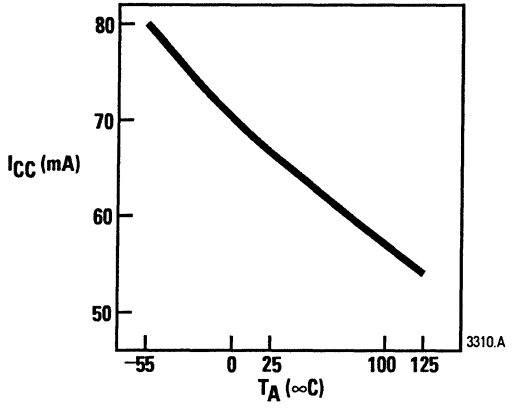
Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option — even for breadboarding. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

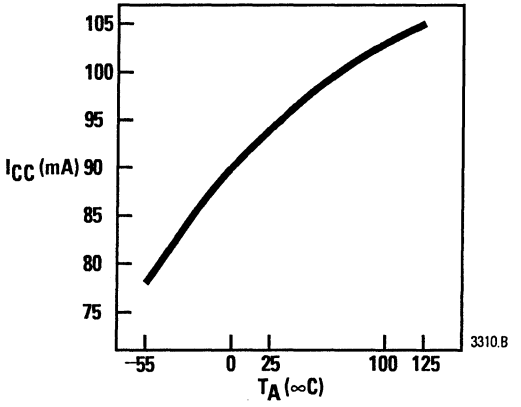
1. Keep the critical analog traces (V_{IN}, R_T, R_B, V_{R+}, V_{R-}) as short as possible and as far as possible away from all digital signals. The TMC1173 should be located near the board edge, close to the analog output connectors.
2. The power plane for the TMC1173 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1173 is the same as that of the system's digital circuitry, power to the TMC1173 should be decoupled with ferrite beads and 0.1 µF capacitors to reduce noise.
3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They typically supply adjacent circuitry on the device, which generate varying amounts of noise. For best results, use 0.1 µF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.
5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC1173, the voltage reference or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1173 and its related analog circuitry can have an adverse effect on performance.
6. CONV should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Typical Performance Curves



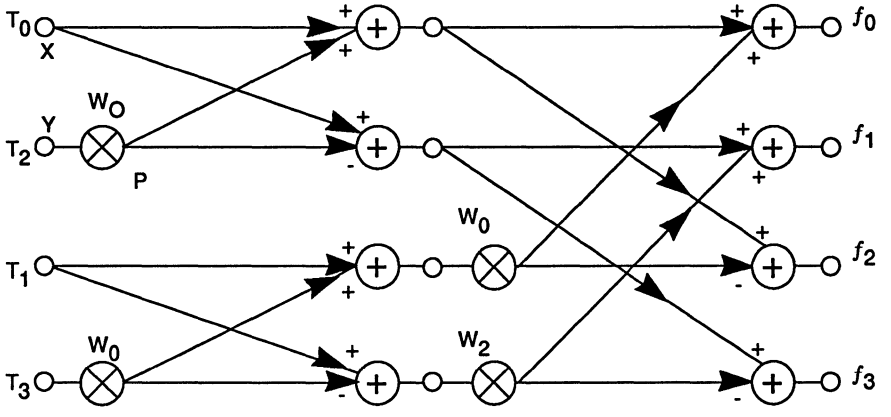
Power Supply Current vs. Temperature



R_{OUT} vs. Temperature

40G06946 Rev D 8/93

Transform Products



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Transform products perform complex conversions from one signal space to another. The high level of integration in Raytheon products yields very efficient, cost-effective implementations of the basic signal processing function.

The Fast Fourier Transform is a basic tool in time/ frequency domain processing. The TMC2310 executes a 1K point, 16 bit FFT in 514 µs (16 points in 4 µs).

The Fast Cosine Transform is the key functional element in image compression. The TMC2311 operates on 12 bit data at a 15 Mega Pixel/s rate.

The TMC2330 is tailored to convert data in polar coordinate space to rectangular space, or vice-versa, at rates of 25 million operations per second.

Product	Description	Size	Clock Rate[1] (MHz)	Power[1] (Watts)	Package	Grade	Notes
TMC2310-1	Fast Fourier Transform	16-Bit	20	0.75	G5, L4, L6	V	1024 point complex FFT in 514 µs with 19-bit
-			20	0.75	H7		internal precision and block floating-point
			15	0.75	G5, L4, L6	V	rescaling.
TMC2311-2	Fast Cosine Transform	12-Bit	17.8	0.7	R1	C	Data compression processor.
-1			14.5	0.7	R1	C	Meets CCITT specifications
-			17.8	0.7	R1	C	8x8, 2-dimension.
TMC2330-1	Coordinate Transform	16x16 Bit	25	0.7	H5, L5	V, C	Cartesian ↔ polar converter.
-			20	0.7	H5, L5	V, C	

Notes:
1. Guaranteed. See product specifications for test conditions.
2. A = High Reliability, T_C = -55°C to 125°C.
   C = Commercial, T_A = 0°C to 70°C.
   V = MIL-STD-883 compliant, T_C = -55°C to 125°C.
   SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C

TMC2310
FFT Processor
16/19-Bit, 20 MHz

Description

The TMC2310 is an advanced integrated circuit which can execute complex Fast Fourier Transforms (FFT), forward or inverse, of up to 1024 points, with or without data windowing. The device operates with either unconditional or conditional overflow block floating-point rescaling. Adaptive and static Finite Impulse Response filtering, real and complex multiplication or multiply-accumulation, and magnitude squared operations are also supported. Sinusoidal coefficients ('Roots of Unity") for Fourier Transforms are provided in a Coefficient Look-Up Table in on-chip ROM. At the maximum clock rate of 20 MHz, the device will execute radix-2 butterflies in 100 ns, and 1024-point complex transforms (5120 butterflies) in 514 µSec.

The TMC2310 provides the arithmetic, control, coefficient memory and address generation logic for a variety of signal processing and vector algorithms. External memory is used for storage of complex data and window or filter coefficients. Each data port is bidirectional and the device can be used with one or two banks or memory for either in-place or bank switched memory configurations, allowing the user to overlap I/O operations with arithmetic execution. All functions utilize the same basic system architecture, ensuring maximum flexibility.

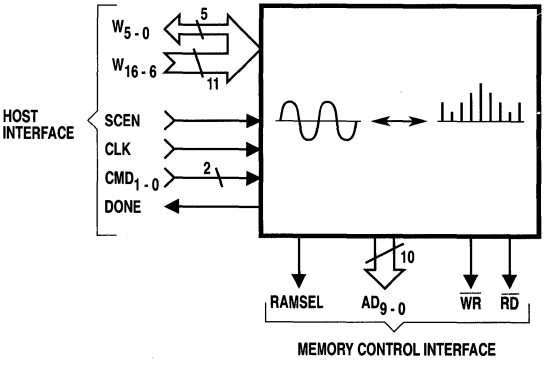
The control structure has been designed to simplify its use as a high-speed arithmetic accelerator. The device is programmed by initializing two internal configuration registers to set device parameters such as function, transform length, data addressing modes, single or bank switching memory architecture, and other options. Once initialized, the device generates data addresses and control for external memory, transfers data, executes the algorithm, and provides a DONE flag to indicate completion.

Built with Raytheon Semiconductor's OMICRON-C™ CMOS process, the TMC2310 is available in 89-pin plastic and 88-pin ceramic pin grid arrays and a 100 leaded ceramic chip carrier.

Features

- Stand alone execution of forward or inverse complex Fast Fourier Transforms, adaptive and non-adaptive FIR filtering, multiplication or multiplication-accumulation (real or complex) magnitude squared
- Fast 100 ns per butterfly yields a 2 MHz to 4 MHz sampling rate in single-device systems (16-point FFT in 4 µsec, 1024-point in 514 µsec)
- Pipelined addressing mode and internal data storage to reduce memory bandwidth
- Multiple-transform array mode to increase throughput
- On-chip ROM coefficient look-up table for FFT coefficients ("Twiddle Factors")
- 16-bit fixed-point data format with 19-bit intermediate and final results for improved precision
- Conditional overflow rescaling or manual scaling (block floating-point) for high signal-to-noise performance
- Scaler (block exponent) output
- User-programmable window functions
- Complete on-chip address generation and control for off-chip data and window/(FIR) coefficient memory

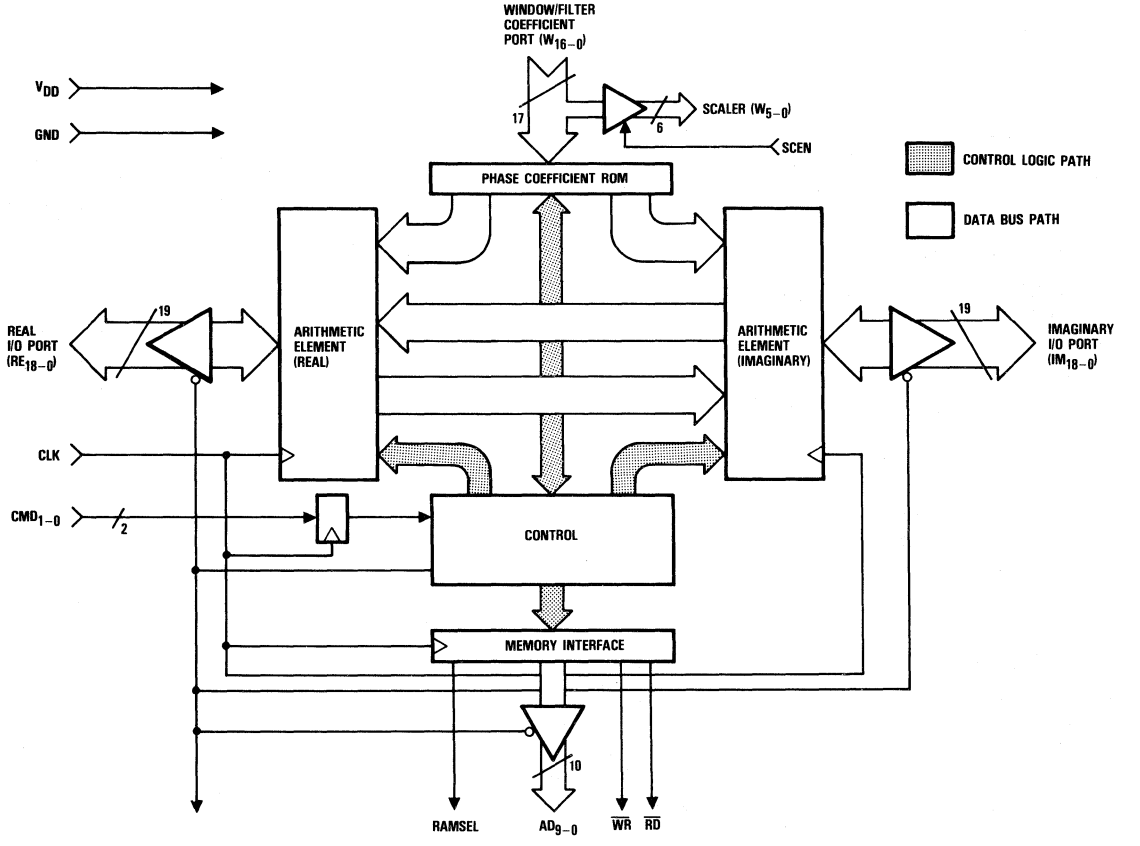
Logic Symbol



Applications

- Radar
- Sonar
- Digital Communications
- High–Speed Modems
- Image Processing, Graphics
- Test Instrumentation
- Medical Electronics
- Spectral Decomposition/Analysis
- Frequency–Multiplex Demodulation
- Adaptive Filtering And Equalization
- Pulse And Image Compression
- Frequency And Time Domain Digital Filtering
- High–Speed Complex Multiplication

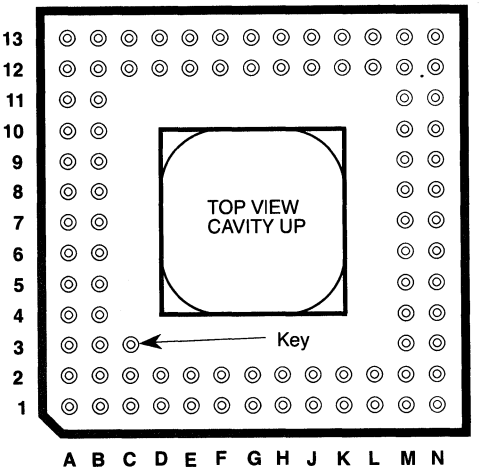
Functional Block Diagram



Pin Assignments – 88 Pin Ceramic (G5) or 89 Pin Plastic (H7) Pin Grid Array

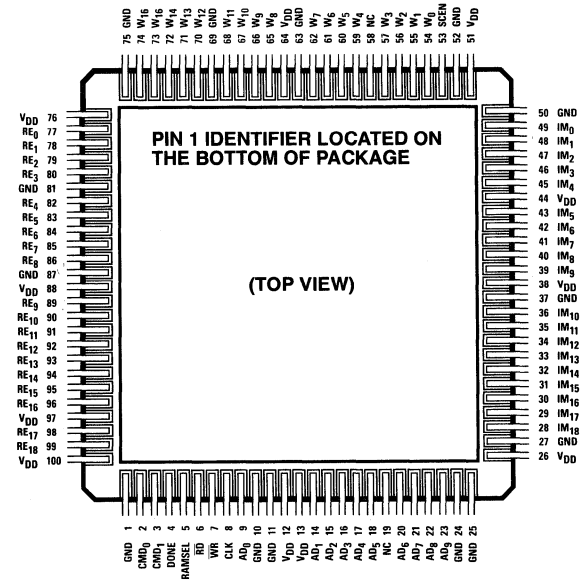
Pin	Name	Pin	Name	Pin	Name	Pin	Name
B1	GND	N2	GND	M13	GND	A12	RE_0
C2	CMD_0	M3	IM_{18}	L12	SCEN	B11	RE_1
C1	CMD_1	N3	IM_{17}	L13	W_0	A11	RE_2
D2	DONE	M4	IM_{16}	K12	W_1	B10	RE_3
D1	RAMSEL	N4	IM_{15}	K13	W_2	A10	GND
E2	RD	M5	IM_{14}	J12	W_3	B9	RE_4
E1	WR	N5	IM_{13}	J13	W_4	A9	RE_5
F2	CLK	M6	IM_{12}	H12	W_5	B8	RE_6
F1	AD_0	N6	IM_{11}	H13	W_6	A8	RE_7
G1	GND	N7	IM_{10}	G13	W_7	A7	RE_8
G2	GND	M7	GND	G12	GND	B7	GND
H1	V_{DD}	N8	V_{DD}	F13	V_{DD}	A6	V_{DD}
H2	V_{DD}	M8	IM_9	F12	W_8	B6	RE_9
J1	AD_1	N9	IM_8	E13	W_9	A5	RE_{10}
J2	AD_2	M9	IM_7	E12	W_{10}	B5	RE_{11}
K1	AD_3	N10	IM_6	D13	W_{11}	A4	RE_{12}
K2	AD_4	M10	IM_5	D12	W_{12}	B4	RE_{13}
L1	AD_5	N11	IM_4	C13	W_{13}	A3	RE_{14}
L2	AD_6	M11	IM_3	C12	W_{14}	B3	RE_{15}
M1	AD_7	N12	IM_2	B13	W_{15}	A2	RE_{16}
N1	AD_8	N13	IM_1	A13	W_{16}	A1	RE_{17}
M2	AD_9	M12	IM_0	B12	GND	B2	RE_{18}

C3 Index Pin (H7 packge only)



Pin Assignments

100 Leaded Ceramic Chip Carrier, L4 Package



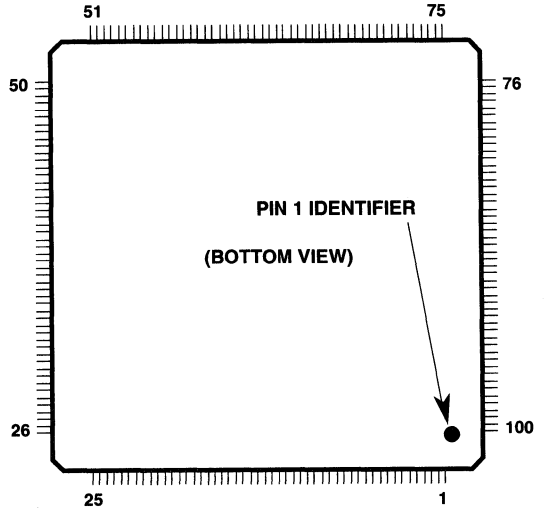


Figure 1. Basic TMC2310 System

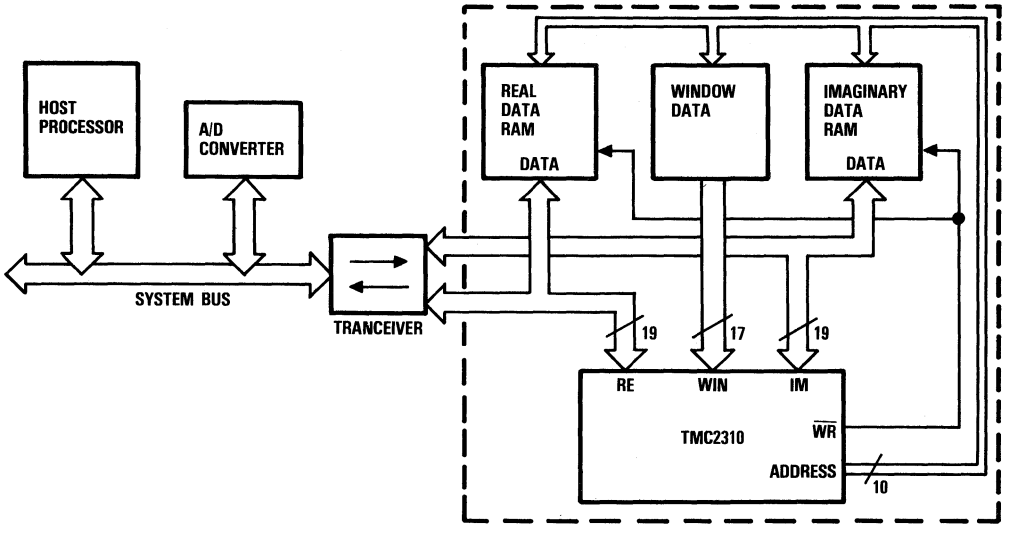
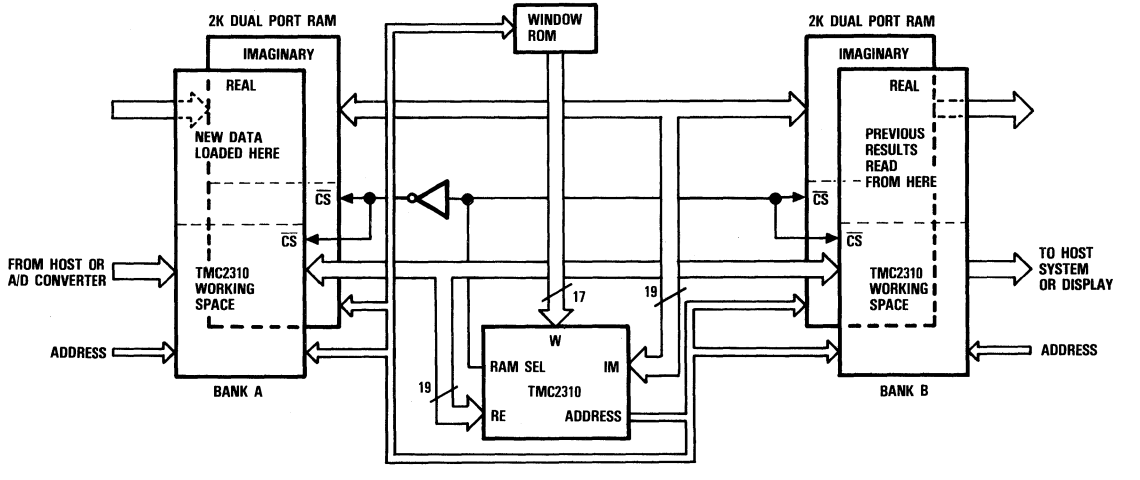


Figure 2. TMC2310 with Dual–Port Memory



Functional Description

General Information

The TMC2310 performs radix-2. Decimation In Time (DIT) Fast Fourier Transforms. It accepts 16-bit input data and maintains 19-bit (RE, IM) data either automatic pass-by-pass or unconditional data rescaling (block floating-pointing). The 19-bit (RE, IM) data buses will accommodate up to three bits of word growth per data pass. Incoming data are rescaled to 16-bit, two's complement fractions on subsequent passes based on the maximum overflow detected during the previous pass (auto scale) or under user control (manual scale). To reduce memory bandwidth requirements (number of passes), the device performs radix-2 butterflies in sets of four (radix-4 addressing). A "pass" is defined as one arithmetic operation performed on the entire data array. Therefore, a butterfly operation is considered to be one data pass. Fourier Transforms require multiple data passes with external memory used for storage of intermediate and final results. All other (non-FFT) operations are completed in one pass.

As shown in Figures 1 and 2, a system can be configured with either single or multi-port RAM, a window coefficient RAM/ROM, and very little additional hardware (see Applications Section). Multi-port memory architecture (Figure 2) allows I/O operations to be overlapped with data processing, maximizing system performance. The internal sequencing and control logic allows the device to operate with minimal support from the host system. External control consists of the programming of two internal configuration registers and a START, LOAD or RESET command. System performance is limited by either the maximum system clock rate or the memory access time. The architecture and sequencing of the TMC2310 are designed to minimize the number of wasted clock cycles between passes, ensuring that each butterfly can be executed in two clock cycles.

The TMC2310 also supports the use of window functions for Fourier transforms. To perform windowing, the user need only provide a set of coefficients in external ROM or RAM and program the device accordingly. Window functions are applied to (multiplied by) the input data during the first data pass. Typical configurations utilize a 1K x 17 (x16 for positive coefficients) block of RAM or ROM on the dedicated window memory bus. For additional information regarding window functions consult reference (1).

The TMC2310 also performs in-place, memory based Finite Impulse Response (FIR) filtering. This function utilizes the external window port memory for storage of filter coefficients. Fixed coefficient and adaptive FIR filters can be implemented with 16 to 1024 coefficients (taps). Time domain filtering is accomplished with a memory based shift register technique in which the accumulated sum of products is determined (convolution of filter coefficients with stored data samples). Adaptive filtering allows real-time updates to filter coefficients by a dynamic update value.

Real and Complex vector arithmetic functions include multiplication, multiply-accumulation, and magnitude squared ($I^2 + Q^2$). By combining functions, a variety of signal processing algorithms can be performed, including frequency domain filtering, signal analysis and signal synthesis.

A multiple-transform array mode offers multiple equal-length transform capability. Any number of equal-length transforms may be selected up to a maximum of 1024 points. For example, the user may execute 16 contiguous 64-point transforms, reducing the computation overhead associated with starting and executing single transforms. The window coefficients may be identical or unique to each transform. Scaling is performed on all points of all transforms equally, based on the maximum overflow of the previous data pass or on the user specified value.

At the end of the transform, the user may read the 19-bit data output and the 6-bit scaling factor ("block exponent") generated by the internal shift/rescale circuitry. The 4-bit "Total Scaler" value indicates the number of shifts performed on the data (block exponent) while the remaining 2 bits indicate the overflow encountered during the final data pass. Nineteen bits are used for intermediate results in order to minimize roundoff error during transforms. Provisions have been made, however, to allow the use of 16-bit wide memory systems. This can reduce memory component count but may increase roundoff error (arithmetic noise).

The TMC2310 consists of five major sections: two arithmetic elements, external memory interface, control logic and coefficient ROM.

Arithmetic Elements (AEs)

Each AE consists of an 18 x 18 bit multiplier, adders/ accumulators and data storage. The AEs interface to external data and window memory as well as internal coefficient ROM. Communication between AEs allows the device to perform complex arithmetic operations. To minimize arithmetic error, each AE retains maximum precision until the output stage where data are rounded to 19 bits (Real and Imaginary). The bidirectional data buses transfer data between the AE and external memory. 19-bit input values are shifted at the input to the multiplier array. This shift is either automatic (FFT auto scale modes) or user controlled (manual scale). On the first pass, if the upper three bits contain significant data, the user must right shift the input data using manual scaling.

External Memory Interface

The TMC2310 provides all the necessary addressing and control for external memory. Read and write address are provided as well as control outputs for write strobes, read enables and a source/destination RAM select for multiple memory bank systems. The single, 10-bit address output is multiplexed for read and write operations. The sequence is determined by the selected function as well as other user specified options.

The sequence may be specified as bit-reversed or sequential for FFT/IFFT operations. The selected sequence has no effect on execution time. However, it does affect the ordering of input data and whether additional memory is required (scratch pad). The device supports a special "pipelined" addressing mode for all operations. Under normal addressing, the address and controls are output during the same clock period as the data. In the pipelined mode, address and controls are output one clock cycle prior to the data, providing added flexibility in the host system interface as well as reducing memory speed requirements (see Timing and Applications).

Coefficient ROM

An internal ROM is included as a coefficient look-up table to the AEs. The ROM supplies the sinusoidal coefficients ("Roots of Unity") required for forward and inverse FFTs. The ROM is accessed under internal control and outputs data to the arithmetic elements during FFT passes (Sine and Cosine values). The ROM contains coefficients to support transforms of up to 1K (1024) data points.

Control

The control section configures the data paths and provides internal sequencing. The device operation is defined by two internal configuration registers. Once the function has been "STARTed", the device performs all sequencing and activates the DONE flag upon completion.

Signal Definitions

Power

V_{DD}, GND — The TMC2310 operates from a single +5V supply. All power and ground lines must be connected.

Clock

CLK — The TMC2310 operates from a single system clock. All internal and external operations are referenced to the rising edge of CLK.

Data Buses

RE_{18-0} — RE-Bus is a bidirectional data bus for "Real" data. This bus is time multiplexed for reads and writes. When the device is Idle, this bus is in the high-impedance state. RE_0 is the Least Significant Bit (LSB). RE_{15-3} is also used to load the internal configuration registers. Data placed on the bus are clocked into a configuration register during a LOAD command. Registers may also be programmed by storing configuration data in address 0 of the Real data memory. A LOAD command causes a read operation with the address bus set to address 0.

IM_{18-0} — IM-Bus is a bidirectional data bus for "Imaginary" data. This bus is time multiplexed for reads and writes. When the device is idle, this bus is in the high-impedance state. IM_0 is the LSB>

W_{16-0} — The W-Bus is used to input the 17-bit window and FIR Filter coefficients. W_{5-0} is also used as an output to access the block exponent and last pass overflow.

Data Buses (cont.)

W_{16-0} The scaler exponent (W_{3-0}) indicates the number of shifts performed on the data for multiple pass transforms while W_{5-4} indicates the overflow (in bits) that occurred during the previous pass. W_{5-4} indicates how many, if any, of the three MSBs (RE_{18-16}, IM_{18-16}) of the final results contain significant data (i.e. bits which are not an extension of the sign). If the largest magnitude result mantissa of a pass falls between -32,768 and +32,767, inclusive, W5-4 following that pass will be 0. If, instead, it falls between -65,536 and -32,769, inclusive, or between +32,768 and +65,535, inclusive, W_{5-4} will be a 1, denoting 1 bit of net word growth to be compensated at the start of the next pass by a right shift.

Control Inputs

CMD1-0 The manifold functions of the TMC2310 FFT processor are selected by the information loaded into its Configuration Registers, CR1 and CR2. The loading of these registers is controlled by the CMD_{1-0} input pins and the clock. The TMC2310 must be RESET and both Command Registers loaded before the first operation (FFT or other transformation) begins. The TMC2310 RESETs automatically after each complete transform, and then CR1 and/or CR2 may be updated for a different operation. If neither CR1 nor CR2 is updated, the previous operation will be repeated on the next data set.

Each register value may be loaded in a separate LOAD sequence, or both values may be loaded sequentially in the same LOAD sequence. CR1 and CR2 may be loaded in any order because bit 15 is an identification bit. The values for CR1 and CR2 may be presented to pins RE_{15-3} from any source. A clever source for one of these values is memory location 0, which is called by the TMC2310 during the LOAD operation.

The LOAD command is given by the first clock rising edge at least t_S after setting CMD_{1-0} =01. The Command Register value is read by the TMC2310 at its RE_{15-3} pins on the third (and fourth, for sequential loading) rising clock edge after the LOAD command. CMD_{1-0} must be held at 01 during the entire LOAD sequence. As long as CMD_{1-0} is held at 01, the TMC2310 command registers track the RE_{15-3} inputs. See the timing diagram 7 and 8 for further information.

Here are the step-by-step instructions:

For the first operation after applying power, the TMC2310 must be RESET. (This step is not required for subsequent operations.)

1. Set CMD_{1-0}=00 for at least 4 clock rising edges. (DONE, WR\and RAMSEL will go HIGH.)

Load the Configuration Registers by entering a LOAD command and presenting the values for CR1 and/or CR2 to the TMC2310.

2. Set CMD_{1-0}=01 at least t_S before a clock rising edge, which we'll label "0."
3. Present the data for CR1 or CR2 to the RE_{15-3} pins at least t_S before clock rising edge 3.
4. To load the selected operation, set CMD_{1-0} =11 to enter the CONTINUE mode, during which the TMC2310 waits for a start command. The START command is given by setting CMD_{1-0} =10 at least t_S before a clock rising edge. For proper operation CMD_{1-0} must be set to 11 (CONTINUE) within 4 clock cycles after to START command. The selected operation is performed to completion.

The registered CoMmanD input is used to RESET the device, LOAD configuration registers, and START an operation. Commands are issued by placing a valid command on the input for one (or more) clock cycle(s) then returning to the CONT command. The input should normally remain in the inactive (CONT) state. The operation of each command is as follows:

CMD_{1-0}	Command	Operation
00	RESET	If RESET is held for at least 4 clock cycles, the DONE flag, WR, RAMSEL are set HIGH. The address bus (AD_{9-0}), data buses RE_{18-0}, IM_{18-0} and W_{16-0} are set to high-impedance state, and the RD output is LOW. A RESET command held for only one cycle does not reset the chip, but causes the last pass scaler (W_{5-4}) to be added to the current scaler exponent (W_{3-0}). The sum then appears on W_{5-0} until cleared. RESET held for more than one cycle will clear the scaler exponent field (W_{5-0}).
01	LOAD	AD_{9-0} is activated and a read is performed with the address set to zero. If LOAD is followed by a CONT then the device will be put into a RESET state.
10	START	START causes the device to begin an operation. The START command must be valid for at least one clock cycle, but not longer than 4 clock cycles. After two start-up cycles, the DONE flag is set LOW and the data and addresses buses become active. Upon completion of the operation, $\overline{WR}$, and DONE are HIGH, $\overline{RD}$ is LOW, AD_{9-0}, RE_{18-0} and IM18-0 are in high-impedance, and execution suspended until the next command. The state of the RAMSEL pin depends on the mode determined in Configuration Register 2. The START command clears the current contents of the scaler exponent (W_{3-0}).
11	CONT	CONTinue is the inactive state for the command input. It has no internal effect. After a command has been issued, the CMD input should be set to this state. Following a start, the CMD input must be set to CONT for the operation to complete properly. If the previous command was a RESET or LOAD then the device remains in RESET.

SCEN

By the end of each N-point transform, the TMC2310 has output a block of N complex results, all of which have been right shifted (rescaled) internally by a common power-of-two scale factor. By bringing SCEN HIGH, the user can read the base-2 logarithm of this scale factor, "A," over W_{3-0}. The unsigned binary value "A" tells how much rescaling, i.e., how many one-binary-place right shifts, occurred cumulatively during all but the first radix-4 pass of the transform.

In general, the largest output word will have grown past the nominal 16-bit input format (the LSBs of the data I/O ports), into bits D_{18}, D_{17}, and D_{16}. While reading "A" over W_{3-0}, the user can also read "C," which tells how much word growth occurred during the final pass, on W_{5-4}. If C=0, then all outputs fit within the 16 LSBs of the data port; if C=1, 2, or 3, then 17, 18, or 19 bits (respectively) are needed to express the largest output value.

After issuing a single RESET (CMD_{1-0}=00) pulse, the user can read unsigned binary value B = A+C over W_{3-0}. This exponent is used when the final results are to be rescaled to 16 bits, via a sign-extending right-shift of C bits. B is read ONLY over W_{3-0} and thus has a maximum readable value of 15 decimal (binary 1111). This should be large enough for almost all applications, since the maximum word growth of a radix-4 FFT pass is a factor of 2.414 x 2.414 = 5.83. A 1024-point transform would entail five of these factors, or a cumulative factor of 6726, which requires up to 13 bits of shifting, i.e., B<14.

Figure 1 depicts the timing relationships among the SCEN, CMD_{1-0}, A, B, and C. In this example, we denote as "2" the first rising edge of CLK after the chip's DONE flag goes high. If we then bring SCEN HIGH before CLK edge 3, we will observe exponent "A" on W_{3-0} and "C" on W_{5-4}, starting t_{ENA} after CLK edge 3. The RESET pulse we issue on CLK edge 4 (CMD_{1-0}=00) cause the HI-Z output on W_{3-0}, t_{DIS} after CLK edge 5, followed by the value "B" on W_{3-0} t_{ENA} after CLK edge 6. The value B will remain on W_{3-0} until the end of the first pass of the next transform, when the first pass exponent of the next transform will replace it.

In general, A will remain on W_{3-0} until after CLK edge N+1 if CMD_{1-0} is 00 before CLK edge N. The output is then disabled for one clock cycle before B appears over the same pins, W_{3-0}.

The SCaler output ENable is used to read the block exponent and last pass overflow. When SCEN is HIGH, the six LSBs of the W-Bus are enabled and consist of the data block (scaler) exponent (W_{3-0}) and the last pass overflow ($_{5-4}$). When SCEN is LOW, the W-Bus is in high-impedance and acts as an input. At the end of an operation, the scaler exponent will show the total number of right-shift performed on the data array (both from manual and auto scaling), and the last pass scaler (W_{5-4}) will give the overflow occurring during the last pass through the data.

Control Outputs

AD_{9-0} The 10-bit ADdress output provides memory addressing for the data and window memories. The device supports sequential and bit-reversed addressing for FFTs, FIR data shift addressing, and multiple transform addressing for both read and write operations. Under normal conditions, the memory address is output on the same clock cycle as the read or write operation. Selecting pipelined addressing causes the address, $\overline{RD}$ and RAMSEL to appear one clock cycle prior to the read/ write data.

$\overline{WR}$ WRite is an active LOW pulse used to strobe data into the external data memory.

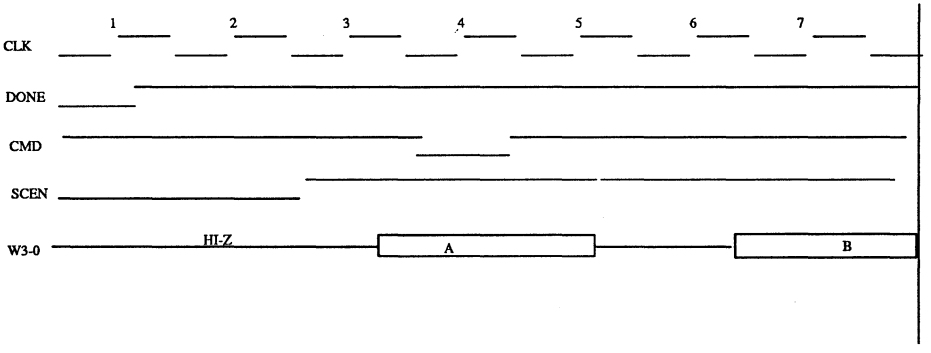


Figure 1.

Control Outputs (cont.)

$\overline{WR}$ (cont.) The address and control outputs are guaranteed to be valid before $\overline{WR}$ is LOW and after $\overline{WR}$ goes HIGH.

$\overline{RD}$ ReaD can be used to control the output enables of external memory. It indicates the direction of the RE and IM data buses. When LOW, the TMC2310 is performing a read (input) operation, and a HIGH indicates a write (outputs enabled) operation. When the DONE output flag is HIGH, $\overline{RD}$ is set LOW.

RAMSEL The RAM SELect output is used to bank select external memory and to identify the location of the initial and final results. Its operation is determined by setting a 2-bit parameter in Configuration Register 2. It can be used to select between physically separate memories or as an additional address line in paged memory systems. Detailed operation of RAMSEL is given in *Tables 3, 4, 5* and *6*.

DONE The DONE flag goes LOW after an operation is "STARTed" and remains LOW until it is complete. One cycle after DONE goes HIGH, the device is idle and final results are available in external memory. DONE= HIGH also indicates that the chip's data (RE and IM) and address (AD_{9-0}) bus drivers are in the high-impedance state, $\overline{WR}$ is inactive (HIGH), and $\overline{RD}$ is LOW. DONE can be used as a host interrupt as well as a control line to allow host system access to data memory and results.

Package Interconnections

Signal Type	Signal Name	Function	G5, H7 Package Pins	L4 Package Pins
Power	V_{DD}	Supply Voltage	H1, H2, N8, F13, A6	12, 13, 26, 38, 44, 51, 64, 76, 88, 97, 100
	GND	Ground	B1, G1, G2, N2, M7, M13, G12, B12, A10, B7	1, 10, 11, 24, 25, 27, 37, 50, 52, 63, 69, 75, 81, 87
Clock	CLK	System Clock	F2	8
Data	RE_{18-0}	Data Bus (Real)	B2, A1, A2, B3, A3, B4, A4, B5, A5, B6, A7, A8, B8, A9, B9, B10, A11, B11, A12	99, 98, 96, 95, 94, 93, 92, 91, 90, 89, 86, 85, 84, 83, 82, 80, 79, 78, 77
	IM_{18-0}	Data Bus (Imaginary)	M3, N3, M4, N4, M5, N5, M6, N6, N7, M8, N9, M9, N10, M10, N11, M11, N12, N13, M12	28, 29, 30, 31, 32, 33, 34, 35, 36, 39, 40, 41, 42, 43, 45, 46, 47, 48, 49
	W_{16-0}	Window/Coefficient Bus	A13, B13, C12, C13, D12, D13, E12, E13, F12, G13, H13, H12, J13, J12, K13, K12, L13	74, 73, 72, 71, 70, 68, 67, 66, 65, 62, 61, 60, 59, 57, 56, 55, 54
Controls	CMD_{1-0}	Command Inputs	C1, C2	3, 2
	SCEN	Scaler Exponent Enable	L12	53
	AD_{9-0}	Address Bus Output	M2, N1, M1, L2, L1, K2, K1, J2 J1, F1	23, 22, 21, 20, 18, 17, 16, 15, 14, 9
	RAMSEL	Source/Target RAM Select	D1	5
	$\overline{RD}$	External Memory Enable	E2	6
	$\overline{WR}$	Write Strobe Output	E1	7
Flags	DONE	Function Complete Flag	D2	4
No Connect	NC	No Connect Pins	-	19, 58
	-	Index Pin	C3	

Device Operation

Upon power-up of the device, the user should immediately issue a RESET command (CMD_{1-0}=00), forcing the device into a "DONE" state. A RESET must be performed prior to any attempt to initialize internal configuration registers. Following the RESET, the DONE flag is HIGH and the address and data (RE, IM and W) buses are set to high-impedance.

Prior to performing any operation, the user must initialize and configure the device by programming two internal configuration registers (CR1, CR2). There are two methods of initializing the registers. Data may be stored in external memory, address location "0" or they may be placed directly on the RE-Bus (RE_{15-3}). A LOAD command (CMD_{1-0}=01) causes a read on the RE-Bus with AD_{9-0}=0. Data read from memory (or directly from the bus) are stored into the configuration register selected by bit 15 of the data word. A minimum of two load commands are required to input the two words, CR1 and CR2. The loads of CR1 and CR2 may be performed consecutively or separately by one or more "continue" cycles.

The configuration registers define the function to be performed as well as other operating parameters. Once programmed, device operation is controlled by the two-bit command control (CMD_{1-0}). Commands are used to begin or suspend operations and to load configuration registers. Operations may be repeated (under the same conditions) without reloading the configuration registers by issuing additional START commands. If the RESET command has been applied after the configuration registers have been loaded, however, it may be necessary to reload Configuration Register 2, since RESET will clear bits 3, 4 and 5 of CR2 and the internal SCaler ENable (SCEN) register.

Once the input data have been stored in external memory (beginning at address 0) and the configuration registers initialized, device operation begins following a START command. After the START command has been initiated, the command input must be set to CONT (CMD_{1-0}=11) within 4 clock cycles for proper operation. During execution, the device takes control of the local data memory bus, enables the address output bus and generates external memory control. The DONE flag will be set HIGH to indicate that the TMC2310 has completed its operations and final results are available in memory.

All intermediate and final results are stored in external memory in 19-bit, two's complement format. Upon completion of the operation, the SCaler ENable input (SCEN) can be used to read the last pass overflow and the scaler exponent. The last pass overflow (W_{5-4}) indicates the word growth that occurred during execution of single pass operations or, during the final butterfly pass of a transform. The 4-bit scaler exponent (W_{3-0}) indicates the number of right-shifts performed on the data array during a multiple pass transform (common data exponent). At the end of an operation, the host system must read the scaler exponent prior to a RESET command. Failure to do so will result in an incorrect scaler exponent value. A RESET command applied for one cycle will cause the last pass overflow to be added to the current value of the scaler exponent. RESET held for more than one clock cycle will clear the scaler exponent field (W_{5-0}). Immediately after a START command, the scaler exponent will be initialized.

Configuration Register 1 (CR1)

Configuration Register 1 defines the operation, transform length, FFT addressing sequence and scaling modes.

Function Codes

Table 1 indicates the input and output values for each function. The RE and IM buses are multiplexed for reads and writes while the W-Bus is used for input only. W-Bus(1) and W-Bus(2) indicate the input for first and second cycle read on the W-Bus, respectively. To input two words, the read address for both W-Bus operands is available during the first (read) cycle. It may be necessary for the user to register the address or data externally for proper synchronization (see Applications Section).

In general, single pass operations (MPY, MAC, MAGSQ) read data from memory and output results to the same address, overwriting the original input data. If the input data are to be saved, use of the RAMSEL allows results to be output to a separate result memory or directly to the host system. All data should be stored in external memory beginning at address 0. The TMC2310 begins all operations at address 0.

Table 1 includes operations designated as "2-Re" (2 Real). "R/I" (Real/Imaginary), and "Cmplx" (Complex). The distinction is as follows:

2-Re These operations involve only a single data word from the W-Bus. The data word

Function Codes (continued)

input in the W–Bus is applied to the data input on both the RE and IM data buses.

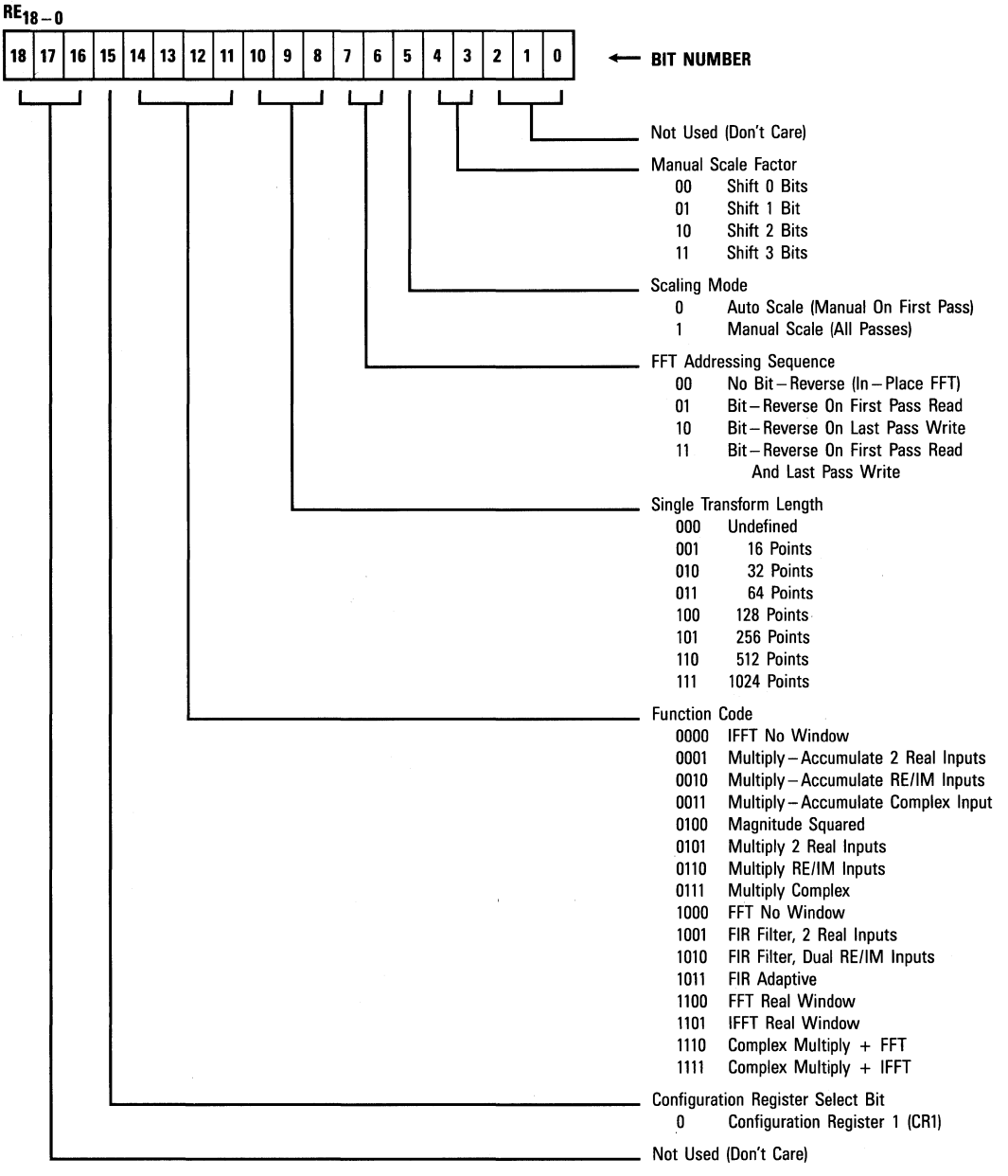
R/I — These operations involve two values input from the W–Bus with the first W–Bus operand applied to the RE data and the second applied to the IM data. No cross terms are evaluated.

Cmplx — These operations involve two W–Bus operands, interpreted as a complex data value. The function involves a complex operation including cross terms.

Table 1. Function Codes vs. Bus Function

Code	Function	Inputs				Outputs	
		RE–Bus	IM–Bus	W–Bus(1)	W–Bus(2)	RE–Bus	IM–Bus
0000	IFFT No–Window	R	I	–	–	Complex IFFT Results	
0001	MPY–ACC 2–Re	R	I	W	–	Σ RW	Σ IW
0010	MPY–ACC R/I	R	I	W_1	W_2	Σ RW_1	Σ IW_2
0011	MPY–ACC Cmplx	R	I	W_R	W_I	Σ $RW_R - IW_I$	Σ $IW_R + \Sigma$ RW_I
0100	MAGSQ	R	I	–	–	$[R^2 + I^2]/2$	$[R^2 + I^2]/2$
0101	MPY 2–Re	R	I	W	–	RW	IW
0110	MPY R/I	R	I	W_1	W_2	RW_1	IW_2
0111	MPY Cmplx	R	I	W_R	W_I	$RW_R - IW_I$	$IW_R + RW_I$
1000	FFT No–Window	R	I	–	–	Complex FFT Results	
1001	FIR 2–Re	R_m	I_m	W_n	–	Σ R_mW_n	Σ I_mW_n
1010	FIR R/I	R_m	I_m	W_{1n}	W_{2n}	Σ R_mW_{1n}	Σ I_mW_{2n}
1011	FIR Adaptive	R_m	C_n	σ	–	Σ R_mC_n	$C_n(1 - \sigma)$
1100	FFT Re–Window	R	I	W	–	Complex FFT Results	
1101	IFFT Re–Window	R	I	W	–	Complex IFFT Results	
1110	Cmplx MPY + FFT	R	I	W_R	W_I	Complex FFT Results	
1111	Cmplx MPY + IFFT	R	I	W_R	W_I	Complex IFFT Results	

Configuration Register 1 (CR1) Format



CR1[14:11]

0000 IFFT No Windowing. A complex Inverse Fast Fourier Transform is performed on data stored in external memory. No windowing is performed (rectangular window) during the IFFT and the W–Bus is unused. The memory addressing sequence and the transform length are determined by other parameters. The N–point inverse FFT is defined by:

$$h(n) = \sum_{k=0}^{N-1} H(k)e^{+j2\pi nk/N}$$

0001 Multiply–Accumulate Two Real Inputs. Both the RE and IM data are multiplied by the data word input on the W–Bus. Results are accumulated and written back to external memory. The output to memory is the sum of all previous multiplications. (e.g. Address 20_{10} = sum of first 21 products (0–20), Address 49_{10} = sum of first 50 products, etc.)

0010 Multiply–Accumulate Real/Imaginary. The RE data input is multiplied by the first word input on the W–Bus. The IM input is multiplied by the second word input on the W–Bus. The output to memory is the accumulation of all previous multiplications.

$$RE_{out}(N) = \sum_{K=0}^{N} RE_{in}(k)W_1(k)$$

$$IM_{out}(N) = \sum_{K=0}^{N} IM_{in}(k)W_2(k)$$

0011 Multiply–Accumulate Complex. Complex multiplication is performed on each (RE, IM) and (W_R, W_I) pair. The output to memory is the accumulation of all previous complex multiplications. Input of a complex operand on the W–Bus is done on two consecutive clock cycles.

$$RE_{out}(N) = \sum_{K=0}^{N} [RE_{in}(k)W_R(k) - IM_{in}(k)W_I(k)]$$

$$IM_{out}(N) = \sum_{K=0}^{N} [IM_{in}(k)W_R(k) + RE_{in}(k)W_I(k)]$$

($W_R = W_1$, $W_I = W_2$)

0100 **Magnitude Squared. The RE and IM data are squared separately. The squares are summed, halved and their most significant portions are output to both the RE and IM data memories.**

$$RE_{out}(n) = IM_{out}(n) = [RE_{in}^2(n) + IM_{in}^2(n)]/2$$

0101 Multiply 2–Real. The RE and IM data are multiplied by the single data word input on the W–Bus during the read cycle. Results are output to the corresponding memory address.

$$RE_{out}(n) = RE_{in}(n)W_1(n)$$
$$IM_{out}(n) = IM_{in}(n)W_1(n)$$

0110 Multiply Real/Imaginary. The RE data value is multiplied by the data input on the first W–Bus cycle. The IM input is multiplied by the data input on the second W–Bus cycle. The result output to memory is:

$$RE_{out}(n) = RE_{in}(n)W_1(n)$$
$$IM_{out}(n) = IM_{in}(n)W_2(n)$$

0111 Multiply Complex. A complex multiplication is performed on the data input on the RE, IM and W–Bus inputs. The complex output to memory is:

$$(RE + jIM)(W_R + jW_I) =$$
$$RE_{out}(n) = [RE_{in}(n)W_R(n)] - [IM(n)_{in}W_I(n)]$$
$$IM_{out}(n) = [IM_{in}(n)W_R(n)] + [RE(n)_{in}W_I(n)]$$

1000 FFT No Windowing. A complex Fast Fourier Transform is performed on data stored in external memory. No windowing is performed (rectangular window) during the FFT and the W–Bus is unused. The memory addressing sequence and the transform length are determined by other parameters. The forward FFT is defined by:

$$H(k) = \sum_{n=0}^{N-1} h(n)e^{-j2\sigma nk/N}$$

CR1[14:11] (continued)

1001 FIR 2–Real. Finite Impulse Response filtering is done by performing a RAM based multiplication–accumulation on data and coefficients stored in external memory. Multiplication with accumulation is performed between filter coefficients input on the W–Bus and the RE and IM data. The RE and IM data are shifted down one location in memory with the final accumulated result written into location N – 1. Two separate data sets may be convolved simultaneously, using the RE and IM data and one filter coefficient data set. (See Applications section for more detailed descriptions of FIR operation.) The output is:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1)_{out} = \sum_{n=0}^{N-1} RE(n)W_1(n)$$

$$IM(i)_{out} = IM(i+1)_{in},\ IM(N-1)_{out} = \sum_{n=0}^{N-1} IM(n)W_1(n)$$

1010 FIR Real/Imaginary. Finite Impulse Response filtering is done by performing a RAM based multiplication–accumulation on data and coefficients stored in external memory. Multiplication with accumulation is performed between filter coefficients input on the W–Bus, and the RE and IM data. The RE and IM data are shifted down one location in memory with the final accumulated result written into location N – 1. When the next input sample is loaded into address N – 1 the operation may be re–STARTed to form the next sum. Two sets of coefficients are used, both input through the W–Bus, one for RE data and a second for IM data. (See Applications section for more detailed description of FIR Operation.) The data outputs are:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1)_{out} = \sum_{n=0}^{N-1} RE(n)W_1(n)$$

$$IM(i)_{out} = IM(i+1)_{in},\ IM(N-1)_{out} = \sum_{n=0}^{N-1} IM(n)W_2(n)$$

1011 FIR Adaptive. Adaptive FIR filtering allows concurrent updates to filter coefficients by the value specified on the W–Bus. The RE–Bus is used for input data and the IM–Bus used for filter coefficients. The W–Bus determines the coefficient update value (σ). The data on the RE–Bus is multiplied, accumulated and shifted down one address in memory. The final convolution result is output to address N – 1. The next input sample is stored in address N – 1, and the operation re–STARTed to form the next sum. The filter coefficients, input on the IM–Bus, are modified and stored back to their original address locations as follows:

$IM(i)_{out} = IM(i)_{in}(1-\sigma(i))$ or,
New Coefficient = [Old Coefficient] • [1 – update value]

Update values are input on the W–Bus for each coefficient (during the read cycle). The data output is:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1) = \sum_{k=0}^{N-1} RE(k)IM(k)$$

1100 FFT Real Window. An FFT is performed on complex data in external memory. During the first FFT pass, the RE and IM data are multiplied by the window coefficients input through the W–Bus. The real data window is applied to both the RE and IM data. The forward FFT with real windowing is defined by:

$$H(k) = \sum_{n=0}^{N-1} h(n)w(n)e^{-j2\pi nk/N}$$

1101 IFFT Real Window. An Inverse FFT is performed on the complex data in external memory. During the first IFFT pass, the RE and IM data are multiplied by the window coefficients input through the W–Bus. The real data window is applied to both the RE and IM data. The inverse FFT with real windowing is defined by:

$$h(n) = \sum_{k=0}^{N-1} H(k)w(k)e^{+j2\pi nk/N}$$

Transforms

1110 Complex Multiplication + FFT. Prior to performing the FFT, a complex multiplication is performed between the RE and IM data and complex data stored in external memory input through the W–Bus. This operation requires one additional pass, compared to the FFT with Real Window, to complete the complex multiplication.

1111 Complex Multiplication + IFFT. Prior to performing the inverse FFT, a complex multiplication is performed between the RE and IM data and complex data stored in external memory and input through the W–Bus. This operation requires one additional pass, compared to the IFFT with Real Window, to perform the complex multiplication.

Single Transform Length CR1[10:8]

000 Undefined
001 16 data points (Recommended for Non–FFT/IFFT Operations)
010 32 data points
011 64 data points
100 128 data points
101 256 data points
110 512 data points
111 1024 data points

This field defines the number of data points for a single transform. To reduce computational overhead, multiple transforms can be performed concurrently up to the 1024–point limit. This field sets the number of points for a single transform while the number of concurrent transforms is determined by Configuration Register 2 (CR2[14:8]). The total number of data points for any operation is obtained by multiplying the single transform length by the "number of transforms" in CR2:

(Transform Length)•(No. of Transforms)=Total number of data points

For all non–transform operations, use of transform length = 16 is recommended. This provides the maximum flexibility in selecting the size of the data set, allowing any number of points which is a multiple of 16 (see Table 2).

FFT Addressing Sequence CR1[7:6]

00 No Bit–reverse (In–Place, Sequential Addressing) (Use for Non–FFT Operations)
01 Bit–reverse address during first pass read
10 Bit–reverse address during last pass write
11 Bit–reverse address during first pass read and last pass write

Several types of address sequences are available for transforms. Data scrambling is required when performing the FFT/IFFT. If the data is scrambled in memory prior to the start of the transform, then it can be done "in–place", thereby reducing the external memory requirements (see Applications). If data is stored in sequence, the TMC2310 must perform scrambling during the first pass of the transform (CR1[7:6] = 01 or 11). The scrambling amounts to a bit–wise reversing of the memory address. When performing the "bit–reversed" addressing, the user must provide additional memory for intermediate storage to avoid overwriting unused input data. The user must also store the window function in either bit–reversed or sequential order to match the ordering to the input data. (See Applications section.)

Bit–reversing the memory address during the last data pass write (CR1[7:6] = 10 or 11) may be useful if the data will undergo additional FFT processing. The final results are placed in scrambled order in preparation for the next operation.

Scaling Modes CR1[5]

0 Auto Scaling
1 Manual Scaling (Use for All Non–FFT Operations)

This field determines the input data shifting. For multiple pass transforms using auto scaling, the input data is shifted by the number of bits set by the manual scale factor (CR1[4:3]) for the first pass or by the Last Pass Overflow scaler (W_{5-4}) determined from the last pass of the previous operation (CR2[3]). Subsequent passes shift the data based on the overflow of the previous pass. During each pass of the FFT, the maximum overflow (0–3 bits) is monitored as results are output to external memory. The overflow value is used as a shift count for incoming data on the next pass. The number of shifts performed during all passes (including the first pass) and the overflow from the final data pass are available on the W–Bus using the SCaler ENable control (SCEN).

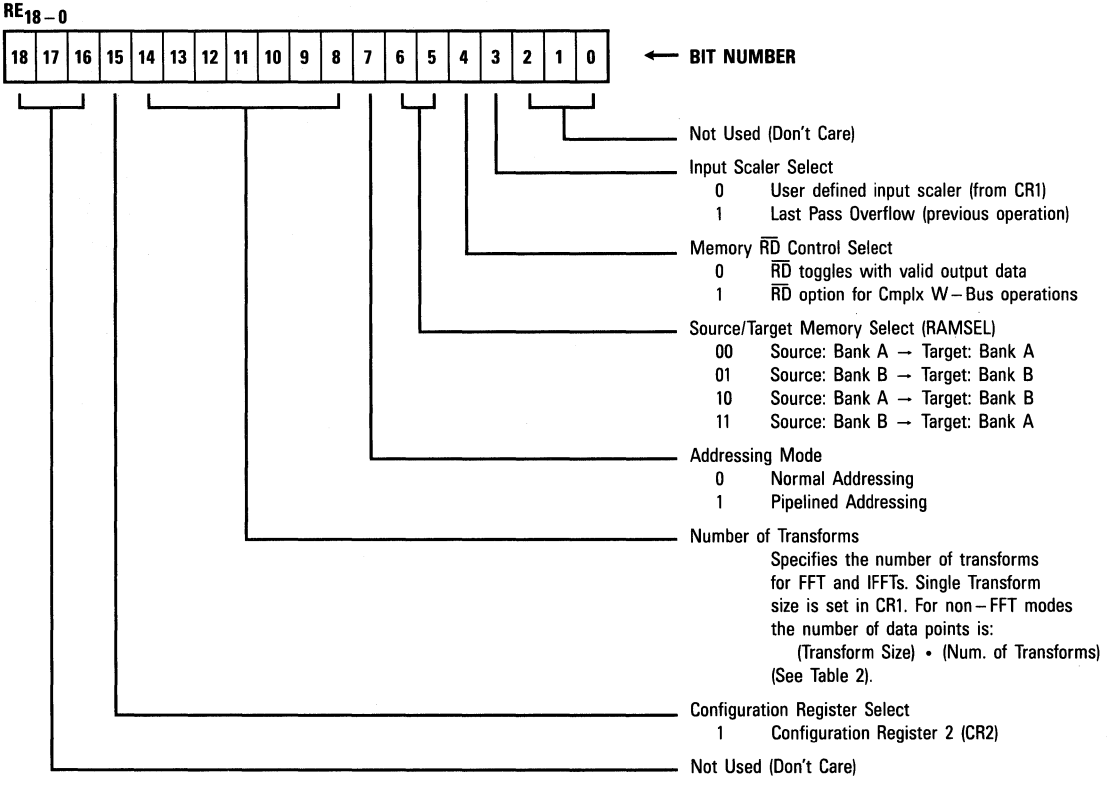
Use of manual scaling disables the overflow detection circuitry and shifts input data on every pass. The shift amount for each pass is determined by the manual scale factor set in CR1[4:3].

Manual Scale Factor CR1[4:3]

00	Shift by 0 bits
01	Shift by 1 bit
10	Shift by 2 bits
11	Shift by 3 bits

This field specifies the number of shifts performed on the input data. In auto scaling, it defines the shift performed on the first data pass only. For manual scaling, the data is shifted by this value on each pass. If the Input Scaler Select (CR2[3]) is activated to use the Last Pass Overflow scaler, then the Manual Scale Factor will be overridden during the first data pass in either the Auto or Manual Scaling modes. Also, the initial or first pass shift factor specified for either Auto or Manual Scaling will not be included in the Data Block (Scaler) exponent. W[3:0]. The user must be cautious when performing manual scaling in order to avoid arithmetic errors due to incorrect scaling. (See Applications Section.) If the original data are all only 16-bits wide, then any initial scale factor may be used, with 0 yielding the best arithmetic noise performance. If one or more 19-bit values are included among the input data, an initial scale factor of 3 is need to guard against first-pass overflow.

Configuration Register 2 (CR2) Format



Configuration Register 2 (CR2)

Configuration Register 2 is used to define the operation of the RAMSEL and $\overline{RD}$ signals, the addressing modes and the total number of data points for each operation.

Number of 16-Point Blocks CR2[14:8]

0000000	Undefined
bbbbbbb	Number of 16-point transforms
bbbbbb0	Number of 32-point transforms
bbbbb00	Number of 64-point transforms
bbbb000	Number of 128-point transforms
bbb0000	Number of 256-point transforms
bb00000	Number of 512-point transforms
1000000	Single 1024-point transform

This parameter is used in conjunction with the single transform lingth set in CR1. The total number of points is determined by multiplying this value by 16. The possible combinations of transform length and number of transform/ data points are specified in Table 2.

Table 2. Possible Combinations of Transform Length and Number of Transforms

Trans. Length CR1[10:8]	Num. Blocks CR2[14:8]	Number of FFT Transforms	Number of Taps or Data Words
xxx	0000000	Undefined for all transform sizes	
000	xxxxxxx	Undefined for all transform sizes	
001 16 – Point	0000001	1 Transform	16 Taps/Words
	0000010	2 Transforms	32 Taps/Words
	0000011	3 Transforms	48 Taps/Words
	•	•	•
	•	•	•
	1000000	64 Transforms	1024 Taps/Words
010 32 – Point	0000010	1 Transform	32 Taps/Words
	0000100	2 Transforms	64 Taps/Words
	0000110	3 Transforms	96 Taps/Words
	•	•	•
	•	•	•
	1000000	32 Transforms	1024 Taps/Words
011 64 – Point	0000100	1 Transform	64 Taps/Words
	0001000	2 Transforms	128 Taps/Words
	0001100	3 Transforms	192 Taps/Words
	•	•	•
	•	•	•
	1000000	16 Transforms	1024 Taps/Words
100 128 – Point	0001000	1 Transform	128 Taps/Words
	0010000	2 Transforms	256 Taps/Words
	0011000	3 Transforms	384 Taps/Words
	•	•	•
	•	•	•
	1000000	8 Transforms	1024 Taps/Words
101 256 – Point	0010000	1 Transform	256 Taps/Words
	0100000	2 Transforms	512 Taps/Words
	0110000	3 Transforms	768 Taps/Words
	1000000	4 Transforms	1024 Taps/Words
110 512 – Point	0100000	1 Transform	512 Taps/Words
	1000000	2 Transforms	1024 Taps/Words
111 1024 – Point	1000000	1 Transform	1024 Taps/Words

Addressing Mode CR2[7]

0 Normal Addressing
1 Pipelined Addressing

This field selects the addressing mode for external memory access. In normal addressing, the memory address, $\overline{RD}$, RAMSEL and the read/write data are output on the same clock cycle. In pipelined addressing, the address, $\overline{RD}$, and RAMSEL outputs appear one clock cycle prior to the data. This enables the system to setup one cycle in advance by externally registering the address and controls. In both modes, the $\overline{WR}$ strobe is synchronized with the data and is guaranteed to meet data setup and hold times. Pipelined addressing is supported for all device operations. (See Applications section.)

Source/Target Memory Select CR2[6:5]

00 Source: Bank A (RAMSEL = HIGH)
Target: Bank A (RAMSEL = HIGH)
01 Source: Bank B (RAMSEL = LOW)
Target: Bank B (RAMSEL = LOW)
10 Source: Bank A (RAMSEL = HIGH)
Target: Bank B (RAMSEL = LOW)
11 Source: Bank B (RAMSEL = LOW)
Target: Bank A (RAMSEL = HIGH)

This field allows the user to select the locations of the initial data inputs and the final data results in multiple memory bank systems. Use of banked memory systems allow I/O operations to be overlapped with arithmetic processing. RAMSEL allows the device to select between the two banks of memory (RAMSEL = HIGH indicating Bank A and RAMSEL = LOW indicating memory Bank B). It may also be used as an additional address line in paged memory systems.

Transform operations require multiple data passes. The state of RAMSEL for each pass is based on the FFT addressing sequence (CR1[7:6]), the pass number and the Source/Target Memory select. Passes involving bit-reversed addressing require that RAMSEL toggle between reading and writing to prevent overwriting unused data. The TMC2310 identifies passes involving bit-reversed addressing and sets RAMSEL accordingly. During a bit-reverse pass, the TMC2310 either reads data with RAMSEL = HIGH and outputs with RAMSEL = LOW, or, reads with RAMSEL = LOW and outputs with RAMSEL = HIGH. Systems utilizing bit-reversed addressing must use RAMSEL for memory control to obtain proper results.

The operation of RAMSEL for transform operations is defined in tables 3, 4, 5 and 6. The state of RAMSEL is shown for each pass. The table indicates the logic level of RAMSEL for input and output during each pass. All single pass (non-FFT) operations (except FIR) allow the source and target data locations to be specified with this two-bit control parameter.

For FIR filter operations, RAMSEL has been designed to differentiate device outputs between shifted data samples and the accumulated convolutional sum output at the end of each pass. When CR2[6:5] is set to "00" or "10" RAMSEL remains HIGH (Bank A) for all reads and writes (data shifting in memory) except during the last write. The last write of an FIR pass is the convolutional sum, which is output with RAMSEL = LOW. When CR2[6:5] is set to "01" or "11" RAMSEL remains LOW (Bank B) for all reads and writes except during the last output cycle when the sum result is written to memory with RAMSEL = HIGH.

Upon power-up RESET, RAMSEL will be in a HIGH state. Once CR2 has been loaded into the device, RAMSEL will reflect the Source/Target Memory Selection specified in CR2[6:5]. After the operation has been completed and the DONE flag has returned to a HIGH state, RAMSEL will return to the "Source" state designated in CR2[6:5] unless a RESET has been applied. RESET will clear CR2[5] and force RAMSEL HIGH.

Application of the RESET command will clear CR2[5] and force RAMSEL = HIGH. CR2 must be loaded into the device to activate this option.

Memory $\overline{RD}$ Control Select CR2[4]

0 $\overline{RD}$ toggles to denote valid output results
1 $\overline{RD}$ option for Complex W-Bus operations

During all device operations, $\overline{RD}$ indicates the direction of the RE and IM data buses. When LOW, the TMC2310 is performing a read (input) operation, and a HIGH indicates a write (outputs enabled) operation. When the device performs operations requiring complex inputs to the W-Bus, real and imaginary inputs are time multiplexed on successive cycles. W_R inputs appear with the RE and IM data inputs ($\overline{RD}$ = LOW) while the W_I inputs appear

on the following cycle, when the device is outputting results ($\overline{RD}$ = HIGH). Due to the latency in the architecture of the device, however, results will not appear for at least seven cycles from the corresponding inputs. Under normal operations (CR2[4] = 0) the $\overline{RD}$ signal will not be activated until the first valid result appears, afterwhich $\overline{RD}$ will toggle on successive cycles. For operations that require complex W–Bus inputs CR2[4] can be set HIGH to allow the $\overline{RD}$ signal to toggle upon application of the START command. This will enable the W_R and W_I inputs to be synchronized with the FALLING and RISING edge of the $\overline{RD}$ signal, respectively. For modes that do not involve complex inputs to the W–Bus the $\overline{RD}$ Control Select should be set LOW.

Application of the RESET command will clear CR2[4], therefore, CR2 must be loaded into the device to activate this option.

Input Scaler Select (First Pass Only) CR2[3]

0 First Pass Input Scaler defined in CR1[4:3]
1 Last Pass Overflow from previous operation used as Scaler Input

Under normal operations, the input data scale factor must be specified for the first pass of any operation using the Manual Scale Factor CR1[4:3]. For some applications, it may be necessary to perform additional signal processing functions on the existing data set. When activated (CR2[3] = 1), this option allows the Last Pass Overflow scaler from the previous operation to be used as the input scaler for the next operation. This feature eliminates the need to extract the W5-4 field from the W-Bus and will be useful to post process the data after a particular application. For example, the user may want to rescale the 19-bit data to 16 bits following an FFT operation. By activating this feature, the Last Pass Overflow scaler (from the FFT) will be used to rescale the data as it is input to the device for a multiplication by 1.0 (0.9999. . .). Additional operations that will benefit from this feature are MAGSQ or a filter multiplication following the FFT.

Application of the RESET command will clear CR2[3] and the scaler exponent field (W_{5-0}). CR2 must be loaded into the device to activate this option.

Tables 3, 4, 5 and 6 show the operation of RAMSEL for multiple pass transforms. The state of RAMSEL is shown for read and write operations during each data pass.

For example:

16–point FFT (Real or No Window)

Source = Bank A; Target = Bank A (CR2[6:5] = 00)
Bit–reverse addressing on first pass read (CR1[7:6] = 01)

Pass 0: Input data with RAMSEL = H (HIGH)
Output data with RAMSEL = L (LOW)
(Data moved from Bank A to Bank B)

Pass 1: Input data with RAMSEL = LOW
Output data with RAMSEL = HIGH
(Data moved from Bank B back to Bank A)

16–point Complex Multiply + FFT

Source = Bank B; Target = Bank B (CR2[6:5] = 01)
Bit–reverse addressing on first pass read (CR1[7:6] = 01)

Pass W: Input data with RAMSEL = L (LOW)
Output data with RAMSEL = L (LOW)
(Data remains in Bank B)

Pass 0: Input data with RAMSEL = L (LOW)
Output data with RAMSEL = H (HIGH)
(Data moved from Bank B to Bank A)

Pass 1: Input data with RAMSEL = HIGH
Output data with RAMSEL = LOW
(Data moved from Bank A back to Bank B)

The tables are valid for single and multiple transforms, however, RAMSEL operation is determined by the single transform size only.

Table 3a. RAMSEL Operation for Source = Bank A (RAMSEL=HIGH); Target = Bank A (RAMSEL=HIGH) Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
00	00	16	H/H	H/H			
		32	H/H	H/H	H/H		
		64	H/H	H/H	H/H		
		128	H/H	H/H	H/H	H/H	
		256	H/H	H/H	H/H	H/H	
		512	H/H	H/H	H/H	H/H	H/H
		1024	H/H	H/H	H/H	H/H	H/H
	01, 10 or 11	16	H/L	L/H			
		32	H/L	L/L	L/H		
		64	H/L	L/L	L/H		
		128	H/L	L/L	L/L	L/H	
		256	H/L	L/L	L/L	L/H	
		512	H/L	L/L	L/L	L/L	L/H
		1024	H/L	L/L	L/L	L/L	L/H

Note: 1. H = HIGH
L = LOW

Table 3b. RAMSEL Operation for Source = Bank A (RAMSEL=HIGH); Target = Bank A (RAMSEL=HIGH) Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
00	00	16	H/H	H/H	H/H			
		32	H/H	H/H	H/H	H/H		
		64	H/H	H/H	H/H	H/H		
		128	H/H	H/H	H/H	H/H	H/H	
		256	H/H	H/H	H/H	H/H	H/H	
		512	H/H	H/H	H/H	H/H	H/H	H/H
		1024	H/H	H/H	H/H	H/H	H/H	H/H
	01, 10 or 11	16	H/H	H/L	L/H			
		32	H/H	H/L	L/L	L/H		
		64	H/H	H/L	L/L	L/H		
		128	H/H	H/L	L/L	L/L	L/H	
		256	H/H	H/L	L/L	L/L	L/H	
		512	H/H	H/L	L/L	L/L	L/L	L/H
		1024	H/H	H/L	L/L	L/L	L/L	L/H

Notes: 1. H = HIGH
L = LOW
2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 4a. RAMSEL Operation for Source = Bank B (RAMSEL=LOW); Target = Bank B (RAMSEL=LOW) Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
01	00	16	L/L	L/L			
		32	L/L	L/L	L/L		
		64	L/L	L/L	L/L		
		128	L/L	L/L	L/L	L/L	
		256	L/L	L/L	L/L	L/L	
		512	L/L	L/L	L/L	L/L	L/L
		1024	L/L	L/L	L/L	L/L	L/L
	01, 10 or 11	16	L/H	H/L			
		32	L/H	H/H	H/L		
		64	L/H	H/H	H/L		
		128	L/H	H/H	H/H	H/L	
		256	L/H	H/H	H/H	H/L	
		512	L/H	H/H	H/H	H/H	H/L
		1024	L/H	H/H	H/H	H/H	H/L

Note: 1. H = HIGH
L = LOW

Table 4b. RAMSEL Operation for Source = Bank B (RAMSEL=LOW); Target = Bank B (RAMSEL=LOW) Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
01	00	16	L/L	L/L	L/L			
		32	L/L	L/L	L/L	L/L		
		64	L/L	L/L	L/L	L/L		
		128	L/L	L/L	L/L	L/L	L/L	
		256	L/L	L/L	L/L	L/L	L/L	
		512	L/L	L/L	L/L	L/L	L/L	L/L
		1024	L/L	L/L	L/L	L/L	L/L	L/L
	01, 10 or 11	16	L/L	L/H	H/L			
		32	L/L	L/H	H/H	H/L		
		64	L/L	L/H	H/H	H/L		
		128	L/L	L/H	H/H	H/H	H/L	
		256	L/L	L/H	H/H	H/H	H/L	
		512	L/L	L/H	H/H	H/H	H/H	H/L
		1024	L/L	L/H	H/H	H/H	H/H	H/L

Notes: 1. H = HIGH
L = LOW
2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 5a. RAMSEL Operation Source = Bank A; Target = Bank B Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
10	00, 01	16	H/L	L/L			
		32	H/L	L/L	L/L		
		64	H/L	L/L	L/L		
		128	H/L	L/L	L/L	L/L	
		256	H/L	L/L	L/L	L/L	
		512	H/L	L/L	L/L	L/L	L/L
		1024	H/L	L/L	L/L	L/L	L/L
	10	16	H/H	H/L			
		32	H/H	H/H	H/L		
		64	H/H	H/H	H/L		
		128	H/H	H/H	H/H	H/L	
		256	H/H	H/H	H/H	H/L	
		512	H/H	H/H	H/H	H/H	H/L
		1024	H/H	H/H	H/H	H/H	H/L
	11	16	Not Allowed				
		32	H/L	L/H	H/L		
		64	H/L	L/H	H/L		
		128	H/L	L/H	H/H	H/L	
		256	H/L	L/H	H/H	H/L	
		512	H/L	L/H	H/H	H/H	H/L
		1024	H/L	L/H	H/H	H/H	H/L

Note: 1. H = HIGH
L = LOW

Table 5b. RAMSEL Operation Source = Bank A; Target = Bank B Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
10	00	16	H/L	L/L	L/L			
		32	H/L	L/L	L/L	L/L		
		64	H/L	L/L	L/L	L/L		
		128	H/L	L/L	L/L	L/L	L/L	
		256	H/L	L/L	L/L	L/L	L/L	
		512	H/L	L/L	L/L	L/L	L/L	L/L
		1024	H/L	L/L	L/L	L/L	L/L	L/L
	01	16	H/H	H/L	L/L			
		32	H/H	H/L	L/L	L/L		
		64	H/H	H/L	L/L	L/L		
		128	H/H	H/L	L/L	L/L	L/L	
		256	H/H	H/L	L/L	L/L	L/L	
		512	H/H	H/L	L/L	L/L	L/L	L/L
		1024	H/H	H/L	L/L	L/L	L/L	L/L
	10	16	H/H	H/H	H/L			
		32	H/H	H/H	H/H	H/L		
		64	H/H	H/H	H/H	H/L		
		128	H/H	H/H	H/H	H/H	H/L	
		256	H/H	H/H	H/H	H/H	H/L	
		512	H/H	H/H	H/H	H/H	H/H	H/L
		1024	H/H	H/H	H/H	H/H	H/H	H/L
	11	16	Not Allowed					
		32	H/H	H/L	L/H	H/L		
		64	H/H	H/L	L/H	H/L		
		128	H/H	H/L	L/H	H/H	H/L	
		256	H/H	H/L	L/H	H/H	H/L	
		512	H/H	H/L	L/H	H/H	H/H	H/L
		1024	H/H	H/L	L/H	H/H	H/H	H/L

Notes: 1. H = HIGH
L = LOW

2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 6a. RAMSEL Operation Source = Bank B; Target = Bank A Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
11	00, 01	16	L/H	H/H			
		32	L/H	H/H	H/H		
		64	L/H	H/H	H/H		
		128	L/H	H/H	H/H	H/H	
		256	L/H	H/H	H/H	H/H	
		512	L/H	H/H	H/H	H/H	H/H
		1024	L/H	H/H	H/H	H/H	H/H
	10	16	L/L	L/H			
		32	L/L	L/L	L/H		
		64	L/L	L/L	L/H		
		128	L/L	L/L	L/L	L/H	
		256	L/L	L/L	L/L	L/H	
		512	L/L	L/L	L/L	L/L	L/H
		1024	L/L	L/L	L/L	L/L	L/H
	11	16	Not Allowed				
		32	L/H	H/L	L/H		
		64	L/H	H/L	L/H		
		128	L/H	H/L	L/L	L/H	
		256	L/H	H/L	L/L	L/H	
		512	L/H	H/L	L/L	L/L	L/H
		1024	L/H	H/L	L/L	L/L	L/H

Note: 1. H = HIGH
L = LOW

Table 6b. RAMSEL Operation Source = Bank B; Target = Bank A Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
11	00	16	L/H	H/H	H/H			
		32	L/H	H/H	H/H	H/H		
		64	L/H	H/H	H/H	H/H		
		128	L/H	H/H	H/H	H/H	H/H	
		256	L/H	H/H	H/H	H/H	H/H	
		512	L/H	H/H	H/H	H/H	H/H	H/H
		1024	L/H	H/H	H/H	H/H	H/H	H/H
	01	16	L/L	L/H	H/H			
		32	L/L	L/H	H/H	H/H		
		64	L/L	L/H	H/H	H/H		
		128	L/L	L/H	H/H	H/H	H/H	
		256	L/L	L/H	H/H	H/H	H/H	
		512	L/L	L/H	H/H	H/H	H/H	H/H
		1024	L/L	L/H	H/H	H/H	H/H	H/H
	10	16	L/L	L/L	L/H			
		32	L/L	L/L	L/L	L/H		
		64	L/L	L/L	L/L	L/H		
		128	L/L	L/L	L/L	L/L	L/H	
		256	L/L	L/L	L/L	L/L	L/H	
		512	L/L	L/L	L/L	L/L	L/L	L/H
		1024	L/L	L/L	L/L	L/L	L/L	L/H
	11	16	Not Allowed					
		32	L/L	L/H	H/L	L/H		
		64	L/L	L/H	H/L	L/H		
		128	L/L	L/H	H/L	L/L	L/H	
		256	L/L	L/H	H/L	L/L	L/H	
		512	L/L	L/H	H/L	L/L	L/L	L/H
		1024	L/L	L/H	H/L	L/L	L/L	L/H

Notes:
1. H = HIGH
   L = LOW
2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Figure 3. Input/Clock Timing

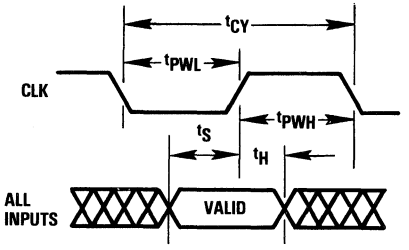


Figure 4. Read Cycle Timing

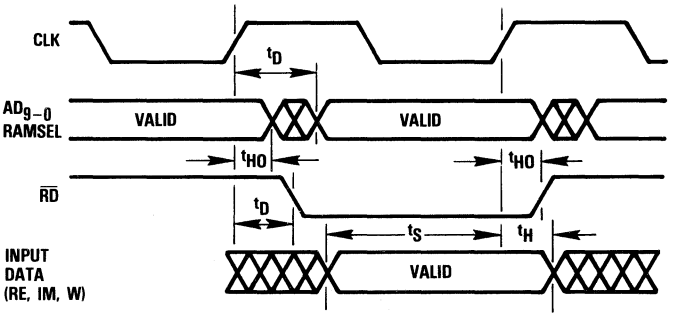


Figure 5. Write Cycle Timing

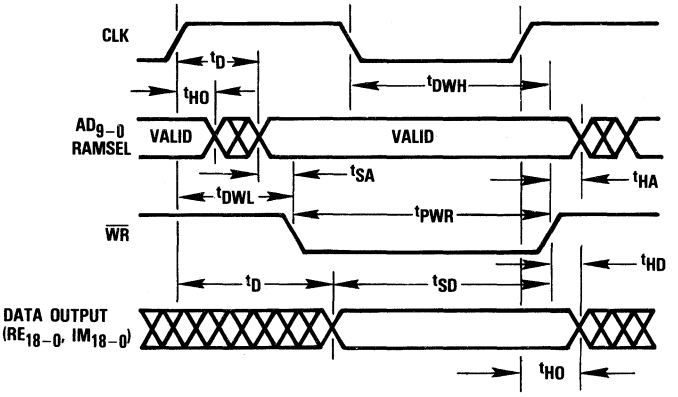
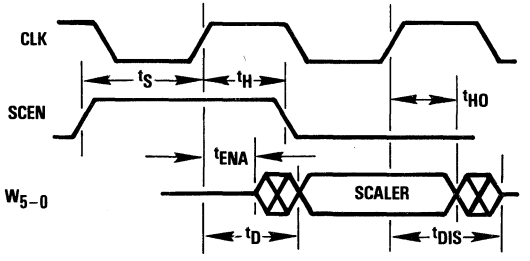


Figure 6. Scaler Timing



Transforms

Figure 7. RESET Timing

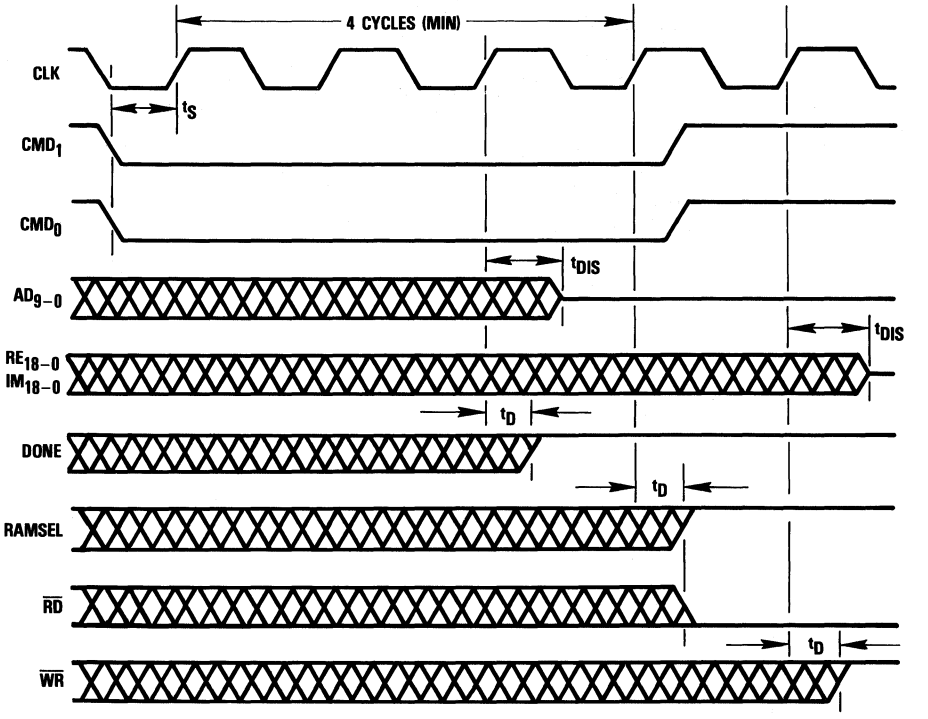


Figure 8. Configuration Register Load Timing

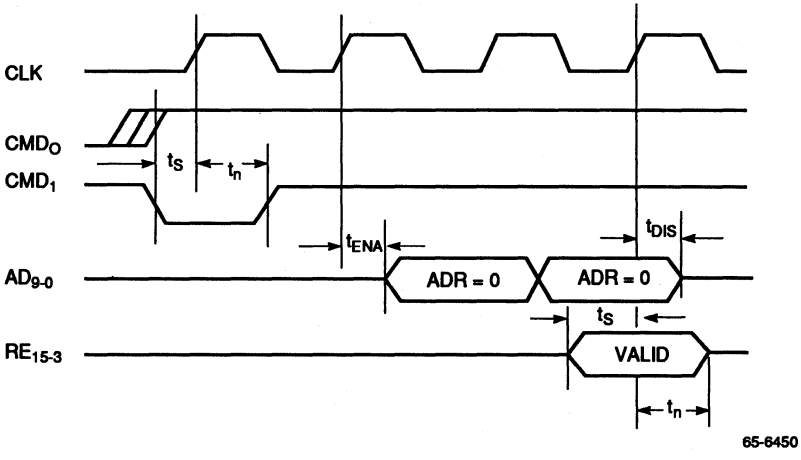


Figure 9. START Timing (Shown for FFT/IFFT with Windowing)

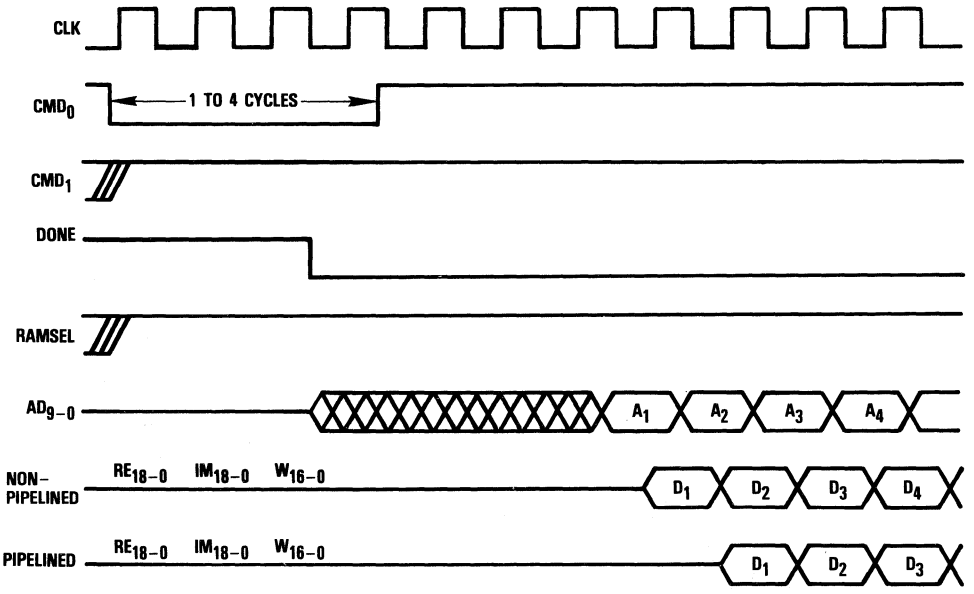


Figure 10. DONE Timing (Shown for FFT/IFFT)

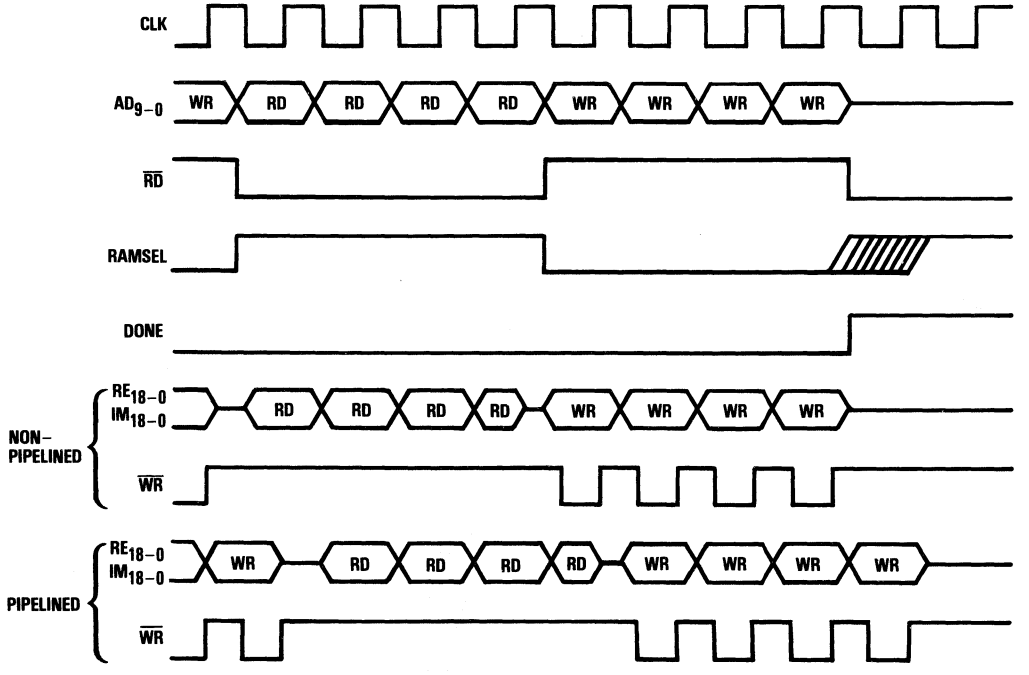
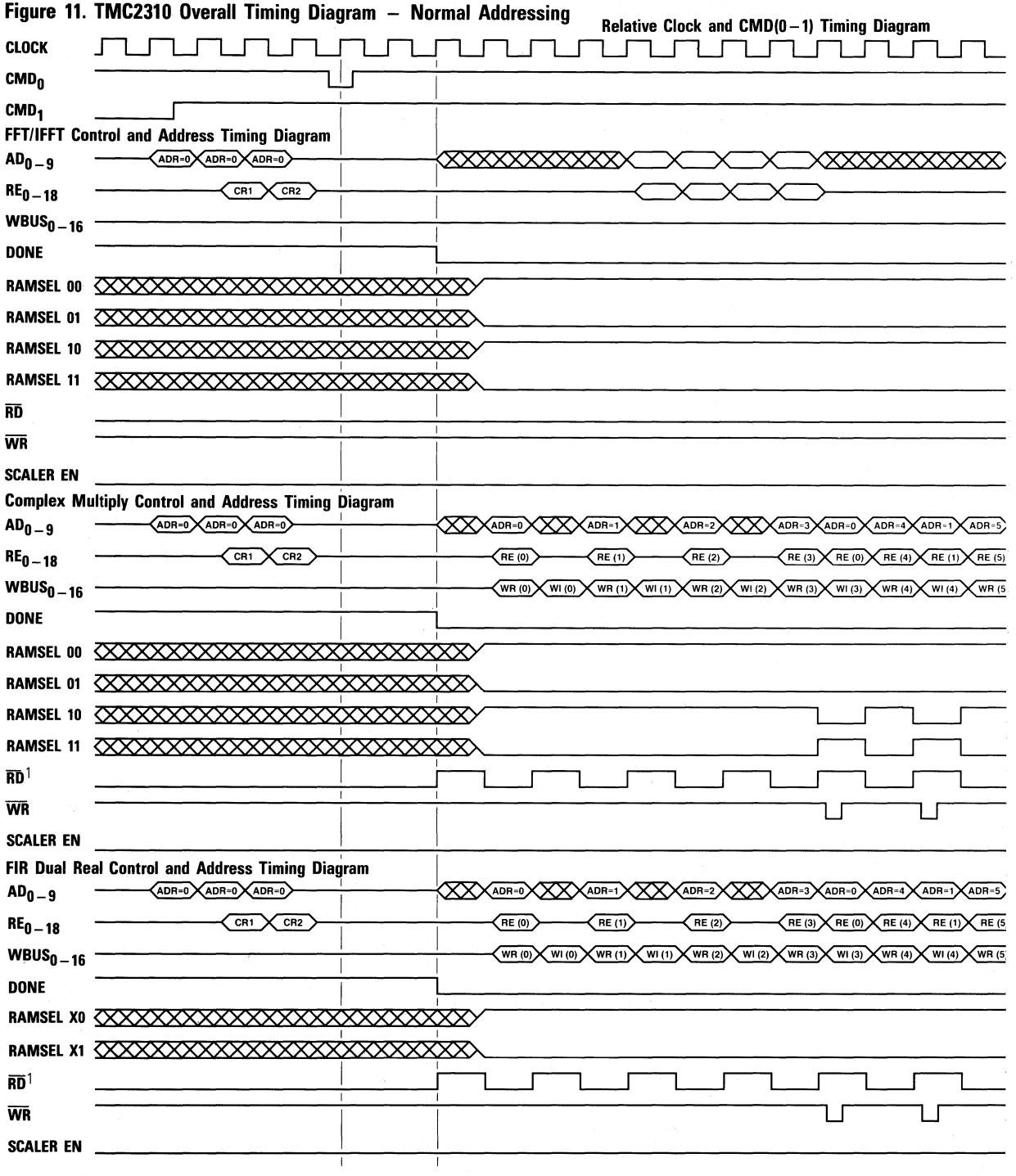


Figure 11. TMC2310 Overall Timing Diagram – Normal Addressing



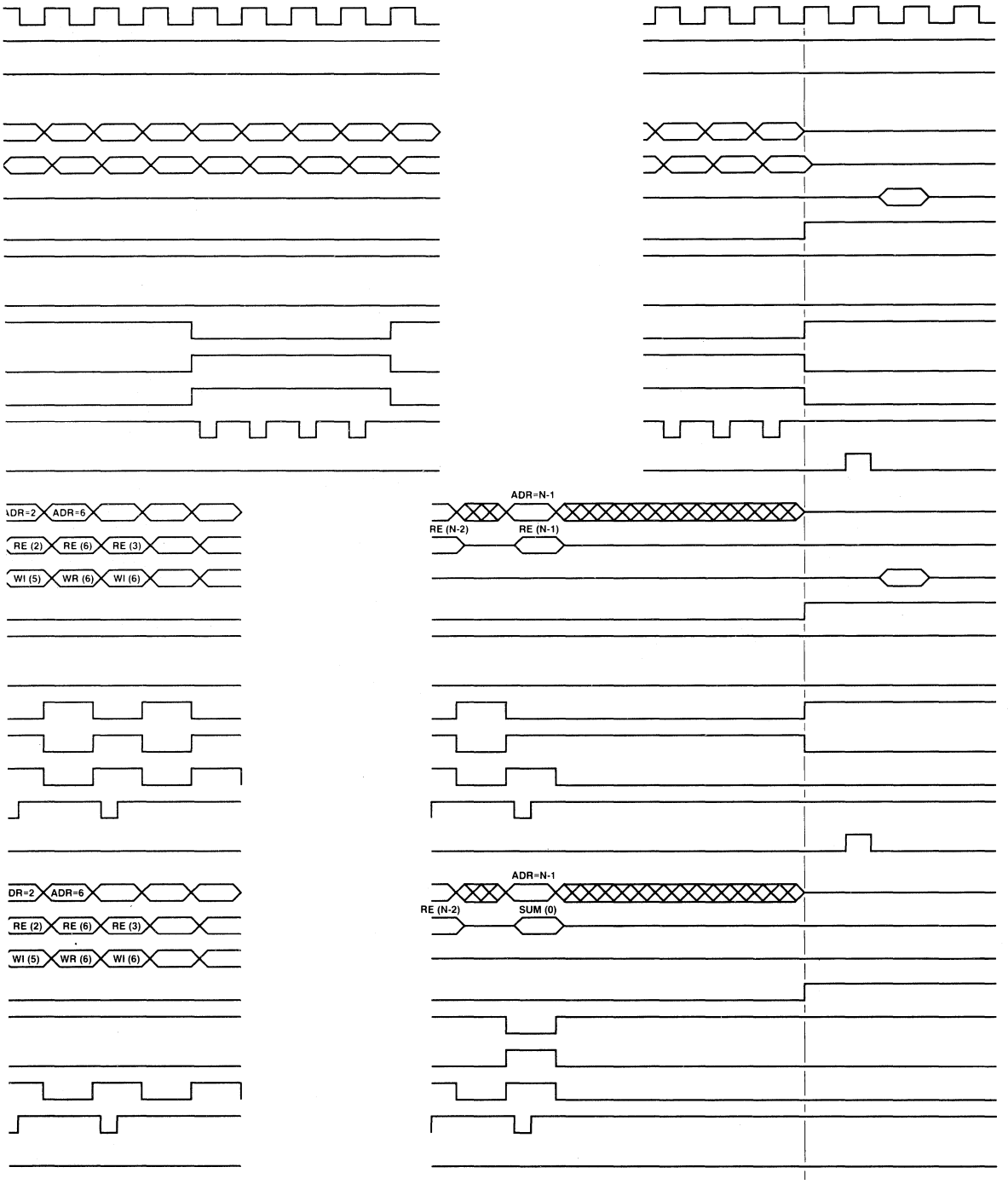
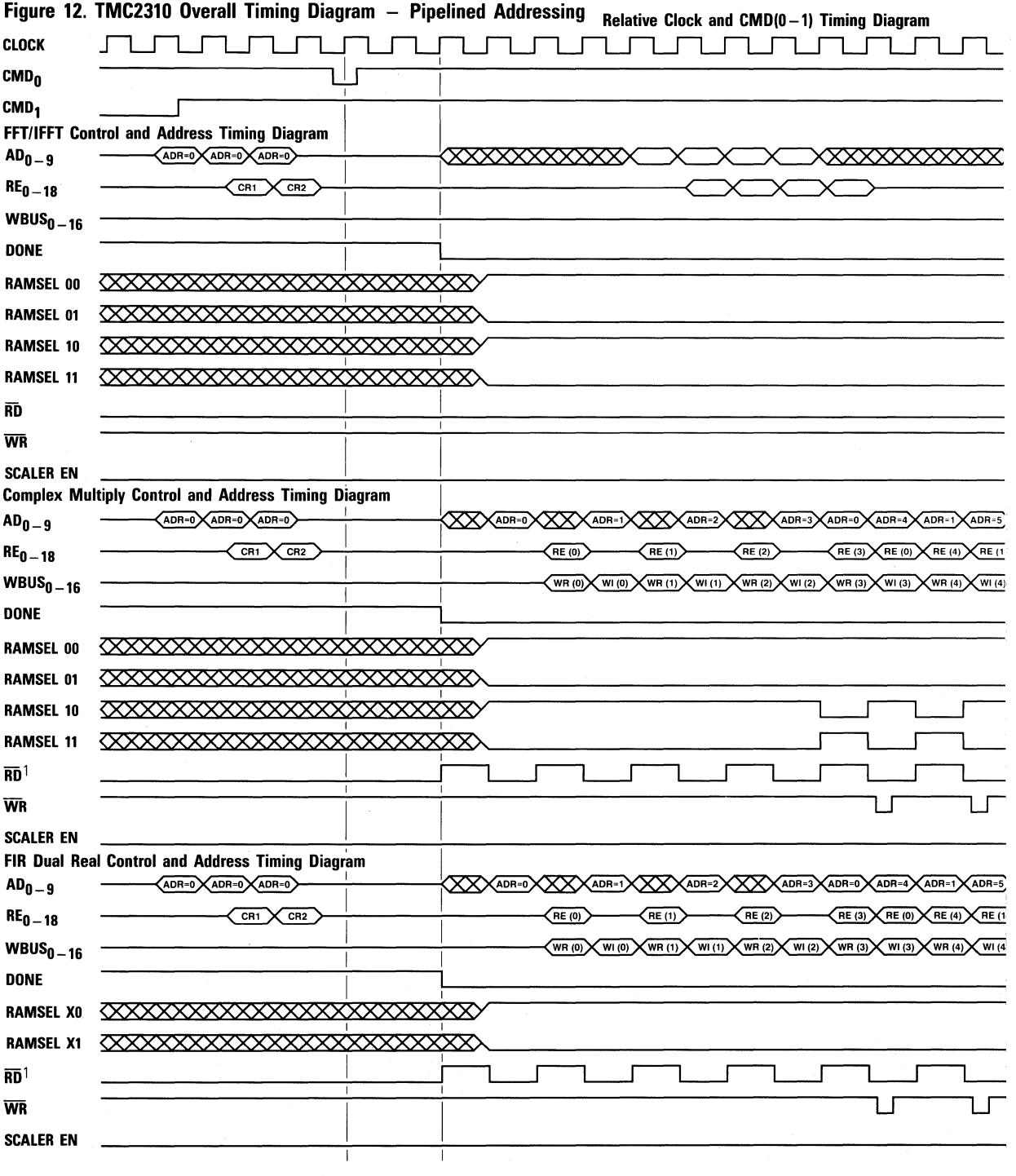

ADR=N-1
RE (N-2)
RE (N-1)
ADR=N-1
RE (N-2)
SUM (0)

Figure 12. TMC2310 Overall Timing Diagram – Pipelined Addressing



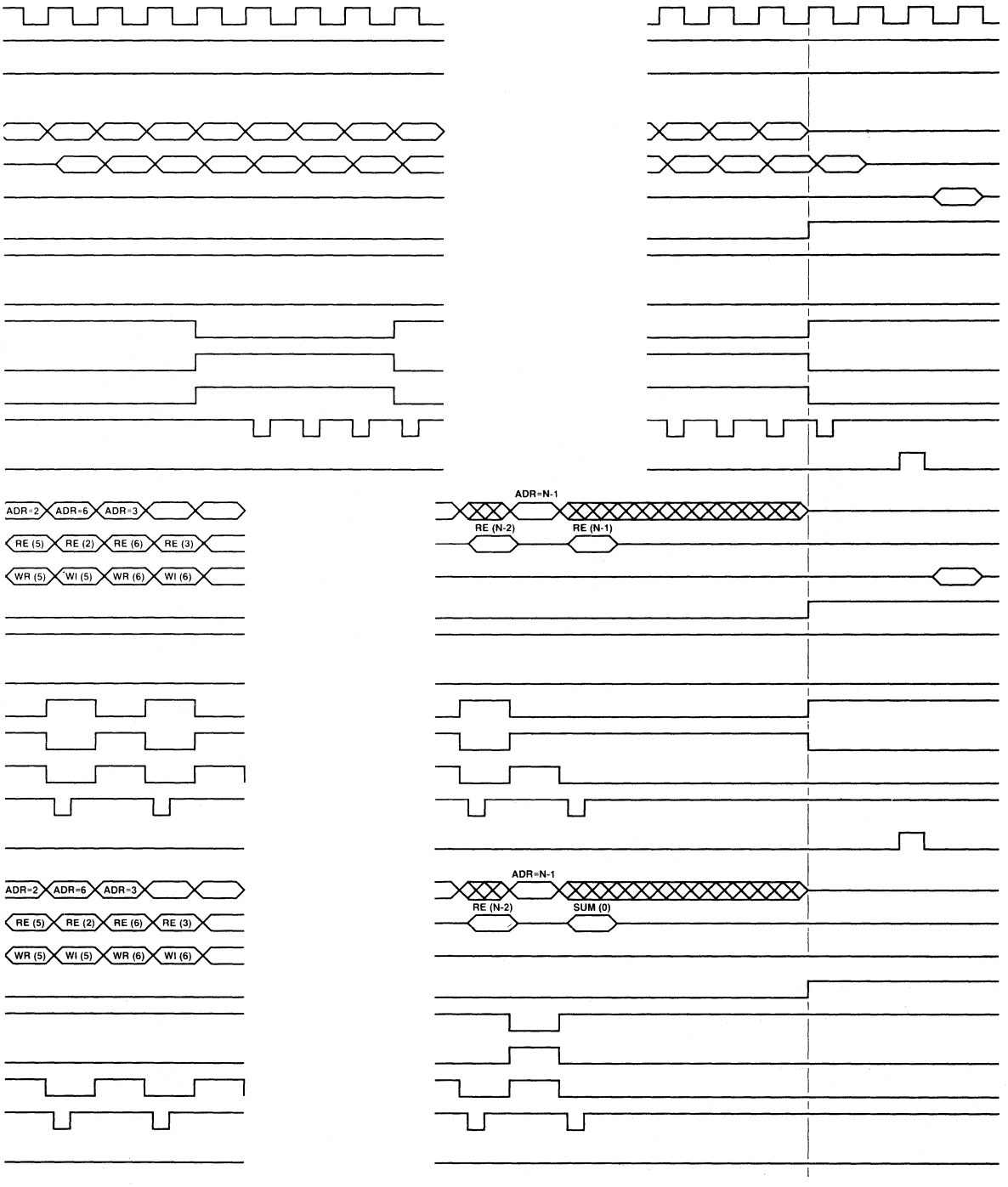

ADR=2
ADR=6
ADR=3
RE (5)
RE (2)
RE (6)
RE (3)
WR (5)
WI (5)
WR (6)
WI (6)
ADR=N-1
RE (N-2)
RE (N-1)
ADR=2
ADR=6
ADR=3
RE (5)
RE (2)
RE (6)
RE (3)
WR (5)
WI (5)
WR (6)
WI (6)
ADR=N-1
RE (N-2)
SUM (0)

Figure 13. Equivalent Input Circuit

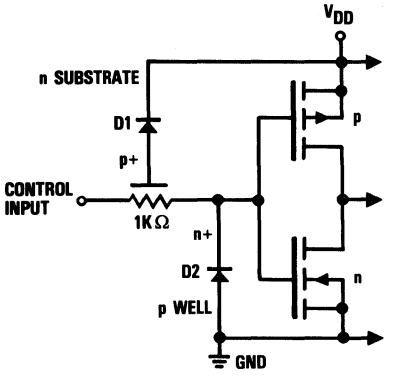
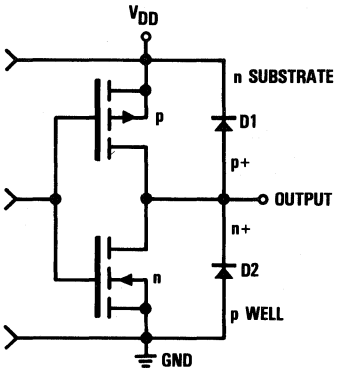


Figure 14. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−3.0 to 6.0mA
Short−circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	+175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended −1 Min	Extended −1 Nom	Extended −1 Max	Extended Min	Extended Nom	Extended Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25				4.5	5.0	5.5	V
t_{CY}	Clock Cycle Time	50			50			66			ns
t_{PWH}	Clock Pulse Width HIGH	25			25			30			ns
t_{PWL}	Clock Pulse Width LOW	20			20			25			ns
t_S	Input Setup Time	7			9			11			ns
t_H	Input Hold Time	1			2			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8						0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0						2.0			V
V_{IHC}	Input Voltage, Clock HIGH	2.2						2.3			V
I_{OL}	Output Current, Logic LOW			4.0						4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0						−2.0	mA
T_A	Ambient Temperature, Still Air	0		70							°C
T_C	Case Temperature							−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V, DONE=HIGH		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=20MHz		150		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=−2mA	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V		−20		−20	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		20		20	μA
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.		−180		−180	mA
I_{OSW}	Short-Circuit Output Current for WR	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.		−180		−180	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Transforms

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended –1 Min	Extended –1 Max	Extended Min	Extended Max	Units
t_D	Delay Clock to Output	V_{DD} = Min, Load = 25pF							
		RE_{18-0}, IM_{18-0}		19		20		25	ns
		AD_{9-0}, RAMSEL		18		18		20	ns
		$\overline{RD}$, DONE		15		16		18	ns
		Scaler (W_{5-0})		32		38		40	ns
t_{HO}	Output Hold Time	V_{DD} = Min, Load = 25pF							
		RE_{18-0}, IM_{18-0}	4				2		ns
		AD_{9-0}, RAMSEL	4				2		ns
		$\overline{RD}$, DONE	2				2		ns
		Scaler (W_{5-0})	5				5		ns
t_{SA}	Setup Time AD_{9-0} to $\overline{WR}$ LOW	V_{DD} = Min, Load = 25pF	0				0		ns
t_{HA}	Hold Time AD_{9-0} to $\overline{WR}$ HIGH	V_{DD} = Min, Load = 25pF	10				5		ns
t_{SD}	Setup Time Data to $\overline{WR}$ HIGH (Data Valid to end of $\overline{WR}$)	V_{DD} = Min, Load = 25pF	24				22		ns
t_{HD}	Hold Time Data to $\overline{WR}$ HIGH (Data Hold from end of $\overline{WR}$)	V_{DD} = Min, Load = 25pF	10				10		ns
t_{PWR}	$\overline{WR}$ Pulse Width LOW	V_{DD} = Min, Load = 25pF	15				14		ns
t_{DWL}	Delay, Clock HIGH to $\overline{WR}$ LOW	V_{DD} = Min, Load = 25pF	11	25			10	28	ns
t_{DWH}	Delay, Clock LOW to $\overline{WR}$ HIGH	V_{DD} = Min, Load = 25pF	7	18				22	ns
t_{ENA}	Three-State Enable Delay	V_{DD} = Min, Load = 25pF		20				21	ns
t_{DIS}	Three-State Disable Delay	V_{DD} = Min, Load = 25pF		14				16	ns

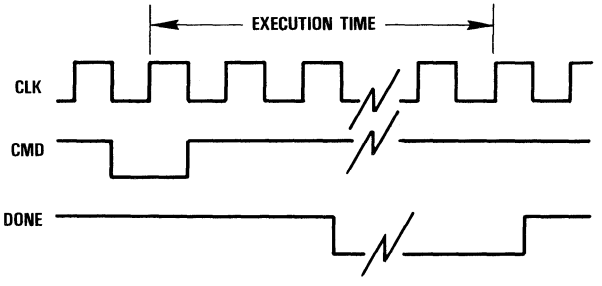
Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Table 7. Performance Benchmarks

Operation	Number of Points	Execution [1] Cycles	Execution Cycles (Multiple Transform Mode)	Execution Time (20MHz)	Execution Time (20MHz) (Multiple Transform)
FFT/IFFT	16	87	64/Transform + 23	4.35 μS	3.2 μS/Transform + 1.25 μS
(Real Window/No Window)	32	223	192/Transform + 31	11.15 μS	9.6 μS/Transform + 1.55 μS
	64	415	384/Transform + 31	20.75 μS	19.2 μS/Transform + 1.55 μS
	128	1063	1024/Transform + 39	53.15 μS	51.2 μS/Transform + 1.95 μS
	256	2087	2048/Transform + 39	104.35 μS	102.4 μS/Transform + 1.95 μS
	512	5167	5120/Transform + 47	258.35 μS	256.0 μS/Transform + 2.35 μS
	1024	10,287	N/A	514.35 μS	N/A
FFT/IFFT	16	132	96/Transform + 36	6.6 μS	4.8 μS/Transform + 1.8 μS
(w/Complex Multiply)	32	300	256/Transform + 44	15.0 μS	12.8 μS/Transform + 2.2 μS
	64	556	512/Transform + 44	27.8 μS	25.6 μS/Transform + 2.2 μS
	128	1332	1280/Transform + 52	66.6 μS	64.0 μS/Transform + 2.6 μS
FIR Filtering	–		2 Cycles/Point + 9		100ns/Point + 450ns
Multiplication					
Multiply – Accumulate					
Magnitude Squared	–		2 Cycles/Point + 15		100ns/Point + 750ns

Note: 1. Execution times are valid for all FFT addressing and scaling modes.
Execution time is defined as the number of clocks from CMD = START until DONE = HIGH (see below).
The number of clock cycles is obtained in the following manner:
Clock Cycles = (Num. of Passes) • (2 • Total Num. of Points) + (Num. of Passes) • 8 + 7
= (2 • Total Num. of Butterflies) + (Processing Overhead).

Figure 15. Execution Cycle Time



Note: 1. For multiple transforms, the total time can be obtained by multiplying the value in the table by the number of concurrent transforms.
Example: 16 transforms of length 64 – points:
From Table 7.: 384 clocks per transform + 31 cycles overhead.
Therefore, the total number of cycles is:
Total = (384/transform) • (16 transforms) + 31 = 6175 cycles.

Applications

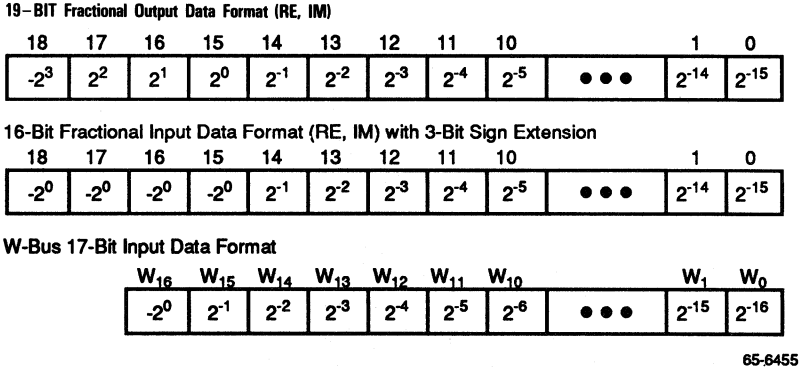
Data Formats

The input and output data formats are shown in Figure 16. Data are output on the RE and IM buses using the two's complement 19-bit data format. Input data must conform to the specified 16-bit data format detailed in Figure 16. During the first pass of any operation data input on the RE and IM buses may require scaling in order to be processed correctly by the device's arithmetic elements. Data input scaling parameters are specified according to the manual scale control set in CR1 or the input scaler select set in CR2. Only the sixteen Least Significant Bits (LSBs) or "shifted" LSBs can be used safely in the arithmetic elements. If no data shift is performed, bits RE_{15} and IM_{15} must be sign extended into the three Most Significant bits ($RE_{18\text{-}16}$, $IM_{18\text{-}16}$) to conform to the internal two's complement data buses. To perform FFTs the device supports an 18 x 17-bit multiply. However, inputs exceeding the 16-bit formats shown above may produce an intermediate overflow within the device's arithmetic elements.

The user is responsible for monitoring and accommodating data overflow for single pass instructions and for multiple pass transforms which utilize manual scaling. During multiple pass transforms, shifting can also be performed automatically (except for the first pass) by selecting the auto scale feature. If an operation may cause an overflow, sufficient memory width must be provided or data shifting performed to prevent loss of significant data. However, certain operation never cause overflow. For example, multiplication of two inputs which are both less than 1.0 will produce a result of less than 1.0. Since the MSBs of the output will always be a sign extension of the result, they can be ignored. This can simplify the memory arrangement by allowing the use of 16-bit memory systems (see Interfacing to Memory).

The W-Bus data may be reduced to 16-bit format to simplify memory interfacing. To maintain maximum accuracy, this can be accomplished in one of two ways. If using only positive window or filter coefficients, the MSB (W_{16}) may be connected to GND through a pull-down resistor (see Interfacing to 16-Bit Memory Systems). If both positive and negative coefficients are used, the LSB (W_0) can be connected to GND through a pull-down resistor.

Figure 16. Data Bus Formats



FIR Filter Operation

The TMC2310 performs both adaptive and non-adaptive coefficient Finite Inpulse Response (FIR) filters by performing a linear convolution between filter coefficients and input data. External data memory is used to store data samples and coefficients. For an N-tap filter, the data (RE, IM) memory retains the N most recent data samples and the window/coefficient memory stores the N filter coefficients.

The output of an N-tap, FIR filter is given by the convolution equation:

$$y(n-N+1) = \sum_{k=0}^{N-1} h(k)x(n-k)$$

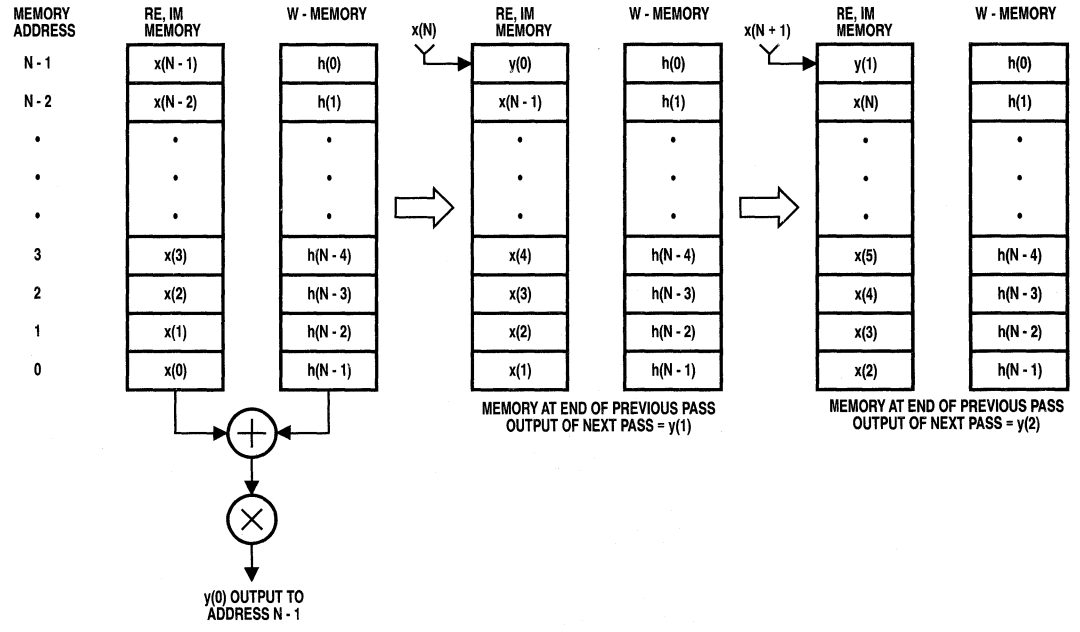
The convolution is accomplished by multiplying data in the RE and IM memories with filter coefficients stored in external RAM or ROM and input on the W-Bus. During the multiplication/accumulation, the RE and IM data are shifted down in memory by one address in preparation for the next pass.

At the start of a pass, the N-most recent data samples (x(n)) are stored in memory addresses from 0 through N−1 in ascending order (oldest sample in address 0).

The filter coefficients are stored in window/coefficient memory in corresponding addresses but in reversed order. After the START command, the coefficients and data are multiplied and accumulated term-by-term, while each value in RE and IM memory is shifted down by one memory location (with RAMSEL=HIGH). Upon completion of the pass, the RE and IM data have been shifted by one location, and the final accumulated result (y(n)) is output to address=N−1 with RAMSEL=LOW. In preparation for the next pass, the result at memory address N−1 is read by the host system. Execution stops at the end of each pass to allow time to read this result and to load the next data sample. To produce the next convolution output, this new data input is stored in location N−1, and a START command is re-issued. This operation is repeated for each output point y(n).

A diagram of the ordering of data samples and filter coefficients before and after successive passes is shown in *Figure 17*. An examination of the arrangement of coefficients (h(k)) and data samples (x(n)) shows that the FIR filter equation is calculated by summing the product of filter coefficients and data points in corresponding addresses.

Figure 17. FIR Filter Operation



FIR Filter Operation (cont.)

The filter order (tap length) is set by the "single transform length" and "number of transform" parameters in CR1 and CR2 respectively. The allowable filter sizes are 16 to 1024 taps, in multiples of 16. The throughput rate is two clock cycles per tap, per channel.

Both the 2-Real and Real/Imaginary FIR filtering are performed as described above. The "FIR 2-Real" (CR1[14:11]=1001) instruction utilizes one set of filter coefficients for both the $RE_{18\text{-}0}$ and $IM_{18\text{-}0}$ data. The FIR Real-Imaginary instruction allows the use of separate filter coefficients for RE and IM data. This allows simultaneous filtering of two independent Real data sets with different filter functions. Coefficients for each set are input on alternate clock cycles through the W-Bus with the use of the $\overline{RD}$ option available in CR2[4].

Adaptive FIR Filtering

Adaptive FIR filtering modifies the filter coefficients concurrently with the convolution. Adaptive filtering operates differently from non-adaptive FIR filtering. As indicated before, the output y(n), can be obtained by convolving input data with filter coefficients:

$$y(n) = \sum_{k=0}^{N-1} h'(k)x(n-k)$$

Adaptive filters produce an error term for each filter output:

[Actual Filter Output] – [Desired Filter Output] = Error

or,

$$y(n) - y(n)' = \sigma(n)$$

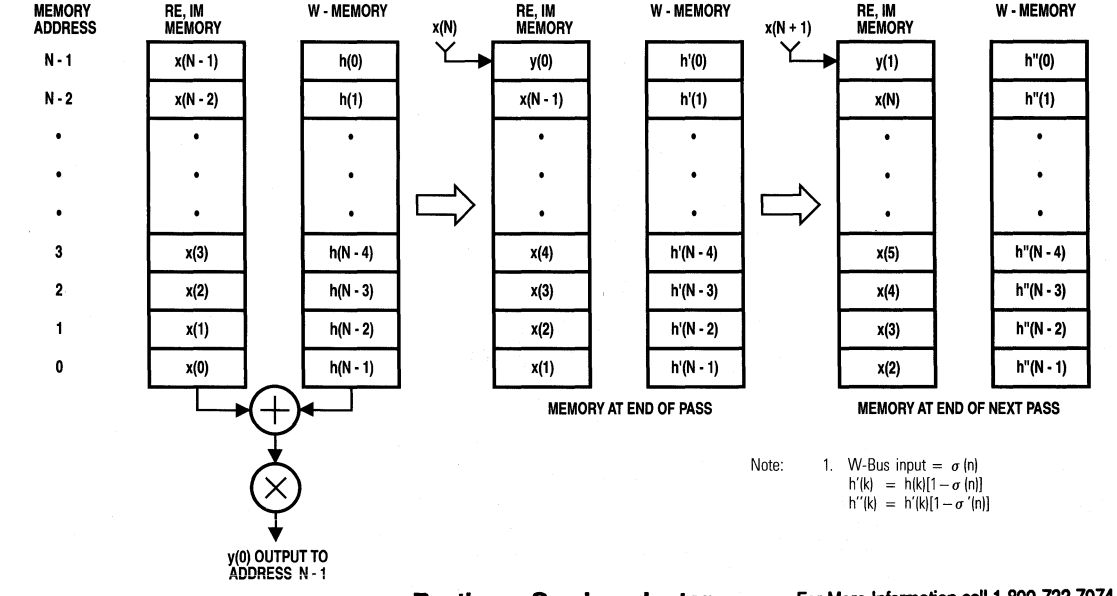
The error term is used to update the filter coefficients for the next data pass. The memory arrangement for adaptive filtering uses the RE memory for data storage and IM memory for existing and modified filter coefficients. During the pass, the data (x(n)) are shifted down one address in memory while the product of data and coefficients is being accumulated (with RAMSEL=HIGH). Concurrent with the determination of the convolution sum and the data shifting in the RE data memory, the filter coefficients are modified by the function:

$$h'(n) = [1 - \sigma(n)]h(n)$$

Where the h' are the filter coefficients used for the next pass.

The update value σ is input on the W-Bus on every read cycle and the modified filter coefficients are stored in IM memory. The operation is shown in ***Figure 18***.

Figure 18. Adaptive Filtering



Note: 1. W-Bus input = $\sigma(n)$
$h'(k) = h(k)[1-\sigma(n)]$
$h''(k) = h'(k)[1-\sigma'(n)]$

Interfacing to Memory

Using the TMC2310 with Lower Resolution Data

The TMC2310 allows data inputs of up to 16 bits for all operations without the risk of an internal overflow. When using data values that are smaller than 16 bits it is recommended that they be placed in the upper MSBs of the RE and IM data ports. For instance, when using 12-bit initial inputs for an FFT operation the real and imaginary data should be placed on both RE_{18-7} and IM_{18-7}, respectively. Using the upper MSBs of each 19-bit data port allows the device to operate in either the AUTO or MANUAL scale mode. Configuration Register 1, CR1[4:3], must be set to perform a right shift of 3 bits on the data input during the first pass. Results from the first pass have the potential of growing up to 19 bits, therefore, to maintain maximum precision the outputs should be contained in 19-bit wide memory.

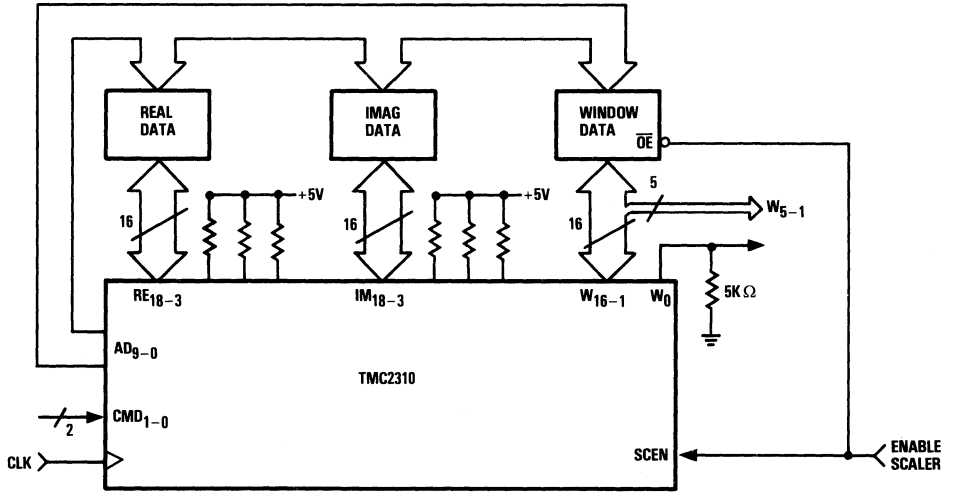
Initial data inputs can be connected to the 12 LSBs, however, since the device uses a two's complement data format each input must be sign extended into RE_{18} and IM_{18}, the MSBs. For operations that require multiple passes (i.e., FFT/IFFT) intermediate results will carry less precision. This will result in a reduction in the overall accuracy of the transform operation.

Interfacing to 16-Bit Memory Systems

The TMC2310 outputs 19 bits of significant data to external memory in order to increase arithmetic precision and minimize roundoff error. To obtain the best results, the memory system should support all 19 data bits. In order to reduce the number of memory devices, the system can be configured with 16-bit wide data memories. While this configuration may reduce system size and cost, there will be a decrease in accuracy due to truncation of the output data. In a 16-bit memory system, data should be left-justified (connected to the 16 MSBs) with the 3 LSBs connected to pull-up (or pull-down) resistors. Configuration Register 1 is programmed to perform auto or manual data scaling with a right shift of 3 bits performed on the data during the first pass (CR[4:3]=11). The 16 MSBs of the output are stored into memory, truncating the three LSBs.

In systems utilizing data windowing, the user may connect either the LSB or the MSB of the W-Bus to ground through a pull-down resistor of 5 kOhms. If both positive and negative window values are to be used, the MSB is required (two's complement format) and the LSB may be grounded. For positive magnitude window functions, the MSB will always be zero, and can therefore be connected to ground through a 5 kOhm resistor.

Figure 19. Interfacing to 16-Bit Memories



Pipelined vs. Non-Pipelined Addressing

Operation of the TMC2310 at its maximum clock rate requires the use of high-speed data memory. By including a special addressing mode, slower memory can be used by the addition of high-speed external address registers. The TMC2310 has been designed to allow the user to make system tradeoffs between memory cost and device count.

Normally, a memory address is output and the data strobed into or out of memory within a single clock cycle. Therefore, the following relationship must be met:

$$t_{CY} \quad [t_{DO}(\text{TMC2310 Addr. Out}) + t_{ACC}(\text{memory}) + t_S(\text{TMC2310 Data In})]$$

or equivalently, the memory access time must meet the requirement:

$$t_{ACC}(\text{memory}) \quad [t_{CY} - t_D(\text{TMC2310}) - t_S(\text{TMC2310})]$$

Use of the "Pipelined Addressing" mode alters the above relationship. In pipelined mode, the address and controls ($\overline{RD}$ and RAMSEL) appear one cycle earlier. For a read operation, the data will be input to the TMC2310 on the following cycle. For a write operation, the output data and the $\overline{WR}$ strobe will occur one cycle after the address and controls. For proper synchronization, the address, $\overline{RD}$ and RAMSEL outputs must be externally registered. The requirement for external memory speed becomes:

$$t_{ACC}(\text{memory}) \quad [t_{CY} - t_D(\text{external register}) - t_S(\text{TMC2310})]$$

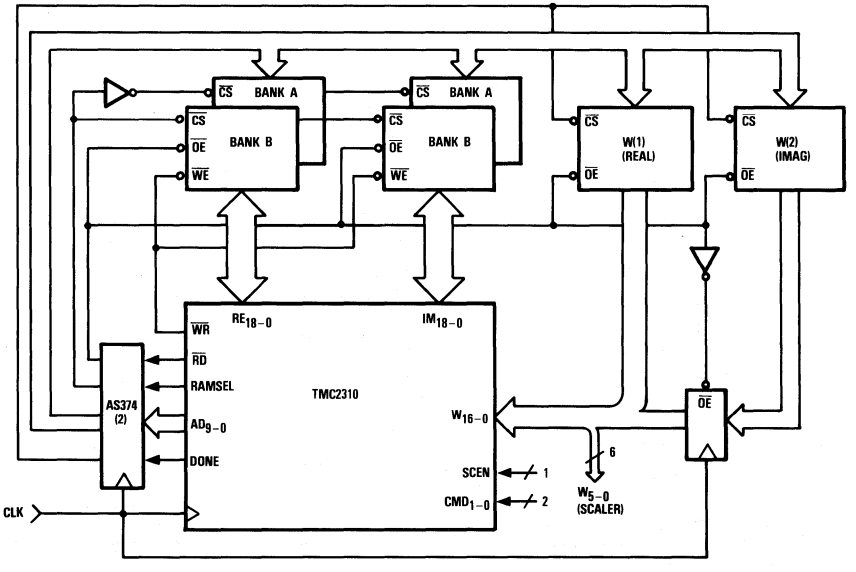
By substitution of the appropriate parameters into the above equation, it can be seen that the use of an external high-speed register ('AS374, F374, etc.) results in a substantial reduction of memory speed (access time) requirements.

Typical System Configuration

Figure 20 shows a typical system configuration utilizing many of the described techniques. The system includes "pipelined addressing", evident by the use of external registers on the TMC2310 memory address and controls. The system also includes a banked (Bank A and Bank B) memory system, which may consists of single port or multi-port memory. (External host interface to memories is not shown.)

Finally, the diagram shows a system utilizing two window memories (for dual real and complex operations). If only one window memory is required (Real Windows) then the Imaginary memory, W(2), and associated output register and inverter may be deleted. For a single window memory, the chip select of W(1) can be connected to a LOW and the output enable connected to the DONE flag to disable the memory when the device is idle.

Figure 20. Typical System Configuration



Applications Information

System Memory Options

Single-port memories for both real and imaginary data can be used with the TMC2310. If single port memories are used, system performance will depend not only on the time required to perform the operation but also the time required to load and unload the memory. Systems requiring continuous operation are better supported with dual-port memories. This approach allows data to be loaded into, for example, the upper 1K portion of a 2K deep memory while the TMC2310 is operating on data in the lower 1K addresses. This technique eliminates the need for arbitration logic available in some dual-port memory. It is recommended that the device be used in the Pipelined Addressing mode to eliminate bus contention between the TMC2310 and the local real and imaginary data memory.

Memory Interface

When determining system memory requirements, the user must also take into account the Bit Reversion necessary to perform the FFT. Either the data must be stored in bit-reversed memory locations prior to performing the FFT, or the TMC2310 must perform the bit-reversal of the addresses when accessing the real and imaginary data on the first pass of the FFT. If data are loaded into memory in bit-reversed locations, the system can be operated using only 1 bank of memory. By supporting an additional bank of real and imaginary memory, the user has the option of allowing the bit reversal of the addresses to be performed by the TMC2310. This is a more efficient approach since it allows the host to load the inputs into one bank and unload the results from the other bank. Enabling and disabling of the memory banks is controlled by the RAMSEL flag provided by the TMC2310.

The operation of the RAMSEL flag is determined in conjunction with the bit reverse option. The user can determine the bank where the final results will be written with the Source/Target Memory Select option in Configuration Register 2. If bit-reversal is performed by the TMC2310, the RAMSEL flag will toggle in such a way as to move the intermediate and/or final results into the second bank of the memory. If the data are loaded into bit-reversed locations of the memory initially, then the RAMSEL flag can be used as a signal to indicate when the final results are being written. CR1[7:6]=10, CR2[6:5]=1X. (In this configuration the results will be written to bit-reversed locations).

Rescaling

After the memory configuration scheme has been defined the user can now tackle the issue of memory resolution. Although the device achieves maximum Signal-to-Noise performance using 19-bit wide memories excellent performance can still be attained using narrower memory. A common application is to use 16-bit memories interfaced to the upper 16 MSBs of each 19-bit data port. Independent of the memory width, rescaling of the data during the computation is necessary to prevent overflow. Signal-to-noise is maximized when the **auto scale** feature is activated, however, the user must then extract the scaler information from the W-Bus so that the proper order of magnitude of the data can be determined. Per definition of the FFT, a shift (or rescale) of 2 bits performed following every second radix-2 butterfly is sufficient to maintain accuracy without the threat of overflow. The TMC2310 supports this mode of operation with the **manual scale** option. For example, when using 12-bit inputs the initial data should be loaded into the memory with MSB at RE_{17}/IM_{17}. RE_{18} and IM_{18} are just sign extensions of RE_{17} and IM_{17}, while $RE_{4\text{-}0}$ and $IM_{4\text{-}0}$ should be set to zero. The initial shift performed at the beginning of the first pass will then have no effect on the data. Subsequent passes will each be rescaled by 2 bits following the butterfly operations. Use the following settings: **CR1[5]=1, CR1[4:3]=10**.

Using the TMC2310 with 17-bit Inputs

For non-FFT applications the device can support 17-bit wide inputs while returning valid results. For convolution operation (i.e., MPY-ACC and FIR modes) the user must be careful not to exceed the accumulator width of the device. Input data can be placed into $RE_{16\text{-}0}$ and $IM_{16\text{-}0}$ of the two data ports. $RE_{18\text{-}17}$ are sign extensions of RE_{16} and $IM_{16\text{-}0}$ of the two data ports. $RE_{18\text{-}17}$ and $IM_{18\text{-}17}$ are sign extensions of RE_{16} and IM_{16} of the initial inputs. The data in the real and imaginary memory can also be interfaced to allow an initial shift of the inputs within the device prior to performing the desired operation. If the real and imaginary data are stored with the MSBs at RE_{17} and IM_{17}, sign extension will be supported internally in the device following the 2-bit shift, **CR1[4:3]=10**.

Generating a Write Pulse

The high-speed operation of the TMC2310 requires the use of fast random access memory. The TMC2310 provides a write enable pin for use with the local real and imaginary data memories. In some circumstances, it is necessary for the user to generate this write strobe to increase the pulse width to meet system requirements. As an alternative, the user can use the RD/ output to generate this write strobe since the RD/ signal is normally LOW and goes HIGH only during write cycles. The RD/Signal should be gated with the system clock to create an active LOW write (enable) strobe. If the device is to be used to implement Unwindowed or Real Windowed FFTs exclusively, then this method should achieve better system timing and performance.

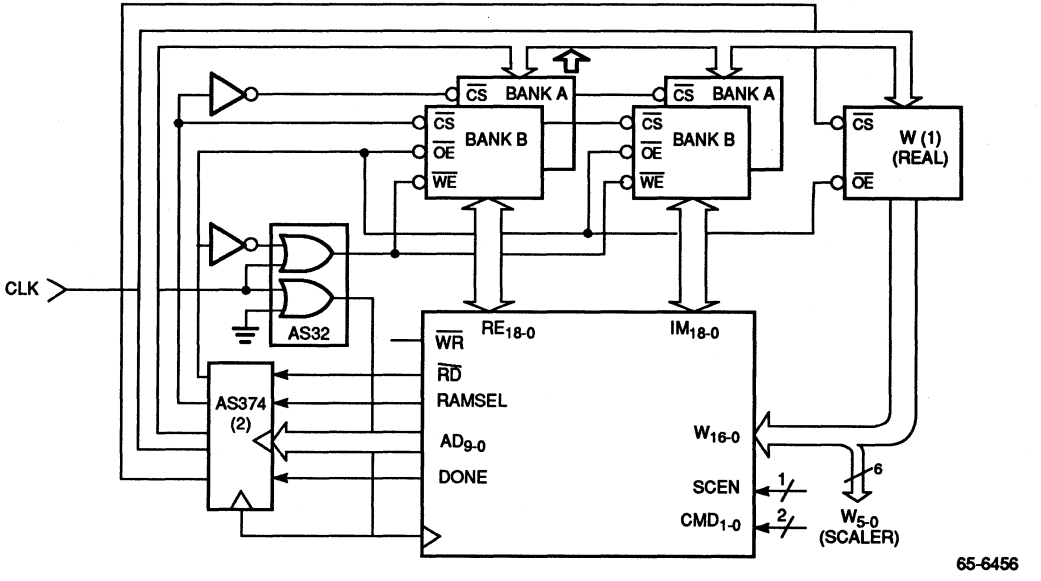


Figure 1. Memory Interface for FFT Systems

Generating a Write Pulse (continued)

More general applications, particularly those that require (2) window coefficient memories (i.e., Complex MPY, RE/IM MPY-ACC etc.), require an alternative circuit for Write strobe generation. The TMC2310 contains an option in CR2 that changes the operation of the RD/ signal. Under normal operations **CR2[4]=0** the RD/ signal will not be activated until the first valid result appears at the real and imaginary data ports, after which RD/ will toggle on successive cycles. If activated, the RD/ signal will toggle following application of the START command so that W_R and W_I inputs can be synchronized with the falling and rising edge of the RD/, respectively. If it is necessary for the write strobe to be generated for these modes (including FFT/IFFT with Complex MPY) then an alternate circuit must be used. Specifically, if CR2[4]=1 RD/ will toggle every cycle and if the write strobe is created by gating RD/ with CLK then the device will incorrectly generate (4) write pulses during the first four read cycles writing over unprocessed data. The following circuit eliminates this situation by setting **CR2[4]=0**:

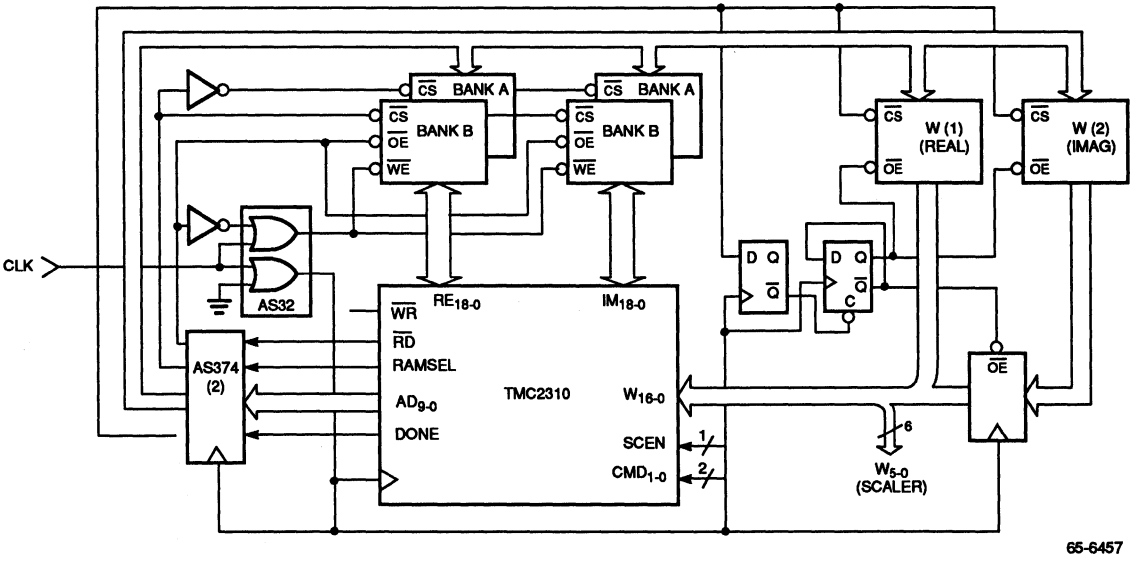


Figure 2. Memory Interface for General Systems

Bit-Reverse Addressing Details

The radix−2, Decimation−In−Time (DIT) FFT/IFFT algorithm performed by the TMC2310 requires data scrambling during the first butterfly pass (Refs. [2],[3]). The scrambling amounts to a bitwise reversal of the address index during the first pass of the FFT. A flow diagram for a general, radix−2, 16−point FFT is shown in Figure 21. By a close examination of the figure, it can be seen that the first butterfly is performed on data points X(0) and X(8) with results stored in X(0) and X(1). It is apparent that results must be written to a secondary memory to prevent the loss of the unused data point X(1).

The TMC2310 allows several addressing options for transforms. While these modes have no effect on speed or processing time, they do affect system memory requirements. If the input data samples are stored in memory in sequential order, then the TMC2310 must perform the bit−reversed addressing (CR1[7:6]=01) during the first butterfly pass. To accomodate the data scrambling and prevent overwriting of unused data, the user must provide additional "scratch pad" memory for intermediate storage during this pass. The RAMSEL output is used to toggle between the two banks during reads and writes of the first pass. RAMSEL must be connected either to the "chip enables" of separate memories or to an additional address line (for a paged memory system). At the completion of the transform, data will be in memory in sequential (frequency or time) order.

A transform can be done without the scratch pad memory by initially storing the data in scrambled order. This is accomplished by a simple reverse ordering of the address lines between the host system address generator (counters, etc.) and the data memory (Figure 22). The transform is then performed "in−place" (no bit−reverse, CR1[7:6]=00). Since the input data has been "pre−scrambled", the TMC2310 will read and write data to memory addresses in a sequence that requires no additional memory. Final results will be available in sequential, frequency bin order. In either case, if windowing is performed, the user must store the window function either in sequential or scrambled order to match that of the input data.

Figure 21. 16−Point FFT

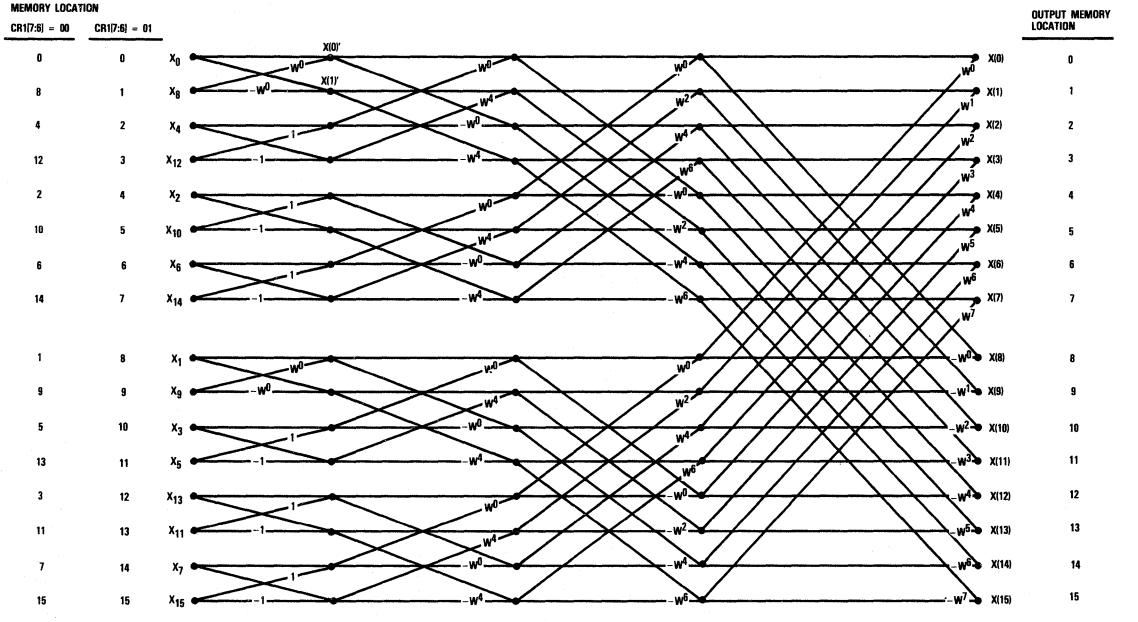
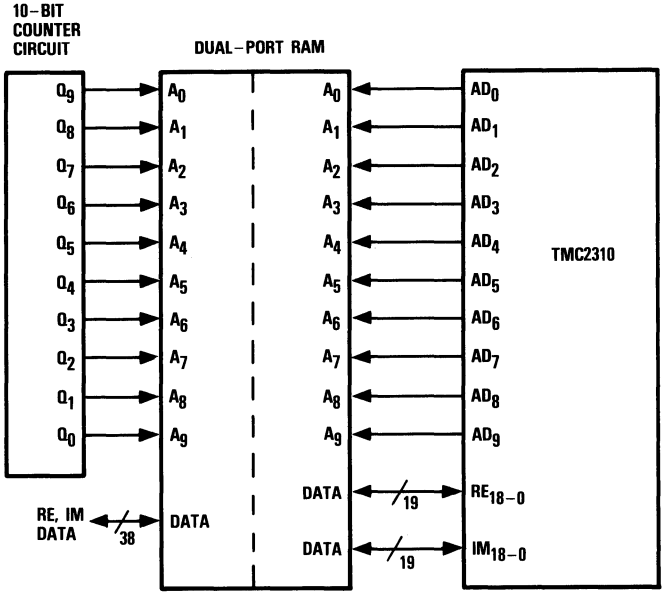


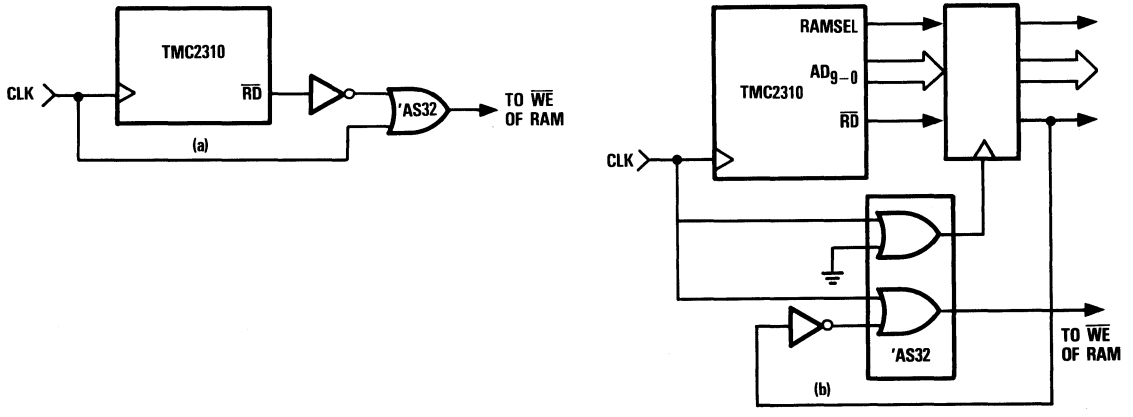
Figure 22. Bit-Reversed Input Data for 1024-Point Transform



Alternate Method For Write Strobe Generation

The high-speed operation of the TMC2310 requires the use of fast random addess memory. In some instances, the pulse-width and timing of the TMC2310's $\overline{WR}$ may not meet the system requirements. As an alternative, the user can use the $\overline{RD}$ output used to generate a write strobe for memory. Since $\overline{RD}$ is normally LOW and goes HIGH only during write cycles, the user can gate $\overline{RD}$ with the system clock to create an active LOW write (enable) strobe. Implementing the write strobe in this method may give better system timing and performance. The strobe will be the LOW portion of the system clock. *Figure 23, part (a)* shows external generation of a write strobe in non-pipelined addressing systems, and *part (b)* for pipelined systems utilizing the external address registers. The external register (74AS821) is clocked by a delayed system clock (through the AS32) to guarantee a valid memory address until WE goes HIGH.

Figure 23. Generating a Write Strobe



Scale Factor (W_{3-0})

In the inverse FFT, the final exponent read at this port will be the true binary exponent for the emerging real and imaginary data. In the forward FFT, this value will exceed the true exponent by N, where the total number of transform points is 2^N. The format for this exponent is 4-bit unsigned integer.

References

[1] Harris, F.J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Proceedings of the IEEE, Vol. 66, No. 1, January, 1978, pp 51-83.

[2] Oppenheim, A.V., Schafer, R.W., "Digital Signal Processing," Prentice-Hall, Inc., 1975.

[3] Rabiner, L.R., Gold, B., "Theory and Applications of Digital Signal Processing," Prentice-Hall, Inc., Copyright-Bell Laboratories.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2310G5V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	88 Pin Ceramic Pin Grid Array	2310G5V
TMC2310G5V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	88 Pin Ceramic Pin Grid Array	2310G5V1
TMC2310H7C	STD–T_A = 0°C to 70°C	Commercial, 20MHz	89 Pin Plastic Pin Grid Array	2310H7C
TMC2310L4V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	100 Leaded Ceramic Chip Carrier	2310L4V
TMC2310L4V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	100 Leaded Ceramic Chip Carrier	2310L4V1
TMC2310L6V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	132 Leaded CERQUAD	2310L6V
TMC2310L6V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	132 Leaded CERQUAD	2310L6V1

40G05263 Rev E 8/93

TMC2311
CMOS Fast Cosine Transform Processor
12 Bits, 15 Million Pixels Per Second

Description

The TMC2311, a high-speed algorithm specific processor, computes the one or two dimensional forward discrete cosine transform (DCT) of an 8 or 8x8 point array of contiguous 9-bit data or the inverse DCT of 12-bit data. Output precision in all cases in 12 bits. It complies with the CCITT Specialists' Group on Visual Telephony (SG XV) accuracy specification for inverse DCT. With its internal coefficient TOM, data transpose RAM, address generators, and sequencer, the TMC2311 accepts high level instructions from a host processor and raw 8x8 blocked data from an external memory and returns transformed data to a second external memory. The TMC2311 also includes a defeatable adder-subtractor for linear predictive coding and differential pulse code modulation. The pipelined TMC2311 can transform continuous 8x8 pixel data blocks at a rate of one per 4.48 µs.

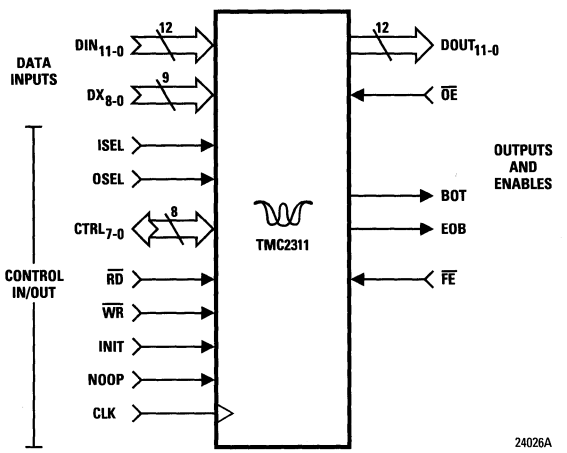
Operating under a system clock of up to 30 MHz, the TMC2311 accepts each incoming data block in row-major ("line-by-line") format at two clock cycles per pixel. Output data are written in column-major format, i.e., down the left-most column of the block, then down the next column to the right, etc., also at two clock cycles per pixel. In the inverse DCT mode, the chip accepts column-major data and returns row-major data. Thus, a pair of TMC2311 chips can transform an image and return it to its original spatial domain, with or without any intervening operation, such as compression, transmission and re-expansion.

Built with a one-micron double level metal OMICRON-C™ low-power CMOS process, the TMC2311 is available in a 68-lead plastic chip carrier.

Features

- Stand alone execution of 8-point forward or inverse cosine transform
- Continuous 8x8-point 2-D DCTs every 4.48 µs including memory transpose and data loading/ unloading
- On-chip cosine coefficient ROM
- On-chip data transpose memory with direct transpose mode
- Auxiliary adder with optional clipped outputs for linear predictive coding and differential pulse code modulation
- Two's complement 12-bit data I/O format
- Two's complement 9-bit add/subtract input
- Full CCITT SGXV compatibility
- All inputs and outputs TTL compatible
- 68 pin Plastic Chip Carrier

Logic Symbol



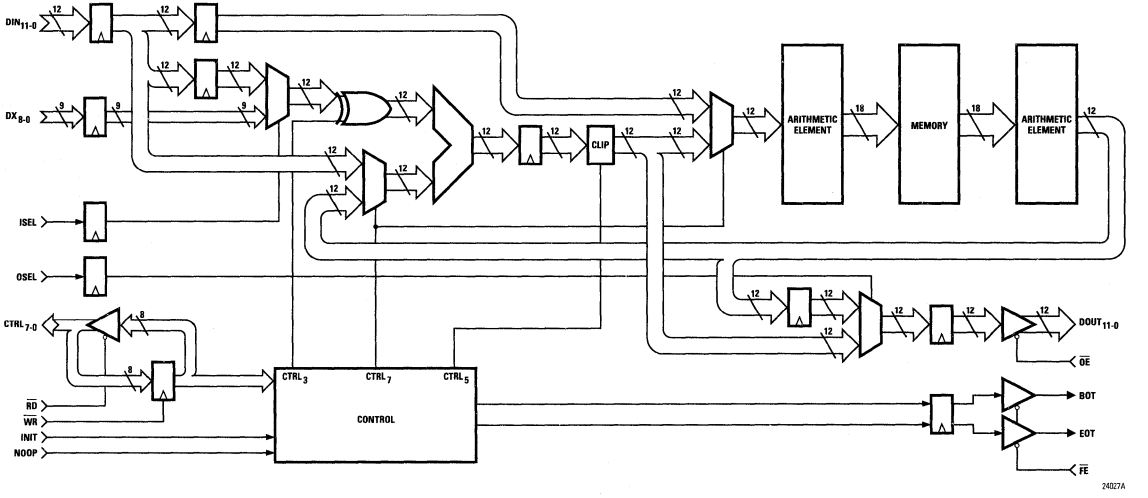
Applications

- Image Processing, Graphics
- Pulse And Image Compression
- Video Teleconferencing
- Linear Predictive Coding
- Differential Pulse Code Modulation
- Electronic Publishing
- Medical Imaging And Archiving

Associated Products

- TMC2220 — 4x32 Correlator
- TMC2250 — 2-D 3x3 FIR Filter
- TMC2272 — Colorspace Converter

Figure 1. Functional Block Diagram



Functional Description

The TMC2311 comprises five internal blocks: a controller, two arithmetic elements, a data transpose memory and an auxiliary adder circuit (*Figure 1*). Each arithmetic element (AE) can compute an 8-point 1-dimensional DCT in 16 clock cycles. When the device is configured to perform 2-dimensional transforms, the first AE computes the DCT of each consecutive row of 8 pixels. The results of each 8x1 DCT are written into the intermediate memory. After eight 1-dimensional transforms are computed, the device computes the DCT of each consecutive 8-pixel column, while (if so instructed) computing the DCTs of the rows of the next block of data. The auxiliary adder/subtractor can be used with a forward and inverse transform in linear predictive coding applications. The adder can also be used alone to perform differential pulse code modulation without the cosine transform. In all modes and configurations the device operates on continuous data at a rate of up to 15 Megapels/second and can perform a complete 8x8 DCT every 128 clock cycles.

Control

The control block includes the chip's preprogrammed controller, sequencer, and microcode generator. The host system needs only to load a single 8-bit control word on C_{7-0} and then strobe the INIT pin. The chip will proceed automatically through the chosen operation without further supervision.

Arithmetic Element #1

Comprising a multiplier and two adder/subtractors, bypassable processor AE1 performs a series of one-dimensional 8-point forward or inverse DCTs on the incoming data, writing its 8-point transform results into the transpose memory.

Data Transpose Memory

This two-port 64-word RAM collects each group of eight consecutive 8-point transformed data sets from AE1 and then passes them to AE2 while collecting the next group, thereby acting as a large pipeline buffer. When enabled, the DTM accepts each 64-point data block in row-major sequence and returns the same data in column-major order, effecting a "corner turn." Bypassing this block leaves the data sequence unchanged.

Arithmetic Element #2

Identical to AE1, bypassable data processor AE2 performs eight 8- point one-dimensional transforms on each 64-point block of data. Each transform pulls one data point from each of the eight transforms done by AE1, completing the 8x8 two-dimensional transform. For one-dimensional transforms, either AE can be bypassed.

Auxiliary Adder

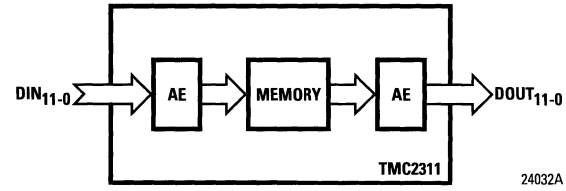
The remaining circuitry in ***Figure 1*** can be employed as either a presubtractor or a post-adder. (See ***Applications Discussions*** of ***Linear Predictive Coding, Differential Pulse Code Modulation,*** and ***Interframe Coding.***) As instructed by $CTRL_3$ (INVERT), $CTRL_7$ (XSEL), ISEL, and OSEL, this adder combines the 9-bit two's complement data entering on port DX_{8-0} with either the incoming or emerging data stream.

Operating Modes

The TMC2311's five operating modes are selected by control pins $CTRL_{2-0}$. The device can be configured in the following ways:

The device will perform a two-dimensional transform if $CTRL_{2-0}$ = 000 or 001. AE1 performs a one-dimensional DCT (IDCT if $CTRL_3$ = 1) on each of eight 8-pixel rows of data supplied row-by-row to DIN_{11-0}. Results from each block of eight transforms are fed via the Transpose Memory to AE2, which performs a one-dimensional DCT (IDCT) on each of the eight 8-pixel columns of data, in turn (***Figure 2***).

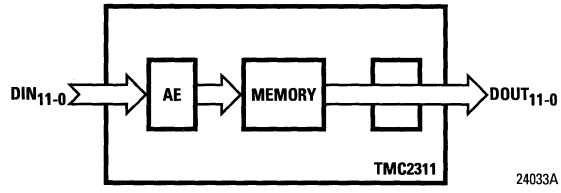
Figure 2. 2-D Transform (With Transpose)



The device can also perform one-dimensional DCTs (IDCTs) with or without memory transpose.

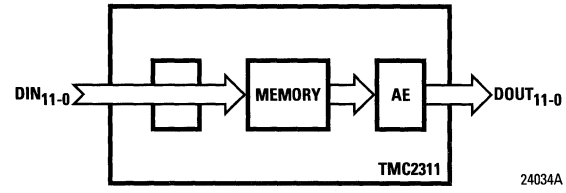
When $CTRL_{2-0}$ = 010, the chip will transform eight 8-point rows of incoming data, then transpose the results without transforming the columns (***Figure 3***).

Figure 3. 1-D Transform With 8x8 Transpose



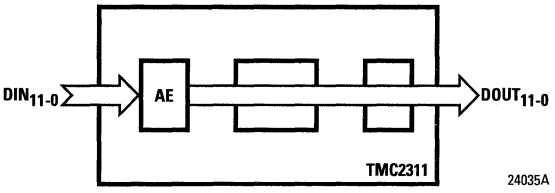
When $CTRL_{2-0}$ = 011, the device accepts eight 8-point rows of data and transposes them before AE2 performs one-dimensional DCTs (IDCTs) of the columns (***Figure 4***).

Figure 4. 8x8 Transpose With 1-D Transform



The device can also perform one-dimensional transforms without transposes. When $CTRL_{2-0}$ = 100 or 101, AE1 performs a one-dimensional DCT or IDCT on each incoming 8-point row of data (***Figure 5***).

Figure 5. 1-D Transform (Without Transpose)



Finally, the device will perform the memory transpose with no DCT when $CTRL_{2-0}$ = 110 or 111 (*Figure 6*).

Figure 6. Memory Transpose (Without Transform)

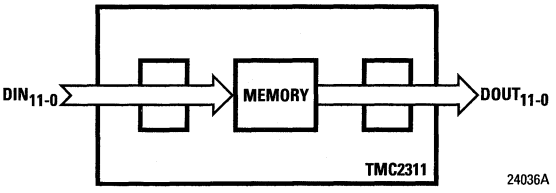


Table 1 summarizes the operation of controls $CTRL_7$, $CTRL_3$, ISEL, and OSEL, which "fine tune" the mode selection by programming the presubtractor/postadder and the transform direction. (Where a full two- dimensional FCT or IFCT is needed, $CTRL_{2-0}$ must be set to 011. $CTRL_7$=1 then enables presubtraction and OSEL=1 enables postaddition, as desired by the user.)

Table 1. Operating Mode Configurations

Application	Function	Device Configuration			
		$CTRL_7$	$CTRL_3$	ISEL	OSEL
2D DCT	2D FCT	0	0	X	0
2D IDCT	2D IFCT	0	1	X	0
Interframe Compress	2D FCT, Presubtract	1	0	0	0
Interframe Decompress	2D IFCT, Post Add	0	1	0	1
LPC	2D FCT, Presubtract	1	0	0	0
ILPC	2D IFCT, Post Add	0	1	0	1
LPC Directly Out	DOUT=DIN-DX	1	0	0	1
ILPC Directly Out	DOUT=DIN+DX	1	1	0	1
DPCM Directly Out	DOUT(k)=DIN(k)-DIN(k-1)	1	0	1	1
IDPCM Directly Out	DOUT(k)=DIN(k)+DIN(k-1)	1	1	1	1
DPCM w/ Transpose	DOUT(k)=DIN(k)-DIN(k-1)	1	0	1	0
IDPCM w/ Transpose	DOUT(k)=DIN(k)+DIN(k-1)	1	1	1	0

Notes: LPC/ILPC Linear Predictive Coding (Forward/Inverse)
DPCM/IDPCM Differential Pulse Code Modulation (Forward/Inverse)

Signal Definitions

Control

INIT — Single pass "start" command. INIT=0 resets the internal logic and output flags and updates the $CTRL_{7-0}$ parameters. INIT is registered and must be LOW for at least 3 clock cycles. INIT returning HIGH starts the transform. The first data point is loaded two cycles later.

NOOP — Input clock disable. NOOP=1 freezes operation of the device on the next CLK rising edge. Operation commences from where it stopped one cycle after NOOP returns LOW.

$\overline{WR}$ — Control word preload command. $\overline{WR}$=0 loads CTRL7-0 parameters into the device's preload register. The next INIT rising edge transfers the preloaded parameters into the chip's working registers.

$\overline{RD}$ — Control word (READ) command. $\overline{RD}$=0 allows the preloaded parameters $CTRL_{7-0}$ to be read.

$CTRL_{2-0}$ — MODE Control. Defines the internal configuration (mode) of the device, selecting either 2-dimensional or 1-dimensional transforms and/or the access to the internal Transpose Memory (***Figures 2*** through ***6***.)

$CTRL_{2-0}$	Operation
000	2–D Transform
001	2–D Transform
010	1–D Transform, Transpose
011	Transpose, 1–D Transform
100	1–D Transform
101	1–D Transform
110	Transpose
111	Transpose

$CTRL_3$ — Inverse Transform Enable (INV). INV=0 selects a forward DCT. If INV=1, the device will compute the Inverse DCT. INV also inverts the data to one side of the auxiliary adder. When and only when INV=0, data from the multiplexer which selects the DX port or delayed DIN port will be inverted.

$CTRL_4$ — Automatic Reinitialization (AUTOINIT). AI=0 allows continuous operation of device. When AI=1, the device will halt at the end of the specified transform.

$CTRL_5$ — Arithmetic Limit (CLIP). CLIP=1 saturates data outputs to 9 bits. CLIP is useful when presubtraction or postaddition is used with the DCT or IDCT.

$CTRL_6$ — Flag Control (FC). FC determines when the output flags, BOT and EOB, appear. When FC=0, both flags are output with the corresponding data result. When FC=1, the flags appear two clock cycles earlier.

$CTRL_7$ — Auxiliary Adder Select (XSEL). XSEL controls two multiplexers within the auxiliary adder circuitry. The first mux feeds the non-inverted input to the adder either the DIN port (XSEL=1) or outputs from the core of the device (XSEL=0). The second mux selects the data entering the core of the device from either the input port (XSEL=0) or adder output (XSEL=1). See ***Applications, Operating Mode Configurations***.

ISEL — Input Data Select. ISEL=0 connects the inverted (optional) input of the auxiliary adder to the DX port. When ISEL=1, the DIN port is connected, via a one data cycle delay. Output from this mux to the adder is inverted when INV=0. See ***Applications, Operating Mode Configurations***.

OSEL — Output Data Select. When OSEL=0, data results from the device core pass to the final output register. When OSEL=1, results from the adder pass to the final output register. See ***Applications, Operating Mode Configurations***.

$\overline{OE}$ — Asynchronous active LOW OUTPUT ENABLE for data output port, $DOUT_{11-0}$. When $\overline{OE}$=1, every output is forced into a high-impedance state.

$\overline{FE}$ — Active LOW asynchronous output FLAG ENABLE. When $\overline{FE}$=1, BOT and EOB are forced into a high-impedance state.

Data Inputs

DIN_{11-0} Data INput Port (12-bit two's complement format). DIN is the input port for both FORWARD and INVERSE transforms. DIN11 is the MSB. For two dimensional forward transforms, data precision is limited to 9 bits, DIN_{8-0}, and must be sign-extended into the remaining MSBs. Data exceeding the lower 9-bit range may cause an internal overflow. For INVERSE transforms, the entire 12-bit input port may used without risk of overflow.

DX_{8-0} Auxiliary Data Input Port (9-bit two's complement format). Feeds one side of auxiliary adder. DX_8 is the MSB. Auxiliary inputs can be provided to the device for linear predictive coding (LPC) where pixel differences are transformed. In the FORWARD direction, inputs supplied to the DX port (and selected via ISEL) will be subtracted from pixel values input simultaneously on the DIN port. In the INVERSE direction, DX inputs will be added to outputs following the desired tranform operation. The DX inputs must be delayed so that they appear at the adder simultaneously with the corresponding pixel outputs.

Data Outputs

$DOUT_{11-0}$ Data OUTput Port (12-bit, two's complement format). DOUT is the output port for both FORWARD and INVERSE transforms. $DOUT_{11}$ is the MSB. When CLIP=1, all data outputs are clipped to 9 bits, $DOUT_{8-0}$, with sign extension into the remaining MSBs. DOUT is forced into a high-impedance state when $\overline{OE}$=1.

Output Flags

BOT Beginning Of Transform. Toggles LOW to denote the first result of each one-dimensional 8-point transform or the first result of each 8-point row or column of a two-dimensional transform. When FC=0, BOT will appear simultaneously with the corresponding result. When FC=1, BOT will appear one data I/O cycle earlier.

EOB End Of Block. Toggles LOW to signal the last result of the entire (8 or 64 point) transform field. When FC=0, EOB appears simultaneously with the last data result. When FC=1, EOB appears two cycles earlier.

Clock

CLK Data Path Clock. The device operates with a clock of 0 to 30MHz. All internal operations are referenced to the rising edges of CLK; I/O operations except $CTRL_{7-0}$ read and write, to alternate rising edges of CLK.

Power

V_{DD}, GND The TMC2311 operates from a single +5 Volt supply. All V_{DD} and GND pins must be connected.

Table 2. Data Formats and Bit Weighting

	11	10	9	8	7	6	5	4	3	2	1	0
	Input Data Format – Forward Transforms											
DIN	S	S	S	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Input Data Format – Inverse Transforms											
DX:	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
				-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Output Data Format – Forward Transforms											
DOUT:	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Output Data Format – Inverse Transforms											
	S	S	S	-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Notes: S = Sign Extension.
In forward transforms, system should feed two's complement sign bit to DIN_{11-8} for 9-bit data size.
In inverse transforms, chip will output two's complement sign bit into pins $DOUT_{11-8}$.

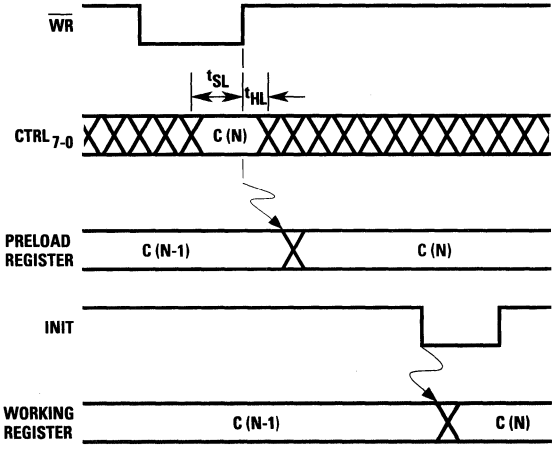
Operation and Timing

Initialization

Control Word Preload Timing

The self-sequencing TMC2311 requires no cycle-to-cycle supervision by the host system. On the rising edge of $\overline{WR}$, the user loads an 8-bit control word ($CTRL_{7-0}$) which sets 5 device parameters: mode and direction of the transform, continuous (or non-continuous) device operation, format of output data and timing of the output flags. The control parameters preloaded via $CTRL_{7-0}$ are registered internally and updated by the INIT signal. Control load timing is displayed in *Figure 7*.

Figure 7. Control Preload Timing



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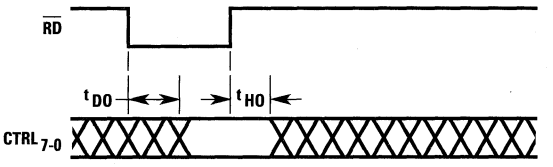
Control Word Read Timing

The TMC2311 also permits the user to read the preloaded control word value back through $CTRL_{7-0}$, a bidirectional port. When $\overline{RD}$=0, the $CTRL_{7-0}$ port outputs the control information stored in the device (*Figure 8*).

Figure 8. Control Read Timing



Data Input Timing

After the TMC2311 is initialized, data are input to DIN_{11-0} and DX_{8-0} on alternate rising edges of the device system clock. When the device is set for forward DCTs with transpose, data inputs are accepted in row-major format, i.e., line-by-line through the 8x8 transform window. When the device performs inverse DCTs, inputs are accepted in column-major format. Following the rising edge of INIT command, data inputs can be continuously loaded into the device on alternate rising edges of the system clock (*Figure 9*).

Data Output Timing

Results are output at half the system clock rate. The initial result latency and the number of results depends on the device operation specified by $CTRL_{2-0}$. Once the first result reaches the output port, remaining results will appear continuously. When the TMC2311 is set to perform forward DCTs with transpose, output data are written in column-major format. In the inverse direction, data results are returned row-by-row (*Figure 10*).

Figure 9. Data Input Timing

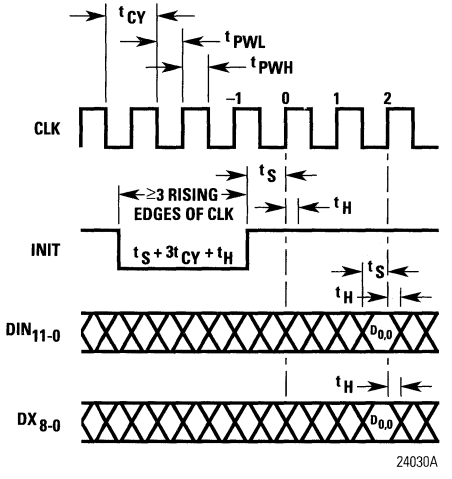
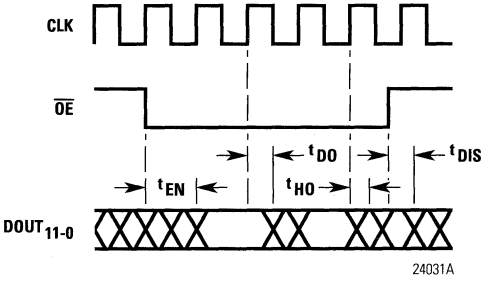


Figure 10. Data Output Timing



Overall Timing

The TMC2311 will expect data in groups of 8 or 64 points at regular intervals based on the mode of operation defined by $CTRL_{2-0}$. Results will be returned by the TMC2311 in similar groups following a predetermined initial latency. For applications that use the auxiliary adder ahead of the core of the device, corresponding DX and DIN inputs should be presented simultaneously to the device. Applications that use the adder after the DCT/memory core must account for the device's internal latency (*Table 3*). Each DX port input must be timed to appear at the adder one data cycle ahead of its corresponding output.

Table 3. Data Output Latency

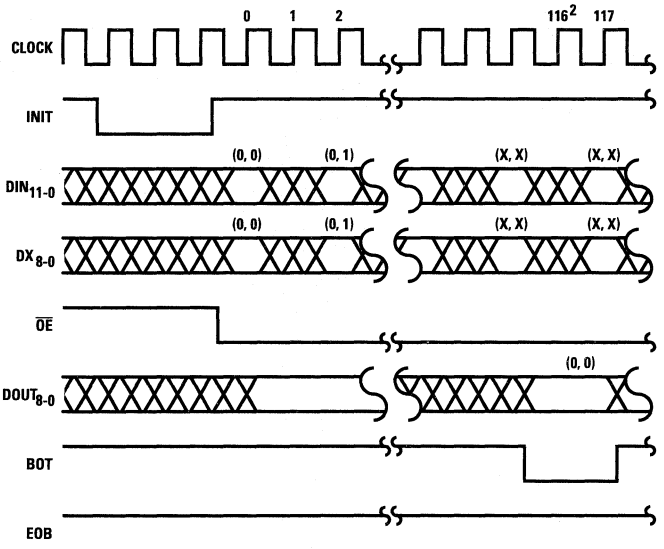
$CTRL_{2-0}$	Operation	Latency*
000	2-D Transform	232 clocks
001	2-D Transform	232
010	1-D Transform, Transpose	200
011	Transpose, 1-D Transform	200
100	1-D Transform	56
101	1-D Transform	56
110	Transpose	168
111	Transpose	168

*cycles after INIT goes high

If AUTOINIT ($CTRL_4$)=0, the device will operate continuously with no interruption between transforms. Otherwise the device will halt after the specified number of data points have been processed. When AUTOINIT=1, device operation will resume with the next INIT signal.

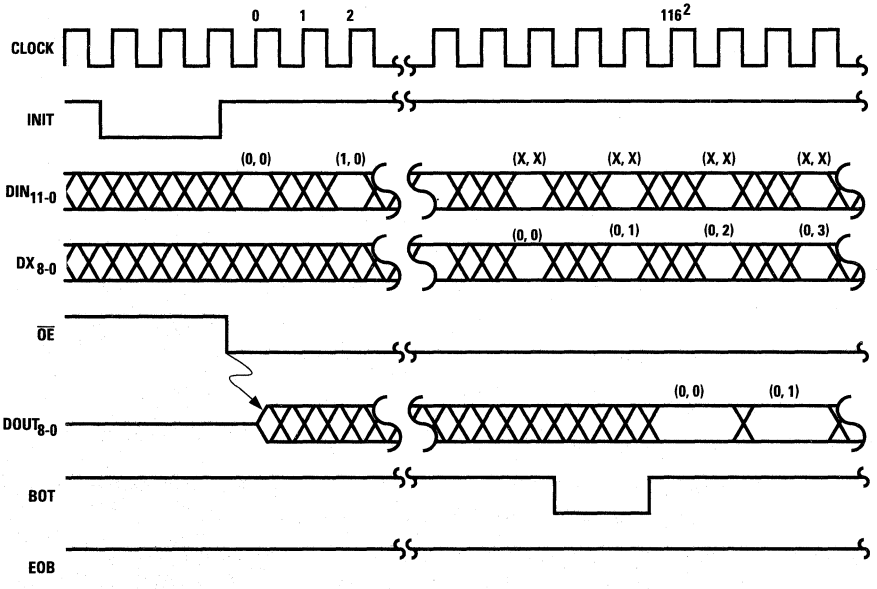
The TMC2311 also provides two output flags to differentiate between the rows/columns of the transform window and between individual transform blocks. The Beginning Of Transform (BOT) flag goes LOW with the first data result of each 8x1 transform row or column. A second flag, End Of Block, EOB, delineates transform blocks. EOB will go LOW when the last data point of each 8x1 (one dimensional mode) or 8x8 (two dimensional mode) transform is output. The user can program these flags to appear with their respective data (FC=0) or one data cycle earlier (FC=1). *Figure 11* shows the overall timing of a forward 2-D DCT with pre-subtraction and FC=0. *Figure 12* shows the overall timing of an inverse 2-D DCT with post addition and FC=1, demonstrating the timing for inputs to auxiliary port DX_{8-0} and the shift in flag timing.

Figure 11. Overall Timing - Forward Transform (Flag Control=0)

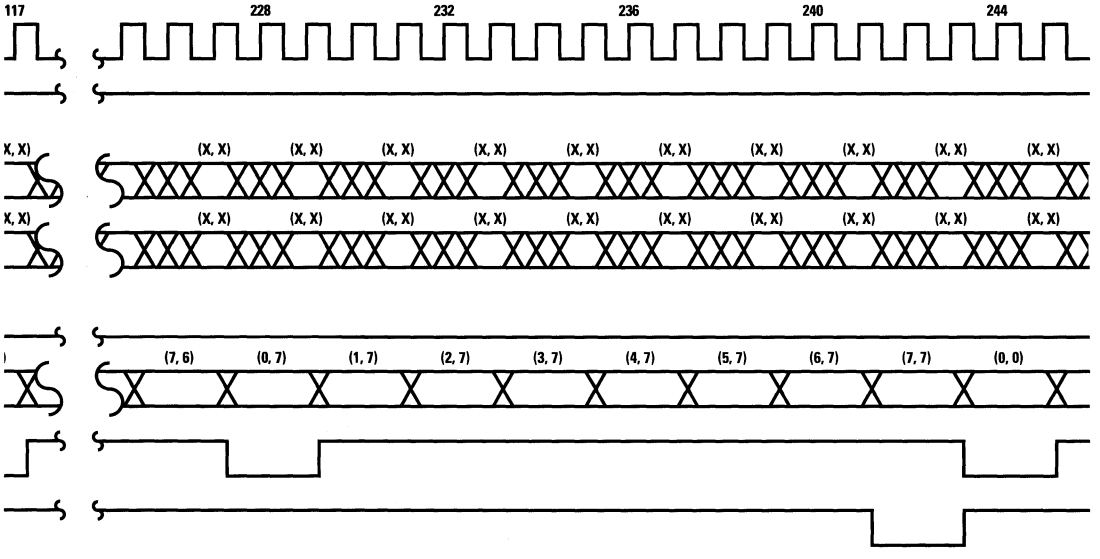


Notes: 1. DIN_{11-0} (i,j) aligned with DX_{8-0} (i,j), but alignment with $DOUT_{11-0}$ is mode-dependent..
2. $DOUT_{11-0}$ (0,0) is valid on CLK rising edge 116 in two-dimensional transfer modes only.

Figure 12. Overall Timing - Inverse Transform (Flag Control=1)



Notes: 1. DX_{8-0} (i,j) precedes $DOUT_{11-0}$ (i,j) by two CLK cycles, but alignment with DIN_{11-0} is mode-dependent.
2. $DOUT_{11-0}$ (0,0) is valid on CLK rising edge 116 in two-dimensional transform modes only.



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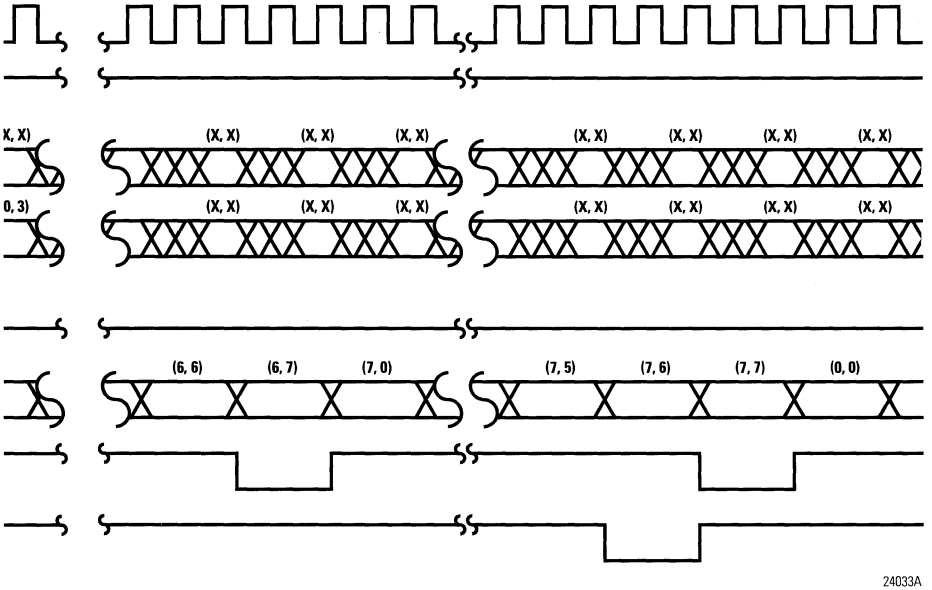

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Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage[2] ..... −0.5 to (V_{DD} + 0.5)V

Output

Applied Voltage[2] ..... −0.5 to (V_{DD} + 0.5V)

Forced Current,[3,4] ..... −3.0 to +6.0mA

Short Circuit Duration

(single output in HIGH state to ground) ..... 1 second

Temperature

Operating, Case ..... −60 to +130°C

Junction ..... +175°C

Lead, Soldering (10 seconds) ..... +300°C

Storage. ..... −65 to +150°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameter are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

2. Applied voltage must be current limited to specified range, and measured with respect to GND.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Nom	Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
t_{CY}	Cycle Time				
	TMC2311	37			ns
	TMC2311-1	34.5			ns
	TMC2311-2	28			ns
t_{PWL}	Clock Pulse Width, LOW	8			ns
t_{PWH}	Clock Pulse Width, HIGH	8			ns
t_S	Input Setup Time	11			ns
t_H	Input Hold Time	0			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C
T_C	Case Temperature				°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{DDQ}	Supply Current, Quiescent[2]	V_{DD}=Max, V_{IN}=0V, TS=5V		30	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=30MHz, TS=5V		130	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V		–10	µA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		+10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current,	V_{DD}=Max, V_{IN}=0V Output LOW		–40	mA
I_{OZH}	Hi-Z Output Leakage Current,	V_{DD}=Max, V_{IN}=0V Output HIGH		+40	mA
I_{OS}	Short Circuit Output Current	V_{DD}=Max, Output HIGH one pin to ground one second duration max.		–45	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown above, but guarantee operation as specified.
2. Following power-on, the TMC2311 must be clocked for at least 10 clock cycles before the clock is disabled.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_{DO}	Output Delay	V_{DD}=Min, C_{Load}=40pF		16	ns
	TMC2311			16	
	TMC2311-1			16	
	TMC2311-2			12	
t_{HO}	Output Hold Time	V_{DD}=Max, C_{Load}=40pF	4		ns
t_{ENA}	Three-State Output Enable Delay	V_{DD}=Min, C_{Load}=40pF		16	ns
	TMC2311			16	
	TMC2311-1			16	
	TMC2311-2			12	
t_{DIS}	Three-State Output Disable Delay	V_{DD}=Min, C_{Load}=40pF		22	ns

Note: 1. All transitions except for t_{DIS} and t_{ENA} are measured at a 1.5V level.

Figure 13. Equivalent Input Circuit

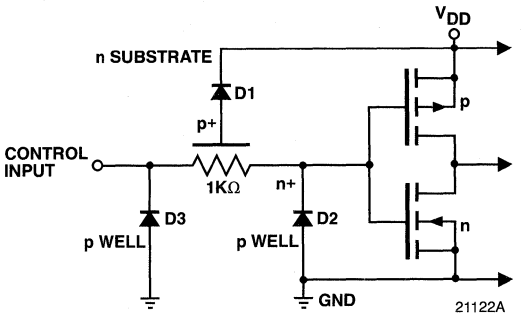
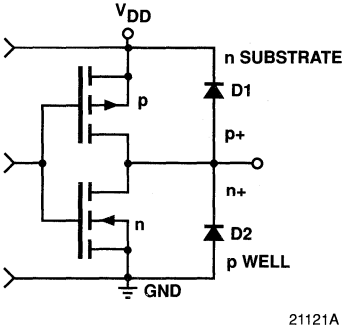


Figure 14. Equivalent Output Circuit



Applications Discussions

Frequency Domain Coding - Basic System

Frequency domain coding entails partitioning an image into (for example) 8x8 pixel blocks, then determining the two-dimensional spatial frequency spectrum of each block. In image compression, each component is then quantized by a frequency-specific factor, which tends to be smaller (more precise) for the dominant lower- frequency components and larger (coarser) for the less crucial higher-frequency components. Quantization effects compression by reducing the number of bits per frequency bin and by zeroing out high-frequency, low-energy bins. Following the quantizer, the scaled frequency data are then (arithmetic or Huffman) coded into a format that will allow them to be transmitted (or archived) even more economically. In particular, the JPEG modified Huffman coding represents each string of "zeroed out" bins with a compact code.

The transmitted images are reconstructed by reversing these operations. Coded information is received and restored to frequency information through a decoder. The received (or retrieved) data then pass through an inverse quantizer that restores the most important frequency components, albeit at somewhat grainier than original levels. Finally, the image is reconstructed by the inverse DCT. In practice, compression ratios of up to 20:1 can provide visually acceptable results with still images.

The basic compression circuit (*Figure 15*) shows a sample implementation of an intraframe compressor. The system contains an encoder comprising the TMC2311 DCT chip, a quantizer and a coder. Images are reconstructed in a complementary system with a decoder, a dequantizer, and a TMC2311 (inverse) DCT chip.

Figure 15. Basic System

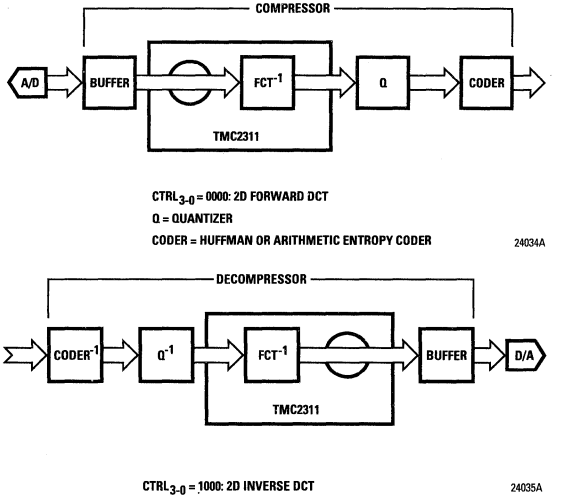
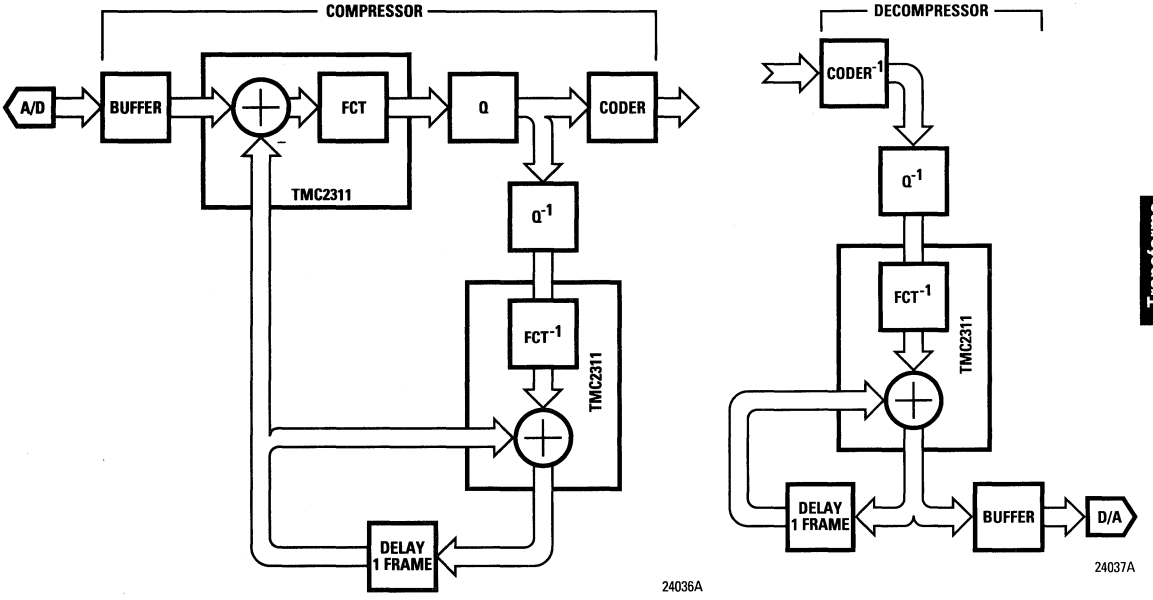


Figure 16. Interframe Compression System



Interframe Compression

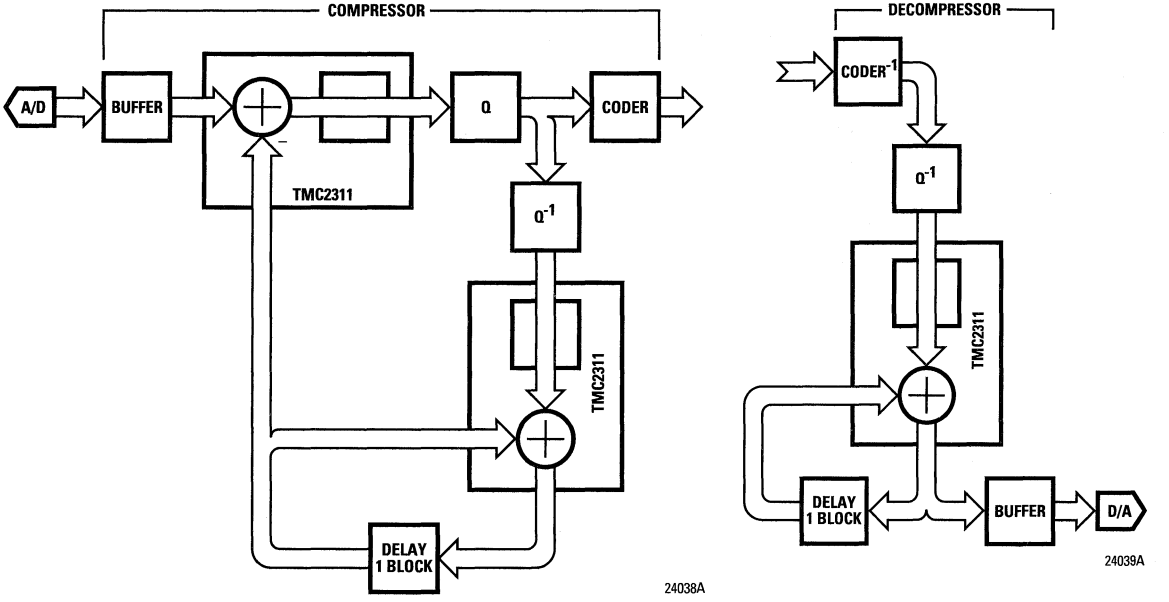
Figure 16 shows a moving picture extension of frequency domain coding, which processes differences between the corresponding pixels of successive image frames. Interframe compression describes areas of change within a moving image by comparing each new frame against earlier frames. Prior to the DCT, a block from the new frame is subtracted from the corresponding block of the previous frame. The resulting differences are transformed, quantized, coded, and transmitted. The compressed data are then reconstructed by reversing the processing steps: decode, dequantize, inverse DCT, then accumulate differences from frame to frame. Transforming only these differences increases the achievable compression.

Linear Predictive Coding System

Many critical biomedical and defense applications require that images be compressed and then restored "losslessly," i.e., without degradation. One technique, referred to as Linear Predictive Coding (LPC), has been very effective in speech compression. For image compression, LPC entails coding the differences between the current and previous pixel blocks of the same frame. This technique of intraframe compression can be used with or without the DCT. Much of the *Figure 16* interframe compression architecture can also be applied here, although the delay block now corresponds to delay within a single frame.

To obtain lossless compression, the user may code the differences between pixel blocks directly, without the DCT. This variety of intraframe compression, demonstrated in *Figure 17*, uses just the auxiliary adder of the TMC2311. In the forward direction, the differences are computed and transferred to the quantizer and coder circuitry where they are readied for transmission. In the inverse direction, the reconstruction process involves inverse coding and quantization, followed by cumulative addition of the image differences by the TMC2311's auxiliary adder.

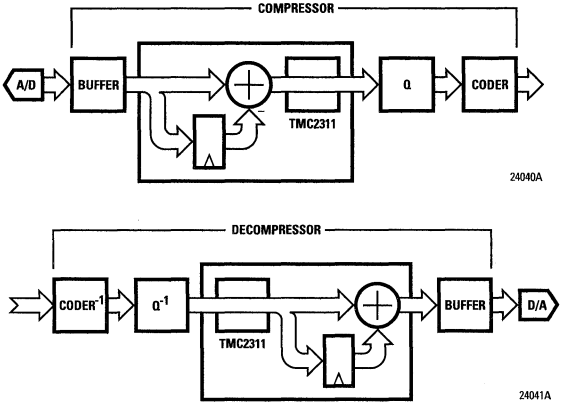
Figure 17. Linear Predictive Coding System (No Cosine Transform)



Differential Pulse Code Modulation

Another linear prediction algorithm, differential pulse code modulation, (DPCM) uses the differences between individual pixels on each line of the image. These differences are quantized, coded and transmitted (or archived). This technique is also used where lossless compression is required. The system shown in *Figure 18* illustrates the use of the auxiliary adder circuit of the TMC2311. The device incorporates a special input delay path that allows a previous pixel value to be added or subtracted from the current input pixel value. The results are then either fed into the device core to perform a transpose function or output directly from the adder. In the forward direction the pixel differences are fed to the quantizer and coder blocks of the system and transmitted. In the inverse direction the coded information is reconstructed by inverse coding followed by inverse quantization and finally the accumulation of pixel differences in the TMC2311.

Figure 18. Differential Pulse Code Modulation System (No Cosine Transform)



Package Interconnections

Signal Type	Signal Name	Function	Value	R1 Package Pin
Power	V_{DD}	Supply Voltage	+5.0V	2 10 17 33 53 68
	GND	Ground	0.0V	1 4 9 13 18 26 35 52 67
Clock	CLK	System Clock	TTL	65
Inputs	DIN_{11-0}	Data Inputs	TTL	44 45 46 47 48 49 50 51 54 55 56 57
	DX_{8-0}	Aux Adder In	TTL	34 36 37 38 39 40 41 42 43
Outputs	$DOUT_{11-0}$	Data Outputs	TTL	5 6 7 8 11 12 14 15 16 19 20 21
	BOT	Begin Transform	TTL	22
	EOB	End Of Block	TTL	23
Control	INIT	Initialize	TTL	60
	NOOP	No Operation	TTL	61
	$\overline{WR}$	Control Preload	TTL	66
	$\overline{RD}$	Read Control	TTL	64
	ISEL	Input Data Select	TTL	59
	OSEL	Output Select	TTL	58
	$\overline{OE}$	Output Enable	TTL	3
	$\overline{FE}$	Flag Enable	TTL	62
	$CTRL_{7-0}$	Control Params	TTL	32 31 30 29 28 27 25 24
	DNR	Test Pin	—	63
Do Not Connect				

Ordering Information

Product Number	Data Rate MHz	Temperature Range	Screening	Package	Package Marking
TMC2311R1C	13.5	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C
TMC2311R1C1	14.5	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C1
TMC2311R1C2	17.8	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C2

40G06753 Rev B 8/93

TMC2330
CMOS Coordinate Transformer
16 x 16 Bit, 25 MOPS

Description

The TMC2330 VLSI circuit converts bidirectionally between Cartesian (real and imaginary) and Polar (magnitude and phase) coordinates at up to 25 MOPS (Million Operations Per Second).

In its Rectangular-to-Polar mode, the TMC2330 can extract phase and magnitude information or backward "map" from a rectangular raster display to a radial (e.g., range-and-azimuth) data set.

The Polar-to-Rectangular mode executes direct digital waveform synthesis and modulation. With its 32-bit phase accumulator, the chip can generate and frequency or phase-modulate quadrature sinusoidal waveforms with a frequency resolution of 0.006 Hz at a 25 MHz clock rate. The TMC2330 greatly simplifies real-time image-space conversion between the radially-generated image scan data found in radar, sonar, and medical imaging systems, and raster-oriented display formats.

All input and output data ports are registered, and a new transformed data word pair is available at the output every 40 ns. The user-configurable phase accumulator structure, input clock enables, and asynchronous three-state output bus enables simplify interfacing. All signals are TTL compatible.

Fabricated in Raytheon Semiconductor's OMICRON-C™ one-micron CMOS process, the TMC2330 operates at up to the 25 MHz maximum clock rate over the full commercial (0 to 70°C) temperature and supply voltage ranges, and is available in a low-cost 120-pin plastic pin grid array package. The MIL-STD-883C version, the TMC2330L5V, is housed in a ceramic chip carrier and is specified over the full extended (-55 to 125°C) case temperature range.

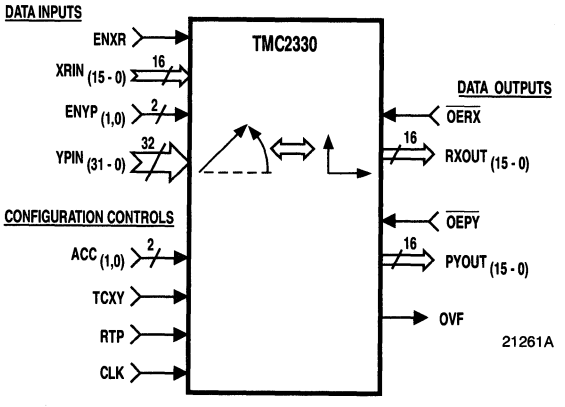
Features

- Rectangular-to-Polar or Polar-to-Rectangular conversion at guaranteed 25 MOPS pipelined throughput rate
- Polar data: 16-bit magnitude, 32-bit input/16-bit output phase
- 16-bit user-selectable two's complement or sign-and-magnitude rectangular data formats
- Input register clock enables and asynchronous output enables simplify interfacing
- User-configurable phase accumulator for waveform synthesis and amplitude, frequency, or phase modulation
- Magnitude output data overflow flag (in Polar-to-Rectangular mode)
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 120-pin plastic pin grid array package
- Available in a 132-leaded CERQUAD

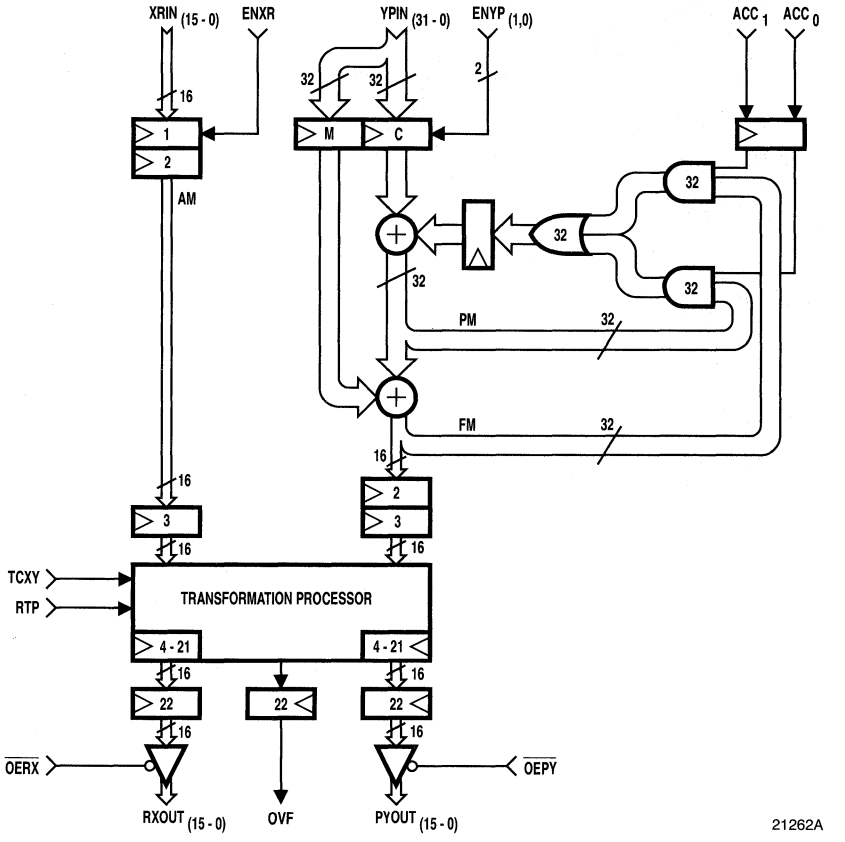
Applications

- Scan conversion (phased array to raster)
- Vector magnitude estimation
- Range and bearing derivation
- Spectral analysis
- Digital waveform synthesis, including quadrature functions
- Digital modulation and demodulation

TMC2330 Logic Symbol



Functional Block Diagram



Functional Description

General Information

The TMC2330 converts between Rectangular (Cartesian) and Polar (Phase and Magnitude) coordinate data word pairs. The user selects the numeric format and transformation to be performed (Rectangular-To-Polar or Polar-To-Rectangular), and the operation is performed on the data presented to the inputs on the next clock. The transformed result is then available at the outputs 22 clock cycles later, with new output data available every 40ns. All input and output data ports are registered, with input clock enables and asynchronous high-impedance output enables to simplify connections to system buses.

When executing a Rectangular-To-Polar conversion, the input ports accept 16-bit Rectangular coordinate words, and the output ports generate 16-bit magnitude and 16-bit phase data. The user selects either two's complement or sign-and-magnitude Cartesian data format. Polar magnitude data are always in magnitude format only. Since the phase angle word is modulo 2π, it may be regarded as either unsigned or two's complement format (*Tables 1 and 2*).

In Polar-To-Rectangular mode, the input ports accept 16-bit Polar magnitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words. Again, the user selects between two's complement or sign-and-magnitude Cartesian data format. The dual 32-bit phase accumulator input registers are useful in signal synthesis applications, storing high-accuracy (0.006Hz at the maximum clock rate) phase increment values with minimal accumulation error. This allows the TMC2330 to generate precision quadrature waveforms unattended, once the accumulator has been enabled. The flexible input phase accumulator structure supports

General Information (cont.)

frequency or phase modulation, as determined by the input register clock enable $ENYP_{1,0}$ and accumulator control word $ACC_{1,0}$. The 16 MSBs (Most Significant Bits) of phase data are used in the transformation itself.

Signal Definitions

Power

V_{DD}, GND — The TMC2330 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK — The TMC2330 operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Inputs/Outputs

$XRIN_{15-0}$ — $XRIN_{15-0}$ is the registered Cartesian X-coordinate or Polar Magnitude (Radius) 16-bit input data port. $XRIN_{15}$ is the MSB.

$YPIN_{31-0}$ — $YPIN_{31-0}$ is the registered Cartesian Y-coordinate or Polar Phase angle 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENYP_{1,0}$. When RTP is HIGH (Rectangular-To-Polar), the input accumulators are normally not used. The 16 MSBs of YPIN are the input port, and the lower 16 bits become "don't cares" if ACC=00. $YPIN_{31}$ is the MSB.

$RXOUT_{15-0}$ — $RXOUT_{15-0}$ is the registered Polar Magnitude (Radius) or X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OERX}$=HIGH. $RXOUT_{15}$ is the MSB.

$PYOUT_{15-0}$ — $PYOUT_{15-0}$ is the registered Polar Phase angle or Cartesian Y-coordinate 16-bit output data port. This output is forced to the high-impedance state when $\overline{OEPY}$=HIGH. $PYOUT_{15}$ is the MSB.

Controls

ENXR — The value presented to the input port XRIN is latched into the input registers on the current clock when ENXR is HIGH. When ENXR is LOW, the value stored in the register remains unchanged.

$ENYP_{1,0}$ — The value presented to the YPIN input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENYP_{1,0}$, as shown below:

$ENYP_{1,0}$	Instruction
00	No registers enabled, current data held
01	M register input enabled, C data held
10	C register input enabled, M data held
11	M register set to 0, C register input enabled

where C is the Carrier register and M is the Modulation register, and 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

RTP — This registered input selects the current transformation mode of the device. When RTP is HIGH, the TMC2330 executes a Rectangular-To-Polar conversion. When RTP is LOW, a Polar-To-Rectangular conversion will be performed. The input and output ports are then configured to handle data in the appropriate coordinate system. This is a static input. See the *Timing Diagram*.

$ACC_{1,0}$ — In applications utilizing the TMC2330 to perform waveform synthesis and modulation in the Polar-To-Rectangular mode (RTP=LOW), the user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word $ACC_{1,0}$, as shown below:

$ACC_{1,0}$	Configuration
00	No accumulation performed
01	PM accumulator path enabled
10	FM accumulator path enabled
11	(Nonsensical) logical OR of PM and FM

where 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees.

Controls (cont.)

$ACC_{1,0}$ (cont.) Note that the accumulators will also function when RTP = HIGH (Rectangular-To-Polar), which is useful when performing backward mapping from Cartesian to polar coordinates. However, most applications will require that $ACC_{1,0}$ be set to 00 to avoid accumulating the Cartesian Y input data.

TCXY The format select control sets the numeric format of the Rectangular data, whether input (RTP = HIGH) or output (RTP = LOW). This control indicates two's complement format when TCXY = HIGH, and sign-and-magnitude when LOW. This is a static input. See the *Timing Diagram*.

OVF When RTP = LOW (Polar-To-Rectangular), the Overflow Flag will go HIGH on the clock that the magnitude of either of the current Cartesian coordinate outputs exceeds the maximum range. It will return LOW on the clock that the Cartesian out-put value(s) return to full-scale or less. See the *Applications Discussion* section. Overflow is not possible in Rectangular-To-Polar mode (RTP = HIGH).

$\overline{OERX}$, $\overline{OEPY}$ Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OERX}$ or $\overline{OEPY}$ is HIGH, the respective output port(s) is in the high-impedance state.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 9, 21, 37, 45, 53, 67, 87, 91, 99, 112, 120
	GND	Ground	D3, E2, F2, G3, K3, L3, L7, K11, J11, G11, E12, D11, C10, C9, C7, C5, C4	5, 11, 14, 17, 29, 33, 49, 75, 83, 89, 95, 104, 108, 116, 124, 129
Clock	CLK	System Clock	F3	13
Inputs	$XRIN_{15-0}$	X or Radius Data	F12, F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	86, 85, 84, 82, 81, 80, 79, 78, 77, 76, 74, 73, 71, 69, 68, 66
	$YPIN_{31-0}$	Y or Phase Data	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	61, 60, 59, 58, 57, 56, 55, 54, 52, 51, 50, 48, 47, 46, 44, 43, 42, 41, 40, 39, 38, 36, 34, 31, 30, 28, 27, 26, 25, 24, 23, 22
Outputs	$RXOUT_{15-0}$	Radius or X Data	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	90, 92, 93, 94, 96, 97, 100, 102, 105, 106, 107, 109, 110, 111, 113, 114
	$PYOUT_{15-0}$	Phase or Y Data	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	117, 118, 119, 121, 122, 123, 125, 126, 127, 130, 132, 3, 4, 6, 7, 8
Controls	ENXR	X or Radius In Enable	M11	63
	$ENYP_{1,0}$	Y or Phase In Enable	G1, G2	18, 16
	RTP	Conversion Select	E1	12
	$ACC_{1,0}$	Accumulate Control	H2, H1	20, 19
	TCXY	Cartesian Data Format	F1	15
	$\overline{OERX}$	Radius or X Out Enable	E13	88
	$\overline{OEPY}$	Phase or Y Out Enable	D1	10
Flags	OVF	Overflow Flag	B7	115
No Connect	NC	No Connect Pins	–	2, 32, 35, 62, 64, 65, 72, 98, 101, 103, 128, 131
		Index Pin	D4	–

Static Control Inputs

The controls RTP and TCXY determine the transformation mode and the assumed numeric format of the Rectangular data. The user must exercise caution when changing either of these controls, as the new transformed results will not be seen the at the outputs until the entire internal pipe (22 clocks) has been flushed. Thus, these controls are considered static.

Table 1. Data Input/Output Formats – Integer Format

Port	RTP	TCXY	Bit # 31	30	29	. . .	16	15	14	. . .	0	Format	
XRIN	0	X						2^{15}	2^{14}	. . .	2^{0}.		U
XRIN	1	0						NS	2^{14}	. . .	2^{0}.		S
XRIN	1	1						-2^{15}	2^{14}	. . .	2^{0}.		T
YPIN	0	X	$\pm 2^{0}$.	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	$(x\pi)$T/U	
YPIN	1	0	NS	2^{14}	2^{13}		2^{0}.						S
YPIN	1	1	-2^{15}	2^{14}	2^{13}	. . .	2^{0}.						T
RXOUT	0	0						NS	2^{14}	. . .	2^{0}.		S
RXOUT	0	1						-2^{15}	2^{14}	. . .	2^{0}.		T
RXOUT	1	X						2^{15}	2^{14}	. . .	2^{0}.		U
PYOUT	0	0						NS	2^{14}	. . .	2^{0}.		S
PYOUT	0	1						-2^{15}	2^{14}	. . .	2^{0}.		T
PYOUT	1	X						$\pm 2^{0}$.	2^{-1}	. . .	2^{-15}	$(x\pi)$T/U	

Table 2. Data Input/Output Formats – Fractional Format

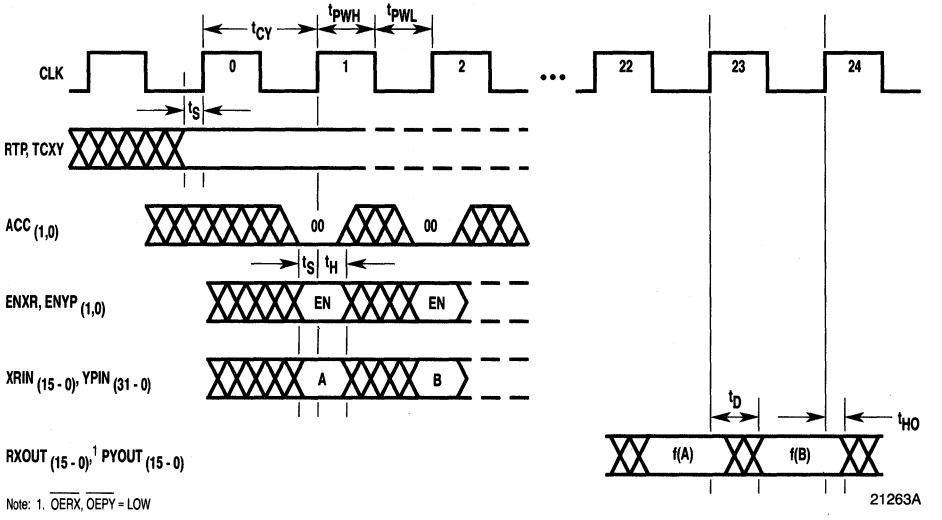
Port	RTP	TCXY	Bit # 31	30	29	. . .	16	15	14	. . .	0	Format	
XRIN	0	X						2^{0}.	2^{-1}	. . .	2^{-15}		U
XRIN	1	0						NS.	2^{-1}	. . .	2^{-15}		S
XRIN	1	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
YPIN	0	X	$\pm 2^{0}$.	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	$(x\pi)$T/U	
YPIN	1	0	NS.	2^{-1}	2^{-2}	. . .	2^{-15}						S
YPIN	1	1	-2^{0}	2^{-1}	2^{-2}	. . .	2^{-15}						T
RXOUT	0	0						NS.	2^{-1}	. . .	2^{-15}		S
RXOUT	0	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
RXOUT	1	X						2^{0}.	2^{-1}	. . .	2^{-15}		U
PYOUT	0	0						NS.	2^{-1}	. . .	2^{-15}		S
PYOUT	0	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
PYOUT	1	X						$\pm 2^{0}$.	2^{-1}	. . .	2^{-15}	$(x\pi)$T/U	

Notes:

1. -2^{15} denotes two's complement sign bit.
2. NS denotes negative sign, i.e., '1' negates the number.
3. $\pm 2^{0}$ denotes two's complement sign or highest magnitude bit – since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $+\pi$ or $-\pi$.
4. All phase angles are in terms of π radians, hence notation "$x\pi$."
5. If A_{CC}=00, YPIN (15-0) are "don't cares."
6. Formats:
   T=Two's Complement
   S=Signed Magnitude
   U=Unsigned

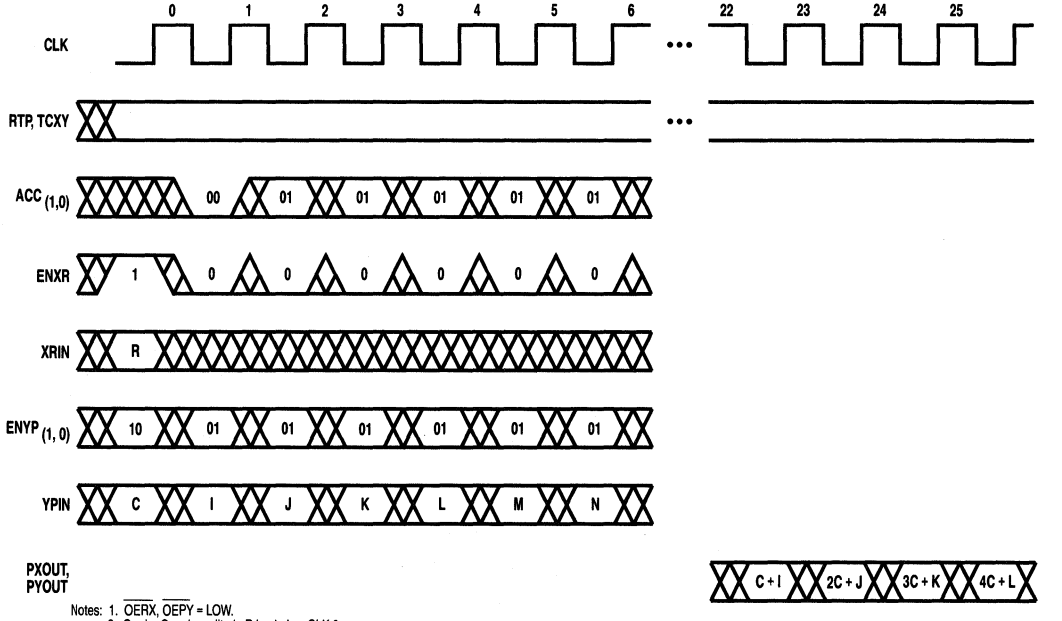
HEX	U	T	S
FFFF	65535	−1	−32767
−−	−−	−−	−−
8001	32769	−32767	−1
8000	32768	−32768	0
7FFF	32767	32767	32767
−−	−−	−−	−−
0001	1	1	1
0000	0	0	0

Figure 1. Timing Diagram – No Accumulation



Note: 1. $\overline{OERX}$, $\overline{OEPY}$ = LOW

Figure 2. Timing Diagram – Phase Modulation



Notes:
1. $\overline{OERX}$, $\overline{OEPY}$ = LOW.
2. Carrier C and amplitude R loaded on CLK 0.
3. Modulation values I, J, K, L, . . . loaded on CLK 1, CLK 2, etc.
4. Output corresponding to modulation loaded at CLK i emerged t_{DO} after CLK i + 21.
5. To modulate amplitude, vary XRIN with ENXR = 1.

Figure 3. Equivalent Input Circuit

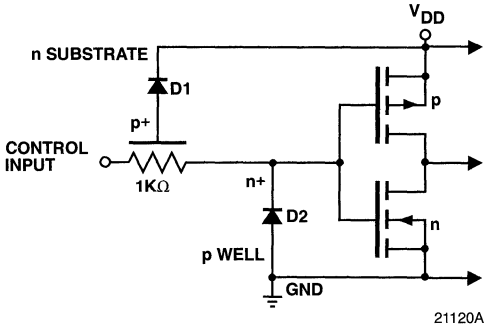


Figure 4. Equivalent Output Circuit

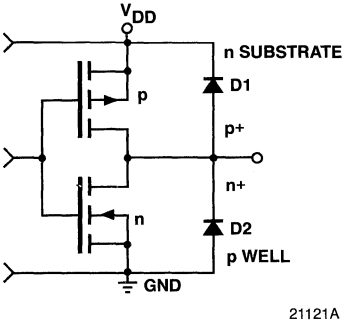
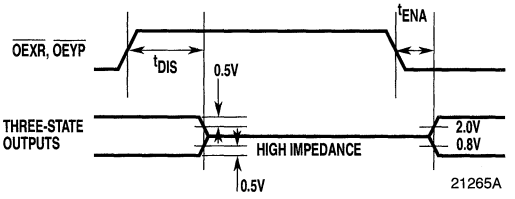


Figure 5. Transition Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD}+0.5)V
Output Voltage	
Applied voltage	−0.5 to (V_{DD}+0.5)V [2]
Forced current	−6.0 to 6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
V_{DD}	Supply Voltage		4.75	5.25	4.5	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8		0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		V
I_{OL}	Output Current, Logic LOW			8.0		8.0	mA
I_{OH}	Output Current, Logic HIGH			−4.0		−4.0	mA
t_{CY}	Cycle Time	V_{DD}=Min	50		55		ns
		TMC2330-1	40		45		ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	10		11		ns
		TMC2330-1	8		8		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	8		8		ns
		TMC2330-1	6		6		ns
t_S	Input Setup Time		12		13		ns
		TMC2330-1	10		11		ns
t_H	Input Hold Time		1		2		ns
		TMC2330-1	1		2		ns
T_A	Ambient Temperature, Still Air		0	70			°C
T_C	Case Temperature				−55	125	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=20MHz $\overline{OERX}$ and $\overline{OEPY}$=V_{DD}		160		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V		−10		−10	µA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		10		10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V		−40		−40	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		40		40	µA
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.	−20	−100	−20	−100	µA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but specified operation is guaranteed.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		22		25	ns
		TMC2330-1		20		23	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF		4		4	ns
		TMC2330-1		4		4	ns
t_{ENA}	Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF		13		17	ns
		TMC2330-1		12		15	ns
t_{DIS}	Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		14		14	ns
		TMC2330-1		13		13	ns

Transforms

Applications Discussion

Numeric Overflow

Because the TMC2330 accommodates 16-bit unsigned radii and 16-bit signed Cartesian coordinates, Polar-To-Rectangular conversions can overflow for incoming radii greater than 32767 = 7FFFh and will overflow for all incoming radii greater than 46341 = B505h. (In signed magnitude mode, a radius of 46340 = B504h will also overflow at all angles.) The regions of overflow and of correct conversion are illustrated in *Figure 6*.

In signed magnitude mode, overflows are circularly symmetrical – if a given radius overflows at an angle P, it will also overflow at the angles $\pi - P$, $\pi + P$, and $-P$. This is because $-X$ will overflow if and only if X overflows, and $-Y$ will overflow if and only if Y overflows.

In two's complement mode, the number system's asymmetry complicates the overflow conditions slightly. An input vector with an X component of −32768 = 8000h will not overflow, whereas one with an X component of +32768 will. *Table 3* summarizes several simple cases of overflow and near-overflow.

Numeric Underflow

In RTP = 1 (Rectangular-To-Polar mode), if XRIN = YPIN = 0, the angle is undefined. Under these conditions, the TMC2330 will output the expected radius of 0 (RXOUT = 0000) and an angle of 1.744 radians (PYOUT = 4707). This angle is an artifact of the CORDIC algorithm and is not flagged as an error, since the angle of any 0 length vector is arbitrary.

Table 3a. X-Dimensional Marginal Overflows

TC YPIN	OV RXOUT	CORRECT X
0 0000 = 0	1 0000 = +0	+32768
0 8000 = π	1 8000 = −0	−32768
1 0000 = 0	1 8000 = −32768	+32768
1 8000 = π	0 8000 = −32768	−32768

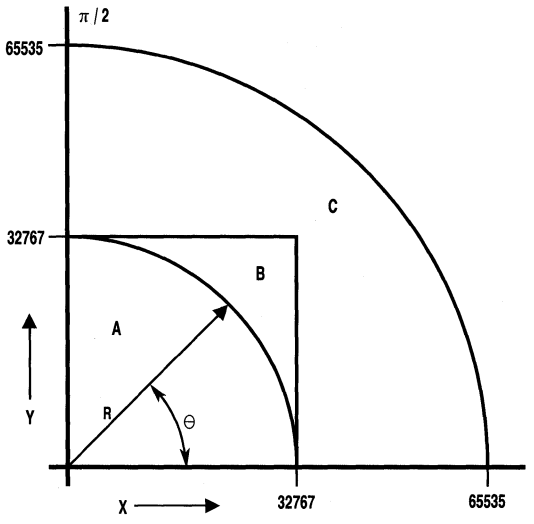
In all cases, RTP = 0 (Polar-To-Rectangular mode) and XRIN = 8000 (incoming radius = 32768).

Table 3b. Maximal Overflow (Radius In = 65535)

TC YPIN	OV RXOUT	CORRECT X
0 0000 = 0	1 7FFF = +32767	+65535
0 8000 = π	1 FFFF = −32767	−65535
1 0000 = 0	1 FFFF = −1	+65535
1 8000 = π	1 0001 = +1	−65535

In all cases, RTP = 0 (Polar-To-Rectangular mode) and XRIN = 7FFF (incoming radius = 65535, which will always overflow).

Figure 6. First Quadrant Coordinate Relationships



$X = R(\cos\Theta)$
$Y = R(\sin\Theta)$

and

$R = \sqrt{X^2 + Y^2}$
$\Theta = \tan^{-1}(Y/X)$

If R < 32768, overflow will not occur (region A).
If R > 32767, overflow will occur (region C) if |X| > 32767 or |Y| > 32767.
If R > 32767, overflow will not occur (region B) if |X| < 32768 and |Y| < 32768.

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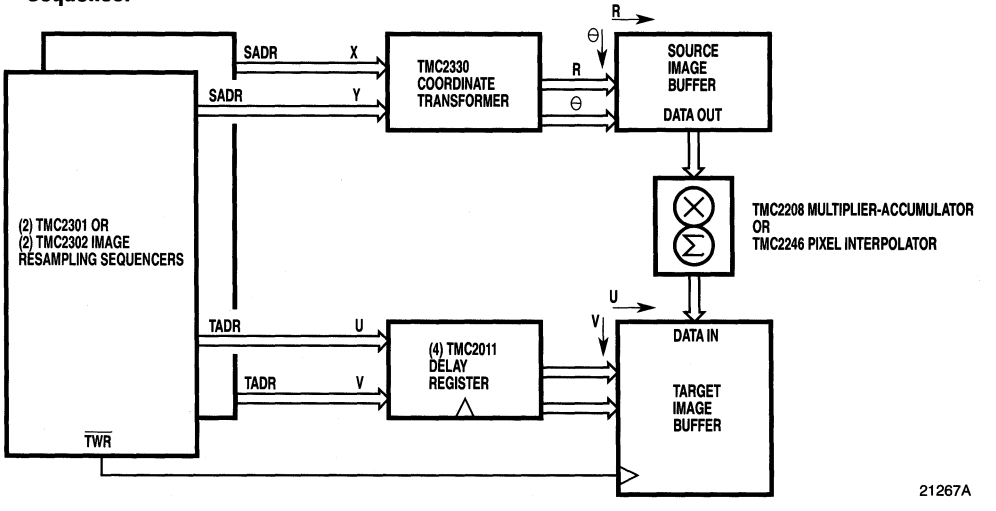
Performing Scan Conversion with the TMC2330

Medical Imaging Systems such as Ultrasound, MRI, and PET, and phased array Radar and Sonar systems generate radial-format coordinates (range or distance, and bearing) which must be converted into raster-scan format for further processing and display. Utilizing the TRW TMC2301 Image Resampling Sequencer, a minimum chipcount Scan Converter can be implemented which utilizes the trigonometric translation performed by the TMC2330 to backwards-map from a Cartesian coordinate set into the Polar source image buffer address space.

Figure 7. Block Diagram of Scan Converter Circuit Utilizing TMC2330 and TMC2301 Image Resampling Sequencer



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As shown in *Figure 7*, the TMC2330 transforms the Cartesian source image addresses from the TMC2301 directly to vector distance and angle coordinates, while the TMC2301 writes the resulting resampled pixel values into the target memory in raster fashion. Note that the ability to perform this spatial transformation in either direction gives the user the freedom to process images in either coordinate space, with little restriction. Image manipulation such as zooms or tilts can easily be included in the transformation by programming the desired image manipulation into the TMC2301's transformation parameter registers.

Statistical Evaluation of Double Conversion

In this empirical test, 10,000 random Cartesian vectors were converted to and from polar format by the TMC2330. The resulting Cartesian pairs were then compared against the original ones. The unrestricted data base represents uniform sampling over a square bounded by $-32769 < x < 32768$ and $-32769 < y < 32768$.

The results of the 10,000-vector study were as follows:

Mean Error (X)	= +0.0052 LSB
Mean Error (Y)	= +0.0031 LSB
Mean Absolute Error (X)	= 0.662 LSB
Mean Absolute Error (Y)	= 0.664 LSB
Root Mean Square Error (X)	= 1.025 LSB
Root Mean Square Error (Y)	= 1.020 LSB
Max Error (X)	= +4/−5 LSB
Max Error (Y)	= +5/−4 LSB

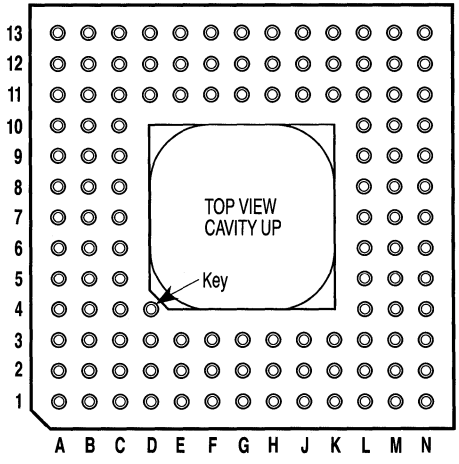
Since this is a double conversion (rectangular to polar and back) which includes a wide variety of "good case" and "bad case" vectors, the chip should perform even better in many actual systems. Repeating the experiment and restricting the original data set to an annulus defined by $8196 < R < 32768$ reduced the mean square error to 0.89 LSB and the peak error to ±4 LSB (x or y). These latter results are more germane to synthesizer, demodulator, and other applications in which the amplitude can be restricted to lie between quarter and full scale.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2330H5C1	STD: T_A = 0 to 70°C	Commercial	121-Pin Plastic Pin Grid Array	2330H5C1
TMC2330H5C	STD: T_A = 0 to 70°C	Commercial	121-Pin Plastic Pin Grid Array	2330H5C
TMC2330L5V1	EXT:T_C = -55°C to 125°C	MIL-STD-883	132-Leaded CERQUAD	2330L5V1
TMC2330L5V	EXT:T_C = -55°C to 125°C	MIL-STD-883	132-Leaded CERQUAD	2330L5V
TMC2330G1V1	EXT:T_C = -55°C to 125°C	MIL-STD-883	120-Pin Ceramic PGA	2330G1V1
TMC2330G1V	EXT:T_C = -55°C to 125°C	MIL-STD-883	120-Pin Ceramic PGA	2330G1V

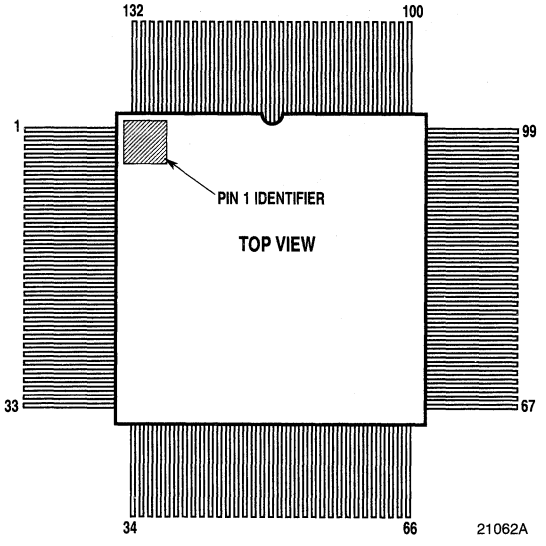
Pin Assignments — 121-Pin Plastic Pin Grid Array, H5 Package; 120-Pin Ceramic PGA, G1 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	$PYOUT_5$	B3	$PYOUT_6$	C5	GND	E1	RTP	G11	GND	K1	$YPIN_2$	L10	$YPIN_{31}$	M12	$XRIN_1$
A2	$PYOUT_7$	B4	$PYOUT_9$	C6	V_{DD}	E2	GND	G12	$XRIN_{12}$	K2	$YPIN_4$	L11	V_{DD}	M13	$XRIN_2$
A3	$PYOUT_8$	B5	$PYOUT_{11}$	C7	GND	E3	V_{DD}	G13	$XRIN_{13}$	K3	GND	L12	$XRIN_3$	N1	$YPIN_8$
A4	$PYOUT_{10}$	B6	$PYOUT_{13}$	C8	V_{DD}	E11	V_{DD}	H1	ACC_0	K11	GND	L13	$XRIN_4$	N2	$YPIN_{10}$
A5	$PYOUT_{12}$	B7	OVF	C9	GND	E12	GND	H2	ACC_1	K12	$XRIN_5$	M1	$YPIN_6$	N3	$YPIN_{12}$
A6	$PYOUT_{14}$	B8	$RXOUT_1$	C10	GND	E13	$\overline{OERX}$	H3	V_{DD}	K13	$XRIN_6$	M2	$YPIN_9$	N4	$YPIN_{15}$
A7	$PYOUT_{15}$	B9	$RXOUT_3$	C11	V_{DD}	F1	TCXY	H11	$XRIN_9$	L1	$YPIN_5$	M3	$YPIN_{11}$	N5	$YPIN_{17}$
A8	$RXOUT_0$	B10	$RXOUT_5$	C12	$RXOUT_{11}$	F2	GND	H12	$XRIN_{10}$	L2	$YPIN_7$	M4	$YPIN_{13}$	N6	$YPIN_{19}$
A9	$RXOUT_2$	B11	$RXOUT_7$	C13	$RXOUT_{13}$	F3	CLK	H13	$XRIN_{11}$	L3	GND	M5	$YPIN_{16}$	N7	$YPIN_{21}$
A10	$RXOUT_4$	B12	$RXOUT_9$	D1	$\overline{OEPY}$	F11	V_{DD}	J1	$YPIN_0$	L4	V_{DD}	M6	$YPIN_{18}$	N8	$YPIN_{22}$
A11	$RXOUT_6$	B13	$RXOUT_{12}$	D2	$PYOUT_0$	F12	$XRIN_{15}$	J2	$YPIN_1$	L5	$YPIN_{14}$	M7	$YPIN_{20}$	N9	$YPIN_{24}$
A12	$RXOUT_8$	C1	$PYOUT_1$	D3	GND	F13	$XRIN_{14}$	J3	$YPIN_3$	L6	V_{DD}	M8	$YPIN_{23}$	N10	$YPIN_{26}$
A13	$RXOUT_{10}$	C2	$PYOUT_2$	D11	GND	G1	$ENYP_1$	J11	GND	L7	GND	M9	$YPIN_{25}$	N11	$YPIN_{29}$
B1	$PYOUT_3$	C3	V_{DD}	D12	$RXOUT_{14}$	G2	$ENYP_0$	J12	$XRIN_7$	L8	V_{DD}	M10	$YPIN_{28}$	N12	$YPIN_{30}$
B2	$PYOUT_4$	C4	GND	D13	$RXOUT_{15}$	G3	GND	J13	$XRIN_8$	L9	$YPIN_{27}$	M11	ENXR	N13	$XRIN_0$



Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	23	$YPIN_1$	45	V_{DD}	67	V_{DD}	89	GND	111	$RXOUT_2$
2	NC	24	$YPIN_2$	46	$YPIN_{18}$	68	RXIN1	90	$RXOUT_{15}$	112	VDD
3	$PYOUT_4$	25	$YPIN_3$	47	$YPIN_{19}$	69	RXIN2	91	V_{DD}	113	$RXOUT_1$
4	$PYOUT_3$	26	$YPIN_4$	48	$YPIN_{20}$	70	GND	92	$RXOUT_{14}$	114	$RXOUT_0$
5	GND	27	$YPIN_5$	49	GND	71	$RXIN_3$	93	$RXOUT_{13}$	115	OVF
6	$PYOUT_2$	28	$YPIN_6$	50	$YPIN_{21}$	72	NC	94	$RXOUT_{12}$	116	GND
7	$PYOUT_1$	29	GND	51	$YPIN_{22}$	73	$RXIN_4$	95	GND	117	$PYOUT_{15}$
8	$PYOUT_0$	30	$YPIN_7$	52	$YPIN_{23}$	74	$RXIN_5$	96	$RXOUT_{11}$	118	$PYOUT_{14}$
9	V_{DD}	31	$YPIN_8$	53	V_{DD}	75	GND	97	$RXOUT_{10}$	119	$PYOUT_{13}$
10	$\overline{OEPY}$	32	NC	54	$YPIN_{24}$	76	$RXIN_6$	98	NC	120	V_{DD}
11	GND	33	GND	55	$YPIN_{25}$	77	$RXIN_7$	99	V_{DD}	121	$PYOUT_{12}$
12	RTP	34	$YPIN_9$	56	$YPIN_{26}$	78	$RXIN_8$	100	$RXOUT_9$	122	$PYOUT_{11}$
13	CLK	35	NC	57	$YPIN_{27}$	79	$RXIN_9$	101	NC	123	$PYOUT_{10}$
14	GND	36	$YPIN_{10}$	58	$YPIN_{28}$	80	$RXIN_{10}$	102	$RXOUT_8$	124	GND
15	TCXY	37	V_{DD}	59	$YPIN_{29}$	81	$RXIN_{11}$	103	NC	125	$PYOUT_9$
16	$ENYP_0$	38	$YPIN_{11}$	60	$YPIN_{30}$	82	$RXIN_{12}$	104	GND	126	$PYOUT_8$
17	GND	39	$YPIN_{12}$	61	$YPIN_{31}$	83	GND	105	$RXOUT_7$	127	$PYOUT_7$
18	$ENYP_1$	40	$YPIN_{13}$	62	NC	84	$RXIN_{13}$	106	$RXOUT_6$	128	NC
19	ACC_0	41	$YPIN_{14}$	63	ENXR	85	$RXIN_{14}$	107	$RXOUT_5$	129	GND
20	ACC_1	42	$YPIN_{15}$	64	NC	86	$RXIN_{15}$	108	GND	130	$PYOUT_6$
21	V_{DD}	43	$YPIN_{16}$	65	NC	87	V_{DD}	109	$RXOUT_4$	131	NC
22	$YPIN_0$	44	$YPIN_{17}$	66	$XRIN_0$	88	$\overline{OERX}$	110	$RXOUT_3$	132	$PYOUT_5$



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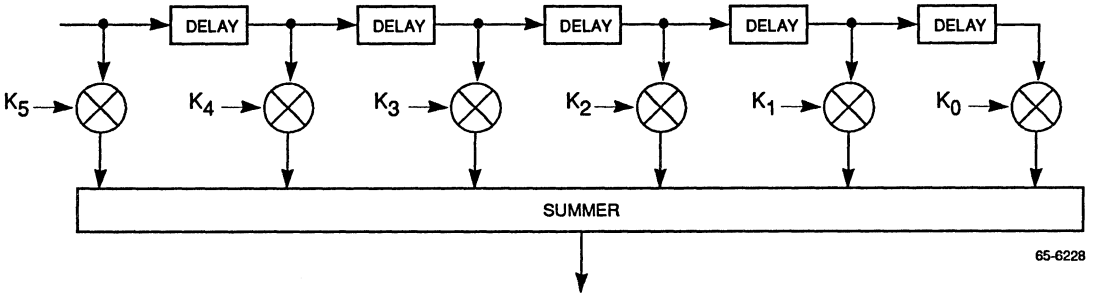
Vector Processing



Vector Processing, also known as Systolic Processing, operates in parallel on an array of data, or on a data stream. Very high processing throughput rates are thus achieved.

Raytheon's vector processors include FIR filters (the TDC1028, TMC2242 and TMC2243), which all operate at video word rates. The TMC2246 Image Filter supports fast pixel manipulation of a 1- or 2-dimensional picture. The TMC2249 is ideal for mixing two digital video streams, while the TMC2250 and TMC2255 perform high speed matrix multiplication and convolution.

Product	Description	Size	Clock Rate[1] (MHz)	Power[1] (Watts)	Package	Grade	Notes
TMC2242-1	Half-Band Digital Filter	2/16 Bit	40	0.5	R2	C	2:1 interpolate or decimate.
-			30	0.5	R2	C	Low-pass (-60 dB @ 0.25 F_s)
TMC2243	Video Filter	10x10x3	20	0.5	G8, H8	C, V	Cascadeable.
TMC2246-1	Image Filter	10x11 bit	40	0.5	H5, L5	C, V	Four-pixel interpolator.
-			30	0.5	H5, L5	C, V	
TMC2249-1	Digital Mixer	12x12x2	30	0.5	H5, L5	C, V	Cascadeable. Programmable delays.
-			25	0.5	H5, L5	C, V	
TMC2250-2	Matrix Multiplier	12x10x9	40	1.2	H5	C	2D convolution 3x3, 2x4.
-1			36	1.2	H5, G1	C, V	1D convolution, 9 taps.
-			30	1.2	H5, G1	C, V	3x3 matrix x 3x1 vector
TMC2255-1	2D Convolver	5x5x8 bit	12.5	0.6	R1	C	3x3, symmetric 5x5 2D convolver.
-			10	0.6	R1	C	

Notes:
1. Guaranteed. See product specifications for test conditions.
2. A = High Reliability, T_C = -55°C to 125°C.
   C = Commercial, T_A = 0°C to 70°C.
   V = MIL-STD-883 compliant, T_C = -55°C to 125°C.

TMC2250
Matrix Multiplier
12 x 12 Bits, 40 MHz

Description

The TMC2250 is a flexible high-performance nine-multiplier array VLSI circuit which can execute a cascadeable 9-tap FIR filter, a cascadeable 4 x 2 or 3 x 3-pixel image convolution, or a 3 x 3 color space conversion. All configurations offer throughput at up to the maximum guaranteed 40 MHz clock rate with 12-bit data and 10-bit coefficients. All inputs and outputs are registered on the rising edges of the clock.

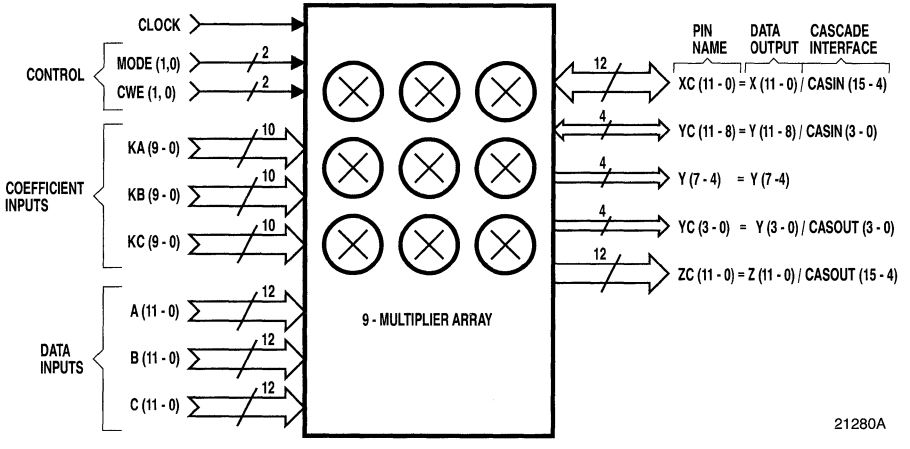
The 3 x 3 matrix multiply or color conversion configuration can perform video standard conversion (YIQ or YUV to RGB, etc.) or three-dimensional perspective translation at real-time video rates.

The 9-tap FIR filter configuration, useful in Video, Telecommunications, and Signal Processing, features a 16-bit cascade input to allow construction of longer filters.

The cascadeable 3 x 3 and 4 x 2-pixel image convolver functions allow the user to perform numerous image processing functions, including static filters and edge detectors. The 16-bit cascade input port facilitates two-chip 40 MHz cubic convolution (4 x 4-pixel kernel).

The TMC2250 is fabricated in a one-micron CMOS process and operates at clock speeds of up to 40 MHz over the full commercial (0°C to 70°C) temperature and supply voltage ranges. It is available in a 121-pin plastic pin grid array (PPGA) package. All input and output signals are TTL compatible.

Logic Symbol



Features

- Four User-Selectable Filtering And Transformation Functions:
  - Triple Dot Product (3 x 3) Matrix Multiply
  - Cascadeable 9-Tap Systolic FIR Filter
  - Cascadeable 3 x 3-Pixel Image Convolver
  - Cascadeable 4 x 2-Pixel Image Convolver
- 40MHz (25ns) Pipelined Throughput
- 12-Bit Input And Output Data, 10-Bit Coefficients
- 16-Bit Cascade Input And Output Ports In All Filter Modes
- Onboard Coefficient Storage, With Three-Cycle Updating Of All Nine Coefficients

Applications

- Image Filtering And Manipulation
- Video Effects Generation
- Video Standards Conversion And Encoding/Decoding
- Three-Dimensional Image Manipulation
- Medical Image Processing
- Edge Detection For Object Recognition
- FIR Filtering For Communications Systems

Functional Description

General Information

The TMC2250 is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product) or cascadeable 9-tap FIR filter, 3 x 3-pixel convolver, or 4 x 2-pixel convolver, all in one monolithic circuit. With a 30MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A, B, C) accept 12-bit two's complement integer data, which is also the format for the output ports (X, Y, Z) in the matrix multiply mode (Mode 00). In the filter configurations (Modes 01, 10, and 11), the cascade ports assume 12-bit integer, 4-bit fractional two's complement data on both input and output. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. ***Table 1*** details the bit weighting of the input and output data in all configurations.

Operating Modes

The TMC2250 can implement four different digital filter architectures. Upon selection of the desired function by the user ($MODE_{1-0}$), the device reconfigures its internal data paths and input and output buses appropriately. The output ports (XC, YC, and ZC) are configured in all filter modes as 16-bit Cascade In and Cascade Out ports so that multiple devices can be connected to build larger filters. These modes are described individually below. The I/O pin-function configurations for all four modes are shown in ***Table 1***.

Definitions

The calculations performed by the TMC2250 in each mode are also shown below, utilizing the following notation:

A(1), B(5), C(2), CASIN(3)	Indicates the data word presented to that input port during the specified clock rising edge (x). Applies to all input ports A_{11-0}, B_{11-0}, C_{11-0}, and $CASIN_{15-0}$.
KA1(1), KB3(4)	Indicates coefficient data stored in the specified one of the nine onboard coefficient registers KA1 through KC3, as shown in the block diagram for that mode, input during or before the specified clock rising edge (x).
X(1), Y(4), Z(6), CASOUT(6)	Indicates data available at that output port t_{DO} after the specified clock rising edge (x). Applies to all output ports X_{11-0}, Y_{11-0}, Z_{11-0}, and $CASOUT_{15-0}$.

Table 1. Data Port Formatting by Mode

	Inputs						Inputs/Outputs		Outputs		
Mode	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	XC_{11-0}	YC_{11-8}	Y_{7-4}	YC_{3-0}	ZC_{11-0}
00	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	X_{11-0}	Y_{11-8}	Y_{7-4}	Y_{3-0}	Z_{11-0}
01	A_{11-0}	A_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
10	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
11	A_{11-0}	B_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$

Numeric Format

Table 2 shows the binary weightings of the input and output ports of the TMC2250. Although the internal sums of products could grow to 23 bits, in the matrix multiply mode (Mode 00) the outputs X, Y, and Z are truncated to yield 12-bit integer words. Thus the output format is identical to the input data format. In the filter configurations (Modes 01, 10, and 11) the cascade output is always half-LSB rounded to 16 bits, specifically 12 integer bits and 4 fractional guard bits, with no overflow "headroom." The user is of course free to half-LSB round the output word to any size less than 16 bits by forcing a 1 into the bit position of the cascade input immediately below the desired LSB. In all modes, bit weighting is easily adjusted if desired by applying the same scaling correction factor to both input and output data words. If the coefficients are rescaled, the relative weightings of the CASIN and CASOUT ports will differ accordingly.

Data Overflow

As shown in *Table 2*, the TMC2250's matched input and output data formats accommodate 0 dB (unity) gain. Therefore, the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific algorithm performed to ensure that no overflow occurs.

Signal Definitions

Power

V_{DD}, GND — The TMC2250 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The TMC2250 operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.

Table 2. Bit Weightings For Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
Inputs																						
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	.									
Coefficients KA, KB, KC												$-K_9$	.	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Modes 01, 10, 11 CASIN	$-CI_{15}$	CI_{14}	CI_{13}	CI_{12}	CI_{11}	CI_{10}	CI_9	CI_8	CI_7	CI_6	CI_5	CI_4	.	CI_3	CI_2	CI_1	CI_0					
Internal Sum	X_{20}	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	.	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Outputs																						
Mode 00 X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	.									
Modes 01, 10, 11 CASOUT	$-CO_{15}$	CO_{14}	CO_{13}	CO_{12}	CO_{11}	CO_{10}	CO_9	CO_8	CO_7	CO_6	CO_5	CO_4	.	CO_3	CO_2	CO_1	CO_0					

Note: 1. A minus sign indicates a two's complement sign bit.

3 x 3 Matrix Multiplier (Mode 00)

This mode utilizes all six input and output ports in the basic configuration to realize a "triple dot product," in which each output is the sum of all three input words in that column multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words half-LSB rounded to 12 bits are then available every clock cycle.

$$X(5) = A(1)KA1(1) + B(1)KB1(1) + C(1)KC1(1)$$
$$Y(5) = A(1)KA2(1) + B(1)KB2(1) + C(1)KC2(1)$$
$$Z(5) = A(1)KA3(1) + B(1)KB3(1) + C(1)KC3(1)$$

Figure 1. 3 x 3 Matrix Multiplier Impulse Response (Mode 00)

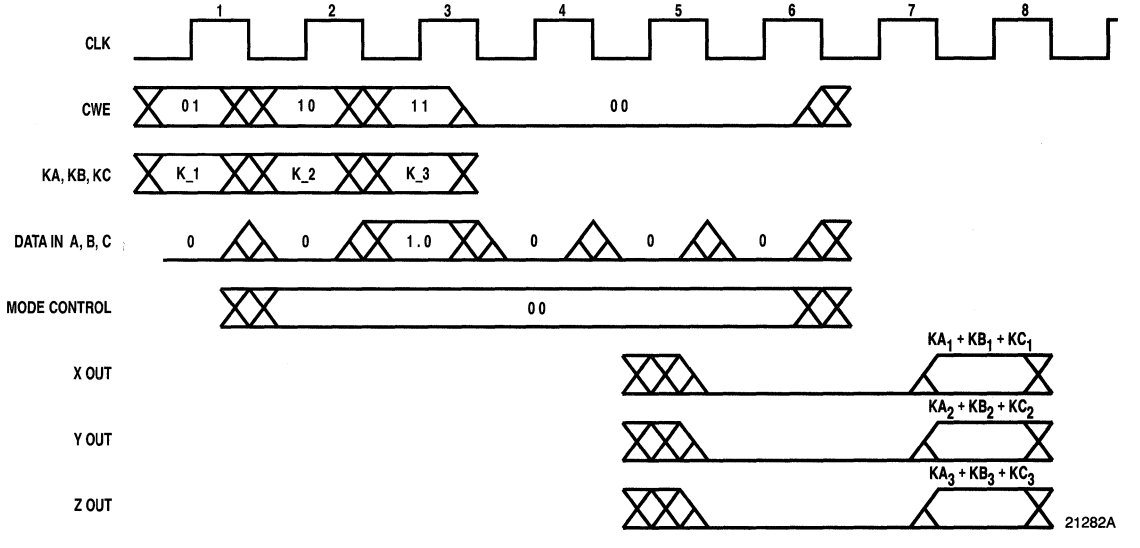
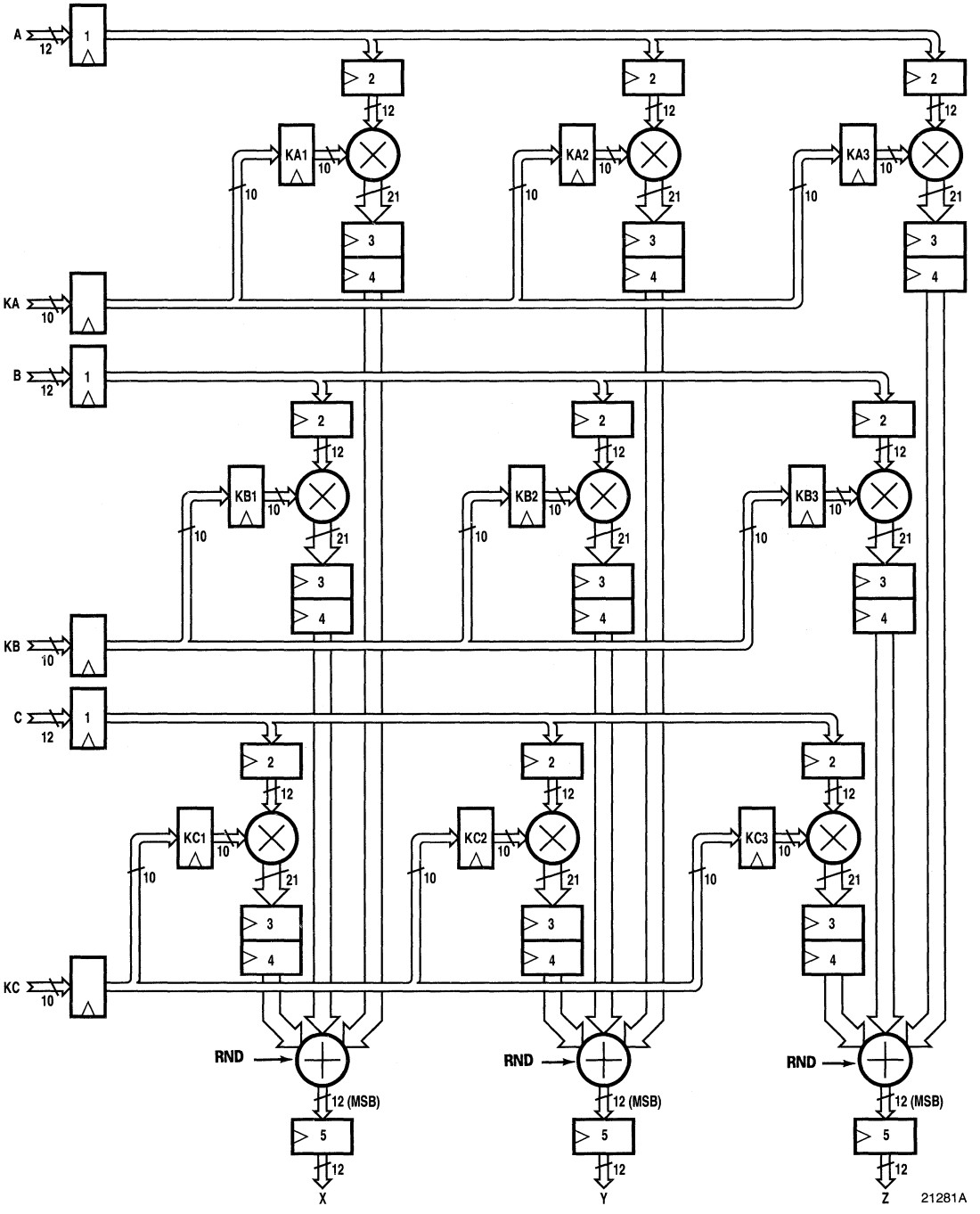


Figure 2. 3 x 3 Matrix Multiplier Configuration (Mode 00)



9-Tap FIR Filter (Mode 01)

The architecture for this configuration is shown in ***Figure 4.*** The user loads the desired coefficient set, presents input data to ports A and B simultaneously (most applications will wire the A and B inputs together), and receives the resulting 9-sample response, half-LSB rounded to 16 bits, 5 to 13 clock cycles later. A new output data word is available every clock cycle. The figure shows that the input data are automatically right-shifted one location through the row of multiplier input registers on every clock in anticipation of a new input data word.

$$\begin{aligned}CASOUT(13) = {} & A(9)KA3(9) + A(8)KA2(8) + A(7)KA1(7) \\ & + B(6)KB3(9) + B(5)KB2(8) + B(4)KB1(7) \\ & + B(3)KC3(9) + B(2)KC2(8) + B(1)KC1(7) \\ & + CASIN(10)\end{aligned}$$

Latency: Impulse in to center of 9-tap response = 9 registers. Cascade In to Cascade Out = 4 registers.

Figure 3. 9-Tap FIR Filter Impulse Response (Mode 01)

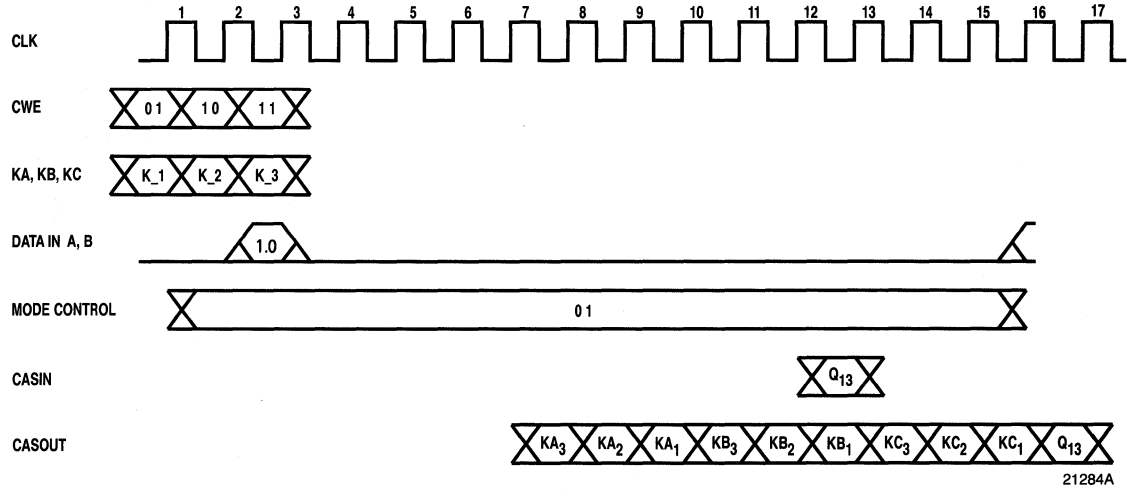
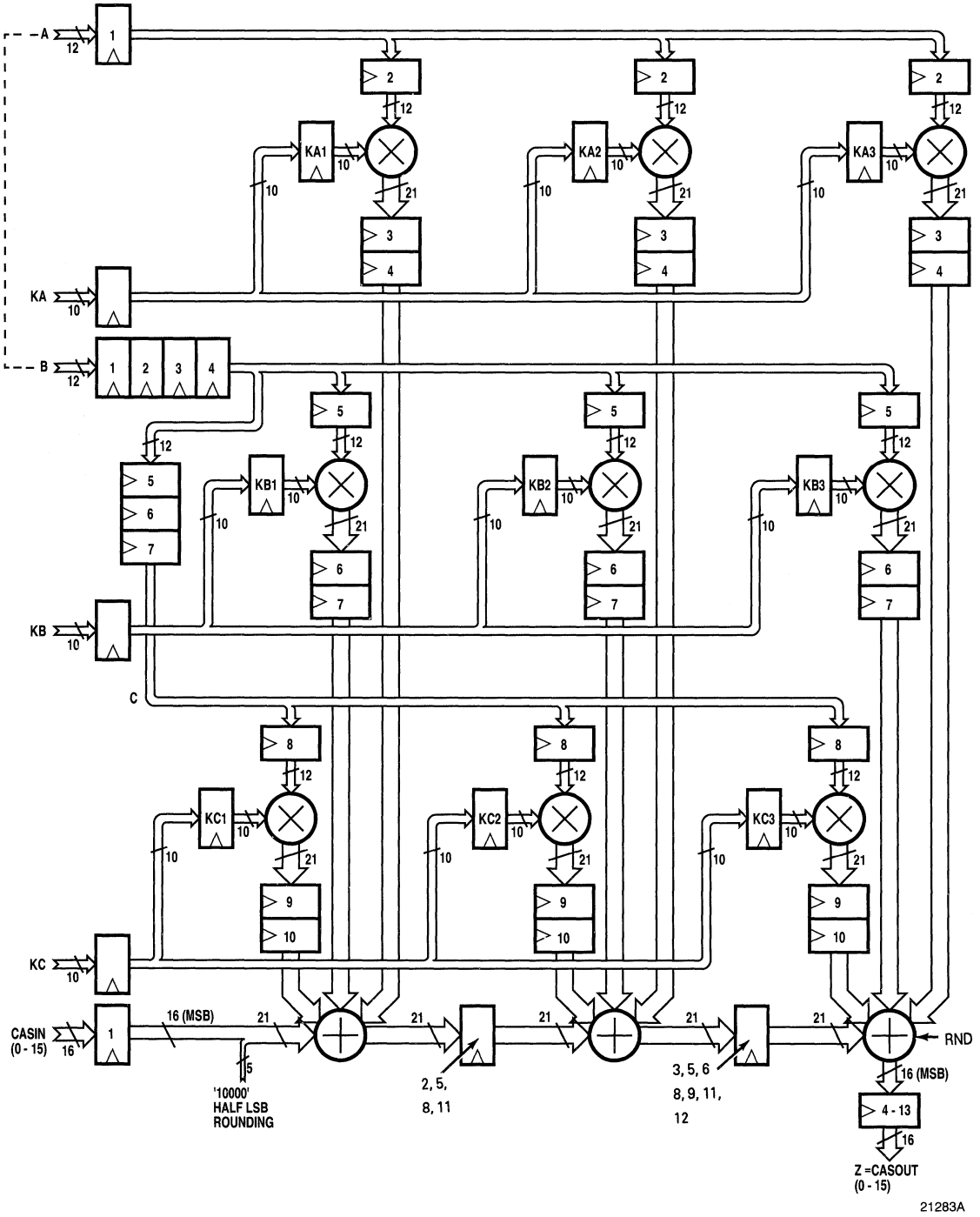


Figure 4. 9-Tap FIR Filter Configuration (Mode 01)



3 x 3-Pixel Convolver (Mode 10)

This filter configuration accepts a 3-pixel-square neighborhood, side-loaded three pixels at a time through input ports A, B, and C, and multiplies the 9 most recent pixel values by the coefficient set currently stored in the registers. These products are summed with the data presented to the cascade input, and a new 3-cycle impulse response, rounded to 16 bits, is available at the output port 5-7 clocks later, with a new output available on every clock cycle. The input pixel data are automatically shifted one location to the right through the three rows of multiplier input registers on every clock in anticipation of three new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned}CASOUT(7) = {} & A(3)KA3(3) + A(2)KA2(2) + A(1)KA1(1) \\ & + B(3)KB3(3) + B(2)KB2(2) + B(1)KB1(1) \\ & + C(3)KC3(3) + C(2)KC2(2) + C(1)KC1(1) \\ & + CASIN(4)\end{aligned}$$

Latency: Impulse in to center of 3-tap response = 6 registers. Cascade In to Cascade Out = 4 registers.

Figure 5. 3 x 3-Pixel Convolver Impulse Response (Mode 10)

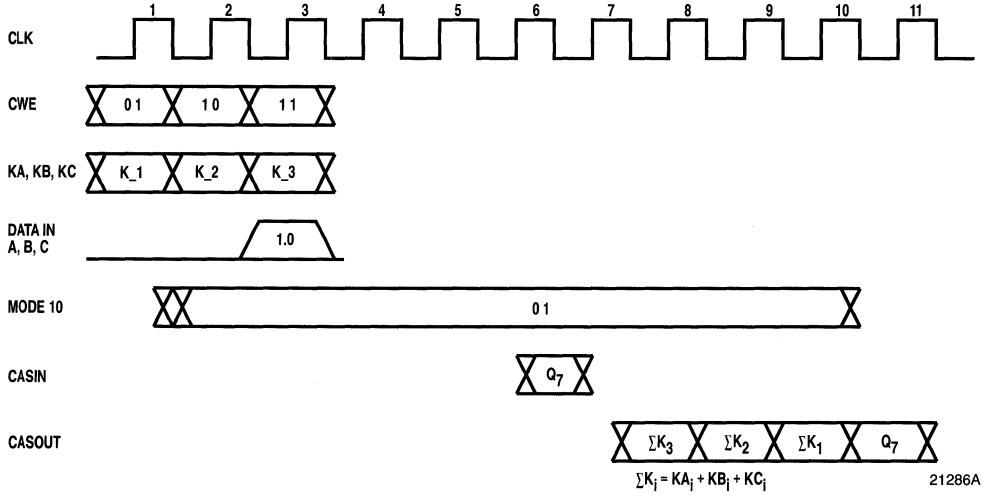
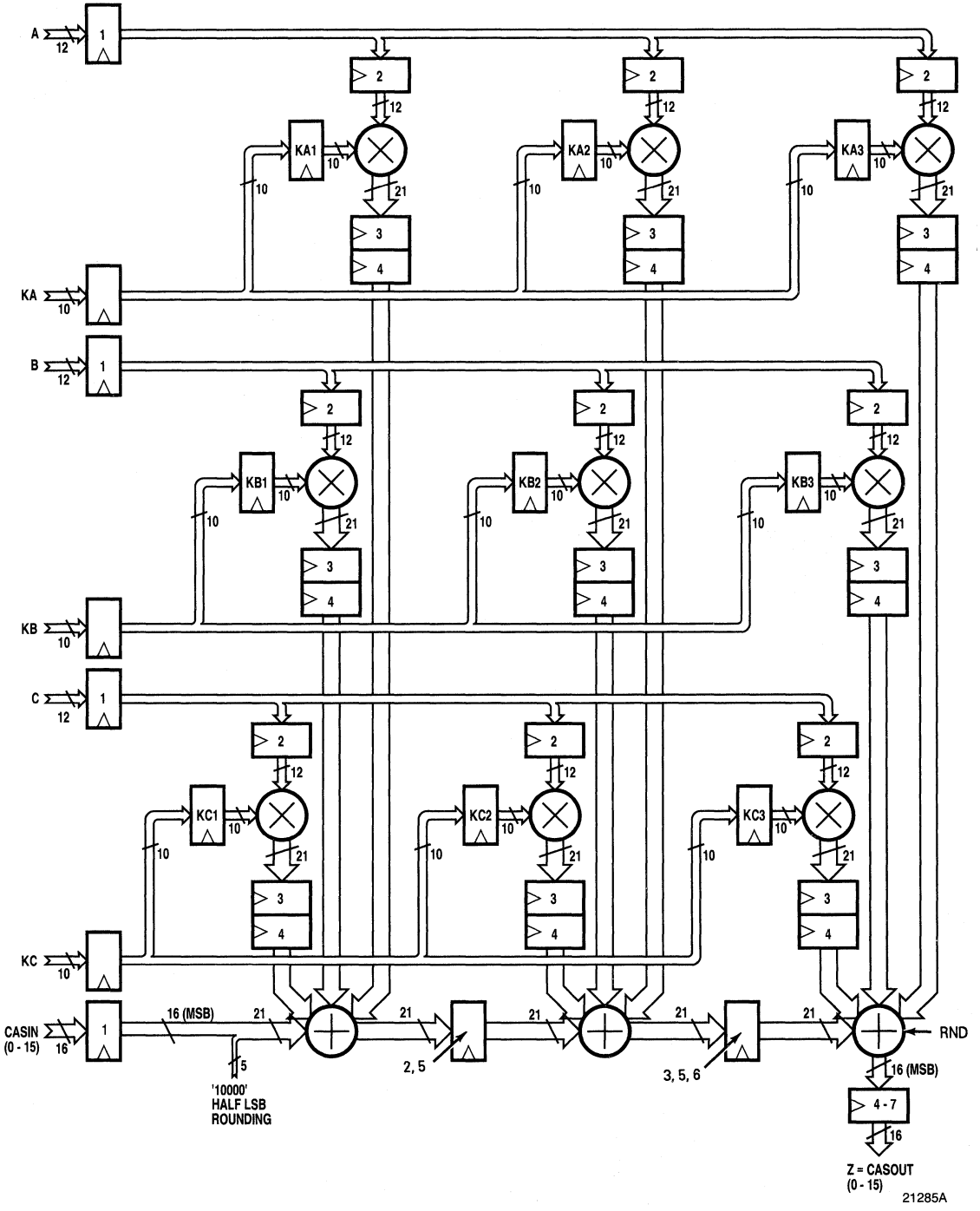


Figure 6. 3 x 3-Pixel Convolver Configuration (Mode 10)



4 x 2-Pixel Cascadeable Convolver (Mode 11)

Similar to Mode 10, the 4 x 2-pixel convolver allows the user to perform full-speed cubic convolution with only two TMC2250 devices and the TMC2111 Pipeline Delay Register to synchronize the cascade ports (see the *Applications Discussion* section). Pixel data are side-loaded into ports A and B, multiplied by the onboard coefficients, summed with the cascade input, and half-LSB rounded to 16 bits. The four-cycle impulse response emerges at the cascade output port 5 to 8 clock cycles later. A new output word is available on every clock cycle. Note that Multiplier KC2 is not used in this mode and that its stored coefficient is ignored. As shown below, the column of input pixel data is automatically shifted one location to the right through the two rows of multiplier input registers on every clock in anticipation of two new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned}\text{CASOUT}(8) = {} & A(4)KA3(4) + A(3)KA2(3) + A(2)KA1(2) \\ & + A(1)KB3(4) + B(4)KB3(4) + B(3)KB2(3) \\ & + B(2)KB1(2) + B(1)KC1(2) + \text{CASIN}(5)\end{aligned}$$

Figure 7. 4 x 2-Pixel Convolver Impulse Response (Mode 11)

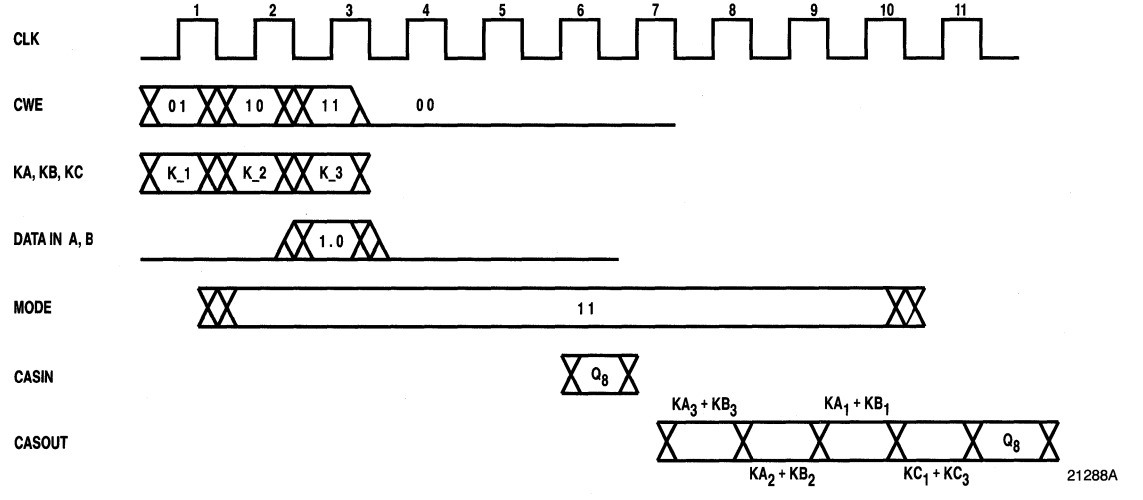
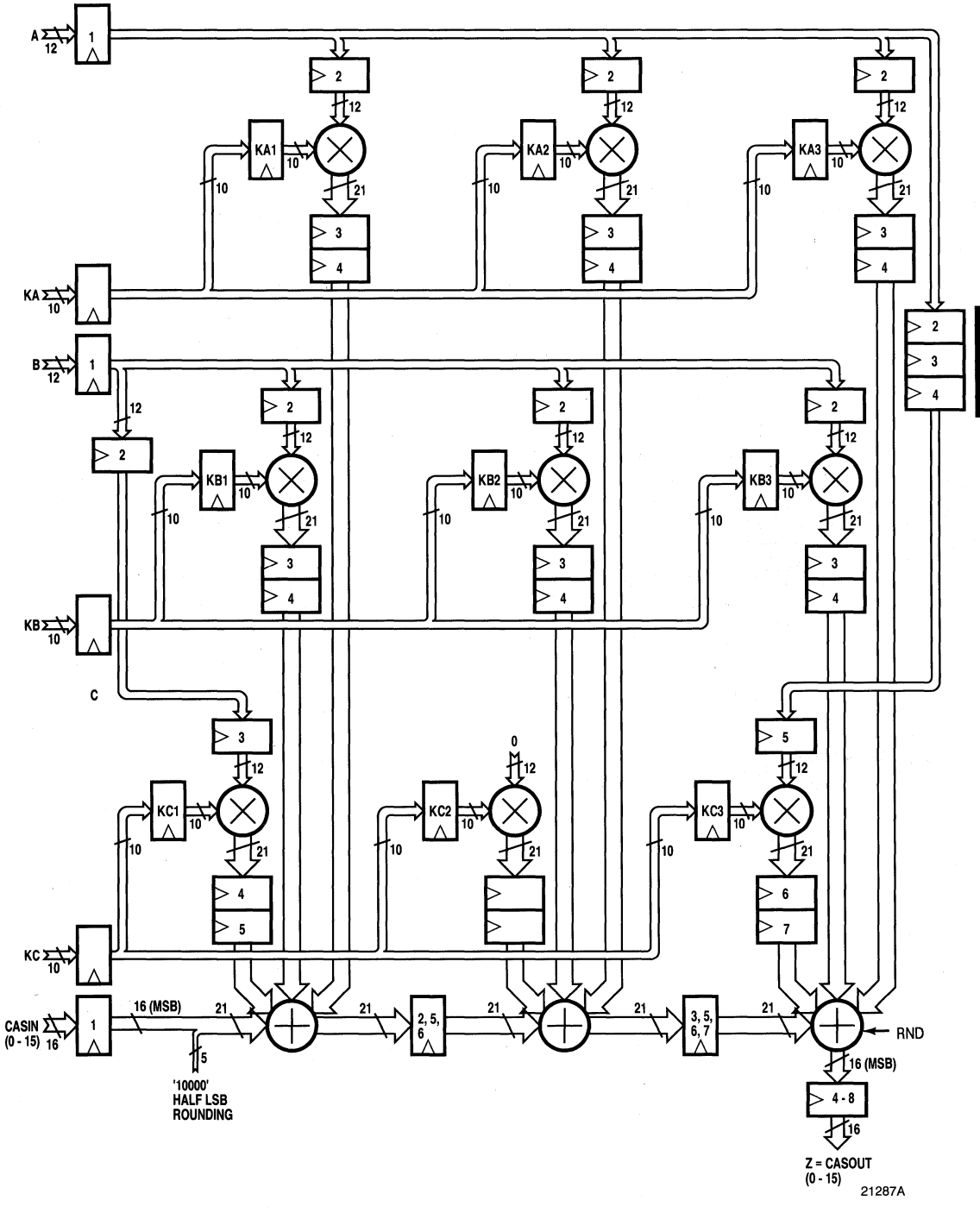


Figure 8. 4 x 2-Pixel Convolver Configuration (Mode 11)



Signal Definitions (cont.)

Controls

$MODE_{1,0}$ The TMC2250 will switch to the configuration selected by the user (as shown in *Table 3*) on the next clock. This registered control is usually static; however, should the user wish to switch between modes, the internal pipeline latencies of the device must be taken into account. Valid data will not be available at the outputs in the new configuration until enough clocks in the new mode have passed to flush the internal registers.

Table 3. Configuration Mode Word

$MODE_{1,0}$	Configuration Mode
00	3 x 3 Matrix Multiply
01	9-Tap One-Dimensional FIR
10	3 x 3-Pixel Convolver
11	4 x 2-Pixel Convolver

$CWE_{1,0}$ Data presented to the coefficient input ports (KA, KB, and KC) will update three of the internal coefficient storage registers, as indicated by the simultaneous Coefficient Write Enable select, on the next clock. See *Table 4* and the *Functional Block Diagram*.

Table 4. Coefficient Write Enable Word

$CWE_{1,0}$	Coefficient Set Selected
00	Hold all registers
01	Update KA1, KB1, KC1
10	Update KA2, KB2, KC2
11	Update KA3, KB3, KC3

Table 5. Coefficient Input Ports

Input Port	Registers Available
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

Inputs And Outputs

A_{11-0}, B_{11-0}, C_{11-0} Data presented to the 10-bit registered data input ports A, B, and C are latched into the multiplier input registers for the currently selected configuration (*Table 3*). In all modes except Mode 00, new data are internally right-shifted to the next filter tap on each rising edge of CLK.

KA_{9-0}, KB_{9-0}, KC_{9-0} Data presented to the 10-bit registered coefficient input ports KA, KB, and KC are latched three at a time into the internal coefficient storage register set indicated by the Coefficient Write Enable $CWE_{1,0}$ on the next clock, as shown in *Table 4*.

$CASIN_{15-0}$ In all modes except Mode 00, the x port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Input port $CASIN_{15-0}$. Data presented to this input will be added to the weighted sums of the data words which were presented to the input ports (A, B, and C).

X_{11-0}, Y_{11-0}, Z_{11-0} In the matrix multiply mode, data are available at the 12-bit registered output ports X, Y, and Z t_{DO} after every clock. These ports are reconfigured in the filtering modes as 16-bit Cascade Input and Output ports.

NOTE: The output ports X, Y, Z and CASOUT, and the input port CASIN are internally reconfigured by the device as required for each mode of the device. The multiple-function pins have names which are combinations of these titles, as appropriate.

$CASOUT_{15-0}$ In all modes except Mode 00, the Z port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Output port $CASOUT_{15-0}$.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8, C4
	GND	Ground	E3, G3, J3, L4, L6, H11, C7, C5
Clock	CLK	System Clock	D11
Controls	$MODE_{1,0}$	Mode Control	B5, A4
	$CWE_{1,0}$	Coefficient Write Enable	J12, J13
Input/Output	A_{11-0}	Data Input A	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12
	B_{11-0}	Data Input B	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12
	C_{11-0}	Data Input C	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9
	KA_{9-0}	Coefficient Input A1, A2, A3	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13
	KB_{9-0}	Coefficient Input B1, B2, B3	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8
	KC_{9-0}	Coefficient Input C1, C2, C3	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5
	XC_{11-0}	$CASIN_{15-4}$/Output X	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2
	YC_{11-8}	$CASIN_{3-0}$/Output Y_{11-0}	D1, E2, E1, F2
	Y_{7-4}	Output Y_{7-4} Only	F1, G2, G1, H1
	YC_{3-0}	$CASOUT_{3-0}$/Output Y_{3-0}	K1, J2, J1, H2
	ZC_{11-0}	$CASOUT_{15-4}$/Output Z_{11-0}	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2

Vector

Figure 9. Input/Output Timing Diagram

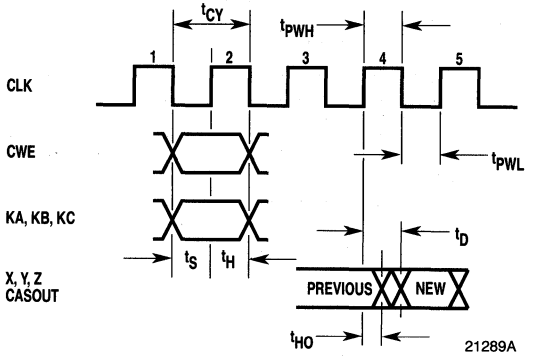


Figure 10. Equivalent Input Circuit

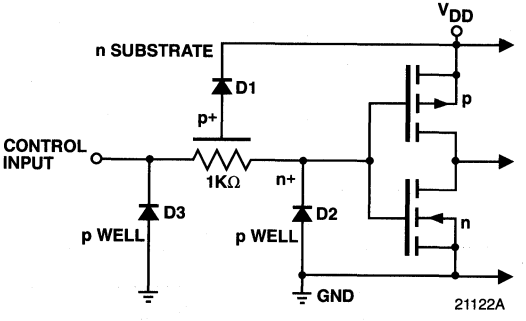
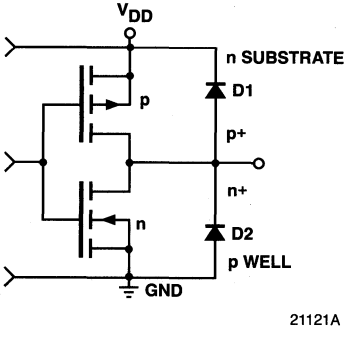


Figure 11. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+5.0)V

Output

Applied voltage ..... −0.5 to (V_{DD}+5.0)V [2]

Forced current ..... −6.0 to 6.0mA [3,4]

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

		Temperature Range						
		Standard			Extended			
Parameter		Min	Nom	Max	Min	Nom	Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
	CLK Only			0.8			0.6	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
t_{CY}	Cycle Time							
	TMC2250	33			33			ns
	TMC2250-1	27.7			27.7			ns
	TMC2250-2	25						ns
t_{PWL}	Clock Pulse Width, LOW							
	TMC2250	15			15			ns
	TMC2250-1	12			12			ns
	TMC2250-2	10						ns
t_{PWH}	Clock Pulse Width, HIGH	10			10			ns
t_S	Input Setup Time							
	TMC2250	8			8			ns
	TMC2250-1	7			7			ns
	TMC2250-2	6						ns
t_H	Input Hold Time							
	TMC2250	3			3			ns
	TMC2250-1	3			3			ns
	TMC2250-2	2						ns
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		12		12	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=20MHz		160		160	mA
I_{IL}	Input Current, Logic LOW [2]	V_{DD}=Max, V_{IN}=0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH [2]	V_{DD}=Max, V_{IN}=V_{DD}		10		10	μA
I_{OIL}	Input Current, Logic LOW [3]	V_{DD}=Max, V_{IN}=0V		−40		−40	μA
I_{OIH}	Input Current, Logic HIGH [3]	V_{DD}=Max, V_{IN}=V_{DD}		40		40	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=−2mA	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to to ground, one second duration max.	−20	−80	−20	−80	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10		10	pF

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Except pins XC_{11-0}, YC_{11-8}.
3. Pins XC_{11-0}, YC_{11-8} only.

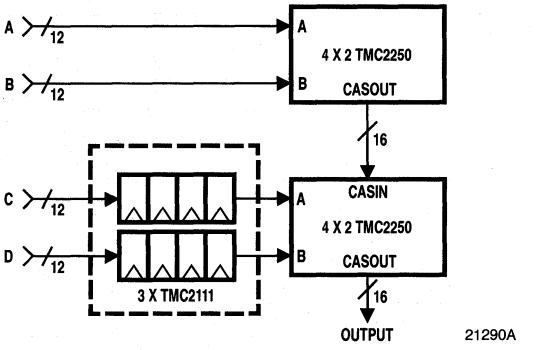
Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD}=Min, C_{LOAD}=25pF					
	TMC2250			18		20	ns
	TMC2250-1			17		18	ns
	TMC2250-2			16			ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=25pF					
	TMC2250		3		3		ns
	TMC2250-1		3		3		ns
	TMC2250-2		3		3		ns

Performing Large-Kernel Pixel Interpolation

The Cascade Input and Output Ports of the TMC2250 allow the user to stack multiple devices to perform larger interpolation kernels with no decrease in pixel throughput. *Figure 12* illustrates a basic application utilizing Mode 11 to realize a 4 x 4-pixel kernel, also called Cubic Convolution. This example utilizes the TMC2011 Variable-Length Shift Register to compensate for the internal latency of each TMC2250. Alternatively, some applications may utilize RAM, FIFOs, or other methods to store multiple-line pixel data. In these cases the user may compensate for latency by simply offsetting the access sequencing of the storage devices.

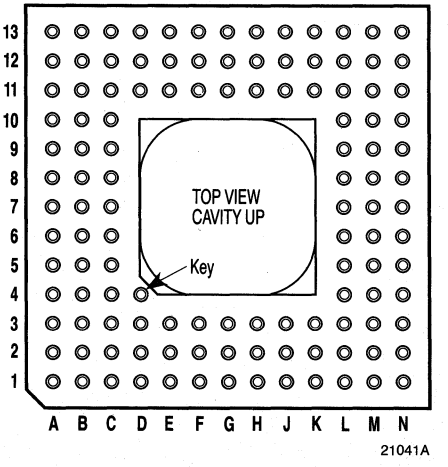
Figure 12. Performing Cubic Convolution with Two TMC2250s



Pin Assignments – 121 Pin Plastic (H5) or Ceramic (G1) Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	XC_7	B3	XC_8	C5	GND	E1	YC_9	G11	A_3	K1	YC_3	L10	KB_8	M12	KA_2
A2	XC_9	B4	XC_{11}	C6	C_{10}	E2	YC_{10}	G12	A_2	K2	ZC_0	L11	KA_1	M13	KA_3
A3	XC_{10}	B5	$MODE_1$	C7	GND	E3	GND	G13	A_4	K3	ZC_3	L12	KA_5	N1	ZC_5
A4	$MODE_0$	B6	C_9	C8	V_{DD}	E11	A_{11}	H1	Y_4	K11	KA_4	L13	KA_6	N2	ZC_8
A5	C_{11}	B7	C_6	C9	C_0	E12	A_9	H2	YC_0	K12	KA_7	M1	ZC_2	N3	ZC_{10}
A6	C_8	B8	C_4	C10	B_8	E13	A_8	H3	V_{DD}	K13	KA_9	M2	ZC_7	N4	KC_1
A7	C_7	B9	C_2	C11	B_5	F1	Y_7	H11	GND	L1	ZC_1	M3	ZC_9	N5	KC_3
A8	C_5	B10	B_{11}	C12	B_3	F2	YC_8	H12	A_0	L2	ZC_4	M4	ZC_{11}	N6	KC_5
A9	C_3	B11	B_9	C13	B_1	F3	V_{DD}	H13	A_1	L3	ZC_6	M5	KC_2	N7	KC_7
A10	C_1	B12	B_6	D1	YC_{11}	F11	A_7	J1	YC_1	L4	GND	M6	KC_4	N8	KC_8
A11	B_{10}	B13	B_2	D2	XC_0	F12	A_6	J2	YC_2	L5	KC_0	M7	KC_6	N9	KB_1
A12	B_7	C1	XC_1	D3	XC_3	F13	A_5	J3	GND	L6	GND	M8	KC_9	N10	KB_3
A13	B_4	C2	XC_2	D11	CLK	G1	Y_5	J11	KA_8	L7	V_{DD}	M9	KB_2	N11	KB_6
B1	XC_4	C3	XC_6	D12	B_0	G2	Y_6	J12	CWE_1	L8	KB_0	M10	KB_5	N12	KB_7
B2	XC_5	C4	V_{DD}	D13	A_{10}	G3	GND	J13	CWE_0	L9	KB_4	M11	KB_9	N13	KA_0

D4 Index Pin (Unconnected)

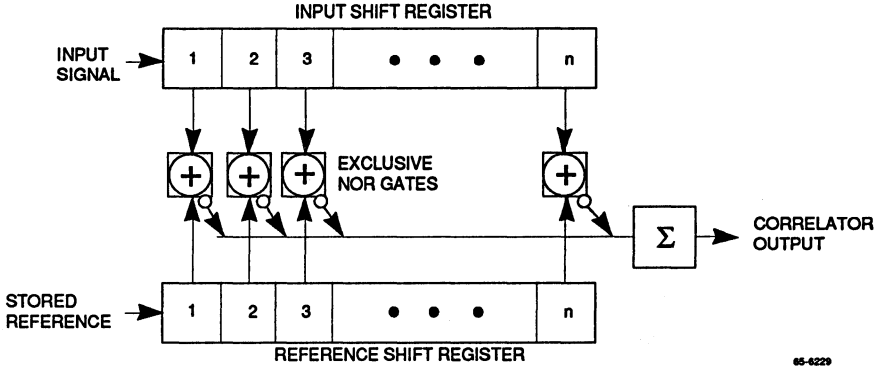


Ordering Information

Product Number	Speed (MHz)	Temperature Range	Screening	Package	Package Marking
TMC2250H5C	30	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C
TMC2250H5C 1	36	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C 1
TMC2250H5C 2	40	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C 2
TMC2250G1V	30	MIL – T_C = –55°C to 125°C	MIL-STD-883	121 Pin Ceramic Pin Grid Array	2250G1V
TMC2250G1V1	36	MIL – T_C = –55°C to 125°C	MIL-STD-883	121 Pin Ceramic Pin Grid Array	2250G1V1

40G06391 Rev B 8/93

Correlators



Raytheon is the industry leader in correlators for high performance communications, signal, radar and image processing applications. Correlators measure the similarity between two digital signal streams, which is key to pattern recognition and data synchronization applications. All Raytheon correlators are TTL compatible.

Product	Description	Size	Clock Rate[1] (MHz)	Power[1] (Watts)	Package	Grade	Notes
TMC2023-1	Correlator	64x1	50	0.4	B2, B7, C3	C, V, SMD	Pin compatible with TDC1023.
			35	0.4	B2, B7, C3	C, V, SMD	Threshold flag.
			25	0.4	B2, B7	C, V, SMD	
TMC2220-1	Correlator	4x32	20	0.3	G8, H8	C, V	Programmable.
			17	0.3	G8, H8	C, V	Optional I&Q modes.
TMC2221-1	Correlator	1x128	20	0.3	B6	C, V	Programmable.
			17	0.3	B6	C, V	

Notes:
1. Guaranteed. See product specifications for test conditions.
2. C = Commercial, T_A = 0°C to 70°C.
   V = MIL-STD-883 Compliant, T_C = -55°C to 125°C.
   SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C.

TMC2023
CMOS Digital Output Correlator
64-Bit, 25, 30, 35, and 50 MHz

Description

The TMC2023 is a monolithic 64-bit correlator with a 7-bit three-state buffered digital output. This device consists of three 64-bit independently clocked shift registers, one 64-bit reference holding latch, and a 64-bit independently clocked digital summing network. The device is available in versions capable of 25, 30, 35, and 50 MHz parallel correlation rates.

The 7-bit threshold register allows the user to preload a binary number from 0 to 64. Whenever the correlation is equal to or greater than the number in the threshold register, the threshold flag goes HIGH.

The 64-bit shift mask register (M register) allows the user to mask or selectively choose "no compare" bit positions enabling total word length flexibility.

The reference word is serially shifted into the B register. Bringing LDR HIGH parallel loads the data into the R reference latch. This allows the user to serially preload a new reference word into the B register while correlation is taking place between the A register and the R latch. The two words are continually compared bit-by-bit by exclusive-OR circuits. Each exclusive-OR provides one bit to the digital summer. The output is a 7-bit word representing the number of positions which agree at any one time between the A register and R latch. A control provides either true or inverted binary output formats.

Built with Raytheon Semiconductor La Jolla's one-micron double level metal OMICRONC™ low power CMOS process, the TMC2023 is available in a 24-pin CERDIP package and 28-contact chip carrier. The CMOS TMC2023 is pin compatible with the bipolar TDC1023.

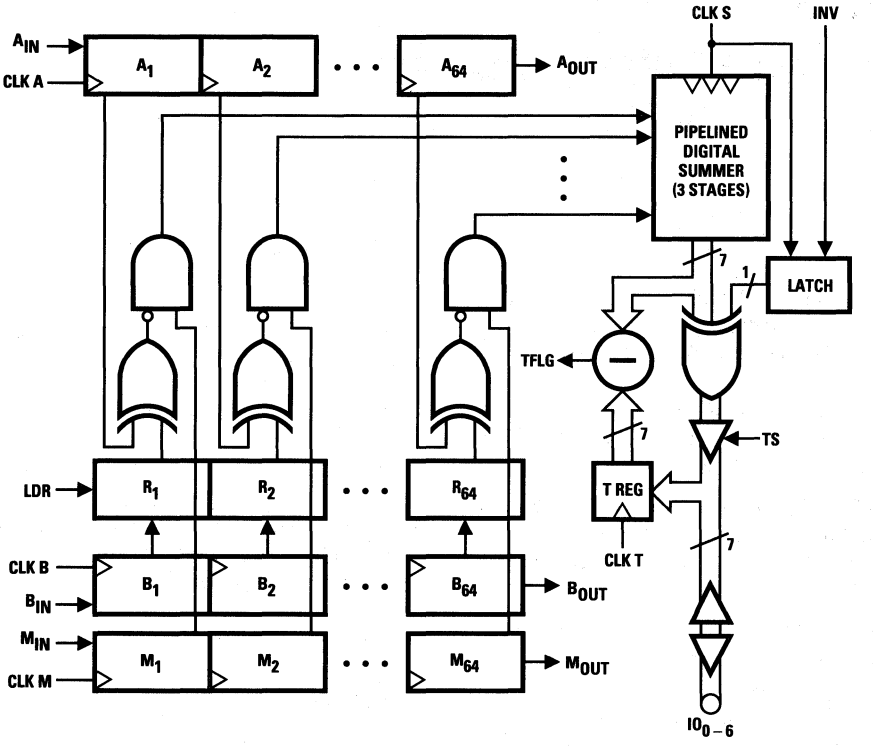
Features

- 25, 30, 35, and 50 MHz correlation rates
- All inputs and outputs TTL compatible
- Serial data input, parallel correlation output
- Programmable word length
- Independently clocked registers
- Programmable threshold detection and flag output
- Available in 24-pin CERDIP and 28-contact chip carrier
- Available to Standard Military Drawing (SMD)
- Pin-Compatible with TDC1023
- Output format flexibility
- Three-state outputs
- Low-power CMOS

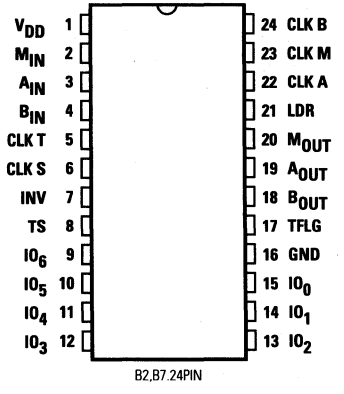
Applications

- Check sorting equipment
- High density recording
- Bar code identification
- Radar signature recognition
- Video frame synchronization
- Electro-optical navigation
- Pattern and character recognition
- Cross-correlation control systems
- Error correction coding
- Asynchronous communication
- Matched filtering

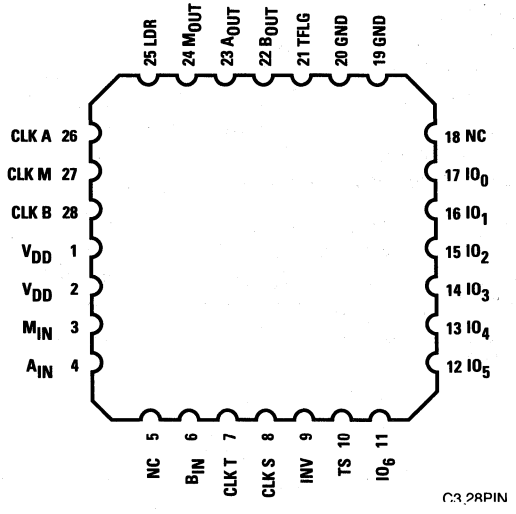
Functional Block Diagram



Pin Assignments



24 Pin CERDIP - B2, B7 Package



28 Contact Chip Carrier - C3 Package

Functional Description

General Information

The TMC2023 consists of an input section and an output section. The input section contains the A, B, and M registers, an R latch, XOR/AND logic and a pipelined summer network. The output section consists of threshold, inversion and three-state logic.

Continuous Correlation

The TMC2023 contains three 1 x 64 serial shift registers (A, B, and M). The operation of these registers is identical and each has its own input, output, and clock. As shown in the Timing Diagrams, valid data is loaded into register A (B, M) on the rising edge of CLK A (CLK B, CLK M). Data is valid if present at the input for a setup time of at least t_{SSR} before and a hold time of t_H after the rising clock edge.

The summing process is initiated when the comparison result between the A register and R latch is clocked into the summing network by a rising edge of CLK S. Typically, CLK A and CLK S are tied together so that a new correlation score is computed for each new alignment of the A register and R latch. When LDR goes HIGH, the contents of register B are copied into the R latch. With LDR LOW, a new template may be entered serially into register B, while parallel correlation takes place between register A and the R latch. In the case of continuous correlation, LDR is held HIGH so that the R latch contents continuously track those of the B register.

The summing network consists of three pipelined stages. Therefore, the total correlation score for a given set of A and B register contents appears at the summer output three CLK S cycles later. Data on the output pins IO_{0-6} is available after an additional propagation delay, denoted t_{DCOR} on the Timing Diagrams.

The correlation result is compared with the contents of the threshold register. TFLG goes HIGH if the correlation equals or exceeds the threshold value. TFLG is valid after a delay of t_{DF} from the third CLK S rising edge.

Cross-Correlation

When LDR goes HIGH, the B register contents are copied into the reference latch (R latch). This useful feature allows correlation to take place between data in the R latch and the A register while a new reference is being serially clocked into the B register. If the new reference is n bits long, it requires n rising edges of CLK to load this data into the B register. For the timing diagram, n = 64. LDR is set HIGH during the final (n^{th}) CLK B cycle, so that the new reference word is copied into the R latch. The minimum LOW and HIGH level pulse widths for LDR are shown as t_{PWL} and t_{PWH}, respectively.

After the new reference is loaded, the data to be correlated is clocked through the A register. Typically, CLK A and CLK S can be tied together. This allows a new correlation score to be computed for each shift of the A register data relative to the fixed reference word in the R latch. The digital summer is internally partitioned into three pipelined stages. Therefore, a correlation score for a particular alignment of the A register data and the R latch reference appears at the summer output three CLK S cycles later. After an additional output delay of t_{DCOR}, the correlation data is valid at the output pins (IO_{0-6}). If this correlation result is equal to or exceeds the value in the threshold register, then TFLG goes HIGH. TFLG is valid t_{DF} after the third rising edge of CLK S.

Threshold Register Load

The timing sequence for loading the threshold (T) register is shown in the Timing Diagrams. The T register holds the 7-bit threshold value to be compared with each correlation result. The rising edge of CLK T loads the data present on the IO_{0-6} pins into the T register. T flag logic is pipelined 3 stages, with the summer. The new value loaded into the threshold register will affect the TFLG on the third CLK S (plus an output delay t_{DF}) following the T register load.

The output buffers must be in a high-impedance state (disabled) when the T register is programmed from an external source. After a delay of t_{DIS} from the time TS goes HIGH, the output buffers are disabled. The data pins IO_{0-6} may then be driven externally with the new threshold data. The data must be present for a setup time of t_{SCOR} before and t_H after the rising edge of CLK T for correct operation. The minimum LOW and HIGH level pulse widths for CLK T are shown below as t_{PWL} and t_{PWH}, respectively.

After TS is set LOW, there is an enable delay of t_{ENA} before the internal correlation data is available at pins IO_{0-6}.

Invert Control Timing

Most applications will tie the INVert control HIGH or LOW depending on system requirements. In the few situations in which the control is used dynamically, the user must observe special timing constraints.

Because INVERT governs logic located between the master and slave latches of the data output register, its setup and hold requirements differ from those of the data and other controls. The device will respond to changes on INV whenever CLOCK is HIGH and will ignore it when CLOCK is LOW. To minimize the data output delay and to avoid inducing errors, the user should observe the following timing constraints:

1. Set INVERT to the desired state for the next output on or before the rising edge of CLOCK. If INVERT is asserted a few nanoseconds after the rising edge, the data output may be similarly delayed.
2. More importantly, keep INVERT in the desired state until after the falling edge of CLOCK, to avoid corrupting the output data. If INVERT is changed several nanoseconds before the falling edge of CLOCK, the data will likewise change. If it is changed just before the falling edge, an indeterminate output may result.

Mask Register

In addition to the A and B shift references, the TMC2023 has another independently clocked register: the M, or mask register. The M register functions identically to the A and B register, except that its parallel outputs are ANDed with the exclusive-ORed outputs from the A register and R latch.

Many uses of the TMC2023 digital correlator require disabling the correlation between certain bit positions (A_i and R_i) of input words A and R. While correlation data is being clocked into the A and/or B register, a mask word may be entered into the M register. Where no comparison is to be made, zeroes are entered in those M register positions. The exclusive-OR result between each bit position is ANDed with a bit from the M register. Thus, if a particular mask bit (M_i) is zero, the output correlation between A and B for that bit position will be disabled. Consequently, a zero correlation is presented to the digital summer for each masked bit position.

The Mask register is useful for changing correlation word length and location within the registers. Where a word is undefined or no correlation is to take place, the M register should contain zeroes.

The M register is useful for building logic functions. Note that for each bit A_i and R_i, the correlation logic is:

$A_i + R_i \quad A_i \overline{R_i} + \overline{A_i} R_i$ (A_i exclusive-OR R_i)

This result is complemented at the input of the AND gates and ANDed with the mask bit (M_i) resulting in:

$$\overline{[A_i \overline{R_i} + \overline{A_i} R_i]} * M_i$$

The last step, performed in the digital summer, is to sum the above result over all bit positions simultaneously for a correlation at time n:

$$C(n+3) = \sum_{i=n-63}^{n} [(A_i \text{ XNOR } B_i) \text{ AND } M_i]$$

where i = 1, 2, 3... and n = correlation word length

Signal Definitions

Power

V_{DD}, GND	The TMC2023 operates from a single +5V supply. All V_{DD} and GND pins must be connected.

Control

INV	Control that inverts the 7-bit digital output. When a HIGH level is applied to this pin, the outputs IO_{0-6} are logically inverted. See the Timing Diagrams for setup and hold requirements.
TS	The three-state control enables and disables the output buffers. A HIGH level applied to this pin forces outputs into the high-impedance state. This control also allows loading of the internal threshold register.
LDR	Control that allows parallel data to be loaded from the B register into the reference latch for correlation. If LDR is held HIGH, the R latch is transparent.

Clocks

CLK A, CLK M, CLK B	Input clocks. Clock input pins for the A, M, and B registers, respectively. Each register may be independently clocked.
CLK T	Threshold register clock. Clock input used to load the T register.

CLK S — Digital summer clock. Clock input that allows independent clocking of the pipelined summer network.

Data Inputs

M_{IN} — Mask register input. Allows the user to choose "no-compare" bit positions. A "0" in any bit location will result in a no-compare state for that location (bit position masked).

A_{IN}, B_{IN} — Shift register inputs to the A and B 64-bit serial registers.

Data Outputs

IO_{0-6} — Bi-directional data pins. When outputs are enabled (TS LOW), data is a 7-bit binary representation of the correlation between the unmasked portions of the R latch and the A register. IO_6 is the MSB. These pins also serve as parallel inputs to load the threshold register. Data present one setup time before CLK T goes HIGH will be latched into the threshold register.

TFLG — The TFLG output goes HIGH whenever the correlation score is equal to or greater than the number loaded into the T register (0 to 64).

B_{OUT} — Shift register outputs of the three 64-bit shift register:

A_{OUT} — B, A, and M, respectively. These outputs may be used to

M_{OUT} — For cascading multiple devices.

No Connect

NC — These pins should be left unconnected.

Package Interconnections

Signal Type	Signal Name	Function	B2, B7 Package	C3 Package
Power	GND	Ground	16	19, 20
	V_{DD}	Supply Voltage	1	1, 2
Control	INV	Inverter Output	7	9
	TS	Three-State Enable	8	10
	LDR	Load Reference	21	25
Clocks	CLK A	A Register Clock	22	26
	CLK M	M Register Clock	23	27
	CLK B	B Register Clock	24	28
	CLK T	Threshold Register	5	7
	CLK S	Digital Summer Clock	6	8
Inputs	M_{IN}	Mask Register	2	3
	A_{IN}	Shift Register	3	4
	B_{IN}	Shift Register	4	6
Outputs	IO_{6-0}	Correlation Score	9,10,11,12, 13,14,15	11,12,13,14, 15,16,17
	TFLG	Threshold Flag	17	21
	B_{OUT}	Shift Register B	18	22
	A_{OUT}	Shift Register A	19	23
	M_{OUT}	Shift Register M	20	24
No Connect	NC	No Connect	None	5, 18

Figure 1. Continuous Correlation

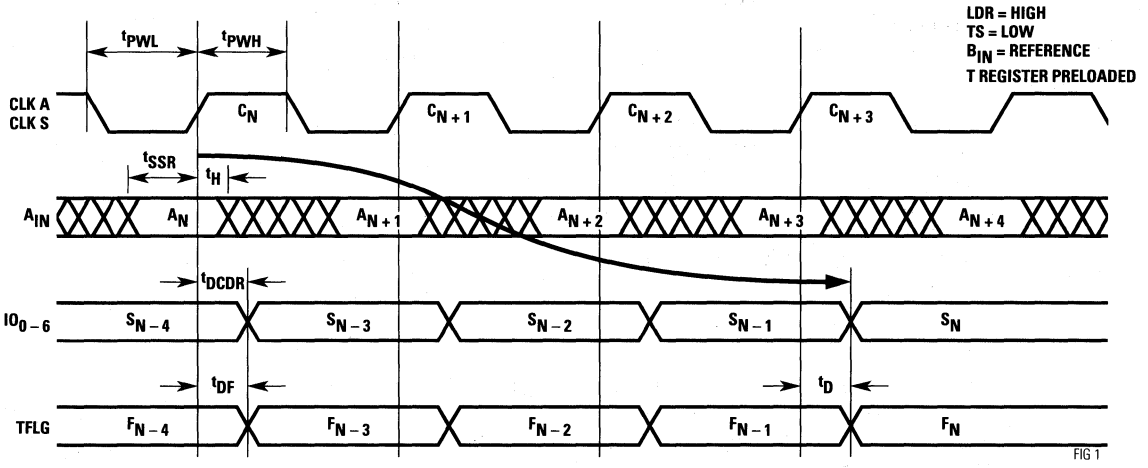


FIG 1

Figure 2. Cross-Correlation

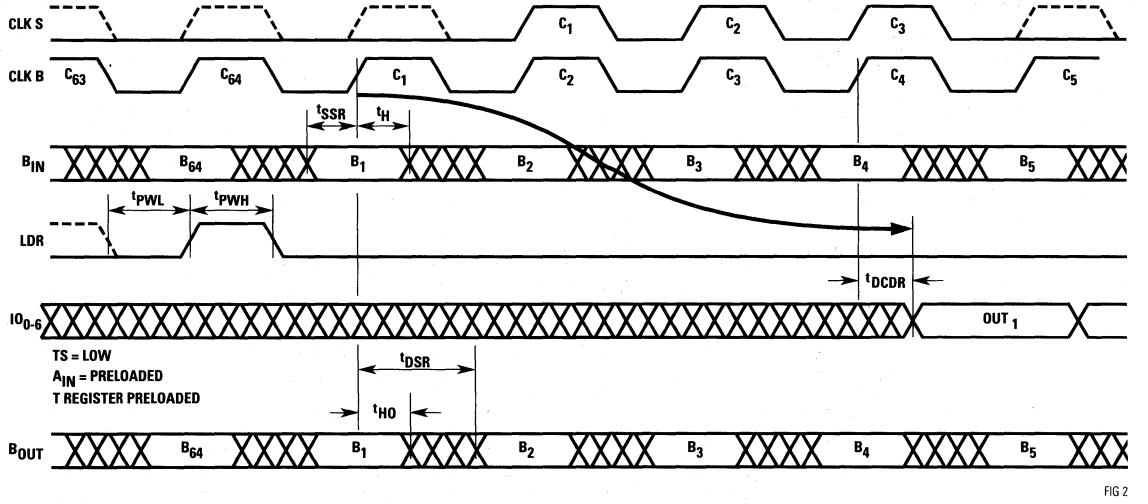


FIG 2

Figure 3. Threshold Register Loading

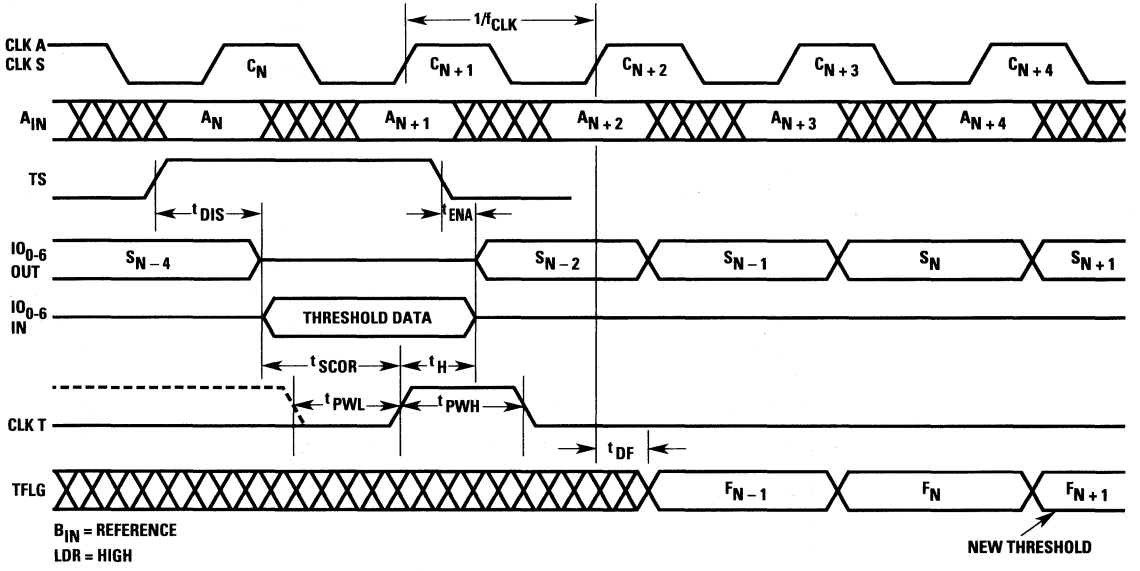


Figure 4. Invert Control Timing

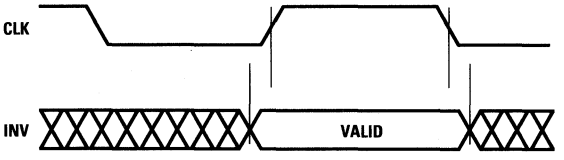


Figure 5. Equivalent Input Circuit

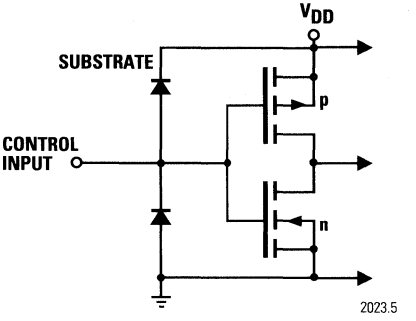


Figure 6. Equivalent Output Circuit

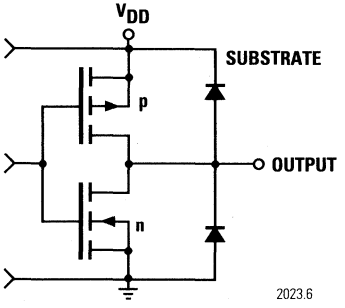
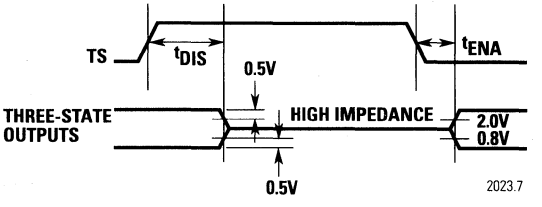


Figure 7. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged)[1]

Power Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD}+0.5) V
Outputs	
Applied Voltage[2]	−0.5 to (V_{DD}+0.5) V
Forced Current[3,4]	−3.0 to 6.0 mA
Short Circuit Duration (Single output in HIGH state to GND)	1 second
Temperature	
Operating, case	−60 to +130°C
Operating, Junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	Volts
t_{PWL}	Clock Pulse Width, LOW							
	TMC2023	15			15			ns
	TMC2023-1, -2	12			14			ns
	TMC2023-3	8			10			ns
t_{PWH}	Clock Pulse Width, HIGH							
	TMC2023	15			15			ns
	TMC2023-1, -2	12			14			ns
	TMC2023-3	8			8			ns
t_{SCOR}	Data Setup Time, Correlator							
	TMC2023	12			14			ns
	TMC2023-1, -2	10			10			ns
	TMC2023-3	9			10			ns
t_{SSR}	Data Setup Time, Shift Register (A_{IN}, B_{IN}, M_{IN})							
	TMC2023	12			13			ns
	TMC2023-1, -2	8			10			ns
	TMC2023-3	7			9			ns
t_H	Data Input Hold Time, Correlator and Shift Register							
	All grades	0			0			ns
f_{CLK}	CLK Frequency, Correlator, Shift Register and Flag Sections							
	TMC2023			25			25	MHz
	TMC2023-1			30			30	MHz
	TMC2023-2			35			35	MHz
	TMC2023-3			50			50	MHz
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
V_{IHC}	Input Voltage, Logic HIGH, A,B,M,S CLKS	2.0			2.4			V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
I_{OH}	Output Current, Logic HIGH			-2.0			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

Electrical Characteristics

Parameter		Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, V_{IN} = LOW, TS = HIGH		5		10	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, TS = HIGH					
		TMC2023, f_{CLK} = 25 MHz		55		55	mA
		TMC2023-1, f_{CLK} = 30 MHz		75		75	mA
		TMC2023-2. f_{CLK} = 35 MHz		75		75	mA
		TMC2023-3, f_{CLK} = 50 MHz		100		100	mA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+10		+10	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		-10		-10	µA
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
I_{OZH}	Output Leakage Current, HIGH[1]	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	µA
I_{OZL}	Output Leakage Current, LOW[1]	V_{DD} = Max, V_{IN} = GND		-40		-40	µA
I_{OS}	Short Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration		-100		-100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1 MHz		10		10	pF

Note: 1. These values are the I_{IL} and I_{IH} for the T Register.

Switching Characteristics

Parameter		Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{DCOR}	Output Delay, Correlator	V_{DD} = Min, C_{LOAD} = 40 pF					
	TMC2023			22		22	ns
	TMC2023-1, -2			19		20	ns
	TMC2023-3			17		18	ns
t_{DSR}	Output Delay, shift Register	V_{DD} = Min, C_{LOAD} = 40 pF					
	TMC2023			22		25	ns
	TMC2023-1, -2			20		22	ns
	TMC2023-3			18		20	ns
t_{DF}	Output Delay, Flags	V_{DD} = Min, C_{LOAD} = 40 pF					
	TMC2023			20		22	ns
	TMC2023-1, -2			17		19	ns
	TMC2023-3			15		17	ns
t_{HO}	Output Hold Time	V_{DD} = Min, C_{LOAD} = 40 pF					
	All grades			4		4	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40 pF					
	TMC2023			20		25	ns
	TMC2023-1, -2			16		20	ns
	TMC2023-3			15		18	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40 pF					
	TMC2023			20		24	ns
	TMC2023-1, -2			16		18	ns
	TMC2023-3			14		16	ns

Application Notes

The TMC2023 can be cascaded to implement correlations of more than 64 bits. Typically, all clocks are tied together and the A, B, and M outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score. Use of the T register and TFLG require additional hardware for this configuration. The TMC2221 correlator provides 128 taps.

When comparing a multi-bit word to a single-bit reference, the outputs from the individual correlators must be appropriately weighted. This weighting reflects the relative importance of the different bit positions. Normally simple shifts (division by 2, 4, 8,...) provide the required weighting. The TMC2220 correlator provides 32-tap 4x1 correlation.

Figure 8. Cascading for Extended-Length Correlation

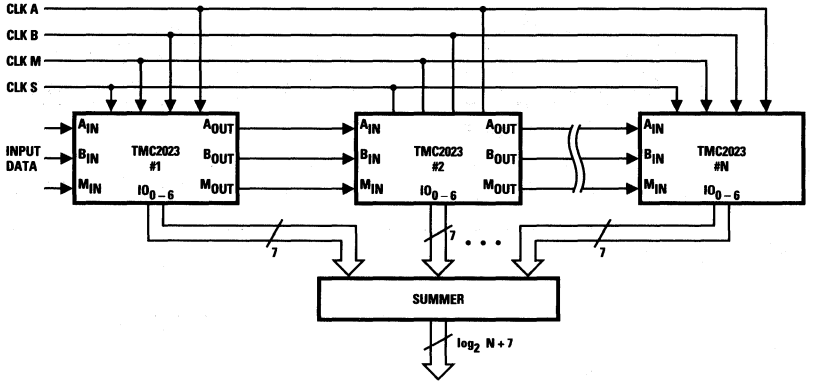
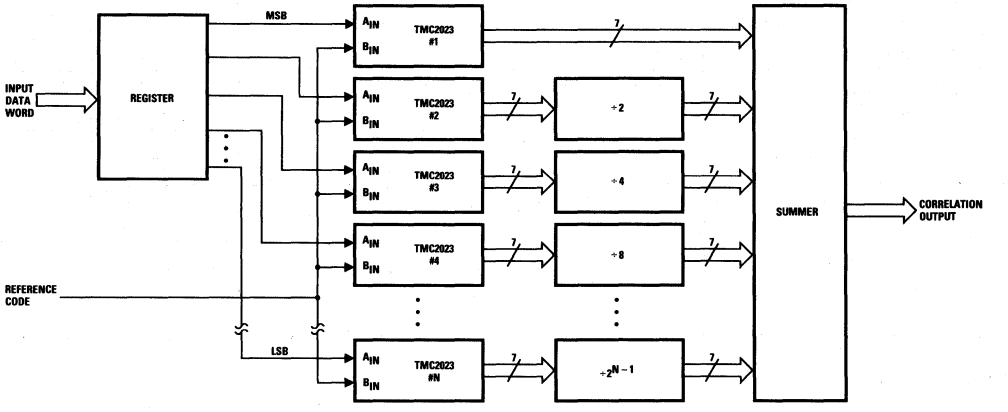


Figure 9. Multi-Bit x 1-Bit Correlation



Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMD). The nearest vendor equivalent product is shown in the table; however, the applicable SMD is the sole controlling document defining the SMD product.

SMD	TRW Product	Speed	Package
5962-89711 01JA	TMC2023B7V	25MHz	24 Pin CERDIP 0.6" Wide
5962-89711 02JA	TMC2023B7V1	30MHz	24 Pin CERDIP 0.6" Wide
5962-89711 01LA	TMC2023B2V	25MHz	24 Pin CERDIP 0.6" Wide
5962-89711 02LA	TMC2023B2V1	30MHz	24 Pin CERDIP 0.6" Wide
5962-89711 013A	TMC2023C3V	25MHz	28 Contact Chip Carrier
5962-89711 023A	TMC2023C3V1	30MHz	28 Contact Chip Carrier

Ordering Information

Product Number	f_{CLK} (MHz)	Temperature	Screening	Package	Package Marking
TMC2023B2C	25	STD: T_A = 0 to 70°C	Commercial	24-pin CERDIP, 0.3" Wide	2023B2C
TMC2023B2C1	30	STD: T_A = 0 to 70°C	Commercial	24-pin CERDIP, 0.3" Wide	2023B2C1
TMC2023B2C2	35	STD: T_A = 0 to 70°C	Commercial	24-pin CERDIP, 0.3" Wide	2023B2C2
TMC2023B2C3	50	STD: T_A = 0 to 70°C	Commercial	24-pin CERDIP, 0.3" Wide	2023B2C3
TMC2023B2V	25	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin CERDIP, 0.3" Wide	2023B2V
TMC2023B2V1	30	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin CERDIP, 0.3" Wide	2023B2V1
TMC2023B2V2	35	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin CERDIP, 0.3" Wide	2023B2V2
TMC2023B2V3	50	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin CERDIP, 0.3" Wide	2023B2V3
TMC2023B7C	25	STD: T_A = 0 to 70°C	Commercial	24-pin CERDIP, 0.6" Wide	2023B7C
TMC2023B7C1	30	STD: T_A = 0 to 70°C	Commercial	24-pin CERDIP, 0.6" Wide	2023B7C1
TMC2023B7C2	35	STD: T_A = 0 to 70°C	Commercial	24-pin CERDIP, 0.6" Wide	2023B7C2
TMC2023B7C3	50	STD: T_A = 0 to 70°C	Commercial	24-pin CERDIP, 0.6" Wide	2023B7C3
TMC2023B7V	25	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin CERDIP, 0.6" Wide	2023B7V
TMC2023B7V1	30	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin CERDIP, 0.6" Wide	2023B7V1
TMC2023B7V2	35	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin CERDIP, 0.6" Wide	2023B7V2
TMC2023B7V3	50	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin CERDIP, 0.6" Wide	2023B7V3
TMC2023C3C	25	STD: T_A = 0 to 70°C	Commercial	28-Contact Hermetic Ceramic Chip Carrier	2023C3C
TMC2023C3C1	30	STD: T_A = 0 to 70°C	Commercial	28-Contact Hermetic Ceramic Chip Carrier	2023C3C1
TMC2023C3C2	35	STD: T_A = 0 to 70°C	Commercial	28-Contact Hermetic Ceramic Chip Carrier	2023C3C2
TMC2023C3C3	50	STD: T_A = 0 to 70°C	Commercial	28-Contact Hermetic Ceramic Chip Carrier	2023C3C3
TMC2023C3V	25	EXT: T_C = -55 to 125°C	MIL-STD-883	28-Contact Hermetic Ceramic Chip Carrier	2023C3V
TMC2023C3V1	30	EXT: T_C = -55 to 125°C	MIL-STD-883	28-Contact Hermetic Ceramic Chip Carrier	2023C3V1
TMC2023C3V2	35	EXT: T_C = -55 to 125°C	MIL-STD-883	28-Contact Hermetic Ceramic Chip Carrier	2023C3V2
TMC2023C3V3	50	EXT: T_C = -55 to 125°C	MIL-STD-883	28-Contact Hermetic Ceramic Chip Carrier	2023C3V3

40G00283 Rev I 8/93

TMC2220/TMC2221
CMOS Programmable Digital Output Correlators
4 x 32 Bit, 20 MHz; 1 x 128 Bit 20 MHz

Description

The TMC2220 20 MHz, TTL compatible CMOS correlator is composed of four separate 1 x 32 correlator modules. The correlation scores of the four modules are weighted, combined and output on two separate parallel, three-state ports.

Each module contains a 32-bit serial data register, a 32-bit serial reference preload register, a 32-bit parallel reference latch and a 32-bit parallel mask latch. Correlation is performed by 32 exclusive-NOR (XNOR) gates. Each XNOR gate compares one (single bit) reference word. While correlation is being performed between the data and the present reference, the next reference pattern may be preloaded through one of two multiplexed input ports. Shorter sampling windows and bipolar correlation are also supported. Each module outputs a 6-bit binary correlation score. Either an unsigned (range 0 through 32) or bipolar (range -16 through +16) representation may be selected. The outputs of each pair of correlator modules is added, with user-selected weighting factors, producing intermediate correlation scores which can be combined or output directly to the main or auxiliary output ports.

Since the four modules can be cascaded serially or in parallel, the TMC2220 supports numerous single and dual channel applications involving 1, 2 or 4-bit wide data and window lengths up to 32, 64, 96 or 128 bits. Multiple devices can be combined to support large correlation operations.

The TMC2221 combines the four 32-bit modules in series for a fixed channel configuration of 1-bit by 128. The reduced complexity and package size of the TMC2221 is ideal for applications requiring less versatility than the TMC2220. By making use of the mask function, any size single channel length of up to 128 bits is possible.

With the TMC2221, the reference word is serially loaded through the single two-input multiplexed reference port of the first correlator module. Although the configuration is fixed, the reference loading process and basic operation for each module is similar to that of the TMC2220. The outputs are summed with equal weighting, and the result is output through the single 8-bit output port. Unsigned magnitude or two's complement (bipolar) output score may be selected.

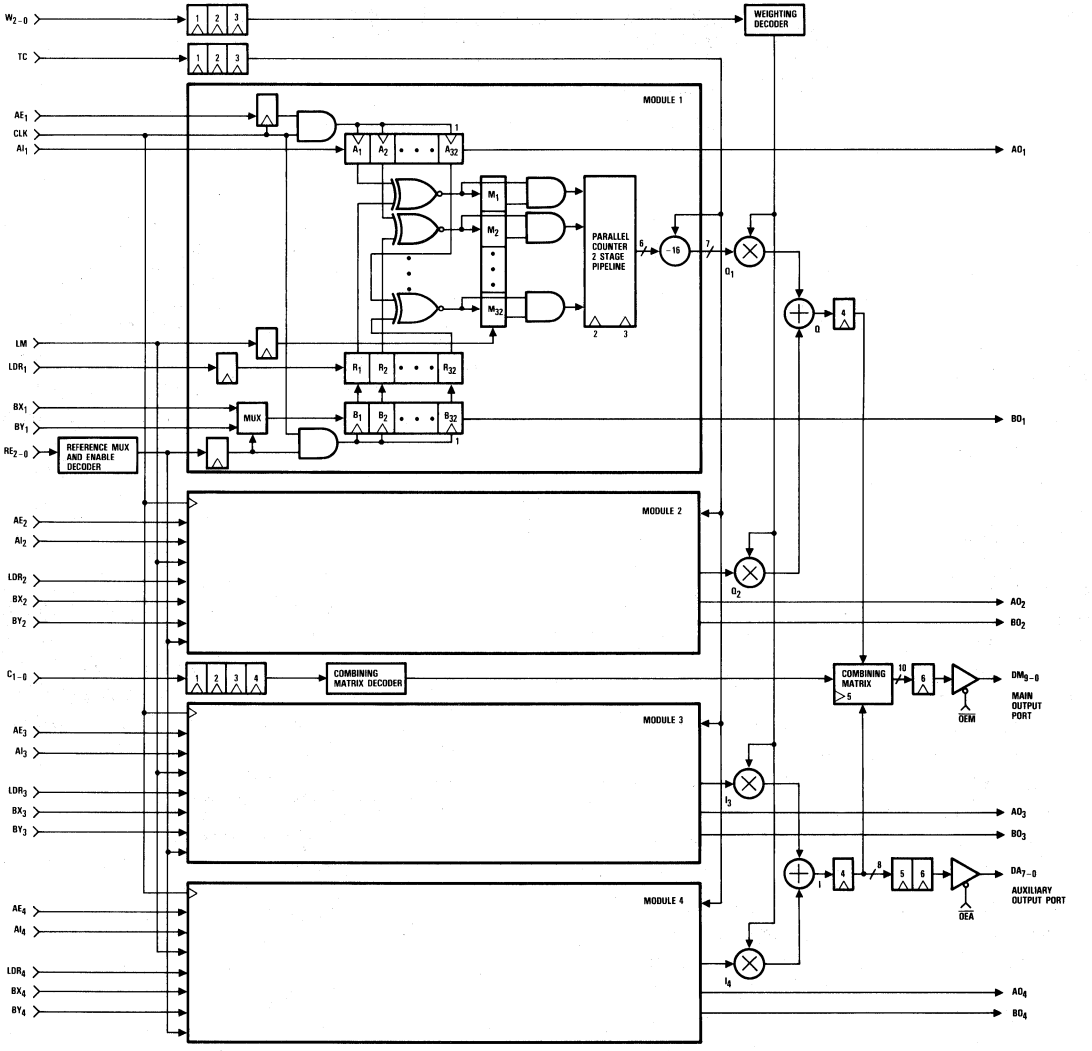
Features

- 20 MHz continuous correlation rate
- Fully programmable masking
- Two's complement or unsigned magnitude correlation score
- User-programmable reference load multiplexing
- Channel weighting and output formatting (TMC2220)
- Multi-bit, dual-channel or non-coherent (quadrature) correlation (TMC2220)
- Single +5V power supply
- Low power CMOS construction
- Three-state TTL compatible outputs
- TMC2220 available in 68-pin grid array and 69-pin plastic PGA packages
- TMC2221 available in a 28-pin CERDIP

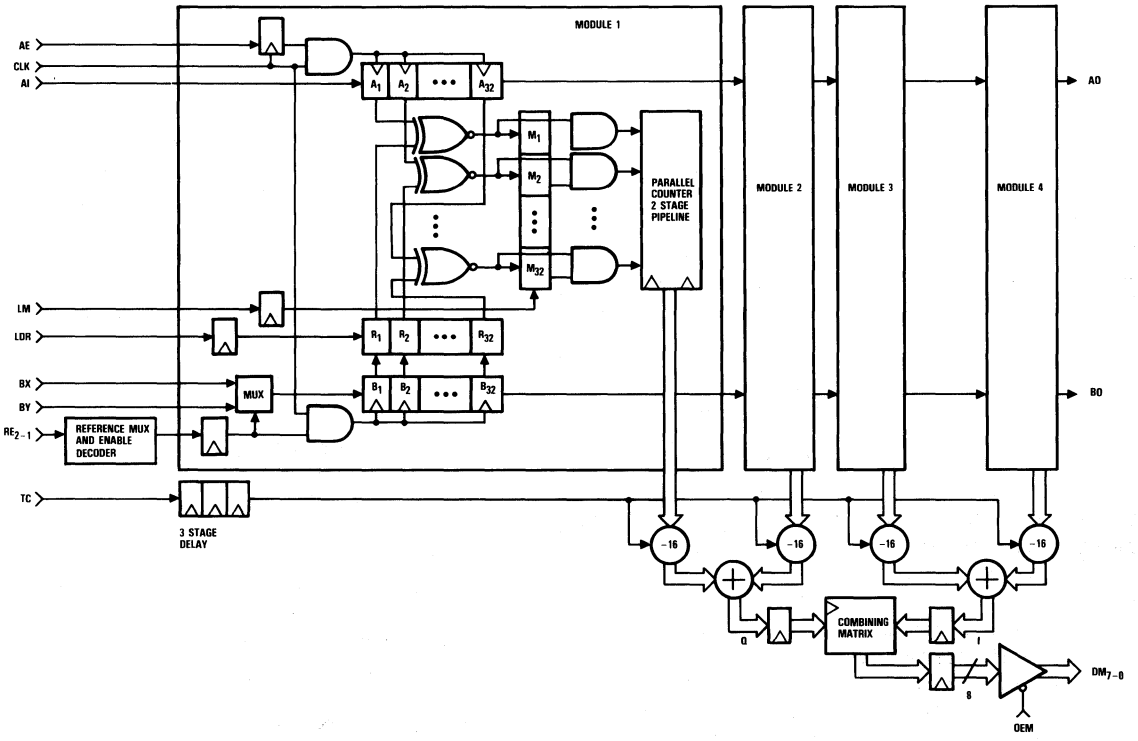
Applications

- Signal detection
- Radar signature recognition
- Secure communications
- Robotics/automated assembly
- Automatic test equipment
- Electro-optical navigation
- Pattern and character recognition
- Assembly line inspection

TMC2220 Functional Block Diagram



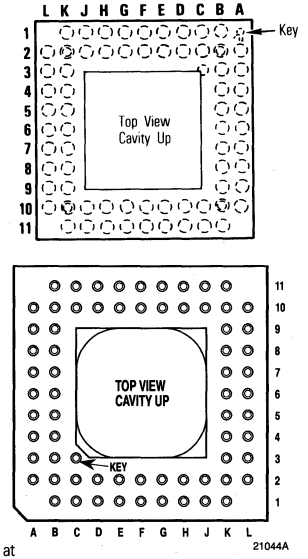
Functional Block Diagram



TMC2220 Pin Assignments

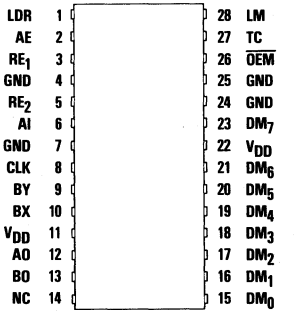
68 Pin Grid Array – G8 Package
69 Pin Plastic Pin Grid Array – H8 Package [1]

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	DA_1	K2	GND	K10	RE_2	B10	LDR_4
B1	DA_0	L2	V_{DD}	K11	AI_2	A10	AE_4
C2	DM_0	K3	GND	J10	BY_2	B9	LDR_3
C1	DM_1	L3	$\overline{OEM}$	J11	BX_2	A9	AE_3
D2	DM_2	K4	W_2	H10	AI_1	B8	$\overline{OEA}$
D1	DM_3	L4	W_1	H11	BY_1	A8	V_{DD}
E2	DM_4	K5	W_0	G10	BX_1	B7	AO_4
E1	DM_5	L5	C_1	G11	GND	A7	BO_4
F2	V_{DD}	K6	C_0	F10	CLK	B6	AO_3
F1	DM_6	L6	TC	F11	GND	A6	BO_3
G2	DM_7	K7	LM	E10	BY_3	B5	DA_7
G1	DM_8	L7	LDR_1	E11	BX_3	A5	DA_6
H2	DM_9	K8	AE_1	D10	AI_3	B4	DA_5
H1	BO_1	L8	LDR_2	D11	BY_4	A4	DA_4
J2	AO_1	K9	AE_2	C10	BX_4	B3	DA_3
J1	BO_2	L9	RE_0	C11	AI_4	A3	DA_2
K1	AO_2	L10	RE_1	B11	V_{DD}	A2	GND



Note: 1. Pin D4 is a mechanical orientation pin on the H8 package at manufacturer's option.

TMC2221 Pin Assignments



28 Pin CERDIP – B6 Package

Functional Description

General Information

The TMC2220 consists of four independent 1 x 32 correlator channels with weighted correlation scores which are combined and output on the two output ports (main and auxiliary). By taking advantage of the instruction set and I/O structure, the TMC2220 can be adapted to a wide variety of applications.

The TMC2221 consists of the four 1 x 32 correlator modules cascaded internally for a single 1 x 128 correlator. The outputs of each module are given a unity weighting, summed and placed on the output port.

Correlator Channel Modules

Each of the four modules (i = 1 to 4) contains two 32-bit serial synchronous shift registers, A_i (data) and B_i (reference preload); two 32-bit parallel latches, R_i (reference) and M_i (mask); 32 exclusive-NOR gates; 32 AND gates; a 32-bit parallel binary counter with a 6-bit unsigned output and a defeatable half-scale (-16) subtractor with a 7-bit two's complement output.

Whenever a given A_i or B_i register is enabled, the next rising edge of the clock loads the value at the corresponding A_i or BX_i/BY_i input port into the first cell of the register, and shifts the contents of each cell to the next, overwriting the contents of the last cell. These serial-in, parallel-tapped registers form the first of six registers which account for the six internal delays. After an output buffer delay t_D, the new contents of the last cell of A_i and B_i become available at the outputs AO_i and BO_i respectively. These outputs are used for cascading multiple devices. In addition, the B_i input multiplexer selects which of two input ports, BX_i or BY_i, is to be used on that cycle.

The reference latch R_i tracks the contents of B_i when control LDR_i was HIGH on the previous cycle and holds when LDR_i was LOW. A HIGH on LDR_i transfers the contents of B_i in parallel into R_i on the next clock cycle where correlation takes place. When LDR_i is held HIGH, R_i is transparent, enabling direct correlation between A_i and B_i.

Each of the 32 outputs of R_i is correlated against the corresponding tap of A_i by an XNOR gate whose output is connected to both the masking AND gate and the masking latch M_i.

Each M_i tracks if LM was HIGH on the previous cycle and holds if LM was LOW. When LM is held HIGH, all M_i latches are transparent and the output of each XNOR gate is sent to both inputs of the corresponding AND gate to prevent masking or disabling from occurring. A LOW on LM loads the next unmasked correlation pattern (from the XNOR gates) into each M_i. Wherever the latch holds a logic one, normal correlation is enabled; wherever it is a logic zero, correlation is masked by the AND gate.

A 32-bit parallel counter encodes the number of logic ones emerging from the AND gates as a 6-bit binary number between 0 and 32 (100000). The clock drives the two pipeline registers in the counter (the second and third registers in the six register pipeline).

The 6-bit unsigned binary output of each parallel counter then enters a half-scale subtractor where it passes unchanged if the pipelined control TC is LOW and is reduced by 16 if TC is HIGH. If TC is HIGH, the range of correlation scores becomes -16 through +16 where +16 denotes a perfect match between the contents of A_i and those of R_i with no masking. A score of -16 denotes that no unmasked data bit matches the corresponding reference bit (anti-correlation). The TC control is pipelined by 3 registers, such that it is aligned with new data entering the A_i or B_i register.

Weighting and Merging Circuitry

On the TMC2220, the 7-bit two's complement output of each correlator module (I_1, I_2, I_3, I_4) is multiplied by a factor of 0, 1, 2, 3, 4 or 5 according to controls W_{2-0}. The outputs of each pair of multipliers is then added and the results Q and I are loaded into the fourth pipeline register.

Following two additional pipeline delays from the fifth and sixth registers, correlation sum I is available on the TMC2220 at the 8-bit auxiliary output port, DA_{7-0}, if the buffer is enabled ($\overline{OEA}$ = LOW).

Under controls C_{1-0}, the TMC2220 combiner blends Q and I into a single final correlation score which is sent to the 10-bit main output port, DM_{9-0}, if $\overline{OEM}$ is LOW. The combiner pipeline register stage 5 and the main output register stage 6 are balanced by the auxiliary port double output register. In the simplest mode, the combiner outputs correlation sum Q permitting the TMC2220 to be used in two separate correlator channels. In this application, the combined results from modules 1 and 2 emerge through DM_{9-0} while the results from modules 3 and 4 emerge through DA_{7-0}. In the three remaining modes, the output at the main port will reflect the correlations of all four modules.

In the second mode, the combiner outputs the unweighted sum, Q + I. In the third mode, it outputs the weighted sum, Q + I/2, for single channel binary applications. In the fourth mode, the combiner extracts the absolute values of Q and I and adds the greater magnitude value to one half of the lesser value. This final mode is an approximation of the Pythagorean vector magnitude formula:

$$M = (X^2 + Y^2)^{1/2}$$

The TMC2220 contains a total of five pipeline registers plus the data and reference preload shift registers making the total delay six clock cycles. Instructions and data paths are pipelined so the instructions presented on a given clock cycle apply to the value entering registers A_i and B_i. Instructions RE, LM, LDR and AE, all of which enable registers or latches, must be set one cycle early (see timing diagram).

For the TMC2221, the correlation score of each module is passed unchanged (TC = LOW) or reduced by sixteen (TC = HIGH). Each module score is given a unity weighting then sent to the combining matrix where the four scores are added and output on the 8-bit data bus if $\overline{OEM}$ is LOW.

In magnitude mode (TC = LOW) and masking disabled, a perfect match between the data and reference will produce a correlation score of 128 (10000000_B) and correlation score of 0 shall indicate no matches (anti-correlation). In two's complement mode (TC = HIGH), perfect correlation will produce a score of 64 (01000000_B) and anti-correlation shall have an output of −64 (11000000_B). A total of five register delays plus the input register cause the result to be available on the sixth clock cycle after the loading of the input data.

Signal Definitions

Power

V_{DD}, GND — The TMC2220/TMC2221 operate from a single +5V power supply. All power and ground pins must be connected.

Inputs

AI_{1-4} — Each data input is a single-bit serial input to the A_i register of each correlator module.

BX_{1-4}, BY_{1-4} — The main, BX_i, and alternate, BY_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.

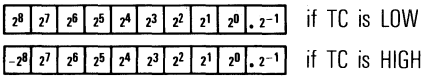
Outputs

AO_{1-4} — Each cascade data output is a single-bit serial output from the A_i register of each correlator module.

BO_{1-4} — Each cascade reference preload output is a single-bit serial output from the B_i register of each correlator module.

DM_{9-0} — The 10-bit main correlation output (TMC2220 only) is a combination of the four module output scores, Q_1, Q_2, I_3, I_4, which are dependent on the W_{2-0} weighted adder and C_{1-0} combining matrix controls. The main output port is enabled by $\overline{OEM}$.

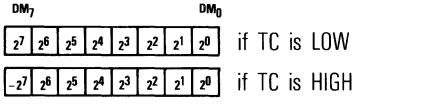
The TMC2220 10-bit output format is:



The TMC2221 has an 8-bit correlation output DM_{7-0} which always outputs the sum:

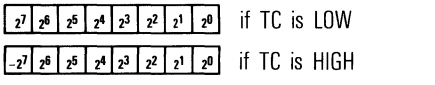
$$Q_1 + Q_2 + I_3 + I_4$$

Where each term is either unsigned magnitude or magnitude minus 16 depending on the TC control. The TMC2221 8-bit output format is:



DA_{7-0} — (TMC2220 only) The 8-bit auxiliary correlation output is the sum of two module output scores, I_3 and I_4, which are dependent on the W_{2-0} weighted adder controls. The auxiliary output port is enabled by $\overline{OEA}$.

The 8-bit binary output format is:



Correlation

Clocks

CLK — The clock for A_i data and B_i reference preload registers can be toggled at up to 20MHz. All registers are strobed on the rising edge of CLK and dependent on the registered enable controls, AE_i for the A_i registers, and RE_{2-0} for the B_i registers. The pipeline delay registers for the controls, W_{2-0}, C_{1-0} (TMC2220 only) and TC are also strobed on the rising edge of CLK.

Controls

AE_{1-4} — The clock enable for the four A_i data registers is a registered, active HIGH control. When AE_i is LOW on the previous cycle, no shifting of data occurs on A_i. AE_i is read on the rising edge of CLK, thus the shifting of data in A_i will occur on the next rising edge of CLK.

C_{1-0} — (TMC2220 only) These pipelined instructions select the function to be executed by the combining matrix and output through the main output port, DM_{9-0}.

LDR_{1-4} — The Load Reference control copies the contents of register B_i into latch R_i for correlation. If LDR_i was LOW on the previous clock cycle, the present contents of the latch remain in R_i. If LDR_i was HIGH, R_i is transparent and the B_i are values used in the current correlation.

LM — The Load Mask control allows the user to mask or select "no compare" bit positions in each channel. Inputs shifted into A_i and B_i produce a correlation pattern as the desired mask. Control LM must be HIGH on the previous cycle to track and LOW to store the pattern in the mask latches M_i. If no masking is required, LM is kept HIGH, making M_i transparent.

$\overline{OEA}$ — (TMC2220 only) The asynchronous output enable for the auxiliary output port, DA_{7-0}, is an active LOW control. When $\overline{OEA}$ is HIGH, the output is in a high-impedance state.

$\overline{OEM}$ — The asynchronous output enable for the main output port, DM_{9-0} (DM_{7-0} on the TMC2221), is an active LOW control. When $\overline{OEM}$ is HIGH, the output is in a high-impedance state.

RE_{2-0} — The encoded clock enable and load selector controls determine the various combinations of BX_i and BY_i reference inputs that may be selected for the four reference preload registers B_i. The B_i register clocks may also be selectively enabled. Like LDR, LM and AE_i, this control is delayed by one clock cycle. (RE_{2-1} used on the TMC2221 to select BX or BY.) See Table 1.

TC — The Two's Complement control forces the outputs of the four correlator modules to be unipolar (0 to 32) or bipolar (−16 to +16). When TC is LOW, the outputs of the correlator modules are passed unchanged to the weighting circuitry. When TC is HIGH, 16 is subtracted from each correlator output which is then interpreted as a two's complement value.

W_{2-0} — (TMC2220 only) The weighted adder controls determine the relative weightings of the four correlation module scores.

TMC2220 Package Interconnections

Signal Type	Signal Name	Function	G8, H8 Package Pins
Power	V_{DD}	Supply Voltage	F2, L2, B11, A8
	GND	Ground	K2, K3, G11, F11, A2
Inputs	AI_{1-4}	Data Input	H10, K11, D10, C11
	BX_{1-4}	Main Reference Preload	G10, J11, E11, C10
	BY_{1-4}	Alternate Reference Preload	H11, J10, E10, D11
Outputs	AO_{1-4}	Data Output	J2, K1, B6, B7
	BO_{1-4}	Reference Preload Output	H1, J1, A6, A7
	DM_{9-0}	Main Port	H2, G1, G2, F1, E1, E2, D1, D2, C1, C2
	DA_{7-0}	Auxiliary Port	B5, A5, B4, A4, B3, A3, B2, B1
Clock	CLK	Master Clock	F10
Controls	AE_{1-4}	Register Clock Enable	K8, K9, A9, A10
	C_{1-0}	Combining Matrix	L5, K6
	LDR_{1-4}	Reference Load	L7, L8, B9, B10
	LM	Mask Load	K7
	$\overline{OEA}$	Auxiliary Port Output Enable	B8
	$\overline{OEM}$	Main Port Output Enable	L3
	RE_{2-0}	Reference Load Select	K10, L10, L9
	TC	Two's Complement	L6
	W_{2-0}	Module Weighting Factor	K4, L4, K5

TMC2221 Package Interconnections

Signal Type	Signal Name	Function	B6 Package
Power	V_{DD}	Supply Voltage	11, 22,
	GND	Ground	4, 7, 24, 25
Inputs	AI	Data Input	6
	BX	Main Reference Preload	10
	BY	Alternate Reference Preload	9
Outputs	AO	Data Output	12
	BO	Reference Preload Output	13
	DM_{7-0}	Main Port	23, 21, 20, 19, 18, 17, 16, 15
Clock	CLK	Master Clock	8
Controls	AE	Register Clock Enable	2
	LDR	Reference Load	1
	LM	Mask Load	28
	$\overline{OEM}$	Port Output Enable	26
	RE_{2-1}	Reference Load Select	5, 3
	TC	Two's Complement	27
No Connection	NC		14

Table 1. Reference Preload Register Input and Enable Operation

RE_i Controls	Selected Reference Port (TMC2220)				Selected Reference Port (TMC2221)
RE_{2-0}	1	2	3	4	
000	Dis	Dis	Dis	Dis	Dis
001	Dis	Dis	Dis	BX_4	
010	Dis	Dis	BY_3	BX_4	BY
011	Dis	Dis	BY_3	BY_4	
100	BX_1	BX_2	BX_3	BX_4	BX
101	BY_1	BX_2	BX_3	BX_4	
110	BY_1	BX_2	BY_3	BX_4	BY
111	BY_1	BY_2	BY_3	BY_4	

Notes:

1. Dis = B_i register disabled (hold mode).
2. LSB (RE_0) not used on the TMC2221.

Table 2. Module Weighting Factor Operation (TMC2220 Only)

W_i Controls	Internal Channel Configuration	
W_{2-0}	Q	I
000	$Q_1 + Q_2$	$I_3 + I_4$
001	$3Q_1 + Q_2$	$3I_3 + I_4$
010	$4Q_1 + Q_2$	$4I_3 + I_4$
011	Q_2	I_4
100	Q_1	I_3
101	$3Q_1 + 2Q_2$	$3I_3 + 2I_4$
110	$4Q_1 + 2Q_2$	$4I_3 + 2I_4$
111	$5Q_1 + 2Q_2$	$5I_3 + 2I_4$

Table 3. Combining Matrix Operation (TMC2220 Only)

C_i Controls	Main Output Port Function
C_{1-0}	DM_{9-0}
00	Q
01	Q + I/2
10	Q + I
11	Max (|Q|, |I|) + 1/2 Min (|Q|, |I|)[1]

Notes:

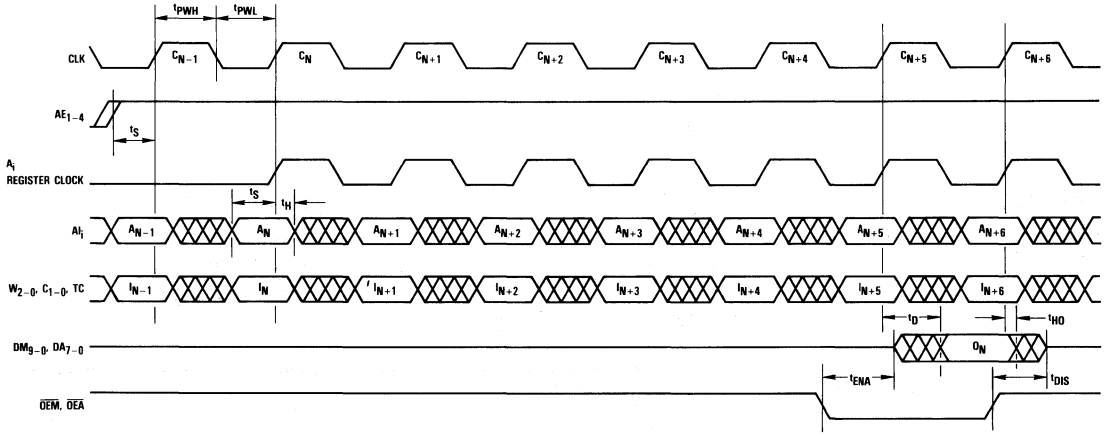
1. The larger magnitude value of Q or I plus one-half of the smaller magnitude value.
2. The TMC2221 always outputs the sum $Q_1 + Q_2 + I_3 + I_4$.

Sliding Correlation Timing

The TMC2220 and TMC2221 have a six register pipeline. There are registers for the input data and reference, parallel counter, weighting circuitry, combining matrix, and output. CLK is used to load all A_i, B_i and instruction pipeline registers. With the register controls enabled, a data or reference word is loaded into its respective A_i or B_i register on every rising edge of CLK. Data A_N enters register A_i on the rising edge of clock C_N. The reference latch is static if the previous LDR_i was LOW or tracks B_i if LDR_i was HIGH. If reference preload is not desired, holding control LDR_i HIGH makes latch R_i transparent and direct correlation between A_i and B_i occurs. Data is valid if present at the input for a setup time t_S before and a hold time t_H after the rising clock edge. Setup and hold time requirements also apply to instructions and controls, however, AE, LDR, LM and RE must be valid one cycle before taking effect.

Because of the six internal pipeline delays, the correlation score for a given set of A_i and B_i register contents appears at the output ports six clock cycles plus an output delay t_D later. When the main and auxiliary (TMC2220 only) output ports are enabled ($\overline{OEM}$ = LOW and $\overline{OEA}$ = LOW), the correlation score O_N of data window A_{N-31} through A_N is output after rising clock edge C_{N+5} (A_{N-127} through A_N on the TMC2221). Instructions TC, W and C are registered and pipelined so that the instructions will be aligned with the data. The instructions I_N (see timing diagram) which are loaded on rising clock edge C_N apply to a correlation between data and reference words N-31 (N-127) through N. Masking is assumed to be preset (previous LM = LOW) or unused (previous LM = HIGH). The same timing applies if the reference is shifting and data is fixed.

Figure 1. Sliding Correlation Timing



Reference Register Load Timing

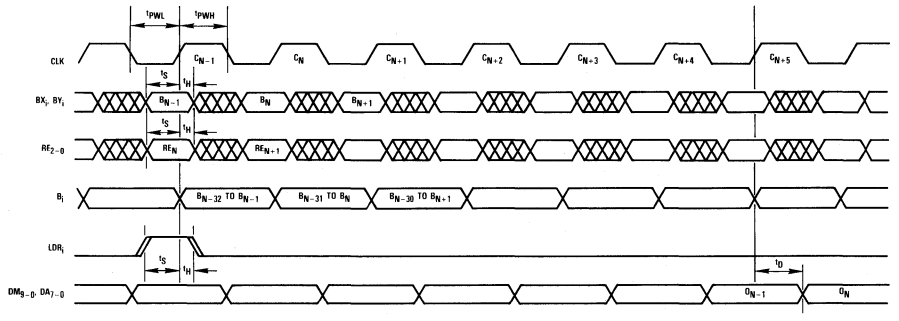
The HIGH on LDR_i transfers the contents of B_i in parallel into R_i in the next clock period. R_i tracks B_i when control LDR_i is HIGH and holds when LDR_i is LOW. N rising edges of CLK are required to load N reference words into the reference preload register B_i. The rising edge of clock C_N loads reference word B_N so that B_i contains words B_{N-31} through B_N.

Figure 2 illustrates the LDR_i instruction timing to transfer reference window B_{N-31} through B_N into the reference latch. With this timing, correlation against the old reference pattern is preserved during the "LDR" clock cycle and that correlation against the new reference pattern B_{N-31} to B_N should commence immediately after the "LDR" clock cycle. The user must meet the normal input setup and hold time requirements and setup the instruction one clock cycle before the desired transfer.

A completely new reference can be loaded into latch R on every 32nd clock cycle. With the output ports enabled, the correlation score O_N (correlation between data A_{N-31} through A_N and reference B_{N-31} through B_N) is available an output delay t_D after the rising edge of clock C_{N+5} because of the six register pipeline.

Operation of the TMC2221 is similar to the operation described for the TMC2220 except the length of the reference word is 128 bits rather than 32. The reference register will therefore contain the pattern B_{N-127} through B_N, and correlation occurs between this reference and data A_{N-127} through A_N. A new reference word therefore requires 128 clock cycles to completely load the new value. With the output ports enabled, the correlation score O_N (correlation between data A_{N-127} through A_N and reference B_{N-127} through B_N) is available an output delay t_D after the rising edge of clock C_{N+5}.

Figure 2. Reference Latch Load Timing

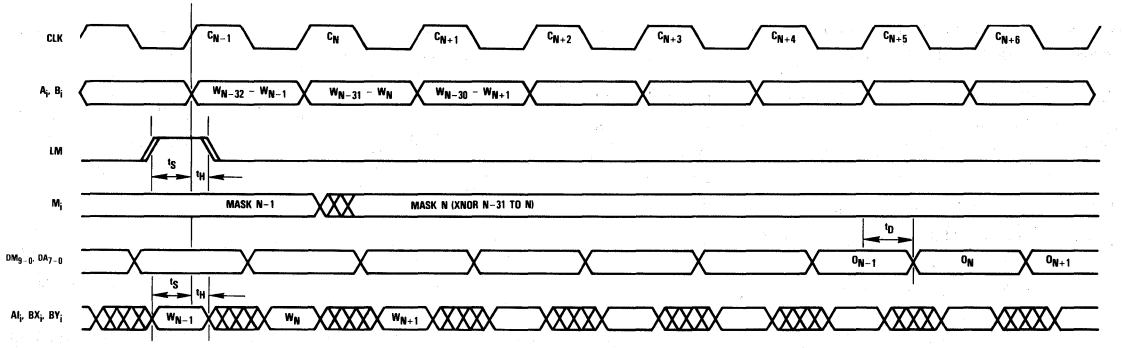


Mask Register Loading

Control LM latches a mask pattern into M_i which selectively disables word positions in each correlator module. Masking latch M_i tracks the XNOR output if, on the the previous clock cycle, LM was HIGH and holds if LM was LOW. Figure 3 illustrates the TMC2220 LM timing to latch a mask generated by the exclusive NOR of A_{N-31} through A_N with R_{N-31} through R_N. LM must be set HIGH t_S before the rising edge of clock C_{N-1} to load the mask for A_{N-31} thru A_N. LM must be set LOW before the next rising edge of C_N to ensure words N–31 to N remain latched as the mask pattern. A completely new mask may be loaded on every 32nd clock cycle. However, to permit time for data and reference loading, mask loading is generally limited to every 64th clock cycle. The first correlation score which reflects mask N is output t_D after the rising edge of clock cycle C_{N+6}.

Operation of the TMC2221 is similar that of the TMC2220 but requires 128 clock cycles to completely load a new mask pattern. To permit time to load new data and a new reference pattern once the mask is loaded, an additional 128 clock cycles is required. Therefore, mask loading is generally limited to every 256 clock cycles in the TMC2221. The mask pattern loaded will be the exclusive–NOR of A_{N-127} through A_N with R_{N-127} through R_N.

Figure 3. Masking Latch Load Timing



Applications Discussion

The TMC2220 architecture provides the flexibility for a number of configurations. The cascade outputs and the internal weighting and adder logic allow a single TMC2220 to be configured as four independent 32-bit correlators, independent 96-bit and 32-bit correlators, two independent 64-bit correlators, or as a single 128 x 1 correlator. The TMC2220 may also be cascaded serially or in parallel to increase the length or width of correlation.

To increase the correlation length in a single TMC2220 system, the cascade outputs of a module (AO_i, BO_i) can be connected to the inputs of the next module (AI_{i+1}, BI_{i+1}). When using this configuration, the input enables and load controls should be connected together. Figure 4 shows the configuration for a dual 64 x 1 correlation. In this application, the outputs of module 1 are connected to the inputs of module 2 and the outputs of module 3 are connected to the inputs of module 4. The weighting logic is set for 1:1 weighting and the combining logic is set to output $Q_1 + Q_2$ on the main output DM_{9-0}, and $I_3 + I_4$ on the auxiliary output DA_{7-0}.

Figure 4. Dual 64 x 1 Configuration

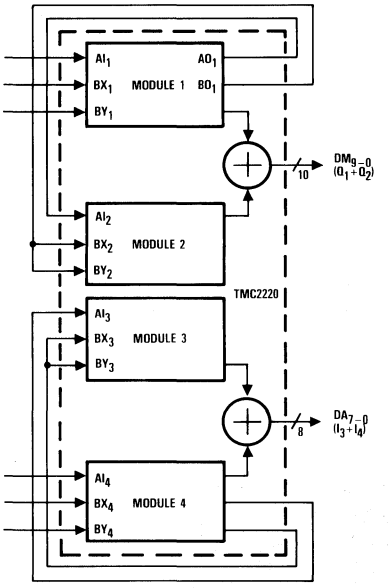
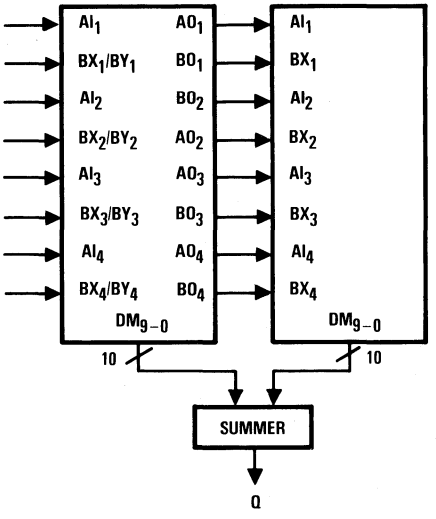


Figure 5. Cascading the TMC2220 for Extended-Length Correlation

Figure 5 shows an example of multi-bit correlation with extended length. This example shows 4-bit correlation with a length of 64-bits. The outputs of the two TMC2220s must be externally added to obtain the 64-bit correlation score. The weighting and combining of the module correlation scores should be set as required by the application.



Correlation

Figure 6. 8-Bit Correlation with the TMC2220

Figure 6 shows an example of 8-bit, two's complement correlation. Two TMC2220s are used in parallel and externally summed to obtain the properly weighted correlation score. To obtain a properly weighted correlation score, each bit of the output must be multiplied by an appropriate binary scaling factor. The 8-bit data input and reference are connected as shown. The weighting control of each TMC2220 is set for 4:1 weighting (W_{2-0} = 010). This multiplies the upper two bits of each TMC2220 by a factor of 4 (Q_1, I_3). The next step is to multiply the 2nd and 4th bits (Q_2, I_4) by a factor of 2. An equivalent operation is to divide the 1st and 3rd bits by 2. This operation is accomplished by setting the combining logic to output the sum Q + I/2 (C_{1-0} = 01). The final output of each TMC2220 will be equivalent to:

$$DM_{9-0} = (4 \times Q_1) + (2 \times I_3) + (1 \times Q_2) + (1/2 \times I_4)$$

Setting the weighting and combining controls as described will produce a correlation score with each bit properly weighted based on its 4-bit binary position. The final step is to multiply the correlation output of the most-significant TMC2220 (bits 7-4) by a factor of 16 then combine the outputs of the two TMC2220s. This is done using external adder circuitry. Multiplication is performed by simply shifting the output lines of the upper TMC2220 by four places at the input to the adder logic. The output of the summer, therefore, shall give the binary weighted correlation score of a quantized 8-bit input. The same circuit can be used with unsigned data if the inverter on the most-significant-bit of the reference input is omitted.

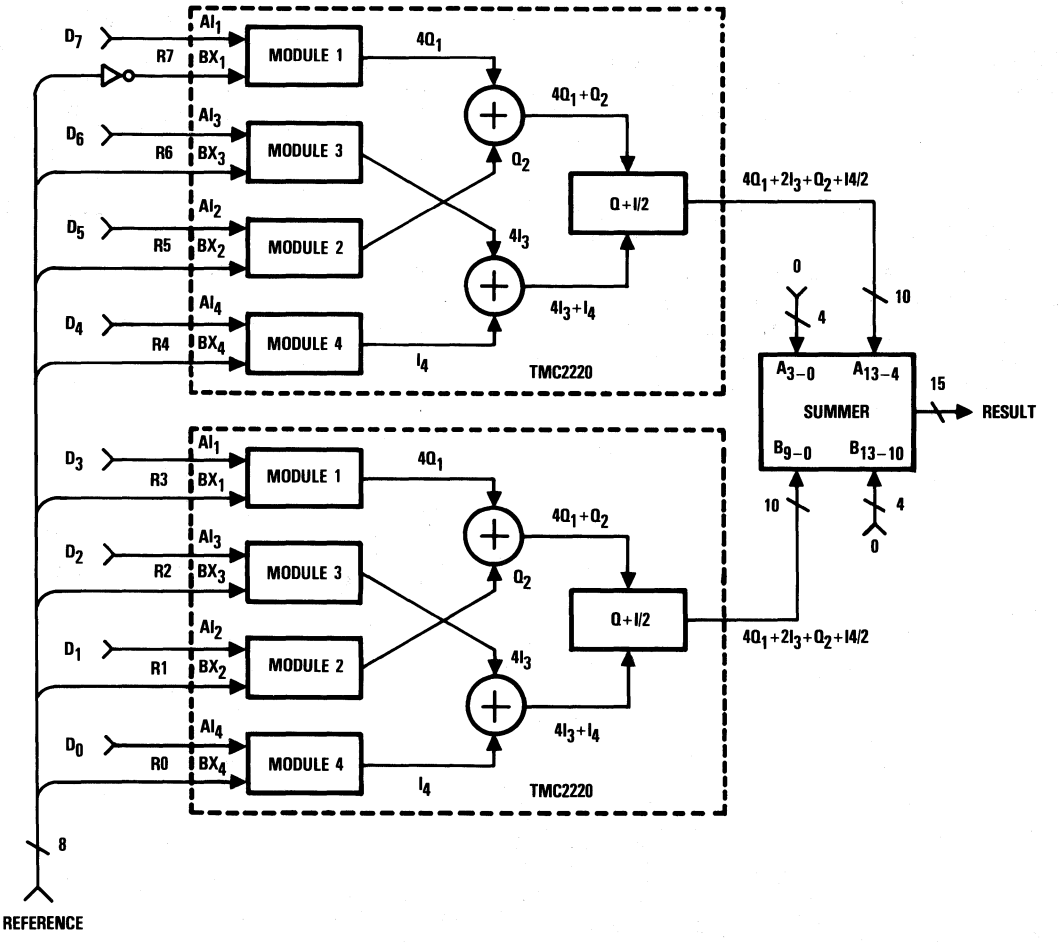
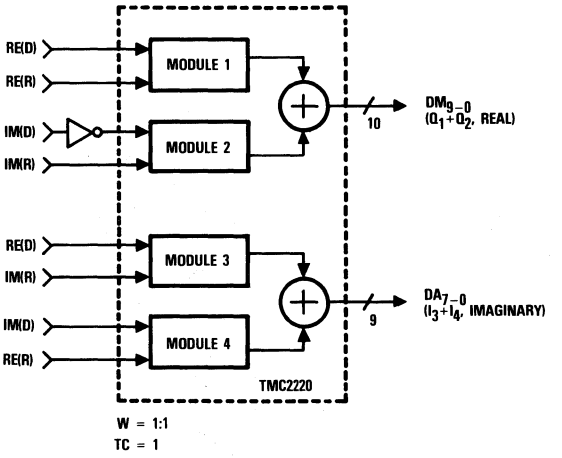


Figure 7. Full Complex Correlation with the TMC2220

Figure 7 is an example of full complex correlation. In this example, separate real and imaginary terms are multiplied and summed internally to provide a real and imaginary result. This method preserves the phase information of the input. Inputs are connected as shown in the figure. The imaginary term in Im(D) x Im(R) is negated (inverted) for proper sign in the summation. The TMC2220 is set for 1:1 (Q_1 + Q_2, I_3 + I_4) weighting, two's complement mode, and the combining control is set to output Q on the main output and I on the auxiliary output. All 32 internal taps are used.



A simple example would be to find a sine wave in a demodulated data stream. The references would be set to:

$$Re(R) = Cos(\omega t) \text{ and } Im(R) = Sin(\omega t)$$

where, ω is the modulation frequency. Each term is set to:

1 for positive and 0 for negative

The data inputs are set to:

$$Re(D) = data_{in} \times Cos(ft) \text{ and } Im(D) = data_{in} \times Sin(ft)$$

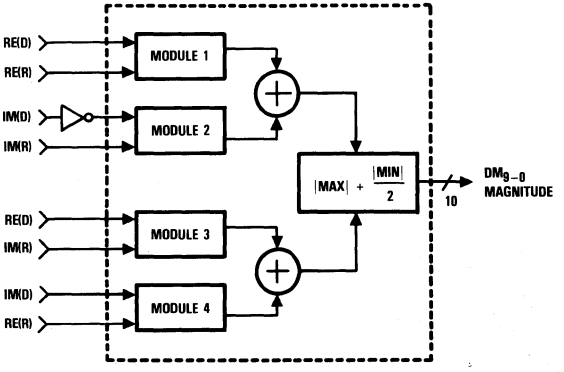
where, f is the mixer or carrier frequency.

Figure 8. Complex Correlation with Magnitude Result

Figure 8 is similar to full complex correlation, however, in this example the output is magnitude only. This application is used when the phase relationship is not required. The inputs are connected as in the previous example, however, rather than a full complex output, the outputs are combined internally to:

$$Max(|Q|, |I|) + 1/2\ Min(|Q|, |I|)$$

(C_{1-0} = 11) to obtain the approximate magnitude output. Multiplying the output by 15/16 will reduce the error in the magnitude approximation.



Correlation

Figure 9. Cascading the TMC2221 for Extended–Length Correlation

The TMC2221 can be cascaded to implement correlations of more than 128–bits. Typically all clocks, reference inputs and enables are connected together and the A and B outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score.

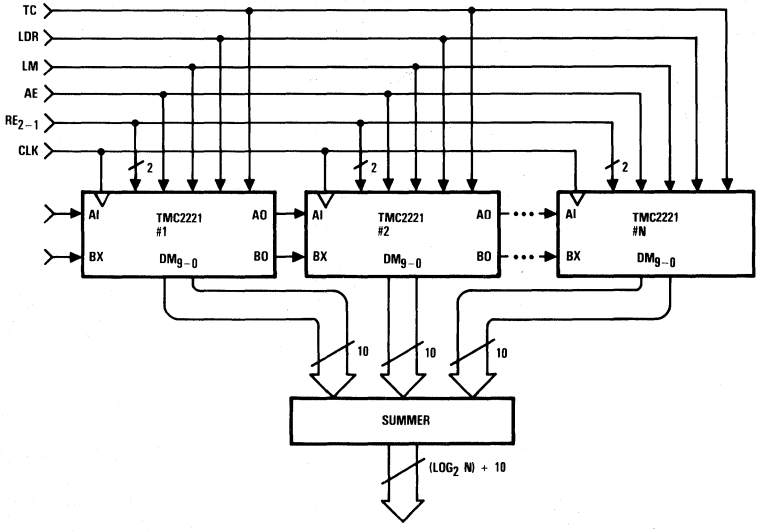


Figure 10. Multi–Bit x 1 Bit Correlation

The TMC2221 may also be used to compare multi–bit words with a single–bit reference. When this is done, the output of each TMC2221 must be appropriately weighted to the adder circuitry. The weighting reflects the relative importance of the different bit positions. Weighting can normally be accomplished by simple bit shifts at the input to the summer.

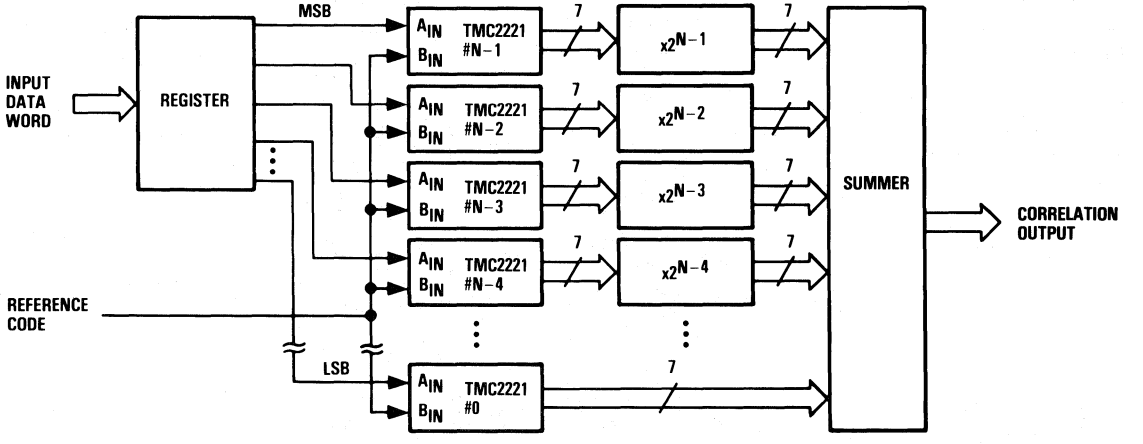


Figure 11. Equivalent Input Circuit

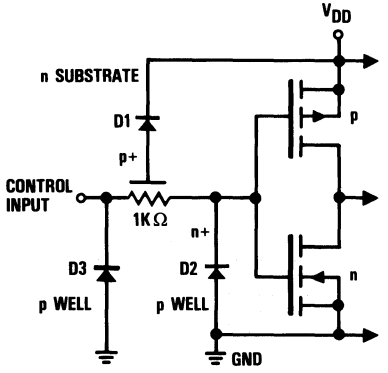


Figure 12. Equivalent Output Circuit

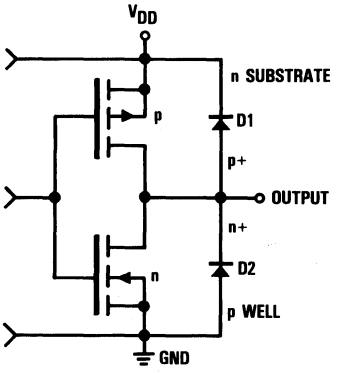
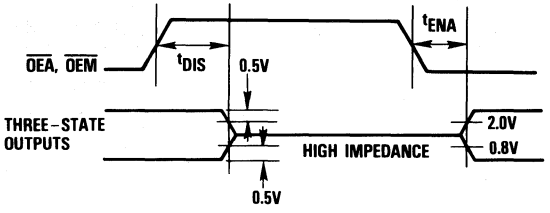


Figure 13. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5V)
Output	
Applied voltage [2]	−0.5 to (V_{DD} +0.5V)
Forced current [3,4]	−1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Correlation

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OEM}$, $\overline{OEA}$ = 5V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz, $\overline{OEM}$, $\overline{OEA}$ = 5V		70		80	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−40		−40		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	−40		−40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−150		−150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

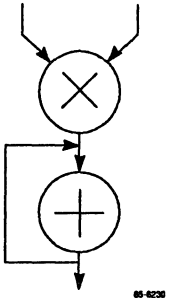
Parameter		Test Conditions	Temperature Range								Units
			Standard				Extended				
			-1				-1				
			Min	Max	Min	Max	Min	Max	Min	Max	
F_C	Clock (Correlation) Rate	V_{DD}=Min		20		17		20		17	MHz
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	25		30		25		30		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	15		15		15		15		ns
t_S	Input Setup Time		15		15		17		17		ns
t_H	Input Hold Time		0		0		0		0		ns
t_D	Output Delay	V_{DD}=Min, C_{LOAD}=40pF		25		25		25		25	ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=40pF	3		3		3		3		ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD}=Min, C_{LOAD}=40pF		17		17		17		17	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD}=Min, C_{LOAD}=40pF		22		22		22		22	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2220G8C	STD–T_A=0°C to 70°C	Commercial, 17MHz	68 Pin Grid Array	2220G8C
TMC2220G8V	EXT–T_C=–55°C to 125°C	MIL-STD-883, 17MHz	68 Pin Grid Array	2220G8V
TMC2220G8C1	STD–T_A=0°C to 70°C	Commercial, 20MHz	68 Pin Grid Array	2220G8C1
TMC2220G8V1	EXT–T_C=–55°C to 125°C	MIL-STD-883, 20MHz	68 Pin Grid Array	2220G8V1
TMC2220H8C	STD–T_A=0°C to 70°C	Commercial, 17MHz	69 Pin Plastic Pin Grid Array	2220H8C
TMC2220H8C1	STD–T_A=0°C to 70°C	Commercial, 20MHz	69 Pin Plastic Pin Grid Array	2220H8C1
TMC2221B6C	STD–T_A=0°C to 70°C	Commercial, 17MHz	28 Pin CERDIP	2221B6C
TMC2221B6V	EXT–T_C=–55°C to 125°C	MIL-STD-883, 17MHz	28 Pin CERDIP	2221B6V
TMC2221B6C1	STD–T_A=0°C to 70°C	Commercial, 20MHz	28 Pin CERDIP	2221B6C1
TMC2221B6V1	EXT–T_C=–55°C to 125°C	MIL-STD-883, 20MHz	28 Pin CERDIP	2221B6V1

Fixed-Point Arithmetic



Since the first monolithic multiplier was introduced by TRW LSI Products (now Raytheon) in 1976, and multiplication was changed from something difficult to something easy, this building block has become ubiquitous in the world of signal processing. Raytheon continues to provide the broadest line of fixed-point multipliers, with word sizes from 8 to 16 bits, with and without embedded accumulators.

Bringing the same ease-of-application to another difficult arithmetic problem in signal processing, the TMC3211 Integer Divider produces a 32 bit quotient at 20 million operations/second. Now it is no longer necessary to avoid division in image and signal processing algorithms.

Product	Description	Size	Cycle Time (ns)	Power[1] (Watts)	Package	Grade[2]	Notes
TMC208K-1	Multiplier	8x8	45	0.55	B5, N5	C	Two's complement.
			50	0.55	B5, C2	V, SMD	Compatible with MPY008H.
			65	0.55	B5, N5	V, SMD	
			70	0.55	B5, C2	C, V, SMD	
TMC28KU-1	Multiplier	8x8	45	0.55	B5, N5	C	Unsigned magnitude.
			50	0.55	B5	V, SMD	Compatible with MPY008H.
			65	0.55	B5, N5	C	
			70	0.55	B5	V, SMD	
TMC2208	Multiplier-Accumulator	8x8	40	0.4	J4, N4, R1	C	Compatible with TDC1008.
			50	0.4	J4	V	
TMC2210-95	Multiplier-Accumulator	16x16	95	0.33	N0, J0, G8	C, V	Industry-standard 16-bit MAC.
-80			80	0.33	R1, N0, J0, H8, G8	C, V	
-65			65	0.33	R1, N0, H8, G8	C, V	
-55			55	0.33	R1, N0, H8, G8	C, V	
-45			45	0.33	R1, N0, H8	C, V	
TMC3211	Integer Divider	32-bit	50	0.82	H5	C	32-bit dividend, quotient.

Notes:
1. Guaranteed. See product specifications for test conditions.
2. A = High Reliability, T_C = -55°C to 125°C. C = Commercial, T_A = 0°C to 70°C.
   V = MIL-STD-883 Compliant, T_C = -55°C to 125°C.
   SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C.

TMC208K, TMC28KU
CMOS Multiplier
8 x 8 Bit, 45 ns, 65 ns

Description

The TMC208K and TMC28KU are high-speed 8 x 8 bit parallel multipliers which operate at a 45 or 65 ns cycle time (22.2 or 15.3 MHz multiplication rate). The multiplicand and multiplier are both two's complement numbers in the TMC208K and unsigned magnitude numbers in the TMC28KU, yielding a full precision 16-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are constructed using positive-edge-triggered D-type flip-flops. Built with Raytheon Semiconductor La Jolla's OMICRON-C™ CMOS process, the TMC208K and TMC28KU are pin and function compatible with the MPY008H and MPY08HU yet operate with greater speeds at much less power dissipation.

TMC208K

- Pin compatible with MPY008H
- Two's complement multiplication

TMC28KU

- Pin compatible with MPY08HU
- Unsigned magnitude multiplication

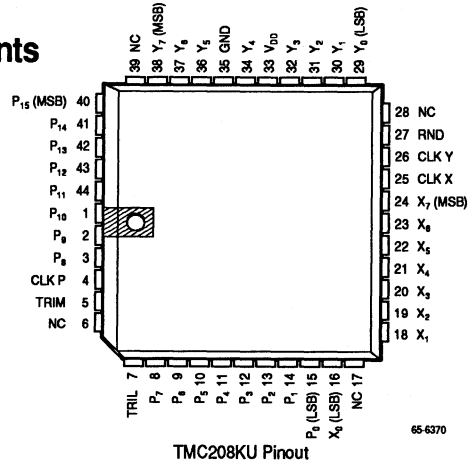
Applications

- Array processors
- Video processors
- Radar signal processors
- FFT processors
- General purpose digital signal processors
- Microcomputer/minicomputer accelerators

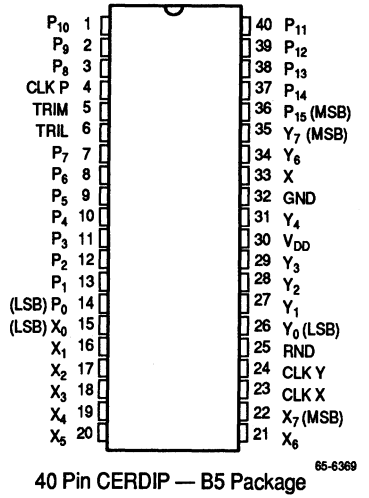
Features

- 45 or 65 ns multiply time
- 8 x 8 bit parallel multiplication with 16-bit product output
- Three-state outputs
- TTL compatible
- Available in an 40-pin CERDIP or plastic DIP

Pin Assignments



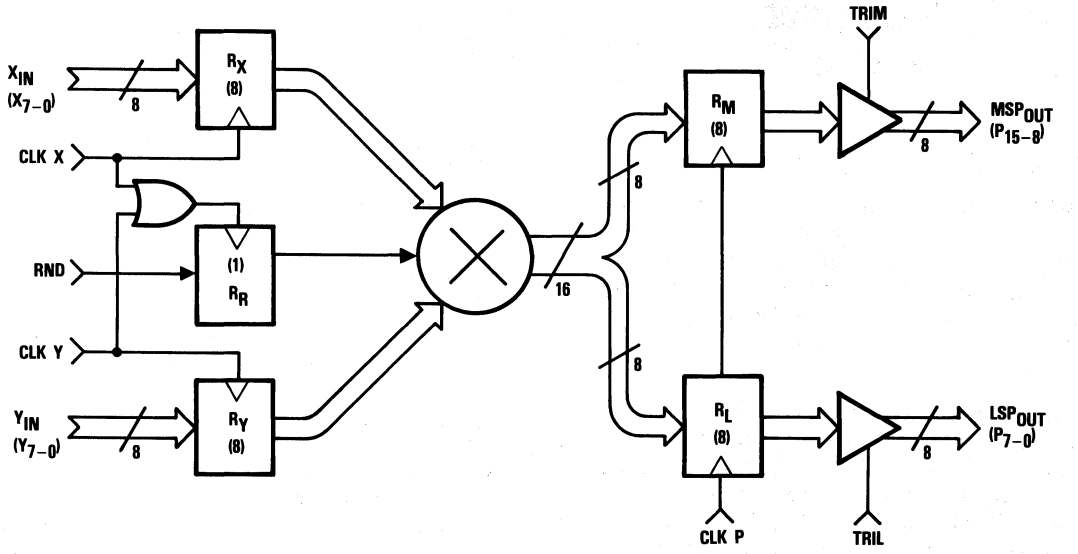
TMC208KU Pinout



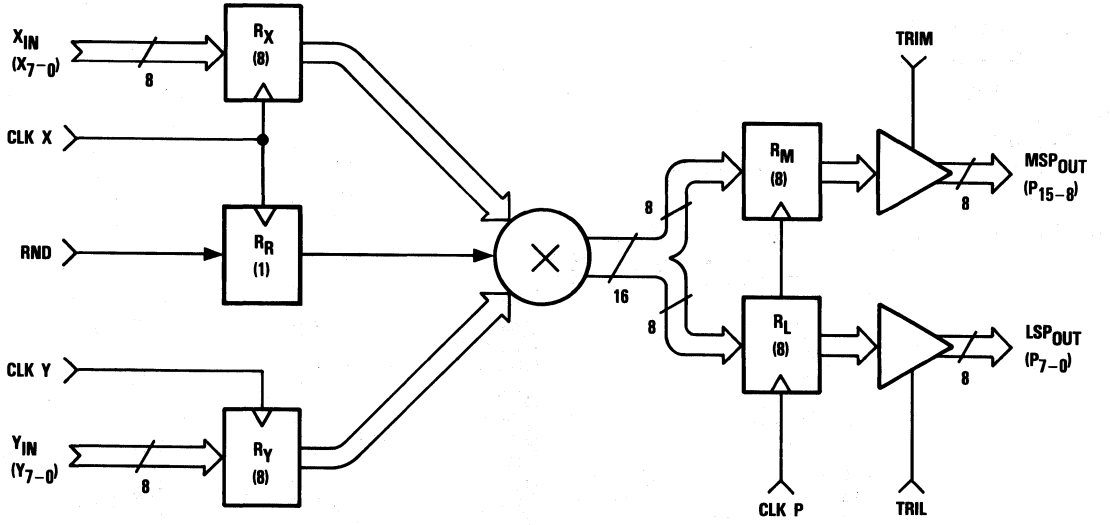
40 Pin CERDIP — B5 Package
40 Pin Plastic DIP — N5 Package

Fixed-Point

TMC208K Functional Block Diagram



TMC28KU Functional Block Diagram



Functional Description

General Information

The TMC208K and TMC28KU have three functional sections: input registers, an asynchronous multiplier array and output registers. The input registers store the two 8-bit numbers which are to be multiplied and the instruction which controls output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders designed to handle two's complement numbers in the TMC208K or unsigned magnitude numbers in the TMC28KU. The output registers hold the product as two 8-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the multipliers to be used on a bus, or allow the MSP and LSP to be multiplexed over the same 8-bit output lines.

Signal Definitions

Power

V_{DD}, GND — The TMC208K and TMC28KU operate from a single +5 Volt supply. All power and ground lines must be connected.

Data Inputs

X_{7-0},Y_{7-0} — The TMC208K has two 8-bit two's complement data inputs labeled X and Y. The TMC28KU has two 8-bit unsigned magnitude data inputs labeled X and Y. The Most Significant Bits (MSBs), X_7 and Y_7, carry the sign information for the two's complement notation in the TMC208K. The remaining bits are X_{6-0} and Y_{6-0} with X_0 and Y_0 the LSBs. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown in Figures 1 through 4.

Data Outputs

P_{15-0} — The TMC208K has a 16-bit two's complement output which is the product of the two input X and Y values. The TMC28KU has a 16-bit unsigned magnitude output which is the product of the two input X and Y values. This output is divided into two 8-bit output words, the MSP and LSP. The MSB of both the MSP and the LSP is the sign bit in the TMC208K. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown in Figures 1 through 4. Note that since +1 cannot be exactly represented in fractional two's complement notation, some provision for handling the case (-1) x (-1) must be made. The TMC208K outputs a -1 in this case. As a result, external error handling provisions may be required.

Clocks

CLK X, CLK Y, CLK P — The TMC208K and TMC28KU have three clock lines, one for each input register (CLK X and CLK Y) and one for the product register (CLK P). Data present at the inputs of these registers are loaded into the registers on the rising edge of the appropriate clock. In the TMC208K, the RND input is registered and clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks. In the TMC28KU, the RND input is registered and clocked in on the rising edge of CLK X.

Controls

TRIM, TRIL — TRIM and TRIL are the three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when LOW. TRIM and TRIL are not registered.

RND — When RND (Round) is HIGH, a one is added to the MSB of the LSP. A one will be added to the P_6 bit in the 208K or to the P_7 bit in the 28KU. Note that rounding always occurs in the positive direction. In some applications this may introduce a systematic bias. The RND input is registered and used when a rounded 8-bit product is desired.

Fixed-Point

Package Interconnections

Signal Type	Signal Name	Function	B5, N5 Package
Power	V_{DD}	Supply Voltage	30
	GND	Ground	32
Data Inputs	X_{7-0}	X Input Word	22–15
	Y_{7-0}	Y Input Word	35–33, 31, 29–26
Data Outputs	P_{15-8}	MSP Output	36–40, 1–3
	P_{7-0}	LSP Output	7–14
Clocks	CLK X	X Register Clock	23
	CLK Y	Y Register Clock	24
	CLK P	Product Register Clock	4
Controls	TRIM	MSP Three-State	5
	TRIL	LSP Three-State	6
	RND	Round	25

Figure 1. Fractional Two's Complement Notation (TMC208K)

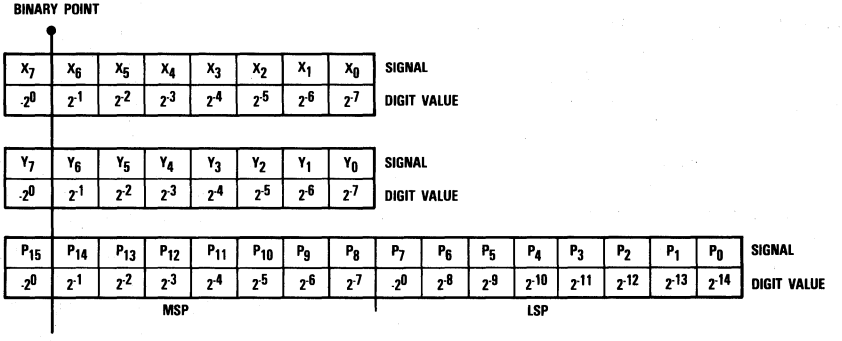


Figure 2. Integer Two's Complement Notation (TMC208K)

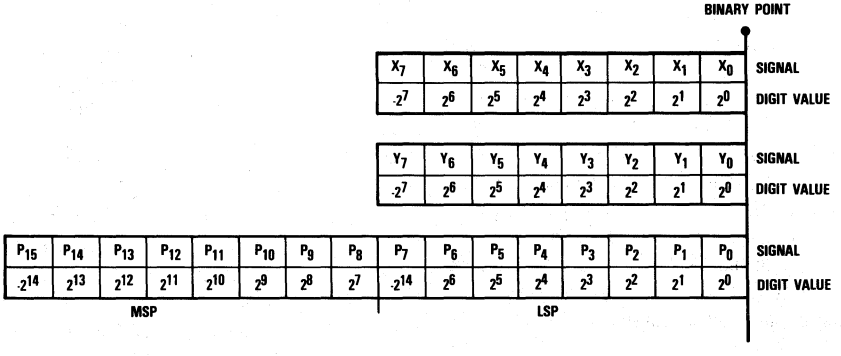


Figure 3. Fractional Unsigned Magnitude Notation (TMC28KU)

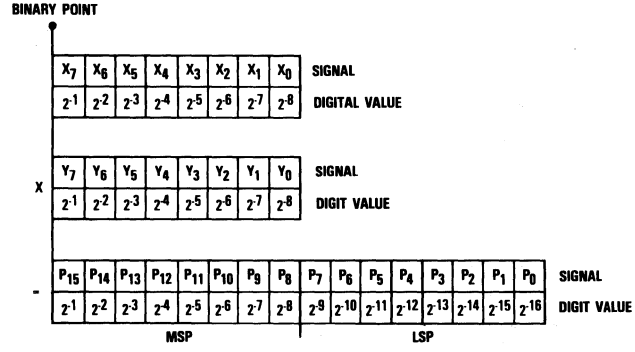


Figure 4. Integer Unsigned Magnitude Notation (TMC28KU)

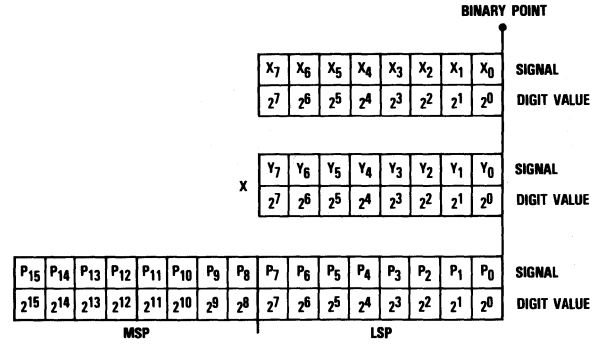


Figure 5. Timing Diagram

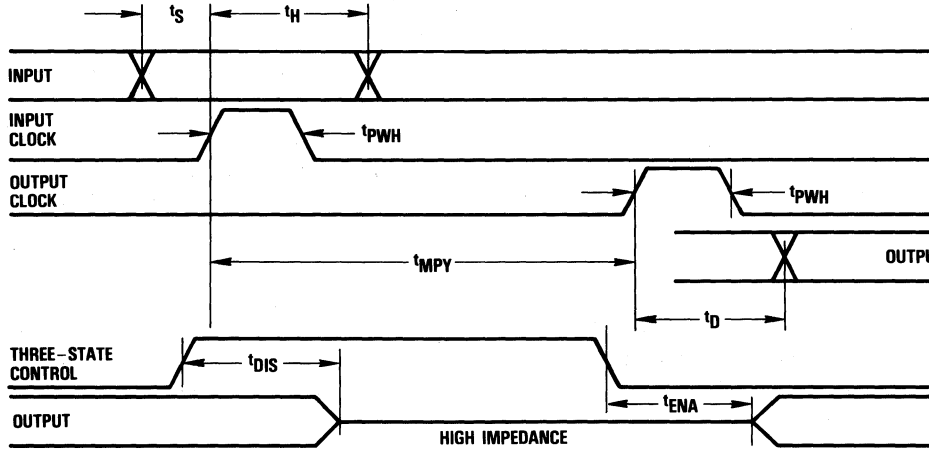


Figure 6. Equivalent Input Circuit

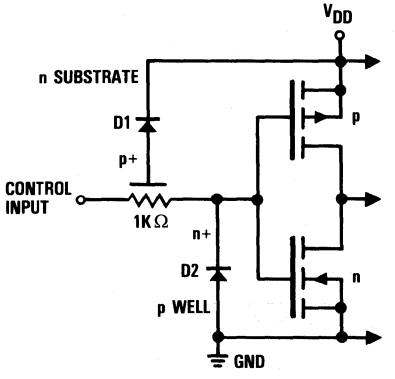


Figure 7. Equivalent Output Circuit

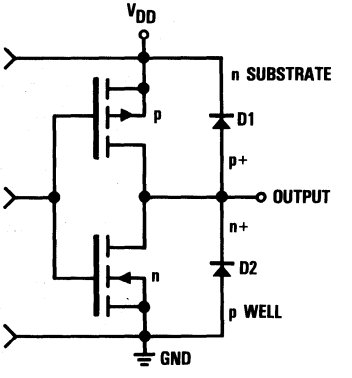
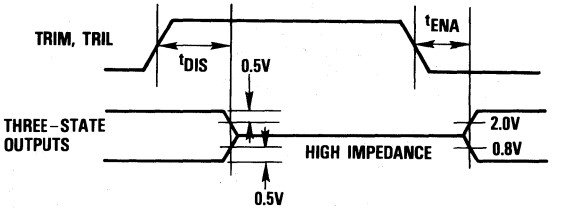


Figure 8. Threshold Levels For Three–State Measurements



Application Discussion

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, the TMC208K and TMC28KU do not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer or fractional notation. If integer notation is used, the LSBs of the multiplier, multiplicand and product all have the same value. If fractional notation is used, the MSBs of the multiplier, multiplicand and product all have the same value.

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, TRIM, TRIL = 5V, f = 10MHz		50		50	mA
		V_{DD} = Max, TRIM, TRIL = 5V, f = 22MHz		100		100	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. 2f = 20 MHz for ETR.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MPY}	Multiply Time	V_{DD} = Min					
		TMC208K, TMC28KU		65		70	ns
		TMC208K-1, TMC28KU-1		45		50	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15		15		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15		15		ns
t_S	Input Setup Time	TMC208K, TMC28KU	25		30		ns
		TMC208K-1, TMC28KU-1	20		25		ns
t_H	Input Hold Time		0		0		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		25		30	ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		20		25	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		20		25	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−1.0 to 6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
TMC208KB5C	STD - T_A = 0 to 70°C	Commercial	40-pin CERDIP	208KB5C
TMC208KB5C1	STD - T_A = 0 to 70°C	Commercial	40-pin CERDIP	208KB5C1
TMC208KB5V	EXT - T_C = -55 to 125°C	MIL-STD-883	40-pin CERDIP	208KB5V
TMC208KB5V	EXT - T_C = -55 to 125°C	MIL-STD-883	40-pin CERDIP	208KB5V1
TMC208KN5C	STD - T_A = 0 to 70°C	Commercial	40-pin Plastic DIP	208KN5C
TMC208KN5C1	STD - T_A = 0 to 70°C	Commercial	40-pin Plastic DIP	208KN5C1
TMC28KUB5C	STD - T_A = 0 to 70°C	Commercial	40-pin CERDIP	28KUB5C
TMC28KUB5C1	STD - T_A = 0 to 70°C	Commercial	40-pin CERDIP	28KUB5C1
TMC28KUB5V	EXT - T_C = -55 to 125°C	MIL-STD-883	40-pin CERDIP	28KUB5V
TMC28KUB5V1	EXT - T_C = -55 to 125°C	MIL-STD-883	40-pin CERDIP	28KUB5V1
TMC28KUN5C	STD - T_A = 0 to 70°C	Commercial	40-pin Plastic DIP	28KUN5C
TMC28KUN5C1	STD - T_A = 0 to 70°C	Commercial	40-pin Plastic DIP	28KUN5C1
TMC208KR2C	STD - T_A = 0 to 70°C	Commercial	44 J-Lead PLCC	208KR2C
TMC208KR2C1	STD - T_A = 0 to 70°C	Commercial	44 J-Lead PLCC	208KR2C1
TMC28KUR2C	STD - T_A = 0 to 70°C	Commercial	44 J-Lead PLCC	**28KUR2C**
TMC28KUR2C1	STD - T_A = 0 to 70°C	Commercial	44 J-Lead PLCC	**28KUR2C1**

40G05076 Rev D 8/93

TMC2208
CMOS Multiplier-Accumulator
8 x 8 Bit, 40 ns

Description

The TMC2208 is a high-speed 8 x 8 bit parallel multiplier-accumulator which operates at a 40 ns cycle time (25 MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 16-bit product. Products may be accumulated to a 19-bit result.

Individually clocked input and output registers are used to provide maximum system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), an 8-bit Most Significant Product (MSP). Individual three-state output ports are provided for the XTP, MSP, and LSP. The output register can be preloaded directly via the output ports.

The TMC2208 is pin and function compatible with the TDC1008 in the 48-pin DIP. Built with Raytheon Semiconductor La Jolla's OMICRON-CC™ one micron CMOS process, power consumption is greatly reduced.

Features

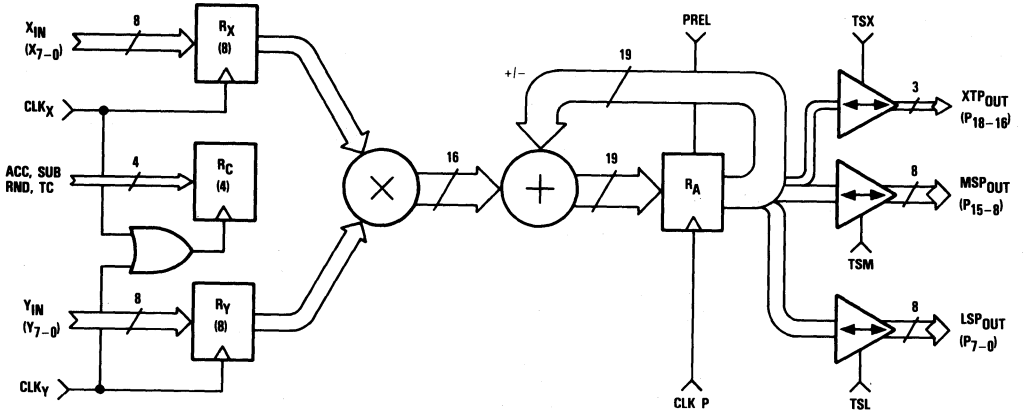
- Function compatible with the TDC1008 (pin compatible in 48-pin DIP package)
- 40 ns multiply-accumulate time (worst case commercial)
- 8 x 8 parallel multiplication with accumulation to 19-bit result
- Selectable accumulation, subtraction, rounding, and accumulator preload
- All inputs and outputs are registered and TTL compatible
- Three-state outputs
- Two's complement or unsigned magnitude operation
- Single +5V power supply
- Low power CMOS construction
- Available in 48-pin ceramic or plastic DIP and PLCC

Applications

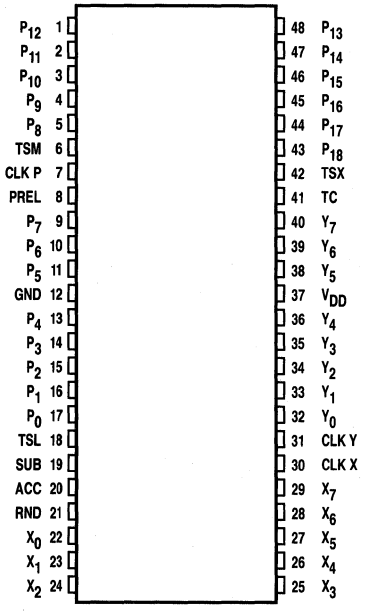
- Array processors
- Video processors
- Radar signal processors
- FFT processors
- General purpose digital signal processors
- Micro/mini-computer

Fixed-Point

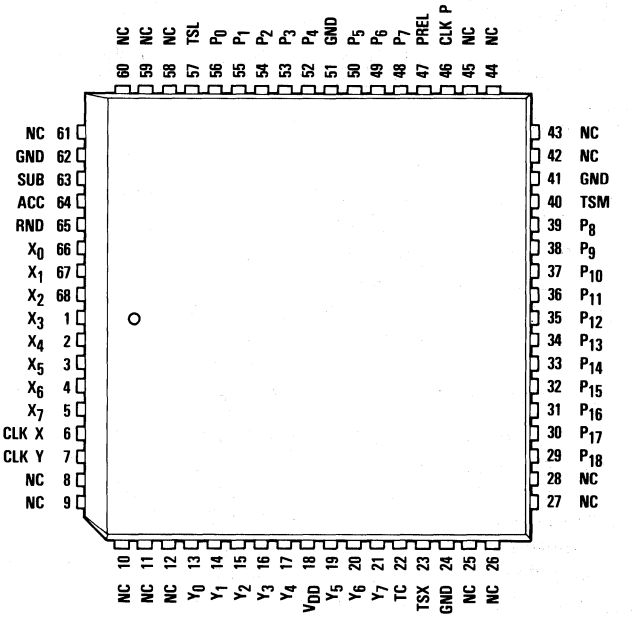
Functional Block Diagram



Pin Assignments



48 Pin Hermetic Ceramic DIP – J4 Package
48 Pin Ceramic DIP – N4 Package



68 Leaded Plastic Chip Carrier – R1 Package

Functional Description

General Information

The TMC2208 consists of four functional sections: input registers, an asynchronous multiplier array, an adder and output registers. The input registers store the two 8-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each input is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 8-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP) and the eXTended Product (XTP). Three-state output drivers permit the TMC2208 to be used on a bus, or allow the outputs to be multiplexed over the same 8-bit output lines.

Signal Definitions

Power

VDD, GND — The TMC2208 operates from a single +5V supply. All power and ground lines must be connected.

Data Inputs

X_{7-0} — The 8-bit two's complement or unsigned magnitude X data input. X_7 is the MSB and contains the sign information for two's complement notation. The data on the X input is clocked into the input register on the rising edge of CLK X.

Y_{7-0} — The 8-bit two's complement or unsigned magnitude Y data input. Y_7 is the MSB and contains the sign information for two's complement notation. The data on the Y input is clocked into the input register on the rising edge of CLK Y.

Data Outputs

P_{18-0} — P_{18-0} is the accumulated product result for the TMC2208. The 19-bit output is either the two's complement or unsigned magnitude result of the accumulated products. The output is divided into two 8-bit output words (MSP, LSP) and one 3-bit output word (XTP). P_{18} is the MSB and contains the sign information for two's complement notation. Formats for two's complement, fractional unsigned magnitude, integer two's complement and integer unsigned notation are shown in ***Figures 1 through 4***.

Clocks

CLK X, CLK Y — The rising edge of CLK X (CLK Y) loads the data lines into the appropriate input register. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) control inputs are registered and loaded on the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems can be avoided by the use of normally LOW clocks.

CLK P — CLK P is used to clock the accumulated product sum into the output register. If ACC is HIGH, the content of the output register is added to the next product generated and loaded into the output register. CLK P is also used to preload the output register from the output pins (see ***Table 1***).

Controls

TSX, TSM, TSL — TSX is the three-state control for the 3-bit XTP output drivers. TSM and TSL are the three-state controls for the MSP and LSP outputs respectively. The outputs are in the high-impedance state when the control is HIGH, and enabled when the control is LOW.

PREL — PRELoad is the active-HIGH control used to directly load the output register (see ***Table 1***). When PREL is HIGH, all output buffers are forced into the high-impedance state. Second, when any or all the the TSX, TSM and TSL controls is also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded.

RND — The RouND input is used to control the rounding of results. When RND is HIGH, a 1 is added to the Most Significant Bit (MSB) of the LSP for rounding the product in the MSP and XTP rather than truncating it. This control is used to improve accuracy when the LSP will not be used.

TC — The Two's Complement input is used to control how the TMC2208 interprets the data on the X and Y inputs. TC HIGH makes both inputs two's complement, while TC LOW makes both inputs unsigned magnitude numbers.

ACC — When ACCumulate is HIGH, the content of the output register is added or subtracted from the next product generated, and their sum stored back into the output register on the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.

SUB — SUBtract is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

Package Interconnections

Signal Type	Signal Name	Function	J4, N4 Package Pins	R1 Package Pins
Power	V_{DD}	Supply Voltage	37	18
	GND	Ground	12	24, 41, 51, 62
Data Input	X_{7-0}	X Input Data	29, 28, 27, 26, 25, 24, 23, 22	5, 4, 3, 2, 1, 68, 67, 66
	Y_{7-0}	Y Input Data	40, 39, 38, 36, 35, 34, 33, 32	21, 20, 19, 17, 16, 15, 14, 13
Data Outputs	P_{18-0}	Product Output Data	43, 44, 45, 46, 47, 48, 1, 2, 3, 4, 5, 9, 10, 11, 13, 14, 15, 16, 17	29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 48, 49, 50, 52, 53, 54, 55, 56
Clock	CLK X	X Input Clock	30	6
	CLK Y	Y Input Clock	31	7
	CLK P	Output Register Clock	7	46
Control	TSX	XTP Three-State Control	42	23
	TSM	MSP Three-State Control	6	40
	TSL	LSP Three-State Control	18	57
	PREL	Preload Output Register	8	47
	RND	Round MSP of Product	21	65
	TC	Two's Complement Control	41	22
	ACC	Accumulate Control	20	64
	SUB	Subtract Control	19	63
No Connect	NC	Unused		8, 9, 10, 11, 12, 25, 26, 27, 28, 28, 42, 43, 44, 45, 58, 59, 60, 61

Preload Truth Table

PREL [1]	TSX [1]	TSM [1]	TSL [1]	XTP	MSP	LSP
L	L	L	L	Register → Output Pin	Register → Output Pin	Register → Output Pin
L	L	L	H	Register → Output Pin	Register → Output Pin	Hi-Z
L	L	H	L	Register → Output Pin	Hi-Z	Register → Output Pin
L	L	H	H	Register → Output Pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register → Output Pin	Register → Output Pin
L	H	L	H	Hi-Z	Register → Output Pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register → Output Pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H [2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H [2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H [2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H [2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H [2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H [2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H [2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H [2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes: 1. PREL, TSX, TSM and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Figure 1. Fractional Two's Complement Notation

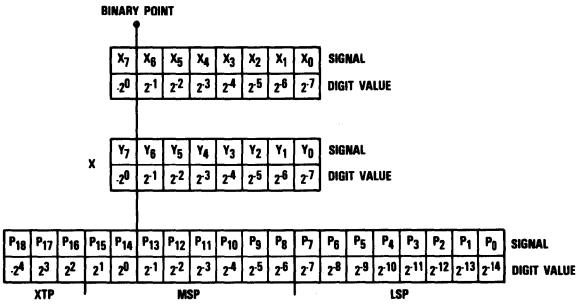


Figure 2. Fractional Unsigned Magnitude Notation

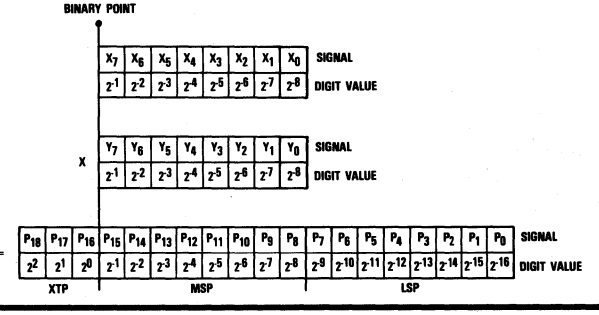


Figure 3. Integer Two's Complement Notation

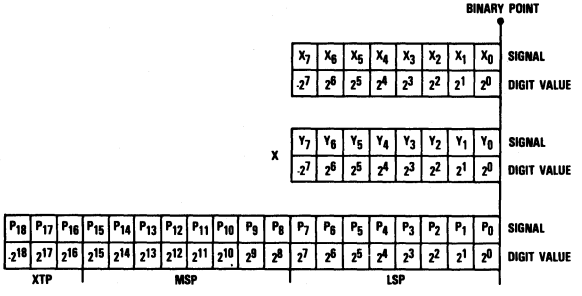
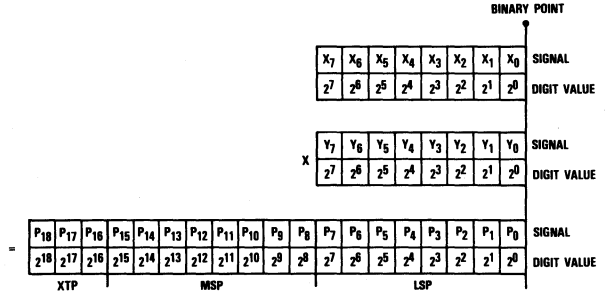


Figure 4. Integer Unsigned Magnitude Notation



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+0.5)V

Output

Applied voltage [2] ..... −0.5 to (V_{DD}+0.5)V

Forced current [3,4] ..... −1.0 to +6.0mA

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... +175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width HIGH	15			15			ns
t_S	Input Setup Time (Except PREL)	10			11			ns
t_S	Input Setup Time (PREL)	12			13			ns
t_H	Input Hold Time	0			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V TSL, TSM, TSX=5V		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=25MHz TSL, TSM, TSX=5V		30		35	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=−2mA	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.		−100		−100	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		15		15	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		15		15	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{DD}=Min		40		50	ns
t_D	Output Delay	V_{DD}=Min, Load=40pF		23		25	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD}=Min, Load=40pF		19		21	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD}=Min, Load=40pF		16		18	ns

Notes: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Figure 5. Timing Diagram

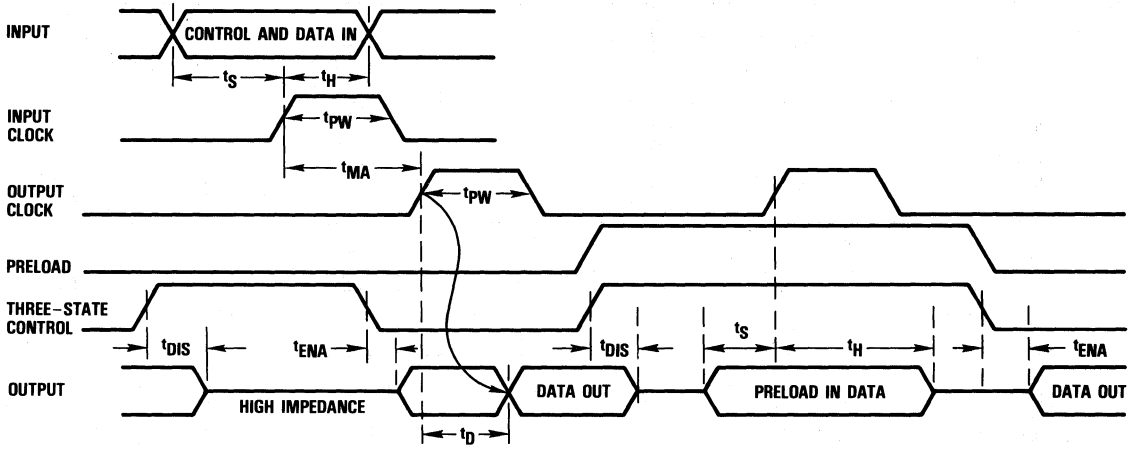


Figure 6. Equivalent Input Circuit

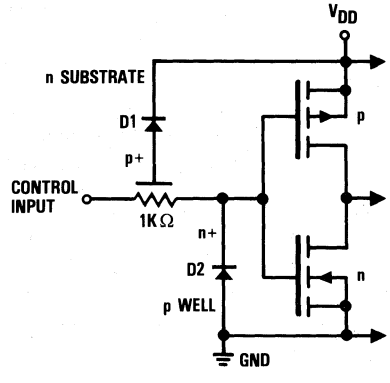
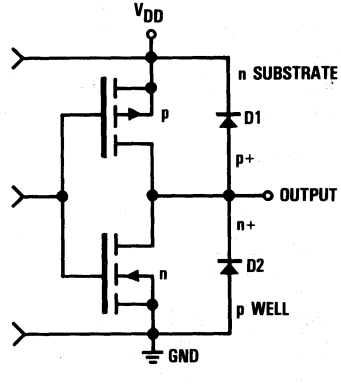


Figure 7. Equivalent Output Circuit



Application Notes

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and the register not be loaded again until a new constant is required. The multiply cycle then consists of loading new data into the remaining input register and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, the TMC2208 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in *Figures 1 through 4.*

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2208J4C	STD–T_A=0°C to 70°C	Commercial	48 Pin Hermetic Ceramic DIP	2208J4C
TMC2208J4V	EXT–T_C= –55°C to 125°C	MIL-STD-883C	48 Pin Hermetic Ceramic DIP	2208J4V
TMC2208N4C	STD–T_A=0°C to 70°C	Commercial	48 Pin Plastic DIP	2208N4C
TMC2208R1C	STD–T_A=0°C to 70°C	Commercial	68 Leaded Plastic Chip Carrier	2208R1C

40G05581 Rev D 8/93

TMC2210
CMOS Multiplier-Accumulator
16 x 16 Bit, 65, 80, 95 ns

Description

The TMC2210 is a high-speed 16 x 16 bit digital multiplier-accumulator which is available in speed bins of 65, 80 or 95 ns. Input data may be specified as two's complement or unsigned magnitude, yielding a 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are constructed using positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit Extended Product (XTP), a 16-bit Most Significant Product (MSP) and a 16-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP and MSP. The LSP is multiplexed with the Y operand inputs. The output register can be preloaded directly via the output ports.

The TMC2210 is a drop in replacement for the TMC2010 and the TMC2110, and is pin and function compatible with the industry standard Raytheon Semiconductor La Jolla TDC1010, the LMA1010/2010, IDT7210 and CY7510.

Features

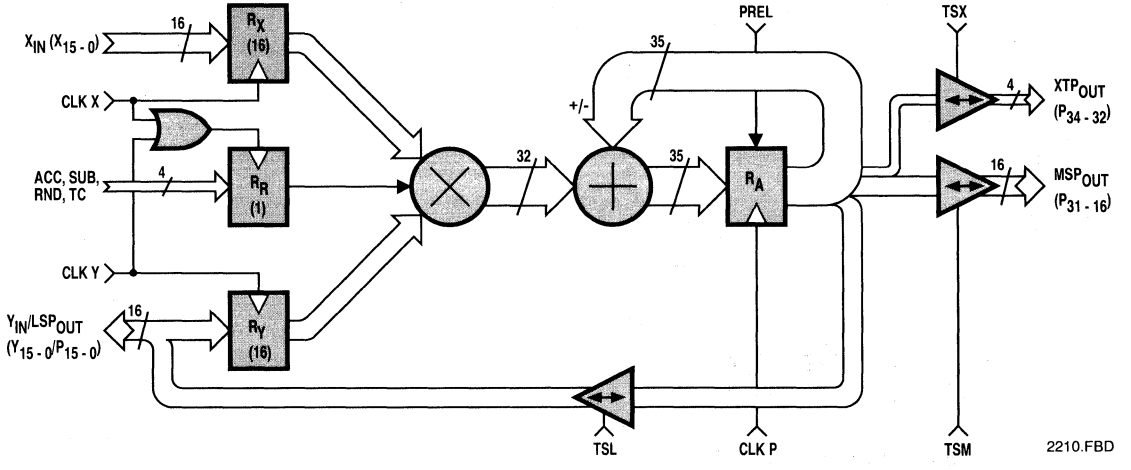
- 65, 80 or 95 ns multiply-accumulate time
- 16 x 16 parallel multiplication with accumulation to 35-bit result
- Selectable accumulation, subtraction, rounding, and accumulator preload
- Two's complement or unsigned magnitude operation
- All inputs and outputs are registered and TTL compatible
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 64-pin ceramic or plastic DIP, 68-pin grid array and 68-lead plastic J-leaded chip carrier

Applications

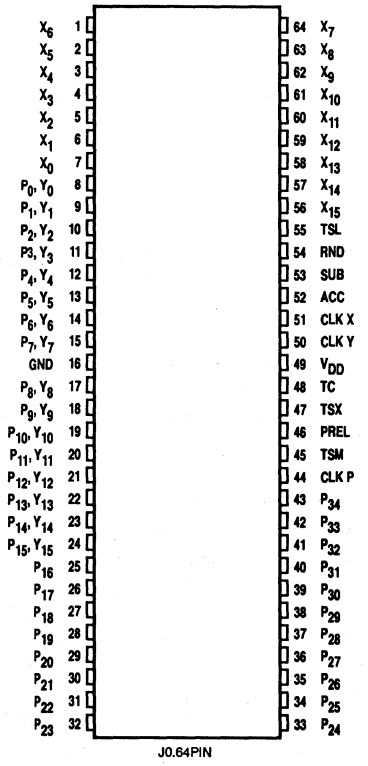
- Array processors
- Video processors
- Radar signal processors
- FFT processors
- General purpose digital signal processors
- Microcomputer/minicomputer accelerators

Fixed-Point

Functional Block Diagram

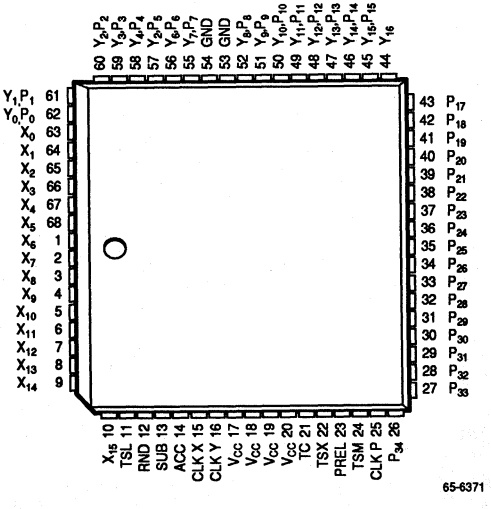


Pin Assignments



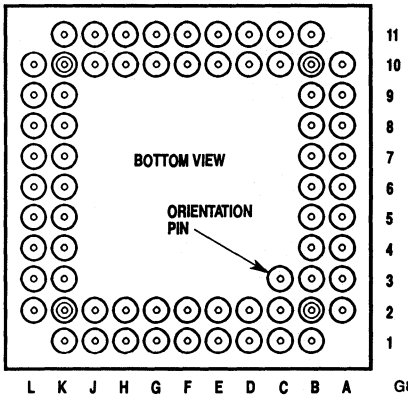
J0.64PIN

64 Pin Hermetic Ceramic DIP – J0, NO Package



65-6371

68-Lead Plastic J-Leaded chip Carrier — R1 Package



G8.69PIN/H8.69PIN

68 Pin Ceramic (G8) or Plastic (H8) Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	X_{12}	F10	V_{DD}	K4	P_{20}
A3	P_0, Y_0	B10	X_{14}	F11	CLK Y	K5	P_{22}
A4	X_1	B11	NC	G1	P_{11}, Y_{11}	K6	P_{24}
A5	X_3	C1	P_4, Y_4	G2	P_{10}, Y_{10}	K7	P_{26}
A6	X_5	C2	P_3, Y_3	G10	TSX	K8	P_{28}
A7	X_7	C10	TSL	G11	TC	K9	P_{30}
A8	X_9	C11	X_{15}	H1	P_{13}, Y_{13}	K10	P_{32}
A9	X_{11}	D1	P_6, Y_6	H2	P_{12}, Y_{12}	K11	P_{33}
A10	X_{13}	D2	P_5, Y_5	H10	TSM	L2	P_{17}
B1	P_2, Y_2	D10	SUB	H11	PREL	L3	P_{19}
B2	P_1, Y_1	D11	RND	J1	P_{15}, Y_{15}	L4	P_{21}
B3	X_0	E1	GND	J2	P_{14}, Y_{14}	L5	P_{23}
B4	X_2	E2	P_7, Y_7	J10	P_{34}	L6	P_{25}
B5	X_4	E10	CLK X	J11	CLK P	L7	P_{27}
B6	X_6	E11	ACC	K1	NC	L8	P_{29}
B7	X_8	F1	P_9, Y_9	K2	P_{16}	L9	P_{31}
B8	X_{10}	F2	P_8, Y_8	K3	P_{18}	L10	NC

Functional Description

General Information

The TMC2210 consists of four functional sections: input registers, an asynchronous multiplier array, an adder and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array uses a modified Booth's algorithm and has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words and one 3-bit word: the MSP, the LSP and the XTP. Three-state output drivers permit the TMC2210 to be used on a bus or allow the outputs to be multiplexed over the same 16-bit output lines. The LSP is multiplexed with the Y input.

The TMC2210 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers are loaded into the registers on the rising edge of the appropriate clock. The Round (RND), Two's Complement (TC), Accumulate (ACC) and Subtract (SUB) inputs are registered and all four bits are clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Signal Definitions

Power

V_{DD}, GND — The TMC2210 operates from a single +5V supply. All power and ground lines must be connected.

Data Inputs

X_{15-0}, Y_{15-0} — There are two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information when two's complement notation is used. The remaining bits are denoted X_{14-0} and Y_{14-0} (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers on the rising edge of the appropriate clock.

Data Outputs

P_{34-0} — There is a 35-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 16-bit output words, the MSP and LSP, and one 3-bit output word, the XTP. The MSB of the XTP is the sign bit if two's complement notation is used.

Clocks

CLK X, CLK Y, CLK P — CLK X is the clock input for the X_{15-0} data register. CLK Y is the clock input for the Y_{15-0} data register. CLK P is the clock input for the product register.

Controls

TSX, TSM, TSL — TSX, TSM and TSL are three-state enable lines for the XTP, the MSP and the LSP, respectively. The output driver is in the high-impedance state when TSX, TSM or TSL is HIGH and enabled when the appropriate control is LOW.

PREL — PREL (Preload) is an active HIGH control which has several effects when active. First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL) and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RND — RND (Round) controls the addition of a one to the MSB of the LSP for rounding. When RND is HIGH, a one is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating.

Controls (cont.)

TC — TC (Two's Complement) controls how the device interprets data on the X and Y inputs. When TC is HIGH, both inputs are two's complement inputs. When TC is LOW, both inputs are unsigned magnitude only inputs. The necessary sign extension for negative two's complement numbers is provided internally.

ACC — When ACC (Accumulate) is HIGH, the content of the output register is added to or subtracted from the next product generated, and the result is stored back into the output registers on the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated will be stored into the output registers directly. This operation is used for the first term in a summation to eliminate the need for a separate "clear" operation.

SUB — The SUB (Subtract) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated, and the difference is stored back into the output register. When ACC is HIGH and SUB is LOW, the content of the output register is added to the next product generated and the sum is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

No Connects

NC — The pin grid array version of the TMC2210 has four pins which are not connected internally.

Package Interconnections

Signal Type	Signal Name	Function	G8, H8 Package Pins	J0, N0 Package Pins	R1 Package Pins
Power	V_{DD}	Supply Voltage	F10	49	17, 18, 19, 20
	GND	Ground	E1	16	53, 54
Data Inputs	X_{15-0}	X Input Word	C11, B10, A10, B9, A9, B8, A8, B7, A7, B6, A6, B5, A5, B4, A4, B3	56-64, 1-7	1-10, 63-68
	Y_{15-0}	Y Input Word	J1, J2, H1, H2, G1, G2, F1, F2, E2, D1, D2, C1, C2, B1, B2, A3	24-17, 15-8	45-52, 55-62
Data Outputs	P_{34-0}	Product Output	J10, K11, K10, L9, K9, L8, K8, L7, K7, L6, K6, L5, K5, L4, K4, L3, K3, L2, K2, J1, J2, H1, H2, G1, G2, F1, F2, E2, D1, D2, C1, C2, B1, B2, A3	43-17, 15-8	26-52, 55-62
Clocks	CLK X	X Register Clock	E10	51	15
	CLK Y	Y Register Clock	F11	50	16
	CLK P	P Regsiter Clock	J11	44	25
Controls	TSX	XTP Three-State	G10	47	22
	TSM	MSP Three-State	H10	45	24
	TSL	LSP Three-State	C10	55	11
	PREL	Preload	H11	46	23
	RND	Round	D11	54	12
	TC	Two's Complement	G11	48	21
	ACC	Accumulate	E11	52	14
	SUB	Subtract	D10	53	13
No Connects	NC	No Connection	K1, L10, B11, A2	–	–

Figure 1. Fractional Two's Complement Notation

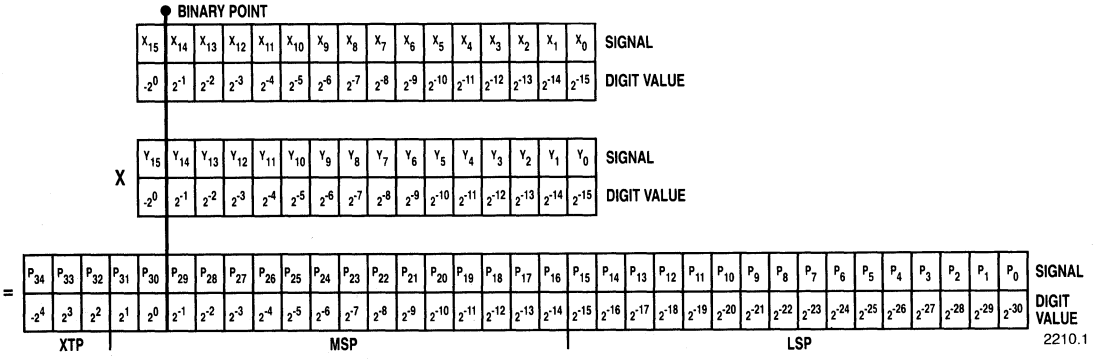


Figure 2. Fractional Unsigned Magnitude Notation

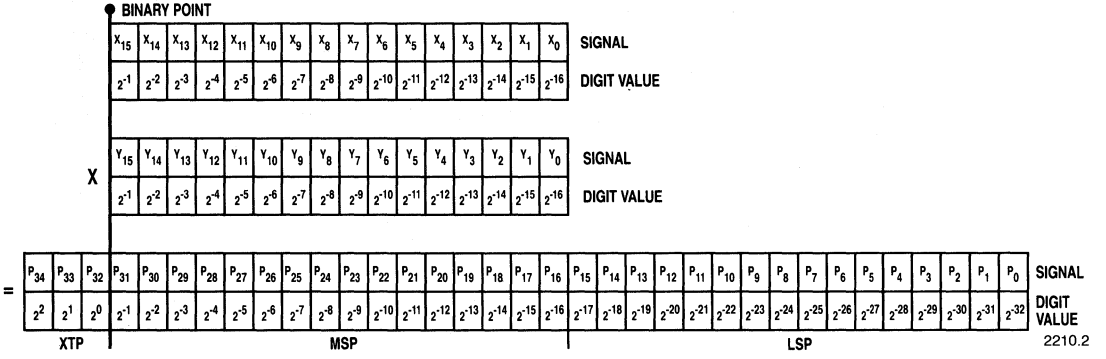
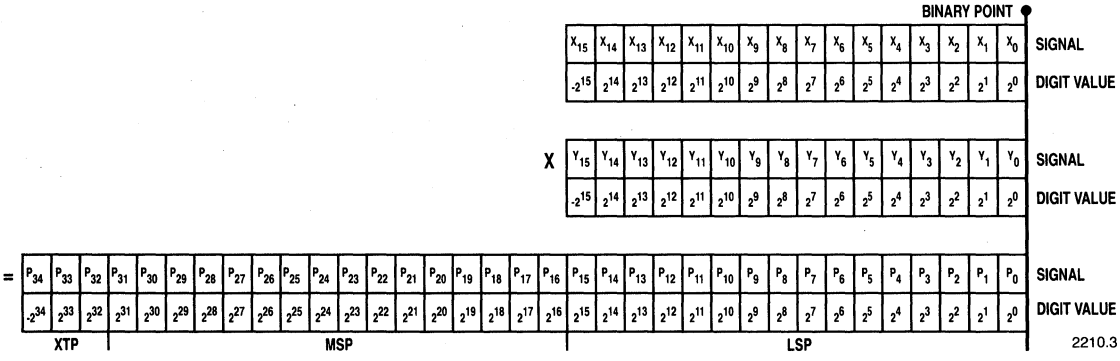


Figure 3. Integer Two's Complement Notation



Fixed-Point

Figure 4. Integer Unsigned Magnitude Notation

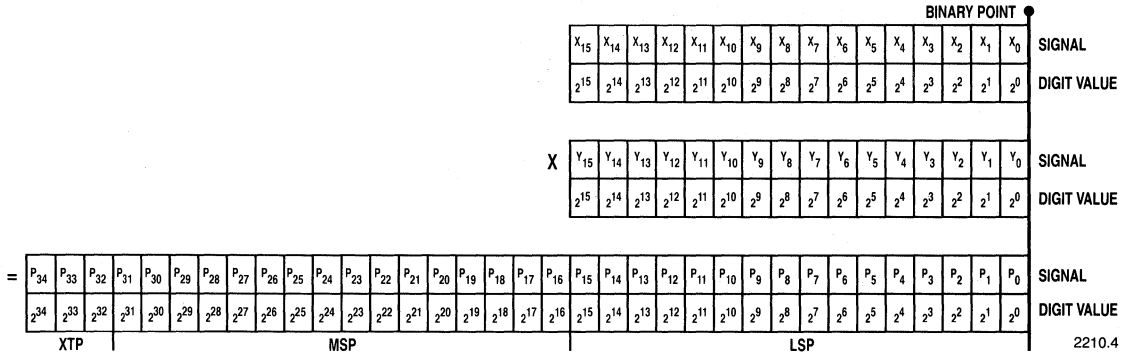


Figure 5. Timing Diagram

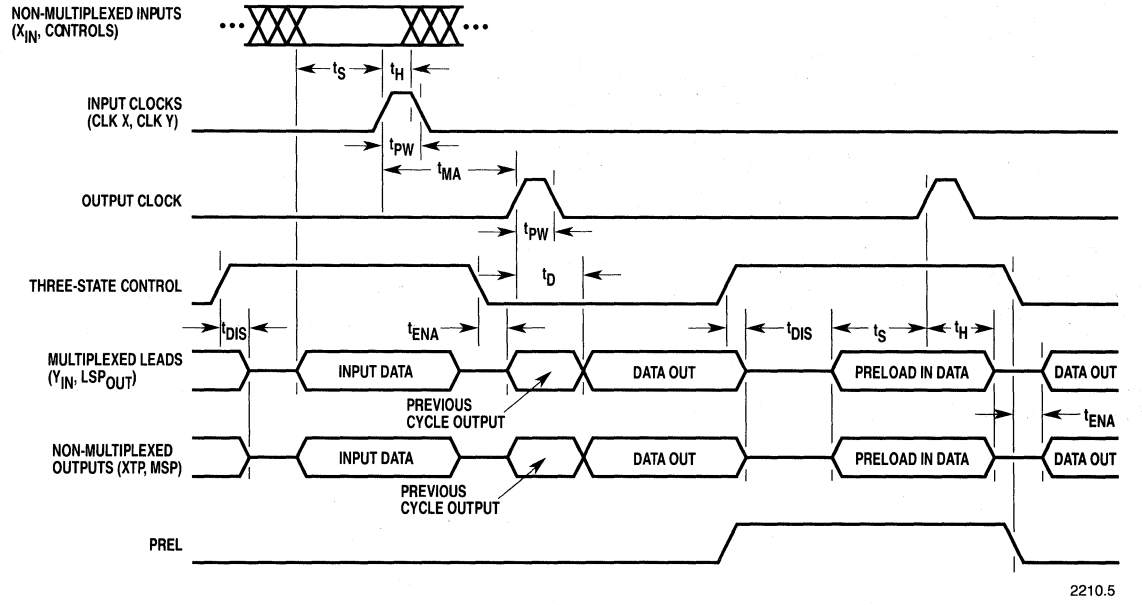


Figure 6. Equivalent Input Circuit

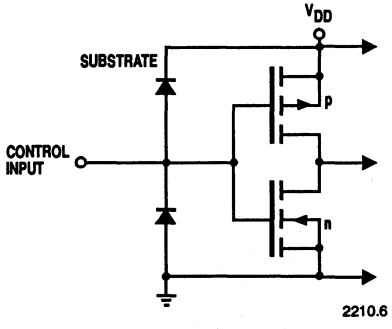


Figure 7. Equivalent Output Circuit

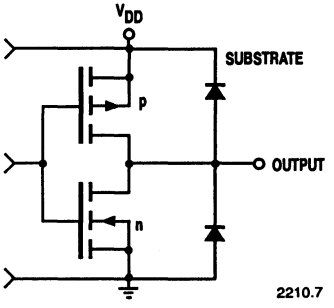
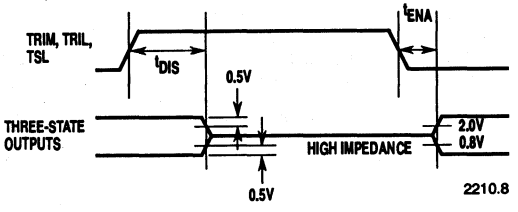


Figure 8. Threshold Levels for Three-State Measurements



Preload Truth Table

PREL[1, 2]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
0	0	0	0	Register → Output Pin	Register → Output Pin	Register → Output Pin
0	0	0	1	Register → Output Pin	Register → Output Pin	Hi-Z
0	0	1	0	Register → Output Pin	Hi-Z	Register → Output Pin
0	0	1	1	Register → Output Pin	Hi-Z	Hi-Z
0	1	0	0	Hi-Z	Register → Output Pin	Register → Output Pin
0	1	0	1	Hi-Z	Register → Output Pin	Hi-Z
0	1	1	0	Hi-Z	Hi-Z	Register → Output Pin
0	1	1	1	Hi-Z	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Hi-Z	Hi-Z
1	0	0	1	Hi-Z	Hi-Z	Hi-Z Preload
1	0	1	0	Hi-Z	Hi-Z Preload	Hi-Z
1	0	1	1	Hi-Z	Hi-Z Preload	Hi-Z Preload
1	1	0	0	Hi-Z Preload	Hi-Z	Hi-Z
1	1	0	1	Hi-Z Preload	Hi-Z	Hi-Z Preload
1	1	1	0	Hi-Z Preload	Hi-Z Preload	Hi-Z
1	1	1	1	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes: 1. PREL, TSX, TSM, and TSL are not registered.
2. When PREL is HIGH, any change of output register (for those outputs in which the three-state control is LOW) is inhibited.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Outputs	
Applied voltage	−0.5 to (V_{DD} + 0.5)V [2]
Forced current	−1.0 to 6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

		Temperature Range						
		Commercial			Military			
Parameter		**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Units**
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions

Parameter		Conditions	Temperature Range				Units
			Commercial		Military		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V					
		All Except		5		10	mA
		TMC2210-45, -55, Outputs Open		0.5		0.5	mA
I_{DDO}	Supply Current, Unloaded [1]	V_{DD} = Max, TSL, TSM, TSX = 5V					
		f = 15MHz		75		75	mA
		f = 10MHz		50		50	mA
		f = 6.2MHz		30		30	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V					
		X_{15-0}, Controls, Clocks		−10		−10	mA
		P_{15-0}, Y_{15-0}		−40		−40	mA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}					
		X_{15-0}, Controls, Clocks		10		10	mA
		P_{15-0}, Y_{15-0}		40		40	mA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = +4.0mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = −400μA	2.6		2.6		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		−40		−40	μA
C_I	Input Capacitance	f = 1.0MHz, T_A = 25°C		10		10	pF
C_O	Output Capacitance	f = 1.0MHz, T_A = 25°C		10		10	pF
$C_{I/O}$	I/O Capacitance	f = 1.0MHz, T_A = 25°C		15		15	pF

Note: 1. Supply current is proportional to f_{CLK}, typically 5mA per MHz.

AC characteristics within specified operating conditions [1]

Parameter		Conditions	Temperature Range				Units
			Commercial		Military		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	TMC2210-95		95		95	ns
		TMC2210-80		80		80	ns
		TMC2210-65		65		65	ns
t_{PWL}	Clock Pulse Width, LOW	TMC2210-95	15		15		ns
		TMC2210-80	15		15		ns
		TMC2210-65	15		25		ns
t_{PWH}	Clcok PUlse Width, HIGH	TMC2210-95	15		15		ns
		TMC2210-80	15		15		ns
		TMC2210-65	15		25		ns

Notes: 1. All transitions are measured at a 1.5V level except t_{ENA} and t_{DIS} which are measured as shown in Figure 8.
2. V_{DD} = Min.

Fixed-Point

AC characteristics within specified operating conditions [1](cont.)

Parameter		Conditions	Temperature Range				Units
			Commercial		Military		
			Min	Max	Min	Max	
t_S	Input Setup Time	Data, ACC, SUB, RND, TC					
		TMC2210-95	20		20		ns
		TMC2210-80	20		20		ns
		TMC2210-65	15		25		ns
		PREL, TSL, TSM, TSX					
		TMC2210-95	30		30		ns
		TMC2210-80	30		30		ns
		TMC2210-65	30		25		ns
t_H	Input Hold Time	Data, ACC, SUB, RND, TC					
		TMC2210-95	0		0		ns
		TMC2210-80	0		0		ns
		TMC2210-65	0		3		ns
		PREL, TSL, TSM, TSX					
		TMC2210-95	3		3		ns
		TMC2210-80	3		3		ns
		TMC2210-65	3		3		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40 pf					
		TMC2210-95		40		40	ns
		TMC2210-80		35		35	ns
		TMC2210-65		35		35	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40 pf					
		TMC2210-95		40		40	ns
		TMC2210-80		30		35	ns
		TMC2210-65		30		30[2]	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40 pf					
		TMC2210-95		35		35	ns
		TMC2210-80		30		30	ns
		TMC2210-65		30		30[2]	ns

Notes: 1. All transitions are measured at a 1.5V level except t_{ENA} and t_{DIS} which are measured as shown in Figure 8.
2. V_{DD} = Min.

Application Discussion

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, there is no difference between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the LSBs of the multiplier, multiplicand and product all have the same value. If fractional notation is used, the MSBs of the multiplier, multiplicand and product all have the same value.

Ordering Information

Product Number	Multiply/ Accumulate Time (ns)	Temperature	Screening	Package	Package Marking
TMC2210G8C65	65	STD: T_A = 0 to 70°C	Commercial	68-pin Ceramic Pin Grid Array	2210G8C65
TMC2210G8C80	80	STD: T_A = 0 to 70°C	Commercial	68-pin Ceramic Pin Grid Array	2210G8C80
TMC2210G8V65	65	EXT: T_C = -55 to 125°C	MIL-STD-883C	68-pin Ceramic Pin Grid Array	2210G8V65
TMC2210G8V80	80	EXT: T_C = -55 to 125°C	MIL-STD-883C	68-pin Ceramic Pin Grid Array	2210G8V80
TMC2210G8V95	95	EXT: T_C = -55 to 125°C	MIL-STD-883C	68-pin Ceramic Pin Grid Array	2210G8V95
TMC2210H8C65	65	STD: T_A = 0 to 70°C	Commercial	68-pin Plastic Pin Grid Array	2210H8C65
TMC2210H8C80	80	STD: T_A = 0 to 70°C	Commercial	68-pin Plastic Pin Grid Array	2210H8C80
TMC2210J0V80	80	EXT: T_C = -55 to 125°C	MIL-STD-883C	64-pin Hermetic Ceramic DIP	2210J0V80
TMC2210J0V95	95	EXT: T_C = -55 to 125°C	MIL-STD-883C	64-pin Hermetic Ceramic DIP	2210J0V95
TMC2210N0C65	65	STD: T_A = 0 to 70°C	Commercial	64-pin Plastic DIP	2210N0C65
TMC2210N0C80	80	STD: T_A = 0 to 70°C	Commercial	64-pin Plastic DIP	2210N0C80
TMC2210N0C95	95	STD: T_A = 0 to 70°C	Commercial	64-pin Plastic DIP	2210N0C95
TMC2210R1C65	65	STD: T_A = 0 to 70°C	Commercial	68-Lead Plastic J-Leaded Chip Carrier	2210R1C65
TMC2210R1C80	80	STD: T_A = 0 to 70°C	Commercial	68-Lead Plastic J-Leaded Chip Carrier	2210R1C65

40G02412 Rev E 8/93

TMC3211
Integer Divider
32-Bit, 20 MOPS

Description

The TMC3211 is a fast monolithic two's complement integer divider which can divide a 32-bit dividend by a 16-bit divisor to produce a 32-bit quotient, with a maximum pipelined throughput of 20 MOPS (Million Operations Per Second). Data is input on separate busses, and quotients are available on a 32-bit output bus with synchronous three-state enable. All data inputs and outputs are registered and TTL compatible. All input and output signal timing is referenced to the rising edge of Clock.

The TMC3211 has a single system clock and separate load enable controls for the dividend and divisor registers. This allows the device to be used in applications requiring division by a constant. Underflow automatically produces the expected zero quotient, and dividing by zero sets a divide-by-zero output flag.

The internal architecture of the TMC3211 allows all 32-bit two's complement integer dividends and nonzero 16-bit two's complement integer divisors, without prenormalization. The output quotient format is 32-bit integer.

The TMC3211 makes a full-precision, full-speed divide function available to designers of workstations, image processors, and radar systems who need to perform perspective extractions, matrix operations, range scaling, and other complex functions.

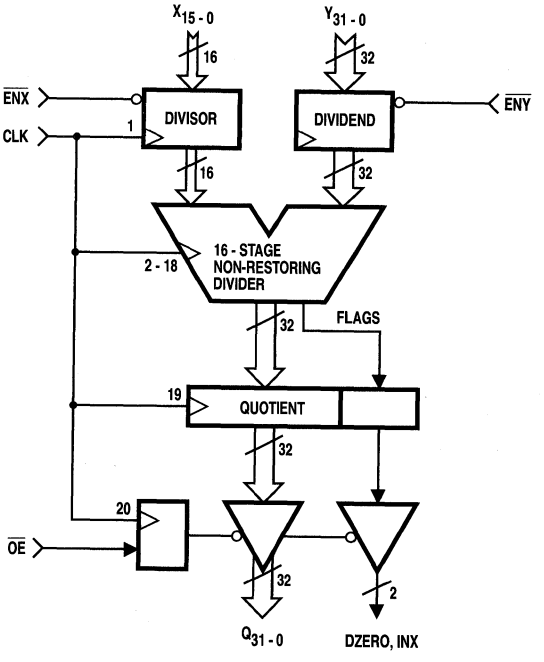
Features

- 32-bit by 16-bit fixed-point integer division with 32-bit quotient
- 20 MHz clock rate and pipelined throughput rate
- Three-bus I/O architecture allows unrestricted throughput
- Easy system interfacing
- Status flags for divide-by-zero and inexact result
- All inputs and outputs TTL compatible

Applications

- Graphics and image processors
- Matrix operations and geometric transforms
- Perspective extraction
- Radar signal processing
- Range scaling

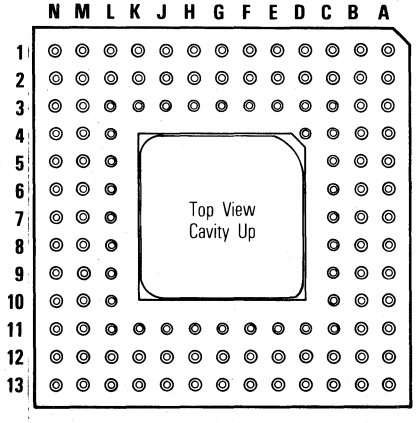
Functional Block Diagram



Pin Assignments

120-Pin Plastic Pin Grid Array – H5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	V_{DD}	L3	GND	L11	V_{DD}	C11	GND
B2	Y_{15}	M2	X_0	M12	GND	B12	Q_7
B1	$\overline{YEN}$	N2	X_1	M13	Q_{25}	A12	Q_6
D3	GND	L4	V_{DD}	K11	V_{DD}	C10	Q_5
C2	V_{DD}	M3	X_2	L12	GND	B11	Q_4
C1	Y_{16}	N3	X_3	L13	Q_{24}	A11	Q_3
D2	Y_{17}	M4	X_4	K12	Q_{23}	B10	Q_2
E3	GND	L5	GND	J11	V_{DD}	C9	Q_1
D1	Y_{18}	N4	X_5	K13	Q_{22}	A10	Q_0
E2	Y_{19}	M5	X_6	J12	Q_{21}	B9	DZ
E1	Y_{20}	N5	X_7	J13	Q_{20}	A9	REM
F3	V_{DD}	L6	X_8	H11	GND	C8	Y_0
F2	Y_{21}	M6	X_9	H12	Q_{19}	B8	Y_1
F1	Y_{22}	N6	X_{10}	H13	Q_{18}	A8	Y_2
G2	GND	M7	X_{11}	G12	V_{DD}	B7	Y_3
G3	V_{DD}	L7	V_{DD}	G11	Q_{17}	C7	Y_4
G1	Y_{23}	N7	X_{12}	G13	Q_{16}	A7	Y_5
H1	Y_{24}	N8	X_{13}	F13	Q_{15}	A6	Y_6
H2	Y_{25}	M8	X_{14}	F12	Q_{14}	B6	Y_7
H3	GND	L8	X_{15}	F11	V_{DD}	C6	Y_8
J1	Y_{26}	N9	$\overline{XEN}$	E13	Q_{13}	A5	Y_9
J2	Y_{27}	M9	CLK	E12	Q_{12}	B5	Y_{10}
K1	Y_{28}	N10	$\overline{OEQ}$	D13	Q_{11}	A4	V_{DD}
J3	V_{DD}	L9	Q_{31}	E11	GND	C5	Y_{11}
K2	Y_{29}	M10	Q_{30}	D12	Q_{10}	B4	Y_{12}
L1	Y_{30}	N11	Q_{29}	C13	Q_9	A3	Y_{13}
M1	Y_{31}	N12	Q_{28}	B13	Q_8	A2	Y_{14}
K3	GND	L10	Q_{27}	D11	V_{DD}	C4	GND
L2	V_{DD}	M11	GND	C12	GND	B3	V_{DD}
N1	GND	N13	Q_{26}	A13	V_{DD}	A1	GND



Functional Description

General Information

The TMC3211 consists of input registers, a pipelined array divider, and output (quotient) registers. The 16-bit divisor and 32-bit dividend input registers can each be loaded independently using the two synchronous load enable controls. The divider is a 16-stage pipelined non-restoring array which produces a 32-bit quotient and condition flags which indicate an attempted division by zero, or operations which yield a non-zero remainder or inexact result. The 32-bit parallel quotient output register includes three-state output drivers with synchronous enable control, which permits multiple TMC3211s to be operated in parallel or connected directly to a system bus.

The TMC3211 requires a total of 19 clock cycles to generate a full 32-bit quotient result. Once the internal pipeline is full, a new quotient is available at the output every clock cycle.

Signal Definitions

Power

V_{DD}, GND — The TMC3211 operates on a single +5V supply. All power and ground lines must be connected.

Clock

CLK — The TMC3211 has a single Clock input. All input and output signal timing is referenced to the rising edge of Clock.

Inputs

Y_{31-0} — The 32-bit Dividend is presented through the registered Y input port. Y_{31} is the sign bit. The LSB is Y_0.

X_{15-0} — The 16-bit Divisor is presented through the registered X input port. X_{15} is the sign bit. The LSB is X_0.

Outputs

Q_{31-0} — The current Quotient is available on the registered Q output bus. Q_{31} is the sign bit. The LSB is Q_0.

Controls

$\overline{YEN}$ Data present at the Dividend input Y_{31-0} is latched into the input registers on the rising edge of clock when the enable control $\overline{YEN}$ is LOW.

$\overline{XEN}$ Data present at the Divisor input X_{15-0} is latched into the input registers on the rising edge of clock when the enable control $\overline{XEN}$ is LOW.

$\overline{OEQ}$ The quotient output bus Q_{31-0} and flags DZ and REM are in the high-impedance state when the registered Output Enable $\overline{OEQ}$ is HIGH. When $\overline{OEQ}$ is LOW, they are enabled on the next clock cycle.

Flags

DZ Whenever a zero divisor is input, the resulting invalid output quotient will be accompanied by a registered Divide-By-Zero Flag HIGH.

REM Whenever a division operation leaves a nonzero remainder, the resulting quotient is accompanied by a registered nonzero Remainder Flag HIGH.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package
Power	V_{DD}	Supply Voltage	B3, A4, A13, D11, F11, G12, J11, K11, L11, L7, L4, L2, J3, G3, F3, C2, C3
	GND	Ground	A1, C4, C11, C12, E11, H11, L12, M12, M11, L5, L3, N1, K3, H3, G2, E3, D3
Clock	CLK	System Clock	M9
Inputs	Y_{31-0}	Dividend Data	M1, L1, K2, K1, J2, J1, H2, H1, G1, F1, F2, E1, E2, D1, D2, C1, B2, A2, A3, B4, C5, B5, A5, C6, B6, A6, A7, C7, B7, A8, B8, C8
	X_{15-0}	Divisor Data	L8, M8, N8, N7, M7, N6, M6, L6, N5, M5, N4, M4, N3, M3, N2, M2
Outputs	Q_{31-0}	Quotient Data	L9, M10, N11, N12, L10, N13, M13, L13, K12, K13, J12, J13, H12, H13, G11, G13, F13, F12, E13, E12, D13, D12, C13, B13, B12, A12, C10, B11, A11, B10, C9, A10
Controls	$\overline{YEN}$	Dividend Write Enable	B1
	$\overline{XEN}$	Divisor Write Enable	N9
	$\overline{OEQ}$	Quotient Output Enable	N10
Flags	DZ	Divide-By Zero Flag	B9
	REM	Inexact Remainder Flag	A9
No Connect		Index Pin	D4

Applications Discussion

Division Using A Constant

By utilizing the separate input data register load enable controls, the TMC3211 can perform division by a constant. The data currently held remain in the input registers until updated by the user.

Data Formats

The TMC3211 supports fixed-point two's complement data formats. By keeping track of the binary points of the input data, the user can then interpret the resulting quotient properly. Two possible binary weightings of the input and output bits are as follows:

Figure 1. Integer Data Format

Pin	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Y	-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X																	-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
Q	-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Figure 2. Fractional Data Format

Y	-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}
X																	-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
Q	-2^{15}	$.2^{14}$	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

where a leading minus sign indicates a sign bit.

Care must be taken when adopting fractional data formats. By observing the binary weighting applied to the input data in the dividend and divisor, the binary point of the quotient can then be correctly established. The difference lies only in constant scale factors, which must be considered in order to maintain a data format which is compatible with the bit weighting of the hardware system. The two most common choices are fractional and integer notation. If integer notation is used, the LSBs of the dividend, divisor, and quotient all have the same value. With fractional notation the MSBs are all of equal weight.

Divide by Zero

The flag DZ indicates that the divisor input for the current calculation was a zero, independent of the dividend. Dividing by zero is an undefined operation yielding a meaningless quotient. Thus, this flag must be monitored to guard against possible errors.

Inexact Results

The flag REM is provided to indicate that the current quotient left a nonzero remainder and was truncated toward zero.

Negative Full-Scale Overflow

Due to a finite data word width, a two's complement overflow error occurs under the following unique condition:

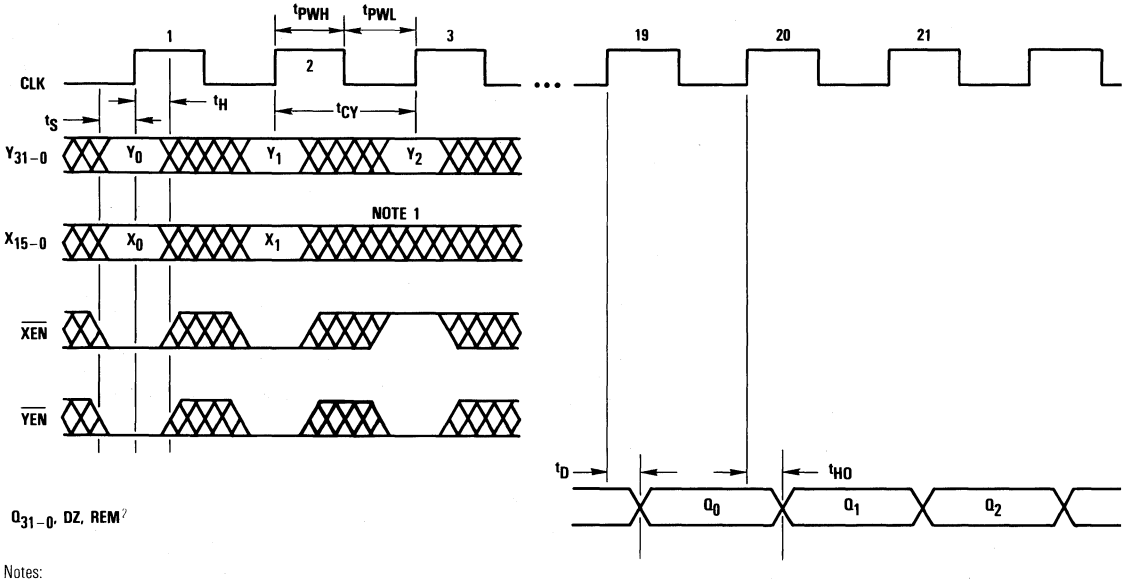
Divisor $Y = 80000000_H$ (−Full-Scale)
Dividend $X = FFFF_H$ (−1)

Result:

Quotient $Q = 80000000_H$ (−Full-Scale)

As stated above, this is due to a limitation in the number of bits available to indicate a positive full-scale quotient, and data overflows into the MSB position to indicate an incorrect sign.

Figure 3. Timing Diagram



Notes:

1. Demonstrates division by a constant, $Q_2 = Y_2/X_1$.
2. Assumes $\overline{OEQ}$ = LOW.

Figure 4. Equivalent Input Circuit

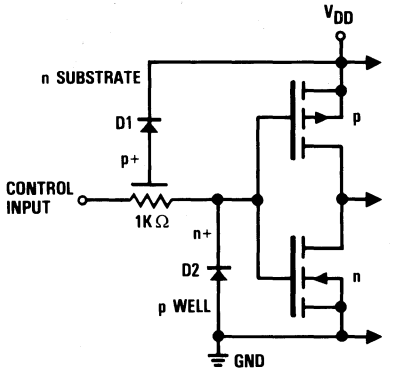
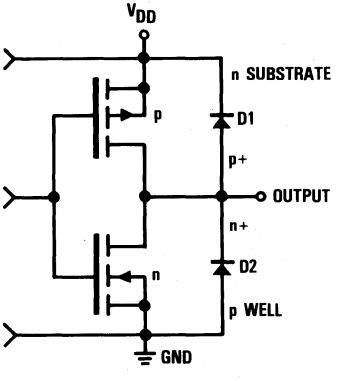


Figure 5. Equivalent Output Circuit



Fixed-Point

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−3.0 to 6.0mA
Short−circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
V_{IL}	Input Voltage, Logic LOW				0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			V
I_{OL}	Output Current, Logic LOW				4.0	mA
I_{OH}	Output Current, Logic HIGH				−2.0	mA
t_{CY}	Cycle Time	V_{DD} = Min			50	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15			ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15			ns
t_S	Input Setup Time		12			ns
t_H	Input Hold Time		6			ns
T_A	Ambient Temperature, Still Air		0		70	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, $\overline{OEQ}$=5V, f=20MHz		150	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.		−150	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

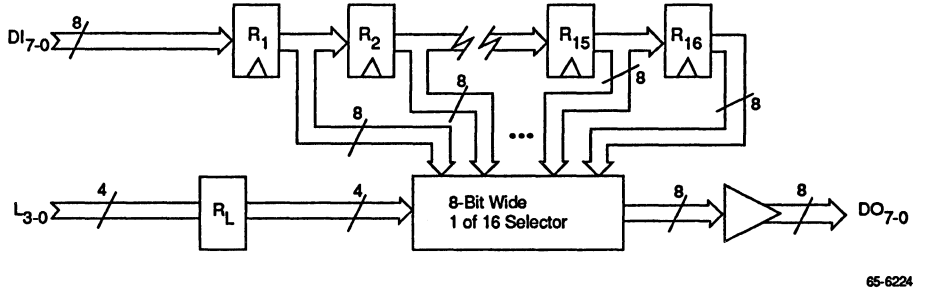
Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_D	Output Delay [1]	V_{DD}=Min, C_{LOAD}=25pF		35	ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=25pF	5		ns

Note: 1. Equivalent to t_{DIS} and t_{ENA} of the three-state outputs.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3211H5C	STD−T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	3211H5C

Memory/Storage



Signal processing puts extraordinary demands on memory and storage elements. The highly pipelined architectures require a variety of short, wide, variable delays to compensate unequal data paths. At times, long delays are needed.

Raytheon provides solutions to all of those problems with special-purpose memory and storage elements. The TDC1005 and TDC1006 shift registers are basic long, fast serial storage elements. For delay equalization problems, the TMC2011/2111 provides an easy solution, with a byte-wide architecture and fully programmable lengths up to 18 words.

Product	Description	Size	Clock Rate[1] (MHz)	Power[1] (Watts)	Package	Grade	Notes
TMC2011-1	Programmable Digital Delay	3-18x8 bit	40	0.1	B2, R3	C	Also 21-36x4 split mode.
-			30	0.1	B2, C3	C, V, SMD	
TMC2111-1	Programmable Digital Delay	1-16x8 bit	40	0.1	B2, R3	C	
-			30	0.1	B2, C3	C, V, SMD	

Notes
1. Guaranteed. See product specifications for test conditions.
2. A = High Reliability, T_C = -55°C to 125°C.
   C = Commercial, T_A = 0°C to 70°C.
   V = MIL-STD-883 compliant, T_C = -55°C to 125°C.
   SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C.

TMC2011/TMC2111
CMOS, Variable-Length Shift Register
8-Bit, 40 MHz

Description

The TMC2011 and TMC2111 are high-speed, byte-wide shift registers with programmable delay lengths.

The TMC2011 can be programmed to any length between 3 and 18 stages. If offers a special split-word mode which allows for mixed delay lengths. The TMC2011, constructed in low-power CMOS, is pin and function compatible with the bipolar TDC1011.

The TMC2111 is a byte-wide shift register that can be programmed to lengths of 1 to 16 stages.

The TMC2011 and TMC2111 are fully synchronous, with all operations controlled by a single master clock. Input and output registers are positive-edge triggered D-type flip-flops. The length and mode controls are also registered. Both devices operate with a maximum clock rate of 40 MHz.

Built with Raytheon Semiconductor's OMICRON-C™ one micron CMOS process, the TMC2011 and TMC2111 are TTL-compatible, low-power replacements for the popular TDC1011, used in applications ranging from video to bit-slice processors.

Features

- Low power CMOS
- Pin compatible replacement for the TDC1011 (TMC2011)
- Inputs and outputs are TTL-compatible
- DC — 40 MHz clock rate
- Selectable delay lengths (TMC2011: 3 to 18 stages, TMC2111: 1 to 16 stages)
- Special 4-bit wide mixed-delay mode (TMC2011)
- Available in 24-pin CERDIP and 28-contact plastic or ceramic chip carrier
- Commercial and MIL-STD-883C grades

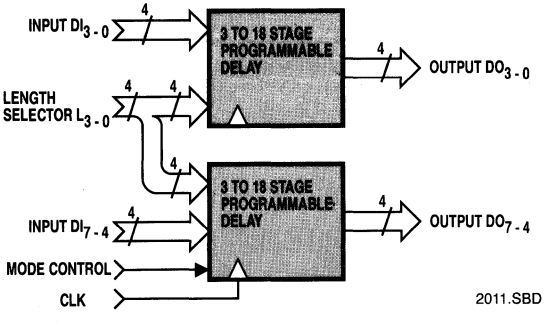
Applications

- Video filtering
- High speed data acquisition
- Local storage registers
- Digital delay lines
- Television special effects
- Pipeline register

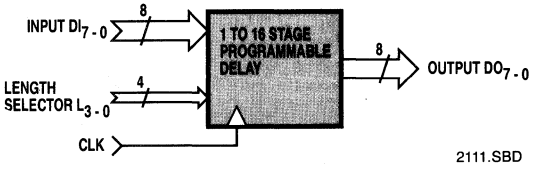
Memory

Simplified Block Diagrams

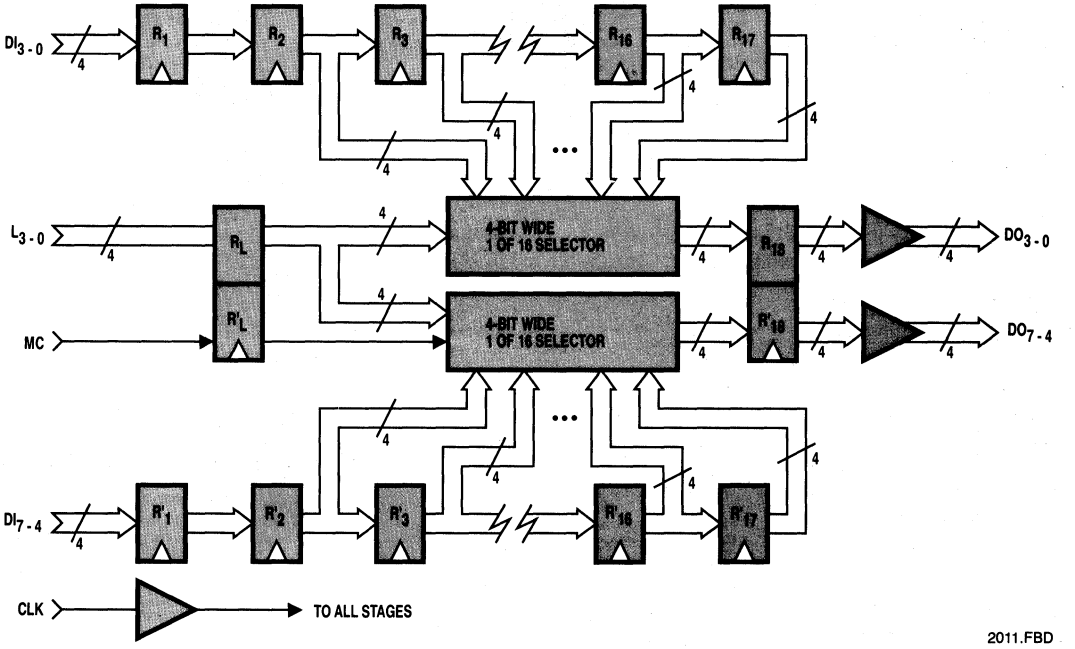
TMC2011



TMC2111

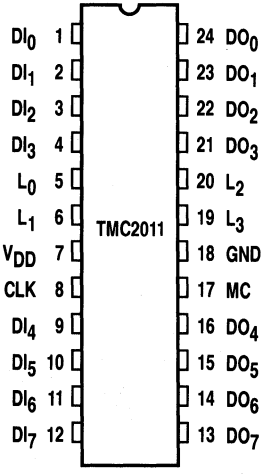


TMC2011 Functional Block Diagram



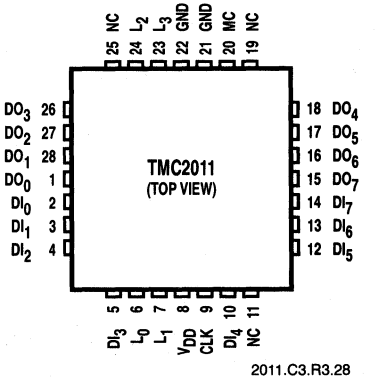
2011.FBD

TMC2011 Pin Assignments



2011.B2.24

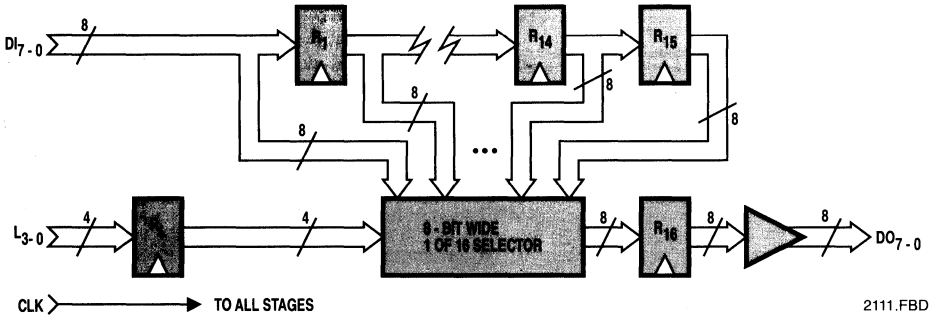
24 Pin CERDIP – B2 Package



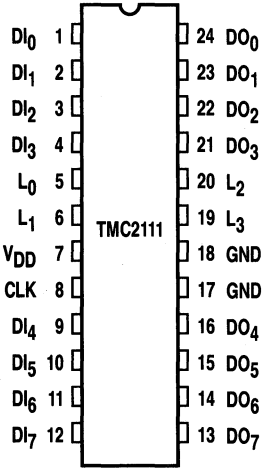
2011.C3.R3.28

28 Contact Chip Carrier – C3 Package
28 Lead Plastic J-Leaded Chip Carrier – R3 Package

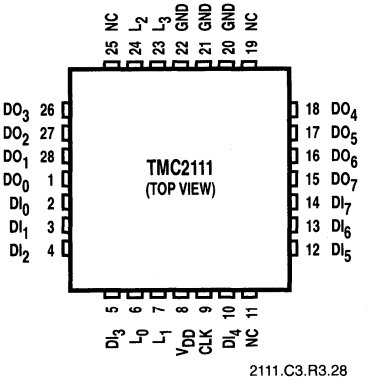
TMC2111 Functional Block Diagram



TMC2111 Pin Assignments



24 Pin CERDIP – B2 Package



28 Contact Chip Carrier – C3 Package
28 Lead Plastic J-Leaded Chip Carrier – R3 Package

Functional Description

General Information

The TMC2011 consists of two 4-bit wide, programmable length shift registers. The TMC2111 consists of a single 8-bit wide, programmable length shift register. The internal registers of each device share control signals and a common clock.

Signal Definitions

Power

V_{DD}, GND — The TMC2011 and TMC2111 operate from a single +5V supply. All power and ground lines must be connected.

Data Inputs

DI_{0-7} — Eight inputs are provided for the data, which pass through the shift register unchanged. The eight inputs on the TMC2011 are divided into two groups of four bits to allow mixed delay operation. The lengths of these two groups are different when the Mode Control (MC) is HIGH (see *Table 1*). When MC is LOW both groups have equal delays. The TMC2111 consists of a single group of eight bits with all data bits having equal delays.

Data Outputs

DO_{0-7} — The outputs of the shift register are delayed relative to the input signals. The amount of the delay is programmable (see *Table 1*). The outputs remain valid for a minimum of t_{HO} nanoseconds after the leading edge of CLK. This allows the data to be latched into circuits with non-zero hold time requirements.

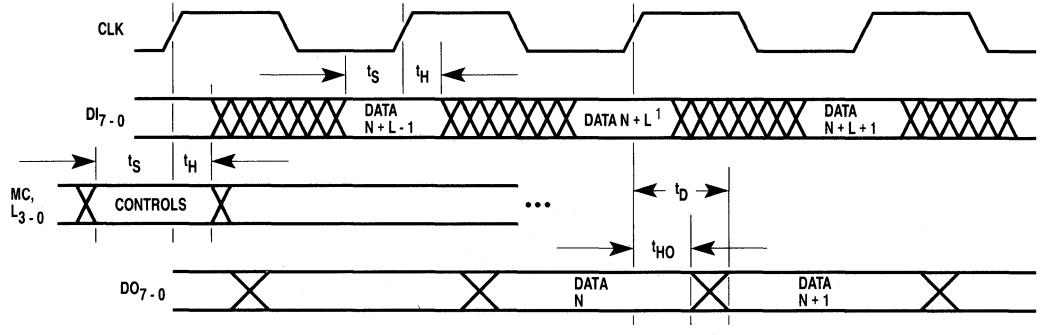
Controls

CLK — All inputs and outputs are synchronous and operate from a single master clock. All operations occur on the rising edge of the master clock.

L_{0-3} — The length select input is used to determine the register delay of the TMC2011 and TMC2111. This input is registered and affects the output t_{DO} after the clock edge after it is input to the device (see *Timing Diagram*). Delay lengths are specified in *Table 1*.

MC — The Mode Control (TMC2011 Only) is used to select the special 4-bit wide split mode on the TMC2011. When HIGH the delay on DO_{7-4} is fixed at 18 stages, while DO_{3-0} have the delay specified by the length select. When MC is LOW, all eight bits have equal delays as specified by the length select.

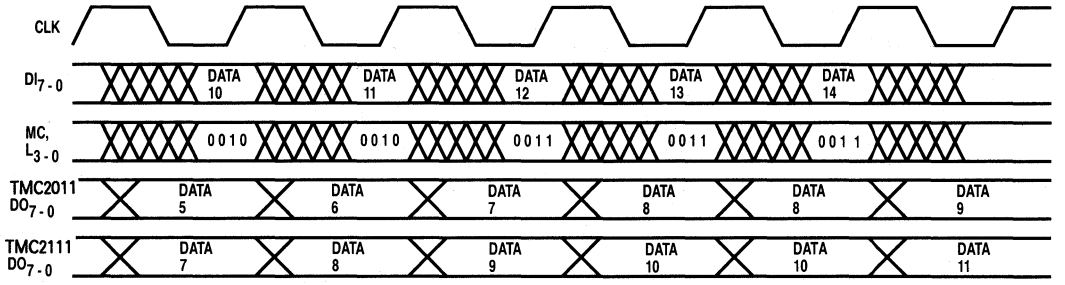
Figure 1. Timing Diagram (Preset Length Controls)



Note: 1. Lis DO_{7-4} Length from ***Table 1***.

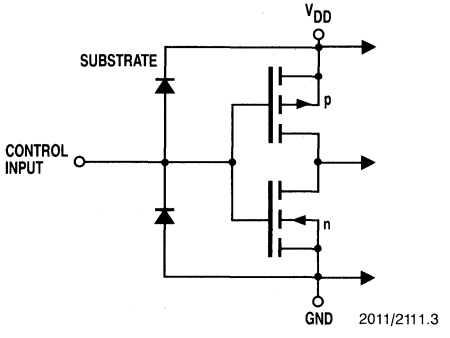
2011/2111.1

Figure 2. Length Control Operation



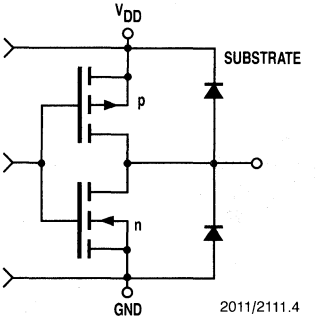
2011/2111.2

Figure 3. Equivalent Input Circuit



2011/2111.3

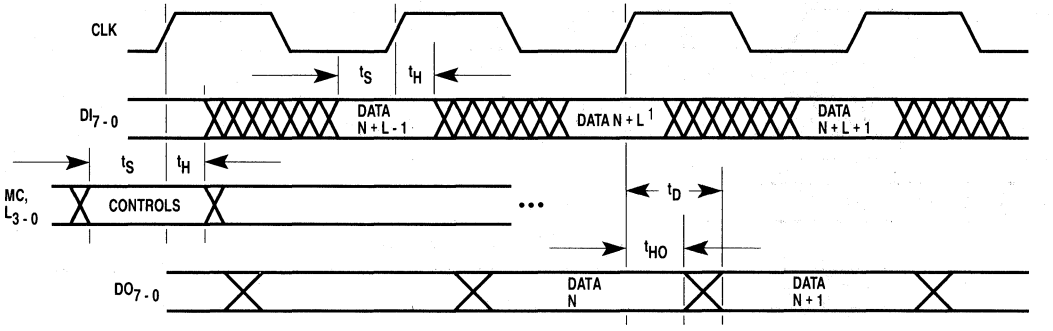
Figure 4. Equivalent Output Circuit



2011/2111.4

Memory

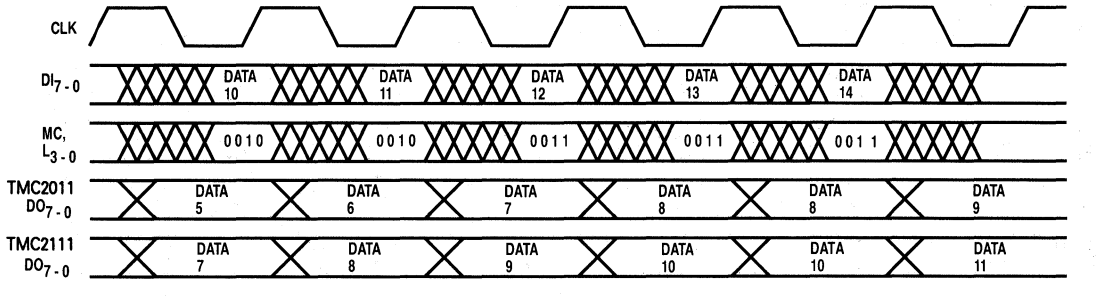
Figure 1. Timing Diagram (Preset Length Controls)



Note: 1. Lis DO_{7-4} Length from ***Table 1***.

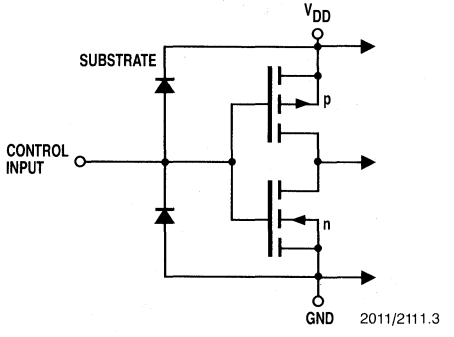
2011/2111.1

Figure 2. Length Control Operation



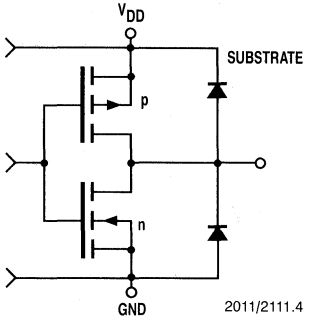
2011/2111.2

Figure 3. Equivalent Input Circuit



2011/2111.3

Figure 4. Equivalent Output Circuit



2011/2111.4

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−3.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
case (plastic package (R3) only)	−20 to +90°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	12			12			ns
t_{PWH}	Clock Pulse Width, HIGH	12			12			ns
t_S	Input Setup Time							
	TMC2011	10			10			ns
	TMC2011-1	8						ns
	TMC2111	10			12			ns
	TMC2111-1	8						ns
t_H	Input Hold Time	1.0			3.0			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH							
	DI_{7-0}, L_{3-0}, MC	2.0			2.0			V
	CLK	2.4			2.4			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz					
	TMC2011			40		40	mA
	TMC2111			40		40	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+10		+10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
f_{CLK}	Maximum Clock Rate	V_{DD} = Min					
	TMC2011, TMC2111		30		30		MHz
	TMC2011-1, TMC2111-1		40				MHz
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF					
	TMC2011, TMC2111			20		25	ns
	TMC2011-1, TMC2111-1			17			ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	5		5		ns

Note: 1. All transitions are measured at a 1.5V level.

Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

Standard Military Drawing	Nearest Equivalent Raytheon Prod. No.	Package
5962-8944601LA	TMC2011B2V	24 Pin CERDIP
5962-89446013A	TMC2011C3V	24 Contact Chip Carrier
5962-8944602LA	TMC2111B2V	24 Pin CERDIP
5962-89446023A	TMC2111C3V	24 Contact Chip Carrier

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2011B2C	STD–T_A=0°C to 70°C	Commercial	24 Pin 0.3" CERDIP	2011B2C
TMC2011B2C1	STD–T_A=0°C to 70°C	Commercial	24 Pin 0.3" CERDIP	2011B2C1
TMC2011B2V	EXT–T_C=–55°C to 125°C	MIL-STD-883	24 Pin 0.3" CERDIP	2011B2V
TMC2011C3V	EXT–T_C=–55°C to 125°C	MIL-STD-883	28 Contact Hermetic Chip Carrier	2011C3V
TMC2011R3C	STD–T_A=0°C to 70°C	Commercial	28 Lead Plastic J-Leaded Chip Carrier	2011R3C
TMC2011R3C1	STD–T_A=0°C to 70°C	Commercial	28 Lead Plastic J-Leaded Chip Carrier	2011R3C1
TMC2111B2C	STD–T_A=0°C to 70°C	Commercial	24 Pin 0.3" CERDIP	2111B2C
TMC2111B2V	EXT–T_C=–55°C to 125°C	MIL-STD-883	24 Pin 0.3" CERDIP	2111B2V
TMC2111C3V	EXT–T_C=–55°C to 125°C	MIL-STD-883	28 Contact Hermetic Chip Carrier	2111C3V
TMC2111R3C	STD–T_A=0°C to 70°C	Commercial	28 Lead Plastic J-Leaded Chip Carrier	2011R3C
TMC2111R3C1	STD–T_A=0°C to 70°C	Commercial	28 Lead Plastic J-Leaded Chip Carrier	2011R3C1

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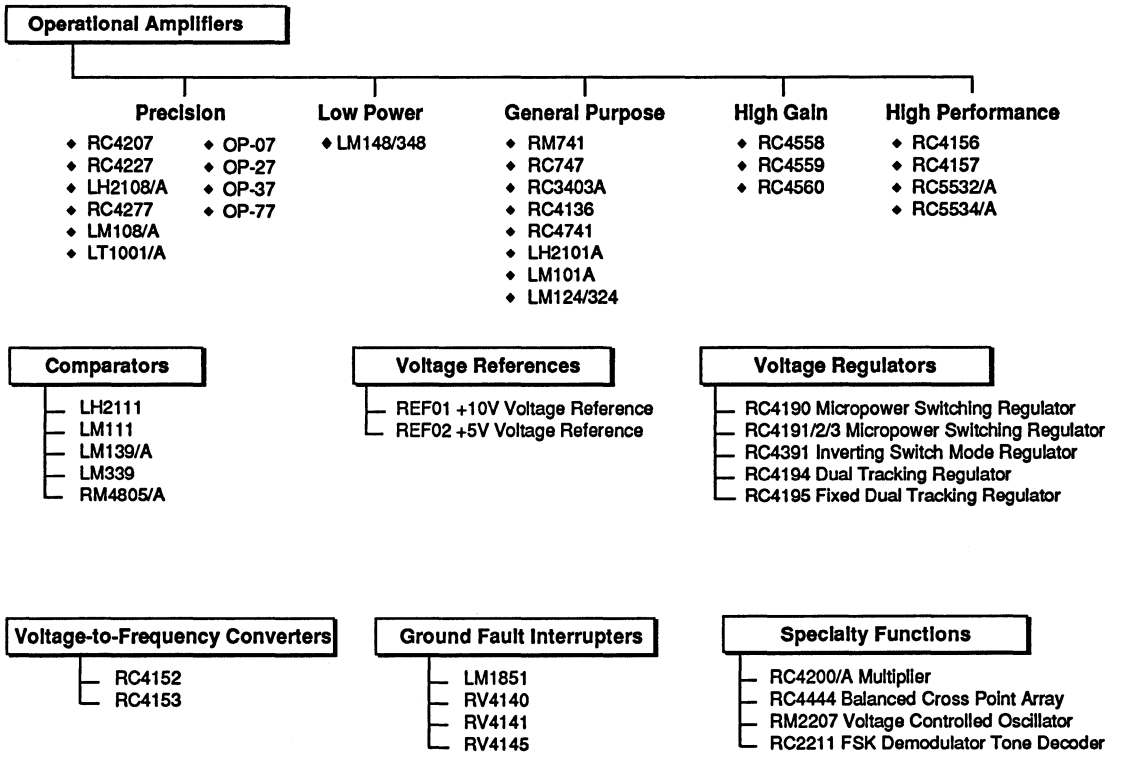
Standard Linear Products



65-6152

At Raytheon Semiconductor we're committed to analog technology. Our growing line of standard linear products have provided circuit solutions for thousands of designers over the years. These products are based on our investment in people and technology, total quality control, just-in-time manufacturing, along with three decades of providing analog solutions to many design problems.

A variety of low noise precision operational amplifiers, instrumentation amps, comparators, D/A multiplier/dividers, precision voltage references, voltage-to-frequency converters, low power switching regulators and voltage regulators and specialty circuits comprise this product line.

The products are fabricated on a bipolar-based junction isolated process. The process provides precision, low noise, low offset input stages, current sources and moderate power stages when needed.

Precision instrumentation grade op amps are achieved with the addition of temperature stable silicon chromium thin film resistors, Zener zap trimming, low noise epitaxial growth process, and our patented V_{OS} digital offset nulling technique. This technique provides commercial grade products with ±10 μV offset, with a worst-case voltage drift of 0.1 μV/°C.

Screening Options Available:

- JAN Class B
- Standard Military Drawings (SMD)
- MIL-STD-883, Class B
- Source Control Drawing (SCD)
- Environmental Stress Screening
- Military Temperature Range
- Industrial Temperature Range
- Commercial Temperature Range

Precision Operational Amplifiers

Type	Description	Electrical Characteristics (min/max except*)						
		V_{os} (μV)	TCV_{os} (μV/°C)	I_{os} (nA)	I_b (nA)	CMRR (dB)	Gain (V/μV)	I_{sy} (mA)
RC4207F	Dual Low Noise	75	1.3	5	±5	100	0.4	6.67
RC4207G		150	0.7*	10	±10	94	0.25	8.0
RC4227F	Dual Low Noise	75	1.3	10	±15	104	0.5	6.67
RC4227G		150	0.4*	15	±25	100	0.4	8.0
RM4227B		75	1.3	10	±15	104	0.5	6.67
RC4277F		75	1.0	5.0	±5.0	110	2.0	5.5
RV4277F		75	1.0	5.0	±5.0	110	2.0	5.5
LH2108A	Dual Low Noise	500	5.0	0.2	±2.0	96	.04	0.4
LH2108		2000	15	0.2	±2.0	85	.025	0.4
LM108A		500	5.0	0.2	±2.0	96	.04	0.4
LM108		2000	15	0.2	±2.0	85	.025	0.4
OP-07A	Low V_{os}	25	0.6	2.0	±2.0	110	0.3	4.0
OP-07		75	1.3	2.8	±3.0	110	0.2	4.0
OP-07E		75	1.3	3.8	±4.0	106	0.2	4.0
OP-07C		150	1.8	6.0	±7.0	100	0.12	5.0
OP-07D		150	2.5	6.0	±12.0	94	0.12	5.0
OP-27A	Ultra Low Noise	25	0.6	35	±40	114	1.0	4.67
OP-27B		60	1.3	50	±55	106	1.0	4.67
OP-27C		100	1.8	75	±80	100	0.7	5.67
OP-27E		25	0.6	35	±40	114	1.0	4.67
OP-27F		60	1.3	50	±55	106	1.0	4.67
OP-27G		100	1.8	75	±80	100	0.7	5.67
OP-37A	Decompensated	25	0.6	35	±40	114	1.0	4.67
OP-37B	(AC stable with	60	1.3	50	±55	106	1.0	4.67
OP-37C	$AV_{CL} \geq 5$)	100	1.8	75	±80	100	0.7	5.67
OP-37E	Ultra Low Noise	25	0.6	35	±40	114	1.0	4.67
OP-37F		60	1.3	50	±55	106	1.0	4.67
OP-37G		100	1.8	75	±80	100	0.7	5.67
OP-77A	Low V_{os}	25	0.3	1.5	±2.0	120	5.0	2.0
OP-77B		60	0.6	2.8	±2.8	116	2.0	2.0
OP-77E		25	0.3	1.5	±2.0	120	5.0	2.0
OP-77F		60	0.6	2.8	±2.8	116	2.0	2.0
OP-77G		100	1.2	2.8	±2.8	116	2.0	2.0

Slew (V/μS)	GBW* (MHz)	1 kHz Noise** (nV/√Hz)	Packages M SOIC	D CDIP	N PDIP	T TO-99	L LCC	Temperature Range -55°C to +125°C	-25°C to +85°C	0°C to +70°C	MIL-STD 883/B Availability
0.3	1.5	10.3*			X					X	
0.3	1.5	10.3*			X					X	
2.7	8.0	3.8*		X	X					X	
2.7	8.0	3.8*		X	X					X	
2.7	8.0	3.8*		X				X			X
0.3	1.5	10.3*			X				X		
0.3	1.5	10.3*		X					X		
.05	1.0	30		X				X			X
.05	1.0	30		X				X			X
.05	1.0	30		X		X	X	X			X
.05	1.0	30		X		X	X	X			X
0.3	0.5	18		X		X		X			X
0.3	0.5	18		X		X		X			X
0.3	0.5	18	X		X					X	
0.3	0.5	20	X		X					X	
0.3	0.5	20	X		X					X	
2.8	8.0	5.5		X		X		X			X
2.8	8.0	5.5		X		X		X			X
2.8	8.0	8.0		X		X		X			X
2.8	8.0	5.5	X		X				X	X	
2.8	8.0	5.5	X		X				X	X	
2.8	8.0	8.0	X		X				X	X	
17	63	5.5		X		X		X			X
17	63	5.5		X		X		X			X
17	63	8.0		X		X		X			X
17	63	5.5	X		X					X	
17	63	5.5	X		X					X	
17	63	8.0	X		X					X	
0.3	0.6	18		X		X		X			X
0.3	0.6	18		X		X		X			X
0.3	0.6	18	X		X					X	
0.3	0.5	20	X		X					X	
0.3	0.6	20	X		X					X	

**10 Hz

Precision Operational Amplifiers

Input Offset Voltage Selection Table by Package Type (+25°C limits, in microvolts)

Part Type	Plastic DIP (N)	SOIC (M)	Ceramic DIP (D)	Leadless Chip Carrier (L)	Metal Can TO-99 (T)
RC4207*	±75		±75		
RC4227*	±75		±75		
RC4277*	±30		±30		±25
OP-07	±75	±75	±25		±25
OP-27	±25	±25	±25		±25
OP-37	±25	±25	±25		±25
OP-77	±25	±60	±25		±25
LM108/A			±500	±500	±500
LH2108/A*			±500	±500	±500

*Dual

Audio and General Purpose Operational Amplifiers

Single Operational Amplifiers

Type	Description	Maximum Input Specifications @25°C Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)	Typ.[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/µS)	Temp[2] Range	Available Packages D	L	M	N	T
LM101A	General Purpose with Improved Input Characteristics	2.0	10	75	1.0	0.5	M	X				X
RM741	General Purpose, Internal Comp	5.0	200	500	1.0	0.5	M	X				X
RC5534	High Performance, Low Noise	4.0	300	1500	10	13	C				X	
RM5534		2.0	200	800	10	13	M	X				X
RC5534A[3]		4.0	300	1500	10	13	C				X	
RM5534A[3]		2.0	200	800	10	13	M	X				X

Notes:
1. Gain bandwidth product for 5534/A series and closed loop bandwidth for OP series. 2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C. 3. RM/RC5534A guarantees maximum input noise specification.

Dual Operational Amplifiers

Type	Description	Maximum Input Specifications @25°C Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)	Typ.[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/µS)	Temp[2] Range	Available Packages D	L	M	N	T
LH2101A	High Performance	2	10	75		0.5		X				
RM747	Dual 741	5	200	500	1	0.5	M	X				X
RC4558	Wideband 741	6	200	500	3	1	C			X	X	
RM4558		5	200	500	3	1	M	X				X
RC4559	High Performance	6	100	250	4 (3)	2 (1,5)	C	X		X	X	
RM4559		5	100	250	4 (3)	2 (1,5)	M	X				X
RC4560	Wide Bandwidth	7	300	800	10	4	C			X	X	
RC5532	High Performance,	4	150	800	10	8	C	X			X	
RM5532	Low Noise	2	100	400	10	8	M	X				X
RC5532A[3]		4	150	800	10	8	C	X			X	
RM5532A[3]		2	100	400	10	8	M	X				X

Notes:
1. Gain bandwidth product for 5532A series. 2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C. 3. RM/RC5532A guarantees maximum input noise specification. ( ) Denotes guaranteed specifications.

Quad Operational Amplifiers

Type	Description	Maximum Input Specifications @25°C: Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)	Typ.[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[1] Range	Available Packages: D	L	M	N	T
RM4741	741 General Purpose	3	30	200	3.5	1.6	M	X				
RC4741		5	50	300	3.5	1.6	C				X	
LM124	Single Supply	5	30	150	1	—	M	X				
LM148	Low Power 741	5	25	100	1	0.5	M	X				
LM324	Single Supply	7	50	250	1	—	C			X	X	
RC3403A	Ground Sensing	6	50	500	1	1.2	C				X	
RC4136	741 General Purpose	6	200	500	3	1	C			X	X	
RM4136		4	150	400	3	1.5	M	X				
RC4156	High Performance	5	50	300	3.5 (2.8)	1.6 (1.3)	C			X	X	
RM4156		3	30	200	3.5 (2.8)	1.6 (1.3)	M	X				
RC4157	High Speed, Decompensated	5	50	300	19 (15)	8 (6.5)	C			X	X	
RM4157		3	30	200	19 (15)	8 (6.5)	M	X				

Notes:
1. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
( ) Denotes guaranteed specification.

Comparators

Type	Description	Maximum Input Specifications @25°C: Offset Voltage (mV)	Bias Current (nA)	Offset Current (nA)	Voltage Gain (V/mV typ)	Max Sat. Voltage	Output Leakage Current (nA typ)	Available Packages: D	L	M	N	T
LH2111	Dual Precision Voltage	3.0	100	10	200	& 12V	0.2	X				
LM111	Low Input Current	3.0	100	10	200	& 12V	0.2	X				X
LM139	Quad Single Supply	5.0	100	25	200	0.40	0.1	X				
LM139A	Quad Single Supply	±2.0	100	25	200	0.40	0.1	X				
LM339	Quad Single Supply	5.0	250	50	200	0.40	0.1			X	X	
RM4805	Precision High Speed	0.6	1800	150	20	0.40	—	X				
RM4805A		0.25	1200	80	20	0.40	—	X				

Package Codes:
D = Ceramic DIP L = Leadless Chip Carrier M = Plastic SOIC N = Plastic DIP T = Metal Can (TO-99)

Voltage References

Device	Nominal Voltage Out	Typical Tempco (ppm/°C)	Temp. Range	Typical ΔV_{OUT} Over Temp. (%)	Typical Line Reg. (%/Volt)	Typical Load Reg. (%/mA)	Typical Load Current (mA)	Input Voltage Range (Voltage)
REF-01	10.00	10.0	Mil	.18	.006	.006	15	12 to 40
REF-01C	10.00	20.0	Comm	.14	.009	.006	15	12 to 40
REF-01D	10.00	70.00	Comm	.49	.012	.009	15	12 to 40
REF-02	5.00	10.00	Mil	.18	.006	.006	15	7 to 40
REF-02C	5.00	20.00	Comm	.14	.009	.006	15	7 to 40
REF-02D	5.00	70.00	Comm	.49	.012	.009	15	7 to 40

Voltage Regulators

Product	Regulator Type	Operating Range	Efficiency	Typ. Regulation Line	Typ. Regulation Load	Typ. Supply Current
RC4190	Low Power Switcher	1.3 to 30V	85%	.04% Vo	0.2% Vo	235 µA
RC4191/2/3	Low Power Switcher	2.2 to 30V	85%	.04% Vo	0.2% Vo	225 µA
RC4194	Adj. Dual Tracker	±45V	n/a	0.04% Vout	0.002% vout	+0.8 and -1.8 mA
RC4195	Fixed Dual Tracker	±30V	n/a	2.0 mV	5.0 mV	±1.5 mA
RC4391	Inverting Switcher	4 to 30V	70%	1.0 to 1.5% Vo	.07 to 0.2% Vo	300 µA

Voltage-to-Frequency Converters

Product	Description	High Accuracy	Bandwidth	Tempco
RC4152	VFC or FVC	0.05% Max	DC to 100 kHz	150 ppm/°C
RC4153	VFC	0.01% Max	DC to 250 kHz	50 ppm/°C

Ground Fault Circuit Interrupters (GFCI)

Raytheon Semiconductor has been involved with GFCI/ALCI markets since 1973. Keeping pace with mandated UL regulations surrounding GFCI/ALCI type safety devices in homes has created a very high demand for low cost, easy to assemble, reliable ICs. Raytheon Semiconductor has met this challenge by providing the following standard GFCI/ALCI products.

Features	LM1851	RV4140	RV4141	RV4145
GFCI Applications	Yes	No	Yes	Yes
ALCI Application	No	Yes	Yes	Yes
$I_{QUIESCENT}$	2.5 mA	375 µA	500 µA	450 µA
Ext. parts for GFCI	20	n/a	13	21
Ext. parts for ALCI	18	10	10	12
110V/220V Operation	No	Yes	Yes	Yes
Built-in Rectifier	No	Yes	Yes	No
Packaging				
8-SOIC	Yes	Yes	Yes	Yes
8-DIP	Yes	Yes	Yes	Yes
Dice	Yes	Yes	Yes	Yes

RC4447 Quad PIN Diode Switch Driver

- Drives PIN Diodes or MOSFETs
- 50 ns response time (low to high)
- 10 MHz pulse rate
- Quad Driver, die or packaged units

RC2211 FSK Demodulator/Tone Decoder

- Excellent tempco — 20 ppm/°C
- Wide frequency range — 0.01 Hz to 300 KHz
- FSK demodulation with carrier-detector

RM2207 Voltage Controlled Oscillator

- 20 ppm/°C tempco
- Adjustable duty cycle — 0.1% to 99.9%
- Wide frequency range — 0.01 Hz to 1 MHz
- Two or four FSK capability

RC4444 4 x 4 x 2 Balanced Switching Crosspoint Array

- Low bidirectional R_{ON}
- High R_{OFF}
- Low capacitance
- High rate firing
- Predictable holding current
- Superior gate matching

RC4200/A Multiplier

- Non-linearity — 0.1% max.
- Tempco — 0.005%
- Wide bandwidth — 4 MHz
- Signal-to-noise ratio — 94 dB
- Multiply, divide square, square root, RMS-to-DC conversion, AGC, modulate/demodulate

LM101A/LH2101A
General Purpose Operational Amplifier

Description

The LM101A/LH2101A is a general purpose high performance operational amplifier fabricated monolithically on a silicon chip by an advanced epitaxial process. The LH2101A consists of two LM101A ICs in one 16-lead DIP. The units may be fully compensated with the addition of a 30 pF capacitor stabilizing the circuit for all feedback configurations including capacitive loads.

The device may be operated as a comparator with a differential input as high as 30V. Used as a comparator the output can be clamped at any desired level to make it compatible with logic circuits.

The LM101A and LH2101A operate over the full military temperature range from -55°C to +125°C.

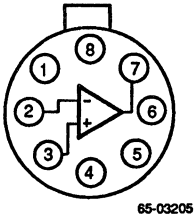
Features

- Input offset voltage 0.7 mV
- Input bias current 30 nA
- Input offset current 1.5 nA
- Full frequency compensation 30pF
- Supply voltage ±5.0V to ±20V

LM101A/LH2101A

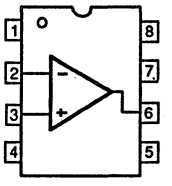
Connection Information

8-Lead TO-99 Metal Can
(Top View)



65-03205

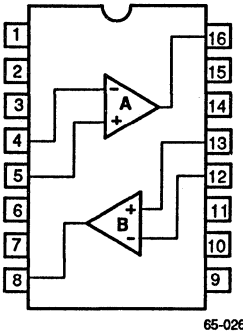
8-Lead Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	Comp/V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	V_{OS} Trim
6	Output
7	$+V_S$
8	Comp

16-Lead Dual In-Line Package
(Top View)



65-02658

Pin	Function	Pin	Function
1	$+V_S$ (A)	9	$+V_S$ (B)
2	Comp (A)	10	Comp (B)
3	Comp/V_{OS} Trim (A)	11	Comp/V_{OS} Trim (B)
4	-Input (A)	12	-Input (B)
5	+Input (A)	13	+Input (B)
6	$-V_S$	14	V_{OS} Trim (A)
7	V_{OS} Trim (B)	15	NC
8	Output (B)	16	Output (A)

Ordering Information

Part Number	Package	Operating Temperature Range
LM101AD	D	-55°C to +125°C
LM101AD/883B	D	-55°C to +125°C
LM101AT	T	-55°C to +125°C
LM101AT/883B	T	-55°C to +125°C
LH2101AD	D	-55°C to +125°C
LH2101AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D = 8-lead ceramic DIP (LM101 types)
D = 16-lead ceramic DIP (LH2101 types)
T = 8-lead metal can (TO-99)
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Output Short-Circuit Duration[2] ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
LM101A, LH2101A ..... -55°C to +125°C
Lead Soldering Temperature (60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	16-Lead Ceramic DIP
Max. Junction Temp.	+175°C	+175°C	+175°C
Max. P_D T_A <50°C	833 mW	658 mW	1042 mW
Therm. Res θ_{JC}	45°C/W	50°C/W	60°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W	120°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C	8.33 mW/°C

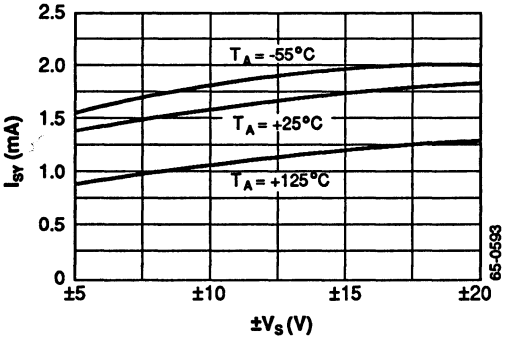
Electrical Characteristics

($C = 30$ pF; $\pm 5.0V \leq V_S \leq \pm 20V$; $-55°C \leq T_A \leq +125°C$ unless otherwise specified)

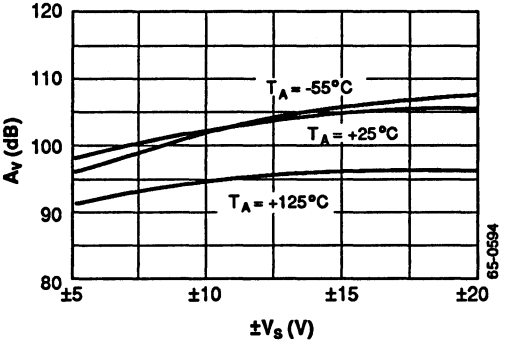
Parameters	Test Conditions	LM101A/LH2101A Min	Typ	Max	Units
Input Offset Voltage	$T_A = +25°C$, $R_S \leq 50$ kΩ		0.7	2.0	mV
Input Offset Current	$T_A = +25°C$		1.5	10	nA
Input Bias Current	$T_A = +25°C$		30	75	nA
Input Resistance	$T_A = +25°C$	1.5	4.0		MΩ
Supply Current	$T_A = +25°C$ $V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = +25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2$ kΩ	50	160		V/mV
Input Offset Voltage	$R_S \leq 50$ kΩ			3.0	mV
Average Input Offset Voltage Drift	$R_S \leq 50$ kΩ		3.0	15	µV/°C
Input Offset Current				20	nA
Average Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		0.01	0.1	
	$-55°C \leq T_A \leq +25°C$		0.02	0.2	nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2$ kΩ	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$ $R_L = 10$ kΩ	±12	±14		V
	$R_L = 2$ kΩ	±10	±13		
Input Voltage Range	$V_S = \pm 20V$	±15			V
Common Mode Rejection Ratio	$R_S \leq 50$ kΩ	80	96		dB
Power Supply Rejection Ratio	$R_S \leq 50$ kΩ	80	96		dB

Typical Performance Characteristics

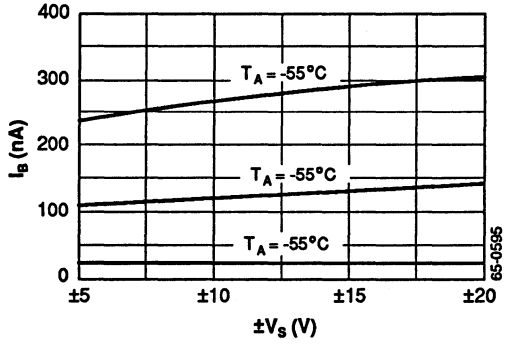
Supply Current vs. Supply Voltage



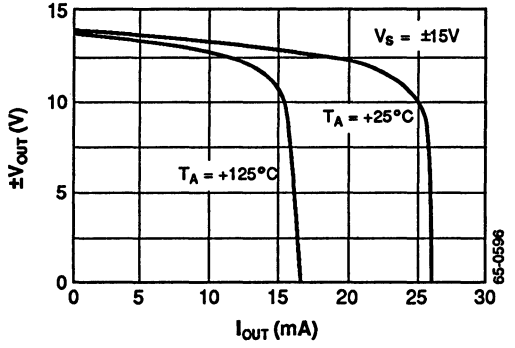
Voltage Gain vs. Supply Voltage



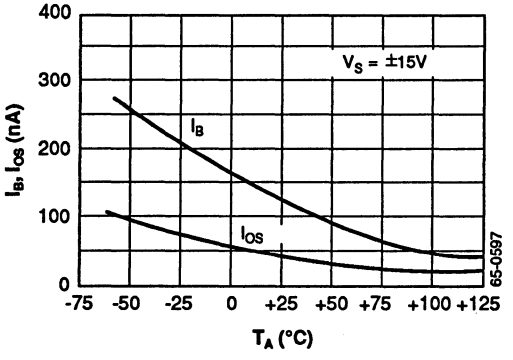
Input Bias Current vs. Supply Voltage



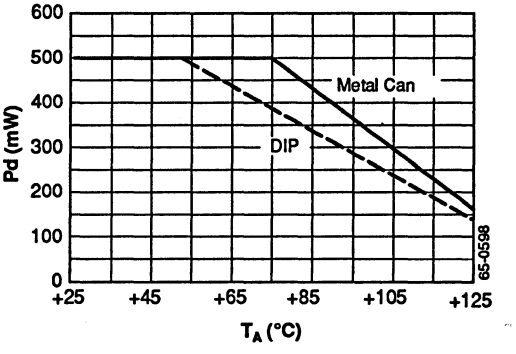
Current Limiting
Output Voltage vs. Output Current



Input Bias, Offset Current vs. Temperature



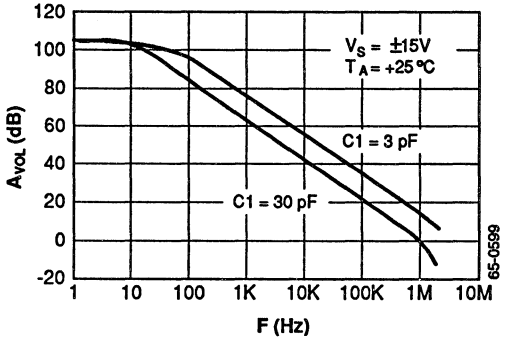
Maximum Power Dissipation vs. Temperature



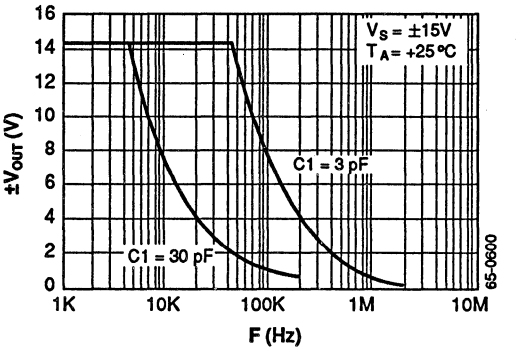
Linear

Typical Performance Characteristics (Continued)

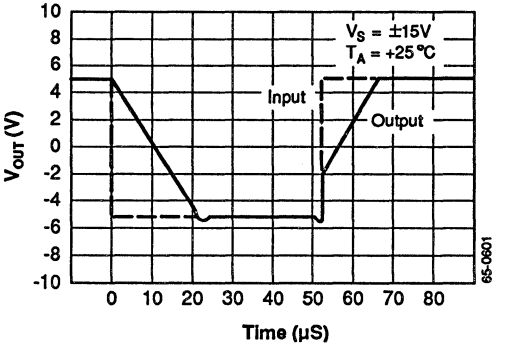
Open Loop Gain vs. Frequency



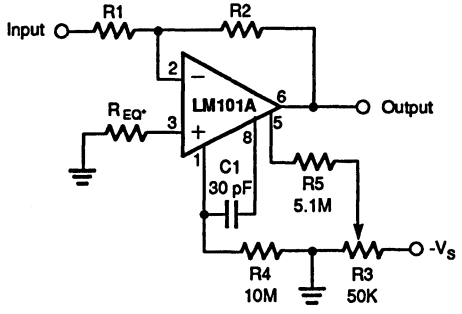
Output Voltage Swing vs. Frequency



Follower Large Signal Pulse Response
Output Voltage vs. Time



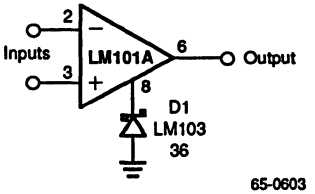
Typical Applications



*Maybe zero or equal to parallel combination of R1 and R2 for minimum offset.

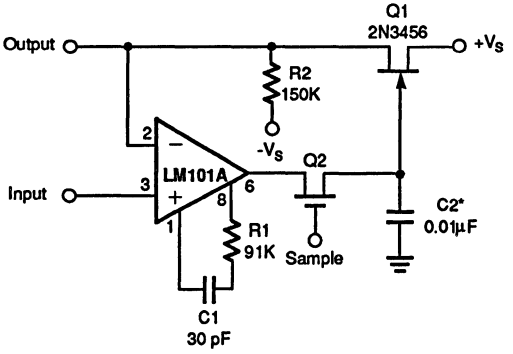
65-0602

Inverting Amplifier With Balancing Circuit



65-0603

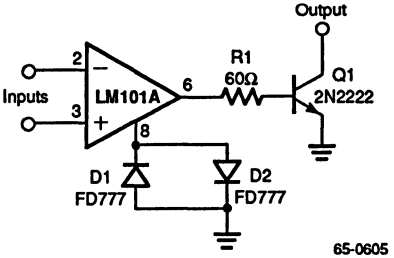
Voltage Comparator for Driving DTL or TTL ICs



*Polycarbonate dielectric capacitor

65-0604

Low Drift Sample and Hold

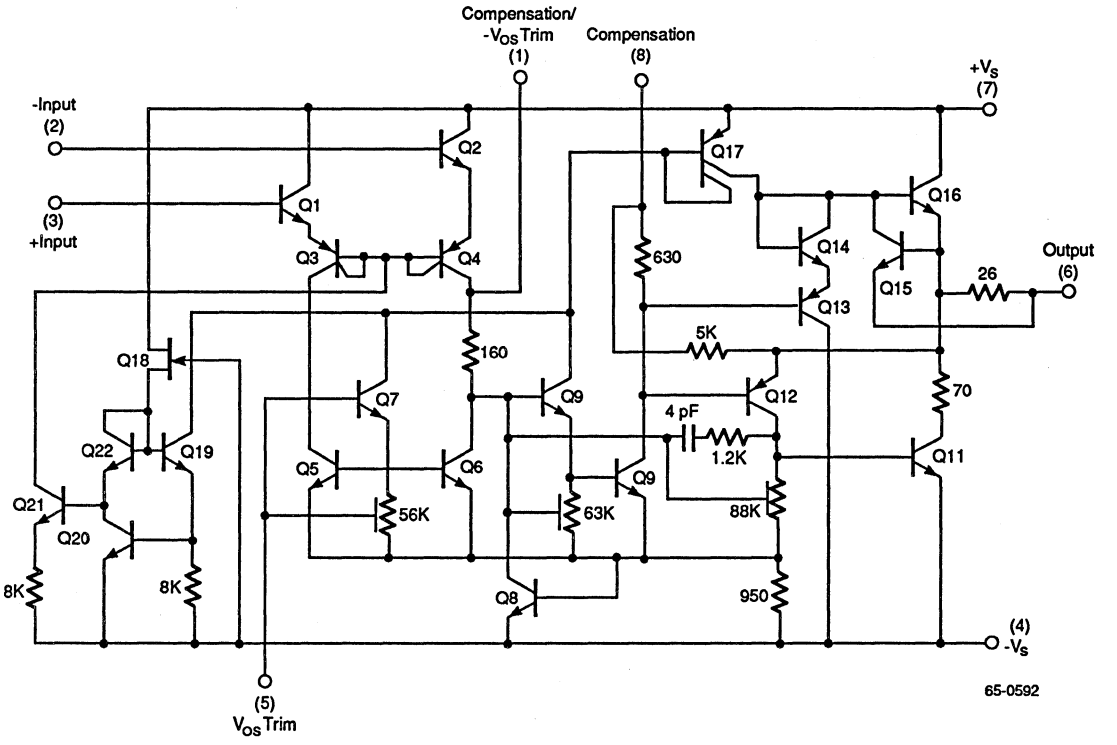


65-0605

Voltage Comparator for Driving RTL logic or High Current Driver

Linear

Schematic Diagram



LM108A/LH2108A
Precision Operational Amplifiers

Description

The LM108A operational amplifiers features low input bias current combined with the advantages of bipolar transistor construction; input offset voltages and currents are kept low over a wide range of temperature and supply voltage. Raytheon's superbeta bipolar manufacturing process includes extra treatment at epitaxial growth to ensure low input voltage noise.

The LH2108 consists of two LM108 ICs in one 16-lead DIP. The "A" versions meet tighter electrical specifications than the plain versions. All types are available with 883B military screening.

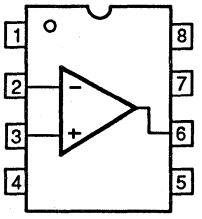
Features

- Low input bias current — 2 nA
- Low input offset current — 200 pA
- Low input offset voltage — 500 μV
- Low input offset drift — 5 μV/°C
- Wide supply range — ±3V to ±20V
- Low supply current — 0.6 mA
- High PSRR — 96 dB
- High CMRR — 96 dB
- MIL-STD-883B available

LM108A/LH2108A

Connection Information

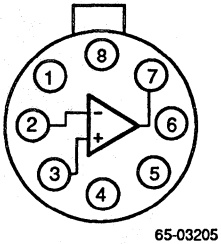
8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Comp
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	Comp

65-03206A

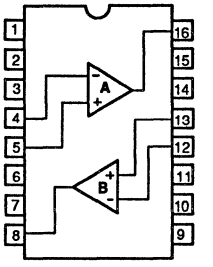
8-Lead
TO-99 Metal Can
(Top View)



Pin	Function
1	Comp
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	Comp

65-03205

16 Lead DIP
(Top View)



Pin	Function	Pin	Function
1	$+V_S$ (A)	9	$+V_S$ (B)
2	Comp (A)	10	Comp (B)
3	Comp (A)	11	Comp (B)
4	-Input (A)	12	-Input (B)
5	+Input (A)	13	+Input (B)
6	$-V_S$	14	NC
7	NC	15	NC
8	Output (B)	16	Output (A)

65-02658

Ordering Information

Part Number	Package	Operating Temperature Range
LM108D	D	-55°C to +125°C
LM108D/883B	D	-55°C to +125°C
LM108AD	D	-55°C to +125°C
LM108AD/883B	D	-55°C to +125°C
LM108T	T	-55°C to +125°C
LM108T/883B	T	-55°C to +125°C
LM108AT	T	-55°C to +125°C
LM108AT/883B	T	-55°C to +125°C
LH2108D	D	-55°C to +125°C
LH2108D/883B	D	-55°C to +125°C
LH2108AD	D	-55°C to +125°C
LH2108AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D = 16 lead ceramic DIP (LH2108)
D = 8 lead ceramic DIP (LM108)
T = 8-lead metal can TO-99

Absolute Maximum Ratings

Supply Voltage ..... ±20V
Differential Input Current[1] ..... ±10 mA
Input Voltage[2] ..... ±15 V
Output Short Circuit[2] ..... Continuous
Operating Temperature Range
Range ..... -55°C to +125°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Notes:
1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Thermal Characteristics

	8-Lead TO-99 Metal Can	8-Lead Ceramic DIP	16-Lead Ceramic DIP
Max. Junction Temp.	+175°C	+175°C	+175°C
Max. P_D T_A <50°C	658 mW	833 mW	1042 mW
Therm. Res θ_{JC}	50°C/W	45°C/W	60°C/W
Therm. Res. θ_{JA}	190°C/W	150°C/W	120°C/W
For T_A >50°C Derate at	5.26 mW/°C	8.33 mW/°C	8.38 mW/°C

Electrical Characteristics

($\pm 5V \leq V_S \leq \pm 20V$ and $T_A \leq +25°C$ unless otherwise noted)

Parameters	Test Conditions	LM108A/LH2108A			LM108/LH2108			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.3	0.5		0.7	2.0	mV
Input Offset Current			0.05	0.2		0.05	0.2	nA
Input Bias Current			0.8	2.0		0.8	2.0	nA
Input Resistance1		30	70		30	70		MΩ
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	80	300		50	300		V/mV
Supply Current	Each Amplifier		0.3	0.6		0.3	0.6	mA

Electrical Characteristics

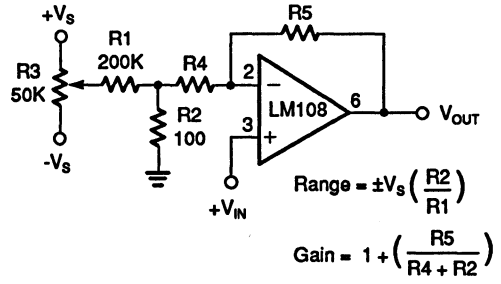
($\pm 5V \leq V_S \leq \pm 20V$; $-55°C \leq T_A \leq +125°C$ unless otherwise noted)

Parameters	Test Conditions	LM108A/LH2108A			LM108/LH2108			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.4	1.0		1.0	3.0	mV
Avg. Input Offset Voltage Drift$_2$			1.0	5.0		3.0	15	µV/°C
Input Offset Current			0.1	0.4		0.1	0.4	nA
Avg. Input Offset Current Drift$_2$			0.5	2.5		0.5	2.5	pA/°C
Input Bias Current			1.0	3.0		1.0	3.0	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	40	200		25	200		V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$ $V_S = \pm 20V$	±16	±18		±16	±18		V
Input Voltage Range	$V_S = \pm 15V$	±13.5			±13.5			V
Common Mode Rejection Ratio	$V_{CM} = \pm 13.5$ $V_S = \pm 15V$	96	110		85	100		dB
Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 20V$	96	110		80	96		dB
Supply Current	Each Amplifier			0.6			0.6	mA

Notes:
1. Guaranteed by input bias current specification.
2. Sample tested

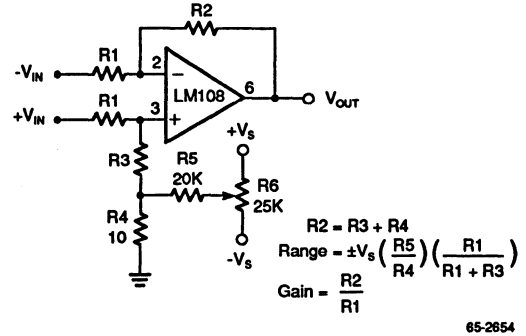
Typical Applications

The LM108 series has very low input offset and bias currents; the user is cautioned that printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to achieve the LM108A's rated performance. It is suggested that board leakage be minimized by encircling the input pins with a guard ring maintained at a potential close to that of the inputs. The guard ring should be driven by a low impedance source such as an amplifiers's output or ground.



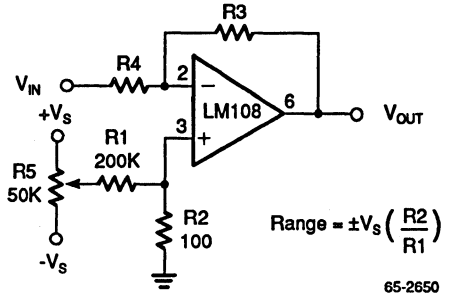
65-2652

Offset Adjustment for non-Inverting Amplifiers



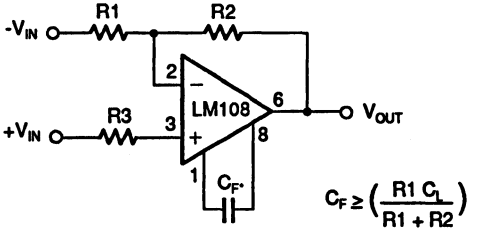
65-2654

Offset Adjustment for Differential Amplifiers



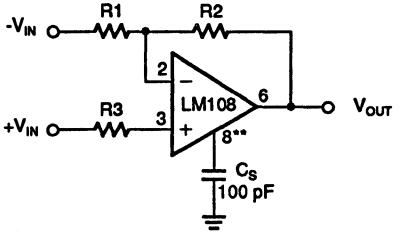
65-2650

Offset Adjustment for Inverting Amplifiers



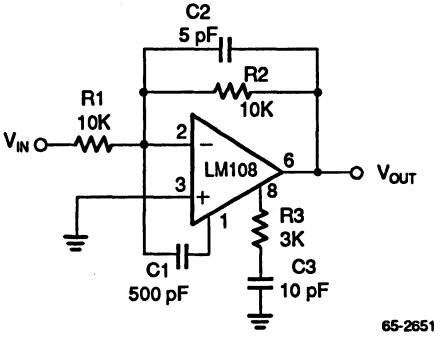
65-2653

Standard Compensation Circuit



65-2655

Alternate Frequency Compensation

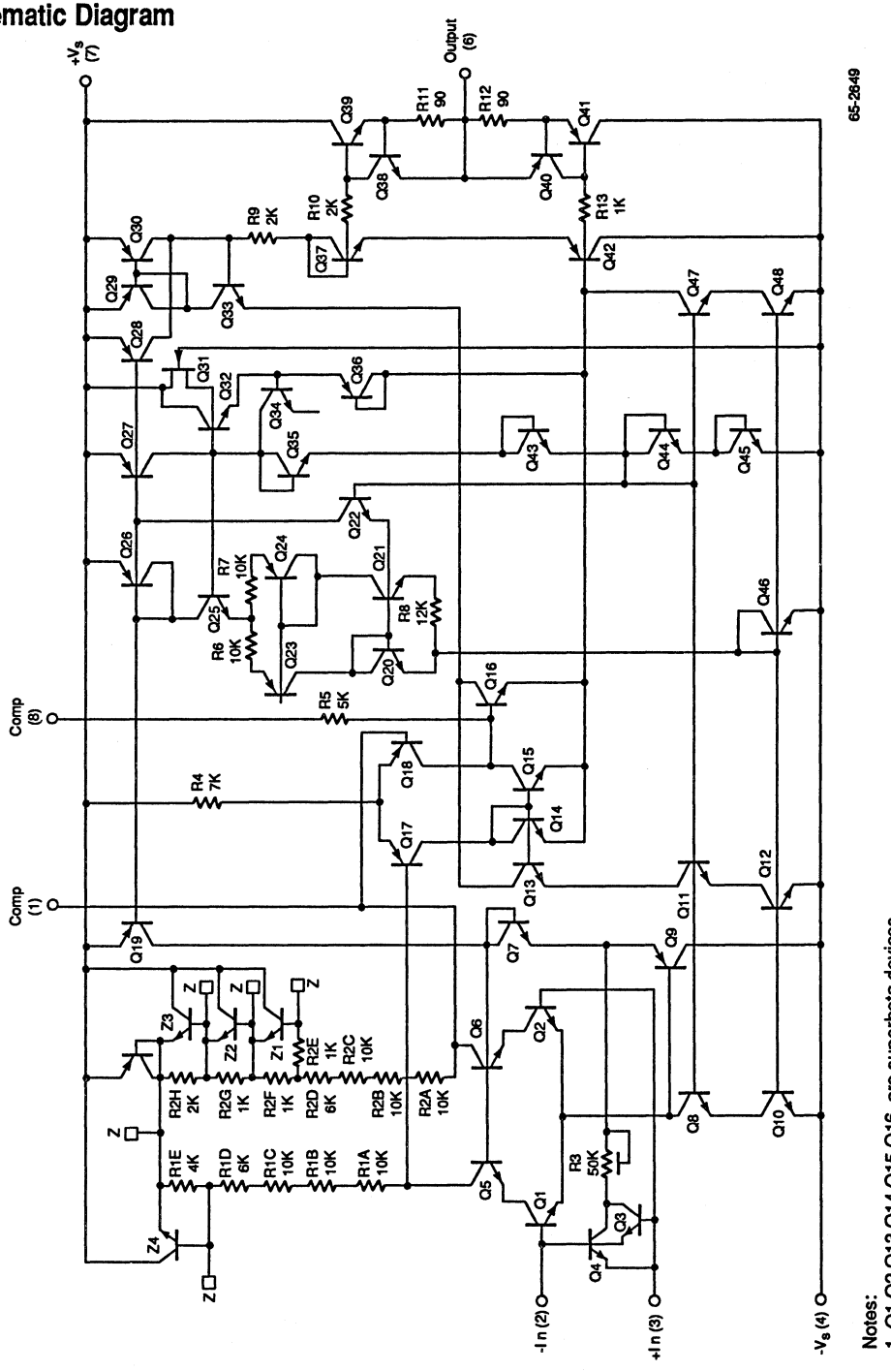


65-2651

Feedforward Compensation

Linear

Schematic Diagram



Notes:
1. Q1,Q2,Q13,Q14,Q15,Q16 are superbeta devices.
2. Pin numbers shown are for 8-lead packages.

LM124/324
Single-Supply Quad Operational Amplifier

Description

Each of the devices in this series consists of four independent high-gain operational amplifiers that are designed for single-supply operation. Operation from split power supplies is also possible and the low power supply drain is independent of the magnitude of the power supply voltage.

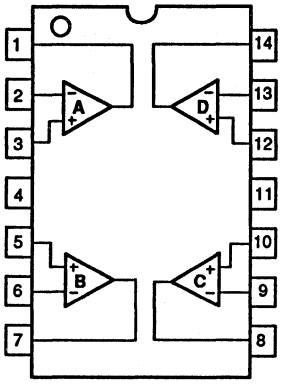
Used with a dual supply, the circuit will operate over a wide range of supply voltages. However, a large amount of crossover distortion may occur with loads to ground. An external current-sinking resistor to $-V_S$ will reduce crossover distortion. There is no crossover distortion problem in single-supply operation if the load is direct-coupled to ground.

Features

- Large DC voltage gain — 100 dB
- Compatible with all forms of logic
- Temperature compensated
- Unity Gain Bandwidth — 1 MHz
- Large output voltage swing — 0V to ($+V_S$ -1.5V)
- Input common mode voltage range includes ground

Connection Information

14-Lead Dual In-Line Package
(Top View)



65-0418

Pin	Function	Pin	Function
1	Output (A)	8	Output (C)
2	-Input (A)	9	-Input (C)
3	+Input (A)	10	+Input (C)
4	$+V_S$	11	Ground
5	+Input (B)	12	+Input (D)
6	-Input (B)	13	-Input (D)
7	Output (B)	14	Output (D)

Ordering Information

Part Number	Package	Operating Temperature Range
LM324M	M	0°C to +70°C
LM324N	N	0°C to +70°C
LM124D	D	-55°C to +125°C
LM124D/883B	D	-55°C to +125°C

Notes:
883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
M = 14-lead plastic SOIC

Absolute Maximum Ratings

Supply Voltage ..... +32V or ±16V
Differential Input Voltage 32V
Input Voltage ..... -0.3V to +32V
Output Short Circuit to Ground[1]
(One Amplifier) + $V_s \leq 15V$ and
T_A = +25°C ..... Continuous
Input Current ($V_{IN} < -0.3V$)[2] ..... 50 mA
Operating Temperature Range
LM124 ..... -55°C to +125°C
LM324 ..... 0°C to +70°C

See Notes on next page.

Thermal Characteristics

	14-Lead Small Outline	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+125°C	+175°C
Max. P_D T_A <50°C	300 mW	468 mW	1042 mW
Therm. Res θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Electrical Characteristics

($+V_S$ = +5.0V[3] and T_A= +25°C, unless otherwise noted)

Parameters	Test Conditions	LM124			LM324			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage [3]			±2.0	±5.0		±2.0	±7.0	mV
Input Bias Current [4]			45	150		45	250	nA
Input Offset Current			±3.0	±30		±5.0	±50	nA
Input Voltage Range [5]	$+V_S$ = +30V	0		$+V_S$ -1.5	0		$+V_S$ -1.5	V
Supply Current	R_L = ∞, $+V_S$ = 30V		1.5	3.0		1.5	3.0	mA
(Over Temperature)	R_L = ∞ on all op amps		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	$+V_S$ = 15V (for large V_{OUT} swing) $R_L \geq 2$ kΩ	50	100		25	100		V/mV
Output Voltage Swing								
V_{OH}	$+V_S$ = +30V, R_L = 2kΩ	26			26			V
V_{OH}	$R_L \geq 10$ kΩ	27	28		27	28		V
V_{OL}	$+V_S$ = +5.0V, R_L = 10 kΩ		5.0	20		5.0	20	mV
Common Mode Rejection Ratio		70	85		65	70		dB
Power Supply Rejection Ratio		65	100		65	100		dB
Channel Separation [6]	F = 1 kHz to 20 kHz (input referred)		-120			-120		dB
Output Current								
Source	V_{IN+} = 1V, V_{IN-} = 0V, $+V_S$ = 15V	20	40		20	40		mA
Sink	V_{IN-} = 1V, V_{IN+} = 0V, $+V_S$ = 15V	10	20		10	20		mA
	V_{IN-} = 1V, V_{IN+} = 0V, V_{OUT} = 200 mV	12	50		12	50		µA

Notes:

1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $+V_S$. At values of supply voltage in excess of $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns to a value greater than -0.3V.
3. V_{OUT} = 1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V; and over the full common mode range (0V to $+V_S$ -1.5V).
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
5. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +32V without damage.
6. Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Electrical Characteristics

($+V_S$ = +5.0V), 124 = -55° ≤ T_A ≤ 125°C, 324 = 0°C ≤ T_A ≤ 70°C unless other wise noted)

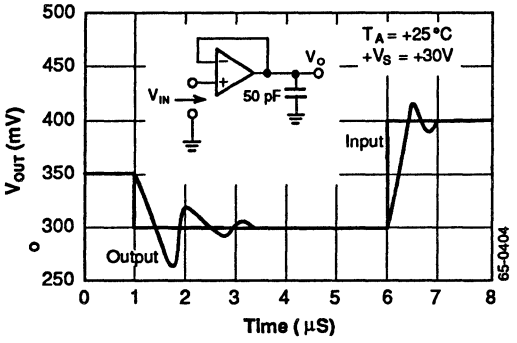
Parameters	Test Conditions	LM124			LM324			Units
		Min	Typ	Max	Min	Typ	Max	
Short Circuit Current[1]	T_A = +25°C		40	60		40	60	mA
Input Offset Voltage [2]				±7.0			±9.0	mV
Input Offset Voltage Drift	R_S = 0Ω		7.0			7.0		µV/°C
Input Offset Current				±100			±150	nA
Input Offset Current Drift			10			10		pA/°C
Input Bias Current[3]			40	300		40	500	nA
Input Voltage Range[4]	$+V_S$ = +30V	0		$+V_S$ -2.0	0		$+V_S$ -2.0	V
Large Signal Voltage Gain	$+V_S$ = +15V (For Large V_{OUT} Swing) R_L ≥ 2.0 kΩ	25			15			V/mV
Output Voltage Swing								
V_{OH}	$+V_S$ = +30V, R_L = 2 kΩ	26			26			V
V_{OH}	R_L ≥ 10 kΩ	27	28		27	28		V
V_{OL}	$+V_S$ = +5.0V, R_L = 10 kΩ		5.0	20		5.0	20	mV
Output Current								
Source	V_{IN+} = +1.0V, V_{IN-} = 0V, $+V_S$ = +15V	10	20		10	20		mA
Sink	V_{IN-} = +1.0V, V_{IN+} = 0V, $+V_S$ = +15V	5.0	8.0		5.0	8.0		mA
Differential Input Voltage[4]				$+V_S$			$+V_S$	V

Notes:

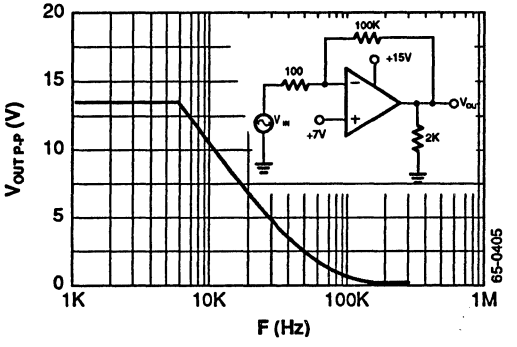
1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $+V_S$. At values of supply voltage in excess of $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. V_{OUT} = 1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V; and over the full common mode range (0V to $+V_S$ -1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +32V without damage.

Typical Performance Characteristics

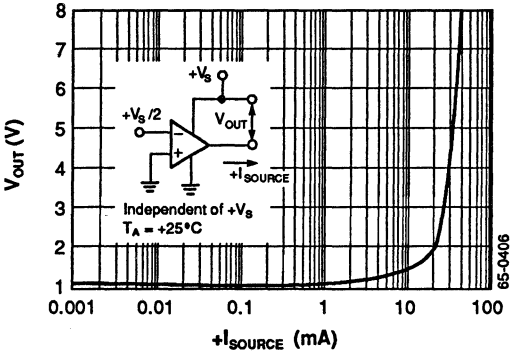
Follower Small Signal Pulse Response



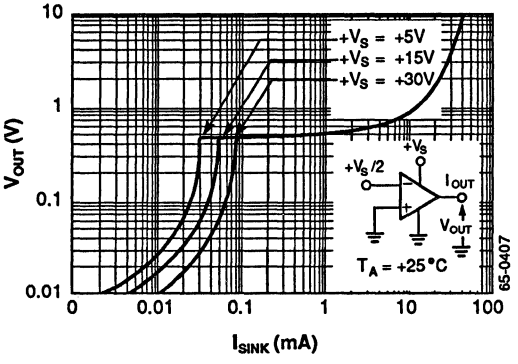
Output Voltage Swing vs. Frequency



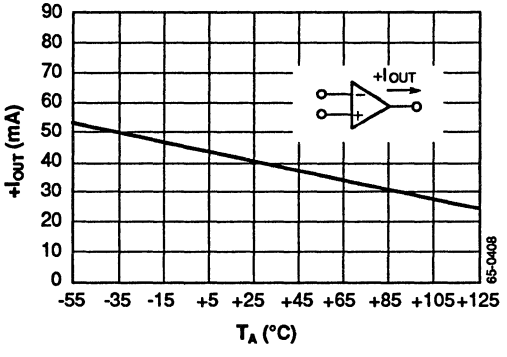
Output Voltage vs. Output Source Current



Output Voltage vs. Output Sink Current



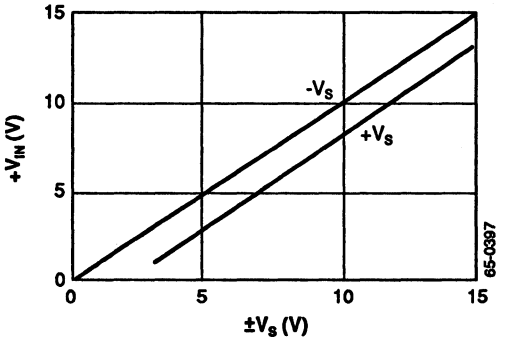
Current Limiting
Output Current vs. Temperature



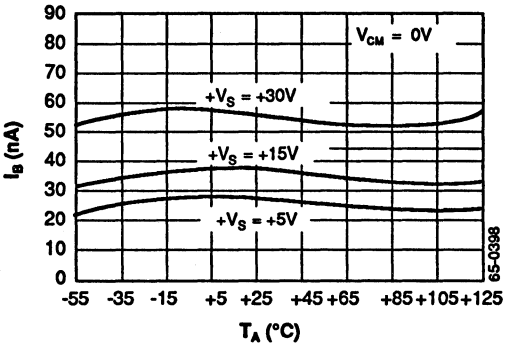
Linear

Typical Performance Characteristics (Continued)

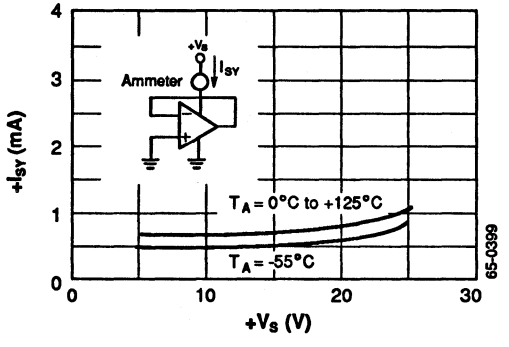
Input Voltage vs. Supply Voltage



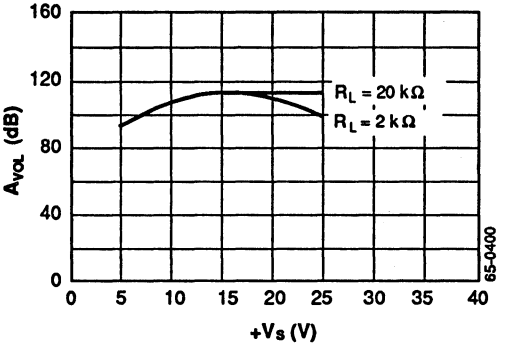
Input Bias Current vs. Temperature



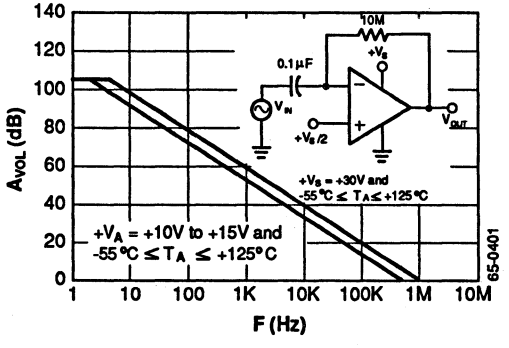
Supply Current vs. Supply Voltage



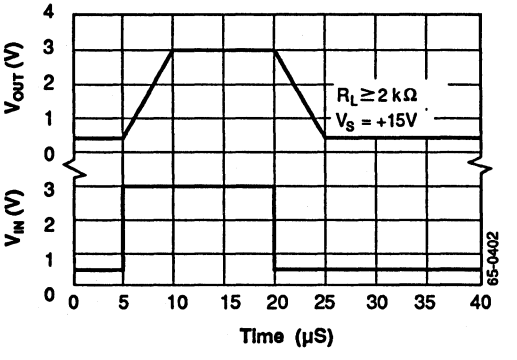
Open loop Voltage Gain vs. Supply Voltage



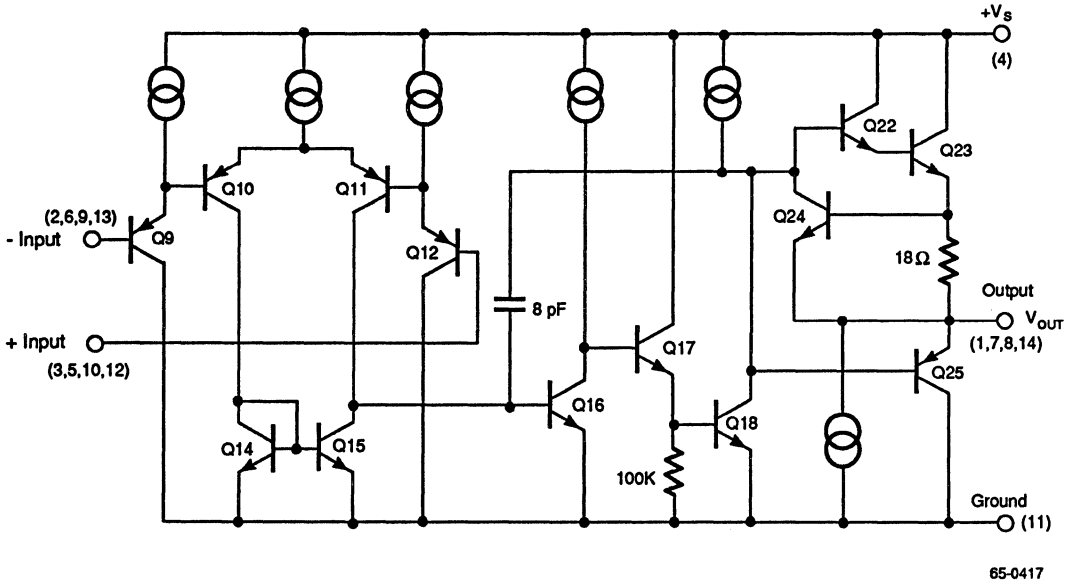
Open Loop Voltage Gain vs Frequency



Follower Large Pulse Response Signal vs. Time



Schematic Diagram



LM148
Low Power Quad 741 Operational Amplifier

Description

The LM148 is a true quad 741. It consists of four independent high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias currents which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple 741 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

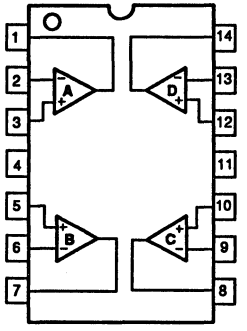
Features

- 741 op amp operating characteristics
- Low supply current drain — 0.6 mA/amplifier
- Class AB output stage — no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage — 1.0 mV
- Low input offset current — 4.0 nA
- Low input bias current — 30 nA
- Unity gain bandwidth — 1.0 MHz
- Channel Separation — 120 dB
- Input and output overload protection

LM148

Connection Information

14-Lead Dual In-Line Package
(Top View)



65-0418

Pin	Function	Pin	Function
1	Output (A)	8	Output (C)
2	-Input (A)	9	-Input (C)
3	+Input (A)	10	+Input (C)
4	$+V_S$	11	Ground
5	+Input (B)	12	+Input (D)
6	-Input (B)	13	-Input (D)
7	Output (B)	14	Output (D)

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Differential Input Voltage 44V
Input Voltage[1] ..... ±22V
Output Short Circuit Duration[2] ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
LM148 ..... -55°C to +125°C
Lead Soldering Temperature (60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit to ground on one amplifier only.

Ordering Information

Part Number	Package	Operating Temperature Range
LM148D	D	-55°C to +125°C
LM148D/883B*	D	-55°C to +125°C

Notes:
*/883B suffix denotes Mil-Std-883, Level B processing
D = 14-lead ceramic DIP

Thermal Characteristics

	14-Lead Ceramic DIP
Max. Junc. Temp.	+175°C
Max. P_D T_A < 50°C	1042 mW
Therm. Res. θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A > 50°C Derate at	8.33 mW per °C

Electrical Characteristics

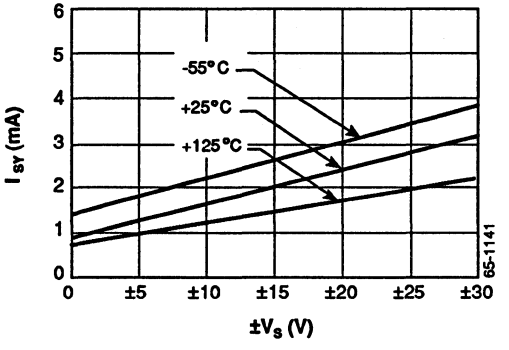
(V_S = ±15V and T_A = 25°C, unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0	mV
Input Offset Current			4.0	25	nA
Input Bias Current			30	100	nA
Input Resistance[1] (Differential Mode)		0.8	2.5		MΩ
Supply Current All Amplifiers	V_S = ±15V		2.4	3.6	mA
Large Signal Voltage Gain	V_S = ±15V V_{OUT} = ±10V, $R_L \geq 2k\Omega$	50	160		V/mV
Channel Separation	F =1 Hz to 20 kHz		120		dB
Unity Gain Bandwidth			1.0		MHz
Phase Margin				60	Degrees
Slew Rate				0.5	V/μS
Short Circuit Current			25		mA
The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ + 125°C.					
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0	mV
Input Offset Current				75	nA
Input Bias Current				325	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = 10V25 $R_L < 2\ k\Omega$				V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13		V
	R_L = 2 kΩ	±10	±12		V
Input Voltage Range	V_S = ±15V	±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		dB

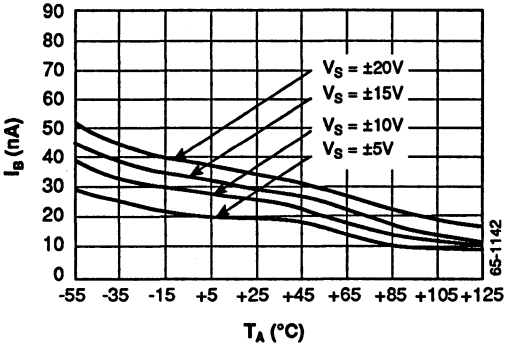
Note:
1. Guaranteed by design but not tested.

Typical Performance Characteristics

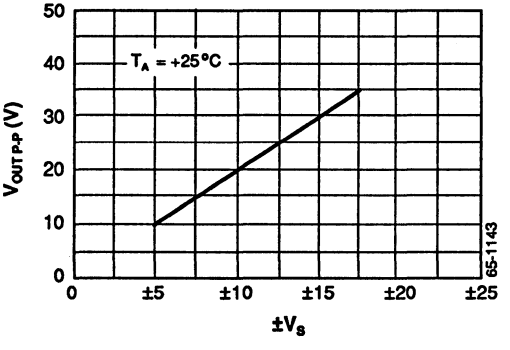
Supply Current vs. Supply Voltage



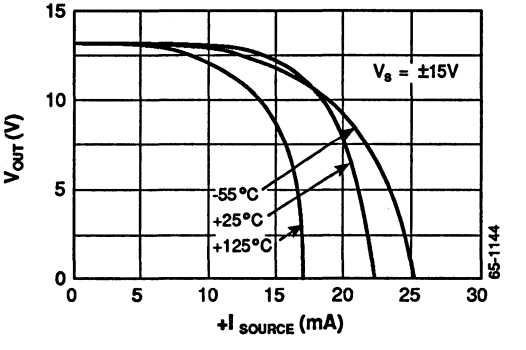
Input Bias Current vs. Temperature



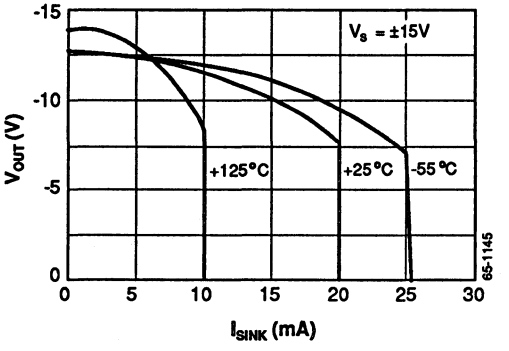
Output Voltage Swing vs. Supply Voltage



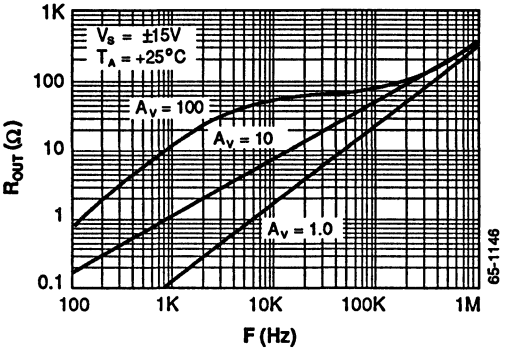
Positive Current Limit
Output Voltage vs. Output Source Current



Negative Current Limit
Output Voltage vs. Output Sink Current

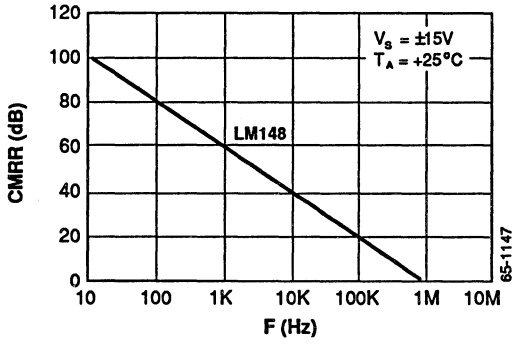


Output Impedance vs. Frequency

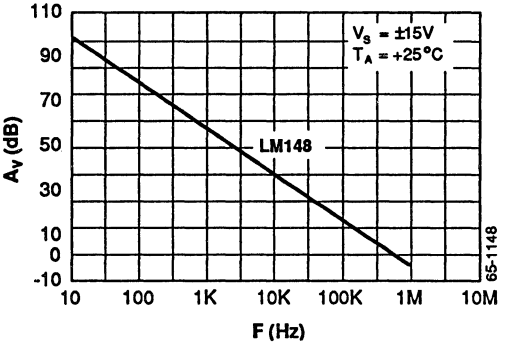


Typical Performance Characteristics (Continued)

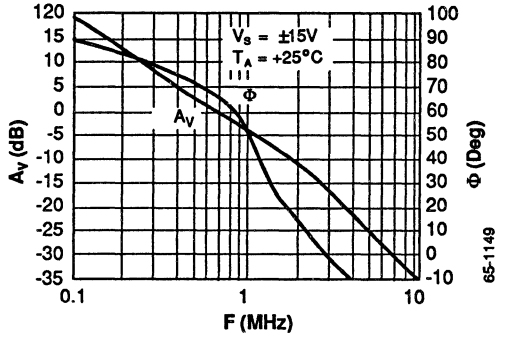
CMRR vs. Frequency



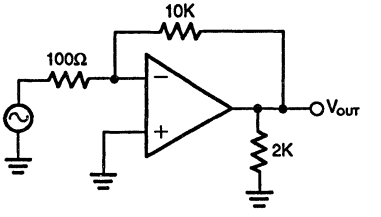
Open Loop Gain vs. Frequency



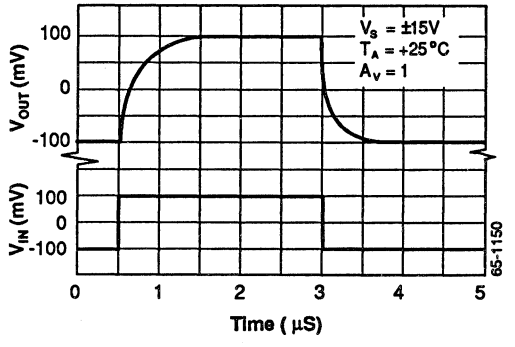
Gain, Phase vs. Frequency



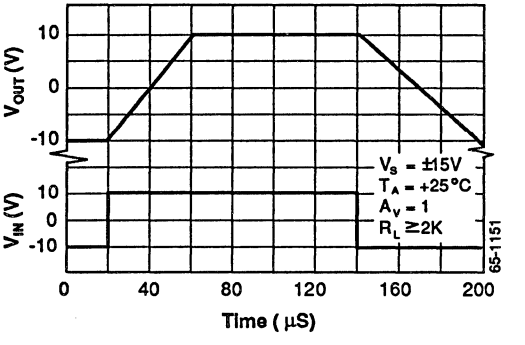
Gain, Phase Test Circuit



Small Signal Pulse Response
Input, Output Voltage vs. Time



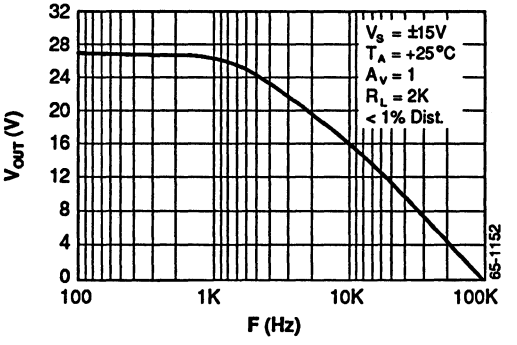
Large Signal Pulse Response
Output Voltage vs. Time



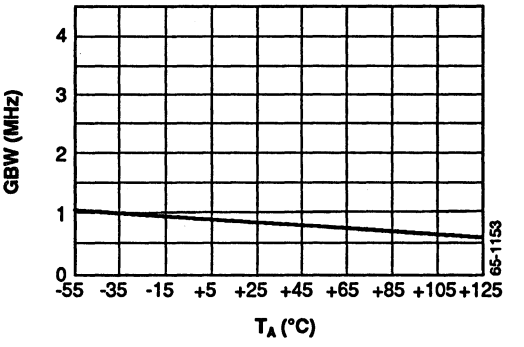
Linear

Typical Performance Characteristics (Continued)

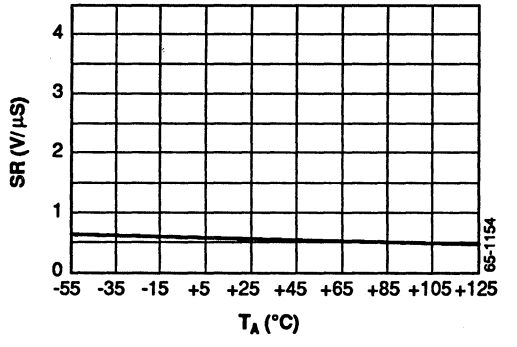
Undistorted Output Voltage Swing vs. Frequency



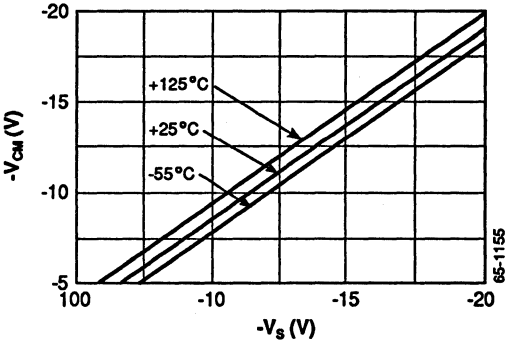
Gain Bandwidth Product vs. Temperature



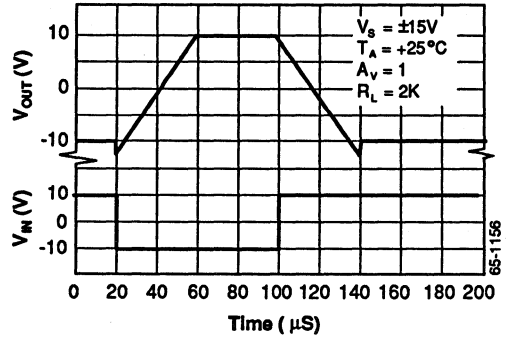
Slew Rate vs. Temperature



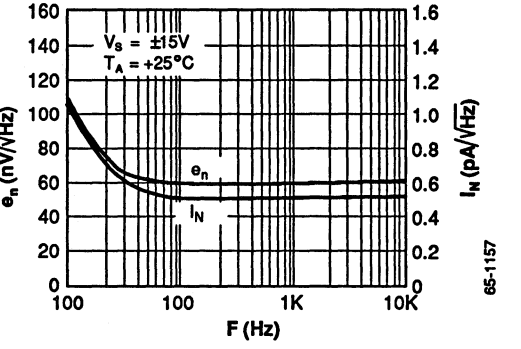
Negative Common Mode Input Voltage vs. Supply Voltage



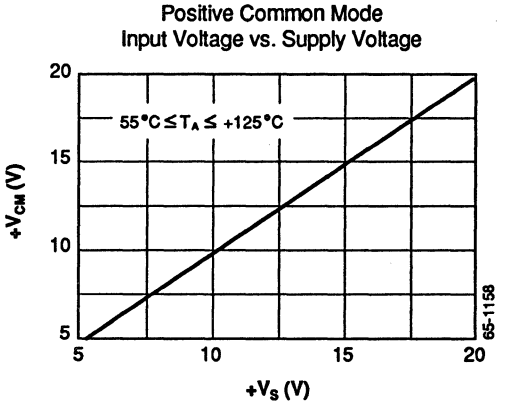
Inverting Large Signal Pulse Response Input, Output Voltage vs. Time



Input Noise Voltage, Current Densities vs. Frequency



Typical Performance Characteristics (Continued)



Typical Simulation

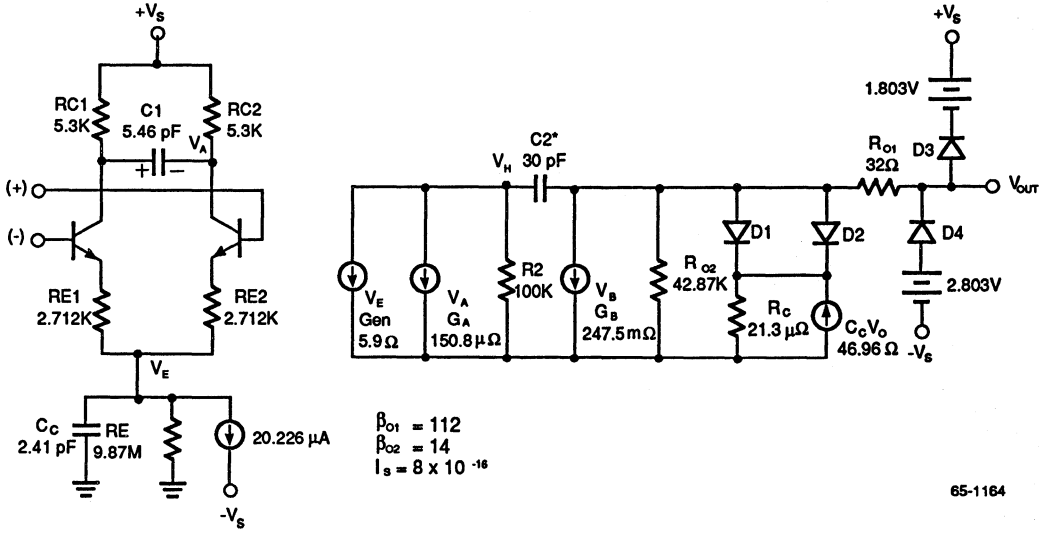


Figure 1. LM148 Macromodel for Computer Simulation

Linear

Typical Applications

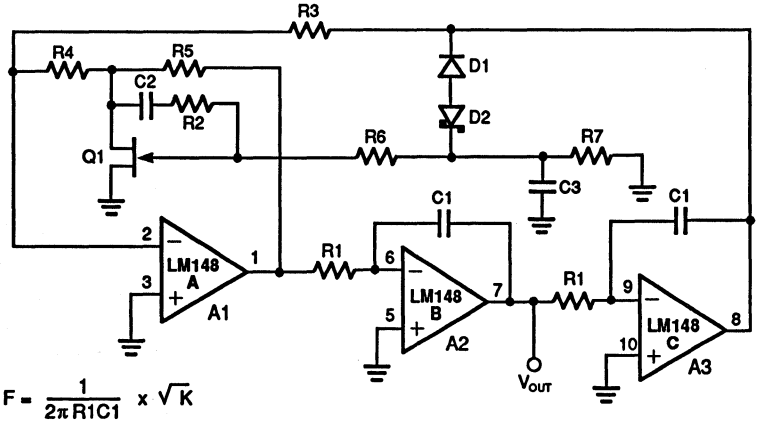
The LM148 low power quad operational amplifier exhibits performance comparable to the popular 741. Substitution can therefore be made with no change in circuit behavior.

The input characteristics of these devices allow differential voltages which exceed the supplies. Output phase will be correct as long as one of the inputs are within the operating common mode range. If both exceed the negative limit, the output will latch positive. Current limiting resistors should be used on the inputs in case voltages become excessive.

When capacitive loading becomes much greater than 100pF, a resistor should be placed between the output and feedback connection in order to reduce phase shift.

The 148 is short circuit protected to ground or the supplies continuously when only one of the tour amplifiers is shorted. If multiple shorts occur simultaneously, the unit can be destroyed due to excessive power dissipation.

To assure stability and to minimize pickup, feedback resistors should be placed close to the input to maximize the feedback pole frequency (a function of input to ground capacitance). A good rule of thumb is that the feedback pole frequency should be 6 times the operating -3.0B frequency. If less, a lead capacitor should be placed between the output and input.



$$F = \frac{1}{2\pi R1C1} \times \sqrt{K}$$

$$K = \frac{R4R5}{R3}\left(\frac{1}{R_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right)$$

65-1139

$$R_{DS} \cong \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

F_{MAX} = 5.0 kHz, THD≤ 0.03%

R1 = 100K pot., C1 = 0.0047μF, C2 = 0.01μF, C3 = 0.1μF, R2 = R6 = R7 = 1M, R3 = 5.1K, R4 = 12Ω.

R5 = 240Ω, Q1 = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in feedback loop of A3.

Figure 2. One Decade Low Distortion Sinewave Generator

Typical Applications (Continued)

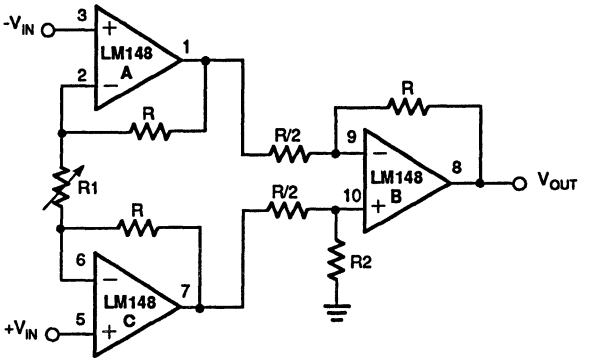


Figure 3. Low Cost Instrumentation Amplifier

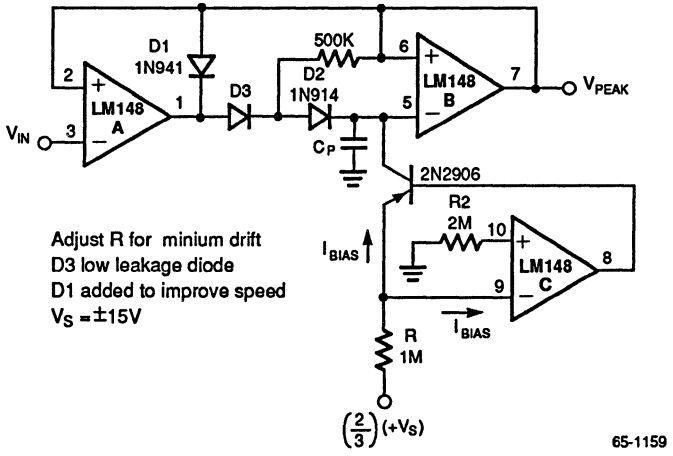
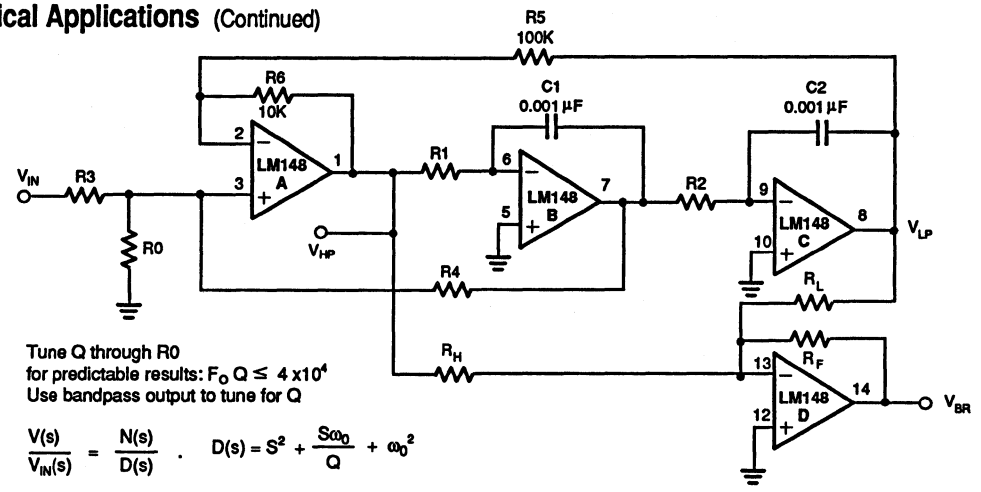


Figure 4. Low Voltage Peak Detector With Bias Current Compensation

Linear

Typical Applications (Continued)



Tune Q through R0
for predictable results: $F_O\,Q \leq 4 \times 10^4$
Use bandpass output to tune for Q

$$\frac{V(s)}{V_{IN}(s)} = \frac{N(s)}{D(s)} \quad . \quad D(s) = S^2 + \frac{S\omega_0}{Q} + \omega_0^2$$

$$N_{HP(S)} = S^2\,H_{OHP},\ N_{BP(S)} = \frac{-S\omega_0\,H_{OBP}}{Q} \qquad N_{LP} = \omega_0^2\,H_{OLP}$$

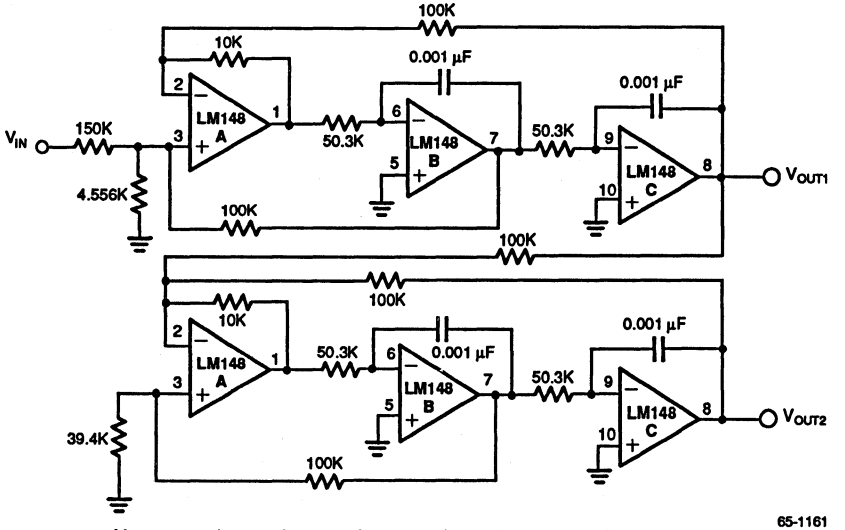
$$F_O = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}}\ , \quad t1 = R1C1,\ Q = \left(\frac{1 + R4 \mid R3 + R4 \mid R0}{1 + R6 \mid R5}\right)\left(\frac{R6}{R5}\ \frac{t1}{t2}\right)^{1/2}$$

$$F_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L\,t1\ t2}\right)^{1/2}\ ,\ H_{OHP} = \frac{1 + R6 \mid R5}{1 + R3 \mid R0 + R3 \mid R4}\ ,\ H_{OBP} = \frac{1 + R4 \mid R3 + R4 \mid R0}{1 + R3 \mid R0 + R3 \mid R4}$$

$$H_{OLP} = \frac{1 + R5 \mid R6}{1 + R3 \mid R0 + R3 \mid R4}$$

65-1160

Figure 5. Universal State-Space Filter

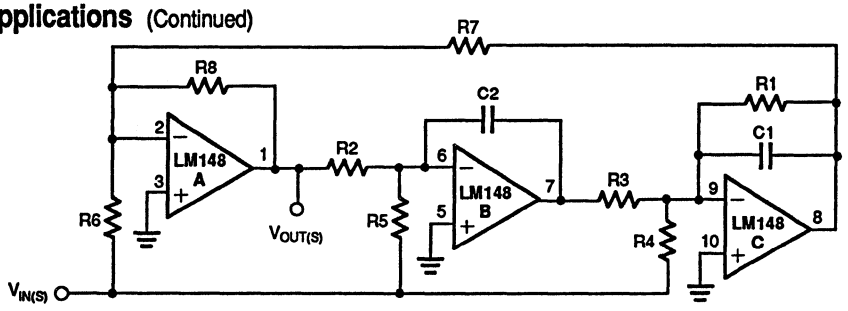


65-1161

Use general equations, and tune each section separately.
Q_{1st} Section = 0.541, Q_{2nd} Section = 1.306.
The response should have 0 dB peaking.

Figure 6. 1 kHz 4-Pole Butterworth Filter

Typical Applications (Continued)



$$Q = \sqrt{\frac{R8}{R7}}\left(\frac{R1C1}{\sqrt{R3C2R2C1}}\right), F_O = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}}\left(\frac{1}{\sqrt{R2R3C1C2}}\right), F_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

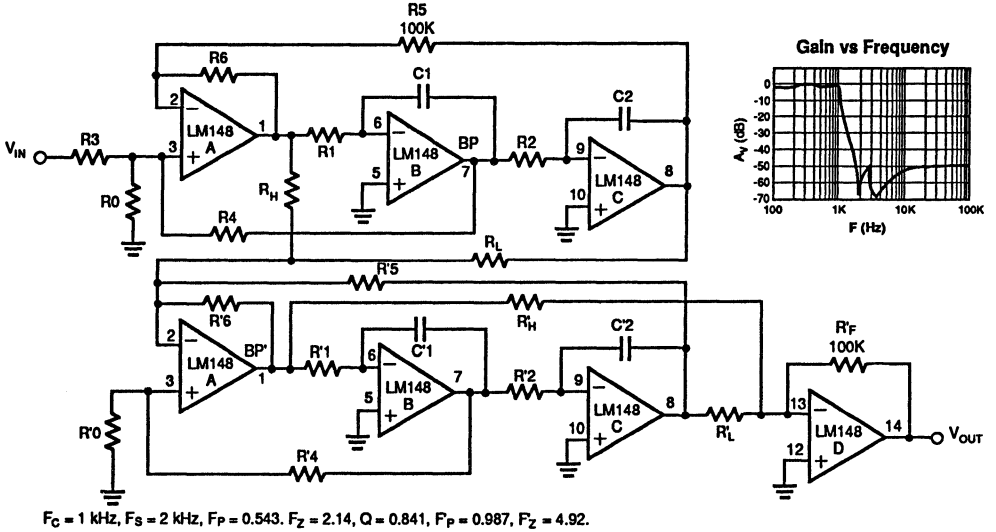
Necessary condition for notch : $\frac{1}{R6} = \frac{R1}{R4R7}$

Examples: F_{NOTCH} = 3 kHz, Q = 5, R1 = 270K, R2 = R3 = 20K, R4 = 27K, R5 = 20K, R6 = R8 = 10K, R7 = 100K. C1 = C2 = 0.001 µF.

Better noise performance than the state-space approach.

65-1162

Figure 7. 3 Amplifier Bi-Quad Notch Filter



F_C = 1 kHz, F_S = 2 kHz, F_P = 0.543. F_Z = 2.14, Q = 0.841, F'_P = 0.987, F'_Z = 4.92.
Q' = 4.403 normalized to ripple BW.

$$F_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\left(\frac{1}{t}\right), F_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}}\left(\frac{1}{t}\right), Q = \frac{1 + R4/R3 + R4/R0}{1 + R6/R5} \times \sqrt{\frac{R6}{R5}}, Q' = \sqrt{\frac{R'6}{R'5}} \times \frac{1 + R'4/R'0}{1 + R'6/R'5 + R'6/R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the B'P outputs to tune Q, Q', tune the 2 sections separately.
R1 = R2 = 92.6K, R3 = R4 = R5 = 100K, R6 = 10K, R0 = 107.8K, R_L = 100K, R_H = 155.1K,
R'1 = R'2 = 50.9K, R'4 = R'5 = 100K, R'6 = 10K, R'0 = 5.78K, R'_L = 100K, R'_H = 248.12K, R'_F = 100K.

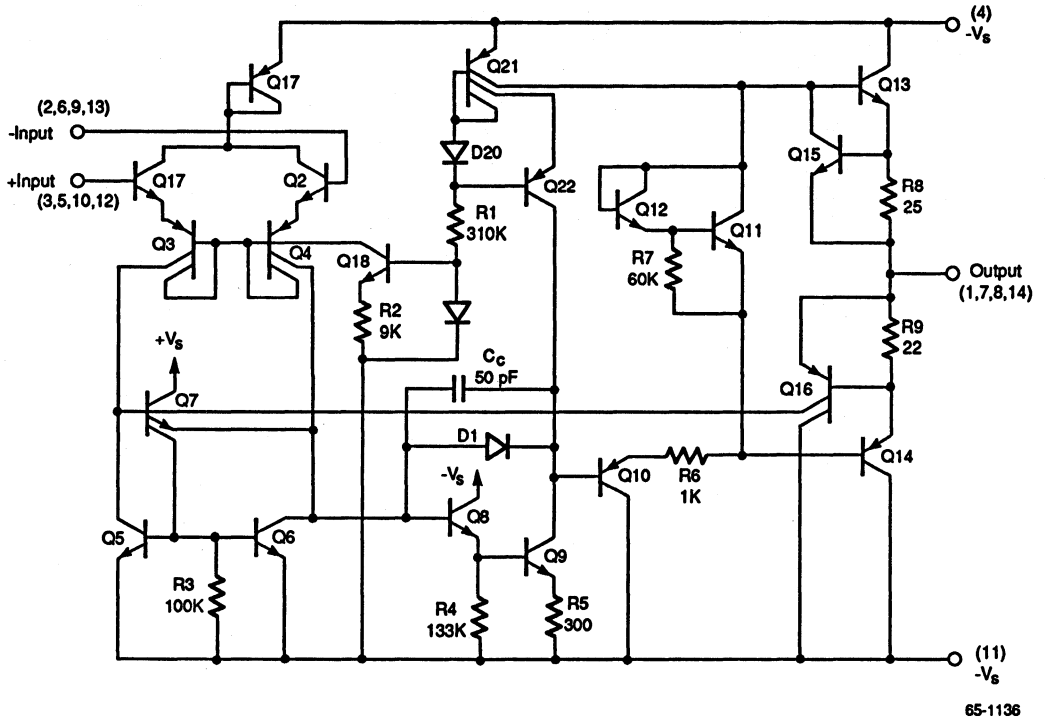
65-1163

All capacitors are 0.001 µF.

Figure 8. 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)

Linear

Schematic Diagram (1/4 Shown)



OP- 07
Precision Operational Amplifier

Description

The OP-07 operational amplifier is designed for precision low-level signal conditioning where ultra low V_{OS} and TCV_{OS} are required along with very low bias currents. Internal compensation eliminates the need for external components. Novel circuit design and tight process controls are used to obtain very low values of V_{OS} which is further reduced by computer controlled digital nulling techniques at test. Low frequency noise is minimized. Internal biasing techniques reduce external bias and offset currents to values on the order of ±1 nA over the military temperature range. The OP-07 is a direct replacement for the 108A. The OP-07 can also replace chopper stabilized amplifiers in many applications.

Features

- Low noise – 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Ultra low V_{OS} – 10 μV
- Ultra low V_{OS} drift – 0.2 $\mu V/^{\circ}C$
- Long term stability — 0.2 $\mu V/Mo$
- Low Input bias current — ±1 nA
- High CMRR – 120 dB min
- Wide input voltage range — ±14V
- Wide supply voltage range — ±3V to ±22V
- Fits 108A and 741 sockets

OP-07

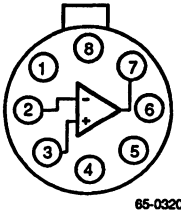
Ordering Information

Part Number	Package	Operating Temperature Range
OP-07CN	N	0°C to +70°C
OP-07DN	N	0°C to +70°C
OP-07EN	N	0°C to +70°C
OP-07CM	M	0°C to +70°C
OP-07DM	M	0°C to +70°C
OP-07EM	M	0°C to +70°C
OP-07T	T	-55°C to +125°C
OP-07T/883B	T	-55°C to +125°C
OP-07AT	T	-55°C to +125°C
OP-07AT/883B	T	-55°C to +125°C
OP-07D	D	-55°C to +125°C
OP-07D/883B	D	-55°C to +125°C
OP-07AD	D	-55°C to +125°C
OP-07AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC

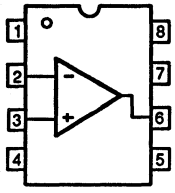
Connection Information

8-Lead
TO-99 Metal Can
(Top View)



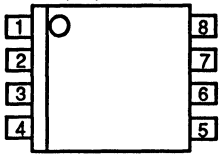
65-03205

8-Lead
Dual In-Line Package
(Top View)



65-03206A

8-Lead Plastic
Dual In-Line SO-8
(Top View)



65-02666

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$ (Case)
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation[2] ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
  Range ..... -65°C to +150°C
Operating Temperature Range
  OP-07A ..... -55°C to +125°C
  OP-07E/C/D ..... -25°C to +85°C
Lead Soldering Temperature
  SO-8 (10 sec) ..... +260°C
  TO-99, DIP (60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic SO	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+175°C	+125°C	+125°C
Max. P_D T_A <50°C	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	45°C/W	50°C/W	–	–
Therm. Res. θ_{JA}	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			10	25		30	75	µV
Long Term V_{OS} Stability[3,4]			0.2	1.0		0.2	1.0	µV/Mo
Input Offset Current			0.3	2.0		0.4	2.8	nA
Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2]	F_O = 10 Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10	13		10	13	
	F_O = 1000 Hz		9.6	11		9.6	11	
Input Noise Current[2]	0.1 Hz to 10 Hz		14	30		14	35	pA_{p-p}
Input Noise Current Density[2]	F_O = 10 Hz		0.32	0.80		0.32	0.80	$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14	0.23		0.14	0.23	
	F_O = 1000 Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[3]		30	80		20	60		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	300	500		200	500		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500$ kΩ, V_{OUT} = ±0.5V, V_S = ±3V	150	500		150	500		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ,	±12.5	±13		±12.5	±13		V
	$R_L \geq 2$ kΩ,	±12	±12.8		±12	±12.8		
	$R_L \geq 1$ kΩ,	±10.5	±12		±10.5	±12		
Slew Rate	$R_L \geq 2$ kΩ,	0.1	0.3		0.1	0.3		V/µS
Unity Gain Bandwidth	A_{VOL} = +1.0		0.8			0.8		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60		Ω
Power Consumption	V_S = ±15V		75	120		75	120	mW
	V_S = ±3V		4.0	6.0		4.0	6.0	
Offset Adjustment Range	R_{TRIM} = 20 kΩ		±4.0			±4.0		mV

Notes:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. OP-07A is tested fully warmed up.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.
4. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.54 µV.

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	75		60	150		60	150	µV
Long Term Input Offset Voltage Stability[3,4]			0.3	1.5		0.4	2.0		0.5	3.0	µV/Mo
Input Offset Current			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current			±1.2	±4.0		±1.8	±7.0		±2.0	±12	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.35	0.6		0.38	0.65		0.38	0.65	μV_{p-p}
Input Noise Voltage Density[2]	F_O = 10 Hz		10.3	18		10.5	20		10.5	20	$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10	13		10.2	13.5		10.2	13.5	
	F_O = 1000 Hz		9.6	11		9.8	11.5		9.8	11.5	
Input Noise Current[2]	0.1 Hz to 10 Hz		14	30		15	35		15	35	pA_{p-p}
Input Noise Current Density[2]	F_O = 10 Hz		0.32	0.8		0.35	0.9		0.35	0.9	$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14	0.23		0.15	0.27		0.15	0.27	
	F_O = 1000 Hz		0.12	0.17		0.13	0.18		0.13	0.18	
Input Resistance (Differential Mode)[3]		15	50		8.0	335		7.0	31		MΩ
Input Resistance (Common Mode)			160			120			120		GΩ
Input Voltage Range		±13	±14		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	94	107		90	104		90	104		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	200	500		1200	400		120	400		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500$ kΩ, V_{OUT} = ±0.5V, V_S = ±3V	150	500		100	400			400		V/mV
Output Voltage Swing	RL ≥ 10 kΩ	±12.5	±13		±12	±13		±12	±13		V
	$R_L \geq 2$ kΩ	±12	±12.8		±11.5	±12.8		±11.5	±12.8		
	$R_L \geq 1$ kΩ	±10.5	±12		±12						
Slew Rate	$R_L \geq 2$ kΩ	0.1	0.3		0.1	0.3		0.1	0.3		V/µS
Unity Gain Bandwidth	A_{VCL} = +1.0	0.8			0.8			0.8			MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		75	120		80	150		80	150	mW
	V_S = ±3V, R_L = ∞		4.0	6.0		4.0	8.0		4.0	8.0	
Offset Adjustment Range	R_{TRIM} = 20 kΩ		±4.0			±4.0			±4.0		mV

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤+125°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07B			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			25	60		60	200	µV
Average Input Offset Voltage Drift without External Trim[1]			0.2	0.6		0.3	1.3	µV/°C
With External Trim[3]	R_{TRIM} = 20 kΩ		0.2	0.6		0.3	1.3	
Input Offset Current			0.8	4.0		1.2	5.6	nA
Average Input Offset Current Drift[2]			5.0	25		8.0	50	pA/°C
Input Bias Current			±1.0	±4.0		±2.0	±6.0	nA
Average Input Bias Current Drift[2]			8.0	25		13	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM}= ±13V	106	123		106	123		dB
Power Supply Rejection Ratio	V_S = ± 3V to ±18V	94	106		94	106		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	200	400		150	400		V/mV
Output Voltage	R_L ≥ 2 kΩ,	±12	±12.6		±12	±12.6		V

Electrical Characteristics (V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			45	130		85	250		85	250	µV
Average Input Offset Voltage Drift without External Trim			0.3	1.3		0.5	1.8		0.7	2.5	µV/°C
With External Trim[3]	R_{TRIM} = 20 kΩ		0.3	1.3		0.4	1.6		0.7	2.5	
Input Offset Current			0.9	5.3		1.6	8.0		1.6	8.0	nA
Average Input Offset Current Drift[2]			8.0	35		12	50		12	50	pA/°C
Input Bias Current			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Average Input Bias Current Drift[2]			13	35		18	50		18	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM}= ±13V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	V_S = ± 3V to ±18V	90	104		86	100		86	100		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	180	450		100	400		100	400		V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±12	±12.6		±11	±12.6		±11	±12.6		V

Notes:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.

Digital Nulling Technique

The digital nulling technique involves the Zener diode nulling network of Figure 1. The zener diodes have relatively high breakdown voltages and never operate in the Zener mode. The purpose of the Zeners is to short out resistors R1, 2R1, 4R1, or 8R1 by forcing a high reverse current through the diode to metalize the junction. The input offset voltage can be adjusted by varying the collector resistor ratio. If the difference in the two collector resistors (R_C) is a small increment ΔR_C. V_{OS} can be written as:

$$V_{OS} = V_T \ln \frac{R_C + \Delta R_C}{R_C} = V_T \ln\left(1 + \frac{\Delta R_C}{R_C}\right)$$

for $\Delta R_C/R_C << 1.0$ $\ln(1+\Delta R_C/R_C) \sim \Delta R_C/R_C$, thus:

$$V_{OS} \approx V_T \frac{\Delta R_C}{R_C}$$

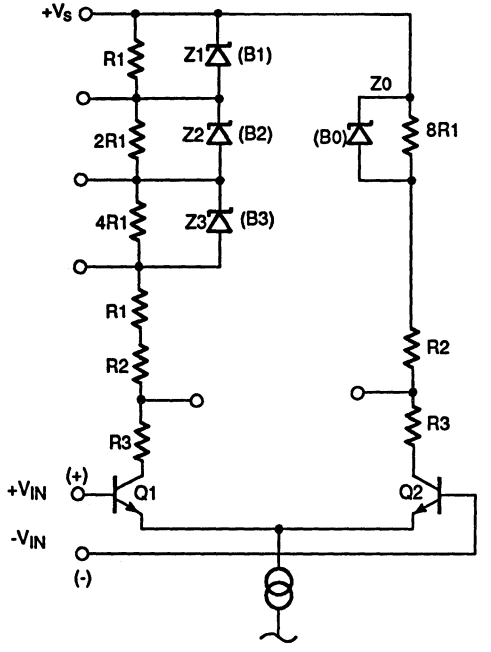
For Figure 1, R2 + R3 >> 8R1, thus

$$V_{OS} \approx V_T \frac{R_1}{8R1 + R2 + R3} (7 - B_3B_2B_1) \qquad (B0 = 1)$$

Or:

$$V_{OS} \approx V_T \frac{R1}{R2 + R3} (1 + B_3B_2B_1) \qquad (B0 = 0)$$

Where $B_3B_2B_1$ is a binary number which corresponds to the state of zener diodes Z1, Z2 and Z3 per Figure 1.



$$\Delta V_{OS}\ (25°C) \approx \frac{-2.6\ mV\ (7 - B_3B_2B_1)\ R1}{8R1 + R2 + R3} \qquad (B_0 = 1)$$

$B_n = 1$ for Z_n unshorted

$B_n = 0$ for Z_n shorted

$B_3B_2B_1$ = Binary number with values from 0 to 7

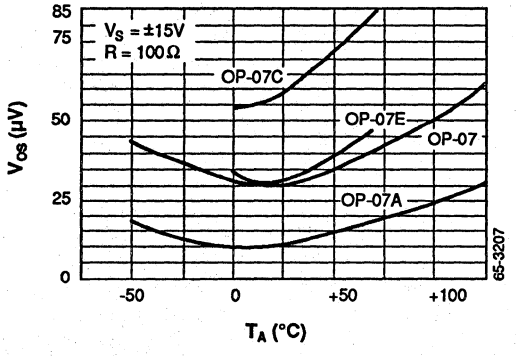
$$\Delta V_{OS}\ (25°C) \approx \frac{2.6\ mV\ (1 + B_3B_2B_1)\ R1}{R2 + R3} \qquad (B_0 = 0)$$

65-0365

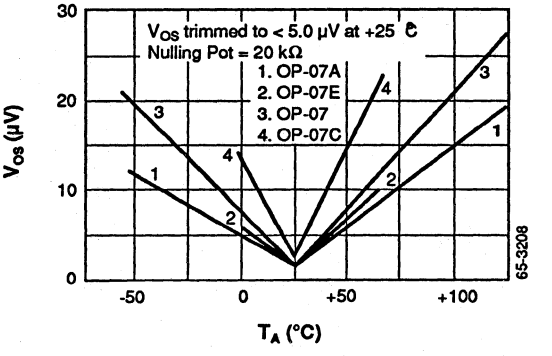
Figure 1. Digital Nulling Network

Typical Performance Characteristics

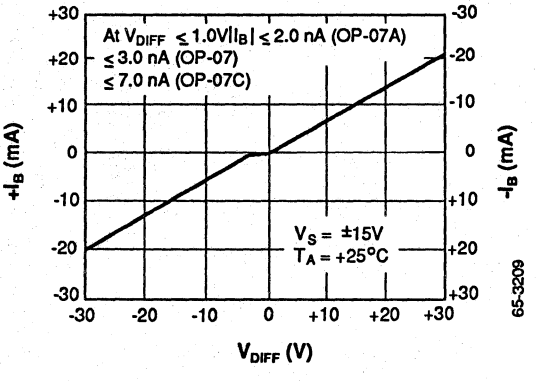
Untrimmed Offset Voltage vs. Temperature



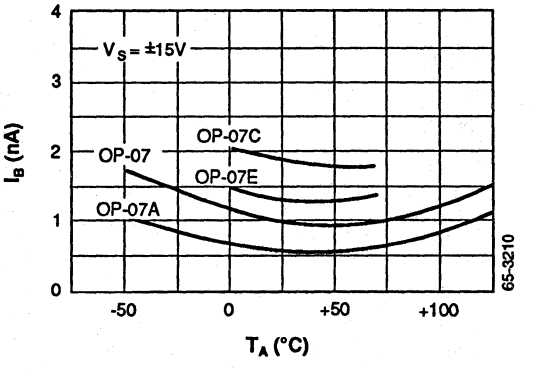
Trimmed Offset Voltage vs. Temperature



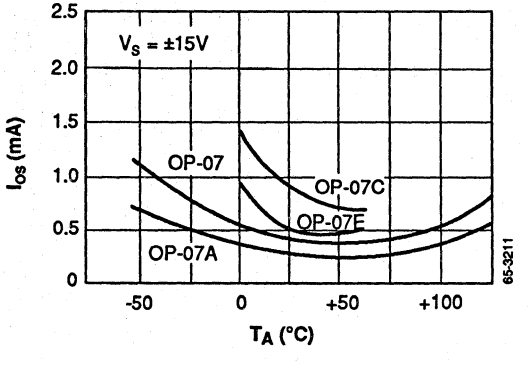
Input Bias Current vs. Differential Input Voltage



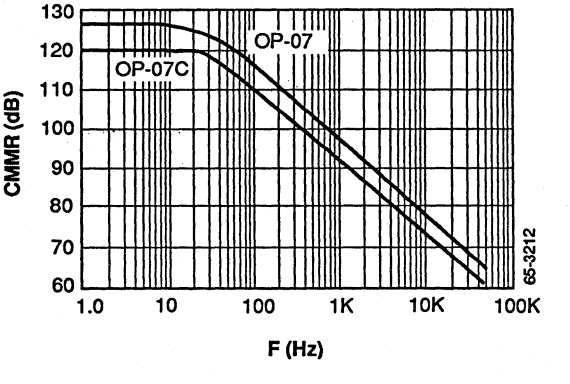
Input Bias Current vs. Temperature



Input Offset Current vs. Temperature

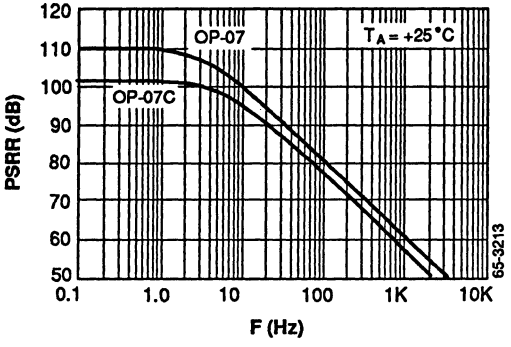


CMRR vs. Frequency

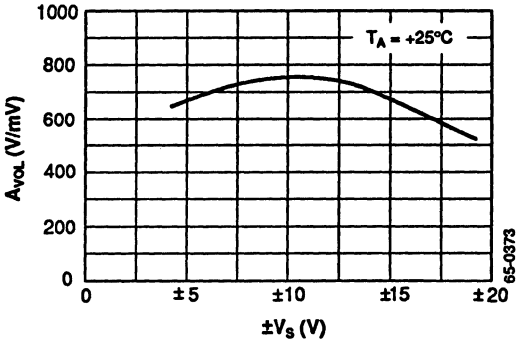


Typical Performance Characteristics

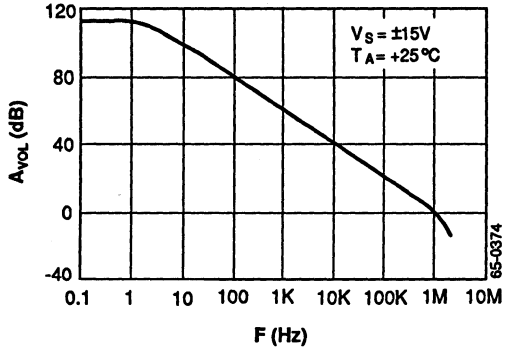
PSRR vs. Frequency



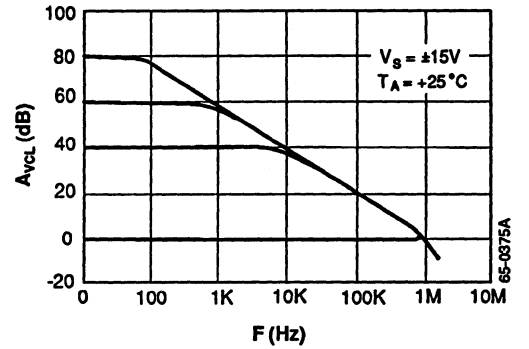
Open Loop Gain vs. Supply Voltage



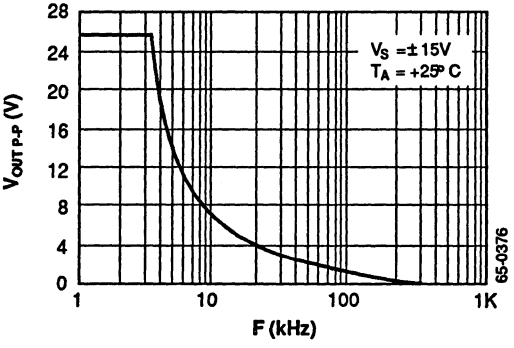
Open Loop Gain vs. Frequency



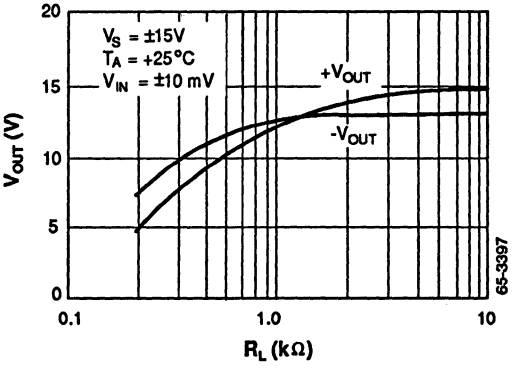
Closed Loop Response for Various Gain Configurations



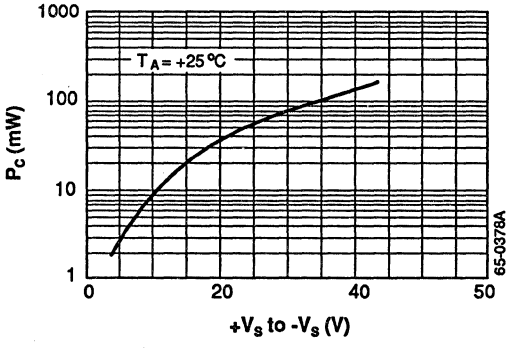
Maximum Undistorted Input vs. Frequency



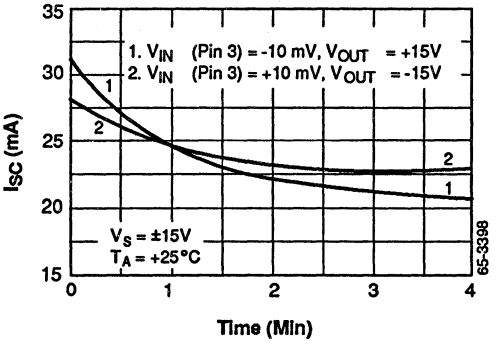
Output Voltage vs. Load Resistance to Ground



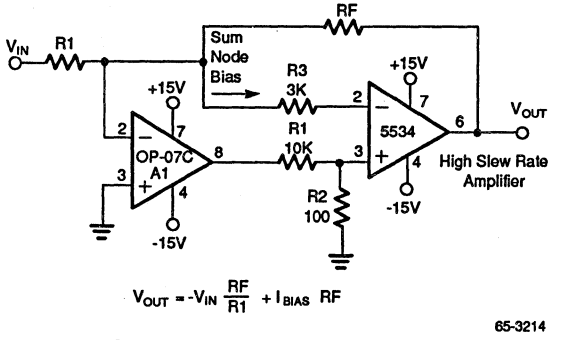
Typical Performance Characteristics



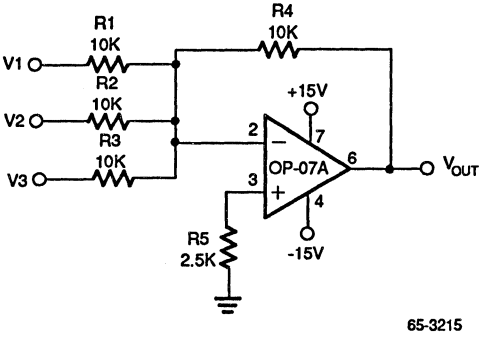
Output Short Circuit Current vs. Time



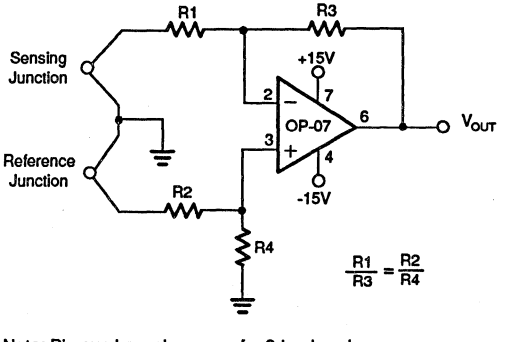
Typical Applications



High Speed, Low V_{OS} Composite Amplifier



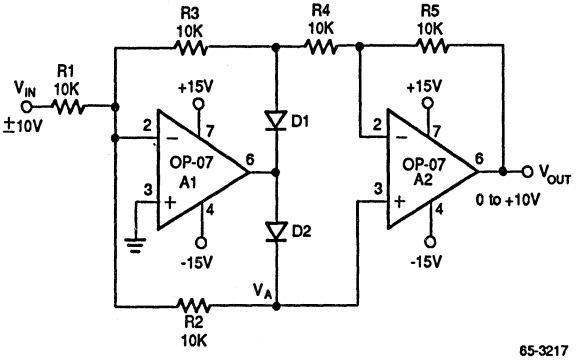
Adjustment-Free Precision Summing Amplifier



Note: Pin numbers shown are for 8-lead packages.

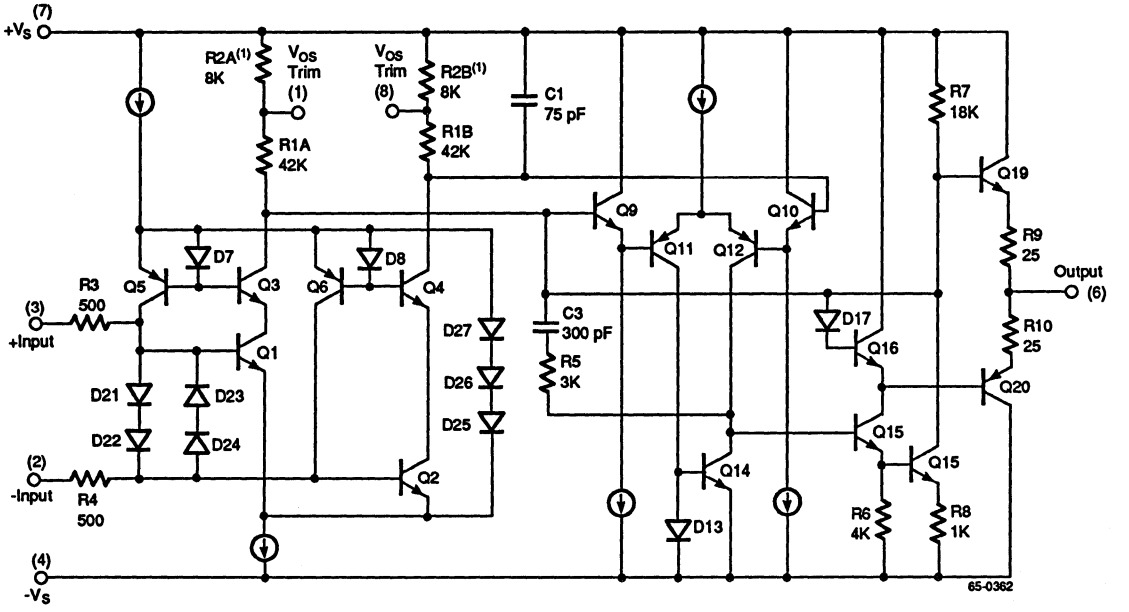
65-3216

High Stability Thermocouple Amplifier



Precision Absolute Value Circuit

Schematic Diagram



Notes:

1. R2A and R2B are electronically adjusted during factory test for minium V_{OS}.
2. Pin numbers shown are for 8-lead packages.

OP-27
Low Noise Operational Amplifier

Description

The OP-27 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70°) in a unity gain configuration.

Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 25 μV. Input bias current cancellation techniques are used to obtain 10 nA input bias currents.

The OP-27 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 120 dB. A phase margin of 70° at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000 pF*. Input offset voltage can be externally trimmed without affecting input offset voltage drift with temperature or time. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metal at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The OP-27 is available in SO-8 (small-outline), TO-99 can, plastic mini-DIP and ceramic mini-DIP packages, and can be ordered with Mil-Std-883 Level B processing.

*By decoupling the load capacitance with a series resistor of 50Ω or more, load capacitances larger than 2000 pF can be accommodated.

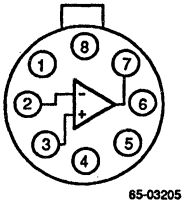
Features

- Very low noise
  Spectral noise density — 3.0 nV/√Hz
  1/F noise corner frequency — 2.7 Hz
- Very low V_{os} drift
  0.2 μV/Mo
  0.2 μV/°C
- High gain — 1800 V/mV
- High output drive capability — ±12V into 600Ω load
- High slew rate —2.8 V/μS
- Wide gain bandwidth product — 8 MHz
- Good CMRR — 126 dB
- Low V_{os} — 10 μV
- Low noise — 0.08 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input bias current — ±10 nA

OP-27

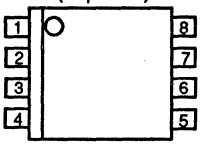
Connection Information

8-Lead
TO-99 Metal Can
(Top View)



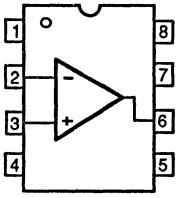
65-03205

8-Lead Plastic
Dual In-Line SO-8
(Top View)



65-02666

8-Lead
Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
OP-27EN	N	0°C to +70°C
OP-27FN	N	0°C to +70°C
OP-27GN	N	0°C to +70°C
OP-27EM	M	0°C to +70°C
OP-27FM	M	0°C to +70°C
OP-27GM	M	0°C to +70°C
OP-27AD	D	-55°C to +125°C
OP-27AD/883	D	-55°C to +125°C
OP-27BD	D	-55°C to +125°C
OP-27BD/883	D	-55°C to +125°C
OP-27CD	D	-55°C to +125°C
OP-27CD/883	D	-55°C to +125°C
OP-27AT	T	-55°C to +125°C
OP-27AT/883	T	-55°C to +125°C
OP-27BT	T	-55°C to +125°C
OP-27BT/883	T	-55°C to +125°C
OP-27CT	T	-55°C to +125°C
OP-27CT/883	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 0.7V
Internal Power Dissipation[2] ..... 658 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-27A/B/C ..... -55°C to +125°C
OP-27E/F/G ..... 0°C to +70°C

Lead Soldering Temperature
(SO-8, 10 sec) ..... +260°C
(DIP,TO-99; 60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Small Outline	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic DIP
Max. Junction Temp.	+125°C	+175°C	+175°C	+125°C
Max. P_D T_A <50°C	300 mW	833 mW	658 mW	468 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W	—
Therm. Res. θ_{JA}	240°C/W	150°C/W	190°C/W	160°C/W
For T_A >50°C Derate at	4.17 mW/°C	8.33 mW/°C	5.26 mW/°C	6.25 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-27A/E			OP-27B/F			OP-27C/G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[5]			10	25		20	60		30	100	µV
Long Term Input Offset Voltage Stability[1, 4]			0.2	1.0		0.3	1.5		0.4	2.0	µV/Mo
Input Offset Current			7.0	35		9.0	50		12	75	nA
Input Bias Current			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.08	0.18		0.08	0.18		0.09	0.25	μV_{p-p}
	F_O = 10 Hz		3.5	5.5		3.5	5.5		3.8	8.0	
Input Noise Voltage	F_O = 30 Hz		3.1	4.5		3.1	4.5		3.3	5.6	nV
Density[2]	F_O = 1000 Hz		3.0	3.8		3.0	3.8		3.2	4.5	$\sqrt{Hz}$
	F_O = 10 Hz		1.7	4.0		1.7	4.0		1.7		
Input Noise Current	F_O = 30 Hz		1.0	2.3		1.0	2.3		1.0		pA
Density[2]	F_O = 1000 Hz		0.4	0.6		0.4	0.6		0.4	0.6	$\sqrt{Hz}$
Input Resistance (Diff. Mode)[4]		1.5	6.0		1.2	5.0		0.8	4.0		MΩ
Input Resistance (Com. Mode)			3.0			2.5			2.0		GΩ
Input Voltage Range[3]		±11	±12.3		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	V_S ±4V to ±18V	100	120		100	120		94	118		dB
	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	1000	1800		1000	1800		700	1500		
Large Signal Voltage Gain	$R_L \geq 1$ kΩ, V_{OUT} = ±10V	800	1500		800	1500			1500		V/mV
	V_{OUT} = ±1V, V_S = ±4V	250	700		250	700		200	500		
	$R_L \geq 2$ kΩ,	±12	±13.8		±12	±13.8		±11.5	±13.5		
Output Voltage Swing	$R_L \geq 600$Ω,	±11	±12		±11	±12		±11	±12		V
Slew Rate[4]	$R_L \geq 2$ kΩ,	1.7	2.8		1.7	2.8		1.7	2.8		V/µS
Gain Bandwidth Product[4]		5.0	8.0		5.0	8.0		5.0	8.0		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		70			70			70		Ω
Power Consumption			90	140		90	140	100	170	mW	
Offset Adjustment Range	R_{TRIM} = 10 kΩ		±4.0			±4.0			±4.0		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. This parameter is tested on a sample basis only.
3. Caution: The Common Mode Input Range is a function of supply voltage. See Typical Performance Curves. Also, the input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
4. Parameter is guaranteed but not tested.
5. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-27A			OP-27B			OP-27C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	60		50	200		70	300	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			15	50		22	85		30	135	nA
Input Bias Current			±20	±60		±28	±95		±35	±150	nA
Input Voltage Range		±10.3	±11.5		±10.3	±11.5		±10.2	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	96	116		94	114		86	110		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	600	1200		500	1000		300	800		V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±11.5	±13.5		±11	±13.2		±10.5	±13		V

Electrical Characteristics

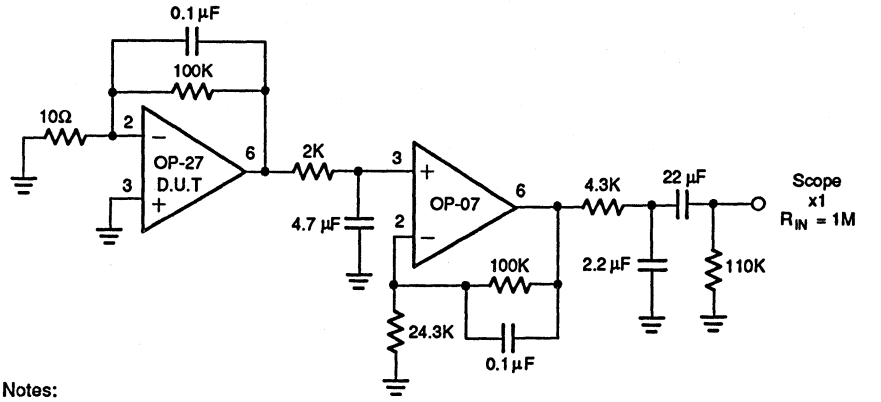
(V_S = ±15V, 0°C ≤ T_A ≤ +70°C for plastic package unless otherwise noted)

Parameters	Test Conditions	OP-27E			OP-27F			OP-27G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	50		40	140		55	220	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			10	50		14	85		20	135	nA
Input Bias Current			±14	±60		±18	±95		±25	±150	nA
Input Voltage Range		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		102	121		96	118		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	97	118		96	116		90	114		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±11.7	±13.6		±11.4	±13.5		±11	±13.3		V

Notes:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. $T_C V_{OS}$ performance is guaranteed untrimmed or when trimmed with R_{TRIM} = 8.0 kΩ to 20 kΩ.

Typical Performance Characteristics

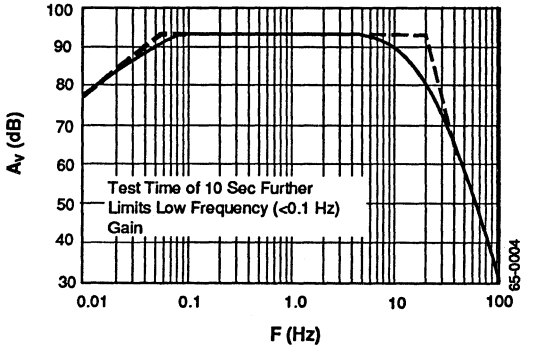


Notes:
1. Peak-to-peak noise measured in a 10-second interval.
2. The device under test should be warmed up for 3 minutes and shielded from air currents .
3. Voltage gain = 50,000.

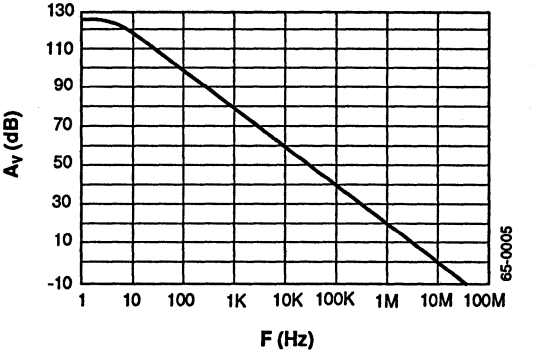
65-0003A

0.1 Hz to 10 Hz Noise Test Circuit

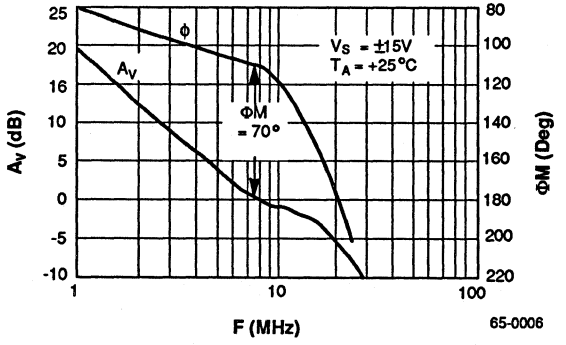
0.1 Hz to 10 Hz Noise Gain vs. Frequency



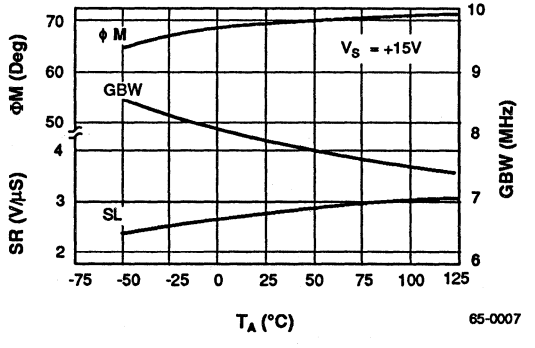
Open Loop Gain vs. Frequency



Gain, Phase Shift vs. Frequency

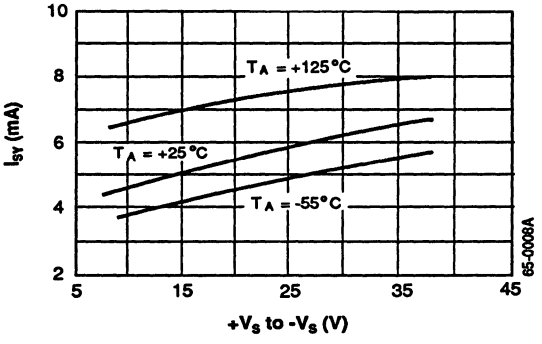


Slew Rate, Gain Bandwidth Product, Phase Margin vs. Temperature

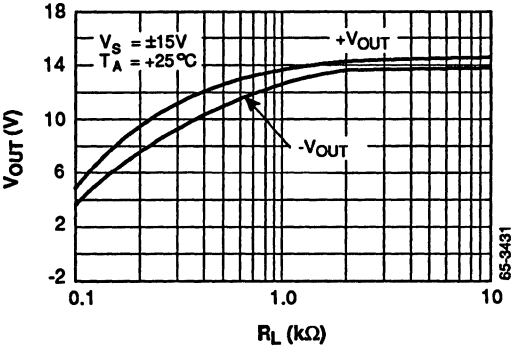


Typical Performance Characteristics (Continued)

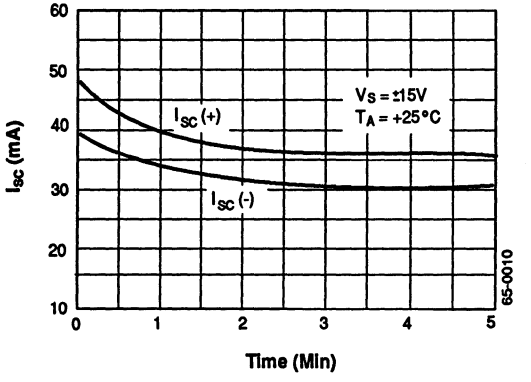
Supply Current vs. Total Supply Voltage



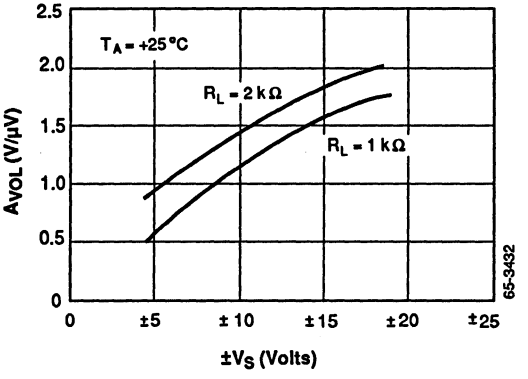
Maximum Output Swing vs. Load Resistance



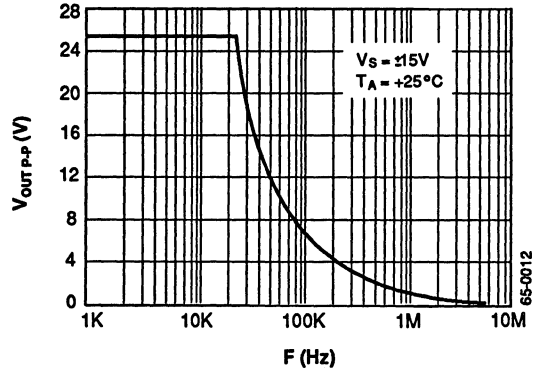
Short Circuit Current vs. Time



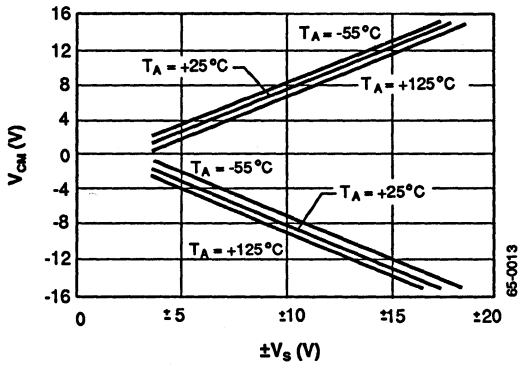
Open Loop Gain vs. Supply Voltage



Gain, Phase Shift vs. Frequency



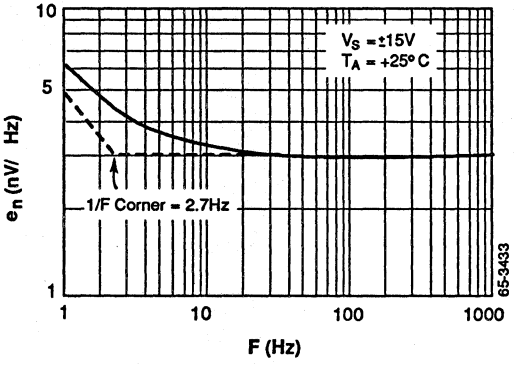
Common Mode Input Range vs. Supply Voltage



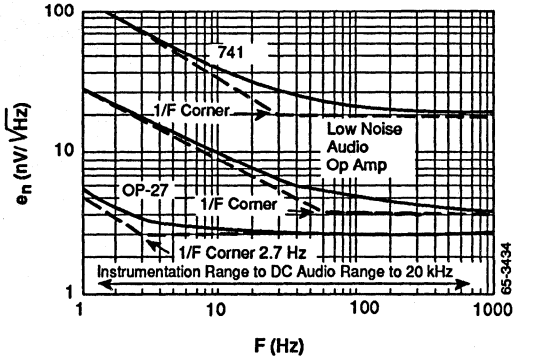
Linear

Typical Performance Characteristics (Continued)

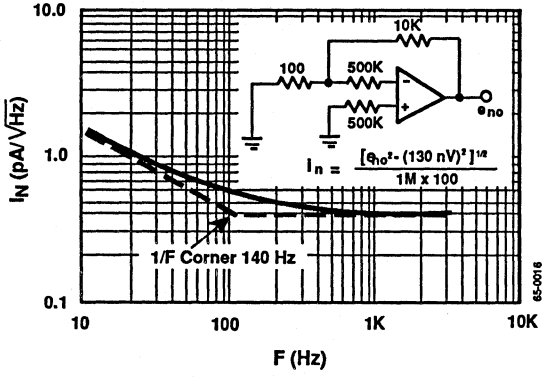
Input Noise Voltage Density vs. Frequency



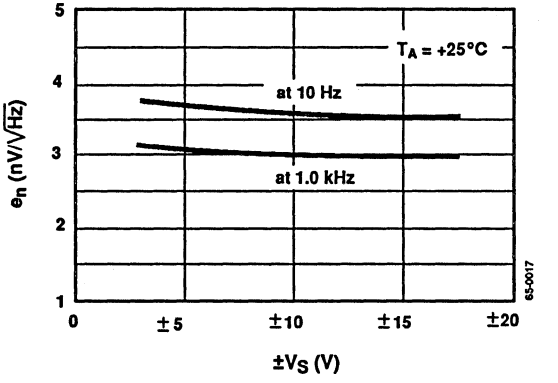
Op Amp Comparison
Input Noise Voltage Density vs. Frequency



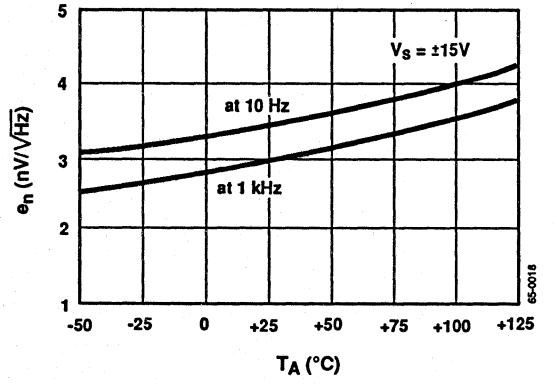
Input Noise Current Density vs. Frequency



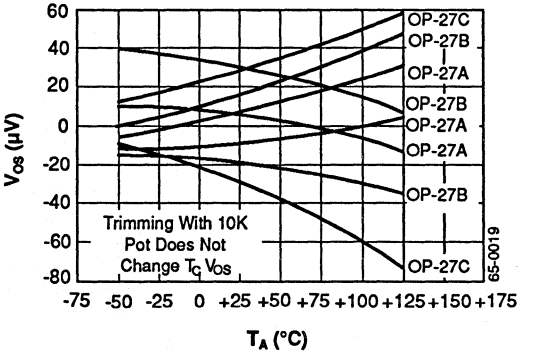
Input Noise Voltage Density vs. Supply Voltage



Input Noise Voltage Density vs. Temperature

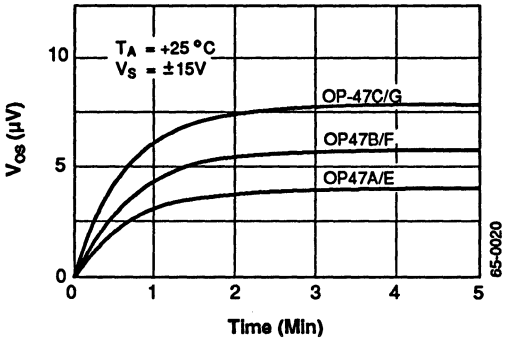


Input Offset Voltage Drift of Representative Units

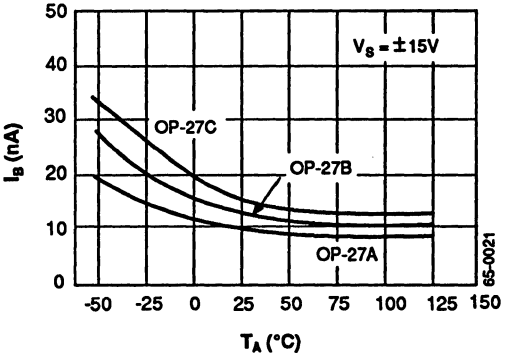


Typical Performance Characteristics (Continued)

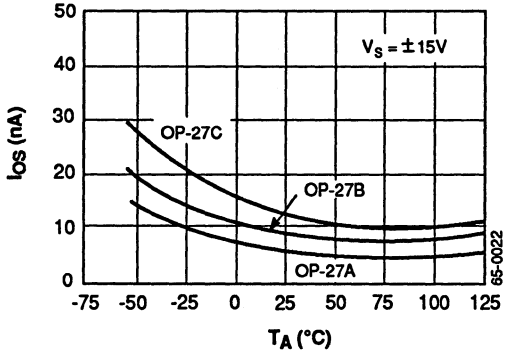
Input Offset Voltage vs. Time
(Warm-Up Drift)



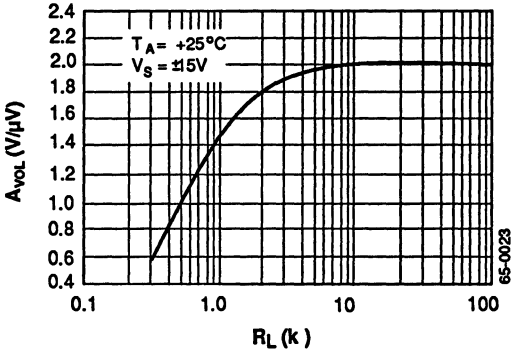
Input Bias Current vs. Temperature



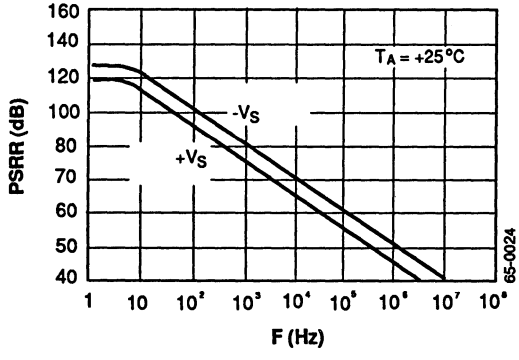
Input Offset Current vs. Temperature



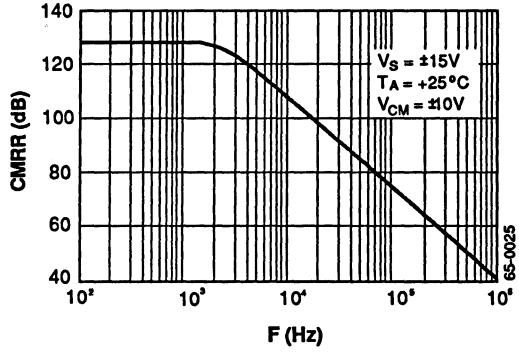
Open Loop Gain vs. Load Resistance



PSRR vs. Frequency



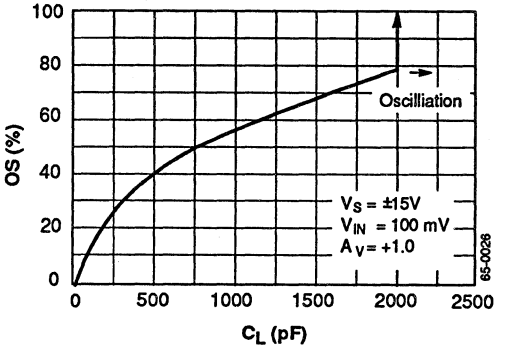
CMRR vs. Frequency



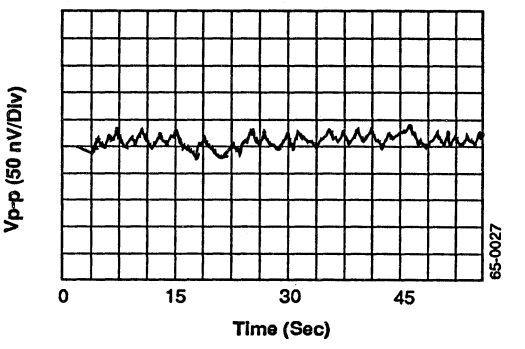
Linear

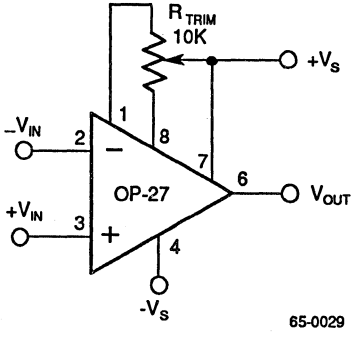
Typical Performance Characteristics (Continued)

Small Signal Overshoot vs. Capacitive Load

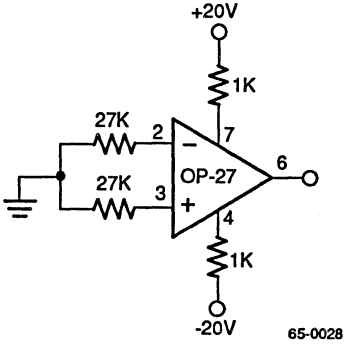


0.1 Hz to 10 Hz Peak-to-Peak Noise vs. Time

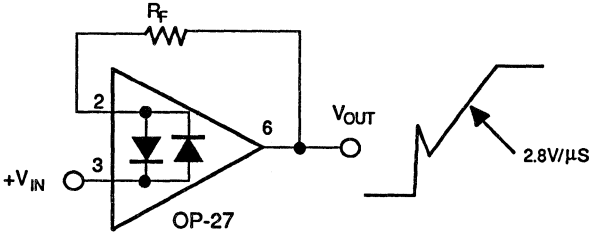




Input Offset Trimming Circuit



Burn-In Circuit



When $R_F \leq 100\Omega$ and the input is driven with a fast, large signal pulse ($\geq 1.0V$), the output waveform will appear as shown.

Note: Pin numbers shown are for 8-lead packages.

65-0030

Large Signal Transient Response

Typical Applications

RIAA Phono Preamplifier (Figure 1)

The new moving coil magnetic phono cartridges have sensitivities that are an order of magnitude lower than the sensitivity of a typical moving magnet cartridge (0.1 mV per CM/S versus 1.0 mV per CM/S). This places a greater burden on the preamplifier to achieve more gain and less noise. The OP-27 is ideally suited for this task. The object in designing an RIAA phono preamp is to achieve the RIAA gain-frequency response curve while contributing as little noise as possible to avoid masking the very small signal generated by the cartridge. The circuit shown is adjusted to match a 40 dB RIAA curve as shown in Figure 2. Note that by convention the RIAA gain is specified at 1 kHz. With the "break points" of the curves specified at 50,500 and 2.1 kHz, respectively, the entire curve is fixed by the specified gain at 1kHz.

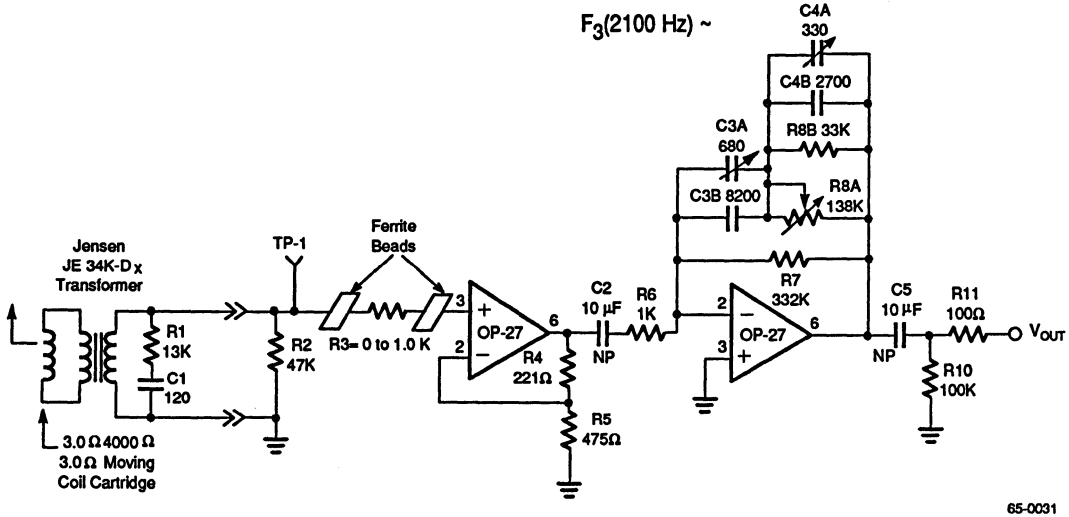
The circuit is designed to operate with a 3/4000Ω step-up transformer to present the optimum source impedance to the amplifier for best noise figure. The optimum source impedance is obtained as the ratio of the spectral noise voltage en to the spectral noise current I_N (when e_n has dimensions of nV/√Hz and I_N has dimensions of pA/√Hz and the ratio has dimensions of kΩ). The circuit is designed to be tested and adjusted independent of the transformer. For testing, introduce a very low level signal of 1 mV at test point TP-1. The first stage is a wideband stage which provides a small amount of gain (1 + R4/R5) approximately equal to 10 dB. Low value feedback resistors must be used to prevent additional noise due to the spectral current noise or excessive Johnson noise. The gain of the first stage reduces the noise contribution of the second stage. The RIAA transfer curve poles and zeros are due entirely to the feedback network of the second stage.

The poles and zeros of the RIAA feedback network are sufficiently separated in frequency that they may be estimated with the following equations:

$$F_1(50\ Hz) \sim \frac{1}{2\pi R7C3}$$

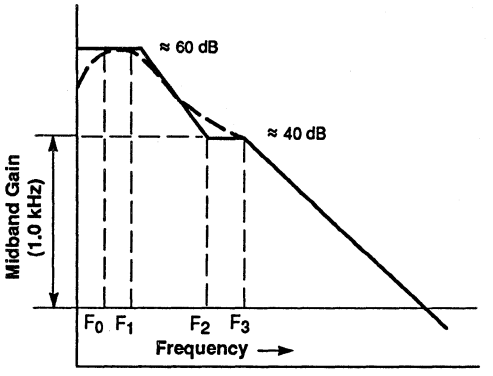
$$F_2(500\ Hz) \sim \frac{1}{2\pi R8C3}$$

$$F_3(2100\ Hz) \sim \frac{1}{2\pi R8C2}$$



Notes:
1. To test, disconnect transformer and inject signal at TP-1.
2. Pin numbers shown are for 8-lead packages.

Figure 1. RIAA Phono Preamplifier



F_0 = Low end rolloff frequency (user selected)
F_1 = 50 Hz
F_2 = 500 Hz
F_3 = 2.1 kHz

65-0032

Figure 2. RIAA Phono Playback Equalication Curve

These equations are only approximations. Final tuning is performed with the adjustable capacitors and potentiometers. The following sequence can be used to adjust for the RIAA response after injecting a low level signal into TP-1 (transformer disconnected).

1. At 100 Hz adjust C3A for an output level 6 dB lower than the low frequency output.
2. At 1000 Hz adjust R8A for an output level 20 dB lower than the low frequency output.
3. At 21 kHz adjust C4A for an output 40 dB less than the low frequency output.

Low Impedance Microphone Preamp (Figure 3)

In this preamp the transformer converts the low microphone impedance up to a value that is close to the optimum source impedance required by the OP-27 for best noise performance. The optimum source impedance can be calculated as the ratio of e_n/I_N, which for the OP-27 is approximately 7000Ω. Fortunately the noise performance does not degrade appreciably until the source impedance is four or five times this optimum value and the source impedance at the output of this transformer, approximately 15 kΩ, still provides near optimum noise performance. (A high quality audio transformer with a step-up ratio of 6.7 to one is not available.) The voltage gain of the amplifier, not including the transformer step-up, is unity up to about 1.5 Hz. It may be desirable to reduce the size of this capacitor to minimize burst noise even though the OP-27 has a 1/F noise corner below 3 Hz. C2 rolls off the high frequency response at 90 kHz giving a noise power bandwidth of 140 kHz.

Instrumentation

The OP-27 is particularly adaptable to instrumentation applications. When wired into a single op amp difference amplifier configuration, the OP-27 exhibits outstanding common mode rejection ratio. The spot voltage noise is so low that it is dominated almost entirely by the resistor Johnson noise. (Figures 4 through 7).

The three op amp instrumentation amplifier of Figure 8 avoids the low input impedance characteristics of difference amplifiers at the expense of two more operational amplifiers and a slight degradation in noise performance. The noise increases because two amplifiers are contributing to the input voltage spectral noise instead of one. Thus the noise contribution, exclusive of resistor Johnson noise, increases by slightly more than $\sqrt{2}$. The spectral noise voltage increases from approximately 3 nV/$\sqrt{Hz}$ to approximately 4.9 nV/$\sqrt{Hz}$, with the third amplifier contributing about 10% of the noise. The gain of the input amplifier is set at 25 and the second stage at 40 for an overall gain of 1000. R7 is trimmed to optimize the common mode rejection ratio (CMRR) with frequency. With balanced source resistors a CMRR of 100 dB is achieved. With a 1 kΩ source impedance imbalance CMRR is degraded to 80 dB at 5 kHz due to the finite (3 GΩ) input impedance.

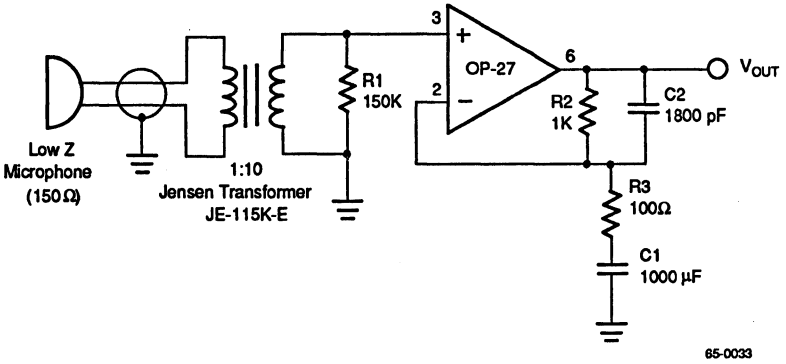
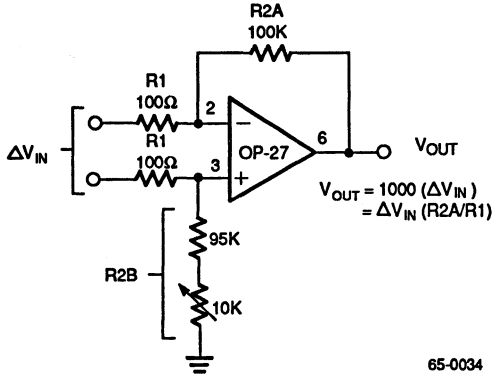


Figure 3. Low Impedance Microphone Preamplifier



Note:
Pin numbers shown are for 8-lead packages.

Figure 4. Difference Amplifier

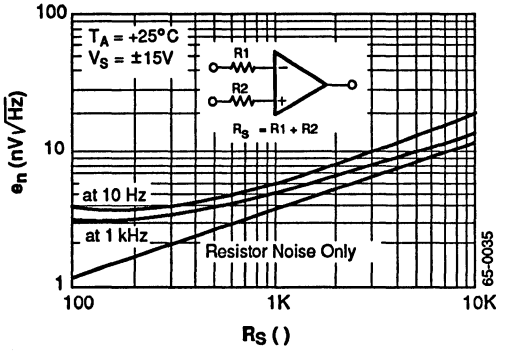


Figure 5. Difference Amplifier
Input Voltage Noise Density vs. Source Resistance

Linear

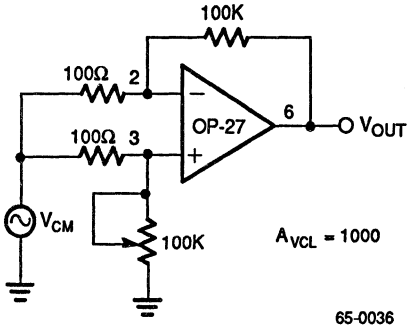


Figure 6. CMRR Test Circuit

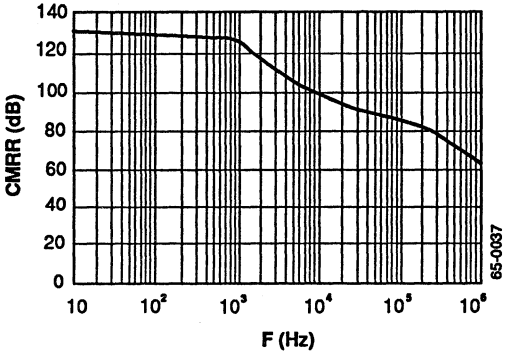
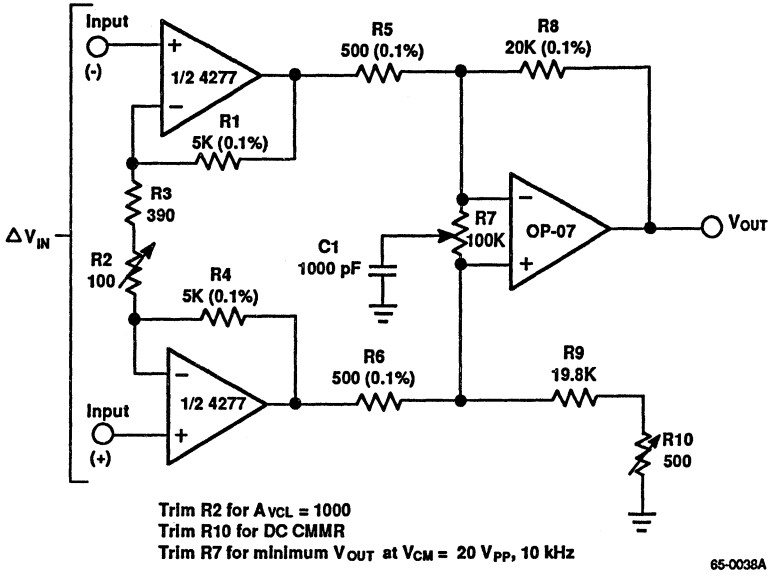


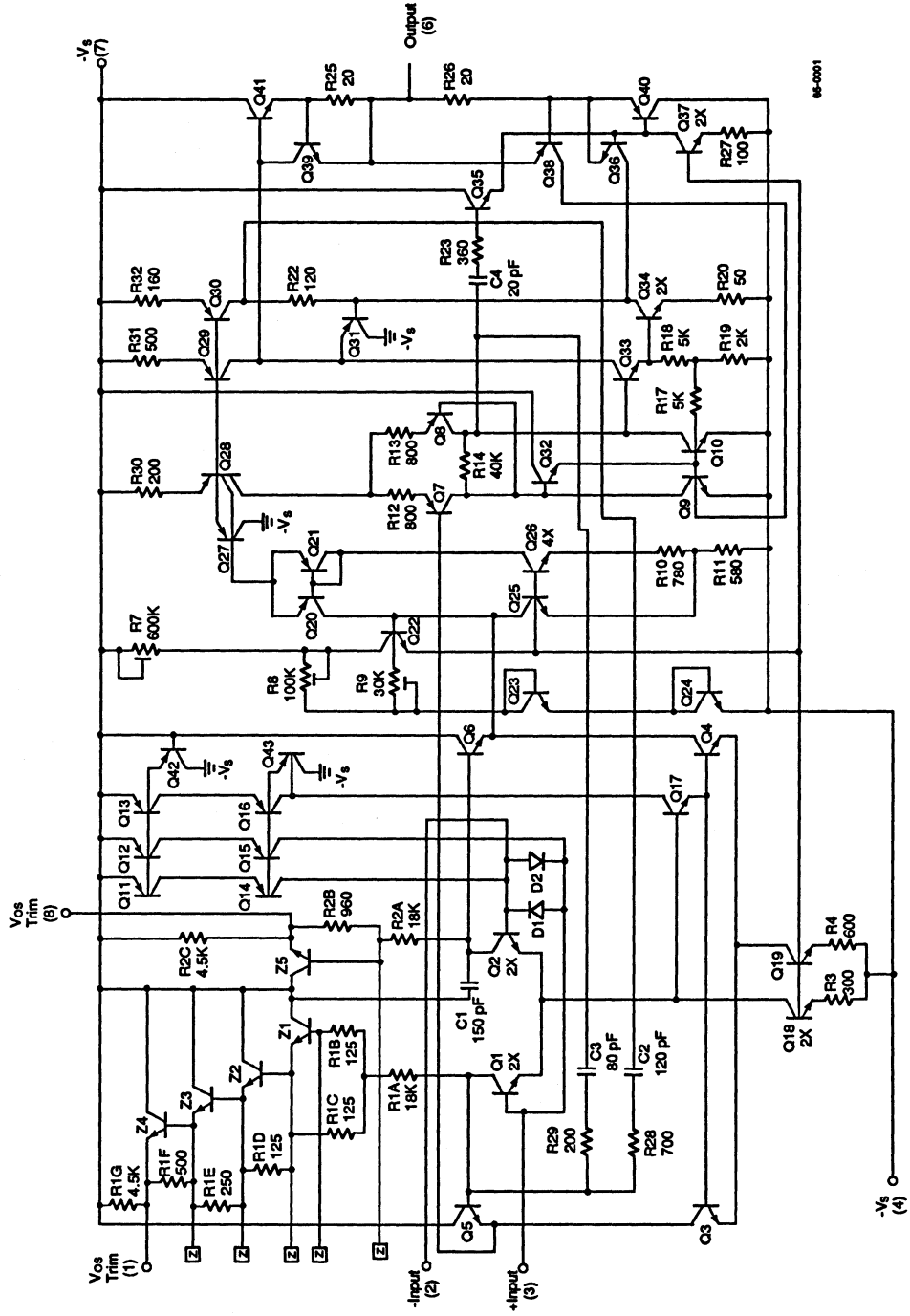
Figure 7. Difference Amplifier CMRR vs. Frequency



Note: Pin numbers shown are for 8-lead packages.

Figure 8. Three Op Amp Instrumentation Amplifier

Schematic Diagram



OP-37
Low Noise Operational Amplifier

Description

The OP-37 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. The OP-37 is a decompensated version of the OP-27 and is AC stable in gain configurations equal to five and higher.

Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 25 μV. Input bias current cancellation techniques are used to obtain 10 nA input bias currents.

The OP-37 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 120 dB. Input offset voltage can be externally trimmed without affecting input offset voltage drift with temperature or time. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metal at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The OP-37 is available in, SO-8 (small-outline), TO-99 can, plastic mini-DIP and ceramic mini-DIP packages, and can be ordered with Mil-Std-883 Level B processing.

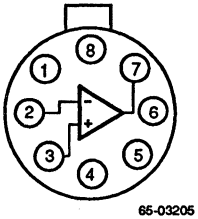
Features

- Very low noise
  Spectral noise density — 3.0 nV/√Hz
  1/F noise corner frequency — 2.7 Hz
- Very low V_{OS} drift
  0.2 μV/Mo
  0.2 μV/°C
- High gain — 1800 V/mV
- High output drive capability — ±12V into 600Ω load
- High slew rate —17 V/μS
- High gain bandwidth product — 63 MHz
- Good CMRR — 126 dB
- Low V_{OS} — 10 μV
- Low noise — 0.08 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input bias current — ±10 nA
- Compensated for AC stability with $A_{VCL} \geq 5$

OP-37

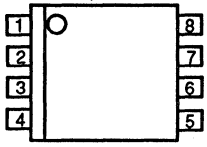
Connection Information

8-Lead TO-99 Metal Can
(Top View)



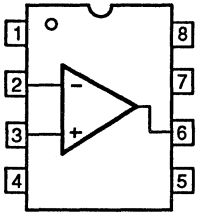
65-03205

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02668

8-Lead Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
OP-37EN	N	0°C to +70°C
OP-37FN	N	0°C to +70°C
OP-37GN	N	0°C to +70°C
OP-37EM	M	0°C to +70°C
OP-37FM	M	0°C to +70°C
OP-37GM	M	0°C to +70°C
OP-37AD	D	-55°C to +125°C
OP-37AD/883	D	-55°C to +125°C
OP-37BD	D	-55°C to +125°C
OP-37BD/883	D	-55°C to +125°C
OP-37CD	D	-55°C to +125°C
OP-37CD/883	D	-55°C to +125°C
OP-37AT	T	-55°C to +125°C
OP-37AT/883	T	-55°C to +125°C
OP-37BT	T	-55°C to +125°C
OP-37BT/883	T	-55°C to +125°C
OP-37CT	T	-55°C to +125°C
OP-37CT/883	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 0.7V
Internal Power Dissipation[2] ..... 658 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-27A/B/C ..... -55°C to +125°C
OP-27E/F/G ..... -25°C to +85°C
OP-27E/F/G ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8, 10 sec) ..... +260°C
(DIP, TO-99; 60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Small Outline	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic DIP
Max. Junction Temp.	+125°C	+175°C	+175°C	+125°C
Max. P_D T_A <50°C	300 mW	833 mW	658 mW	468 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W	—
Therm. Res. θ_{JA}	240°C/W	150°C/W	190°C/W	160°C/W
For T_A >50°C Derate at	4.17 mW/°C	8.33 mW/°C	5.26 mW/°C	6.25 mW/°C

OP-37

Electrical Characteristics
(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-37A/E			OP-37B/F			OP-37C/G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[5]			10	25		20	60		30	100	µV
Long Term Input Offset Voltage Stability[1, 2]			0.2	1.0		0.3	1.5		0.4	2.0	µV/Mo
Input Offset Current			7.0	35		9.0	50		12	75	nA
Input Bias Current			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.08	0.18		0.08	0.18		0.09	0.25	μV_{p-p}
Input Noise Voltage Density[2]	F_O = 10 Hz		3.5	5.5		3.5	5.5		3.8	8.0	$\frac{nV}{\sqrt{Hz}}$
	F_O = 30 Hz		3.1	4.5		3.1	4.5		3.3	5.6	
	F_O = 1000 Hz		3.0	3.8		3.0	3.8		3.2	4.5	
Input Noise Current Density[2]	F_O = 10 Hz		1.7	4.0		1.7	4.0		1.7		$\frac{pA}{\sqrt{Hz}}$
	F_O = 30 Hz		1.0	2.3		1.0	2.3		1.0		
	F_O = 1000 Hz		0.4	0.6		0.4	0.6		0.4	0.6	
Input Resistance (Diff. Mode)[4]		1.5	6.0		1.2	5.0		0.8	4.0		MΩ
Input Resistance (Com. Mode)			3.0			2.5			2.0		GΩ
Input Voltage Range[3]		±11	±12.3		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4V to ±18V	100	120		100	120		94	118		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, $V_{O\ UT}$ = ±10V	1000	1800		1000	1800		700	1500		V/mV
	R_L ≥ 1 kΩ, V_{OUT} = ±10V	800	1500		800	1500			1500		
	V_{OUT} = ±1V, V_S = ±4V	250	700		250	700		200	500		
Output Voltage Swing	R_L ≥ 2 kΩ,	±12	±13.8		±12	±13.8		±11.5	±13.5		V
	R_L ≥600Ω,	±11	±12		±11	±12		±11	±12		
Slew Rate[4]	R_L ≥ 2 kΩ,	11	17		11	17		11	17		V/µS
Gain Bandwidth Product[4]	F_O = 10 kHz	45	63		45	63		45	63		MHz
	F_O = 1 MHz		40			40			40		
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		70			70			70		Ω
Power Consumption			90	140		90	140		100	170	mW
Offset Adjustment Range	R_{TRIM} = 10 kΩ		±4.0			±4.0		±4.0			mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. This parameter is tested on a sample basis only.
3. Caution: The Common Mode Input Range is a function of supply voltage. See Typical Performance Curves. Also, the input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
4. Parameter is guaranteed but not tested.
5. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-37A			OP-37B			OP-37C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	60		50	200		70	300	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			15	50		22	85		30	135	nA
Input Bias Current			±20	±60		±28	±95		±35	±150	nA
Input Voltage Range		±10.3	±11.5		±10.3	±11.5		±10.2	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	96	116		94	114		86	110		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	600	1200		500	1000		300	800		V/mV
Output Voltage Swing	R_L ≥2 kΩ	±11.5	±13.5		±11	±13.2		±10.5	±13		V

Electrical Characteristics

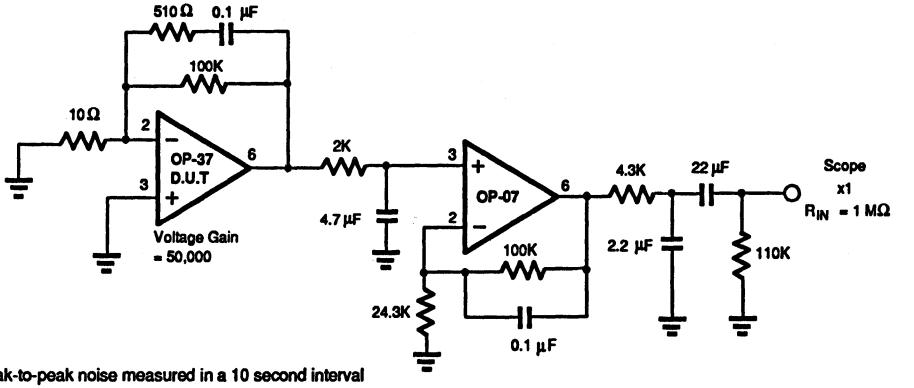
(V_S = ±15V,0°C ≤ T_A ≤ +70°C for plastic packages unless otherwise noted)

Parameters	Test Conditions	OP-37E			OP-37F			OP-37G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	50		40	140		55	220	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			10	50		14	85		20	135	nA
Input Bias Current			±14	±60		±18	±95		±25	±150	nA
Input Voltage Range		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		102	121		96	118		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	97	118		96	116		90	114		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	R_L ≥2 kΩ	±11.7	±13.6		±11.4	±13.5		±11	±13.3		V

Notes:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. $T_C V_{OS}$ performance is guaranteed untrimmed or when trimmed with R_{TRIM} = 8.0 kΩ to 20 kΩ.

Typical Performance Characteristics

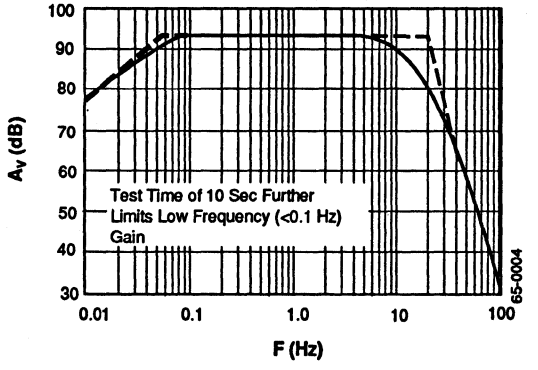


Note:
1. Peak-to-peak noise measured in a 10 second interval
2. The device under test should be warmed up for 3 minutes and shielded from air current.
3. Voltage gain = 50,000.
4. All capacitor values are for non-polarized capacitors only.
5. Pin numbers shown sare for 8-lead package.

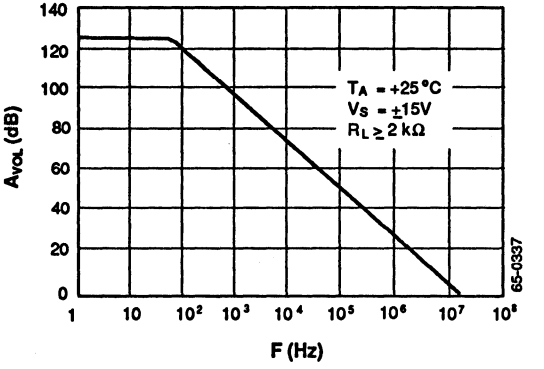
65-0336

0.1 Hz to 10 Hz Noise Test Circuit

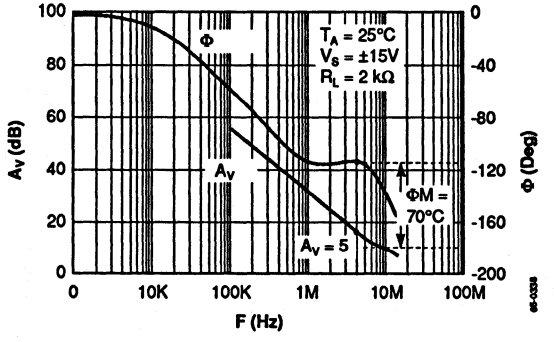
0.1 Hz to 10 Hz Noise Test Circuit
Gain vs. Frequency



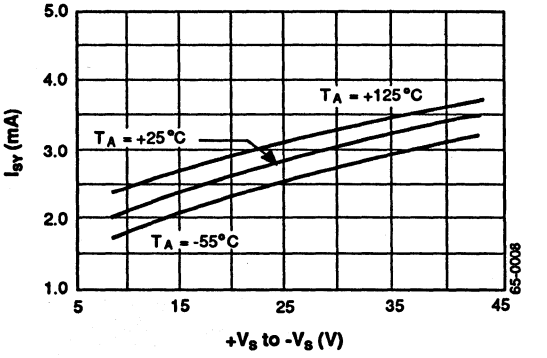
Open Loop Gain vs. Frequency



Gain, Phase Shift vs. Frequency

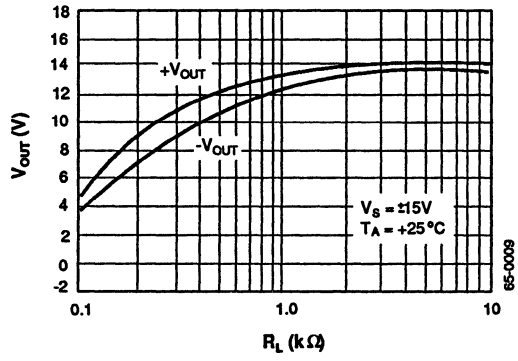


Supply Current vs. Total Supply Voltage

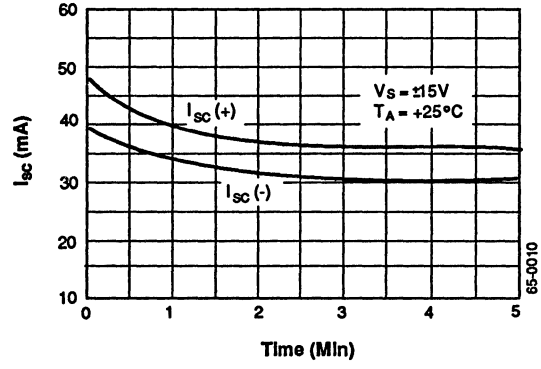


Typical Performance Characteristics (Continued)

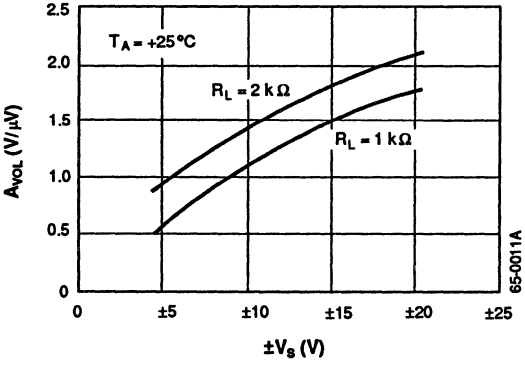
Maximum Output Swing vs. Load Resistance



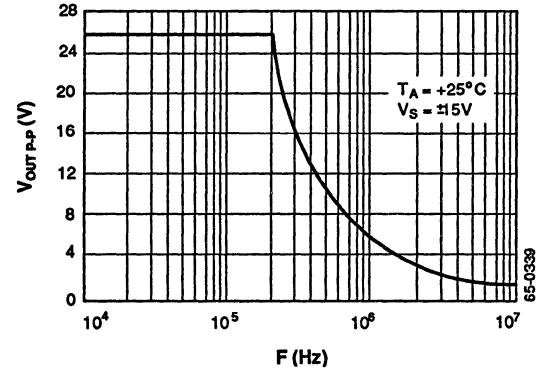
Short Circuit Current vs. Time



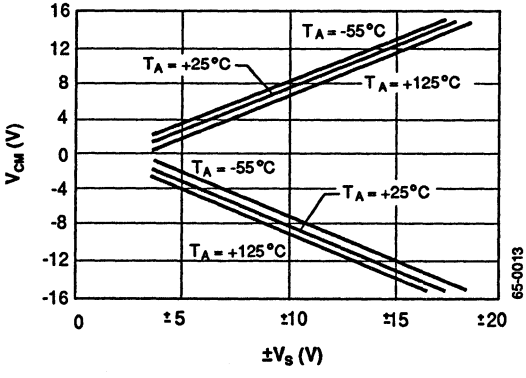
Open Loop Gain vs. Supply Voltage



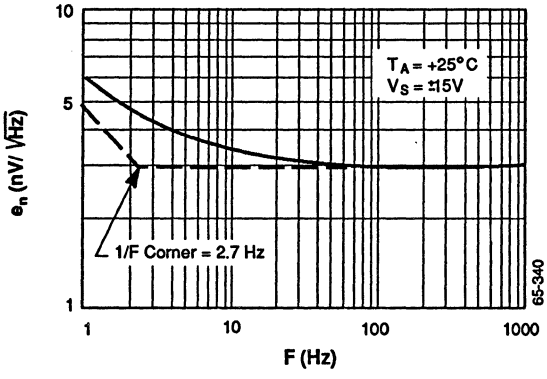
Maximum Undistorted Output vs. Frequency



Common Mode Input Range vs. Supply Voltage



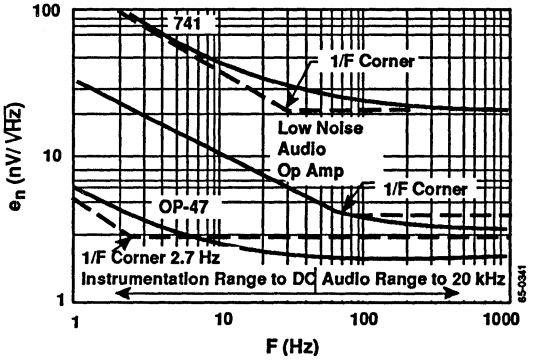
Input Noise Voltage Density vs. Frequency



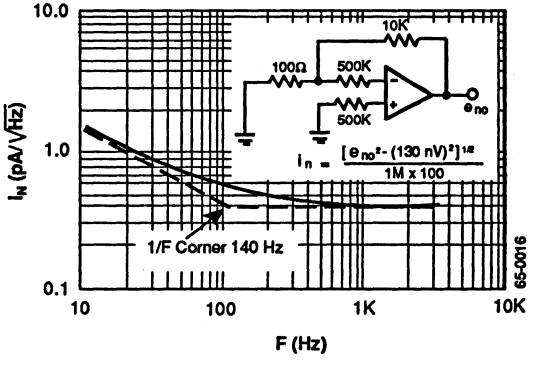
Linear

Typical Performance Characteristics (Continued)

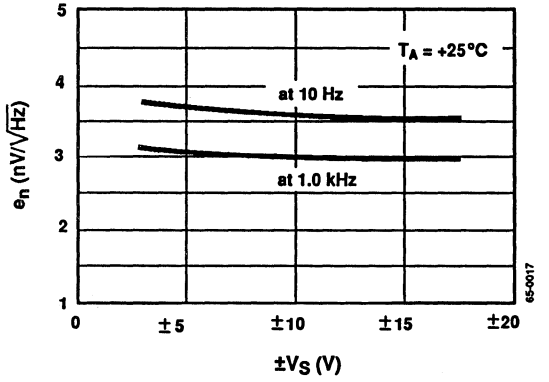
Op Amp Comparison
Input Noise Voltage Density vs. Frequency



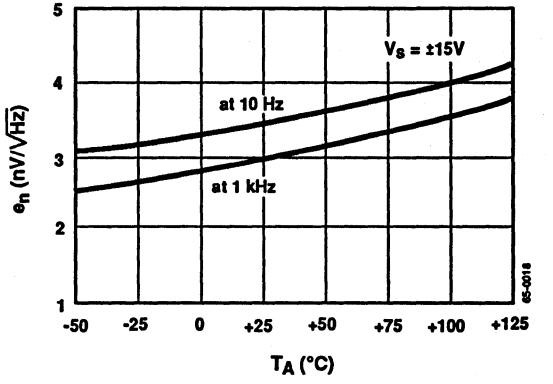
Input Noise Current Density vs. Frequency



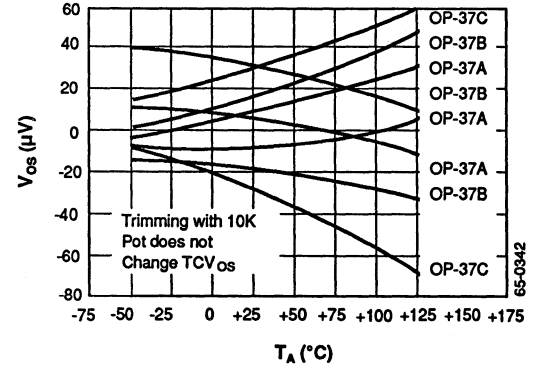
Input Noise Voltage Density vs. Total Supply Voltage



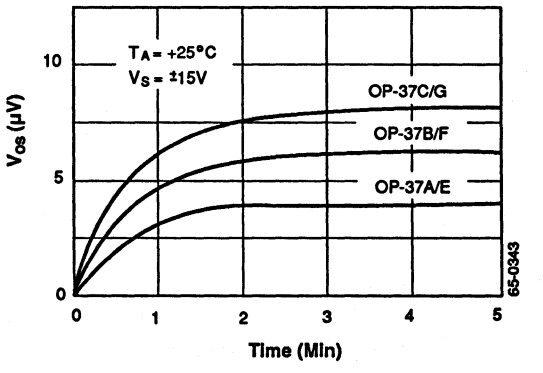
Input Noise Voltage Density vs. Temperature



Input Offset Voltage Drift of
Representative Units

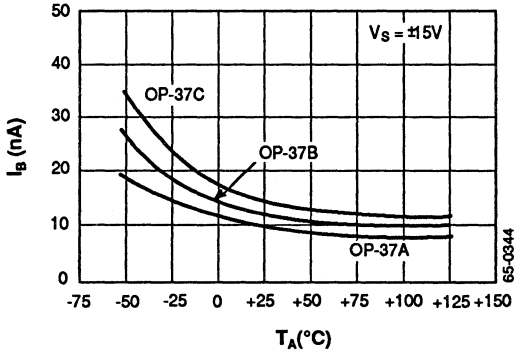


Input Offset Voltage vs. Time
(Warm-up Drift)

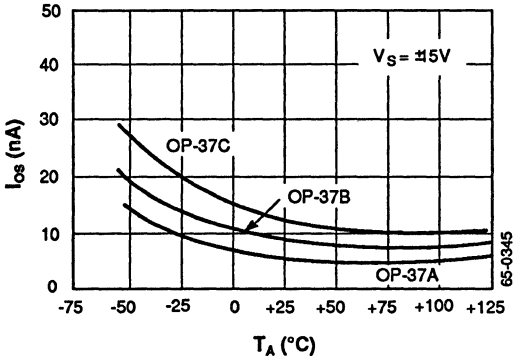


Typical Performance Characteristics (Continued)

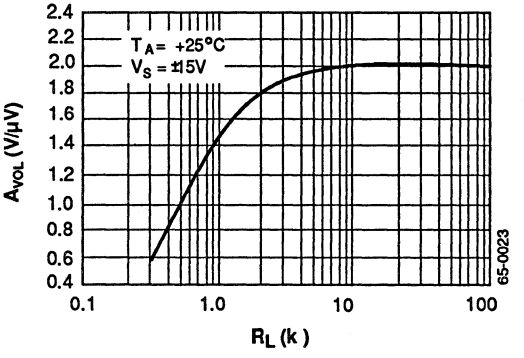
Input Bias Current vs. Temperature



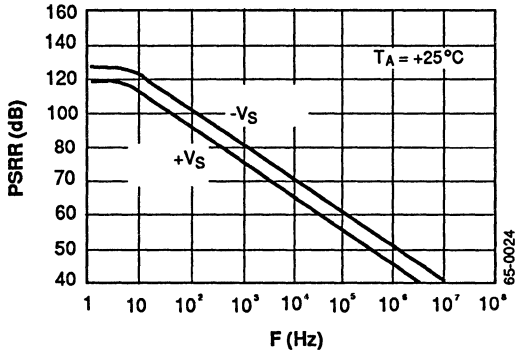
Input Offset Current vs. Temperature



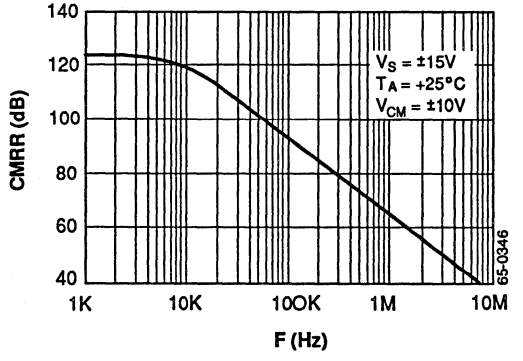
Open Loop Gain vs. Load Resistance



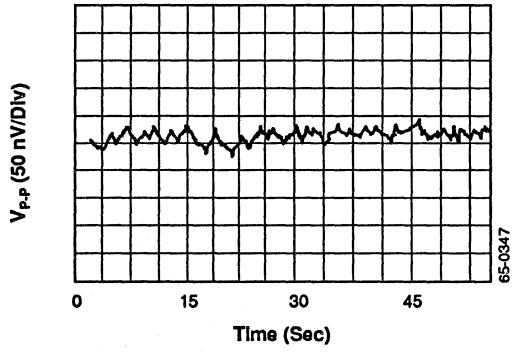
PSRR vs. Frequency



CMRR vs. Frequency



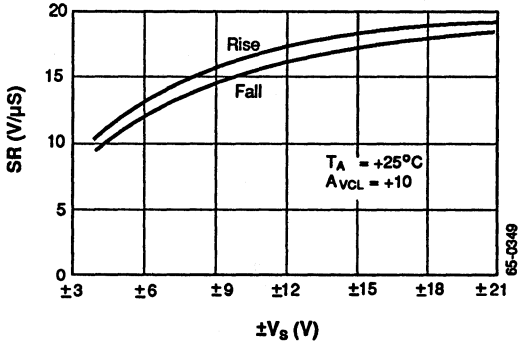
0.1 Hz to 10 Hz Peak-to-Peak Noise vs. Time



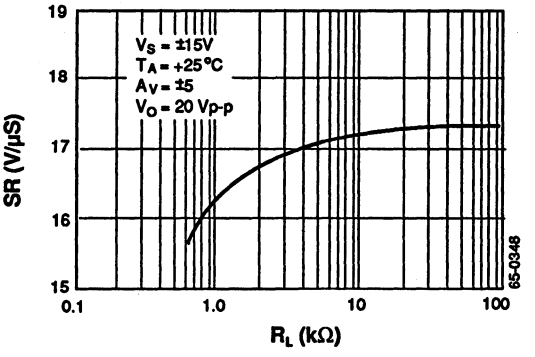
Linear

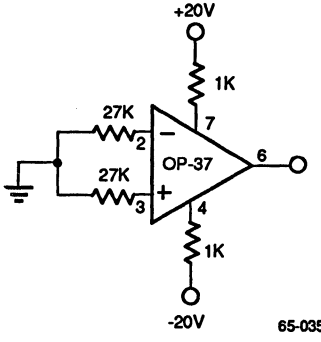
Typical Performance Characteristics (Continued)

Slew Rate vs. Supply Voltage



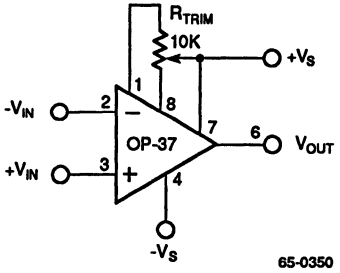
Slew Rate vs. Load Resistance





Note: Pin numbers shown are for 8-lead packages.

Burn-In Circuit



Input Offset Trimming Circuit

Typical Applications

Low Impedance Microphone Preamp (Figure 1)

In this preamp, the transformer converts the low microphone impedance up to a value that is close to the optimum source impedance required by the OP-37 for best noise performance. The optimum source impedance can be calculated as the ratio of e_n/I_N which for the OP-37 is approximately 7000Ω. Fortunately, the noise performance does not degrade appreciably until the source impedance is four or five times this optimum value. The source impedance at the output of this transformer of 15 kΩ still provides near optimum noise performance. (A high quality audio transformer with a step-up ratio of 6.7 to one is not available.) C1 rolls off the high frequency response at 90 kHz giving a noise power bandwidth of 140 kHz.

Instrumentation

The OP-37 is particularly adaptable to instrumentation applications. When wired into a single op amp difference amplifier configuration, the OP-37 exhibits outstanding common mode rejection ratio. The spot voltage noise is so low that is dominated almost entirely by the resistor Johnson noise (Figures 2 through 5).

The three op amp instrumentation amplifier of Figure 5 OP-37OP-37 avoids the input impedance characteristics of difference amplifiers at the expense of two more operational amplifiers and a slight degradation in noise performance. The noise increases because two amplifiers are contributing to the input voltage spectral noise instead of one. Thus, the noise contribution, exclusive of resistor Johnson noise, increases by slightly more than √2. The spectral noise voltage increases from approximately 3 nV/√Hz to approximately 4.9 nV/√Hz, with the third amplifier contributing about 10% of the noise. The gain of the input amplifier is set at 25 and the second stage at 40 for an overall gain of 1000. R7 is trimmed to optimize the common mode rejection ratio (CMRR) with frequency. With balanced source resistors, a CMRR of 100 dB is achieved. With a 1 kΩ source impedance imbalance CMRR is degraded to 80 dB at 5 kHz due to the finite (3 GΩ) input impedance.

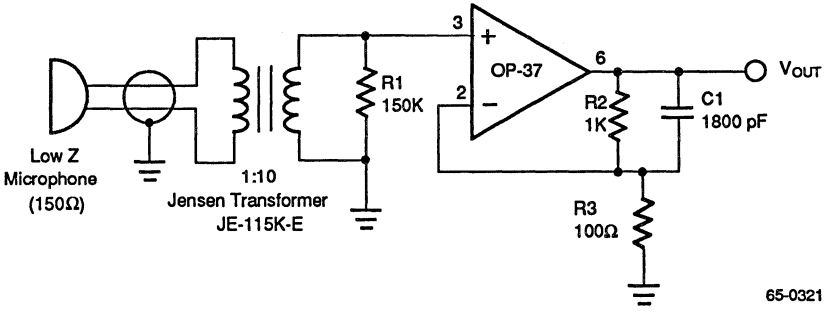


Figure 1. Low Impedance Microphone Preamplifier

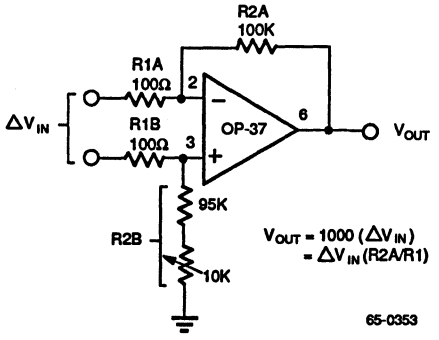


Figure 2. Difference Amplifier

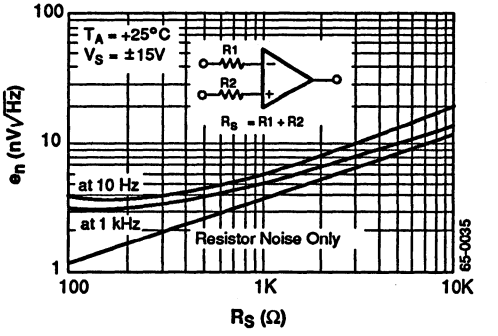
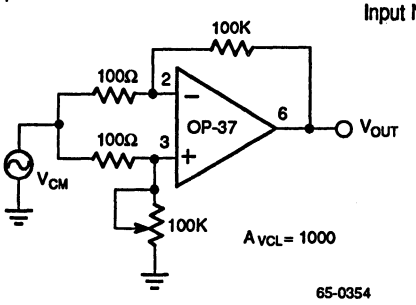


Figure 3. Difference Amplifier
Input Noise Voltage Density vs. Source Resistance



Note: Pin number shown are for 8-lead packages.

Figure 4. CMRR Test Circuit

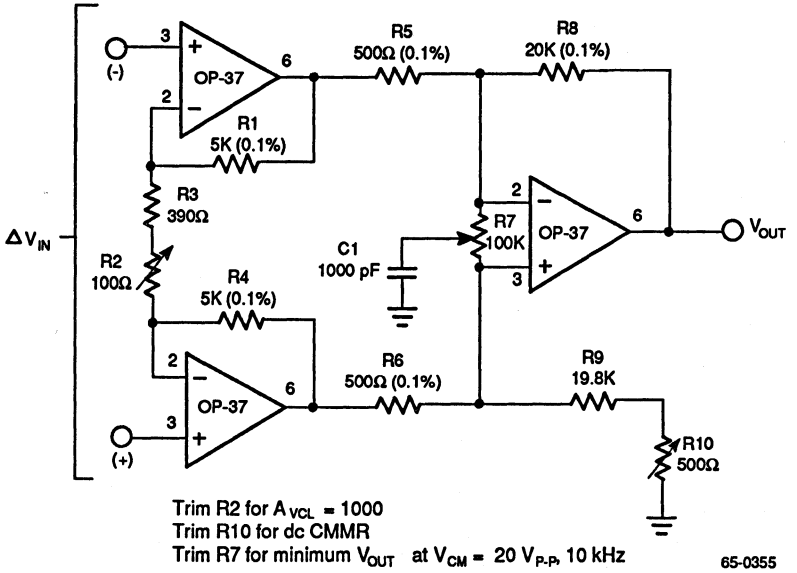
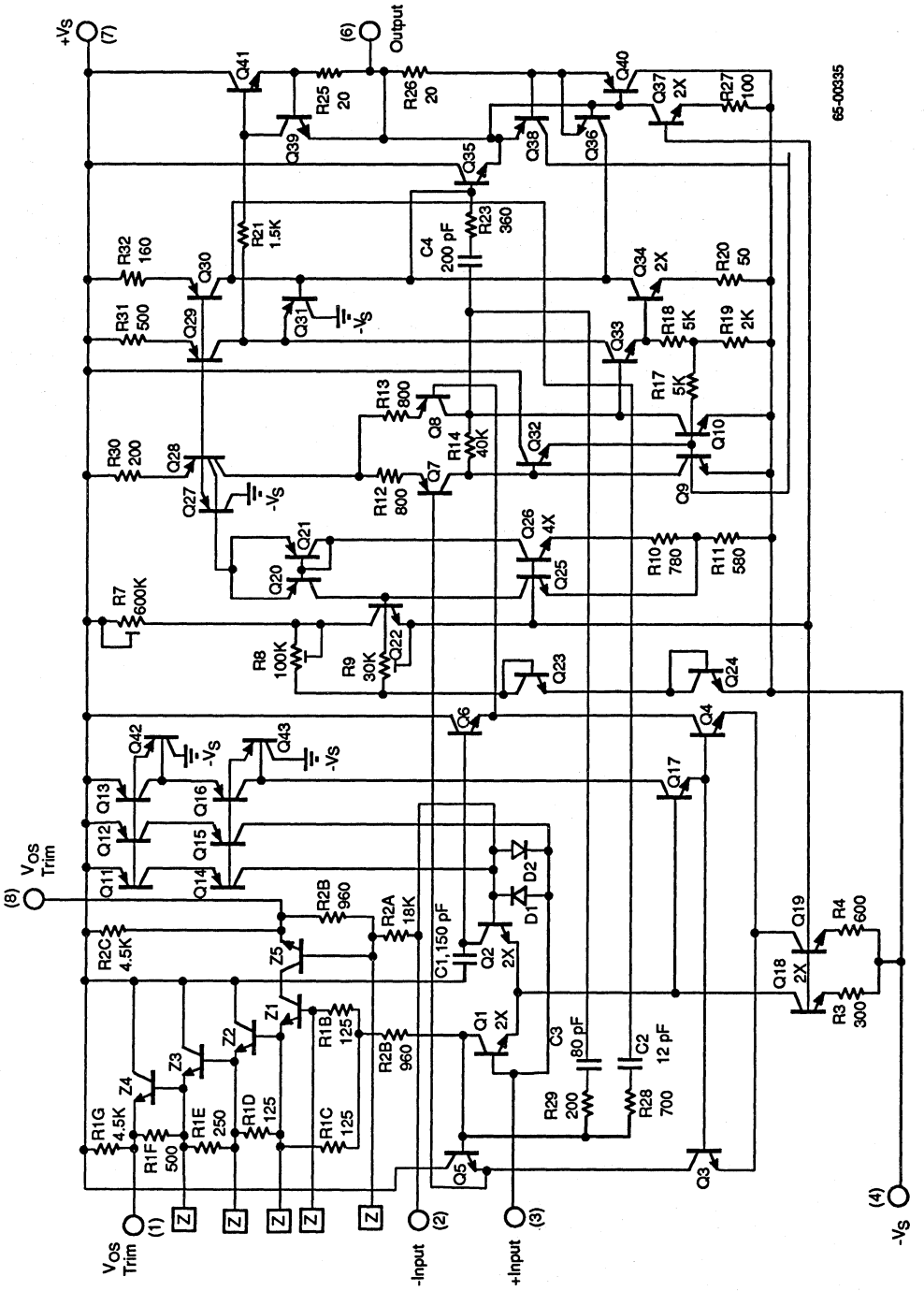


Figure 5. Three Op Amp Instrumentation Amplifier

Schematic Diagram



Note: Pin numbers shown are for 8-lead packages.

Linear

OP-77
Precision Operational Amplifier

Description

Designed to upgrade OP-07 and other similar precision op amps, the OP-77 offers ultra high performance in applications requiring high gain, superior gain-linearity, and extremely low TCV_{OS}. The OP-77's outstanding gain-linearity, which eliminates incorrectable system nonlinearities common in previous precision op amps, is achieved by an exceptional open-loop gain of more than 10 million maintained over ±10V output range. The excellent TCV_{OS} of 0.1 µV/°C, plus an extremely low power consumption of 35 mW (which reduces warm-up drift) significantly increases system accuracy over temperature. These characteristics, along with low V_{OS}, low I_{OS}, high CMRR, high PSRR, and low input noise levels, combine to raise the performance level of many high-resolution instrumentation and data conversion systems.

Advanced circuit design and wafer processing are Raytheon Semiconductor's added advantages in quality and reliability. A patented, proprietary V_{OS} trimming method after packaging significantly enhances yield and availability of top grade (A/E) devices.

Features

- Ultra high gain – 12000 V/mV
- Outstanding gain linearity
- Ultra low V_{OS} drift – 0.1 µV/°C
- Low V_{OS} – 10 µV max
- Low noise – 0.3 μV_{p-p} (0.1 Hz to 10 Hz)
- Low power consumption – 35 mW
- Low input offset current — 0.3 nA
- High CMRR – 140 dB min
- High PSRR – 120 dB min
- Replaces OP-07, 108, 741 types
- Wide range of package types

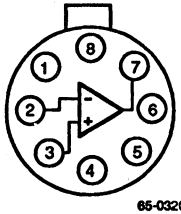
Ordering Information

Part Number	Package	Operating Temperature Range
OP-77EN	N	0°C to +70°C
OP-77FN	N	0°C to +70°C
OP-77GN	N	0°C to +70°C
OP-77EM	M	0°C to +70°C
OP-77FM	M	0°C to +70°C
OP-77GM	M	0°C to +70°C
OP-77AT	T	-55°C to +125°C
OP-77AT/883B	T	-55°C to +125°C
OP-77BT	T	-55°C to +125°C
OP-77BT/883B	T	-55°C to +125°C
OP-77AD	D	-55°C to +125°C
OP-77AD/883B	D	-55°C to +125°C
OP-77BD	D	-55°C to +125°C
OP-77BD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC

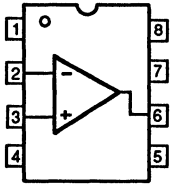
Connection Information

8-Lead TO-99 Metal Can
(Top View)



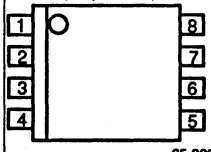
65-03205

8-Lead Dual In-Line Package
(Top View)



65-03206A

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation[2] ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
  Range ..... -65°C to +150°C
Operating Temperature Range
  OP77A,B ..... -55°C to +125°C
  OP77E,F,G ..... 0°C to +70°C
Lead Soldering Temperature
  TO-99, DIP, (60 sec) ..... +300°C
  SO-8 (10 sec) ..... +260°C

Notes:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Small Outline	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+175°C	+125°C	+125°C
Max. P_D T_A <50°C	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	45°C/W	50°C/W	–	–
Therm. Res. θ_{JA}	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-77A			OP-77B			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			±10	±25		±20	±60	µV
Long Term V_{OS} Stability[1]			0.2			0.2		µV/Mo
Input Offset Current			±0.3	±1.5		±0.3	±2.8	nA
Input Bias Current			±1.2	±2.0		±1.2	±2.8	nA
Input Noise Voltage[5]	0.1 Hz to 10 Hz		0.35	0.6		0.35	0.65	μV_{p-p}
Input Noise Voltage Density[5]	F_O = 10 Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10	13		10	13	
	F_O = 1000 Hz		9.6	11		9.6	11	
Input Noise Current[5]	0.1 Hz to 10 Hz		14	30		14	35	pA_{p-p}
Input Noise Current Density[5]	F_O = 10 Hz		0.32	0.8		0.32	0.8	$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14	0.23		0.14	0.23	
	F_O = 1000 Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[2]		26	45		18.5	45		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range[4]		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	120	140		116	140		dB
Power Supply Rejection Ratio	V_S = ±3V to ±8V	110	120		110	120		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	5000	12000		2000	8000		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ,	±13	±13.5		±13	±13.5		V
	$R_L \geq 2$ kΩ,	±12.5	±13		±12.5	±13		
	$R_L \geq 1$ kΩ,	±12	±12.5		±12	±12.5		
Slew Rate[2]	$R_L \geq 2$ kΩ,	0.1	0.2		0.1	0.2		V/µS
Closed Loop Bandwidth[2]	A_{VCL} = +1.0	0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		35	60		35	60	mW
	V_S = ±3V, R_L = ∞		2.0	4.5		2.0	4.5	
Offset Adjustment Range	R_{TRIM} = 20 kΩ		±3.5			±3.5		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. The OP-77A grade in T, D, and L packages are tested fully warmed up.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
5. Sample tested.

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-77E			OP-77F			OP-77G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			±10	±25		±20	±60		±50	±100	µV
Long Term Input Offset Voltage Stability[1]			0.3			0.4			0.4		µV/Mo
Input Offset Current			±0.3	±1.5		±0.3	±2.8		±0.3	±2.8	nA
Input Bias Current			±1.2	±2.0		±1.2	±2.8		±1.2	±2.8	nA
Input Noise Voltage[5]	0.1 Hz to 10 Hz		0.35	0.6		0.38	0.65		0.38	0.65	μV_{p-p}
	F_O = 10 Hz		10.3	18		10.5	20		10.5	20	
Input Noise Voltage	F_O = 100 Hz		10	13		10.2	13.5		10.2	13.5	nV
Density[5]	F_O = 1000 Hz		9.6	11		9.8	11.5		9.8	11.5	$\sqrt{Hz}$
Input Noise Current[5]	0.1 Hz to 10 Hz		14	30		15	35		15	35	pA_{p-p}
	F_O = 10 Hz		0.32	0.8		0.35	0.9		0.35	0.9	
Input Noise Current	F_O = 100 Hz		0.14	0.23		0.15	0.27		0.15	0.27	pA
Density[5]	F_O = 1000 Hz		0.12	0.17		0.13	0.18		0.13	0.18	$\sqrt{Hz}$
Input Resistance (Diff. Mode)[2]		26	45		18.5	45		18.5	45		MΩ
Input Resistance (Com. Mode)			200			200			200		GΩ
Input Voltage Range[4]		±13	±14		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	120	140		116	140		116	140		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	110	123		110	123		110	123		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	5000	12000		2000	6000		2000	6000		V/mV
	$R_L \geq 10$ kΩ	±13	±13.5		±13	±13.5		±13	±13.5		
Output Voltage Swing	$R_L \geq 2$ kΩ	±12.5	±13		±12.5	±13		±12.5	±13		V
	$R_L \geq 1$ kΩ	±12	±12.5		±12	±12.5		±12	±12.5		
Slew Rate[2]	$R_L \geq 2$ kΩ	0.1	0.2		0.1	0.2		0.1	0.2		V/µS
Closed-Loop Bandwidth[2]	A_{VCL} = +1.0	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		35	60		35	60		35	60	mW
	V_S = ±3V, R_L = ∞		2.0	4.5		2.0	4.5		2.0	4.5	
Offset Adjustment Range	R_{TRIM} = 20 kΩ		±3.5			±3.5			±3.5		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. The OP-77E grade on T, D, and L packages are tested fully warmed up.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
5. Sample tested.

Electrical Characteristics

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-77A			OP-77B			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			±25	±60		±45	±120	µV
Average Input Offset Voltage Drift[1]			0.1	0.3		0.2	0.6	µV/°C
Input Offset Current			±0.8	±2.2		±1.0	±4.5	nA
Average Input Offset Current Drift[2]			±5.0	±25		±5.0	±50	pA/°C
Input Bias Current			±2.4	±4.0		±2.4	±6.0	nA
Average Input Bias Current Drift[2]			±8.0	±25		±15	±35	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	120	140		110	140		dB
Power Supply Rejection Ratio	V_S = ±3V to ±8V	110	120		106	120		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	2000	6000		1000	4000		V/mV
Maximum Output Voltage Swing	R_L ≥ 2 kΩ,	±12	±13		±12	±13		V
Power Consumption	R_L = ∞		40	75		40	75	mW

Electrical Characteristics

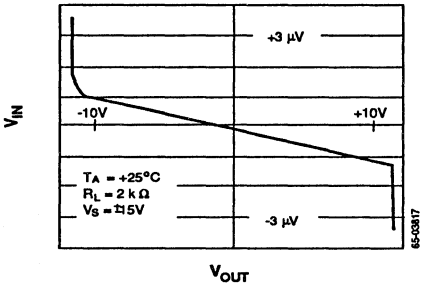
(V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

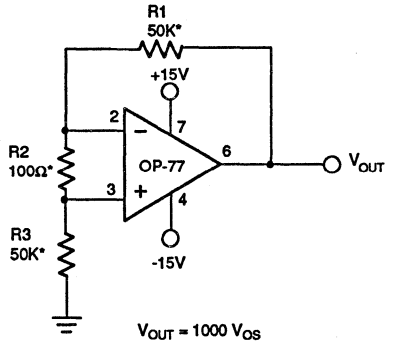
Parameters	Test Conditions	OP-77E			OP-77F			OP-77G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			±10	±45		±20	±100		±80	±100	µV
Average Input Offset Voltage Drift			0.1	0.3		0.2	0.6		0.3	1.2	µV/°C
Input Offset Current			±0.5	±2.2		±0.5	±4.5		±0.5	±4.5	nA
Average Input Offset Current Drift[2]			±1.5	±40		±1.5	±85		±1.5	±85	pA/°C
Input Bias Current			±2.4	±4.0		±2.4	±6.0		±2.4	±6.0	nA
Average Input Bias Current Drift[2]			±8	±40		±15	±60		±15	±60	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	120	140		110	140		110	140		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	110	120		106	120		106	120		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	2000	6000		1000	4000		1000	4000		V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±12	±13		±12	±13		±12	±13		V
Power Consumption	R_L = ∞		40	75		40	75		40	75	mW

Notes: 1. 100% tested for Grade A and T packages.
2. Sample tested.

Typical Performance Characteristics

OP-77 Improved Open-Loop Gain Linearity
Input vs. Output Voltage

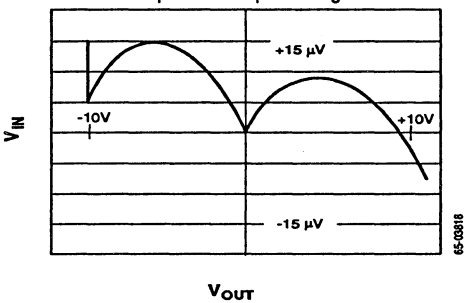


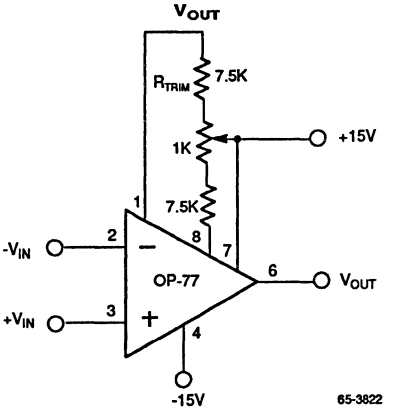


* Resistors must have low thermoelectric potential

65-03821

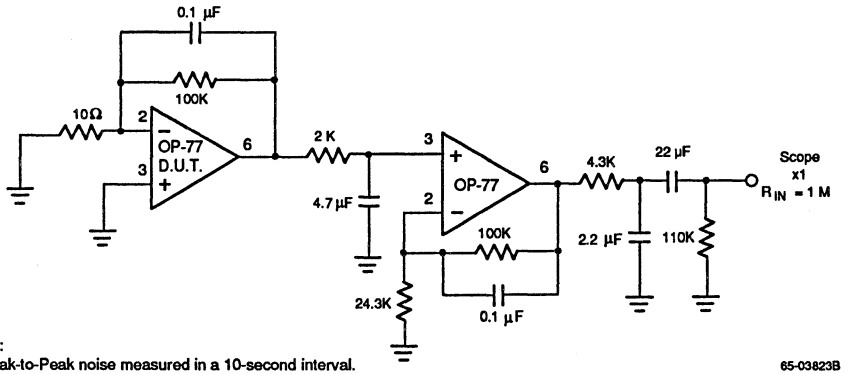
Typical Precision Op Amp Gain Linearity
Import vs. Output Voltage





Test Circuit for Input Offset Voltage and Its Drift with Temperature

Input Offset Voltage Adjustment

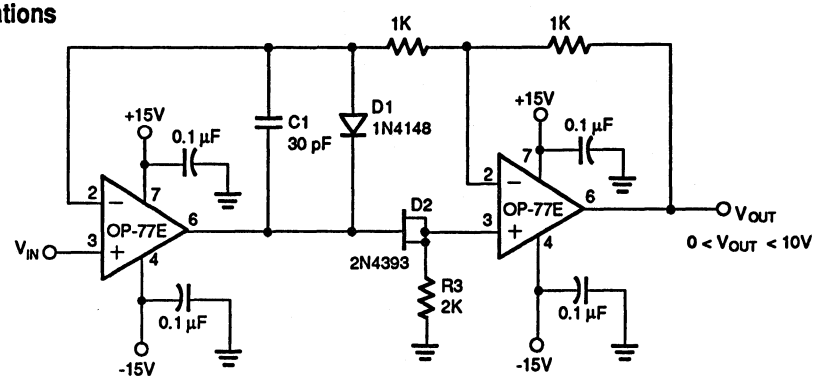


Notes:
1. Peak-to-Peak noise measured in a 10-second interval.
2. The device under test should be warmed up for 3 minutes and shielded from air currents.
3. Voltage Gain = 50,000
4. All capacitor values are for non-polarized capacitors only.
5. Pin numbers shown are for 8-lead packages.

0.1 Hz to 10 Hz Noise Test Circuit

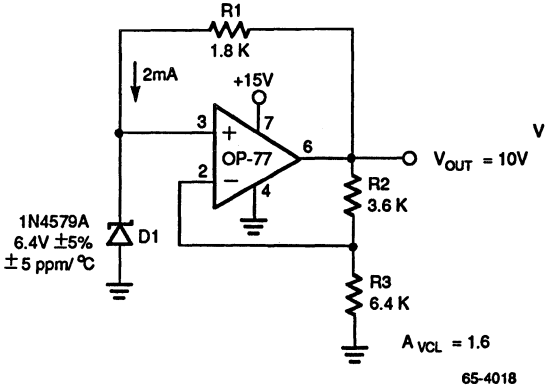
Linear

Typical Applications



The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. The OP-77E CMRR of 1 µV/V assures errors of less than 2 ppm. 65-4017

Precision Absolute Value Amplifier



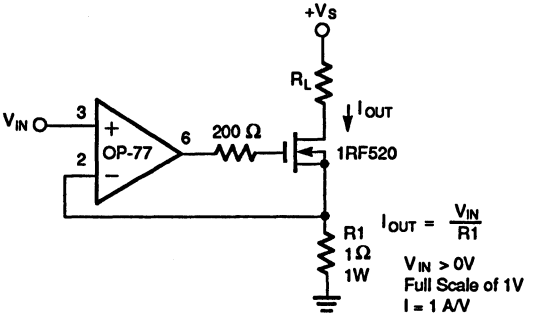
65-4018

This simple bootstrapped voltage reference provides a precise 10V virtually independent of changes in power supply voltage, ambient temperature and output loading. Correct zener operating current of exactly 2 mA is maintained by R1, a selected 5 ppm/°C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5 ppm/°C temperature coefficient of D1, 1 ppm/°C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

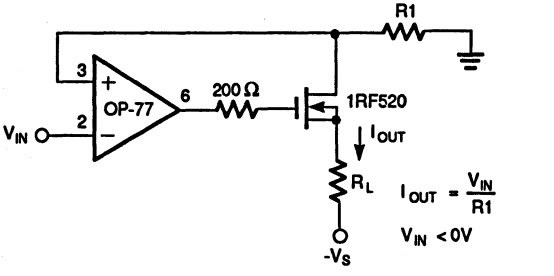
V_{OS} errors, amplified by 1.6 (A_{VCL}), appear at the output and can be significant with most monolithic amplifiers. For example: an ordinary amplifier with TCV_{OS} of 5 µV/°C contributes 0.8 ppm/°C of output error while the OP-77, with TCV_{OS} of 0.3 µV/°C, contributes but 0.05 ppm/°C of output error, thus effectively eliminating TCV_{OS} as an error consideration.

High Stability Voltage Reference

Positive Current Sink



Positive Current Source



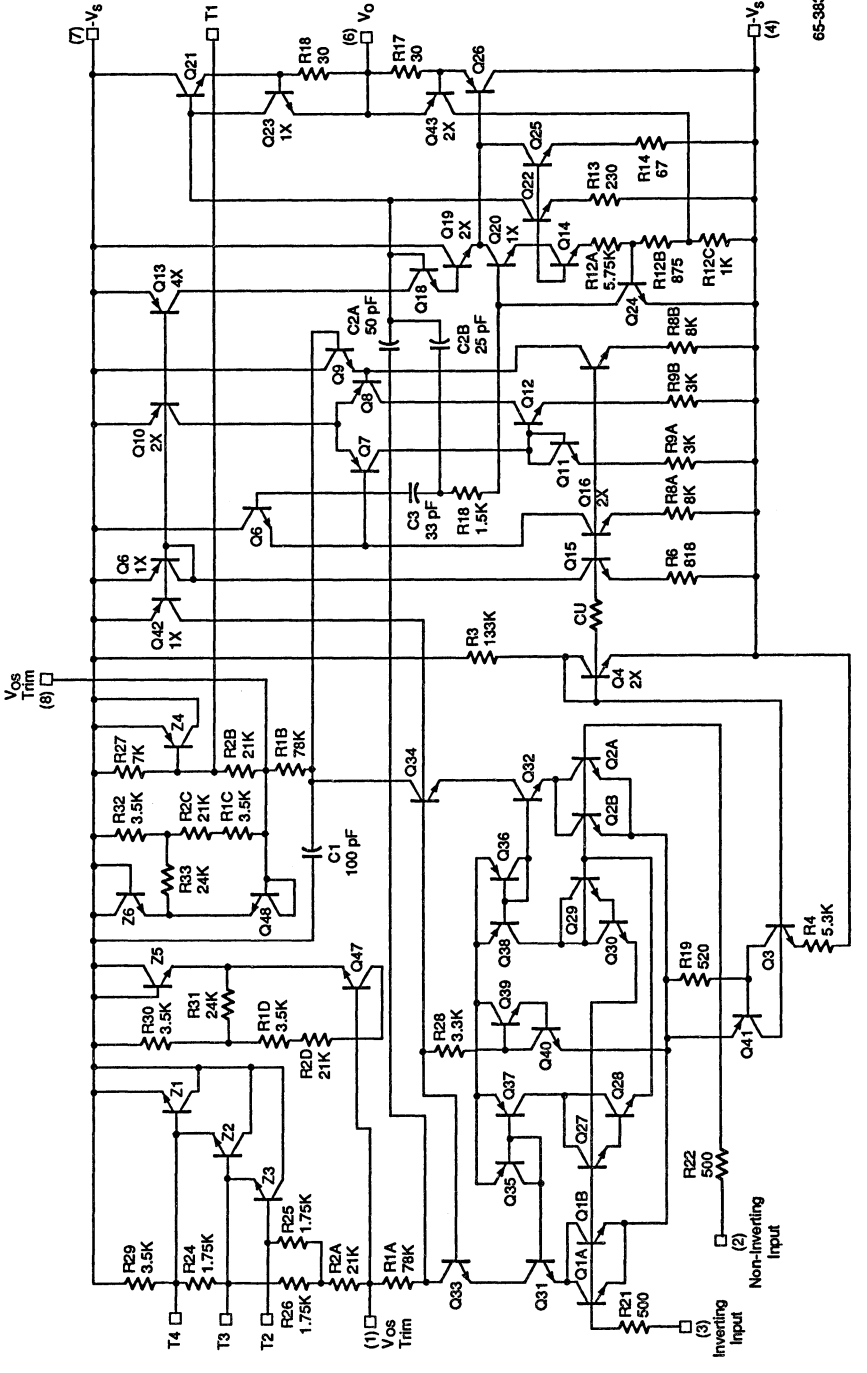
65-4019

This simple high current sink/source requires that the load float between the power supply and the sink/sources.

In these circuits, the OP-77's high gain, high CMRR, and low TCV_{OS} assure high accuracy.

Precision Current Sinks

Simplified Schematic Diagram



Note: Pin numbers shown are for 8-lead packages.

Linear

RC3403A
Ground Sensing Quad Operational Amplifier

Description

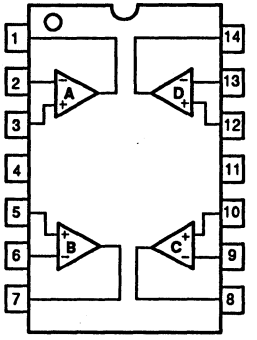
The RC3403A is a high performance ground sensing quad operational amplifier featuring improved dc specifications equal to or better than the standard 741 type general purpose op amp. The ground sensing differential input stage of this op amp provides increased slew rate compared to 741 types.

Features

- Class AB output stage — no crossover distortion
- Output voltage swings to ground in single supply operation
- High slew rate — 1.2 V/μS
- Single or split supply operation
- Wide supply operation — +2.5V to +36V or ±1.25V to ±18V
- Pin compatible with LM324 and MC3403
- Low power consumption — 0.8 mA/amplifier
- Common mode range includes ground

Connection Information

14-Lead Dual In-Line Package
(Top View)



65-0418

Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$+V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	Output (C)
9	-Input (C)
10	+Input (C)
11	$-V_S$ (Gnd)
12	+Input (D)
13	-Input (D)

Ordering Information

Part Number	Package	Operating Temperature Range
RC3403AN	N	0°C to +70°C

Notes:
N = 14-lead plastic DIP.

Absolute Maximum Ratings (1)

Supply Voltage ..... +36V or ±18V
Input Voltage ..... -0.3 to +36V
Differential Input Voltage 36V
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range .. 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Notes:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Thermal Characteristics

	14-Lead Plastic DIP
Max. Junction Temp.	+125°C
Max. P_D T_A <50°C	468mW
Therm. Res θ_{JC}	—
Therm. Res. θ_{JA}	160°C/W
For T_A >50°C Derate at	6.25 mW/°C

Low Voltage Electrical Characteristics

($+V_S$ = +5V, $-V_S$ = GND, and T_A = +25° C)

Parameters	Test Conditions	RC3403A Min	RC3403A Typ	RC3403A Max	Units
Input Offset Voltage			2.0	10	mV
Input Bias Current			-150	-500	nA
Input Offset Current			30	50	nA
Supply Current	$R_L = \infty$ All Amplifiers		2.5	5.0	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	20	200		V/mV
Output Voltage Swing[1]	$R_L \geq 10k\Omega$	3.5			V_{p-p}
Channel Separation	1kHz ≤F≤ 200kHz (Input referred)		120		dB
Power Supply Rejection Ratio		76			dB

Note 1. Output will swing to ground.

Electrical Characteristics

($\pm V_S$ = ±15V, 0°C ≤T_A ≤ +70°C)

Parameters	Test Conditions	RC3403A Min	RC3403A Typ	RC3403A Max	Units
Input Offset Voltage				10	mV
Input Bias Current				-800	nA
Input Offset Current				200	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V

Electrical Characteristics

($\pm V_S = \pm 15V$, T_A +25° C)

Parameters	Test Conditions	RC3403A			Units
		Min	Typ	Max	
Input Offset Voltage			2.0	6.0*	mV
Input Bias Current			-150	-500	nA
Input Offset Current			30	50	nA
Input Voltage Range		0		$+V_S$ -2	V
Supply Current	$R_L = \infty$ On All Op Amps		3.0	5.0*	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	25*	100		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±13	±14		V
Common Mode Rejection Ratio	DC	70	90		dB
Channel Separation	±1 kHz to 20kHz		120		dB
Output Source Current	$+V_{IN} = 1V$, $-V_{IN} = 0V$	20	40		mA
Output Sink Current		10	20		mA
Unity Gain Bandwidth			1.0		MHz
Slew Rate	$A_V = 1$, $-10 \leq V_{IN} < +10$		1.2*		V/µS
Distortion (Crossover)	F = 20kHz, $V_{OUT} = 10V_{p-p}$		1.0		%
Power Bandwidth	$V_{OUT} = 10V_{p-p}$		40		kHz
Power Supply Rejection Ratio		80	94		dB

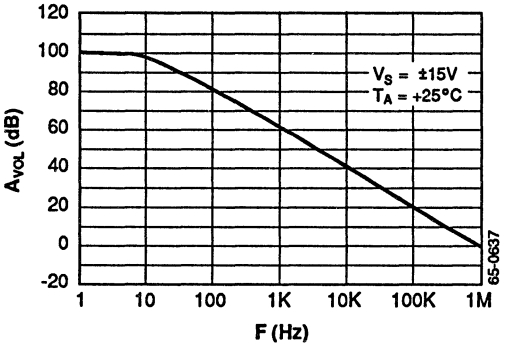
*Significantly improved performance.

Electrical Characteristics Comparison
RC3403A, MC3403, LM324

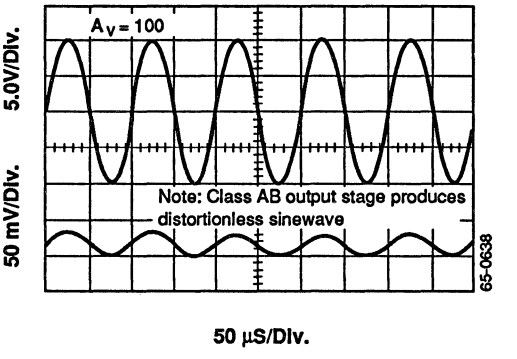
MAX Ratings	RC3403A			MC3403			LM324			Units
Supply Voltage	+36 or ±18			+36 or ±18			+32 or ±16			V
Differential Input Voltage	36			36			32			V
Input Voltage	36			36			32			V
Electrical Characteristics	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Test Conditions		±15			±15			+5.0		V
Input Offset Voltage		2.0	6.0		2.0	8.0		2.0	7.0	mV
Input Offset Current		±30	±50		±30	±50		±5.0	±50	nA
Input Bias Current		150	500		200	500		45	500	nA
Input Voltage Range	0		$+V_S$ -2	0		$+V_S$ -2	0		$+V_S$ -1.5	V
Supply Current		3.0	5.0		2.8	7.0		0.8	2.0	mA
Large Signal Voltage Gain	25	100		20	200			100		V/mV
Output Voltage Swing	±13	±14		±10	±13		0		$+V_S$ -1.5	V
Common Mode Rejection Ratio	70	90		70	90			85		dB
Power Supply Rejection Ratio	80	94		76	90			85		dB
Unity Gain Bandwidth		1.0			1.0			1.0		MHz
Slew Rate		1.2			0.6			0.4		V/μS
Output Sink Current	10	20						20		mA
Output Source Current	20	40					20	40		mA
Channel Separation		120			120			120		dB
Distortion (Crossover)		1.0			1.0					%

Typical Performance Characteristics

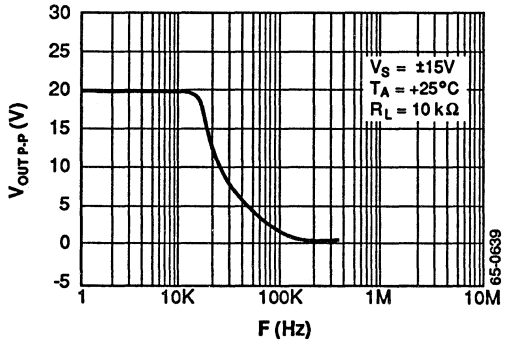
Open Loop Gain vs. Frequency



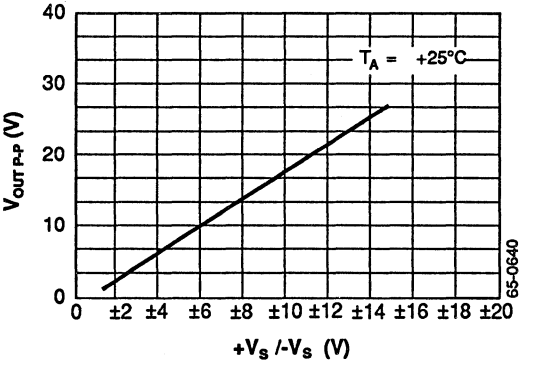
Sinewave Response



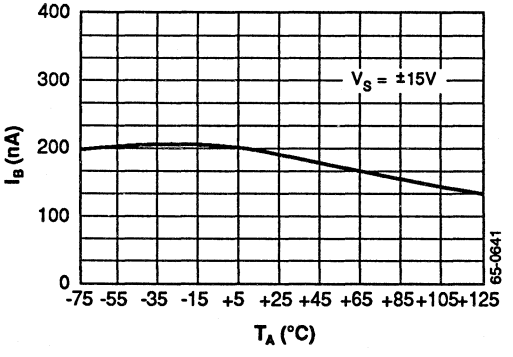
Output Voltage vs. Frequency



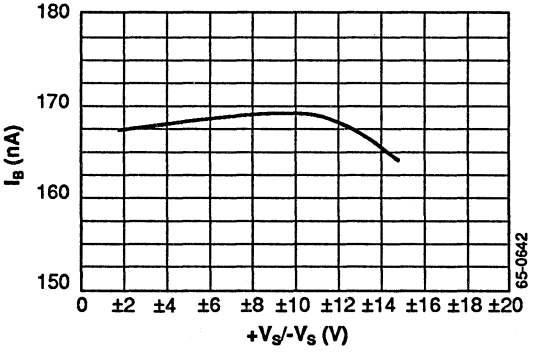
Output Swing vs. Supply Voltage



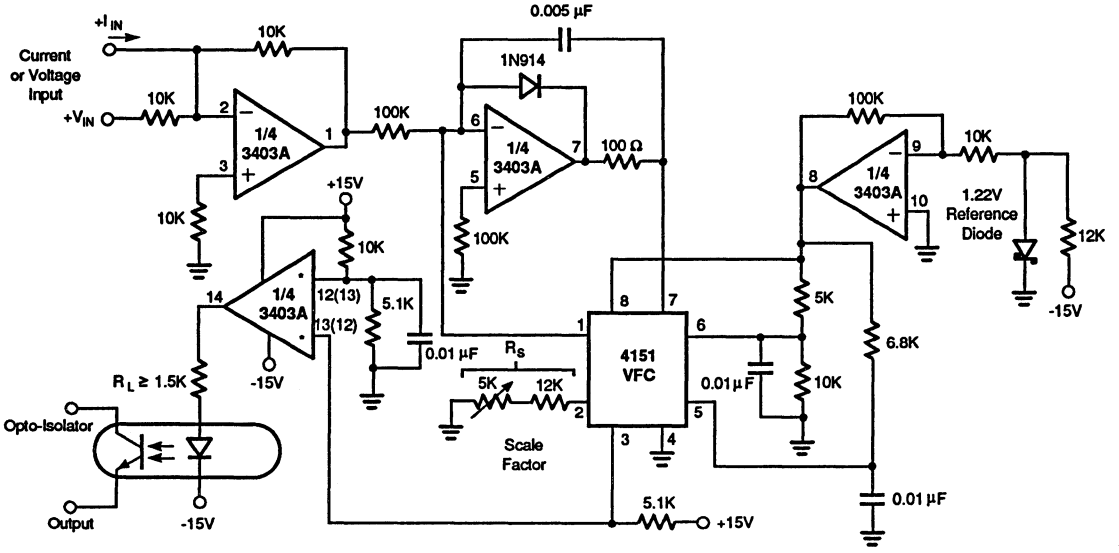
Input Bias Current vs. Temperature



Input Bias Current vs. Supply Voltage



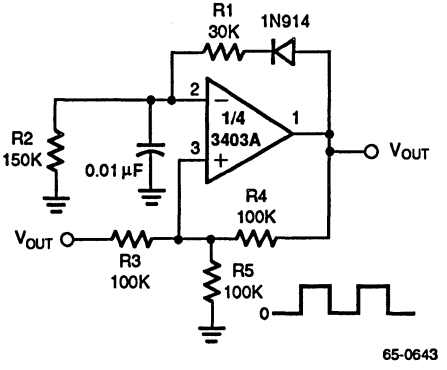
Typical Applications



*Polarity determined by desired relationship between pulse output level and LED "On" state.

65-0636

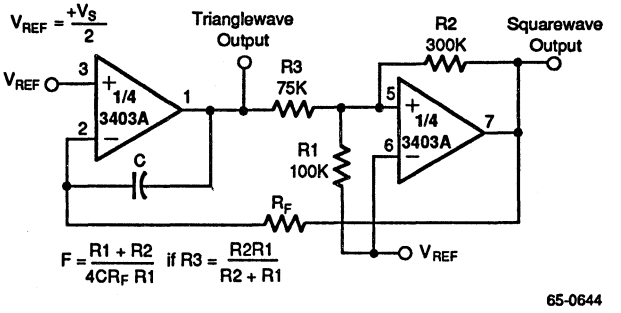
Precision Voltage-to-Frequency Converter With Isolated Output



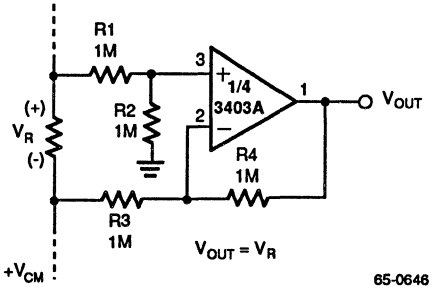
65-0643

Pulse Generator

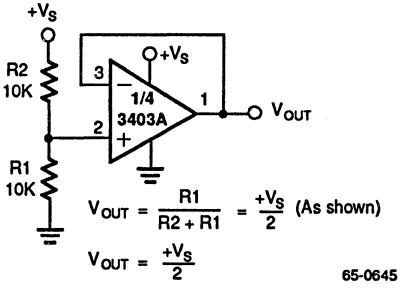
Typical Applications (Continued)



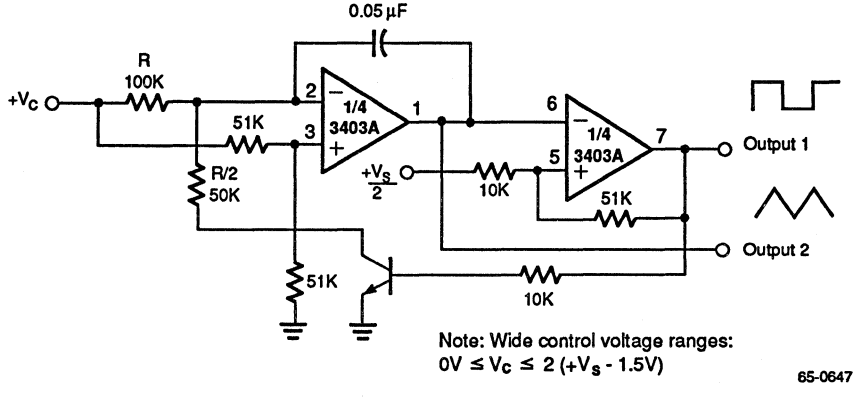
Function Generator



Ground Referencing a Differential Input Signal

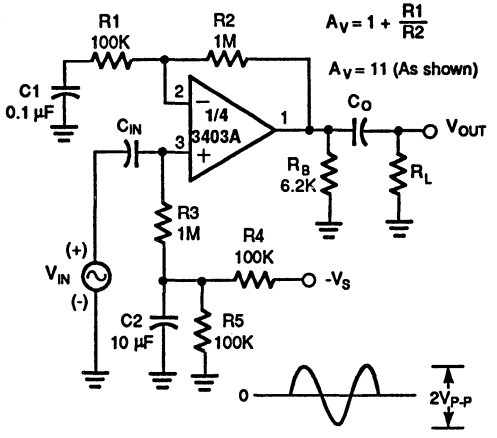


Voltage Reference

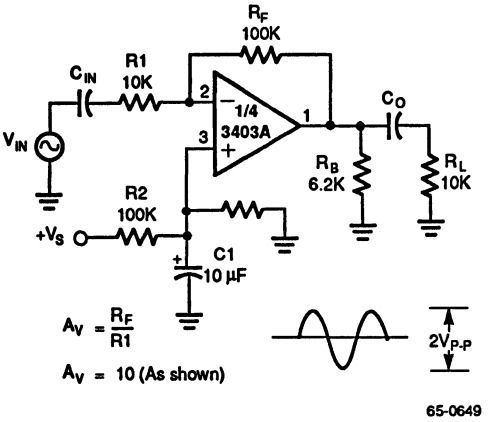


Voltage Controlled Oscillator

Typical Applications (Continued)

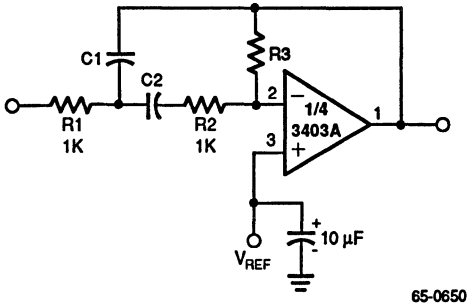


AC Coupled Non-Inverting Amplifier 65-0648



65-0649

AC Coupled Inverting Amplifier



65-0650

F_O Δ Center Frequency
BW Δ Bandwidth
R in kΩ
C in µF

$Q = \frac{F_O}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

$R1 = R2 = 1$
$R3 = 9Q^2 - 1$ } Use scaling factors in these expressions.

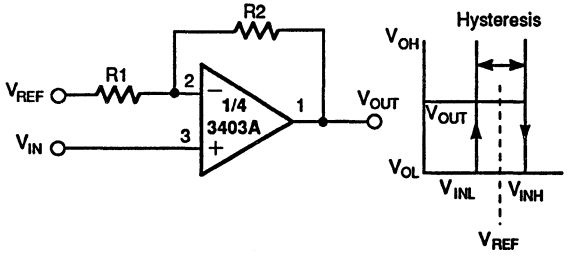
If source impedance is high or varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

Design Example:

Given: Q = 5, F_O = 1 kHz
Let R1 = R2 = 10 kΩ
Then R3 = 9 $(5)^2$ - 10
R3 = 215 kΩ

$C = \frac{5}{3} = 1.6$ nF

Multiple Feedback Bandpass Filter



$V_{INL} = \frac{R1}{R1 + R2} (V_{OL} - V_{REF}) + V_{REF}$

$V_{INH} = \frac{R1}{R1 + R2} (V_{OH} - V_{REF}) + V_{REF}$

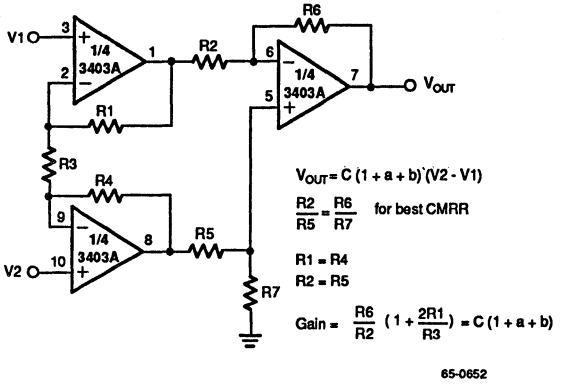
$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$

65-0653

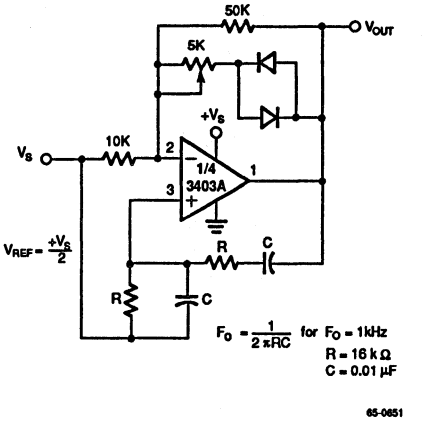
Comparator With Hysteresis

Linear

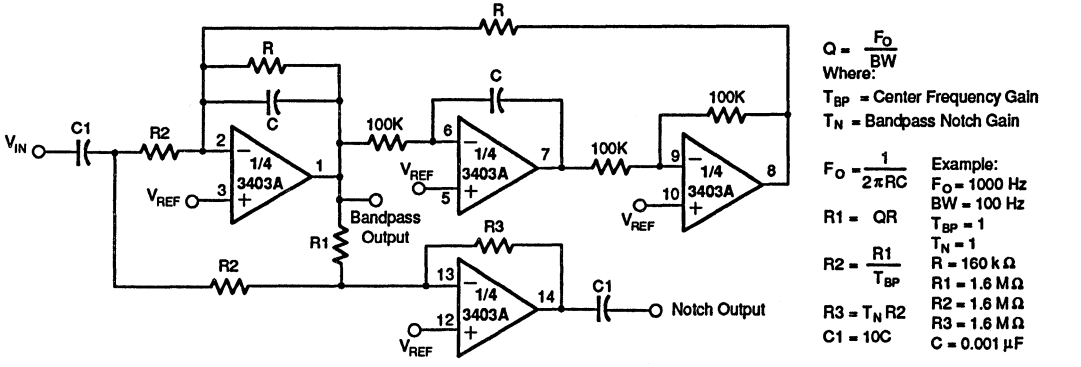
Typical Applications (Continued)



High Impedance Differential Amplifier

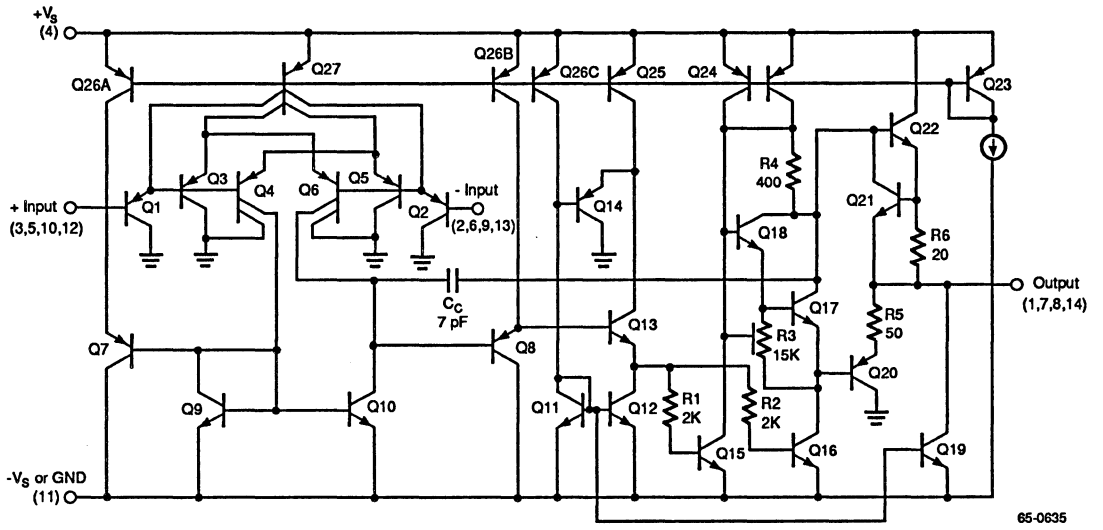


Wein Bridge Oscillator



Bi-Quad Filter

Schematic Diagram (1/4 Shown)



Linear

RC4136
General Performance Quad 741 Operational Amplifier

Description

The 4136 is made up of four 741 type independent high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial process.

This amplifier meets or exceeds all specifications for 741 type amplifiers. Excellent channel separation allows the use of the 4136 quad amplifier in all 741 operational amplifier applications providing the highest possible packaging density.

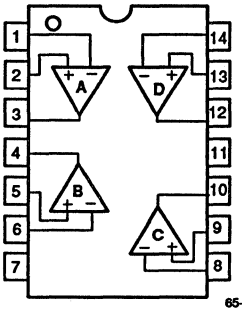
The specially designed low noise input transistors allow the 4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners.

Features

- Unity gain bandwidth — 3 MHz
- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Connection Information

14-Lead Dual-In-Line Package
(Top View)



Pin	Function
1	-Input (A)
2	+Input (A)
3	Output (A)
4	Output (B)
5	+Input (B)
6	-Input (B)
7	$-V_S$
8	-Input (C)
9	+Input (C)
10	Output (C)
11	$+V_S$
12	Output (D)
13	+Input (D)
14	-Input (D)

Thermal Characteristics

	14-Lead Small Outline	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+125°C	+175°C
Max. P_D T_A <50°C	300 mW	468 mW	1042 mW
Therm. Res θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW per °C	6.25 mW per °C	8.38 mW per °C

Absolute Maximum Ratings

Supply Voltage
- RM4136 ..... ±22V
- RC4136 ..... ±18V

Input Voltage[1] ..... ±30V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
- RM4136 ..... -55°C to +125°C
- RC4136 ..... 0°C to +70°C

Lead Soldering Temperature
- (DIP, 60 sec) ..... +300°C
- (SO-14, 10 sec) ..... +260°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground, typically 45 mA.

Ordering Information

Part Number	Package	Operating Temperature Range
RC4136N	N	0°C to +70°C
RC4136M	M	0°C to +70°C
RM4136D	D	-55°C to +125°C
RM4136D/883B	D	-55°C to +125°C

Notes:
883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
M = 14-lead plastic SOIC

Electrical Characteristics

(V_S = ±15V and T_A = +25°C, unless otherwise noted)

Parameters	Test Conditions	RM4136			RC4136			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		76	100		dB
Power Consumption	$R_L = \infty$, All Outputs		210	340		210	340	mW
Transient Response								
Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.13			0.13		µS
Overshoot	$C_L \leq 100pF$		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate	$R_L \geq 2k\Omega$		1.5			1.0		V/µS
Channel Separation	F = 1.0kHz, R_S=1kΩ		90			90		dB

The following specifications apply for RM = -55°C ≤ T_A ≤ = 125° RC = 0°C ≤ T_A ≤ = 70°, V_S = ± 15V

Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption			240	400		240	400	mW

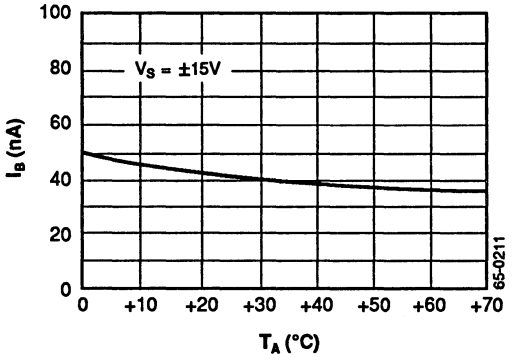
Electrical Characteristics Comparison

(V_S = ±15V and T_A +25°C unless otherwise noted)

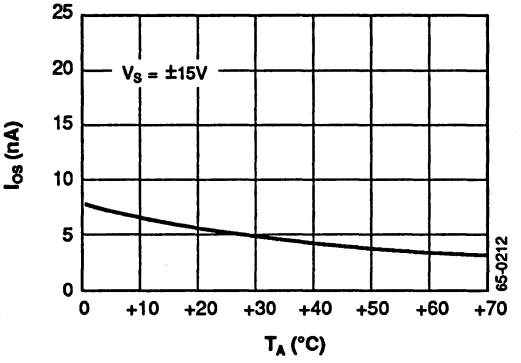
Parameter	RC4136(Typ)	RC741(Typ)	LM324(Typ)	Units
Input Offset Voltage	0.5	2.0	2.0	mV
Input Offset Current	5.0	10	5.0	nA
Input Bias Current	40	80	55	nA
Input Resistance	5.0	2.0		MΩ
Large Signal Voltage Gain (R_L = 2kΩ)	300	200	100	V/mV
Output Voltage Swing (R_L = 2kΩ)	±13V	±13V	$\lvert +V_S - 1.2V \rvert$ to $-V_S$	V
Input Voltage Range	±14V	±13V	$\lvert +V_S - 1.5V \rvert$ to $-V_S$	V
Common Mode Rejection Ratio	100	90	85	dB
Power Supply Rejection Ratio	100	90	100	dB
Transient Response				
Rise Time	0.13	0.3		µS
Overshoot	5.0	5.0		%
Unity Gain Bandwidth	3.0	0.8	0.8	MHz
Slew Rate	1.0	0.5	0.5	V/µS
Input Noise Voltage Density (F= 1kHz)	10	22.5		nV/√Hz
Short Circuit Current	±45	±25		mA

Typical Performance Characteristics

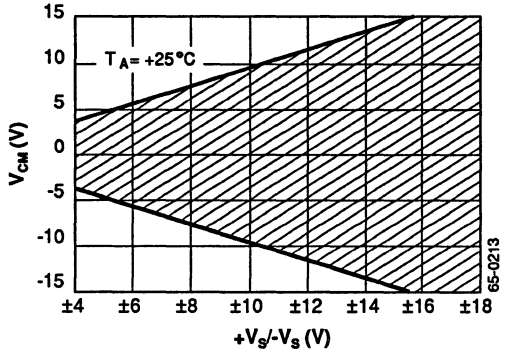
Input Bias Current vs. of Temperature



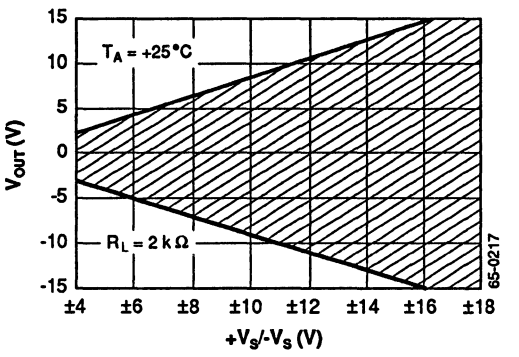
Input Offset Current vs. Temperature



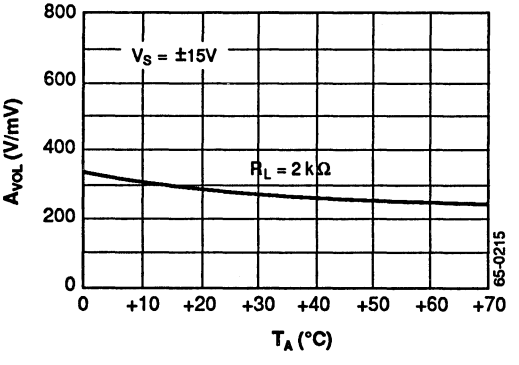
Input Common Mode Voltage Range vs. Supply Voltage



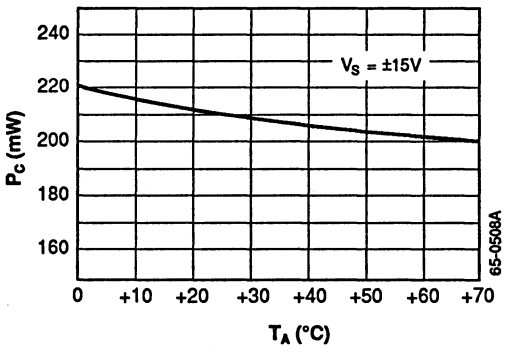
Output Voltage vs. Supply Voltage



Open Loop Gain vs. Temperature



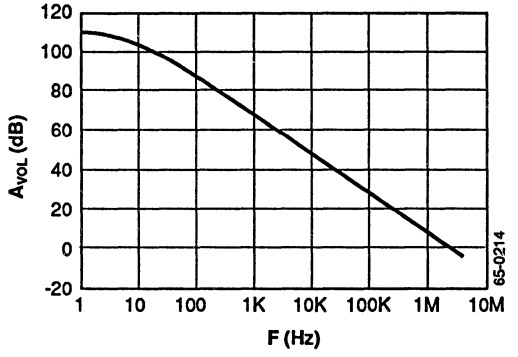
Power Consumption vs. Temperature



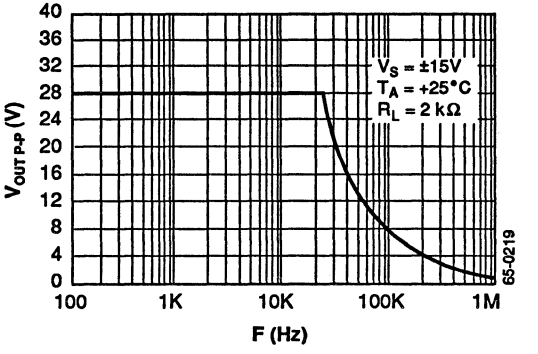
Linear

Typical Performance Characteristics (Continued)

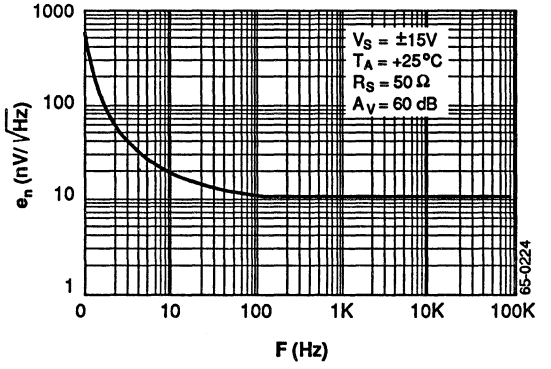
Open Loop Gain vs. Frequency



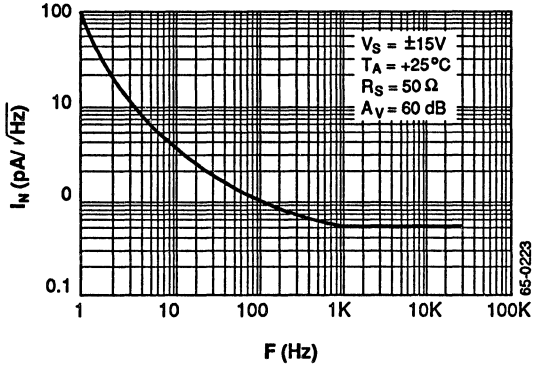
Output Voltage Swing vs. Frequency



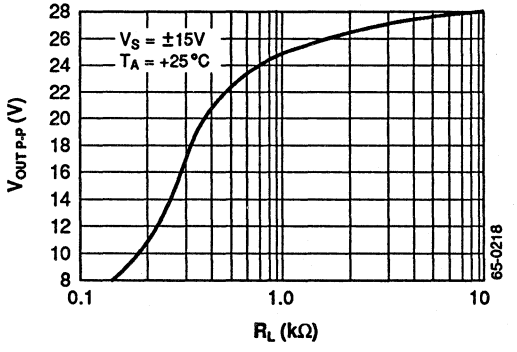
Input Noise Voltage Density vs. Frequency



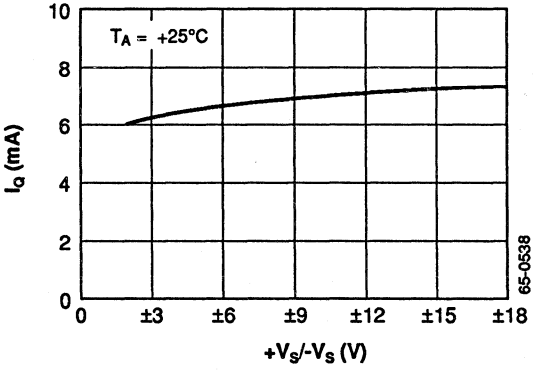
Input Noise Current Density vs. Frequency



Output Voltage Swing vs. Load Resistance

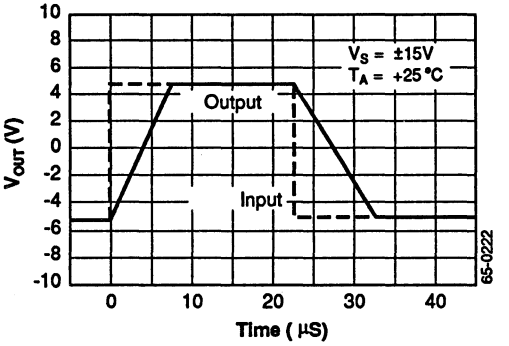


Quiescent Current vs. Supply Voltage

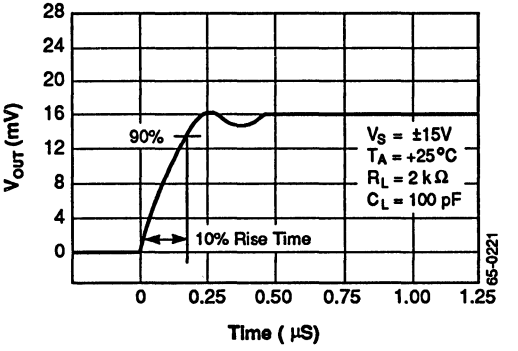


Typical Performance Characteristics (Continued)

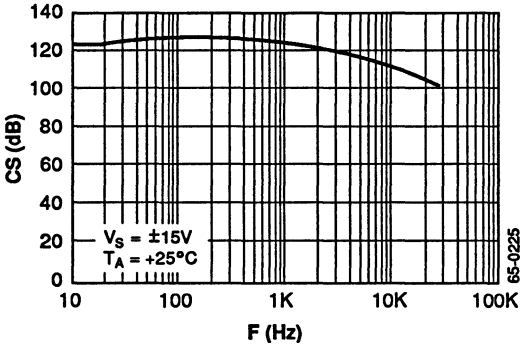
Follower Large Signal Pulse Response



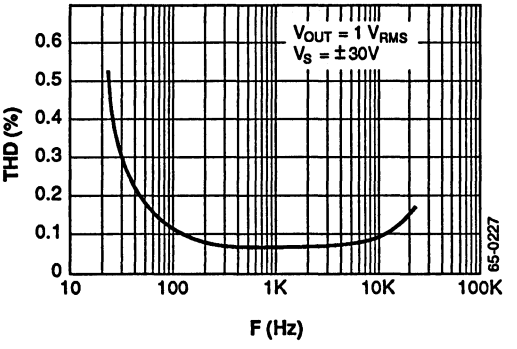
Transient Response Output Voltage vs. Time



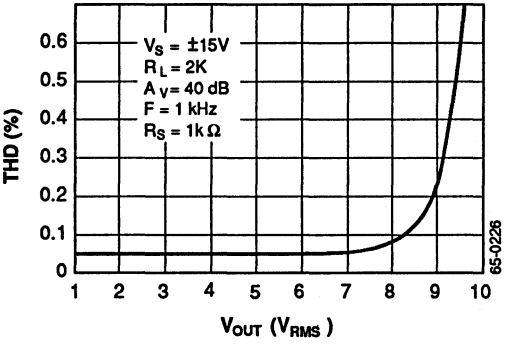
Channel Separation vs. Frequency



Total Harmonic Distortion vs. Frequency



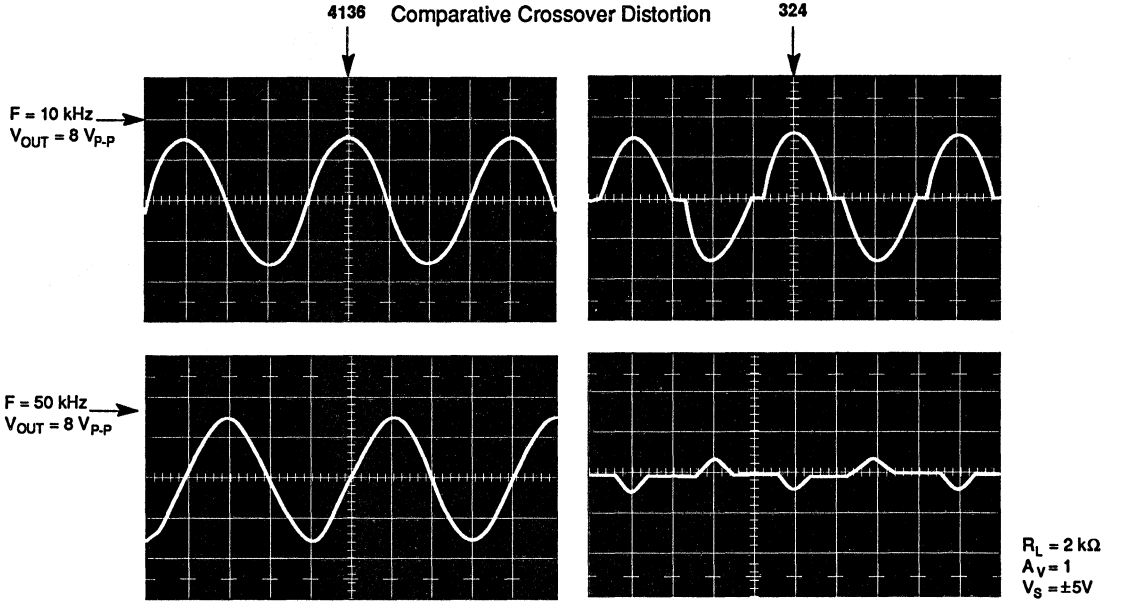
Total Harmonic Distortion vs. Output Voltage



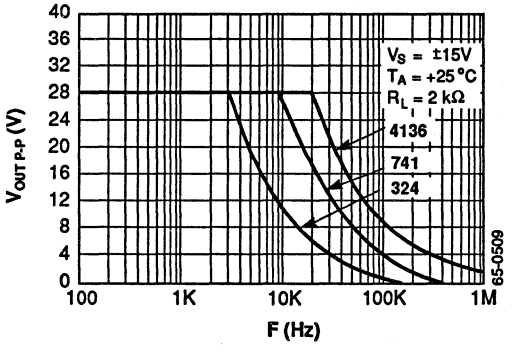
Linear

4136 Versus 324

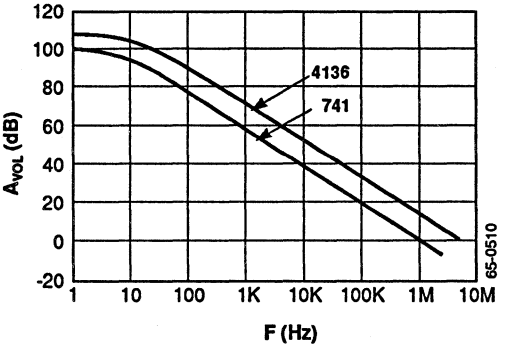
Although the 324 is an excellent device for single-supply applications where ground sensing is important, it is a poor substitute for four 741s in split supply circuits. The simplified input circuit of the 4136 exhibits much lower noise than that of the 324 and exhibits no crossover distortion as compared with the 324 (see illustration). The 324 shows significant crossover distortion and pulse delay in attempting to handle a large signal input pulse.



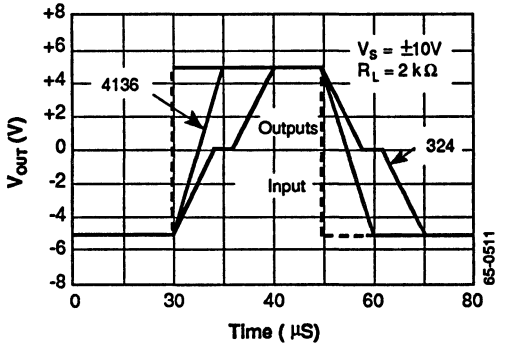
Output Voltage Swing vs. Frequency



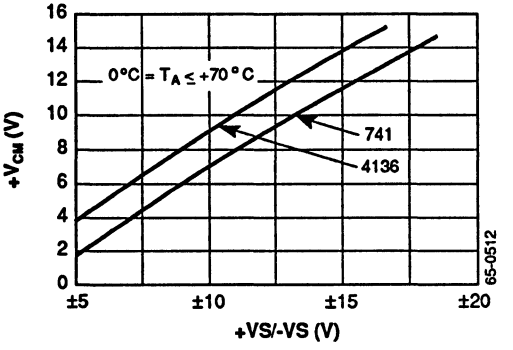
Open Loop Gain vs. Frequency



Follower Large Signal Pulse Response
Output Voltage vs. Time



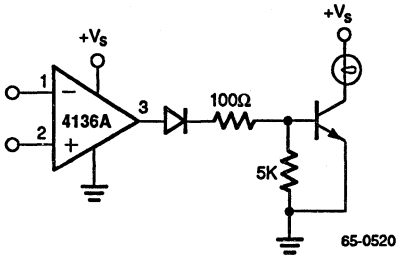
Input Common Mode Voltage Range vs.
Supply Voltage



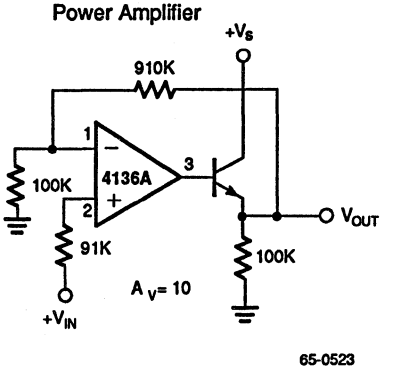
Linear

Typical Applications (Continued)

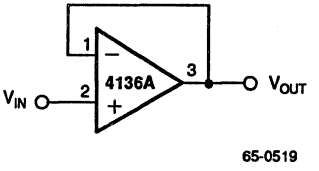
Lamp Driver



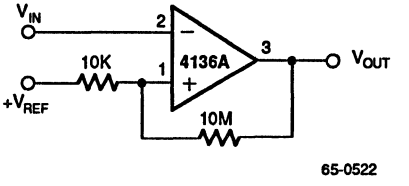
Power Amplifier



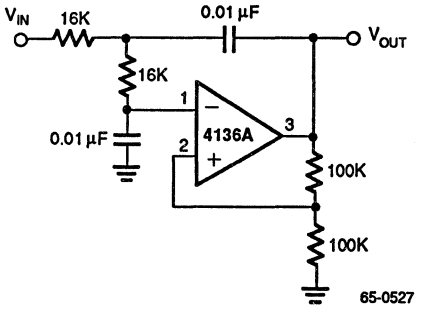
Voltage Follower



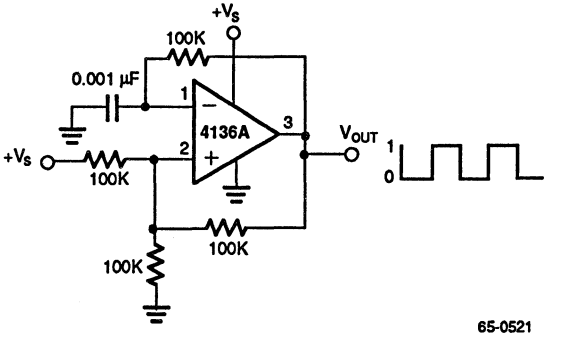
Comparator with Hysteresis



DC Coupled 1 kHz Lowpass Active Filter

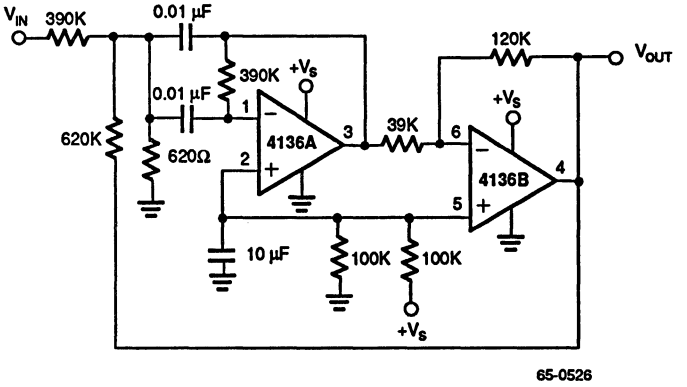


Squarewave Oscillator



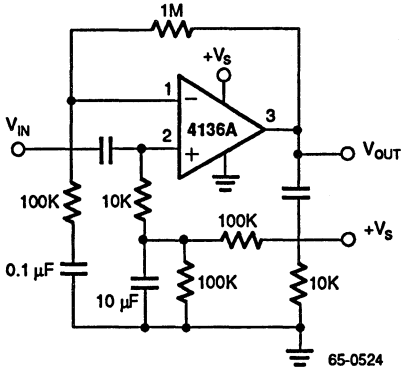
Typical Applications (Continued)

1 kHz Bandpass Active Filter



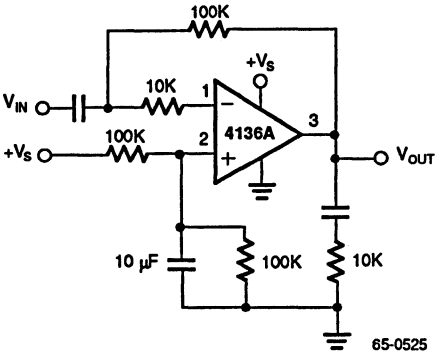
65-0526

AC Coupled Non-Inverting Amplifier



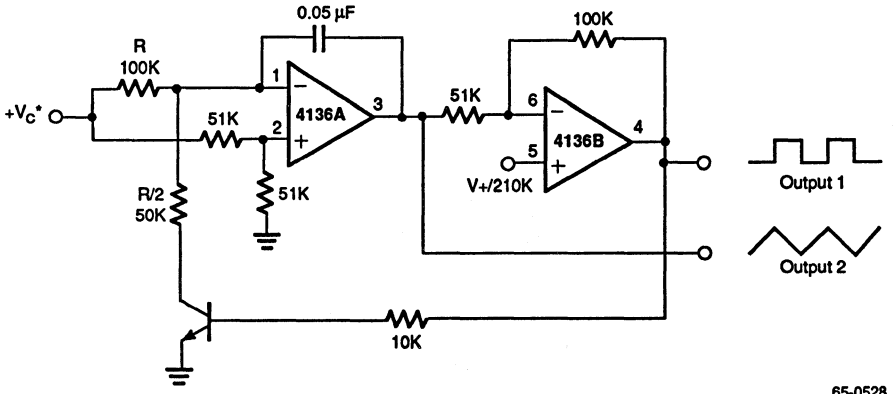
65-0524

AC Coupled Inverting Amplifier



65-0525

Voltage Control Oscillator (VCO)



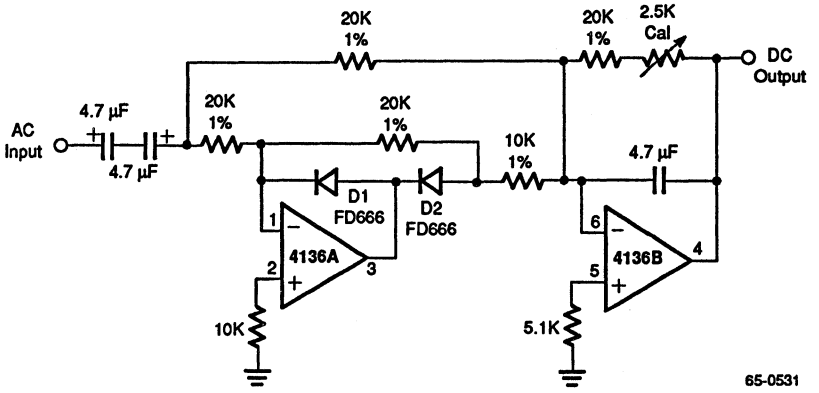
65-0528

* Wide control voltage range: 0V < V_C < 2(+V_S-1.5V)

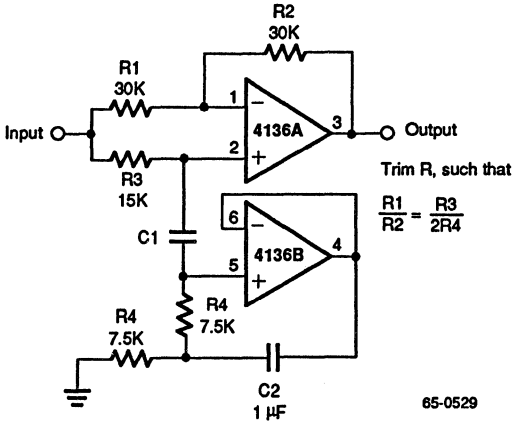
Linear

Typical Applications (Continued)

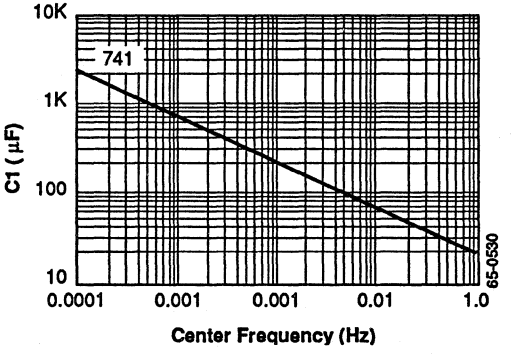
Full-Wave Rectifier and Averaging Filter



Notch Filter Using the 4136 as a Gyrator

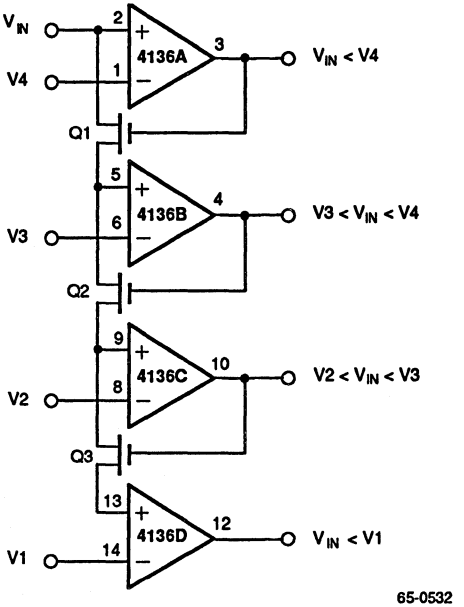


Notch Frequency vs. C1

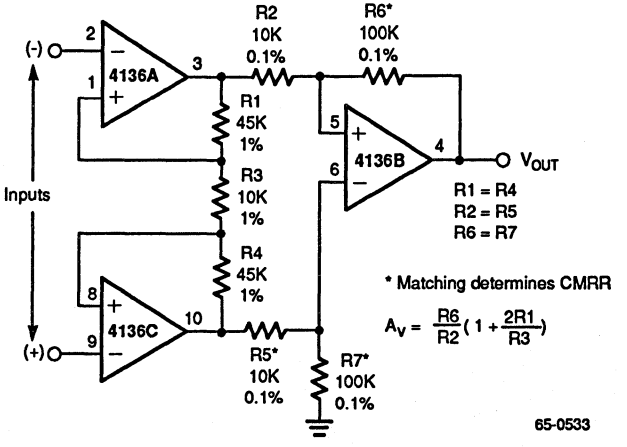


Typical Applications (Continued)

Multiple Aperture Window Discriminator



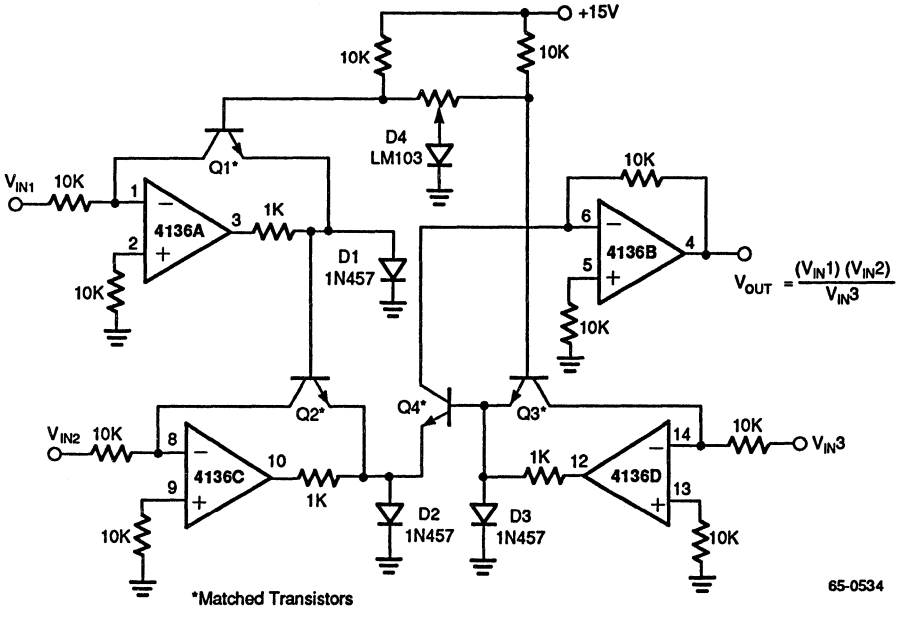
Differential Input Instrumentation Amplifier with High Common Mode Rejection



Linear

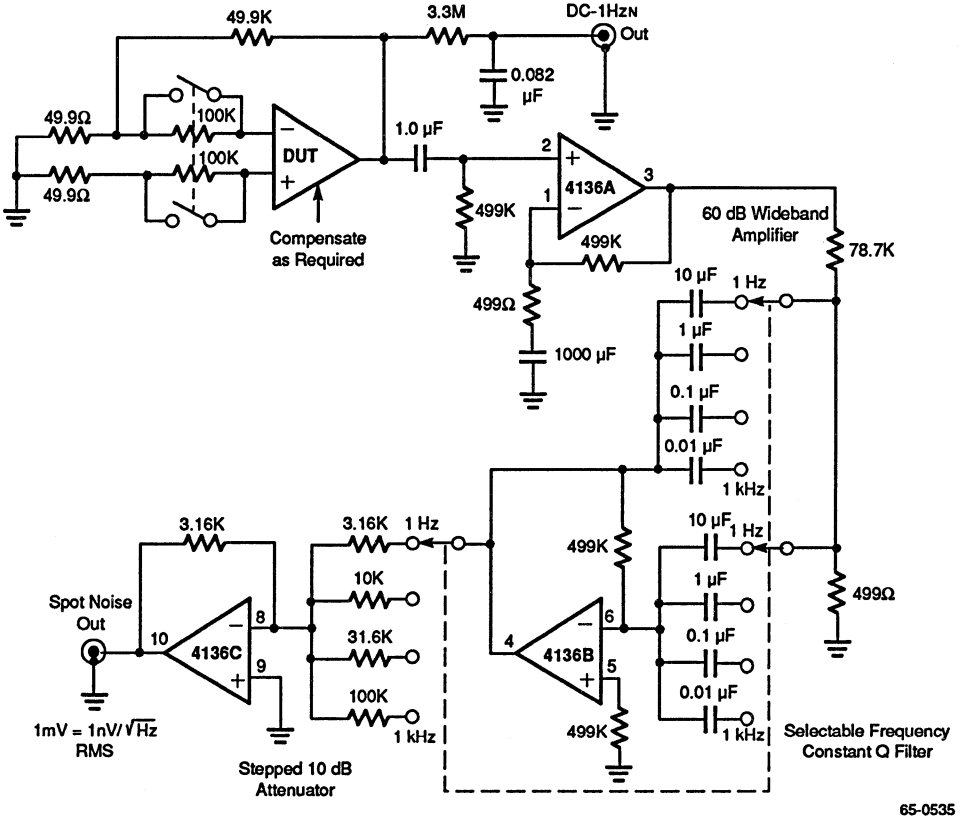
Typical Applications (Continued)

Analog Multiplier/Divider



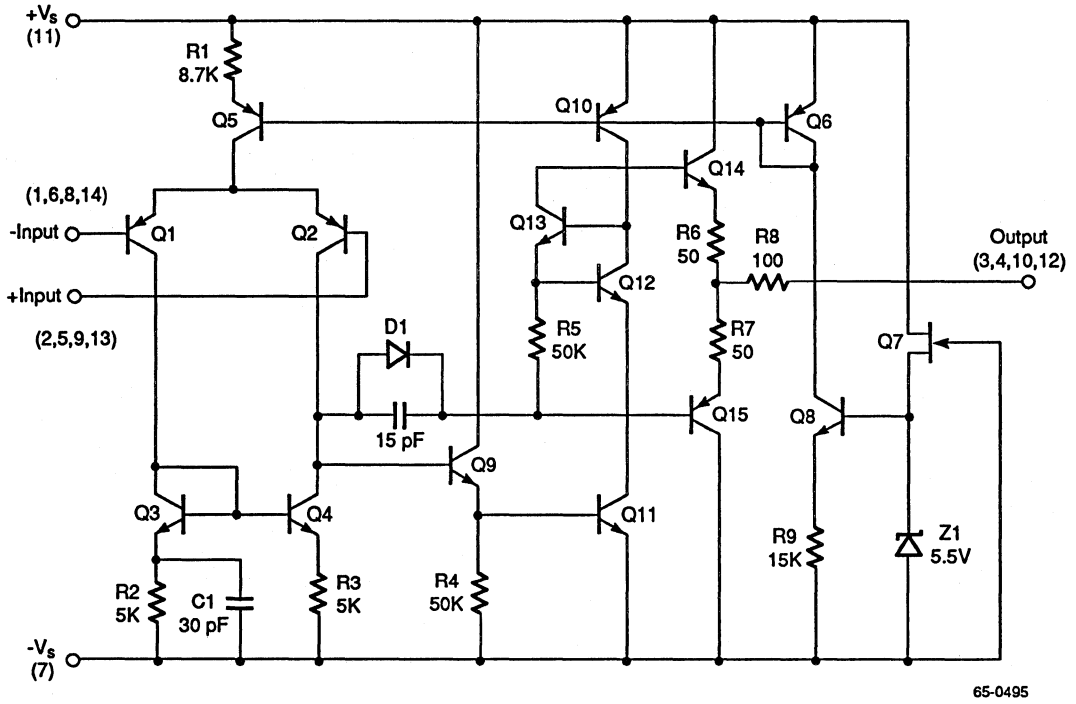
Typical Applications (Continued)

Spot Noise Measurement Test Circuit



Linear

Schematic Diagram



RC4156/RC4157
High Performance Quad Operational Amplifiers

Description

The 4156 and 4157 are monolithic integrated circuits, consisting of four independent high performance operational amplifiers constructed with an advanced epitaxial process.

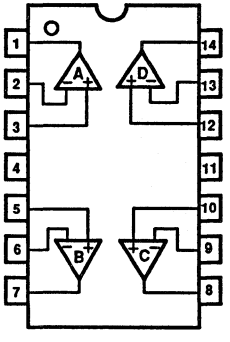
These amplifiers feature guaranteed AC performance which far exceeds that of the 741 type amplifiers. Also featured are excellent input characteristics and guaranteed low noise, making this device the optimum choice for audio, active filter and instrumentation applications. The 4157 is a decompensated version of the 4156 and is AC stable in gain configurations of -5 or greater.

Features

- Unity gain bandwidth for 4156 — 3.5 MHz
- Unity gain bandwidth for 4157 — 19 MHz
- High slew rate for 4156 — 1.6 V/μS
- High slew rate for 4157 — 8.0V/μS
- Low noise voltage —1.4 μV_{RMS}
- Indefinite short circuit protection
- No crossover distortion

Connection Information

14-Lead
Dual In-Line Package
(Top View)



65-0736

Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$+V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	Output (C)
9	-Input (C)
10	+Input (C)
11	$-V_S$
12	+Input (D)
13	-Input (D)
14	Output (D)

Ordering Information

Part Number	Package	Operating Temperature Range
RC4156N	N	0°C to +70°C
RC4156M	M	0°C to +70°C
RC4156D	D	0°C to +70°C
RC4157N	N	0°C to +70°C
RC4157M	M	0°C to +70°C
RM4156D	D	-55°C to +125°C
RM4156D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
M = 14-lead plastic SOIC

Absolute Maximum Ratings

Supply Voltage ..... ±20V
Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Output Short Circuit Duration[2] ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4156/4157 ..... -55°C to +125°C
RC4156/4157 ..... 0°C to +70°C
Lead Soldering Temperature
(DIP; 60 sec) ..... +300°C
(SO-14; 10 sec) ..... +260°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit to ground on one amplifier only.

Thermal Characteristics

	14-Lead Plastic SO-14	14 Lead Plastic DIP	14 Lead Ceramic DIP
Max. Junction Temp.	+125°C	+125°C	+175°C
Max. P_D T_A<50°C	300mW	468mW	1042mW
Therm. Res θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Electrical Characteristics

(V_S = ±15V, RM = -55°C ≤ T_A ≤ +125°C, RC = 0°C ≤ T_A ≤ +70°C)

Parameters	Test Conditions	RM4156/4157			RC4156/4157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤ 10 kΩ			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				320			400	nA
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} ±10V	25			15			V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±10			±10			V
Supply Current			10			10		mA
Average Input Offset Voltage Drift			5.0			5.0		µV/°C

Linear

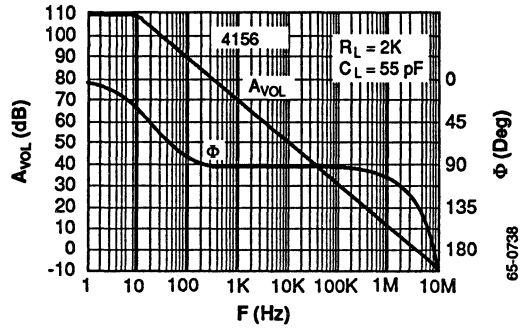
Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

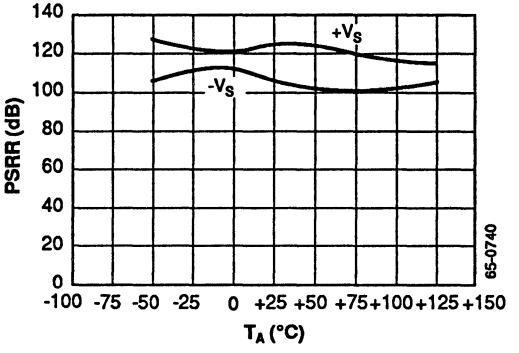
Parameters	Test Conditions	RM4156/4157			RC4156/4157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	80			80			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ	80			80			dB
Supply Current (All Amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response (4156)								
Rise Time			60			60		nS
Overshoot			25			25		%
Slew Rate		1.3	1.6		1.3	1.6		V/µS
Unity Gain Bandwidth (4156)		2.8	3.5		2.8	3.5		MHz
Phase Margin (4156)	R_L = 2 kΩ, C_L = 50 pF		50			50		%
Transient Response (4157)	A_V = -5							
Rise Time			50			50		nS
Overshoot			25			25		%
Slew Rate		6.5	8.0		6.5	8.0		V/µS
Unity Gain Bandwidth (4157)	A_V = - 5	15	19		15	19		MHz
Phase Margin (4157)	A_V = - 5 R_L = 2 kΩ, C_L = 50 pF		50			50		%
Power Bandwidth	$V_{OUT} = 20V_{P-P}$	20	25		20	25		kHz
Input Noise Voltage	F= 20 Hz to 20 kHz		1.4	2.0		1.4	2.0	μV_{RMS}
Input Noise Current	F = 20 Hz to 20 kHz		15			15		pA_{RMS}
Channel Separation			108			108		dB

Typical Performance Characteristics

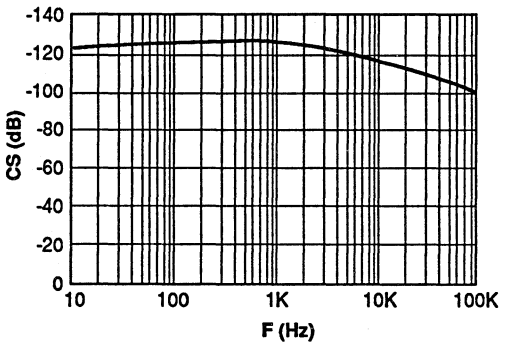
Open Loop Gain, Phase vs. Frequency

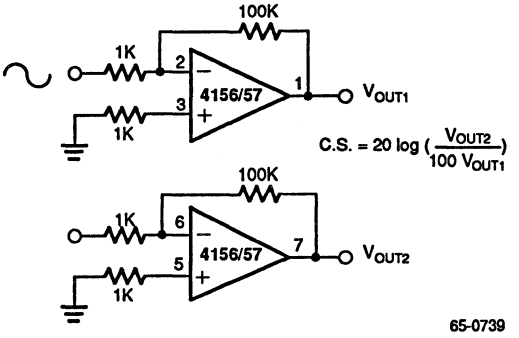


PSRR vs. Temperature

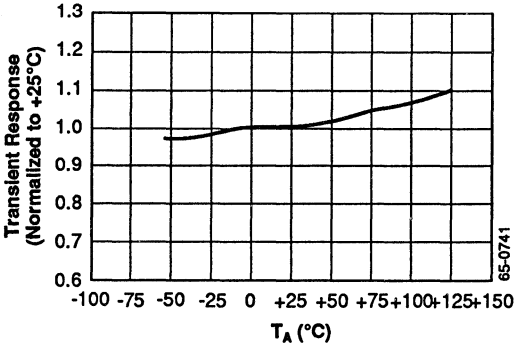


Channel Separation vs. Frequency

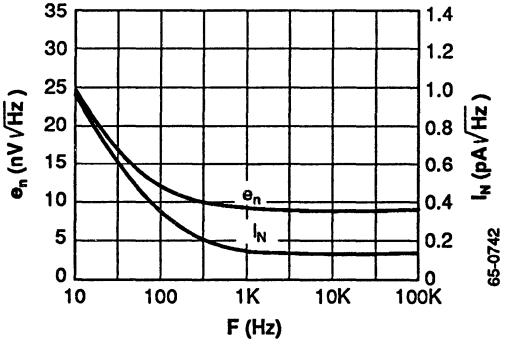




Transient Response vs. Temperature



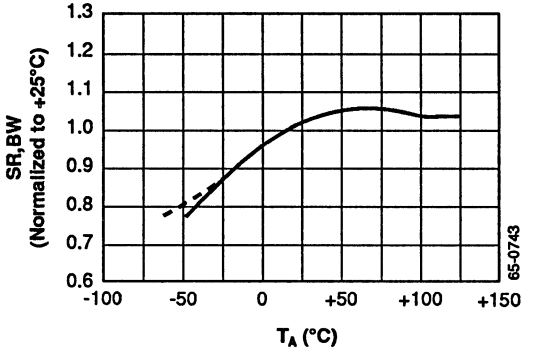
Input Noise Voltage, Current Density vs. Frequency



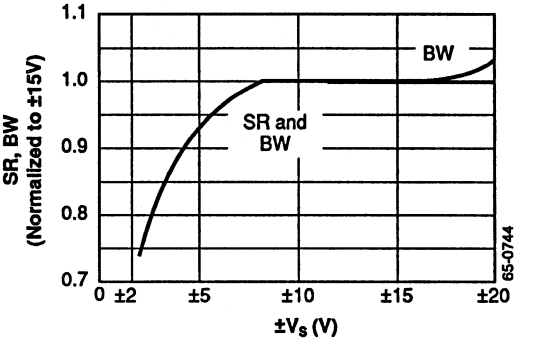
Linear

Typical Performance Characteristics (Continued)

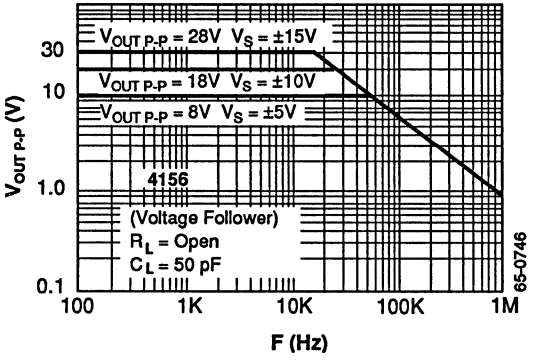
Slew Rate, Bandwidth vs. Temperature



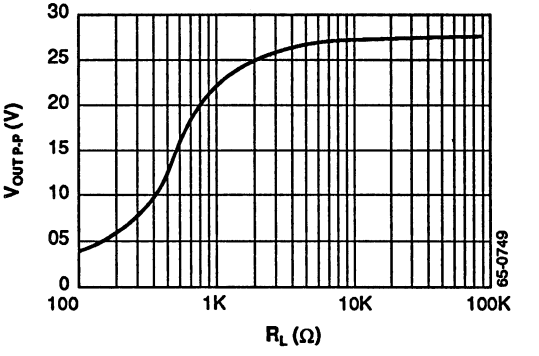
Slew Rate, Bandwidth vs. Supply Voltage



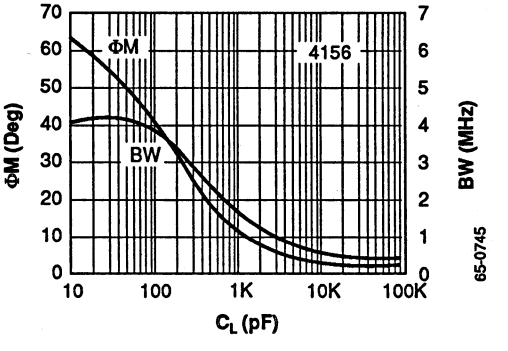
Output Voltage Swing vs. Frequency



Output Voltage Swing vs. Load Resistance

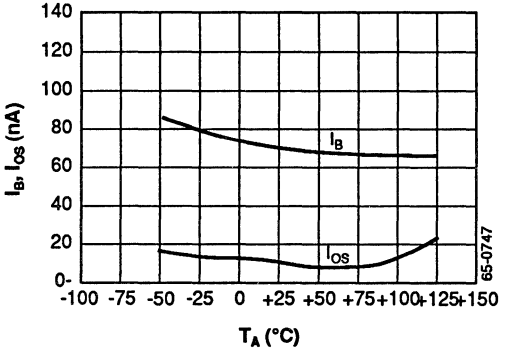


Small Signal Phase Margin, Unity Gain Bandwidth vs. Load Capacitance

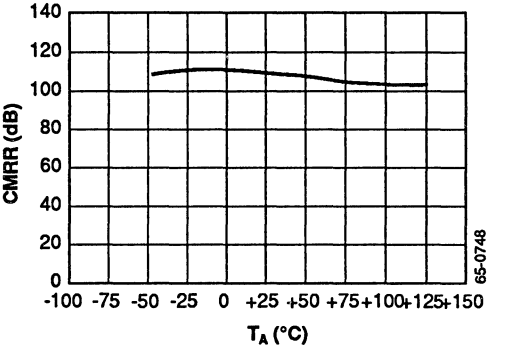


Typical Performance Characteristics (Continued)

Input Bias, Offset Current vs. Temperature



CMRR vs. Temperature



Applications

The 4156 and 4157 quad operational amplifiers can be used in almost any 741 application and will provide superior performance. The higher unity gain bandwidth and slew rate make it ideal for applications requiring good frequency response, such as active filter circuits, oscillators and audio amplifiers.

The following applications have been selected to illustrate the advantages of using the Raytheon 4156 and 4157 quad operational amplifiers.

Triangle and Square Wave Generator

The circuit of Figure 1 uses a positive feedback loop closed around a combined comparator and integrator. When power is applied the output of the comparator will switch to one of two states, to the maximum positive or maximum negative voltage. This applies a peak input signal to the integrator, and the integrator output will ramp either down or up, opposite of the input signal. When the integrator output (which is connected to the comparator input) reaches a threshold set by R1 and R2, the comparator will switch to the opposite polarity. This cycle will repeat endlessly, the integrator charging positive then negative, and the comparator switching in a square wave fashion.

The amplitude of V_2 is adjusted by varying R1. For best operation, it is recommended that R1 and V_R be set to obtain a triangle wave at V_2 with ±12V amplitude. This will then allow A3 and A4 to be used for independent adjustment of output-offset and amplitude over a wide range.

The triangle wave frequency is set by C0, R0, and the maximum output voltages of the comparator. A more symmetrical waveform can be generated by adding a back-to-back Zener diode pair as shown in Figure 2.

An asymmetric triangle wave is needed in some applications. Adding diodes as shown by the dashed lines is a way to vary the positive and negative slopes independently.

The frequency range can be very wide and the circuit will function well up to about 10 kHz. The square wave transition time at V_1 is less than 21 µS when using the 4156.

Linear

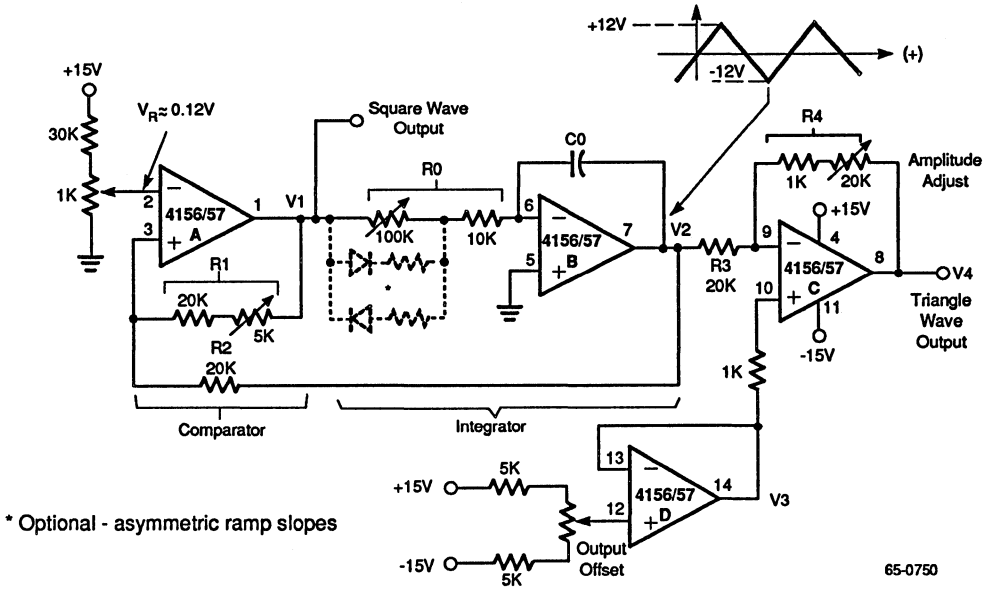


Figure 1. Triangle and Square Wave Generator

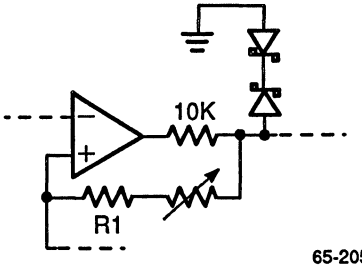
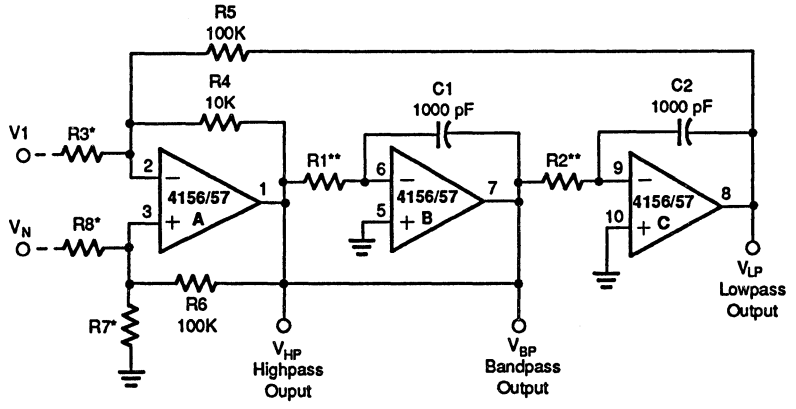


Figure 2. Triangle Generator — Symmetrical Output Option

Active Filters

The introduction of low-cost quad op amps has had a strong impact on active filter design. The complex multiple-feedback, single op amp filter circuits have been rendered obsolete for most applications. State-variable active-filter circuits using three to four op amps per section offer many advantages over the single op amp circuits. They are relatively insensitive to the passive-component tolerances and variations. The Q, gain, and natural frequency can be independently adjusted. Hybrid construction is very practical because resistor and capacitor values are relatively low and the filter parameters are determined by resistance ratios rather than by single resistors. A generalized circuit diagram of the 2-pole state-variable active filter is shown in Figure 3. The particular input connections and component-values can be calculated for specific applications. An important feature of the state-variable filter is that it can be inverting or non-inverting and can simultaneously provide three outputs: lowpass, bandpass, and highpass. A notch filter can be realized by adding one summing op amp.

The 4156 was designed and characterized for use in active filter circuits. Frequency response is fully specified with minimum values for unity-gain bandwidth, slew-rate, and full-power response. Maximum noise is specified.



* Input connections are chosen for inverting or non-inverting response. Values of R3,R7,R8 determine gain and Q.
** Values of R1 and R2 determine natural frequency. 65-0751

Figure 3. 2 - Pole State-Variable Active Filter

Output swing is excellent with no distortion or clipping. The 4156 provides full, undistorted response up to 20 kHz and is ideal for use in high-performance audio and telecommunication equipment.

In the state-variable filter circuit, one amplifier performs a summing function and the other two act as integrators. The choice of passive component values is arbitrary, but must be consistent with the amplifier operating range and input signal characteristics. The values shown for C1, C2, R4, R5 and R6 are arbitrary. Pre-selecting their values will simplify the filter tuning procedures, but other values can be used if necessary.

The generalized transfer function for the state-variable active filter is:

$$T(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}$$

Filter response is conventionally described in terms of a natural frequency ω_0 in radians/sec, and Q, the quality of the complex pole pair. The filter parameters ω_0 and Q relate to the coefficients in T(s) as:

$$\omega_0 = \sqrt{b_0} \text{ and } Q = \frac{\omega_0}{b_0}$$

The input configuration determines the polarity (inverting or non-inverting), and the output selection determines the type of filter response (lowpass, bandpass, or highpass).

Notch and all-pass configurations can be implemented by adding another summing amplifier.

Bandpass filters are of particular importance in audio and telecommunication equipment. A design approach to bandpass filters will be shown as an example of the state-variable configuration.

Design Example — Bandpass Filter

For the bandpass active filter (Figure 4) the input signal is applied through R3 to the inverting input of the summing amplifier and the output is taken from the first integrator (V_{BP}). The summing amplifier will maintain equal voltage at the inverting and non-inverting inputs (see equation on next page).

Linear

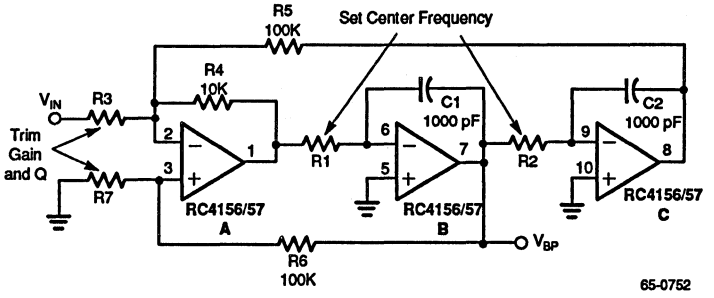


Figure 4. Bandpass Active Filter

$$\frac{\frac{R3R5}{R3+R5}}{R4+\frac{R3R5}{R3+R5}} V_{HP}(s) + \frac{\frac{R3R4}{R3+R4}}{R5+\frac{R3R4}{R3+R4}} V_{LP}(s) + \frac{\frac{R4R5}{R4+R5}}{R3+\frac{R4R5}{R4+R5}} V_{IN}(s) + \frac{R7}{R6+R7} V_{BP}(s)$$

These equations can be combined to obtain the transfer function:

$$V_{BP}(s) = -\frac{1}{R1C1S} V_{HP}(s) \text{ and } V_{LP}(s) = -\frac{1}{R2C2S} V_{BP}(s)$$

$$\frac{V_{BP}(s)}{V_{IN}(s)} = \frac{\frac{R4}{R3}\ \frac{1}{R1C1}\ S}{S^2 + \frac{R7}{R6+R7}\left(1+\frac{R4}{R5}+\frac{R4}{R3}\right)\left(\frac{1}{R1C1}\right)S + \left(\frac{R4}{R5}\right)\left(\frac{1}{R1C1R2C2}\right)}$$

Defining 1/R1C1 as ω_1, 1/R2C2 as ω_2, and substituting in the assigned values for R4, R5, and R6, then the transfer function simplifies to:

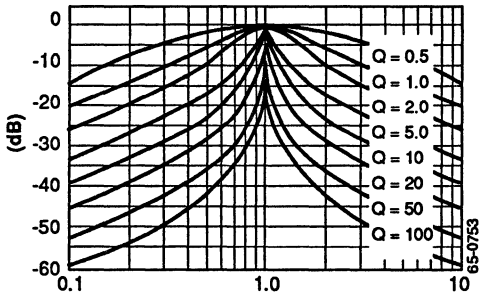
$$\frac{V_{BP}(s)}{V_{IN}(s)} = \frac{\frac{10^4}{R3}\ \omega_1 S}{S^2 + \left[\frac{1.1+\frac{10^4}{R3}}{1+\frac{10^5}{R7}}\right]\omega_1 S + \frac{1}{\omega_1\omega_2}}$$

This is now in a convenient form to look at the center-frequency ω_0 and filter Q.

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2} \qquad \text{and } Q = \left[\frac{1+\frac{10^5}{R7}}{1.1+\frac{10^4}{R3}}\right]\omega_0$$

$$\omega_0 = 10^{-9}\sqrt{0.1\,R1R2}$$

The frequency response for various values of Q are shown in Figure 5.



$$\frac{V_{BP}}{V_{IN}} = \frac{\frac{\omega}{\omega_o}\frac{1}{Q}}{\sqrt{\left[1-\left(\frac{\omega}{\omega_o}\right)^2\right]^2 + \left(\frac{1}{Q}\frac{\omega}{\omega_o}\right)^2}}$$

Figure 5. Bandpass Transfer Characteristics Normalized for Unity Gain and Frequency

These equations suggest a tuning sequence where ω is first trimmed via R1 or R2, then Q is trimmed by varying R7 and/or R3. An important advantage of the state-variable bandpass filter is that Q can be varied without affecting center frequency ω_0.

This analysis has assumed ideal op amps operating within their linear range, which is a valid design approach for a reasonable range of ω_0 and Q. At extremes of ω_0 and at high values of Q, the op amp parameters become significant. A rigorous analysis is very complex, but some factors are particularly important in designing active filters.

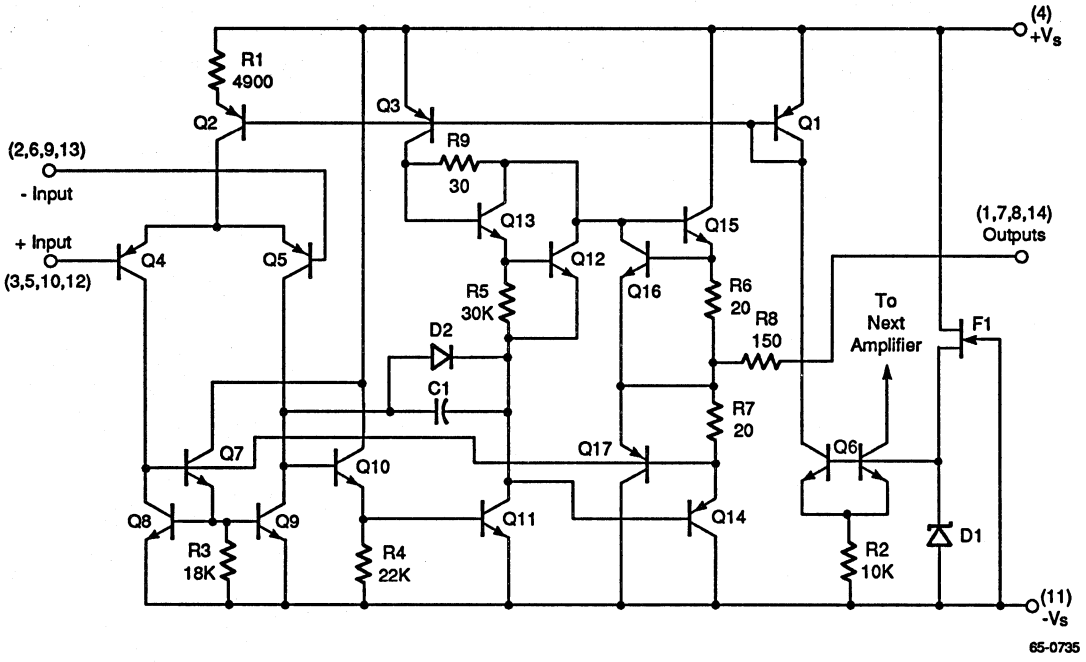
1. The passive component values should be chosen such that all op amps are operating within their linear region for the anticipated range of input signals. Slew rate, output current rating, and common-mode input range must be considered. For the integrators, the current through the feedback capacitor (I = C dV/dt) should be included in the output current computations.

2. From the equation for Q, it should seem that infinite Q could be obtained by making R7 zero. But as R7 is made small, the Q becomes limited by the op amp gain at the frequency of interest. The effective closed-loop gain is being increased directly as R7 is made smaller, and the ratio of open-loop gain to closed-loop gain is becoming less. The gain and phase error of the filter at high Q is very dependent on the op amp open-loop gain at ω_0.

3. The attenuation at extremes of frequency is limited by the op amp gain and unity-gain bandwidth. For integrators, the finite open-loop op amp gain limits the accuracy at the low-end. The open-loop roll-off of gain limits the filter attenuation at high frequency.

The 4156 quad operational amplifier has much better frequency response than a conventional 741 circuit and is ideal for active filter use. Natural frequencies of up to 10 kHz are readily achieved and up to 20 kHz is practical for some configurations. Q can range up to 50 with very good accuracy and up to 500 with reasonable response. The extra gain of the 4156 at high frequencies gives the quad op amp an extra margin of performance in active-filter circuits.

Schematic Diagram (1/4 Shown)



RC4558
Dual High-Gain Operational Amplifier

Description

The 4558 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon IC using an advanced epitaxial process.

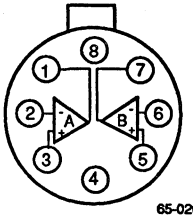
Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of this dual device in dense single 741 operational amplifier applications. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

Features

- 2.5 MHz unity gain bandwidth
- Supply voltage ±22V for RM4558 and ±18V for RC/RV4558
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

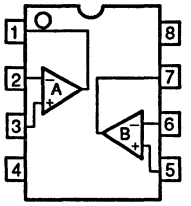
Connection Information

8-Lead TO-99 Metal Can
(Top View)



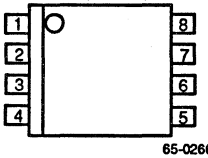
65-0209

8-Lead Dual In-Line Package
(Top View)



65-0210

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666

Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$-V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	$+V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
RC4558M	M	0°C to +70°C
RC4558N	N	0°C to +70°C
RM4558D	D	-55°C to +125°C
RM4558D/883B	D	-55°C to +125°C
RM4558T	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC

Absolute Maximum Ratings

Supply Voltage
- RM4558 ..... ±22V
- RC4558 ..... ±18V

Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Operating Temperature Range
- RM4558 ..... -55°C to +125°C
- RC4558 ..... 0°C to +70°C

Lead Soldering Temperature
- (SO-8; 10 sec) ..... +260°C

Lead Soldering Temperature
- (DIP, TO-99; 60 sec) ..... +300°C

Notes:
1. For supply voltages less than -15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one op amp only. Rating applies to +75°C ambient temperature.

Thermal Characteristics

	8-Lead Small Outline	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	+125°C	+125°C	+175°C	+175°C
Max. P_D T_A <50°C	300 mW	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	240°C/W	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	4.17 mW/°C	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Matching Characteristics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	RM/RC4558 Typ	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current	$R_L \geq 2$ kΩ	±15	nA
Input Offset Current	$R_L \geq 2$ kΩ	±7.5	nA

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

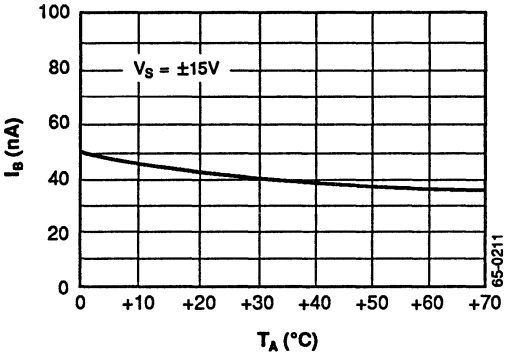
Parameters	Test Conditions	RM4558			RC4558			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		76	100		dB
Power Consumption	R_L = ∞		100	170		100	170	mW
Transient Response	V_{IN} = 20 mV							
Rise Time	R_L = 2kΩ		0.3			0.3		µS
Overshoot	$C_L \leq 100pF$		35			35		%
Slew Rate	$R_L \geq 2k\Omega$		0.8			0.8		V/µS
Channel Separation	F = 10kHz, R_S = 1kΩ		90			90		dB
Unity Gain Bandwidth (Gain = 1)		2.5	3.0		2.0	3.0		MHz

The following specifications apply for RM = -55°C ≤ T_A ≤ +125°C, RC = 0° ≤ T_A ≤ +70°C

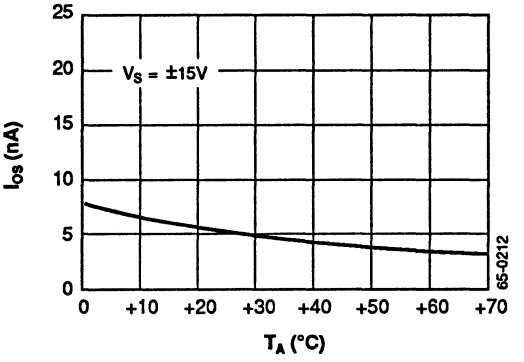
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current RC4558				500			300	nA
Input bias Current RC4558				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption	R_L = ∞		120	200		120	200	mW

Typical Performance Characteristics

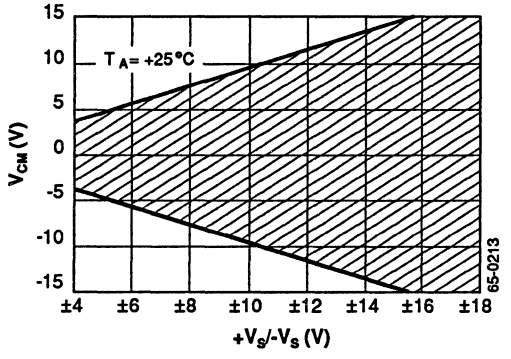
Input Bias Current vs. Temperature



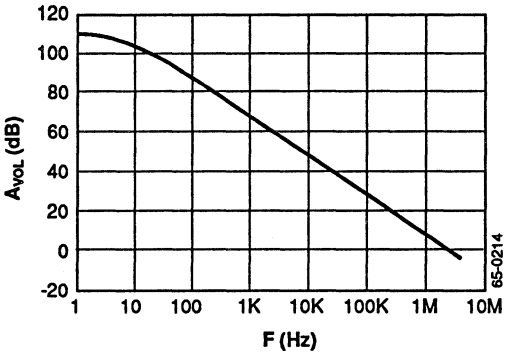
Input Offset Current vs. Temperature



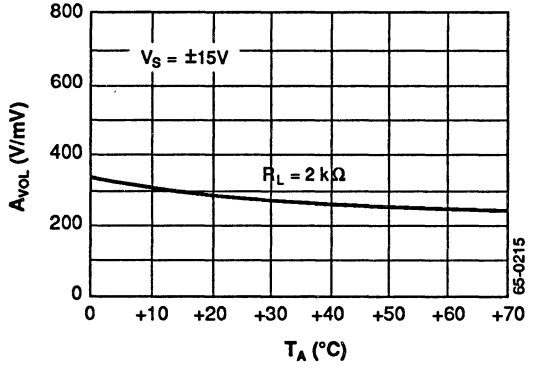
Input Common Mode Voltage Range vs. Supply Voltage



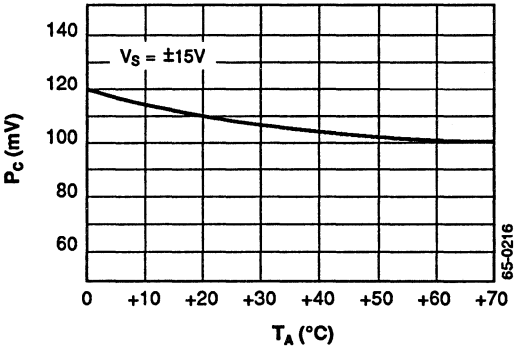
Open Loop Voltage Gain vs. Frequency



Open Loop Voltage Gain vs. Temperature



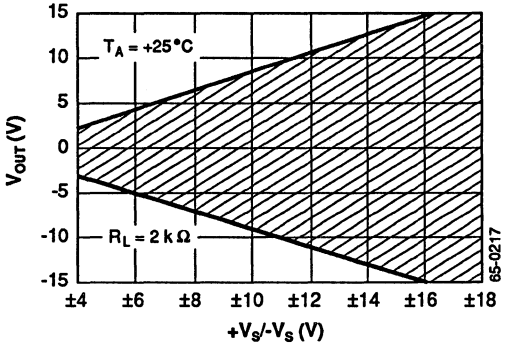
Power Consumption vs. Temperature



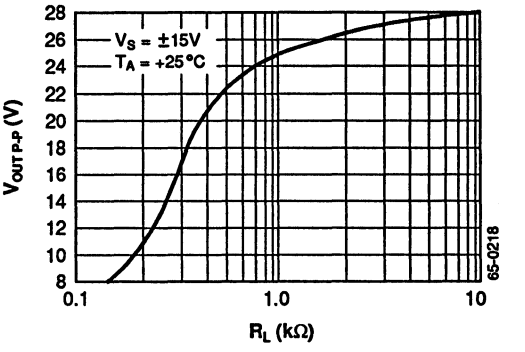
Linear

Typical Performance Characteristics (Continued)

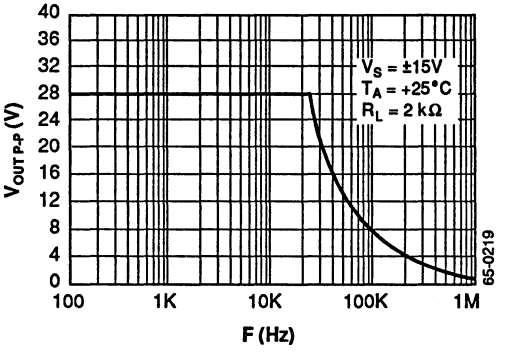
Output Voltage Swing vs. Supply Voltage



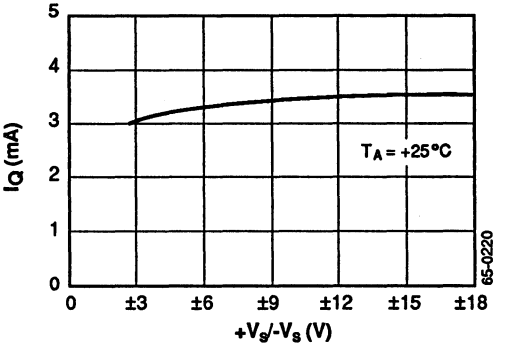
Output Voltage Swing vs. Load Resistance



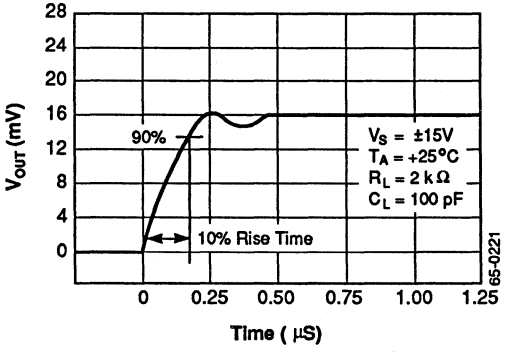
Output Voltage Swing vs. Frequency



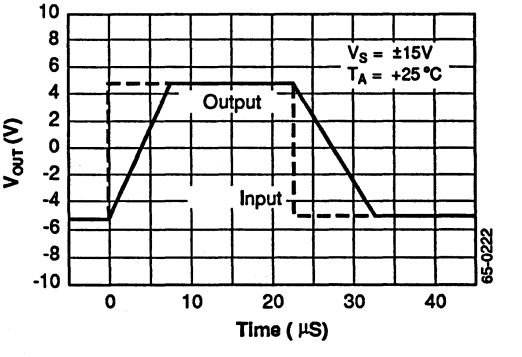
Quiescent Current vs. Supply Voltage



Transient Response
Output Voltage vs. Time

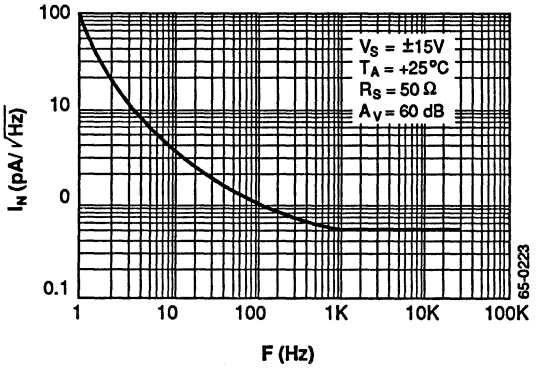


Follower Large Signal Pulse Response
Output Voltage vs. Time

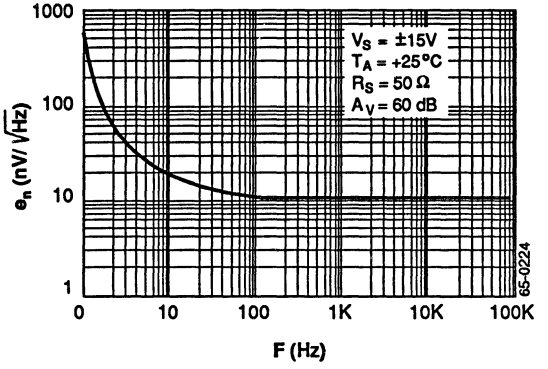


Typical Performance Characteristics (Continued)

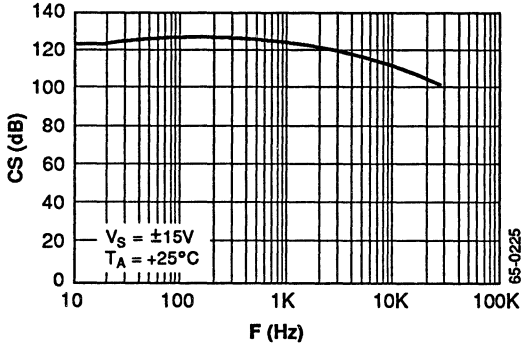
Input Noise Current Density vs. Frequency



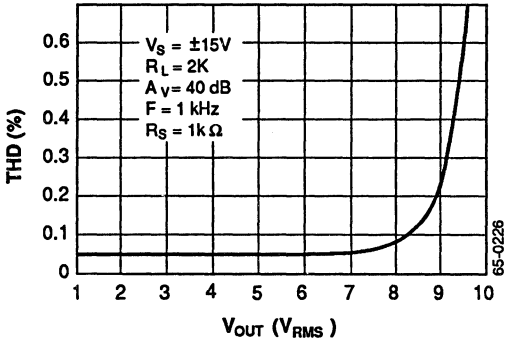
Input Noise Voltage Density vs. Frequency



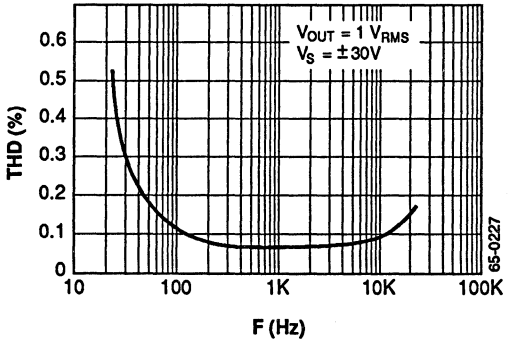
Channel Separation vs. Frequency



Total Harmonic Distortion vs. Output Voltage



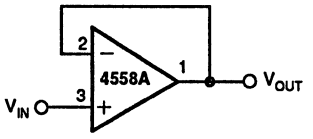
Distortion vs. Frequency



Linear

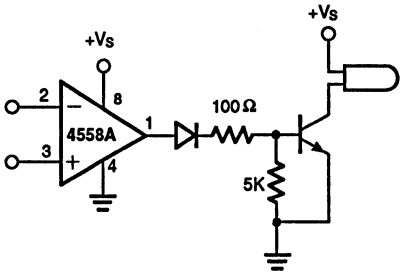
Typical Applications

Voltage Follower



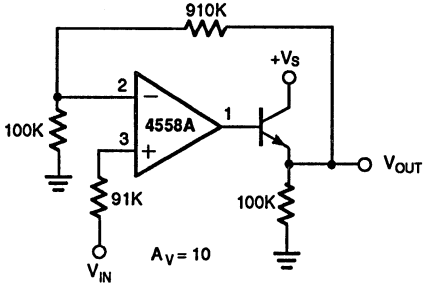
65-0228

Lamp Driver



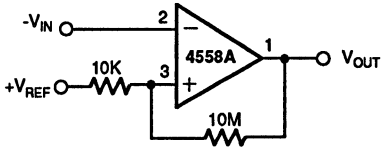
65-0229

Power Amplifier



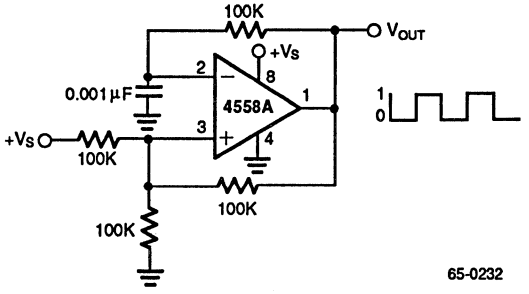
65-0230

Comparator With Hysteresis



65-0231

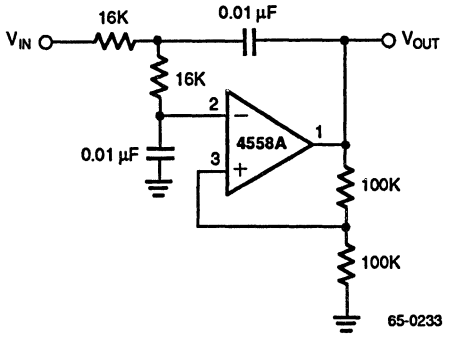
Squarewave Oscillator



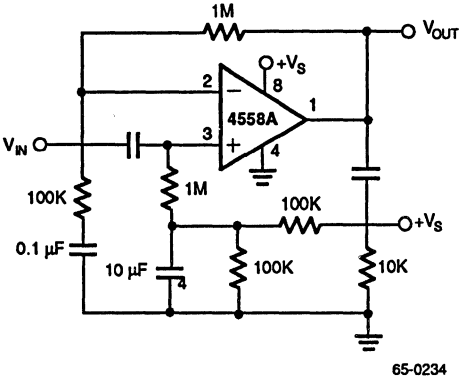
65-0232

Typical Applications (Continued)

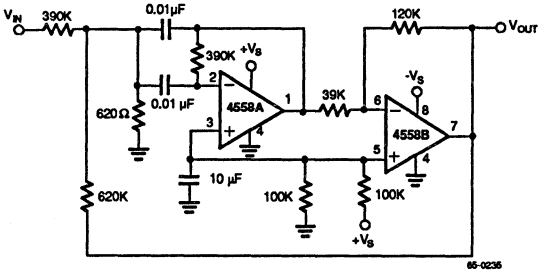
DC Coupled 1kHz Low-Pass Active Filter



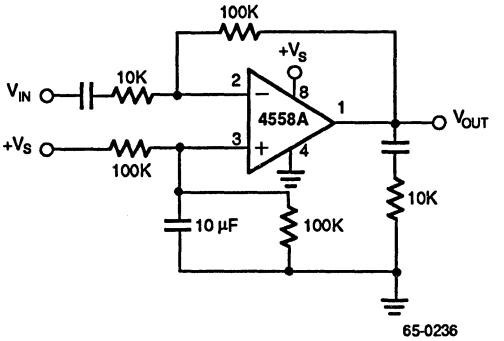
AC Coupled Non-Inverting Amplifier



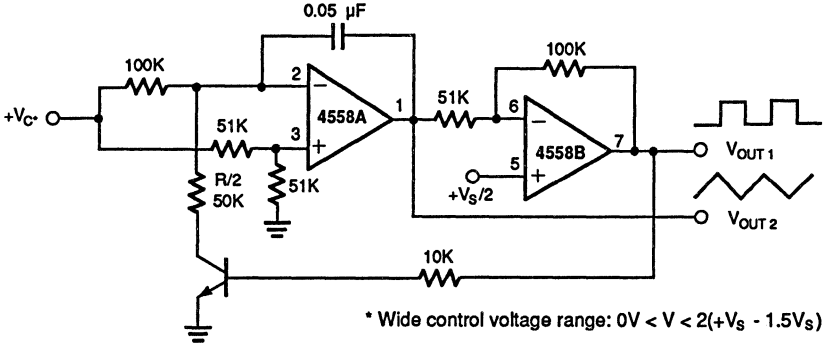
1kHz Bandpass Active Filter



AC Coupled Inverting Amplifier

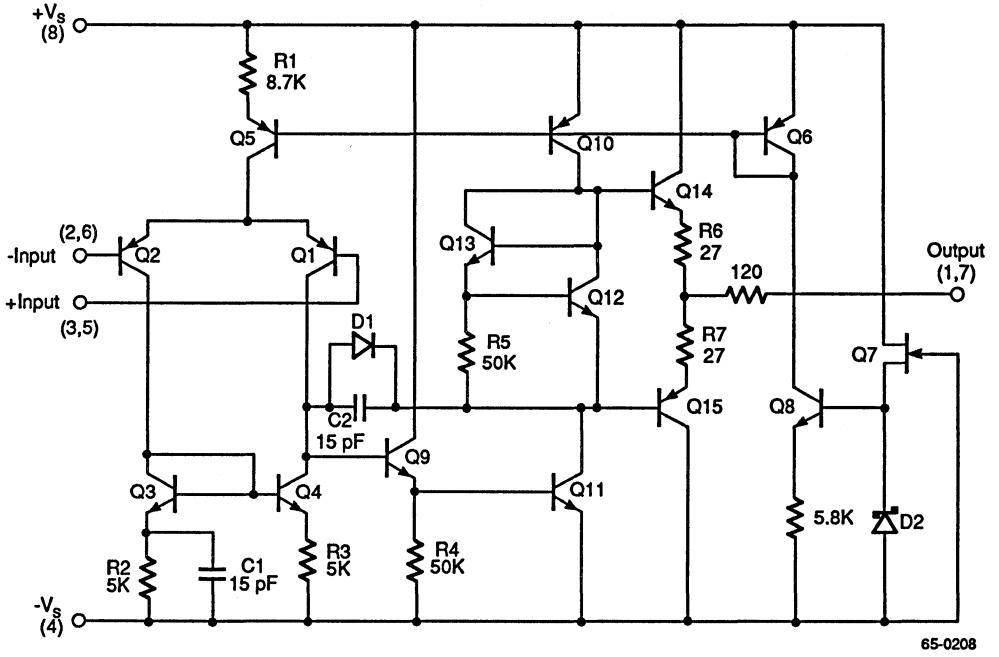


Voltage Controlled Oscillator (VCO)



Linear

Schematic Diagram



RC4559
High-Gain Dual Operational Amplifier

Description

The 4559 integrated circuit is a high performance dual operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

These amplifiers feature guaranteed AC performance which far exceeds that of the 741-type amplifiers. The specially designed low-noise input transistors allow the 4559 to be used in low-noise signal processing applications such as audio preamplifiers and signal conditioners.

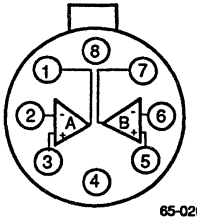
The 4559 also has more output drive capability than 741-type amplifiers and can be used to drive a 600Ω load.

Features

- Unity gain bandwidth — 4.0 MHz
- Slew rate — 2.0 V/μS
- Low noise voltage — 1.4 μV_{RMS}
- Supply voltage — ±22V for RM4559 and ±18V for RC/RV4559
- No frequency compensation required
- No latch up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

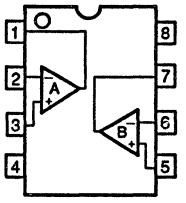
Connection Information

8-Lead TO-99 Metal Can
(Top View)



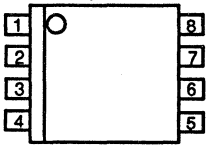
65-0209

8-Lead Dual In-Line Package
(Top View)



65-0210

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02668

Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$-V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	$+V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
RC4559M	M	0°C to +70°C
RC4559N	N	0°C to +70°C
RC4559D	D	0°C to +70°C
RM4559D	D	-55°C to +125°C
RM4559D/883B	D	-55°C to +125°C
RM4559T	T	-55°C to +125°C
RM4559T/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC

Absolute Maximum Ratings

Supply Voltage
- RM4559 ..... ±22V
- RC4559 ..... ±18V

Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Operating Temperature Range
- RM4559 ..... -55°C to +125°C
- RC4559 ..... 0°C to +70°C

Lead Soldering Temperature
- (SO-8; 10 sec) ..... +260°C

Lead Soldering Temperature
- (DIP, TO-99; 60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one op amp only. Rating applies to +75°C ambient temperature.

Thermal Characteristics

	8-Lead Small Outline	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	+125°C	+125°C	+175°C	+175°C
Max. P_D T_A<50°C	300 mW	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	240°C/W	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	4.17 mW/°C	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Matching Characteristics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	RM/RC4559 Typ	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

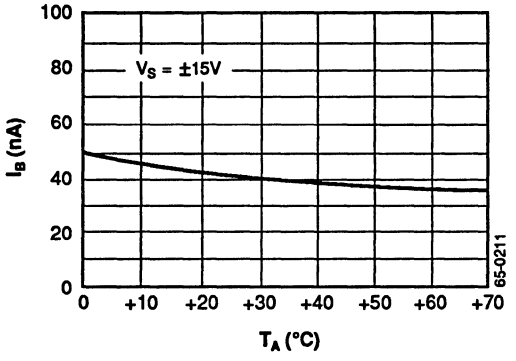
Parameters	Test Conditions	RM4559 Min	RM4559 Typ	RM4559 Max	/RC4559 Min	/RC4559 Typ	/RC4559 Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	100		5.0	100	nA
Input Bias Current			40	250		40	250	nA
Input Resistance (Differential Mode)		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
	$R_L \geq 600\Omega$	±9.5	±10		±9.5	±10		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	100		80	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	82	100		82	100		dB
Supply Current	$R_L = \infty$		3.3	5.6		3.3	5.6	mA
Transient Response	V_{IN} = 20mV							
Rise Time	R_L = 2kΩ		80			80		nS
Overshoot	$C_L \leq 100pF$		35			35		%
Slew Rate		1.5	2.0		1.5	2.0		V/μS
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Power Bandwidth	$V_{OUT} = 20V_{p-p}$	24	32		24	32		kHz
Input Noise Voltage	F= 20Hz to 20kHz		1.4	2.0		1.4	2.0	μV_{RMS}
Input Noise Current	F= 20Hz to 20kHz		25			25		pA_{RMS}
Channel Separation	Gain = 100, F= 10kHz R_S = 1kΩ		90			90		dB

The following specifications apply for RM = -55°C ≤ T_A ≤ + 125°C, RC = 0°C ≤ T_A ≤ +70°C RM4559/RC4559

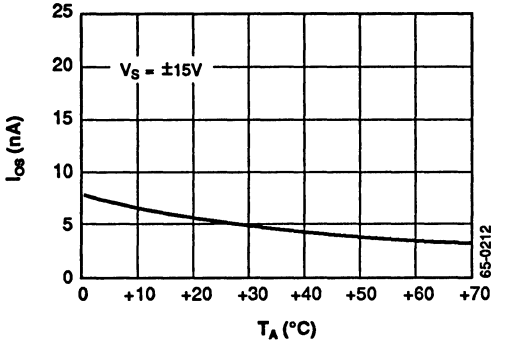
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				300			200	nA
Input Bias Current				500			500	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Supply Current	$R_L = \infty$		4.0	6.6		4.0	6.6	mA

Typical Performance Characteristics

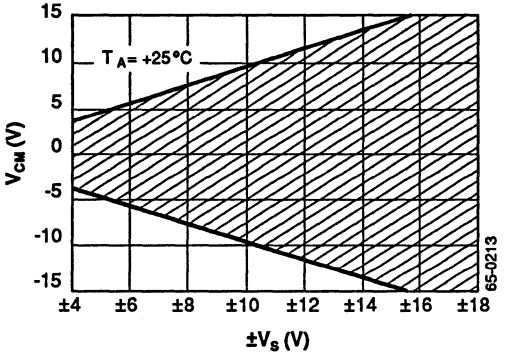
Input Bias Current vs. Temperature



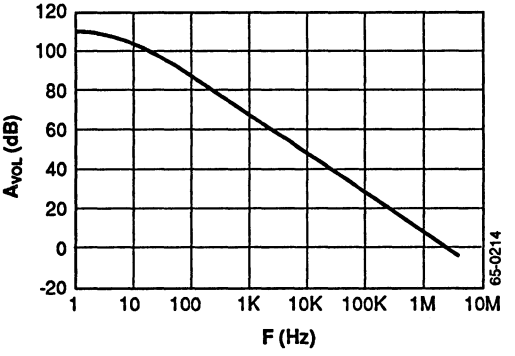
Input Offset Current vs. Temperature



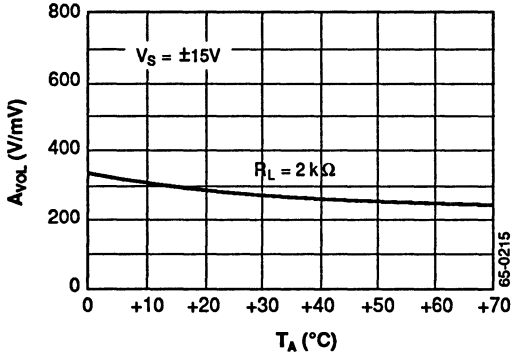
Input Common Mode Voltage Range vs. Supply Voltage



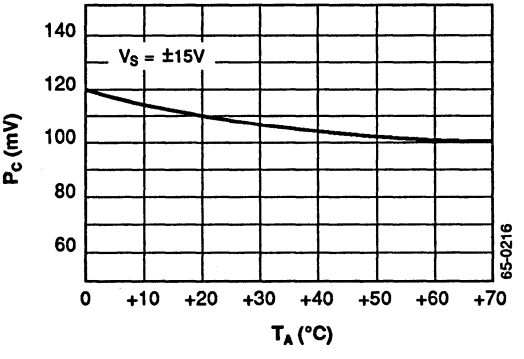
Open Loop Voltage Gain vs. Frequency



Open Loop Voltage Gain vs. Temperature



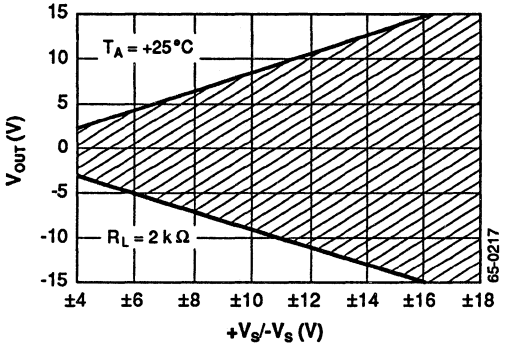
Power Consumption vs. Temperature



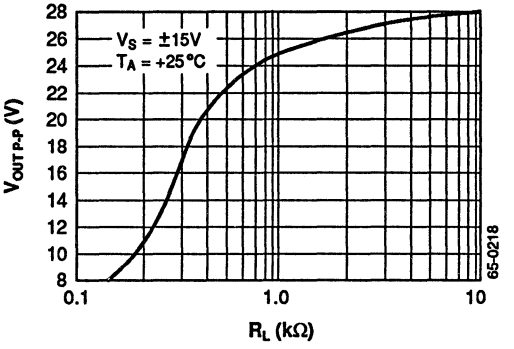
Linear

Typical Performance Characteristics (Continued)

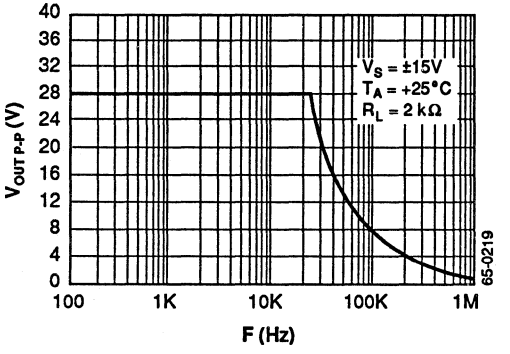
Output Voltage Swing vs. Supply Voltage



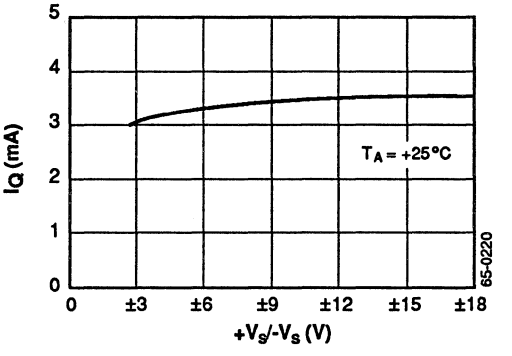
Output Voltage Swing vs. Load Resistance



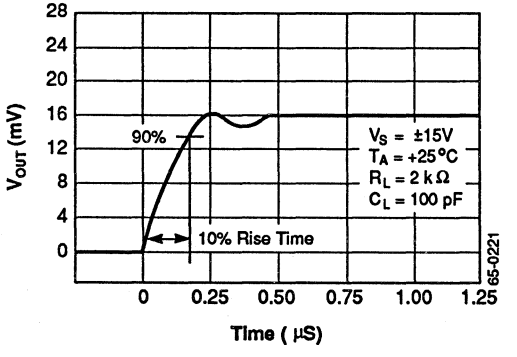
Output Voltage Swing vs. Frequency



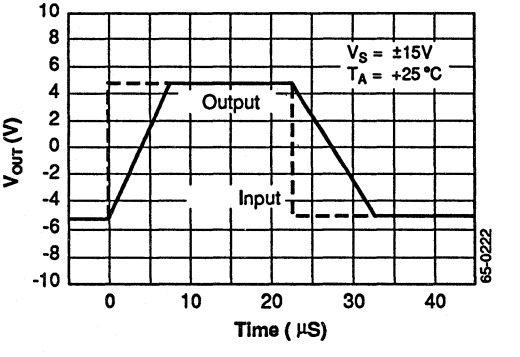
Quiescent Current vs. Supply Voltage



Transient Response
Output Voltage vs. Time

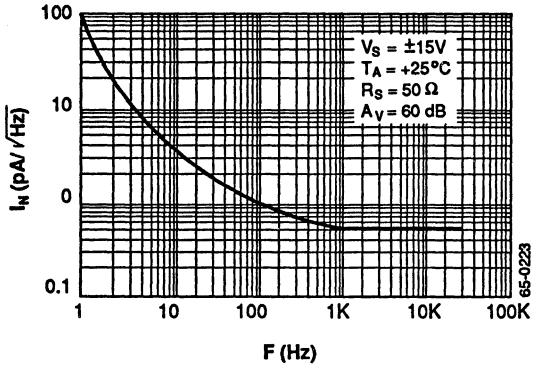


Follower Large Signal Pulse Response
Output Voltage vs. Time

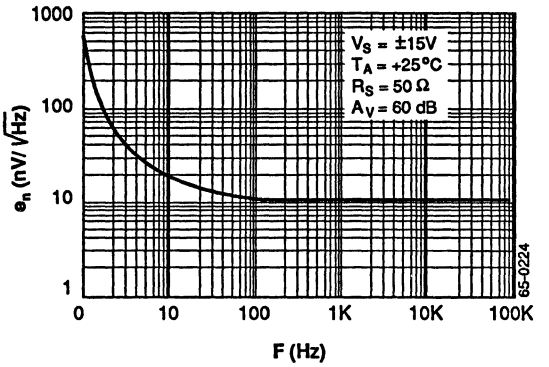


Typical Performance Characteristics (Continued)

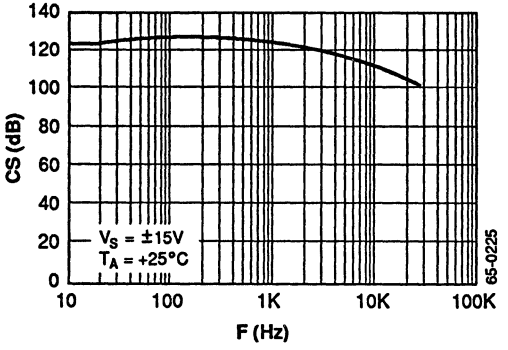
Input Noise Current Density vs. Frequency



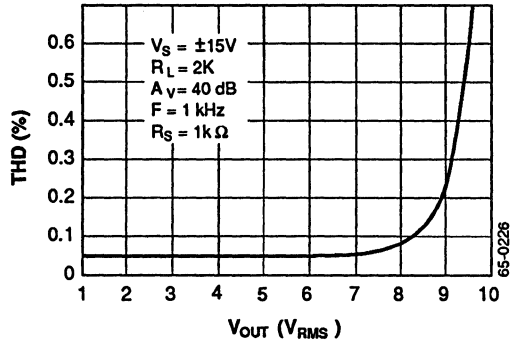
Input Noise Voltage Density vs. Frequency



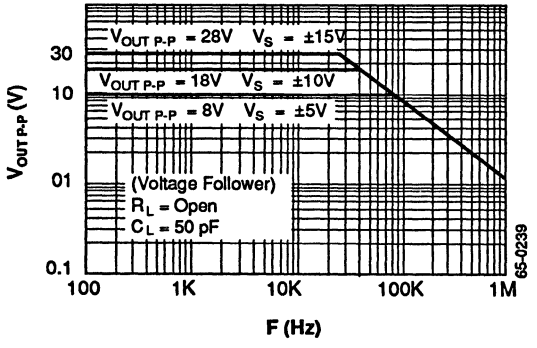
Channel Separation vs. Frequency



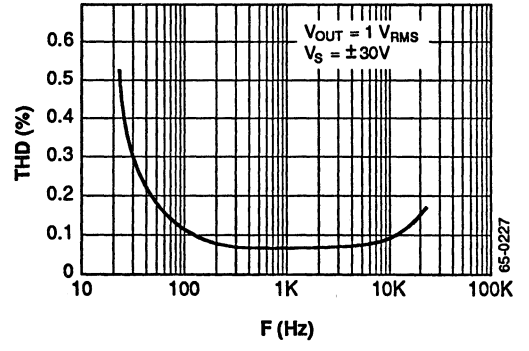
Total Harmonic Distortion vs. Output Voltage



Output Voltage Swing vs. Frequency



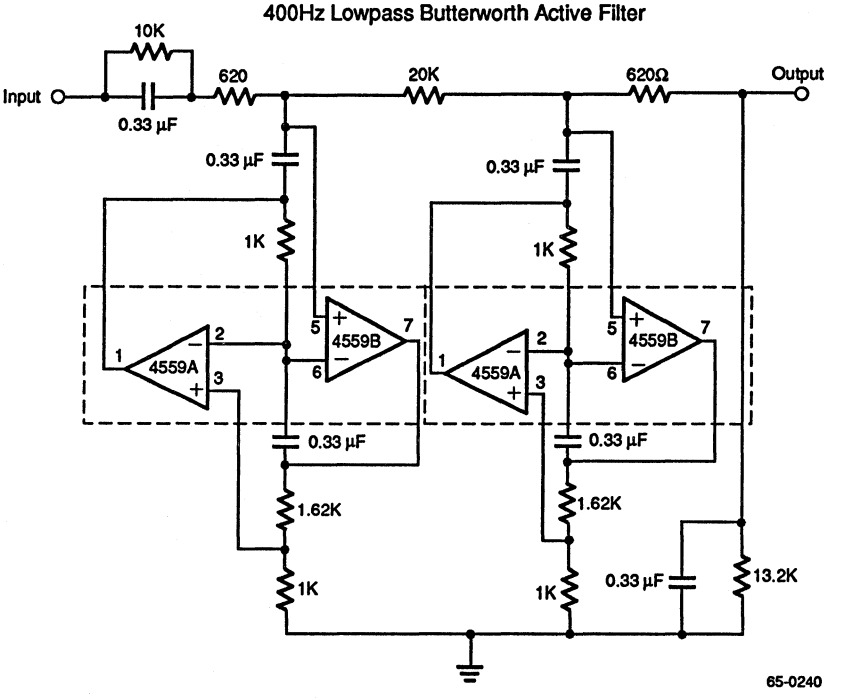
Total Harmonic Distortion vs. Frequency



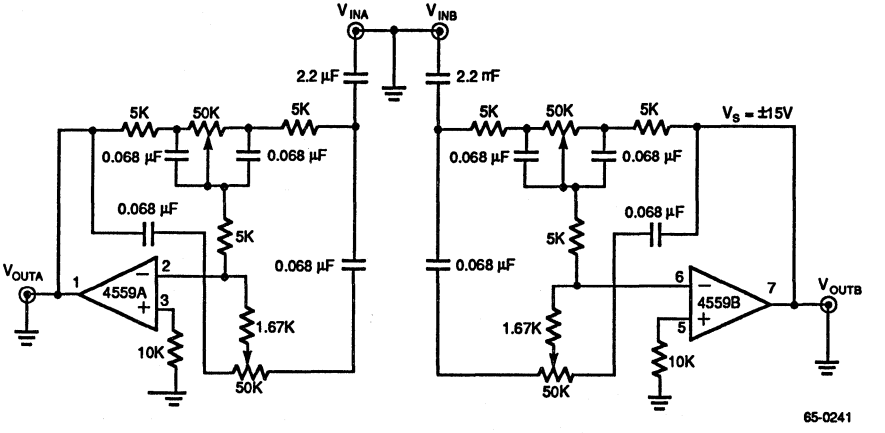
Linear

Typical Applications

400Hz Lowpass Butterworth Active Filter

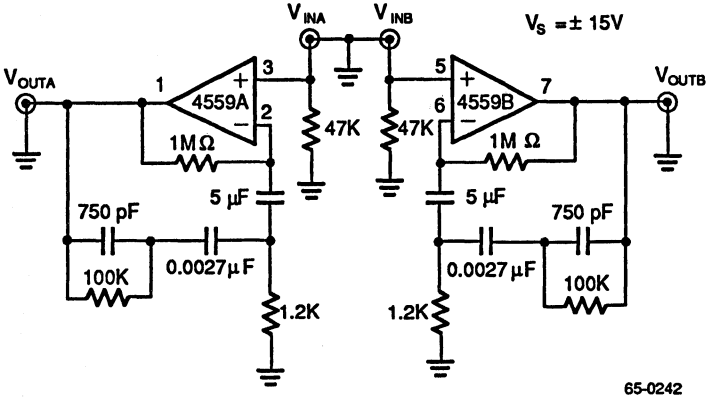


Stereo Tone Control

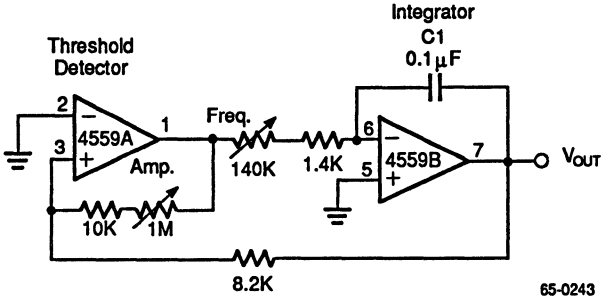


Typical Applications (Continued)

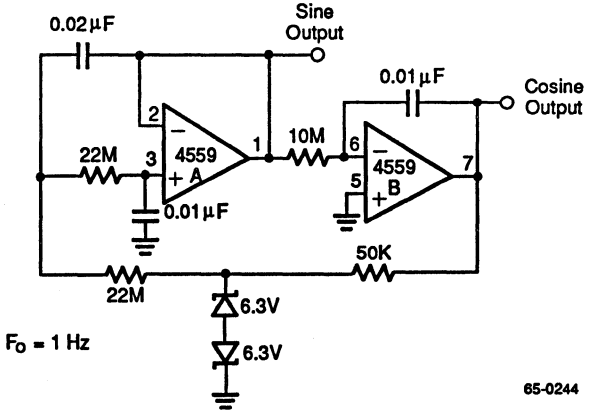
RIAA Preamplifier



Triangular-Wave Generator

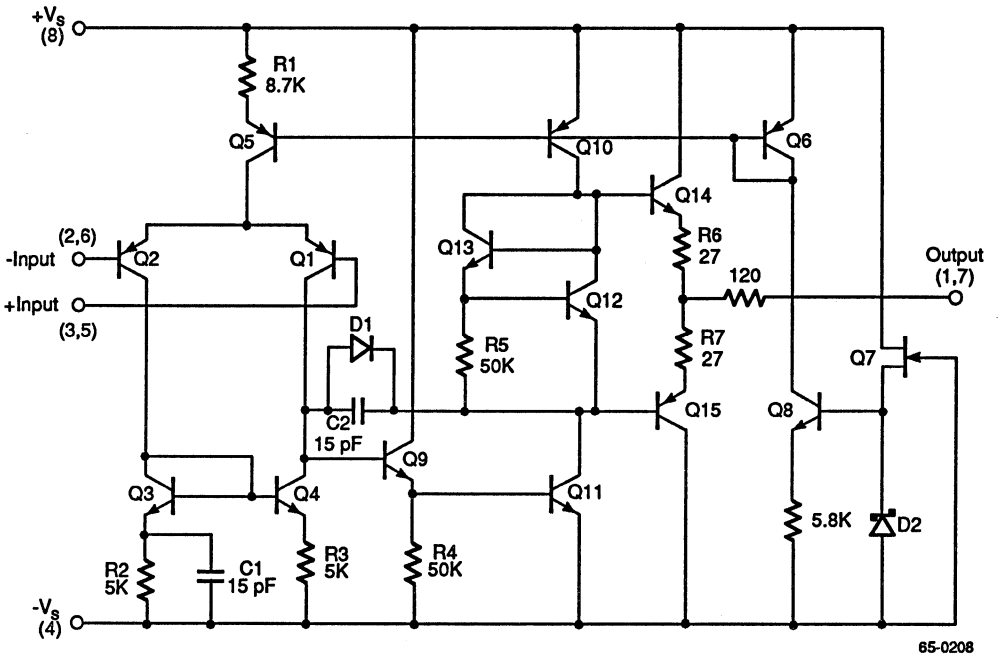


Low Frequency Sine Wave Generator with Quadrature Output



Linear

Schematic Diagram



RC4207
Precision Dual Operational Amplifier

Description

Designed for low level signal conditioning and instrumentation applications, the 4207 is a precision dual amplifier combining excellent DC input specifications with low input noise characteristics. Ultra low input offset voltage, low drift, high CMRR, and low input bias currents serve to reduce input related errors to less than 0.01% in a typical high gain instrumentation amplifier system (A_V = 1000). The 4207 contains two separate amplifiers with a high degree of isolation between them; each is complete requiring no external compensation capacitors or offset nulling potentiometers. The inherent V_{OS} is typically less than 150 µV, resulting in superior temperature drift, and this low initial offset is further reduced by "Zener-zap" nulling when the wafers are tested.

Advanced thin film and nitride dielectric processing allows the 4207 to achieve its high performance and small size (the 4207 is offered in 8-lead DIPs). The 4207 fits the industry standard 8-lead op amp pin-out.

Features

- Low Noise — 0.35 µVp-p (0.1 Hz to 10 Hz)
- Ultra-low V_{os} — 75 µV
- Ultra-low V_{os} drift — 1.3 µV/°C
- Long term V_{os} stability — 0.2 µV/Mo
- Low input bias and offset currents — ±5 nA
- High gain — 400 V/mV
- Fits 4558 socket
- Industry standard pinout
- 8-lead mini-DIP

Ordering Information

Part Number	Package	Operating Temperature Range
RC4207FN	N	0°C to +70°C
RC4207GN	N	0°C to +70°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Input Voltage[1] ..... ±18V
Differential Input Voltage 30V
Internal Power Dissipation[2] ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range RC4207F/G ..... 0°C to +70°C
Lead Soldering Temperature (60 sec) ..... +300°C

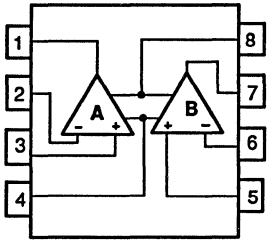
Notes:
1. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Plastic DIP
Max. Junction Temp.	+125°C
Max. P_D T_A <50°C	468 mW
Therm. Res. θ_{JC}	—
Therm. Tes. θ_{JA}	160°C/W
For T_A > 50°C derate at	6.25 mW/°C

Connection Information

8-Lead
Dual In-Line Package
(Top View)



65-01782

Pin	Function
1	Output A
2	-Input A
3	+Input A
4	$-V_S$
5	+Input B
6	-Input B
7	Output B
8	$+V_S$

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	4207F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	µV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.7		µV/°C
Input Offset Current			±2.0	±10		±1.6	±15	nA
Average Input Offset Current Drift			8.0			12		pA/°C
Input Bias Current			±2.0	±10		±3.0	±15	nA
Average Input Bias Current Drift			13			18		pA/°C
Input Voltage Range		±10	±13.5		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	94	120		92	106		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	94	115		92	100		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	200	450		75	400		V/mV
Maximum Output Voltage Swing	R_L > 2.0kΩ	±11	±12.6		±11	±12.6		V
Power Consumption	R_L = ∞		150	240		150	240	mW

Electrical Characteristics

(V_S = ±15V, and T_A = +25°C unless otherwise noted)

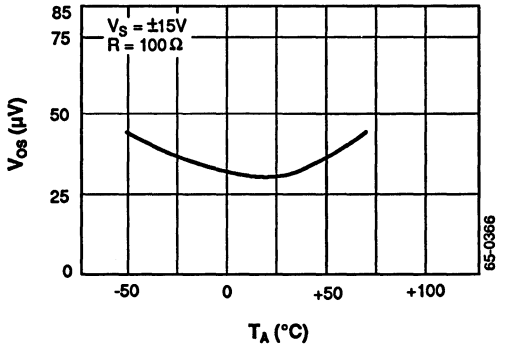
Parameters	Test Conditions	4207B/F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			30	75		60	150	µV
Long Term V_{OS} Stability[1]			0.2			0.5		µV/Mo
Input Offset Current			±0.5	±5		±2	±10	nA
Input Bias Current			±0.5	±5		±2	±10	nA
Input noise Voltage	0.1 Hz to 10 Hz		0.35			0.35		µVp-p
Input Noise Voltage Density	F_O = 10 Hz		10.3			10.3		nV/√Hz
	F_O = 100 Hz		10			10		
	F_O = 1000 Hz		9.6			9.6		
Input Noise Current	0.1 Hz to 10 Hz		14			14		pAp-p
Input Noise Current Density	F_O = 10 Hz		0.32			0.32		pA/√Hz
	F_O = 100 Hz		0.14			0.14		
	F_O = 1000 Hz		0.12			0.12		
Input Resistance (Diff. Mode)			60			31		MΩ
Input Resistance (Com. Mode)			200			120		GΩ
Input Voltage Range[4]		±11	±14		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	100	126		94	110		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	110		94	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	400	600		250	400		V/mV
	V_{OUT} = ±1.0V, RL = 1KΩ, V_S = ±4.0V	200	400		100	200		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		0.1	0.3		V/µs
Closed Loop Bandwidth	A_{VOL} = +1.0		1.5			1.5		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		150	200		160	240	mW
	V_S = ±4.0V, R_L = ∞		35	50		48	64	
Crosstalk		126	155		126	155		dB

Notes:

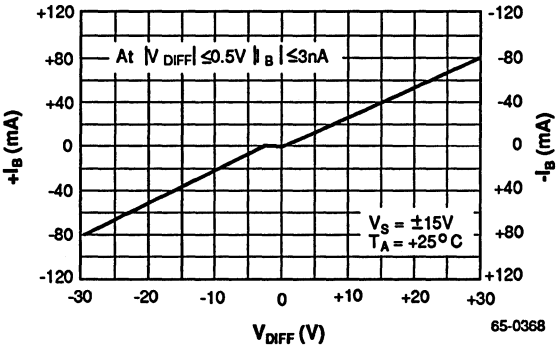
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Typical Performance Characteristics

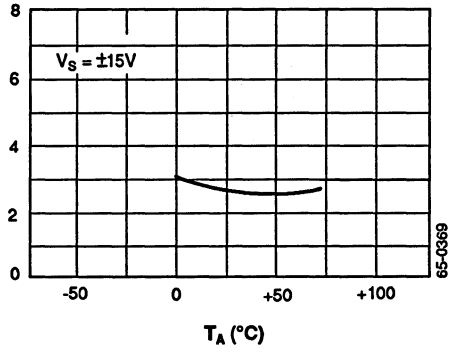
Input Offset Voltage vs. Temperature



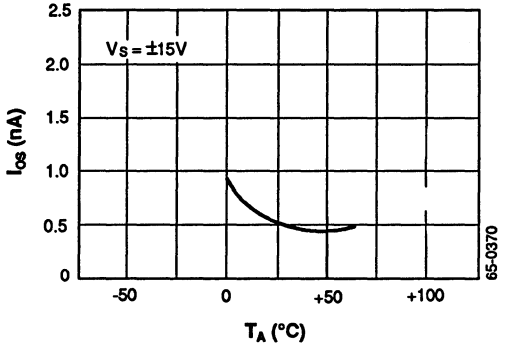
Input Bias Current vs. Differential Input Voltage



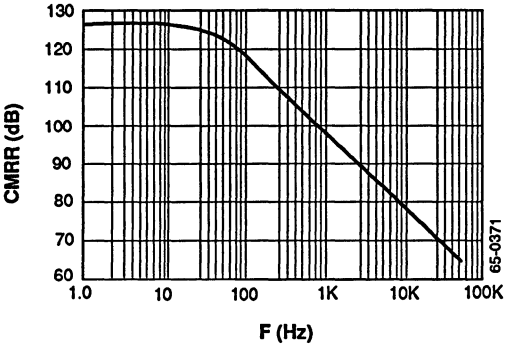
Input Bias Current vs. Temperature



Input Offset Current vs. Temperature



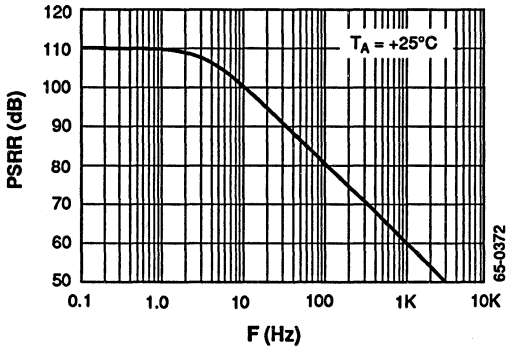
CMRR vs. Frequency



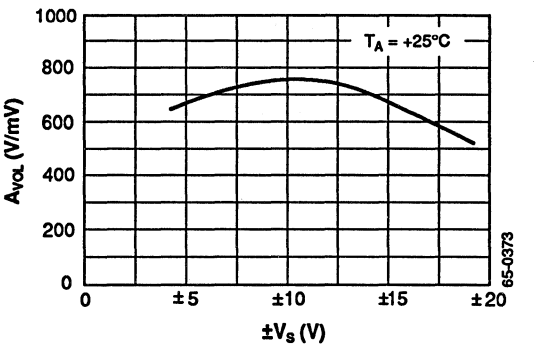
Linear

Typical Performance Characteristics

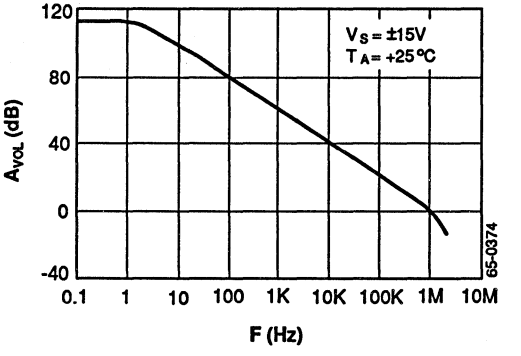
PSRR vs. Frequency



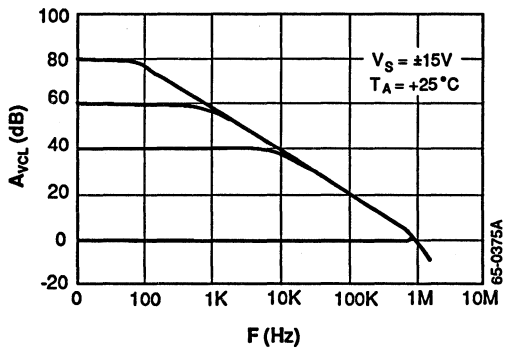
Open Loop Gain vs. Supply Voltage



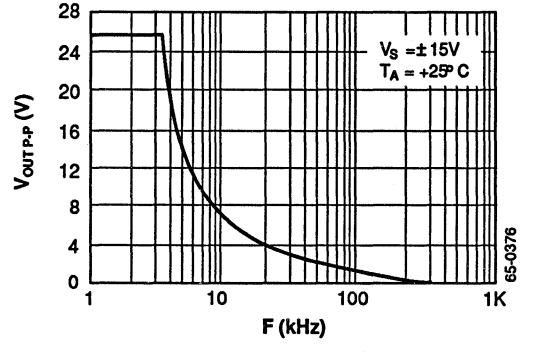
Open Loop Gain vs. Frequency



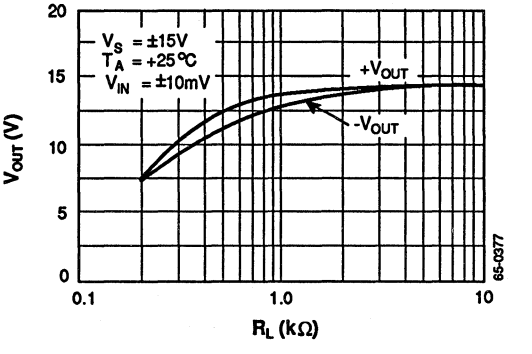
Closed Loop Response for Various Gain Configurations



Maximum Undistorted Output vs. Frequency

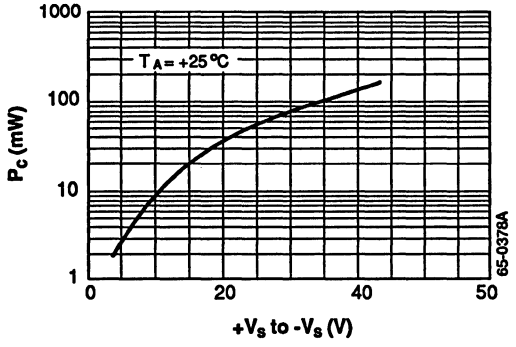


Output Voltage vs. Load Resistance to Ground

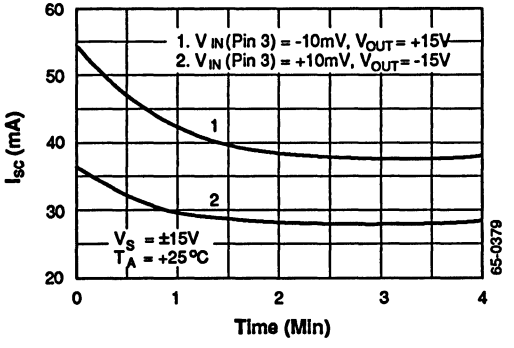


Typical Performance Characteristics

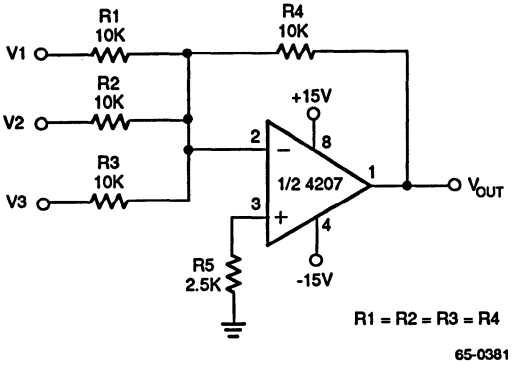
Power Consumption vs. Total Supply Voltage



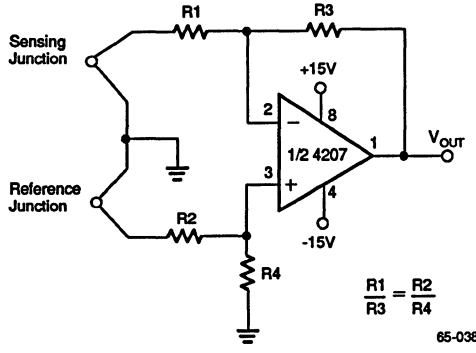
Output Short Circuit Current vs. Time



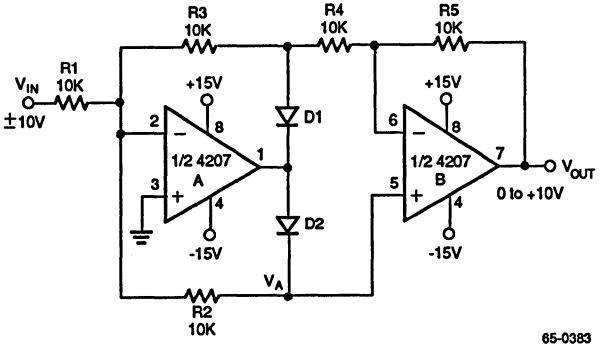
Typical Applications



Adjustment-Free Precision Summing Amplifier

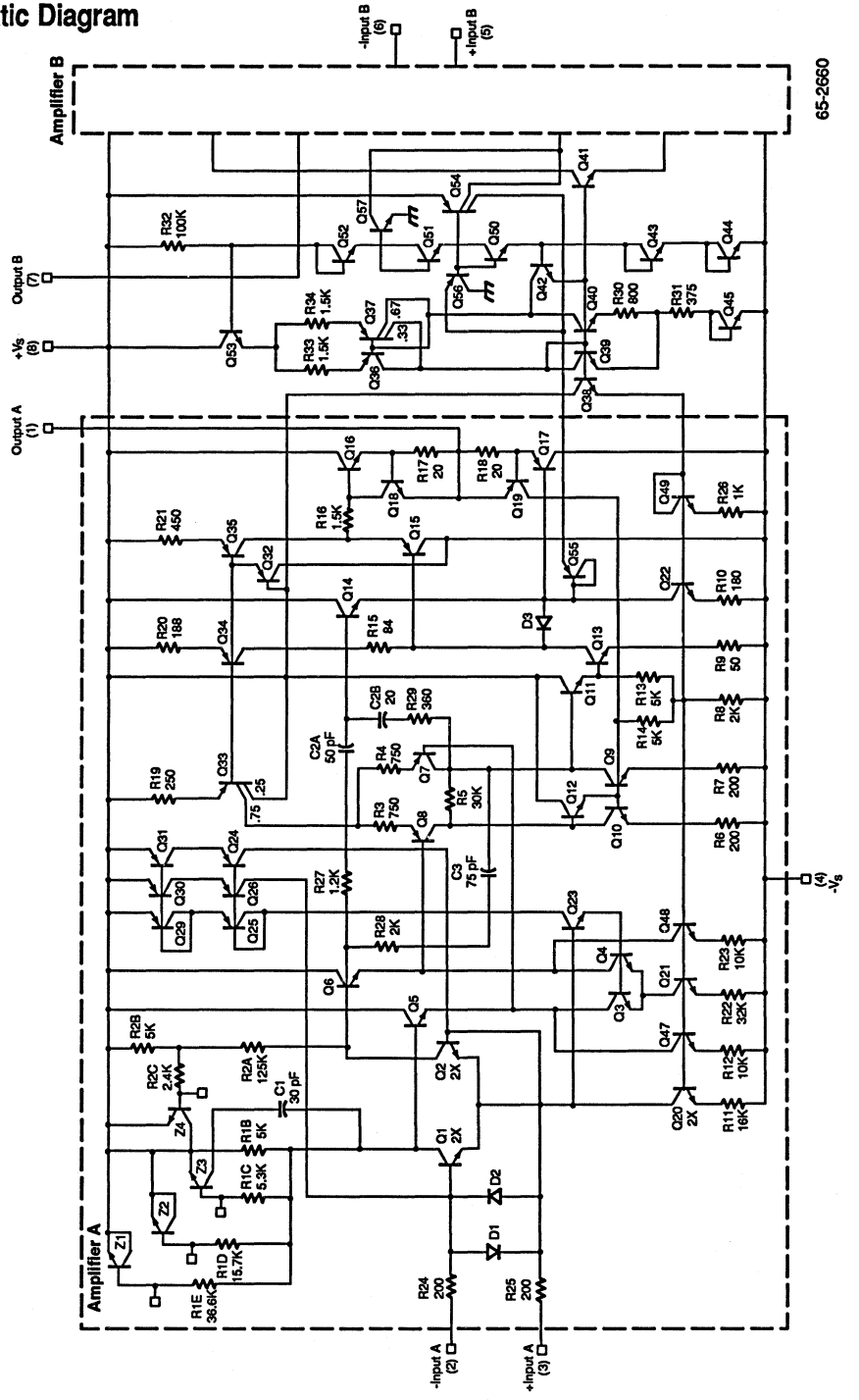


High Stability Thermocouple Amplifier



Precision Absolute Value Circuit

Schematic Diagram



RC4227
Dual Precision Operational Amplifier

Description

The 4227, a dual version of the OP-27, is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70°) in a unity gain configuration. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 75 μV max. Input bias current cancellation techniques are used to obtain ±45 nA max. input bias currents.

In addition to providing superior performance for audio frequency range applications, the 4227 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 100 dB. A phase margin of 70° at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000 pF.[1] The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The performance of the 4227 is achieved using precision amplifier design techniques coupled with a process that combines nitride transistors and capacitors with precision thin-film resistors. The die size savings of nitride capacitors and thin film resistors allow the 4227 to be offered in an 8-pin mini-dip package and fit the industry standard dual op amp pinout.

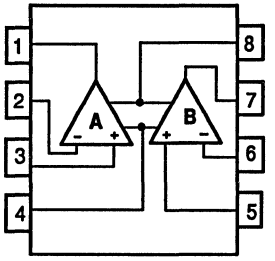
[1]By decoupling the load capacitance with a series resistor of 50Ω or more, load capacitances larger than 2000 pF can be accommodated.

Features

- Very low noise
  Spectral noise density — 3.8 nV/$\sqrt{Hz}$
  1/F noise corner frequency — 2.7 Hz
- Very low V_{OS} drift —
  0.3 μV/Mo; 0.3 μV/°C
- High gain — 500 V/mV
- High output drive capability — ±10V into 1K load
- High slew rate — 2.7 V/μS
- Wide gain bandwidth product — 8 MHz
- High common mode rejection ratio — 104 dB
- Low input offset voltage — 75 μV
- Low frequency noise — 0.08 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input offset current — 2.5 nA
- Industry standard pinout
- 8-Lead mini-DIP

Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function 65-01782
1	Output A
2	-Input A
3	+Input A
4	$-V_S$
5	+Input B
6	-Input B
7	Output B
8	$+V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
RC4227FN	N	0°C to +70°C
RC4227GN	N	0°C to +70°C
RM4227BD	D	-55°C to +125°C
RM4227BD/883B	D*	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D = 8-lead ceramic DIP
N = 8-lead plastic DIP

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Input Voltage[1] ..... ±18V
Differential Input Voltage 0.7V
Internal Power Dissipation[2] ..... 658 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4227B ..... -55°C to +125°C
RC4227F/G ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+125°C
Max. P_D T_A <50°C	833 mW	468 mW
Therm. Res. θ_{JC}	45°C/W	—
Therm. Tes. θ_{JA}	150°C/W	160°C/W
For T_A > 50°C derate at	8.33 mW/°C	6.25 mW/°C

Electrical Characteristics

(V_S = ±15V, and $T_A \leq +25°C$ unless otherwise noted)

Parameters	Test Conditions	4227B/F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			20	75		30	150	µV
Long Term V_{OS} Stability[1]			0.3			0.4		µV/Mo
Input Offset Current			±2.5	±10		±5	±15	nA
Input Bias Current			±5	±15		±7.5	±25	nA
Input noise Voltage	0.1 Hz to 10 Hz		0.08			0.08		µVp-p
Input Noise Voltage Density	F_O = 10 Hz		3.8			3.8		nV/√Hz
	F_O = 30 Hz		3.3			3.3		
	F_O = 1000 Hz		3.2			3.2		
Input Noise Current Density	F_O = 10 Hz		1.7			1.7		pA/√Hz
	F_O = 30 Hz		1.0			1.0		
	F_O = 1000 Hz		0.4			0.4		
Input Resistance (Diff. Mode)			5.0			4.0		MΩ
Input Resistance (Com. Mode)			2.5			2.0		GΩ
Input Voltage Range[2, 4]		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	104	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	104	120		100	118		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	500	1000		400	800		V/mV
	V_{OUT} = ±10V, R_L = 1KΩ,	400	800		300	600		
	V_{OUT} = ±1.0V, V_S = ±4.0V $R_L \geq 1.0k\Omega$	250	500		200	400		
Output Voltage Swing	$R_L \geq 2.0k\Omega$	±12	±13.8		±12	±13.8		V
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate[2]	$R_L \geq 2.0k\Omega$	1.5	2.7		0.1	0.3		V/µs
Gain Bandwidth Product		5.0	8.0		5.0	8.0		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		70			70		Ω
Power Consumption	RL = ∞		160	200		180	240	mW
Crosstalk		126	155		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	4227B			Units
		Min	Typ	Max	
Input Offset Voltage[1]			50	200	µV
Average Input Offset Voltage Drift[2]			0.3	1.3	µV/°C
Input Offset Current			±10	±35	nA
Input Bias Current			±15	±45	nA
Input Voltage Range		±10	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	119		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	114		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	350	650		V/mV
Output Voltage Swing	$R_L \geq 2.0$ kΩ	±11	±13.2		V
Power Consumption	$R_L = \infty$		200	280	mW

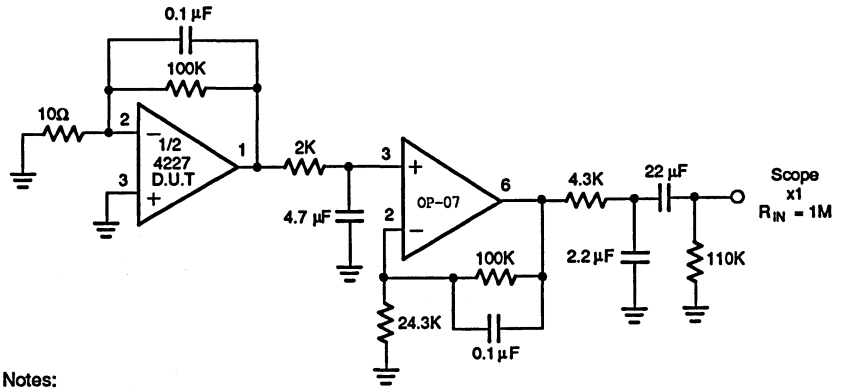
Notes:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	4227F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	µV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.4		µV/°C
Input Offset Current			±8	±15		±10	±35	nA
Input Bias Current			±10	±30		±15	±45	nA
Input Voltage Range		±10	±11.8		±10	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	121		92	118		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	116		92	114		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	350	700		250	500		V/mV
Output Voltage Swing	R_L > 2.0kΩ	±11	±13.5		±11	±13.5		V
Power Consumption	$R_L = \infty$		180	240	200	280		mW

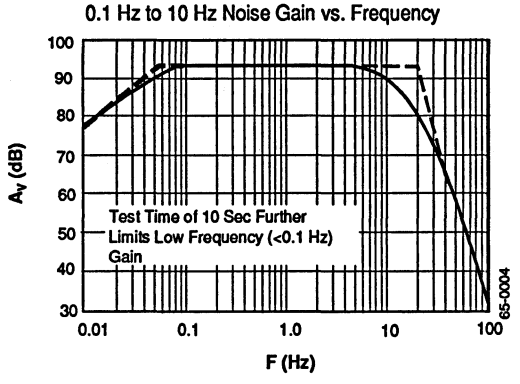
Typical Performance Characteristics

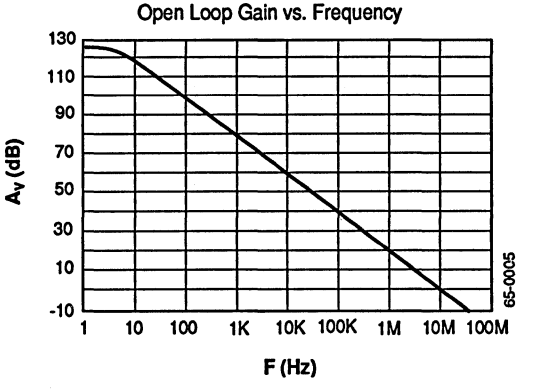


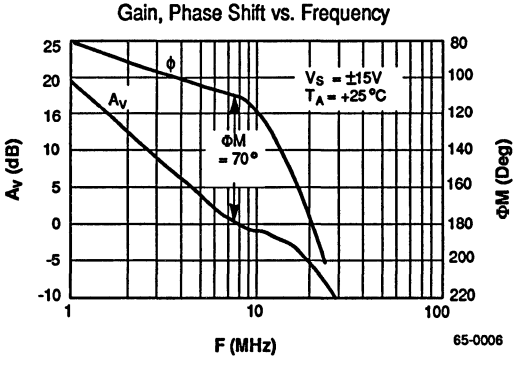
Notes:
1. Peak-to-peak noise measured in a 10-second interval.
2. The device under test should be warmed up for 3 minutes and shielded from air currents .
3. Voltage gain = 50,000.

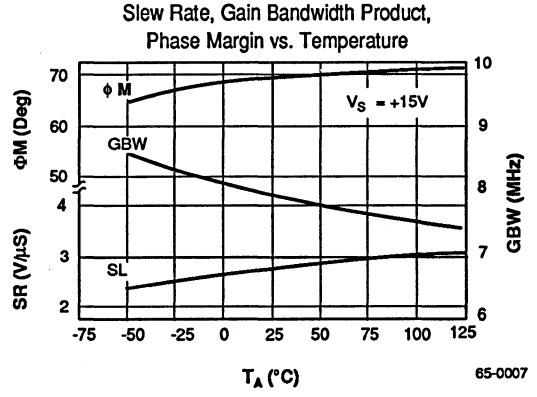
65-0003

0.1 Hz to 10 Hz Noise Test Circuit (1/2 Shown)





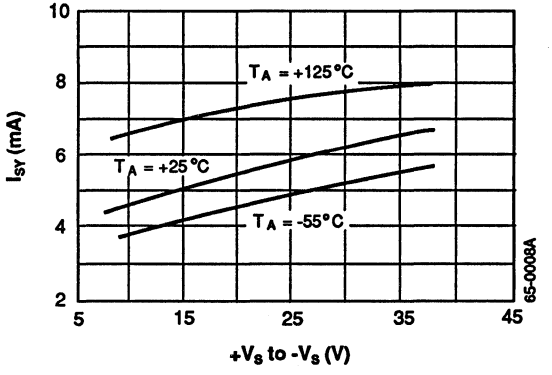




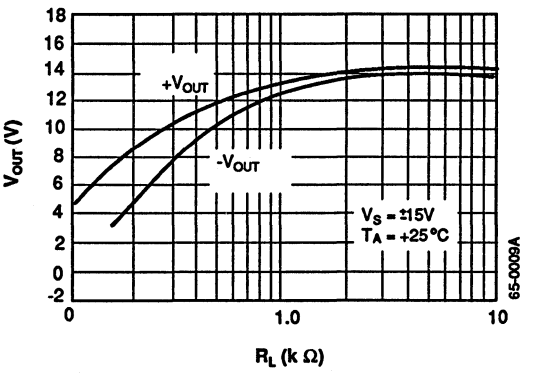
Linear

Typical Performance Characteristics (Continued)

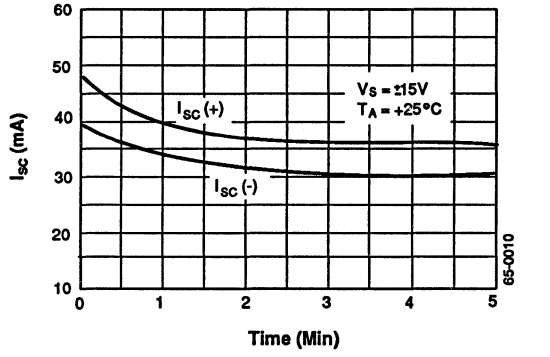
Supply Current vs. Total Supply Voltage



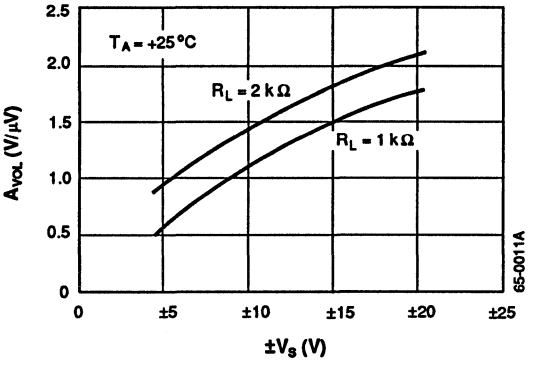
Maximum Output Swing vs. Load Resistance



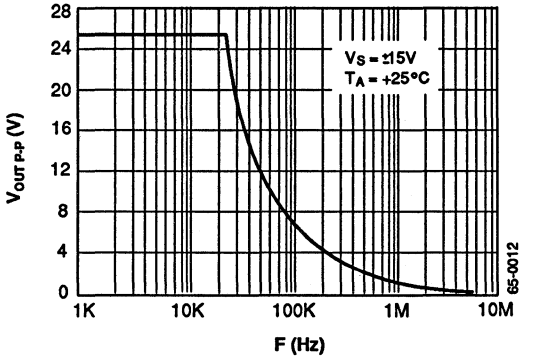
Short Circuit Current vs. Time



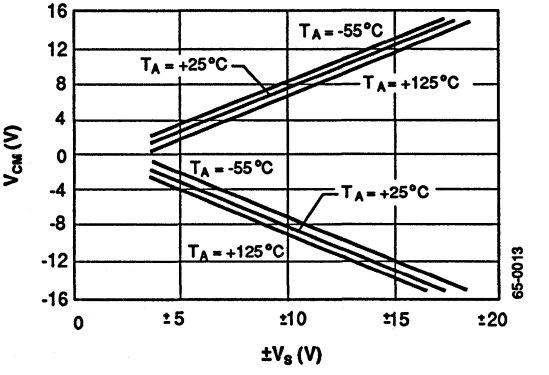
Open-Loop Gain vs. Total Supply Voltage



Maximum Undistorted Output vs. Frequency

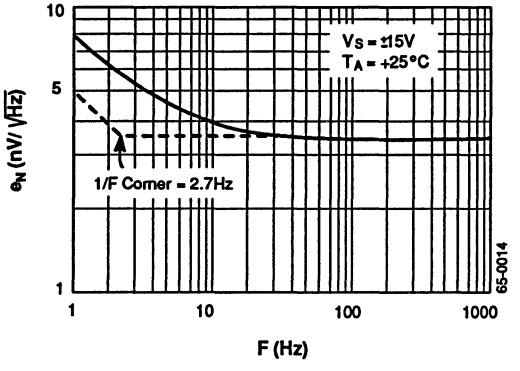


Common-Mode Input Range vs. Supply Voltage

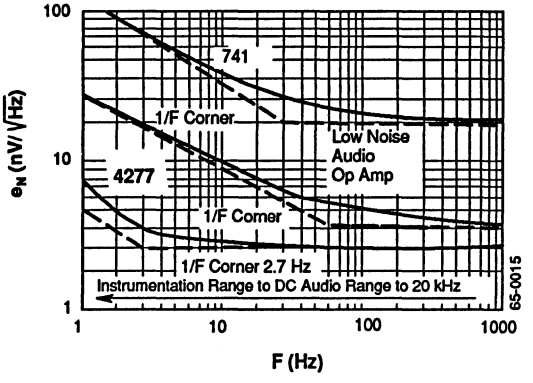


Typical Performance Characteristics (Continued)

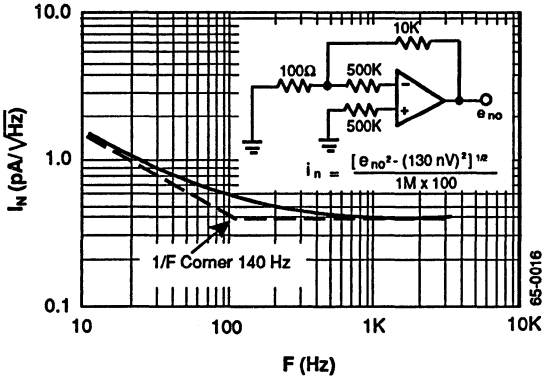
Input Noise Voltage Density vs. Frequency



Op Amp Comparison
Input Noise Voltage Density vs. Frequency

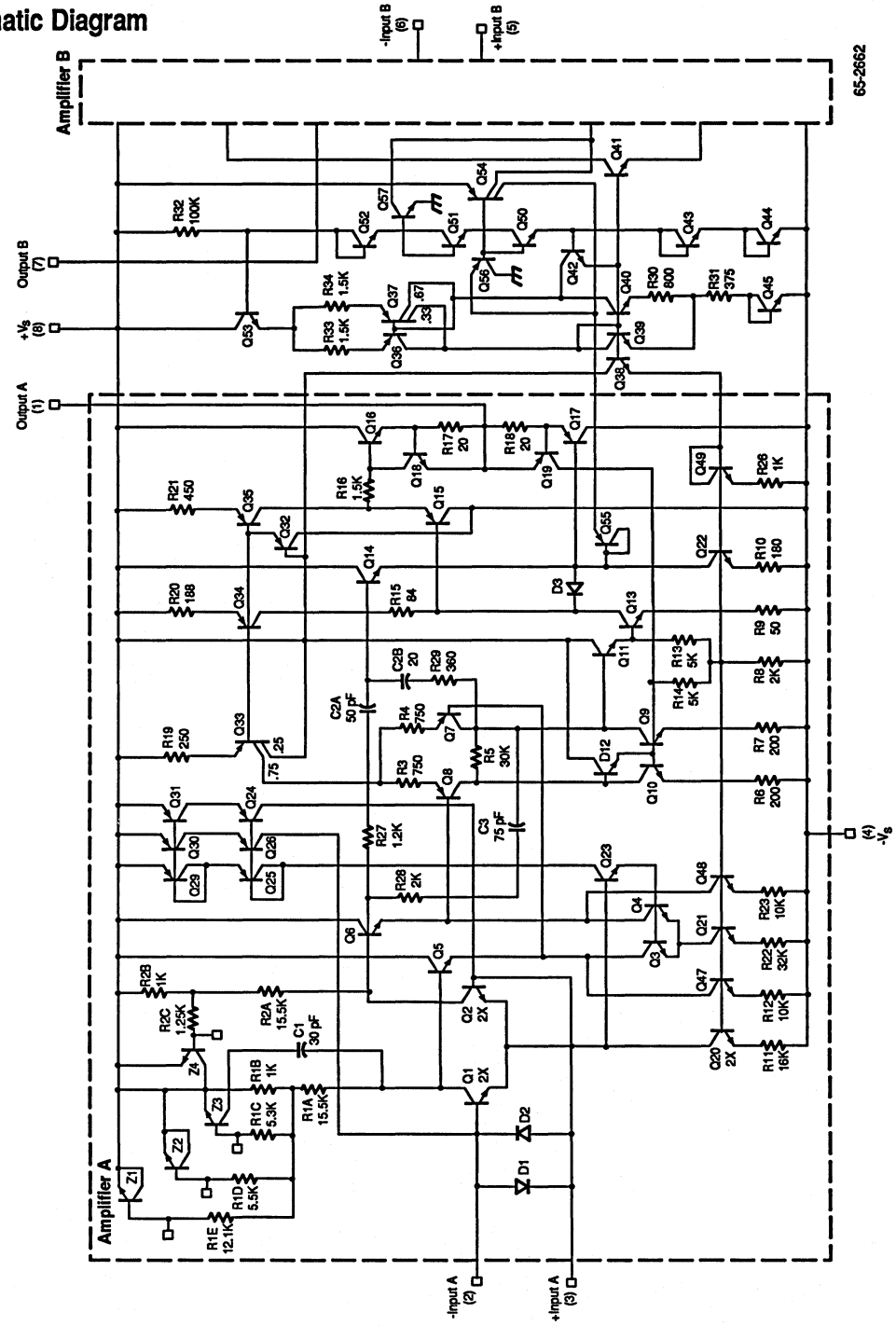


Input Noise Current Density vs. Frequency



Linear

Schematic Diagram



RC4277
Dual Precision Operational Amplifier

Description

The RC4277 provides the highest precision available in a dual bipolar operational amplifier. A monolithic dual version of the RC4077, the RC4277 is designed to replace OP-07 and OP-77 type amplifiers in applications requiring high PC board layout density. The RC4277 has a well-balanced, mutually supporting set of input specifications. Low V_{OS}, low I_B, high open-loop gain, and excellent matching characteristics combine to raise the performance level of many instrumentation, low-level signal conditioning, and data conversion applications. PSRR, CMRR, V_{OS} drift, and noise levels also support high precision operation.

The high performance of the RC4277 results from two innovative and unconventional manufacturing steps, plus careful circuit layout and design. The key steps are SiCr thin-film resistor deposition and post-package trimming of the input offset voltage characteristic. The low 75 µV max V_{OS} specification is maintained in high-volume production by way of the post-package trim procedure, where internal resistors are trimmed through the device input leads at the final test operation. Devices retain this low offset through the stability and accuracy of the trimmed thin-film resistors.

The RC4277 is available in 8-lead plastic and ceramic DIPs.

Features

- High DC precision
- Very low V_{OS} — 30 µV
- Very low V_{OS} drift — 0.3 µV/°C
- High open-loop gain — 5000 V/mV
- High CMRR — 120 dB
- High PSRR — 120 db
- Low noise — 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input bias current — 3.0 nA
- Low power consumption — 140 mW

Ordering Information

Part Number	Package	Operating Temperature Range
RC4277FN	N	0°C to +70°C
RV4277FD	D	-25°C to +85°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP

Thermal Characteristics

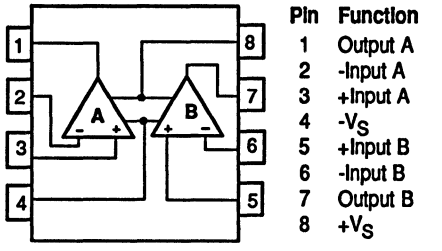
	8-Lead Ceramic DIP	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+125°C
Max. P_D T_A <50°C	833 mW	468 mW
Therm. Res θ_{JC}	45°C/W	—
Therm. Res. θ_{JA}	150°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	6.25 mW/°C

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation[2] ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
RV4277 ..... -25°C to +85°C
RC4277 ..... 0°C to +70°C
Lead Soldering Temperature (60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Connection Information



Pin	Function
1	Output A
2	-Input A
3	+Input A
4	$-V_S$
5	+Input B
6	-Input B
7	Output B
8	$+V_S$

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage[3]			30	75	µV
Input Offset Voltage Match			25	150	µV
Long Term V_{OS} Stability[1]			0.3		µV/Mo
Input Offset Current			0.5	5.0	nA
Input Bias Current			±0.5	±5.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.35		μV_{p-p}
Input Noise Voltage Density	F_O = 10 Hz		10.3		nV/√Hz
	F_O = 100 Hz		10		
	F_O = 1000 Hz		9.6		
Input Noise Current	0.1 Hz to 10 Hz		14		pA_{p-p}
Input Noise Current Density	F_O = 10 Hz		0.32		pA/√Hz
	F_O = 100 Hz		0.14		
	F_O = 1000 Hz		0.12		
Input Voltage Range[2, 4]		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	110	132		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	110	132		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	1300	3500		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12.5	±13		V
	$R_L \geq 2$ kΩ	±12	±12.8		
	$R_L \geq 1$ kΩ	±11	±12		
Slew Rate	$R_L \geq 2$ kΩ	0.1	0.3		V/µS
Closed Loop Bandwidth	A_{VCL} = +1.0		0.8		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		60	100	mW
Crosstalk		126	150		dB

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

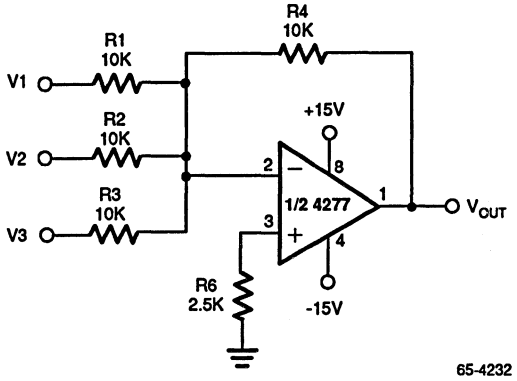
Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C for plastic packages unless otherwise noted)

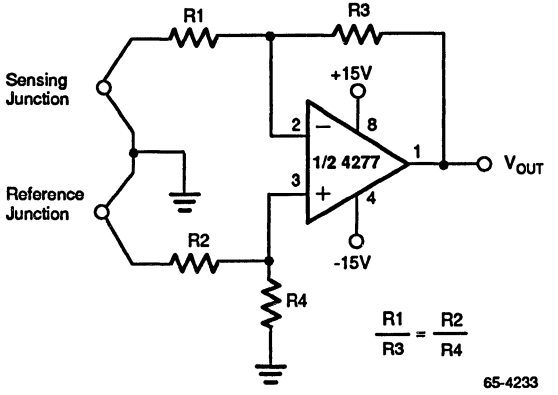
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	0°C ≤ T_A ≤ +70°C -25°C ≤ T_A ≤ +85°C		50 50	120 135	µV µV
Average Input Offset Voltage Drift[2]			0.3	1.0	µV/°C
Input Offset Current			1.5	5.0	nA
Input Bias Current			±1.5	±5.0	nA
Input Voltage Range		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	110	124		dB
Large Signal Voltage Gain	R_L > 2 kΩ, V_{OUT} = ±10V	1300	3000		V/mV
Maximum Output Voltage Swing	R_L > 2 kΩ	±11	±12.6		V
Power Consumption	R_L = ∞		70	120	mW

Notes:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

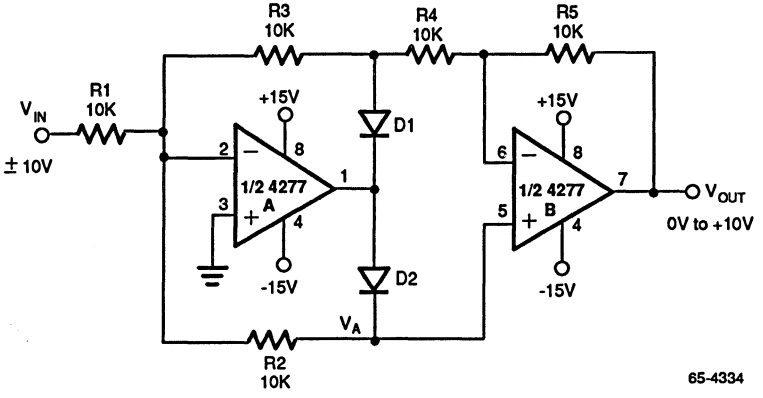
Typical Applications



Adjustment-Free Precision Summing Amplifier



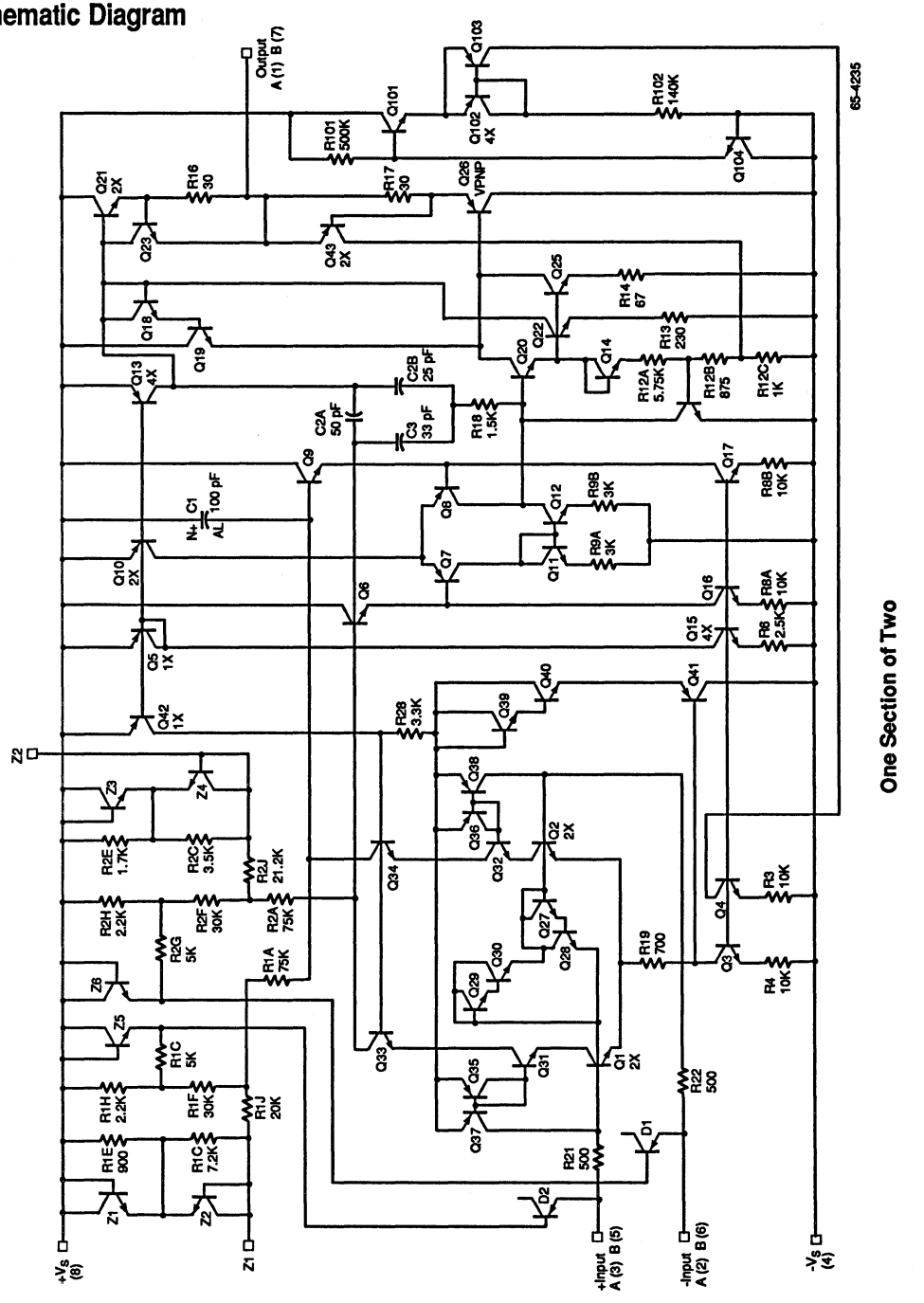
High Stability Thermocouple Amplifier



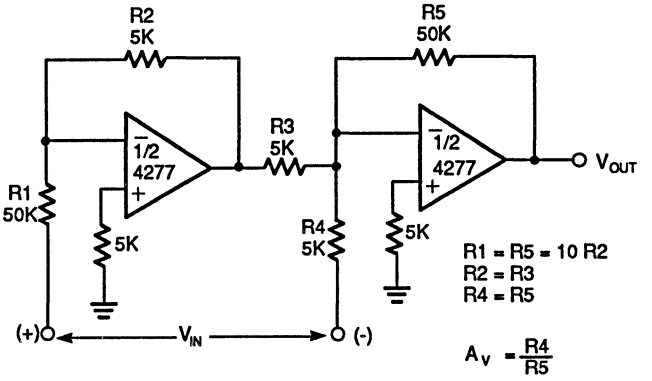
Precision Absolute Value Circuit

Linear

Schematic Diagram



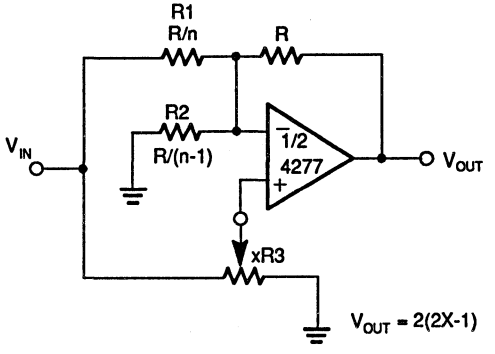
Typical Applications



Note: This circuit can tolerate input voltages that exceed the 4277's supply voltage rating as long as the slew rate do not exceed the op amp's slew rate.

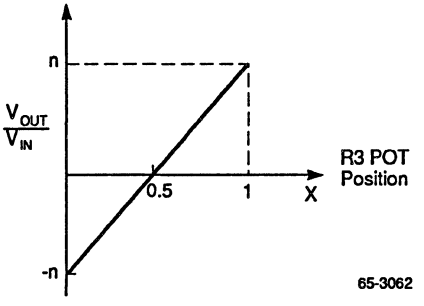
65-4427

High Voltage Differential Amplifier



65-4428

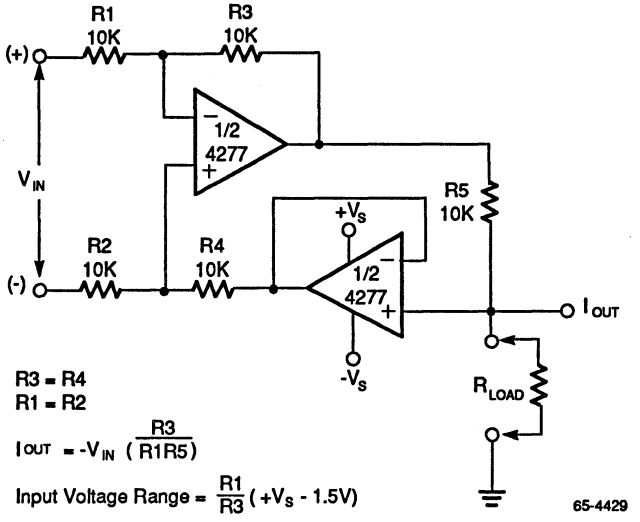
Polarity Changing Gain Controlled Amplifier



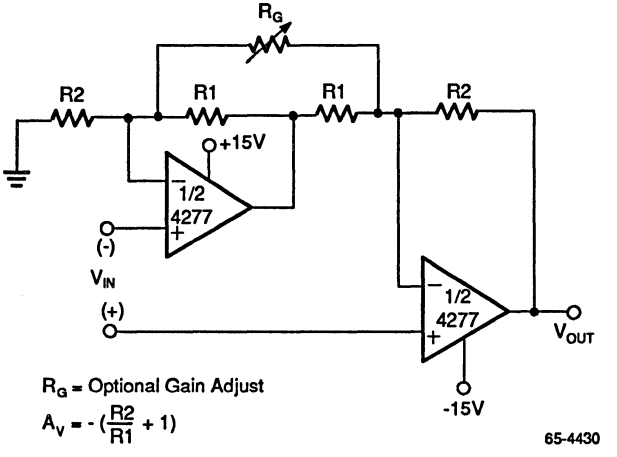
65-3062

Gain Controlled Amplifier Transfer Function

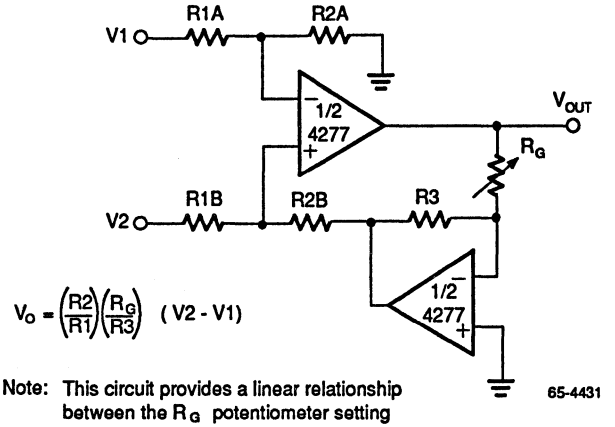
Linear



Differential Input Current Source

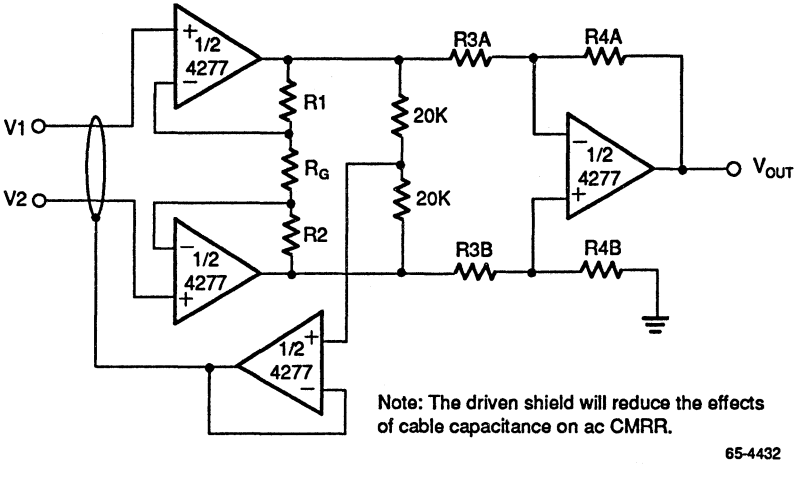


High Input Impedance Subtractor



Note: This circuit provides a linear relationship between the R_G potentiometer setting and circuit gain.

Difference Amplifier with Linear Gain Control

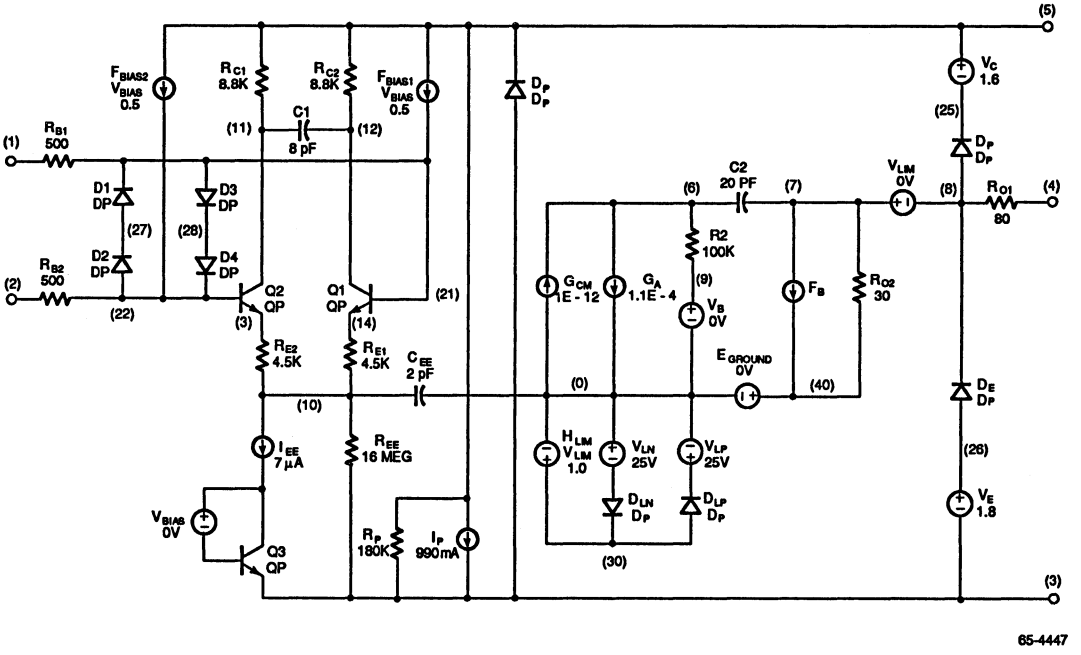


Three Op Amp Instrumentation Amplifier with Driven Shield

Linear

RM4277 SPICE Macro Model

This circuit models AC and DC characteristics including slew rate, bandwidth, V_{OS},I_B,I_{OS}, CMRR, output voltage range, and gain. The circuit produces typical values for these parameters.



65-4447

RC4560
Wide-Bandwidth Dual Operational Amplifier

Description

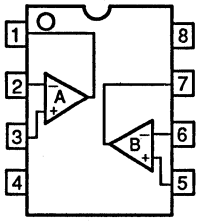
The 4560 integrated circuit is a high-gain, wide-bandwidth, dual operational amplifier capable of driving 20V peak-to-peak into 400Ω loads. The 4560 combines many of the features of the 4558 as well as providing the capability of wider bandwidth, and higher slew rate makes the 4560 ideal for active filters, data and telecommunications, and many instrumentation applications. The availability of the 4560 in the surface mounted package allows the 4560 to be used in critical applications requiring very high packing densities.

Features

- Unity gain bandwidth (A_V = 1) — 10MHz
- Slew rate — 4.0 V/μS
- Noise voltage at 1kHz — 7.0nV/√Hz
- Noise voltage current at 1kHz — 0.4pA/√Hz
- ±10V Output into 400Ω loads (±25mA)
- Supply current per amplifier — 1.8mA
- Input offset voltage — 2.0mV
- Input offset current — 5.0nA
- Unity gain frequency compensated
- Output short circuit protected

Connection Information

8-Lead
Dual In-Line Package
(Top View)



65-0210

Pin	Function
1	A Output
2	A -Input
3	A +Input
4	$+V_S$
5	B +Input
6	B -Input
7	B Output
8	$-V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
RC4560M	M	-20°C to +75°C
RC4560NB	N	-20°C to +75°C

Notes:
N: 8-lead plastic DIP
M = 8-lead plastic SOIC

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Input Voltage[1] ..... ±15V
Differential Input Voltage ..... +30V
Output Short Circuit Duration[2] ..... Indefinite
Operating Temperature
Range ..... -20°C to +75°C
Lead Soldering Temperature (10 Sec)
RC4560NB ..... +300°C
RC4560M ..... +260°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Thermal Characteristics

	Small Outline SO-8	8-Lead Plastic DIP
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A<50°C	300 mW	468 mW
Therm. Res θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For T_A >50°C Derate at	4.17 mW/°C	6.25 mW/°C

Matching Characteristics

(V_S = ±15V, T_A = +25°C)

Parameter	Conditions	Typ	Units
Voltage Gain	$R_L \geq 2\ k\Omega$	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

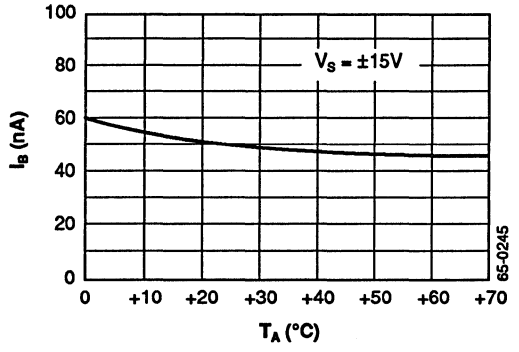
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0	mV
Input Offset Current			5.0	200	nA
Input Bias Current			50	500	nA
Input Resistance (Differential Mode)		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	20	300		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±12	±14		V
	I_0 = 25mA	±10	±11.5		
Input Voltage Range		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	90		dB
Power Consumption	R_L = ∞		135	200	mW
Transient Response					
Rise Time	V_{IN} = 20mV, R_L = 2 kΩ		0.05		µS
Overshoot	$C_L \leq 100pF$, Gain = 1		35		%
Slew Rate	$R_L \geq 2k\Omega$, Gain = 1		4.0		V/µS
Channel Separation	f = 10kHz R_S = 1kΩ, Gain = 100		100		dB
Unity Gain Bandwidth	A_V = +1, V_0 = -3dB		10		MHz

The following specifications apply for -20°C ≤ T_A ≤ +75°C

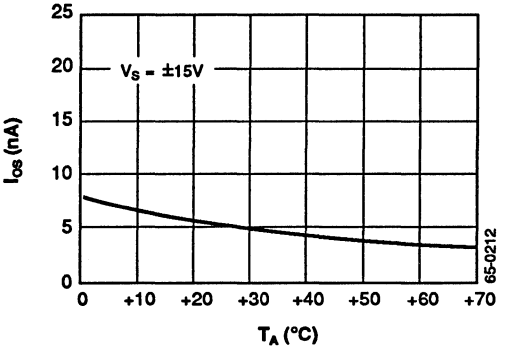
Input Offset Voltage	$R_S \leq 10k\Omega$			7.0	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V
Power Consumption	T_A = +75°C		135	200	mW
	T_A = -20°C		165	230	

Typical Performance Characteristics

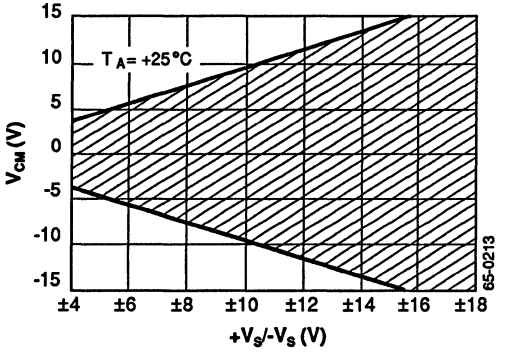
Input Bias Current as a Function of Ambient Temperature



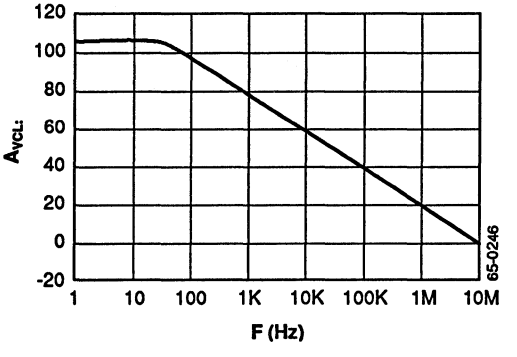
Input Offset Current as a Function of Ambient Temperature



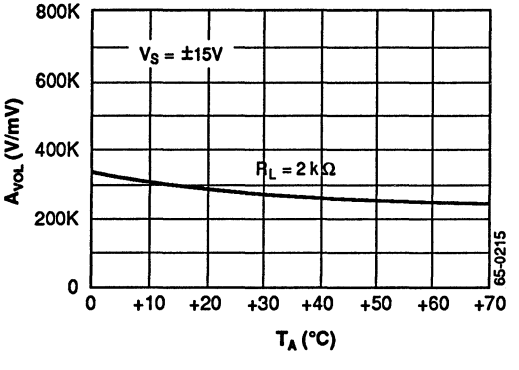
Common Mode Range as a Function of Supply Voltage



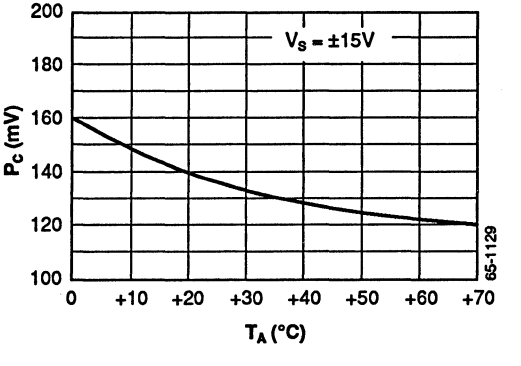
Open Loop Voltage Gain as a Function of Frequency



Open Loop Voltage Gain as a Function of Temperature



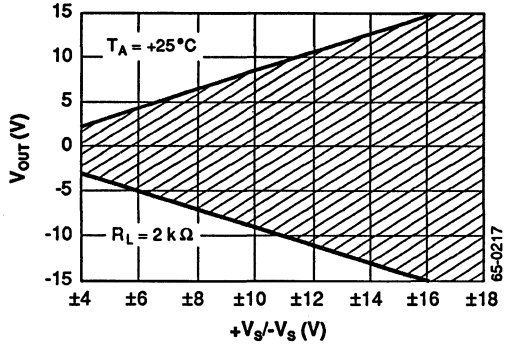
Power Consumption as a Function of Ambient Temperature



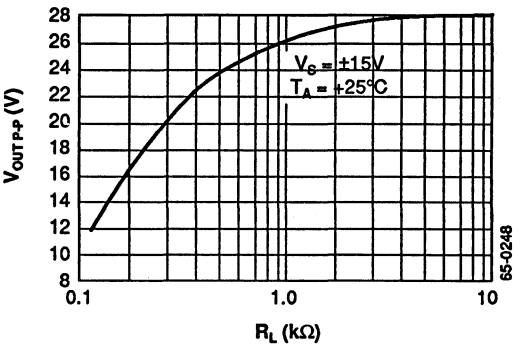
Linear

Typical Performance Characteristics (Continued)

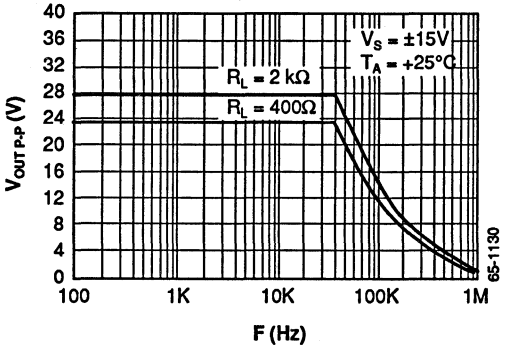
Typical Output Voltage as a Function of Supply Voltage



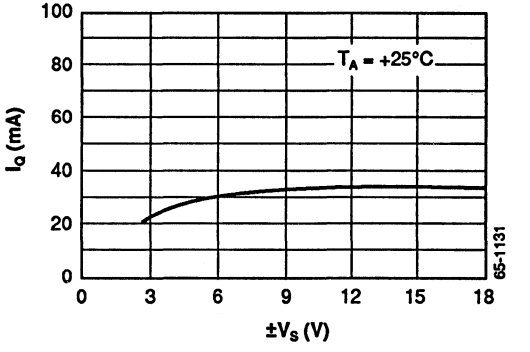
Output Voltage Swing as a Function of Load Resistance



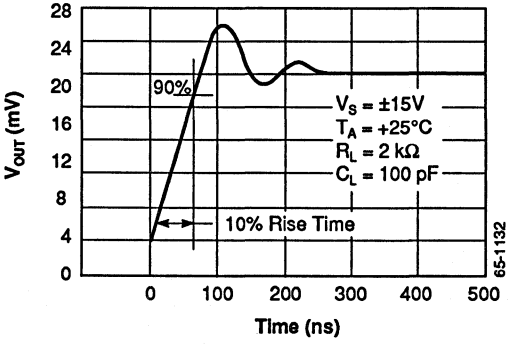
Output Voltage Swing as a Function of Frequency



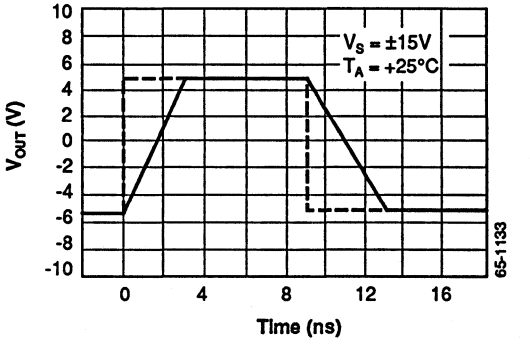
Quiescent Current as a Function of Supply Voltage



Transient Response

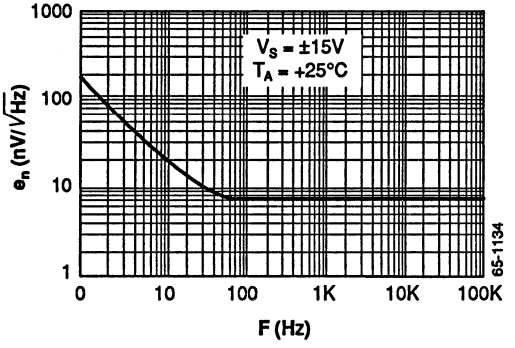


Voltage Follower Large Signal Pulse Response

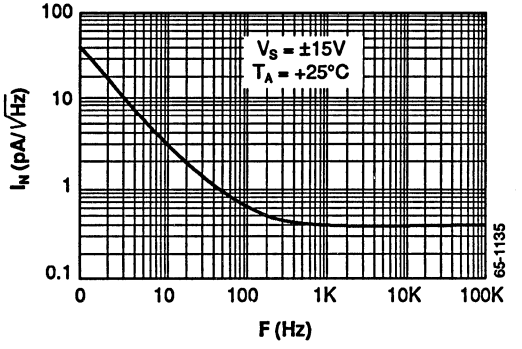


Typical Performance Characteristics (Continued)

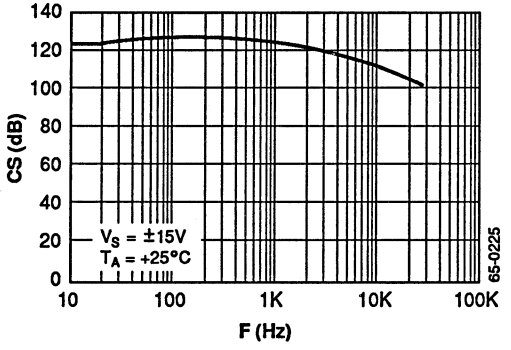
Input Noise as a Function of Frequency



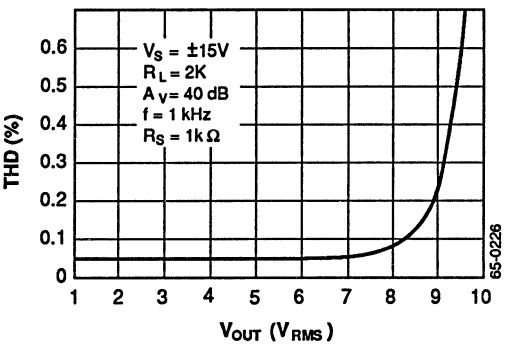
Input noise Current as a Function of Frequency



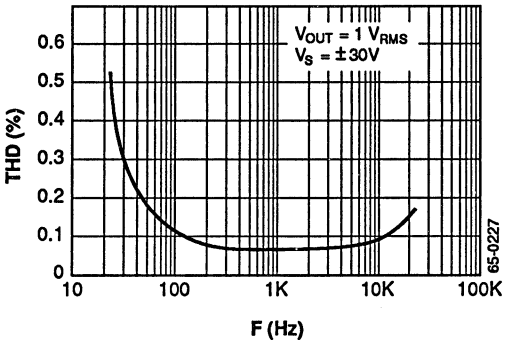
Channel Separation



Total Harmonic Distortion vs. Output Voltage

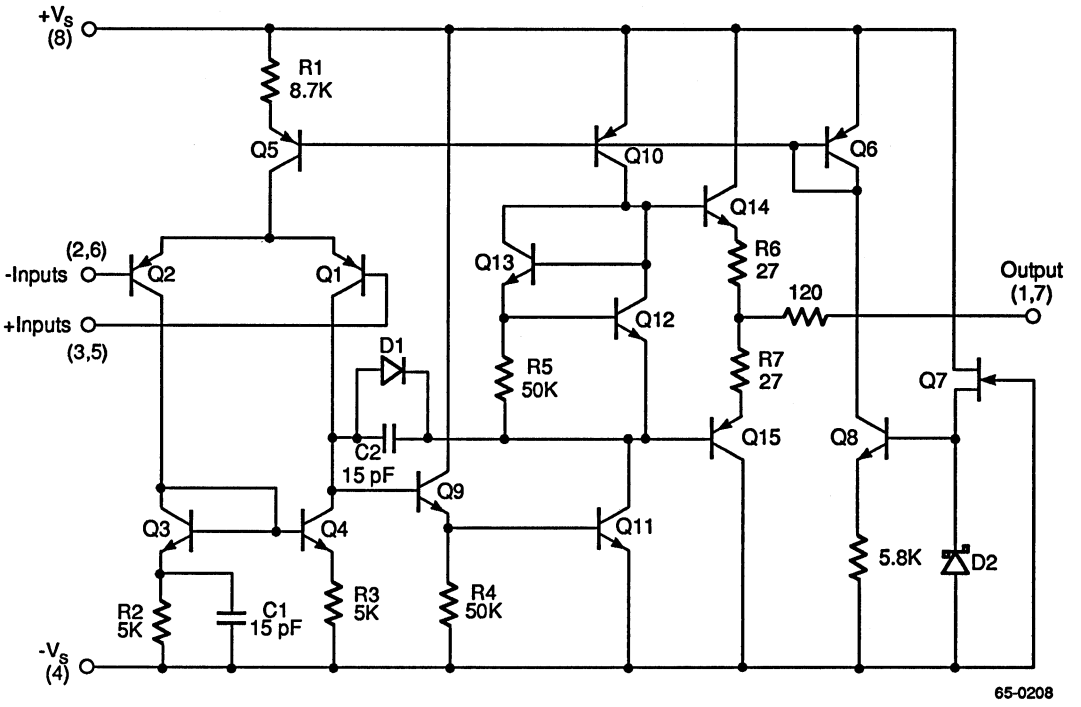


Distortion vs. Frequency



Linear

Schematic Diagram



RC4741
General Purpose Operational Amplifier

Description

The RC4741 is a monolithic integrated circuit, consisting of four independent operational amplifiers constructed with the planar epitaxial process.

These amplifiers feature AC and DC performance which exceed that of the 741 type amplifiers. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

A wide range of supply voltages (±2V to ±20V) can be used to power the RC4741, making it compatible with almost any system including battery powered equipment.

Features

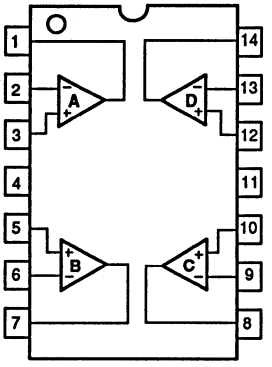
- Unity gain bandwidth — 3.5 MHz
- High slew rate — 1.6 V/μS
- Low noise voltage — 9 nV/$\sqrt{Hz}$
- Input offset voltage — 0.5 mV
- Input bias current — 60 nA
- Indefinite short circuit protection
- No crossover distortion
- Internal compensation
- Wide power supply range — ±2V to ±20V

Applications

- Universal active filters
- Audio amplifiers
- Battery powered equipment

Connection Information

14-Lead Dual In-Line Package
(Top View)



65-0418

Pin	Function
1	Output (A)
2	-Input (A)
3	+ Input (A)
4	$+V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	Output (C)
9	-Input (C)
10	+Input (C)
11	$-V_S$
12	+Input (D)
13	-Input (D)
14	Output (D)

Ordering Information

Part Number	Package	Operating Temperature Range
RC4741M	M	0°C to +70°C
RC4741N	N	0°C to +70°C
RM4741D	D	-55°C to +125°C
RM4741D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
M = 14-lead small outline

Absolute Maximum Ratings

Supply Voltage ..... ±20V
Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Output Short Circuit
Duration[2] ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4741 ..... -55°C to +125°C
RC4741 ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec, DIP) ..... +300°C
(10 Sec, SOIC) ..... +260°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit to ground on one amplifier only.

Thermal Characteristics

	14-Lead Small Outline	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp	+125°C	+125°C	+175°C
Max. P_D T_A,50°C	300 mW	468 mW	1042 mW
Therm. Res θ_{JC}	-	-	60°C/W
Therm Res. θ_{JC}	200°C/W	160°C/W	120°C/W
For T_A > 50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = 25°C unless otherwise specified)

		RM4741			RC4741			
Parameters	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	R_S ≤10kΩ		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	R_L ≥ 2kΩ V_{OUT} ±10V	50	100		25	50		V/mV
Input Voltage Range		±12			±12			V
Output Resistance			300			300		Ω
Output Current	V_{OUT} ±10V	±5	±15		±5	±15		mA
Common Mode Rejection Ratio	R_S ≤10kΩ ΔV = ±5	80			80			dB
Supply Current (All Amplifiers)			4.5	5.0		5.0	7.0	mA
Transient Response								
Rise Time			75			75		nS
Overshoot			25			25		%
Slew Rate			1.6			1.6		V/μS
Unity Gain Bandwidth			3.5			3.5		MHz
Power Bandwidth	V_{OUT} = 20Vp-p R_L = 2k		25			25		kHz
Input Noise Voltage Density	F=1kHz		9.0			9.0		nV/√Hz
Channel Separation			108			108		dB

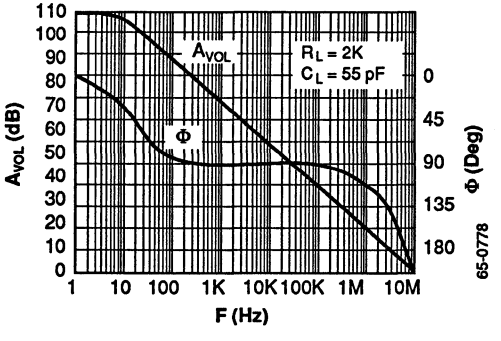
Electrical Characteristics

(VS = ±15V, RM = -55° C ≤ T_A ≤ +125° C, RC = 0°C ≤ T_A + 70°C)

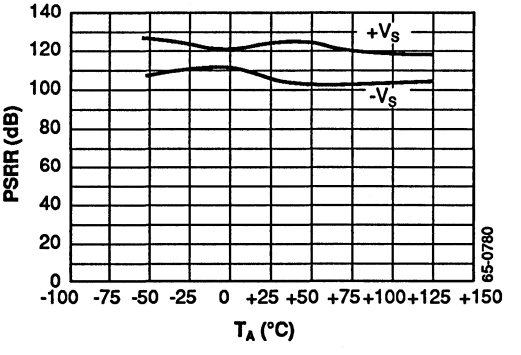
Parameters	Test Conditions	RM4741			RC4741			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤ 10kΩ		4.0	5.0		5.0	6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	R_L ≥ 2kΩ V_{OUT} ±10V	25			15			V/mV
Output Voltage Swing	R_L ≥ 10kΩ	±12	±13.7		±12	±13.7		V
	R_L ≥ 2kΩ	±10	±12.5		±10	±12.5		
Supply Current (All Amplifiers)			10			10		mA
Average Input Offset Voltage Drift			5.0			5.0		µV/°C
Common Mode Rejection Ratio	R_S ≤ 10kΩ ΔV ±5.0V	74			74			dB
Power Supply Rejection Ratio	R_S ≤ 10kΩ ΔV ±5.0V	80			80			dB

Typical Performance Characteristics

Open Loop Gain, Phase vs. Frequency

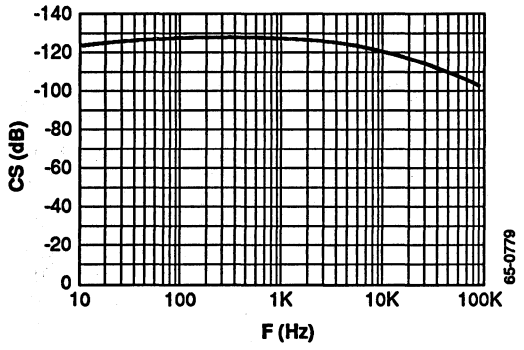


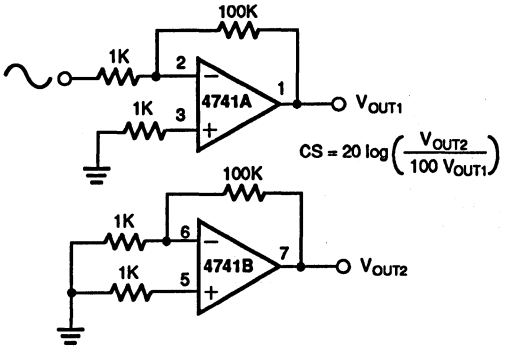
PSRR vs. Temperature



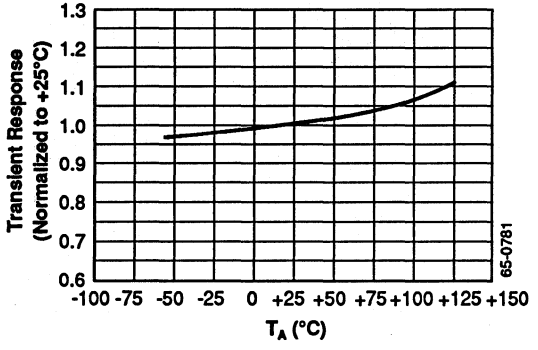
Typical Performance Characteristics (Continued)

Channel Separation vs. Frequency

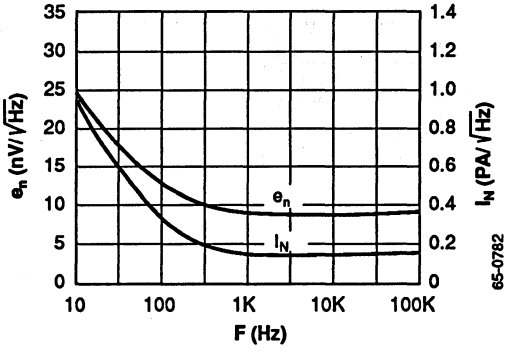




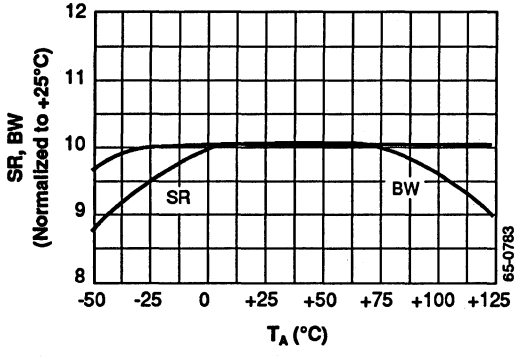
Transient Response vs. Temperature



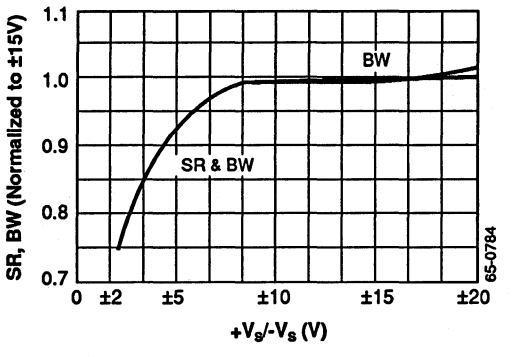
Input Noise Voltage vs. Frequency



Slew Rate, Bandwidth vs. Temperature



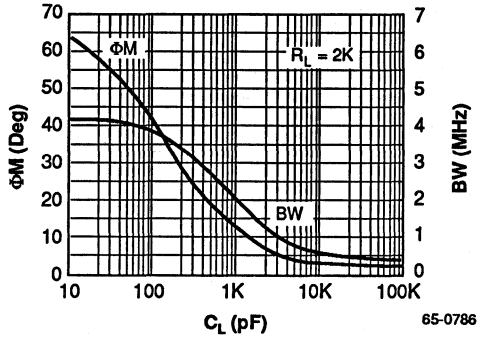
Slew Rate, Bandwidth vs. Supply Voltage



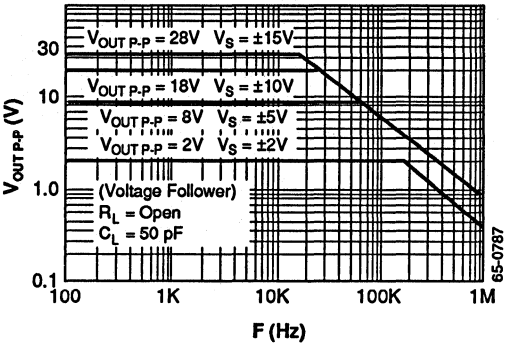
Linear

Typical Performance Characteristics (Continued)

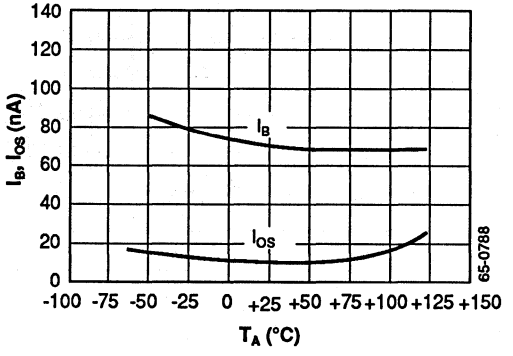
Small Signal Phase Margin, Unity Gain Bandwidth vs. Load Capacitance



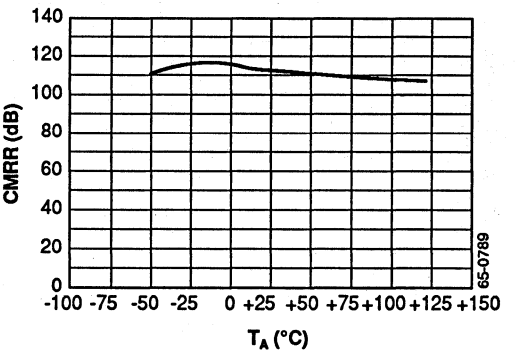
Output Voltage Swing vs. Frequency



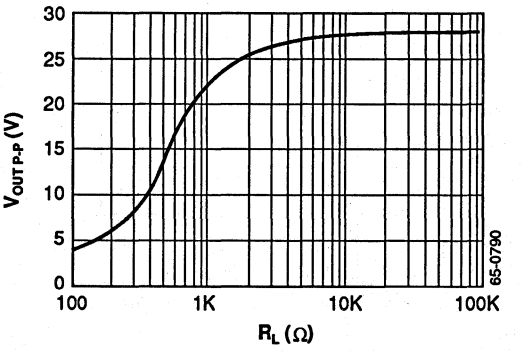
Input Bias, Offset Current vs. Temperature



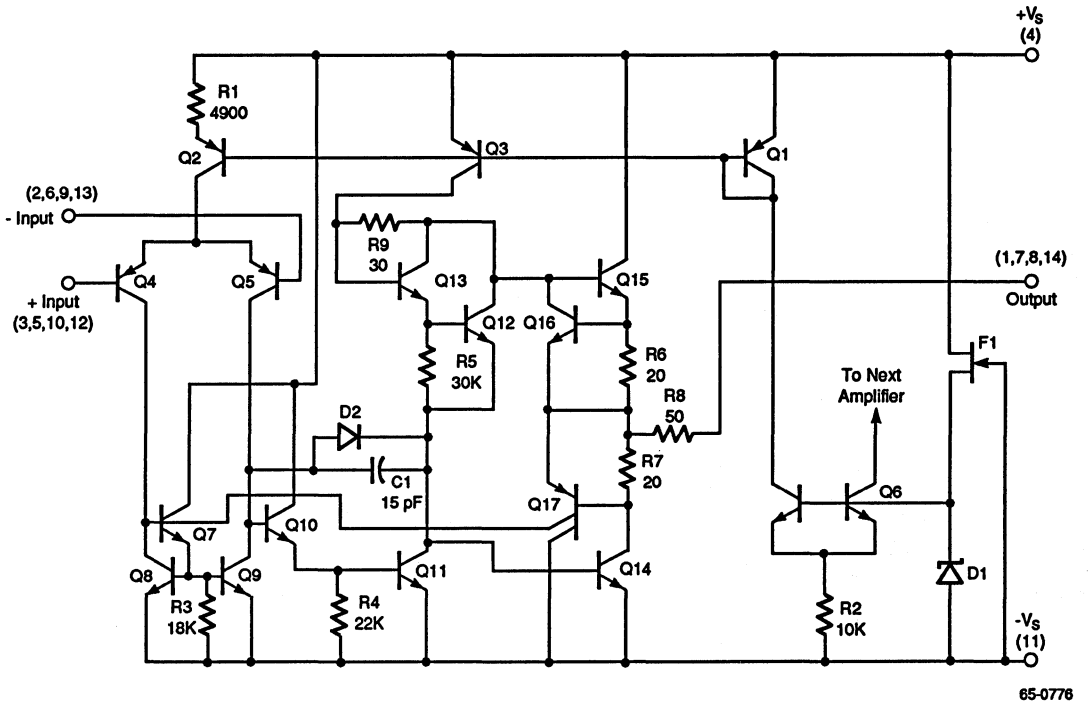
CMRR vs. Temperature



Output Voltage Swing vs. Load Resistance



Schematic Diagram (1/4 Shown)



Linear

RC5532/5532A
High Performance Dual Low Noise Operational Amplifier

Description

The 5532 is a high performance, dual low noise operational amplifier. Compared to standard dual operational amplifiers, such as the RC747, it shows better noise performance, improved output drive capability, and considerably higher small-signal and power bandwidths.

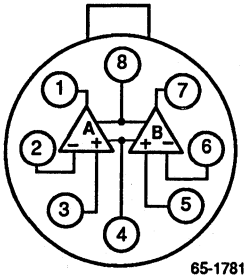
This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation, control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise specifications.

Features

- Small signal bandwidth — 10 MHz
- Output drive capability — 600Ω, 10 V_{RMS}
- Input noise voltage — 5 nV/√Hz
- DC voltage gain — 50,000
- AC voltage gain — 2200 at 10 kHz
- Power bandwidth — 140 kHz
- Slew rate — 8 V/μS
- Large supply voltage range — ±3V to ±20V

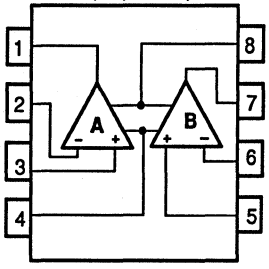
Connection Information

8-Lead TO-99 Metal Can
(Top View)



65-1781

8-Lead
Dual In-Line Package
(Top View)



65-01782

Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$-V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	$+V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
RC5532D	D	0°C to -70°C
RC5532N	N	0°C to +70°C
RC5532AD	D	0°C to -70°C
RC5532AN	N	0°C to +70°C
RM5532D	D	-55°C to +125°C
RM5532D/883B	D	-55°C to +125°C
RM5532AD	D	-55°C to +125°C
RM5532AD/883B	D	-55°C to +125°C
RM5532T	T	-55°C to +125°C
RM5532T/883B	T	-55°C to +125°C
RM5532AT	T	-55°C to +125°C
RM5532AT/883B	T	-55°C to +125°C

Notes:
883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
T = 8-lead metal can TO-99

Absolute Maximum Ratings(1)

Supply Voltage ..... ±22V
Input Voltage ..... $\pm V_S$
Differential Input Voltage 0.5V
Operating Temperature Range
RM5532/A ..... -55°C to +125°C
RC5532/A ..... 0°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

DC Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM5532/5532A			RC5532/5532A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.5	2.0		0.5	4.0	mV
	Over Temperature			3.0			5.0	mV
Input Offset Current				100		10	150	nA
	Over Temperature			200			200	nA
Input Bias Current			200	400		200	800	nA
	Over Temperature			700			1000	nA
Supply Current			6.0	11		6.0	16	mA
	Over Temperature			13			22	mA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio		80	100		70	100		dB
Power Supply Rejection Ratio		86	100		80	100		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	50			25	100		V/mV
	Over Temperature	25			15	50		
	$R_L \geq 600\Omega$, V_{OUT} = ±10V	40			15	50		
	Over Temperature	20			10			
Output Voltage Swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
	R_L = 600Ω, V_S = ±18V	±15	±16		±15	±16		
	$R_L \geq 2k\Omega$	±12	±13					
Input Resistance (Diff. Mode)			300			300		kΩ
Short Circuit Current			38			38		mA

Notes: 1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum input current should be limited to ±10mA.

2. Over Temperature: RM = 55 °C ≤ T_A 125°C; RC = 0°C ≤ T_A ≤70°C

Electrical Characteristics

(V_S = +15V and T_A = +25°C)

Parameters	Test Conditions	RC/RM5532			RC/RM5532A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Noise Voltage Density	F_O = 30 Hz F_O = 1 kHz		8.0 5.0			8.0 5.0	12 6.0	nV/√Hz
Input Noise Current Density	F_O = 30 Hz F_O - 1 kHz		2.7 0.7			2.7 0.7		pA/√Hz
Channel Separation	F = 1 kHz, R_S = 5 kΩ		110			110		dB

Linear

AC Electrical Characteristics

(V_S = ±15V and T_A = +25°C)

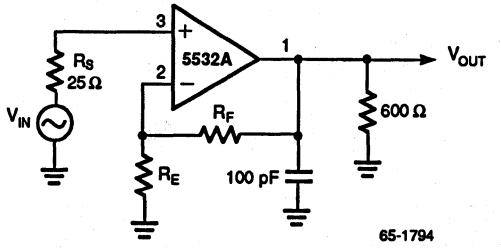
Parameters	Test Conditions	RC/RM5532/5532A Min	Typ	Max	Units
Output Resistance	A_V = 30 dB Closed Loop, F = 10 kHz, R_L = 600Ω		0.3		Ω
Overshoot	Unity Gain, V_{IN} = 100 mV_{P-P} C_L = 100 pF, R_L = 600Ω		10		%
Gain	F = 10 kHz		2.2		V/mV
Gain Bandwidth Product	C_L = 100 pF, R_L = 600Ω		10		MHz
Slew Rate			8.0		V/µS
Power Bandwidth	V_{OUT} = ±10V		140		kHz
	V_{OUT} = ±14V, R_L = 600Ω, V_S = ±18V		100		kHz

Thermal Characteristics

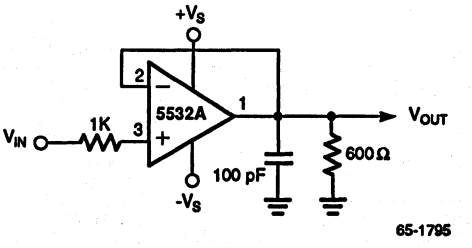
	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal ICan
Max. Junction Temp.	+125°C	+175°C	+175°C
Max. P_D T_A<50°C	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Test Circuits

Closed Loop Frequency Response

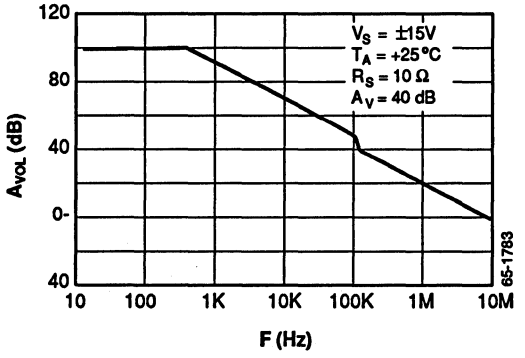


Follower, Transient Response

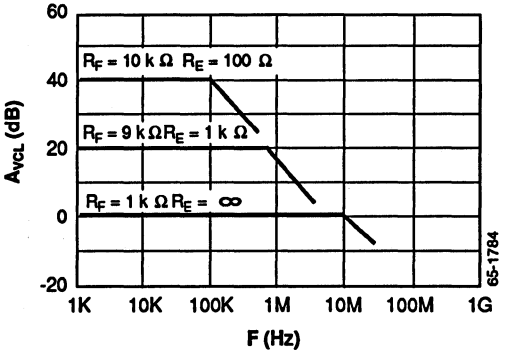


Typical Performance Characteristics

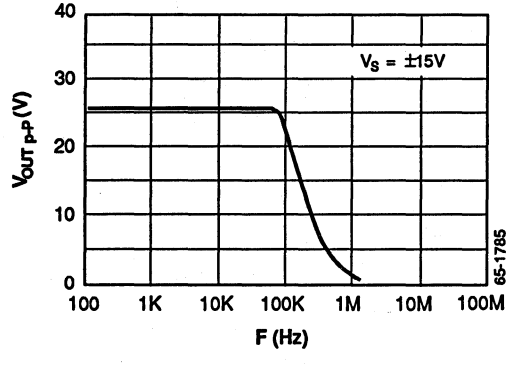
Open Loop Gain vs. Frequency



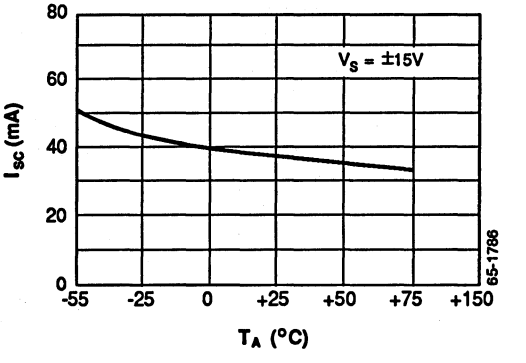
Closed Loop Gain vs. Frequency



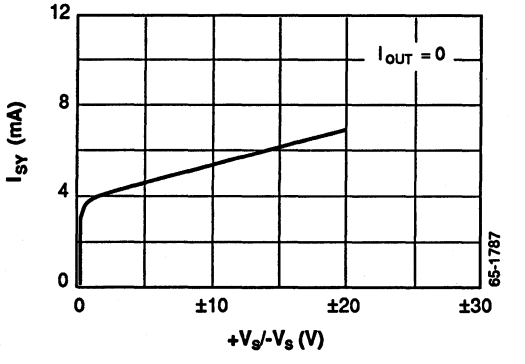
Output Voltage Swing vs. Frequency



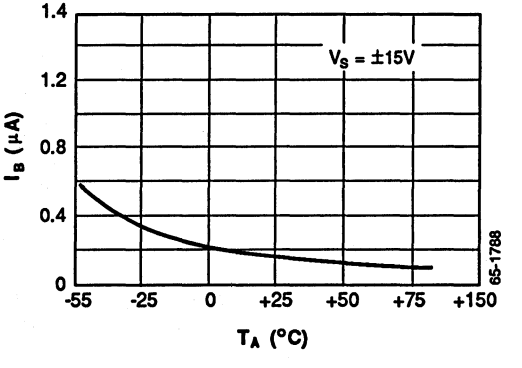
Short Circuit Current vs. Temperature



Supply Current vs. Supply Voltage



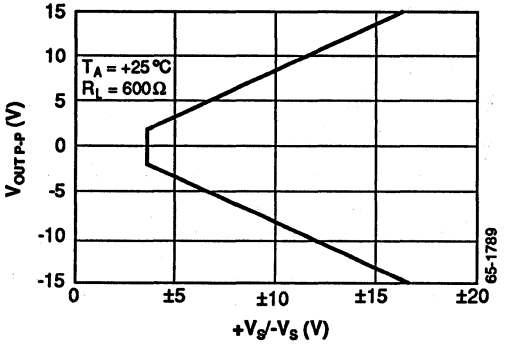
Input Bias Current vs. Temperature



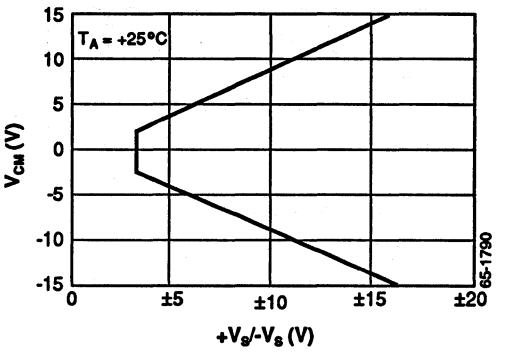
Linear

Typical Performance Characteristics (Continued)

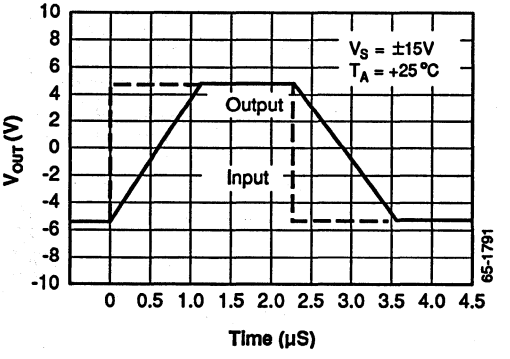
Output Voltage Swing vs. Supply Voltage



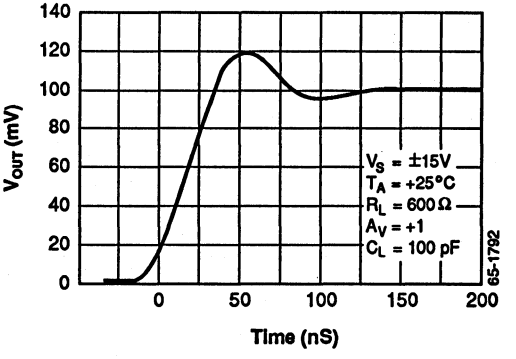
Common Mode Input Range vs. Supply Voltage



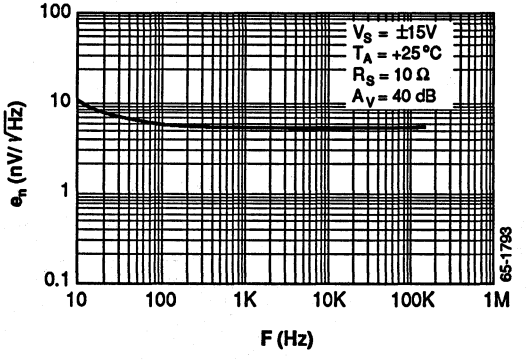
Follower Large Signal Pulse Response
Output Voltage vs. Time



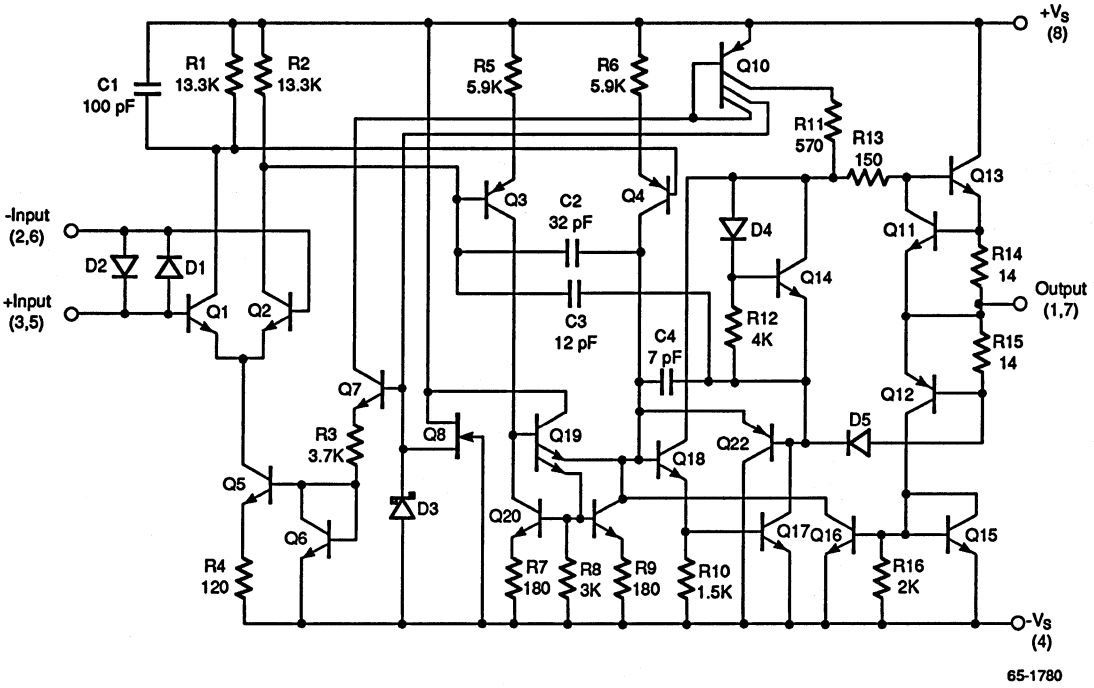
Transient Response
Output Voltage vs. Time



Input Noise Voltage Density vs. Frequency



Schematic Diagram (1/2 Shown for 5532)



Linear

RC5534/5534A
High Performance Low Noise Operational Amplifier

Description

The 5534 is a high performance, low noise operational amplifier. This amplifier features popular pin-out, superior noise performance, and high output drive capability.

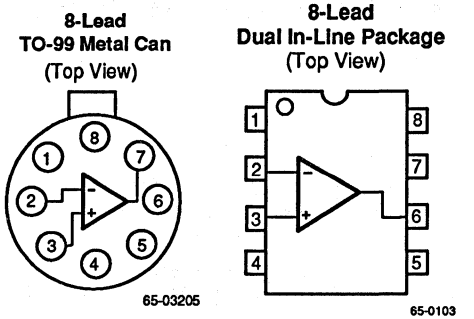
This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product, power bandwidth, and slew rate which far exceeds that of the 741 type amplifiers. The 5534 is internally compensated for a gain of three or higher and may be externally compensated for optimizing specific performance requirements of various applications such as unity-gain voltage followers, drivers for capacitive loads or fast settling.

The specially designed low noise input transistors allow the 5534 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifiers.

Features

- Small signal bandwidth — 10 MHz
- Output drive capability — 600Ω, 10 V_{RMS} at V_S = ±18V
- Input noise voltage — 4 nV/√Hz
- DC voltage gain — 100,000
- AC voltage gain — 6000 at 10 kHz
- Power bandwidth — 200 kHz
- Slew rate — 13 V/μS
- Large supply voltage range — ±3V to ±20V

Connection Information



Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	Comp
6	Output
7	$+V_S$
8	V_{OS} Trim/Comp

Ordering Information

Part Number	Package	Operating Temperature Range
RC5534N	N	0°C to +70°C
RC5534AN	N	0°C to +70°C
RM5534D	D	-55°C to +125°C
RM5534D/883B	D	-55°C to +125°C
RM5534AD	D	-55°C to +125°C
RM5534AD/883B	D	-55°C to +125°C
RM5534T	T	-55°C to +125°C
RM5534T/883B	T	-55°C to +125°C
RM5534AT	T	-55°C to +125°C
RM5534AT/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
T = 8-lead metal can (TO-99)

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Differential Input Voltage 0.5V
Input Voltage ..... $\pm V_S$
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature
Range
RM5534/A ..... -55°C to +125°C
RC5534/A ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C
Output Short Circuit Duration[1] ..... +300°C

Notes:
1. Short circuit may be to ground only. Rating applies to +125°C case temperature or +175°C junction temperature.

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	+125°C	+175°C	+175°C
Max. P_D T_A <50°C	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

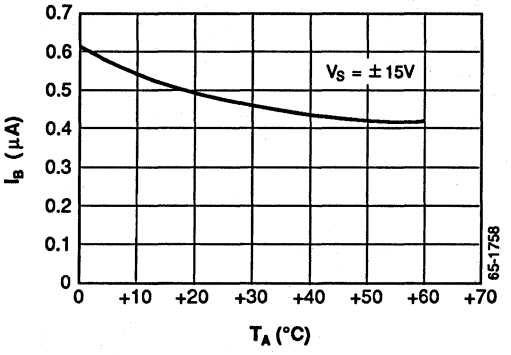
Parameters	Test Conditions	RM5534/A Min	RM5534/A Typ	RM5534/A Max	RC5534/A Min	RC5534/A Typ	RC5534/A Max	Units
Input Offset Voltage	$R_S \leq 1k\Omega$		0.5	2.0		0.5	4.0	mV
Input Offset Current			10	200		20	300	nA
Input Bias Current			400	800		500	1500	nA
Input Resistance (Diff. Mode)			100			100		kΩ
Large Signal Voltage Gain	$R_L \geq 600\Omega$, V_{OUT} = ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 1k\Omega$	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 1k\Omega$	86	100		86	100		dB
Supply Current	$R_L = \infty$		4.0	6.5		4.0	8.0	mA
Transient Response Rise Time	V_{IN} = 50 mV, R_L = 600Ω, C_L = 100 pF, C_C = 22 pF		35			35		nS
Overshoot			17			17		%
Slew Rate	C_C = 0		13			13		V/μS
Gain Bandwidth Product	C_C = 22 pF, C_L = 100 pF		10			10		MHz
Power Bandwidth	$V_{OUT} = 20V_{P-P}$, C_C = 0		200			200		kHz
Input Noise Voltage	F = 20 Hz to 20 kHz		1.0			1.0		μV_{RMS}
Input Noise Current	F = 20 Hz to 20 kHz		25			25		pA_{RMS}
Channel Separation	F = 1 kHz, R_S = 5 kΩ		110			110		dB
			5534A			5534		
Input Noise Voltage Density	F_O = 30 Hz		5.5	7.0		7.0		$\frac{nV}{\sqrt{Hz}}$
	F_O = 1 kHz		3.5	4.5		4.0		$\frac{nV}{\sqrt{Hz}}$
Input Noise Current Density	F_O = 30 Hz		1.5			2.5		$\frac{pA}{\sqrt{Hz}}$
	F_O = 1 kHz		0.4			0.6		$\frac{pA}{\sqrt{Hz}}$
Broadband Noise Figure	F = 10 Hz - 20 kHz, R_S = 5 kΩ		0.9					dB

The following specifications apply for RM; -55°C ≤ T_A ≤ +125°C = RC = 0°C ≤ T_A ≤ + 70°C, V_S = ±15V

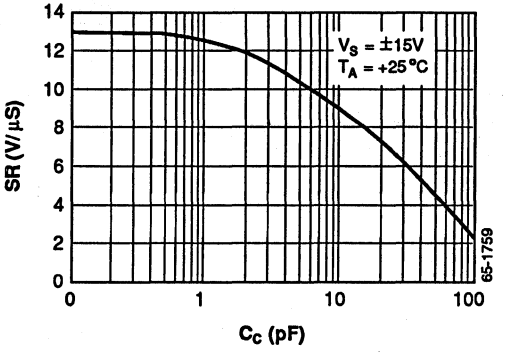
		RM5534/A			RC5534/A			
Input Offset Voltage	$R_S \leq 1$ kΩ			3.0			5.0	mV
Input Offset Current				500			400	nA
Input Bias Current				1500			2000	nA
Large Signal Voltage Gain	$R_L \geq 600\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 600\Omega$	±10			±10			V
Supply Current	V_S = ±15V, $R_L = \infty$			9.0			14	mA

Typical Performance Characteristics

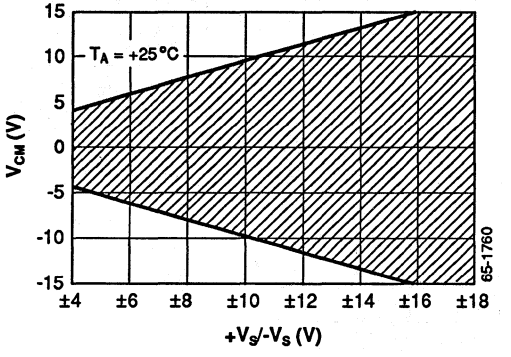
Input Bias Current vs. Temperature



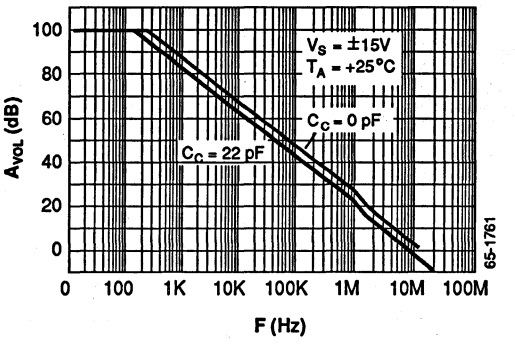
Slew Rate vs. Compensation Capacitor



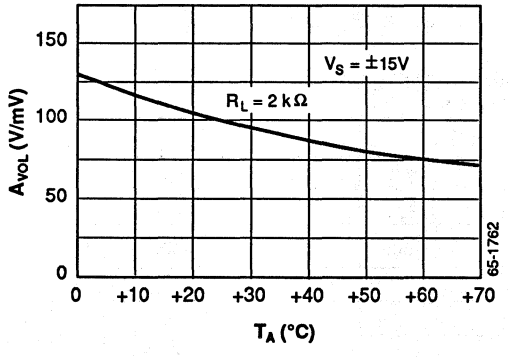
Common Mode Input Range vs. Supply Voltage



Open Loop Gain vs. Frequency

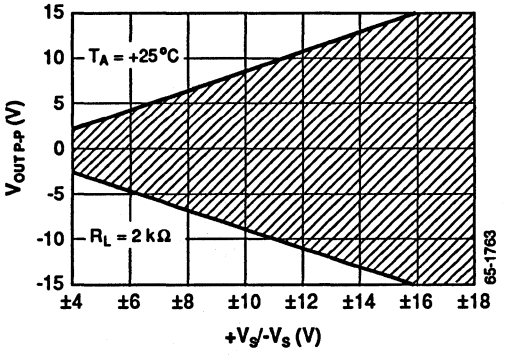


Open Loop Gain vs. Temperature

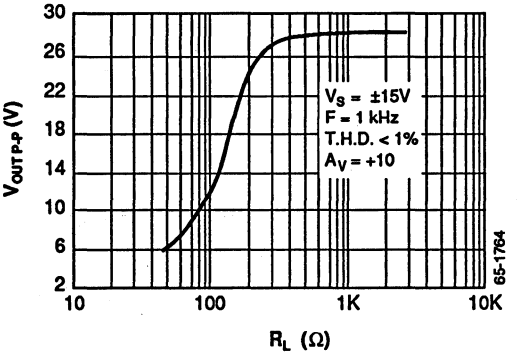


Typical Performance Characteristics (Continued)

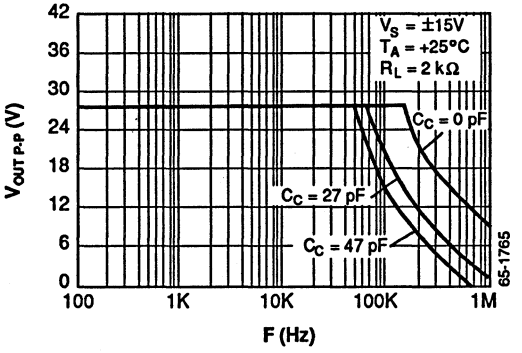
Output Voltage Swing vs. Supply Voltage



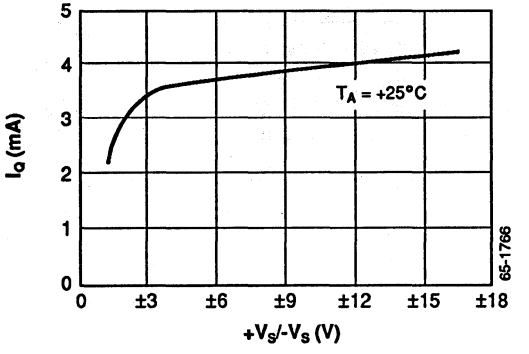
Output Voltage Swing vs. Load Resistance



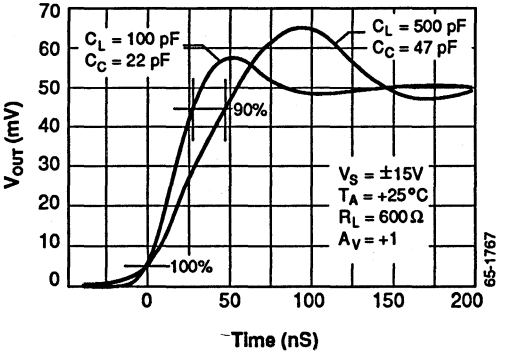
Output Voltage Swing vs. Frequency



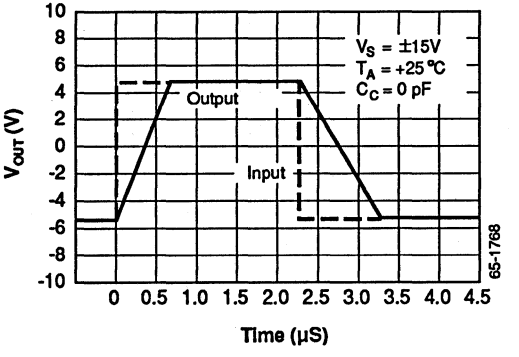
Quiescent Current vs. Supply Voltage



Transient Response
Output Voltage vs. Time



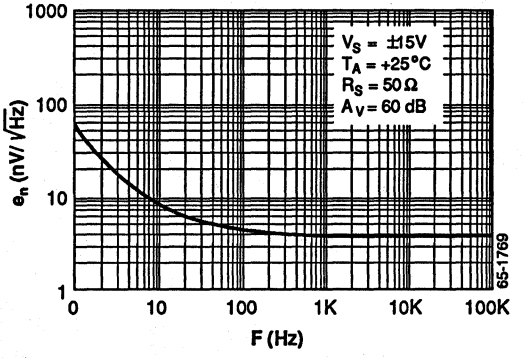
Follower Large Signal Pulse Response
Output Voltage vs. Time



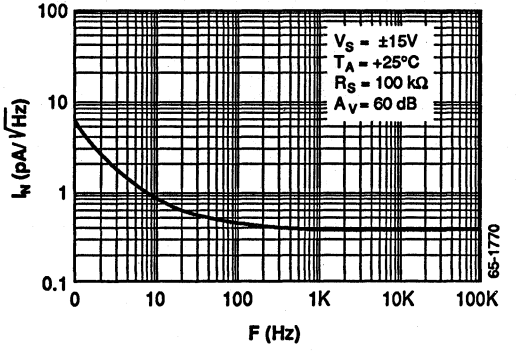
Linear

Typical Performance Characteristics (Continued)

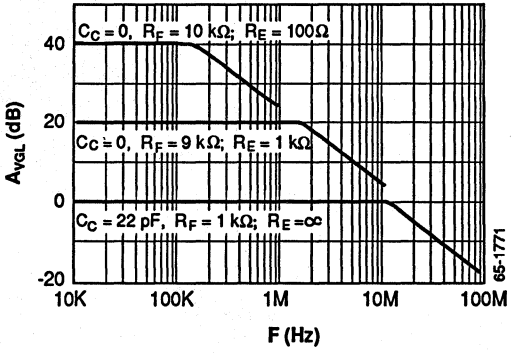
Input Noise Voltage Density vs. Frequency



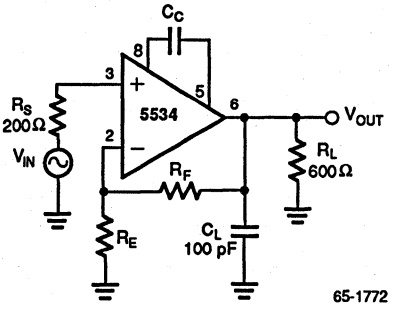
Input Noise Current Density vs. Frequency



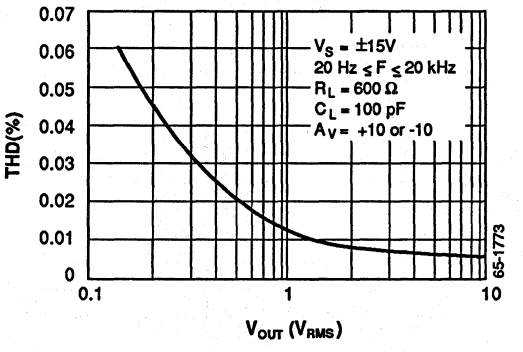
Closed Loop Gain vs. Frequency



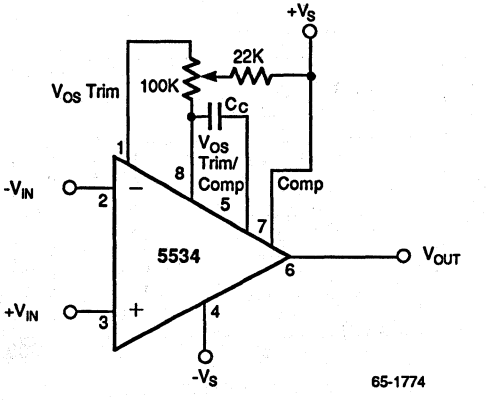
Closed Loop Frequency Response Test Circuit



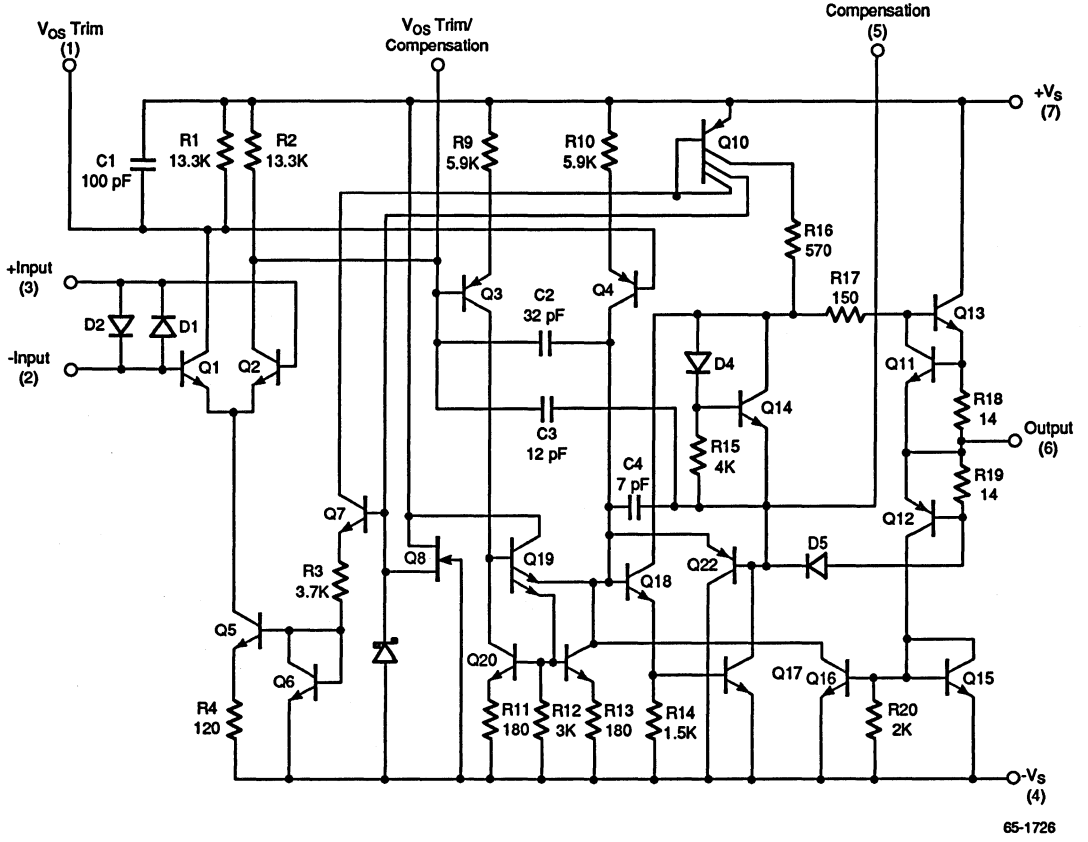
Total Harmonic Distortion vs. Output Voltage



Offset Voltage Trim Circuit



Schematic Diagram



Linear

RM741
General Purpose Operational Amplifier

Description

The RM741 integrated circuit is a high-performance, high-gain, internally compensated monolithic operational amplifier fabricated on a single silicon chip using an advanced epitaxial process.

High common-mode voltage range and absence of latch-up tendencies make the RM741 ideal for use as a voltage follower. High gain and wide ranges of operating voltages provide superior performance in integrator, summing amplifier and general feedback applications.

The RM741 is pin compatible with the LM101A. The RM741 operates over a temperature range from -55°C to +125°C.

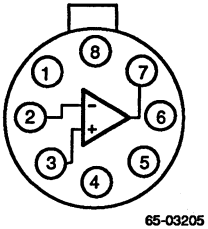
Features

- Supply voltage
  RM741 — ±22V
- Offset voltage null capability
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption

RM741

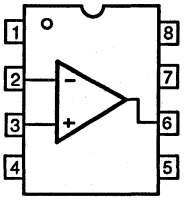
Connection Information

8-Lead
TO-99 Metal Can
(Top View)



65-03205

8-Lead
Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	V_{OS} Trim
2	- Input
3	+ Input
4	$-V_S$
5	V_{OS} Trim
6	Output
7	$+V_S$
8	NC

Ordering Information

Part Number	Package	Operating Temperature Range
RM741D	D	-55°C to +125°C
RM741D/883B	D	-55°C to +125°C
RM741T	T	-55°C to +125°C
RM741T/883B	T	-55°C to +125°C

Notes: 883B suffix denotes Mil-Std-883, Level B processing
D = 8 lead ceramic DIP
T = 8-lead metal can TO-99

Absolute Maximum Ratings

Supply Voltage
RM741 ..... ±22V
Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Output Short Circuit Duration .. Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM741 ..... -55°C to +125°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Note:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	+175°C	+175°C
Max. P_D T_A <50°C	833 mW	658 mW
Therm. Res θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage[1]	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance (Differential Mode)		0.3	2.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	50	200		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ	76	90		dB
Power Consumption			50	85	mW
Transient Response Rise Time	V_{IN} = 20 mV, R_L = 2kΩ		0.3		µS
Over shoot	$C_L \leq 100$ pF		5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/µS

Note: 1. Offset voltage is nulled by connecting a 10kΩ potentiometer across the Vos trim pins and connecting the wiper pin to $-V_S$.

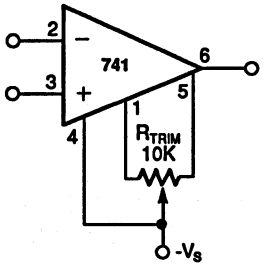
Electrical Characteristics

($V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$)

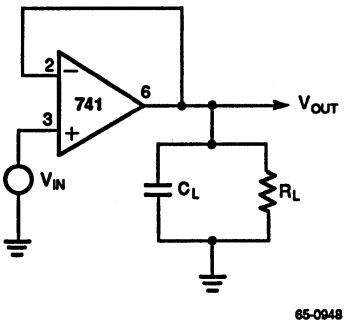
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_L \geq 10\ k\Omega$			6.0	mV
Input Offset Current				200	nA
Input Bias Current				500	nA
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10V$	25			V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$		±12		V
	$R_L \geq 2\ k\Omega$		±10		
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		70		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		76		dB
Supply Current	+125°C				mA
	-55°C				
Power Consumption	+125°C				mW
	-55°C				

Typical Performance Characteristics

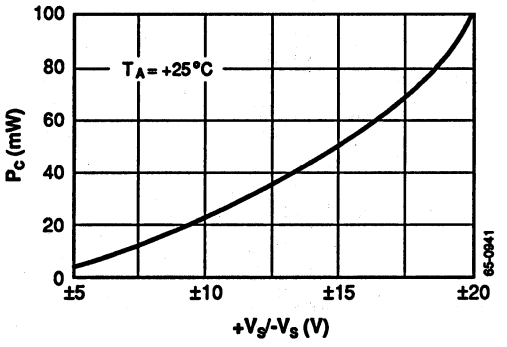
Input Offset Voltage
Trim Circuit



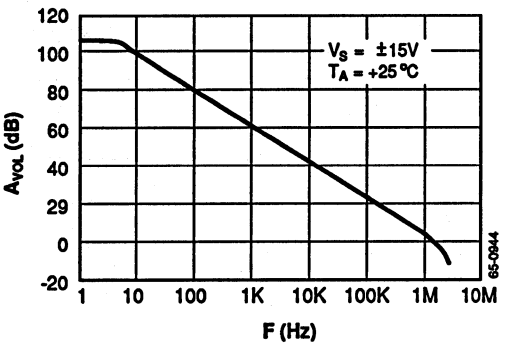
Transient Response
Test Circuit



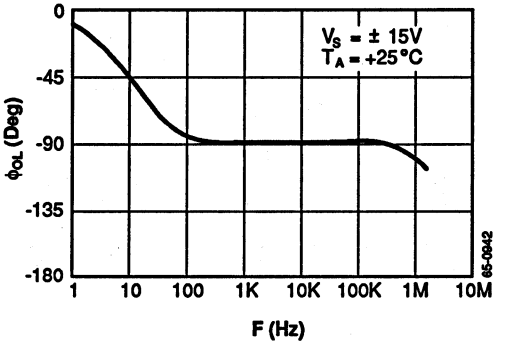
Power Consumption vs. Supply Voltage



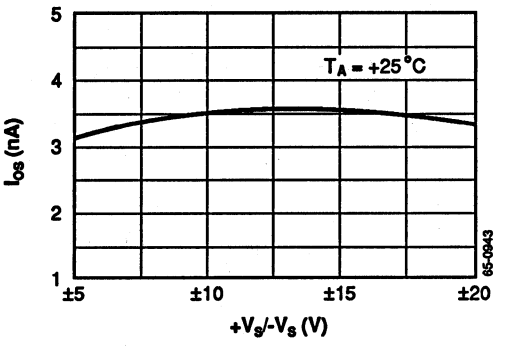
Open Loop Gain Vs. Frequency



Open Loop Phase vs. Frequency



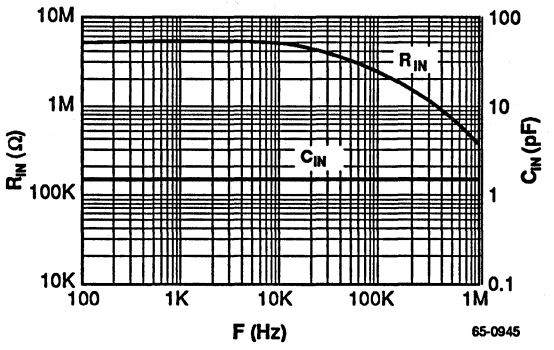
Input Offset Current vs. Supply Voltage



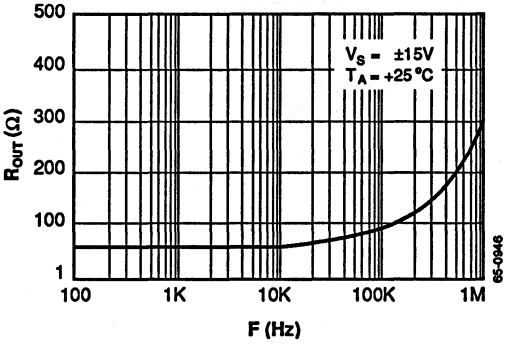
Linear

Typical Performance Characteristics (Continued)

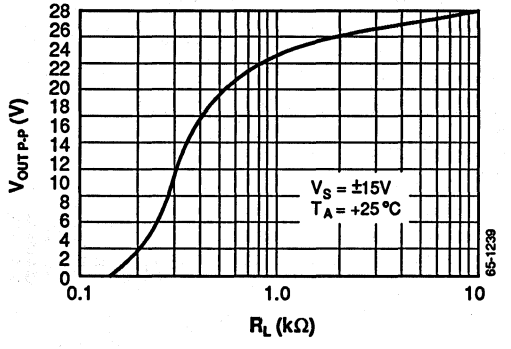
Input Resistance, Capacitance vs. Frequency



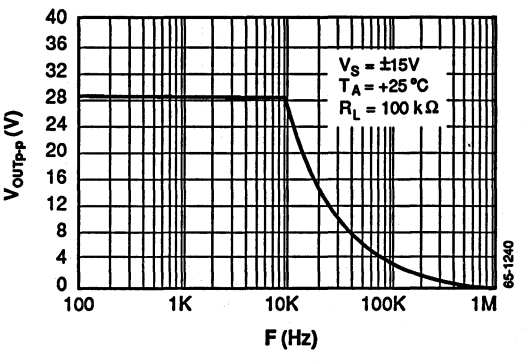
Output Resistance vs. Frequency



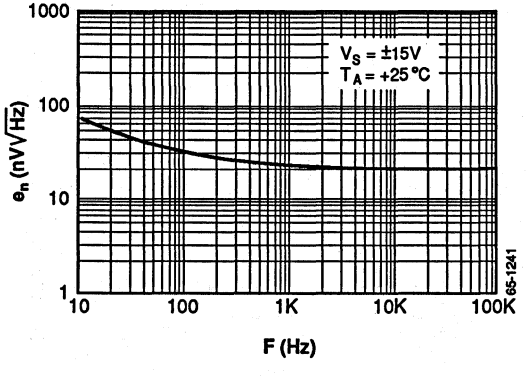
Output Voltage Swing vs. Load Resistance



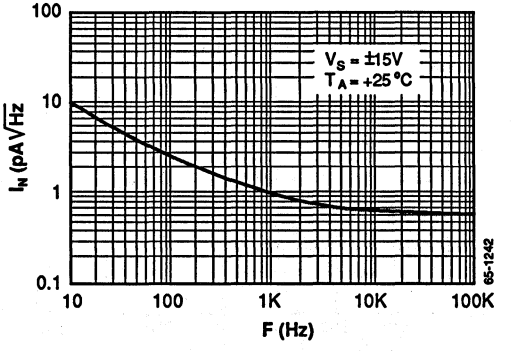
Output Voltage Swing vs. Frequency



Input Noise Voltage Density vs. Frequency

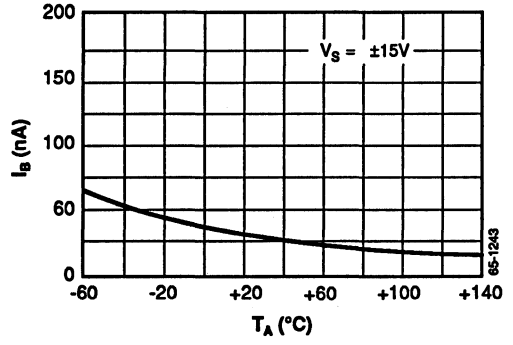


Input Noise Current Density vs. Frequency

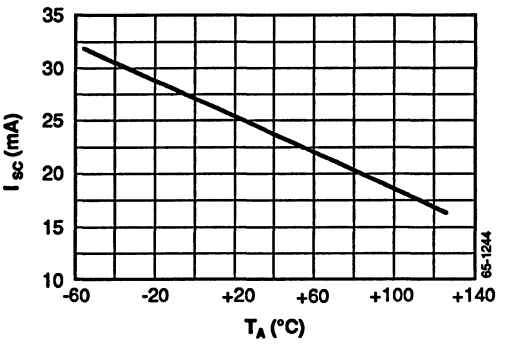


Typical Performance Characteristics (Continued)

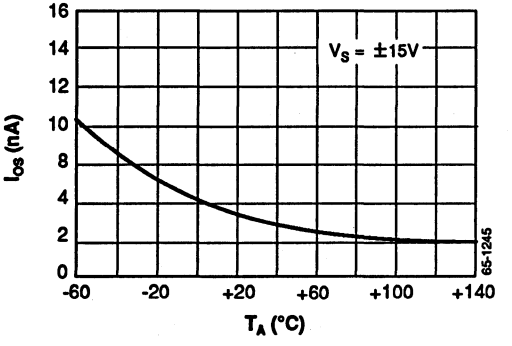
Input Bias Current vs. Temperature



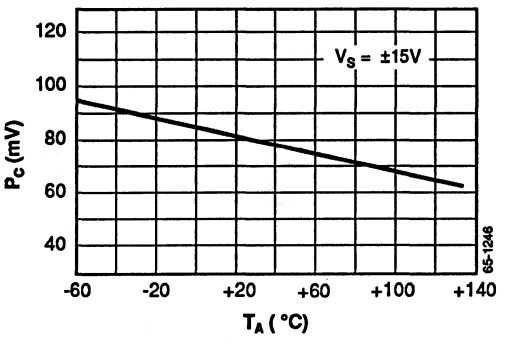
Short Circuit Current vs. Temperature



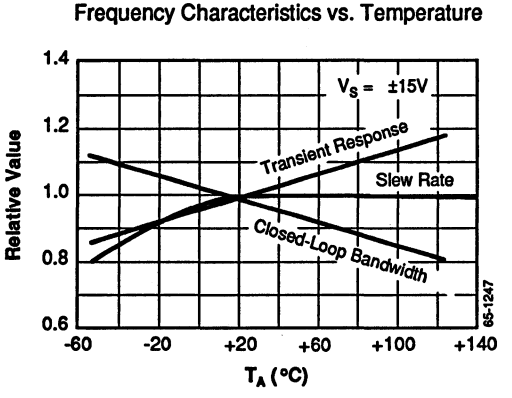
Input Offset Current vs. Temperature



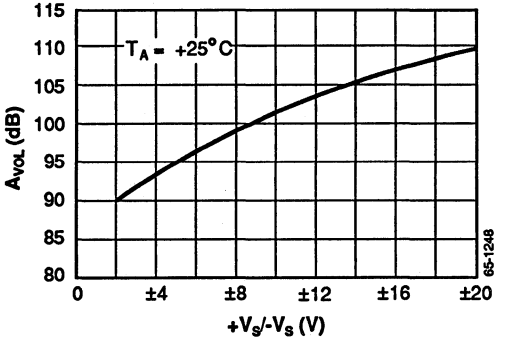
Power Consumption vs. Temperature



Frequency Characteristics vs. Temperature



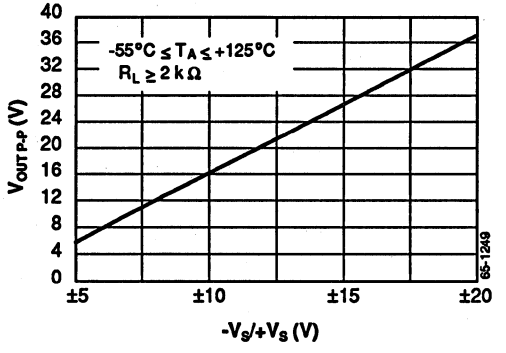
Open Loop Gain vs. Supply Voltage



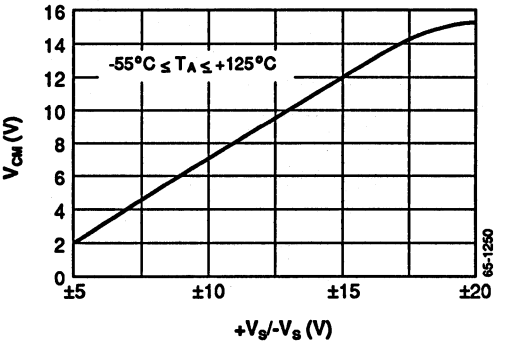
Linear

Typical Performance Characteristics (Continued)

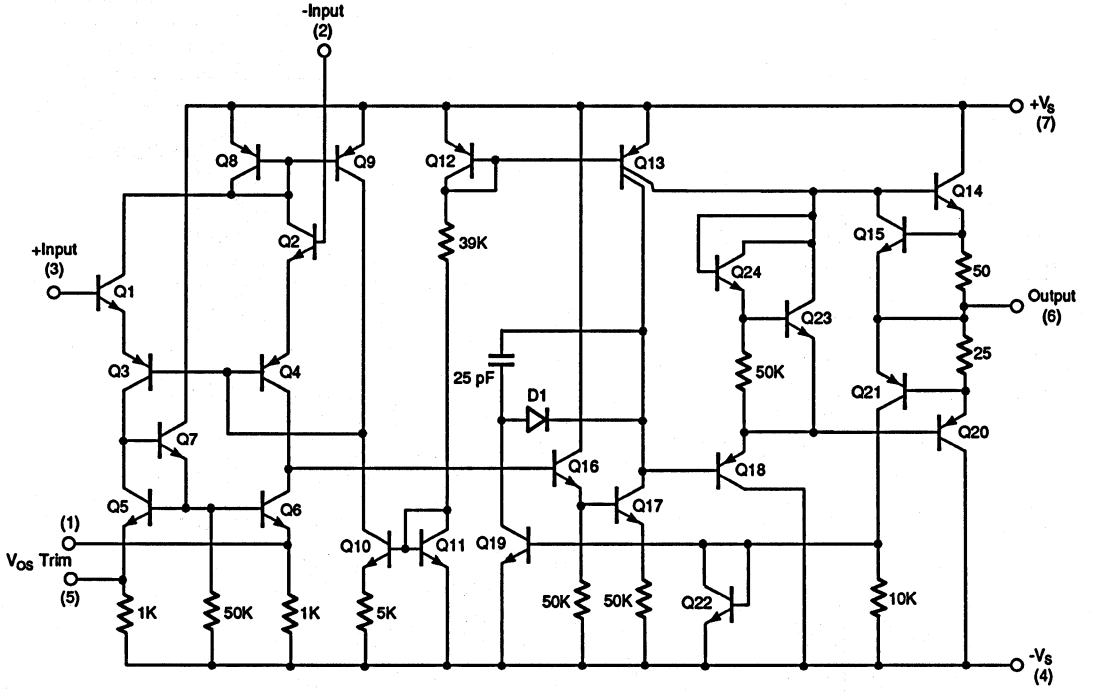
Output Voltage Swing vs. Supply Voltage



Common Mode Input Range vs. Supply Voltage



Schematic Diagram



Note: All resistance and capacitance values are nominal.

65-0940

RM747
General Purpose Dual Operational Amplifier

Description

The RM747 integrated circuit is a high gain, operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

The RM747, operates over a temperature range from -55°C to +125°C.

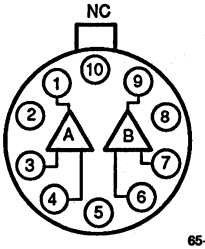
Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in all single 741 operational amplifier applications providing high packaging density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

Features

- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Connection Information

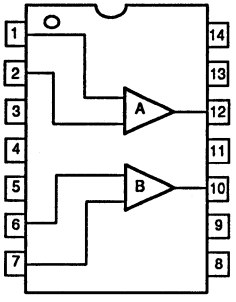
10-Lead TO-100 Metal Can
(Top View)



65-0872

Pin	Function
1	Output A
2	$-V_S$ A
3	-Input A
4	+Input A
5	$-V_S$
6	+Input B
7	-Input B
8	$+V_S$ B
9	Output B
10	NC

14-Lead Dual In-Line Package
(Top View)



65-0873

Pin	Function
1	- Input A
2	+ Input A
3	V_{OS} Trim A
4	$-V_S$
5	V_{OS} Trim B
6	+Input B
7	-Input B
8	V_{OS} Trim B
9	$+V_S$ B
10	Output B
11	NC
12	Output A
13	$+V_S$ A
14	V_{OS} Trim A

Ordering Information

Part Number	Package	Operating Temperature Range
RM747D	D	-55°C to +125°C
RM747D/883B	D	-55°C to +125°C
RM747T	T	-55°C to +125°C
RM747T/883B	T	-55°C to +125°C

Notes:
883B suffix denotes Mil-Std-883, Level B processing
D = 14-lead ceramic DIP
T = 10-lead metal can TO-100

Absolute Maximum Ratings

Supply Voltage
RM747 ..... ±22V
Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM747 ..... -55°C to +125°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Thermal Characteristics

	14-Lead Ceramic DIP	10-Lead TO-100 Metal Can
Max. Junction Temp.	+175°C	+175°C
Max. P_D T_A <50°C	1042 mW	658 mW
Therm. Res θ_{JC}	60°C/W	50°C/W
Therm. Res. θ_{JA}	120°C/W	190°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance (Diff. Mode)		0.3	2.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	50	200		V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$	76	90		dB
Power Consumption			100	170	mW
Transient Response					
Rise Time	V_{IN} = 20 mV, R_L = 2 kΩ		0.3		µS
Overshoot	$C_L \leq 100$ pF		5.0		%
Slew Rate	$R_L \geq 2\ k\Omega$		0.5		V/µS
Channel Separation	F = 1 kHz		98		dB

Linear

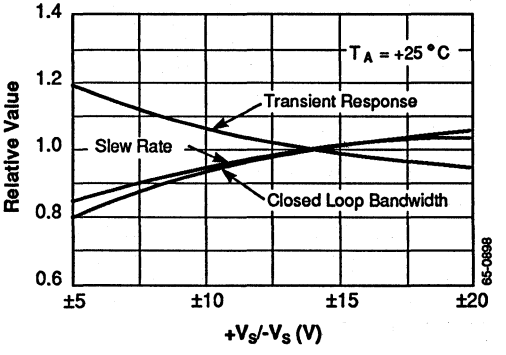
Electrical Characteristics

(V_S = ± 15V, -55°C ≤ T_A ≤ +125°C)

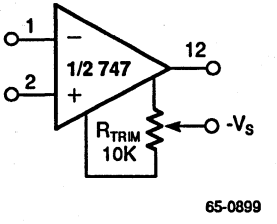
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	R_S ≤ 10 kΩ			6.0	mV
Input Offset Current	T_A = +125°C, T_A = +70°C			200	nA
	T_A = -55°C T_A = 0°C			500	nA
Input Bias Current	T_A = +125°C, T_A = +70°C			500	nA
	T_A = -55°C, T_A = 0°C			1500	nA
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	25			V/mV
Output Voltage Swing	R_L ≥ 10K	±12			V
	R_L ≥ 2 kΩ	±10			V
Common Mode Rejection Ratio	R_S ≤ 10 kΩ	70			dB
Power Supply Rejection Ratio	R_S ≤ 10 kΩ	76		150	dB
Power Consumption	T_A = +125°C			150	mW
	T_A = -55°C			200	mW
Input Voltage Range		±12			V

Typical Performance Characteristics

Frequency Characteristics vs. Supply Voltage



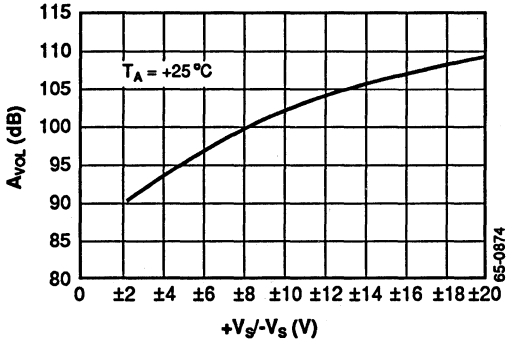
Input Offset Voltage Trim Circuit



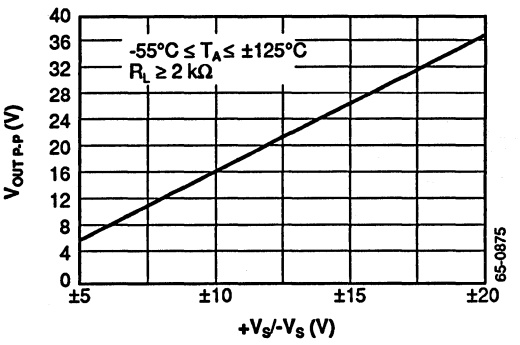
Note: Pin numbers shown are for 14-lead packages

Typical Performance Characteristics (Continued)

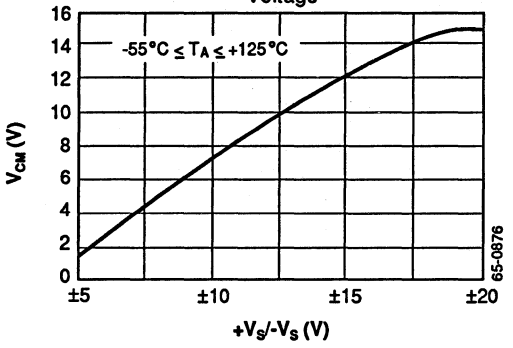
Open Loop Gain vs. Supply Voltage



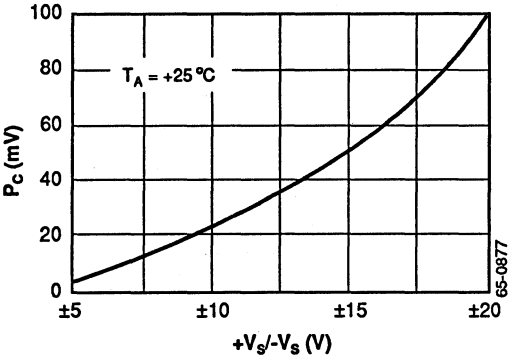
Output Voltage Swing vs. Supply Voltage



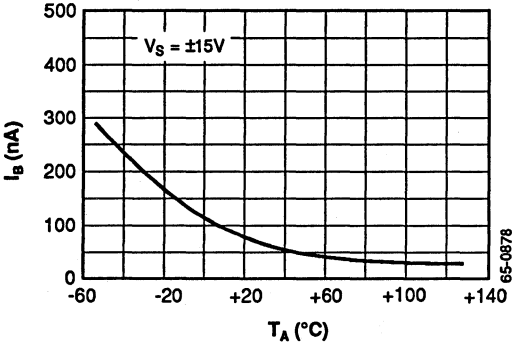
Common Mode Input Range vs. Supply Voltage



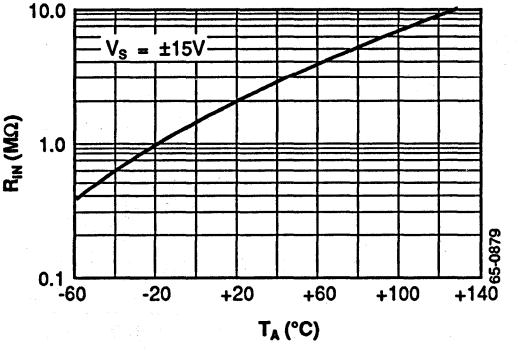
Power Consumption vs. Supply Voltage



Input Bias Current vs. Temperature



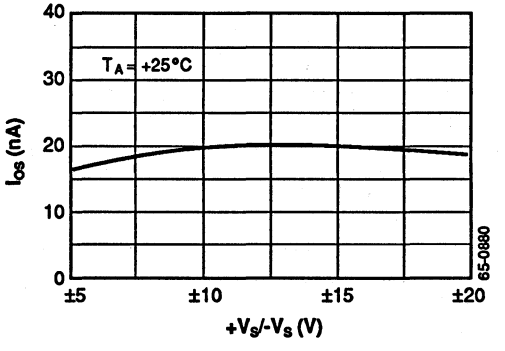
Input Resistance vs. Temperature



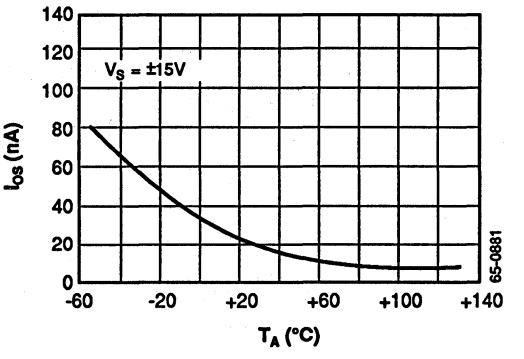
Linear

Typical Performance Characteristics (Continued)

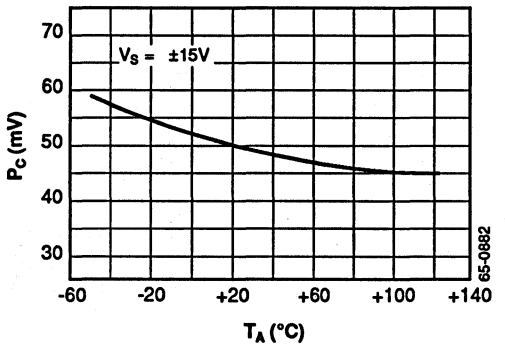
Input Offset Current vs. Supply Voltage



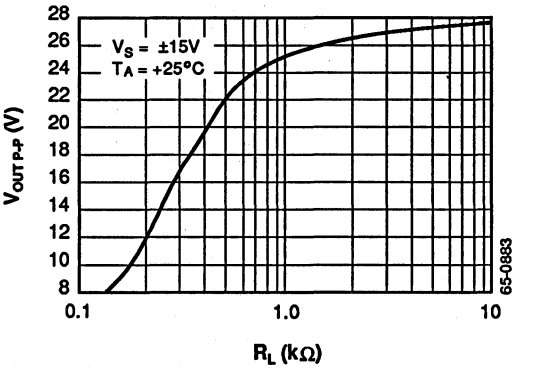
Input Offset Current vs. Temperature



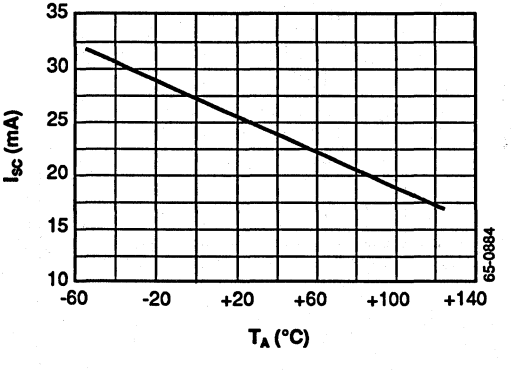
Power Consumption vs. Temperature



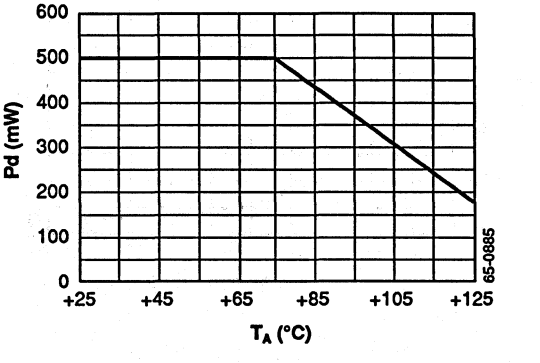
Output Voltage Swing vs. Load Resistance



Short Circuit Current vs. Temperature

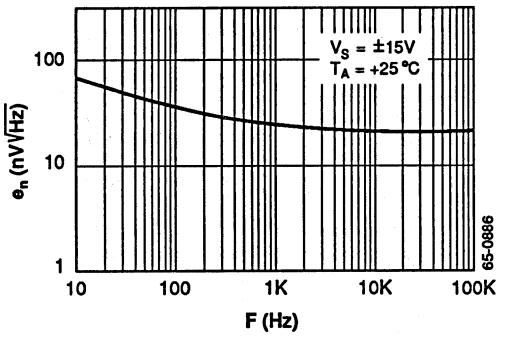


Absolute Maximum Power Dissipation vs. Temperature

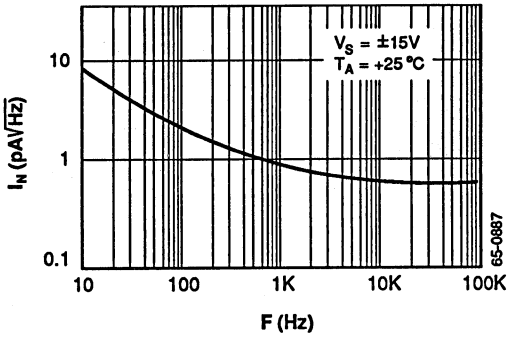


Typical Performance Characteristics (Continued)

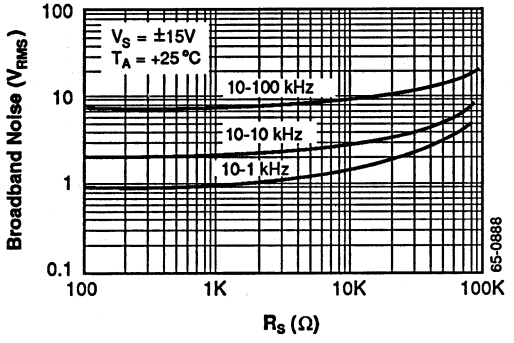
Input Noise Voltage Density vs. Frequency



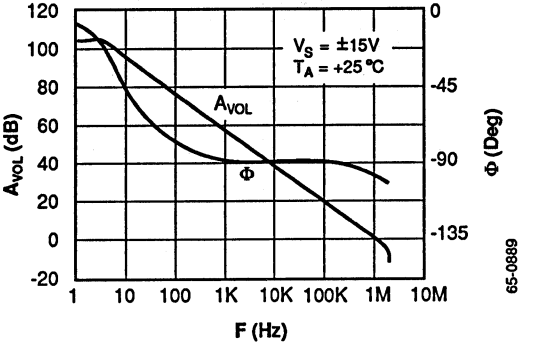
Input Noise Current Density vs. Frequency



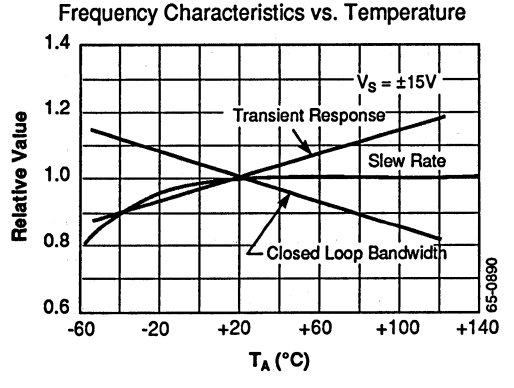
Broadband Noise Referred to Input vs. Source Resistance



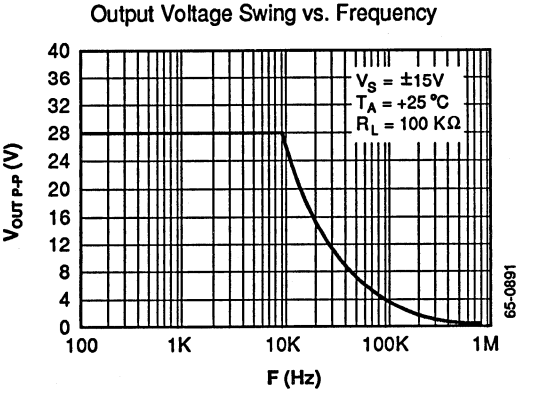
Open Loop Gain, Phase vs. Frequency



Frequency Characteristics vs. Temperature



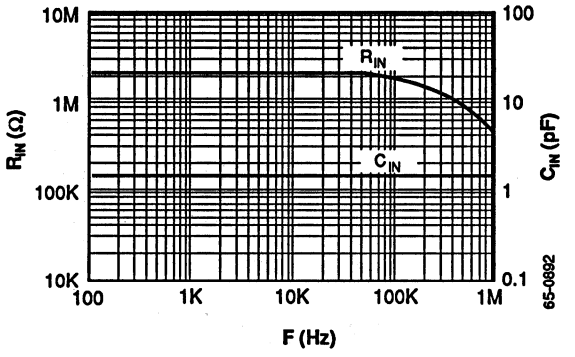
Output Voltage Swing vs. Frequency



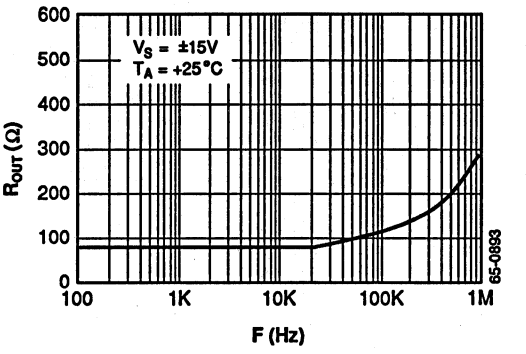
Linear

Typical Performance Characteristics (Continued)

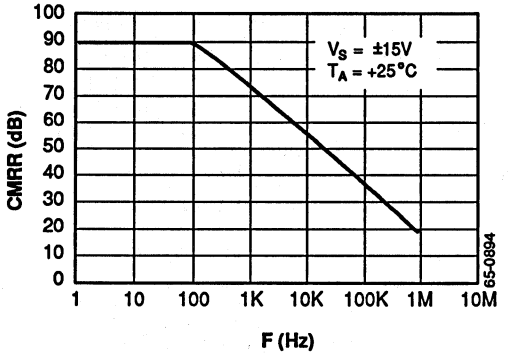
Input Resistance, Capacitance vs. Frequency



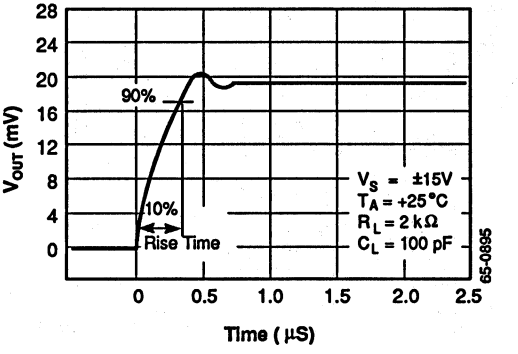
Output Resistance vs. Frequency



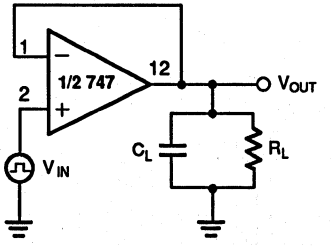
CMRR vs. Frequency



Transient Response Output Voltage vs. Time



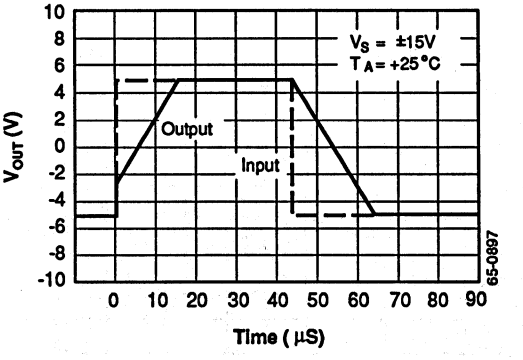
Transient Response Test Circuit



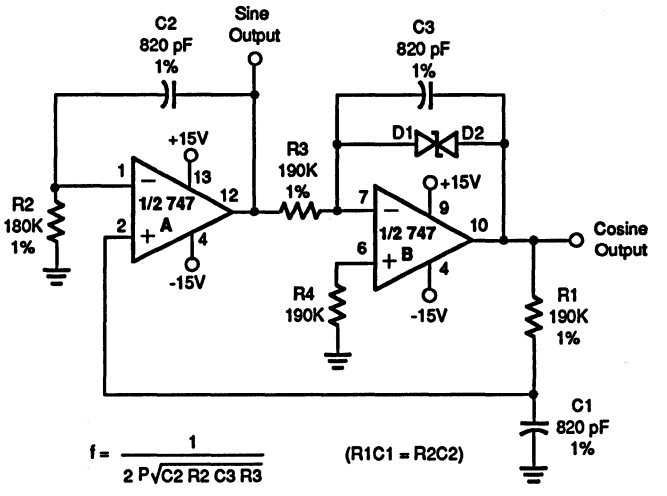
Note: Pin numbers shown are for 14-lead packages

65-0896

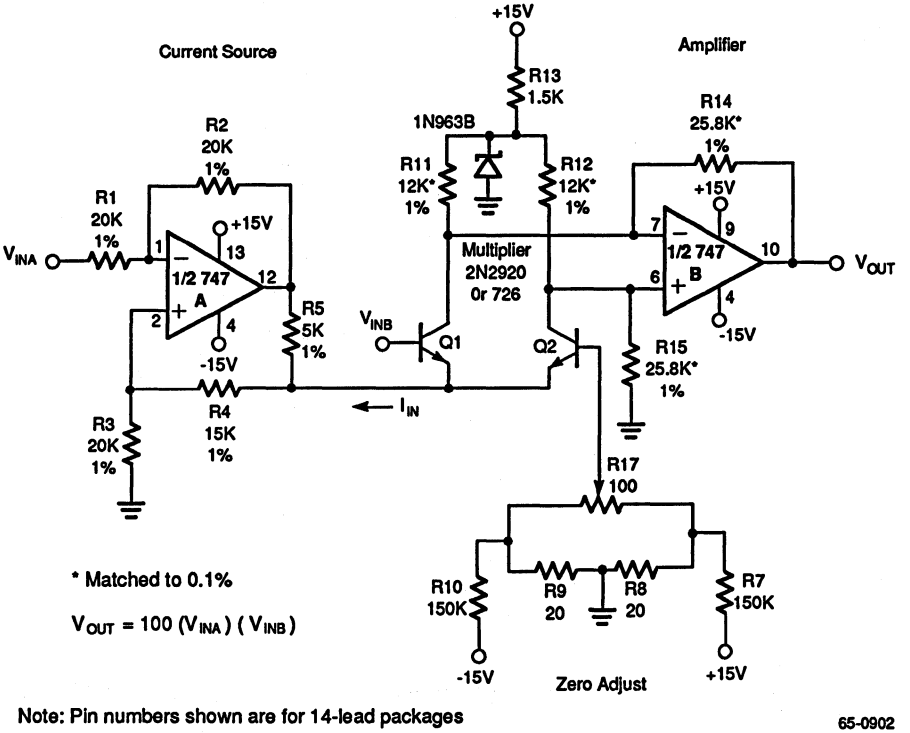
Follower Large Signal Pulse Response
Ouput Voltage vs. Time



Typical Applications



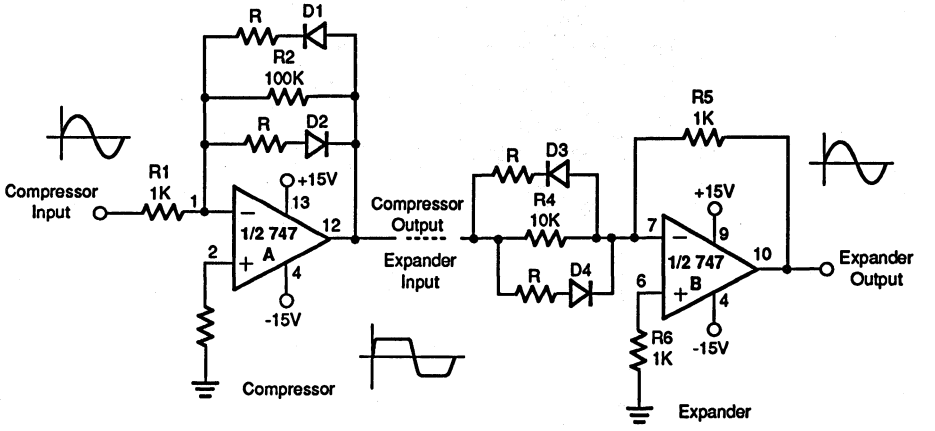
Quadrature Oscillator



Analog Multiplier

Linear

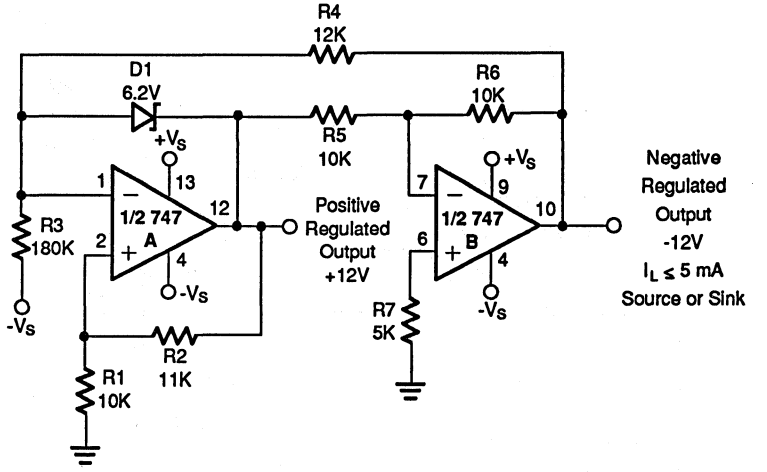
Typical Applications (Continued)



Maximum compressor expansion ratio = R1/R (10 kΩ> R ≥ 0)
Note: Diodes D1 through D4 are matched FD6666 or equivalent

65-0903

Compressor/Expander Amplifiers



$$\text{Positive Output} = V_{D1} \times \frac{R1 + R2}{R2}$$

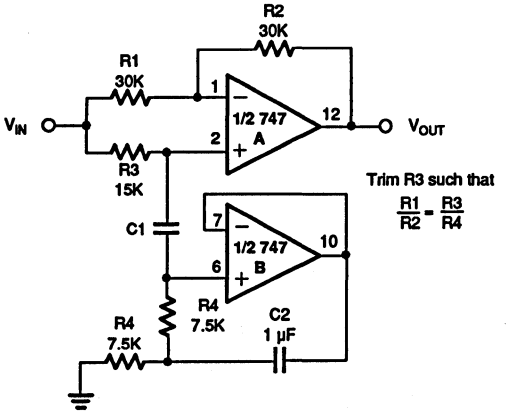
$$\text{Negative Output} = - \text{Positive Output} \times \frac{R6}{R5}$$

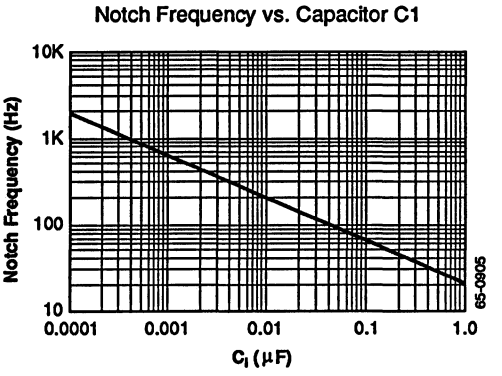
65-0904

Note: Pin numbers shown are for 14-lead packages.

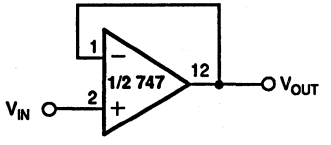
Tracking Positive and Negative Voltage References

Typical Applications (Continued)





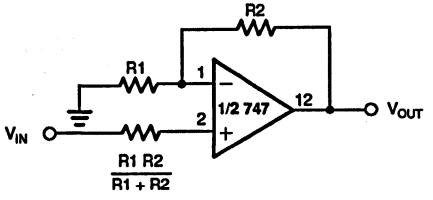
Notch Filter Using the 747 as a Gyrator



R_{IN} = 400 MΩ
C_{IN} = 1 pF
$R_{OUT} \leq 1\Omega$
BW = 1 MHz

65-0906

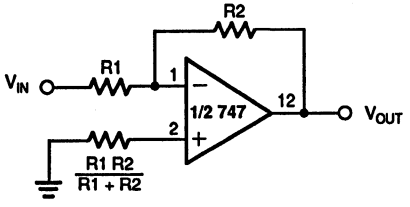
Unity Gain Voltage Follower



Gain	R1	R2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 kΩ	9.9 kΩ	10 kHz	280 MΩ
1000	100 kΩ	99.9 kΩ	1 kHz	80 MΩ

65-0907

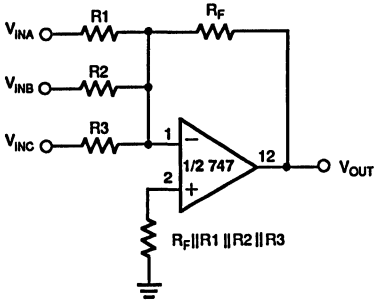
Non-Inverting Amplifier



Gain	R1	R2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 kΩ	100 kΩ	1 kHz	100Ω

65-0908

Inverting Amplifier



$V_{OUT} = -V_{INA}\left(\frac{R_F}{R1}\right) - V_{INB}\left(\frac{R_F}{R2}\right) - V_{INC}\left(\frac{R_F}{R3}\right)$

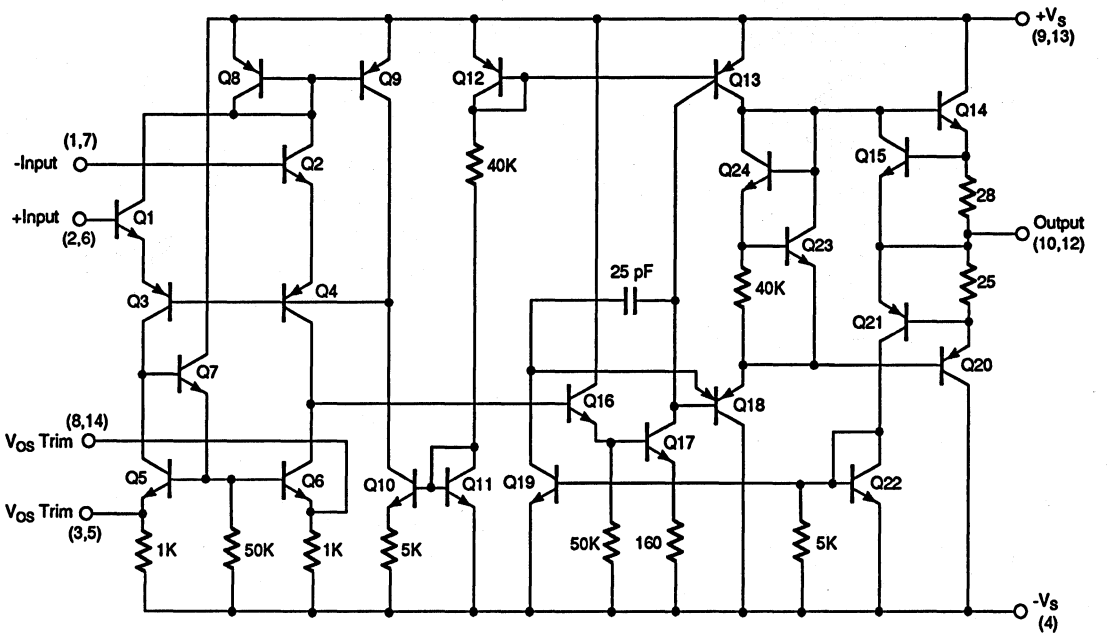
Note: Pin numbers shown are for 14-lead packages

65-0909

Weighted Averaging Amplifier

Linear

Schematic Diagram (1/2 Shown)



Note: Pin numbers shown are for 14-lead packages

65-0871

LM139/139A, LM339
Single Supply Quad Comparators

Description

These devices offer higher frequency operation and faster switching than can be had from internally compensated quad op amps. Intended for single supply applications, the Darlington PNP input stage allows them to compare voltages that include ground. The two-stage common-emitter output circuit provides gain and output sink capacity of 3.2 mA at an output level of 400 mV. The output collector is left open, permitting the designer to drive devices in the range of 2V to 36V.

They are intended for applications not needing response time less than 1 µs, but demanding excellent op amp input parameters to offset voltage, current and bias current, to ensure accurate comparison with a reference voltage.

Features

- Input common mode voltage range includes ground
- Wide single supply voltage range — 2V to 36V
- Output compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Very low supply current drain (0.8 mA) independent of supply voltage

Absolute Maximum Ratings

Supply Voltage ..... + 36V or ±18V
Differential Input Voltage 36V
Input Voltage Range ..... -0.3 to +36V(2)
Output Short Circuit to Ground (1) ..... Continuous
Input Current (V_{IN} < -0.3V)(2) ..... 50 mA
Operating Temperature Range
LM139 ..... -55°C to +125°C
LM339 ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature
SO-14, 10 sec. ..... +260°C
DIP, 60 sec. ..... +300°C

See Notes.

Ordering Information

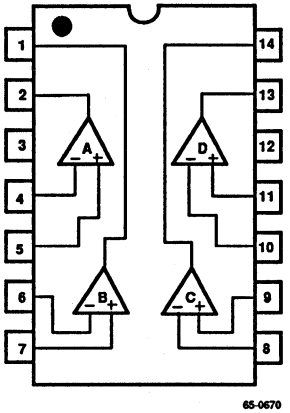
Part Number	Package	Operating Temperature Range
LM339M	M	0°C to +70°C
LM339N	N	0°C to +70°C
LM139D	D	-55°C to +125°C
LM139D/883B	D	-55°C to +125°C
LM139AD	D	-55°C to +125°C
LM139AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
M = 14-lead plastic SOIC
N = 14-lead ceramic DIP
D = 14-lead ceramic DIP

Thermal Characteristics

	14-Lead Plastic SO	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+125°C	+175°C
Max. P_D T_A <50°C	300 mW	468 mW	1042mW
Therm. Res θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Connection Information



Pin	Function	Pin	Function
1	Output B	8	-Input C
2	Output A	9	+Input C
3	$+V_S$	10	-Input D
4	-Input A	11	+Input D
5	+Input A	12	Ground
6	-Input B	13	Output D
7	+Input B	14	Output C

Electrical Characteristics

(V_S = +5V, see note 3)

Parameters	Test Conditions	LM139A			Units
		Min	Typ	Max	
Input Offset Voltage	T_A = +25°C (8)		±1.0	±2.0	mV
Input Bias Current	Output in Linear Range T_A = +25°(4), V_{CM} = 0V		25	100	nA
Input Offset Current	T_A = +25°C, V_{CM} = 0V		±3.0	±25	nA
Input Voltage Range	T_A = +25°C(5), V_S = 30V	0		$+V_S$ -1.5	V
Supply Current	R_L = ∞ on all comparators, T_A = +25°C		0.8	2.5	mA
Large Signal Voltage Gain	R_L = ∞, $+V_S$ = 30V, R_L ≥ 15 kΩ, $+V_S$ = +5V (to support large V_{OUT} swing), T_A = +25°C	50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1 kΩ, T_A = +25°C		300		ns
Response Time	V_{RL} = 5V, R_L = 5.1 kΩ, T_A = +25°C (6)		1.3		µs
Output Sink Current	V_{IN-} ≥ 1V, V_{IN+} = 0 V_{OUT} ≤ 1.5V, T_A = +25°C	6.0	16		mA
Saturation Voltage	V_{IN-} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA, T_A = 25°C		250	400	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 5V, T_A = +25°C		0.1		µA
Input Offset Voltage	Note 8			±4.0	mV
Input Offset Current	V_{CM} = 0V			±100	nA
Input Bias Current	V_{CM} = 0V			300	nA
Input Voltage Range	$+V_S$ = 30V	0		$+V_S$ -2.0	V
Saturation Voltage	V_{IN-} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA			700	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 30V			1.0	µA
Differential Input Voltage (10)	$V_{IN±}$ ≥0V, (or $-V_S$, if used) (7)			36	V

See Notes.

Electrical Characteristics

($+V_S$ = +5V, see note 3)

Parameters	Test Conditions	LM139			LM339			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = +25°C (8)		±2.0	±5.0		±2.0	±5.0	mV
Input Bias Current	Output in Linear Range T_A = +25°C (4), V_{CM} = 0V		25	100		25	250	nA
Input Offset Current	T_A = +25°C, V_{CM} = 0V		±3.0	±25		±5.0	±50	nA
Input Voltage Range	T_A = +25°C (5), $+V_S$ = 30V	0		$+V_S$ -1.5	0		$+V_S$ -1.5	V
Supply Current	R_L = ∞ on all comparators, T_A = +25°C		0.8	2.5		0.8	2.5	mA
Large Signal Voltage Gain	R_L = ∞, $+V_S$ = 30V, R_L ≥ 15 kΩ, $+V_S$ = +5V (to support large V_{OUT} swing), T_A = +25°C	25	200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1 kΩ, T_A = +25°C		300			300		ns
Response Time	V_{RL} = 5V, R_L = 5.1 kΩ, T_A = +25°C (6)		1.3			1.3		µS
Output Sink Current	V_{IN-} ≥ 1V, V_{IN+} = 0, V_{OUT} ≤ 1.5V, T_A = +25°C	6.0	16		6.0	16		mA
Output Voltage, V_{OL}	V_{IN-} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA, T_A = +25°C		250	400		250	400	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 5V, T_A = +25°C		0.1			0.1		µA
Input Offset Voltage	Note 8			±9.0			±9.0	mV
Input Offset Current				±100			±150	nA
Input Bias Current	V_{CM} = 0V			300			400	nA
Input Voltage Range	V_{CM} = 30V	0		$+V_S$ -2.0	0		$+V_S$ -2.0	V
Output Voltage V_{OL}	V_{IN-} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA			700			700	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 30V			1.0			1.0	µA
Differential Input Voltage (10)	$V_{IN\pm}$ ≥ 0V (or $-V_S$, if used) (7)			36			36	V

See Notes.

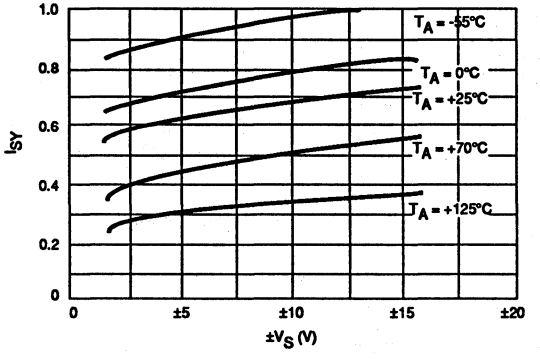
Electrical Characteristics (Continued)

Notes:

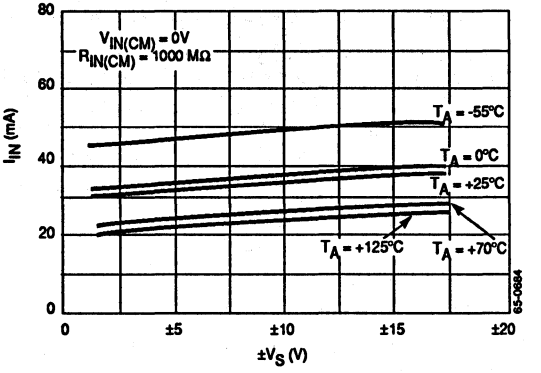
1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of $+V_S$.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
3. These specifications apply for $+V_S = 5V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. The LM339 temperature specifications are limited to $0°C \leq T_A \leq +70°C$.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +30V without damage.
6. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained. See Typical Performance Characteristics section.
7. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
8. At output switch point, $V_{OUT} = 1.4V$, $R_S = 0\Omega$ with $+V_S$ from 5V to 30V; and over the full input common mode range (V_{OUT} to $+V_S$ -1.5V).
9. For input signals that exceed $+V_S$, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.
10. Guaranteed by design.

Typical Performance Characteristics

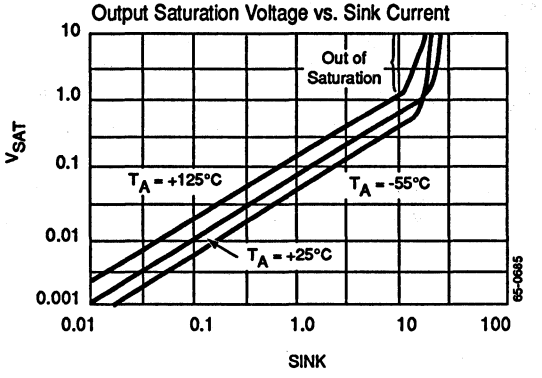
Supply Current vs. Supply Voltage

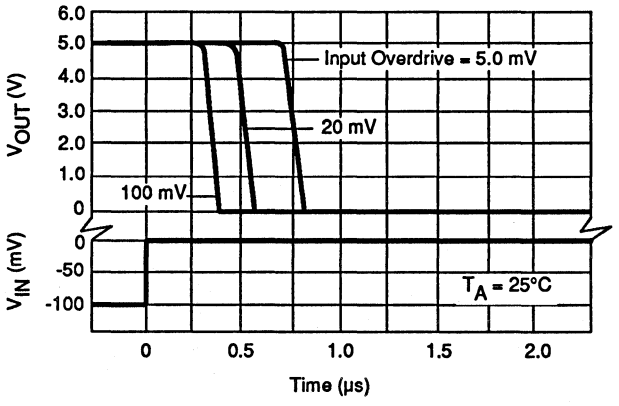


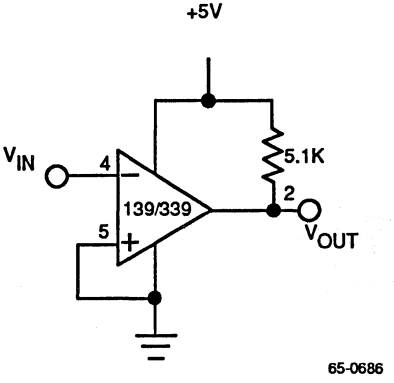
Input Current vs. Supply Voltage



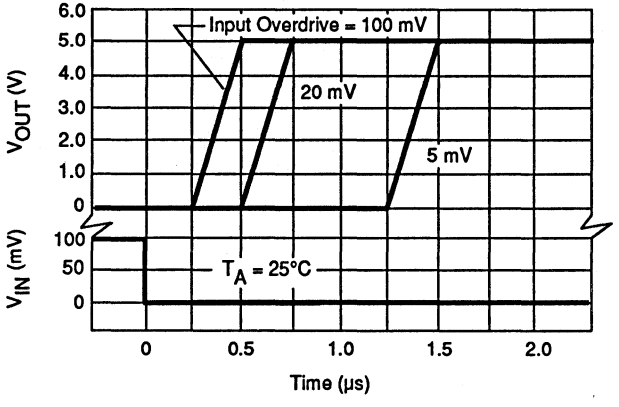
Output Saturation Voltage vs. Sink Current

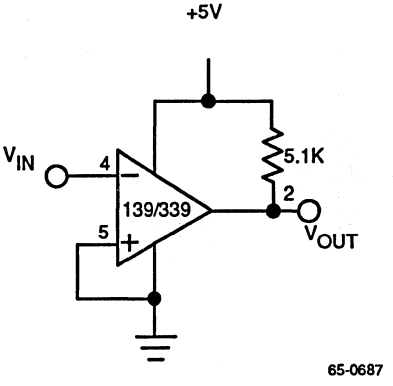






Input Overdrive Response Time

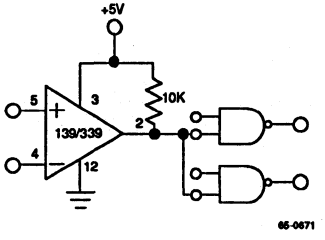




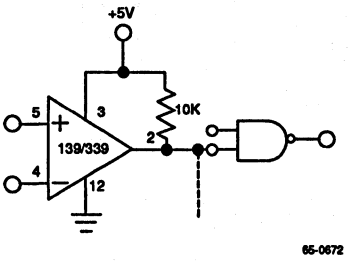
Input Overdrive Response Time

Linear

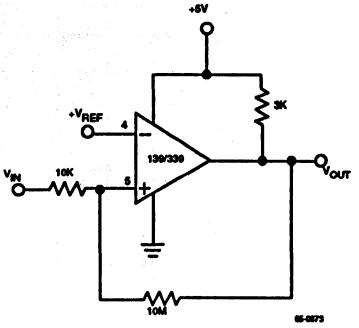
Typical Applications — Single Supply ($+V_S$ = +15V)



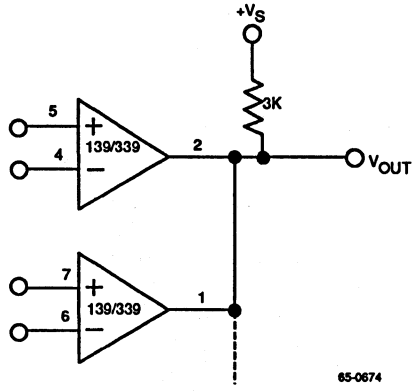
Driving TTL



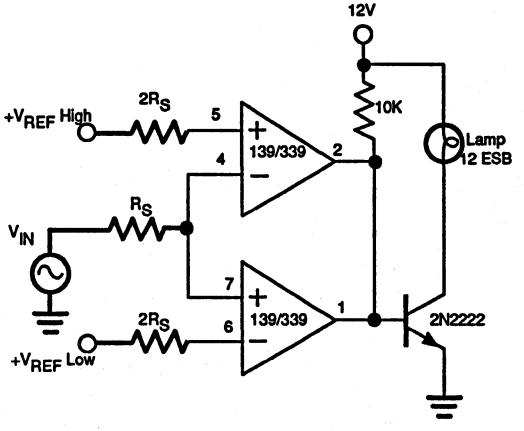
Driving CMOS



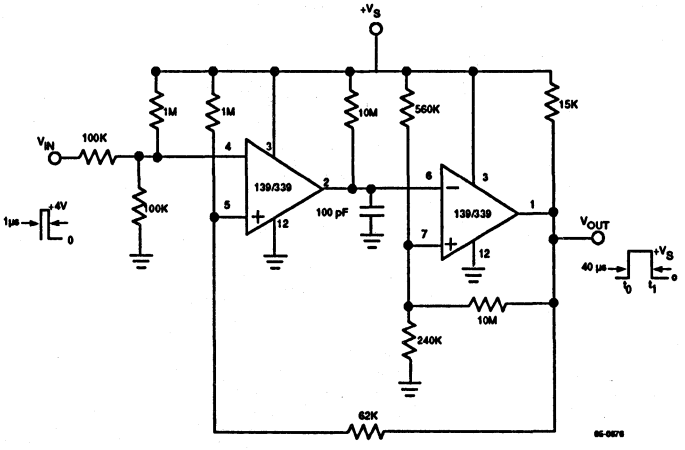
Comparator with Hysteresis



ORing the Output

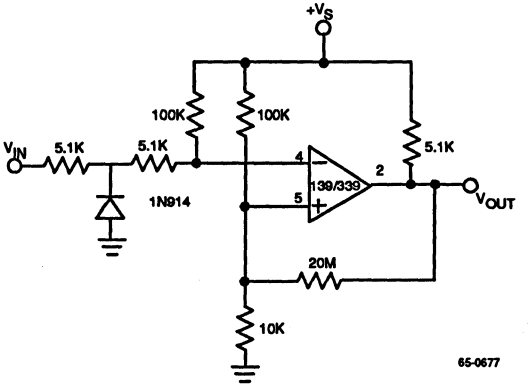


Limit Comparator 65-0675

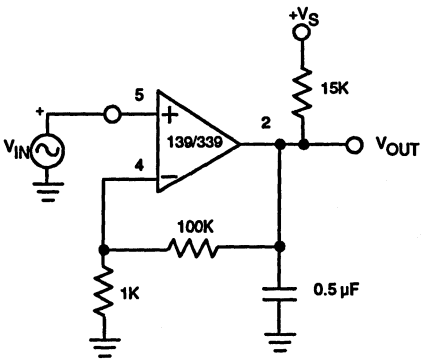


One-Shot Multivibrator with Input Lock Out

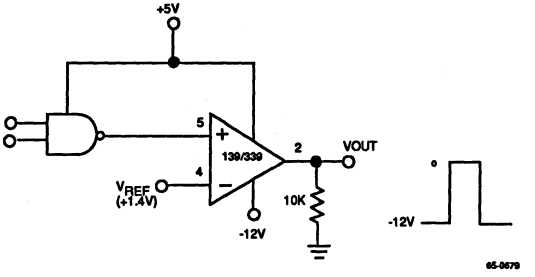
Typical Applications — Single Supply (Continued)



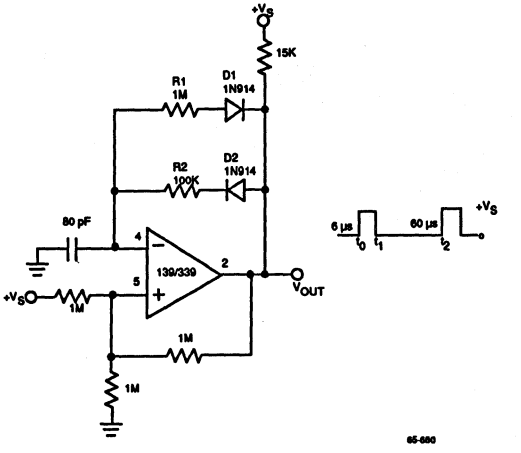
Zero Crossing Detector (Single Power Supply)



Low Frequency Op Amp



TTL to MOS Logic Converter



Pulse Generator

RM4805
Precision High Speed Latching Comparator

Description

The RM4805 is an ideal comparator for high speed, high precision applications. The input errors are factor trimmed to less than 1/10 LSB of a 12-bit, 10V system. The latch function allows the system designer additional flexibility. When the latch input is a TTL low, the comparator functions normally. When the input is raised to a TTL high, the comparator output is latched in its current state.

The RM4805 is ideal for ultra precise, very fast system designs. Typical applications include successive approximation A/D converters of 12 or more bits, zero crossing detectors, high speed sampling and window detectors.

The RM4805 high speed comparator is functionally equivalent to the popular comparators AM686, SE527, CMP-05 and μA760. Propagation delay is 35 ns with a 1/2 LSB overdrive in a 12-bit, 10V system.

Features

- 22 ns propagation delay
- Low offset voltage — 100 μV
- Low offset current — 10 nA
- TTL compatible latch
- TTL output

Absolute Maximum Ratings

Supply Voltage ..... +5.5V/-16.5V
Differential Input Voltage 1V
Internal Power Dissipation[1] ..... 500 mW
Input Voltage ..... ±4V
Storage Temperature Range ..... -65°C to +150 °C
Operating Temperature Range
RM4805 ..... -55°C to +125°C
RC4805 ..... 0°C to +70°C
Lead Soldering Temperature (60 sec.) ..... +300°C

Note:
1 See table of Thermal Characteristics for maximum ambient temperature derating factor.

Ordering Information

Part Number	Package	Operating Temperature Range
RM4805D/883B	D	-55°C TO +125°C
RM4805AD/883B	D	-55°C TO +125°C

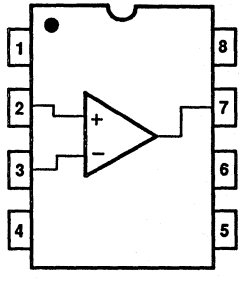
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
D = 8-lead ceramic DIP

Thermal Characteristics

	8-Lead Ceramic DIP
Max. Junction Temp.	+175°C
Max. P_D T_A <50°C	833 mW
Therm. Res θ_{JC}	45°C/W
Therm. Res. θ_{JA}	150°C/W
For T_A >50°C Derate at	8.33 mW/°C

Connection Information

8-Lead
Dual In-Line Package
(Top View)



65-0506

Pin	Function
1	Ground
2	+ Input
3	- Input
4	$-V_S$
5	NC
6	Latch Enable
7	Output
8	$+V_S$

Electrical Characteristics

(V_S = ±5V and T_A = +25°C, Latch Enable = 0V unless otherwise noted)

Parameters	Test Conditions	RM4805A			RM4805			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 50\Omega$		100	250		250	600	µV
Input Offset Current			10	80		25	150	nA
Input Bias Current			0.7	1.2		0.9	1.8	µA
Large Signal Voltage Gain		15	50		10	40		V/mV
Output Voltage Swing	V_{IN} > 10 mV, I_{OUT} = 200 µA	2.4	2.7		2.4	2.7		V
	V_{IN} < -10 mV, I_{SINK} = 8 mA		0.3	0.4		0.3	0.4	V
Input voltage Range		±2.2	±2.7		±2.0	±2.7		V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, V_{CM} = Min Input Voltage Range	86			84			dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$, $+V_S$ = +5V, -5.25V ≤ $-V_S$ ≤ -4.75V and $-V_S$ = -5V, +4.75V ≤ $+V_S$ ≤ +5.25V	86			84			dB
	$R_S \leq 50\Omega$ $+V_S$ = +5V, -5V ≤ $-V_S$ ≤ -15V	86			84			dB
Supply Current (Positive)	$V_{OUT} \leq 0.4V$		11	16		13	18	mA
Supply Current (Negative)	$V_{OUT} \leq 0.4V$	-16	-12		-18	-13		mA
Power Consumption	$V_{OUT} \leq 0.4V$		115	160		130	180	mW
Propagation Delay*	100 mV Step, V_{OD} = 5 mV		22	35		22	35	ns
	100 mV Step, V_{OD} = 1.2 mV		35			35		ns
Latch								
Enable Time	V_{OD} = 5 mV		16			16		ns
Disable Time	V_{OD} = 5 mV		22			22		ns
Latch								
High Voltage		2.0			2.0			V
Low Voltage				0.8			0.8	V
Latch								
High Current	V_{LH} = 3.0V			40			75	µA
Low Current	V_{LL} = 0.8V			10			20	µA

*Minimize lead length by soldering the 4805 directly to PC board. The use of sockets may cause oscillations from stray capacitive coupling.

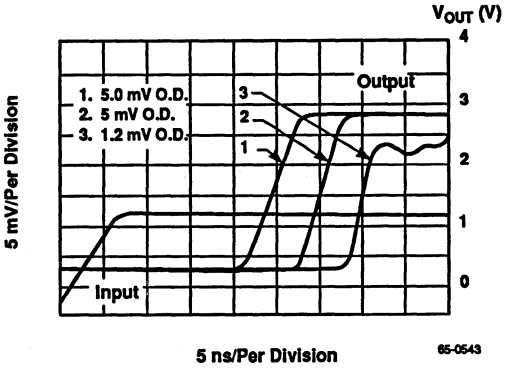
Electrical Characteristics

(V_S = ±5V, RM = -55°C ≤T_A ≤ +125°C; RC = 0°C ≤ T_A ≤ +70°C, Latch Enable = 0V unless otherwise noted)

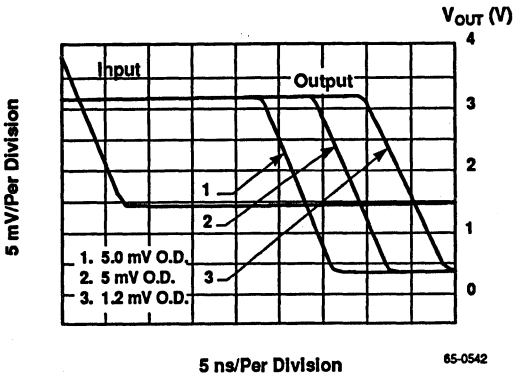
Parameters	Test Conditions	RC4805E/RM4805A			RC4805/RM4805			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤ 50Ω		0.25	0.80		0.50	1.5	MV
Average Input Offset Voltage Drift	(Note 1)		1.5	5.0		2.5	7.5	µV/°C
Input Offset Current				200			400	nA
Input Bias Current				2.5			3.8	µA
Large Signal Voltage Gain			15			10		V/mV
Output Voltage Swing	V_{IN} > 10 mV, I_{OUT} = 200 µA	2.2	2.5		2.2			V
	V_{IN} < -10 mV, I_{SINK} = 6.4 mA		0.3	0.45		0.3	0.45	
Input Voltage Range		±2.0			±2.0			V
Common Mode Rejection Ratio	R_S ≤ 50Ω, V_{CM} = ±2V Input Voltage Range	85			80			dB
Power Supply Rejection Ratio	R_S ≤ 50Ω, $+V_S$ =+5V, -5.25V ≤ $-V_S$ ≤-4.75V and $-V_S$ = -5V, +4.75V ≤ $+V_S$ < +5.25V	75			72			dB
Supply Current (Positive)	V_{OUT} ≤ 0.4V		13	18		15	20	mA
Supply Current (Negative)	V_{OUT} ≤ 0.4V	-20	15		-20	15		mA
Power Consumption	V_{OUT} ≤ 0.4V		140	190		150	200	mW
Propagation Delay 1	100 mV Step, V_{OD} = 5 mV		30	50		35	55	ns
	100 mV Step, V_{OD} = 1.2 mV		50			50		ns

Note:
1. Guaranteed but not tested

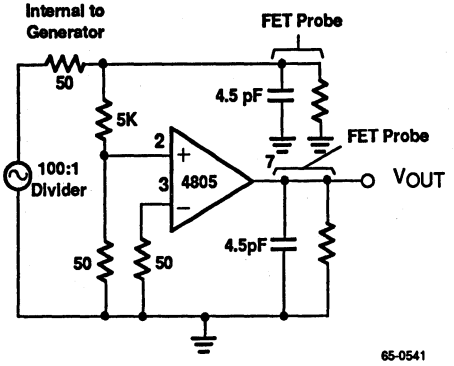
Typical Performance Characteristics



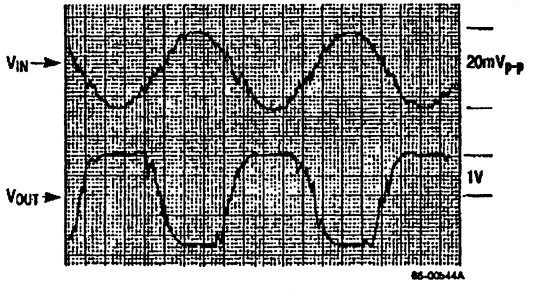
Rising Edge Response Time



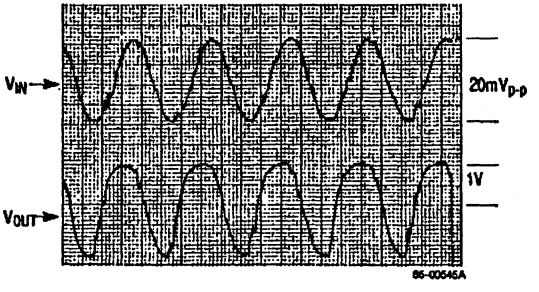
Falling Edge Response Time



Response Time Test Setup

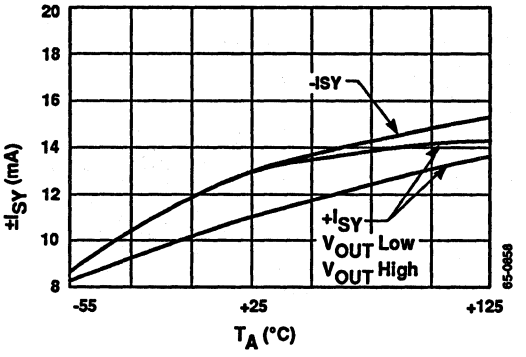


Response to 25 MHz Sine Wave

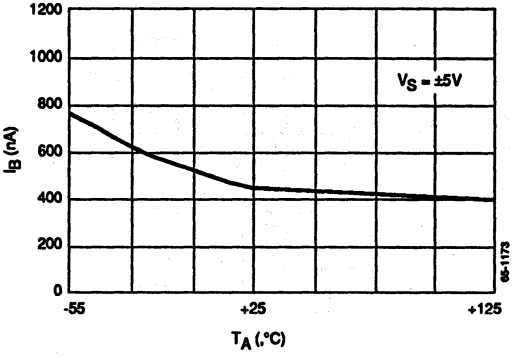


Response to 50 MHz Sine Wave

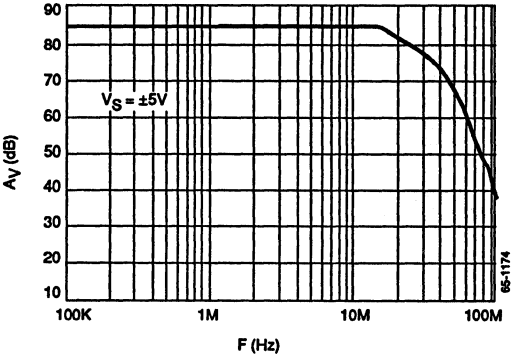
Typical Performance Characteristics (continued)



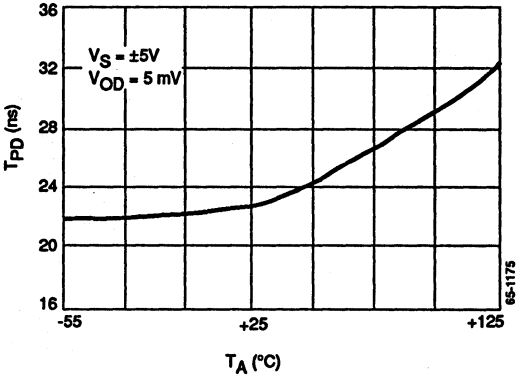
Supply Current vs. Temperature



Input Bias Current vs. Temperature



Gain vs. Frequency



Propagation Delay vs. Temperature

Applications Information

Optimal performance of the 4805 in high speed applications circuits requires that careful layout and circuit design techniques are used. The use of good power supply bypass capacitors, minimum lead lengths and a good ground plane are essential. Clamping diodes for the inputs may also be required.

Bypass Capacitors

Tantalum electrolytics connected close to the power supply leads are usually sufficient; sometimes a smaller ceramic capacitor in parallel with the tantalum may improve high frequency response even further. Typical values would be 10 µF in parallel with 0.01 µF.

Minimize Lead Lengths

Short input leads are essential to eliminate stray capacitance that might otherwise induce oscillations. Avoid the use of sockets; solder the IC directly to the PC board. When laying out a PC board, position the signal source as close to the comparator inputs as is physically possible. Avoid stray capacitance from the inputs to ground, and route the output away from the inputs. Best response times will occur when the source impedance driving the inputs is kept low (<1 kΩ). Avoid driving heavy capacitive loads with the output (example: coaxial cable, which has a parasitic capacitance of 50 pF per foot).

Ground Plane

A ground plane reduces the parasitic inductance of PC traces. Current flow through the PC trace is mirrored by a return current flow that passes through the ground plane adjacent to the PC trace. This sets up a magnetic field that cancels the magnetic field in the PC trace, thus reducing parasitic inductance.

Use the component side of the board for the ground pane. Cover that side as completely as is practical, especially under traces carrying high frequency signals. Mount high frequency components close to the board.

Clamping Diodes

If the differential input voltage will be greater than 1V, the inputs should be clamped with high speed low capacitance diodes.

Latch Enable

The effective gain at low levels of input overdrive can be increased by applying a carefully timed positive going step to the latch enable input. This technique is especially useful in successive approximation A/D converters, where the exact time of comparison is well defined. After the SAR changes the DAC output, a delayed pulse applied to pin 6 will increase the effective gain from about 5 V/mV to 20 V/mV, and therefore speeds up the response time for low level input signals. In a 12-bit ±10V A/D system, the propagation delay for 1 LSB will decrease about 30%. Figure 1 shows the waveforms for this technique, and Figure 2 shows a one-shot time delay circuit using a TTL IC that can be used to create the pulse.

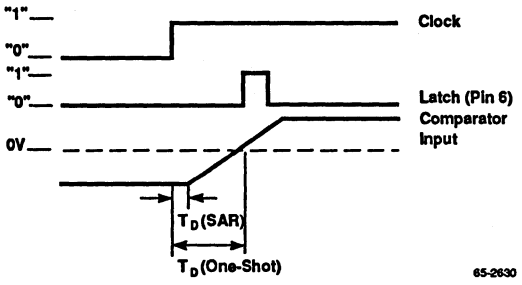


Figure 1. Gain Boost Waveforms

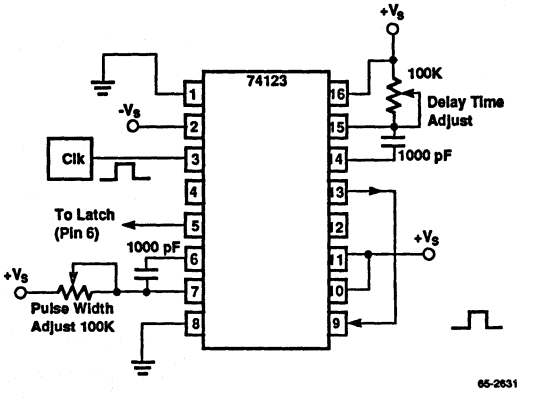
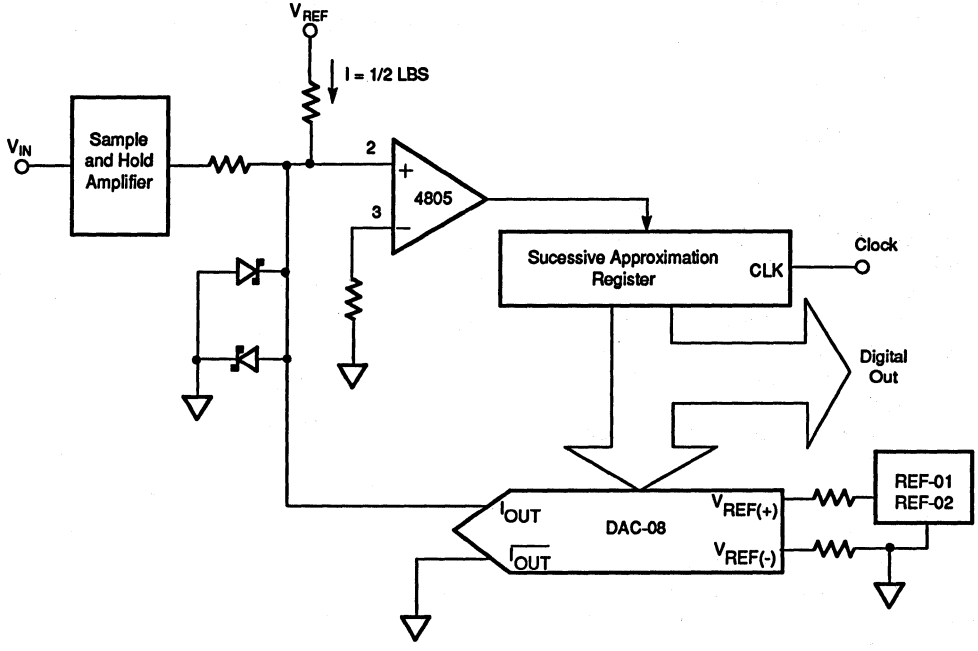


Figure 2. Delayed Pulse Circuit

Linear

Typical Applications

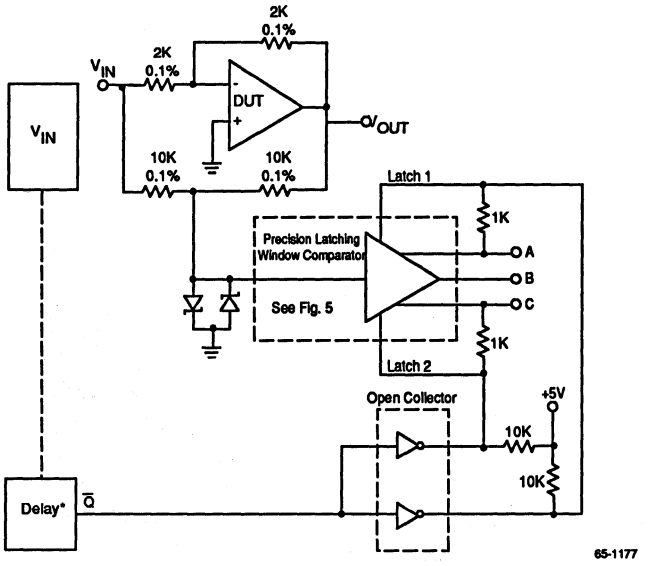
	Conversion Time 8-Bits
4805 Response	20 ns
DAC settling Time*	135 ns
SAR Delay Time	50 ns
Total-Cycle Time	205 ns
Number Cycles + Reset	x9
Total Conversion Time	**1.8 µs**



* Response will be affected by DAC's output capacitance and equivalent resistance.

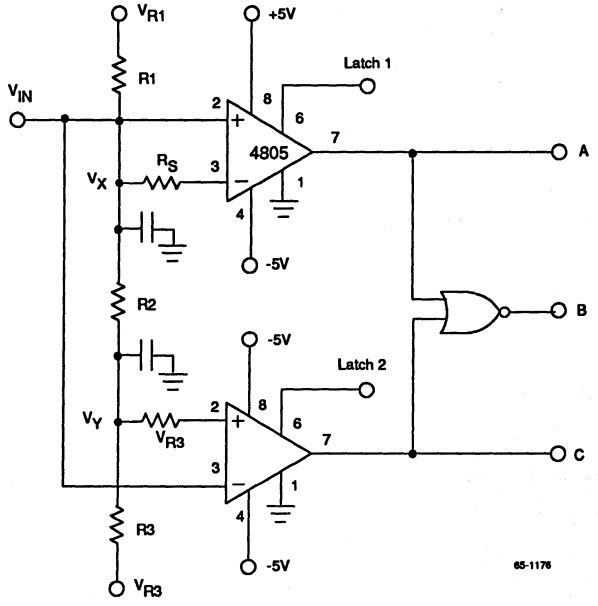
Figure 3. Successive Approximation ADC

Typical Applications (Continued)



*Delay should equal the settling time specification minus 30 ns minus appropriate guard band.

Figure 4. Op Amp Settling Time Test Circuit



The settling time test circuit uses the precision latching window comparator to automate op amp settling time testing. If the DUT is not settled by the end of the time delay, the A output is latched low.

V_{IN} ($V_X > V_Y$)*	A	B	C
$V_{IN} > V_X$	1	0	0
$V_X > V_{IN} > V_Y$	0	1	0
$V_Y > V_{IN}$	0	0	1

*Both latches low

Figure 5. Precision Latching Window Comparator

Fast Latching ECL to TTL Line Translator, Up to 50 MHz

The high speed differential input and the latched TTL output makes the 4805 ideally suited for use as an ECL to TTL translator. Existing logic supplies of -5.2V and +5.0V are compatible with the 4805 power supply requirements. With a TTL compatible latch input, the 4805 can be latched from the TTL subsystem or from the ECL subsystem, by using another 4805 on the latch signal.

In ECL systems, the termination resistors and pull-down resistors can be combined in a network as shown in Figure 6, a typical ECL to TTL translator. The configuration shown in Figure 7 has a common mode range of ±2.0V. By using a -15V supply on the 4805, the common mode range is extended to -8.0V to +2.0V as shown in Figure 8.

Not all ECL families have the same logic levels, the same logic level V_S supply voltage, or the same temperature characteristics. By using the same logic type as a reference, a single-end ECL to TTL translator can be made to track changes in logic levels. A typical circuit is shown in Figure 9.

In system design one subsystem may be in one configuration, be driven with ECL line drivers, but in another configuration the same subsystem may be driven from a TTL gate.

High gain, low input bias current and ±2.0V common mode range on the 4805 allow the easy design of an adaptive ECL-TTL to TTL translator. The ECL interface is the same as shown in Figure 6. By adding pull-up resistors and a bypassed level shifting resistor to the TTL outputs (see Figure 9), the same subsystem line receiver can interface with ECL or TTL with no hardware change in the receiver.

The 4805 is a very flexible system element that allows the system designer to interface ECL to TTL in a number of easy to use configurations. The4805 can also be used in an adaptive ECL-TTL to TTL interface.

Typical Examples

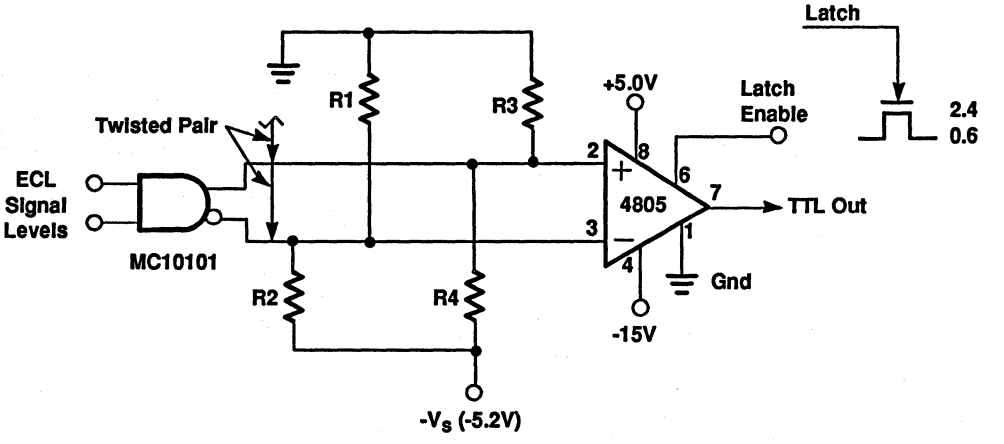


Figure 6. ECL to TTL Translator

Typical Examples (Continued)

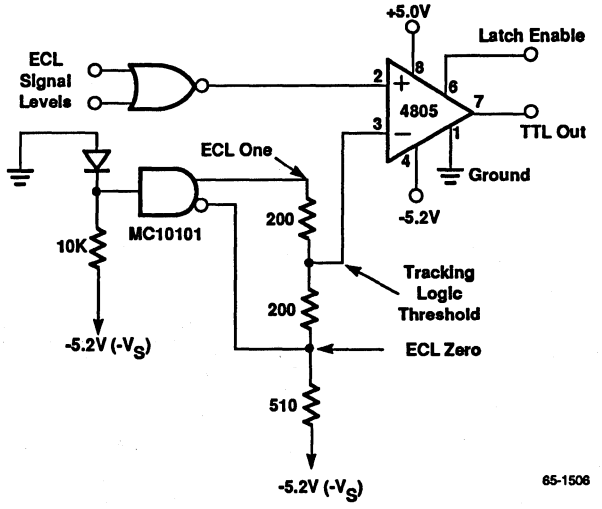
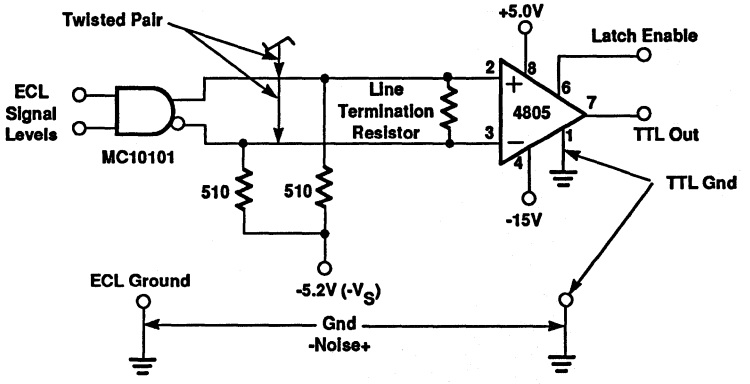


Figure 7. Single-Ended ECL to TTL Translator with Tracking ECL Reference



Notes:
1. Common mode range of 4805 is -8.0V to +2.0V.
2. The 4805 can stand -3.0V, +5.0V of ground noise from the ECL Gnd to the TTL Gnd.

Figure 8. ECL to TTL Translator with extended Common Mode Range

Linear

Typical Examples (Continued)

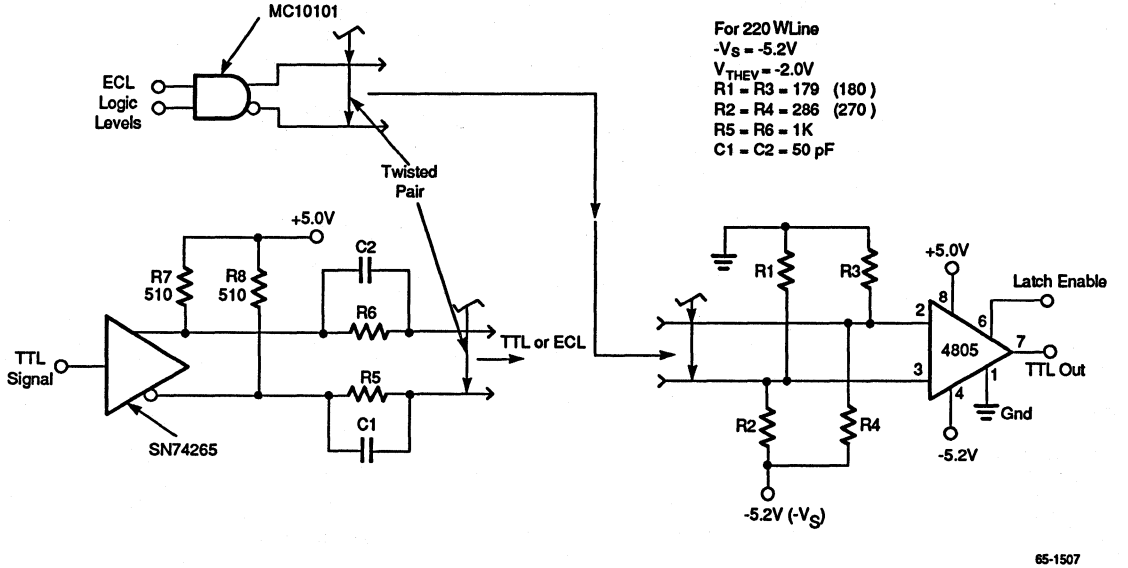
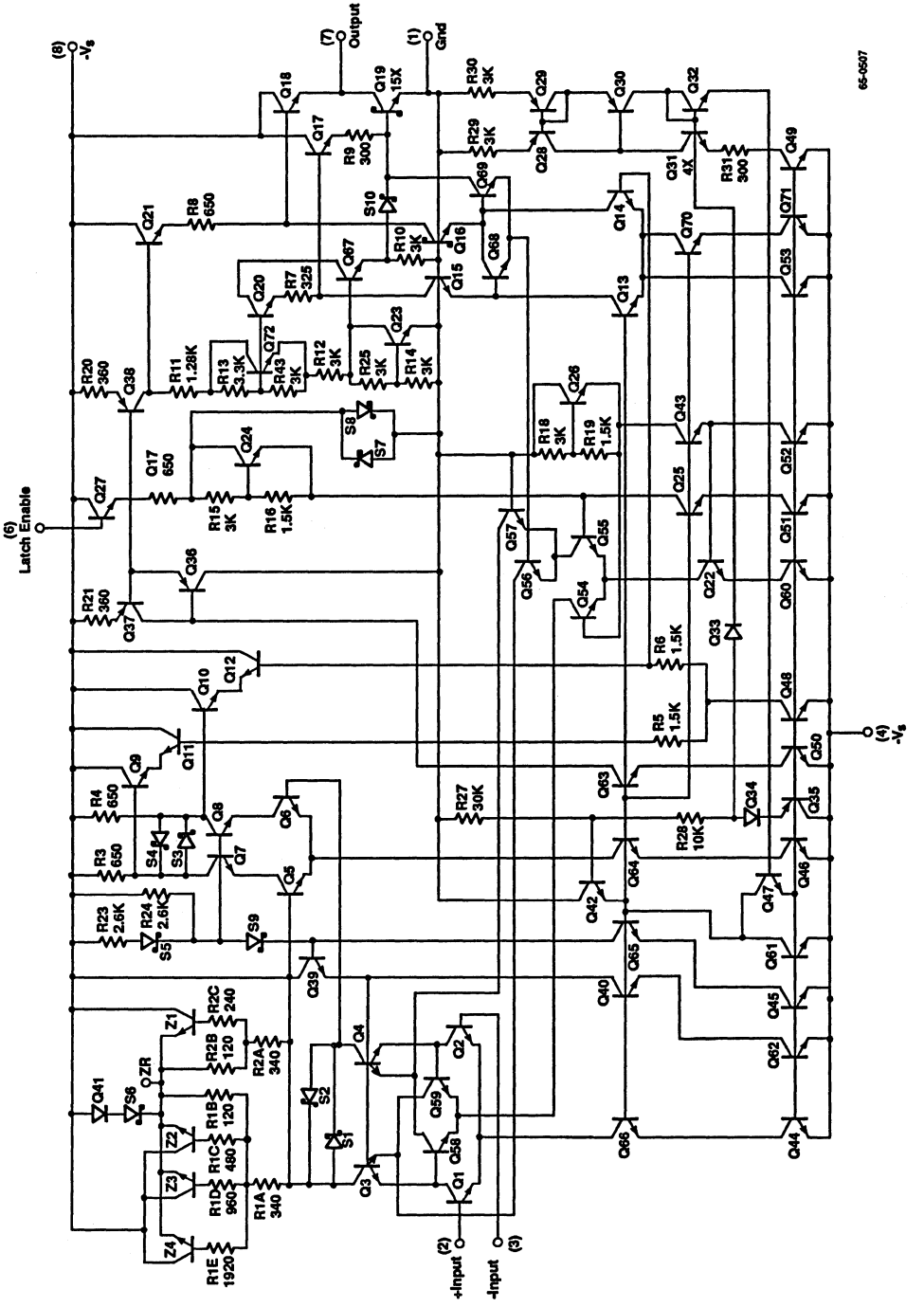


Figure 9. Adaptive ECL -TTL to TTL Translator

Schematic Diagram



LM111/LH2111
Voltage Comparators

Description

These low input current voltage comparators are designed to operate over a wide range of supply voltages, including ±15V and single +5V supplies. Their outputs are compatible with DTL, RTL, TTL and MOS devices, and can be connected in "wire-OR" configuration. The LH2111 consists of two LM111 ICs packaged in a 16-lead DIP. The LH2111 is available with MIL-STD-883B screening.

Features

- Low input offset current — 4 nA
- Low input bias current — 60 nA
- Operates from a single +5V supply
- Response Time — 200 ns

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Output to $-V_S$ 50V
Ground to $-V_S$ 30V
Differential Input Voltage 30V
Input Voltage [1] ..... ±15V
Power Dissipation[2] ..... 500 mW
Output Short Circuit Duration ..... 10 sec.
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -55°C to +125°C
Voltage at Strobe Pin ..... $+V_S$ -5V
Lead Soldering Temperature (60 sec.) ..... +300°C

Notes:
1. For supply voltages other than ±15V, the maximum input is equal to the supply voltage.
2. Observe package thermal characteristics.

Ordering Information

Part Number	Package	Operating Temperature Range
LM111T/883B	T	-55°C to +125°C
LM111D/883B	D	-55°C to +125°C
LH2111D	D	-55°C to +125°C
LH2111D/883B	D	-55°C to +125°C

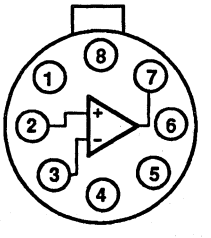
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
D = 8-lead ceramic DIP (LM111)
D = 16-lead ceramic DIP (LH2111)
T = 8-lead metal can (TO-99)

Thermal Characteristics

	8-Lead TO-99 Metal Can	8-Lead Ceramic DIP	16-Lead Ceramic DIP
Max. Junction Temp.	+175°C	+175°C	+175°C
Max. P_D T_A <50°C	658 mW	833 mW	1042 mW
Therm. Res θ_{JC}	50°C/W	45°C/W	60°C/W
Therm. Res. θ_{JA}	190°C/W	150°C/W	120°C/W
For T_A >50°C Derate at	5.26 mW/°C	8.33 mW/°C	8.38 mW/°C

Connection Information

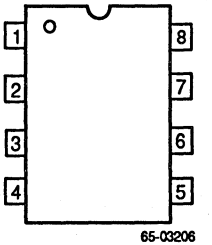
8-Lead TO-99 Metal Can
(Top View)



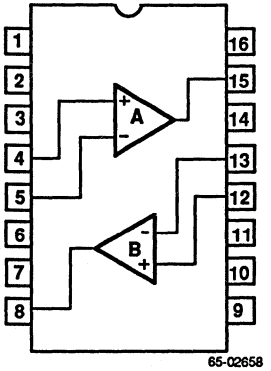
65-03205

Pin	Function
1	Ground
2	+Input
3	- Input
4	$-V_S$
5	Balance
6	Balance/Strobe
7	Output
8	$+V_S$

8-Lead Dual In-Line Package
(Top View)



65-03206



65-02658

Pin	Function
1	+Vs (A)
2	Ground (A)
3	+ Input
4	-Input (A)
5	$-V_S$
6	Balance (B)
7	Bal/Strobe (B)
8	Output (B)
9	$+V_S$
10	Ground (B)
11	+Input (B)
12	-Input (B)
13	Balance (A)
14	Bal/Strobe (A)
15	Output (A)
16	NC

Electrical Characteristics

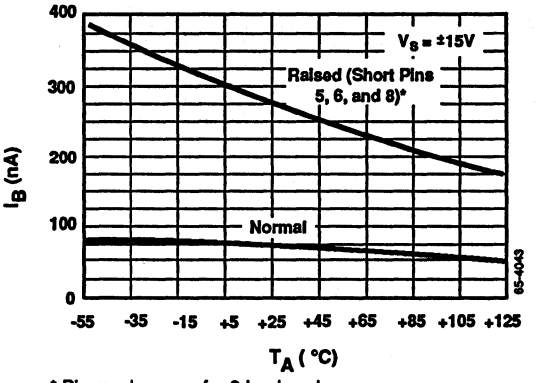
($V_S = \pm 15V$[1] and $-55°C \leq T_A \leq +125°C$ unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage [2]	$T_A = +25°C$, $R_S \leq 50\ k\Omega$		0.7	3.0	mV
Input Offset Current[2]	$T_A = +25°C$		4.0	10	nA
Input Bias Current	$T_A = +25°C$		60	100	nA
Large Signal Voltage Gain	$T_A = +25°C$	40	200		V/mV
Response Time	$T_A = +25°C$, 100 mV step, 5 mV overdrive		200		ns
Output Voltage Low (V_{OL})	$V_{IN} \leq 5$ mV, $I_L = 50$ mA, $T_A = +25°C$		3.0		mA
Output Leakage current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$, $T_A = +25°C$, $I_{STROBE} = 3$ mA		0.2	10	nA
Input Offset Voltage[2]	$R_S \leq 50\ k\Omega$		1.5	4.0	mV
Input Offset Current [2]			5.0	20	nA
Input Bias Current			100	150	nA
Input Voltage Range	Pin 7 pull up may go to +5V	-14.5		13.0	V
Output Voltage Low (V_{OL})	$+V_S = 4.5V$, $-V_S = 0V$, $V_{IN} \leq -6$ mV, $I_{OUT} = 8.0$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		100	500	nA
Positive Supply Current	$T_A = +25°C$, each amplifier		5.1	6.0	mA
Negative Supply Current	$T_A = +25°C$, each amplifier		4.1	5.0	mA

Notes:

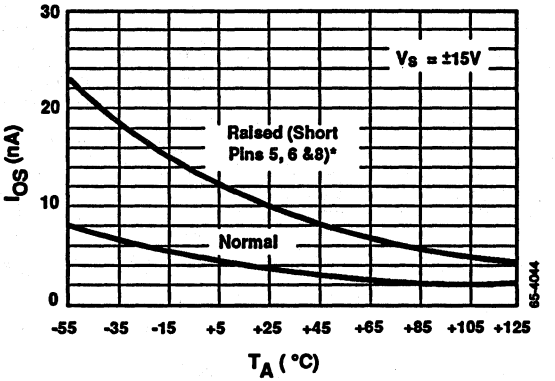
1. V_{OS}, I_{OS} and I_B specifications apply for $V_S = +5V$ to $V_S = \pm 15V$.
2. V_{OS} and I_{OS} are maximum values required to drive the output to within 1V of either supply with a 1 mA load.
3. Do not short circuit the strobe pin to ground — drive it with a 3 to 5 mA current instead.
4. If the strobe and balance pins are unused, short them together for maximum AC stability.

Typical Performance Characteristics



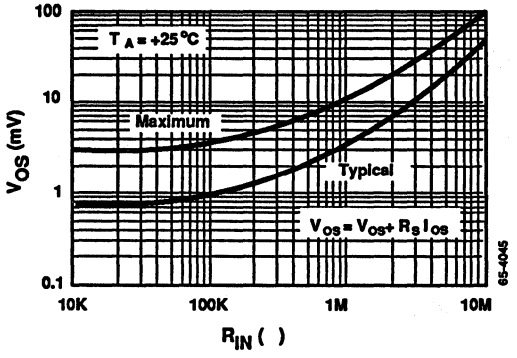
* Pin numbers are for 8-lead packages

Input Bias Current vs. Temperature

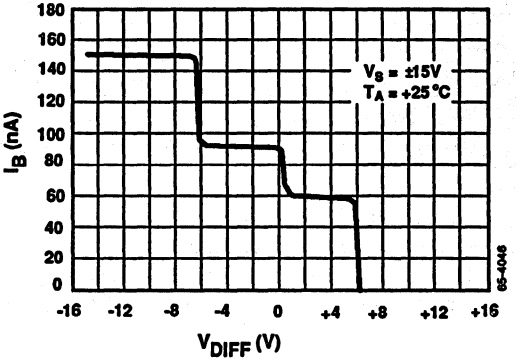


* Pin numbes are for 8-lead packages

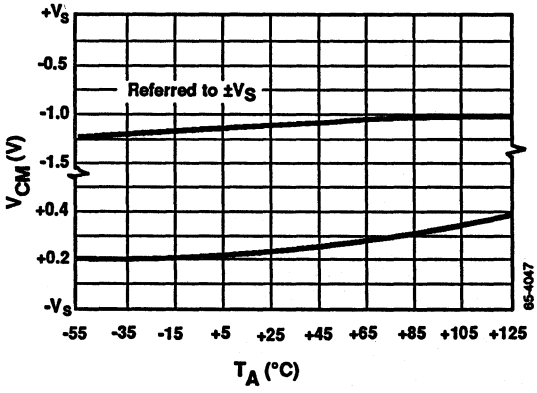
Input Offset Current vs. Temperature



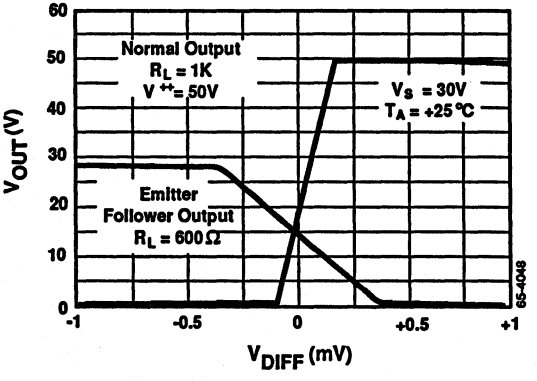
Equivalent Input Offset Voltage vs. Input Resistance



Input Bias Current vs. Differential Input Voltage

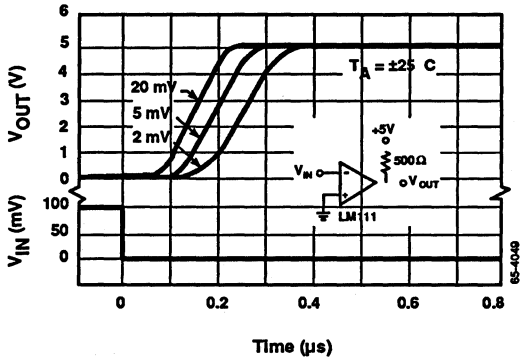


Common Mode Limits vs. Temperature

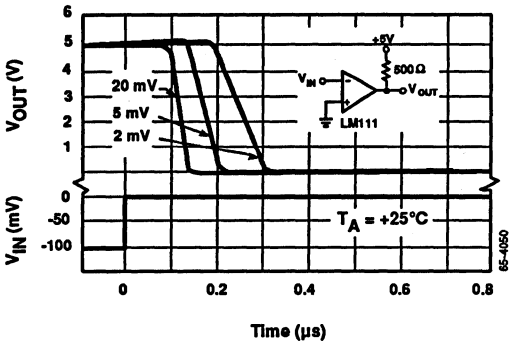


Output Voltage vs. Differential Input Voltage

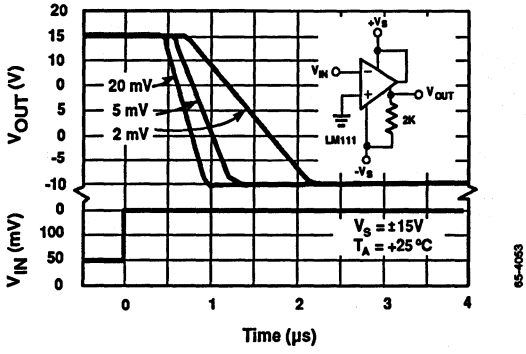
Typical Performance Characteristics (Continued)



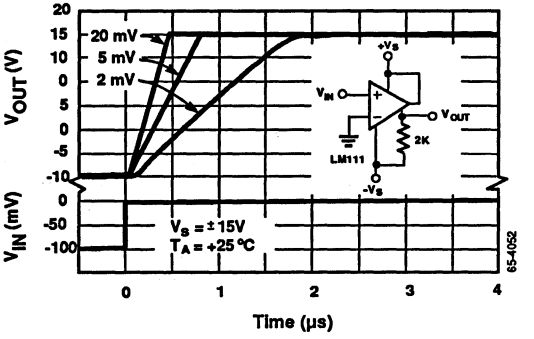
Input Overdrive vs. Response Times



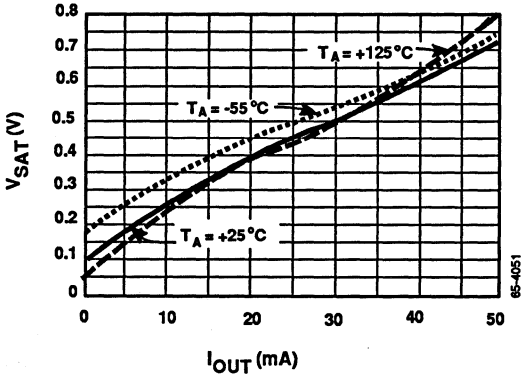
Input Overdrive vs. Response Times



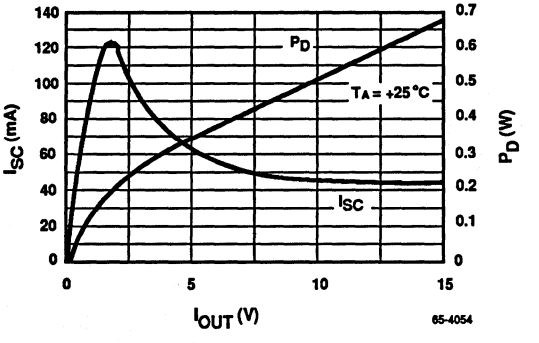
Input Overdrive vs. Response Times



Input Overdrive vs. Response Times



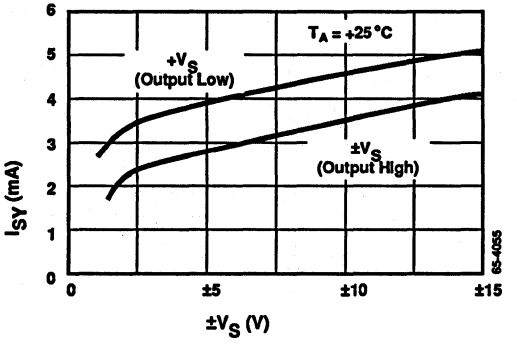
Output Saturation Voltage vs. Output Current



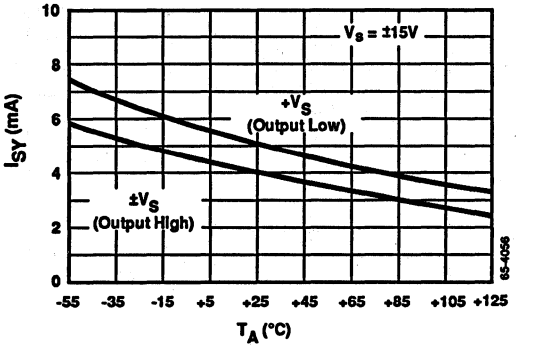
Short Circuit Current, Power Dissipation vs. Output Voltage

Linear

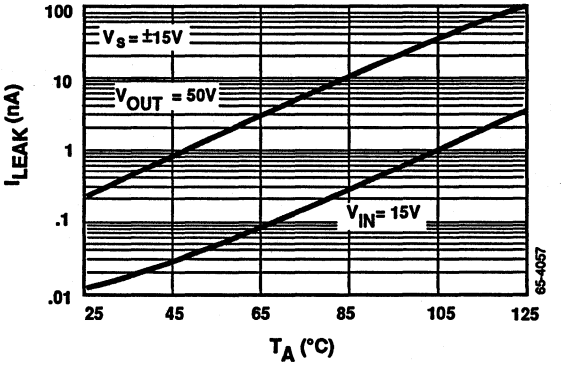
Typical Performance Characteristics (Continued)



Supply Current vs. Supply Voltage

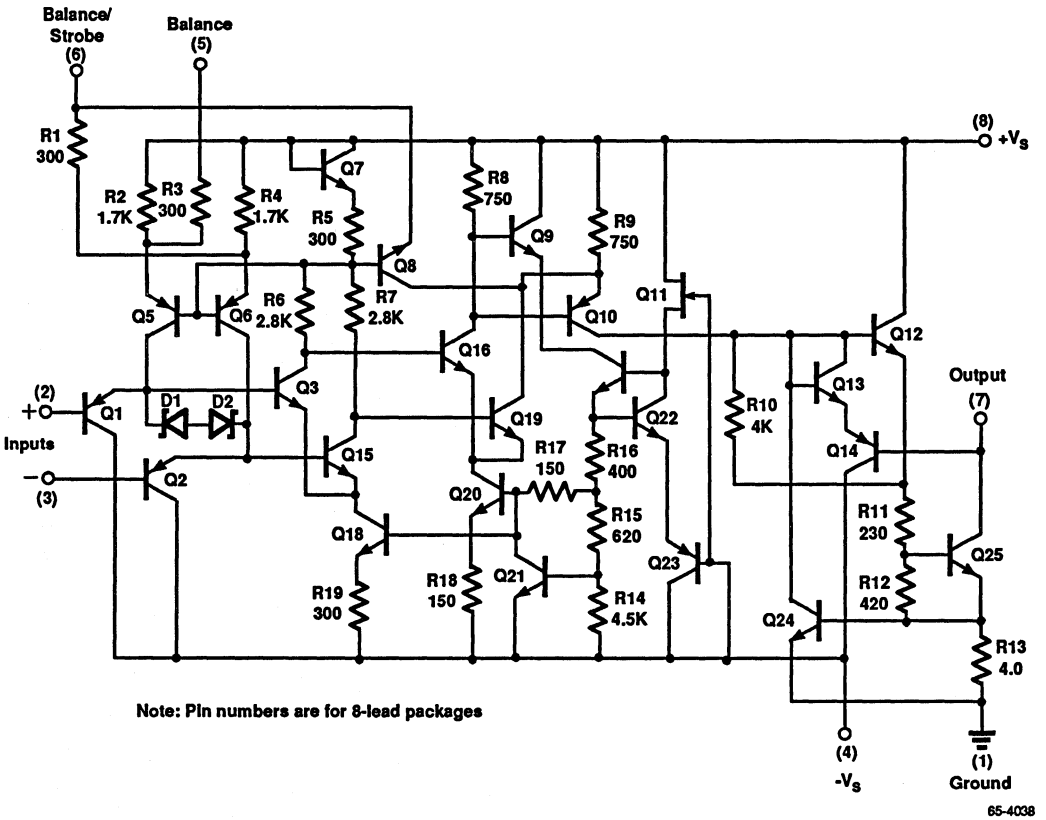


Supply Current vs. Temperature



Leakage Current vs. Temperature

Schematic Diagram



Linear

REF-01
+10V Precision Voltage Reference

Description

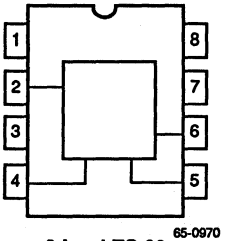
The REF-01 Precision Voltage Reference contains a bandgap reference using thin-film resistors, a step-up amplifier, short circuit protection, and a zener trim network. The REF-01's +10V output shows excellent stability for large changes of temperature, load current, and input voltage. A trim pin is provided that can change the output voltage by at least 3% with little effect on temperature coefficient.

Features

- +10V output — ±0.3%
- Adjustable — ±3%
- Excellent temperature stability — 3 ppm/°C
- Low noise — 20 μV_{p-p}
- Wide input voltage range — +12V to +40V
- No external components
- Short circuit proof
- Low power consumption — 15 mW

Connection Information

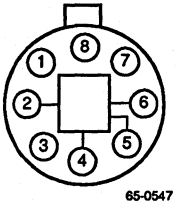
8-Lead
Dual In-Line Package
(Top View)



65-0970

Pin	Function
1	NC
2	$+V_S$
3	NC
4	Ground
5	Trim
6	Output
7	NC
8	NC

8-Lead TO-99
Metal Can
(Top View)



65-0547

Ordering Information

Part Number	Package	Operating Temperature Range
REF-01CD	D	0°C to +70°C
REF-01DD	D	0°C to +70°C
REF-01CN	N	0°C to +70°C
REF-01DN	N	0°C to +70°C
REF-01D	D	-55°C to +125°C
REF-01D/883B	D	-55°C to +125°C
REF-01T	T	-55°C to +125°C
REF-01T/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D = 8-lead ceramic DIP
N = 8-lead plastic DIP
T = 8-lead metal can (TO-99)

Absolute Maximum Ratings

Supply Voltage
- REF-01 ..... +40V
- REF-01C, D ..... +30V

Internal Power Dissipation ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- REF-01, ... -55°C to +125°C
- REF-01C,D ..... 0°C to +70°C

Lead Soldering Temperature
- (60 Sec) ..... +300°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic Metal Can	8-Lead TO-99 Metal Can
Max. Junction Temp.	+125°C	+175°C	+175°C
Max. P_D T_A <50°C	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-01 Min	REF-01 Typ	REF-01 Max	Units
Output Voltage	I_{LOAD}= 0mA	9.95	10.00	10.05	V
Output Adjustment Range	R_{TRIM} = 10 kΩ	±3.0	±3.3		%
Output Voltage Noise[1]	0.1Hz to 10Hz		20	30	µVp-p
Supply Voltage		12		40	V
Line Regulation[2]	V_S = +13V to +33V		0.006	0.010	%/V
Load Regulation[2]	I_{LOAD} = 0mA to 10mA		0.006	0.010	%/mA
Turn-on Setting Time	To ±0.1% of Final Value		5.0		µS
Supply Current	No Load		1.0	1.4	mA
Load Current		10	21		mA
Sink Current		-0.3	-0.5		mA
Short Circuit Current	V_{OUT}= 0		30		mA

Electrical Characteristics

(V_S = ±15V and -55°C≤ T_A ≤+125°C unless otherwise noted)

Parameters	Test Conditions	REF-01 Min	REF-01 Typ	REF-01 Max	Unit
Output Voltage Change With Temperature [3, 4]	Over Temp. Range		0.18	0.45	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_{TRIM} = 10kΩ		0.7		ppm/%
Line Regulation[2]	V_S = +13V to +33V		0.009	0.015	%/V
Load Regulation[2]	I_{LOAD} = 0mA to 8mA		0.007	0.012	%/mA

Notes:
1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX}-V_{MIN}}{10V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature} \times 10^6}{(100\%)\,(180°C)}$

Linear

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-01C			REF-01D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_{LOAD}=0mA	9.90	10.00	10.10	9.850	10.00	10.150	V
Output Adjustment Range	R_{TRIM} = 10 kΩ	±2.7	±3.3		±2.0	±3.3		%
Output Voltage Noise[1]	0.1Hz to 10Hz		25	35		25		µVp-p
Supply Voltage		12		30	12		30	V
Line Regulation[2]	V_S = +13V to +33V		0.009	0.015		0.012	0.04	%/V
Load Regulation[2]	I_{LOAD} = 0mA to 8mA		0.006	0.015				%/mA
	I_{LOAD} = 0mA to 4mA		0.006	0.015		0.009	0.04	
Turn-on Setting Time	To ±0.1% of Final Value		5.0			5.0		µS
Supply Current	No Load		1.0	1.6		1.0	2.0	mA
Load Current		8.0	21		8.0	21		mA
Sink Current		-0.2	-0.5		-0.2	-0.5		mA
Short Circuit Current	V_{OUT}=0		30			30		mA

Notes: 1. Guaranteed by design.

2. Line and load regulation specifications include the effects of self heating.

Electrical Characteristics

(V_S = +15V, 0°C ≤ T_A ≤ +70°C, and I_{OUT} = 0 unless otherwise noted)

Parameters	Test Conditions	REF-01C			REF-01D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature [3, 4]	Over Temp. Range		0.14	0.45		0.49	1.7	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		20	65		70	250	ppm/°C
Change in V_{OUT} Temperature Coeffiecient With Output Adjustment	R_{TRIM} = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +13V to +30V		0.011	0.018		0.020	0.025	%/V
Load Regulation[2]	I_{LOAD} = 0mA to 8mA		0.008	0.018		0.020	0.025	%/mA

Notes: 1. Guaranteed by design.

2. Line and load regulation specifications include the effects of self heating.

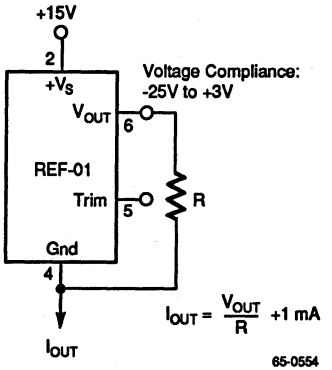
3. Output voltage change with temperature = $\frac{V_{MAX}-V_{MIN} \times 100\%}{10V}$

4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.

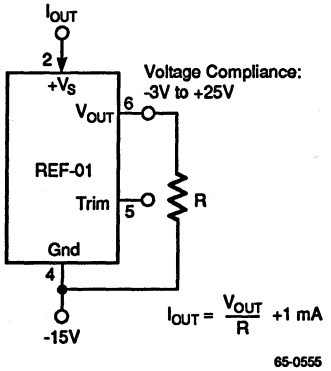
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature} \times 10^6}{(100\%)\ (70°C)}$

Typical Applications

Current Source

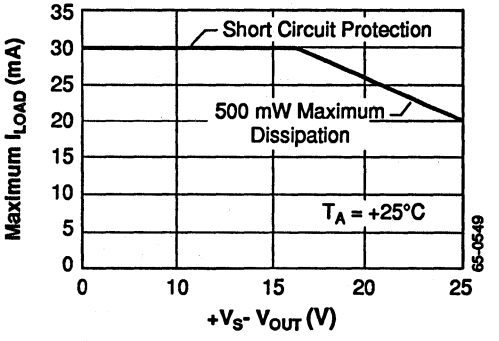


Current Sink

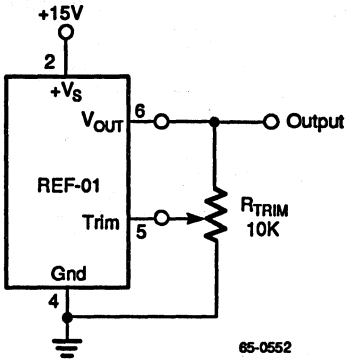


Typical Performance Characteristics

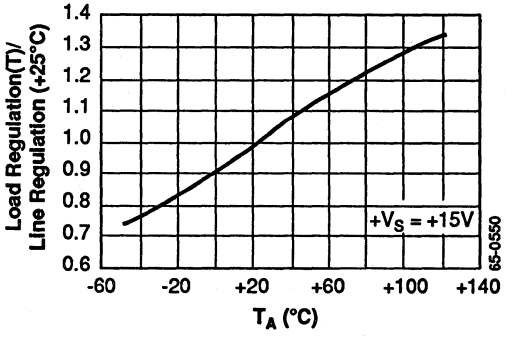
Maximum Load Current vs. Differential Input Voltage



Output Adjust

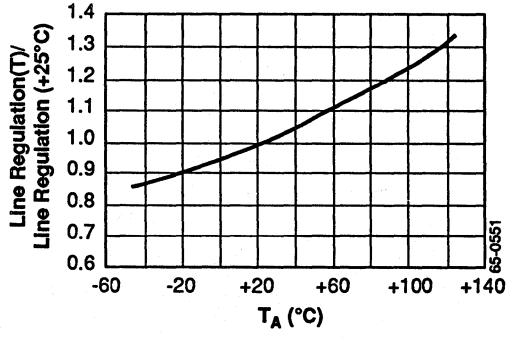


Normalized Load Regulation (DI_{LOAD} = 10 mA) vs. Temperature

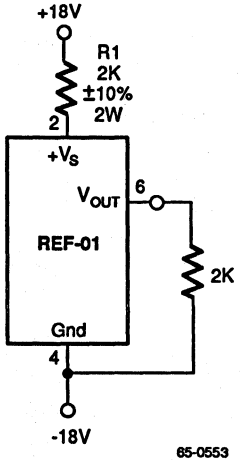


The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V or to 10.240V for binary operation. Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7 ppm/°C for 100mV of output adjustment.

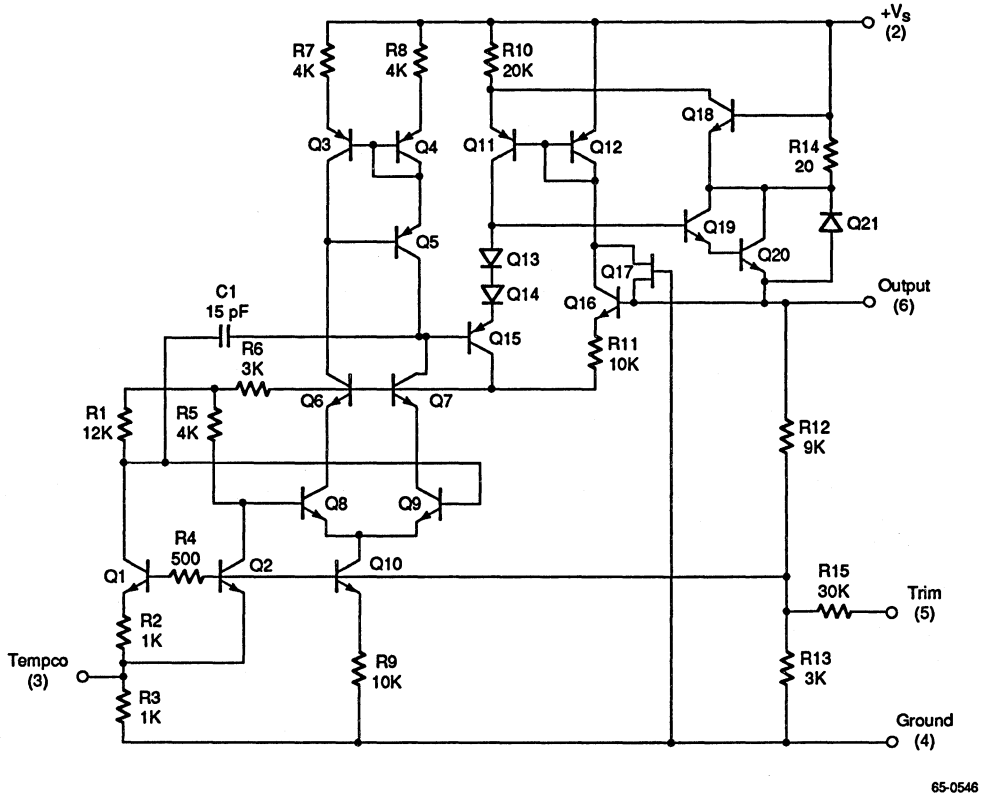
Normalized Line Regulation vs. Temperature



Burn-In Circuit



Schematic Diagram



Linear

REF-01

REF-02
+5V Precision Voltage Reference

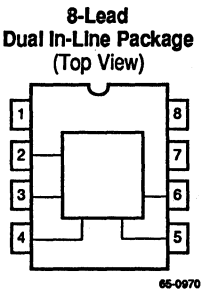
Description

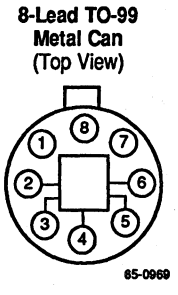
The REF-02 Precision Voltage Reference contains a bandgap reference using thin-film resistors, a step-up amplifier, short circuit protection, and a zener trim network. The REF-02's +5V output shows excellent stability for large changes of temperature, load current, and input voltage. A trim pin is provided that can change the output voltage by at least 3% with little effect on temperature coefficient. A tempco pin also provides a voltage that varies linearly with temperature, typically from +470 mV to +830 mV over the military temperature range.

Features

- +5V output — ±0.3%
- Adjustable — ±3%
- Excellent temperature stability — 3 ppm/°C
- Low noise — 10 μV_{p-p}
- Wide input voltage range — +7V to +40V
- No external components
- Short circuit proof
- Low power consumption — 10 mW

Connection Information





Pin	Function
1	NC
2	$+V_S$
3	Tempco
4	Ground
5	Trim
6	Output
7	NC
8	NC

Ordering Information

Part Number	Package	Operating Temperature Range
REF-02CD	D	0°C to +70°C
REF-02DD	D	0°C to +70°C
REF-02CN	N	0°C to +70°C
REF-02DN	N	0°C to +70°C
REF-02D	D	-55°C to +125°C
REF-02D/883B	D	-55°C to +125°C
REF-02T	T	-55°C to +125°C
REF-02T/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D = 8-lead ceramic DIP
N = 8-lead plastic DIP
T = 8-lead metal can (TO-99)

Absolute Maximum Ratings

Supply Voltage
- REF-02 ..... +40V
- REF-02C,D ..... +30V

Internal Power Dissipation ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- REF-02 ..... -55°C to +125°C
- REF-02C,D ..... 0°C to +70°C

Lead Soldering Temperature
- (60 Sec) ..... +300°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	+125°C	+175°C	+175°C
Max. P_D T_A <50°C	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Electrical Characteristics

(V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-02/H			Units
		Min	Typ	Max	
Output Voltage	I_{LOAD} =0mA	4.975	5.000	5.025	V
Output Adjustment Range	R_{TRIM} = 10kΩ	±3.0	±6.0		%
Output Voltage Noise[1]	0.1Hz to 10Hz		10	15	μV_{p-p}
Supply Voltage		7		40	V
Line Regulation[2]	V_S = +8V to +33V		0.006	0.010	%/V
Load Regulation[2]	I_{LOAD} = 0mA to 10mA		0.006	0.010	%/mA
Turn-on Setting Time	To ±0.1% of Final Value		5.0		µS
Supply Current	No Load		1.0	1.4	mA
Load Current		10	21		mA
Sink Current		-0.3	-0.5		mA
Short Circuit Current	V_{OUT} = 0		30		mA
Tempco Voltage Output[6]			630		mV

Electrical Characteristic

(V_S = +15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	REF-02			Units
		Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.18	0.45	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_{TRIM} = 10kΩ		0.7		ppm/%
Line Regulation[2]	V_S = +8V to +33V		0.009	0.015	%/V
Load Regulation[2]	I_{LOAD} = 0mA to 8mA		0.007	0.012	%/mA
Output Voltage Temperature Coefficient[6]			2.1		mV/°C

Notes: 1. Guaranteed by design.

2. Line and load regulation specifications include the effects of self heating.

3. Output voltage change with temperature = (V_{MAX} - V_{MIN}) X 100%/5V

4. Output voltage change with temperature specification applies untrimmed, or trimmed to +5V.

5. Output voltage temperature coefficient = (Output voltage change with temperature X 10^6)/[(100%) (180°C)]

6. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

Electrical Characteristics

(V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-02C			REF-02D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_{LOAD} =0mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	R_{TRIM} = 10kΩ	±2.7	±6.0		±2.0	±6.0		%
Output Voltage Noise[1]	0.1Hz to 10Hz		12	18		12		µVp-p
Supply Voltage		7.0		30	7.0		30	V
Line Regulation[2]	V_S = +8V to +33V		0.009	0.015		0.012	0.04	%/V
Load Regulation[2]	I_{LOAD}= 0mA to 8mA I_{LOAD}= 0mA to 4mA		0.006	0.015		0.009	0.04	%/mA
Turn-on Setting Time	To ±0.1% of Final Value		5.0			5.0		µS
Supply Current	No Load		1.0	1.6		1.0	2.0	mA
Load Current		8.0	21		8.0	21		mA
Sink Current		-0.2	-0.5		-0.2	-0.5		mA
Short Circuit Current	V_{OUT} = 0		30			30		mA
Tempco Voltage Output[3]			630			630		mV

Notes:

1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

Electrical Characteristics

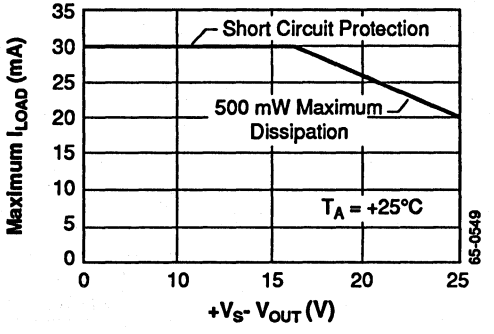
(V_S = +15V, 0° and T_A = 0°C ≤ T_A ≤ +70°C and I_{OUT} = 0 unless otherwise noted)

Parameters	Test Conditions	REF-02C			REF-02D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3, 4]	Over Temp. Range		0.14	0.45		0.49	1.7	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		20	65		70	250	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_{TRIM} = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +8V to +33V		0.011	0.018		0.020	0.025	%/V
Load Regulation[2]	I_{LOAD} = 0mA to 5mA		0.008	0.018		0.020	0.025	%/mA
Tempco Voltage Output Temperature Coefficient[6]			2.1			2.1		mV/°C

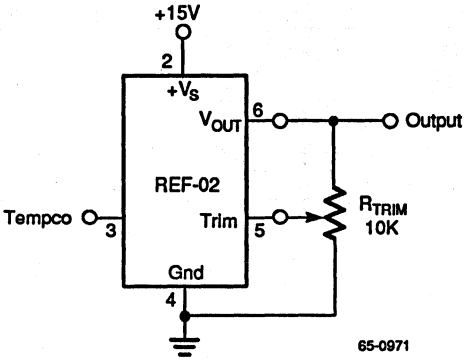
Notes:
1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $(V_{MAX} - V_{MIN}) \times 100\%/5V$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +5V.
5. Output voltage temperature coefficient = (Output voltage change with temperature X 10^6)/[(100%)(70°C)]
6. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

Typical Performance Characteristics

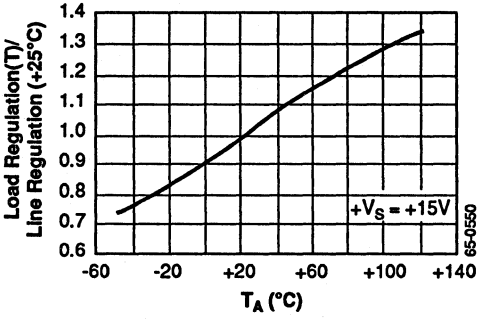
Maximum Load Current vs. Differential Voltage



Output Adjustment

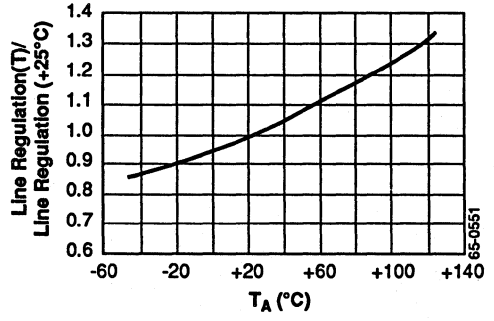


Normalized Load Regulation (ΔI_{LOAD} = 10 mA) vs. Temperature

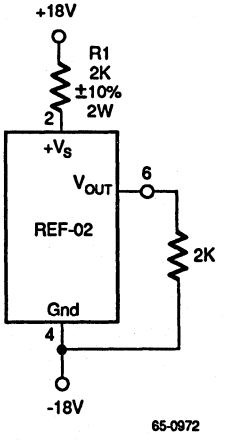


The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary operation. Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

Normalized Line Regulation vs. Temperature



Burn-In Circuit



Typical Applications

Figure 3 shows how the REF-02 can be connected with an OP-07 to create an electronic thermometer. The circuit uses the +5V reference output and the op amp to level shift and amplify the 2.1mV/°C Tempco output into a voltage signal dependent on the ambient temperature. Different scaling can be obtained by selecting appropriate resistors from the table in Figure 3, giving output slopes calibrated in degrees Celsius or degrees Fahrenheit.

To calibrate, first measure the voltage on the Tempco pin (V_{TEMPCO}) and the ambient room temperature (T_A in °C). Put those values into the following equation:

$$X = \frac{V_{TEMPCO}\ (\text{in millivolts})}{(S)\ (T_A + 273)}$$

Where S = Slope factor for your circuit selected from the table in Figure 3 (in millivolts per °C or °F).

Then turn the circuit power off, short VOUT 9 pin 6) of the REF-02 to ground, and while applying exactly 100.00mV to the op amp output, adjust R_{B2} so that V_B = (X) (100mV). Now remove the short and the 100mV source, reapply circuit power and adjust R_{TRIM} so that the op amp output voltage equals $(T_A)(S)$. The system is now exactly calibrated.

For remote sensor applications a 1.5Ω resistor (R_S) must be connected in series with the Tempco pin to isolate it from cable capacitances. Low temperature coefficient metal film resistors must be used for R_A, R_B and R_C.

Better grades of REF-02 will provide greater accuracy over a wider range of temperatures. To decrease op amp input errors, use an OP-27 instead of an OP-07. A system using a REF-02 and an OP-07 will provide a typical accuracy of ±0.5% over the military temperature range.

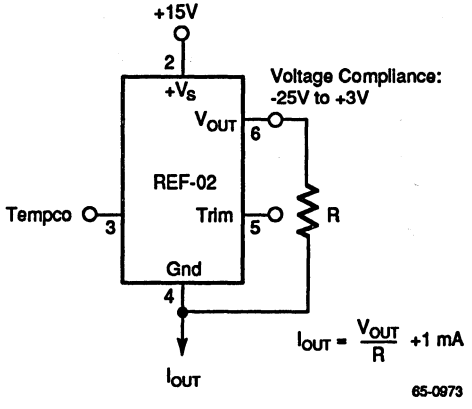


Figure 1. Current Source

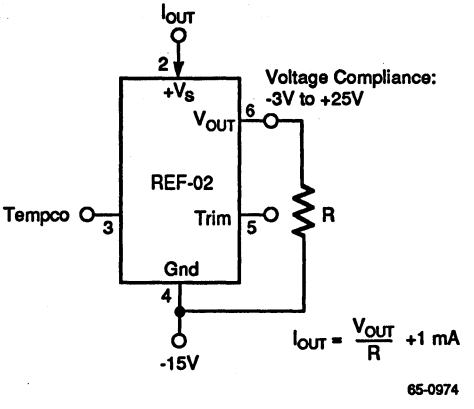
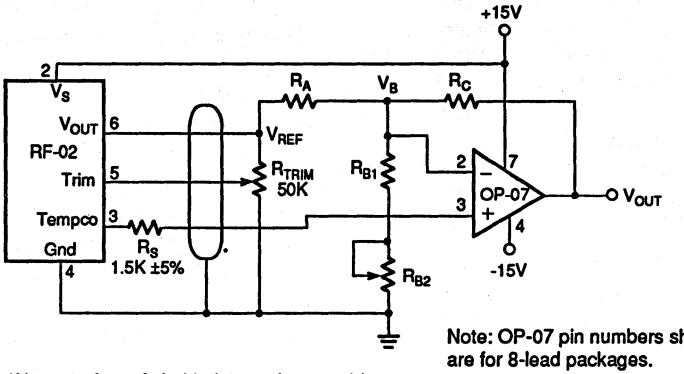


Figure 2. Current Sink



Note: OP-07 pin numbers shown are for 8-lead packages.

*Up to 10 feet of shelded 4-conductor cable.

$$T_C V_{OUT} = (2.1\ mV/°C)\left(1 + \frac{R_C}{R_A \| R_B}\right) \quad \text{Where } R_B = R_{B1} + R_{B2}$$

$$V_{OUT} = \left(H \frac{R_C}{R_A \| R_B}\right) V_{TEMPCO} - \left(\frac{R_C}{R_A}\right)(V_{OUT})$$

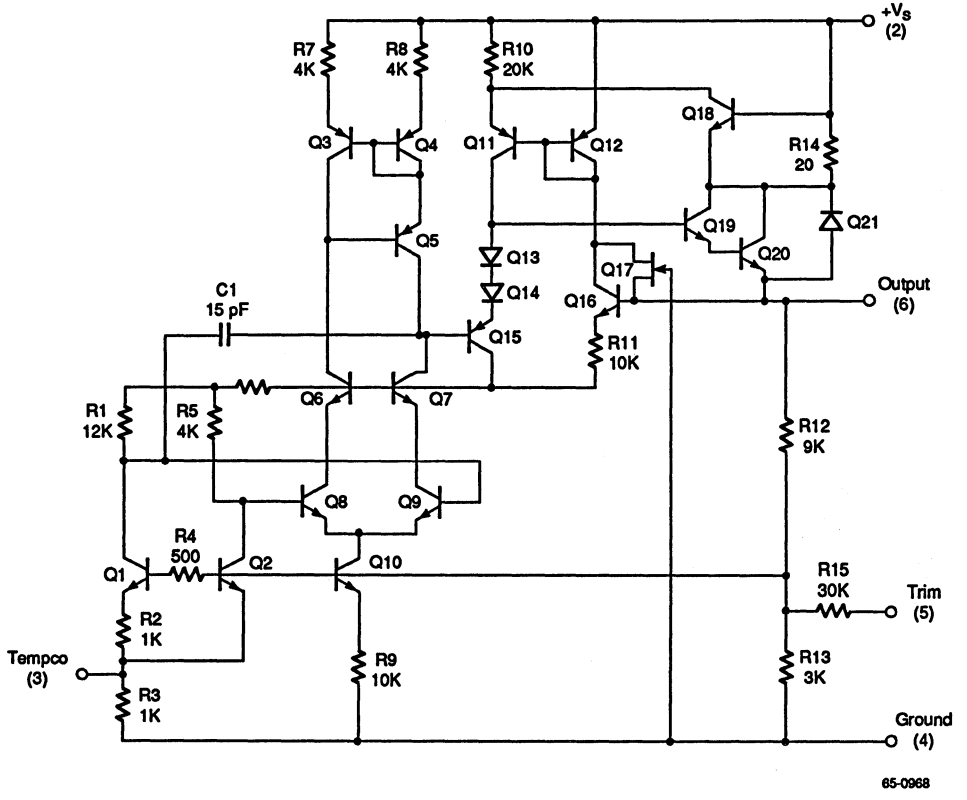
65-0556

Resistor Values

TCV_{OUT} Slope(s)	10mV/°C	100mV/°C	10mV/°F
Temperature Range	-55°C to +125°C	-55°C to +125°C	-65°F to +257°F
Output Voltage Range	-0.55V to +1.25V	-5.5V to 12.5V	-.67V to +2.57V
Zero Scale	0V at 0°C	0V at 0°C	0V at 0°F
R_A (±1% Resistor)	9.09KΩ	15KΩ	8.25KΩ
R_{B1} (±1% Resistor)	1.5KΩ	1.82KΩ	1.0KΩ
R_{B2} (Potentiometer)	200Ω	500Ω	200Ω
R_C (±1% Resistor)	5.11KΩ	84.5KΩ	7.5KΩ

Figure 3. Precision Electronic Thermometer

Schematic Diagram



Linear

RC4190
Micropower Switching Regulators

Description

The RC4190 monolithic IC is a low power switch mode regulator intended for miniature power supply applications. This DC-to-DC converter IC provides all of the active components needed to create supplies for micropower circuits (load power up to 400 mW, or up to 10W with an external power transistor). Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

Application areas include on-card circuits where a non-standard voltage supply is needed, or in battery operated instruments where a 4190 can be used to extend battery lifetime.

These regulators can achieve up to 85% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 μA.

The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the 4190 adaptable to a wide range of miniature power supply applications.

The 4190 is most suited for single ended step-up ($V_{OUT} > V_{IN}$) circuits because the NPN internal switch transistor is referenced to ground. It is complemented by another Raytheon micropower switching regulator, the 4391, which is dedicated to step-down ($V_{OUT} < V_{IN}$) and inverting $V_{OUT} = -V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the 4391 data sheet for step-down and inverting applications.

With some optional external components the application circuit can be designed to signal a display when the battery has decayed below a predetermined level, or designed to signal a display at one level and then shut itself off after the battery decays to a second level. See the applications section for these and other unique circuits.

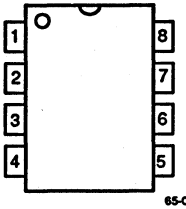
The 4190 micropower switching regulator series consists of three devices, each with slightly different specifications. The RM4190 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The RC4190 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V (RC4190) and 30V (RC4190A). Other specifications are identical. Each type is available in plastic and ceramic DIPs, or SO-8 packages.

Features

- High efficiency — 85% typical
- Low quiescent current — 215 μA
- Adjustable output — 1.3V to 30V
- High switch current — 200 mA
- Bandgap reference — 1.31V
- Accurate oscillator frequency — ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8-lead packages including small outline (SO-8)

Connection Information

8-Lead DIP (Top View)



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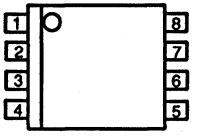
Small Outline SO-8 (Top View)



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Pin	Function
1	Low Battery (Set) Resistor (LBR)
2	Timing Capacitor (C_X)
3	Ground
4	External Inductor (L_X)
5	+Supply Voltage ($+V_S$)
6	Reference Set Current (I_C)
7	Feedback Voltage (V_{FB})
8	Low Battery Detector Output (LBD)

Ordering Information

Part Number	Package	Operating Temperature Range
RC4190M	M	0°C to +70°C
RC4190AM	M	0°C to +70°C
RC4190N	N	0°C to +70°C
RM4190D	D	-55°C to +125°C
RM4190D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
M = 8-lead plastic SOIC

Absolute Maximum Ratings(1)

Supply Voltage (Without External Transistor)
- RM4190, RC4190A ..... +30V
- RC4190 ..... +24V

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- RM4190 ..... -55°C to +125°C
- RC4190, RC4190A ..... 0°C to +70°C

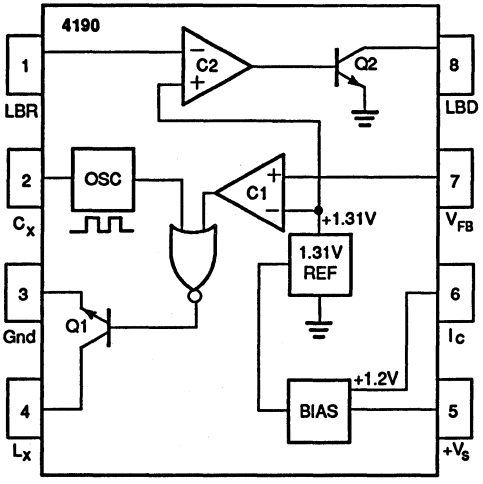
Switch Current ..... 375 mA Peak

Note:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	Small Outline SO-8
Max. Junction Temp.	+125°C	+175°C	+125°C
Max. P_D T_A<50°C	468 mW	833 mW	300 mW
Therm. Res θ_{JC}	—	45°C/W	—
Therm. Res. θ_{JA}	160°C/W	150°C/W	240°C/W
For T_A>50°C Derate at	6.25 mW/°C	8.33 mW/°C	4.17 mW/°C

Functional Block Diagram



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Electrical Characteristics

($+V_S$ = +6.0V, I_C = 5.0 µA over the full operating temperature range unless otherwise noted.)

Parameters	Symbol	Conditions	RM4190/RC4190A			RC4190/RC4190A			Units
			Min	Typ	Max	Min	Typ	Max	
Supply Voltage	$+V_s$		2.6		30	2.6		24/30	V
Reference Voltage (Internal)	V_{REF}		1.25	1.31	1.37	1.20	1.31	1.42	V
Supply Current	I_{SY}	Measure at Pin 5 I4 = 0		235	350		235	350	µA
Line Regulation		0.5 $V_{OUT} < V_S < V_{OUT}$		0.2	0.5		0.5	1.0	% V_O
Load Regulation	L_I	V_S = 0.5 V_{OUT} P_L = 150 mW		0.5	1.0		0.5	1.0	% V_O
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	µA
Switch Leakage Current	I_{CO}	V_4 = 24V (RC4190) 30V (RM4190, RC4190A)			30			30	µA
Supply Current (Disabled)	I_{SO}	$V_C \leq$ 200 mV			30			30	µA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1200		500	1200		µA
Oscillator Frequency Temperature Drift				±200			±200		ppm/°C

Linear

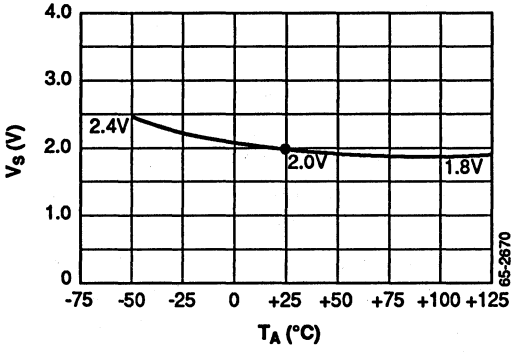
Electrical Characteristics

($+V_S$ = +6.0V, I_C = 5.0 µA, and T_A = +25°C unless otherwise noted.)

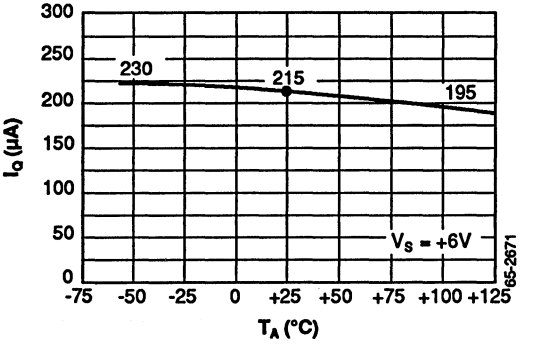
Parameters	Symbol	Conditions	RM4190//RV4190/ RC4190A			RC4190/RV4190/ RC4190A			Units
			Min	Typ	Max	Min	Typ	Max	
Supply Voltage	$+V_S$		2.2		30	2.2		24/30	V
Reference Voltage (Internal)	V_{REF}		1.29	1.31	1.33	1.24	1.31	1.38	V
Switch Current	I_{SW}	V_4 = 400 mV	100	200		100	200		mA
Supply Current	I_{SY}	Measure at Pin 5 I_4 = 0		215	300		215	300	µA
Efficiency	ef			85			85		%
Line Regulation		0.5 $V_{OUT} < V_S < V_{OUT}$		0.04	0.2		0.04	0.5	% V_O
Load Regulation	L_I	V_S = +0.5 V_{OUT} P_L = 150 mW		0.2	0.5		0.2	0.5	% V_O
Operating Frequency Range	F_O		0.1	25	75	0.1	25	75	kHz
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	µA
Switch Leakage Current	I_{CO}	V_4 = 24V (RC4190) 30V (RM4190, RC4190A)		0.01	5.0		0.01	5.0	µA
Supply Current (Disabled)	I_{SO}	$V_C \leq$ 200 mV		0.1	5.0		0.1	5.0	µA
Low Battery Bias Current	I_1	V_1 = 1.2V		0.7			0.7		µA
Capacitor Charging Current	I_{CX}			8.6			8.6		µA
Oscillator Frequency Tolerance				±10			±10		%
Capacitor Threshold Voltage +	$+V_{THX}$			1.4			1.4		V
Capacitor Threshold Voltage -	$-V_{THX}$			0.5			0.5		V
Feedback Input Current	I_{FB}	V_7 = 1.3V		0.1			0.1		µA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1500		500	1500		µA

Typical Performance Characteristics

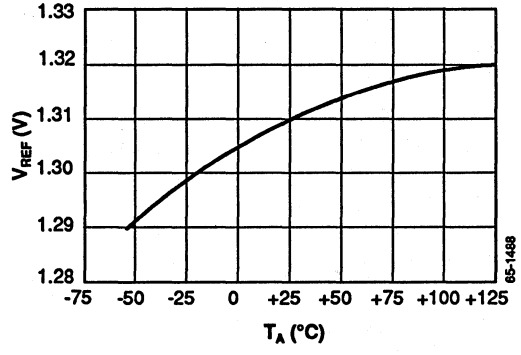
Minimum Supply Voltage vs. Temperature



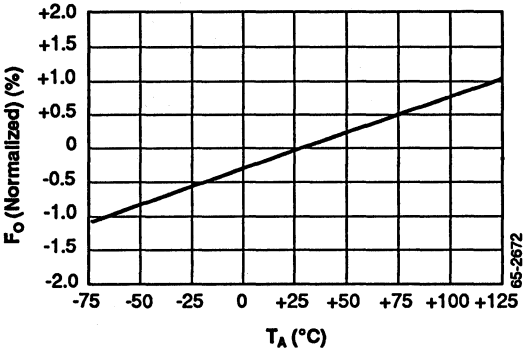
Quiescent Current vs. Temperature



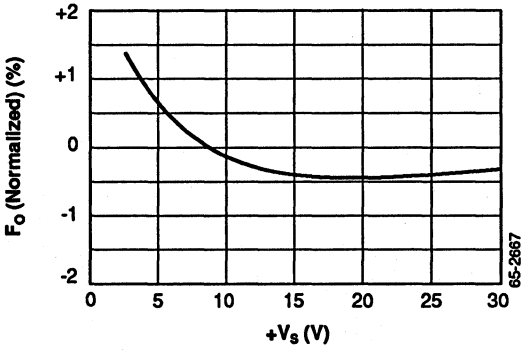
Reference Voltage vs. Temperature



Oscillator Frequency vs. Temperature



Minimum Supply Voltage vs. Temperature



Linear

Principles of Operation

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up ($V_{OUT} > V_{BAT}$) DC-to-EC Converter (Figure 1).

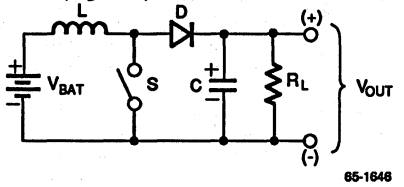


Figure 1. Simple Set-Up

When switch S is closed, the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened, the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{MAX} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant dc voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened, the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete 4190 regulator, a feedback control system adjusts the on time of the switch, controlling the level of inductor current, so that the average inductor discharge current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in figure 2. The ideal switch in the DC-to-DC Converter diagram is replaced by an open collector NPN transistor Q1. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the 4190 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} - V_D$.

At this point, the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again, the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple DC-to-DC Converter does; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter, this feedback system will vary the duration of the on time in response to changes in load current or battery voltage (see Figure 3). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and time.

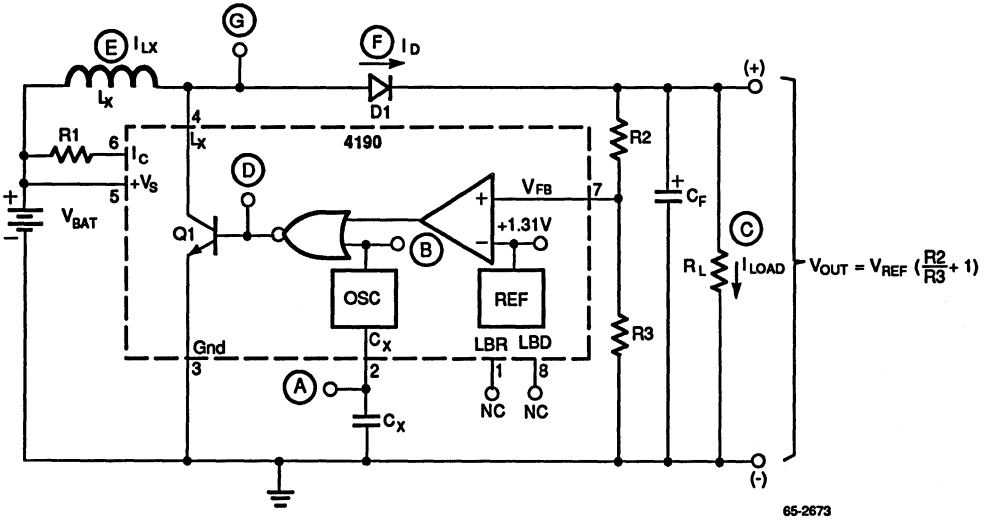


Figure 2. Complete Step-Up Regulator

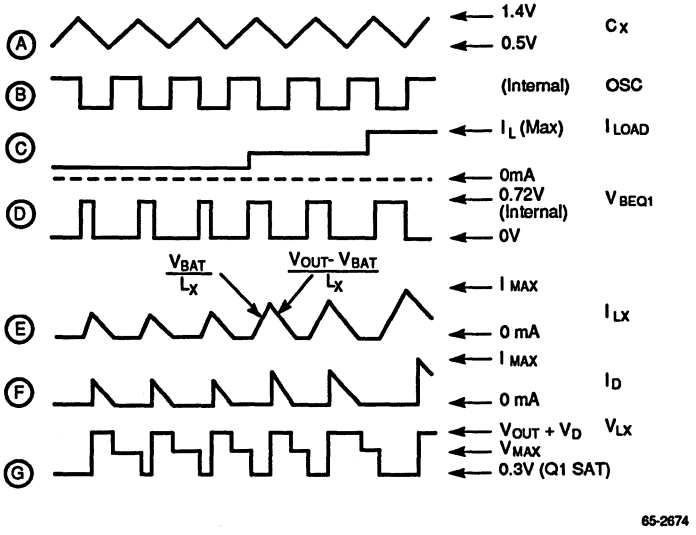


Figure 3. Step-Up Regulator Waveforms

The inductor value and oscillator frequency must be carefully tailored to the battery voltage, output current, and ripple requirements of the application (refer to the Design Equations Section). If the inductor value is too high or the oscillator frequency is too high, then the inductor current will never reach a value high enough to meet the load current drain and the output voltage will collapse. If the inductor value is too low or the oscillator frequency too low, then the inductor current will build up too high, causing excessive output voltage ripple, or over stressing of the switch transistor, or possibly saturating the inductor.

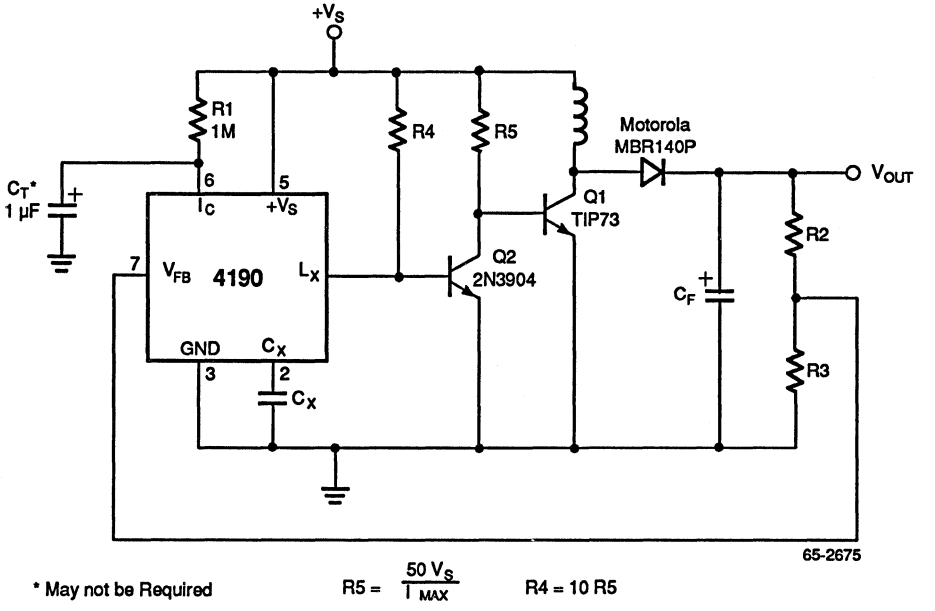


Figure 4. High Power Step-Up Regulator
(With the addition of a power transistor (TIP73) and a few components, the 4190 can accommodate load power up to 10W)

Simple Step-Down Converter

Figure 5 shows a step-down DC-to-DC Converter ($V_{OUT} \leq V_{BAT}$) with no feedback control.

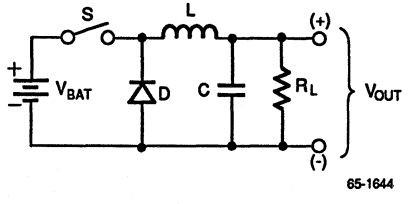


Figure 5. Simple Step-Down Converter

When S is closed, the battery voltage minus the output voltage is applied across the inductor. All of the inductor current will flow into the load until the inductor current exceeds the load current. The excess current will then charge the capacitor and the output voltage will rise. When S is opened, the voltage applied across the inductor will discharge into the load. As in the step-up case, the average inductor current equals the load current. The maximum inductor current I_{MAX} will equal $(V_{BAT} - V_{OUT})/L$ times the maximum on time of the switch transistor (T_{ON}). Current flows to the load during both half cycles of the oscillator.

Complete Step-Down Regulator

Most step-down applications are better served by the 4391 step-down and inverting switching regulator (refer to the 4391 data sheet). However, there is a range of load power for which the 4190 has an advantage over the 4391 in step-down applications. From approximately 500 mW to 2W of load power, the 4190 step-down circuit of Figure 6 offers a lower component count and simpler circuit than the comparable 4391 circuit, particularly when stepping down a voltage greater than 30V.

Since the switch transistor in the 4190 is in parallel with the load, a method must be used to convert it to a series connection for step-down applications. The circuit of Figure 6 accomplishes this. The 2N2907 replaces S of Figure 5, and R6 and R7 are added to provide the base drive to the 2N2907 in the correct polarity to operate the circuit properly.

Greater Than 30V Step-Down Regulator

Adding a zener diode in series with the base of the 2N2907 allows the battery voltage to increase by the value of the zener, with only a slight decrease in efficiency. As an example, if a 24V zener is used, the maximum battery voltage can go to 48V* when using a 4190. Refer to Figure 7.

Note: The addition of the zener diode will not alter the maximum change of supply. With a 24V zener, the circuit will stop operating when the battery voltage drops below 24V + 2.2V = 26.2V.

*Maximum battery voltage is 54V when using RM4190 (30V + 24V).

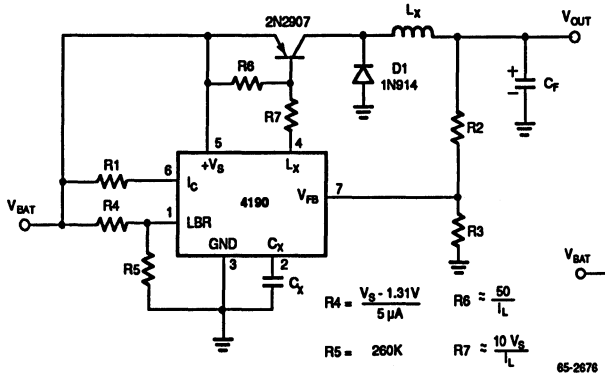


Figure 6. Complete Step-Down Regulator

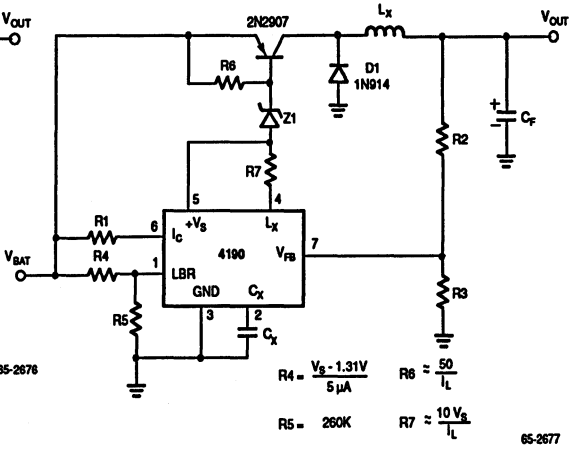


Figure 7. Step-Down Regulator Greater Than 30V

Linear

Design Equations

The inductor value and timing capacitor (C_X) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (I_{MAX}) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±20% as a maximum change from the nominal oscillator frequency.

The worst-case conditions for calculating ability to supply load current are found at the minimum supply voltage; use $+V_S$ (min) to calculate the inductor value. Worst-case conditions for ripple are at $+V_S$ (max).

The value of the timing capacitor is set according to the following equation:

$$f_O\,(Hz) = \frac{2.4 \times 10^6}{C_X\,(pF)}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 4. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Find a value for the start-up resistor R1:

$$R1 = \frac{V_S - 1.2V}{5\,\mu A}$$

Find a value for the feedback resistors R2 and R3:

$$R2 = \frac{V_{OUT} - 1.31V}{I_A}$$

$$R3 = \frac{1.31V}{I_A}$$

Where I_A is the feedback divider current (recommended value is between 50 µA and 100 µA).

Step-Up Design Procedure

1. Select an operating frequency and timing capacitor as shown above (10 kHz to 40kHz is typical).
2. Find the maximum on time (add 5 µS for the turn-off base recombination delay of Q1):

$$T_{ON} = \frac{1}{2F_O} + 5\,\mu s$$

3. Calculate the peak inductor current I_{MAX} (if this value is greater than 375 mA, then an external power transistor must be used in place of Q1):

$$I_{MAX} = \left(\frac{V_{OUT} + V_D - V_S}{(F_O)\,T_{ON}\,[V_S - V_{SW}]}\right) 2I_L$$

where:
V_S = supply voltage
V_D = diode forward voltage
I_L = dc load current
V_{SW} = saturation voltage of Q1 (typ 0.5V)

4. Find an inductance value for L_X:

$$L_X\,(Henries) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right) T_{ON}$$

The inductor chosen must exhibit approximately this value at a current level equal to I_{MAX}

5. Calculate a value for the output filter capacitor:

$$C_F\,(\mu F) = \frac{T_{ON}\left(\frac{V_s\,I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

where V_R = ripple voltage (peak)

Step-Down Design Procedure

1. Select an operating frequency.
2. Determine the maximum on time (T_{ON}) as in the step-up design procedure.

3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(F_O)(T_{ON})\left(\frac{V_S - V_{OUT}}{V_{OUT} - V_D}\right) + 1}$$

4. Calculate L_X:

$$L_X = \left(\frac{V_S - V_{OUT}}{I_{MAX}}\right)(T_{ON})$$

5. Calculate a value for the output filter capacitor:

$$C_F(\mu F) = \frac{(T_{ON})\left(\frac{(V_S - V_{OUT})\, I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

Alternate Design Procedure

The design equations above will not work for the certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, used the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example, the inductor current will be continuous and the alternate procedure will be necessary.

1. Select an operating frequency (a value between 10 kHz and 40 kHz is typical).
2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.
3. Adjust the inductor value down until the desired output voltage is achieved, then go a little lower (approximately 20%) to cover manufacturing tolerances.
4. Check the output voltage with an oscilloscope for ripply, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents [eff = $(V_{OUT})(I_{OUT})/(+V_S)(I_{SY})$ x 100%$].
5. If the efficiency is poor, go back to (1) and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Compensation

When large values (>50 kΩ) are used for the voltage setting resistors, R2 and R3 of Figure 2, stray capacitance at the V_{FB} input can add a lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100 pF to 10 nF in parallel with R2 in Figure 2.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for breadboarding prototypes. Care must be taken to choose a permeable enough core to handle the magnetic flux produced at I_{MAX}; if the core saturates, then efficiency and output current capability are severely degraded and excessive current will flow though the switch transistor. A pot core inductor design section is provided later in this datasheet.

An isolated AC current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 8). This level is determined by the +1.3V reference level and by the selection of two external resistors according to the equation:

Where V_{TH} = Threshold Voltage for Detection

Linear

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery voltage drops below this threshold Q2 will turn on and sink over 1500 µA typically. The low battery detector circuitry may also be used for other, less conventional applications (see Figures 14 and 15).

Automatic Shutdown

The bias control current for the reference is externally set by a resistor from the I_C pin to the battery. This current can vary from 1.0 µA to 50 µA without affecting the operation of the IC. Interrupting this current will disable the entire circuit, causing the output voltage to go to 0V for step-down applications, and reducing the supply current to less than 1.0 µA.

Automatic shutdown of the 4190 can be achieved using the circuit of Figure 9.

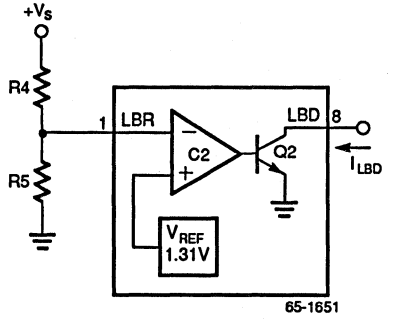


Figure 8. Low Battery Detector

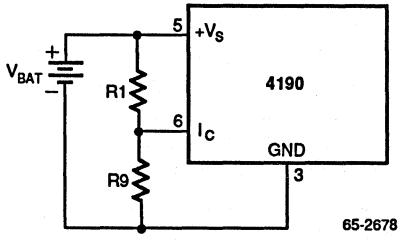


Figure 9. Automatic Shutdown

A resistor is placed from the I_C pin to ground, creating a voltage divider. When the voltage at the I_C pin is less than 1.2V, the 4190 will begin to turn off. This scheme should only be used in limited temperature range applications since the "turn off" voltage at the I_C pin has a temperature coefficient of -4.0 mV/°C. At 25°C, typically 250 nA is the minimum current required by the I_C pin to sustain operation. A 5.0 µA voltage divider works well taking into account the sustaining current of 250 nA and a threshold voltage of 0.4V at turn off. As an example, if 3.0V is to be the turn off voltage, then R9 = 1.1/4.75 µA and R1 = (3.0 - 1.1) 5.0 µA or about 240 kΩ and 390 kΩ respectively. The tempco at the top of the divider will be -4.0 mV (R1 + R9)/R9 or -10.5 mV/°C, an acceptable number for many applications.

Another method of automatic shutdown without temperature limitations is the use of a zener diode in series with the I_C pin and set resistor. When the battery voltage falls below V_Z + 1.2V the circuit will start to shut down. With this connection and the low battery detector, the application can be designed to signal a display when the battery voltage has dropped to the first programmed level, then shut itself off as the battery reaches the zener threshold.

The set current can also be turned off by forcing the I_C pin to 0.2V or less using an external transistor or mechanical switch. An example of this is shown in Figure 10.

In this circuit an external control voltage is used to determine the operating state of the 4190. If the control voltage V_C is a logic 1 at the input of the 4025 (CMOS Triple NOR Gate), the voltage at the I_C pin will be less than 0.5V forcing the 4190 off (<0.1 µA I_{CC}). Both the 2N3904 and 2N2907 will be off insuring long shelf for the battery since less than 1.0 µA is drawn by the circuit.

When V_C goes to a logic 0, 2.0 µA is forced into the I_C pin through the 2.2 MΩ resistor and the NOR gate, and at the same time the 2N3904 and 2N2907 turn on, connecting the battery to the load.

As long as V_C remains low the circuit will regulate the

output to 5.0V. This type of circuit is used to back up the main supply voltage when line interruptions occur, a particularly useful feature when using volatile memory systems.

9.0V Battery Life Extender

Figure 11 shows a common application: a circuit to extend the lifetime of a 9.0V battery. The regulator remains in its quiescent state (drawing only 215 µA) until the battery voltage decays below 7.5V, at which time it will start to switch and regulate the output at 7.0V until the battery falls below 2.2V.

If this circuit operates at its typical efficiency of 80%, with an output current of 10 mA, at 5.0V battery voltage, then the average input current will be I_{IN} = (V_{OUT} x I_L) ÷ (V_{BAT} x e_i) or (7.0V x 10 mA) ÷ (5.0V x 0.8 mA) = 17.5 mA.

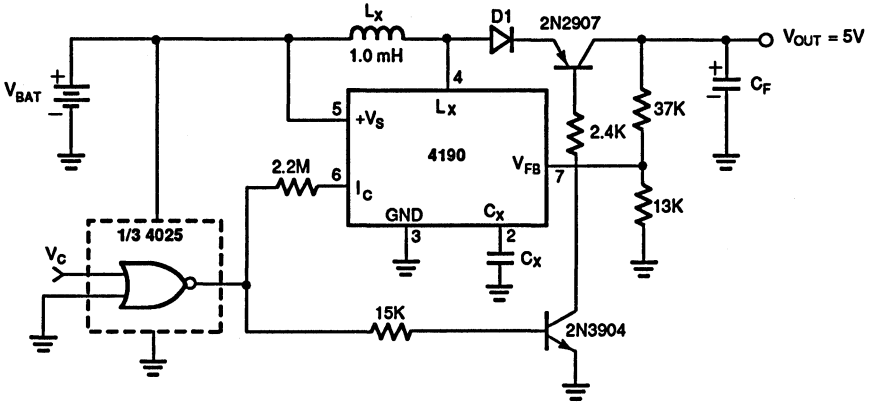
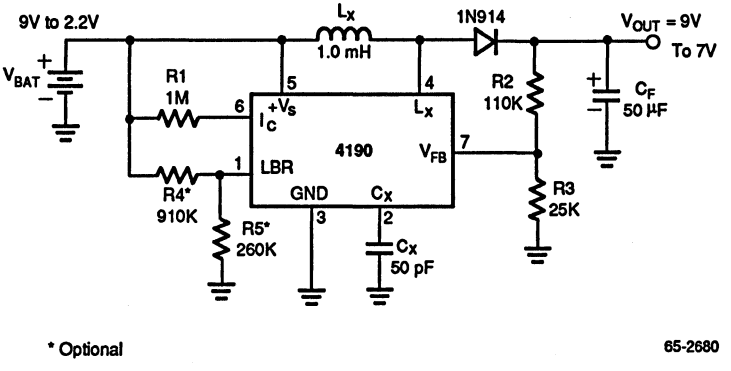


Figure 10. Battery Back-Up Circuit

65-2679



* Optional

65-2680

Figure 11. 9.0V Battery Life Extender

Bootstrapped Operation (Step-Up)

In step-up applications, power to the 4190 can be derived from the output voltage by connecting the $+V_S$ pin and the top of R1 to the output voltage (Figure 12).

One requirement for this circuit is that the battery voltage must be greater than 3.0V when it is energized or else there will not be enough voltage at pin 5 to start up the IC. The big advantage of this circuit is the ability to operate down to a discharged battery voltage of 1.0V.

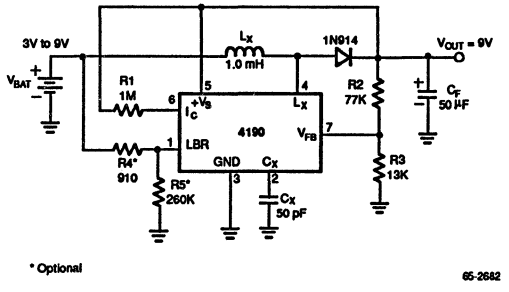


Figure 12. Bootstrapped Operation (Step-Up)

Buck-Boost Circuit (Step-Up/Down)

A disadvantage of the standard step-up and step-down circuits is the limitation of the input voltage range; for a step-up circuit, the battery voltage must always be less than the programmed output voltage, and for a step-down circuit, the battery voltage must always be greater than the output voltage. The following circuit eliminates this disadvantage, allowing a battery voltage above the programmed output voltage to decay to well below the output voltage (see Figure 13).

The circuit operation is similar to the step-up circuit operation, except that both terminal of the inductor are connected to switch transistors. This switching method allows the inductor to be disconnected from the battery during the time the inductor is being discharged. A new discharge path is provided by D1, allowing the inductor to be referenced to ground and independent of the battery voltage. The efficiency of this circuit will be reduced to 55-60% by losses in the extra switch transistor and diode. Efficiency can be improved by choosing transistors with low saturation voltages and by using power Schottky diodes such as Motorola's MBR030.

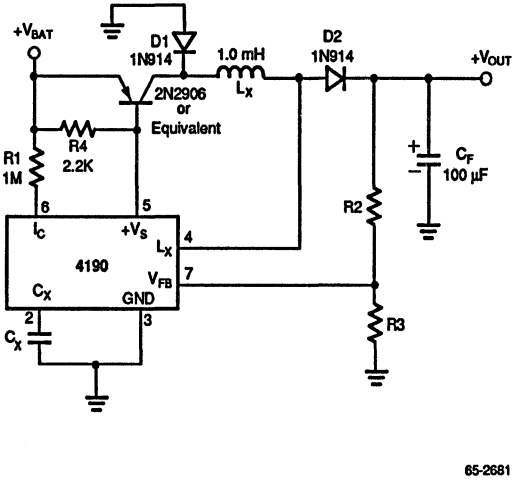


Figure 13. Buck Boost Circuit (Step-Up/Down)

Step-Up Voltage Dependent Oscillator

The 4190's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best, however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This trade-off between load current capability and output ripple can be improved with the circuit connection shown in Figure 14. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre-programmed threshold is reached.

The threshold is programmed exactly as the noram low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery voltage reaches this threshold, the comparator will turn on the open collector transistor at pin 8, effectively putting C2 in parallel with C_x. This added capacitance will reduce the oscillator frequency according to the following equation:

$$F_o \sim \frac{2.4 \times 10^{-6}}{C_x + C2}$$

Where C is in pF and F_o is in Hz.

Component values for a typical application might be R2 = 330 kΩ, R5 = 150 kΩ, C_x = 100 pF, and C2 = 100 pF. These values would set the threshold voltage at 4.1V and change the operating frequency from 48 kHz to 24 kHz. Note that this technique may be used for step-up, step-down, or inverting applications.

Step-Down Regulator With Protection

One disadvantage of the simple application circuits is their lack of short circuit protection, especially for the step-up circuit, which has a very low resistance path for current flow from the input to the output. A current limiting circuit which senses the output voltage and shuts down the 4190 if the output voltage drops too low can be built using the low battery detector circuitry. The low battery detector is connected to sense the output voltage and will shut off the oscillator by forcing pin 2 low if the output voltage drops. Figure 15 shows a schematic of a step-down regulator with this connection.

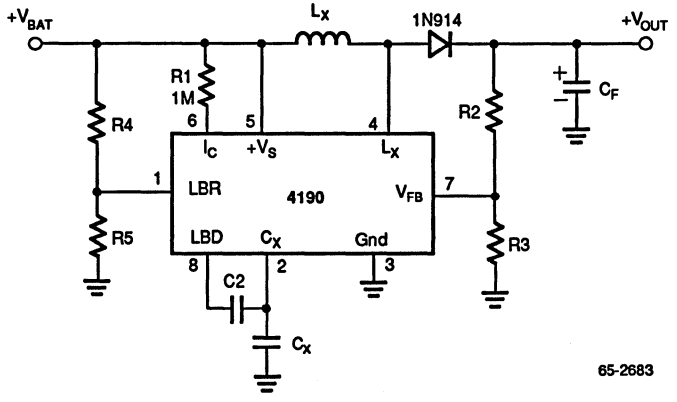


Figure 14. Step-Up Voltage-Dependent Oscillator

R2 and R3 set the output voltage, as in the circuit of Figure 2. Choose resistor values so R5 = R3 and R4 = R2, and make R8 25 to 35 times higher than R3. When the output is shorted, the open collector transistor at pin 8 will force pin 2 low and shut off the oscillator and therefore shut off the external switch transistor. The regulator will then remain in a low current off condition until power is removed and reapplied. C2 provides momentary current to ensure proper start-up. This scheme will not work with the simple step-up regulator, but will work with the boost-buck converter, providing short circuit protection in both step-up and step-down modes.

4190/4391 ± Power Supply

A positive and negative dual tracking power supply using a step-up 4190 and an inverting 4391 is shown in Figure 16. The inductor and capacitor values were chosen to achieve the highest practical output currents from a +12V battery, as it decays, while keeping the output voltage ripple under 100 mVp-p at ±15V output.

The circuit may be adapted to other voltages and currents, but note that the 4190 is step-up, so V_{OUT} must be greater than V_{BAT}.

The output voltages may both be trimmed by adjusting a single resistor value (R3 or R4), because the reference for the negative output is derived from $+V_{OUT}$. This connection also allows the output voltages to track each other with changes in temperature and line voltage.

The timing capacitors are set up exactly as in the voltage dependent oscillator application of Figure 14. The values of R2, R5, C6, and C4 that are given were chosen to optimize for the +12V battery conditions, setting the threshold for oscillator frequency change at V_{BAT} = +8.5V.

As given, this power supply is capable of delivering +45 mA and -15 mA with regulation, until the battery decays below 5.0V.

For information on adjusting the 4391 to meet a specific application refer to the Raytheon 4391 data sheet.

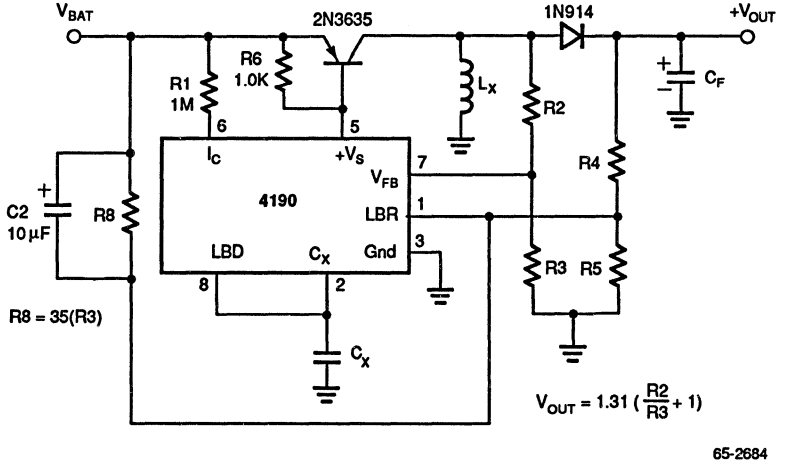


Figure 15. Step-Down Regulator With Protection

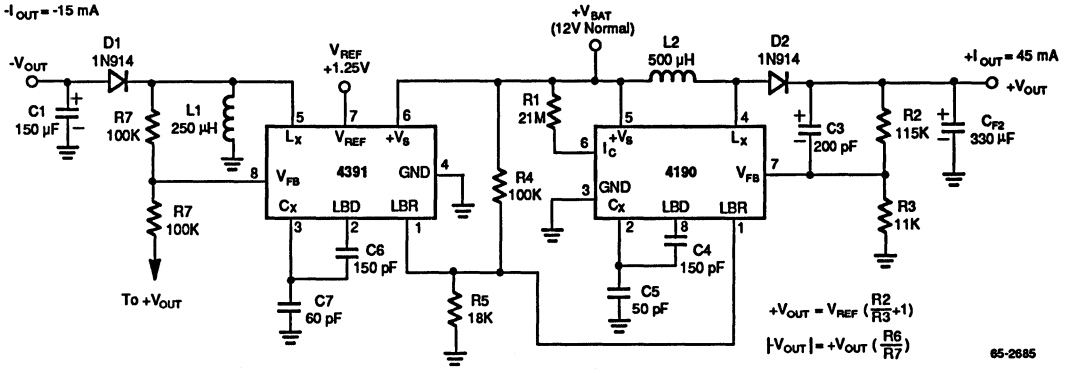


Figure 16. 4190/4391 Power Supply (±15V)

Negative Step-Up Regulator

In the circuit of Figure 17, a bootstrap arrangement of supply and ground pins helps generate an output voltage more negative than the input voltage. On power-up, the output filter capacitor (C_F) will charge through D2 and L_X. When the voltage goes below -2.4V, the 4190 begins switching and charging C_F. The output will regulate at a value equal to the reference voltage (1.31V) plus the zener voltage of D1. RZ sets the value of zener current, stabilized at 1.31V/R2.

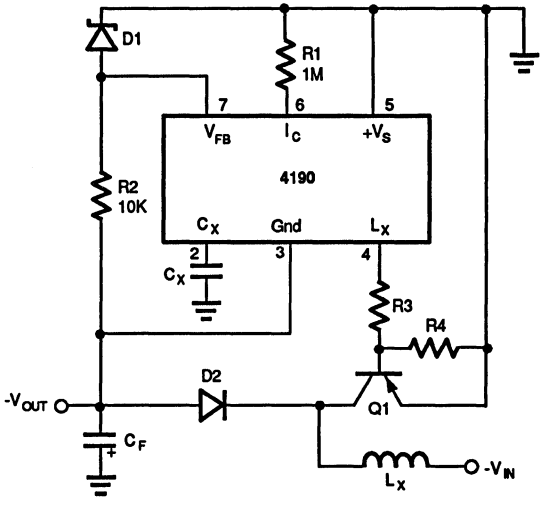
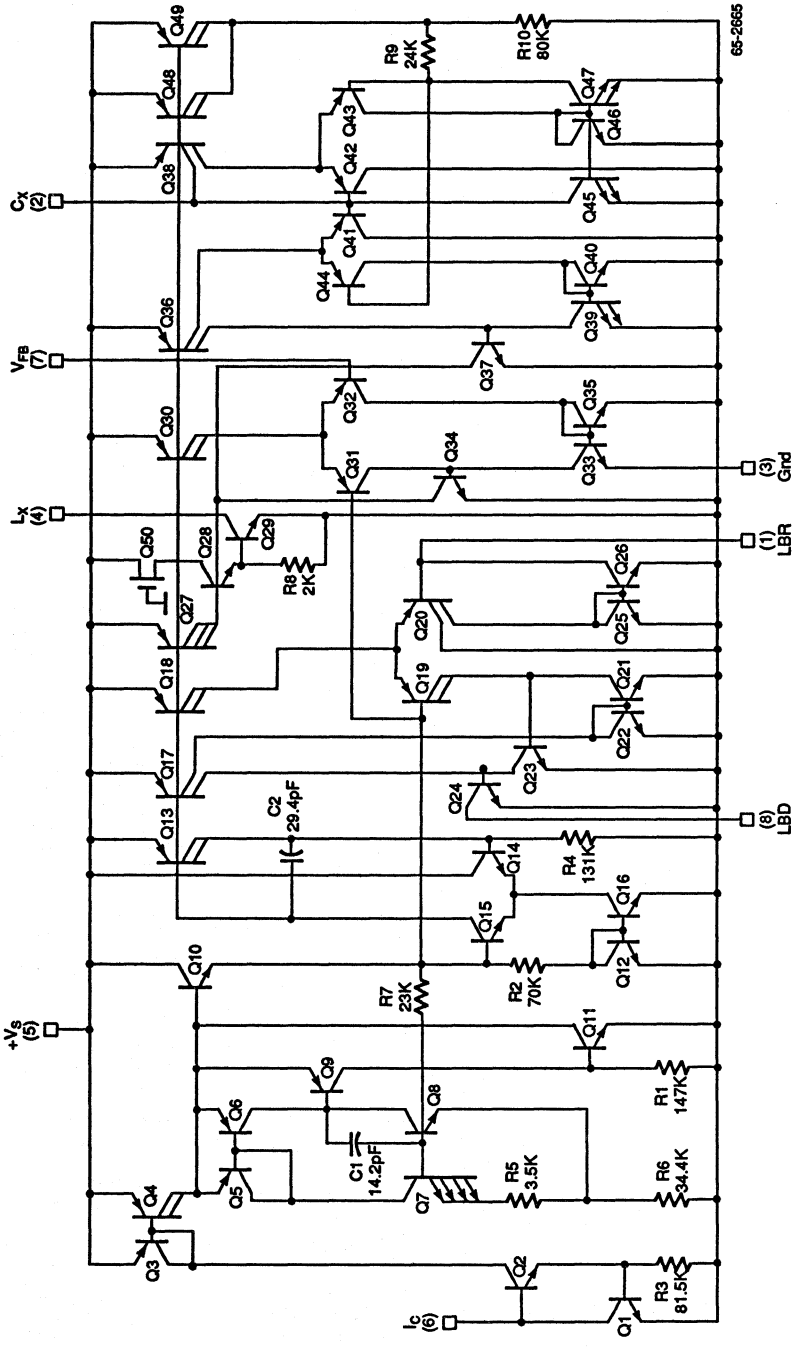
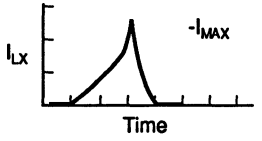
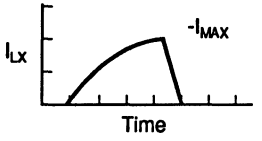
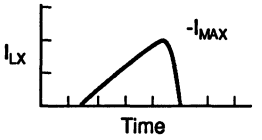


Figure 17. Negative Step-Up Regulator 65-4131

Schematic Diagram



Troubleshooting Chart

Symptom	Possible Problem
Draws excessive supply current on start-up	Battery not "stiff" — inadequate supply bypass capacitor. Inductance value too low. Operating frequency (F_O) too low.
Output voltage is low.	Inductance value too high for F_O or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
L_X in appears noisy — scope will not synchronize.	Normal operating condition.
 Inductor current shows nonlinear waveform.	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
 Inductor current shows nonlinear waveform.	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
 65-6349 Inductor current is linear until high current is reached.	External transistor lacks base drive or beta is too low.
Poor efficiency.	Core saturating. Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high V_{CE} SAT). High series resistance. Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback capacitor from V_{OUT} to V_{FB} (pin 7), 100 to 1000 pF.

Background Information

During the past several years there have been various switching regulator ICs introduced by many manufacturers, all of which attended to the same market, namely controllers for use in power supplies delivering greater than 10W of DC power. Raytheon felt there was another area which could use a switching regulator to even more advance the area of battery powered equipment. Battery powered systems have problems peculiar unto themselves: changes in supply voltage, space considerations, battery life and usually cost. The 4190 was designed with each of these in mind.

The 4190 was partitioned to work in an eight pin package, making it smaller than other controllers which go into 14 and 16 pin packages.

Battery powered applications require the load as seen by the battery to be as small as possible to extend battery life. To this end, the quiescent current of the 4190 is 15 to 100 times less than controllers designed for nonbattery applications. At the same time, the switch transistor can sink 200 mA at 0.4V., comparable to or better than higher powered controllers. As an example, the 4190 configured in the step-up mode can supply 5.0V at 40 mA output with an input of 3.0V.

Cost is usually a primary consideration in battery powered systems. The 4190, guaranteed to work down to 2.2V, can save the designer and end user money as well because battery costs decrease as the number of cells needed goes down.

Soft Start

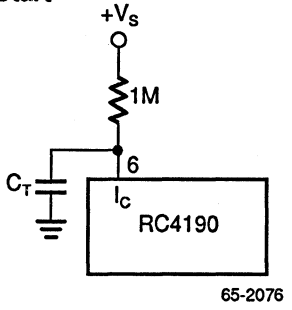


Figure 18: Soft Start Circuit

The delay introduced by the RC time constant at start-up allows the output filter capacitor to charge up, reducing the instantaneous supply current. A typical value for C is in the 0.1µF range.

Bootstrapped Low Voltage Start-Up

Figure 19 shows the bootstrapped application can be "kicked on" using an extra capacitor and triple pole double throw switch (3PDT). This connection allows the circuit to start up using a single Ni-Cad cell of 1.2V to 1.6V. When power is first applied the 1.2V battery does not provide enough voltage to meet the minimum 2.2V supply voltage requirement. The 22µF capacitor, when switched, temporarily doubles the battery voltage to bias up the 4190.

When the switch is the down position, the capacitor charges up to the battery voltage. The, when the switch is changed to the up position, the capacitor is put in series connection with the battery, and the doubled voltage is applied directly to the positive power supply lead of the 4190. This voltage is enough to bias the junctions internal to the 4190 and gets it started. Then, when the stepped up output voltage reaches a high enough value, diode D1 is forward biased and the output voltage takes over supplying power to the 4190. The circuit is shown with component values for +5V output, but the circuit can be set up for other voltages.

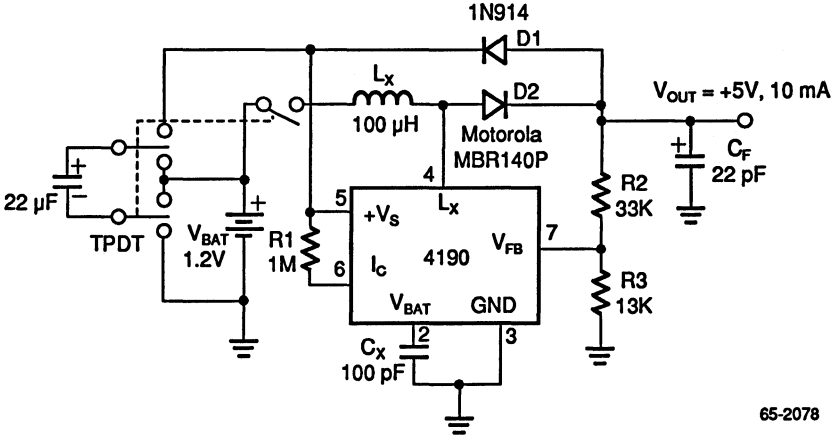


Figure 19: Bootstrapped Low Voltage Start-up

Linear

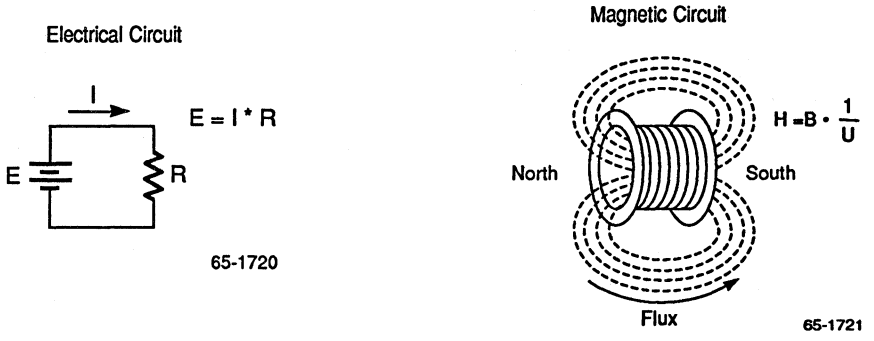


Figure 20. Electricity Versus Magnetism

Electricity Versus Magnetism

Electrically the inductor must meet just one requirement, but that requirement can be hard to satisfy. The inductor must exhibit the correct value of inductance (L, in Henrys) as the inductor current rises to its highest operating value (I_{MAX}). This requirement can be met most simply by choosing a very large core and winding it until it reaches the correct inductance value, but that brute force technique wastes size, weight and money. A more efficient design technique must be used.

Question: What happens if too small a core is used?

First, one must understand how the inductor's magnetic field works. The magnetic circuit in the inductor is very similar to a simple resistive electrical circuit (see Figure 20). There is a magnetizing force (H, in oersteds), a flow of magnetism, or flux density (B, in Gauss), and resistance to the flux, called permeability (U, in Gauss per oersted). H is equivalent to voltage in the electrical model, flux density is like current flow, and permeability is like resistance (except for two important differences discussed on the following page).

First Difference: Permeability, instead of being analogous to resistance, is actually more like conductance (1/R). As permeability increases, flux increases.

Second Difference: Resistance is a linear function. As voltage increases, current increases proportionally, and the resistance value stays the same. In a magnetic circuit the value of permeability varies as the applied magnetic force varies. This nonlinear characteristic is usually shown in graph form in ferrite core manufacturer's data sheets. See Figure 21.

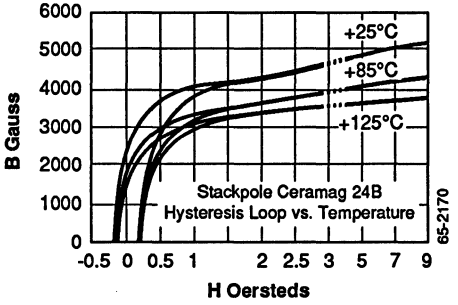


Figure 21: Typical Manufacturer's Curve Showing Saturation Effects

As the applied magnetizing force increases, at some point the permeability will start decreasing, and therefore the amount of magnetic flux will not increase any further, even as the magnetizing force increases. The physical reality is that, at the point where the permeability decreases, the magnetic field has realigned all of the magnetic domains in the core material. Once all of the domains have been aligned the core will then carry no more flux than just air; it becomes as if there were no core at all. This phenomenon is called saturation. Because the inductance value, L, is dependent on the amount of flux, core saturation will cause the value of L to decrease dramatically, in turn causing excessive and possibly destructive inductor current.

Pot Cores for 4190

Pot core inductors are best suited for the 4190 micropower switching regulator for several reasons:

1. **They are available in a wide range of sizes.** 4190 applications are usually low power with relatively low peak currents (less than 500mA). A small inexpensive pot core can be chosen to meet the circuit requirements.
2. **Pot cores are easily mounted.** They can be bolted directly to the PC card adjacent to the regulator IC.
3. **Pot cores can be easily air-gapped.** The length of the gap is simply adjusted using different washer thicknesses. Cores are also available with predetermined air gaps.
4. **Electromagnetic interference (EMI) is kept to a minimum.** The completely enclosed design of pot core reduces stray electromagnetic radiation — an important consideration of the regulator circuit is built on a PC card with other circuitry.

Core Size

Question: Is core size selected according to load power?

Not quite. Core size is dependent on the amount of energy stored, not on load power. Raising the operating frequency allows smaller cores and windings. Reduction of the size of the magnetics is the main reason switching regulator design tends toward higher operating frequency. Designs with the 4190 should use 75kHz as a maximum running frequency, because the turn off delay of the power transistor and stray capacitive coupling begin to interfere. Most applications are in the 10 to 50kHz range, for efficiency and EMI reasons.

The peak inductor current (IMAX) must reach a high enough value to meet the load current drain. If the operating frequency is increased, and simultaneously the inductor value is decreased, then the core can be made smaller. For a given core size and winding, an increase in air gap spacing (an air gap is a break in the material in the magnetic path, like a section broken off a doughnut) will cause the inductance to

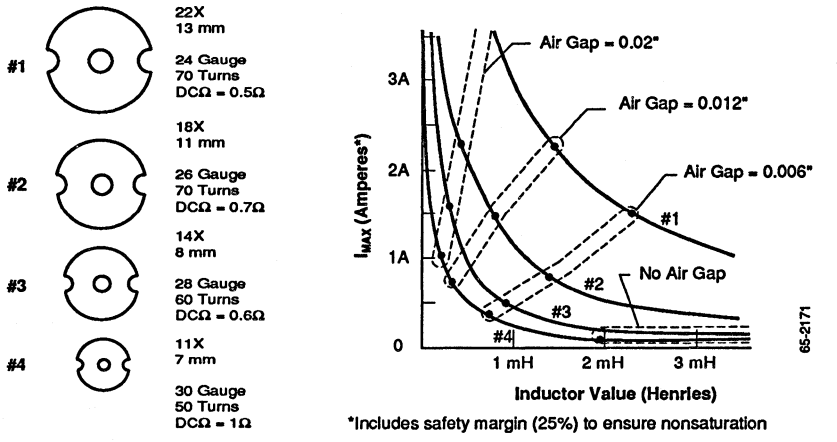


Figure 22: Inductor Design Aid

decrease and I_{MAX} (the usable peak current before saturation) to increase.

The curves shown in Figure 21 are typical of the ferrite manufacturer's power HF material, such as Siemens N27 or Stackpole 24B, which are usually offered in standard millimeter sizes including the sizes shown.

Use of the Design Aid Graph (Figure 22)

1. From the application requirement, determine the inductor value (L) and the required peak current (I_{MAX}).
2. Observe the curves of the design aid graph and determine the smallest core that meets both the L and I requirements.
3. Note the approximate air gap at I_{MAX} for the selected core, and order the core with the gap. (If the gapping is done by the user, remember that a washer spacer results in an air gap of twice the washer thickness, because two gaps will be created, one at the center post and one at the rim, like taking two bites from a doughnut.)
4. If the required inductance is equal to the indicated value on the graph, then wind the core with the number of turns shown in table of sizes. The turns given are the maximum number for that gauge of wire that can be easily wound in the cores winding area.
5. If the required inductance is less than the value indicated on the graph, a simple calculation must be done to find the adjusted number of turns. Find AL (inductance index) for a specific air gap.

$$\frac{L\ (\text{indicated})}{\text{Turns}^2} = A_L\ (\text{in Henrys/turn}^2)$$

Then divide the required inductance value by A_L to give the actual turns squared, and take the square root to find the actual turns needed.

$$\text{Actual Turns} = \frac{L\ (\text{required})}{A_L}$$

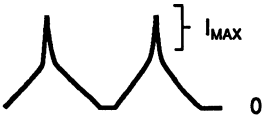
If the actual number of turns is significantly less than the number from the table then the wire size can be increased to use up the left-over winding area and reduce resistive losses.

6. Wind and gap the core as per calculations, and measure the value with an inductance meter. Some adjustment of the number of turns may be necessary.

   The saturation characteristics may be checked with the inductor wired into the switching regulator application circuit. To do so, build and power up the circuit. Then (recommend Tektronix P6042 or equivalent) around the inductor lead and monitor the current in the inductor. Draw the maximum load current from the application circuit so that the regulator is running at close to full duty cycle. Compare the waveform you see to those pictured in Figure 23.

   Check for saturation at the highest expected ambient temperature.

Proper Operation
(Waveform is Fairly Linear)



65-1723

Improper Operation
(Waveform is Nonlinear, Inductor is Saturating)

65-1723

Figure 23: Inductor Current Waveforms

7. After the operation in circuit has been checked, reassemble and pot the core using a potting compound recommended by the manufacturer.

   If the core material differs greatly in magnetic characteristics from the standard power material shown in Figure 22, then the following general equation can be used to help in winding and gapping. This equation can be used for any core geometry, such as an E-E core.

$$L_x = \frac{(1.26)(N^2)(Ae)(10^8)}{g = (le/ue)}$$

   Where: N = number of turns
   Ae = core area from data sheet (in cm^2)
   le = magnetic path length from data sheet (in cm)
   ue = permeability of core from manufacturer's graph
   g = center post air gap (in cm)

Manufacturers
Below is a list of several pot core manufacturers:

Ferroxcube Company
5083 Kings Highway
Saugerties, NY 12477

Indiana General Electronics
Keasley, NJ 08832

Siemens Company
186 Wood Avenue South
Iselin, NJ 08830

Stackpole Company
201 Stackpole Street
St. Mary, PA 15857

TDK Electronics
13-1-Chome
Nihonbaski, Chuo-ku, Tokyo

RC4191/4192/4193
Micropower Switching Regulators

Description

The RC4191/4192/4193 series of monolithic ICs are low power switch mode regulators intended for miniature power supply applications. These DC-to-DC converter ICs provide all of the active components needed to create supplies for micropower circuits. Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

These regulators can achieve up to 85% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 µA.

The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the 4193 adaptable to a wide range of miniature power supply applications.

The 4193 is most suited for single ended step-up ($V_{OUT} > V_{IN}$) circuits because the NPN internal switch transistor is referenced to ground. It is complemented by Raytheon's micropower switching regulator, the 4391, which is dedicated to step-down ($V_{OUT} < V_{IN}$) and inverting $V_{OUT} = -V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the 4391 data sheet for step-down and inverting applications.

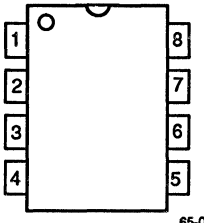
The 4191/92/93 series of micropower switching regulators consists of three devices, each with slightly different specifications. The RM4191 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The RC4192 has a 3.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 30V. The 4193 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical for the 4191, 4192 and 4193. Each type is available in commercial, industrial, and military temperature ranges, and in plastic and ceramic DIPs and S0-8 packages.

Features

- High efficiency — 85% typical
- Low quiescent current — 215 µA
- Adjustable output — 1.3V to 30V
- High switch current — 200 mA
- Bandgap reference — 1.31V
- Accurate oscillator frequency — ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8-lead packages

Connection Information

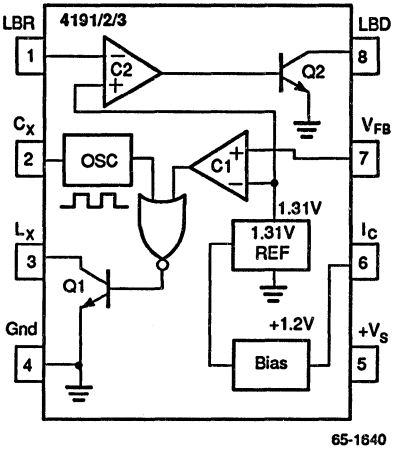
8-Lead DIP
(Top View)



65-0070

Pin	Function
1	Low Battery (Set) Resistor (LBR)
2	Timing Capacitor (C_X)
3	External Inductor (L_X)
4	Ground
5	+ Supply Voltage ($+V_S$)
6	Reference Set Current (I_C)
7	Feedback Voltage (V_{FB})
8	Low Battery Detector Output (LBD)

Functional Block Diagram



65-1640

Ordering Information

Part Number	Package	Operating Temperature Range
RC4191M	M	0°C to +70°C
RC4192M	M	0°C to +70°C
RC4193M	M	0°C to +70°C
RC4191N	N	0°C to +70°C
RC4192N	N	0°C to +70°C
RC4193N	N	0°C to +70°C
RV4191N	N	-25°C to +85°C
RV4192N	N	-25°C to +85°C
RV4193N	N	-25°C to +85°C
RM4191D	D	-55°C to +125°C
RM4192D	D	-55°C to +125°C
RM4193D	D	-55°C to +125°C
RM4191D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
M = 8-lead plastic SOIC

Absolute Maximum Ratings(1)

Supply Voltage (Without External Transistor)
- 4191, 4192 ..... +30V
- 4193 ..... +24V

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- RM4191/2/3 ..... -55°C to +125°C
- RV4191/2/3 ..... -25°C to +85°C
- RC4191/2/3 ..... 0°C to +70°C

Switch Current ..... 375 mA Peak

Note:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	Small Outline SO-8
Max. Junction Temp.	+125°C	+175°C	+125°C
Max. P_D T_A<50°C	468 mW	833 mW	300 mW
Therm. Res θ_{JC}	—	45°C/W	—
Therm. Res. θ_{JA}	160°C/W	150°C/W	240°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	4.17 mW/°C

Electrical Characteristics

(V_S = +6.0V, I_C = 5.0 µA, and T_A = +25°C unless otherwise noted)

			4191			4192			4193			
Parameters	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Supply Voltage	$+V_S$		2.2		30	2.2		30	2.2		24	V
Reference Voltage (Internal)	V_{REF}		1.29	1.31	1.33	1.27	1.31	1.35	1.24	1.31	1.38	V
Switch Current	I_{SW}	V_3 = 400mV	100	200		100	200		100	200		mA
Supply Current	I_{SY}	Measure at Pin 5 I_3 = 0		215	300		215	300		215	300	µA
Efficiency	ef			85			85			85		%
Line Regulation		0.5 V_0<V_S<V_0		0.04	0.2		0.04	0.5		0.04	0.5	%V_0
Load Regulation	L_I	V_S = +0.5 V_0, P_L = 150mW		0.2	0.5		0.2	0.5		0.2	0.5	%V_0
Operating Frequency Range[1]	F_0		0.1	25	75	0.1	25	75	0.1	25	75	kHz
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	µA
Switch Leakage Current	I_{CO}	V_3 = 24V (4193) V_3 = 30V(4191/2)		0.01	5.0		0.01	5.0		0.01	5.0	µA
Supply Current (Disabled)	I_{SO}	V_C≤ 200 mV		0.1	5.0		0.1	5.0		0.1	5.0	µA
Low Battery Bias Current	I_1	V_1 = 1.2V		0.7			0.7			0.7		µA
Capacitor Charging Current	I_{CX}			8.6			8.6			8.6		µA
Oscillator Frequency Tolerance				±10			±10			±10		%

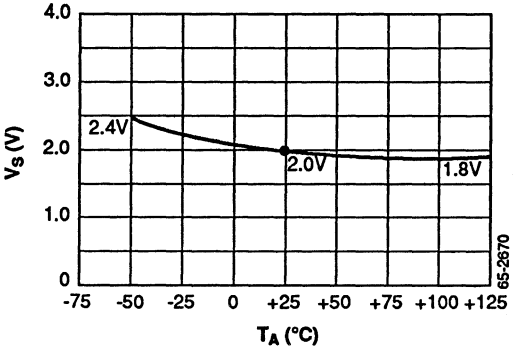
Electrical Characteristics (Continued)

(V_S = +6.0V, I_C = 5.0 µA, and T_A = +25°C unless otherwise noted)

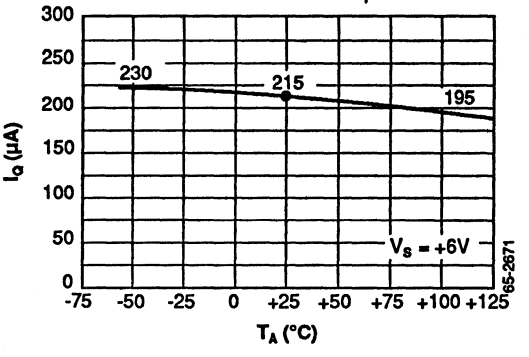
Parameters	Symbol	Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Capacitor Threshold Voltage +	$+V_{THX}$			1.4			1.4			1.4		V
Capacitor Threshold Voltage -	$-V_{THX}$			0.5			0.5			0.5		V
Feedback Input Current	I_{FB}	V_7 = 1.3V		0.1			0.1			0.1		µA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V V_1 = 1.1V	500	1500		500	1500		500	1500		µA
($+V_S$ = 6.0V, I_C = 5.0 µA, unless otherwise noted, over the full operating temperature range)												
Supply Voltage	$+V_S$		2.6		30	2.6		30	2.6		24	V
Reference Voltage (Internal)	V_{REF}		1.25	1.31	1.37	1.23	1.31	1.39	1.20	1.31	1.42	V
Supply Current	I_{SY}	Measure at Pin 5 I_3 = 0		225	350		225	350		225	350	µA
Line Regulation		$0.5V_0 < +V_S < V_0$		0.2	0.5		0.5	1.0		0.5	1.0	%V0
Load Regulation	L_1	V_S = +0.5 V_0, P_L = 150 mW		0.5	1.0		0.5	1.0		0.5	1.0	%V0
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	µA
Switch Leakage Current	I_{CO}	V_3 = 24V (4193) V_3 = 30V(4191/2)			30			30			30	µA
Supply Current (Disabled)	I_{SO}	$V_C \leq$ 200 mV			30			30			30	µA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1200		500	1200		500	1200		µA
Oscillator Frequency Temperature Drift				±200			±200			±200		ppm/°C

Typical Performance Characteristics

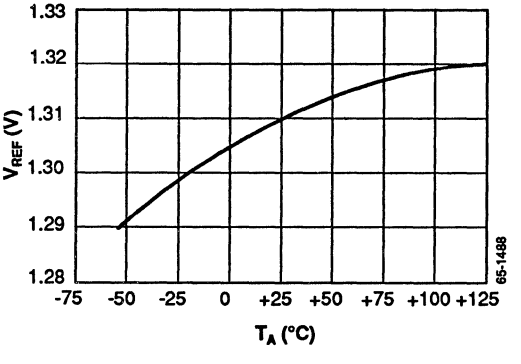
Minimum Supply Voltage vs. Temperature



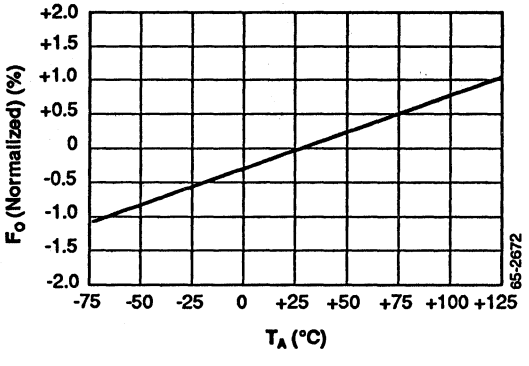
Quiescent Current vs. Temperature



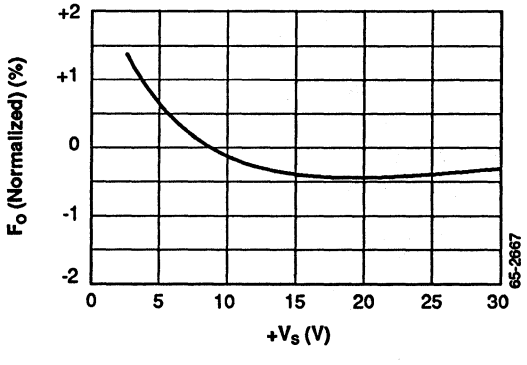
Reference Voltage vs. Temperature



Oscillator Frequency vs. Temperature



Oscillator Frequency vs. Supply Voltage



Linear

Principles of Operation

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up ($V_{OUT} > V_{BAT}$) DC-to-DC Converter (Figure 1).

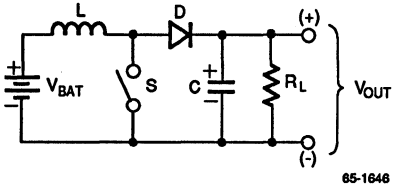


Figure 1. Simple Step-Up Converter

When switch S is closed, the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened, the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{MAX} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant DC voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened, the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete 4193 regulator, a feedback control system adjusts the on-time of the switch, controlling the level of inductor current, so that the average inductor discharge current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in figure 2. The ideal switch in the DC-to-DC Converter diagram is replaced by an open collector NPN transistor Q1. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the 4193 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} - V_D$.

At this point, the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again, the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple DC-to-DC Converter does; i.e., it stores energy in the inductor during the on-time and releases it into the capacitor during the off-time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter, this feedback system will vary the duration of the on-time in response to changes in load current or battery voltage (see Figure 3). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and time.

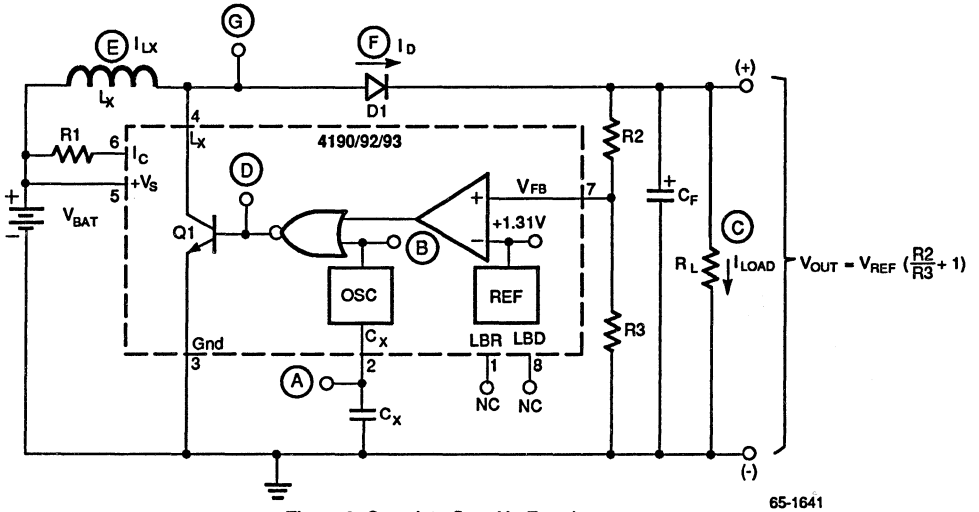


Figure 2. Complete Step-Up Regulator

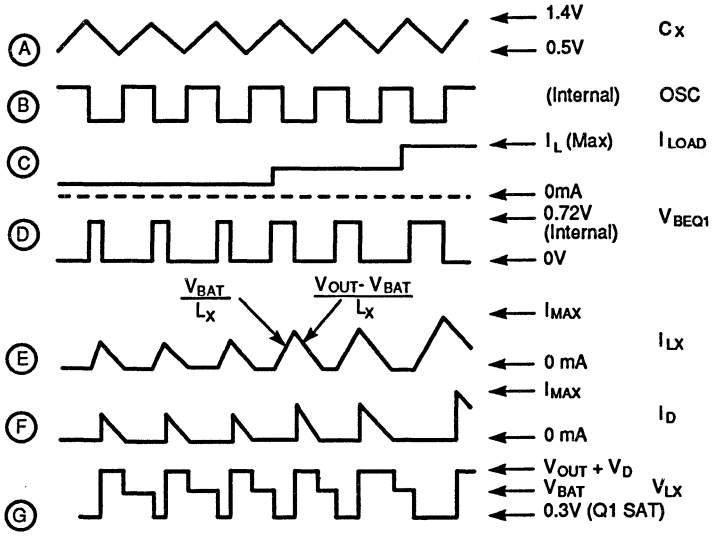
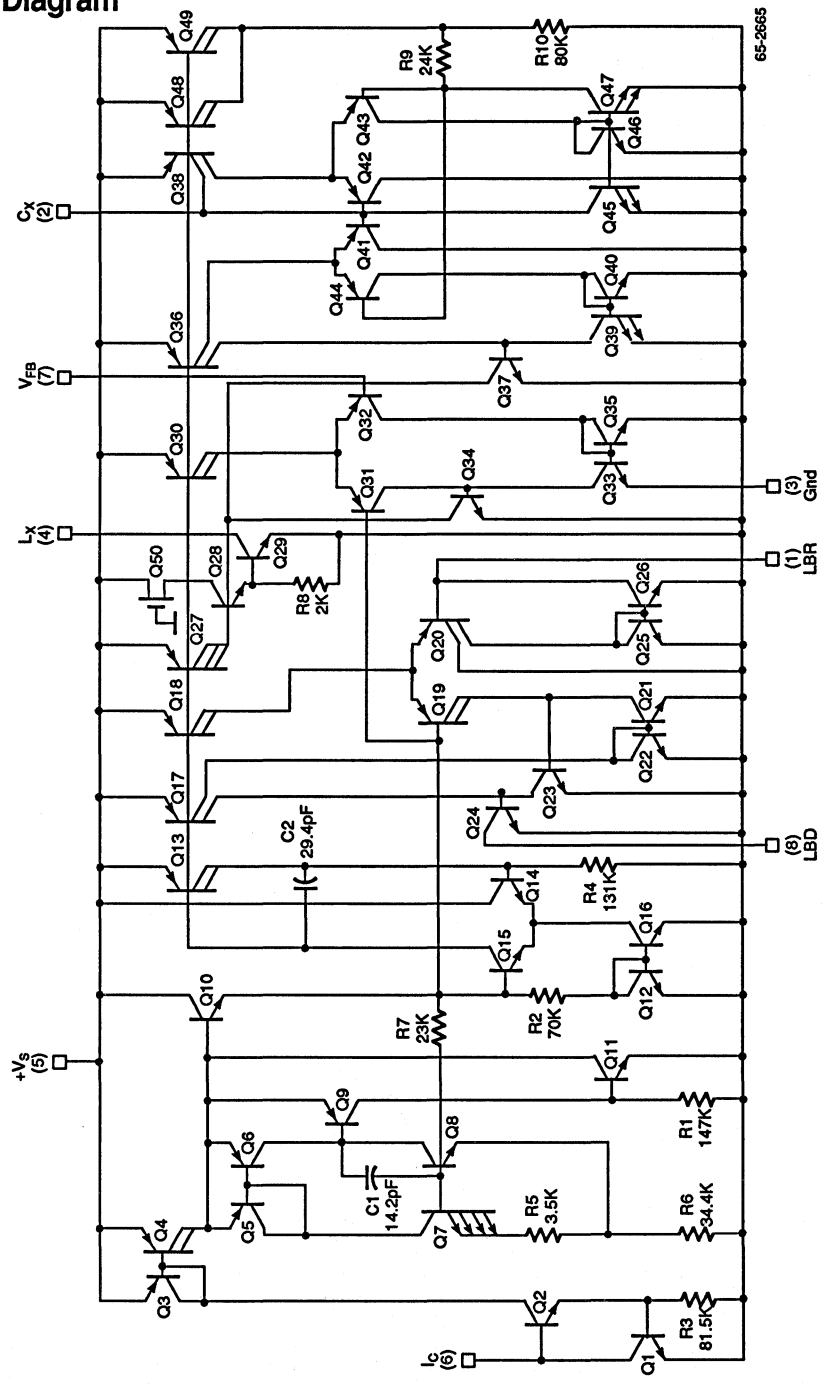


Figure 3. Step-Up Regulator Waveforms

Linear

Schematic Diagram



RC4194
Dual Tracking Voltage Regulators

Description

The RC/RM4194 are dual polarity tracking regulators designed to provide balanced or unbalanced positive and negative output voltages at currents to 200 mA. A single external resistor adjustment can be used to change both outputs between the limits of ±50 mV and ±42V.

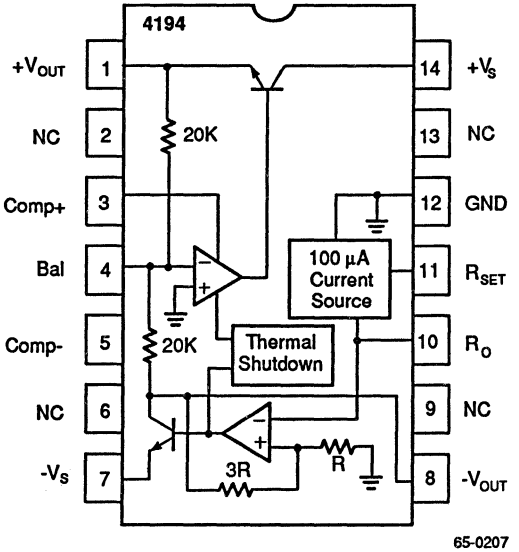
These devices are designed for local "on-card" regulation, eliminating distribution problems associated with single-point regulation. To simplify application the regulators require a minimum number of external parts.

The device is available in three package types to accommodate various power requirements. The K (TO-66) power package can dissipate up to 3W at T_A = +25°C. The D 14-pin dual in-line will dissipate up to 1W and the N 14-pin dual in-line will dissipate up to 625 mW.

Features

- Simultaneously adjustable outputs with one resistor to ±42V
- Load current — ±200 mA with 0.04% load regulation
- Internal thermal shutdown at T_J = +175°C
- External balance for $\pm V_{OUT}$ unbalancing
- 3W power dissipations

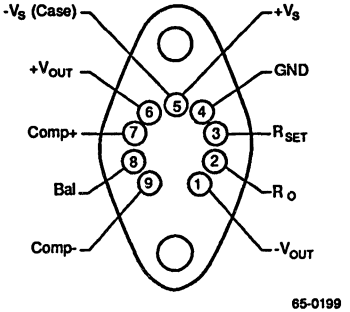
Functional Block Diagram



65-0207

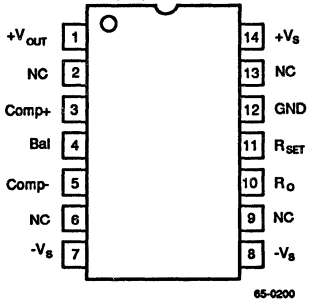
Connection Information

9-Lead TO-66 Package (Top View)



65-0199

14-Lead Plastic & Ceramic DIP (Top View)



65-0200

Linear

Ordering Information

Part Number	Package	Operating Temperature Range
RC4194N	N	0°C to +70°C
RC4194D	D	0°C to +70°C
RC4194K	K	0°C to +70°C
RM4194D	D	-55°C to +125°C
RM4194D/883B	D	-55°C to +125°C
RM4194K	K	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
K = 9-lead TO-66

Absolute Maximum Ratings(1)

Supply Voltage
RC4194 ..... ±35V
RM4194 ..... ±45V
Supply Input to Output Voltage Differential
RC4194 ..... ±35V
RM4194 ..... ±45V
Load Current
N Package ..... 100 mA
D Package ..... 150 mA
K Package ..... 250 mA
Operating Temperature Range
RC4194 ..... 0°C to +70°C
RM4194 ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature (60 sec) ..... +300°C

Note:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP	9-Lead TO-66 Metal Can
Max. Junction Temp.	+125°C	+175°C	+150°C
Max. P_D T_A<50°C	468mW	1042mW	2381mW
Therm. Res θ_{JC}	—	60°C/W	7°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W	42°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.38 mW/°C	23.81 mW/°C

Electrical Characteristics

($\pm 5 \le V_{OUT} \le V_{MAX}$; $-V_{IN} \le -8V$; $I_L = \pm 1mA$; RM4194: $-55°C \le T_A \le +125°C$; RC4194: $0°C \le T_A \le +70°C$ unless otherwise specified)

Parameters	Test Conditions	Min	Typ	Max	Units
Line Regulation	$\Delta V_S = 0.1\ V_{IN}$		0.04	0.1	$\%V_{OUT}$
Load Regulation[1]	4194K: $I_L < 200$ mA 4194D: $I_L < 100$ mA $\pm V_S = \pm(V_{OUT} + 5)V$		0.002	0.004	$\%V_{OUT} / I_L$ (mA)
Output Voltage Drift With Temperature [2]					
Positive Output	$V_{OUT} = \pm 5V$		0.002	0.015	%/°C
Negative Output	$V_{OUT} = \pm 5V$		0.,003	0.015	%/°C
Supply Current[3] (Positive)	$V_S = \pm V_{MAX}$, $V_{OUT} = 0V$, $I_L = 0$ mA		+0.8	+2.5	mA
Supply Current[4] (Negative)	$V_S = \pm V_{MAX}$, $V_{OUT} = 0V$, $I_L = 0$ mA		-1.8	-4.0	mA
Supply Voltage	RM4194	±9.5		±45	V
	RC4194	±9.5		±35	
Output Voltage Scale Factor	$R_{SET} = 71.5$ kΩ, $T_A = +25°C$, $V_S = \pm V_{MAX}$	2.38	2.5	2.62	kΩ/V
Output Voltage Range	RM4194: $R_{SET} = 71.5$ kΩ, $I_L = 25$ mA	0.05		±42	V
	RC4194: $R_{SET} = 71.5$ kΩ, $I_L = 25$ mA	0.05		±42	
Output Voltage Tracking			±0.4	±2.0	%
Ripple Rejection	F = 120 Hz, $T_A = +25°C$		70		dB
Input-Output Voltage Differential	$I_L = 50$ mA, $T_A = +25°C$	3.0			V
Short Circuit Current	$V_S = \pm 30V$, $T_A = +25°C$		300		mA
Output Noise Voltage	$C_L = 4.7$ µF, $V_{OUT} = \pm 15V$ F = 10 Hz to 100 kHz		250		μV_{RMS}
Internal Thermal Shutdown			175		°C

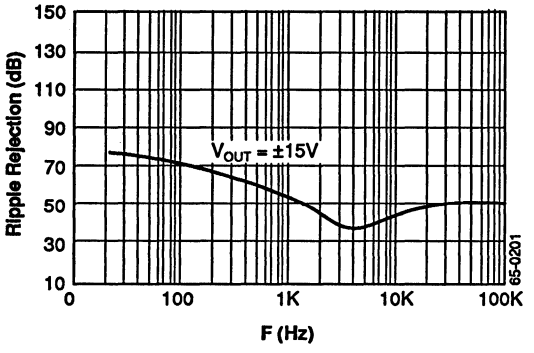
Notes:

1. Measured as $\left(\frac{\Delta V_{OUT}}{V_{OUT}} \times 100\%\right) / I_L$ (mA)
2. Output voltage temperature drift guaranteed by design.
3. The current drain will increase by $50\mu A/V_{OUT}$ on positive side and $100\mu A/V_{OUT}$ on negative side.
4. The specifications above apply for the given junction temperatures since pulse test conditions are used.

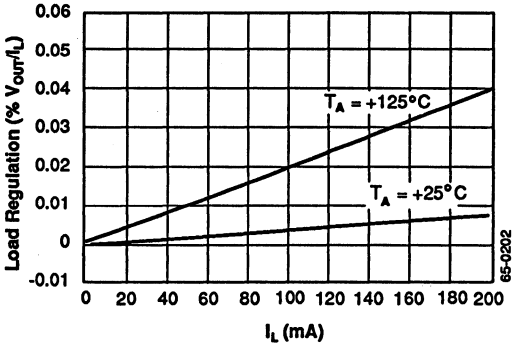
Linear

Typical Performance Characteristics

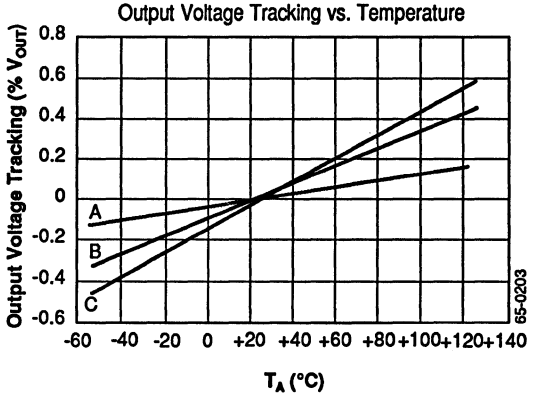
Ripple Rejection vs. Frequency



Load Regulation vs. Load Current



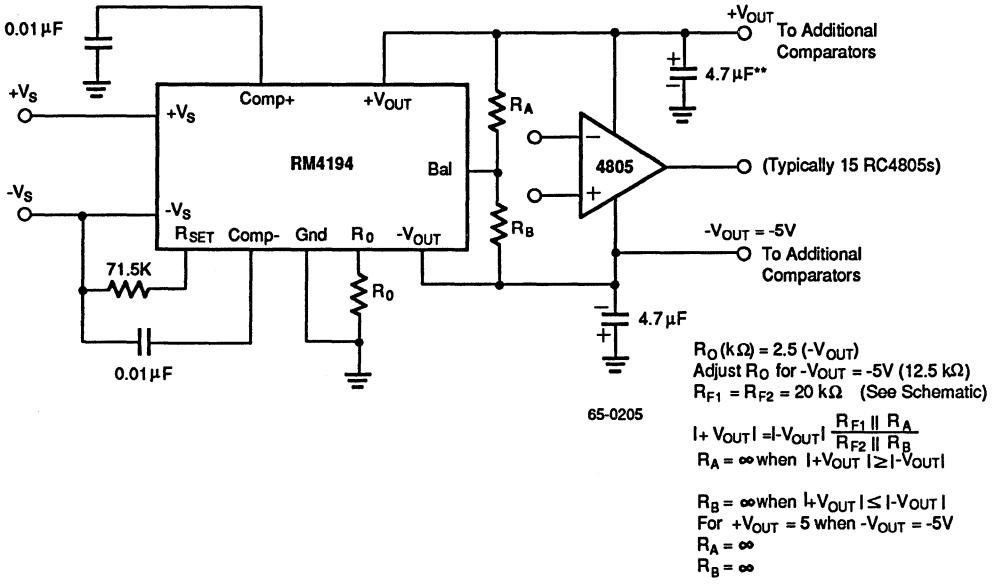
Output Voltage Tracking vs. Temperature



A = % Tracking of V_{OUT}
B = T.C. for Positive Regulator
C = T.C. for Negative Regulator

Typical Applications

Unbalanced Output Voltage — Comparator Application



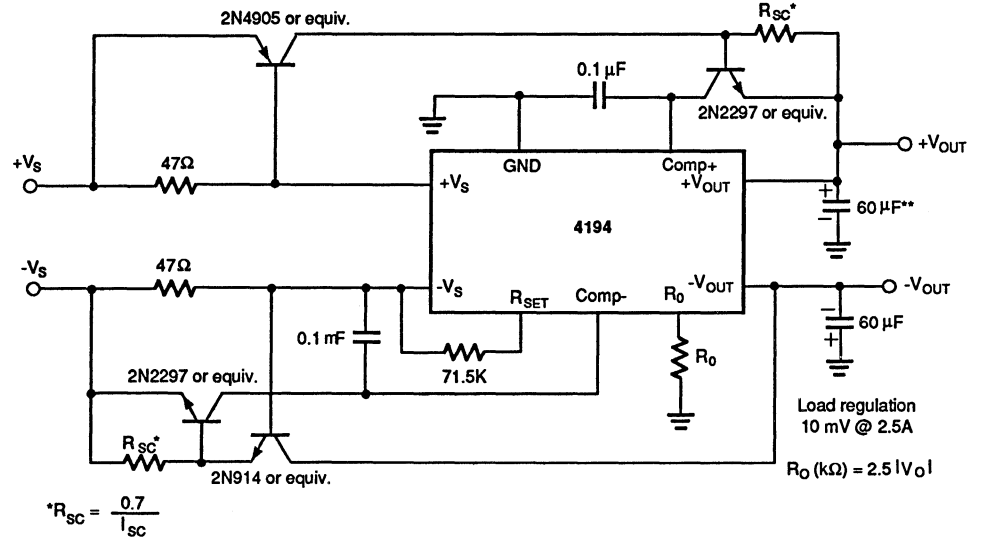
R_O (kΩ) = 2.5 ($-V_{OUT}$)
Adjust R_O for $-V_{OUT}$ = -5V (12.5 kΩ)
$R_{F1} = R_{F2}$ = 20 kΩ (See Schematic)

$$|+V_{OUT}| = |-V_{OUT}| \frac{R_{F1} \parallel R_A}{R_{F2} \parallel R_B}$$

$R_A = \infty$ when $|+V_{OUT}| \geq |-V_{OUT}|$

$R_B = \infty$ when $|+V_{OUT}| \leq |-V_{OUT}|$
For $+V_{OUT}$ = 5 when $-V_{OUT}$ = -5V
$R_A = \infty$
$R_B = \infty$

High Output Application



R_O (kΩ) = 2.5 $|V_O|$

$^*R_{SC} = \frac{0.7}{I_{SC}}$

**Optional usage - Not as critical as $-V_O$ bypass capacitors.

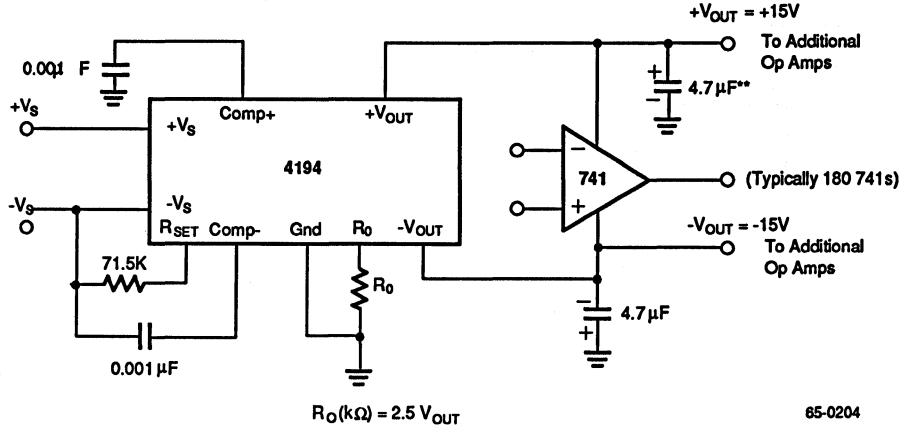
Note: Compensation and bypass capacitor connections should be close as posibe to the 4194

65-0206

Linear

Typical Applications (Continued)

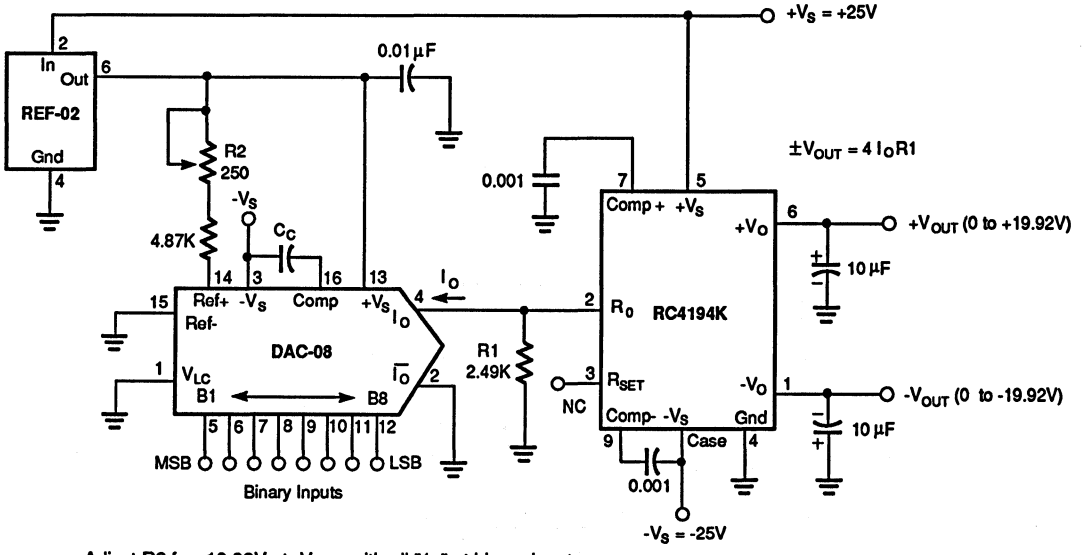
Balanced Output Voltage — Op Amp Application



$R_O(k\Omega) = 2.5\ V_{OUT}$

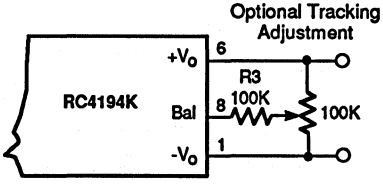
65-0204

Digitally Controlled Dual 200 mA Voltage Regulator



Adjust R2 for -19.92V at $-V_{OUT}$ with all "1s" at binary inputs, then optionally adjust R3 for +19.92V at $+V_{OUT}$

Optional Tracking Adjustment



65-1725

4194 Switchable Power Supply

The outputs of the 4194 can be simultaneously switched on or off under logic control as shown in Figure 1. In the "off" state, the outputs will be forced to a minimum voltage, or about ±20 mV, rather than becoming open-circuit. The turn-on time, with the outputs programmed to ±12V, is approximately 200 µS. This circuit works by forcing the R_0 pin to ground with an analog switch.

Refer to the 4194 internal schematic diagram. A reference voltage that regulates with respect to $-V_S$ is generated at the R_{SET} pin by the zener diode Q12 and the buffer circuit of Q11 and Q13. When the external 71.5k R_{SET} resistor is connected between the R_{SET} pin and $-V_S$, a precision current of 100 µA is generated which then flows into Q13's collector. Since Q13's collector is tied to the R_0 pin, the 100 µA current will develop a ground-referenced voltage drop proportional to the value of R_0, which is then amplified by the internal error amplifier. When the analog switch in Figure 1 turns on, it effectively shorts out R_0 and causes 0V to be applied to the error amplifier. The output voltage in the off state will be approximately ±20 mV. If a higher value (50 to 100 mV) is acceptable, then the DG201 analog switch can be replaced with a low-cost small signal transistor, as shown in the alternate switch configuration.

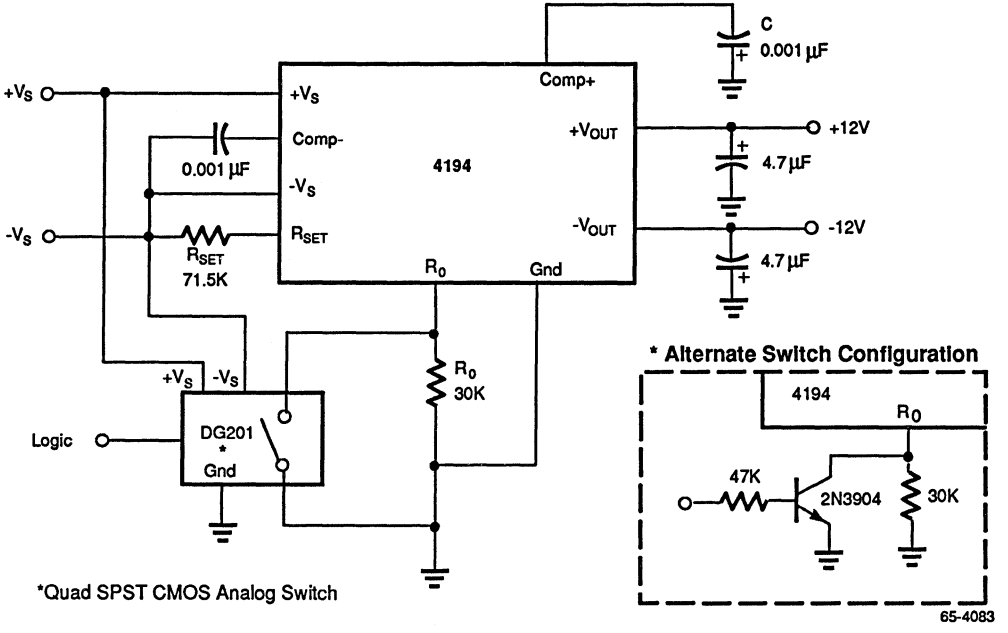


Figure 1. ±12V Switchable Power Supply

Compensation

For most applications, the following compensation technique is sufficient. The positive regulator section of the 4194 is compensated by a 0.001 µF ceramic disc capacitor from the Comp+ terminal to ground. The negative regulator requires compensation at two points. The first is the Comp- pin, which should have 0.001 µF to the $-V_s$ pin, or case. A ceramic disc is ideal here. The second compensation point for the negative side is the $-V_{OUT}$ terminal, which ideally should be a 4.7 µF solid tantalum capacitor with enough reserve voltage capacity to avoid the momentary shorting and reforming which can occur with tantalum caps. For systems where the cost of a solid tantalum capacitor cannot be justified, it is usually sufficient to use an aluminum capacitor with a 0.03 µF ceramic disc in parallel to bypass high frequencies. In addition, if the rectifier filter capacitors have poor high frequency characteristics (like aluminum electrolytics) or if any impedance is in series with the $+V_s$ and $-V_s$ terminals, it is necessary to bypass these two points with 0.01 µF ceramic disc capacitors. Just as with monolithic op amps, some applications may not require these bypass caps, but if in doubt, be sure to include them.

All compensation and bypass caps should have short leads, solid grounds, and be located as close to the 4194 as possible. Refer to Figure 2 for recommended compensation circuitry.

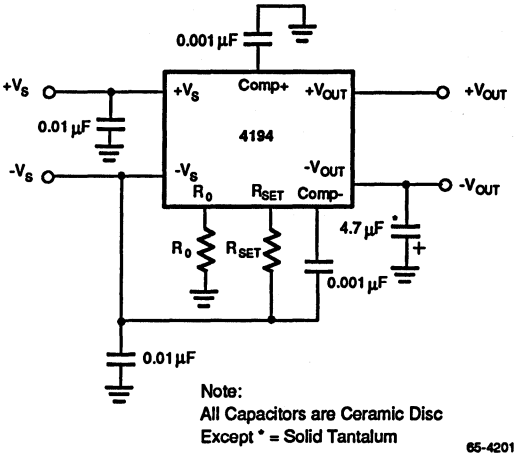


Figure 2. 4194 Recommended Compensation

Protection

In systems using monolithic voltage regulators, a number of conditions can exist which, left uncorrected, will destroy the regulator. Fortunately, regulators can easily be protected against these potentially destructive conditions. Monolithic regulators can be destroyed by any reversal of input or output voltage polarity, or if the input voltage drops below the output voltage in magnitude. These conditions can be caused by inductive loads at the inputs or outputs of the regulator. Other problems are caused by heavy loads at the unregulated inputs to the regulator, which might cause the input voltage to drop below the output voltage at turn-off. If any of the preceding problem conditions are present in your system, it is recommended that you protect the regulator using diodes. These diodes should be high speed types capable of handling large current surges. Figure 3 shows all six of the possible protection diodes. The diodes at the inputs and outputs prevent voltages at those points from becoming reversed. Diodes from outputs to inputs prevent the output voltage from exceeding the input voltage. Chances are that the system under consideration will not require all six diodes, but if in doubt, be sure to include them.

Brownout Protection

The 4194 is one of the most easily applied and trouble-free monolithic ICs available. When used within the data sheet ratings (package power dissipation, maximum output current, minimum and maximum input voltages) it provides the most cost-effective source of regulated ±15V for powering linear ICs.

Sometimes occasions arise in which the 4194 ratings must be exceeded. One example is the "brownout". During a brownout, line voltages may be reduced to as low as 75 V_{RMS}, causing the input voltage to the 4194 to drop below the minimum dropout voltage. When this happens, the negative output voltage can go to positive. The maximum amount of current available is approximately 5 mA.

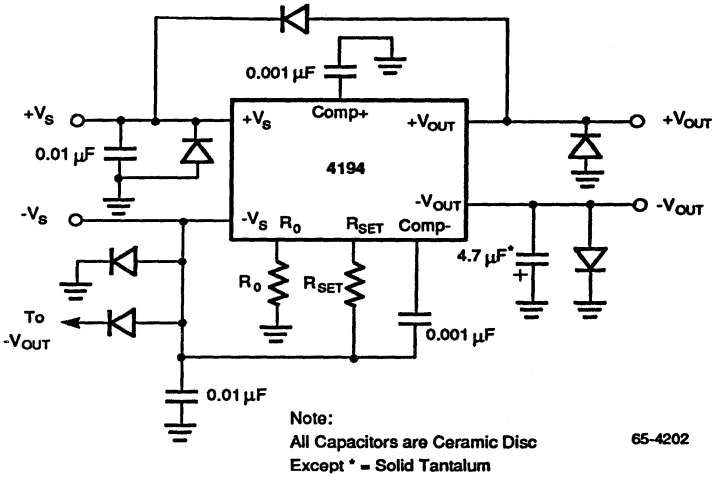


Figure 3. 4194 Regulator Showing All Protective Diodes

In general this is not enough current to damage most ICs which the 4194 might be supplying, but it is a potentially destructive condition. Fortunately, it is easy to protect against. As shown in the typical application circuit in Figure 4, a diode, D, can be connected to the negative output.

If a small signal silicon diode is used, it will clamp the negative output voltage at about +0.55V. A Schottky barrier or germanium device would clamp the voltage at about +0.3V. Another cure which will keep the negative output negative at all times is the 1 mΩ resistor connected between the +15V output and the Comp- terminal. This resistor will then supply drive to the negative output transistor, causing it to saturate to -1V during the brownout.

Heatsinking

Voltage Regulators are power devices which are used in a wide range of applications.

When operating these devices near their extremes of load current, ambient temperature and input-output differential, consideration of package dissipation becomes important to avoid thermal shutdown at 175°C. The 4194 has this feature to prevent damage to the device. It typically starts affecting load regulation approximately 2°C below 175°C. To avoid shutdown, some form of heatsinking should be used or one of the above operating conditions would need to be derated.*

Balanced Output (V_{OUT} = ±15V)

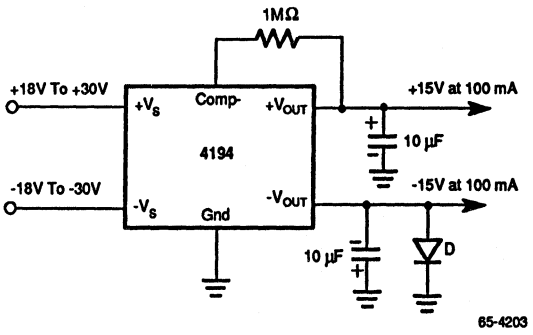


Figure 4. 4194 Typical Application Circuit

*In allowing for process deviations, the user should work with a maximum allowable function temperature of 150°C.

The following is the basic equation for junction temperature:

$$T_J = T_A + P_D \theta_{J-A} \quad (1)$$

where
T_J = junction temperature (°C)
T_A = ambient air temperature (°C)
P_D = power dissipated by device (W)
θ_{J-A} = thermal resistance from junction to ambient air (°C/W)

The power dissipated by the voltage regulator can be detailed as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q \quad (2)$$

where
V_{IN} = input voltage
V_{OUT} = regulated output voltage
I_O = load current
I_Q = quiescent current drain

Let's look at an application where a user is trying to determine whether the 4194 in a high temperature environment will need a heatsink.

Given:

T_J at thermal shutdown = 150°C

T_A = 125°C

θ_{J-A} = 41.6°C/W, K (TO-66) pkg.

V_{IN} = 40V

V_{OUT} = 30V

I_Q = 1 mA + 75 µA/V_{OUT} x 30V
= 3.25 mA *

$$\theta_{J-A} = \frac{T_J - T_A}{P_D}$$

$$P_D = \frac{T_J - T_A}{\theta_{J-A}} = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Solve for I_O,

$$I_O = \frac{T_J - T_A}{\theta_{J-A}(V_{IN} - V_{OUT})} - \frac{V_{IN} \times I_Q}{(V_{IN} - V_{OUT})}$$

$$I_O = \frac{150°C - 125°C}{41.6°C/W \times 10V} - \frac{40 \times 3.25 \times 10^{-3}}{10}$$

= 60 mA - 13 mA ~ 47 mA

If this supply current does not provide at least a 10% margin under worst case load conditions, heatsinking should be employed. If reliability is of prime importance, the multiple regulator approach should be considered.

In equation 1, θ_{J-A} can be broken into the following components:

$$\theta_{J-A} = \theta_{J-C} + \theta_{C-S} + \theta_{S-A}$$

where
θ_{J-C} = junction-to-case thermal resistance
θ_{C-S} = case-to-heatsink thermal resistance
θ_{S-A} = heatsink-to-ambient thermal resistance

In the above example, let's say that the user's load current is 200 mA and he wants to calculate the combined θ_{C-S} and θ_{S-A} he needs:

Given: I_O = 200 mA,

$$\theta_{J-A} = \frac{T_J - T_A}{(V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q}$$

$$= \frac{50°C - 125°C}{10V \times 200\ mA + 40 \times 3.25 \times 10\text{-}3}$$

= 11.75°C/W

* The current drain will increase by 50µA/V_{OUT} on positive side and 100µA/V_{OUT} on negative side.

Given θ_{J-C} = 7.15°C/W for the 4194 in the K package,

$$\theta_{C-S} + \theta_{S-A} = 11.75°C/W - 7.15°C/W$$

$$= 4.6°C/W$$

When using heatsink compound with a metal-to-metal interface, a typical θ_{C-S} = 0.5°C/W for the K package. The remaining θ_{S-A} of approximately 4°C/W is a large enough thermal resistance to be easily provided by a number of heatsinks currently available. Table 1 is a brief selection guide to heatsink manufacturers.

Table 1. Commercial Heatsink Selection Guide

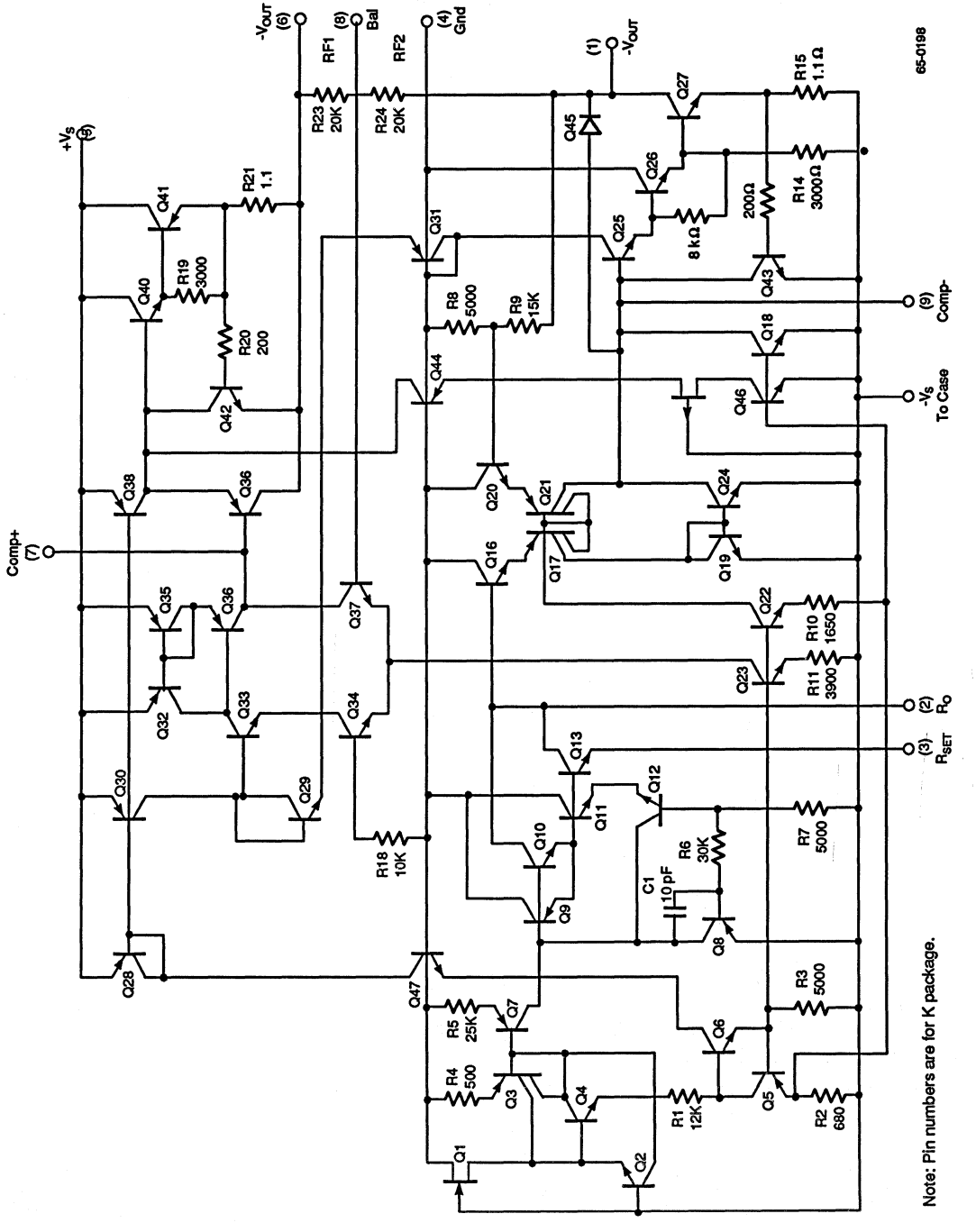
No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

θ_{S-A}*(°C/W)	Manufacturer/Series or Part Number
	TO-66 Package
0.31-1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0 - 3.0	Wakefield — 641 Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0 - 5.0	Wakefield — 621, 623 Thermalloy — 6606, 6129, 6141, 6303 IERC — HP Staver — V3-3-2
5.0 - 7.0	Wakefield — 690 Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC — LB Staver— V3-5-2
7.0 - 10.0	Wakefield — 672 Thermalloy — 6001, 6016, 6051, 6105, 6601 IERC — LA, uP Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10.0-25.0	Thermalloy — 6-13, 6014, 6015, 6103, 6104, 6105, 6117
	Dual In-line Package
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LI
60	Wakefield — 650, 651

Staver Co., Inc.: 41-51 N Saxon Ave., Bay Shore, NY 11706
IERC: 135 W Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W Valley View Ln., Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

* All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

Schematic Diagram



RC4195
Fixed ±15V Dual Tracking Voltage Regulator

Description

The RM/RC4195 is a dual polarity tracking regulator designed to provide balanced positive and negative 15V output voltages at currents up to 100mA. This device is designed for local "on-card" regulation, eliminating distribution problems associated with single point regulation. The regulator is intended for ease of application. Only two external components are required for operation (two 10 µF bypass capacitors).

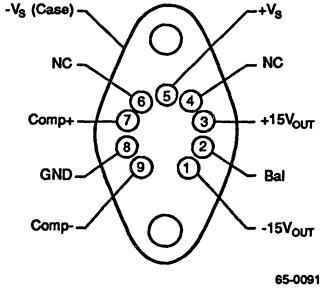
The device is available in four package types to accommodate various applications requiring economy, high power, dissipation, and reduced component density.

Features

- ±15V operational amplifier power at reduced cost and component density
- thermal shutdown at Tj = +175°C in addition to short circuit protection
- Output currents to 100 mA
- May be used as single output regulator with up to +50V output
- Available in TO-66, TO-99 and 8-lead mini-DIP

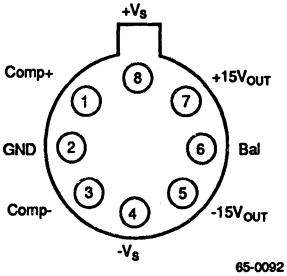
Connection Information

TO-66 Metal Can
(Top View)



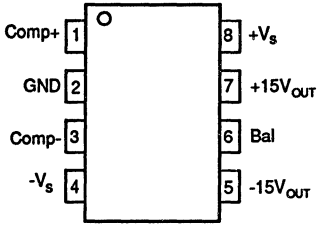
65-0091

TO-99 Metal Can
(Top View)



65-0092

8-Lead DIP
(Top View)



65-0093

Linear

Ordering Information

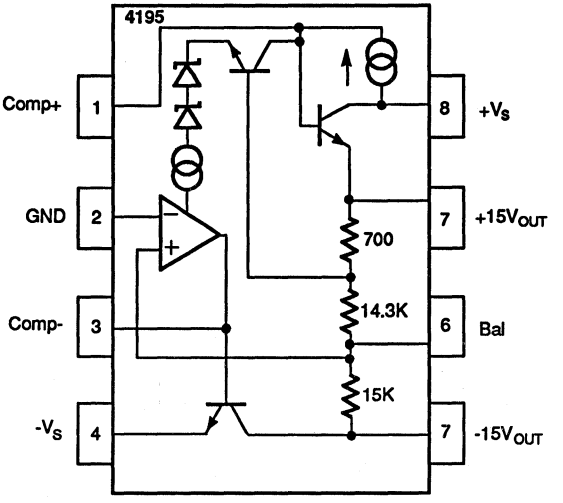
Part Number	Package	Operating Temperature Range
RC4195N	N	0°C to +70°C
RC4195T	T	0°C to +70°C
RC4195K	K	0°C to +70°C
RM4195T	T	-55°C to +125°C
RM4195T/883B	T	-55°C to +125°C
RM4195K	K	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
T = 8-lead metal can TO-99
K = 9-lead metal can TO-66

Absolute Maximum Ratings

Supply Voltage($\pm V_S$) to Ground .....±30V
Load Current
K Package .....150 mA
T and N Package .....100 mA
Storage Temperature
Range .....-65°C to +150°C
Operating Temperature Range
RC4195 .....0°C to +70°C
RM4195 .....55°C to +125°C
Lead Soldering Temperature
(60 sec) .....+300°C

Functional Block Diagram



Pinout for dual-in-line package shown. 65-0089

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead T0-99 Metal Can	9-Lead T0-66 Metal Can
Max. Junction Temp.	+125°C	+175°C	+150°C
Max. P_D T_A<50°C	468mW	658mW	2381mW
Therm. Res θ_{JC}	—	50°C/W	7°C/W
Therm. Res. θ_{JA}	160°C/W	190°C/W	42°C/W
For T_A >50°C Derate at	6.25 mW/°C	5.26 mW/°C	23.81 mW/°C

Electrical Characteristics

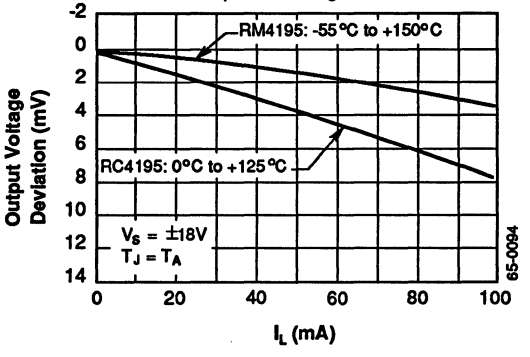
(I_L = ±1mA; V_S = ±20V, C_L = 10µF; RM4195: -55°C ≤ T_A ≤ +125°C; RC4195: 0°C ≤ T_A ≤ +70°C unless otherwise specified)[1]

Parameters	Test Conditions	RC/RM4195 Min	RC/RM4195 Typ	RC/RM4195 Max	Units
Line Regulation	V_S = ±18V to ±30V		2	20	mV
Load Regulation	I_L = 1mA to 100mA		5	30	mV
Output Voltage Drift With Temperature			0.005	0.015	%/°C
Supply Current	V_S = ±30V, I_L = 0 mA		±1.5	±4.0	mA
Supply Voltage		±18		±30	V
Output Voltage	T_A = +25°C	14.5	15.0	15.5	V
Output Voltage Tracking			±50	±300	mV
Ripple Rejection	F = 120 Hz, T_A = +25°C		75		dB
Input-Output Voltage Differential	I_L = 50 mA	3.0			V
Short Circuit Current	T_A = +25°C		220		mA
Output Noise Voltage	T_A = +25°C, F = 100Hz to 120kHz	60			μV_{RMS}
Internal Thermal Shutdown			175		°C

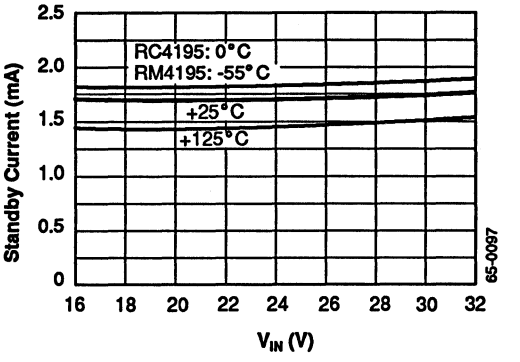
[1]The specifications above apply for the given junction temperatures since pulse test conditions are used.

Typical Performance Characteristics

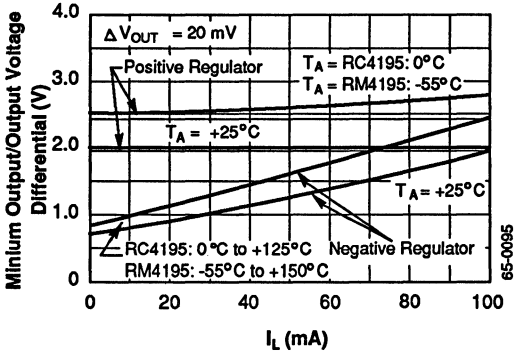
Output Load Regulation



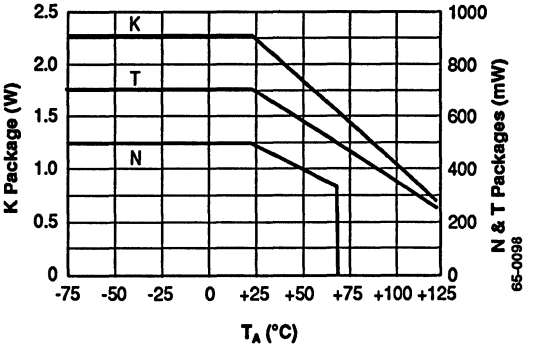
Standby Current Drain



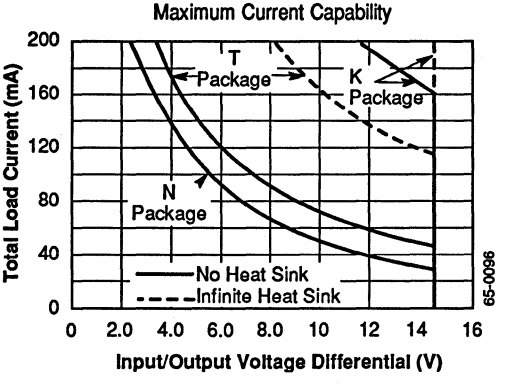
Regulator Dropout Voltage



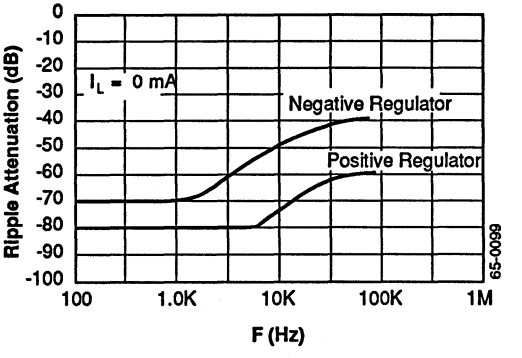
Power Dissipation



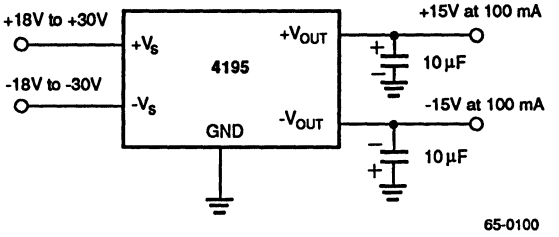
Maximum Current Capability



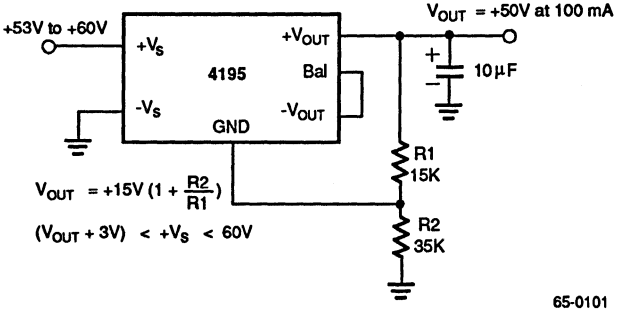
Ripple Rejection



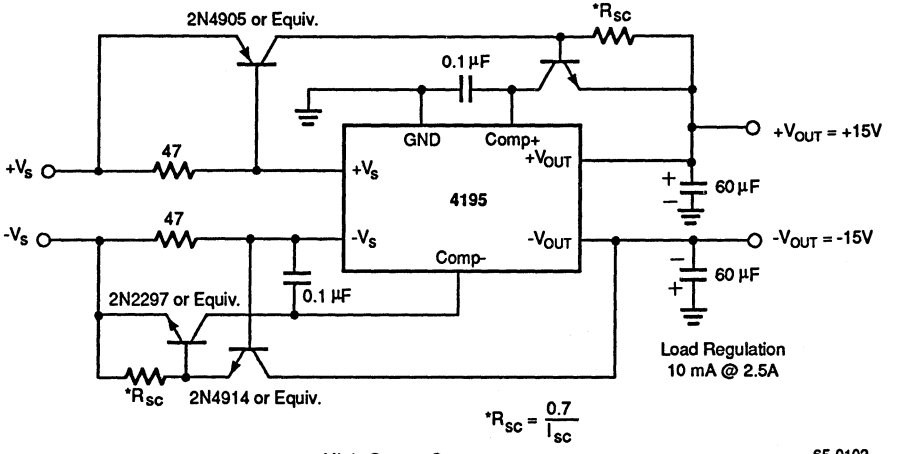
Typical Applications



Balanced Output ($V_{OUT} = \pm 15V$)



Positive Single Supply ($+15V < V_{OUT} < +50V$)



High Output Current

Brownout Protection

The 4195 is one of the most easily applied and trouble-free monolithic ICs available. When used within the data sheet ratings (package power dissipation, maximum output current, minimum and maximum input voltages) it provides the most cost-effective source of regulated ±15V for powering linear ICs.

Sometimes occasions arise in which the 4195 ratings must be exceeded. One example is the "brownout". During a brownout, line voltages may be reduced to as low as 75 V_{RMS}, causing the input voltage to the 4195 to drop below the minimum dropout voltage. When this happens, the negative output voltage can go to positive. The maximum amount of current available is approximately 5 mA.

In general this is not enough current to damage most ICs which the 4195 might be supplying, but it is a potentially destructive condition. foretunately, it is easy to protect against. As shown in the typical application circuit, a diode, D, can be connected to the negative output.

If a small signal silicon diode is used, it will clamp the negative output voltage at about +0.55V. A Schottky barrier or germanium device would clamp the voltage at about +0.3V. Another cure which will keep the negative output negative all times is the 1 mΩ resistor connected between the +15V output and the comp - terminal. this resistor will then supply drive to the negative output transistor, causing it to saturate to -1V during the brownout.

Heatsinking

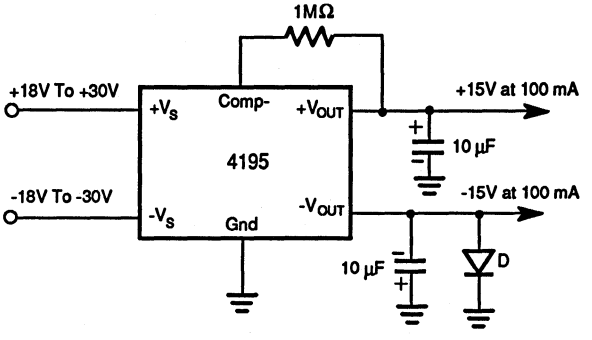
When operating these devices near their extremes of load current, ambient temperature and input-output differential, consideration of package dissipation becomes important to avoid thermal shutdown at 175°C. The 4195 has this feature to prevent damage to the device. It typically starts affecting load regulation approximately 2°C below 175°C. To avoid shutdown, some form of heatsinking should be used or one of the above operating conditions would need to be derated.*

The following is the basic equation for junction temperature:

$$T_J = T_A + P_D \theta_{J\text{-}A} \qquad (1)$$

where
T_J = junction temperature (°C)
T_A = ambient air temperature (°C)
P_D = power dissipated by device (W)
$\theta_{J\text{-}A}$ = thermal resistance from junction to ambient air (°C/W)

Balanced Output (V_{OUT} = ±15V)



Typical Application Circuit

* In allowing for process deviations, the user should work with a maximum allowable function temperature of 150°C

The power dissipated by the voltage regulator can be detailed as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q \qquad (2)$$

where
V_{IN} = input voltage
V_{OUT} = regulated output voltage
I_O = load current
I_Q = quiescent current drain

Let's look at an application where a user is trying to determine whether the 4195 in a high temperature environment will need a heatsink.

Given:

T_J at thermal shutdown = 150°C
T_A = 125°C
θ_{J-A} = 41.6°C/W, K (TO-66) pkg.
V_{IN} = 40V
V_{OUT} = 30V
I_Q = 1 mA + 75 µA/V_{OUT} x 30V
= 3.25 mA *

$$\theta_{J-A} = \frac{T_J - T_A}{P_D}$$

$$P_D = \frac{T_J - T_A}{\theta_{J-A}} = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Solve for I_O,

$$I_O = \frac{T_J - T_A}{\theta_{J-A}(V_{IN} - V_{OUT})} - \frac{V_{IN} \times I_Q}{(V_{IN} - V_{OUT})}$$

$$I_O = \frac{150°C - 125°C}{41.6°C/W \times 10V} - \frac{40 \times 3.25 \times 10^{-3}}{10}$$

= 50 mA - 13 mA ~ 47 mA

If this supply current does not provide at least a 10% margin under worst case load conditions, heatsinking should be employed. If reliability is of prime importance, the multiple regulator approach should be considered.

In equation 1, θ_{J-A} can be broken into the following components:

$$\theta_{J-A} = \theta_{J-C} + \theta_{C-S} + \theta_{S-A}$$

where
θ_{J-C} = junction-to-case thermal resistance
θ_{C-S} = case-to-heatsink thermal resistance
θ_{S-A} = heatsink-to-ambient thermal resistance

In the above example, let's say that the user's load current is 200 mA and he wants to calculate the combined θ_{C-S} and θ_{S-A} he needs:

Given: I_O = 200 mA,

$$\theta_{J-A} = \frac{T_J - T_A}{(V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q}$$

$$= \frac{50°C - 125°C}{10V \times 200\ mA + 40 \times 3.25 \times 10\text{-}3}$$

= 11.75°C/W

Given θ_{J-C} = 7.15°C/W for the 4195 in the K package,

$$\theta_{C-S} + \theta_{S-A} = 11.75°C/W - 7.15°C/W$$

$$= 4.6°C/W$$

When using heatsink compound with a metal-to metal interface, a typical θ_{C-S} = 0.5°C/W for the K package. The remaining θ_{S-A} of approximately 4°C/W is a large enough thermal resistance to be easily provided by a number of heatsinks currently available. Table 1 is a brief selection guide to heatsink manufacturers.

* The current drain will increase by 50µA/V_{OUT} on positive side and 100µA/V_{OUT} on negative side.

Linear

Table 1. Commercial Heatsink Selection Guide

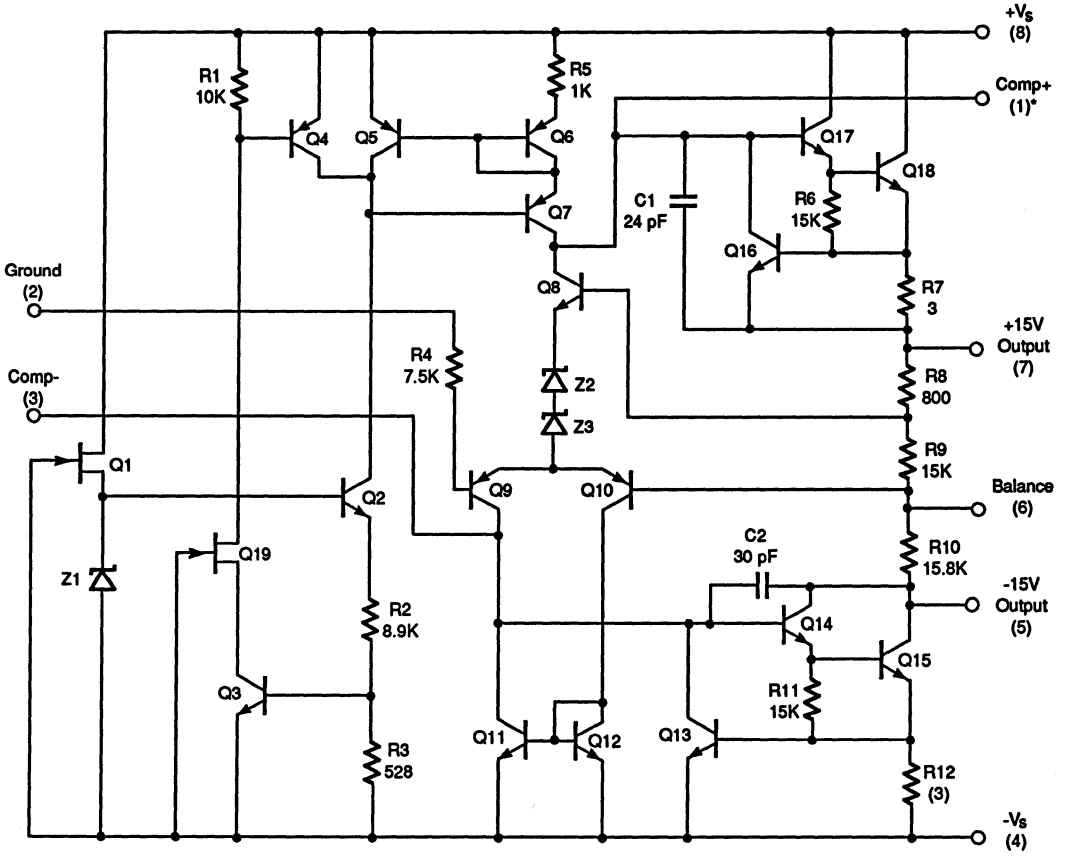
No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

θ_{S-A}*(°C/W)	Manufacturer/Series or Part Number
	TO-66 Package
0.31-1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0 - 3.0	Wakefield — 641 Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0 - 5.0	Wakefield — 621, 623 Thermalloy — 6606, 6129, 6141, 6303 IERC — HP Staver — V3-3-2
5.0 - 7.0	Wakefield — 690 Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC — LB Staver— V3-5-2
7.0 - 10.0	Wakefield — 672 Thermalloy — 6001, 6016, 6051, 6105, 6601 IERC — LA, uP Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10.0-25.0	Thermalloy — 6-13, 6014, 6015, 6103, 6104, 6105, 6117
	TO-99 Package
12.0 - 20.0	Wakefield — 260 Thermalloy — 1101, 1103 Staver — V3A-5
20.0 - 30.0	Wakefield — 209 Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005 IERC — LP Staver — F5-5
3.0 - 50.0	Wakefield — 207 Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264
	Dual In-line Package
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LI
60	Wakefield — 650, 651

* All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

Staver Co., Inc.: 41-51 N Saxon Ave., Bay Shore, NY 11706
IERC: 135 W Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W Valley View Ln., Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

Schematic Diagram



*Pin numbers are for 8-pin packages.

65-0090

Linear

RC4391
Inverting and Step-Down Switching Regulator

Description

Raytheon's RC4391 is a monolithic switch mode power supply controller for micropower circuits. The 4391 integrates all the active functions needed for low power switching supplies, including oscillator, switch, reference and logic, into a small package. Also, the quiescent supply current drawn by the 4391 is extremely low; this combination of low supply current, function, and small package make it adaptable to a variety of miniature power supply applications.

The 4391 complements another Raytheon switching regulator IC, the RC4190. The 4190 is dedicated to step-up ($V_{OUT} > V_{IN}$) applications, while the 4391 was designed for inverting ($V_{OUT} = -V_{IN}$) and step-down ($V_{OUT} < V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the 4190 data sheet for information on step-up applications.

The functions provided are:

- Squarewave oscillator (adjustable externally)
- Bandgap voltage reference
- High current PNP switch transistor
- Feedback comparator
- Logic for gating the comparator
- Circuitry for detecting a discharged battery condition (in battery powered systems)

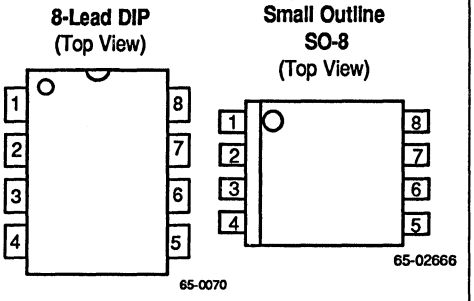
Few external components are required to build a complete DC-to-DC converter:

- Inductor
- Low value capacitor to set the oscillator frequency
- Electrolytic filter capacitor
- Steering diode
- Two resistors

Features

- Versatile —
  Inverting function (+ to -)
  Step-down function
  Adjustable output voltage
  Regulates supply changes
- Micropower —
  Low quiescent current — 170 µA
  Wide supply range — 4V to 30V
- High performance —
  High switch current —375 mA
  High efficiency — 70% typically
- Low battery detection capability
- 8-lead mini-DIP or S.O. package

Connection Information



Pin	Function
1	Low Battery Resistor (LBR)
2	Low Battery Detector (LBD)
3	Timing Capacitor (C_X)
4	Ground
5	External Inductor (L_X)
6	+Supply Voltage ($+V_S$)
7	+1.25V Reference Voltage (V_{REF})
8	Feedback Voltage (V_{FB})

Ordering Information

Part Number	Package	Operating Temperature Range
RC4391N	N	0°C to +70°C
RC4391M	M	0°C to +70°C
RV4391N	N	-25° C to +85°C
RM4391D	D	-55°C to +125°C

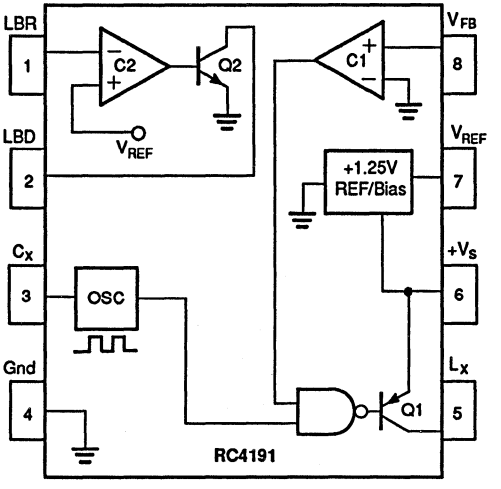
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
M = 8-lead plastic SOIC

Absolute Maximum Ratings

Internal Power Dissipation ..... 500 mW
Supply Voltage[1]
(Pin 6 to Pin 4 or
Pin 6 to Pin 5) ..... +30V
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4391 ..... -55°C to +125°C
RV4391 ..... -25°C to +85°C
RC4391 ..... 0°C to +70°C
Switch Current (I_{MAX}) ..... 375 mA peak

Note:
1. The maximum allowable supply voltage ($+V_S$) in inverting applications will be reduced by the value of the negative output voltage, unless an external power transistor is used in place of Q1.

Functional Block Diagram



Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	Small Outline SO-8
Max. Junction Temp.	+125°C	+175°C	125°C
Max. P_D T_A<50°C	468 mW	833 mW	300 mW
Therm. Res θ_{JC}	—	45°C/W	—
Therm. Res. θ_{JA}	160°C/W	150°C/W	240°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	4.17 mW/°C

Electrical Characteristics

(V_S = +6.0V, over the full operating temperature range unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	$+V_S$	(Note 1)	4.0		30	V
Supply Current	I_{SY}	V_S = +25V		300	500	µA
Reference Voltage	V_{REF}		1.13	1.25	1.36	V
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V	-5.5	-5.0	-4.5	V
		$V_{OUT\ nom}$ = -15V	-16.5	-15.0	-13.5	
Line Regulation	LI_1	$V_{OUT\ nom}$ = -5.0V, C_X = 150pF, V_S = +5.8V to +15V		2.0	4.0	$\%V_{OUT}$
		$V_{OUT\ nom}$ = -15V, C_X = 150pF, V_S = +5.8V to +15		1.5	3.0	
Load Regulation	LO_1	$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.5	$\%V_{OUT}$
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.3	
Switch Leakage Current	I_{CO}	Pin 5 = -20V		0.1	30	µA

Note 1. The maximum allowable supply voltage (+VS) in inverting applications will be reduced by the value of the negative output voltage, unless an external power transistor is used.

Linear

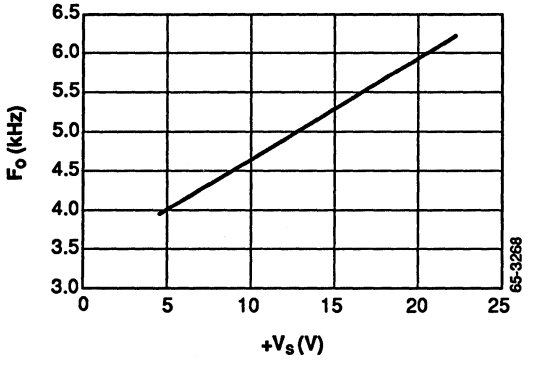
Electrical Characteristics

(V_S = +6.0V, T_A = +25°C unless otherwise noted)

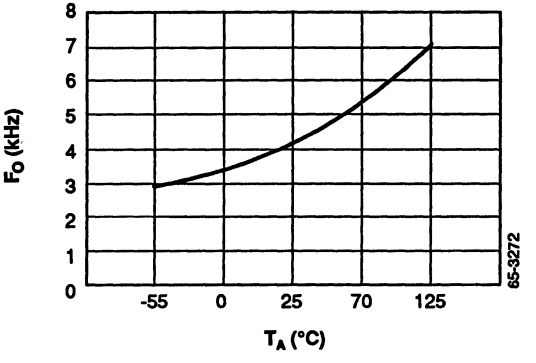
Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	I_{SY}	V_S = +4.0V, No External Loads		170	250	µA
		V_S = +25V No External Loads		300	500	
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V	-5.35	-5.0	-4.65	V
		$V_{OUT\ nom}$ = -15V	-15.85	-15.0	-14.15	
Line Regulation	LI_1	$V_{OUT\ nom}$ = -5.0V, CX = 150pF, V_S = +5.8V to +15V		1.5	3.0	$\%V_{OUT}$
		$V_{OUT\ nom}$ = -15V, C_X = 150pF V_S = +5.8V to +15V		1.0	2.0	
Load Regulation	LO_1	$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.4	$\%V_{OUT}$
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, VS = +4.5V, P_{LOAD} = 0mW to 75mW		0.07	0.14	
Reference Voltage	V_{REF}		1.18	1.25	1.32	V
Switch Current	I_{SW}	Pin 5 = 5.5V	75	100		mA
Switch Leakage Current	I_{CO}	Pin 5 = -24V		0.01	5.0	µA
Cap. Charging Current	I_{CX}	Pin 3 = 0V	6.0	10	14	µA
LBD Leakage Current	I_{LBDL}	Pin 1 = 1.5V, Pin 2 = 6.0V		0.01	5.0	µA
LBD On Current	I_{LBDO}	Pin 1 = 1.1V, Pin 2 = 0.4V	210	600		µA
LBR Bias Current	I_{LBRB}	Pin 1 = 1.5V		0.7		µA

Typical Performance Characteristics

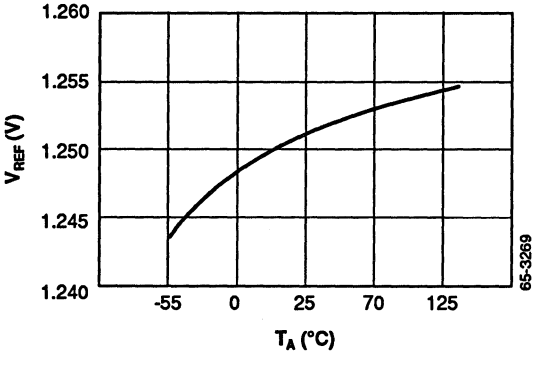
Oscillator Frequency vs. Supply Voltage



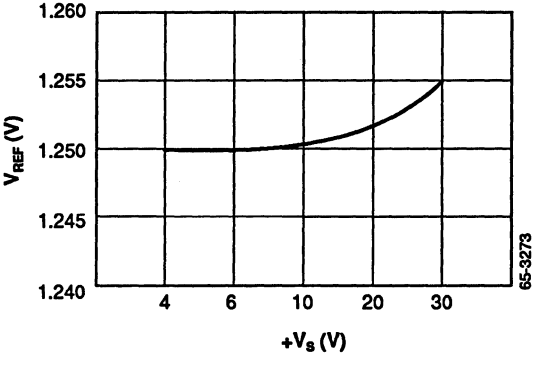
Oscillator Frequency vs. Temperature



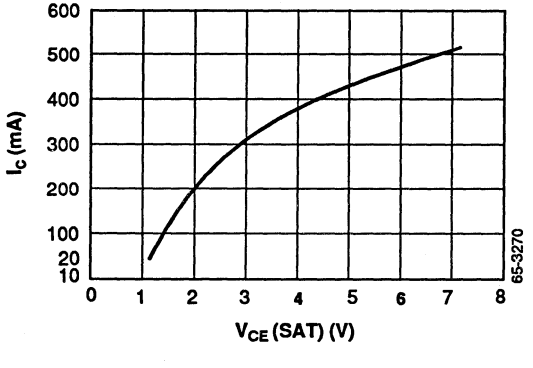
Reference Voltage vs. Temperature



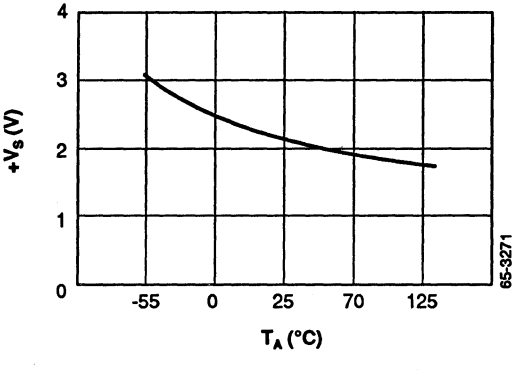
Reference Voltage vs. Supply Voltage



Collector Current vs. Q1 Saturation Voltage



Minimum Supply Voltage vs. Temperature



Linear

Principles of Operation

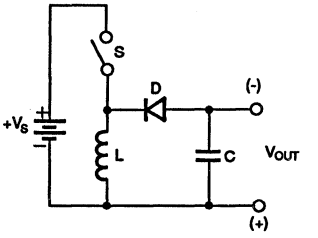
The basic switching inverter circuit is the building block on which the complete inverting application is based.

A simplified diagram of the voltage inverter circuit with ideal components and no feedback circuitry is shown in Figure 1. When the switch S is closed, charging current from the battery flows through the inductor L, which builds up a magnetic field, increasing as the switch is held closed. When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a current which flows through the inductor in the same direction as the changing current. Because there is no path for this current to flow through the switch, the current must flow through the diode to charge the capacitor C. The key to the inversion is the ability of the inductor to become a source when the charging current is removed.

The equation V = L (di/dt) gives the maximum possible voltage across the inductor; in the actual application, feedback circuitry and the output capacitor will decrease the output voltage to a regulated fixed value.

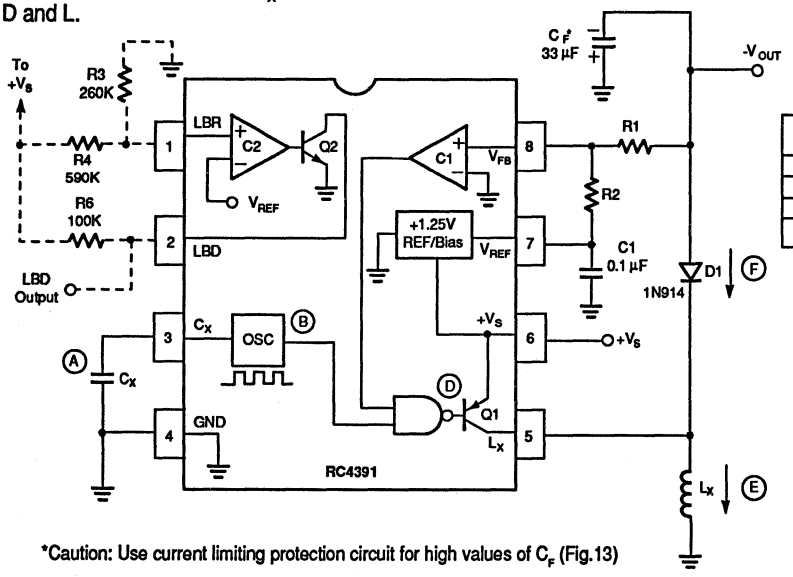
A complete schematic for the standard inverting application is shown in Figure 2. The ideal switch in the simplified diagram is replaced by the PNP transistor switch between pins 5 and 6. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the ground sensing comparator (pin 8) compares the output voltage to the +1.25V voltage reference. Because C_F is initially discharged a positive voltage is applied to the comparator, and the output of the comparator gates the squarewave oscillator. This gated squarewave signal turns on, then off, the PNP output transistor. This turning on and off of the output transistor performs the same function as opening and closing the ideal switch in the simplified diagram; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.



65-1601

Figure 1. Simple Inverting Regulator



Parts List	-5.0V Output	-15V Output
R1 =	300 kΩ	900 kΩ
R2 =	75 kΩ	75 kΩ
Cx =	150 pF	150 pF
Lx =	1.0 mH Dale TE3 Q4 TA	

- - - - - - - = Optional

$-V_{OUT} = (1.25V)\left(\frac{R1}{R2}\right)$

65-1602

*Caution: Use current limiting protection circuit for high values of C_F (Fig.13)

Figure 2. Inverting Regulator — Standard Circuit

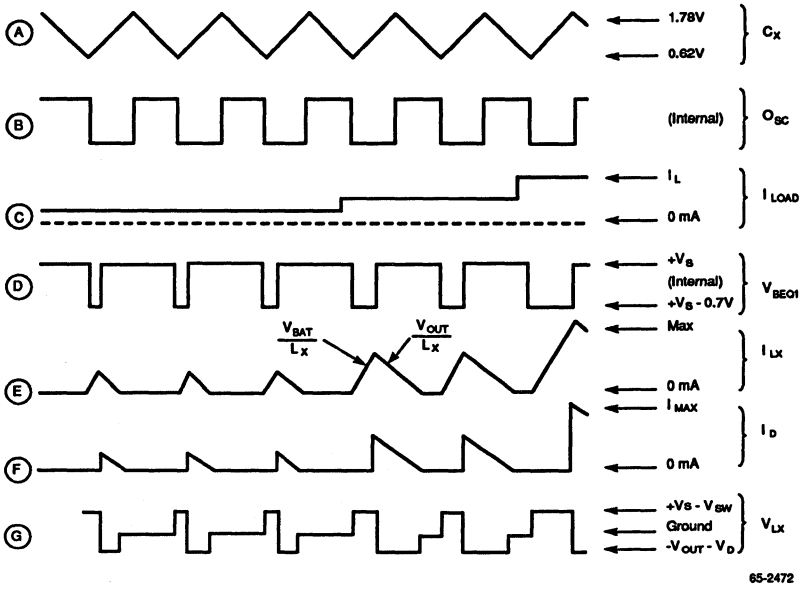


Figure 3. Inverting Regulator Waveforms

The comparator will continue to allow the oscillator to turn the switch transistor on and off until enough energy has been stored in the output capacitor to make the comparator input voltage decrease to less than 0V. The voltage applied to the comparator is set by the output voltage, the reference voltage, and the ratio of R1 to R2.

This feedback system will vary the duration of the on time in response to changes in load current or battery voltage (see Figure 3). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle, (waveform B) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.

Step-Down Regulator

The step-down circuit function is similar to inversion; it uses the same components (switch, inductor, diode, filter capacitor), and charges and discharges the inductor by closing and opening the switch. The great difference is that the inductor is in series with the load; therefore, both the charging current and the discharge current flow into the load. In the inverting circuit only the discharge current flows into the load. Refer to Figure 4.

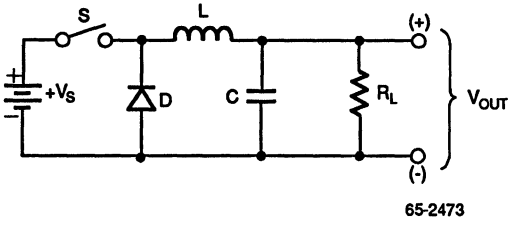


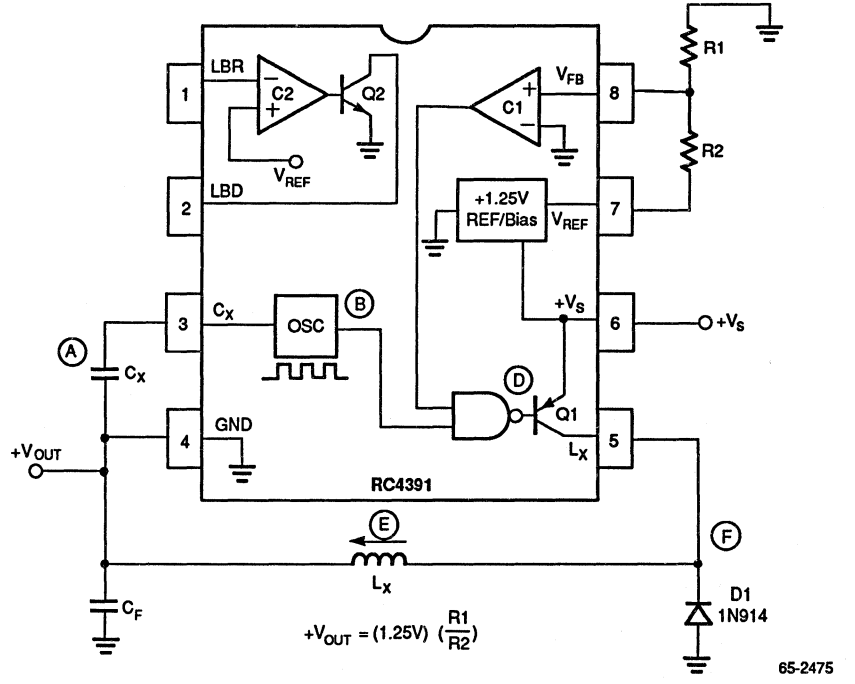
Figure 4. Simple Step-Down Regulator

When the switch S is closed, current flows from the battery, through the inductor, and through the load resistor to ground. After the switch is opened, stored energy in the inductor causes current to keep flowing through the load, the circuit being completed by the catch diode D. Since current flows to the load during charge and discharge, the average load current will be greater than in an inverting circuit. The significance of that is that for equal load currents the step-down circuit will require less peak inductor current than an inverting circuit. Therefore, the inductor will not require as large of a core, and the switch transistor will not be stressed as heavily for equal load currents.

Figure 5 depicts a complete schematic for a step-down circuit using the 4391. Observe that the ground lead of the 4391 is **not** connected to circuit ground; instead, it is tied to the output voltage. It is by this rearrangement that the feedback system, which senses voltages more negative than the ground lead, can be used to regulate a non-negative output voltage.

When power is first applied, the output filter capacitor is discharged so the ground lead potential starts at 0V. The reference voltage is forced to +1.25V above the ground lead and pulls the feedback input (pin 8) more positive than the ground lead. This positive voltage forces the control network to begin pulsing the switch transistor. As the switching action pumps up the output voltage, the ground lead rises with the output until the voltage on the ground lead is equal to the feedback voltage. At that point, the control network reduces the time on time of the switch to maintain a constant output.

This control network will vary the on time of the switch in response to changes in load current or battery voltage (see Figure 6). If the load current increases (waveform C), then the transistor will remain on (waveformD) for a longer portion of the oscillator cycle, (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.



Important Note: This circuit must have a minimum load ≥ 1 mA always connected.

Figure 5. Step-Down Regulator — Standard Circuit

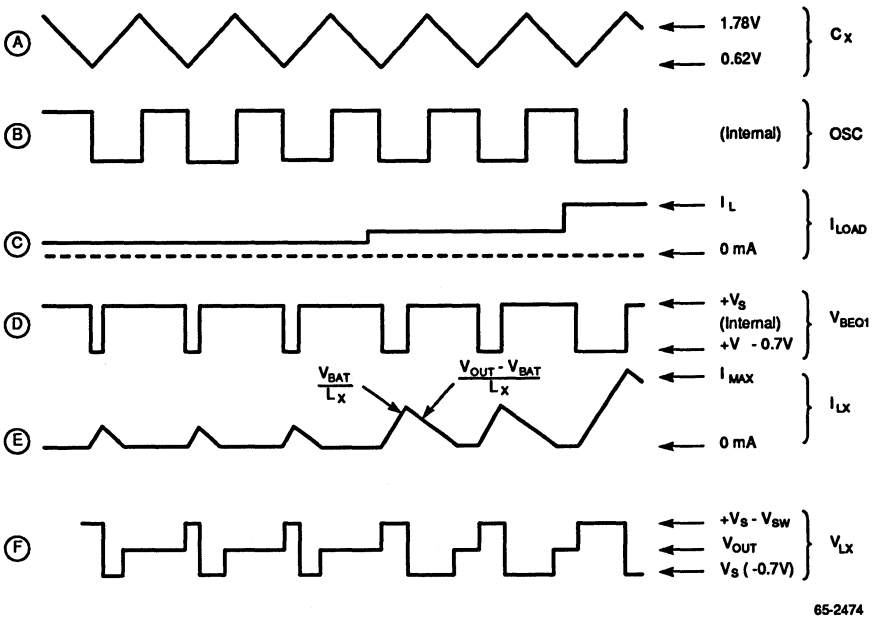


Figure 6. Step-Down Regulator Waveforms

Design Equations

The inductor value and timing capacitor (C_X) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (I_{MAX}) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±30% as a maximum variation of oscillator frequency.

The oscillator creates a squarewave using a method similar to the 555 timer IC, with a current steering flip-flop controlled by two voltage sensing comparators. The oscillator frequency is set by the timing capacitor (C_X) according to the following equation.

$$F_O\,(Hz) = \frac{4.1 \times 10^{-6}}{C_X\,(pF)}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 3. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Inverting Design Procedure

1. Select an operating frequency and timing capacitor value as shown above (frequencies from 10kHz to 50kHz are typical).
2. Find the maximum on time T_{ON} (add 3µS for the turn off base recombination delay of Q1):

$$T_{ON} = \frac{1}{2\,F_O} + 3\mu S$$

Linear

3. Calculate the peak inductor current I_{MAX} (if this value is greater than 375mA then an external power transistor must be used in place of Q1):

$$I_{MAX} = \frac{(V_{OUT} + V_D)\, 2I_L}{(F_O)\,(T_{ON})\,(V_S - V_{SW})}$$

Where:

V_S	=	Supply Voltage
V_{SW}	=	Saturation Voltage of Q1 (typically 0.5V)
V_D	=	Diode Forward Voltage (typically 0.7V)
I_L	=	DC Load Current

4. Find an inductance value for L_X:

$$L_X(\text{Henries}) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right)(T_{ON})$$

The inductor chosen must exhibit this value of inductance and have a current rating equal to I_{MAX}.

Step-Down Design Procedure

1. Select an operating frequency.
2. Determine the maximum on time T_{ON} as in the inverting design procedure.
3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(F_o)\,(T_{ON})\left[\frac{(V_S - V_{OUT})}{(V_{OUT} - V_D)} + 1\right]}$$

4. Calculate L_X:

$$L_X(\text{Henries}) = \left(\frac{V_S - V_{OUT}}{I_{MAX}}\right)(T_{ON})$$

Alternate Design Procedure

The design equations above will not work for certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, use the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example the inductor current will be continuous and the alternate procedure will be necessary. The alternate procedure may also be used for discontinuous circuits.

1. Select an operating frequency based on efficiency and component size requirements (a value between 10kHz and 50kHz is typical).
2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.
3. Adjust the inductor value down until the desired output voltage is achieved, then decrease its value by 30% to cover manufacturing tolerances.
4. Check the output voltage with an oscilloscope for ripple, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents
(eff = $(V_{OUT})\,(I_{OUT})/(+V_S)\,(I_{SY})$ x 100%).
5. If the efficiency is poor, go back to step 1. and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Compensation

When large values (> 50 kΩ) are used for the voltage setting resistors (R1 and R2 of Figure 2) stray capacitance at the V_{FB} input can add lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100 pF to 10 nF. In inverting applications, the capacitor connects between $-V_{OUT}$ and V_{FB}; for step-down circuits it connects between ground and V_{FB}. Most applications do not require this capacitor.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for bread-boarding prototypes. Care must be taken to choose a core with enough permeability to handle the magnetic flux produced at I_{MAX}. If the core saturates, then efficiency and output current capability are severely degraded and excessive current will flow through the switch transistor. A pot core inductor design section is provided later in this datasheet.

An isolated AC current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 7). This level is determined by the +1.25V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery drops below this threshold Q2 will turn on and sink typically 600µA. The low battery detection circuit can also be used for other less conventional applications such as the voltage dependent oscillator circuit of Figure 12.

Device Shutdown

The entire device may be shut down to an extremely low current non-operating condition by disconnecting the ground (pin 4). This can be easily done by putting an NPN transistor in series with ground pin and switching it with an external signal. This switch will not affect the efficiency of operation, but will add to and increase the reference voltage by an amount equal to the saturation voltage of the transistor used. A mechanical switch can also be used in series between circuit ground and pin 4, without introducing any reference offset.

Power Transistor Interfaces

The most important consideration in selecting an external power transistor is the saturation voltage at $I_C = I_{MAX}$. The lower the saturation voltage is, the better the efficiency will be. Also, a higher beta transistor requires less base drive and therefore less power will be.

Also, a higher beta transistor requires less base drive and therefore less power will be consumed in driving it, improving efficiency losses in the interface. The part numbers given in the following applications are recommended, but other types may be more appropriate depending on voltage and power levels.

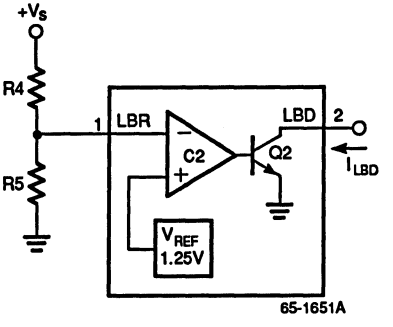


Figure 7. Low Battery Detector

When troubleshooting external power transistor circuits, ensure that clean, sharp-edged waveforms are driving the interface and power transistors. Monitor these waveforms with an oscilloscope — disconnect the inductor, and tie the V_{FB} input (pin 8) high through a 10K resistor. This will cause the regulator to pulse at maximum duty cycle without drawing excessive inductor currents. Check for expected on time and off time, and look for slow rise times that might cause the power transistor to enter its linear operating region.

The following external power transistor circuits may demand some adjustment to resistor values to satisfy various power levels and input/output voltages. C_X and L_X values must be selected according to the design equations (pages 9 and 10).

Inverting Medium Power Application

Figure 8 is a schematic of an inverting medium power supply (250mW to 1W) using an external PNP switch transistor. Supply voltage is applied to the IC via R3: when the internal switch transistor is turned on current through R4 is also drawn through R3; creating a voltage drop from base to emitter of the external switch transistor. This drop turns on the external transistor.

Voltage pulses on the supply lead (pin 6) do not affect circuit operation because the internal reference and bias circuitry have good supply rejection capabilities. A power Schottky diode is used for higher efficiency.

Inverting High Power Application

For higher power applications (500mW to 5W), refer to Figure 9. This circuit uses an extra external transistor to provide well controlled drive current in the correct phase to the power switch transistor. The value of R3 sets the drive current to the switch by making the interface transistor act as a current source. R4 and R5 must be selected such that the RC time constant of R4 and the base capacitance of Q2 do not slow the response time (and affect duty cycle), but not so low in value that excess power is consumed and efficiency suffers. The resistor values chosen should be proportional to the supply voltage (values shown are for +5V).

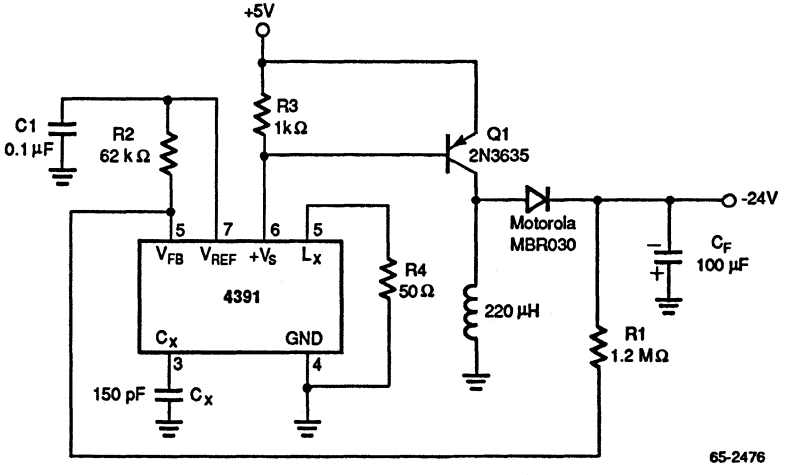


Figure 8. Inverting Medium Power Application

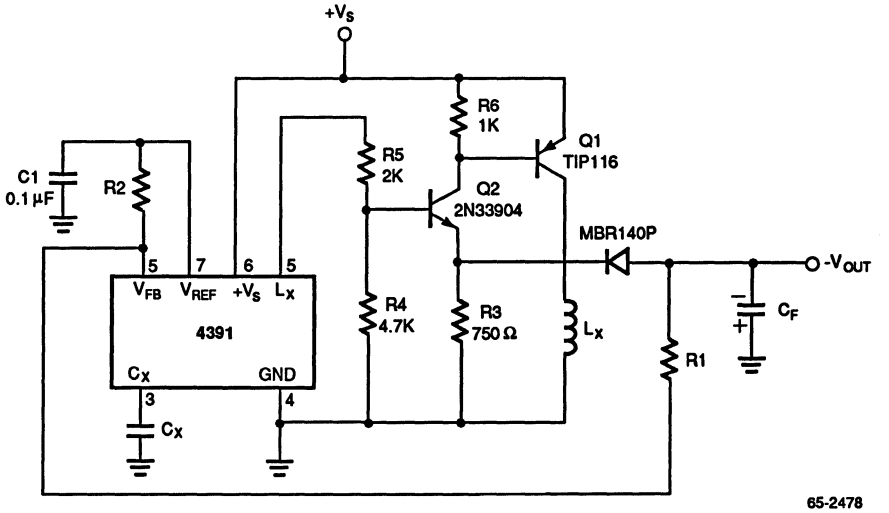


Figure 9. Inverting High Power Application

Step-Down Power Applications

Figures 10 and 11 show medium and high power interfaces modified to perform step-down functioning. The design equations and suggestions for the circuits of Figures 8 and 9 also apply to these circuits. For a certain range of load power, the RC4193 can be used for step-sown applications. A load range from 400mW to 2W can be sustained with fewer components (especially when stepping down greater than 30V) than the comparable 4391 circuit. Refer to Raytheon's RC4191/4192/4193 data sheet for a schematic of this medium power step-down application.

Voltage Dependent Oscillator

The 4391's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best, however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This trade-off between load current capability and output ripple can be improved with the circuit connection shown in Figure 12. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre-programmed threshold is reached.

The threshold is programmed exactly as the normal low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery voltage reaches this threshold the comparator will turn on the open collector transistor at pin 2, effectively pulling C_Y in parallel with C_X. This added capacitance will reduce the oscillator frequency, according to the following equation:

$$F_o(Hz) = \frac{4.1 \times 10^{-6}}{C_X(pF) + C_Y(pF)}$$

Current Limiting

The oscillator (C_X) pin can be used to add short circuit protection and to protect against over current at start-up (when using large values for the output filter capacitor — greater than 100 µF). A transistor V_{BE} is used as a current sensing comparator which resets the oscillator upon sensing an over current condition, thus providing cycle-by-cycle current limiting. Figure 13 shows how this is applied.

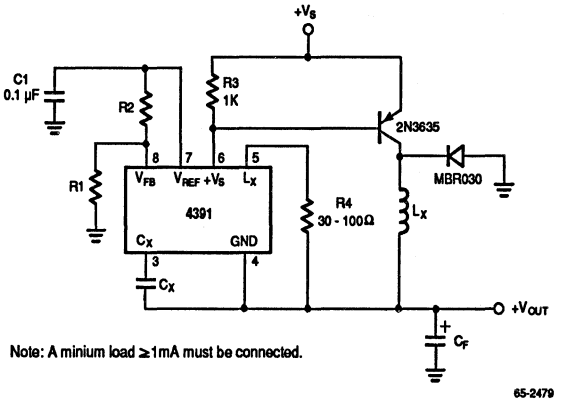


Figure 10. Step-Down Medium Power Application

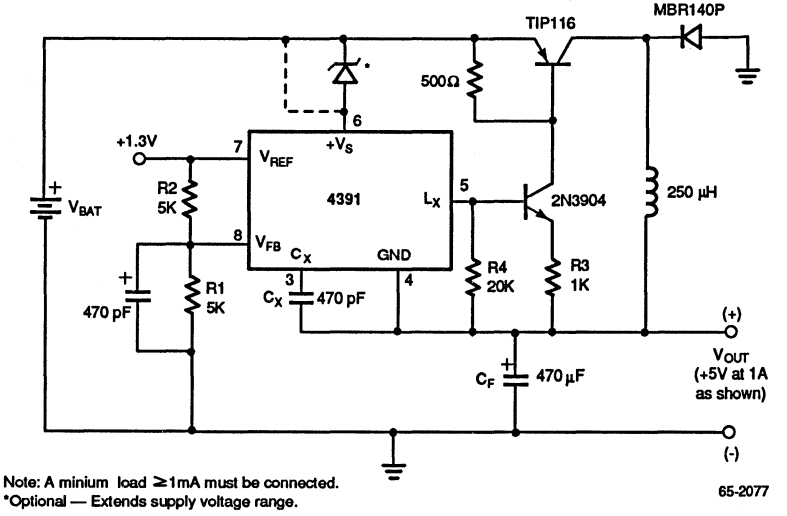


Figure 11. Step-Down High Power Application

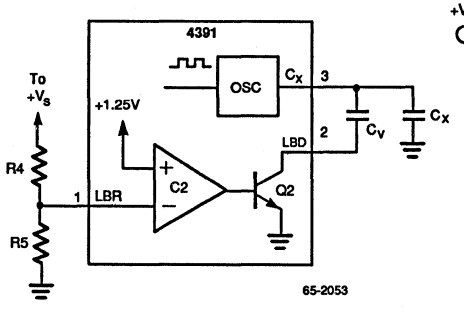


Figure 12. Voltage Dependent Oscillator

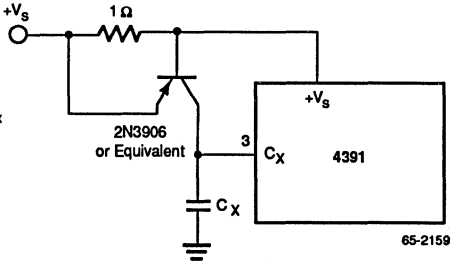
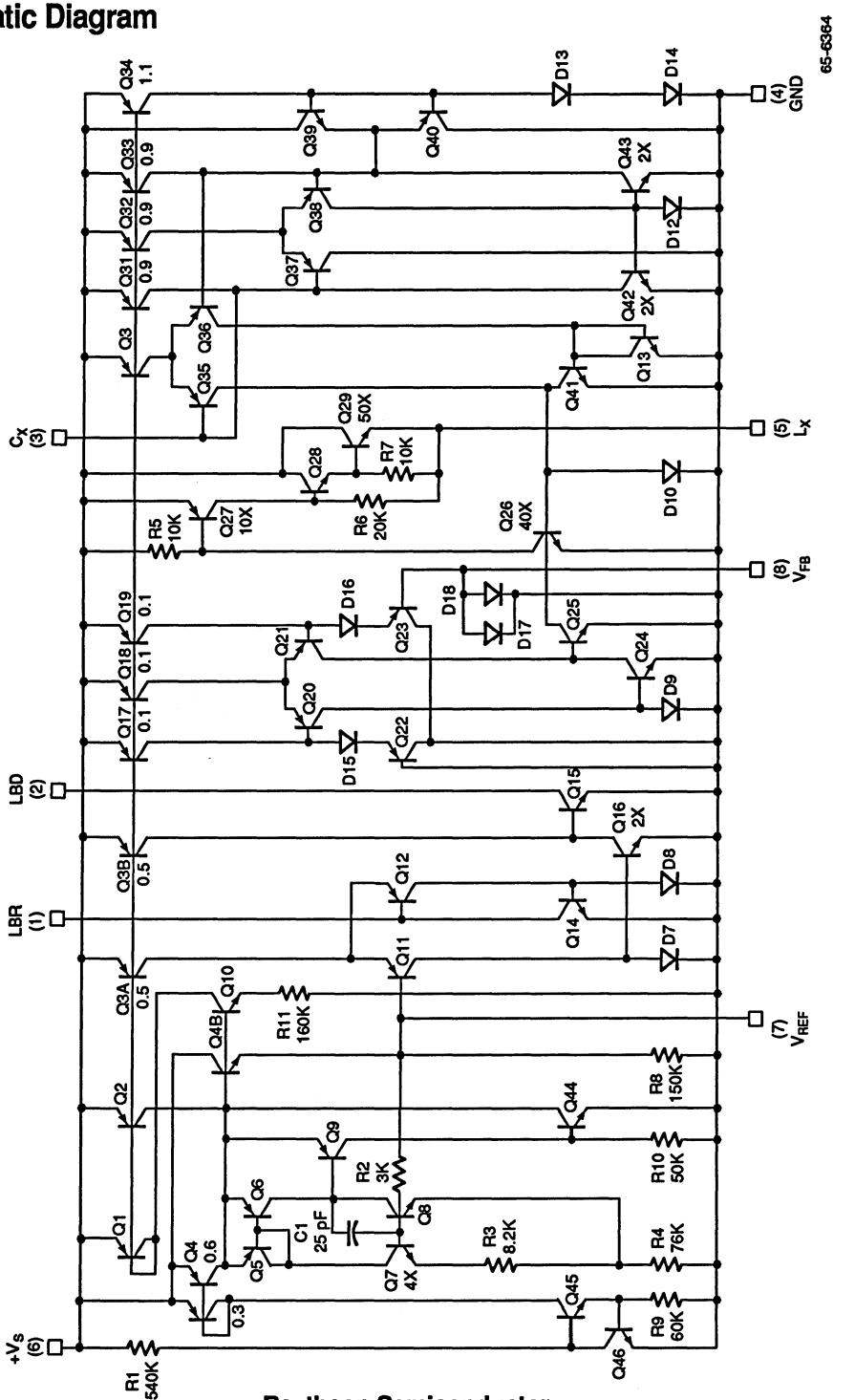
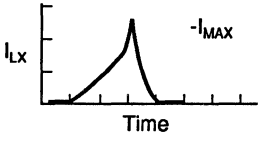
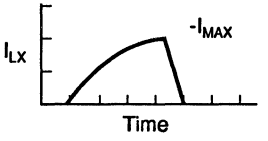
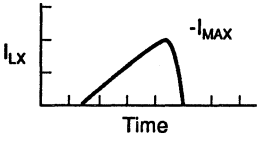


Figure 13. Current Limiting

Schematic Diagram



Troubleshooting Chart

Symptom	Possible Problems
Draws excessive supply current on star-up.	Inductance value too low. Output frequency (F_o) too low. Combination of low resistance inductor and high value filter capacitor — needs current limiting circuit (Figure 13).
Output voltage is low.	Inductance value too high for F_o or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
L_x pin appears noisy — scope will not synchronize.	Normal operating condition.
 Inductor current shows nonlinear waveform.	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
 Inductor current shows nonlinear waveform.	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
 Inductor current is linear until high current is reached. 65-6349	External transistor lacks base drive or beta is too low.
Poor efficiency.	Core saturating. Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high V_{CE}SAT). High series resistance. Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback capacitor from V_{OUT} to V_{FB} (pin 8), 100pF to 1000pF.

Pot Core Inductor Design

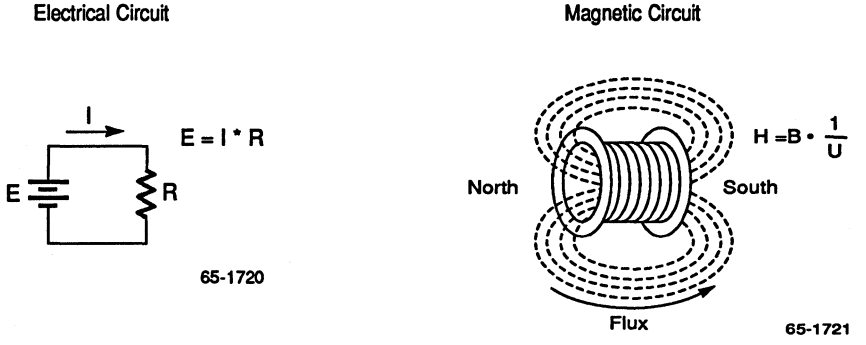


Figure 14. Electricity vs. Magnetism

Electricity Versus Magnetism

Electrically the inductor must meet just one requirement, but that requirement can be hard to satisfy. The inductor must exhibit the correct value of inductance (L, in Henrys) as the inductor current rises to its highest operating value (I_{MAX}). This requirement can be met most simply by choosing a very large core and winding it until it reaches the correct inductance value, but that brute force technique wastes size, weight and money. A more efficient design technique must be used.

Question: What happens if too small a core is used?

First, one must understand how the inductor's magnetic field works. The magnetic circuit in the inductor is very similar to a simple resistive electrical circuit. There is a magnetizing force (H, in oersteds), a flow of magnetism, or flux density (B, in Gauss), and a resistance to the flux, called permeability (U, in Gauss per oersted). H is equivalent to voltage in the electrical model, flux density is like current flow, and permeability is like resistance (except for two important differences discussed to the right).

First Difference: Permeability instead of being analogous to resistance, is actually more like conductance (1/R). As permeability increases, flux increases.

Second Difference: Resistance is a linear function. As voltage increases, current increases proportionally, and the resistance value stays the same. In a magnetic circuit the value of permeability varies as the applied magnetic force varies. This nonlinear characteristic is usually shown in graph form in ferrite core manufacturer's data sheets .

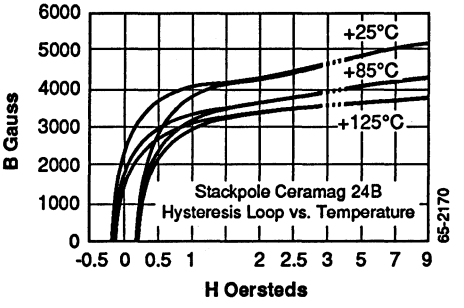


Figure 15. Typical Manufacturer's Curve Showing Saturation Effects

Linear

As the applied magnetizing force increases, at some point the permeability will start decreasing, and therefore the amount of magnetic flux will not increase any further, even as the magnetizing force increases. The physical reality is that, at the point where the permeability decreases, the magnetic field has realigned all of the magnetic domains in the core material. Once all of the domains have been aligned the core will then carry no more flux than just air, it becomes as if there were no core at all. This phenomenon is called saturation. Because the inductance value, L, is dependent on the amount of flux, core saturation will cause the value of L to decrease dramatically, in turn causing excessive and possibly destructive inductor current.

Pot Cores for RC4391

Pot core inductors are best suited for the RC4391 switching regulator for several reasons:

1. **They are available in a wide range of sizes.** RC4391 applications are usually low power with relatively low peak currents (less than 500mA). A small inexpensive pot core can be chosen to meet the circuit requirements.

2. **Pot cores are easily mounted.** They can be bolted directly to the PC card adjacent to the regulator IC.

3. **Pot cores can be easily air-gapped.** The length of the gap is simply adjusted using different washer thicknesses. cores are also available with predetermined air gaps.

4. **Electromagnetic Interference (EMI) is kept to a minimum.** the completely enclosed design of a pot core reduces stray electromagnetic radiation — an important consideration if the regulator circuit is built on a PC card with other circuitry.

Core Size

Question: Is core size selected according to load power?

Not quite. Core size is dependent on the amount of energy stored, not on load power. Raising the operating frequency allows smaller cores and windings. Reduction of the size of the magnetics is the main reason switching regulator design tends toward higher operating frequency. Designs with the RC4391 should use 75 kHz as a maximum running frequency, because the turn off delay of the power transistor and stray capacitive coupling begin to interfere. Most applications are in the 10 to 50 kHz range, for efficiency and EMI reasons.

The peak inductor current (I_{MAX}) must reach a high enough value to meet the load current and simultaneously the inductor value is decreased, then the core can be made smaller. For a given core size and winding, an increase in air gap spacing (an air gap is a break in the material in the magnetic path, like a section broken off a doughnut) will cause the inductance to decrease and I_{MAX} (the usable peak current before saturation)to increase.

The curves shown are typical of the ferrite manufacturer's power HF material, such as Siemens N27 or Stackpole 24B, which are usually offered in standard millimeter sizes including the sizes shown.

Use of the Design Aid Graph

1. From the application requirement, determine the inductor value (L) and the required peak current (I_{MAX}).

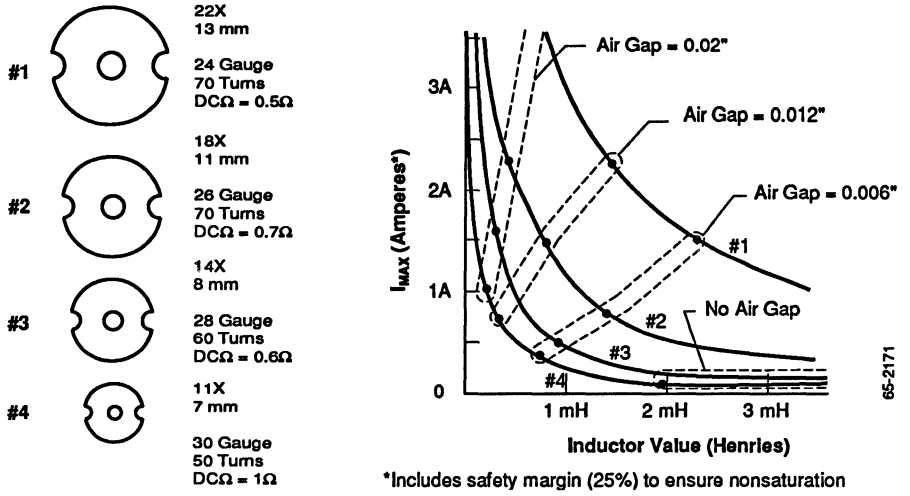


Figure 16. Inductor Design Aid

2. Observe the curves of the design aid graph and determine the smallest core that meets both the L and I requirements.
3. Note the approximate air gap at I_{MAX} for the selected core, and order the core with the gap. (If the gapping is done by the user, remember that a washer lspacer results in an air gap of twice the washer thickness, because two gaps will be created, one at the center post and one at the rim, like taking two bites from a doughnut.)
4. If the required inductance is equal to the indicated value on the graph, then wind the core with the number of turns shown in the table of sizes. The turns given are the maximum number for that gauge of wire that can be easily wound in cores winding area.
5. If the required inductance is less than the value indicated on the graph, a simple calculation must be done to find the adjusted number of turns. Find A_L (inductance index) for a specific air gap.

$$\frac{L\ (\text{indicated})}{\text{Turns}^2} = A_L\ (\text{in Henries/Turn}^2)$$

Then divide the required inductance value by AL to give the actual turns squared, and take the square root to find the actual turns needed.

$$\text{Actual Turns} = \frac{L\ (\text{required})}{A_L}$$

If the actual number of turns is significantly less than the number from the table then the wire size can be increased to use up the leftover winding area and reduce resistive losses.

6. Wind and gap the core as per calculations, and measure the value with an inductance meter. Some adjustment of the number of turns may be necessary.

The saturation characteristics may be checked with the inductor wired into the switching regulator application circuit. To do so, build and power up the circuit. Then clamp an oscilloscope current probe (recommend Tektronix P6042 or equivalent) around the inductor lead and monitor the current in the inductor. Draw the maximum load current from the application circuit so that the regulator is running at close to full duty cycle. Compare the waveform you see to those pictured.

Check for saturation at the highest expected ambient temperature.

Proper Operation
(Waveform is Fairly Linear)

65-1722

Improper Operation
(Waveform is Nonlinear, Inductor is Saturating)

65-1723

Figure 17. Inductor Current Waveforms

7. After the operation in circuit has been checked, reassemble and pot the core using a potting compound recommended by the manufacturer.

   If the core material differs greatly in magnetic characteristics from the standard power material shown in Figure 16, then the following general equation can be used to help in winding and gapping. This equation can be used for any core geometry, such as an E-E core.

$$L_x = \frac{(1.26)\ (N^2)(Ae)(10^8)}{g = (le/ue)}$$

Where:
- N = number of turns
- Ae = core area from data sheet (in cm^2)
- le = magnetic path length from data sheet (in cm)
- ue = permeability of core from manufacturer's graph
- g = center post air gap (in cm)

Manufacturers

Below is a list of several pot core manufacturers:

Ferroxcube Company
5083 Kings Highway
Saugerties, NY 12477

Indiana General Electronics
Keasley, NJ 08832

Siemens Company
186 Wood Avenue South
Iselin, NJ 08830

Stackpole Company
201 Stackpole Street
St. Mary, PA 15857

TDK Electronics
13-1, 1-Chrome
Nihonbaski, Chuo-ku, Tokyo

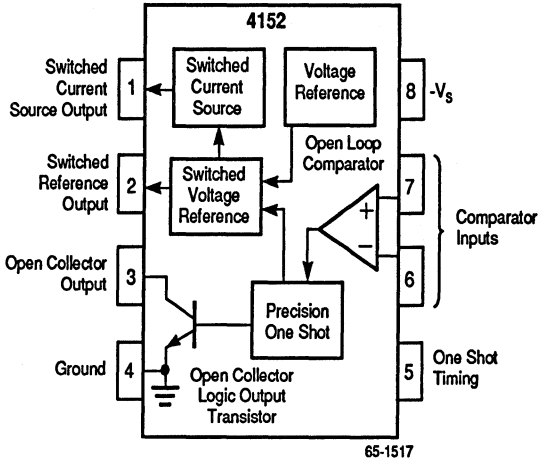
RC4152
Voltage-to-Frequency Converters

Description

The 4152 is a monolithic circuit containing all of the active components needed to build a complete voltage-to-frequency converter. Circuits that convert a DC voltage to a pulse train can be built by adding a few resistors and capacitors to the internal comparator, one-shot, voltage reference, and switched current source. Frequency-to-voltage converters (FVCs) and may other signal conditioning circuits are also easily created using these converters.

Raytheon was the first company to introduce a monolithic VFC. The 4151 offers guaranteed temperature and accuracy specifications. The converter is available in a standard 8-pin plastic DIP.

Functional Block Diagram



Features

- Single supply operation
- Pulse output DTL/TTL/CMOS compatible
- Programmable scale factor (K)
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- V-F or F-V conversion
- Voltage or current input
- Wide dynamic range

Applications

- Precision voltage-to-frequency converters
- Pulse-width modulators
- Programmable pulse generators
- Frequency-to-voltage converters
- Integrating analog-to-digital converters
- Long-term analog integrators
- Signal conversion:
  - — Current-to-Frequency
  - — Temperature-to-Frequency
  - — Pressure-to-Frequency
  - — Capacitance-to-Frequency
  - — Frequency-to-Current
- Signal isolation:
  - — VFC—opto-isolation—FVC
  - — ADC with opto-isolation
- Signal encoding:
  - — FSK modulation/demodulation
  - — Pulse-width modulation
- Frequency scaling
- DC motor speed control

Absolute Maximum Ratings

Supply Voltage ..... + 22V
Internal Power Dissipation ..... 500 mW
Input Voltage ..... -0.2V to $+V_S$
Output Sink Current
(Frequency Output) ..... 20 mA
Output Short Circuit to Ground ..... Continuous
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
RC4152 ..... 0°C to +70°C
RV4152N ..... -25°C to +85°C

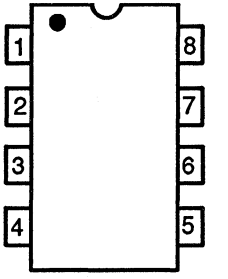
Note:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of electrical Characteristics provide conditions for actual device operation.

Ordering Information

Part Number	Package	Operating Temperature Range
RC4152N	N	0°C to +70°C
RC4152M	M	0°C to 70°C
RV4152N	N	-25°C to +85°C

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC

Connection Information



65-1529

Pin	Function
1	Switched Current Source Output (I_{OUT})
2	Switched Voltage Reference (R_S)
3	Logic Output (Open Collector) (F_{OUT})
4	Ground (GND)
5	One-Shot R, C Timing (C_O)
6	Threshold (V_{TH})
7	Input Voltage (V_{IN})
8	$+V_S$

Thermal Characteristics

	8-Lead Plastic DIP	Small Outline SO-8
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A <50°C	468 mW	300mW
Therm. Res θ_{JC}	—	—
Therm. Res. θ_{JA}	160°C/W	240°C/W
For T_A >50°C Derate at	6.25 mW/°C	4.17mW/°C

Electrical Characteristics

(V_S = +15V, and T_A = +25°C unless otherwise noted)

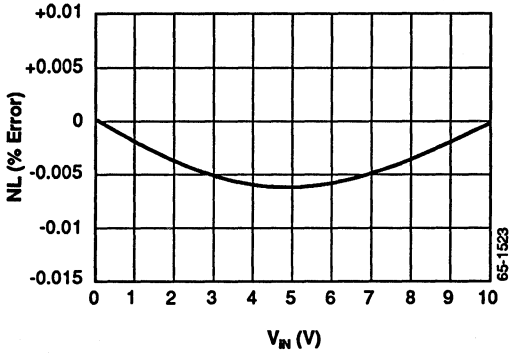
Parameters	Test Conditions	Min	Typ	Max	Units
Power Supply Requirements (Pin 8)					
Supply Current	V_S = +15V		2.5	6.0	mA
Supply Voltage		+7.0	+15	+18	V
Input Comparator (Pins 6 and 7)					
V_{OS}			±2.0	±10	mV
Input Bias Current			-50	-300	nA
Input Offset Current			±30	±100	nA
Input Voltage Range		0	V_S-2	V_S-3	V
One Shot (Pin 5)					
Threshold Voltage		0.65	0.67	0.69	V
Input Bias Current			-50	-500	nA
Saturation Voltage	I = 2.2 mA		0.1	0.5	V
Drift of Timing vs.	T = 75 µs				
Temperature[2]	over specified temperature range		±30	±50	ppm/°C
Timing Drift vs. Supply Voltage			±100		ppm/V
Switched Current Source (pin 1) [1]					
Output Current	R_S = 16.7K, over		+138		µA
Drift vs. Temperature[2]	specified temperature range		±50	±100	ppm/°C
Drift vs. Supply Voltage			0.10		%/V
Leakage Current	Off State		1.0	50	nA
Compliance	Pin 1 = 0V to +10V	1.0	2.5		µA
Reference Voltage (Pin 2)					
V_{REF}		2.0	2.25	2.5	V
Drift vs. Temperature[2]	over specified temperature range		±50	±100	ppm/°C
Logic Output (Pin 3)	I_{SINK} = 3 mA		0.1	0.5	V
Saturation Voltage	I_{SINK} = 10 mA		0.8		
Leakage Current	Off State		0.1	1.0	µA
Nonlinearity Error					
(Voltage Sourced Circuit of Figure 3)	1.0 Hz to 10 kHz		0.007	0.05	%
Temperature Drift Voltage[2]	F_{OUT} = 10 kHz, over				
(Voltage Sourced Circuit of Figure 3)	over specified temperature range		±75	±150	ppm/°C

Notes:

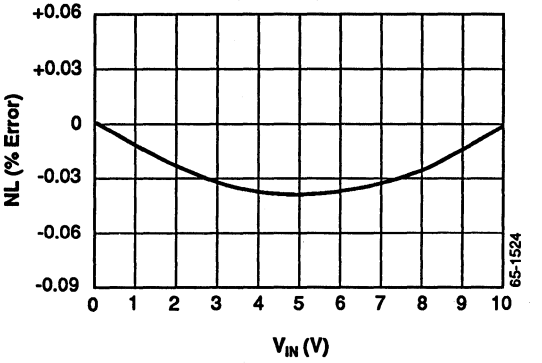
1. Temperature coefficient of output current source (pin 1 output) exclusive of reference voltage drift.
2. Guaranteed but not tested.

Typical Performance Characteristics

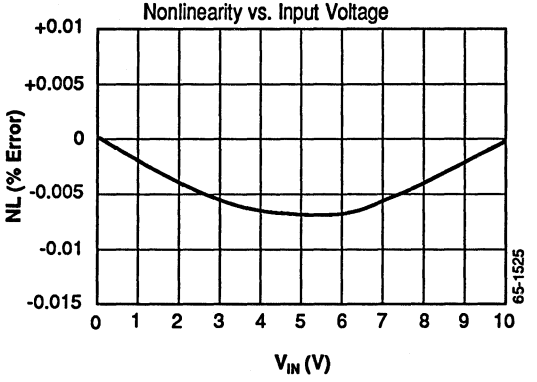
10 KHz Current-Sourced VFC
Nonlinearity vs. Input Voltage



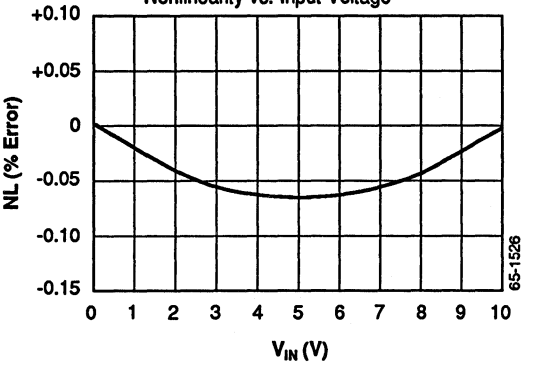
100 KHz Current-Sourced VFC
Nonlinearity vs. Input Voltage



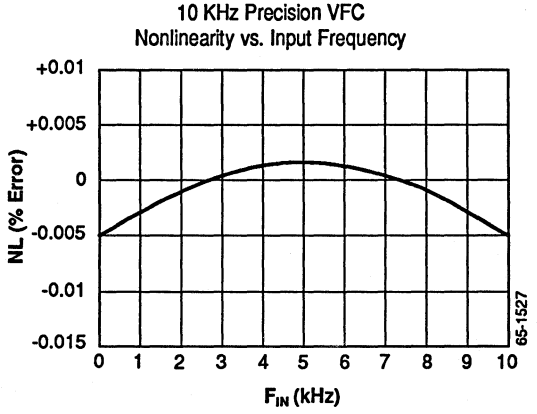
10 KHz Voltage-Sourced VFC
Nonlinearity vs. Input Voltage



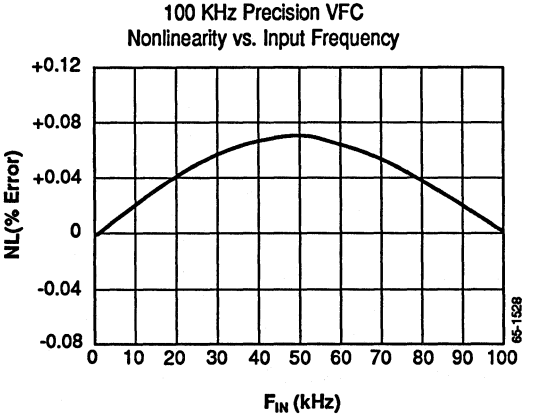
100 KHz Voltage-Sourced VFC
Nonlinearity vs. Input Voltage



10 KHz Precision VFC
Nonlinearity vs. Input Frequency



100 KHz Precision VFC
Nonlinearity vs. Input Frequency



Principles of Operation

The 4152 contains the following components: an open loop comparator, a precision one-shot timer, a switched voltage reference, a switched current source, and an open collector logic output transistor. These functional blocks are internally interconnected in a special way. By adding some external resistors and capacitors, a designer can create a complete voltage-to-frequency converter.

The comparator's output controls the one-shot (monostable timer). The one-shot in turn controls The switched voltage reference, the switched current source and the open collector output transistor. The functional block diagram shows the components and their interconnection.

To detail, if the voltage at pin 7 is greater than the voltage at pin 6, the comparator switches and triggers the one-shot. When the one-shot is triggered, two things happen. First, the one-shot begins its timing period. Second, the one-shot's output turns on the switched voltage reference, the switched current source and the open collector output transistor.

The one-shot creates its timing period much like the popular 555 timer does, by charging a capacitor from a resistor tied to $+V_S$. The one-shot senses the voltage on the capacitor (pin 5) and ends the timing period when the voltage reaches 2/3 of the supply voltage. At the end of the timing period, the capacitor is discharged by a transistor similar to the open collector output transistor.

Meanwhile, during the timing period of the one-shot, the switched current source, the switched voltage reference, and the open collector output transistor all will be switched on. The switched current source (pin 1) will deliver a current proportional to both the reference and an external resistor, R_S. The switched reference (pin 2) will supply an output voltage equal to the internal reference voltage (2.25V). The open collector output transistor will be turned on, forcing the logic output (pin 3) to a low state. At the end of the timing period all of these outputs will turn off. The switched voltage reference has produced an off-on-off voltage pulse, the switched current source has emitted a quanta of charge, and the open collector output has transmitted a logic pulse.

To summarize, the purpose of the circuit is to produce a current pulse, well-defined in amplitude and duration, and to simultaneously produce an output pulse which is compatible with most logic families. The circuit's outputs show a pulse waveform in response to a voltage difference between the comparators inputs.

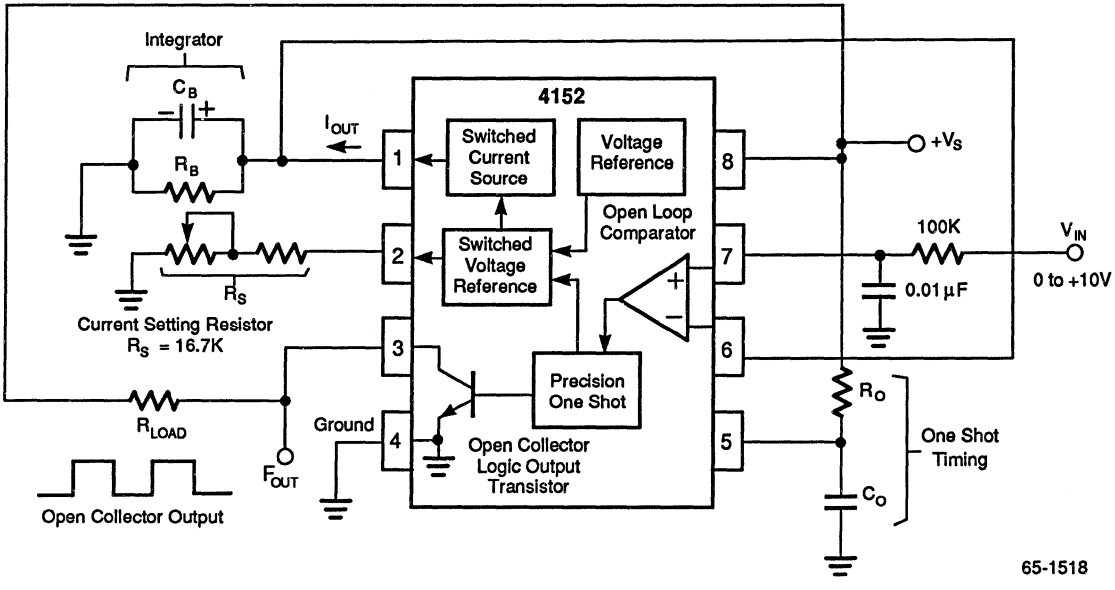


Figure 1. Single Supply VFC

Linear

Applications

Single Supply VFC

The stand-alone voltage-to-frequency converter is one of the simplest applications for the 4152. This application uses only passive external components to create the least expensive VFC circuit (see Figure 1).

The positive input voltage VIN is applied to the input comparator through a low pass filter. The one-shot will fire repetitively and the switched current source will pump out current pulses of amplitude V_{REF}/RS and duration 1.1 R_OC_O into the integrator. Because the integrator is tied back to the inverting comparator input, a feedback loop is created. The pulse repetition rate will increase until the average voltage on the integrator is equal to the DC input voltage at pin 7. The average voltage at pin 6 is proportional to the output frequency because the amount of charge in each current pulse is precisely controlled.

Because the one-shot firing frequency is the same as the open collector output frequency, the output frequency is directly proportional to V_{IN}.

The external passive components set the scale factor. For best linearity, R_S should be limited to a range of 12 kΩ to 20 kΩ.

The reference voltage is nominally 1.9V for the 4151 and 2.25V for the 4152. Recommended values for different operating frequencies are shown in the table below.

Operating Range	R_O	C_O	R_B	C_B
DC to 1.0 kHz	6.8 kΩ	0.1 µF	100 kΩ	10 µF
DC to 10 kHz	6.8 kΩ	0.01 µF	100 kΩ	10 µF
DC to 100 kHz	6.8 kΩ	0.001 µF	100 kΩ	10 µF

The single supply FVC is recommended for uses where dynamic range of the input is limited, and the input does not reach 0V. With 10 kHz values, nonlinearity will be less than 1.0% for a 10 mV to 10V input range, and response time will be about 135 ms.

Precision Current Sourced VFC

This circuit operates similarly to the single supply VFC, except that the passive R-C integrator has been replaced by an active op amp integrator. This increases the dynamic range down to 0V, improves the response time, and eliminates the nonlinearity error introduced by the limited compliance of the switched current source output.

The integrator algebraically sums the positive current pulses from the switched current source with the current V_{IN}/R_B. To operate correctly, the input voltage must be negative, so that when the circuit is balanced, the two currents cancel.

$$T = \frac{1}{F_{OUT}}$$

$$\frac{|V_{IN}|}{R_B} = I_{OUT}\left[\frac{T_P}{T}\right] \quad \text{where } TP = 1.1\ R_OC_O$$

$$I_{OUT} = \frac{V_{REF}}{R_S}$$

By rearranging and substituting,

$$F_{OUT} = \left[\frac{R_S}{1.1\ R_OC_OR_B}\right]\left[\frac{T_P}{T}\right]$$

Recommended component values for different operating frequencies are shown in the table below.

Range Input V_{IN}	Output F_O	Scale Factor	R_O	C_O	C_I	R_B
0 to -10V	0 to 1.0 kHz	0.1 KHz/V	6.8 kΩ	0.1 µF	0.05 µF	100 kΩ
0 to -10V	0 to 10 kHz	1.0 kHz	6.8 kΩ	0.01 µF	0.005 µF	100 kΩ
0 to -10V	0 to 100 kHz	10 kHz/V	6.8 kΩ	0.001 µF	500 pF	100 kΩ

The graphs shown under Typical Performance Characteristics show nonlinearity versus input voltage for the precision current sourced VFC. The best linearity is achieved by using an op amp having greater than 1.0 V/µs slew rate, but any op amp can be used.

Precision Voltage Sourced VFC

This circuit is identical to the current sourced VFC, except that the current pulses into the integrator are derived directly from the switched voltage reference. This improves temperature drift at the expense of high frequency linearity.

The switched current source (pin 1) output has been tied to ground, and R_S has been put in series between the switched voltage reference (pin 2) and the summing node of the op amp. This eliminates temperature drift associated with the switched current source. The graphs under the Typical Performance Characteristics show that the nonlinearity error is worse at high frequency, when compared with the current sourced circuit.

Single Supply FVC

A frequency-to-voltage converter performs the exact

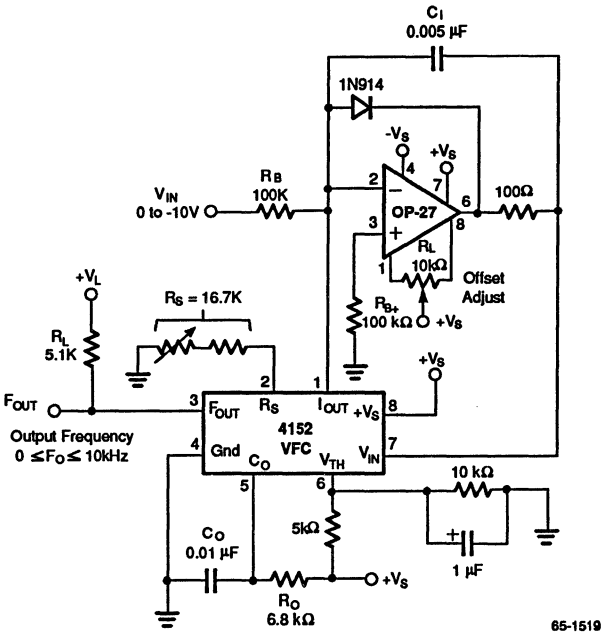


Figure 2. Precision Current Sourced VFC

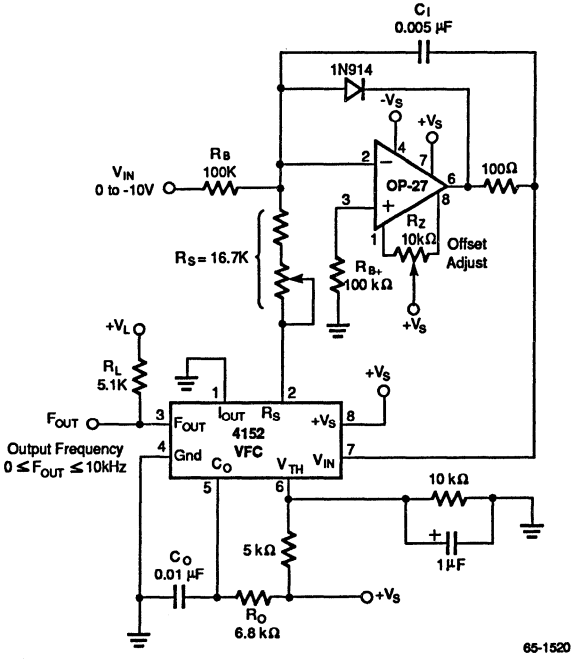


Figure 3. Precision Voltage Sourced VFC

opposite of the VFCs function; it converts an input pulse train into an average output voltage. Incoming pulses trigger the input comparator and fire the one-shot. The one-shot then dumps a charge into the output integrator. The voltage on the integrator becomes a varying DC voltage proportional to the frequency of the input signal. Figure 4 shows a complete single supply FVC.

The input waveform must have fast slewing edges, and the differentiated input signal must be less than the timing period of the one-shot, 1.1 R_OC_O. A differentiator and divider are used to shape and bias the trigger input; a negative going pulse at pin 6 will cause the comparator to fire the one-shot. The input pulse amplitude must be large enough to trip the comparator, but not so large as to exceed the ICs input voltage ratings.

The output voltage is directly proportional to the input frequency:

$$V_{OUT} = \left[\frac{1.1\ R_O C_O R_B\ V_{REF}}{R_S}\right] F_{IN}\,(Hz)$$

Output ripple can be minimized by increasing C_B, but this will limit the response time. Recommended values for various operating ranges are shown in the following table.

Input Operating Range	C_{IN}	R_O	C_O	R_B	C_B	Ripple
0 to 1.0 kHz	0.02 µF	6.8 kΩ	0.1 µF	100 kΩ	100 µF	1.0 mV
0 to 10 kHz	0.002 µF	6.8 kΩ	0.01 µF	100 kΩ	10 µF	1.0 mV
0 to 100 kHz	200 pF	6.8 kΩ	0.001 µF	100 kΩ	1.0 µF	1.0 mV

Precision FVC

Linearity, offset and response time can be improved by adding one or more op amps to form an active lowpass filter at the output. A circuit using a single pole active integrator is shown in Figure 5.

The positive output current pulses are averaged by the inverting integrator, causing the output voltage to be negative. Response time can be further improved by adding a double pole filter to replace the single pole filter. Refer to the graphs under Typical Performance Characteristics that show nonlinearity error versus input frequency for the precision FVC circuit.

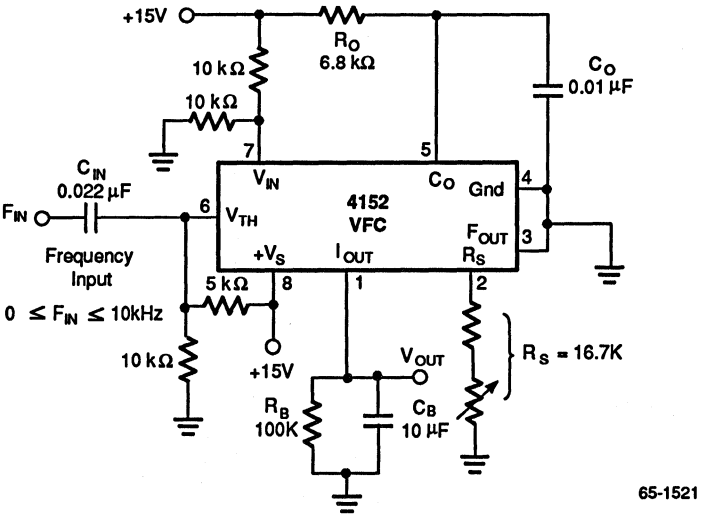


Figure 4. Single Supply FVC

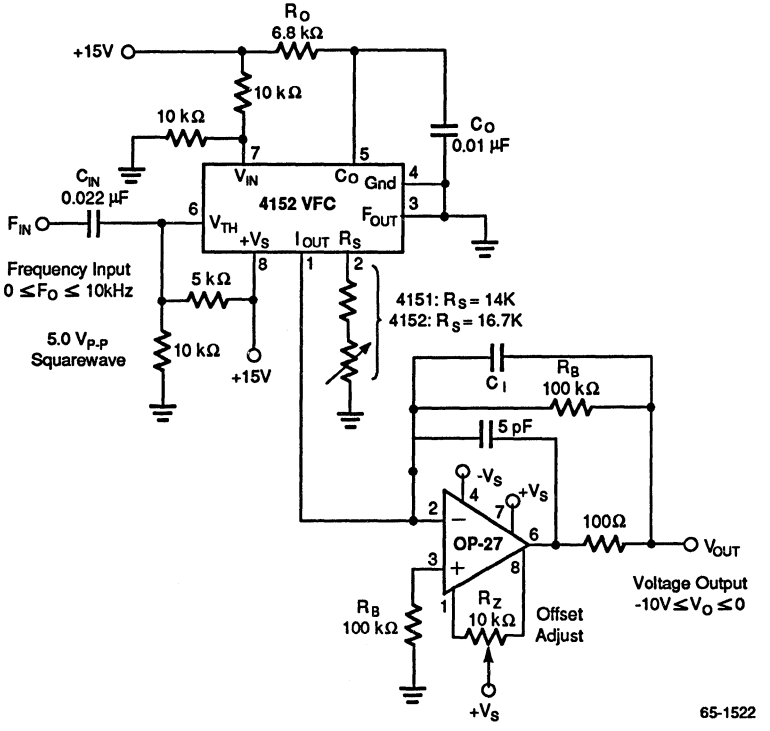
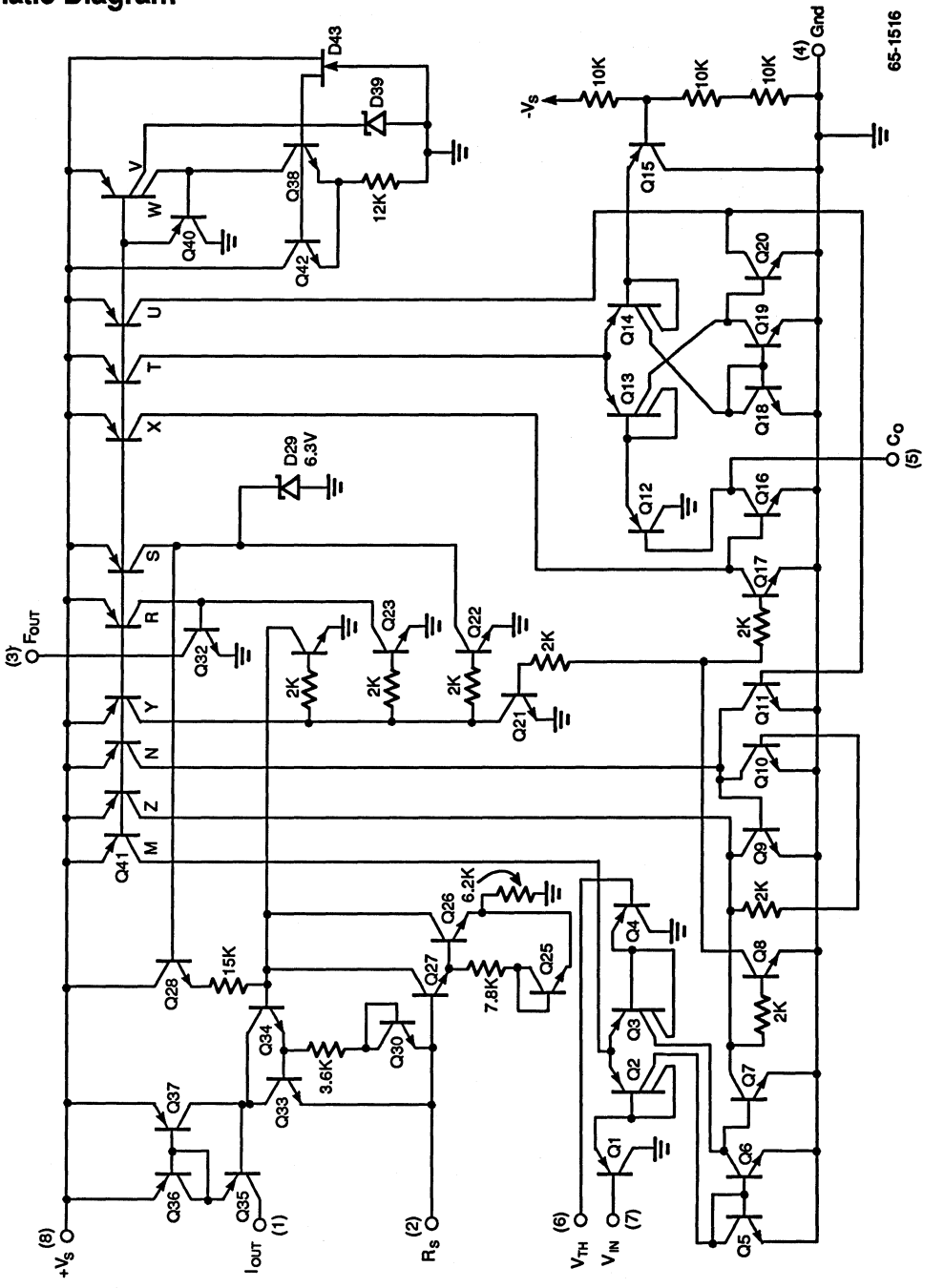


Figure 5. Precision FVC

Schematic Diagram



RC4153
Voltage-to-Frequency Converter

Description

The 4153 sets a new standard for ease of application and high frequency performance in monolithic voltage-to-frequency converters. This voltage-to-frequency converter requires only four passive external components for precision operation, making it ideal for many low cost applications such as A/D conversion, frequency-to-voltage conversion, and serial data transmission. The improved linearity at high frequency makes it comparable to many dual slop A/D converters both in conversion time and accuracy, while retaining the benefits of voltage-to-frequency conversion, i.e., serial output, cost and size. The speed accuracy and temperature performance of the 4153 is achieved by incorporating high speed ECL logic, a high gain, wide bandwidth op amp, and a buried Zener reference on a single monolithic chip.

Features

- 0.1 Hz to 250 kHz dynamic range
- 0.01% F.S. maximum nonlinearity error — 0.1Hz to 10 kHz
- 50 ppm/°C maximum gain temperature coefficient (external reference)
- Few external components required

Applications

- Precision voltage-to-frequency converters
- Serial transmission of analog information
- Pulse width modulators
- Frequency-to-voltage converters
- A/D converters and long term integrators
- Signal isolation
- FSK modulation/demodulation
- Frequency scaling
- Motor speed controls
- Phase lock loop stabilization

Absolute Maximum Ratings(1)

Supply Voltage ..... ±18V
Internal Power Dissipation ..... 500 mW
Input Voltage ..... $-V_S$ to $+V_S$
Output Sink Current
(Frequency Output) ..... 20 mA
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
RM4153 ..... -55°C to +125°C
RC4153 ..... 0°C to +70°C

Note:
1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Thermal Characteristics

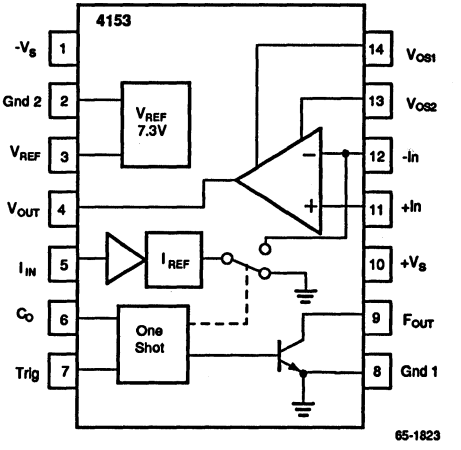
	14-Lead Ceramic DIP
Max. Junction Temp.	+175°C
Max. P_D T_A <50°C	1042 mW
Therm. Res θ_{JC}	60° C/W
Therm. Res. θ_{JA}	120°C/W
For T_A >50°C Derate at	8.33 mW/°C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4153D	D	0°C to +70°C
RM4153D	D	-55°C to +125°C

Notes:
D = 14-lead ceramic DIP

Connection Information



Pin	Function
1	$-V_S$
2	REF Gnd
3	V_{REF} Output
4	V_{OUT} (Op Amp)
5	I_{IN} (REF Input)
6	C_O (Pulse Width)
7	Trigger Input
8	Circuit Gnd
9	Frequency Output (Open Collector)
10	$+V_S$
11	(+) Op Amp Input
12	(-) Op Amp Input
13	V_{OS} Trim
14	V_{OS} Trim

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Min	Typ	Max	Units
Power Supply Requirements				
Supply Voltage	±12	±15	±18	V
Supply Current (+V_S, I_{OUT} = 0)		+4.2	+7.5	mA
(-V_S, I_{OUT} = 0)		-7	-10	
Full Scale Frequency	250	500		kHz
Transfer Characteristics				
Nonlinearity Error Voltage-to-Frequency[1]				
0.1 Hz ≤ F_{OUT} ≤ 10 kHz		0.002	0.01	%FS
1.0 Hz ≤ F_{OUT} ≤ 100 kHz		0.025	0.05	%FS
5.0 Hz ≤ F_{OUT} ≤ 250 kHz		0.06	0.1	%FS
Nonlinearity Error Frequency-to-Voltage[1]				
0.1 Hz ≤ F_{IN} ≤ 10 kHz		0.002	0.01	%FS
1.0 Hz ≤ F_{IN} ≤ 100 kHz		0.05	0.1	%FS
5.0 Hz ≤ F_{IN} ≤ 250 kHz		0.07	0.12	%FS
Scale Factor Tolerance, F = 10 kHz $K = \frac{1}{2V_{REF} R_{IN} C_O}$		±0.5		%
Change of Scale Factor with Supply		0.008		%/V
Reference Voltage (V_{REF})		7.3		V
Temperature Stability (0°C to 70°C) [1, 2, 3]				
Scale Factor 10 KHz Nominal		±75	±150	ppm/°C
Reference Voltage		±50	±100	ppm/°C
Scale Factor (External Ref) 10 KHz FS		±25	±50	ppm/°C
Scale Factor (External Ref) 100 KHz FS		±50	±100	ppm/°C
Scale Factor (External Ref) 250 KHz FS		±100	±150	ppm/°C

Notes:
1. Guaranteed but not tested.
2. V_{REF} Range: 6.6V ≤ V_{REF} ≤ 8.0V.
3. Over the specified operating temperature range.

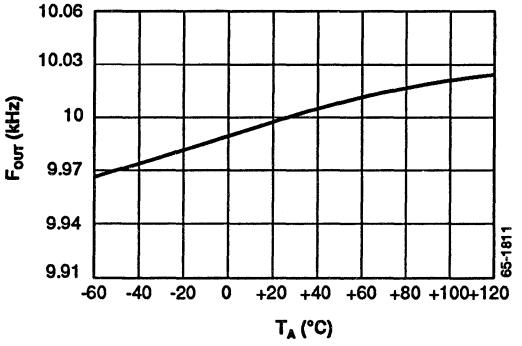
Electrical Characteristics (Continued)

Parameters	Min	Typ	Max	Units
Op Amp				
Open Loop Output Resistance		230		Ω
Short Circuit Current		25		mA
Gain Bandwidth Product [1]	2.5	3.0		MHz
Slew Rate	0.5	2.0		V/μS
Output Voltage Swing ($R_L \geq 2K$)	0 to +10	-0.5 to +14.3		V
Input Bias Current		70	400	nA
Input Offset Voltage (Adjustable to 0)		0.5	5.0	mV
Input Offset Current		30	60	nA
Input Resistance (Differential Mode)		1.0		MΩ
Common Mode Rejection Ratio	75	100		dB
Power Supply Rejection Ratio	70	106		dB
Large Signal Voltage Gain	25	350		V/mV
Switched Current Source				
Reference Current (External Reference)		1.0		mA
Digital Input (Frequency-to-Voltage, Pin 7)				
Logic "0"			0.5	V
Logic "1"	2.0			V
Trigger Current		-50		μA
Logic Output (Open Collector)				
Saturation Voltage (Pin 9)				
I_{SINK} = 4 mA		0.15	0.4	V
I_{SINK} = 10 mA		0.4	1.0	V
I_{LEAK} (Off State)		150		nA

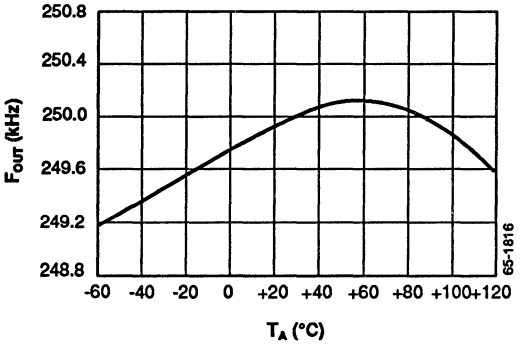
Notes:
1. Guaranteed but not tested.

Typical Performance Characteristics

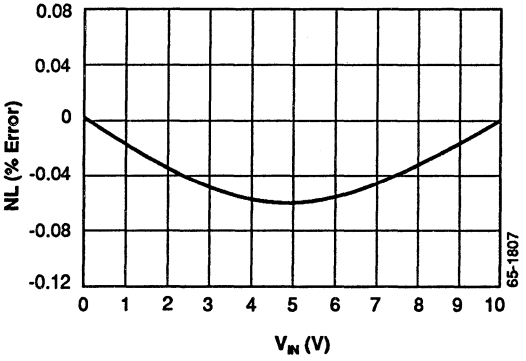
10 kHz Full Scale Drift
Output Frequency vs. Temperature



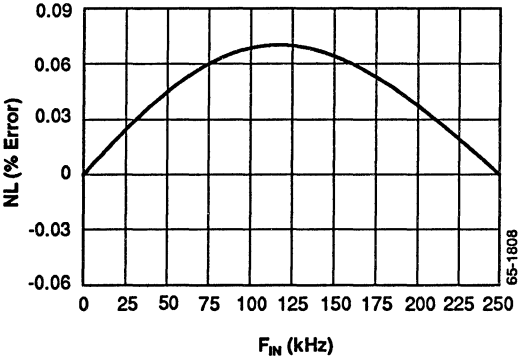
250 kHz Full Scale Drift
Output Frequency vs. Temperature



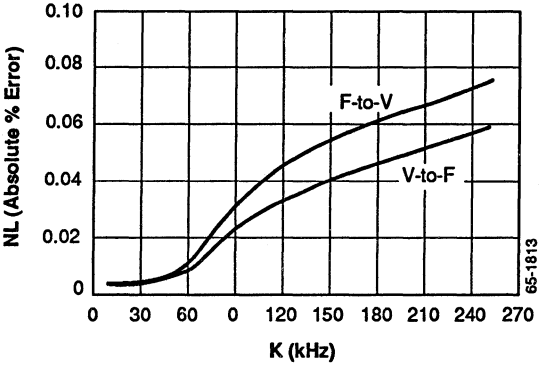
360 kHz Voltage-to-Frequency
Nonlinearity vs. Input Voltage



250 kHz Voltage-to-Frequency
Nonlinearity vs. Input Voltage



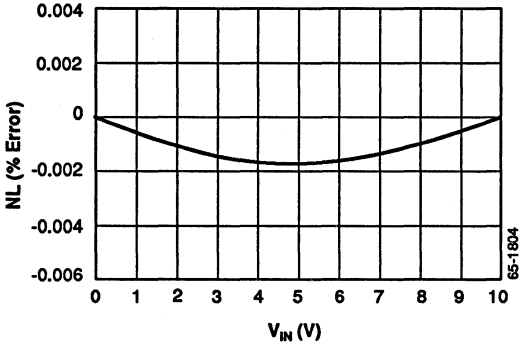
250 KHz Full Scale Peak
Nonlinearity vs. Scale Factor



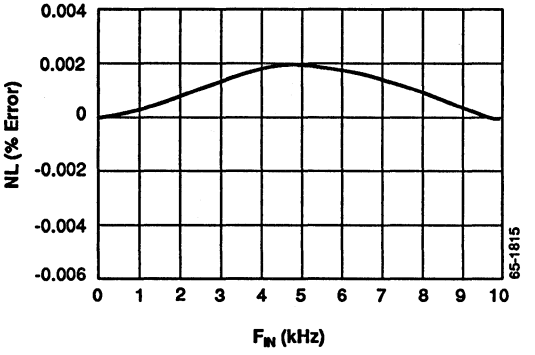
Linear

Typical Performance Characteristics (Continued)

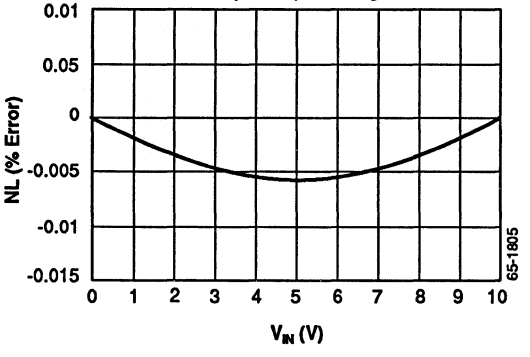
10 KHz Voltage-to-Frequency
Nonlinearity vs. Input Voltage



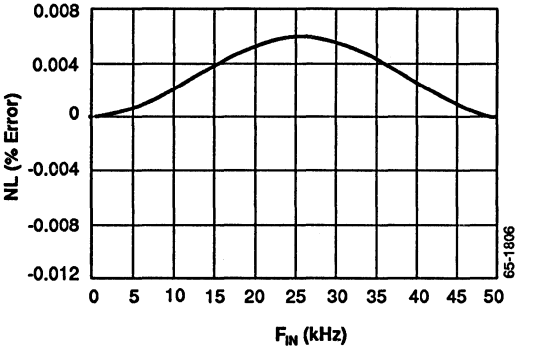
10 KHz Voltage-to-Frequency
Nonlinearity vs. Input Frequency



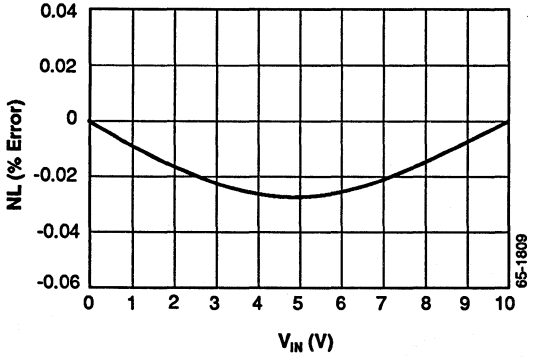
50 KHz Voltage-to-Frequency
Nonlinearity vs. Input Voltage



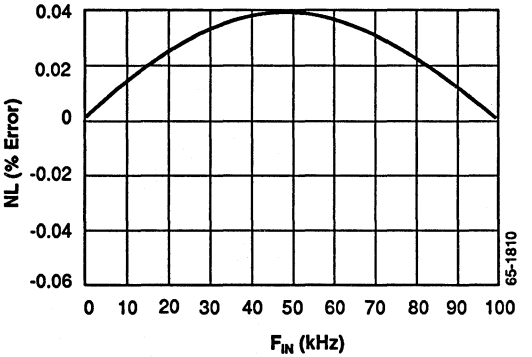
50 KHz Voltage-to-Frequency
Nonlinearity vs. Input Frequency



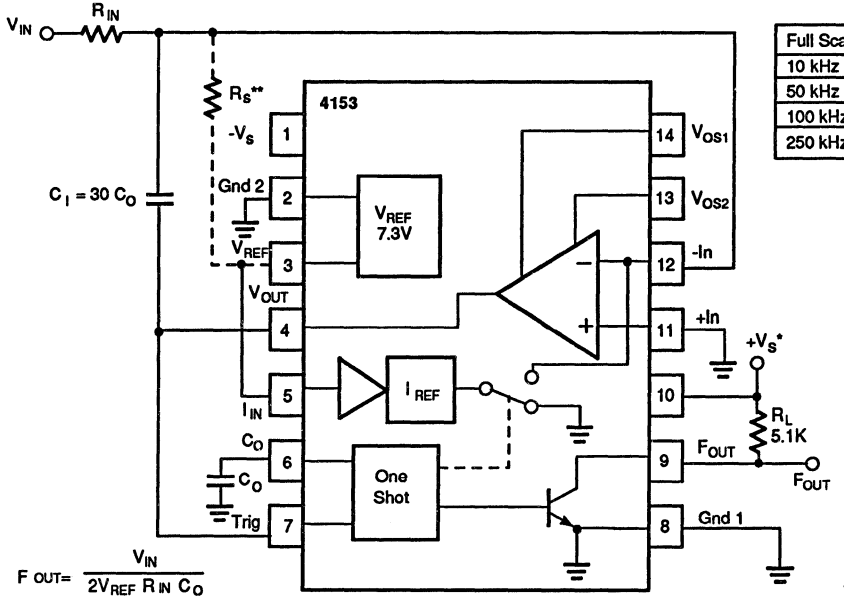
100 KHz Voltage-to-Frequency
Nonlinearity vs. Input Voltage



100 KHz Voltage-to-Frequency
Nonlinearity vs. Input Frequency



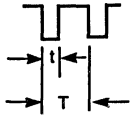
Typical Application Circuits



Full Scale	C_I	C_O	R_{IN}
10 kHz	0.1 µF	3300 pF	20K
50 kHz	0.02 µF	680 pF	20K
100 kHz	4300 pF	330 pF	20K
250 kHz	1000 pF	130 pF	20K

$$F_{OUT} = \frac{V_{IN}}{2V_{REF}\ R_{IN}\ C_O}$$

(V_{REF} = 7.3V)



$$T = \frac{1}{F_{OUT}}$$

$$t = 1.5 \times 10^{-4} C_O$$

$$C_O \leq \frac{5 \times 10^{-5}}{F_{OUT}\ (Max)}$$

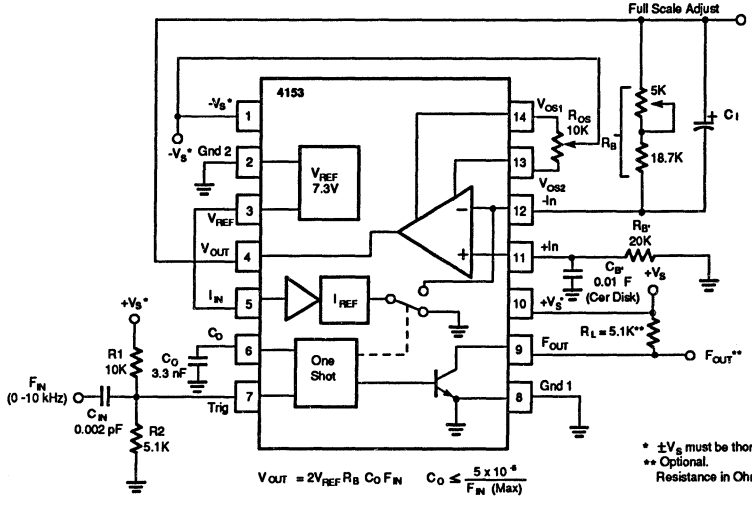
*±V Smust be thoroughly decoupled.
** For bipolar input.
Resistance in Ohms unless otherwise specified.

** For Bipolar Input

$$F_{OUT} = \frac{V_{IN}\ R_{REF} + V_{REF}\ R_{IN}}{2R_{IN}\ R_S\ V_{REF}\ C_O}$$

65-1825

Figure 1. Voltage-to-Frequency Converter Minimum Circuit



Full Scale	C_I	C_O	R_B
10 kHz	10 µF	3300 pF	20K
50 kHz	2 µF	330 pF	40K
100 kHz	1 µF	150 pF	43K
250 kHz	0.2 µF	60 pF	39K

$$V_{RIPPLE} = \frac{2V_{REF}C_O(1 - 1.5 \times 10^4 C_O F_{IN})}{C_I}$$

$$T_{RECOVERY} = 1.36 \times 10^4 C_I\ C_O R_B\ \Delta F_{IN}$$

$V_{OUT} = 2V_{REF} R_B\ C_O F_{IN}$ $\quad C_O \leq \frac{5 \times 10^{-5}}{F_{IN}\ (Max)}$

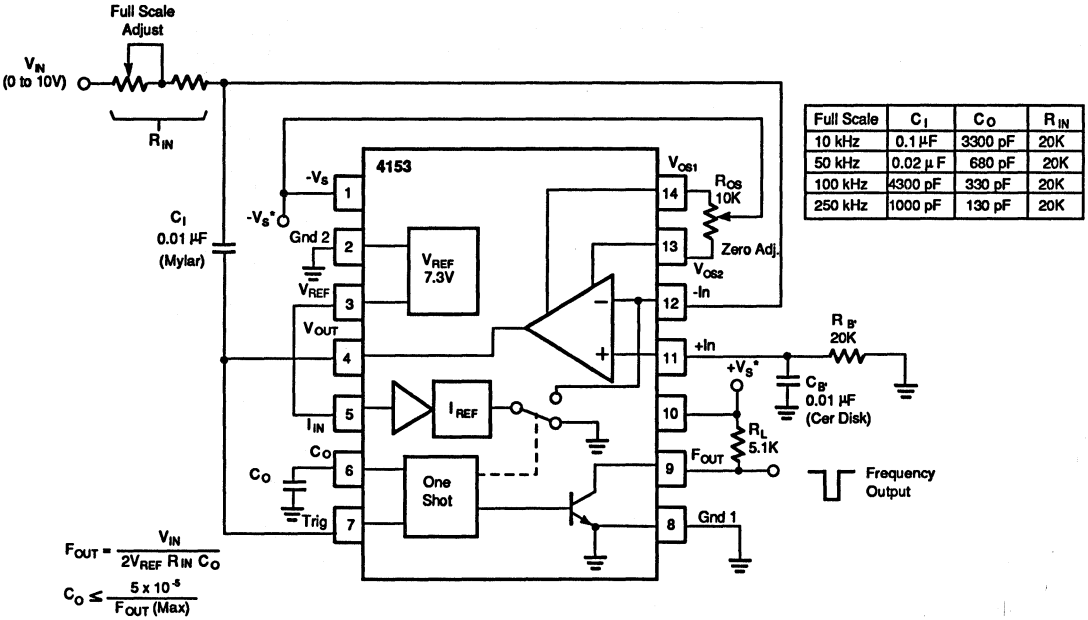
* $\pm V_S$ must be thoroughly decoupled.
** Optional.
Resistance in Ohms unless otherwise specified.

65-1826

Figure 2. Frequency-to-Voltage Converter

Linear

Typical Application Circuits (Continued)



Full Scale	C_I	C_O	R_{IN}
10 kHz	0.1 µF	3300 pF	20K
50 kHz	0.02 µF	680 pF	20K
100 kHz	4300 pF	330 pF	20K
250 kHz	1000 pF	130 pF	20K

$$F_{OUT} = \frac{V_{IN}}{2V_{REF} R_{IN} C_O}$$

$$C_O \leq \frac{5 \times 10^{-5}}{F_{OUT}\,(Max)}$$

* $\pm V_S$ must be thoroughly decoupled.
Resistance in Ohms unless otherwise specified.

65-1828

Figure 3. Voltage-to-Frequency Converter with Offset and Gain Adjusts

Principles of Operation

The 4153 consists of several functional blocks which provide either voltage-to-frequency or frequency-to-voltage conversion, depending on how they are connected. The operation is best understood by examining the block diagram as it is powered in a voltage-to-frequency mode (Figure 4).

When power is first applied, all capacitors are discharged. The input current, V_{IN}/R_{IN}, causes C_I to charge, and point **C** will try to ramp down. The trigger threshold of the one-shot is approximately +1.3V, and if the integrator output is less than +1.3V, the one-shot will fire and pulse the open collector output **E** and the switched current source **A** (see Figures 4 and 5). Because the point **C** is less than +1.3V, the one-shot fires, and the switched current source delivers a negative current pulse to the integrator. This causes C_{IN} to charge in the opposite direction, and point **C** will ramp up until the end of the one-shot pulse. At that time, the positive current V_{IN}/R_{IN} will again make point **C** ramp down until the trigger threshold is reached.

When power is applied, the one-shot will continuously fire until the integrator output exceeds the trigger threshold. Once this is reached, the one-shot will fire as needed to keep the integrator output above the trigger threshold. If V_{IN} is increased, the slope of the downward ramp increases, and the one-shot will fire more often in order to keep the integrator output high. Since the one-shot firing frequency is the same as the open collector output frequency, any increase in V_{IN} will cause an increase in F_{OUT}. This relationship is very linear because the amount of charge in each I_{OUT} pulse is carefully defined, both in magnitude and duration. The duration of the pulse is set by the timing capacitor C_O (point **D**). This feedback system is called a charge-balanced loop.

The scale factor K (the number of pulses per second for a specified V_{IN}), is adjusted by changing either R_{IN} and therefore I_{IN}, or by changing the amount of charge in each I_{OUT} pulse. Since the magnitude of I_{OUT} is fixed at 1 milliamp, the way to change the amount of charge is by adjusting the one-shot duration set by C_O. (I_{OUT} may be adjusted by changing V_{REF}.) The accuracy of the relationship between V_{IN} and F_{OUT} is affected by three major sources of error: temperature drift, nonlinearity and offset.

The total temperature drift is the sum of the individual drift of the components that make up the system. The greatest source of drift in a typical application is in the timing capacitor, C_O. Low temperature coefficient capacitors, such as silver mica and polystyrene, should be measured for drift, using a capacitance meter. Experimentation has shown that the lowest tempco's are achieved by wiring a parallel capacitor composed of 70% silver mica and 30% polystyrene.

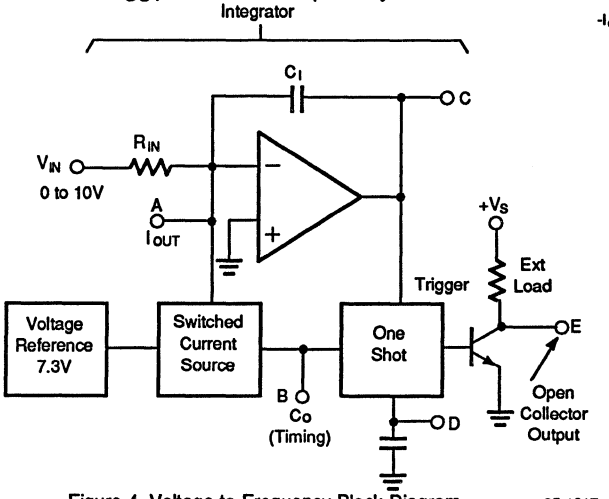


Figure 4. Voltage-to-Frequency Block Diagram 65-1817

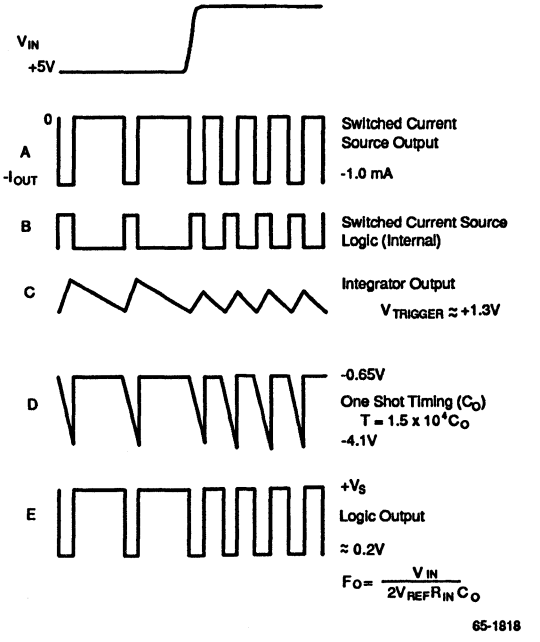


Figure 5. Voltage-to-Frequency Timing Waveforms

Linear

The reference on the chip can be replaced by an external reference with much tighter drift specifications, such as an LM199. The 199's 6.9V output is close to the 4153's 7.3V output, and has less than 10 ppm/°C drift.

Nonlinearity is primarily caused by changes in the precise amount of charge in each I_{OUT} pulse. As frequency increases, internal stray capacitances and switching problems change the width and amplitude of the I_{OUT} pulses, causing a nonlinear relationship between V_{IN} and F_{OUT}. For this reason, the scale factor you choose should be below 1 KHz/V or as low as the acquisition time of your system will allow.

Nonlinearity is also affected by the ratio of C_I to C_O. Less error can be achieved by increasing the value of C_I, but this affects response time and temperature drift. Optimum values for C_I and C_O are shown in the tables in Figures 1, 2, and 3. These values represent the best compromise of nonlinearity and temperature drift. Polypropylene, mylar or polystyrene capacitors should be used for C_I.

The accuracy at low input voltages is limited by the offset and V_{OS} drift of the op amp. To improve this condition, an offset adjust is provided.

Once your system is running, it may be calibrated as follows: apply a measured full scale input voltage and adjust R_{IN} until the scale factor is correct. For precise applications, trimming by soldering metal film resistors in parallel is recommended instead of trimpots, which have bad tempcos and are easily taken out of adjustment by mechanical shock. After the scale factor is calibrated, apply a known small input voltage (approximately 10 mV) and adjust the op amp offset until the output frequency equals the input multiplied by the scale factor.

The output **E** consists of a series of negative going pulses with a pulse width equal to the one-shot time. The open collector pull-up resistor may be connected to a different supply (such as 5V for TTL) as long as it does not exceed the value of $+V_S$ applied to pin 10. The load current should be kept below 10 mA in order to minimize strain on the device. Pins 2 and 8 must be grounded in all applications, even if the open collector transistor is not used.

Figure 6 shows the complete circuit for a precision frequency-to-voltage converter. This circuit converts an input frequency to a proportional voltage by integrating the switched current source output. As the input frequency increases, the number of I_{OUT} pulses delivered to the integrator increases, thus increasing the average output voltage. Depending on the time constant of the integrator, there will be some ripple on the output. The output may be further filtered, but this will reduce the response time. A second order filter will decrease ripple and improve response time.

The input waveform must meet three conditions for proper frequency-to-voltage operation. First, it must have sufficient amplitude and offset to swing above and below the 1.3V trigger threshold (See Figure 6 for an example of AC coupling and offset bias.) Second, it must be a fast slewing waveform having a quick rise time. A comparator may be used to square it up. Finally, the input pulse width must not exceed the one-shot time, in order to avoid retriggering the one-shot (AC couple the input).

Capacitive coupling between the trigger input and the timing capacitor pin may occur if the input waveform is a squarewave or the input has a short period. This can cause gross nonlinearity due to changes in the one-shot timing waveform (See Figure 7). This problem can be avoided by keeping the value of C_O small, and thereby keeping the timing period less than the input waveform period.

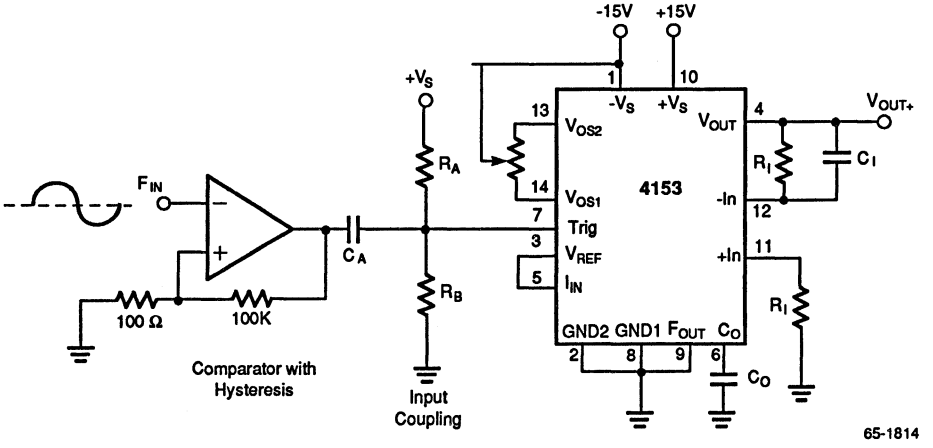


Figure 6. Frequency-to-Voltage Precision Converter

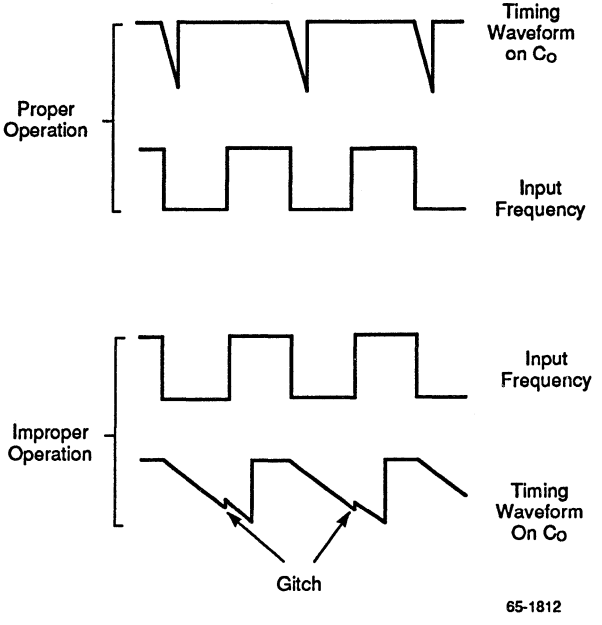


Figure 7. Frequency-to-Voltage Timing Waveforms

Linear

Detailed Circuit Operation

The circuit consists of a buried zener reference (breakdown occurs below the surface of the die, reducing noise and contamination), a high speed one-shot, a high speed switched precision voltage-to-current converter and an open-collector output transistor.

Figure 8 shows a block diagram of the high speed one-shot and Figure 9 shows the monolithic implementation. A trigger pulse sets the R-S latch, which lets C_O charge from I_T. When the voltage on C_O exceeds V_{TH}, the comparator resets the latch and discharges C_O. Looking at the detailed schematic, a positive trigger voltage turns on Q5, turns off Q4, and turns on Q3. Q3 provides more drive to Q5 keeping it on and latching the base of Q11 low. This turns on the switched current source and turns off Q1, allowing C_O to charge in a negative direction. When the voltage on C_O exceeds V_{TH}, Q13's collector pulls Q3's base down, resetting the latch, turning off the switched current source and discharging C_O through Q1. Note that all of the transistors in the signal path are NPNs, and that the voltage swings are minimized ECL fashion to reduce delays. Minimum delay means minimum drift of the resultant VFC scale factor at high frequency.

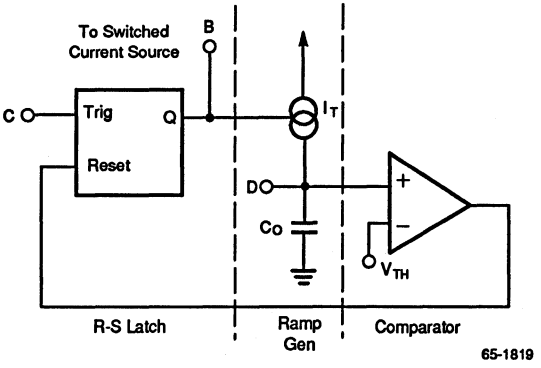


Figure 8. One-Shot Block Diagram

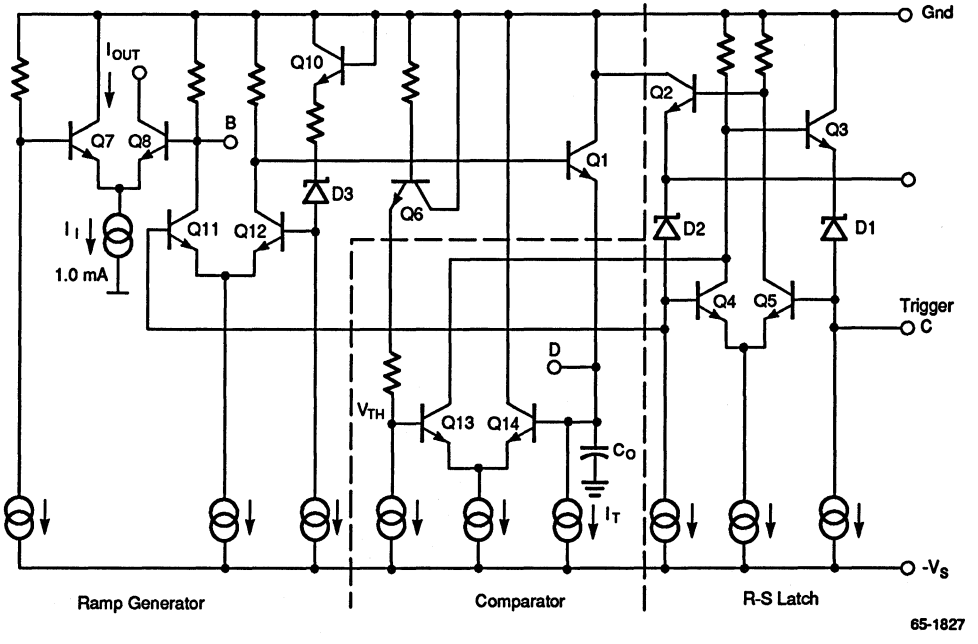


Figure 9. One-Shot (Detail)

The switched current source is shown as a block diagram in Figure 10 and detailed in Figure 11. The summing node (+ input of the op amp) is held at 0V by the amplifier feedback, causing V_{REF} to be applied across R60. This current (V_{REF}/R60), minus the small amplifier bias current, flows through Q35. Q35 develops a V_{BE} dependent on that current. This V_{BE} is developed across Q36. Since Q35 and Q36 are equal in area, their currents are equal. This mirrored current is switched by the one-shot output.

The detail schematic shows the amplifier and load (Q21 through Q34), the mirror transistors (Q35, Q36) and the differential switching transistors (Q7, Q8). The amplifier uses a complementary paraphase input composed of Q21 through Q26 with a current mirror formed by Q27 through Q30, which converts from differential to single-ended output. Level-shift diodes Q32 and Q34 and emitter follower Q31 bootstrap the emitters of the mirror devices Q29 and Q30 to increase gain and lower input offsets, which would otherwise be caused by unbalanced collector voltages on Q23 and Q26. Matching emitter currents in Q35 and Q36 are assured by degeneration resistors R3 and R4. The differential switch allows the current source to remain active continuously, shunting to ground in the off state. This helps stabilize the output, and again, NPNs reduce switching time, timing errors, and most important, drift of timing errors over temperature.

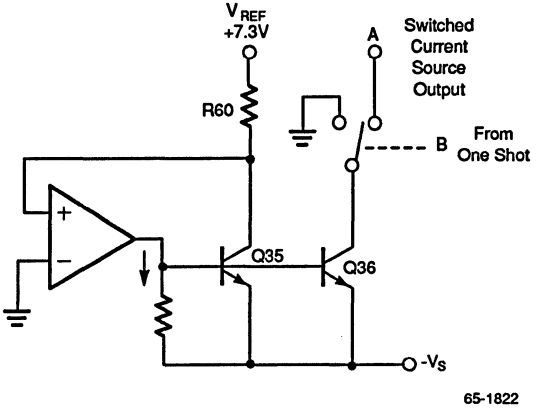


Figure 10. Switched Current Source Block Diagram

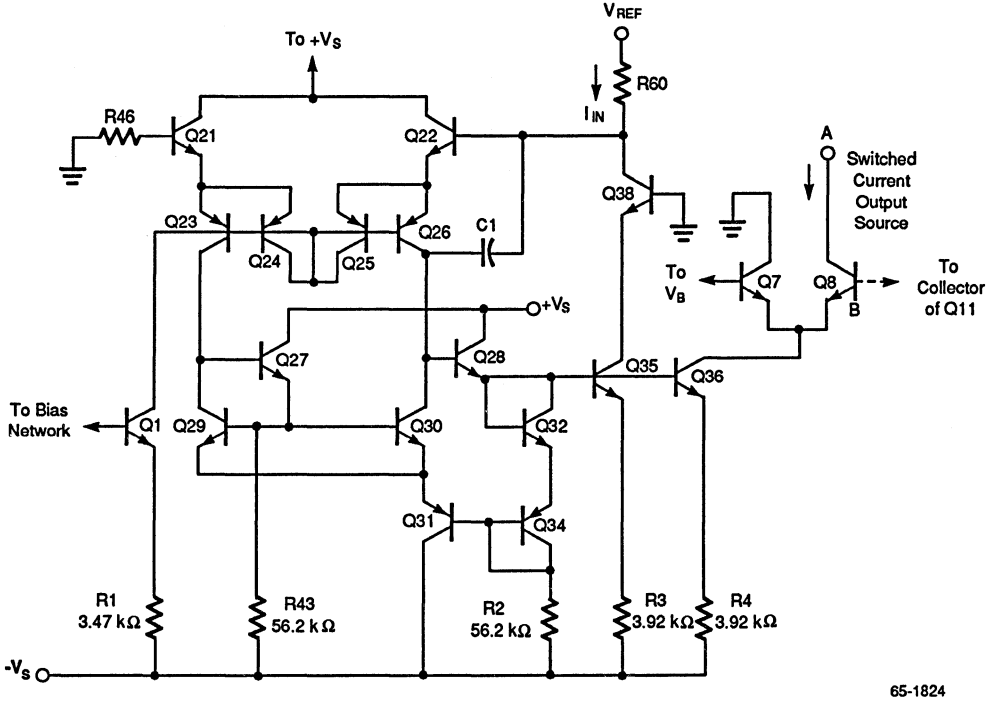
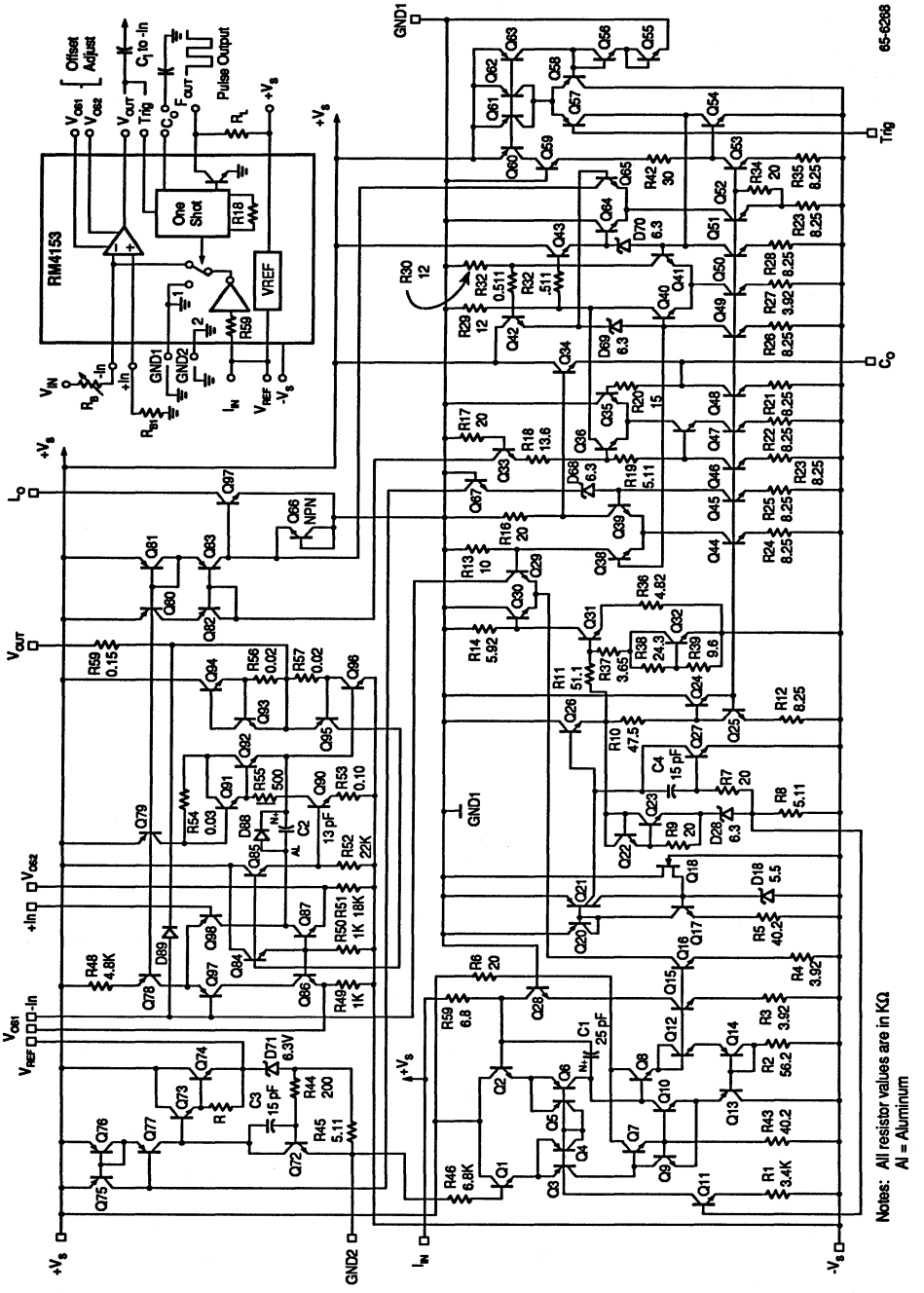


Figure 11. Switched Current Source (Detail)

Schematic Diagram



RV4140
Low Power Two-Wire Ground Fault Interrupter Controller

Description

The RV4140 is a low power controller for AC outlet appliance leakage circuit interrupters. These devices detect hazardous current paths to ground such as an appliance falling into water. The interrupter then open circuits the line before a harmful or lethal shock occurs.

Internally, the RV4140 has a diode bridge rectifier, zener shunt regulator, op amp, current reference, time delay circuit, latch and SCR driver.

An external sense transformer, SCR, relay, two resistors and three capacitors complete the design of the circuit interrupter. The simple layout and minimum component count ensure ease of application and long term reliability.

Features

- Powered from the AC line
- Built-in bridge rectifier
- Direct interface to SCR
- 350 µA quiescent current
- Adjustable trip current
- Adjustable time delay
- Minimum external components
- Meets UL 943 requirements
- Specifically for two-wire systems
- For use with 110V or 220V systems

Absolute Maximum Ratings

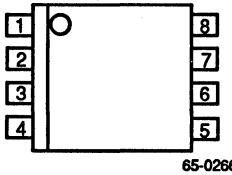
Supply Current ..... 7 mA
Internal Power Dissipation ..... 500 mW
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -35°C to +80°C
Lead Soldering Temperature
(DIP, 60 sec.) ..... +300°C
(SO, 10 sec.) ..... +260°C

Thermal Characteristics

	8 Lead Plastic SOIC	8 Lead Plastic DIP
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A<50°C	300 mW	468 mW
Therm. Res θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For T_A >50°C Derate at	4.1 mW/°C	6.25 mW/°C

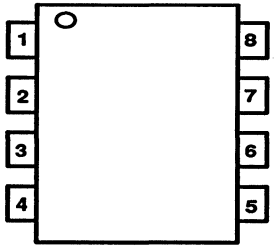
Connection Information

8-Lead Plastic
Dual In-Line SO-8
(Top View)



65-02666

8-Lead Plastic
Dial In-Line Package
(Top View)



65-0093

Pin	Function
1	R_{SET}
2	VFB
3	Common (+2.5V)
4	Ground
5	Line
6	Neutral
7	SCR Trigger
8	C Delay

Ordering Information

Part Number	Package	Operating Temperature Range
RV4140N	N	-35°C to +80°C
RV4140M	M	-35°C to +80°C

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC

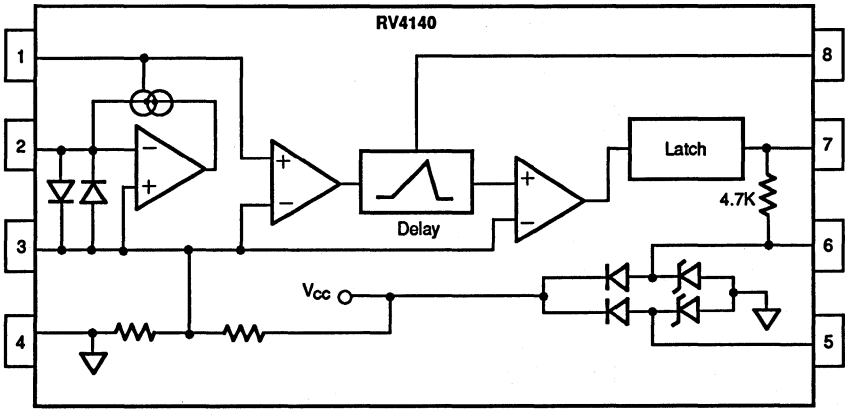
Electrical Characteristics

I line = 1.2 mA, T_A = 25°C, R_{SET} = 290 kΩ

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator (pins 5 to 6)					
Regulated Voltage	I2-3 = 11 µA	6.8	7.2	7.6	Volts
Regulated Voltage	I line = 700 µA, I2-3 = 9 µA	6.8	7.2	7.6	Volts
Sense Amplifier (pins 2 to 3)					
Offset Voltage	Design Value	-3.0	0	3.0	mV
Gain Bandwidth	Design Value		2.0		MHz
Input Bias Current	Design Value		30	100	nA
SCR Trigger (pins 7 to 6)					
Output Resistance	V5-6 = open, I2-3 = 0 µA	4.0	4.7	5.4	kΩ
Output Voltage	I2-3 = 9 µA	0	0.1	10	mV
Output Voltage	I2-3 = 11 µA	1.4	2.0	2.6	Volts
Output Current	V7-6 = 0V, I2-3 = 11 µA	300	420	600	µA
Reference Voltage (pins 3 to 4)					
Reference Voltage	I line = 700 µA	2.6	2.9	3.2	Volts
Delay Timer (pins 8 to 4)					
Delay Time (1)	C8-4 = 20 nF	—	2.0	—	ms
Delay Current	I2-3 = 11 µA	23	29	35	µA

Notes:
1. Delay time is defined as starting when the instantaneous sense current (I2-3) exceeds 2.9V/R_{SET} and ending when the SCR Trigger voltage V7-6 goes high.

Functional Block Diagram



65-4650

Principles of Operation

(Refer to Block Diagram and Figure 1)

The shunt regulator generated by a 6.5V zener diode is built into the internal bridge rectifier. It is divided to create an internal reference voltage of 2.9V connected to pin 3. The secondary of the sense transformer is AC coupled to the inverting input of the sense amplifier at pin 2; the non-inverting input is referenced to pin 3. A current feedback loop around the sense amplifier ensures a virtual ground will be presented to the secondary of the sense transformer. In this manner it acts as a current transformer instead of a voltage transformer. In this mode, the transformer's characteristics are very predictable and circuit adjustments are not necessary in production.

The sense transformer has a toroidal core made of laminated steel rings or solid ferrite material. The secondary of the transformer is 500 to 1000 turns of #40 wire wound through the toroid. The primary is one turn made by passing the AC hot and neutral wires through the center of the toroid. When a ground fault exists, a difference exists between the current flowing in hot and neutral wires. The difference primary current, divided by the number of secondary turns, flows through the secondary wire of the transformer.

The AC coupled transformer secondary current then flows through the sense amplifier's feedback loop, creating a full wave rectified version of the secondary fault current. This current passes through R_{SET} at pin 1, generating a voltage equal to R_{SET} times the peak fault current divided by the sense transformer turns ratio. This voltage is compared with the reference voltage at pin 3.

If the voltage at pin 1 is greater than pin 3, a comparator will charge C2 through a 29 μA current source at pin 8. If the voltage at pin 1 exceeds pin 3 for longer than the delay time, a 400 μA current will pulse between pins 7 and 6 which will trigger the gate of the SCR.

If the voltage at pin 1 exceeds pin 3 for less than the delay time, the SCR will not trigger.

The fault current at which the controller triggers the SCR is dependent on the value of R_{SET} and the time delay determined by C2.

UL 943 requires the circuit interrupter trip when the ground fault exceeds 6 mA and not trip when the fault current is less than 4 mA.

Supply Current Requirements

The RV4140 has a built-in diode bridge rectifier that provides power to the chip independent of the polarity of the AC line. This eliminates the external rectifier required for previous GFCI controllers.

R_{LINE} limits the shunt regulator current to 2 mA. The recommended value is 47K to 91K for 110V systems and 91K to 150K for 220V systems. The recommended maximum peak line current through R_{LINE} is 7 mA.

DO NOT connect a filter capacitor between pins 5 and 6 in an attempt to filter the supply voltage at the RV4140. Proper operation of the RV4140 requires the internal supply voltage to be unfiltered.

SCR Driver

The SCR must have a high dV/dt rating to ensure that line noise (generated by electrically noisy appliances) does not falsely trigger the SCR. Also, the SCR must have a gate drive requirement less than 200 μA. C3 is a noise filter that prevents high frequency line pulses from triggering the SCR.

The relay solenoid used should have a 3 ms or less response time to meet the UL 943 timing requirement.

Supplier of Sense Transformers and Cores

Magnetic Metals Corporation, Camden, NJ 08101, (609) 964-7842, supplies a full line of ring cores and transformers designed specifically for GFCI and related applications.

Determining the Values of R_{SET} and C2

Determine the ground fault trip current requirement. This will be typically 5 mA in North America (117 VAC) and 10 mA in the UK and Europe.

Determine the minimum amount of time delay required to prevent nuisance tripping. This will typically be 1 to 2 ms.

The value of C2 required to provide the desired delay time is:

$$C2 = 10 \times T$$

where:

C2 is in nF
T is the desired delay time in ms.

The value of R_{SET} to meet nominal ground fault trip current specification is:

$$R_{SET} = \frac{2.05 \times N}{I_{FAULT} \times \cos 180\ (T/P)}$$

Where:
R_{SET} is in kΩ
T is the time delay in ms
P is the period of the line frequency in ms

I_{FAULT} is the desired ground fault trip current in mA RMS
N is the number of sense transformer secondary turns.

This formula assumes an ideal sense transformer is used. The calculated value of R_{SET} may have to be changed up to 30% when using a non-ideal transformer.

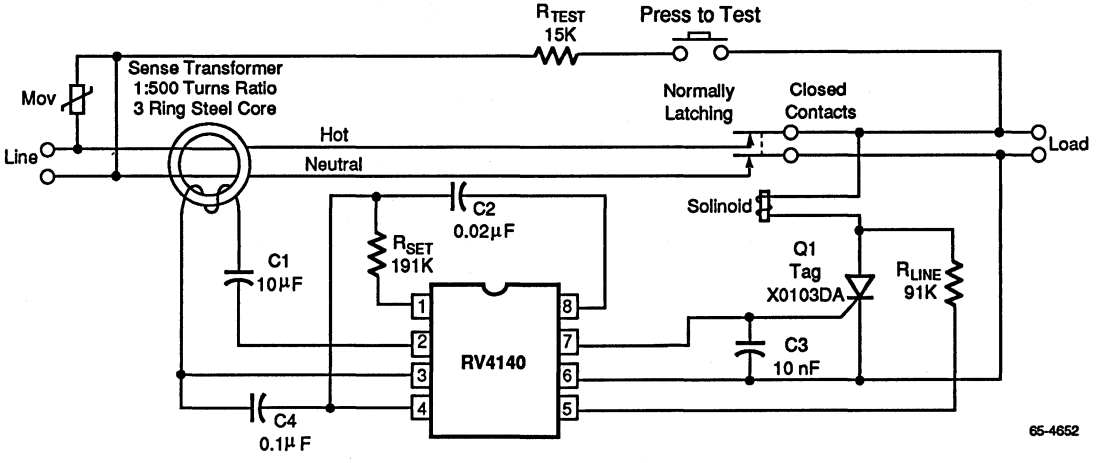
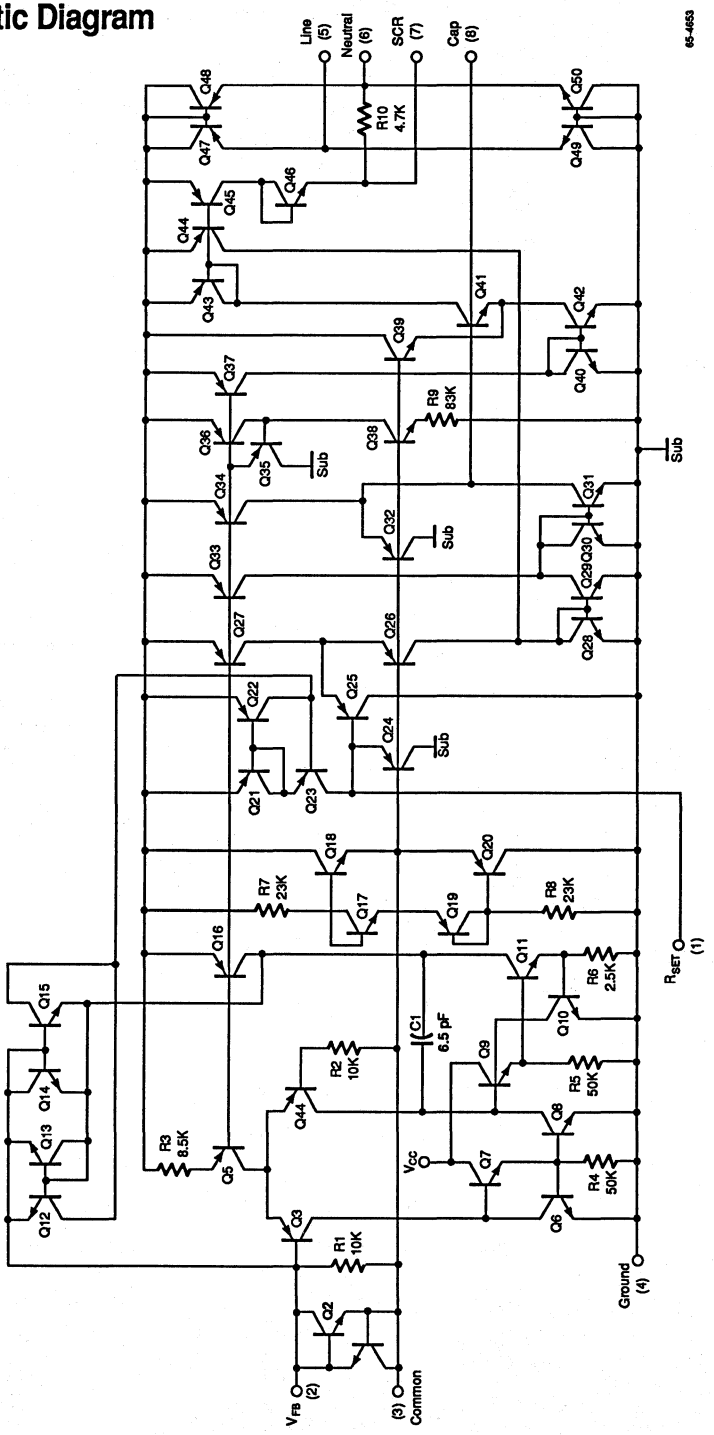


Figure 1. Appliance Leakage Detector Circuit Application

Schematic Diagram



RV4141
Low Power Ground Fault Interrupter

Description

The RV4141 is a low power controller for AC receptacle ground fault circuit interrupters. These devices detect hazardous current paths to ground and ground to neutral faults. The circuit interrupter then disconnects the load from the line before a harmful or lethal shock occurs.

Internally, the RV4141 contains a diode rectifier, shunt regulator, precision sense amplifier, current reference, time delay circuit, and SCR driver.

Two sense transformers, SCR, solenoid, three resistors and four capacitors complete the design of the basic circuit interrupter. The simple layout and minimum component count insure ease of application and long term reliability.

Features not found in other GFCI controllers include a low offset voltage sense amplifier eliminating the need for a coupling capacitor between the sense transformer and sense amplifier, and an internal rectifier to eliminate high voltage rectifying diodes.

The RV4141 is powered only during the positive half period of the line voltage, but can sense current faults independent of its phase relative to the line voltage. The gate of the SCR is driven only during the positive half cycle of the line voltage.

Features

- Powered from the AC line
- Built-in rectifier
- Direct interface to SCR
- 500 µA quiescent current
- Precision sense amplifier
- Adjustable time delay
- Minimum external components
- Meets UL 943 requirements
- For use with 110V or 220V systems
- Available in 8 pin DIP or SOIC package

RV4141

Absolute Maximum Ratings

Supply Current ..... 10 mA
Internal Power Dissipation ..... 500 mW
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature
Range ..... -35°C to +80°C
Lead Soldering Temperature
(60 Sec., DIP) ..... +300°C
(10 Sec., SO) ..... +260°C

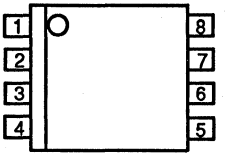
Ordering Information

Part Number	Package	Operating Temperature Range
RV4141N	N	-35°C to +80°C
RV4141M	M	-35°C to +80°C

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC

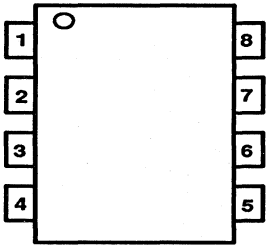
Connection Information

8-Lead Plastic
Dual In-Line SO-8
(Top View)



65-02666

8-Lead Plastic
Dial In-Line Package
(Top View)

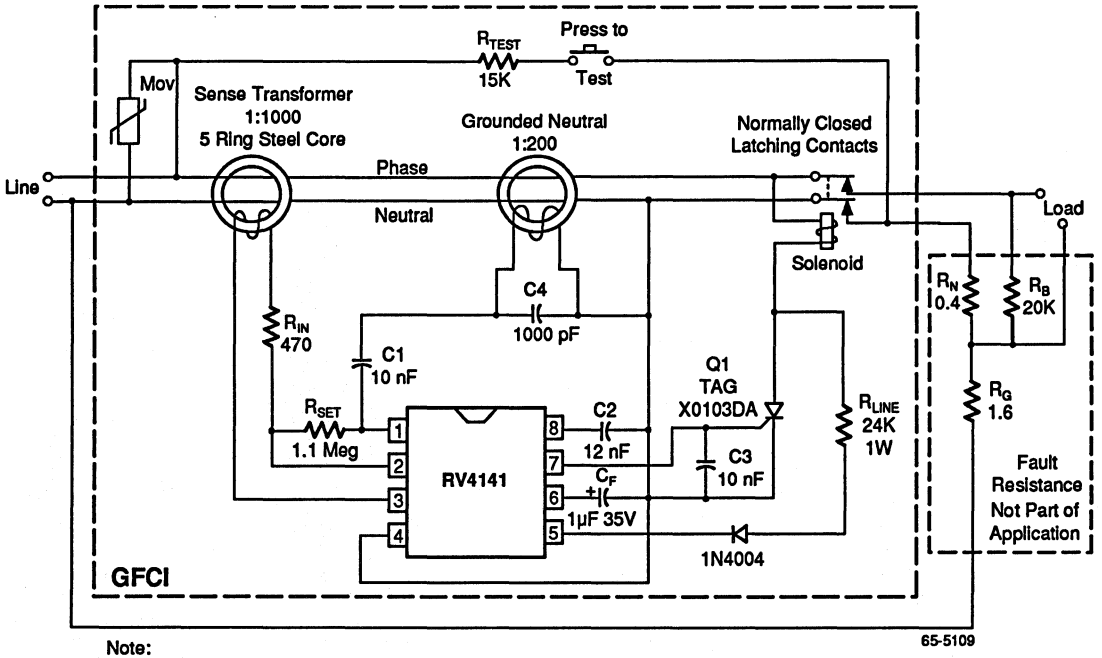


65-0093

Pin	Function
1	Amp Out
2	V_{FB}
3	V_{REF} (+13V)
4	Ground
5	Line
6	$+V_S$
7	SCR Trigger
8	Delay Cap

Thermal Characteristics

	8-Lead Plastic SOIC	8-Lead Plastic DIP
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A <50°C	300 mW	468 mW
Therm. Res θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For T_A >50°C Derate at	4.1 mW per °C	6.25 mW per °C



Note:
Portions of this schematic are subject to
U.S. patents 3,878,435 and Re. 30,678

Figure 1. GFI Application Circuit

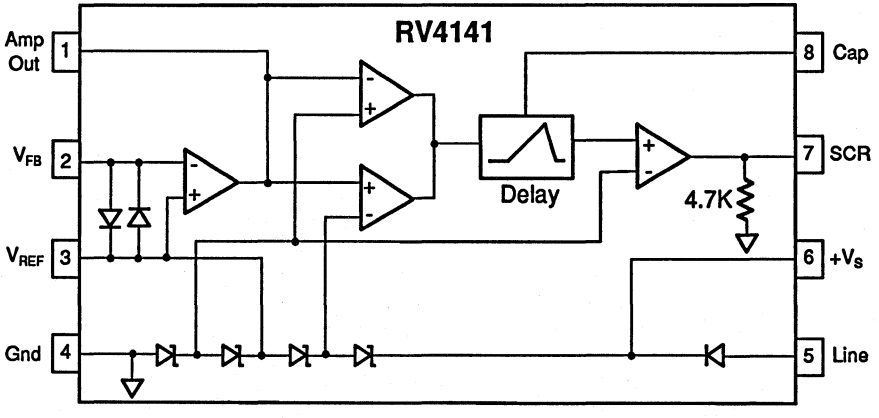
Electrical Characteristics

(I_{LINE} = 1.5 mA and T_A = +25°C, R_{SET} = 650 kΩ)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator (Pins 5 to 4)					
Regulated Voltage	I_{2-3} = 11 µA	25.0	27.0	29.0	Volts
Regulated Voltage	I_{LINE} = 750 µA, I_{2-3} = 9 µA	25.0	27.0	29.0	Volts
Quiescent Current	V_{5-4} = 24V	—	500	—	µA
Sense Amplifier (Pins 2 to 3)					
Offset Voltage		200	0	200	µV
Gain Bandwidth	(Design Value)	—	1.5	—	MHz
Input Bias Current	(Design Value)		30	100	nA
SCR Trigger (Pins 7 to 4)					
Output Resistance	V_{7-4} = Open, I_{2-3} = 0 µA	4.0	4.7	5.4	kΩ
Output Voltage	I_{2-3} = 9 µA	0	0.1	10	mV
Output Voltage	I_{2-3} = 11 µA	2.4	3.0	3.6	Volts
Output Current	V_{7-4} = 0V, I_{2-3} = 11 µA	400	600	800	µA
Reference Voltage (Pins 3 to 4)					
Reference Voltage	I_{LINE} = 750 µA	12.0	13.0	14.0	Volts
Delay Timer (Pins 8 to 4)					
Delay Time (Note 1)	C_{8-4} = 12 nF	—	2.0	—	ms
Delay Current	I_{2-3} = 11 µA	30	40	50	µA

Note:
1. Delay time is defined as starting when the instantaneous sense current (I_{2-3}) exceeds 6.5 V/R_{SET} and ending when the SCR trigger voltage V_{7-4} goes high.

Functional Block Diagram



65-5108

Circuit Operation

(Refer to Block Diagram and Figure 1)

The precision op amp connected to Pins 1 through 3 senses the fault current flowing in the secondary of the sense transformer, converting it to a voltage at Pin 1. The ratio of secondary current to output voltage is directly proportional to feedback resistor, R_{SET}.

R_{SET} converts the sense transformer secondary current to a voltage at Pin 1. Due to the virtual ground created at the sense amplifier input by its negative feedback loop, the sense transformer's burden is equal to the value of R_{IN}. From the transformer's point of view, the ideal value for R_{IN} is 0Ω. This will cause it to operate as a true current transformer with minimal error. However, making R_{IN} equal to zero creates a large offset voltage at Pin 1 due to the sense amplifier's very high DC gain. R_{IN} should be selected as high as possible consistent with preserving the transformer's operation as a true current mode transformer. A typical value for R_{IN} is between 200 and 1000Ω.

As seen by the equation below, maximizing R_{IN} minimizes the DC offset error at the sense amplifiers output. The DC offset voltage at Pin 1 contributes directly to the trip current error. The offset voltage at Pin 1 is:

$$V_{OS} \times R_{SET}/(R_{IN} + R_{SEC})$$

Where:
V_{OS} = Input offset voltage of sense amplifier
R_{SET} = Feedback resistor
R_{IN} = Input resistor
R_{SEC}= Transformer secondary winding resistance

The sense amplifier has a specified maximum offset voltage of 200 µV to minimize trip current errors.

Two comparators connected to the sense amplifier output are configured as a window detector, whose references are -6.5 volts and +6.5 volts referred to Pin 3. When the sense transformer secondary RMS current exceeds $4.6/R_{SET}$ the output of the window detector starts the delay circuit. If the secondary current exceeds the predetermined trip current for longer than the delay time a current pulse appears at Pin 7, triggering the SCR.

The SCR anode is directly connected to a solenoid or relay coil. The SCR can be tripped only when its anode is more positive than its cathode.

Supply Current Requirements

The RV4141 is powered directly from the line through a series limiting resistor called R_{LINE}, its value is between 24 kΩ and 91 kΩ. The controller IC has a built-in diode rectifier eliminating the need for external power diodes.

The recommended value for R_{LINE} is 24 kΩ to 47 kΩ for 110V systems and 47 kΩ to 91 kΩ for 220V systems. When R_{LINE} is 47 kΩ the shunt regulator current is limited to 3.6 mA. The recommended maximum peak line current through R_{LINE} is 10 mA.

GFCI Application

(Refer to Figure 1)

The GFCI detects a ground fault by sensing a difference current in the line and neutral wires. The difference current is assumed to be a fault current creating a potentially hazardous path from line to ground. Since the line and neutral wires pass through the center of the sense transformer, only the differential primary current is transferred to the secondary. Assuming the turns ratio is 1:1000 the secondary current is 1/1000th the fault current. The RV4141's sense amplifier converts the secondary current to a voltage which is compared with either of the two window detector reference voltages. If the fault current exceeds the design value for the duration of the programmed time delay, the RV4141 will send a current pulse to the gate of the SCR.

Detecting ground to neutral faults is more difficult. R_B represents a normal ground fault resistance, R_N is the wire resistance of the electrical circuit between load/neutral and earth ground. R_G represents the ground to neutral fault condition. According to UL 943, the GFCI must trip when R_N = 0.4Ω, R_G = 1.6Ω and the normal ground fault is 6 mA.

Assuming the ground fault to be 5 mA, 1 mA and 4 mA will go through R_G and R_N, respectively, causing an effective 1 mA fault current. This current is detected by the sense transformer and amplified by the sense amplifier. The ground/neutral and sense transformers are now mutually coupled by R_G, R_N and the neutral wire ground loop, producing a positive feedback loop around the sense amplifier. The newly created feedback loop causes the sense amplifier to oscillate at a frequency determined by ground/neutral transformer secondary inductance and C4. Typically it occurs at 8 KHz.

C2 is used to program the time required for the fault to be present before the SCR is triggered. Refer to the equation below for calculating the value of C2. Its typical value is 12 nF for a 2 ms delay.

R_{SET} is used to set the fault current at which the GFCI trips. When used with a 1:1000 sense transformer, its typical value is 1 MΩ for a GFCI designed to trip at 5 mA.

R_{IN} should be the highest value possible which insures a predictable secondary current from the sense transformer. If R_{IN} is set too high, normal production variations in the transformer permeability will cause unit to unit variations in the secondary current. If it is too low, a large offset voltage error at Pin 1 will be present. This error voltage in turn creates a trip current error proportional to the input offset voltage of the sense amplifier. As an example, if R_{IN} is 500Ω, R_{SET} is 1 MΩ, R_{SEC} is 45Ω and the V_{OS} of the sense amplifier is its maximum of 200 μV, the trip current error is ±5.6%.

The SCR anode is directly connected to a solenoid or relay coil. It can be tripped only when its anode is more positive than its cathode. It must have a high dV/dt rating to ensure that line noise (generated by electrically noisy appliances) does not falsely trigger it. Also the SCR must have a gate drive requirement less than 200 μA. C3 is a noise filter that prevents high frequency line pulses from triggering the SCR.

The relay solenoid used should have a response time of 3 ms or less to meet the UL 943 timing requirement.

Sense Transformers and Cores

The sense and ground/neutral transformer cores are usually fabricated using high permeability laminated steel rings. Their single turn primary is created by passing the line and neutral wires through the center of its core. The secondary is usually from 200 to 1500 turns.

Magnetic Metals Corporation, Camden, NJ 08101, (609) 964-7842 and Magnetics, 900 E. Butler Road, P.O. Box 391, Butler, PA 16003, (412) 282-8282 are full-line suppliers of ring cores and transformers designed specifically for GFCI and related applications.

Calculating The Values of R_{SET} and C2.

Determine the nominal ground fault trip current requirement. This will be typically 5 mA in North America (117V AC) and 22 mA in the UK and Europe (220V AC).

Determine the minimum delay time required to prevent nuisance tripping. This will typically be 1 to 2 ms.

The value of C2 required to provide the desired delay time is:

$$C2 = 6 \times T$$

where:

C2 is in nF
T is the desired delay time in ms.

The value of R_{SET} to meet the nominal ground fault trip current specification is:

$$R_{SET} = \frac{4.6 \times N}{I_{FAULT} \times \cos 180(T/P)}$$

Where:

R_{SET} is in kΩ
T is the time delay in ms
P is the period of the line frequency in ms
I_{FAULT} is the desired ground fault trip current in mA RMS
N is the number of sense transformer secondary turns.

This formula assumes an ideal sense transformer is used. The calculated value of R_{SET} may have to be changed up to 30% to when using a non-ideal transformer.

RV4145
Low Power Ground Fault Interrupter

Description

The RV4145 is a low power controller for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions, such as equipment (connected to opposite phases of the AC line) in contact with a pool of water and open circuits the line before a harmful or lethal shock occurs.

Contained internally are a 26V zener shunt regulator, an op amp, and an SCR driver. With the addition of two sense transformers, a bridge rectifier, an SCR, a relay, and a few additional components, the 4145 will detect and protect against both hot wire to ground and neutral wire to ground faults. The simple layout and conventional design ensure ease of application and long term reliability.

Features

- No potentiometer required
- Direct interface to SCR
- Supply voltage derived from AC line — 26V shunt
- Adjustable sensitivity
- Grounded neutral fault detection
- Meets U.L. 943 standards
- 450 μA quiescent current
- Ideal for 120V or 220V systems

RV4145

Absolute Maximum Ratings

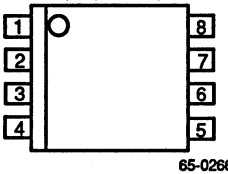
Supply Current ..... 18 mA
Internal Power Dissipation ..... 500 mW
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature
Range ..... -35°C to +85°C
Lead Soldering Temperature
(60 Sec, DIP) ..... +300°C
(10 Sec, SOIC) ..... +260°C

Thermal Characteristics

	8-Lead Plastic SOIC	8-Lead Plastic DIP
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A<50°C	300 mW	468 mW
Therm. Res θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For T_A >50°C Derate at	4.1 mW/°C	6.25 mW/°C

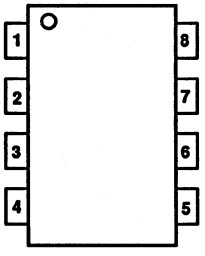
Connection Information

8-Lead Plastic
Dual In-Line SO-8
(Top View)



65-02666

8-Lead Plastic
Dual In-Line Package
(Top View)



65-0093

Pin	Function
1	V_{FB}
2	+Input
3	V_{REF} (+13V)
4	GND
5	SCR Trigger
6	$+V_S$ (+26V)
7	Op Amp Output
8	NC

Ordering Information

Part Number	Package	Operating Temperature Range
RV4145N	N	-35°C to +85°C
RV4145M	M	-35°C to +85°C

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC

Electrical Characteristics

(I_S = 1.5 mA and T_A = +25°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator					
Zener Voltage (+V_S)	Pin 6 to Pin 4	25	26	29.2	V
Reference Voltage (V_{REF})	Pin 3 to Pin 4	12.5	13	14.6	V
Quiescent Current (I_S)	+V_S = 24V		450	750	µA
Operational Amplifier					
Offset Voltage	Pin 2 to Pin 3	-3.0	0.5	+3.0	mV
+Output Voltage Swing	Pin 7 to Pin 3	6.8	7.2	8.1	V
-Output Voltage Swing	Pin 7 to Pin 3	-9.5	-11.2	-13.5	V
+Output Source Current	Pin 7 to Pin 3		650		µA
-Output Sink Current	Pin 7 to Pin 3		1.0		mA
Gain Bandwidth Product	F = 50 kHz	1.0	1.8		MHz
Detector Reference Voltage	Pin 7 to Pin 3	6.8	7.2	8.1	±V
Resistors	I_S = 0 mA				
R1	Pin 1 to Pin 3		10		kΩ
R2	Pin 2 to Pin 3		10		kΩ
R3	Pin 5 to Pin 4	4.0	4.7	5.4	kΩ
SCR Trigger Voltage	Pin 5 to Pin 4				
Detector On		1.5	2.8		V
Detector Off		0	1	10	mV

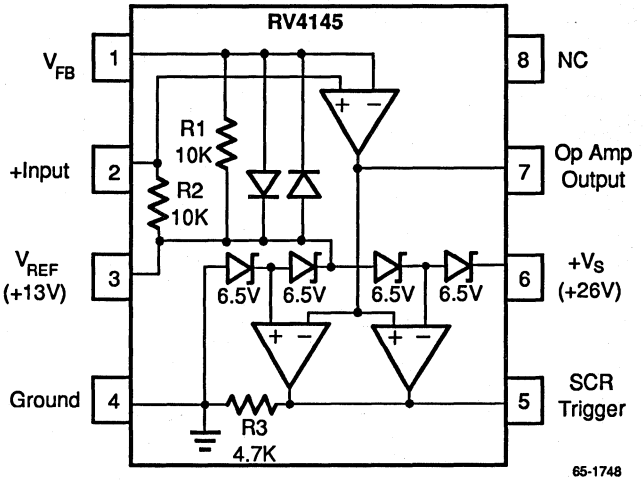
Electrical Characteristics

(I_S = 1.5 mA and -35°C ≤ T_A ≤ +85°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator					
Zener Voltage (+V_S)	Pin 6 to Pin 4	24	26	30	V
Reference Voltage (V_{REF})	Pin 3 to Pin 4	12	13	15	V
Quiescent Current (I_S)	+V_S = 23V		500		µA
Operational Amplifier					
Offset Voltage	Pin 2 to Pin 3	-5.0	0.5	+5.0	mV
+Output Voltage Swing	Pin 7 to Pin 3	6.5	7.2	8.3	V
-Output Voltage Swing	Pin 7 to Pin 3	-9	-11.2	-14	V
Gain Bandwidth Product	F = 50 kHz		1.8		MHz
Detector Reference Voltage	Pin 7 to Pin 3	6.5	7.2	8.3	±V
Resistors	I_S = 0 mA				
R1	Pin 1 to Pin 3		10		kΩ
R2	Pin 2 to Pin 3		10		kΩ
R3	Pin 5 to Pin 4	3.8	4.7	5.6	kΩ
SCR Trigger Voltage	Pin 5 to Pin 4				
Detector On		1.3	2.8		V
Detector Off		0	3	50	mV

RV4145

Functional Block Diagram



Principles of Operation

The 26V shunt regulator voltage generated by the string of zener diodes is divided into three reference voltages: 3/4 V_S, 1/2 V_S, and 1/4 V_S. V_{REF} is at 1/2 V_S and is used as a reference to create an artificial ground of +13V at the op amp non-inverting input.

Figure 1 shows a three-wire 120V AC outlet GFI application using a 4145. Fault signals from the sense transformer are AC coupled into the input and are amplified according to the following equation:

$$V_7 = R_{SENSE} \times I_{SENSE}/N$$

Where V_7 is the RMS voltage at pin 7 relative to pin 3, R_{SENSE} is the value of the feedback resistor connected from pin 7 to pin 1, I_{SENSE} is the fault current in amps RMS and N is the turns ratio of the sense transformer. When V_7 exceeds plus or minus 7.2V relative to pin 3 the SCR Trigger output will go high and fire the external SCR.

The formula for V_7 is approximate because it does not include the sense transformer characteristics.

Grounded neutral fault detection is accomplished when a short or fault closes a magnetic path between the sense transformer and the grounded neutral transformer. The resultant AC coupling closes a positive feedback path around the op amp, and therefore the op amp oscillates. When the peaks of the oscillation voltage exceed the SCR trigger comparator thresholds, the SCR output will go high.

Shunt Regulator

R_{LINE} limits the current into the shunt regulator; 220V applications will require substituting a 47 kΩ 2W resistor. In addition to supplying power to the IC, the shunt regulator creates internal reference voltages (see above).

Operational Amplifier

R_{SENSE} is a feedback resistor that sets gain and therefore sensitivity to normal faults. To adjust R_{SENSE} follow this procedure: apply the desired fault current (a difference in current of 5 mA is the UL 943 standard). Adjust R_{SENSE} upward until the SCR activates. A fixed resistor can be used for R_{SENSE}, since the resultant ±15% variation in sensitivity will meet UL's 4-6 mA specification window.

The roll-off frequency is greater than the grounded neutral fault oscillation frequency, in order to preserve loop gain for oscillation (which is determined by the inductance of the 200:1 transformer and C4).

The sensitivity to grounded neutral faults is adjusted by changing the frequency of oscillation. Increasing the frequency reduces the sensitivity by reducing the loop gain of the positive feedback circuit. As frequency increases, the signal becomes attenuated and the loop gain decreases. With the values shown the circuit will detect a grounded neutral fault having resistance of 2Ω or less.

The inputs to the op amp are protected from overvoltage by back-to-back diodes.

SCR Driver

The SCR used must have a high dV/dt rating to ensure that line noise (generated by noisy appliances such as a drill motor) does not falsely trigger the SCR. Also, the SCR must have a gate drive requirement of less than 200 µA. C_F is a noise filter capacitor that prevents narrow pulses from firing the SCR.

The relay solenoid used should have a 3 ms or less response time in order to meet the UL 943 timing requirement.

Sense Transformers and Cores

The sense and grounded neutral transformer cores are usually fabricated using high permeability laminated steel rings. Their single turn primary is created by passing the line and neutral wires through the center of its core. The secondary is usually from 200 to 1500 turns.

Magnetic Metals Corporation, Camden, NJ 08101, (609) 964-7842 and Magnetics, 900 E. Butler Road, P.O. Box 391, Butler, PA 16003, (412) 282-8282 are full line suppliers of ring cores and transformers designed specifically for GFI applications.

Two-Wire Application Circuit

Figure 2 shows the diagram of a 2-wire 120V AC outlet GFI circuit using a 4145. This circuit is not designed to detect grounded neutral faults. Thus, the grounded neutral transformer and capacitors C3 and C4 of Figure 1 are not used.

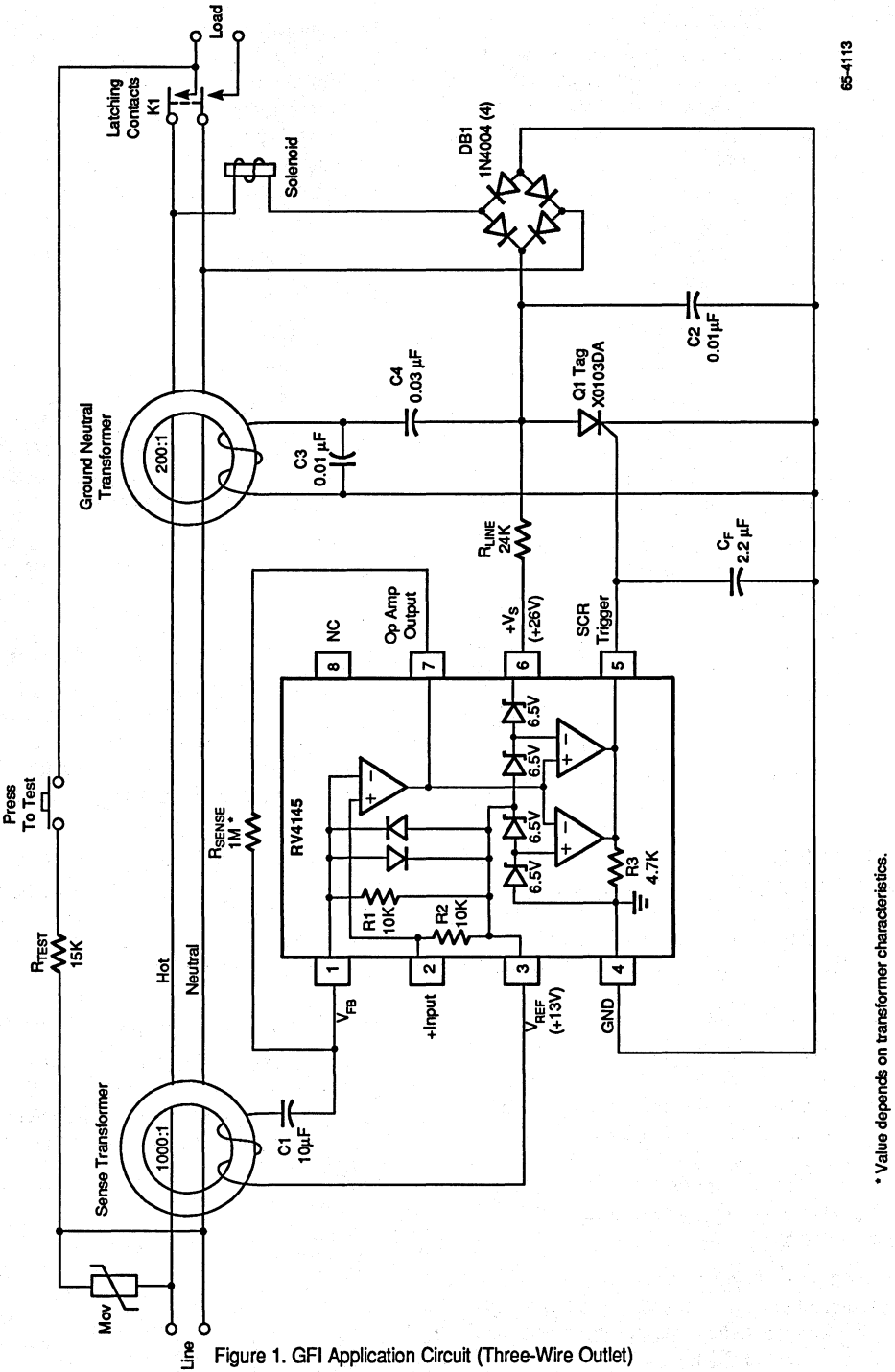


Figure 1. GFI Application Circuit (Three-Wire Outlet)

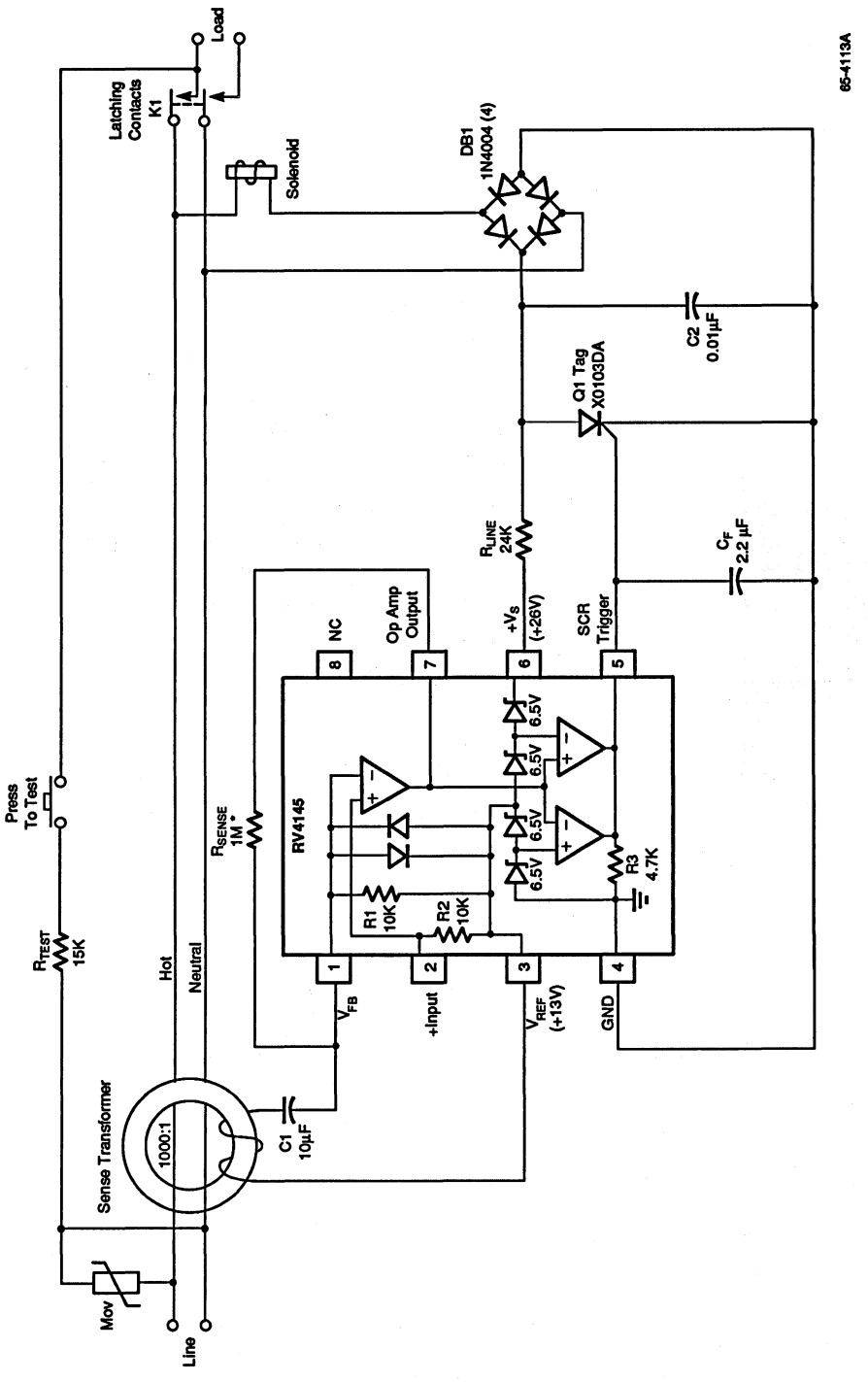
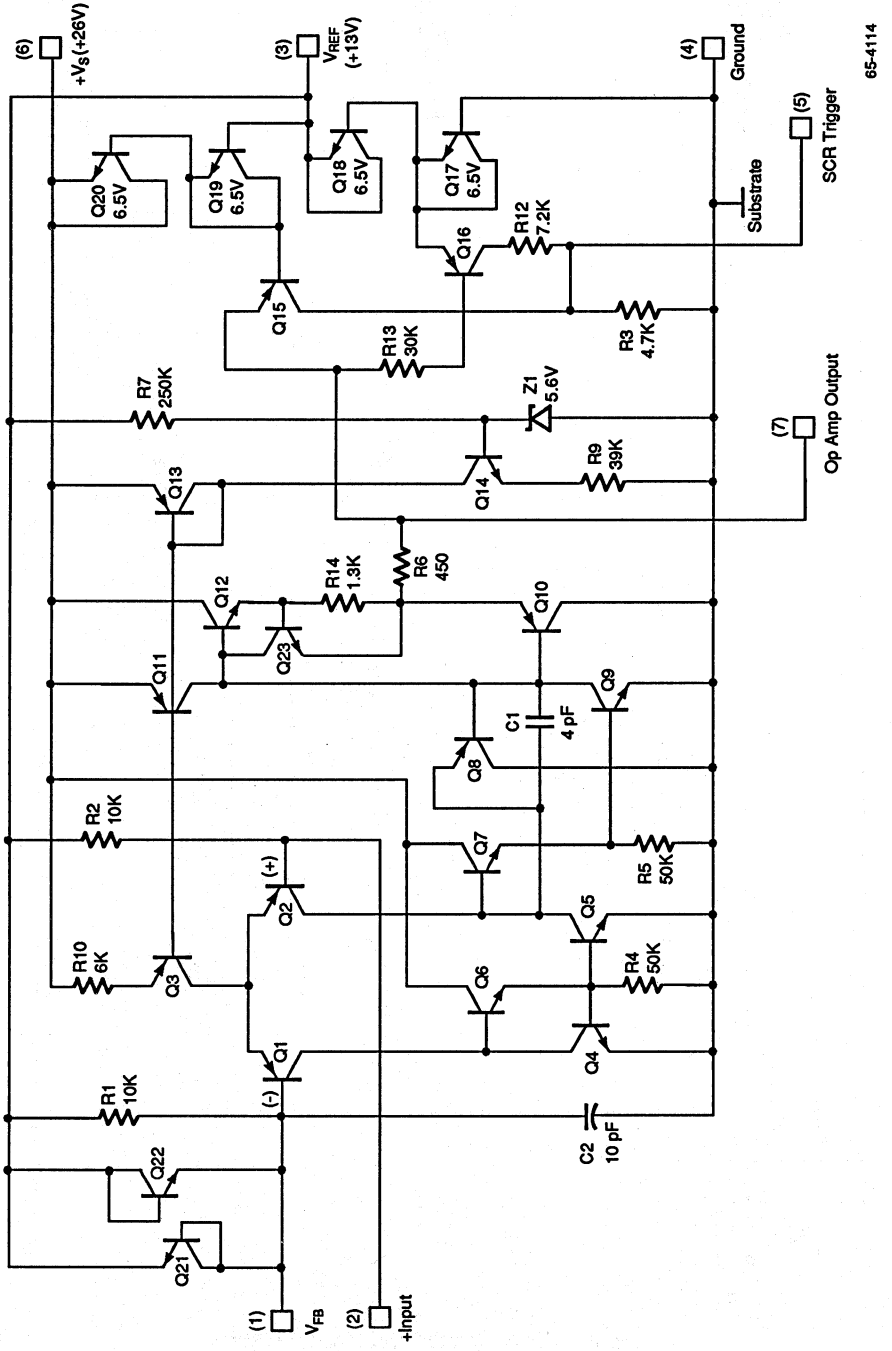


Figure 2. GFI Application Circuit (Two-Wire Outlet)

RV4145

Schematic Diagram



LM1851
Ground Fault Interrupter

Description

The LM1851 is a controller for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions (example: a pool of water and electrical equipment connected to opposite phases of the AC line) in consumer and industrial environments. The output of the IC triggers an external SCR, which in turn opens a relay circuit breaker to prevent a harmful or lethal shock.

Full advantage of the U.S. UL943 timing specification is taken to ensure maximum immunity to false triggering due to line noise. A special feature is found in circuitry that rapidly resets the integrating timing capacitor in the event that noise pulses introduce unwanted charging currents. Also, flip-flop is included that ensures firing of even a slow circuit breaker relay on either half- cycle of the line voltage when external full wave rectification is used.

The application circuit can be configured to detect both normal faults (hot wire to ground) and grounded neutral faults.

Features

- No potentiometer required
- Direct interface to SCR
- Supply voltage derived from AC line — 26V shunt
- Adjustable sensitivity
- Grounded neutral fault detection
- Meets UL943 standards
- 450 µA quiescent current
- Ideal for 120V or 220V systems

Absolute Maximum Ratings

Supply Current ..... 19 mA
Power Dissipation ..... 570 mW
Operating Temperature Range ..... -40°C to +70°C
Operating Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature (SO-8, 10 sec) ..... +260°C
Lead Soldering Temperature (DIP, 60 sec) ..... +300°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Small Outline
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A<50°C	468 mW	300 mW
Therm. Res θ_{JC}	—	—
Therm. Res. θ_{JA}	160°C/W	240°C/W
For T_A >50°C	6.25 mW/	4.17 mW/
Derate at	°C	°C

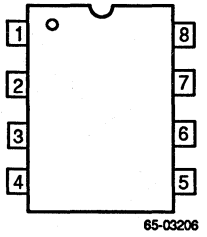
Ordering Information

Part Number	Package	Operating Temperature Range
LM1851N	N	-40°C to +70°C
RV4145M	M	-40°C to +70°C

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC

Connection Information

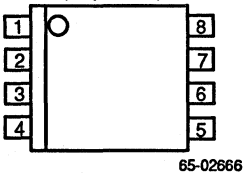
8-Lead Dual In-Line Package (Top View)



65-03206

Pin	Function
1	SCR Trigger
2	- Input
3	+ input
4	Ground
5	Amp Out
6	R_{SET}
7	C_T
8	$+V_S$

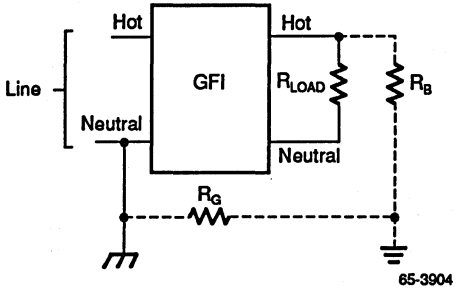
8-Lead Plastic Dual In-Line SO-8 (Top View)



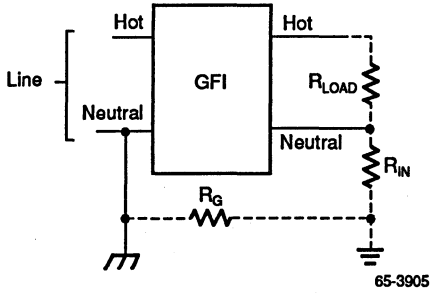
65-02666

Definition of Terms

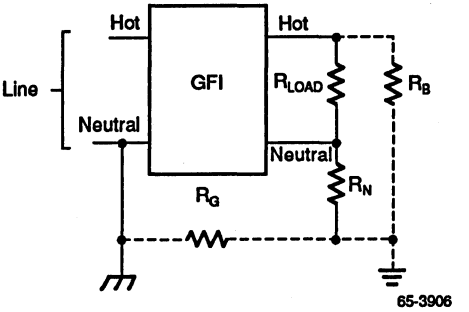
Normal Fault: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.



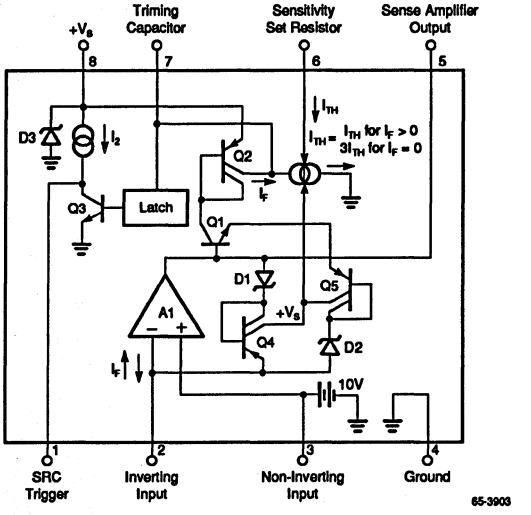
Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.



Normal Fault Plus Grounded Neutral Fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.



Functional Block Diagram



DC Electrical Characteristics

(T_A = +25°C, I_{SHUNT} = 5 mA)

Parameters	Test Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1 With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1 Without Fault		100	240	mV
Output Saturation Resistance	Pin 1 Without Fault		100		Ω
Output External Current Sinking Capability	Pin 1 Without Fault, V_{PIN1} Held to 0.3V[3]	2	5		mA
Noise Integration Sink Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault Fault and Fault Conditions	2.0	2.8	3.6	µA/µA

AC Electrical Characteristics

(T_A = +25°C, I_{SHUNT} = 5 mA)

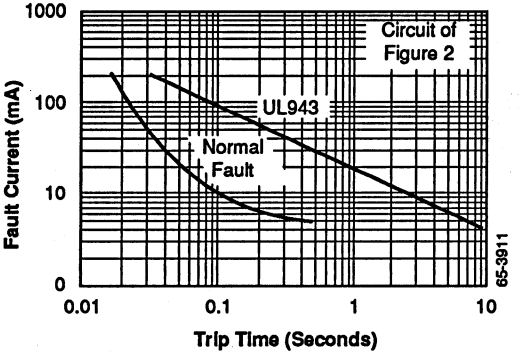
Parameters	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity	See Figure 1 [2]	3	5	7	mA
Normal Fault Trip Time	500Ω Fault (see Fig. 2) [1]		18		mS
Normal Fault With Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral (see Fig. 2) [1]		18		mS

Notes:
1. Average of 10 trials.
2. Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity will be necessary.
3. This externall applied current is in addition to the internal "output drive current" source.

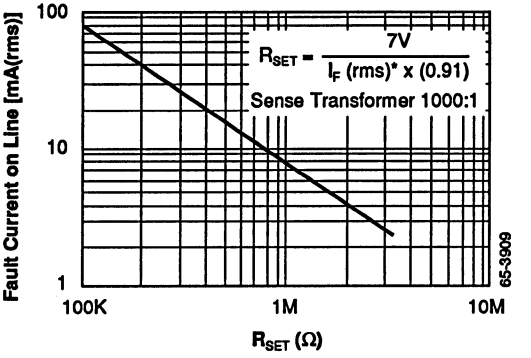
Typical Performance Characteristics

(T_A = +25°C)

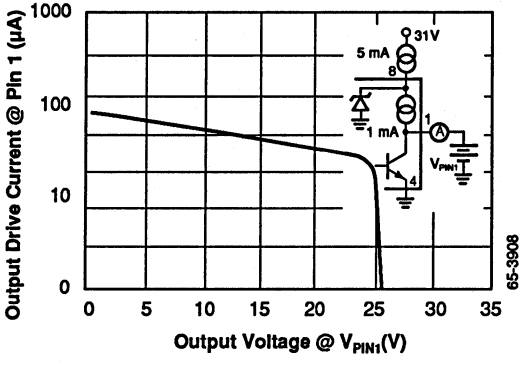
Average Trip Time vs. Fault Current



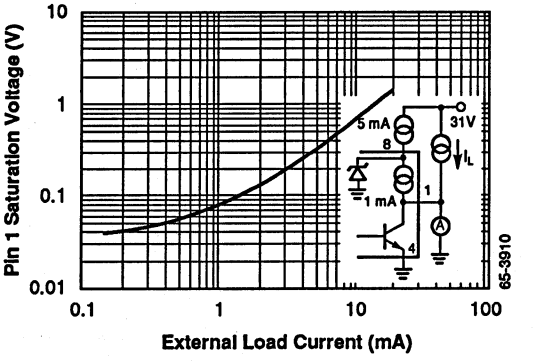
Normal Fault Current Threshold vs. R_{SET}



Output Drive Current vs. Output Voltage



Pin 1 Saturation Voltage vs. External Load Current, I_L



Linear

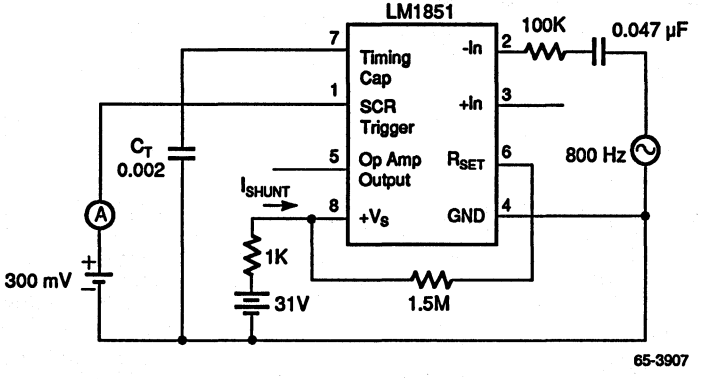


Figure 1. Normal Fault Sensitivity Test Circuit

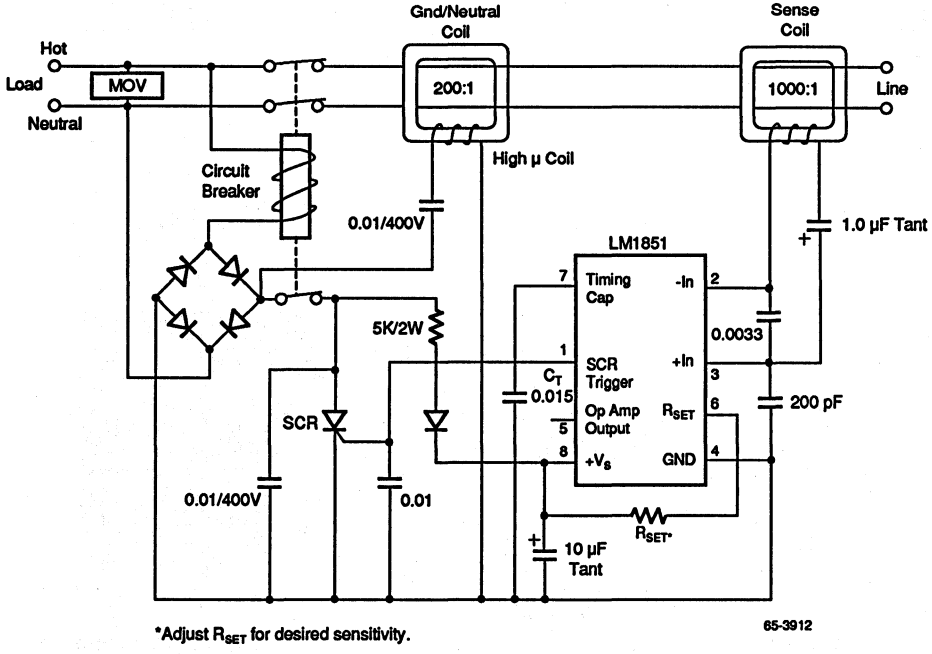


Figure 2. 120 Hz Neutral Transformer Application

Principles of Operation

(Refer to Functional block Diagram)

The voltage at the supply pin is clamped to +26V by the internal shunt regulator D3. This shunt regulator also generates an artificial ground voltage for the noninverting input of A1 (shown as a +10V source). A1, Q1, and Q2 act as a current mirror for fault current signals (which are derived from an external transformer). When a fault signal is present, the mirrored current charges the external timing capacitor until its voltage exceeds the latch trigger threshold (typically 17.5V). When then this threshold is exceeded, the latch engages and Q3 turns off, allowing I_2 to drive the SCR connected to pin 1.

Extra Circuitry in the feedback path of A1 works with the switched current source I_1 to remove any charge on C_T induced by noise in the transformer. If no fault current is present, then I_1 discharges C_T with a current equal to 3 I_{TH}, where I_{TH} is the value of current set by the external R_{SET} resistor. If fault signals are present at the input of A! (which is held at virtual ground, +10V), one of the two current mirrors in the feedback path of A1 (Q4 and Q5) will become active, depending on which half-cycle the fault occurs in. This action will raise the voltage at V_S, switching I_1 to a value equal to I_{TH}, and reducing the discharge rate of C_T to better allow fault currents to charge it.

Notice that I_{TH} discharges C_T during both half-cycles of the line, while I_F only charges C_T during the half-cycle in which I_F exits pin 2 (since Q1 will only carry fault current in one direction). Thus, during one half-cycle, I_F-I_{TH} charges C_T, while during the other half-cycle I_{TH} discharges it.

Application Circuit

A typical ground fault interrupter circuit is shown in Figure 2. It is designed to operate on 120 VAC line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the dc power required by the IC. A 1μF capacitor at pin 8 used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load.

At this time no fault current flows and the C_T discharge current increases from I_{TH} to 3I_{TH} (see Block Diagram). This quickly resets both the timing capacitor and the output latch. The circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the got and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH} = \frac{7V}{R_{SET}} \div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH} = \frac{I_F\,(rms)}{2} \times 0.91 \qquad (2)$$

Where I_F(rms) is the rms input fault current to the operational amplifier and the factor of 2 is due to the fact that IF charges the timing capacitor only during one half-cycle, while ITH discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have:

$$R_{SET} = \frac{7V}{I_F\,(rms) \times 0.91} \qquad (3)$$

For example, to obtain 5 mA(rms) sensitivity for the circuit in Figure 2 we have:

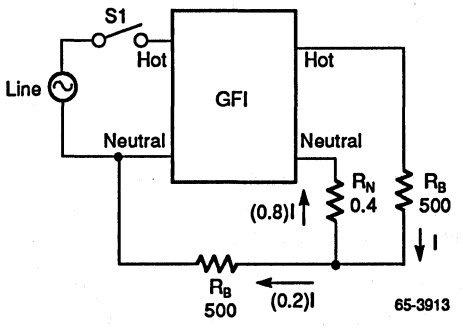
$$R_{SET} = \frac{7V}{\frac{5\,mA \times 0.91}{1000}} = 1.5\,M\Omega \qquad (4)$$

Linear

The correct value for RSET can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of RSET depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA to 6mA, provision should be made to adjust R_{SET} with a potentiometer.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_T. Due to the large number of variables involved, proper selection of C_T is best done empirically. The following design example should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GFI start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagrammatically below.



UL943 specifies ≤ 25 ms average trip time under these conditions. Calculation of CT based upon charging currents due to normal fault only is as follows:

- Start with a ≤ 25 ms specification. Subtract 3 ms GFI turn-on time (15k and 1 µF). Subtract 8 ms potential loss of one half-cycle due to fault current sense of half-cycles only.
- Subtract 4 ms time required to open a sluggish circuit breaker.
- This gives a total ≤ 10 ms maximum integration time that could be allowed.
- To generate 8 ms value of integration time that accommodates component tolerances and other variables:

$$C_T = \frac{1 \times T}{V} \qquad (5)$$

where T = integration time
V = threshold voltage
I = average fault current into C_T

$$I = \underbrace{\left(\frac{120\ V_{AC(rms)}}{R_B}\right)}_{\text{heavy fault current generated (swamps } I_{TH})} \underbrace{\left(\frac{RN}{RG + RN}\right)}_{\text{portion of fault current shunted around GFI}}$$

$$\times \underbrace{\left(\frac{1\ \text{turn}}{1000\ \text{turns}}\right)}_{\text{current division of input sense transformer}} \times \underbrace{\left(\frac{1}{2}\right)}_{\text{CT charging on half-cycles only}} \times \underbrace{(0.91)}_{\text{rms to average conversion}} \qquad (6)$$

therefore:

$$C_T = \frac{\left[\left(\frac{120}{500}\right) \times \left(\frac{0.4}{1.6 + 0.4}\right) \times \left(\frac{1}{1000}\right) \times \left(\frac{1}{2}\right) \times (0.91)\right] \times 0.008}{17.5}$$

$$CT = 0.01\ \mu F \qquad (7)$$

In practice, the actual value of C_T will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C_T.

For UL943 requirements, 0.015 µF has been found to be the best compromise between timing and noise.

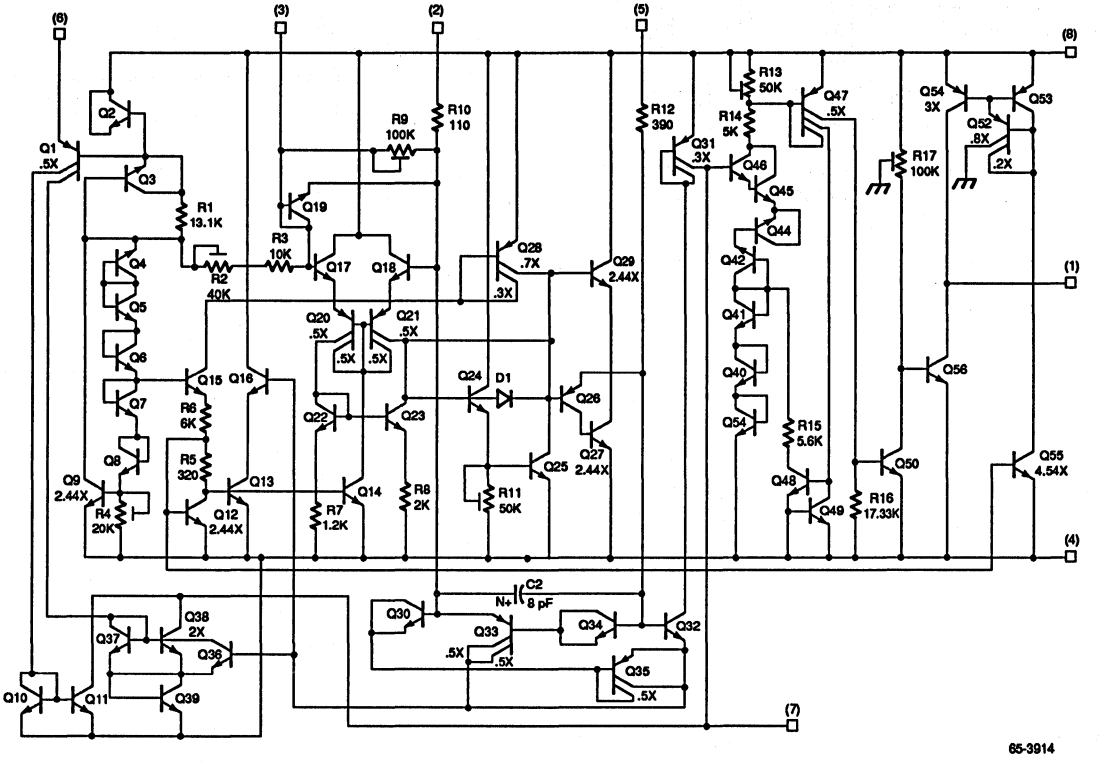
For those GFI standards not requiring grounded neutral detection, a still larger value capacitor can be used and better noise immunity obtained.

The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In Figure 2, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Transformers may be obtained from Magnetic Metals, Inc., 21st Street and Hayes Street, Camden, NJ 08101 — (609) 964-7842.

Schematic Diagram



RM2207
Voltage Controlled Oscillator

Description

The RM2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK and sweep or tone generation as well as for phase-locked loop applications.

As shown in the Block Diagram, the circuit is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and squarewave outputs. The internal switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The RM2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

Features

- Excellent temperature stability — 20 ppm/°C
- Linear frequency sweep
- Adjustable duty cycle — 0.1% to 99.9%
- Two or four level FSK capability
- Wide sweep range — 1000:1 min.
- Logic compatible input and output levels
- Wide supply voltage range — ±4V to ±13V
- Low supply sensitivity ± 0.15%/V
- Wide frequency range — 0.01 Hz to 1 MHz
- Simultaneous triangle and squarewave outputs

Applications

- FSK generation
- Voltage and current-to-frequency conversion
- Stable phase-locked loop
- Waveform generation triangle, sawtooth, pulse, squarewave
- FM and sweep generation

Absolute Maximum Ratings

Supply Voltage ..... +26V
Storage Temperture Range ..... -65°C to +150°C
Operating Temperature Range ..... -55°C to +125°C
Lead Soldering Temperature ..... +300°C
(60 sec)

Thermal Characteristics

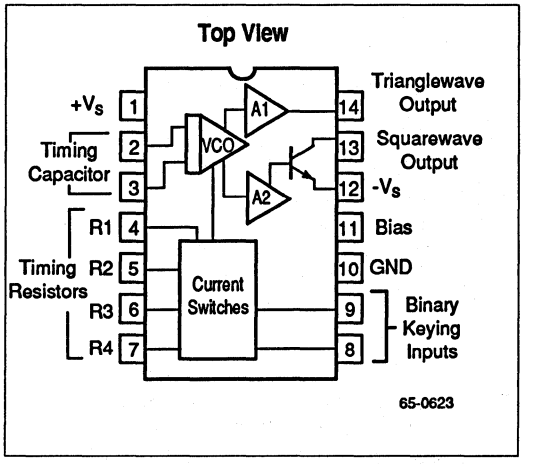
	14-Lead Ceramic DIP
Max. Junction Temp.	+175°C
Max. P_D T_A < 50°C	1042 mW
Therm. Res θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A > 50°C Derate at	8.33 mW/°C

Ordering Information

Part Number	Package	Operating Temperature Range
RM2207D	D	-55°C to +125°C
RM2207D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
D = 14-Lead Ceramic DIP

Connection Information



Electrical Characteristics

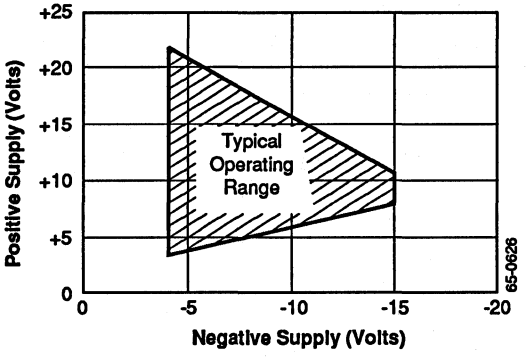
(Test Circuit of Figure 1, $V_S = \pm 6V$, $T_A = +25°C$, C = 5000 pF, R1 = R2 = R3 = R4 = 20 kΩ, R_L = 4.7 kΩ, binary inputs grounded, S1 and S2 closed unless otherwise specified)

Parameters	Test Conditions	Min	Typ	Max	Units
General Characteristics					
Supply Voltage	See Typical Performance				
Single Supply	Characteristics	+8.0	+12	+26	V
Split Supplies		±4	±6	±13	V
Supply Current	Measured at pin 1,				
Single Supply	S1 open (See Fig. 2)		5.0	7.0	mA
Split Supplies	Measured at pin 1,				
Positive	S1 open (See Fig. 1)		5.0	7.0	mA
Negative	Measured at pin 12, S1, S2 open		4.0	6.0	mA
Binary Keying Inputs					
Switching Threshold	Measured at pins 8 and 9. Refer to pin 10.	1.4	2.2	2.8	V
Input Resistance			5.0		kΩ
Oscillator Section — Frequency Characteristics					
Upper Frequency Limit	C = 500 pF, R3 = 2 kΩ	0.5	1.0		MHz
Lower Practical Frequency	C = 50 µF, R3 = 2 kΩ		0.01		Hz
Frequency Accuracy			±1.0	±3.0	% of f_0
Frequency Matching			0.5		% of f_0
Frequency Stability					
vs. Temperature (Note 1)	$0°C < T_A < +75°C$		20	50	ppm/°C
vs. Supply Voltage			0.15		%/V
Sweep Range	R3 = 1.5 kΩ for f_H R3 = 2 MΩ for f_L	1000:1	3000:1		f_H/f_L
Sweep Linearity	C = 5000 pF				
10:1 Sweep	f_H = 10 kHz, f_L = 1 kHz		1.0	2.0	%
1000:1 Sweep	f_H = 100 kHz, f_L = 100 Hz		5.0		%
FM Distortion	±10% FM Deviation		0.1		%
Recommended Range of Timing Resistors	See Characteristic Curves	1.5		2000	kΩ
Impedance at Timing Pins	Measured at pins 4, 5, 6, or 7		75		Ω
DC Level at Timing Terminals			10		mV
Output Characteristics					
Triangle Output	Measured at pin 14				
Amplitude		4	6		V_{P-P}
Impedance			10		Ω
DC Level	Referenced to pin 10		+100		mV
Linearity	from 10% to 90% of swing		0.1		%
Squarewave Output	Measured at pin 13,				
Amplitude	S2 Closed	11	12		V_{P-P}
Saturation Voltage	Referenced to pin 12		0.2	0.4	V
Rise Time	$C_L \leq 10$ pF		200		ns
Fall Time	$C_L \leq 10$ pF		20		ns

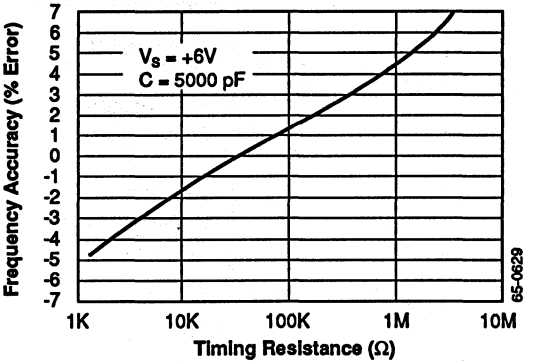
Note: 1. Guaranteed by design.

Typical Performance Characteristics

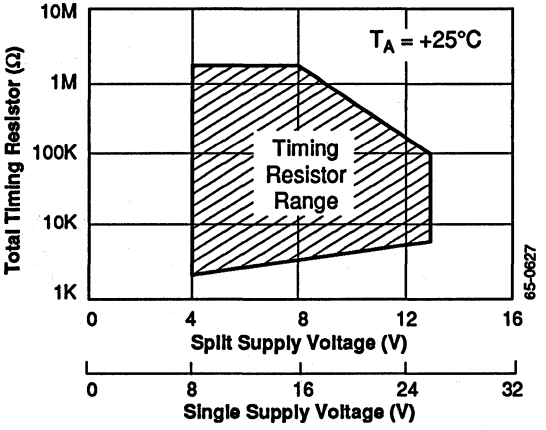
Typical Operating Range for Split Supply Voltage



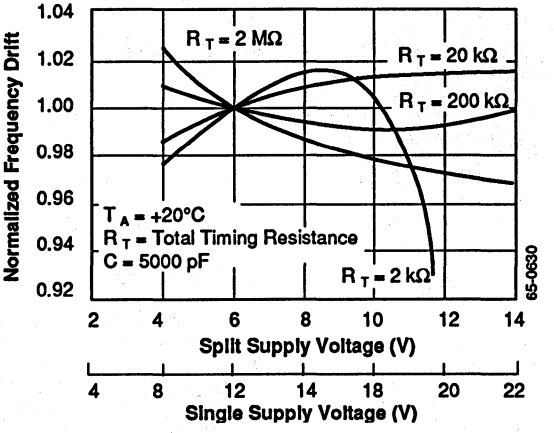
Frequency Accuracy vs. Timing Resistance



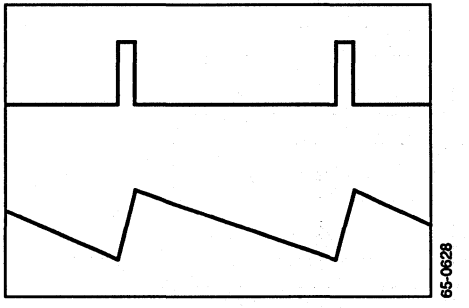
Recommended Timing Resistor Value vs. Power Supply Voltage*



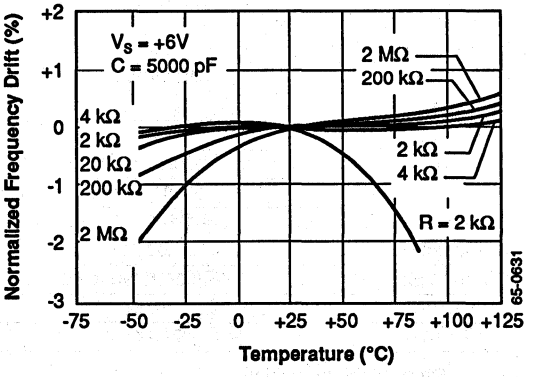
Normalized Frequency Drift vs. Supply Voltage



Pulse and Sawtooth Outputs



Normalized Frequency Drift vs. Temperature



*R_T = Parallel combination of activated timing resistors

Description of Circuit Controls

Timing Capacitor (pins 2 and 3)
The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100 pF to 100 µF. The capacitor should be non-polarized.

Timing Resistors (pins 4, 5, 6 and 7)
The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 1.5 kΩ to 2 MΩ; however, for optimum temperature and power supply stability, recommended values are 4 kΩ to 200 kΩ. To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noise environments, unused or deactivated timing terminals should be bypassed to ground through 0.1 µF capacitors. Otherwise, they may be left open.

Supply Voltage (pins 1 and 12)
The RM2207 is designed to operate over a power supply range of ±4V to ±13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced. Performance is optimum for ±6V, or 12V single supply operation.

Binary Keying Inputs (pins 8 and 9)
The internal impedance at these pins is approximately 5 kΩ. Keying levels are <1.4V for "zero" and > 3V for "one" logic levels referenced to the DC voltage at pin 10.

Bias for Single Supply (pin 11)
For single supply operations, pin 11 should be externally biased to a potential between $+V_S/3$ and $+V_S/2$ (see Figure 2). The bias current at pin 11 is nominally 5% of the total oscillation timing current I_T.

Ground (pin 10)
For split supply operation, this pin serves as circuit ground. For single supply operation, pin 10 should be AC grounded through a 1 µF bypass capacitor. During split supply operation, a ground current of 2 I_T flows out of this terminal, where I_T is the total timing current.

Squarewave Output (pin 13)
The squarewave output at pin 13 is an "open-collector" stage capable of sinking up to 20 mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1 kΩ to 10 kΩ.

Trianglewave Output (pin 14)
The output at pin 14 is a trianglewave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a very low output impedance of 10Ω and is internally protected against short circuits.

Note: Triangle waveform linearity is sensitive to parasitic coupling between the square and the trianglewave outputs (pins 13 and 14). In board layout or circuit wiring, care should be taken to minimize stray wiring capacitance between these pins.

Operating Instructions

Precautions

The following precautions should be observed when operating the RM2207 family of integrated circuits:

1. Pulling excessive current from the timing terminals will adversely affect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the total current drawn from pins 4, 5, 6 and 7 be limited to <6 mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10 mA.
2. Terminals 2, 3, 4, 5, 6 and 7 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
3. The keying logic pulse amplitude should not exceed the supply voltage.

Split Supply Operation

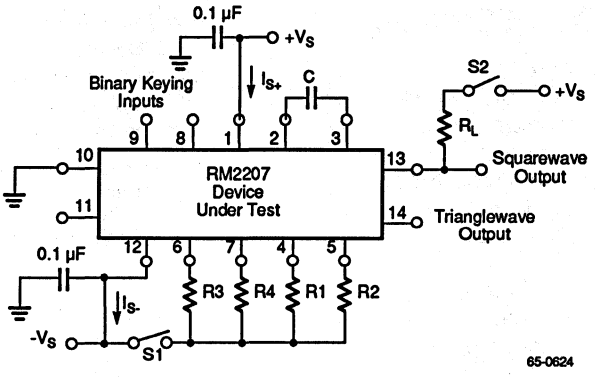
Figure 1 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R1 through R4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in Table 1. If a single timing resistor activated, the frequency is 1/RC.

Table 1. Logic Table for Binary Keying Controls

Logic Level		Selected Timing Pins	Frequency	Definitions
8	9			
0	6	f_1	$f_1 = 1/R3C$,	$\Delta f_1 = 1/R4C$
0	1	6 & 7	$f_1 + \Delta f_1$	$f_2 = 1/R2C$, $\Delta f_2 = 1/R1C$
1	0	5	f2	Logic levels: 0 = Ground
14	& 5	f2 + fΔ2	Logic levels:	1 = ≥3V

Note: For single supply operation, logic levels are referenced to voltage at pin 10.

Linear



Note: This circuit is for Bench Tests only. DC testing is normally performed with automated test equipment using an equivalent circuit.

Figure 1. Test Circuit for Split Supply Operation

Otherwise, the frequency is either 1/(R1| |R2)C or 1/(R1| |R4)C.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5 kΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of $+V_S/2$.

The circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs with ±6V supplies.

Single Supply Operation

The circuit should be interconnected as shown in Figure 2 for single supply operation. Pin 12 should be grounded, and pin 11 biased from $+V_S$ through a resistive divider to a value of bias voltage between $+V_S/3$ and $+V_S/2$. Pin 10 is bypassed to ground through a 0.1 µF capacitor.

For single supply operation, the DC voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B, the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

On-Off Keying

The RM2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1 Hz) residual oscillation in the "off" state due to internal bias current. If this effect is undesirable, it can be eliminated by connecting a 10 MΩ resistor from pin 3 to $+V_S$.

Frequency Control (Sweep and FM)

The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pins 4, 5, 6 or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C as shown in Figure 3.

For split supply operation, a *negative* control voltage, V_C, applied to the circuit of Figure 3 causes the total timing current, I_T, and the frequency, to increase.

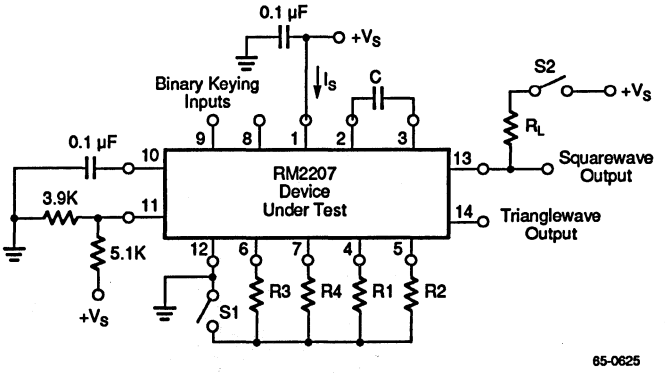
As an example, in the circuit of Figure 3, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation is determined by:

$$f = \frac{1}{R3C_B}\left[1 - \frac{V_C R3}{(R_C)(-V_S)}\right] \text{Hz}$$

Pulse and Sawtooth Operation

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the squarewave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.



Fgure 2. Test Circuit for Single Supply Operation

Figure 4 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0,0" and the "1,0" logic states given in Table 1. Timing pin 5 is activated when the output is "high", and pin 6 is activated when the squarewave output goes to a "low" state.

The duty cycle of the output waveforms is given as:

$$\text{Duty Cycle} = \frac{R2}{R2 + R3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R2 + R3}\right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R2 and R3 to a common control voltage V_C instead of to $-V_S$. The sawtooth and the pulse output waveforms are shown in the Typical Performance Characteristics Graphs.

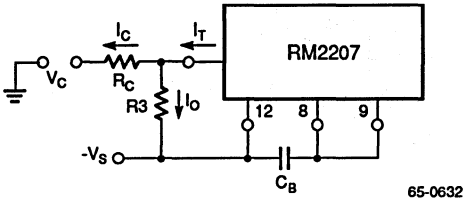


Figure 3. Frequency Sweep Operation

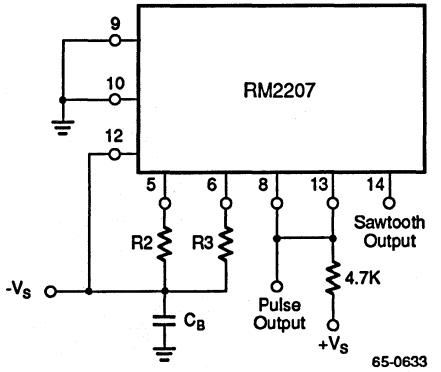
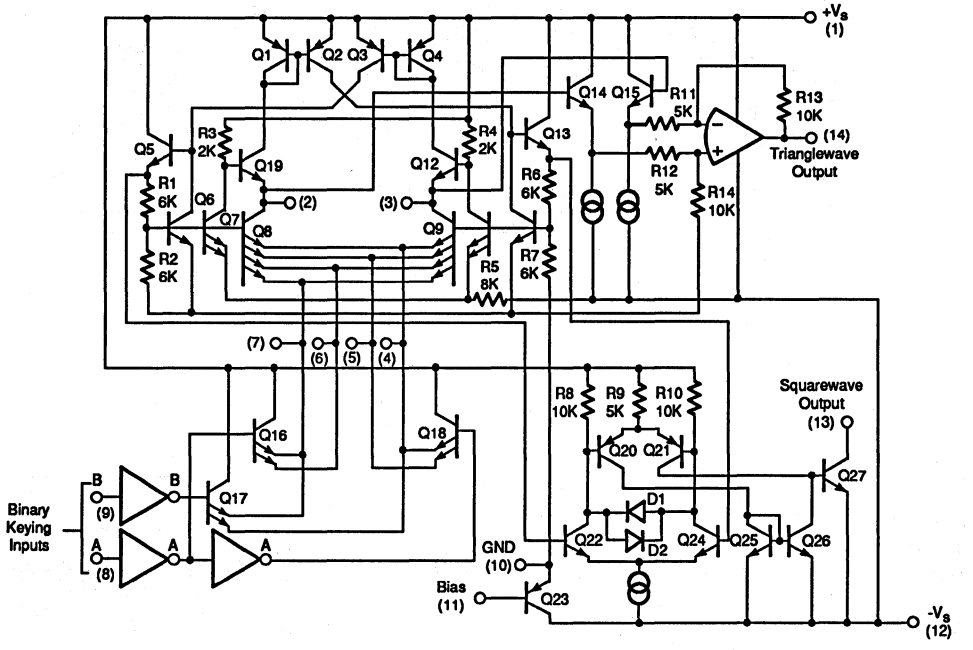


Figure 4. Pulse and Sawtooth Generation

Linear

Schematic Diagram



RC2211
FSK Demodulator/Tone Decoder

Description

The RC2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well-suited for FSK modem applications, and operates over a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth and output delay.

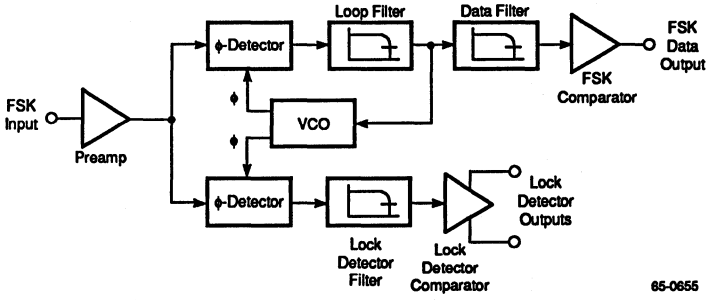
Features

- Wide frequency range — 0.01 Hz to 300 kHz
- Wide supply voltage range — 4.5V to 20V
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range — 2 mV to 3 V_{RMS}
- Adjustable tracking range — ±1% to ±80%
- Excellent temperature stability — 20 ppm/°C typical

Applications

- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

Functional Block Diagram



Linear

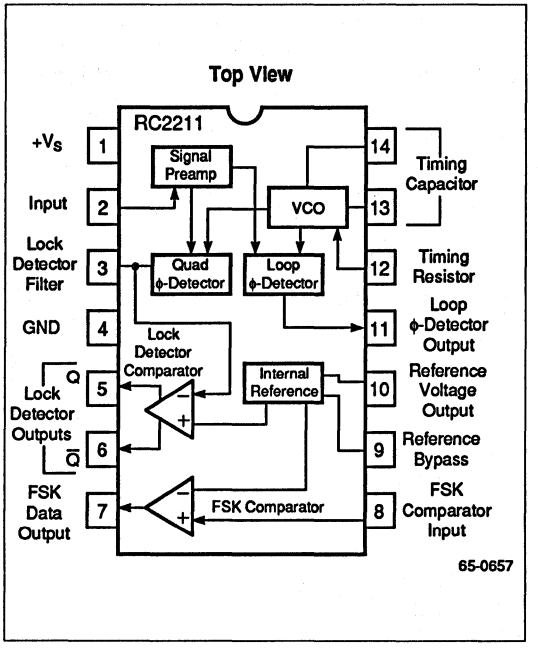
Absolute Maximum Ratings

Supply Voltage ..... ±20V
Input Signal Level ..... 3 V_{RMS}
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
RM2211D ..... -55°C to +125°C
RV2211N ..... -25°C to +85°C
RC2211N ..... 0°C to +70°C
Lead Soldering Temperatuare (60 sec.) ..... +300°C

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A < 50°C	468 mW	1042 mW
Therm. Res θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For T_A > 50°C Derate at	6.5 mW/°C	8.33 mW/°C

Connection Information



Ordering Information

Part Number	Package	Operating Temperature Range
RC2211N	N	0°C to +70°C
RV2211N	N	-25°C to +85°C
RM2211D	D	-55°C to +125°C
RM2211D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
N = 14-Lead Plastic DIP
D = 14-Lead Ceramic DIP

Electrical Characteristics

(Test Conditions $+V_S = +12V$, $T_A = +25°C$, R0 = 30 kΩ, C0 = 0.033 µF. See Figure 1 for component designations.)

Parameters	Test Conditions	RV/RM2211 Min	RV/RM2211 Typ	RV/RM2211 Max	RC2211 Min	RC2211 Typ	RC2211 Max	Units
General								
Supply Voltage[2]		4.5		20	4.5		20	V
Supply Current	R0 ≥ 10 kΩ		4.0	9.0		5.0	11	mA
Oscillator								
Frequency Accuracy	Deviation from f_o = 1/R0C0		±1.0	±3.0		±1.0		%
Frequency Stability[1]								
Temperature Coefficient	R1 = ∞		±20	±50		±20		ppm/°C
Power Supply Rejection	$+V_s$ = 12 ±1V		0.05	0.5		0.05		%/V
	$+V_s$ = 5 ±0.5V		0.2		0.2		%/V	
Upper Frequency Limit	R0 = 8.2 kΩ, C0 = 400 pF	100	300			300		kHz
Lowest Practical Operating Frequency[1]	R0 = 2 MΩ, C0 = 50 µF			0.01		0.01		Hz
Timing Resistor, R0								
Operating Range		5.0		2000	5.0		2000	kΩ
Recommended Range		15		100	15		100	kΩ
Loop Phase Detector								
Peak Output Current	Measured at pin 11	±150	±200	±300	±100	±200	±300	µA
Output Offset Current			±1.0			±2.0		µA
Output Impedance			1.0			1.0		MΩ
Maximum Swing	Ref. to pin 10	±4.0	±5.0		±4.0	±5.0		V
Quadrature Phase Detector								
Peak Output Current[3]	Measured at pin 3	100	150			150		µA
Output Impedance			1.0			1.0		MΩ
Maximum Swing			11			11		V_{P-P}
Input Preamp								
Input Impedance	Measured at pin 2		20			20		kΩ
Input Signal Voltage Required			2.0	10		2.0		mV_{RMS}
to Cause Limiting[3]								
Voltage Comparator								
Input Impedance	Measured at pins 3 & 8		2.0			2.0		MΩ
Input Bias Current			100			100		nA
Voltage Gain[1]	R_L = 5.1 kΩ	55	70		55	70		dB
Output Voltage Low	I_C = 3 mA		300			300		mV
Output Leakage Current	V_0 = 12V		0.01			0.01		µA
Internal Reference								
Voltage Level	Measured at pin 10	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance			100			100		Ω

Notes:
1. Guaranteed by design.
2. Individual applications may need special circuitry to function at <12V.
3. Sample Tested

Description of Circuit Controls

Signal Input (Pin 2)
The input signal is AC coupled to this terminal. The internal impedance at pi n 2 is 20 kΩ. Recommended input signal level is in the range of 10 mV_{RMS} to 3 V_{RMS}.

Quadrature Phase Detector Output, Q (Pin 3)
This is the high impedance output of the quadrature phase detector, and is internally connected to the input of lock detector voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock detector outputs. If this tone detector section is not used, pin 3 can be left open circuited.

Lock Detector Output, Q (Pin 5)
The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting state when the PLL is locked. It is an open collector output and requires a pull-up resistor, R_L, to $+V_S$ for proper operation. In the "low" state it can sink up to 5 mA of load current.

Lock Detector Complement, $\bar{Q}$ (Pin 6)
The output at pin 6 is the logic complement of the lock detector output at pin 5. This output is also an open collector type stage which can sink 5 mA of load current in the low or "on" state.

FSK Data Output (Pin 7)
This output is an open collector stage which requires a pull-up resistor, R_L, to $+V_S$ for proper operation. It can sink 5 mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8)
This is the high impedance input to the FSK voltage comparator. Normally, an FSK post detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

Reference Bypass (Pin 9)
This pin can have an optional 0.1 µF capacitor connected to the ground.

Reference Voltage, V_R (Pin 10)
This pin is internally biased at the reference voltage level, V_R; $V_R = +V_S/2 - 650$ mV. The DC voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 µF capacitor.

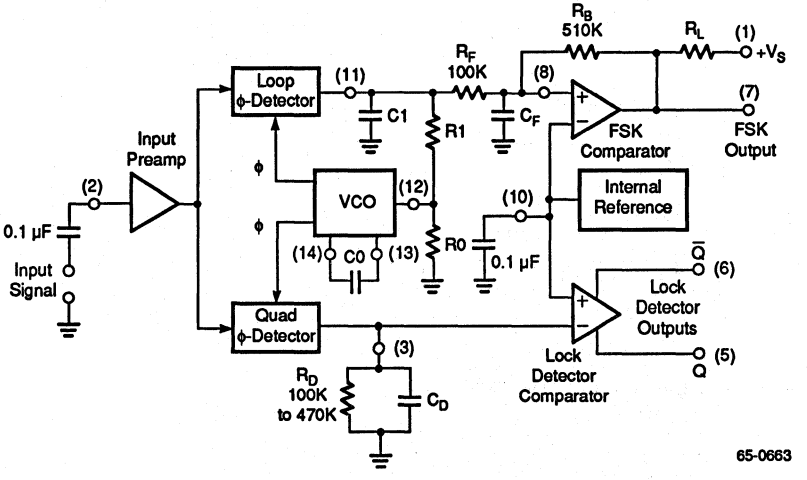


Figure 1. Generalized Circuit Connection for FSK and Tone Detection

Loop Phase Detector Output (Pin 11)
This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12)
VCO free running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free running frequency, f0 is given by:

$$f_0(Hz) = \frac{1}{R0C0}$$

where C0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R0 must be in the range of 10 kΩ to 100 kΩ (see Typical Performance Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_R. The maximum timing current drawn from pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14)
VCO frequency is inversely proportional to the external timing capacitor, C0, connected across these terminals. C0 must be non-polarized, and in the range of 200 pF to 10 µF.

VCO Frequency Adjustment
VCO can be fine tuned by connecting a potentiometer, R_X, in series with R0 at pin 12 (see Figure 2).

VCO Free-Running Frequency, f_0
The RC2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. However, for set-up or adjustment purposes, the VCO free-running frequency can be measured at pin 3 (with C_D disconnected) with no input and with pin 2 shorted to pin 10.

Design Equations

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, f_0:

$$F_0\,(Hz) = \frac{1}{R0C0}$$

2. Internal Reference Voltage, V_R (measured at pin 10):

$$V_R = \left(\frac{+V_s}{2}\right) - 650\ mV$$

3. Loop Lowpass Filter Time Constant, τ:

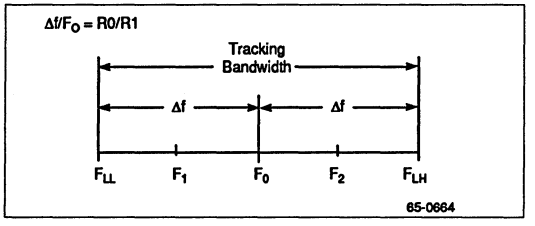
$$\tau = R1C1$$

4. Loop Dampening, ζ:

$$\zeta = \left(\sqrt{\frac{C0}{C1}}\right)\left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:

$$\Delta f/f_0 = R0/R1$$



6. FSK Data Filter Time Constant, τ_F:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, Kϕ (Kϕ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$k\phi\ (\text{in volts per radian}) = \frac{(-2)\ (V_R)}{\pi}$$

8. VCO Conversion Gain, K0 is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K0\ (\text{in Hertz per volt}) = \frac{-1}{C0R1V_R}$$

9. Total Loop Gain, K_T:
K_T (in radians per second per volt) $= 2\pi K\phi K0$
$= 4/C0R1$

10. Peak Phase Detector Current, I_A:

$$I_A\,(mA) = \frac{V_R}{25}$$

Linear

Applications

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R0 and C0 set the PLL center frequency, R1 sets the system bandwidth, and C1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (510 kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table. 1.

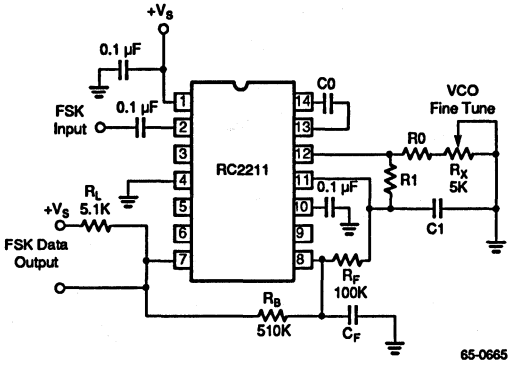


Figure 2. Circuit Connection for FSK Decoding

Table 1. Recommended Component Values for Commonly Used FSK Bands (see Circuit of Figure 2)

FSK Band	Component Values
300 Baud	C0 = 0.039 µF C_F = 0.005 µF
f_1 = 1070 Hz	C1 = 0.01 µF R0 = 18 kΩ
f_2 = 1270 Hz	R1 = 100 kΩ
300 Baud	C0 = 0.022 µF C_F = 0.005 µF
f_1 = 2025 Hz	C1 = 0.0047 µF R0 = 18 kΩ
f_2 = 2225 Hz	R1 = 200 kΩ
1200 Baud	C0 = 0.027 µF C_F = 0.0022 µF
f_1 = 1200 Hz	C1 = 0.01 µF R0 = 18 kΩ
f_2 = 2200 Hz	R1 = 30 kΩ

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components: R0, R1, C0, C1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, f_0

$$f_0 = \frac{f_1 + f_2}{2}$$

2. Choose a value of timing resistor R0 to be in the range of 10 kΩ to 100 kΩ. This choice is arbitrary. The recommended value is R0 = 20 kΩ. The final value of R0 ios normally fine-tuned with the series potentiometer, R_X.

3. Calculate value of C0 from Design Equation No. 1 or from Typical Performance Characteristics:

$$C0 = 1/R0f_0$$

4. Calculate R1 to give a Δf equal to the mark-space deviation:

$$R1 = R0\,[f_0/(f1 - f2)]$$

5. Calculate C1 to set loop damping. (See Design Equation No. 4)

Normally, $\zeta \approx 1/2$ is recommended
Then: C1 = C0/4 for $\zeta = 1/2$

6. Calculate Data Filter Capacitance, C_F:
For R_F = 100 kΩ, R_B = 510 kΩ, the recommended value of C_F is:

$$C_F \text{ (in µF)} = \frac{3}{\text{Baud Rate}}$$

Note: All calculated component values except R0 can be rounded off to the nearest standard value, and R0 can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

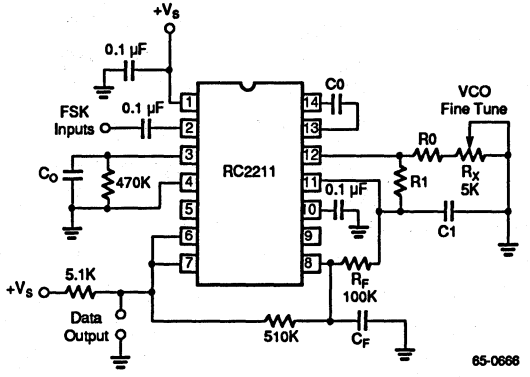
75 Bauk FSK demodulator with mark/space frequencies of 1110/1170 Hz:

Step 1: Calculate f_0:
f_0 = (1110 + 1170) (1/2) = 1140 Hz
Step 2: Choose R0 = 20 kΩ (18 kΩ fixed resistor in series with 5 kΩ potentiometer)
Step 3: Calculate C0 from VCO Frequency vs. Timing Capacitor: C9 = 0.044 µF
Step 4: Calculate R1: R1 = R0 (1140/60) = 380 kΩ
Step 5: Calculate C1: C1 = C0/4 = 0.011 µF

Note: All values except R0 can be rounded off to nearest standard value.

FSK Decoding with Carrier Detector

The lock detector section of the RC2211 can be used as a carrier detector option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock detector output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.



Note: Data output is "low" when no carrier is present.

Figure 3. External Connections for FSK Demodulation with Carrier Detector Capability

The minimum value of the lock detector filter capacitance C_D is inversely proportional to the capture range, $\pm \Delta f_C$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C1. For most applications, $\Delta f_C < \Delta f/2$. For $R_D = 470\ k\Omega$, the approximate minimum value of C_D can be determined by:

$$C_D(\mu F) \geq 16/\text{capture range in Hz}$$

With values of C_D that are too small, chatter can be observed on the lock detector output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detector output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed to the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

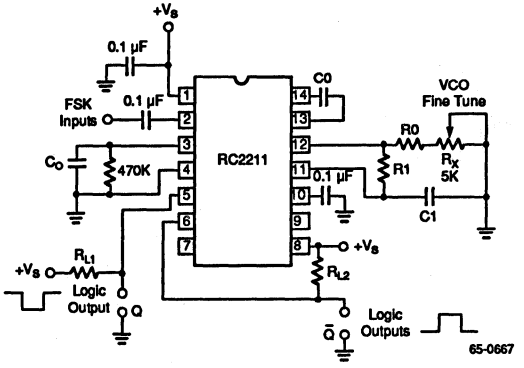


Figure 4. Circuit Connection for Tone Detection

With reference to Figures 1 and 4, the function of the external circuit components can be explained as follows: R0 and C0 set VCO center frequency, R1 sets the detection bandwidth, C1 sets the lowpass-loop filter time constant and the loop dampening factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R0, R1, C0, C1 and C_D. For a given input tone frequency, f_S, these parameters are calculated as follows:

1. Choose R0 to be in the range of 15 kΩ to 100 kΩ. This choice is arbitrary.
2. Calculate C0 to set center frequency, f_0 equal to f_S: $C0 = 1/R0f_S$.
3. Calculate R1 to set bandwidth $\pm\Delta f$ (see Design Equation No. 5): $R1 = R0(f_0/\Delta f)$. Note: The total detection bandwidth covers the frequency range of RC2211RC2211$f_0 \pm \Delta f$.
4. Calculate value of C1 for a given loop damping factor:

$$C1 = C0/16\zeta^2$$

Normally $\zeta \approx 1/2$ is optimum for most tone detector applications, giving C1 = 0.25 C0.

Increasing C1 improves the out-of-band signal rejection, but increases the PLL capture time.

5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470 kΩ, C_D must be:

$$C_D(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows the logic output response time.

Design Examples

Tone detector with a detection band of 1 kHz ±20 Hz:

Step 1: Choose R0 = 20 kΩ (18 kΩ in series with 5 kΩ potentiometer).
Step 2: Choose C0 for f_0 = 1 kHz: C0 = 0.05 µF.
Step 3: Calculate R1: R1 = (R0) (1000/20) = 1 MΩ
Step 4: Calculate C1: for ζ = 1/2, C1 = 0.25 µF, C0 = 0.013 µF.
Step 5: Calculate C_D: C_D = 16/38 = 0.42 µF.
Step 6: Fine tune the center frequency with the 5 kΩ potentiometer, R_X.

Linear FM Detection

The RC2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{OUT} = R1\ V_R/100\ R0 \text{ Volts/\% deviation}$$

where V_R is the internal reference voltage. For the choice of external components R1, R0, C0, C1 and C_F, see the section on Design Instructions.

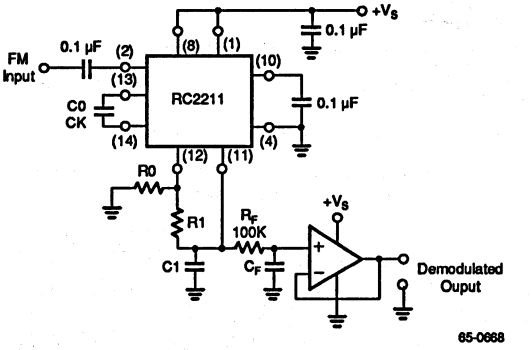
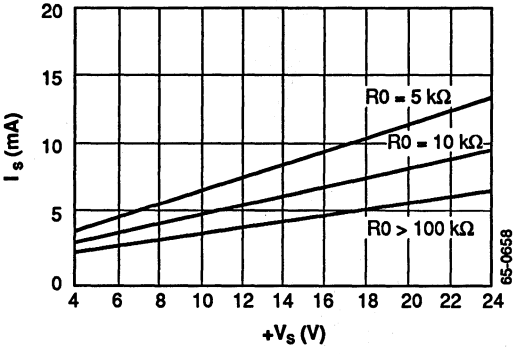


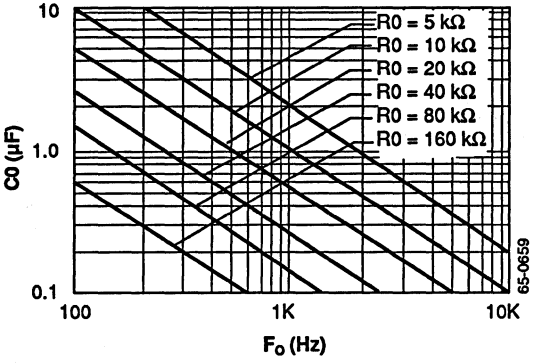
Figure 5. Linear FM Detector Using RC2211 and an External Op Amp

Typical Performance Characteristics

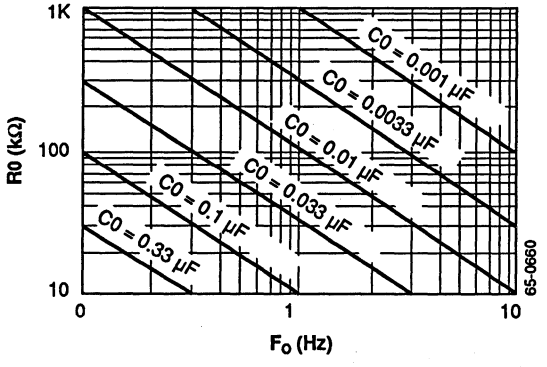
Supply Current vs. Supply Voltage (Logic Outputs Open Circuited)



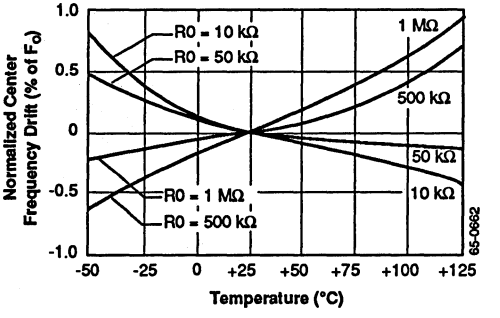
Timing Resistor with Timing Capacitor vs. VCO Frequency



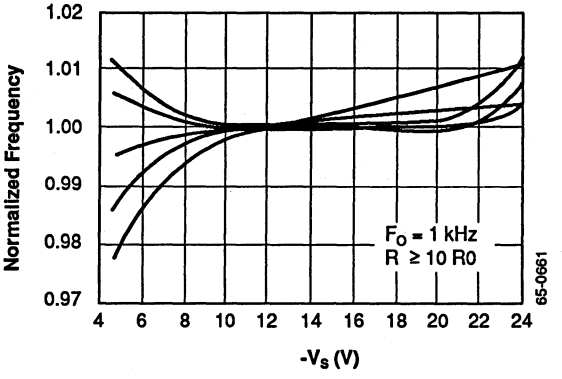
Timing Capacitor with Timing Resistor vs. VCO Frequency



Center Frequency Drift vs. Temperature



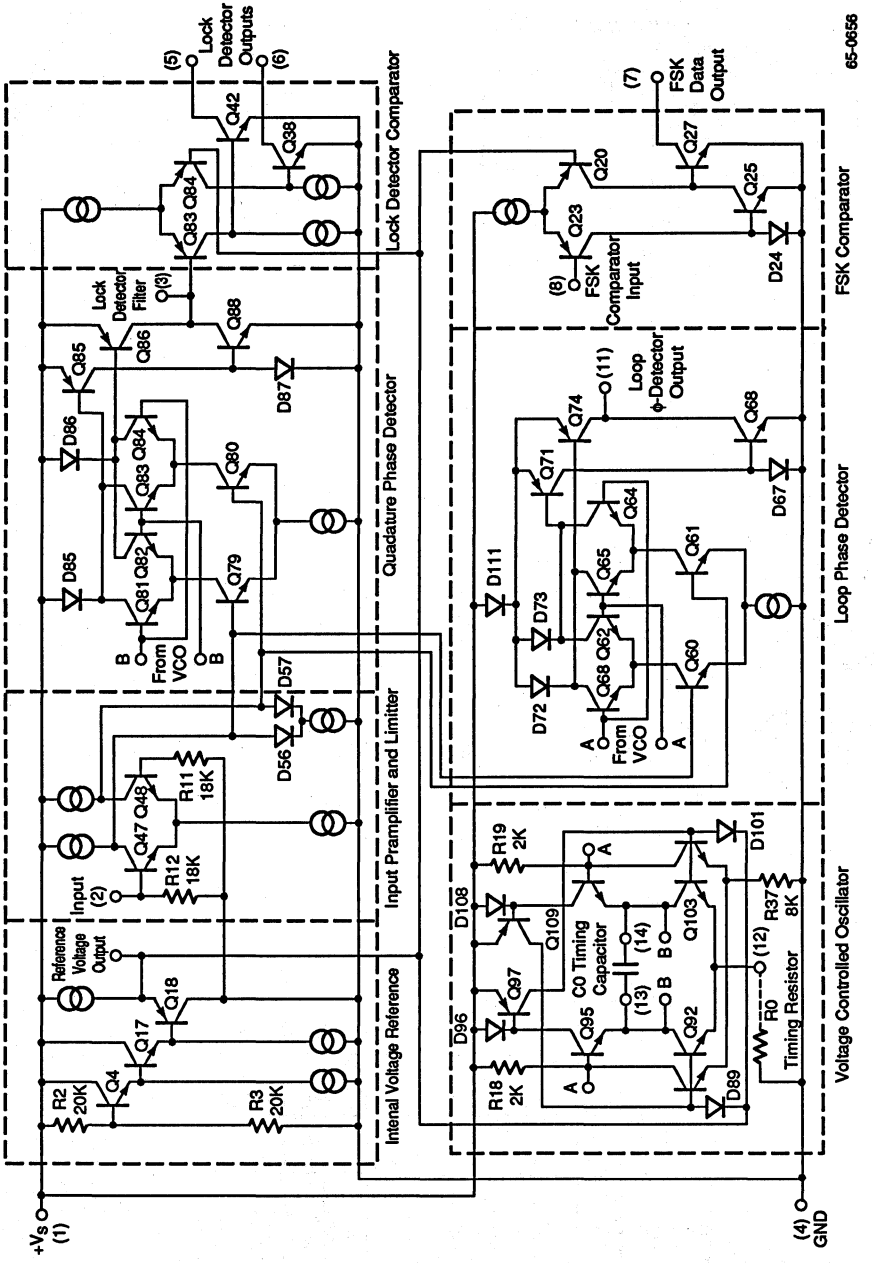
VCO Frequency vs. Supply Voltage



Curve	R0
1	5K
2	10K
3	30K
4	100K
5	300K

Linear

Schematic Diagram



RC4200
Analog Multiplier

Description

The RC4200 analog multiplier has complete compensation for nonlinearity, the primary source of error and distortion. This multiplier also has three on-board operational amplifiers designed specifically for use in multiplier logging circuits. These amplifiers are frequency compensated for optimum AC response in a logging circuit, the heart of a multiplier, and can therefore provide superior AC response.

The RC4200 can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very high accuracy and a low temperature coefficient.

The excellent linearity and versatility were achieved through circuit design rather than special grading or trimming, and therefore, unit cost is very low.

The RC4200 is ideal for use in low distortion audio modulation circuits, voltage-controlled active filters, and precision oscillators.

Features

- High accuracy
  Nonlinearity — 0.1%
  Temperature coefficient — 0.005%/°C
- Multiple functions
  Multiply, divide, square, square root, RMS-to-DC conversion, AGC and modulate/demodulate
- Wide bandwidth — 4 MHz
- Signal-to-noise ratio — 94 dB

Absolute Maximum Ratings

Supply Voltage[1] ..... -22V
Internal Power Dissipation[2] ..... 500 mV
Input Current ..... -5 mA
Storage Temperature Range
RM4200/4200A ..... -65°C to +150°C
RC4200/4200A ..... -55°C to +125°C
Operating Temperature Range
RM4200/4200A ..... -55°C to +125°C
RC4200/4200A ..... 0°C to +70°C

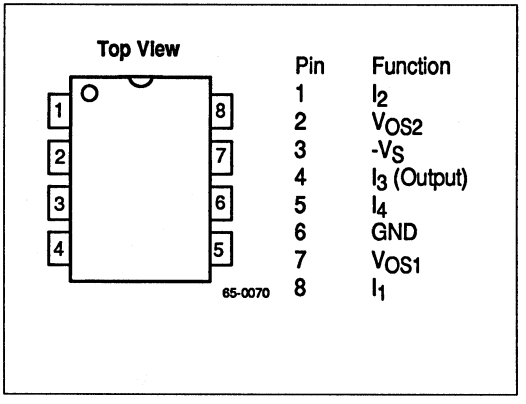
Notes:
1. For a supply voltage greater than -22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Ordering Information

Part Number	Package	Operating Temperature Range
RC4200N	N	0°C to +70°C
RC4200AN	N	0°C to +70°C
RM4200D	D	-55°C to +125°C
RM4200AD	D	-55°C to +125°C
RM4200AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP

Connection Information



Pin	Function
1	I_2
2	V_{OS2}
3	$-V_S$
4	I_3 (Output)
5	I_4
6	GND
7	V_{OS1}
8	I_1

Thermal Characteristics

(Still air, soldered into PC board)

	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A < 50°C	468 mW	833 mW
Therm. Res. θ_{JC}	—	45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For T_A > 50°C Derate at	6.25 mW/°C	8.33 mW/°C

Electrical Characteristics

(Over operating temperature range, V_S = -15V unless otherwise noted)

		4200A			4200			
Parameters	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Total Error as Multiplier	T_A = +25°C							
Untrimmed	Note 1			±2.0			±3.0	%
With External Trim			±0.2			±0.2		%
Versus Temperature			±0.005			±0.005		%/°C
Versus Supply (-9 to -18V)			±0.1			±0.1		%/V
Nonlinearity	50 µA ≤$I_{1,2,4}$ ≤ 250 µA, T_A = +25°C (Note 2)			±0.1			±0.3	%
Input Current Range (I_1, I_2 and I_4)		1.0		1000	1.0		1000	µA
Input Offset Voltage	$I_1 = I_2 = I_4$ = 150 µA, T_A = +25°C			±5.0			±10	mV
Input Bias Current	$I_1 = I_2 = I_4$ = 150 µA, T_A = +25°C			300			500	nA
Average Input Offset Voltage Drift	$I_1 = I_2 = I_4$ = 150 µA			±50			±100	µV/°C
Output Current Range (I_3)	Note 3	1.0		1000	1.0		1000	µA
Frequency Response, -3dB point			4.0			4.0		MHz
Supply Voltage		-18	-15	-9.0	-18	-15	-9.0	V
Supply Current	$I_1 = I_2 = I_4$ = 150 µA, T_A = +25°C			4.0			4.0	mA

Notes:
1. Refer to Figure 6 for example.
2. The input circuits tend to become unstable at I_1, I_2, I_4 < 50 µA and linearity decreases when I_1, I_2, I_4 > 250 µA (eg. @ $I_1 = I_2$ = 500 µA, nonlinearity error ≈ 0.5%).
3. These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700Ω and must be pulled up to a positive supply such that the voltage on pin (4) stays within a range of 0 to +5V.

Functional Description

The RC4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in Figure 1. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{I_1 I_2}{I_4} \qquad (1)$$

The three input currents must be positive and restricted to a range of 1 µA to 1 mA. These currents go into the multiplier chip at op amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capability of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2 and Q4 equal to their respective input currents (I_1, I_2, and I_4). These op amps are designed with current-source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single supply voltage (nominally -15V) and total quiescent current drain is less than 4 mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

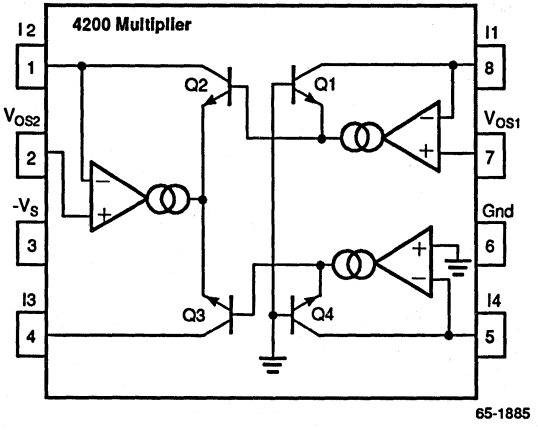


Figure 1. Functional Diagram

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship

$$V_{BEN} = \frac{kT}{Q} \ln \frac{I_{CN}}{I_{SN}} \qquad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. The $I_C r_E$ term introduces a parabolic nonlinearity even with matched transistors. Raytheon has developed a unique and proprietary means of inherently compensating for this undesired $I_C r_E$ term. Furthermore, this Raytheon-developed circuit technique compensates linearity error over temperature changes. The nonlinearity versus temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{KT}{q}\left[\ln\frac{I_1}{I_{S1}} = \ln\frac{I_2}{I_{S2}} - \ln\frac{I_3}{I_{S3}} - \ln\frac{I_4}{I_{S4}}\right] = 0 \qquad (3)$$

This equation reduces to:

$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \qquad (4)$$

The ratio of reverse saturation currents, $I_{S1}I_{S2}/I_{S3}I_{S4}$, depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the ratio is very close to unity, typically 1.0 ±1%. The final result is the desired relationship:

$$I_3 = \frac{I_1 I_2}{I_4} \qquad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

Basic Circuits

Current Multiplier/Divider

The basic design criteria for all circuit configurations using the 4200 multiplier is contained in equation (1):

i.e., $$I_3 = \frac{I_1 I_2}{I_4}$$

The current-product-balance equation restates this as:

$$I_1 I_2 = I_3 I_4 \qquad (6)$$

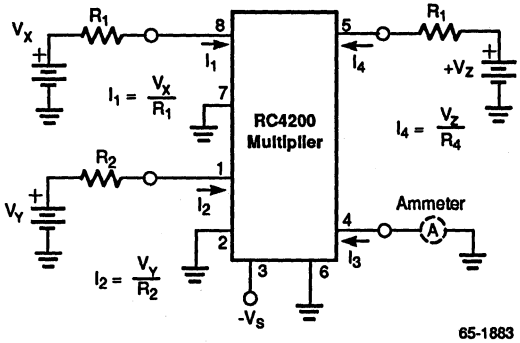
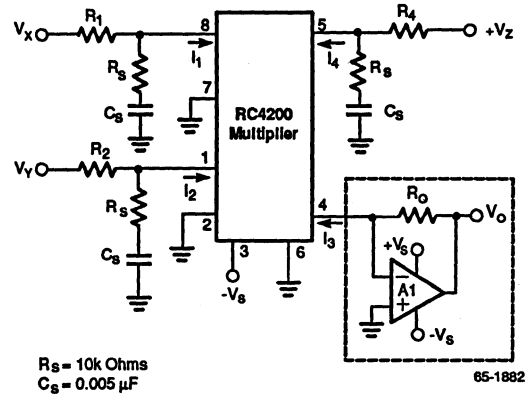


Figure 2

Dynamic Range and Stability

The precision dynamic range for the 4200 is from +50 µA to +250 µA inputs for I_1, I_2 and I_4. Stability and accuracy degrade if this range is exceeded.

To improve the stability for input currents less than 50 µA, filter circuits ($R_S C_S$) are added to each input (see Figure 3).

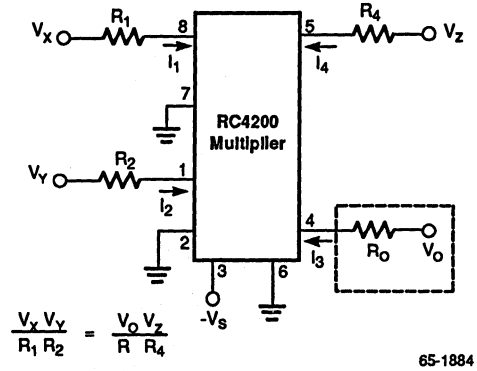


Amplifier A1 is used to convert the I_3 current to an output voltage.

Multiplier: V_Z = constant ≠ 0
Divider: V_Y = constant ≠ 0

Figure 3

Voltage Multiplier/Divider



Solving for $V_O = \frac{V_X V_Y}{V_Z} \frac{R_O R_4}{R_1 R_2}$

For a multiplier circuit $V_Z = V_R$ = constant

Therefore: $V_O = V_X V_Y K$ where $K = \frac{R_O R_4}{V_R R_1 R_2}$

For a divider circuit $V_Y = V_R$ = constant

Therefore: $V_O = \frac{V_X}{V_Z} K$ where $K = \frac{V_R R_O R_4}{R_1 R_2}$

Figure 4

Linear

Extended Range

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The R_SC_S filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50 µA min. and 250 µA max.

Extended Range Multiplier

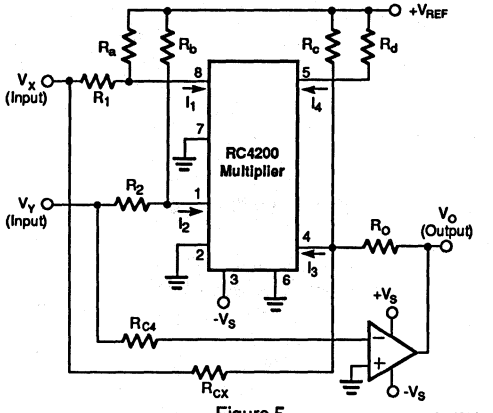


Figure 5 65-1881

Resistors R_a and R_b extend the range of the V_X and V_Y inputs by picking values such that:

$$I_1(\text{min.}) = \frac{V_X(\text{min.})}{R_1} + \frac{V_{REF}}{R_a} = 50\ \mu A,$$

$$\text{and } I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_{REF}}{R_a} = 250\ \mu A;$$

$$\text{also } I_2(\text{min.}) = \frac{V_Y(\text{min.})}{R_2} + \frac{V_{REF}}{R_b} = 50\ \mu A,$$

$$\text{and } I_2(\text{max.}) = \frac{V_Y(\text{max.})}{R_2} + \frac{V_{REF}}{R_b} = 250\ \mu A.$$

Resistor R_C supplies bias current for I_3 which allows the output to go negative.

Resistors R_{CX} and R_{CY} permit equation (6) to balance, ie.:

$$\left(\frac{V_X}{R_1} + \frac{V_{REF}}{R_a}\right) + \left(\frac{V_Y}{R_2} + \frac{V_{REF}}{R_b}\right) = \left(\frac{V_0}{R_0} + \frac{V_{REF}}{R_c} + \frac{V_X}{R_{CX}} + \frac{V_Y}{R_{CY}}\right)\left(\frac{V_{REF}}{R_d}\right)$$

$$\frac{V_YV_X}{R_1R_2} + \frac{V_XV_{REF}}{R_1R_b} + \frac{V_YV_{REF}}{R_2R_a} + \frac{V_{REF}}{R_aR_b} =$$

$$\frac{V_0V_{REF}}{R_0R_d} + \frac{V_XV_{REF}}{R_{CX}R_d} + \frac{V_YV_{REF}}{R_{CY}R_d} + \frac{V_{REF}^2}{R_cR_d}$$

Cross-Product Cancellation

Cross-products are a result of the V_XV_R and V_YV_R terms. To the extend that: $R_1R_b = R_{CX}R_d$ and $R_2R_a = R_{CY}R_d$, cross-product cancellation will occur.

Arithmetic Offset Cancellation

The offset caused by the V_{REF}^2 term will cancel to the extent that: $R_aR_b = R_cR_d$, and the result is:

$$\frac{V_YV_X}{R_1R_2} = \frac{V_0V_{REF}}{R_0R_d} \text{ or } V_0 = V_XV_YK$$

$$\text{Where } K = \frac{R_0R_d}{V_{REF}R_1R_2}$$

Resistor Values

Inputs:

$$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$$

$$\Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$$

$$V_Y(\text{min.}) \le V_Y \le V_Y(\text{max.})$$

$$\Delta V_Y = V_Y(\text{max.}) = V_Y(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

$$K = \frac{V_0}{V_XV_Y} \text{ (Design Requirement)}$$

$$R_1 = \frac{\Delta V_X}{200\ \mu A},\ R_2 = \frac{\Delta V_Y}{200\ \mu A},\ R_d = \frac{V_{REF}}{250\ \mu A}$$

$$R_a = \frac{\Delta V_XV_{REF}}{250\ \mu A\Delta V_X - 200\ \mu A\ V_X(\text{max.})}$$

$$R_b = \frac{\Delta V_YV_{REF}}{250\ \mu A\Delta V_Y - 200\ \mu A\ V_Y(\text{max.})}$$

$$R_c = \frac{R_aR_b}{R_d},\ R_{cx} = \frac{R_1R_b}{R_d},\ R_{cy} = \frac{R_2R_a}{R_d}$$

$$R_0 = \frac{\Delta V_X\Delta V_YK}{160\ \mu A}$$

Multiplying Circuit Offset Adjust

$10K \leq R_5 = R_9 = R_{16} \leq 50K$

$R_7 = R_{11} = R_{14} = 100\Omega$

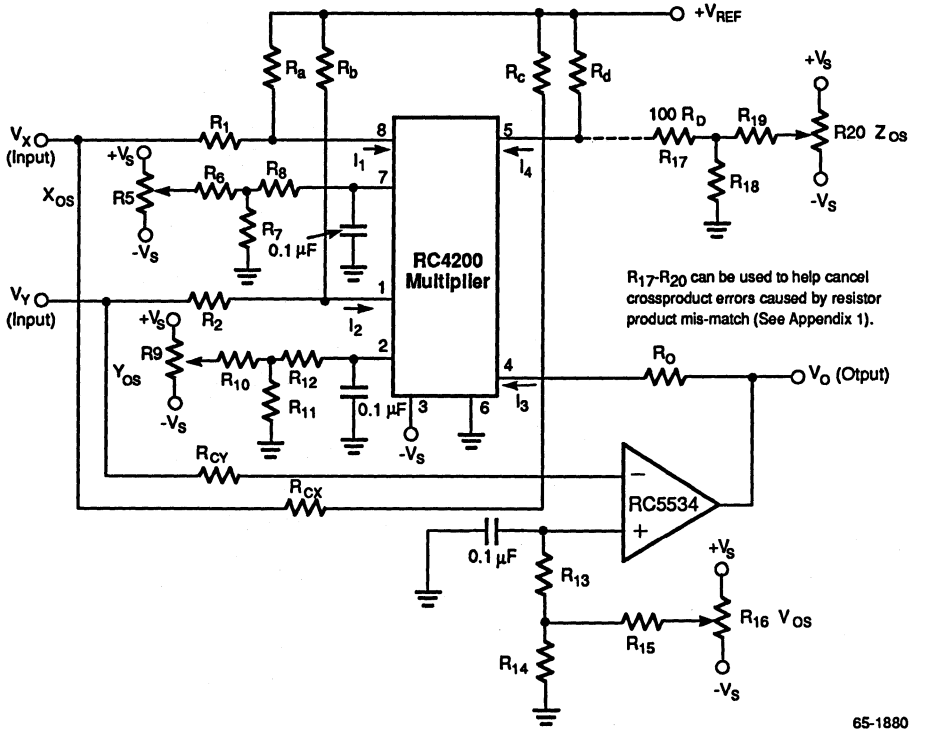
$R_6 = R_{10} = 100\Omega\,(V_S/0.05)$

$R_{15} = 100\Omega\,(V_S/0.10)$

$R_8 = R_1 \,||\, R_a$

$R_{12} = R_2 \,||\, R_b$

$R_{13} = R_0 \,||\, R_C \,||\, R_{CX} \,||\, R_{CY}$



Procedure:

1. Set all trimmer pots to 0V on the wiper.
2. Connect V_X input to ground. Put in a full scale square wave on V_Y input. Adjust $X_{OS}(R_5)$ for no square wave on V_0 output (adjust for 0 feedthrough).
3. Connect V_Y input to ground. Put in a full scale square wave on V_X input. Adjust $Y_{OS}(R_9)$ for no square wave on V_0 output (adjust for 0 feedthrough).
4. Connect V_X and V_Y to ground. Adjust $V_{OS}(R_{16})$ for 0V on V_0 output.

Figure 6

Linear

Extended Range Divider

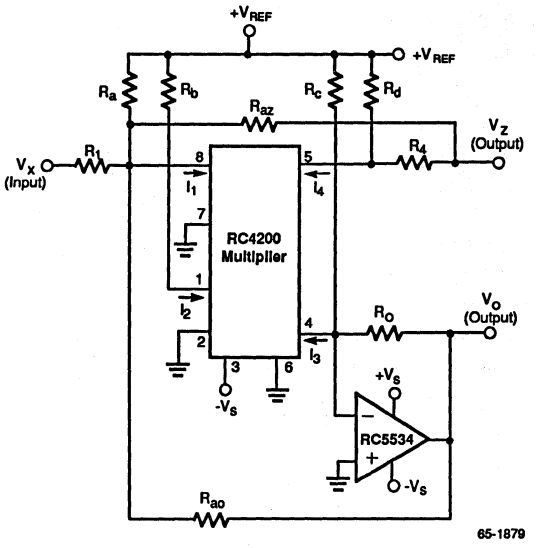


Figure 7

As with the extended range multiplier, resistors R_{az} and R_{ao} are added to cancel the cross-product error caused by the biasing resistors, i.e.,

$$\left(\frac{V_X}{R_1}+\frac{V_0}{R_{ao}}+\frac{V_Z}{R_{az}}+\frac{V_{REF}}{R_a}\right)\left(\frac{V_{REF}}{R_b}\right)=\left(\frac{V_0}{R_0}+\frac{V_{REF}}{R_c}\right)\left(\frac{V_Z}{R_4}+\frac{V_{REF}}{R_d}\right)$$

$$\frac{V_XV_{REF}}{R_1R_b}+\frac{V_0V_{REF}}{R_{ao}R_b}+\frac{V_ZV_{REF}}{R_{az}R_b}+\frac{V_{REF}^2}{R_aR_b}=$$

$$\frac{V_0V_Z}{R_0R_4}+\frac{V_0V_{REF}}{R_0R_d}+\frac{V_ZV_{REF}}{R_4R_c}+\frac{V_{REF}^2}{R_cR_d}$$

To cancel cross-product and arithmetic offset:

$R_{ao}R_b = R_0R_d$, $R_{az}R_b = R_4R_c$ and $R_aR_b = R_cR_d$

and the result is:

$$\frac{V_XV_{REF}}{R_1R_b}=\frac{V_0V_Z}{R_0R_4} \quad \text{or} \quad V_0=\frac{V_X}{V_ZK}$$

$$\text{where } K=\frac{V_{REF}R_0R_4}{R_1R_b}$$

Note: it is necessary to match the above resistor cross-products to within the amount of error tolerable in the output offset, i.e., with a 10V F.S. output, 0.1% resistor cross-product match will give 0.1% x 10V = 10 mV untrimmable output offset voltage.

Resistor Values

Inputs:

$$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$$
$$\Delta V_X = V_X(\text{max.}) = V_X(\text{min.})$$
$$V_Z(\text{min.}) \le V_Z \le V_Z(\text{max.})$$
$$\Delta V_Z = V_Z(\text{max.}) = V_Z(\text{min.})$$
$$V_{REF} = \text{Constant (+7V to +18V)}$$

Outputs:

$$V_0(\text{min.}) \le V_0 \le V_O(\text{max.})$$
$$\Delta V_0 = V_0(\text{max.}) = V_0(\text{min.})$$

$$K=\frac{V_0V_Z}{V_X} \text{ (Design Requirement)}$$

$$R_0=\frac{\Delta V_0}{750\ \mu A},\ R_b=\frac{V_{REF}}{250\ \mu A},\ R_4=\frac{\Delta V_Z}{200\ \mu A}$$

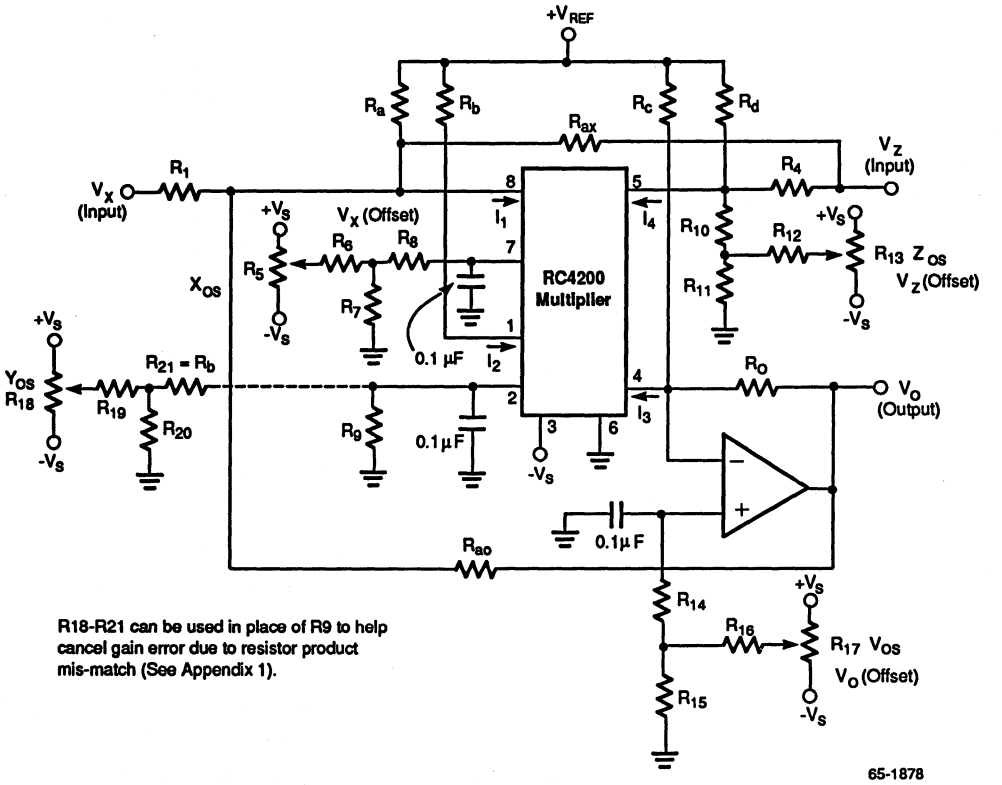
$$R_c=\frac{\Delta V_0V_{REF}}{750\ \mu A\Delta V_0 - 700\ \mu A\ V_0(\text{max.})}$$

$$R_d=\frac{\Delta V_ZV_{REF}}{250\ \mu A\Delta V_Z - 200\ \mu A\ V_Z(\text{max.})}$$

$$R_a=\frac{R_cR_d}{R_b},\ R_{az}=\frac{R_cR_4}{R_b},\ R_{ao}=\frac{R_0R_d}{R_b}$$

$$R_1=\frac{\Delta V_0\Delta V_Z}{600\ \mu AK}$$

Divider Circuit with Offset Adjustment



General

$10K \leq R_5 = R_{13} = R_{17} \leq 50K$

$R_7 + R_8 \approx R_1 | |R_a| |R_{az}| |R_{ao}$

$R_6 \approx R_7 (V_S/0.05)$

$R_9 = R_b$

$R_{10} \approx 100 \times R_4$

$R_{11} = 20K$

$R_{12} = 100K$

$R_{14} + R_{15} \approx R_O | |R_c$

$R_{16} \approx R_{15} (V_S/0.10)$

Example: Two-Quad Divider

$V_O = K (V_X/V_Z)$, $K = k$, $V_{REF} = +V_S = +15V$

$-10 \leq V_X \leq +10$, therefore $\Delta V_X = 20$

$0 \leq V_Z \leq +10$, therefore $\Delta V_Z = 10$

$-10 \leq V_O \leq +10$, therefore $\Delta V_O = 20$

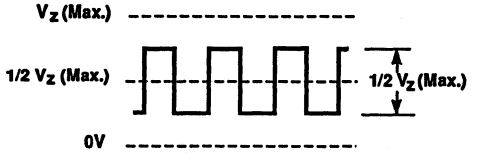
$R_O = 26.7K$
$R_b = 60K$
$R_4 = 50K$
$R_c = 37.5K$
$R_d = 300K$
$R_a = 187.5K$
$R_{az} = 31.25K$
$R_{ao} = 133K$

$R_1 = 333K$
$R_5, R_{13}, R_{17} = 10K$
$R_7, R_{15} = 1K$
$R_8, R_{11} = 20K$
$R_6, R_9, R_{16} = 300K$
$R_{10} = 4.7M$
$R_{12} = 100K$

Figure 8

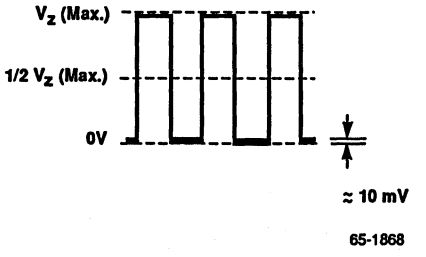
Divider Circuit Offset Adjustment Procedure

1. Set each trimmer pot to 0V on the wiper.
2. Connect V_X (input) to ground. Put a DC voltage of approximately $1/2$ V_Z(max.) DC on the V_Z (input) with an AC (squarewave is easiest) voltage of $1/2$ V_Z (max.) peak-to-peak superimposed on it. Adjust X_{OS} (R_5) for zero feedthrough. (No AC at V_O)



3. Connect V_X (input) to V_Z (input) and put in the $1/2V_Z$(max.) DC with an AC of approximately 20 mV less than V_Z(max.).

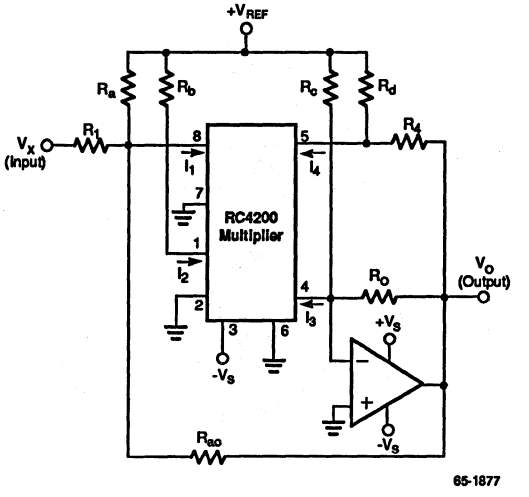
   Adjust Z_{OS}(R_{13}) for zero feedthrough.



4. Return V_X (input) to ground and connect V_Z(max.) DC on V_Z(input). Adjust output V_{OS}(R_{17}) for V_O =0V_O
5. Connect V_X (input) to V_Z (input) and put in V_Z (max.) DC. (The output will equal K.) Decrease the input slowly until the output (V_O = K) deviates beyond the desired accuracy. Adjust Z_{OS} to bring it back into tolerance and return to Step 4. Continue Steps 4 and 5 until V_Z reduces to the lowest value desired.

Note: As the input to V_X and V_Z gets closer to zero (an illegal state) the system noise will predominate so much that an integrating voltmeter will be very helpful.

Square Root Circuit $V_O = N\sqrt{V_X}$



$$\frac{V_X V_{REF}}{R_1 R_b} + \frac{V_{REF}^2}{R_a R_b} + \frac{V_0 V_{REF}}{R_{ao} R_b} = \frac{V_0^2}{R_0 R_4} + \frac{V_0 V_{REF}}{R_c R_4} + \frac{V_0 V_{REF}}{R_o R_d} + \frac{V_{REF}^2}{R_c R_d}$$

If $R_a R_b = R_c R_d$ and $R_{ao} R_b R_0 R_d + R_{ao} R_b R_c R_4 = R_c R_d R_0 R_4$

$$\text{Then } \frac{V_0^2}{R_0 R_4} = \frac{V_X V_{REF}}{R_1 R_b} \text{ or } V_O^2 = V_X K \text{ where } K = \frac{V_{REF} R_0 R_4}{R_1 R_b}$$

and $V_0 = N\sqrt{V_X}$ where $N = \sqrt{K}$

$0 \le V_X \le V_X(\text{max.})$ and $V_0(\text{max.}) = N\sqrt{V_X}(\text{max})$

$$N = \frac{V_0}{\sqrt{V_X}} \text{ (Design Requirement)}$$

$$R_1 = \frac{V_0(\text{max})^2}{74\mu A\, N^2}$$

$$R_a = R_d = \frac{V_{REF}}{50\mu A}$$

$$R_b = R_c = \frac{V_{REF}}{150\mu A}$$

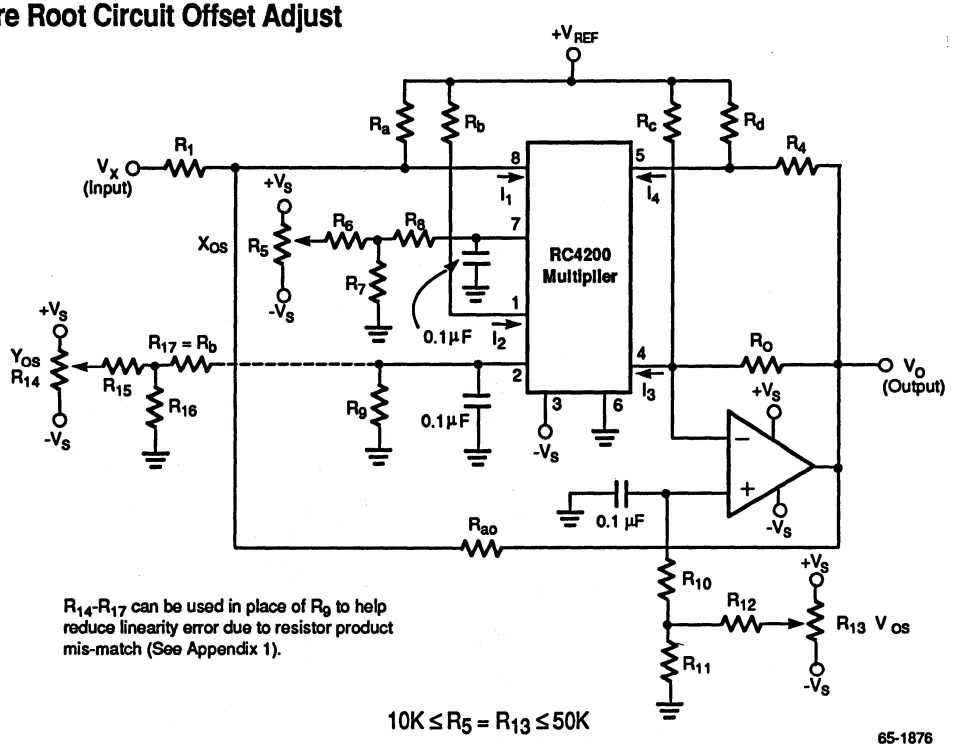
$$R_4 = \frac{\sqrt{V_0(\text{max})}}{50\mu A}$$

$$R_{ao} = \frac{V_0(\text{max})}{125\mu A}$$

$$R_0 = \frac{V_0(\text{max})}{225\mu A}$$

Figure 9

Square Root Circuit Offset Adjust



R_{14}-R_{17} can be used in place of R_9 to help reduce linearity error due to resistor product mis-match (See Appendix 1).

$$10K \leq R_5 = R_{13} \leq 50K$$

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$$R_7 = 100\Omega$$

$$R_6 = R_7 \frac{V_S}{0.05}$$

$$R_8 = R_1 | |R_a| |R_{ao}$$

$$R_9 = R_b$$

$$R_{10} = R_o | |R_c$$

$$R_{11} = 100\Omega$$

$$R_{12} = R_{11} \frac{V_S}{0.1}$$

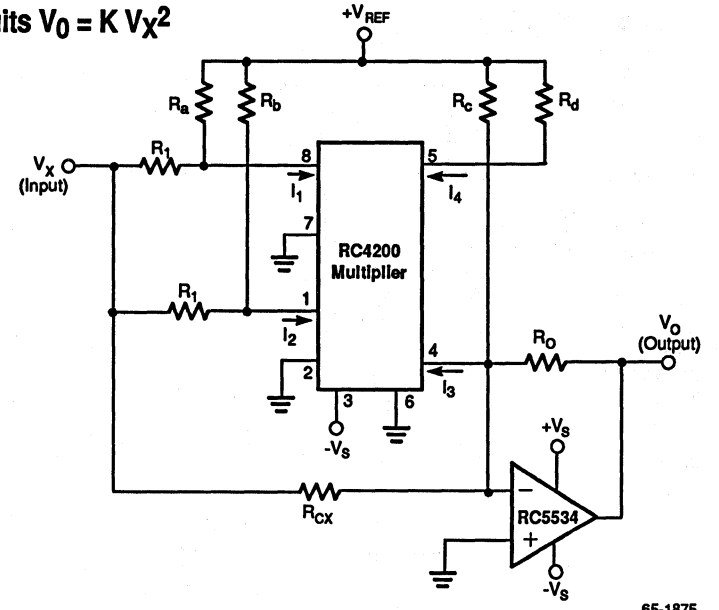
Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (0 to V_X(max.) squarewave on V_X input. Adjust X_{OS}(R_5) for proper peak-to-peak amplitude on V_O output. (Scaling adjust)
3. Connect V_X input to ground. Adjust V_{OS}(R_{13}) for 0V on V_O output.

Figure 10

Linear

Squaring Circuits $V_0 = K V_X^2$



$$\frac{V_X^2}{R_1^2} + \frac{2V_XV_{REF}}{R_1R_a} + \frac{V_{REF}^2}{R_a^2} = \frac{V_0V_{REF}}{R_0R_d} + \frac{V_{REF}^2}{R_cR_d} + \frac{V_XV_{REF}}{R_cR_d}$$

If $R_a^2 = R_cR_d$ and $R_1R_a = 2R_{cx}R_d$

then $\frac{V_0V_{REF}}{R_0R_d} = \frac{V_X^2}{R_1^2}$ or $V_0 = KV_X^2$ where $K = \frac{R_0R_d}{V_{REF}R_1^2}$

$V_X(min.) \leq V_X \leq V_X(max.)$ $\quad \Delta V_X = V_X(max.) - V_X(min.)$

$K = \frac{V_0}{V_X^2}$ (Design Requirement)

$R_1 = \frac{\Delta V_X}{200\mu A}$

$R_a = \frac{\Delta V_X V_{REF}}{250\mu A\, \Delta V_X - 200\mu A\, V_X(max.)}$

$R_d = \frac{V_{REF}}{250\mu A}$

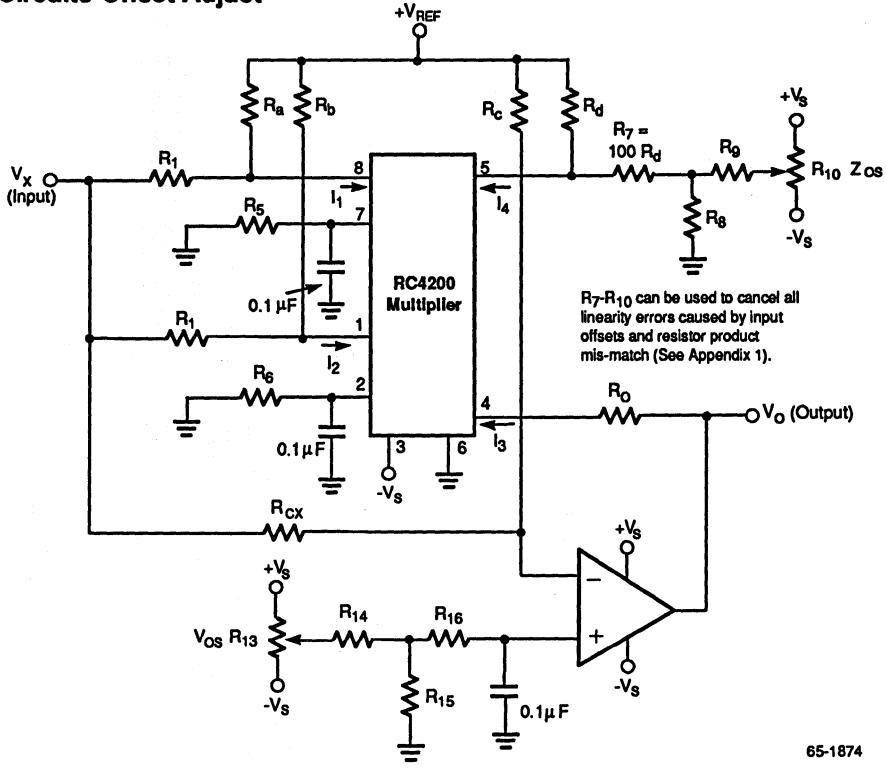
$R_c = \frac{R_a^2}{R_d}$

$R_{cx} = \frac{R_1R_a}{2R_d}$

$R_0 = \frac{\Delta V_X^2 K}{160\mu A}$

Figure 11

Squaring Circuits Offset Adjust



$$10K \leq R_{10}, R_{11} \leq 50K$$

$$R_8, R_{15} = 100\Omega$$

$$R_9, R_{14} = 100\Omega \frac{V_S}{0.1}$$

$$R_5, R_6 = R_1 | |R_a$$

$$R_{16} = R_0 | |R_c| |R_{cx}$$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale ($\pm V_X$) squarewave on V_X input. Adjust $Z_{OS}(R_{10})$ for uniform output.
3. Connect V_X input to ground. Adjust $V_{OS}(R_{11})$ for 0V on V_0 output.

Figure 12

Appendix 1 — System Errors

There are four types of accuracy errors which affect overall system performance. They are:

1. Nonlinearity — Incremental deviation from absolute accuracy. (1)
2. Scaling Error — Linear deviation from absolute accuracy.
3. Output Offset — Constant deviation from absolute accuracy.
4. Feedthrough(2) — Cross-product errors caused by input offsets and external circuit limitations.

The nonlinearity error in the transfer function of the 4200 is ±0.1% max. (±0.03% max. for 4200A).

$$\text{i.e., } I_3 = \frac{I_1 I_2}{I_4} \pm 0.1\%\ \text{F.S.}(4)$$

The other system errors are caused by voltage offsets on the inputs of the 4200 and can be as high as ±3.0% (±2.0% for 4200A).

$$\text{i.e., } V_O = \frac{V_X V_Y}{V_Z}\ \frac{R_O R_4}{R_1 R_2} \pm 3.0\%\ \text{F.S.}(3)(4)$$

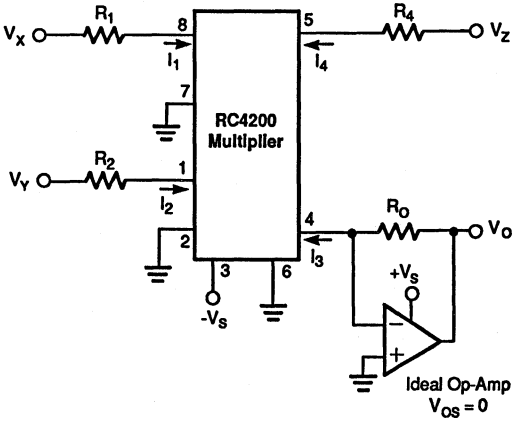


Figure 13

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Notes:

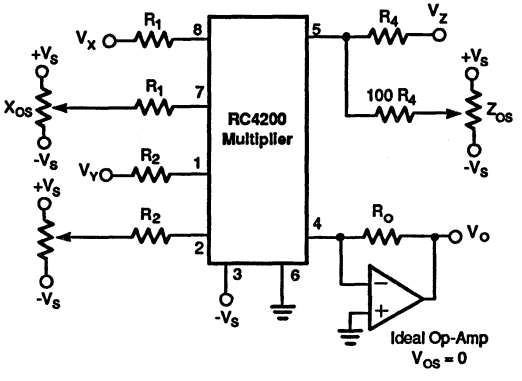
1. The input circuits tend to become unstable at I_1, I_2, $I_4 < 50\ \mu A$ and linearity decreases when I_1, I_2, $I_4 > 250\ \mu A$ (e.g., @ $I_1 = I_2 = 500\ \mu A$ nonlinearity error ≈ 0.5%).
2. This section will not deal with feedthrough which is proportional to frequency of operation and caused by stray capacitance and/or bandwidth limitations. (refer to Figure 21.)
3. Not including resistor tolerance or output offset on the op amp.
4. For $50\ \mu A \le I_1, I_2, I_4 \le 250\ \mu A$.

Errors Caused by Input Offsets

$$V_O = \frac{R_O R_4}{R_1 R_2}\left[\frac{V_X V_Y}{V_Z} \pm \frac{1}{V_Z}\ \underbrace{V_Y V_{OSX}} \pm \underbrace{V_X V_{OSY}} \pm \underbrace{V_O V_{OSZ}} \pm \underbrace{V_{OSX} V_{OSY}}\right]$$

V_Y Feedthrough
V_X Feedthrough
Scaling Error
Output Offset Error

System errors can be greatly reduced by externally trimming the input offset voltages of the 4200. (±3.0% F.S. for 4200 and ±0.1% for 4200A.)



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if; $X_{OS} = X_{OSX}$, $Y_{OS} = Y_{OSY}$, $Z_{OS} = -V_{OSZ}$,

then $V_O\ \frac{V_X V_Y}{V_Z}\ \frac{R_O R_4}{R_1 R_2}\ \pm 0.3\%\ \text{F.S.}(3)$

Figure 14. 4200 with Input Offset Adjustment

Extended Range Circuit Errors

The extended range configurations have a disadvantage in that additional accuracy errors may be introduced by resistor product mismatching.

Multiplier (Figure 6)

An error in resistor product matching will cause an equivalent feedthrough or output offset error:

1. $R_1R_b = R_{CX}R_d \pm\alpha$, V_X feedthrough ($V_Y = 0$) = $\pm\alpha V_X$
2. $R_2R_a = R_{CY}R_d \pm\beta$, V_Y feedthrough ($V_X = 0$) = $\pm\beta V_Y$
3. $R_aR_b = R_CR_d \pm\gamma$, V_0 offset ($V_X = V_Y = 0$) = $\pm\gamma V_{REF}$*

*Output offset errors can always be trimmed out with the output op amp offset adjust, V_{OS} (R_{16}).

Reducing Mismatch Errors (Figure 6)

You need not use .01% resistors to reduce resistor product mismatch errors. Here are a couple of ways to squeeze maximum accuracy out of the extended range multiplier (see Figure 6) using 1% resistors.

Method #1

V_X feedthrough, for example, occurs when $V_Y = 0$ and $V_{OSY} \neq 0$. This V_X feedthrough will equal $\pm V_X V_{OSY}$. Also, if $V_{OSZ} \neq 0$, there is a V_X feedthrough equal to $\pm V_X V_{OSZ}$. A resistor-product error of α will cause a V_X feedthrough of $\pm\alpha V_X$. Likewise, V_Y feedthrough errors are: $\pm V_Y V_{OSX}$, $\pm V_Y V_{OSZ}$ and $\pm\beta V_Y$.

Total feedthrough:
$\pm V_X V_{OSY} \pm V_Y V_{OSX} \pm\alpha V_X \pm\beta V_Y \pm(V_X + V_Y)\, V_{OSZ}$

By carefully adjusting $X_{OS}(R_5)$, $Y_{OS}(R_9)$ and $Z_{OS}(R_{20})$ this equation can be made to very nearly equal zero and the feedthrough error will practically disappear.

A residual offset will probably remain which can be trimmed out with $V_{OS}(R_{16})$ at the output of amp.

Method #2

Notice that the ratios of $R_1R_b : R_{CX}R_d$ and $R_2R_a : R_{CY}R_d$ are both dependent of R_d, also that R_1, R_2, R_a and R_b are all functions of the maximum input requirements. By designing a multiplier for the same input ranges on both V_X and V_Y then $R_1 = R_2$, $R_{CX} = R_{CY}$ and $R_a = R_b$. (Note: It is acceptable to design a four quadrant multiplier and use only two quadrants of it.)

Select R_d to be 1% or 2% below (or above) the calculated value. This will cause α and β to both be positive (or negative) by nearly the same amount. Now the effective value of R_d can be trimmed with an offset adjustment $Z_{OS}(R_{20})$ on pin 5.

This technique will cause: 1) a slight gain error which can be compensated for with the R_0 value, and 2) an output offset error that can be trimmed out with $V_{OS}(R_{16})$ on the output op amp.

Extended Range Divider (Figure 8)

The only cross-product error of interest is the V_Z feedthrough ($V_X = 0$ and $V_{OSX} \neq 0$) which is easily adjusted with $X_{OS}(R_5)$.

Resistor product mismatch will cause scaling errors (gain) that could be a problem for very low values of V_Z. Adjustments to $Y_{OS}(R_{18})$ can be made to improve the high gain accuracy.

Square Root and Squaring (Figures 10 and 12)

These circuits are functions of single variables so feedthrough, as such, is not a consideration. Cross product errors will effect incremental accuracy that can be corrected with $Y_{OS}(R_{14})$ or $Z_{OS}(R_{10})$.

Appendix 2 — Applications

Design Considerations for RMS-to-DC Circuits

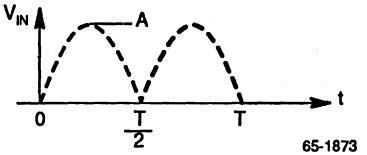
Average Value

Consider $V_{in} = A\sin\omega t$. By definition,

$$V_{AG} = \frac{2}{T}\int_0^{\frac{T}{2}} V_{IN}dt$$

Where T = Period

$$\omega = 2\pi f = \frac{2\pi}{T}$$



65-1873

$$V_{AG} = \frac{2}{T}\int_0^{\frac{T}{2}} A\sin\omega t\,dt$$

$$= \frac{2A}{T}\left[-\frac{1}{\omega}\cos\omega t\right]_0^{\frac{T}{2}}$$

$$= \frac{2A}{2\pi}\left[-\cos(\pi) + \cos(0)\right]$$

Average Value of $A\sin\omega t$ is $\frac{2}{\pi}A$

RMS Value

Again, consider $V_{IN} = A\sin\omega t$

$$V_{rms} = \sqrt{V_{AVG}} = \sqrt{\frac{1}{T}\int_0^T [V_{IN}]^2\,dt}$$

V_{rms} for $A\sin\omega t$ dt:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T A^2\sin^2\omega t\,dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{T}\int_0^T \left[\frac{1}{2} - \frac{1}{2}\cos 2\cos 2\,\omega t\right]dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}\left[\frac{T}{2} - \frac{1}{4\omega}\sin 2\omega t\right]_0^T}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}\left[\frac{T}{2}\right]}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}}$$

therefore, the rms value of $A\sin\omega t$ becomes:

$$V_{rms} = \frac{A}{\sqrt{2}}$$

RMS Value for Rectified Sine Wave

Consider $V_{in} = |A\sin\omega t|$, a rectified wave. To solve, integrate of each half cycle.

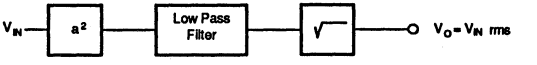
$$\text{i.e. } \frac{1}{T}\int_0^T V_{in}^2\,dt =$$

$$\frac{1}{T}\left[\int_0^{\frac{T}{2}} A^2\sin^2\omega t\,dt + \int_{\frac{T}{2}}^T (-A\sin\omega t)^2 dt\right]$$

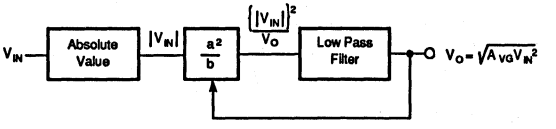
This is the same as $\frac{1}{1}\int_0^T A^2\sin^2\omega t\,dt$

so, $|A\sin\omega t|_{rms} = A\sin\omega t_{rms}$

Practical Consideration: $|A\sin\omega t|$ has high-order harmonics; $A\sin\omega t$ does not. Therefore, non-ideal integrators may cause different errors for two approaches.



(a)



(b)

65-1872

$$\text{Avg}\left[\frac{V_{IN}^2}{V_O}\right] = V_O$$

$$\text{Implies } V_O = \sqrt{\text{Avg}\,(|V_{IN}^2|)}$$

$$V_O = \sqrt{\text{Avg}\,V_{IN}^2}$$

Figure 15

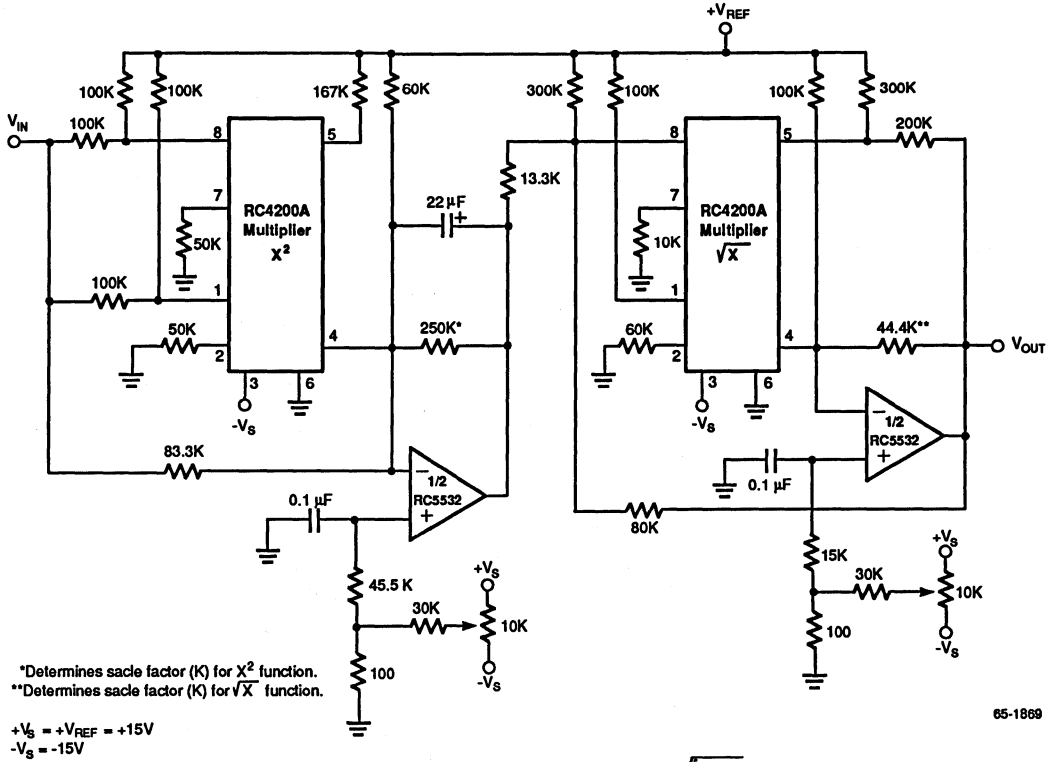


Figure 16. RMS to DC Converter $V_{OUT} = \sqrt{\overline{V_{in}^2}}$

Amplitude Modulator with A.G.C. (Figure 17)

In many AC modulator applications, unwanted output modulation is caused by variations in carrier input amplitude. The versatility of the RC4200 multiplier can be utilized to eliminate this undesired fluctuation. The extended range multiplier circuit (Figure 5) shows an output amplitude inversely proportional to the reference voltage V_{REF}.

$$\text{i.e., } V_0 = \frac{V_X V_Y}{V_{REF}} \quad \frac{R_0 R_d}{R_1 R_2}$$

By making V_{REF} proportional to V_Y (where V_Y is the carrier input) such that:

$$V_{REF} = V_H = \int(|V_Y|),$$

Then the denominator becomes a variable value that automatically provides constant gain, such that the modulating input (V_X) modulates the carrier (V_Y) with a fixed scale factor even though the carrier varies in amplitude.

If V_H is made proportional to the average value of Asinωt (i.e., $2A/\pi$) and scaled by a value of $\pi/2$ then:

$$V_H = A$$

and if: V_X = Modulating input (V_M)

and: V_Y = Carrier input (Asinωt)

Then: $V_0 = K V_M \sin\omega t$ where $K = \frac{R_0 R_d}{R_1 R_2}$

The resistor scaling is determined by the dynamic range of the carrier variation and modulating input.

The resistor values are solved, as with the other extended range circuits, in terms of the input voltages.

Input voltages:

Modulation voltage (V_M): $0 \le V_M \le V_X$(max.)

Carrier (V_Y): $V_Y = A\sin\omega t$

Carrier amplitude fluctuation (ΔA):

$A(\text{min.})\ \text{sin}t \le V_Y \le A(\text{max.})\ \sin\Omega\omega t$

Dynamic Range (N): A(max.)/A(min.),

A(max.) = V_H(max.) and (A(min.) = VH(min.)

Linear

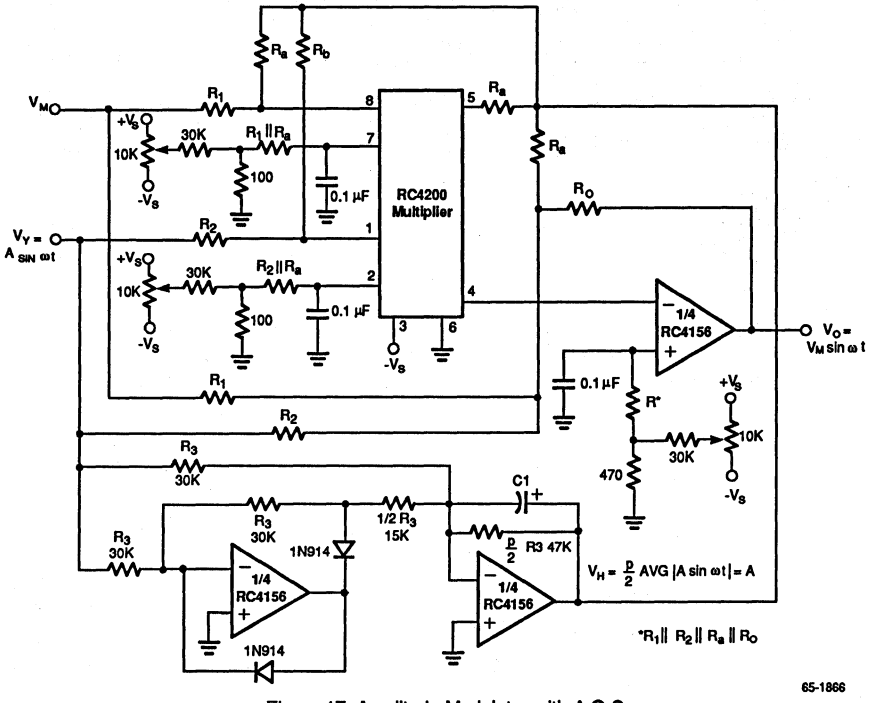


Figure 17. Amplitude Modulator with A.G.C.

The maximum and minimum values for I_1 and I_2 lead to:

$$I_1(max.) = \frac{V_X(max.)}{R_1} + \frac{V_H(max.)}{R_a} = 250\ \mu A$$

$$I_1(min) = \frac{V_H(min.)}{R_a} = 50\ \mu A \quad V_M(min.) = 0$$

$$I_2(max) = \frac{A(max.)}{R_2} + \frac{V_H(max.)}{R_a} = 250\ \mu A$$

$$I_2(min.) = \frac{V_H(min.)}{R_a} = 50\ \mu A$$

For a dynamic range of N, where

$$N = \frac{A(max.)}{A(min.)} < 5,$$

These equations combine to yield:

$$R_1 = \frac{V_X(max.)}{(5 - N)50\mu A}, R_2 \frac{A(max.)}{(5 - N)50\mu A},$$

$$R_a = \frac{A(min.)}{50\mu A} \text{ and } R_O = K \frac{R_1 R_2}{R_a}$$

Example #1

$V_Y = A \sin\omega t$ $2.5V \le A \le 10V$, therefore N = 4
$0V \le V_M \le 10V$, therefore $V_X(max.) = 10V$
K = 1, therefore $V_O = V_M \sin\omega t$

$$R_1 = \frac{V_X(max.)}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_1 = \frac{A(max.)}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_a = \frac{A(min.)}{50\mu A} = \frac{2.5V}{50\mu A} = 50K$$

$$R_O = K \frac{R_1 R_2}{R_a} = 1 \frac{200K \times 200K}{50K} = 800K$$

Example #2

$V_Y = A \sin\omega t$ $3 \le A \le 6$, therefore N = 2
$0V \le V_M \le 8V$, therefore $V_X(max.) = 8V$
K = .2, therefore $V_O = .2\ V_M \sin\omega t$
so:
$R_1 = 53.3K$, $R_2 = 40K$
$R_a = 60K$ and $R_0 = 7.11K$

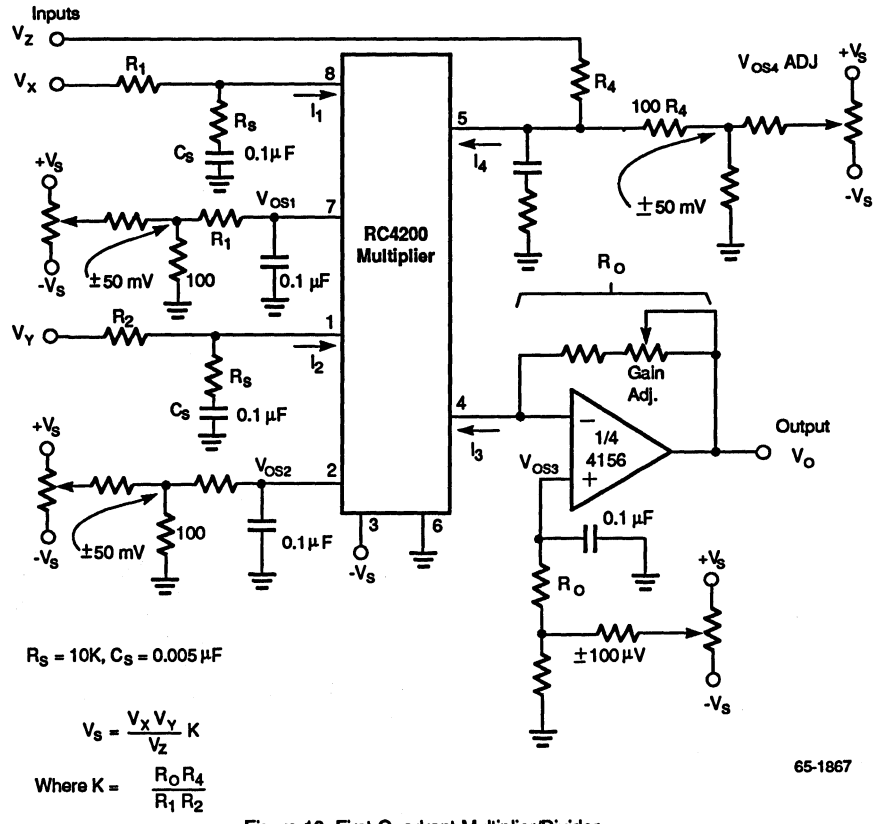


Figure 18. First Quadrant Multiplier/Divider

Limited Range, First Quadrant Applications

The following circuit has the advantage that cross-product errors are due only to input offsets and nonlinearity error is slightly less for lower input currents.

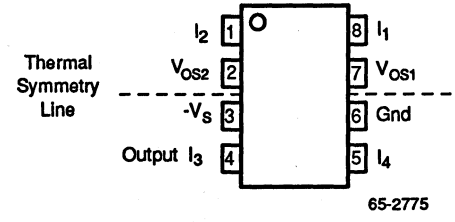
The circuit also has no standby current to add to the noise content, although the signal-to-noise ratio worsens at very low input currents (1-5 µA) due to the noise current of the input stages.

The R_SC_S filter circuits are added to each input to improve the stability for input currents below 50 µA.

Caution

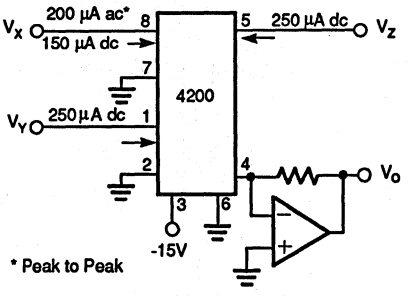
The bandpass drops off significantly for lower currents (<50 µA) and non-symmetrical rise and fall times can cause second harmonic distortion.

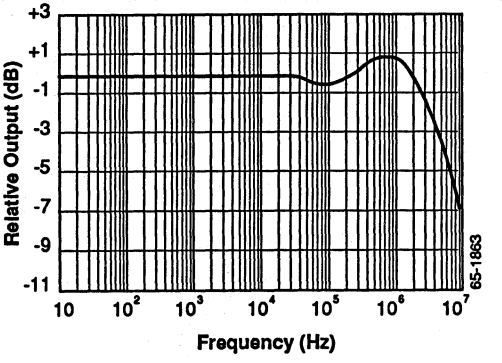
Thermal Symmetry

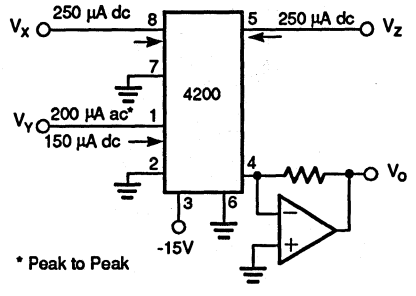


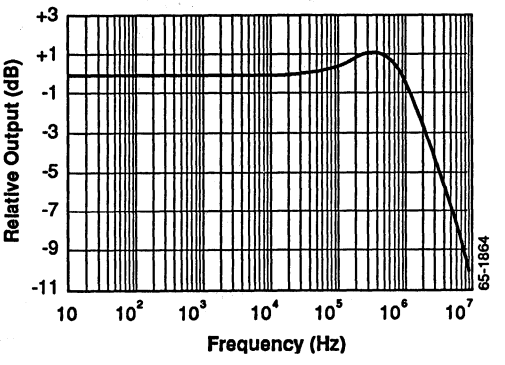
The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that sources generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.

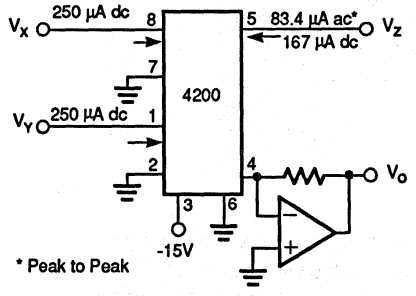
Linear


V_X
200 µA ac*
150 µA dc
8
5
250 µA dc
V_Z
7
4200
V_Y
250 µA dc
1
2
4
V_o
3
6
-15V
* Peak to Peak


+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-1863


V_X
250 µA dc
8
5
250 µA dc
V_Z
7
4200
V_Y
200 µA ac*
150 µA dc
1
2
4
V_o
3
6
-15V
* Peak to Peak


+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-1864


V_X
250 µA dc
8
5
83.4 µA ac*
167 µA dc
V_Z
7
4200
V_Y
250 µA dc
1
2
4
V_o
3
6
-15V
* Peak to Peak

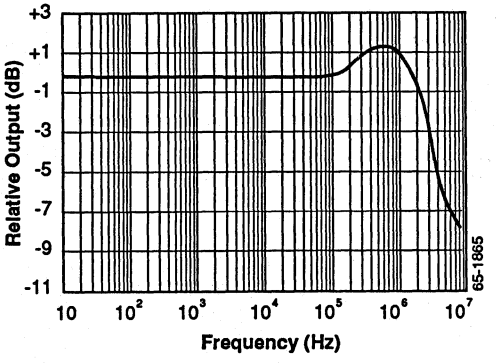

+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-1865

Figure 19

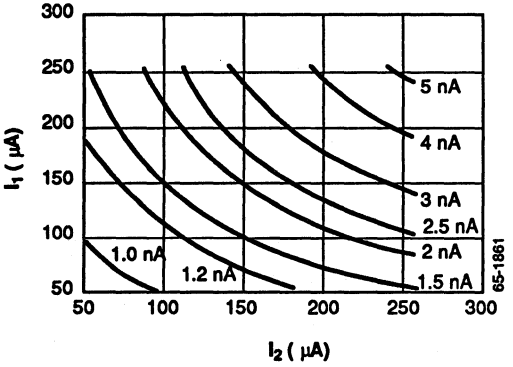


Figure 20a. Output Noise Current (I_3) vs. Input Currents (I_1, I_2) for I_4 = 250 μA

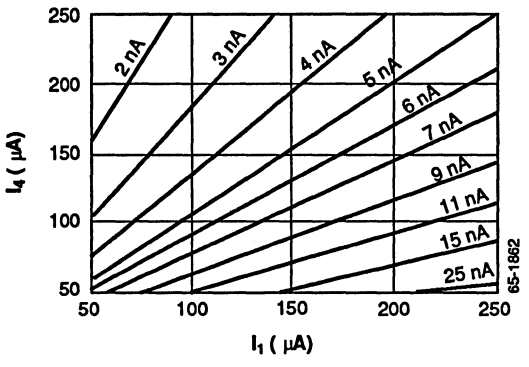


Figure 20a. Output Noise Current (I_3) vs. Input Currents (I_4, I_1) for I_2 = 250 μA

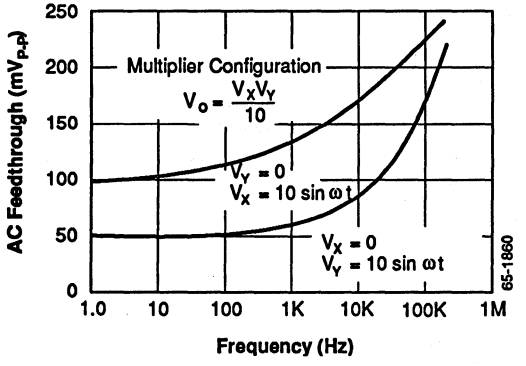
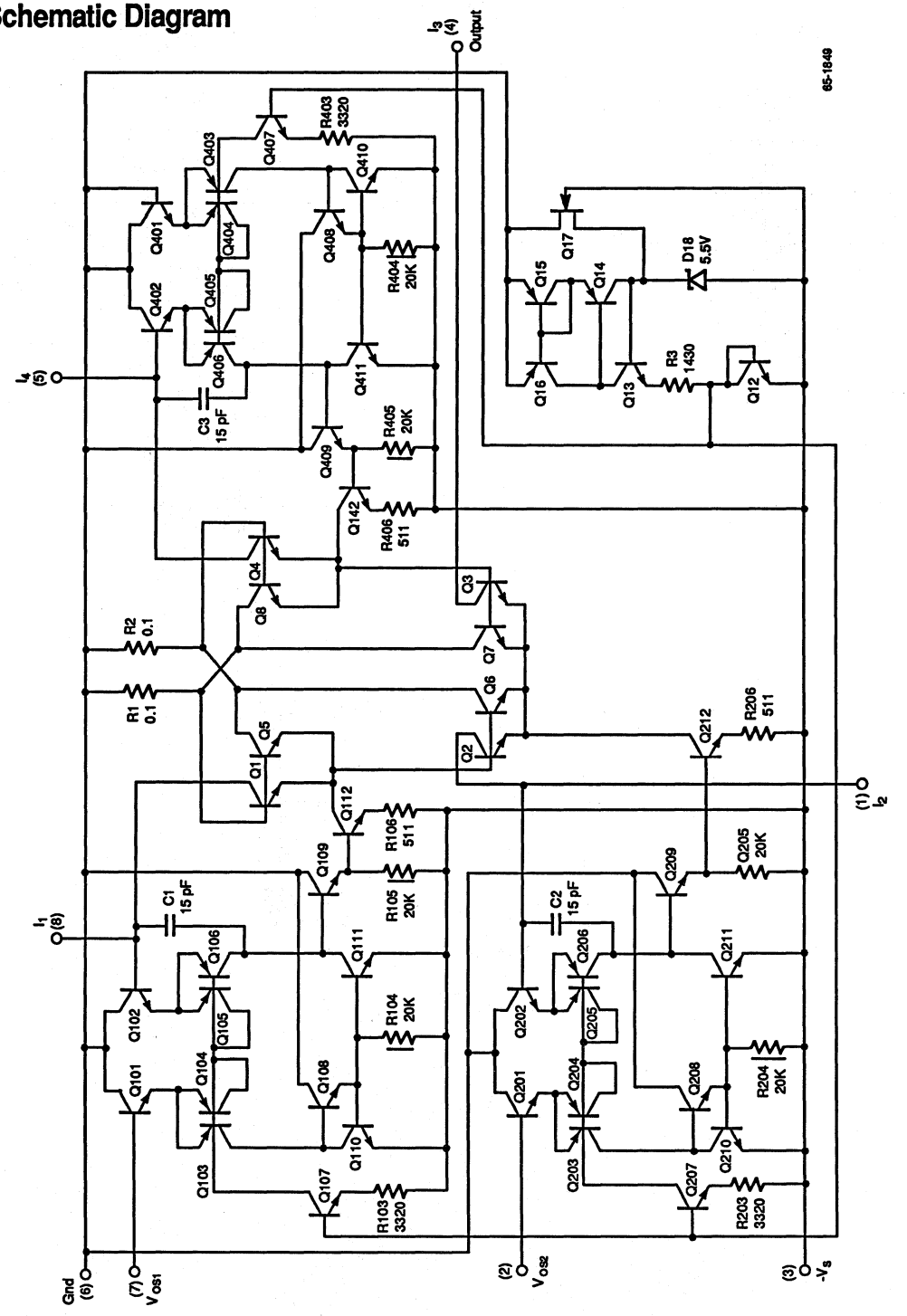


Figure 21. AC Feedthrough vs. Frequency

Schematic Diagram



RC4444
4 x 4 x 2 Balanced Switching Crosspoint Array

Description

The RC4444 is a monolithic dielectrically isolated crosspoint array arranged into a 4 x 4 x 2 matrix. The primary application is for balanced switching of 600Ω transmission lines. The ring and tip are selected by selective biasing of the P+ and P- gate.

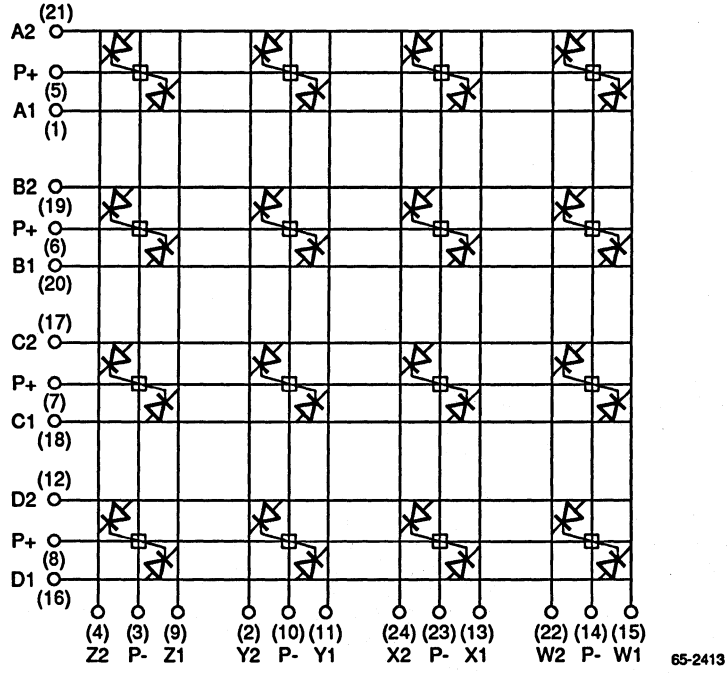
Designed to replace reed relays in telephone switchboards, it does not require a constant gate drive to keep the SCR in the "ON" condition. It is several orders faster, with no bouncing, and has a much longer operating life than its mechanical counterpart.

The 16 SCR pairs with the gating system are packaged in a 24-pin dual in-line package.

Features

- Low bi-directional R_{ON}
- High R_{OFF}
- Excellent matching of gates
- Low capacitance
- High rate firing
- Predictable holding current

Block Diagram



Absolute Maximum Ratings

Operating Voltage ..... +25V
Operating Current per Crosspoint ..... 100 mA
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C
Lead Soldering Temperature ..... +300°C
(60 sec)

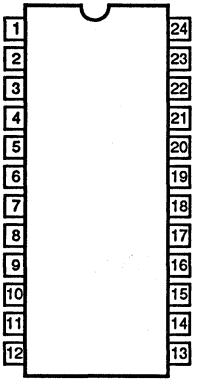
Notes: 1. Maximum voltage from anode to cathode.

Thermal Characteristics

	24-Lead Plastic DIP	24-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A < 50°C	555 mW	1042 mW
Therm. Res θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	135°C/W	120°C/W
For T_A > 50°C Derate at	7.41 mW/°C	8.33 mW/°C

Connection Information

24-Lead
Dual In-Line Package
(Top View)



65-0695

Pin	Function	Pin	Function
1	Anode A1	13	Cathode X1
2	Cathode Y2	14	Row Select W
3	Row Select Z	15	Cathode W1
4	Cathode Z	16	Anode D1
5	Column Select A	17	Anode C2
6	Column Select B	18	Anode C1
7	Column Select C	19	Anode B2
8	Column Select D	20	Anode B1
9	Cathode Z1	21	Anode A2
10	Row Select Y	22	Cathode W2
11	Cathode Y1	23	Row Select X
12	Anode D2	24	Cathode X2

Ordering Information

Part Number	Package	Operating Temperature Range
RC4444N	N	0°C to +70°C
RC4444D	D	0°C to +70°C

Notes:
N = 24-lead 600 wide plastic DIP
D = 24-Lead 600 wide Ceramic DIP

Electrical Characteristics

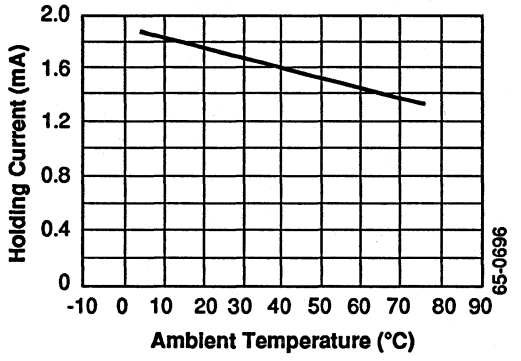
($0°C \leq T_A \leq +70°C$ unless otherwise specified)

Parameters	Test Conditions	RC4444 Min	RC4444 Typ	RC4444 Max	Units
Anode-Cathode Breakdown Voltage	I_{AK} = 25 µA	25			V
Cathode-Anode Breakdown Voltage	I_{AK} = 25 µA	25			V
Base-Cathode Breakdown Voltage	I_{BK} = 25 µA	25			V
Cathode-Base Breakdown Voltage	I_{KB} = 25 µA	25			V
Base-Emitter Breakdown Voltage	I_{BE} = 25 µA	25			V
Emitter-Cathode Breakdown Voltage	I_{EK} = 25 µA	25			V
OFF State Resistance	V_{AK} = 10V	100			MΩ
Dynamic ON Resistance	Center Current = 10 mA Center Current = 20 mA	4.0 2.0		12 10	Ω
Holding Current		0.9		3.8	mA
Enable Current	V_{BE} = 1.5V (Fig. 2)	4.0			mA
Anode-Cathode ON Voltage	I_{AK} = 10 mA I_{AK} = 20 mA			1.0 1.1	V
Gate Sharing Current	Under Select Conditions	0.8		1.25	mA/mA
Ratio at Cathodes	with Anodes Open (fig. 1)	0.8		1.25	mA/mA
Inhibit Voltage	V_B = 3.0V (Fig. 3)			0.3	V
Inhibit Current	V_B = 3.0V (Fig. 3)			0.1	mA
OFF State Capacitance	V_{AK} = 0V			2.0	pF
Turn-ON Time	(Fig. 5)			1.0	µs
Minimum Voltage Ramp	Which Could Fire the SCR Under Transient Conditions (Figure 5)	800			V/µs

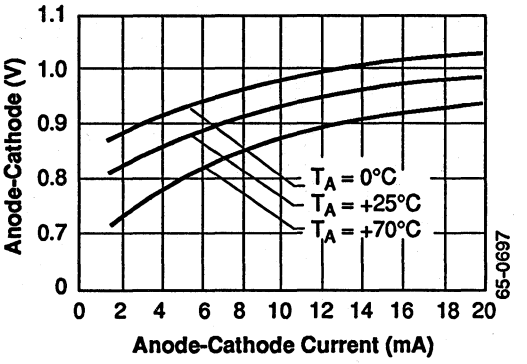
Linear

Typical Performance Characteristics

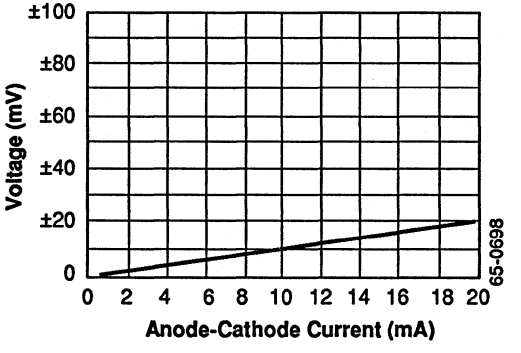
Holding Current vs. Ambient Temperature



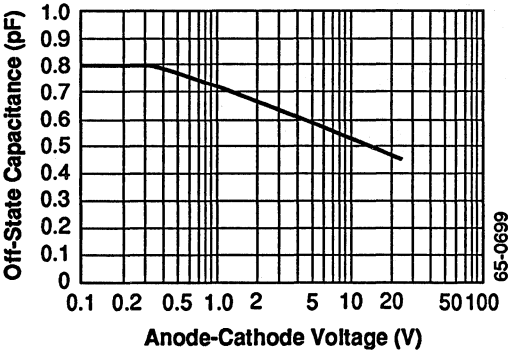
Anode-Cathode on Voltage vs.
Current and Temperature



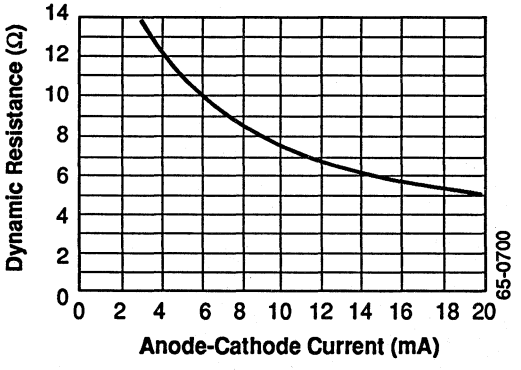
Difference In Anode-Cathode on Voltage
(Between Associate Pairs of SCRs)
vs. Anode-Cathode Current



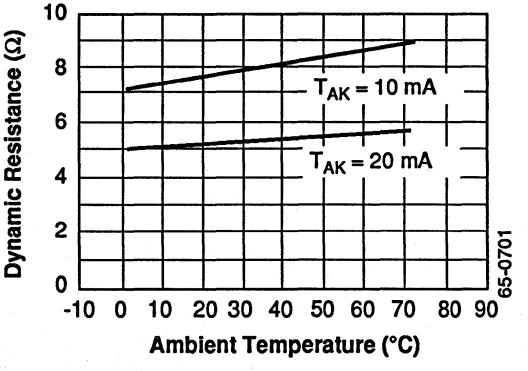
Off-site Capacitance vs. Anode-Cathode Voltage



Dynamic on Resistance vs.
Anode-Cathode Current

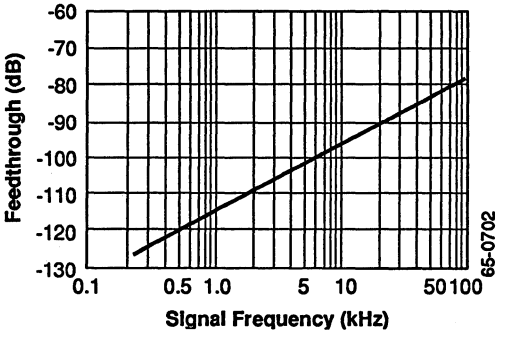


Dynamic on Resistance vs. Ambient Temperature

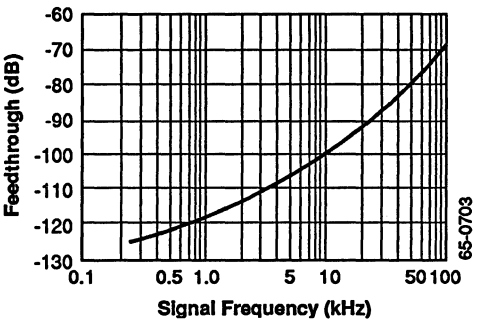


Typical Performance Characteristics (Continued)

Feedback vs. Signal Frequency



Crosstalk vs. Signal Frequency



Test Circuits

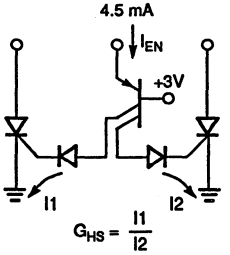


Figure 1. Test Circuit for Gate Sharing Current Ratio

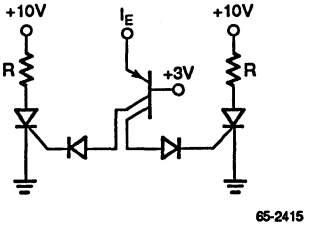


Figure 2. Enable Current (Both SCRs Must Turn On)

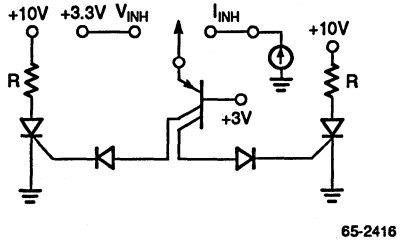


Figure 3. Inhibit Voltage and Inhibit Current (Both SCRs Must Remain Off)

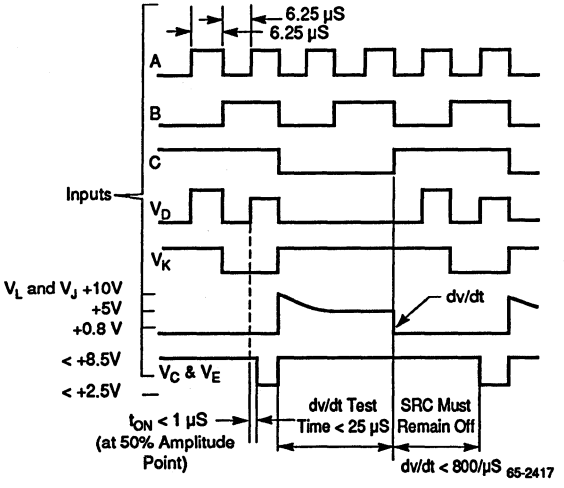


Figure 4. Test Waveforms for dv/dt and t_{on}

Linear

Test Circuits (Continued)

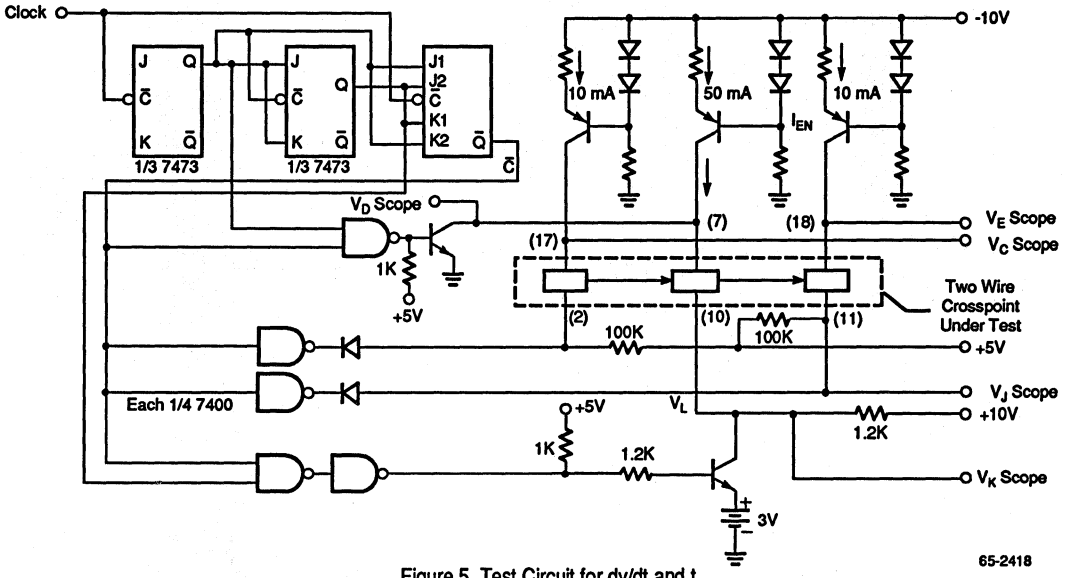
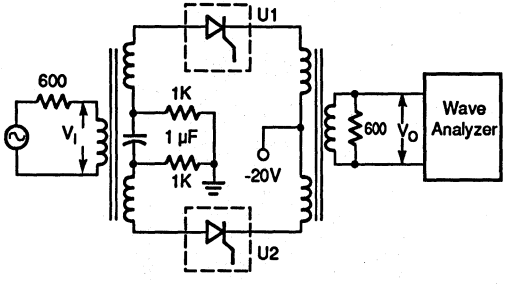


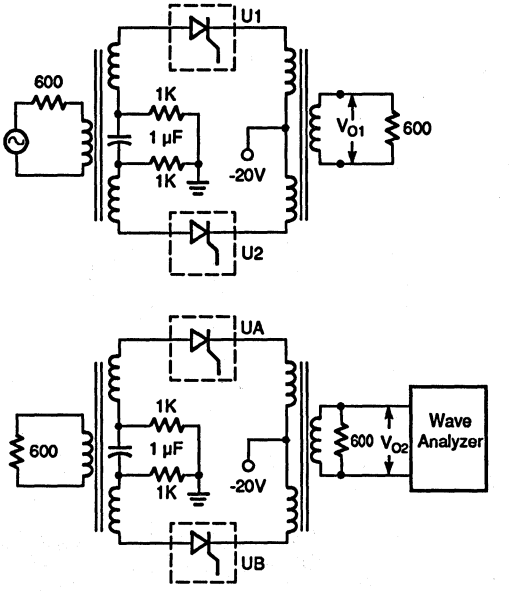
Figure 5. Test Circuit for dv/dt and t_{ON}



T_A = +25°C, V_I = 12 dBm, Crosspoints Off
Feedthrough = 20 Log_{10} (V_O/V_I)

65-2049

Figure 6. Test Circuit for Feedthrough vs. Frequency



T_A = +25°C, V_I = 12 dBm, Crosspoinst On
Feedthrough = 20 Log_{10} (V_{O2}/V_{O1})

65-2050

Figure 7. Test Circuit for Crosstalk vs. Frequency

Typical Applications

The RC4444 crosspoint switch is designed to provide a low-loss analog switching element for telephony signals. It can be addressed and controlled from standard binary decoders and is CMOS compatible. With proper system organization, the RC4444 can significantly reduce the size and cost of existing crosspoint matrices.

Signal Path Considerations

The RC4444 is a balanced 4 x 4 2-wire crosspoint array. It is ideal for balanced transmission systems, but may be applied effectively in a number of single ended applications. Multiple chips may be interconnected to form larger crosspoint arrays. The major design constraint in using SCR crosspoints is that a forward DC current must be maintained through the SCR to retain an AC signal path. This requires that each subscriber-input to the array be capable of sourcing DC current as well as its AC signal. With each subscriber acting as a DC source, each trunk output then acts as a current sink. The instrument-to-trunk connection in Figure 8 shows this configuration. However, with each subscriber acting as a DC source, some method of interconnecting them without a trunk must be provided. Such a local or intercom termination is shown in Figure 9. Here both subscribers source DC current and exchange AC signals. The central current sink accepts current from both subscribers while the high output impedance of the current sink does not disturb the system.

These configurations are system compatible. The DC current restriction is not a restriction in the design of an efficient crosspoint array. Because of the current sink terminations, a signal path may use differing numbers of crosspoints in any connection or in two sides of the same connection further relaxing restrictions in array design.

Figure 10 demonstrates circuit operation. S1, S2 and S3 are open. The Crosspoint SCRs are off as they have not gate drive or DC current path through S1. By closing S2 and S3, gate drive is provided, but the SCRs still remain off as there is no DC current path to hold them on. Close S1 and the circuit is enabled, but with S2 and S3 off there is still no signal path. Closing S2 and S3 with S1 closed — current is injected into both gates and they switch on. DC current through R_L splits around the center-tapped winding and flows through each SCR, back through the lower winding and through S1 to ground. If S2 and S3 are opened, that current path still remains and the SCRs remain on. If an AC signal is injected at either G1 or G2, it will be transmitted to the other signal port with negligible loss in the SCRs. To disconnect the AC signal path, the SCRs must be commutated off. By opening S1 the DC current path is interrupted and the SCRs switch off. The AC signal path is disconnected. With S1 closed, the circuit is enabled and may be addressed again from S2 and S3. This circuit demonstrates a balanced transmission configuration. The transmission characteristics of the SCRs simulate a relay contact in that the AC signal does not incur a contact voltage drop across the crosspoint. The memory characteristics of the crosspoint are demonstrated by the selective application of S1, S2, and S3.

The selection of R_L is governed by the power supply voltage and the desired DC current. If 10 mA is to flow through each SCR then R_L must pass 20 mA. Thus, $(+V_S - V_{AK})/R_L = 20$ mA. The selection of R_P is governed by the characteristics for crosspoint turn on. Adequate enable current must be injected into the column select and R_P should drop at least 1.5V. The PNP transistor has a typical gain of one. Thus, R_P should pass at least 2 mA to provide 4 mA column select current.

Addressing Considerations

The RC4444 crosspoint switch is addressed by selecting and turning on the PNP transistor that controls the SCR pair desired. The drive requirements of the RC4444 can be met with standard CMOS outputs. A particular crosspoint is addressed by putting a logical "1" on the emitter and a logical "0" on the base of the appropriate transistor. A resistor in the base circuit of the transistor is required to limit the current and must also drop 1.5V to assure forward bias of the two diodes in the collector circuits.

The gate current required for SCR turn on is 1 mA typically. CMOS one-of-n decoders are available that provide both active high and active low outputs and are well suited for standard addressing organizations. The major design constraint in organizing the addressing structure is that any signal path which is to be addressed must create a DC path from a source to a sink. If that path requires two crosspoints, they must be addressed simultaneously. Of course, once the path is selected, the addressing hardware is free to initiate other signal paths. To meet the DC path requirement, crosspoint arrays should be designed in block such that any give DC path required only one crosspoint per block. A signal path, however, may still use two crosspoints in the same block by sequentially addressing two DC paths to the same terminator. For example, the left or right pairs of crosspoints in Figure 9 must be addressed simultaneously but the left pair may be addressed in sequence after addressing the right pair. This is not a difficult constraint to meet and it does not require unnecessary addressing hardware.

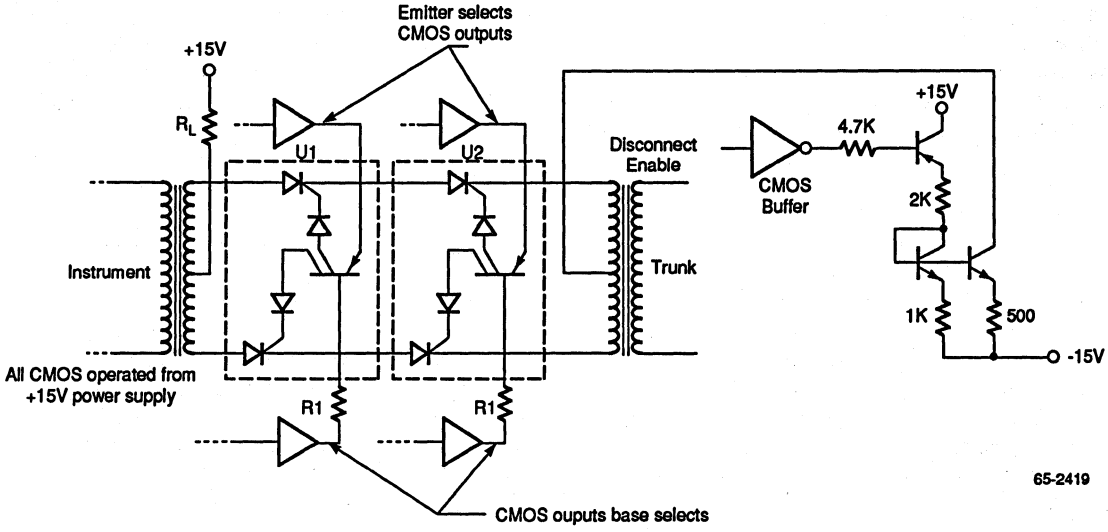


Figure 8. Instrument-to-Trunk Connection

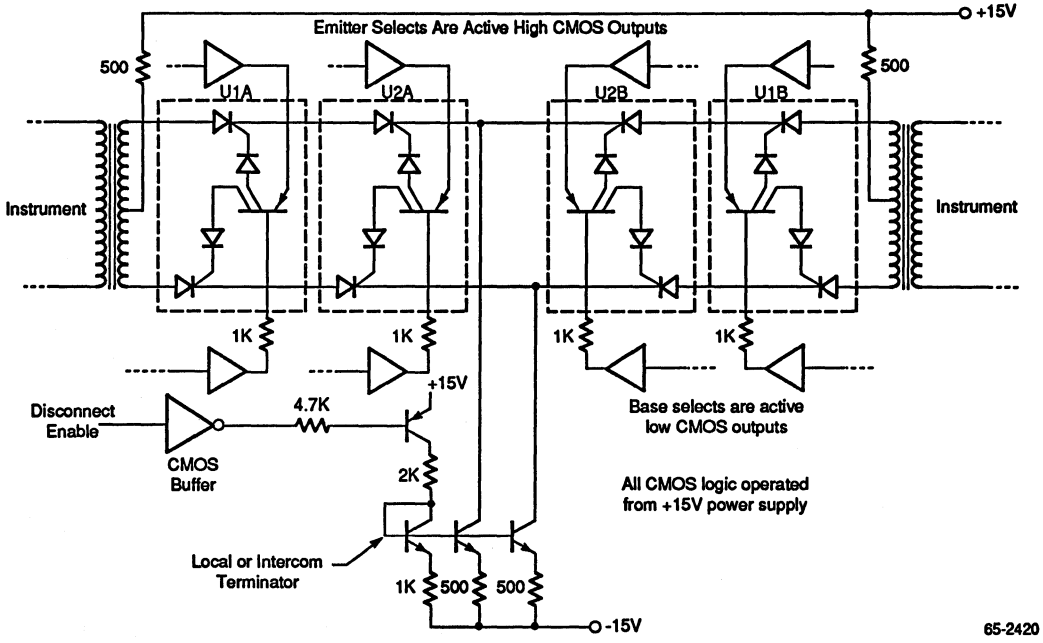
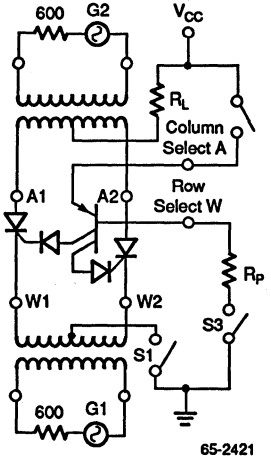


Figure 9. Typical Instrument-to-Instrument Connection

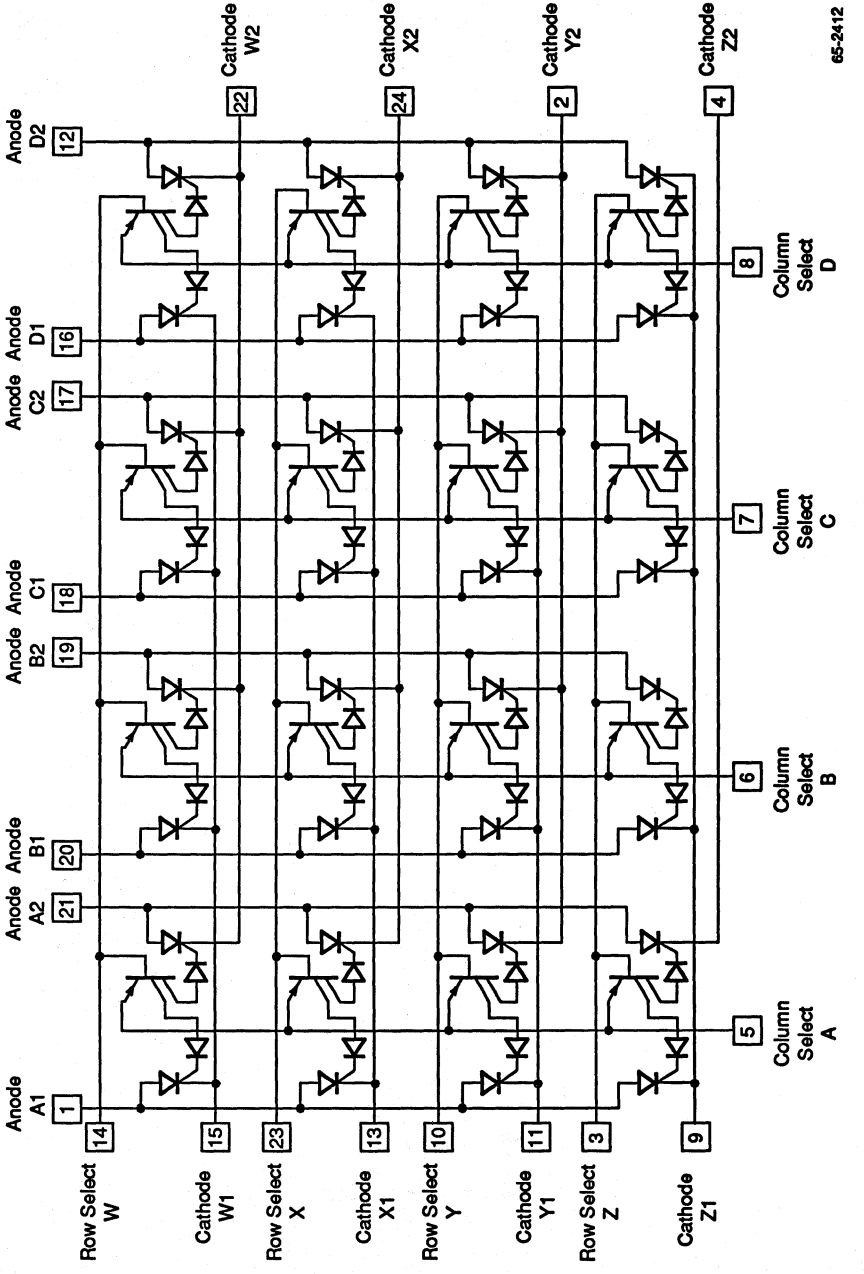


S1	S2	S3	Line Condition
On	X	Off	Enabled, Not Connected
On	Off	X	Enabled, Not Connected
On	On	On	Addressed and Connected
On	X	X	G1 Connected to G2
Off	X	X	Disconnected

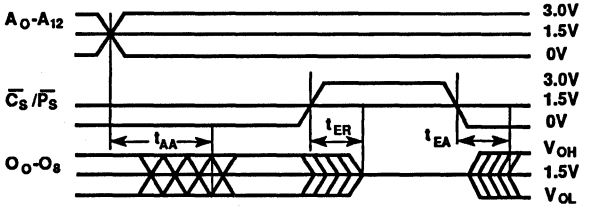
X = Don't Care

Figure 10. Crosspoint Operation Demonstration Circuit

Simplified Schematic Diagram



PROMs



Keys to Timing Diagram

Waveforms	Inputs	Outputs
———	Must be Steady	Will be Steady
———		
XXX	Don't Care. Any Change Permitted	Changing State Unknown
><	Does Not Apply	Center Line is High Impedance Off State

65-4060A

Raytheon Semiconductor bipolar PROMs feature full Schottky clamping and three-state outputs. The devices are available in four- and eight-bit wide JEDEC standard configurations. The PROMs employ nichrome fuse links, which store a logical HIGH and are programmed to a LOWstate. Chip select inputs provide logic flexibility and ease of memory expansion decoding. The devices contain an internal test row and column, which are accessed and programmed during wafer sort test. These fuses ensure a high programming yield and guarantee AC performance and DC parameters.

Raytheon Semiconductor's PROM series includes standard performance and power-switched versions. The devices are available in different speed and package options.

Raytheon Semiconductor's memory products have a high immunity, or resistance, to total dose, neutron fluence and dose rate radiation. Our memory products are well-suited for military and aerospace applications.

Screening Options Available:

- Level S
- JAN Class B
- Standardized Military Drawing (SMD)
- Class B
- Source Control Drawing (SCD)
- Military Temperature Range
- Commercial Temperature Range

Raytheon offers JAN and Standardized Military Drawing product as off-the-shelf devices, on a direct OEM basis or through distributors.

PROM Selection Guide

Product	Size	Organization	Enable (1)	Outputs	Raytheon Package Designator	MIL-STD-1835 Case Outline	θ_{JC} °C/W	Max ICC Power Supply Current	Max ICCD Power Down Supply Current
R29621/1A	4K	512X8	$\overline{CS}$	TS	D	D-8	<11	155 mA	
R29623/3A	4K	512X8	$\overline{PS}$	TS	D	D-8	<11		45 mA
R29631/1A	8K	1024X8	$\overline{CS}^1$, $\overline{CS}^2$	TS	D	D-3	<11	170 mA	
			CS^3, CS^4		L	C-4	<10		
					F	F-6	<10		
R29633/3A	8K	1024X8	$\overline{PS}^1$, $\overline{PS}^2$	TS	D	D-3	<11		45 mA
			PS^3, PS^4		L	C-4	<10		
					F	F-6	<10		
R29651/1A	8K	2048X4	$\overline{CS}$	TS	D	D-6	<11	170 mA	
R29653/3A	8K	2048X4	$\overline{PS}$	TS	D	D-6	<11		45 mA
R29681/1A[2]	16K	2048X8	$\overline{CS}^1$	TS	S	D-9	<11	180 mA	
			CS^2, CS^3		D	D-3	<11		
					L	C-4	<10		
R29683/3A[2]	16K	2048X8	$\overline{PS}^1$	TS	S	D-9	<11		50 mA
			$\overline{PS}^2$, PS^3		D	D-3	<11		
					L	C-4	<10		
R29771	32K	4096X8	$\overline{CS}^1$, CS^2	TS	S	D-9	<11	190 mA	
					D	D-3	<11		
					L	C-4	<10		
					F	F-6A	<10		
R29773	32K	4096X8	$\overline{PS}^1$, PS^2	TS	S	D-9	<11		55 mA
					D	D-3	<11		
					L	C-4	<10		
					F	F-6A	<10		
R29791	64K	8192X8	$\overline{CS}$	TS	S	D-9	<11	190 mA	
					D	D-3	<11		
					F	F-64A	<10		
R29793	64K	8192X8	$\overline{PS}$	TS	S	D-9	<11		50 mA
					D	D-3	<11		
					F	F-6A	<10		

Notes:
1. $\overline{CS}$/CS = Chip Select for PROM
   $\overline{PS}$/PS = Chip Select for SPROM
2. Contact Factory regarding flat pack package.

JAN Ordering Information

MIL-M-38510 Slash Sheet Part Number	Raytheon Part Number
MIL-M-38510/20902BVA	JR29651DQ (2K X 4, 18-pin ceramic DIP)
MIL-M-38510/20904BJA	JR29631DR (1K X 8, 24-pin ceramic DIP)
MILOM-38510/21002BJA	JR29681DR (2K X 8, 24-pin ceramic DIP)

Raytheon Semiconductor CAGE Code — 07933

R296XX/R297XX
Standard PROMs and Power-Switched SPROMs

Description

Raytheon Semiconductor's Bipolar Field Programmable Read-Only Memories include both standard and power-switched versions. CS/PS inputs provide logic flexibility and ease of memory expansion decoding. SPROM power-switch circuitry is activated by the PS input.

Raytheon PROMs and SPROMs are manufactured with nichrome fuses and low power Schottky technology. The devices are shipped with all bits in the HIGH (logical ONE) state. To achieve a LOW state in a given bit location the nichrome link is fused open by passing a short, high current pulse through the link. All devices are programmed using the same programming technique.

Standard PROMs are enabled by a single active LOW CS or by both active LOW $\overline{CS}$ and high $\overline{CS}$ inputs. Power-switched PROMs (SPROMs) are enabled by a single active LOW $\overline{PS}$ or by both active LOW $\overline{PS}$ and HIGH PS inputs. See the individual block diagrams for the enable scheme.

Features

- Devices are available in military (-55°C to +125°C) temperature range
- Standard PROMs are offered in power-switched SPROM versions
- Typically, 75% power savings achieved by deselected SPROMs
- Reliable nichrome fuses
- Three-state outputs
- Devices programmed on standard PROM programmers
- High immunity or resistance to high levels of constant or burst radiation
- Device pinouts comply with JEDEC standards
- Available in surface mount and through-hole packaging
- PROMs and SPROMs are offered in 24-pin, 0.3" wide DIPs

Applications

- Microprogram control store
- Microprocessor program store
- Programmable logic
- Custom look-up tables
- Security encoding/decoding
- Code converter
- Character generator
- Use in redundant systems

Absolute Maximum Ratings

(above which the useful life may be impaired)

Supply Voltage to Ground Potential (continuous), V_{CC} ..... -0.5V to +7.0V
DC Input Current ..... -30 mA to +5.0 mA
DC Input Voltage (address inputs) ..... -0.5V to +5.5V
DC Input Voltage (chip/power select input pin)
R296XX ..... -0.5V to +33V
R297XX ..... -0.5V to +28V
DC Voltage Applied to Outputs (except during programming) ..... -0.5V to +V_{CC} max.
Output Current into Outputs During Programming ..... 240 mA
DC Voltage Applied to Outputs During Programming
R296XX 26V
R297XX 24V
Junction Temperature ..... +175°C
Storage Temperature ..... -65°C to +150°C
Programming Temperature ..... 25 ±5°C
Lead Temperature (soldering, 10 seconds) ..... 300°C
Current Density (metallization) ..... < 5 x 10^5A/cm²
Thermal Resistance, Junction-to-Case θ_{JC}
Dual-In-Line ..... ≤ 11°C/W
Leadless Chip Carrier ..... ≤ 10°C/W
Flat Pack ..... ≤10°C/W

Operating Conditions

Parameter	Description	Military		Unit
		Min.	Max.	
V_{CC}	Supply Voltage	4.5	5.5	V
T_C	Case Operating Temperature	-55	+125	°C
V_{IL1}[1]	DC/Functional Low Level Input Voltage		0.8	V
V_{IH}[1]	DC/Functional High Level Input Voltage	2.0		V
V_{IL}	AC Low Level Input Voltage		0	V
V_{IH}	AC High Level Input Voltage	3.0		V

Note:

1. Functional tests shall be conducted at input test conditions as follows: $V_{IH} = V_{IH}$(min) +20%, -0%; $V_{IL} = V_{IL}$(max) +0%, -50%. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to V_{IH}(min) and V_{IL}(max). CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that V_{IH}(min) and V_{IL}(max) requirements are not violated at the device terminals.

Electrical Characteristics

Over Operating Range

Devices conform to MIL-STD-883, Group A, Subgroups 1, 2 and 3

Parameter	Description	Test Conditions			Min	Max	Units
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -2 mA V_{IN} = V_{IH} or V_{IL}			2.4		V
V_{OL}(1)	Output Low Voltage	V_{CC} = Min,	I_{OL} = 8 mA			0.4	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA			0.5	
I_{IL}	Input Low Current	V_{CC} = Max, V_{IN} = 0.4V		R296XX		-250	µA
				R297XX		-100	
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 2.7V				10	µA
		V_{CC} = Max, V_{IN} = 5.5V				40	
I_{OS}(2)	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.2V(3)			-15	-85	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18 mA				-1.2	V
I_{CEX}	Output Leakage Current	V_{CC} = Max,	V_{OUT} = 5.5V			+40	µA
		Chip Disabled	V_{OUT} = 0.4V			-40	

Notes:
1. This characteristic cannot be tested prior to programming; it is guaranteed by factory testing.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not exceed 1 second.
3. V_{OUT} = 0.0V for R29791/R29793
4. Typical C_{IN} = 5 pF

Pin Names

Symbol	Description
A^0— A^n	Address Inputs
$\overline{CS}$	Chip Select Active Low (PROM)
CS	Chip Select Active High (PROM)
$\overline{PS}$	Chip Select Active Low (SPROM)
PS	Chip Select Active High (SPROM)
O^1— O^n	Data Outputs

512 x 8 PROM — R29621/R29621A

Power and AC Characteristics Over Operating Range

ICC conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits		Units
			29621AM	R29621M	
I_{CC}	Power Supply Current	V_{CC} = Max All Inputs GND	155	155	mA
t_{AA}	Address Access Time	C_L = 30 pF*,	60	80	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	40	40	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	40	40	ns
P_D	Power Dissipation		853	853	mW

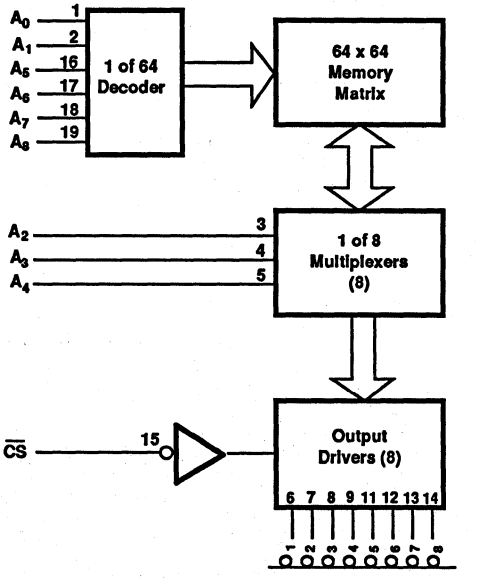
*See AC Test Load Circuit and Switching Waveforms

Ordering Information

Part Type	Package	Operating Temperature Range
R29621DM	D	-55°C to +125°C
R29621DM/883B	D	-55°C to +125°C
R29621DMS	D	-55°C to +125°C
R29621ADM	D	-55°C to +125°C
R29621ADM/883B	D	-55°C to +125°C
R29621ADMS	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 20-lead ceramic DIP

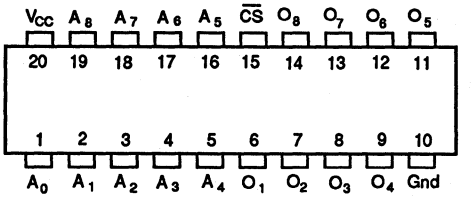
Block Diagram



65-0112

Pin-Out Information

Dual In-Line Package



Pin 15 is also the programming pin (pp)

65-1314

512 x 8 SPROM — R29623/R29623A

Power and AC Characteristics Over Operating Range

ICC conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits		Units
			R29623AM	R29623M	
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max $\overline{PS} = V_{IH}$, All other inputs = GND	45	45	mA
I_{CC}	Supply Current (enabled)	V_{CC} = Max All inputs = Gnd	155	155	mA
t_{AA}	Address Access Time	C_L = 30 pF *	60	85	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	65	85	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	40	40	ns
P_D	Power Dissipation (Disabled)		248	248	mW
P_D	Power Dissipation (Enabled)		853	853	mW

*See AC Test Load Circuit and Switching Waveforms

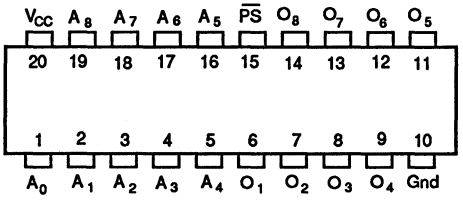
Ordering Information

Part Type	Package	Operating Temperature Range
R29623DM	D	-55°C to +125°C
R29623DM/883B	D	-55°C to +125°C
R29623DMS	D	-55°C to +125°C
R29623ADM	D	-55°C to +125°C
R29623ADM/883B	D	-55°C to +125°C
R29623ADMS	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 20-lead ceramic DIP

Pin Out Information

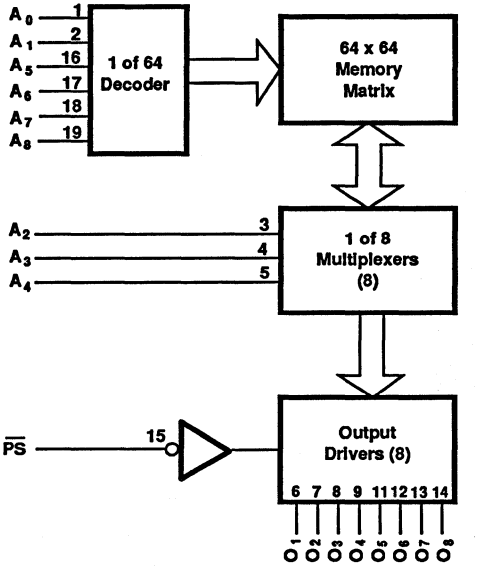
Dual In-Line Package



Pin 15 is also the programming pin (pp)

65-1316

Block Diagram



65-0113

PROM

1024 x 8 PROM — R29631/R29631A

Power and AC Characteristics Over Operating Range

ICC conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29631AM	Maximum Limits R29631M	Units
I_{CC}	Power Supply Current	V_{CC} = Max All inputs = Gnd	170	170	mA
t_{AA}	Address Access Time	C_L = 30 pF *	60	90	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	40	40	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	40	40	ns
P_D	Power Dissipation		935	935	mW

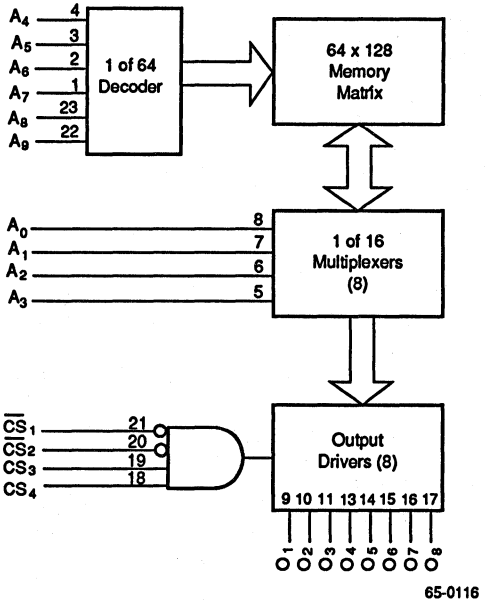
*See AC Test Load Circuit and Switching Waveforms

Ordering Information

Part Type	Package	Operating Temperature Range
R29631DM	D	-55°C to +125°C
R29631DM/883B	D	-55°C to +125°C
R29631DMS	D	-55°C to +125°C
R29631FM	F	-55°C to +125°C
R29631FM/883B	F	-55°C to +125°C
R29631FMS	F	-55°C to +125°C
R29631ADM	D	-55°C to +125°C
R29631ADM/883B	D	-55°C to +125°C
R29631AFMS	D	-55°C to +125°C
R29631ADM	F	-55°C to +125°C
R29631AFM/883B	F	-55°C to +125°C
R29631AFMS	F	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24-lead .600 wide ceramic DIP
F = 24-lead ceramic flat pack (cerpak)

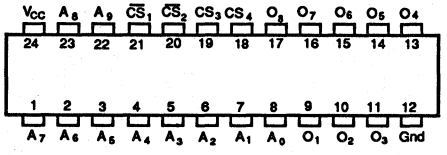
Block Diagram



65-0116

Pin Out Information

Dual-In-Line/Flat Pack Package



Pin 20 is also the programming pin (pp)

65-4069

1024 x 8 SPROM — R29633/R29633A

Power and AC Characteristics Over Operating Range

ICC conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29633AM	Maximum Limits R29633M	Units
I_{CCD}	Power Down, Supply Current (Disabled)	V_{CC} = Max, $\overline{PS}$ = V_{IH}, All other Inputs = GND	45	45	mA
I_{CC}	Supply Current (Enabled)	V_{CC} = Max, All inputs = GND	170	170	mA
t_{AA}	Address Access Time	CL = 30 pF*	70	90	ns
t_{EA}	Enable Access Time	R1 - 300Ω to V_{CC}	70	115	ns
t_{ER}	Enable Recovery Time	R2 - 600Ω to GND, 16 mA Load	40	40	ns
P_D	Power Dissipation (Disabled)		248	248	mW
P_D	Power Dissipation Enabled		935	935	mW

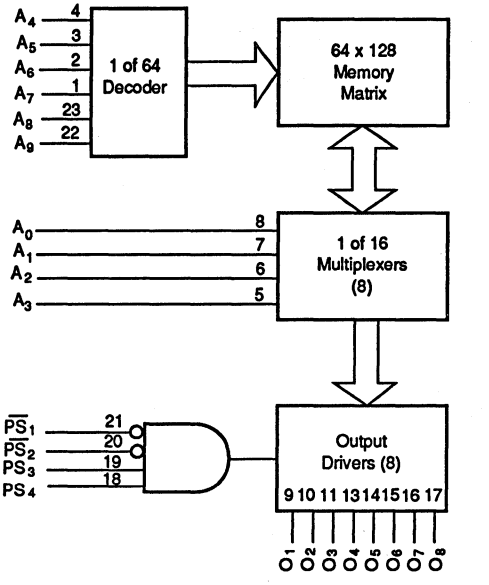
* See AC Test Load Circuit and Switching Waveforms

Ordering Information

Part Type	Package	Operating Temperature Range
R29633DM	D	-55°C to +125°C
R29633DM/883B	D	-55°C to +125°C
R29633DMS	D	-55°C to +125°C
R29633FM	F	-55°C to +125°C
R29633FM/883B	F	-55°C to +125°C
R29633FMS	F	-55°C to +125°C
R29633ADM	D	-55°C to +125°C
R29633ADM/883B	D	-55°C to +125°C
R29633ADMS	D	-55°C to +125°C
R29633AFM	F	-55°C to +125°C
R29633AFM/883B	F	-55°C to +125°C
R29633AFMS	F	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24-lead .600 wide ceramic DIP
F = 24 lead ceramic flat pack (cerpak)

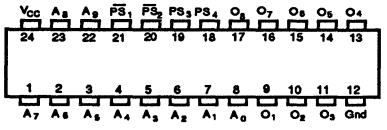
Block Diagram



65-0117

Pin Out Information

Dual In-Line/Flat Pack Package



Pin 20 is also the programming pin (pp)

65-4071

PROM

2048 x 4 PROM — R29651/R29651A

Power and AC Characteristics Over Operating Range

ICC conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29651AM	Maximum Limits R29651M	Units
I_{CC}	Power Supply Current	V_{CC} = Max All inputs = Gnd	170	170	mA
t_{AA}	Address Access Time	C_L = 30 pF *	70	90	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	45	50	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	45	45	ns
P_D	Power Dissipation		935	935	mW

*See AC Test Load Circuit and Switching Waveforms

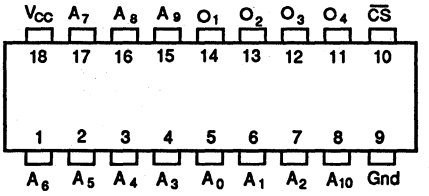
Ordering Information

Part Type	Package	Operating Temperature Range
R29651DM	D	-55°C to +125°C
R29651DM/883B	D	-55°C to +125°C
R29651DMS	D	-55°C to +125°C
R29651ADM	D	-55°C to +125°C
R29651ADM/883B	D	-55°C to +125°C
R29651ADMS	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 18-lead wide ceramic DIP

Pin Out Information

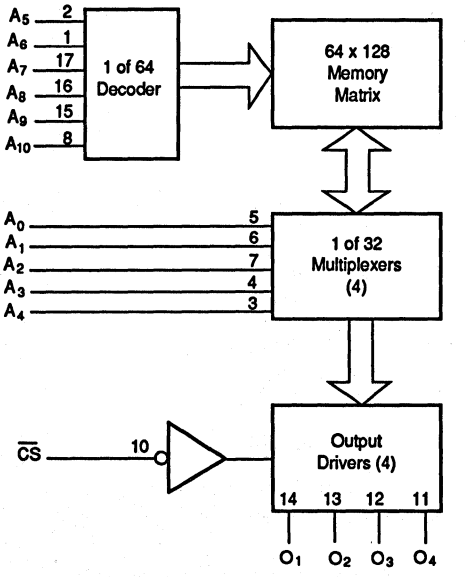
Dual In-Line Package



Pin 10 is also the programming pin (pp)

65-1324

Block Diagram



65-0122

2048 x 4 SPROM — R29653/R29653A

Power and AC Characteristics Over Operating Range

ICC conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29653AM	Maximum Limits R29653M	Units
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max PS = V_{IH}, All other inputs = GND	45	45	mA
I_{CC}	Supply Current (enabled)	V_{CC} = Max All inputs = Gnd	170	170	mA
t_{AA}	Address Access Time	C_L = 30 pF *	75	90	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	80	95	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	45	45	ns
P_D	Power Dissipation (Disabled)		248	248	mW
P_D	Power Dissipation (Enabled)		935	935	mW

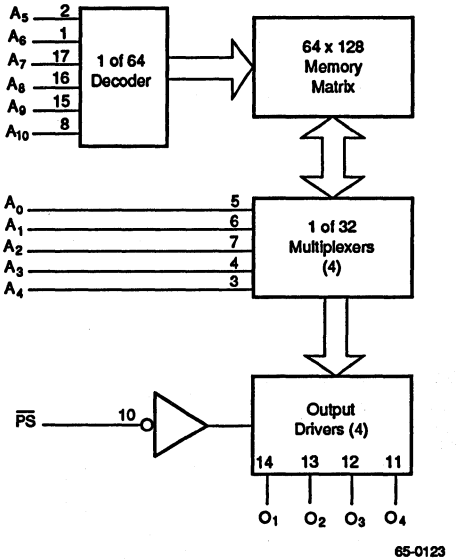
*See AC Test Load Circuit and Switching Waveforms

Ordering Information

Part Type	Package	Operating Temperature Range
R29653DM	D	-55°C to +125°C
R29653DM/883B	D	-55°C to +125°C
R29653DMS	D	-55°C to +125°C
R29653ADM	D	-55°C to +125°C
R29653ADM/883B	D	-55°C to +125°C
R29653ADMS	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 18-lead wide ceramic DIP

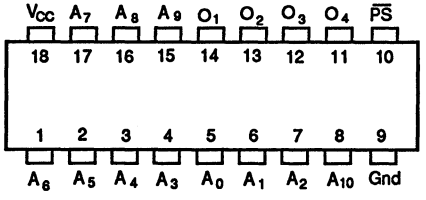
Block Diagram



65-0123

Pin Out Information

Dual In-Line Package



Pin 10 is also the programming pin (pp)

65-1326

PROM

2048 x 8 PROM — R29681/R29681A

Power and AC Characteristics Over Operating Range

ICC conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29681AM	Maximum Limits R29681M	Units
I_{CC}	Power Supply Current	V_{CC} = Max All inputs = Gnd	180	180	mA
t_{AA}	Address Access Time	C_L = 30 pF *	70	100	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	45	50	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	35	45	ns
P_D	Power Dissipation		990	990	mW

*See AC Test Load Circuit and Switching Waveforms

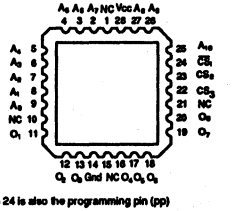
Ordering Information

Part Type	Package	Operating Temperature Range
R29681DM	D	-55°C to +125°C
R29681DM/883B	D	-55°C to +125°C
R29681DMS	D	-55°C to +125°C
R29681LM	L	-55°C to +125°C
R29681LM/883B	L	-55°C to +125°C
R29681LMS	L	-55°C to +125°C
R29681SM	S	-55°C to +125°C
R29681SM/883B	S	-55°C to +125°C
R29681SMS	S	-55°C to +125°C
R29681ADM	D	-55°C to +125°C
R29681ADM/883B	D	-55°C to +125°C
R29681ADMS	D	-55°C to +125°C
R29681ALM	L	-55°C to +125°C
R29681ALM/883B	L	-55°C to +125°C
R29681ALMS	L	-55°C to +125°C
R29681ASM	S	-55°C to +125°C
R29681ASM/883B	S	-55°C to +125°C
R29681ASMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24-lead .600 wide ceramic DIP
L = 28-terminal ceramic leadless chip carrier
S = 24-lead .,300 wide side-brazed ceramic DIP
Contact factory regarding flat pack package

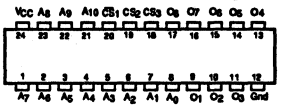
Pin Out Information

Leadless Chip Carrier (28-Terminal)



Pin 24 is also the programming pin (pp)

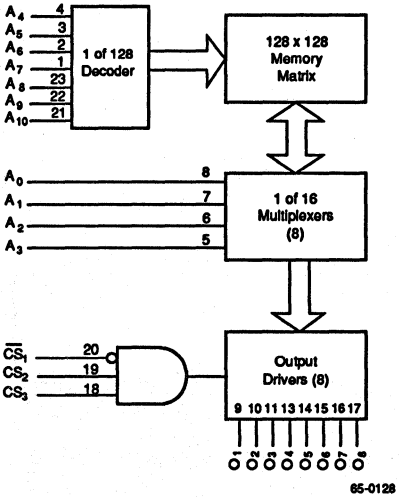
Dual-In-Line
Available in 0.3" and 0.6" Wide Packages



Pin 20 is also the programming pin (pp)

65-4073

Block Diagram



65-0128

2048 x 8 SPROM — R29683/R29683A

Power and AC Characteristics Over Operating Range

ICC conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits R29683AM	Maximum Limits R29683M	Units
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max PS = V_{IH}, All other inputs = GND	50	50	mA
I_{CC}	Supply Current (enabled)	V_{CC} = Max All inputs = Gnd	180	180	mA
t_{AA}	Address Access Time	C_L = 30 pF *	70	105	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	85	105	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	45	50	ns
P_D	Power Dissipation (Disabled)		275	275	mW
P_D	Power Dissipation (Enabled)		990	990	mW

*See AC Test Load Circuit and Switching Waveforms

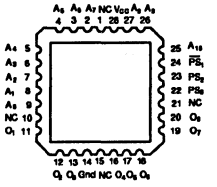
Ordering Information

Part Type	Package	Operating Temperature Range
R29681DM	D	-55°C to +125°C
R29681DM/883B	D	-55°C to +125°C
R29683DMS	D	-55°C to +125°C
R29683LM	L	-55°C to +125°C
R29683LM/883B	L	-55°C to +125°C
R29683LMS	L	-55°C to +125°C
R29683SM	S	-55°C to +125°C
R29683SM/883B	S	-55°C to +125°C
R29683SMS	S	-55°C to +125°C
R29683ADM	D	-55°C to +125°C
R29683ADM/883B	D	-55°C to +125°C
R29683ADMS	D	-55°C to +125°C
R29683ALM	L	-55°C to +125°C
R29683ALM/883B	L	-55°C to +125°C
R29683ALMS	L	-55°C to +125°C
R29683ASM	S	-55°C to +125°C
R29683ASM/883B	S	-55°C to +125°C
R29683ASMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24-lead .600 wide ceramic DIP
L = 28-terminal ceramic leadless chip carrier
S = 24-lead, .300 wide side-brazed ceramic DIP
Contact factory regarding flat pack package

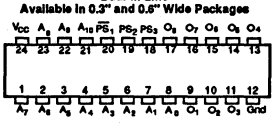
Pin Out Information

Leadless Chip Carrier (28-Terminal)



Pin 24 is also the programming pin (pp)

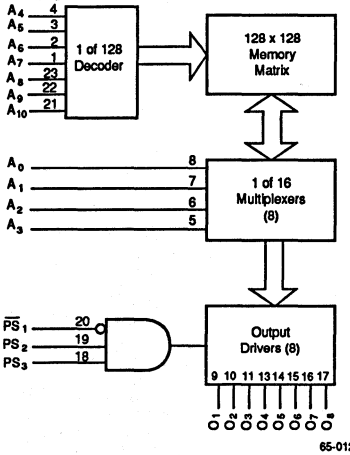
Dual-In-Line
Available in 0.3" and 0.6" Wide Packages



Pin 20 is also the programming pin (pp)

65-4074

Block Diagram



65-0129

PROM

4096 x 8 PROM — R29771

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3. AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29771M	Units
I_{CC}	Power Supply Current	V_{CC} = Max All Inputs GND	190	mA
t_{AA}	Address Access Time	C_L = 30 pF *	65	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	35	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND 16 mA Load	35	ns
P_D	Power Dissipation		1.04	W

*See AC Test Load Circuit and Switching Waveforms

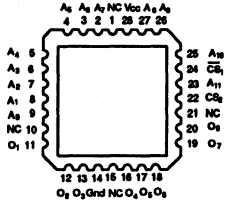
Ordering Information

Part Type	Package	Operating Temperature Range
R29771DM	D	-55°C to +125°C
R29771DM/883B	D	-55°C to +125°C
R29771DMS	D	-55°C to +125°C
R29771FM	F	-55°C to +125°C
R29771FM/883B	F	-55°C to +125°C
R29771FMS	F	-55°C to +125°C
R29771LM	L	-55°C to +125°C
R29771LM/883B	L	-55°C to +125°C
R29771LMS	L	-55°C to +125°C
R29771SM	S	-55°C to +125°C
R29771SM/883B	S	-55°C to +125°C
R29771SMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24-lead .600 wide ceramic DIP
F = 24-lead ceramic bottom-brazed flat pack
L = 28-terminal ceramic leadless chip carrier
S = 24-lead, .300 wide side-brazed ceramic DIP

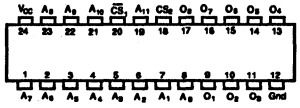
Pin-Out Information

Leadless Chip Carrier (28-Terminal)



Pin 24 is also the programming pin (pp)

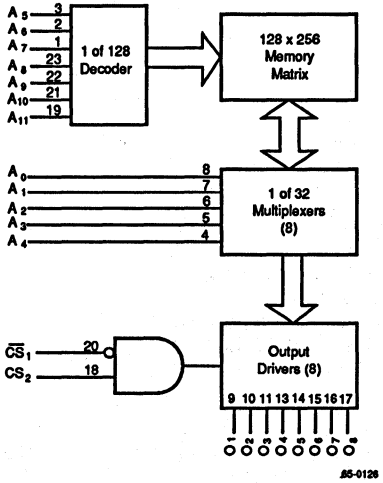
Dual-In-Line Package
Available in 0.3" and 0.6" Wide Packages



Pin 20 is also the programming pin (pp)

85-4662

Block Diagram



85-0126

4096 x 8 SPROM — R29773

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29773M	Units
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max, $\overline{PS}$ = V_{IH}, All other inputs = GND	55	mA
I_{CC}	Supply Current (enabled)	V_{CC} = Max, All inputs = Gnd	190	mA
t_{AA}	Address Access Time	C_L = 30 pF *	65	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	115	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	35	ns
P_D	Power Dissipation (Disabled)		303	mW
P_D	Power Dissipation (Enabled)		1.04	W

*See AC Test Load Circuit and Switching Waveforms

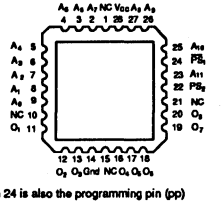
Ordering Information

Part Type	Package	Operating Temperature Range
R29773DM	D	-55°C to +125°C
R29773DM/883B	D	-55°C to +125°C
R29773DMS	D	-55°C to +125°C
R29773FM	F	-55°C to +125°C
R29773FM/883B	F	-55°C to +125°C
R29773FMS	F	-55°C to +125°C
R29773LM	L	-55°C to +125°C
R29773LM/883B	L	-55°C to +125°C
R29773LMS	L	-55°C to +125°C
R29773SM	S	-55°C to +125°C
R29773SM/883B	S	-55°C to +125°C
R29773SMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24-lead .600 wide ceramic DIP
F = 24-lead ceramic bottom-brazed flat pack
L = 28-terminal ceramic leadless chip carrier
S = 24-lead, .300 wide side-brazed ceramic DIP
Contact factory regarding flat pack package

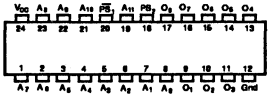
Pin Out Information

Leadless Chip Carrier (28-Terminal)



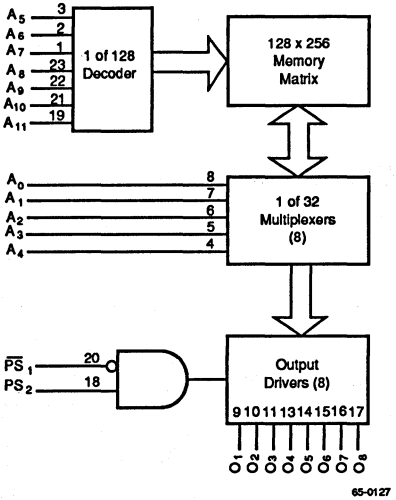
Pin 24 is also the programming pin (pp)

Dual-In-Line/Flat Pack Package
Available in 0.3" and 0.6" Wide Packages



Pin 20 is also the programming pin (pp) 65-4072

Block Diagram



65-0127

PROM

8196 x 8 PROM — R29791

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29791M	Units
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs GND	190	mA
t_{AA}	Address Access Time	C_L = 30 pF[1]	75	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	30	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	30	ns
P_D	Power Dissipation		1.04	W

Note:

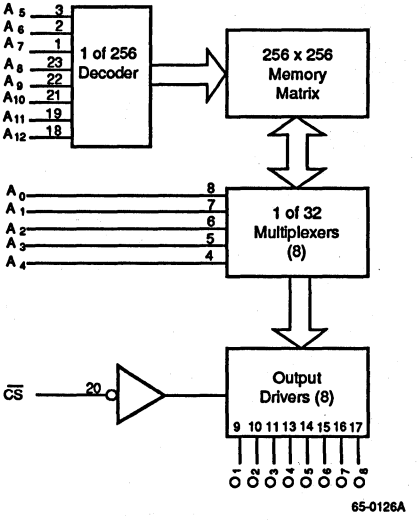
1.See AC Test Load Circuit and Switching Waveforms

Ordering Information

Part Type	Package	Operating Temperature Range
R29791DM	D	-55°C to +125°C
R29791DM/883B	D	-55°C to +125°C
R29791DMS	D	-55°C to +125°C
R29791FM	F	-55°C to +125°C
R29791FM/883B	F	-55°C to +125°C
R29791FMS	F	-55°C to +125°C
R29791SM	S	-55°C to +125°C
R29791SM/883B	S	-55°C to +125°C
R29791SMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24-lead .600 wide ceramic DIP
F = 24-lead ceramic bottom-brazed flat pack
S = 24-lead, .300 wide side-brazed ceramic DIP

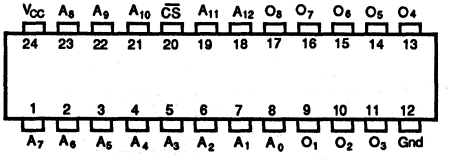
Block Diagram



65-0126A

Pin-Out Information

Dual-In-Line/Flat Pack Package
Available in 0.3" and 0.6" Wide Packages



Pin 20 is also the programming pin (pp)

65-4062A

8192 x 8 SPROM — R29793

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11

Parameter	Description	Test Conditions	Maximum Limits R29793M	Units
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max, $\overline{PS} = V_{IH}$, All other inputs = GND	50	mA
I_{CC}	Supply Current (enabled)	V_{CC} = Max, All inputs = Gnd	190	mA
t_{AA}	Address Access Time	C_L = 30 pF *	75	ns
t_{EA}	Enable Access Time	R1 = 300Ω to V_{CC}	125	ns
t_{ER}	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	30	ns
P_D	Power Dissipation (Disabled)		275	mW
P_D	Power Dissipation (Enabled)		1.04	W

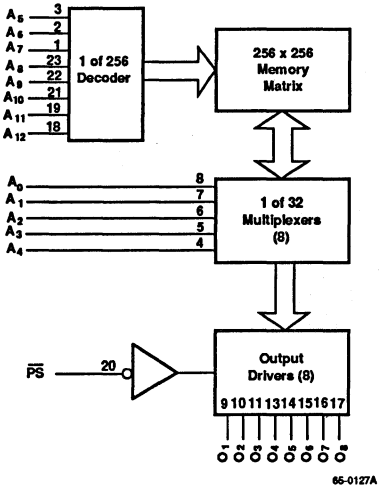
*See AC Test Load Circuit and Switching Waveforms

Ordering Information

Part Type	Package	Operating Temperature Range
R29793DM	D	-55°C to +125°C
R29793DM/883B	D	-55°C to +125°C
R29793DMS	D	-55°C to +125°C
R29793FM	F	-55°C to +125°C
R29793FM/883B	F	-55°C to +125°C
R29793FMS	F	-55°C to +125°C
R29793SM	S	-55°C to +125°C
R29793SM/883B	S	-55°C to +125°C
R29793SMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24-lead .600 wide ceramic DIP
F = 24-lead ceramic bottom-brazed flat pack
S = 24-lead, .300 wide side-brazed ceramic DIP

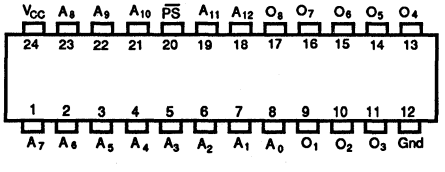
Block Diagram



65-0127A

Pin Out Information

Dual-In-Line/Flat Pack Package
Available in 0.3" and 0.6" Wide Packages

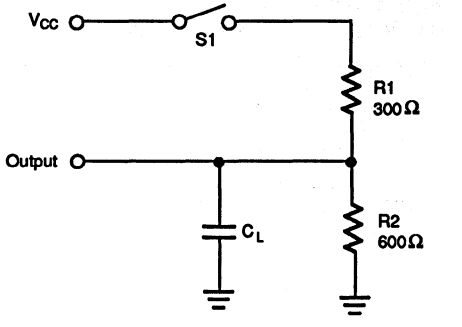


Pin 20 is also the programming pin (pp)

65-4072A

PROM

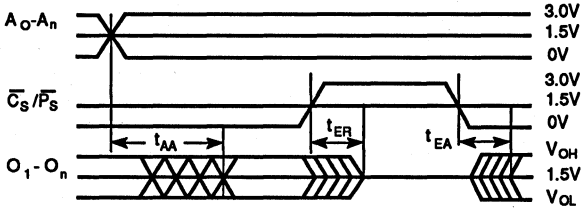
AC Test Load Circuit



65-4059

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30 pF.
2. t_{EA} is tested with C_L = 30 pF; S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.
3. t_{ER} is tested with C_L = 5 pF; S_1 is open for "1" to high impedance test and measured at V_{OH} -0.5V output level and is closed for "0" to high impedance test and measured at V_{OL} +0.5V output level.

Switching Waveforms



Keys to Timing Diagram

Waveforms	Inputs	Outputs
———	Must be Steady	Will be Steady
XXXX	Don't Care. Any Change Permitted	Changing State Unknown
⋈	Does Not Apply	Center Line is High Impedance Off State

65-4811

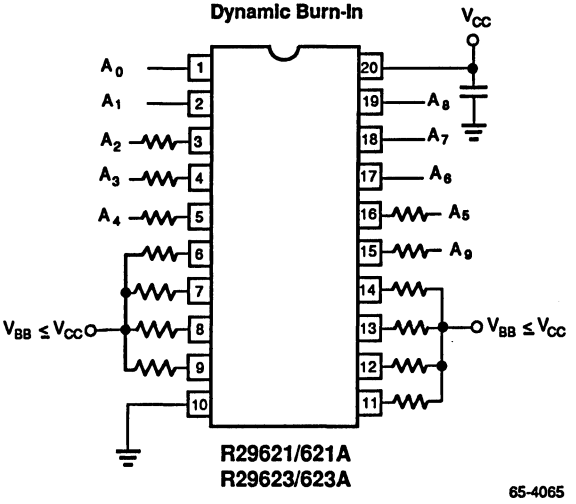
Dynamic Life Test/Burn-In Circuits

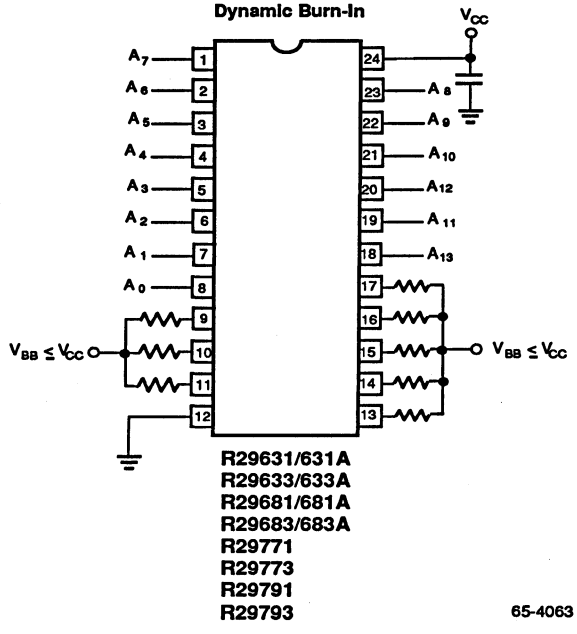
In accordance with MIL-STD-883, Methods 1005/1015, Condition D

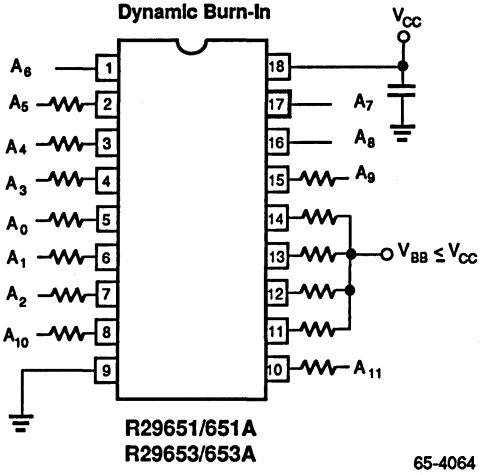
$T_A = 125^{+10}_{-0}$ °C minimum
$V_{CC} = 5.25 \pm 0.25V$

Square Wave Pulses on A^0 to A^n are:
50% ±10% duty cycle
Frequency of each address is to be 1/2 of each preceding input, with A^0 beginning at 100 kHz (e.g., A^0 = 100 kHz ±10%, A^1 = 50 kHz ±10%, A^2 = 25 kHz ±10%,

An = 1/2 An-1 ±10%, etc.)
Resistors are optional on input pins (R = 300Ω ±10%)







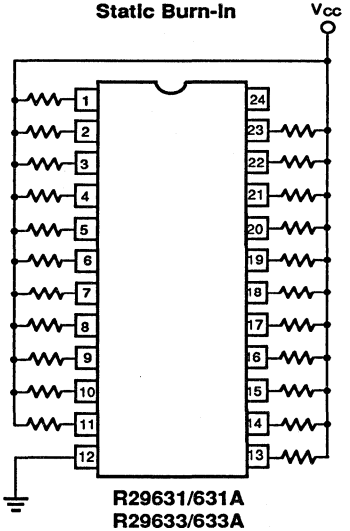
PROM

Static Life Test/Burn-In Circuits

In accordance with MIL-STD-883, Methods 1005/1015, Condition C

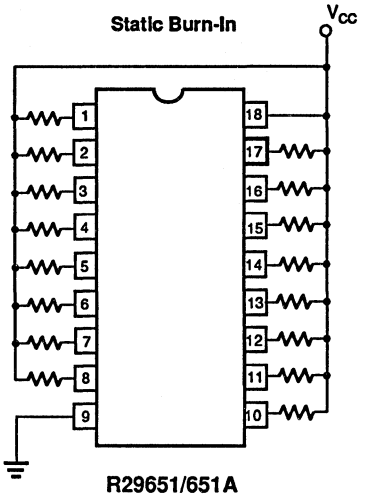
$T_A = 125^{+10}_{-0}$ °C minimum
$V_{CC} = 5.25V \pm 0.25V$

Resistors are optional on input pins
(R = 300Ω ±10%)



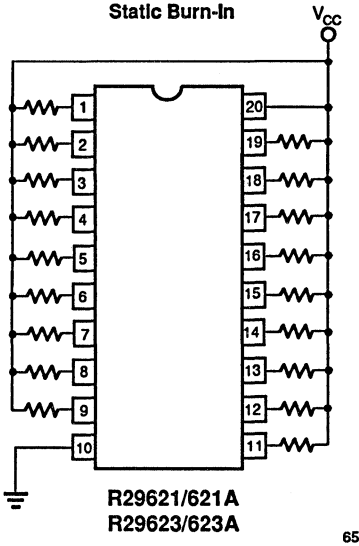
R29631/631A
R29633/633A
R29681/681A
R29683/683A
R29771
R29773
R29791
R29793

65-4066



R29651/651A
R29653/653A

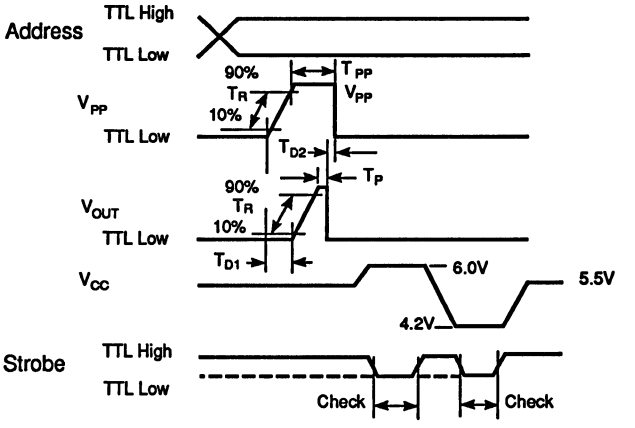
65-4067



R29621/621A
R29623/623A

65-4068

Programming Characteristics



R296XX Series	R297XX Series
T_R = 0.34V/µS Min. — 1.25V/µS Max.	T_R = 0.34V/µS Min. — 1.25V/µS Max.
T_{PP} = 80 µS Min. — 110 µS Max.	T_{PP} = 70 µS Min. — 120 µS Max.
T_P = 1 µS Min. — 40 µS Max.	T_P = 20 µS Min. — 40 µS Max.
T_{D1} = 70 µS Min. — 90 µS Max.	T_{D1} = 60 µS Min. — 100 µS Max.
T_{D2} = 100 nS Min.	T_{D2} = 100 nS Min.
V_{PP} = 27V Min. — 33V Max.	V_{PP} = 26V Min. — 28V Max.
V_{OUT} = 20V Min. — 26V Max.	V_{OUT} = 22V Min. — 24V Max.

Notes:
Output Load = 0.2 mA During 6.0V Check
Output Load = 12 mA During 4.2V Check

65-4810

Programming Timing

Device Programming Inputs

If you would like to have Raytheon program your devices, please submit one of the following:

- Two masters and truth table
- Two masters and checksum

In either case, we require customer approval prior to programming the devices.

If you need blank devices in order to supply programming masters, please do not hesitate to contact Raytheon for unprogrammed samples.

Commercial Programmers (subject to change)

Equipment must be calibrated at regular intervals. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Please contact the following manufacturers for equipment information:

Data I/O Corp.
10525 Willows Road, N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(800) 247-5700

Stag Microsystems Inc. (R296XX Series)
1600 Wyatt Drive, Suite 3
Santa Clara, CA 95054
(408) 988-1118

Commercial Surface Mount Socket Adapter Manufacturer (subject to change)

Please contact the following manufacturer for equipment information:

Emulation Technology, Inc.
2344 Walsh Avenue, Bldg. F
Santa Clara, CA 95051
(408) 982-0660

The companies listed above are not intended to be a complete guide of manufacturers of programmers or adapters, nor does Raytheon endorse any specific company.

Small Signal Transistors (Hermetic Seal)

Raytheon Semiconductor offers a wide variety of industry standard and sole source high reliability (JAN, JANTX, JANTXV) Small Signal Transistors. These transistors are available in a variety of hermetic seal packages (TO18, TO39, TO46, TO72, TO77, TO78, TO86).

Product	Description	Package	JAN	JANTX	JANTXV
2N0657**	NPN General Purpose Amplifier	TO39	X		
2N0697**	NPN General Purpose Amplifier	TO39	X		
2N0706**	NPN Ultra High Speed Switch	TO18	X		
2N0718A	NPN General Purpose Amplifier	TO18	X	X	X
2N0720A**	NPN General Purpose Amplifier	TO18	X	X	
2N0910**	NPN General Purpose Amplifier	TO18	X		
2N0918	NPN UHF Amplifier	TO72	X	X	X
2N0930	NPN Low Noise, High Gain Amplifier	TO18	X	X	
2N1131**	PNP General Purpose Amplifier	TO39	X		
2N1132**	PNP General Purpose Amplifier	TO39	X		
2N1613**	NPN Medium Current General Purpose Amplifier	TO39	X	X	X
2N1711**	NPN General Purpose Amplifier	TO39	X	X	
2N1890**	NPN General Purpose Amplifier	TO39	X	X	
2N1893**	NPN General Purpose Amplifier	TO39	X		
2N2060	NPN Differential Amplifier	TO77	X	X	X
2N2219A	NPN Medium Current General Purpose Amplifier	TO39	X	X	X
2N2222A	NPN Medium Current General Purpose Amplifier	TO18	X	X	X
2N2369A	NPN Ultra High Speed Switch	TO18	X	X	X
2N2484	NPN Low Level Low Noise High Gain Amplifier	TO18	X	X	X
2N2605	PNP Low Level Low Noise High Gain Amplifier	TO46	X	X	X
2N2905A	PNP Medium Current General Purpose Amplifier	TO39	X	X	X
2N2907A	PNP Medium Current General Purpose Amplifier	TO18		X	X
2N2919**	NPN Low Noise High Gain Differential Amplifier	TO77		X	
2N2920	NPN Low Noise High Gain Differential Amplifier	TO77	X	X	X
2N2945A**	PNP Chopper	TO46	X	X	X
2N2946A**	PNP Chopper	TO46	X	X	X
2N3019	NPN General Purpose Amplifier	TO39	X	X	X
2N3057A**	NPN General Purpose Amplifier	TO46	X	X	X
2N3250A**	PNP Low Level Gen Purpose Amp & Switch	TO18		X	X
2N3251A	PNP Low Level Gen Purpose Amp & Switch	TO18	X	X	X
2N3467	PNP Core Driver	TO39		X	X
2N3485A**	PNP Med Current Gen Purpose Amplifier	TO46	X	X	
2N3486A	PNP Med Current Gen Purpose Amplifier	TO46	X	X	
2N3498**	PNP High Voltage Gen Purpose Amplifier	TO39	X	X	
2N3499**	NPN High Voltage Gen Purpose Amplifier	TO39	X	X	

** Designates Sole Source

Small Signal Transistors

Product	Description	Package	JAN	JANTX	JANTXV
2N3500**	NPN High Voltage Gen Purpose Amplifier	TO39	X	X	X
2N3501	NPN High Voltage Gen Purpose Amplifier	TO39	X	X	X
2N3634	PNP High Voltage Gen Purpose Amplifier	TO39			X
2N3635	PNP High Voltage Gen Purpose Amplifier	TO39	X	X	X
2N3636	PNP High Voltage Gen Purpose Amplifier	TO39	X	X	X
2N3637	PNP High Voltage Gen Purpose Amplifier	TO39	X	X	X
2N3700	NPN General Purpose Amplifier	TO18	X	X	X
2N3735	NPN High Current High Speed Switch Core Driver	TO39	X	X	X
2N3737	NPN High Current High Speed Switch Core Driver	TO39	X	X	X
2N3762**	PNP High Current High Speed Switch Core Driver	TO39			X
2N3763**	PNP High Current High Speed Switch Core Driver	TO39			X
2N3810	PNP Low Noise High Gain Differential Amplifier	TO78	X	X	X
2N3811	NPN Low Noise High Gain Differential Amplifier	TO78	X	X	X
2N3866	NPN RF Amplifier	TO39	X	X	X
2N3866A*	NPN RF Amplifier	TO39	X	X	X
2N4029	PNP General Purpose Amplifier	TO39	X	X	X
2N4033	PNP General Purpose Amplifier	TO39	X	X	X
2N4449	NPN Ultra High Speed Switch	TO46	X	X	X
2N4854	NPN/PNP Complementary Dual	TO78	X	X	X
2N5109	NPN RF Amplifier	TO39	X	X	
2N5794	Dual NPN Med Current General Purpose Amp	TO78		X	X
2N5795	Dual NPN Med Current General Purpose Amp	TO78			X
2N5796	Dual NPN Med Current General Purpose Amp	TO78		X	
2N6987	Quad PNP Med Current General Purpose Amp	TO116	X	X	X
2N6988	Quad PNP Med Current General Purpose Amp	TO86	X	X	X
2N6989	Quad NPN Med Current General Purpose Amp	TO116	X	X	X
2N6990	Quad NPN Med Current General Purpose Amp	TO86	X	X	X
SP2219AF	Dual NPN Med Current General Purpose Amp	TO89			
SP2219AQF	Quad NPN Med Current General Purpose Amp	TO86			
SP2484F	Dual NPN Low Noise, High Gain Amp	TO89			
SP2484QD	Quad NPN Low Noise, High Gain Amp	TO116			
SP2484QF	Quad NPN Low Noise, High Gain Amp	TO86			
SP2605F	Dual PNP Low Noise, High Gain Amp	TO89			
SP2605QF	Quad PNP Low Noise, High Gain Amp	TO86			
SP2905AF	Dual PNP Med Current General Purpose Amp	TO89			
SP2905AQD	Quad PNP Med Current General Purpose Amp	TO116			
SP2905AQF	Quad PNP Med Current General Purpose Amp	TO86			
SP3019QF	Quad NPN General Purpose Amp	TO86			
SP3467F	Dual PNP High Current, High Speed Switch	TO89			
SP3467QD	Quad PNP High Current, High Speed Switch	TO116			
SP3467QF	Quad PNP High Current, High Speed Switch	TO86			
SP3724F	Dual NPN High Current, High Speed Switch	TO89			
SP3724QD	Quad NPN High Current, High Speed Switch	TO116			
SP3724QF	Quad NPN High Current, High Speed Switch	TO86			
SP3725F	Dual NPN High Current, High Speed Switch	TO89			
SP3725QD	Quad NPN High Current, High Speed Switch	TO116			
SP3725QF	Quad NPN High Current, High Speed Switch	TO86			

** Designates Sole Source

Section 4
Analog/Mixed-Signal Application Specific Integrated Circuits

Raytheon Semiconductor is a major supplier of high accuracy and high performance analog and mixed-signal ASICs with High Speed Bipolar and CBiCMOS processes. These high performance products are available for customer specific products for both commercial and military applications such as:

- ATE Pin drive and sense electronics
- Video/multimedia products
- Data acquisition products
- RF/IF communications products
- High speed data communications (FDDI, ESCON, Fiber Channel, ATM)
- Power management circuitry

When converting your discrete design into an ASIC, Raytheon's design engineers will use existing analog or digital (mixed-signal) cells from standard cell libraries.

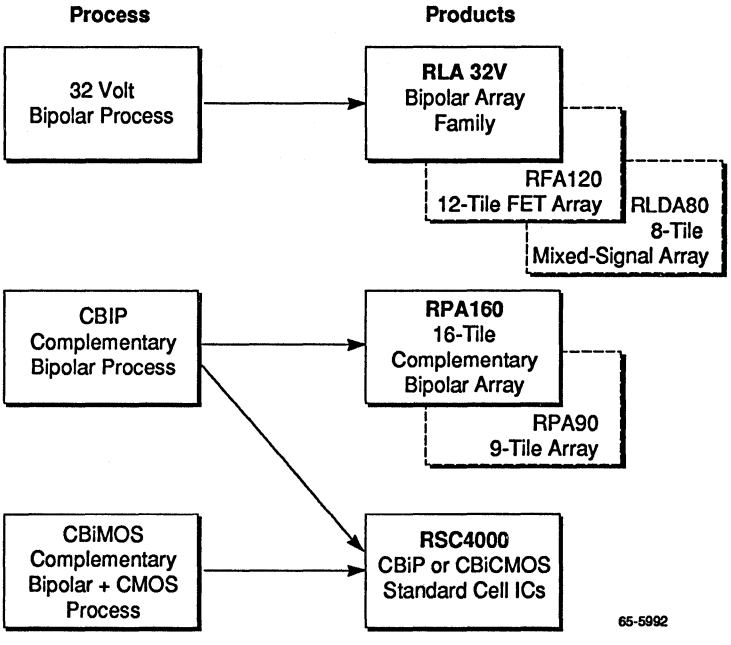
Under the VRSA-Tile (Versatile Raytheon Smart ASICs) concept, Raytheon supports full custom transistor level design, tile array design and standard cell design. These ASIC products are based on both complementary bipolar and CBiCMOS process technologies and are available in a variety of commercial/military DIP or surface mount packages.

A comprehensive, proven CAD system forms an integral part of Raytheon Semiconductor's VRSA-Tile design methodology. Front end design such as Schematic Capture and Circuit Simulation are linked in software to Layout, Design Verification and Testing, sharing a common database for error-free designs. The resulting prototypes, as well as production parts, are manufactured and assembled at Raytheon facilities with particular emphasis on timely delivery of quality products.

ASIC Process Technologies

Features	High Voltage 32 Volt Bipolar	CBICMOS	CBIP	Units
BV_{CEO}	32	12	12	Volts
NPN (f_T)	0.5	4.0	4.0	GHz
Minimum Geometries	(18 x 23)	(2 x 3)	(2 x 3)	µm
NMOS (Drawn)		2.5		µm
PNP (f_T) Vertical		1.5	1.5	GHz
Minimum Geometries	(18 x 23)	(2 x 3)	(2 x 3)	µm
PMOS (Drawn)		2.5		µm
CMOS 1X (Inverter Gate Delay)		1.0	1.0	ns
P-Channel JFET	Yes			
SiCr Resistors	Yes	Yes	Yes	
Matching	1.5	<1.0	<1.0	% max-match
Tempco	200	50	50	ppm/°C
Applied Voltage	200	200	200	Volts
Tolerance	±10	±10	±10	Percent
Zener Zap Capability	Yes	Yes	Yes	
Schottky Diodes (AlSi)	Yes	No	No	
Schottky Diodes (PtSi)	No	Yes	Yes	
Schottky Diodes <1 ns Response Time	No	Yes	Yes	

ASIC Product Offering



Available Design Methodologies

Array 32V & 12V CBiP Design review to prototypes: 6-10 weeks **First Silicon Success** ◆ Pre-designed macrocell library ◆ Array foundation ◆ Low risk, high confidence	**Standard Cell** 32V, 12V CBiP & CBiCMOS Design review to prototypes: 14-16 weeks **Improved Circuit Performance** ◆ Pre-designed standard cell ◆ Smallest die for function (die, package) ◆ Optimized layout ◆ Better performance ◆ Low power for small die ◆ Optimized thermal gradients	**Full Custom** 32V, 12V CBiP & CBiCMOS Design review to prototypes: 18-24 weeks **Optimized Circuit Performance** ◆ Custom designed cells ◆ Lowest thermal gradients ◆ Optimized layout for function ◆ Smallest die for function ◆ Lowest power for die size ◆ Lowest unit price for function
◆ Fast circuit update, 2-4 weeks ◆ 80% (max) array utilization	◆ Circuit changes 6-8 weeks ◆ Efficient utilization of all silicon	◆ Circuit changes 12-14 weeks ◆ Optimized utilization of silicon
◆ Low development cost ◆ Yearly volumes >50K units/yr.	◆ Higher NRE than array ◆ Yearly volumes >100K units/yr.	◆ Highest NRE ◆ Yearly volumes >100K units/yr.

ASIC CAD System

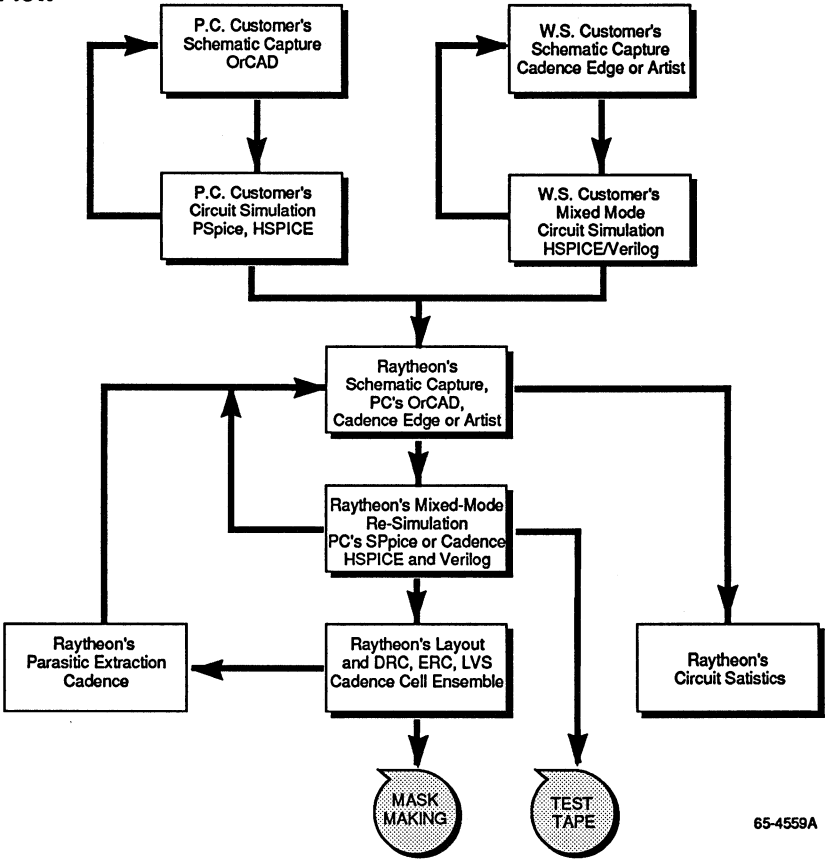
Depending on circuit complexity and the number of digital gates required, PC based or workstation based tools may be used. In the PC environment, OrCAD is used for schematic capture and circuit simulations can be executed in PSpice or HSPICE. However, only a limited amount of digital logic can be handled in this manner before simulation run-times become excessive.

The workstation tools are Cadence based, and either the Edge or the Artist package can be used for schematic capture. The Verilog tool is offered for mixed-signal applications requiring extensive digital circuitry. Mixed-mode simulations using Verilog employ HSPICE for analog simulations. Since circuit simulations are repeated by Raytheon to verify a customer's results, the same CAD environment is used wherever possible.

Once the simulation results have been mutually accepted, the design moves to the Layout phase. Here, Cadence's Cell Ensemble tool is used. This layout tool extracts layout parasitics that are inserted in the simulation models and simulations can be re-run, using this additional information.

When simulation results are acceptable, Design Rule Checking (DRC, ERC) and Layout Verification (LVS) software is run prior to the start of mask making. If simulation results are not satisfactory, changes may have to be made to the layout in order to address observed problems and the cycle is repeated until the post-layout simulation results are acceptable. Only then will the design move on to mask making. Final simulations are used to generate the test program for the design.

Design Flow



32 Volt Linear Arrays (RLA Family)

Bipolar junction isolated wafer fabrication is the basis for the linear macrocells listed below. This process employes projection-based photolithographic imaging, thin film etch definition and a two-layer interconnect technology. A dielectrically isolated SiCr resistor fabrication technique is used along with a conventional, low cost single layer personalization mask step.

The basic unit of our linear arrays is the programmable differential gain block — the op amp or comparator. This allows custom tailoring of high level functions at a single macrocell location. Additional functions can be built by combining macrocells with the onboard transistors and resistors.

BV_{CEO}	Description	Ft (min)	RLA40	RLA80	RLA120	RLA160	RFA120	RLDA80
32V	Type GS Macrocells	500 MHz	4	8	4	7	8	8
32V	Type NGS Macrocell	500 MHz	0	0	8	8	4	0
32V	M_{VREF} V-Reference	500 MHz	No	No	No	Yes	No	Yes
32V	NPNS Transistors	500 MHz	37	46	39	43	71	24
32V	NPNM Transistors	500 MHz	4	0	0	0	4	4
32V	NPNL Transistors	500 MHz	0	3	4	4	0	0
32V	PNPS Transistors	4 MHz	17	19	16	10	27	12
	Digital Macros		0	0	0	0	0	18
	Small Digital Macro		0	0	0	0	0	19
	D-Latch Cell		0	0	0	0	0	16
	Digital I/O Cell		0	0	0	0	0	10
	Extra Current Source		0	0	0	0	0	0
	MNIM 0		3	4	4	4	4	4
	SiCr Resistors (Total)		66	93	196	240	262	128
	Total Resistance		1.6M	2.7M	4.5M	5.7M	6.2M	3.1M
	Bonding Pads		24	24	24	44	32	46

Analog Macrocells Available

MOPA1	Basic Op Amp
MOPA2	Ground Sensing Op Amp
MOPA3	Class AB Op Amp
MCMP1	Ground Sensing Comparator
MCMP2	Open Emitter Comparator
SW	SPDT Analog Switch
UNIREF	Bandgap Reference
DVREG	Voltage Regulator

Op Amps

V_{os} = ± 1 mV typ.
I_{os} = 4 nA typ.
Slew rates 0.7 V/µs
Gain bandwidth = 10 MHz

Comparators

V_{os} = ±1 mV typ.
I_{os} = 20 nA typ.
Response time 1 µs

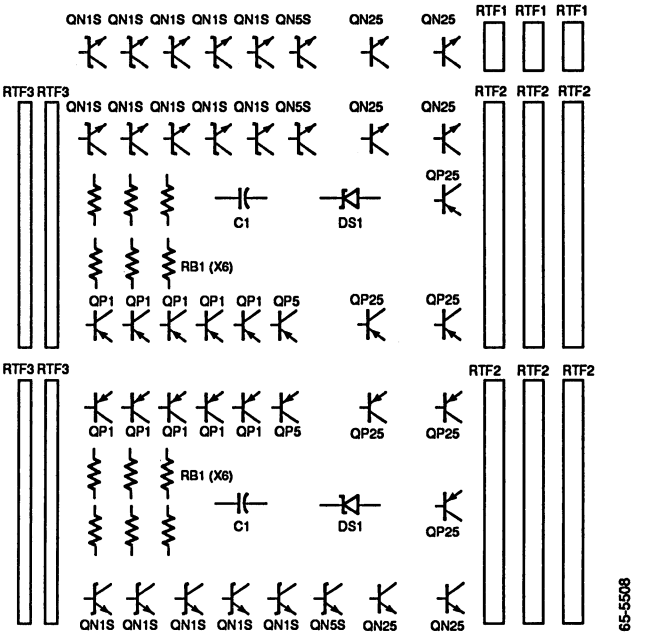
Digital Macrocells Available for RLDA80

AND2	2 Input AND gate
NOR2	2 Input NOR
XNOR2	2 Input exclusive NOR gate
DLP	Positive gate D-latch
DLN	Negative gate D-latch
DITC	TTL/CMOS input cell
DOTC	TTL/CMOS output cell

Precision Complementary Arrays (RPA Family)

The RPA90 and RPA160 are a family of high speed analog customer specific ASICs. These arrays are fabricated on a precision high speed analog process (CBiP) with thin film resistors. The RPA90 has a fixed tile foundation in a 3 x 3 grid pattern, the RPA160 has a 4 x 4 pattern. Each tile has its own axis of symmetry to minimize parasitic and thermal gradients as shown below. By using the tile array's pre-designed and characterized analog macrocells, the risk associated with analog design is reduced. A listing of the available macrocells is located on the following page.

Description	f_T (min)	BV_{CEO}	Quantity/ Tile	RPA160 16 Tiles	RPA90 9 Tiles
QN1S NPN Transistor with Schottky Clamp (1X)	4 GHz	13 Volts	15	240	135
QN5S NPN Transistor with Schottky Clamp (5X)	4 GHz	13 Volts	3	48	27
QN25S NPN Transistor with Schottky Clamp (25X)	4 GHz	13 Volts	6	96	54
QP1 PNP Transistor (1X)	1.5 GHz	15 Volts	10	160	90
QP5 PNP Transistor (5X)	1.5 GHz	15 Volts	2	32	18
QP25 PNP Transistor (25X)	1.5 GHz	15 Volts	6	96	54
DS1 Schottky Diode			2	32	18
MOS Capacitor, largest definable value of 1 pF			2	32	18
RTF1 SiCr Resistor (2.5K max. definable value)			3	48	27
RTF2 SiCr Resistor (15K max. definable value)			6	96	54
RTF1 SiCr Resistor (38K max. definable value)			4	64	36



Precision Complementary Standard Cell Family (RSC4000)

The RSC4000 is a standard cell family which offers the designer a flexible, cost-effective, and low risk method for integrating systems requiring analog and mixed analog/digital functions. The standard cells utilize our Complementary BiCMOS process (CBiCMOS) with thin film resistors.

The standard cell approach frees designers from the boundaries imposed by an array topology and lets them minimize the silicon area necessary to realize the desired system functionality. Individual cells are pre-defined and fully characterized, which minimizes the design risk associated with large VLSI designs and enables circuit densities which rival full custom implementations.

Following is a list of some of the standard cells (RSC4000) and macrocells (RPA160, RPA90) available.

Analog Standard Cells/Macrocells

Name	Cell Description	Std. Cell RSC4000	Macrocells RPA90	Macrocells RPA160
Amplifiers				
AMP01	35 MHz, Unity Stable, General Purpose Op Amp	Yes	Yes	Yes
AMP02	30 MHz, Unit Gain Stable, Ground Sensing Op Amp	Yes	Yes	Yes
AMP03	5 MHz, 2.5 nV/√Hz, Precision Low Noise Op Amp	Yes	Yes	Yes
AMP04	35 MHz, Unit Gain Stable, 50Ω Drive Op Amp	Yes	Yes	Yes
AMP05	160 MHz, Low Noise, Current Feedback Op Amp	Yes	Yes	Yes
HDA01	800 MHz, Very High Speed Differential Amp	Yes	Yes	Yes
HDA02	200 MHz, Low Noise, High Speed Differential Amp	Yes	Yes	Yes
VGA01	250 MHz, Large Dynamic Range, Variable Gain (VGA)	Yes	Yes	Yes
Buffers				
BUF01	150 MHz, 500 V/µs Slew Rate, High Performance Analog Buffer	Yes	Yes	Yes
BUF02	200 MHz, 4000 V/µs Slew Rate, Ultra High Speed Buffer	Yes	Yes	Yes
BUF03	>200 MHz Wide Power Bandwidth Product, Low Power Buffer	Yes	Yes	Yes
Comparators				
CMP01	30 ns TTL/CMOS General Purpose Comparator	Yes	Yes	Yes
CMP02	25 ns TTL/CMOS Single Supply Comparator	Yes	Yes	Yes
CMP03	40 ns, Low Offset Precision Comparator	Yes	Yes	Yes
CMP04	3 ns High Speed ECL-Output Comparator	Yes	Yes	Yes
CMP05	6.5 ns, Low Power High Speed TTL Comparator	Yes	Yes	Yes
VREF				
REF01	80 ppm/°C, 2% Accurate, 2.5V Bandgap Reference	Yes	Yes	Yes
REF02	30 ppm/°C, 0.5% Accurate, 2.5V Bandgap Reference	Yes	Yes	Yes
Signal Conditioning				
MLT01B	12 MHz, Low Noise, High Accuracy, Analog Multiplier/Divider	Yes	Yes	Yes
MXA01B	50 MHz, 8 Channel Multiplexed Video Amplifier	Yes	Yes	Yes
DEM01B	30 MHz, 100 ns, Synchronous Modulator/Demodulator	Yes	Yes	Yes
QMD04B	250 MHz, Quadrature Modulator or Demodulator	Yes	Yes	Yes
TAH01B	38 MHz, Low Droop 0.5 mV/µs, Precision Track and Hold	Yes	Yes	Yes
MIX01B	800 MHz RFin, 400 MHz IF, Wide Bandwidth Mixer/Amplifier	Yes	No	No
PLL Signal Synthesis &Data Recovery				
VCO01B	200 MHz High Speed Voltage Controlled Oscillator (VCO)	Yes	Yes	Yes
PLL01	150 MHz, 50 ppm/°C High Speed Phase Lock Loop	Yes	Yes	Yes
PLL03	200 MHz, 12 ps RMS (typ.) Jitter, Phase Lock Loop	Yes	No	

RSC4000 Digital Functions

Digital Bipolar Standard Cells (Only available on RSC4000)

Gates, Inverters and Buffers

1N11HI	**Inverter**
NI11HI	Buffer
AN21HI	2-Input AND
ND21HI	2-Input AND/NAND
NR21HI	2-Input NOR
OR22CI	2-Input OR/NOR
X022CI	2-Input EX-OR/NOR
ON41HI	4-Input OR/NAND
OA42CI	4-Input OR-AND/NAND

Flip-Flops, Latches

DFNC1I	D Flip-Flop
LANCHI	D Latch

Input/Output Translators

RPNETI	TTL-ECL Input Translator
RPNETP	TTL-PECL Input Translator
DTNEIT	ECL-TTL Output Translator
DTNEPT	PECL-TTL Output Translator

Miscellaneous Functions

MX41EI	4:1 Multiplexer with Enable
MX21EI	2:1 Multiplexer with Enable
DC24EI	1:4 Demultiplexer
DC24EI	2:4 Decoder with Enable
REF03B	ECL Bandgap Reference
REF04B	ECL Voltage Reference
REF05B	Input Voltage Reference

Data Conversion Cells

- 10-Bit, 40 MHz ADC
- 8-Bit, 30 MHz Low Power ADC
- 6-Bit, 70 MHz ADC
- 8-Bit, 50 MHz DAC
- 8-Bit, 15 ns Track and Hold

Digital CMOS Cells

Inverters and Buffers

IN11LC	Inverter (1X)
IN112C	Inverter (2X)
IN113C	Inverter (3X)

Gates

ND21LC	2-Input NAND Gate
AN21LC	2-Input AND Gate
NR21LC	2-Input NOR Gate
OR21LC	2-Input OR Gate
XN21LC	2-Input XNOR Gate
XO21LC	2-Input XOR Gate
ND31LC	3-Input NAND Gate
AN31LC	3-Input AND Gate
NR31LC	3-Input NOR Gate
OR31LC	3-Input OR Gate
ND41LC	4-Input NAND Gate
AN41LC	4-Input AND Gate
NR41LC	4-Input NOR Gate
OR41LC	4-Input OR Gate
AR41LC	4-Input AND-NOR Gate

Latches and Flip-Flops

LANCHC	D Latch
DFNCRC	D Flip-Flop
DFBCRC	D Flip-Flop with Preset, Clear and Buffered Outputs

Input and Output Buffers

RPIECC	CMOS Input Inverter w/Pad, Pullup and ESD
RPIETC	TTL Input Inverter w/Pad, Pullup and ESD
DPIECC	CMOS Driver/Inverter w/Pad and ESD
DPNECT	BiCMOS TTL Driver w/Pad and ESD
DTNECT	BiCMOS TTL Three-State Driver w/Pad and ESD
TTNECT	BiCMOS Transceiver Three-State Driver w/Pad and ESD
LRINCC	CMOS Inverting Line Receiver (no pad)
LRNNCC	CMOS Line Receiver (no pad)
LRINTC	TTL Inverting Line Receiver (no pad)
LRNNTC	TTL Line Receiver (no pad)

Miscellaneous Cells

ASW01C	Transmission Gate (1X)
DM24IC	2:4 Decoder/1:4 Demultiplexer
MX21IC	2:1 Multiplexer
MX41IC	4:1 Multiplexer
MX81IC	8:1 Multiplexer

Analog/Digital Test Capability

Once developed and in production, VRSA-Tile is supported through a variety of high pin count and surface mount plastic and hermetic packages, fully tested on LTX, Teradyne or HP mixed-signal testers.

Analog Test Capability (LTX-80/HP9491)

Parameter	Range
Settling/Acquisition Time	0.4% in 20 ns
Bandwidth	200 MHz
Aperture Time	100 ps
Harmonic Distortion	-86 dB
ADC Conversion Rates	128 MHz
Differential Gain/Phase	2.0/Degree
Slew Rate	500 V/µs at 1V
Pattern Generation	128 MHz

Digital Test Capability (HP9491)

Parameter	Performance
Maximum Pin Count	80
Maximum Test Pattern Rate	128 MHz
Timing Edge Placement Range	0 to 2 Periods
Timing Resolution	±100 ps
Timing Accuracy	±350 ps
Edge and Compare Output Capability	Single/Window/ Double

ASIC Packaging Options

The following table lists the packages that are currently available for Raytheon Semiconductor ASIC products.

Package Description	Typical θ_{JA} Value (C/W)
Ceramic 24 Lead Flat Pack (0.40" wide)	65
Ceramic 44 Lead Quad Flat Pack (0.65" sq.)	50
Ceramic 64 Lead Chip Carrier (0.90" sq.)	44
Ceramic 20 Pad LCC (0.35" sq.)	85
Ceramic 28 Pad LCC (0.45" sq.)	75
Ceramic 44 Pad LCC (0.65" sq.)	65
Plastic 28 Lead Chip Carrier (0.45" sq.)	65
Plastic 44 Lead Chip Carrier (0.65" sq.)	55
Plastic 68 Lead Chip Carrier (0.95" sq.)	45
Plastic 14 Lead DIP (0.30" wide)	70
Plastic 16 Lead DIP (0.30" wide)	65
Plastic 24 Lead DIP (0.30" wide)	50
Plastic 40 Lead DIP (0.60" wide)	45
Plastic 8 Lead SOIC (0.15" wide)	155
Plastic 14 Lead SOIC (0.15" wide)	110
Plastic 16 Lead SOIC (0.15" wide)	105
Plastic 20 Lead SOIC (0.30" wide)	80
Plastic 24 Lead SOIC (0.30" wide)	75

Section 5
Cross References

Industry Type Cross References

Industry Type	Raytheon Semiconductor Nearest Equivalent	Industry Type	Raytheon Semiconductor Nearest Equivalent
AD647	RC4207	LT-1002	RC4227
AD708	RC4277	MAX9686	LM111
HA5127	OP-27	MC1741	RC741
HA5137	OP-37	NE5105	RC4805
HA-5147	OP-47	NE5532	RC5532
LH2108	LH2108	NE5534	RC5534
LM108	LM108	OP-227	RC4227

Contents

Cross References

Analog Devices	Raytheon Semiconductor Nearest Equivalent
AD OP-07A	OP-07A
AD OP-07A/883	OP-07A/883B
AD OP-07C	OP-07C
AD OP-07D	OP-07D
AD OP-07E	OP-07E
AD OP-07	OP-07
AD OP-07/883	OP-07/883B
AD OP-07	OP-07
AD OP-27A	OP-27A
AD OP-27A/883	OP-27A/883B
AD OP-27B	OP-27B
AD OP-27B/883	OP-27B/883B
AD OP-27C	OP-27C
AD OP-27C/883	OP-27C/883B
AD OP-27E	OP-27E
AD OP-27F	OP-27F
AD OP-27G	OP-27G
AD OP-37A	OP-37A
AD OP-37A/883	OP-37A/883B
AD OP-37B	OP-37B
AD OP-37B/883	OP-37B/883B
AD OP-37C	OP-37C
AD OP-37C/883	OP-37C/883B
AD OP-37E	OP-37E
AD OP-37F	OP-37F
AD OP-37G	OP-37G
OP77A	OP-77A
OP77A/883	OP-77A/883B
OP77A	OP-77A
OP77B	OP-77B
OP77B/883	OP-77B/883B
OP77E	OP-77E
OP77F	OP-77F
OP77G	OP-77G
ADVF32	RC4152
ADVF32	RC4153
AD539	RC4200/A
ADREF-01	REF-01
ADREF-01C	REF-01C
REF-02	REF-02
REF-02C	REF-02C
REF-02D	REF-02D

Burr Brown	Raytheon Semiconductor Nearest Equivalent
VFC-32BP	RC4152
VFC-32PB	RC4153
OPA27A/883	OP-27A/883B
OPA27B/883	OP-27B/883B
OPA27C/883B	OP-27C/883B
OPA27A	OP-27A
OPA27B	OP-27B

Burr Brown	Raytheon Semiconductor Nearest Equivalent
OPA27C	OP-27C
OPA27E	OP-27E
OPA27F	OP-27F
OPA27G	OP-27G
OPA37A	OP-37A
OPA37A/883	OP-37A/883B
OPA37B	OP-37B
OPA37B/883	OP-37B/883B
OPA37C	OP-37C
OPA37C/883	OP-37C/883B
OPA37E	OP-37E
OPA37F	OP-37F
OPA37G	OP-37G

Exar	Raytheon Semiconductor Nearest Equivalent
XR2207	RM2207
XR2211	RC2211
XR4136	RC3403A
XR4151	RC4152
XR5532	RC5532
XR5532A	RC5532A
XR5534	RC5534
XR5534A	RC5534A

Goldstar	Raytheon Semiconductor Nearest Equivalent
GL7107	RV4145

Harris	Raytheon Semiconductor Nearest Equivalent
CA124	LM124
CA139	LM139
CA324	LM324
CA339	LM339
CA5403A	RC3403A
HA4741	RC4741
HA3-5101	RC5534
HA3-5102	RC5532
HA3-5102	RC5532A
HS3182	RM3182
HS3182	RM3182A
ICL8013	RC4200/A

Hitachi	Raytheon Semiconductor Nearest Equivalent
LM1851	RV4145

Holt	Raytheon Semiconductor Nearest Equivalent
HI8382	RM3182
HI8382	RM3182A
HI8482	RM3183
HI8482	RM3283

Linear Technology	Raytheon Semiconductor Nearest Equivalent
OP-07A	OP-07AT
OP-07A/883B	OP-07A/883B
OP-07AJ/883B	OP-07A/883B
OP-07C	OP-07C
OP-07E	OP-07E
OP-07	OP-07
OP-07/883B	OP-07/883B
OP-27A	OP-27A
OP-27A/883B	OP-27A/883B
OP-27C	OP-27C
OP-27C/883B	OP-27C/883B
OP-27E	OP-27E
OP-27G	OP-27G
OP-37A	OP-37A
OP-37A/883B	OP-37A/883B
OP-37C	OP-37C
OP-37C/883B	OP-37C/883B
OP-37E	OP-37E
OP-37G	OP-37G
LM108A	LM108A
LM108A/883B	LM108A/883B
LM108	LM108T
LM108/883B	LM108/883B
OP-227EN	RC4227FN
OP-227GN	*RC4227GN
OP-227AJ	*RM4227BD
OP-227AJ/883B	*RM4227BD/883B
REF-01	REF-01
REF-01C	REF-01C
REF-02	REF-02
REF-02C	REF-02C
REF-02D	REF-02D

NOTE: LTC OP-227 contains two die in a 14-pin package.

Raytheon's 4227 is a monolithic IC in an 8-pin package.

Maxim	Raytheon Semiconductor Nearest Equivalent
REF-01	REF-01
REF-01C	REF-01C
REF-01D	REF-01D
REF-02	REF-02
REF-02C	REF-02C
REF-02D	REF-02D
MAC630C	RC4190
MAX630C	RC4191
MAC630C	RC4193
MAX4193C	RC4193
MAC4391C	RC4391

Motorola	Raytheon Semiconductor Nearest Equivalent
LM101A	LM101A
LM111	LM111
LM124	LM124
LM139	LM139
LM324	LM324
LM339	LM339
LM348	RC4156
LM348	RC4157
LM4136	RC4136
MC142100	RC4444
MC1504U10	REF-01
MC1504U10	REF-01C
MC1504U10	REF-01D
MC1404U5	REF-02
MC1404U5	REF-02C
MC1404U5	REF-02D
MC1468	RC4194
MC1468	RC4159
MC1741	RC741
MC3403	RC3403A
MC4558	RC4558
MC4558	RC4559
MC4741	RC4741

Cross References

National	Raytheon Semiconductor Nearest Eqivalent
LM101A	LM101A
LM111	LM111
LM124	LM124
LM139	LM139
LM148	LM148
LM168	REF-02
LM169	REF-01
LM1851	RV4145
LM324	LM324
LM325/326	RC4194
LM331	RC4152
LM339	LM339
LM3403	RC3403A
LM348	RC4156
LM348	RC4157
LM368	REF-02C
LM368	REF-02D
LM369	REF-01C
LM369	REF-01D
LM4136	RC4136

SGS-Thompson	Raytheon Semiconductor Nearest Equivalent
LM101A	LM101A
LM111	LM111
LM124	LM124
LM139	LM139
LM148	LM148
LM324	LM324
LM339	LM339
MC4558	RC4558

Samsung	Raytheon Semiconductor Nearest Equivalent
KA2803	RV4145

Signetics	Raytheon Semiconductor Nearest Equivalent
LM111	LM111
LM124	LM124
LM139	LM139
LM324	LM324
LM339	LM339
NE5532	RC5532
NE5532A	RC5532A
NE5534	RC5534A
SE4558	RC4558
µA741	RC741
µA747	RM747

Texas Instruments	Raytheon Semiconductor Nearest Equivalent
LM101A	LM101A
LM111	LM111
LM124	LM124
LM139	LM139
LM148	LM148
LM324	LM324
LM339	LM339
LM348	RC4156
LM348	RC4157
MC3403	RC3403A
RC4136	RC4136
TL494/6/7	RC4190

Military Bipolar PROMs

Except 6617/17B

Harris Part Type	Raytheon Semiconductor Nearest Equivalent	Difference
HM7649	R29621	t_{EA}/t_{ER}/ICC
HM7649A	R29621A	t_{EA}/t_{ER}/ICC
N/A	R29623	
N/A	R29623A	
HM7681	R29631	t_{EA}/t_{ER}
HM7681A	R29631A	t_{AA}
HM7681P	R29633	t_{EA}/t_{ER}/ICCD
N/A	R29653A	
N/A	R29681	
HM7616	R29681A	t_{AA}/t_{ER}
HM76161	R29681A	t_{AA}/t_{ER}
HM6617	R29683	CMOS/DC/AC/ ICCSB/ICCOP/ Pinout
HM6617B	R29683A	CMOS/DC/AC/ ICCSB/ICCOP/ Pinout
HM76321	R29771	$t_{AA}/t_{EA}/t_{ER}$
N/A	R29773	
HM76641	R29791	
N/A	R29793	

Signetics Part Type	Raytheon Semiconductor Nearest Equivalent	Difference
82S147	R29621	
82S147A	R29621A	
N/A	R29623	
N/A	R29623A	
82S181	R29631	t_{EA}/t_{ER}/ICC
82S181A	R29631A	ICC
N/A	R29633	
N/A	R29633A	
82S185	R29651	t_{AA}/ICC
82S185A	R29651A	$t_{AA}/t_{EA}/t_{ER}$
N/A	R29653	
N/A	R29653A	
82S191	R2981	
82S191A	R29681A	t_{AA}/t_{ER}
R29683	N/A	
R29683A	N/A	
82HS32A	R29771A	t_{AA}
82HS321B	N/A	
N/A	R29773	
82HS641A	R29791	tAA
82HS641B	N/A	
N/A	R29793	

Cross References

Standardized Military Drawings

To stem the proliferation of contractor-generated Source Control Drawings (SCDs), the U.S. Government has established a program to create a single government-controlled SCD for each part in the military inventory. This document is called a Standardized Military Drawing (SMD) and is available for use by any contractor. By greatly reducing the number of part numbers thus generated, it is much more practical to maintain an inventory of these products, reducing acquisition time, cost and overhead.

Raytheon Semiconductor is a strong supporter of this program. We have a number of products currently in the system and the list is growing rapidly. Identified below are the products in the inventory at the time of publication of this data book, along with the "nearest generic equivalent" Raytheon part number. Since the Defense Electronics Supply Center (DESC) in Dayton, Ohio controls the detailed spec, we manufacture and test the product strictly in accordance with that spec. If it varies in any way from the standard specification, the SMD is the controlling document. It is important to verify from DESC that you are working from the latest revision of the SMD.

These products are not only available from the government supply channels and from the Raytheon Semiconductor factory. Many are handled through the normal commercial distribution channels, providing ready access to full-spec military products. They are all fully compliant with the latest release of MIL-STD-883.

If you need a product not listed here, contact the factory. It may be in progress; if not, we will be delighted to work with you to add it to the program.

SMD	Suffix	Raytheon Part No.	Description
5962-87600	01XA	TDC1048B6V	8Bit 20 Msps A/D
	103A	TDC1048C3V	
5962-87786	01VA**	TDC1046B8V	6Bit 20 Msps A/D
5962-88532	01XA**	TDC1049J0V	9 Bit 30 Msps A/D
	01YA**	TDC1049J3V	9 Bit 30 Msps A/D
	01ZA**	TDC1049C1V	
	01UA**	TDC1049L1V	
5962-88739	01QA	TMC208KB5V	8x8 Bit Multiplier
	02QA	TMC208KB5V1	
	03QA	TMC28KUB5V	
	04QA	TMC28KUB5V1	
	01XA	TMC208KC2V	
	02XA	TMC208KC2V1	
	03XA	TMC28KUC2V	
	04XA	TMC28KUC2V1	
5962-89446	01LA	TMC2011B2V	3-18x8 Shift Register
	013A	TMC2011C3V	
	02LA**	TMC2111B2V	
	023A**	TMC2111C3V	
5962-89711	01JA	TMC2023B7V	64 Bit Correlator
	02JA	TMC2023B7V1	
	03JA	TMC2023B7V2	
	04JA	TMC2023B7V3	
	013A	TMC2023C3V	
	023A	TMC2023C3V1	
	033A	TMC2023C3V2	
	043A	TMC2023C3V3	
	01LA	TMC2023B2V	
	02LA	TMC2023B2V1	
	03LA	TMC2023B2V2	
	04LA	TMC2023B2V3	

SMD	Suffix	Raytheon Part No.	Description
5962-89715	01XC**	TMC2301G8V	Image Rotation Seq.
	02XC**	TMC2301G8V1	
	01YA**	TMC2301L1V	
	02YA**	TMC2301L1V1	
5962-89828	01EA**	TDC1044B9V	4 Bit 25 Msps A/D
5962-90596	01JA	TDC1012J7V1	12 Bit ECL DAC
	013A**	TDC1012C3V1	
	02JA	TDC1012J7V2	
	023A**	TDC1012C3V2	
5962-90708	01XCA**	TMC2208J4V	8x8 Bic MAC
5962-90996	01MYA	TMC2009C1V	12x12 Bit MAC
	01MXA	TMC2009J3V	
	01MZA	TMC2009L1V	
5962-91652	01MJC	TDC1112J7V1	12 Bit ECL DAC
	01M3A	TDC1112C3V1	
	02MJC	TDC1112J7V2	
	02M3A	TDC1112C3V2	
5962-86879	01EX	RM3182S/883B	ARINC 429 Differential Line Driver
	013A	RM3182L/883B	
5962-8958	102GA	REF01T/883B	+10V Precision Voltage Reference
	102PA	REF01D/883B	
5962-87738	01GA	OP77BT/883B	Precision Operational Amplifier
	01PA	OP77BD/883B	
	02GA	OP77AT/883B	
	02PA	OP77AD/883B	
5962-87739	01CA	LM139AD/883B	Single Supply Quad Amplifier
5962-88537	01GA	OP37AT/883B	Low Noise Operational Amplifier
	01PA	OP37AD/883B	
	02GA	OP37BT/883B	
	02PA	OP37BD/883B	
	03GA	OP37CT/883B	
	03PA	OP37CD/883B	
7700801CA		LM139D/883B	Single Supply Quad Comparator
7705001CA**		RC2211D/883B	FSK Demoduclator/Tone Decoder
7705401CA**		RM4194D/883B	Dual Tracking Voltage Regulator
7704301CA		LM124D/883B	Single Supply Quad Operational Amplifier
82008013A		R29771LM/883B	4096 x 8 Bipolar PROM
8200801JA			
8200801LC**			
82008043A			
8200804JA			
8200804LC**			
8200901LC**		R29791SM/883B	8192 x 8 Bipolar PROM
8200901JA			
8200901XC			
8203601GA		OP07AT/883B	Precision Operational Amplifier
8203601PA		OP07AD/883B	
8203602GA		OP07T/883B	
8203602PA		OP07D/883B	

Cross References

MIL-M-38510 Products

M38510 Part No.	Raytheon Part No.	Description
10101BCA	MM0741 DCA	General Purpose Operational Amplifier
10101BGA	MM0741 TEA	
10101BPA	MM0741 DEA	
10102BAA**	MM0747CJA	General Purpose Dual Operational Amplifier
10102BCA	MM0747 DCA	
10102BDA	MM0747CAA	
10102BIA	MM0747 TFA	
10103BCA	MM0101ADCA	General Purpose Operational Amplifier
10103BGA	MM0101ATEA	
10103BHA	MM0101ACQA	
10103BPA	MM0101ADEA	
10104BGA	MM0108ATEA	Precision Operational Amplifier
10104BPA	MM0108ADEA	
10104B2A**	MM0108ALSA	
10105BEA	MM2101ADMA	General Purpose Dual Operational Amplifier
10106BEA	MM2108ADMA	Precision Dual Operational Amplifier
10304BCA	MM0111 DFA	Voltage Comparator
10304BGA	MM0111 TEA	
10304BHA	MM0111CQA	
10304BPA	MM0111 DEA	
10304B2A**	MM0111LSA	
10305BEA	MM2111 DMA	
11001BCA	MM0148 DCA	Low Power Quad Operational Amplifier
11003BCA**	MM4156 DCA	High Performance Quad Operational Amplifier
11003BDA**	MM4156CAA	
11004BCA	MM4136 DCA	General Performance Quad Operational Amplifier
11005BCA	MM0124 DCA	Single-Supply Quad Operational Amplifier
11201BCA	MM0139 DCA	Single-Supply Quad Comparator
11201BDA	MM0139CAA	
11201B2A**	MM0139LSA	
11301BEA	MM4818 DMA	8-Bit Multiplying D/A Converter
11302BEA	MM4818ADMA	
13101BGA**	MM5534ATEA	Low Noise Operational Amplifier
13101BPA**	MM5534ADEA	
13102BPA**	MM5532ADHA	Low Noise Dual Operational Amplifier
13501BPA	MM4807ADEA	Precision Operational Amplifier
13501BGA	MM4807ATEA	
13501B2A**	MM4807ALSA	
13502BPA	MM4807 DEA	
13502BGA	MM4807 TEA	
13502B2A**	MM4807LSA	
20902BVA	JR29651DQ	2048 x 4 Bipolar PROM
20904BJA	JR29631DR	1024 x 8 Bipolar PROM
21002BJA	JR29681DR	2048 x 8 Bipolar PROM

**Indicates sole source

Section 6
Quality & Reliability

Raytheon's Commitment to Customers

Raytheon Semiconductor is dedicated providing innovative high performance mixed-signal semiconductor products.

The company has embraced the Total Quality Management (TQM) concept for continuously improving its products and services.

Raytheon Semiconductor maintains relationships which are based upon integrity, open communication and commitment to mutually beneficial, long term business partnerships with its customers and suppliers.

Our definition of quality is meeting customer requirements 100% of the time. The responsibility for this quality is shared by all employees.

With these commitments in mind, the Division has developed a comprehensive Quality/Reliability Policy Manual. Raytheon welcomes the opportunity to discuss these policies with its customers and suppliers, and solicits their questions, comments and/or recommendations for improvement.

Reliability Concepts

Reliability is defined as the probability that product will perform its' intended function for a specified period of time. The reliability model generally assumed for Integrated Circuits is that the failure rate over time follows a "bathtub" curve.

This model predicts an early "infant mortality" period where the failure rate is controlled by extrinsic defects. After these initial failures occur, the failure rate is essentially random and depicts the useful life of the product. In this region of the curve a prediction of the Failure rate In Time can be made, expressed as FITs (assuming a constant failure rate). The "bathtub" curve also predicts a final period in the product life where the failure rate is controlled by wear-out mechanisms inherent in the device construction.

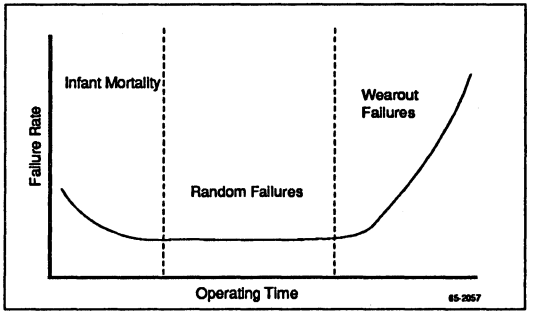


Figure 1. Failure Rate vs. Time

Integrated circuits have demonstrated characteristically long product lifetimes. In order to estimate the reliability of these products, it is necessary to understand extrinsic and intrinsic failure mechanisms and to accelerate possible "useful life" failures. Physical and environmental testing allows an understanding of potential defects contributing to early failures. For extended life prediction, the Arrhenius Model is used to extrapolate from accelerated testing of the product to useful field life.

The Arrhenius Model was originally developed to describe temperature accelerated chemical reaction rates, and is used to predict time/temperature relationship of Integrated Circuit failure rates. Increased temperature operation is one method of accelerating failure. The Arrhenius Model predicts an exponential relationship of temperature and intrinsic failure rate. Using failure statistics obtained from high temperature operation, the failure rate of the process can be estimated and extrapolated to a specified operating temperature range for the product family. An "activation energy" for the expected failure mechanism is used for this estimate of the expected failure rate under use conditions.

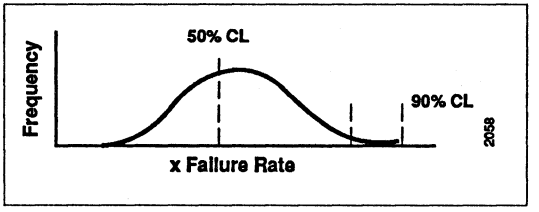


Figure 2. Frequency vs. Failure Rate

The infant mortality and random failures periods can be described through a series of probability calculations. The probability of having a failure at a specific point in time can be expressed by the equation:

$$P_O = e^{-xt}$$

where:

x = the failure rate (failures per unit time)
t = time

The failure rate "x" is usually expressed in % failures per 1000 hours and is sometimes expressed as a mean time between failures (MTBF) through the expression:

$$MTBF = \frac{1}{\text{Failure Rate}}$$

Since the data for the failure rate calculations is derived from a sample of devices from a production lot, a confidence level number is usually stated for the failure rate estimation. A 60% confidence level (CL) is used for the purposes of these calculations.

The failure rate "x" is calculated by using a Chi square (χ^2) distribution through the equation:

$$c = \frac{\chi^2(x.2r + 2)}{2nt}$$

where:

x = 100-%CL/100
r = number of rejects
n = total number of devices
t = time

The number of failures over a period of time (x) is critical in determining an accurate failure rate number. If only device failures at room or operating temperatures were counted, it would take a large number of failures over a long period of time to gather sufficient data. Therefore, accelerated test methods using elevated temperatures are used. Temperature is used to accelerate failures in a device and the increase can be expressed in a form of the Arrhenius equation which states that the reaction rate increases exponentially with temperature.

$$R = R_O e^{\frac{-E}{kT}}$$

where:

R = reaction rate as a function of time and temperature
R_O = constant related to temperature
T = Kelvin temperature
E = activation energy (electron volts)

When this equation is plotted, as shown in Figures 3 and 4, it can be used to determine the failure rate at temperatures other than the test temperature of the device.

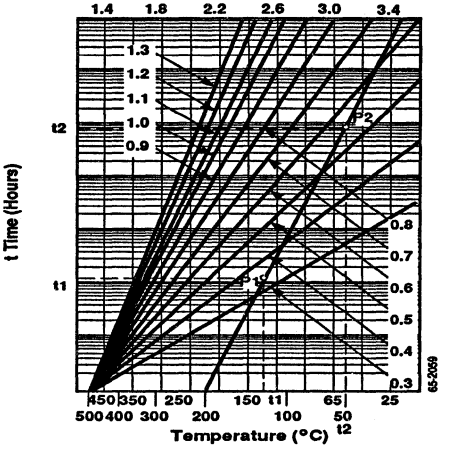


Figure 3. Normalized Time-Temperature Regressions for Various Activation Energy Values (1000/°K)

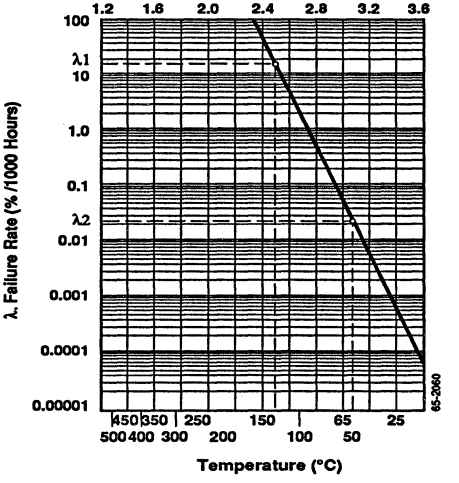


Figure 4. Failure Rate (1000/°K)

Table I. Group A Electrical Tests for Class B Devices(1)

Subgroups(2) Quality/Accept No. = 116/0 (3)(4)
Subgroup 1 Static tests at 25°C
Subgroup 2 Static tests at maximum rated operating temperature
Subgroup 3 Static tests at minimum rated operating temperature
Subgroup 4 Dynamic tests at 25°C
Subgroup 5 Dynamic tests at maximum rated operating temperature
Subgroup 6 Dynamic tests at minimum rated operating temperature
Subgroup 7 Functional tests at 25°C
Subgroup 8A Functional tests at maximum rated operating temperatures
Subgroup 8B Functional tests at minimum rated operating temperatures
Subgroup 9 Switching tests at 25°C
Subgroup 10 Switching tests at maximum rated operating temperature
Subgroup 11 Switching tests at minimum rated operating temperature

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
2. The applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in Table I.), or sets of subgroups.
3. The sample plan (quantity and accept number) for each test shall be 116/0.
4. If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

Table 2 Group B Tests for Class B (1)(2)

Test	MIL-STD-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 2(3)			
a. Resistance to solvents	2015		3(0)
Subgroup 3			
a. Solderability(4)	2022 or 2003	Soldering temperature of 245 ±5°C	10
Subgroup 5			
a. Bond strength(5)	2011		
1. Thermocompression		1. Test condition C or D	
2. Ultrasonic or wedge		2. Test condition C or D	
3. Flip-chip		3. Test condition F	
4. Beam Lead		4. Test condition H	

Notes:
1. Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Subgroups 1, 4, 6, 7, and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.
3. Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.
4. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
5. Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see Method 2011).

Table 3. Group C (Die-Related Tests — For Class B only)

Test	MIL-STD-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 1			
a. Steady-state life test	1005	Test condition to be specified (1,000 hours at 125°C or equivalent in accordance with Table 1.)	5
b. End-point electrical parameters			

Table 4. Group D (Package Related Tests)

Test	MIL-STD-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 1 (1)			
a. Physical dimensions	2016		15
Subgroup 2 (1)			
a. Lead integrity (2)	2004	Test condition B_2 (lead fatigue)	5
b. Seal (3)			
1. Fine	1014	As applicable	
2. Gross			
Subgroup 3 (4)			
a. Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum	15
b. Temperature cycling	1010	Test condition C, 100 cycles minimum	
c. Moisture resistance (5)	1004		
d. Seal	1014	As applicable	
1. Fine			
2. Gross			
e. Visual examination		In accordance with visual criteria of Method 1004 &1010	
f. End-point electrical parameters (6)		As specified in the applicable device specification	
Subgroup 4 (4)			
a. Mechanical shock	2002	Test condition B minimum	15
b. Vibration, variable frequency	2007	Test condition A minimum	
c. Constant acceleration	2001	Test condition E minimum (see 3), Y_1 orientation only	
d. Seal	1014	As applicable	
1. Fine			
2. Gross			
e. Visual examination(7)			
f. End-point electrical parameters		As specified in the applicable device specification	
Subgroup 5 (1)			
a. Salt atmosphere (5)	1009	Test condition A minimum	15
b. Seal	1014	As applicable	
1. Fine			
2. Gross			
c. Visual examination		In accordance with visual criteria of Method 1009	
Subgroup 6 (1)			
a. Internal water-vapor content(8)	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1)
Subgroup 7 (1)			
a. Adhesion of lead finish (9,10)	2025		15
Subgroup 8			
a. Lid torque (1)	2024		5(0)

Notes:
1. Electrical reject devices from that same inspection lot may be used for samples.
2. For leadless chip carrier packaged only, use test condition D. For leaded chip carrier packages, use condition B1. For pin grid array and other rigid leads use Method 2038.
3. Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.
4. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
5. Lead bend stress initial conditioning is not required for leadless chip carrier packages.
6. End-point electrical parameters are performed after moisture resistance and prior to seal test.
7. Visual examination shall be in accordance with Method 1010 or 1011.
8. Test three devices; if one fails, test two additional devices with no failures. At the manufacturers option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot.
9. The adhesion of lead finish test shall not apply to leadless chip carrier packages.
10. LTPD based on number of leads.

Table 5. Typical Qualification Plan for Hermetic Packaged Devices (1)(2)(3)

Test	Conditions Per MIL-STD-883	Quantity	Accept No.
Group B			
Subgroup 3		15	0
Solderability	245 5°C		
Subgroup 5		15	0
Bond Strength	Condition C and record bond pull strength		
Group C			
Subgroup 1		77	1
Operational Life (168, 250, 500, 1000, 2000) Electrical Test 25°C DC) (2 date codes, 77 samples each)	168-hour point will be used to screen out the infant mortality failure. The sample size after the 168-hour point will be 77.		
Group D			
Subgroup 2		25	1
Lead Integrity	Condition B_2		
F&G Leak			
Lid Torque			
Subgroup 4		25	1
Mechanical Shock	Condition B		
Vibration	Condition A		
Constant Acceleration	Condition B Min.		
F&G Leak			
Visual Examination			
Electrical Test 25°C			

Notes:

1. The above group B, C, D are run completely, if the product (package and die) has no history.
2. If the package is pre-qualified, then only Group C, Subgroups 1 and 2, and Group D, Subgroup 4 are conducted.
3. If the product is not JAN or 883 compliant, then 168-hour pre-burn in is not performed to screen out infant mortality prior to Group C Test.

Table 6. Typical Qualification Plan for Plastic Package Devices

Test	Test Conditions	Purpose of Test	Sample Size	Accept No.
Operating Life	Temperature 125°C Time 1000 hrs. Electrical Test at 168 hrs., 500 hrs., 1000 hrs., 250 hrs. Bias — per spec requirements	Accelerated Life	45	0
Autoclave	Pressure 15 PSiG Temperature 121°C, >95° RH Electrical Test at 96 hrs., (no metal deterioration), 144 hrs., 250 hrs., 500 hrs.	Package integrity and moisture resistance	45	0
85°C/85% RH	Temperature 85°C Humidity 85% Time 1000 hrs. (no metal deterioration) Electrical Test at 168 hrs., 250 hrs., 500 hrs., 1000 hrs.,	Accelerated life corrosion resistance	45	0
Storage Life	Temperature 150°C Bias — None Electrical Test at 144 hrs., 250 hrs., 500 hrs.	Determine the effect of high temperature storage	45	0
Temperature Cycle	Temperature -65°C to +150°C No. Cycles 100 Electrical Test 25°C	Determine the resistance to high and low temperatures	45	0
Thermal Shock	Per 883 Method 1011	Determine resistance to rapid temperature change.	45	0
Moisture (10 Day)	Temperature -10°C to +65°C Humidify 90% RH Time 240 hrs. Electrical Test at 240 hrs. Visual Inspection of Leads	Package integrity to moisture, lead corrosion, etc.	45	0
Solderability	Per 883, Method 2003	To determine the solderability of the lead finish	3	0
Lead Fatigue	Per 883, Method 2004 Condition B	To determine the physical resistance to lead bending fatigue	3	0
External Visual	10-30X Magnification	To evaluate physical construction and processing results to package and lead frame	45	0

*2 date codes of 50 each

Reliability Program

The quality and reliability activity at Raytheon is a thorough and continuous activity. It starts with initial design concepts and processes, and carries through to the finished product.

Reliability Engineering, working with Design and Product Engineering, monitors the new device design or process through all stages of development and remains the full and final authority over the qualification status of all products.

Raytheon's established RA Qualification plans are used to approve new devices, processes or manufacturing facilities. Two examples are shown in Tables 5 and 6 for hermetic package devices and plastic package devices.

The Reliability Department continually monitors all product lines through product sampling, routine re-qualification and QCI testing of JAN and other Hi-Rel products to evaluate failure modes and failure rates. The results from these tests are reviewed with Product and Production Engineering and any necessary corrective actions are taken.

Lab Facilities

Raytheon maintains a fully equipped laboratory to conduct its reliability, failure analysis, and environmental testing. The typical types of tests that are performed by this facility include:

- QCI Groups A, B, C and D environmental requirements
- Destructive Physical Analysis
- SEM Analysis
- Microprobe Analysis/Laser Cutter
- X-ray Dispersion Analysis
- Biased 85/85 and Steam Pressure Pot (PCT)
- Highly Accelerated Stress Testing (HAST)
- Electromigration Characterization
- TDDB Testing of MOS Gate Oxide
- Hot Carrier Degradation
- ESD Testing
- PIND Testing

Plastic Package Device Monitor

Raytheon is a major supplier of standard and ASIC products in plastic packages. Products are available in a variety of plastic packages such as DIPs, SOICs, and LCCs. Significant investments have been made in both the technology and manufacture of high-reliability, low-stress plastic encapsulated packages.

Table 7. Typical Plastic Process Monitor Tests

Test	Purpose of Test
Autoclave (steam pressure)	To evaluate the resistance of moisture penetration of the package and the effects of moisture on the chip under accelerated conditions of 15 pounds of steam pressure at 120°C.
Biased 85°C/85% RH	To evaluate the operational life and resistance to moisture penetration of the chip and the plastic package under the accelerated conditions of 85°C and 85% relative humidity.
Operating Life	To evaluate the operational field life of the device under accelerated conditions of 125°C.
Resistance to Solvents	To determine that the brand markings will not become illegible on the package parts when subjected to the solvents and test per MIL-STD-883C, Method 2015.
Solderability	Per Method 2004 of MIL-STD-883.
External Visual	To determine the physical construction and processing results to the package and lead frame at 30X magnification.
Lead Fatigue	To determine the physical resistance to lead bending fatigue per Condition B, Method 2004, of MIL-STD-883.
Thermal Shock	To determine that the device can survive exposure to rapid changes in temperature from -55°C to +125°C per Condition B of Method 1011 of MIL-STD-883.

In addition to quality control check point inspection at every assembly step, reliability process monitoring (see Table 7) is performed.

The autoclave (steam pressure) test determines the package's moisture resistance in the shortest possible time, allowing immediate corrective action where necessary, thus ensuring the long-term reliability of the products.

All products are 100% electrically tested and visually screened followed by sample testing for electrical, visual and mechanical defects to determine the outgoing PPM defect rate. With a quality goal of 100 ppm or less, Raytheon's devices have failure rates well below the industry standards.

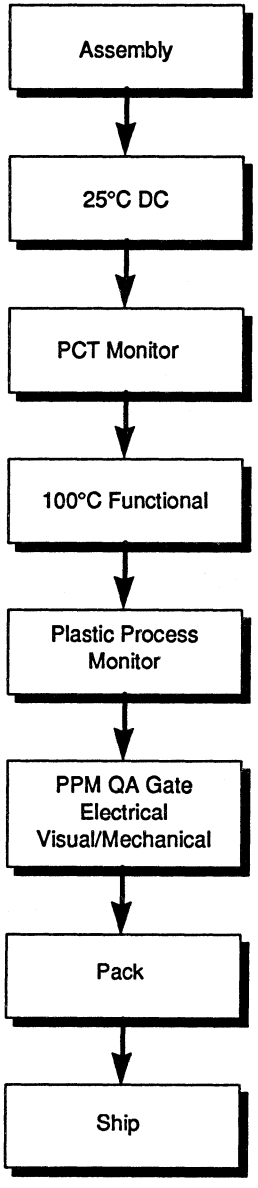


Figure 5. Linear Plastic Flow Chart

Major Programs

Raytheon Semiconductor is involved in major programs which require and support a high level of quality and reliability expertise in the design, manufacture and control of our products.

The commercial programs address such market segments as computers and automotive. These markets are a driving force within Raytheon's commercial product quality and reliability controls.

The most significant military program is JAN 38510 which requires a Defense Electronics Supply Center (DESC) certification of our fabrication and manufacturing lines. The JAN military specifications and MIL-I-45208 form the foundation of our QA system, thereby benefiting all products — JAN, 883 compliant, DESC Standard Military Drawings (SMD), Source Control Drawings (SCD), and commercial.

An extensive statistical process control program has been initiated which includes wafer fabrication processing, quality assurance monitors, assembly monitors, environmental screening and electrical testing.

Internal Audit Program

Raytheon Semiconductor maintains an internal audit program which requires the auditing of all product processing and control systems. This audit verifies conformance to manufacturing and quality procedures identifying areas needing improvement and enhancement.

Process Monitors

Extensive process monitors in fab, assembly and electrical test are a critical part of Raytheon's quality program. These enable early detection of process problems as well as characterization of process improvements.

Reliability Monitor

The Reliability Monitor Program monitors, on a continuing basis, the reliability of all IC products in hermetic and plastic packages. This program requires that periodically several different part types from each microcircuit technology group as detailed in Appendix E of MIL-M-38510 be evaluated to the MIL-STD-883 Test Method 5005 Groups A, B, C and D test requirements. The data generated from this program provide a basic library of reliability information on many product types

and is used to provide Quality Conformance Inspection (QCI) data to meet customer-specific group test data requirements.

Military Programs

JAN-MIL-M-38510

Raytheon's foremost commitment is to the JAN MIL-M-38510 program which is administered by the Defense Electronics Supply Center (DESC) and the Defense Logistics Agency (DLA) of the Department of Defense. We maintain DESC certified wafer fabrication, assembly and test facilities which allow us to provide an extensive number of JAN QPL device types.

The JAN 38510 program is designed to provide a consistently high reliability hermetic product manufactured to a standard process flow and quality/reliability program as defined in MIL-M-38510, MIL-STD-976 and MIL-STD-883 and the resulting baselines.

A JAN device is identified and branded with a unique part number as shown in Figure 7 and Table 8. The device is also branded with our manufacturers' designating symbol (CORP or RP), logo (RAY or R), the sealing cycle date code, country of origin, a two-digit fab quarter code (indicating year and quarter in which die fabrication was completed, and the applicable electrostatic discharge sensitivity identifier.

A current listing of Raytheon's JAN 38510 QPL devices may be obtained by contacting the nearest Raytheon Field Sales Office.

883 Compliant

The 883 compliant program offers hermetic products assembled and tested to the requirements of paragraph 1.2.1 of MIL-STD-883 for Class B devices. With Raytheon as the qualifying activity and offshore assembly permissible, these devices are as close as one can get to JAN 38510 reliability using a standard process flow (See Figure 6).

Raytheon's 883 compliant program is complemented by our active participation in DESC's Standard Military Drawing program.

A current listing of our 883 compliant devices which includes those DESC SMDs for which Raytheon is an approved source of supply may be obtained by contacting the nearest Raytheon Semiconductor Field Sales Office.

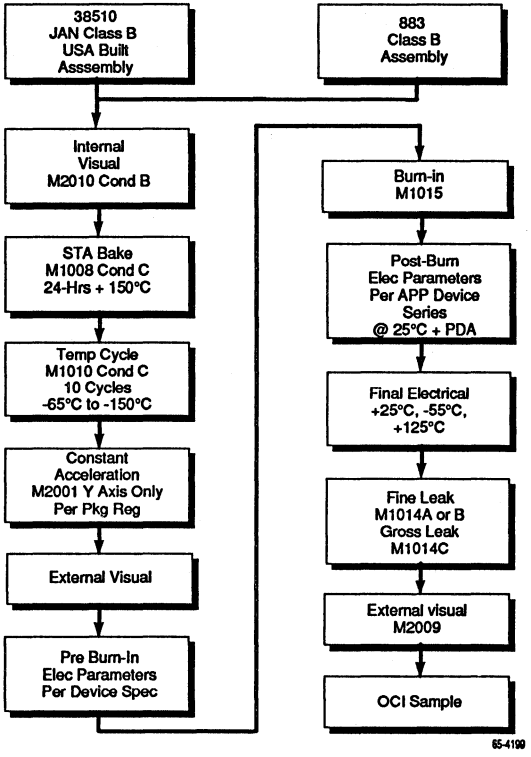


Figure 6. Screening for JAN and 883 Compliant Devices

Lead Finish

Raytheon offers two lead finished — solder dipped and matte tin plate (non-JAN only). The preferred and recommended lead finish is solder which is tin plated prior to dipping.

Raytheon offers a solder lead finish that will meet the solderability requirements of MIL-M-38510.

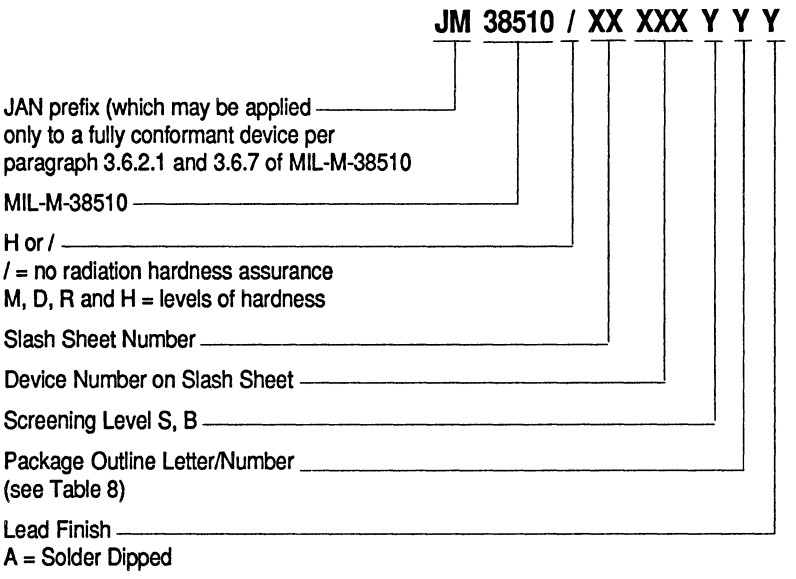


Figure 7. MIL-M-38510 Part Marking

Table 8. JAN Package Codes

38510 Outline Letter/Number	38510 Type Designation	Description
A	F-1	14-lead, 1/4 x 1/4 Cerpak
B	F-3	14-lead, 3/16 x 1/4 Cerpak
C	D-1	14-lead, 1/4 x 3/4 Cerdip
D	F-2	14-lead, 1/4 x 3/8 Cerpak
E	D-2	16-lead, 1/4 x 7/8 Cerdip
F	F-5	16-lead, 1/4 x 7/8 Cerpak
G	A-1	8-lead, TO-99 can
H	F-4	10-lead, 1/4 x 1/4 Cerpak
I	A-2	10-lead, TO-100 can
J	D-3	24-lead, 1/2 x 1-1/4 Cerdip
K	F-6	24-lead, 3/8 x 5/8 Flatpak
L	D-9	24-lead, 1/4 x 1-1/4 Cerdip
P	D-4	8-lead, 1/4 x 3/8 Cerdip
Q	D-5	40-lead, 2 x 5/8 DIP
R	D-8	20-lead, 1/4 x 1-1/16 Sidebraze DIP
S	F-9	20-lead, 1/4 x 1/2 Cerpak
V	D-6	18-lead, 1/4 x 5/16 Cerdip
2	C-2	20-terminal, 3/8 x 3/8 Chip Carrier
3	C-4	28-terminal, 1/2 x 1/2 Chip Carrier

Section 7
Application Notes

Contents

RC4151/52/53
Voltage-to-Frequency Converters

Contents

RC4151/52/53
Voltage-to-Frequency Converters
Application Notes

Prepared by
Bruce Moore

INTRODUCTION

A Voltage-to-Frequency Converter (VFC) acts just as the name suggests: it converts a DC input voltage into a pulse output frequency. As the magnitude of the input voltage increases, the output frequency increases. This is a linear relationship, and high linearity means accuracy in conversion. By connecting the frequency output to a digital counter, and counting for a precise interval, a binary number is stored directly proportional to the input voltage. This creates a voltmeter, or integrating A/D converter.

The conversion is accomplished with a charge balanced feedback loop. This analog method of conversion and its inherent linearity assure that over the entire range of input voltages, there will consistently be a proportional binary code from the counter. This means that the system is inherently monotonic. Specifically, a converter with .01 percent nonlinearity has accuracy and monotonicity equivalent to a 12 bit parallel A/D converter.

When compared to the other methods of A/D conversion, the VFC's disadvantage is longer conversion time, equal to the sample period. This disadvantage can be a positive design feature for measurements in a noisy environment, because the longer sampling period averages out noise. The conversion time may be reduced by using a VFC which is accurate at higher frequency. Raytheon's 4153 VFC can give 3-1/2 digit conversion in less than 5mS. Successive approximation techniques are fast, but very sensitive to noise. In comparable systems, the three different methods of conversion are equivalent in resolution, temperature sensitivity, and nonlinearity. Dual slope conversion is a compromise betweeen successive approximation and V-to-F conversion, because it has good noise rejection and a moderate conversion time.

Modern integrated circuit technology made the VFC a cost effective alternative to these other A/D systems. A few years ago the VFC was a black box; bulky and expensive. Then hybrid and modular versions were introduced, bringing efficiency and priced under one hundred dollars. In 1976 Raytheon introduced the world's first monolithic VFC, the 4151. Since then the 4152 and 4153 have been designed, for increased performance and with fewer external components. Raytheon's monolithic converters offer competitive performance when compared with modular versions, while providing increased flexibility in modifying design parameters, and costing much less.

The future will see increased use of VFC's in places where other methods of conversion are presently employed in addition to a variety of newer non-conventional applications. The advantages of VFC's are in their size, cost, and serial output, which allow them to be located near the source of analog data. VFC's can provide the inverse function, frequency-to-voltage conversion. Raytheon converters can be connected in a number of configurations to fill most needs. The applications described in this publication include microprocessor interfacing, motor speed controls, phase lock loops, and other unique circuits.

BASIC OPERATION

The output of a VFC consists of a series of negative going pulses. The pulse width remains constant (one shot period determined by external components) while the duty cycle varies in response to the input voltage. Thus it is an A/D converter with a serial output. Figure 1 and 2 show the principles of a positive input precision mode VFC using a 4153.

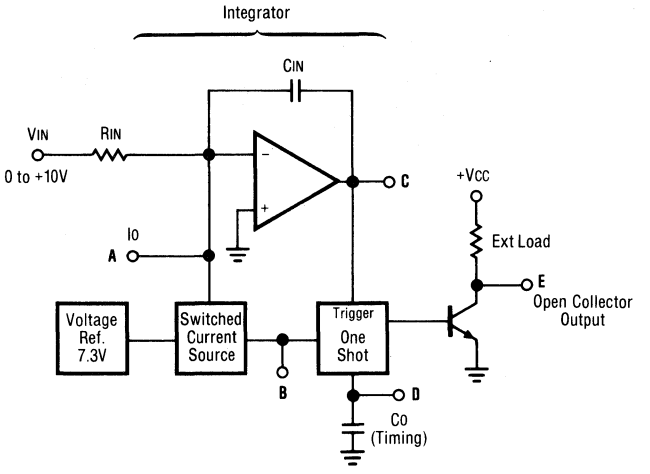


Fig. 1 VFC Block Diagram

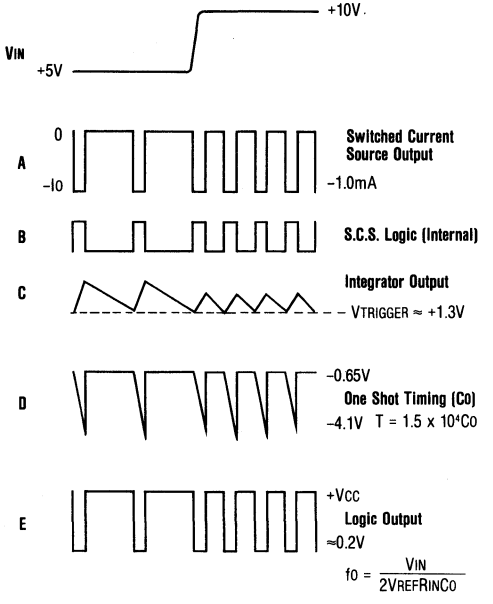


Fig. 2 4153 Timing Waveforms

The heart of a VFC is the switched current source, which can deliver discrete amounts of charge precisely controlled in amplitude and duration.

The integrator algebraically sums the positive current, V_{IN}/R_{IN}, with the negative current pulses from the switched current source. This integrated sum (waveform C of Figure 2) is applied to the trigger input of the one shot. If that voltage becomes less than the trigger threshold, the one shot fires, pulsing the switched current source and the logic output (waveform E). The I_{OUT} pulse from the current source causes the integrator output to ramp up for the period of the one shot, and then ramp back down to the trigger voltage. The slope of this downward ramp is proportional to the input voltage. The system acts as a charge balanced loop, with the interval between one shot firings determining the duty cycle, proportional to the input voltage. To summarize; the one shot works continually, by increasing the frequency of I_{OUT} pulses, to keep the output of the integrator above the trigger threshold. If the positive input increases the frequency of negative I_{OUT} pulses will increase to keep the integrator output high.

Comparison of the 4151 and 4152 to the 4153

The 4151 and 4152 operate much like the 4153, except for differences in polarity and voltage as Figure 3 illustrates. For the precision circuit, the input voltage must be negative, because the switched current source output is positive.

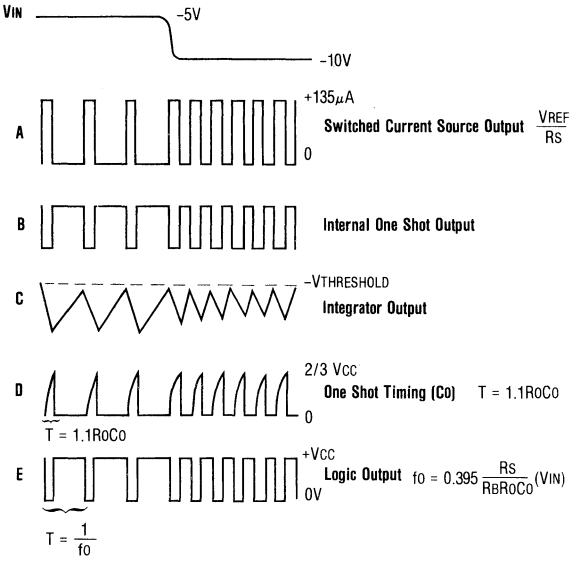


Fig. 3 4151/4152 Timing Waveforms

Consequently the integrator ramps up to the one shot threshold instead of down. The one shot comparator threshold is set externally, and the one shot waveform is inverted. The equations for one shot time and output frequency also differ. These differences are attributable to the philosophy with which the 4153 was designed. The 4153 was intended to be connected in the precision configuration, and contains an internal op amp. The current output was made negative so that the input voltage would always be positive. This function meets more user needs than the requirement of a negative input and allows the use of high performance NPN transistors in the switched current source.

The 4151 was the first monolithic VFC, providing the basic function at low cost (less than one dollar in quantity). The 4151 was followed by the 4152 as a pin compatible replacement offering improved specifications, especially temperature drift. The 4153 combines the basic components with an on board op amp to minimize the number of external components required for precise applications, giving the user additional convenience and improved specifications for temperature drift and linearity, especially at frequencies over 10 kHz.

The graphs in Figures 4 through 9 show the differences in performance of the three Raytheon VFC's. The curves for the 4151 and 4152 were derived with the VFC in the current-sourced precision circuit from the 4151/4152 Data Sheet. The voltage-sourced circuit is slightly different, it has pin 1 (Io) connected to ground rather than to the summing mode of the op amp. When compared to the current-sourced circuit, the voltage-sourced circuit optimizes temperature performance at the expense of linearity.

Figure 4 depicts how linearity is degraded with increasing full scale frequency. Degradation occurs because of switching problems in the one shot affecting the total amount of charge in each Io pulse. Variations from the precise charge cause deviations in the integrator output, affect the intervals between triggering, and change the output frequency from its ideal. Notice that the 4153, with its high speed ECL logic, has improved high frequency linearity.

Temperature drift is affected by increasing frequency as illustrated in Figures 5 and 6 at 10 kHz and 100 kHz. The 4153, with its buried zener reference, outperforms the 4151 and 4152. The reference, the switched current source, the resistor and capacitor temperature coefficients all contribute to temperature drift.

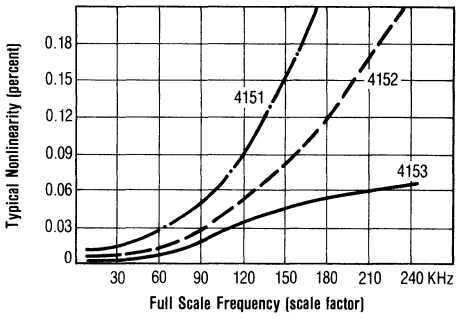


Fig. 4 Scale Factor vs. Typical Peak Nonlinearity

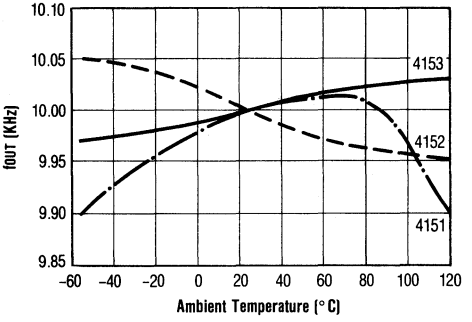


Fig. 5 10KHz Full Scale Temperature Drift

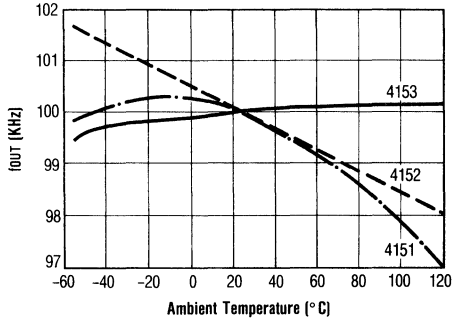


Fig. 6 100KHz Full Scale Temperature Drift

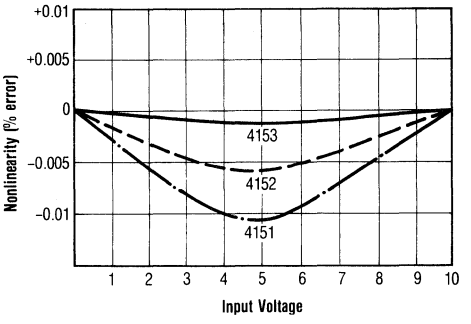


Fig. 7 10KHz V-to-F Nonlinearity

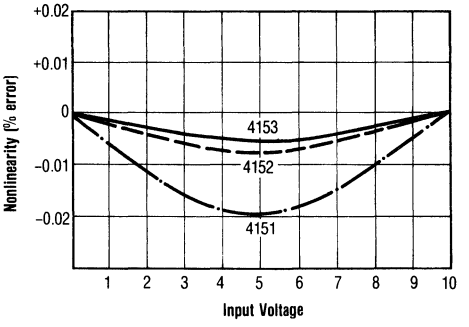


Fig. 8 50KHz V-to-F Nonlinearity

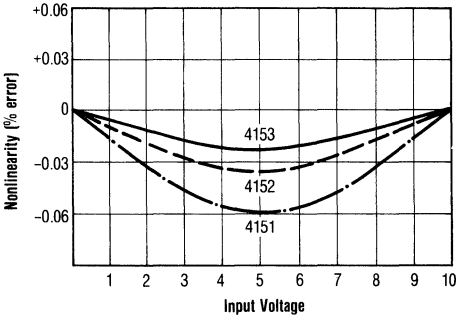


Fig. 9 100KHz V-to-F Nonlinearity

For absolute best performance use a temperature stabilized external reference, such as an LM199, heat the 4153 with an external heater, measure, then select resistor and capacitor temperature coefficients.

Frequency-to-Voltage Conversion

A VFC can also work backward. With a change in configuration the VFC will convert an input pulse train into a DC Voltage proportional to the frequency of the pulses (see Figure 10). The higher the frequency is, the higher the DC output voltage becomes. This mode has one inherent problem - the DC output contains a ripple component equal in frequency to the input pulses. The proper use of filtering can reduce this ripple, but will also decrease the response time. A trade off must be made between response time and ripple. Generally the filtering should be as large as the

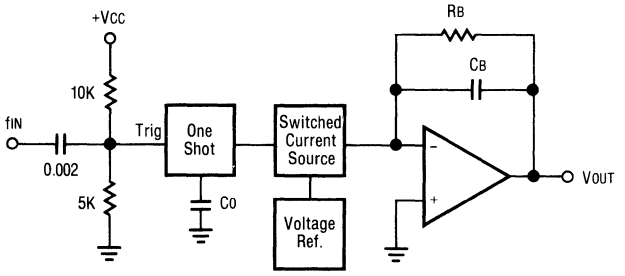


Fig. 10 Frequency-to-Voltage Conversion

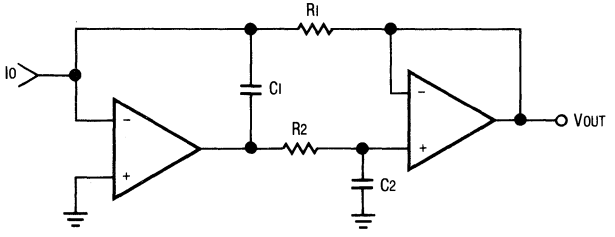


Fig. 11 Second Order Active Filter

acceptable response time will allow. The width of the pulses from the incoming frequency must be less than the period of the one shot (see appendix, FVC Signal Conditioning).

The input triggers the one shot, switching the current source, thereby delivering a well defined amount of charge to the op amp integrator. This produces an average voltage at the output proportional to the repetition rate of the incoming pulses. Replacing the single pole integrator with a second order (double pole) filter improves response time and output ripple (see Figure 11).

The ratio of the time constants R1 C1 and R2 C2 determines the response to a step change in input frequency. The response will be critically damped if R1C1 = 4(R2C2). Optimal results are obtained when R1C1 = R2C2, which provides a damping factor of one half. Choose capacitors C1 and C2 and the one shot timing capacitor for minimum ripple over the desired range of operation. Empirical tests show that the peak to peak ripple is less than 100 mV (10 Hz to 10 kHz) when R1 = 100K and C1 = 0.1 microfarad.

Frequency-to-voltage converters are useful in analog transmission systems where a VFC transmits a pulse train over a twisted pair to be received by a FVC. The FVC converts this back into a voltage for analog signal processing or chart recorder output. Other uses include motor speed controls, phase lock loops, frequency scaling, and FSK demodulation.

INTEGRATORS AND A/D'S

Long Term Integrators

Accurate analog integrators which operate over a wide dynamic range or which integrate over extended periods are difficult to build. Expensive, low drift, low leakage op amps and capacitors can be replaced by a voltage-to-frequency converter and a counter. The signal to be integrated is converted to a frequency and counted over a known sample period, providing a total count equal to the time integral of the signal (See Figure 12).

$$\int V_T = K \int F dt = K \int dN_T \quad \frac{dt}{dt} = KN$$

where N = Total count
and K = VFC Scaling Constant

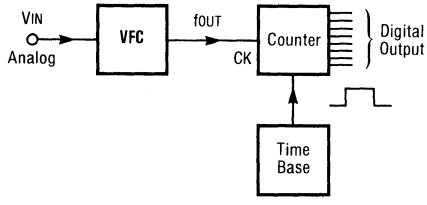


Fig. 12 Simple Integrating A/D Converter

In addition to their ability to integrate over long periods of time, VFC A/D converters have the following advantages:

1. Wide dynamic input range due to inherent VFC linearity (10,000 to 1).
2. The process can be interrupted without affecting the integrated value (no droop due to RC time constants).
3. The output may be directly interfaced to a digital information processing system, used for a seven segment display or converted back to analog with a low cost D/A converter.
4. The digital counter may be preset to any desired value before integrating up (or down).
5. The resolution and conversion speed are totally controlled by the system designer.
6. VFC A/D's have high monotonicity due to their inherent linearity.
7. High noise rejection when integrating with a sample period longer than the period of the noise.

An integrator is an A/D converter with a long sampling period. With many A/D conversions, such as a DVM, the task is not to get integration over long periods but rather to get accurate resolution in a short period. VFC's are scaled to give many pulses in this short period, in order to achieve a high binary count (increasing resolution).

For fast conversion, the 4153 offers the best linearity and temperature accuracy at high frequency. 3-1/2 digit accuracy may be obtained in 5 mS. This is comparable to many dual slope converters, at a lower cost, while retaining the transmission advantages of a VFC converter.

Design Example - Sun Power Integrator

The following example is a system that integrates the amount of sunlight on a photo cell over a 12 hour period. The maximum output of the cell is 5 volts, and the visual display must be accurate to 3 digits. Since it is easy to convert a binary count to decimal display with a binary to seven segment counter-driver, such as an ICM 7225, we need to select a VFC scale factor which will give us a count divisible by 10 after our 12 hour sampling period. The minimum scale factor is 1 Hz per volt, so the output must be equal to or greater than 10 Hz full scale. There are 43,200 seconds in twelve hours, so 43,200 is the minimum binary count per volt. The components used for 1 Hz per volt are somewhat unwieldy, therefore a larger scale factor must be used. If we use a maximum binary count of 5 million for 5V input, a 1 million binary count will equal one volt over 12 hours. One million pulses per 43,200 seconds equals a scale factor of 23.15 Hz per volt. This allows more reasonable values of resistors and capacitors (see data sheet for the specific VFC being used). The seven segment counter driver automatically decodes binary-to-decimal, however with insufficient binary counting stages internally, a pre-counter must be added. By moving the decimal place six places the display reads directly in volts.

The time base can be made from a 555 timer operating at low frequency. The 555's output can be divided further by feeding it into the clock input of a counter, giving extremely long sample periods from the MSB output.

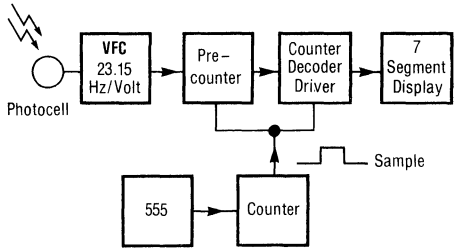


Fig. 13 Sun Power Integrator

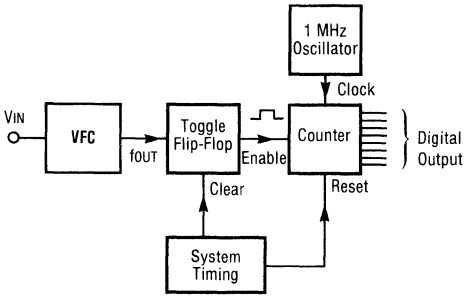


Fig. 14 Low Level Pulse Width A/D Converter

Low Level A/D Converter

A disadvantage of conventional VFC A/D converters is that the resolution of small signals is not as good as for large signals. Small voltages give a total count much less than the capacity of the counter, reducing accuracy, even though the output of the VFC is highly accurate. The normal solution is to add a preamplifier for small signals. However, this causes errors and must be switched out to measure large signals. When small signals must be processed, measure the period, rather than the frequency of the VFC output, by counting a high frequency reference oscillator during the interval between VFC pulses.

The leading edge of the first VFC pulse toggles the flip flop high, enabling the counter to begin counting the 1 MHz oscillator frequency. The leading edge of the second VFC pulse toggles the flip flop again, disabling the counter. The counter now holds a binary count inversely proportional to the voltage input. In this system, the smaller the signal, the greater the resolution. Note that the input must be large enough to provide at least two output pulses, so the interval between them may be measured.

The input may have a small DC bias applied to it, placing it on the threshold of producing an output, to provide resolution in microvolts. This technique is very useful for measuring low level transducer outputs, such as a thermocouple.

The circuit of Figure 14 has the opposite problem of the conventional VFC A/D approach. Large signals applied to the VFC cause a small period, and therefore lower the resolution, because fewer oscillator pulses will be counted. The problem is solved when we combine both techniques. The next circuit measures both the period and the frequency of the VFC output.

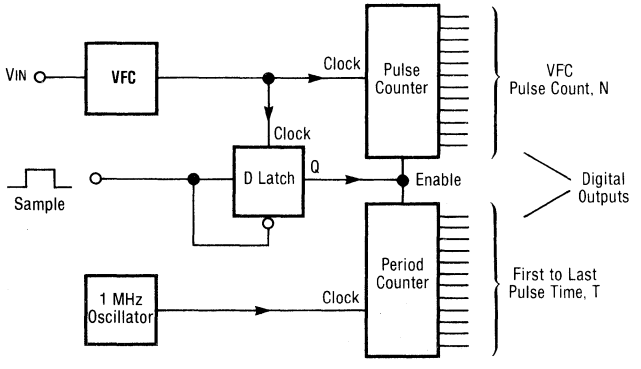


Fig. 15 High Resolution Pulse/Period A/D Converter

Process Trend Indicator

With the conventional technique of VFC integration (Figure 12), the digital count is a true representation of the integration only after the sampling period is completed. To get an integration after some intermediate time, more counters with different sampling periods would be required. The following system is another long term integrator, but has the advantage of continuously updating the digital output with a short sampling period.

The differential amplifier at the input subtracts the present VOUT from the input. This difference signal is put through an absolute value circuit and a scaling pot, which applies a positive voltage proportional to the magnitude of the differential input to the input of the VFC. During the sample period, the up/down counter counts the output frequency of the VFC. The counter counts up or down depending on the sign of the output of the differential amplifier. If the present output is greater than the input, it counts down. If the input is greater, it counts up. At the end of the sampling period the count is latched into the input of the D/A converter, which now supplies the new output. The output of the latches can be used as the digital integrated output. The time derivative of the integration (the degree of smoothing) is determined by the scaling of the inputs to the differential amplifier and by the scaling of the input to the VFC. The change of the output between samplings is proportional to the difference between the present output and the new input.

The two counters are controlled by a D-type positive edge triggered flip flop. The lower one stores a count proportional to the time between the first pulse and the last pulse in the sample period. The upper one is clocked by the VFC output pulses and stores the total number of VFC pulses in the sample period. Deriving the period between pulses and the input voltage is simple arithmetic since we know the total time for a number of pulses. Now we have a flexible system that will measure a wide range of input voltages with high resolution without the use of expensive components.

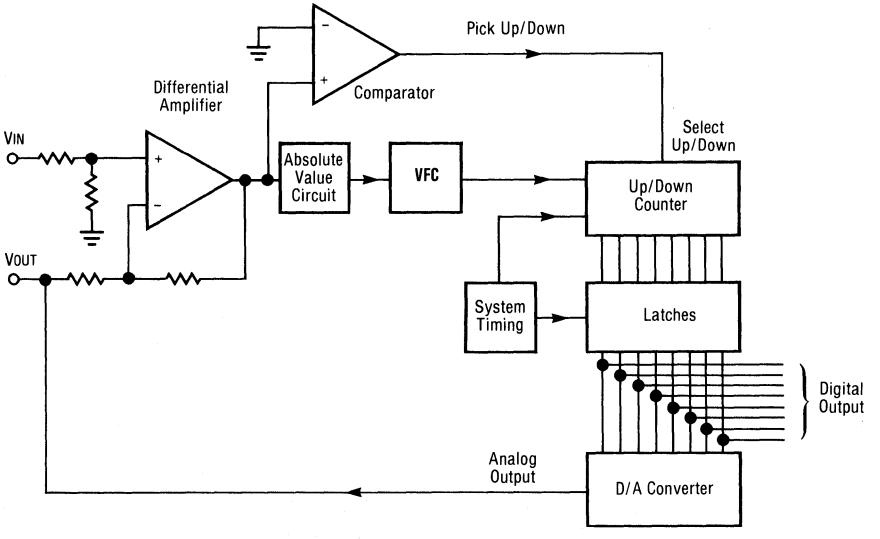


Fig. 16 Process Trend Indicator

Ratio Computers

Sometimes a need arises for a circuit that provides an output proportional to the ratio of two input signals. Examples include power measurement and transfer function determination. The circuit shown in Figure 17 uses two VFC's and some digital processing to produce a binary number proportional to the ratio of two input signals. This digital output may be used directly or converted back to a voltage with a D/A converter. $V_{IN}2$ is converted to a square wave by the flip flop. This square wave (divided by 2) is used to gate the output of VFC 1. Thus, the number of pulses from output one per pulse of output two is counted. Note: The frequency from VFC 1, and therefore the input to VFC 1, must be more than or equal to that of VFC 2.

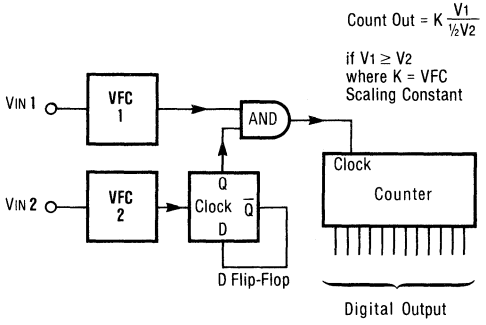


Fig. 17 Amplitude Ratio Computer

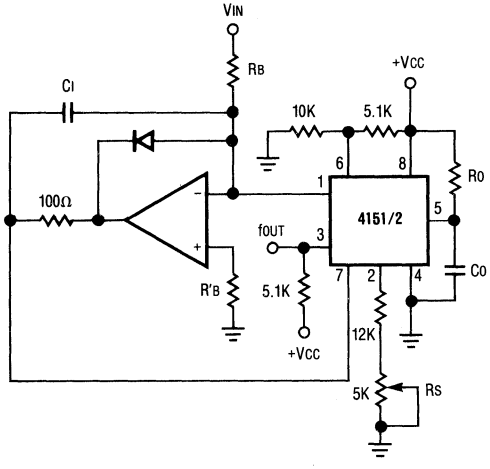


Fig. 18 Precision VFC Ratio Circuit

System timing must be tailored to individual applications. Many modifications to this design are possible. For example, over/under range alarms, channel steering for ratios less then unity, or dB or other non-linear conversions by the use of ROM's in decoding.

Another economical method for achieving ratio measurements that can be accomplished easily with a VFC is measuring resistance ratio. This could be done with the previous circuit by using a bridge and differentially amplifying the output, and then measuring the ratio between the supply voltage and the differential amplifier output. This application will achieve highly accurate results, but there is another method that uses only one VFC in the precision mode (see Figure 18). The equation for output frequency of the 4152 is:

$$f_O = \left(\frac{.486}{R_O C_O}\right)\left(\frac{R_S}{R_B}\right) V_{IN}$$

The output frequency is directly dependent on the ratio

$$\frac{R_S}{R_B}$$

The resistor to be trimmed is connected to the R_S position. The reference resistor is connected to the R_B position. V_{IN} is adjusted to -9.67 volts. When the ratio is unity the output frequency will be 10 kHz. The output could be compared to a reference frequency or read on a frequency counter. Note: this application will not work with a 4153 because the R_S resistor is internal and cannot be adjusted.

A similar application is measuring capacitance. By using the same precision mode circuit, we can derive the value of the C_O by making R_S, R_B, R_O and V_{IN} constant. The output frequency is proportional to

$$\frac{1}{C_O}$$

and the period is directly proportional to the capacitor-under-test C_O. If the need is to compare a capacitor with a reference capacitor, or the measure a single capacitor value in high volume, then the output can be compared to a reference frequency. The difference, or beat, frequency may be monitored as an audio signal as well as read with a counter.

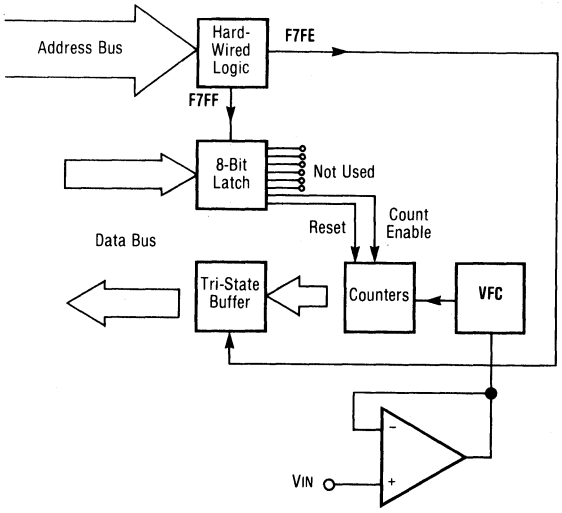


Fig. 19 Block Diagram for Microprocessor DVM

OSI Microprocessor DVM

VFC integrators and A/D converters are very useful in microprocessor controlled systems. Several similar sources of analog data may be multiplexed and then converted with one VFC and counter, or several individually tailored converters may be digitally multiplexed. The sampling period can be derived from the system clock and modified with software to compensate for different scale factors. Offset drift and gain errors can be automatically compensated with an auto-zero approach.

The greatest source of error in VFC converters is scale factor drift. The temperature coefficient of the 4153 is guaranteed at 50ppm/° C with an external reference. Using resistor and capacitor temperature coefficients of 50ppm, the worst case temperature coefficient would be about 150ppm/° C. This would lead to a ±.15% error over a 10° C range. This can be corrected by a careful selection of components, but there is a better approach. By applying a known reference voltage to the VFC, a correction term can be generated to automatically eliminate gain error and offset drift. The correction term can be applied within the program or through a D/A convertor to the VFC. Thermal changes occur slowly in most systems, so the scale factor updating cycle is typically run at a small fraction of the signal conversion rate. In systems requiring very low data rates, program a calibration cycle immediately ahead of the signal conversion cycle.

Figures 19 and 20 show in detail a DVM using a 4153 and an Ohio Scientific C1P microcomputer. The 6502 microprocessor in the C1P controls the counters, and puts the data in memory for display on a CRT.

A 4153 connected for 1 kHz full scale operation clocks two four bit counters, which in turn are buffered into the microprocessor data bus. Control of the buffers and counters is derived from the microprocessor address bus via hard-wired logic and an eight bit latch. Figure 19 shows the block diagram and Figure 20 shows the complete schematic.

The program first clears the display, takes 10 sample readings and averages them, then displays the result. We will look at the program step by step and follow the operation in the diagrams.

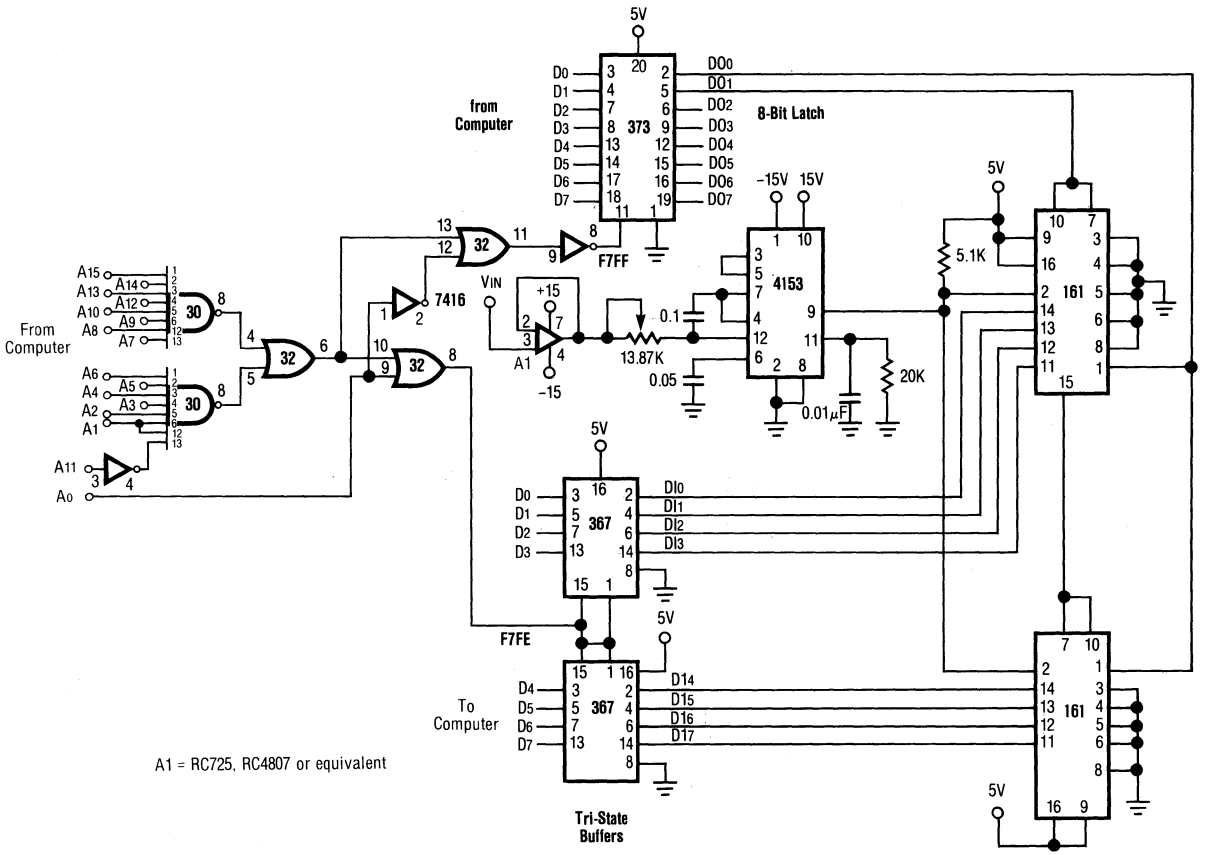


Fig. 20 Complete OSI Microprocessor DVM

```
REM = Remark
10  X=236
20  S=10
30  FOR Y=1 TO 5:PRINT:NEXT
40  A1=0
50  FOR V=1 TO 5
60  POKE 63487,0:REM Clear Counters
70  POKE 63487,255:REM Start to Count
80  FOR T=0 TO X:NEXT
90  POKE 63487,253:REM Stop Count
100 A=PEEK(63486)
110 A=10.004*A/253
120 PRINT A
130 A1=A1+A
140 NEXT V
150 A1=A1/S
160 A1=.01*INT(100*A1)
170 PRINT"READING";A1;"VOLTS"
180 PRINT
190 GOTO 30
```

Figure 21. OSI Program Listing

The first four lines initialize the program, clear the output variables, and erase the display. Line 50 sets up the iterative loop for the averaging routine. Lines 60 through 100 actually take the measurement. The addresses that the hard-wired logic was designed for were selected by checking the memory map for unused locations. Line 60 addresses location F7FF, which latches in the binary number 0 from the data bus. The latch output resets the two binary counters to zero, and keeps them from counting until the next program line. Line 70 again addresses the latch, and the data bus word enables the count to begin. The next two lines are an iterative loop which sets the sample period, which ends when the latch is again addressed. The counters now contain a binary number proportional to the VFC output frequency. Note that there are 6 unused latch outputs which may be used for other purposes.

The program now addresses F7FF, which selects the tri-state buffers and loads the counter outputs onto the data bus. The measured count is converted to an equivalent voltage reading by finding ratio of that count to the full scale count and multiplying it by what has been defined as the full scale input voltage.

$$V_{IN} = \frac{N}{N_{FS}} (V_{FS})$$

Where N = present count, N_{FS} = full scale count, and $V_{FS} = V_{IN}$ for full scale count.

In this application 10.004 volts was applied to the VFC, and the sampling period was adjusted until the counters had counted without going overflow (in this case 253, due to non ideal timing increments).

Example

When 3 volts is applied to the VFC, the counter will count to three tenths of the full scale, or 76. Accuracy to within three digits is obtained by dividing 76 by 253, which equals .30039. Multipling the result by 10.004 will yield an answer of 3.005 volts. When this is combined with the averaging techniques, it will provide three digits of accuracy consistently. This allows for scale factors other than those divisible by ten.

Line 110 provides this computation, and lines 120 through 150 are part of the 10 reading averaging technique. Line 160 truncates the unneeded digits, as the accuracy is limited by the 8-bit data capacity. The last lines display the final averaged result and loop back to the beginning of the program. The value of S set in line 20 determines the number of samples averaged. Line 120 prints the individual voltage readings, and may be deleted after debugging is completed.

Our system was constructed using two separate P.C. boards; one for the interface, the other for the 4153 and counters. The interface can then be used for other purposes. All the IC's in the interface are 54/74 Series TTL, so the interface may be used with any microprocessor with a compatible bus, providing the two address codes are in unused locations.

The 4153 is set up for approximately 1 kHz F.S. operation, but the user can and should experiment with results. The 4153 input is buffered by a voltage follower in order to minimize circuit loading. In order to minimize temperature drift and nonlinearity, good grounding practices, well bypassed supplies, and low temperature coefficient components should be used.

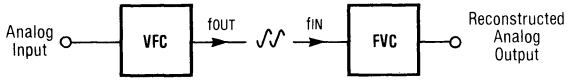


Fig. 22 VFC — FVC Transmission

DATA TRANSMISSION

Telemetry (remote monitoring) is an application that is well suited for converters. Analog information can be transmitted through environments of high electrical noise (such as a manufacturing facility) or over long distances while retaining a high degree of accuracy. While this application could work with conventional A/D and D/A converters transmitting parallel data, or through a parallel to serial converter, a simpler cost effective solution exists. A VFC converts the analog signal directly to serial form, where it is transmitted to a FVC for reconstruction of the analog signal, or is converted directly to digital via a counter and latch.

The open collector output of the VFC can be used directly for twisted pair lengths of several hundred feet. For distances of several thousand feet a line driver and receiver can be used. Longer distances will require radio or telephone FSK transmission.

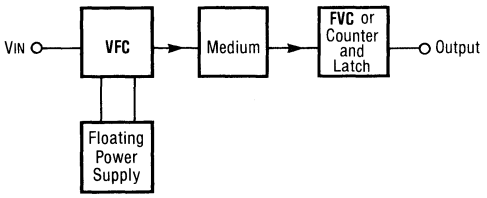


Fig. 23 VFC Isolation

VFC Isolation (Figure 23)

Some applications require that the transmitter be electrically isolated from the receiver due to high voltages existing between them. The classical solution is to use an isolation amplifier and an A/D converter. For high accuracy (12 bit) the cost of these becomes prohibitive when compared to VFC isolation schemes.

The VFC is powered by a floating power supply and transmits a pulse train to the medium. The medium is usually an optoisolator (LED and photo transistor in one package), but it could be a transformer or even a speaker and microphone. The medium can also serve as the transmission line, i.e., an optical fiber, infrared, or radio transmitter. The pulses from the medium can be reconverted with an F to V converter or used for direct digital output.

Figure 24 shows a circuit which uses an LED and a phototransistor to provide electrical isolation between the transducer and the rest of the system. This is generally used to protect microcomputers from transient voltages and grounding problems, or where a transducer has a high voltage on it.

The optoisolator is pulsed directly by the VFC at the relatively low level of 10mA, conserving power. One stage of gain is added to the receiving side. the light emitted by the LED provides base current to turn on the phototransistor, turning off the output transistor and giving a logic High out. This circuit has a wide bandwidth and will drive at least 6 standard TTL loads.

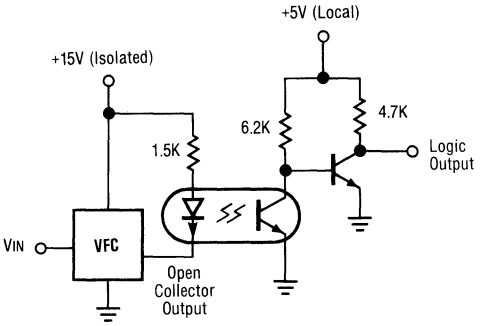


Fig. 24 VFC Optoisolator

Fiberoptic Transmitter

Figure 25 shows a typical scheme for isolation and transmission using a precision VFC and fiberoptics.

Most fiberoptic transmitters require currents in excess of the output drive capability of Raytheon VFC's. Since the current must be a pulse of short duration and the VFC supplies negative going output pulses, the output is inverted with a PNP transistor, Q1. This transistor must be selected for a current capability equal to the requirements of the transmitter. Pulses of light are sent through the fiber to be received by the photodiode. The light received by the photodiode is converted into a small current. This current is amplified by A1 and applied to the comparator, A2. This hysteresis comparator has an adjustable reference to set the threshold for the logic output. The circuit as shown has a bandwidth sufficient to handle 20 kHz signals.

A common requirement of communications is the transmission and decoding of binary data as two or more discrete frequencies. This frequency shift keying function is easily implemented using a VFC, 2 transistors, and a flip flop. Two circuits are shown, one using a 4153, and the other a 4151 or 4152.

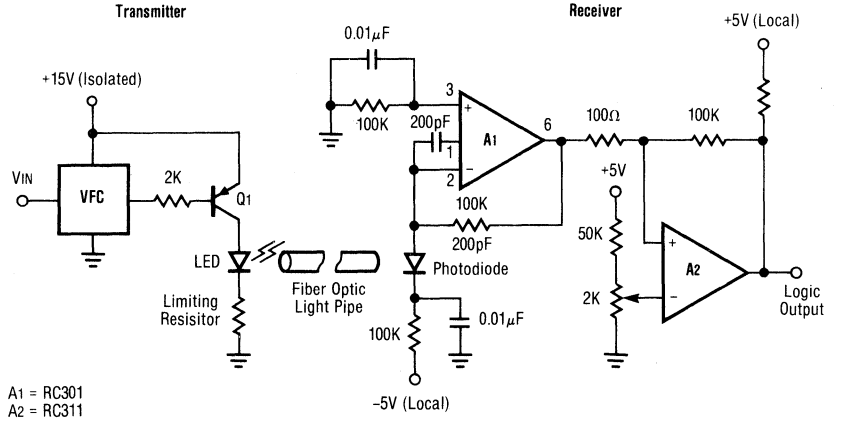


Fig. 25 Fiberoptic Transmission

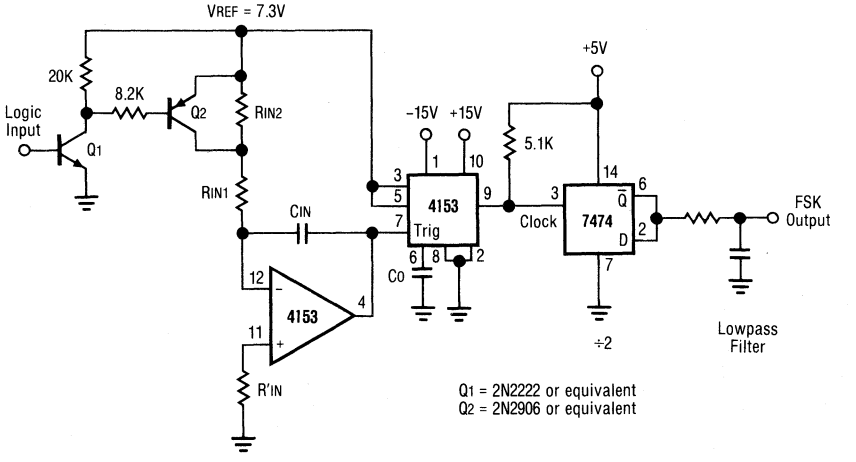


Fig. 26 4153 FSK Modulator

4153 FSK Modulator (Figure 26)

When the logic input goes High, Q1 is turned on, which turns Q2 on. The input current is

$$\frac{V_{REF} - .2V}{R_{IN1}}$$

The one shot frequency will increase to balance this input current. If the logic input goes Low, Q2 turns off. The integrator input current is

$$\frac{V_{REF}}{R_{IN1} + R_{IN2}}$$

so the one shot frequency, and therefore the logic output frequency decreases to balance the loop. The output pulse frequency is applied to the toggle, which divides by two, and provides an output square wave of half the frequency of the VFC. This is applied to a lowpass filter to round the edges for transmission over public telephone lines. Figure 27 is a table of component values for the two ranges of the Bell 103 standard.

Mark = 1070Hz	Mark = 2025Hz
Space = 1270Hz	Space = 2225Hz
R_{IN1} = 28.3K	R_{IN1} = 16.1K
R_{IN2} = 6.0K	R_{IN2} = 1.6K
C_O = 0.0068μF	C_O = 0.0068μF
C_{IN} = 0.1μF	C_{IN} = 0.1μF

Fig. 27 4153 FSK Component Values for 300 Baud Bell 103 Standard

4151/2 FSK Modulator

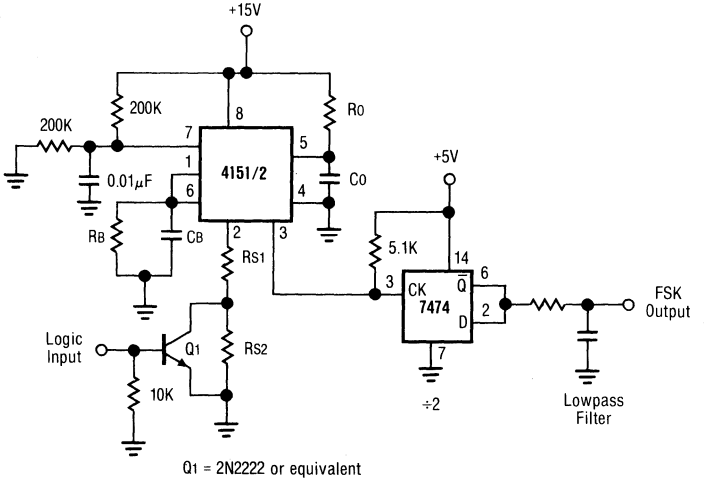
Figure 28 shows a simple FSK modulator using a 4152. When the logic input goes high, Q1 turns on and shorts out R_{S2}, thus changing the scale factor. Overall frequency trim may be changed by trimming R_{IN} or R_B, and relative trim by adjusting R_{S2}. F_O is equal to

$$\frac{(R_S)\ (V_{CC})}{2.53\ R_O C_O R_B}$$

An inverter on the input may be necessary to keep your system's logic polarity correct, as the output frequency decreases with a logic High input. Components for the filter must be selected with the bandwidth and response time limitations of the medium in mind.

Mark = 1070Hz	Mark = 2025Hz
Space = 1270Hz	Space = 2225Hz
R_O = 6.8K	R_O = 6.8K
C_O = 0.025μF	C_O = 0.025μF
R_B = 100K	R_B = 100K
C_B = 4.7μF	C_B = 4.7μF
R_{S1} = 12.3K	R_{S1} = 23.2K
R_{S2} = 2.3K	R_{S2} = 2.3K

Fig. 29 4151/2 FSK Component Values for 300 Baud Bell 103 Standard



Q1 = 2N2222 or equivalent

Fig. 28 FSK Modulator Using 4151/2

Application Notes

Digital Frequency Encoding

Generation of more complex encoding, such as an encoder providing 10 linearly separated frequencies, is easy with an extension of the previous circuits or with the help of a D/A converter.

Figure 30 shows how a D/A can be connected to a VFC. The binary input code is converted to a voltage by the D/A converter, and then applied to the VFC. The VFC's output is then divided by two by the toggle in order to get a square wave output. Figure 21 shows a digitally programmable clock generator using a 4153.

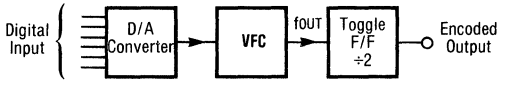


Fig. 30 Digitally Controlled Frequency Generator

This circuit provides a 100 Hz to 9.9 kHz square wave output programmed by thumbwheel switches or by an 8-bit BCD coded binary input word. The output changes in 100 Hz steps - one step for each least significant digit change. The DAC-20 is a 2 digit BCD D/A converter which provides a 0 to 1mA current output. The reference voltage for the D/A is provided by the 4153. A1 converts the D/A's current output to a 0 to 9.9V signal applied to the 4153 VFC. Scale factor for the VFC is 2 kHz/volt, which is then divided by two by the 7474 latch (connected as a toggle). This gives a square wave output of 100 Hz to 9.9 kHz. Scale factor of the VFC may be adjusted to give the desired range, up to a 100 kHz square wave output. To calibrate, set the D/A inputs to maximum (1001 1001), and trim the 5K pot until output is 9.9 kHz. Then set the inputs to minimum (0000 0001) and adjust the offset (10K pot) until the output reads 100 Hz. The 4153's linearity ensures that all other settings are in calibration. Other types of D/A converters may be used, as well as different frequency scalings and output signal conditioning.

Bipolar Telemetry Scheme

Figure 32 shows a complete transceiver for serial transmission of bipolar analog signals over a twisted pair (or any other form of transmission). It overcomes the usual limitations on bipolar serial transmission by encoding the pulse output. Negative input voltages are transmitted as a negative going pulse train and positive voltages as a positive going pulse train. This information is decoded into a frequency output proportional to the magnitude of the input, and a sign output dependent on the polarity of the input.

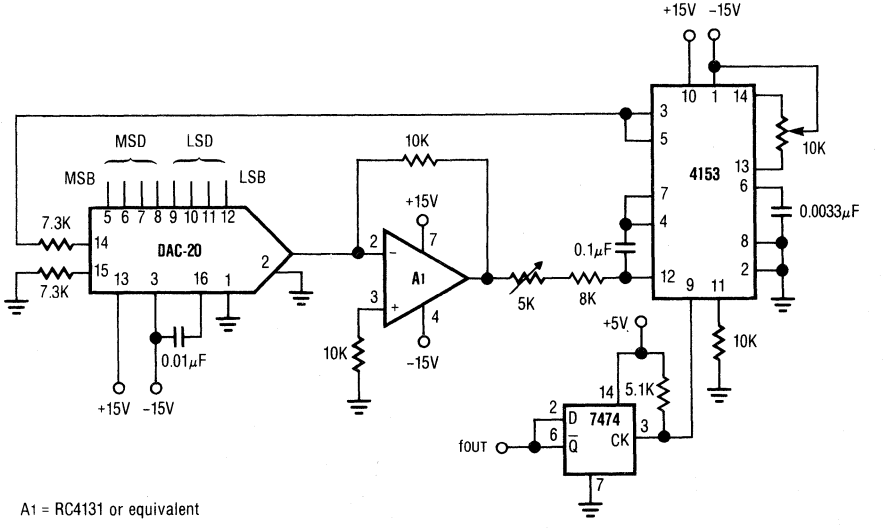


Fig. 31 BCD Input Clock Generator

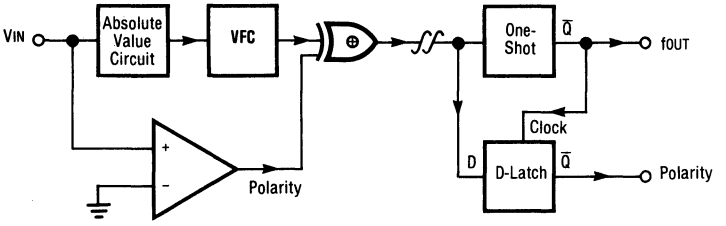


Fig. 32 Bipolar Telemetry Scheme

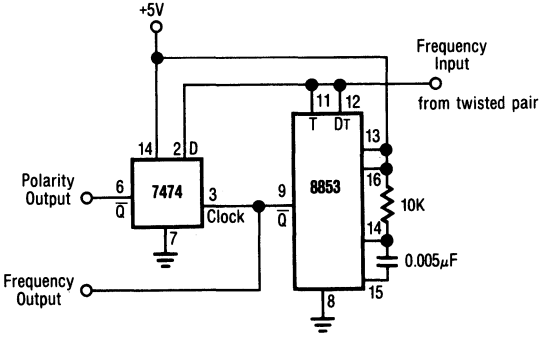


Fig. 33 Bipolar Telemetry Receiver

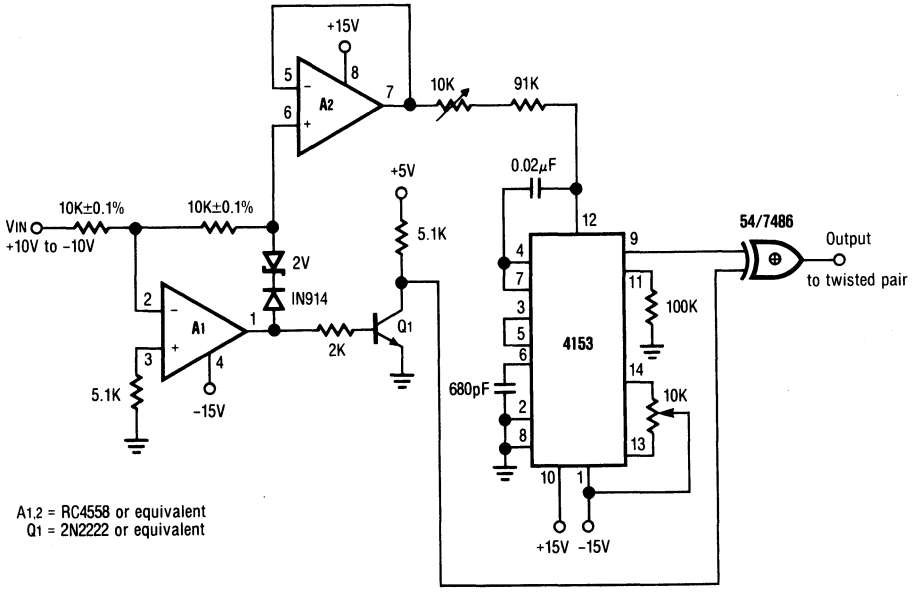


Fig. 34 Bipolar Telemetry Transmitter

The absolute value circuit applies a voltage proportional to the magnitude of the input to the VFC. The frequency output of the VFC is encoded with the polarity output of the comparator, giving a coded signal which is transmitted to the decoder.

The absolute value circuit provides a positive voltage equal to the magnitude of the input voltage.This buffered output is applied to the VFC. The VFC generates 10 μS wide negative going pulses with a scale factor of 1 kHz/volt. Full scale input is therefore 20 volts peak to peak. The transistor provides a logic output dependent on the polarity of V_{IN} (See the absolute value circuit in the appendix on signal conditioning). This polarity signal is used to encode the frequency output of the VFC in a TTL exclusive OR gate. Positive going pulses are generated from positive inputs, and negative going pulses for negative inputs.

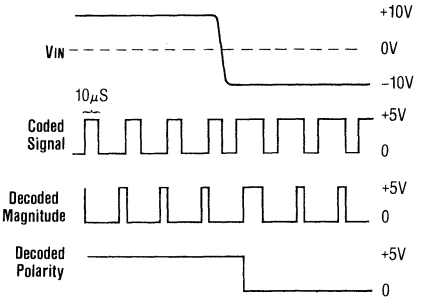


Fig. 35 Bipolar Telemetry Waveforms

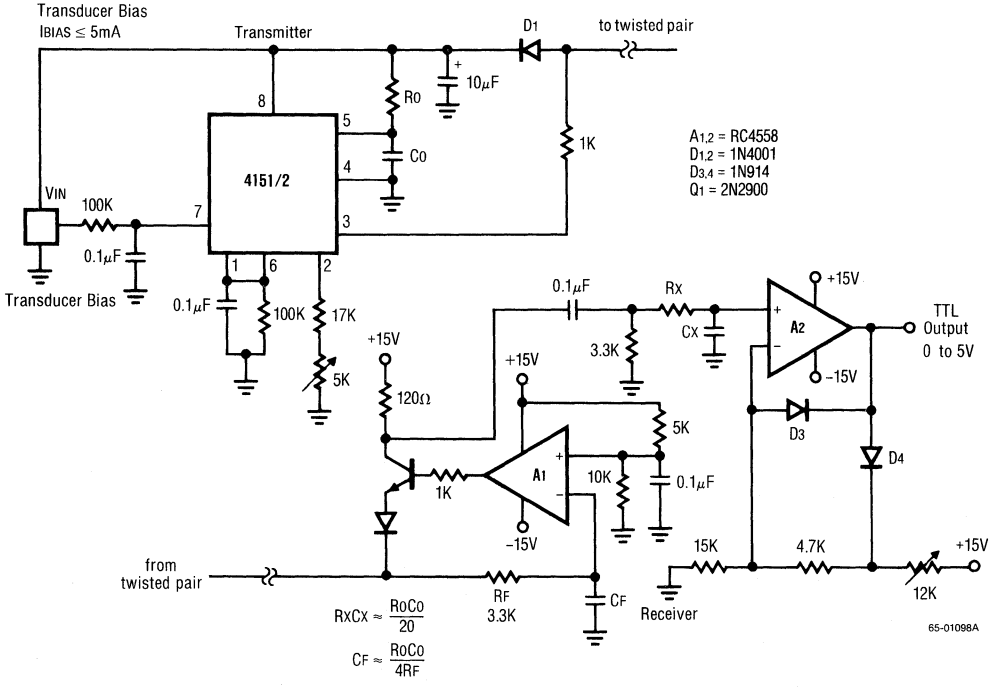


Fig. 36 Two Wire Transmission System

The coded pulse information is transmitted and applied to the D input of the 7474 latch, and to the two trigger inputs of the dual-edge retriggerable one shot (8853). For the components shown, the one shot generates a 25 μS wide negative going pulse for each 10μS input pulse. It will trigger for negative going pulses or positive going pulses on the last edge encountered, thus producing a 25μS wide pulse train equal in frequency to the data (See Figure 35). The rising edge of these pulses clock the D-latch, and the information on the D input will be latched in. If the pulses are negative going, the clock will rise when the D input is High, latching the Q output Low. If the pulses are positive going, the clock will rise when the D input is Low, latching the Q output High. The latch output now corresponds to the polarity of the information transmitted. The values given are not absolutes, and timing and scale factor may be adjusted to your needs.

Two-Wire Transmitter

Figure 36 shows a complete true two-wire transmission system. The same wires that carry the data signal also supply power to the VFC, eliminating batteries or isolated power supplies at the transducer. The circuit as shown uses the 4151 single supply configuration, delivering ≈ 1% accuracy. Greater accuracy may be obtained by adding a single supply op amp for precision mode. The components shown give 0 to 10 kHz operation.

The output of the 4151/2 pulls current pulses from the transmission line, which are detected and output as a TTL signal by the receiver. The blocking diode D1 and 10μF capacitor filter the supply to the VFC and absorb line relections of the transmitted data. Bias voltage for the transducer can be provided by the transmitter supply if the current requirement is less than 5 mA.

Transistor Q1 provides two functions: it acts as a series pass transistor to regulate the transmitter supply, and it acts as a common-base amplifier for the data pulses. The current pulses create a voltage drop across the 120Ω resistor, which is capacitively coupled into a filter and comparator. The comparator is connected so that the output swings from 0V to +5V (TTL logic). C_FR_F and C_XR_X provide noise filtering to reject electromagnetic interference from motors and power lines. C_FR_F controls the response time of the power regulator (A1 and Q1), and C_XR_X provide a lowpass filter for the output amplifier. D2 protects Q1 from transient voltages on the transmission line. Typical values for a 75μS pulse width are:

$C_F = .005\mu F$
$R_X = 1K\Omega$
$C_X = .001\mu F$

Tape Recording

Transducer data may be stored on magnetic tape with a VFC. An application of this might be the taking of data at a remote site with only battery operated equipment available, or file storage for later reference. The data may be retrieved for use in digital format, or reconverted to analog for chart recorder display.

Some signal conditioning and restrictions must be observed when recording data. The frequency response of the deck will limit the dynamic range of the analog data. Most recorders will not accept pulse trains of sharp square waves because of NAB compensation. Accuracy of the system will be limited by motor speed variations (wow and flutter) of the deck. Good battery operated cassette recorders will introduce about 1% to 3% inaccuracy. If battery operation is necessary, be sure the batteries are well charged, or the tape speed may vary as they discharge. Many cassette decks have a 200-300 Hz AC component in the motor speed. This is a function of the motor poles and belt ratios. If higher accuracy is needed, there are a few expensive high quality portable recorders on the market that will give 0.5 percent error.

Figure 37 shows a system for recording the data on tape. The VFC's pulse output is fed to a toggle flip flop, giving a square wave of half the frequency out. This signal is applied to a lowpass filter to round the square wave,

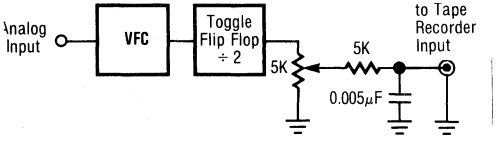


Fig. 37 Tape Recorder Interface

because sharp rise-times will cause the NAB compensation to overload the tape. Both high and low frequency response limit the dynamic range of the input, so it may be necessary to add a DC offset to the transducer to achieve a frequency offset. Excellent results in most applications will be obtained by limiting the recorded signal to a 1 to 5 kHz bandwidth.

The signal may be retrieved from the tape by capacitive coupling of the output to a ground referenced comparator. This will give a square wave output which may be processed digitally or applied to an FVC for analog reconstruction. Remember that the FVC must have twice the scale factor of the VFC for 1-to-1 reproduction.

MOTOR SPEED CONTROLS

Raytheon converters are extremely versatile in motor speed control circuits. There are two general forms for this application; one using an FVC providing an error signal dependent on variations in motor speed, and the form which uses a VFC to provide a pulse frequency to gate a power regulator. Figure 38 shows the FVC feedback system.

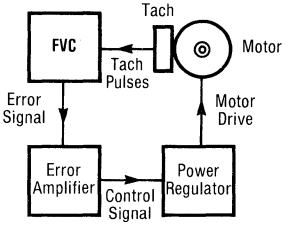


Fig. 38 FVC Provides Error Signal

In this form, tachometer pulses are converted into a voltage dependent on motor speed. This signal is amplified with respect to some reference voltage, to provide a control signal which regulates the power supplied to the load. If the motor slows down, the DC voltage from the FVC decreases, which causes the control signal to increase, which makes the regulator deliver more power, causing the motor to speed up. This general form can be used with varied types of motor, tach, amplifier, and regulator systems. We will discuss a system which uses an optical tachometer, a comparator providing pulse width modulation, and switching transistor providing pulsed DC power to a DC motor. This concept will work with all types of AC tachometers if certain design rules are met. The error amplifier might conceivably be a power op amp with the output driving the motor directly. The power regulator might be a series pass transistor, a switching transistor, a triac, or relay, etc. The reference input to the error amplifier can be used to vary the motor speed or act as a trim for precise applications.

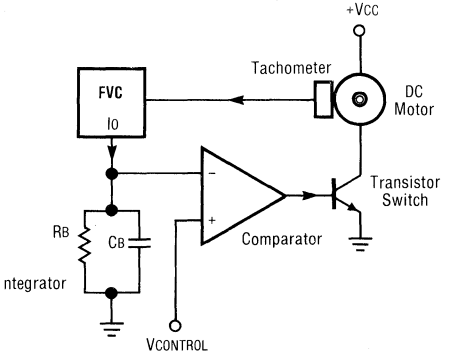


Fig. 39 FVC Provides Ramp for PWM

Pulse Width Modulation Speed Control

Figure 39 uses the general form of Figure 38 to implement a pulse width modulation scheme for switching control of a DC motor. This circuit gives excellent rejection of variations in load, power supply voltage, and temperature. The tachometer sends a pulse train to the FVC, which produces a ramp signal whose DC level is proportional to motor speed. This ramp is compared to a control input to generate a pulse width modulated signal to drive the transistor switch.

The values of the components used are highly dependent on the tachometer, the motor, and its application. For smooth operation, the tach frequency must be much greater than the motor RPM's (approximately 10 times) to ensure that the load friction/inertia product does not slow the motor between tach pulses. If necessary, a frequency multiplier may be used to make the apparent ratio of tach frequency to motor revolutions higher. The tach pulses must be within the input voltage constraints for the FVC circuit (See appendix on FVC Signal Conditioning).

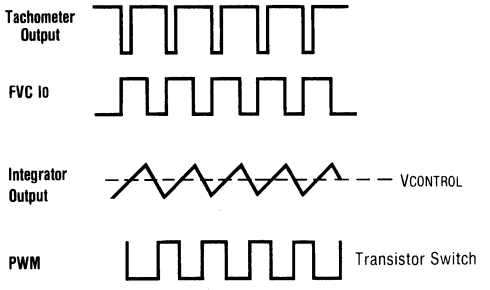


Fig. 40 Pulse Width Modulation Waveforms

The FVC output current pulses of amplitude Io and width T_P are integrated by the parallel RC circuit R_BC_B. The time constant R_BC_B is chosen such that the input to the comparator is a triangle wave. This triangle must have a peak-to-peak amplitude large enough to provide good pulse width modulation, but also have a long enough time constant to provide an average voltage proportional to motor speed. The peak-to-peak voltage is given approximately as:

$$V_{peak\text{-}peak} = V_{high} - V_{low} \approx \frac{I_O}{C_B} T_P \left(1 - \frac{T_P}{T}\right)$$

where: T_P = One Shot Time ($1.1\ R_OC_O$)

and: $T = \frac{1}{\text{Tach Frequency}}$

The average voltage is given as

$$V_{COMP}\ (Avg.) = R_BI_O \left(\frac{T_P}{T}\right)$$

Some experimenting will be necessary to optimize your motor - tachometer combination.

The speed control input (Vcontrol) is compared to the filtered FVC output, which contains a triangular ripple component and a DC component proportional to motor speed. Variations in motor demands or supply or a change in the control input will cause the output of the comparator to vary in duty cycle (Pulse width modulation). A speeding up of the motor will result in less on time of the power transistor, delivering less energy per unit time, thus slowing the motor back down. Component values are generally chosen for approximately 30 to 50 percent duty cycle under normal loading. The comparator must have high gain for positive switching and must be able to drive the output transistor into saturation. For larger motors, add more output transistors (in parallel) to accommodate motor requirements.

Open Loop Switching Control

The preceding application uses an FVC to provide an error signal dependent on motor speed to provide feedback for precise speed control. Perhaps your application does not require precise control, but needs a switching drive to increase efficiency. This brings us to the second type of converter motor speed application, using a VFC to provide a pulse frequency to gate power regulator (See Figure 41).

The VFC provides a pulse train whose frequency is dependent on the speed control voltage. This pulse train is used to switch a power transistor, providing pulsed DC power to drive the motor. This increases the motor's efficiency and allows smoother operation at lower RPM's than a steady DC supply would. This AC supply has a problem of heating the motor if used for extended periods.

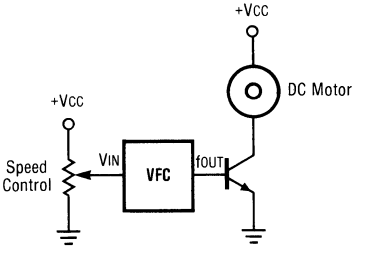


Fig. 41 VFC Provides Open Loop Switching Control

Series - Pass Summing Controller

Figure 42 combines the low speed smoothness of Figure 41 with the advantages of DC power (low heating). The summing amplifier output contains an AC component produced by the VFC, and a DC component proportional to the speed control voltage. This voltage, minus the base-emitter voltage of the pass transistor, appears across the motor. The inputs to the summing amplifier are scaled such that the pulse train is eliminated when the speed control voltage reaches approximately 50

percent of the full scale value. The summing amplifier must be in a non-inverting configuration.

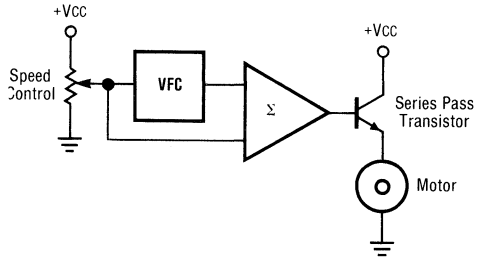


Fig. 42 Series Pass Summing Controller

Phase Locked Loop Speed Control

Figure 43 shows another pulse width modulation scheme which has the advantages of increased gain at high RPM's, and that the tach frequency equals the VFC output frequency.

The VFC provides two functions in the circuit; it converts the speed control voltage into a reference frequency with which to compare the tachometer frequency, and it also provides a triangle waveform from the integrator to be used to pulse width modulate the output.

The output frequency of the VFC is compared to the tachometer frequency in a digital exclusive-OR phase comparator. For proper phase comparison to take place, the VFC output and the tachometer output must both have 50 percent duty cycle when locked. The output of the phase comparator is fed into a lowpass filter to give a varying DC voltage error signal.

This error signal is sent to a comparator which functions much like the comparator in the circuit of Figure 39. It provides pulse width modulation at the output, because the other input is the triangle waveform from the integrator of the VFC. The lowpass filter must have a longer time constant than the integrator of the VFC in order to provide good pulse width modulation.

Since the triangle waveform is equal in frequency to the VFC output, the VFC frequency is not only the same as the tach frequency, but also the drive pulse rate. Therefore, to ensure smooth operation, the tach frequency must be much greater than the motor RPM rate.

The inputs to the phase comparator will vary in angle from 0 degrees to 180 degrees. At 0 degrees, the lowpass filter output will be 0 volts. At 180 degrees, the output will be maximum. To provide a proper error signal, the PWM must be scaled such that the system will balance when the phase angle is 90 degrees.

This type of phase comparator may lock onto harmonics of the tach output. The range of frequencies over which it will lock greatly depends on the relationship of the lowpass filter and time constants of the motor drive. Experimentation with the lowpass filter characteristics, the tach pulse to motor RPM ratio, and scaling of the PWM inputs will be necessary to optimize your system.

In the locked condition, if the motor sees a greater load and slows, the filter output voltage increases and provides more on time to the output transistor to speed it back up. The peak amplitude of the triangle waveform decreases

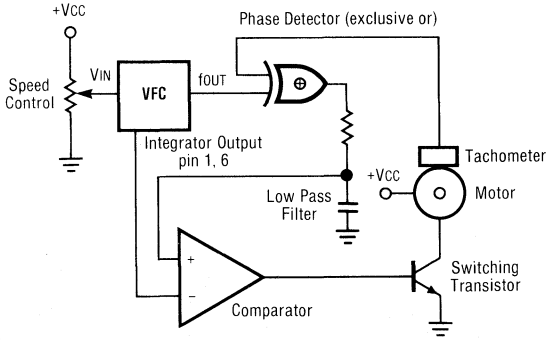


Fig. 43 Phase Locked Loop Speed Control

as the VFC frequency increases. For a 50-to-1 frequency change the peak-to-peak triangle voltage is 3.8 times smaller. This reduction of input voltage to the comparator acts as an increase in loop gain at high frequencies. This 11.6 dB effective gain increase at the high end compensates for the gain reduction at high motor speeds inherent in pulse width modulated DC motor drives.

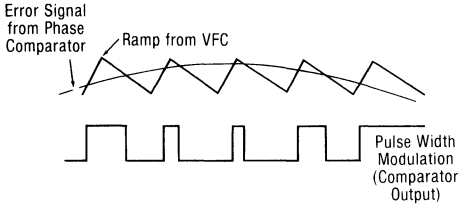


Fig. 44 Phase Locked Loop PWM Waveforms

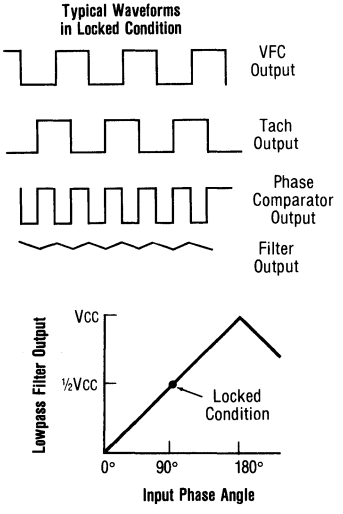


Fig. 45 Phase Comparator Relationships

MISCELLANEOUS APPLICATIONS

Converters are not limited to the standard uses of A/D conversion and telemetry. The 4153, for example, has an op amp, a voltage reference, a comparator and switched current source, and an open collector output, all contained internally. These functions can be combined to create circuits other than just converters. An example of this is seen in Figure 46, where the precise charge dispensing characteristics of a 4152 VFC are used to control a chemical reaction.

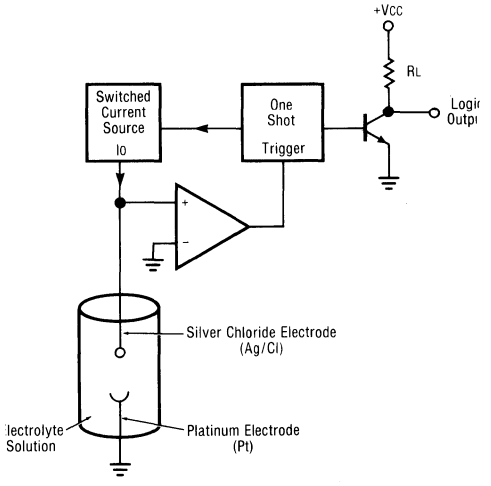


Fig. 46 Chloride Titrator

Titrator

The VFC's current pulses generate Ag^+ ions, which precipitate Cl-ions from the electrolyte solution. If there are Cl-ions in the soultion, the Ag electrode is polarized positive. This switches the ground referenced comparator, which fires the one shot, switches the logic output, and dumps a charge from the Ag electrode into the solution. The charge causes Cl-ions to be absorbed by the Ag electrode, so the one shot keeps firing until all Cl-ions are gone. When that happens, the Ag electrode is polarized negative, below the comparator threshold, and the one shot stops firing. The number of charges dispensed, which equals the number of logic output pulses, is a measure of how may Cl-ions were in the solution.

$$\mu gCl = \frac{(N)\ (Io)\ (1.1\ RoCo)\ (35.3\mu g/\mu Mole)}{.96487 \times 10^{-6}\ Coulombs/\mu Mole}$$

Where N = the number of charges dispensed and $.96487 \times 10^{-6}$coulombs equal the charge dispensed with each pulse. Q = (I) (T) I in amps T in seconds. Titration of a standard solution of Cl- will be necessary to calibrate the measurements.

Application Notes

VCO Stabilization

Low cost VCO's do not have good temperature characteristics or linearity. By adding a low cost F-to-V converter in a feedback loop around the VCO its performance is greatly enhanced, giving linearity of .01 percent and low temperature coefficient, without resorting to heating elements or expensive digital synthesis.

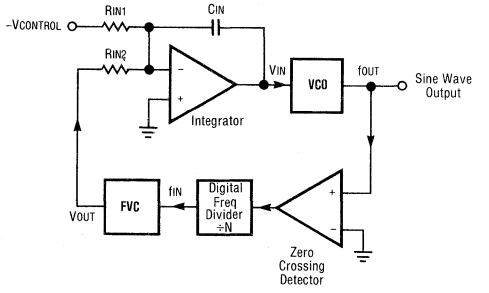


Fig. 47 Voltage Controlled Oscillator Stabilization

The VCO output is a high frequency sine wave. This is squared in a comparator and the frequency is digitally divided down to a frequency usable by the FVC. Some signal conditioning will be necessary at the FVC input (see appendix). The FVC gives an error signal which is applied to a summing integrator. The FVC output is balanced with the V control signal to produce the voltage control input to the VCO. Thus, if the VCO drifts, the FVC output voltage changes, which causes the integrator output to give an error signal correcting the VCO. Low temperature coeffiecient components should be used in the FVC and integrator, such as a low drift op amp and polystyrene capacitors.

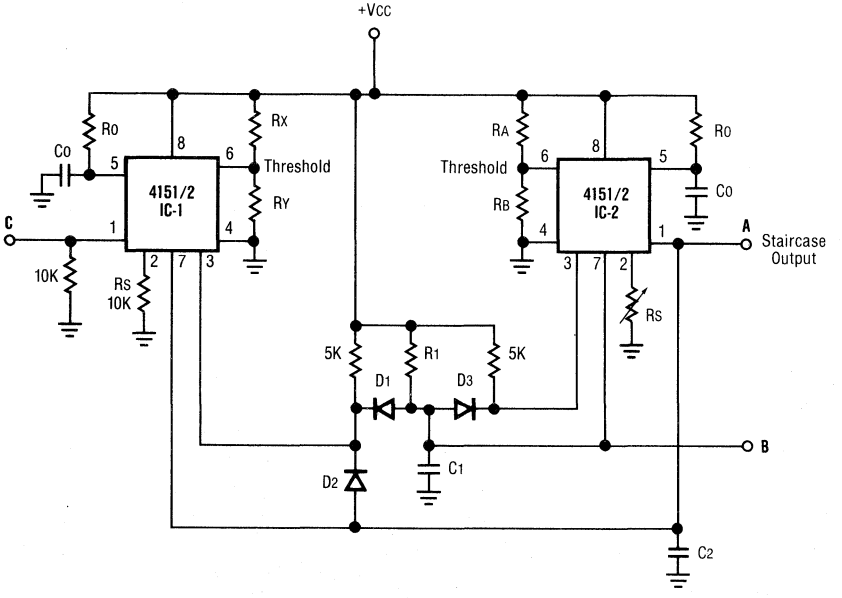
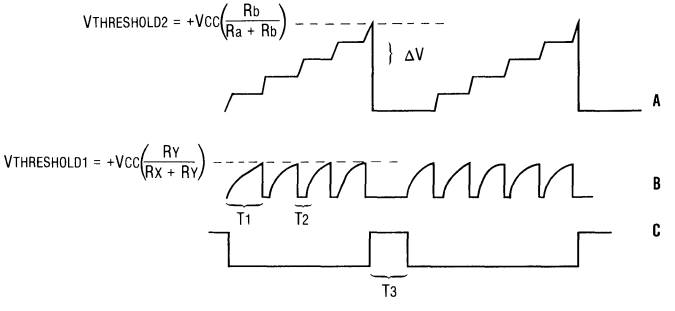


Fig. 48 Staircase Generator

Staircase Generator

Figure 48 illustrates the VFC's versatility, as it uses the functional building blocks to create a circuit not related to conversion. It uses the one shot and comparator of IC-1 to provide a timing function similar to a 555, and the switched current source of IC-2 to charge a capacitor.

To understand the circuit, consider what happens when power is first applied. Both C1 and C2 are discharged, and C1 begins to charge through R1. The voltage on C1 increases until it reaches IC-1's threshold, set by R_A and R_B. When the threshold is exceeded, the one shot fires, bringing pin 3 Low and delivering a discrete amount of charge to C2. C2's voltage rises by an amount proportional to the charge, and the logic output discharges C1 through D3. After the one shot period of IC1, the logic output (pin 3) goes High, allowing C1 to charge again. The cycle repeats itself until enough charges have been delivered to C2 to bring the voltage on C2 above the comparator threshold of IC-1. This threshold is set by R_X and R_Y; when it has been exceeded, IC-1's one shot fires, bringing its logic output Low, and discharging both C1 and C2 through D1 and D2. After the one shot period of IC-1, its logic output goes High, C1 again begins charging through R1, and a greater cycle repeats itself. The basic timing function is provided by the charge and discharge of C1. This timing sets the interval between chargings of C2. C2, not having a discharge path, increases its voltage in steps until the threshold is reached. A low input current buffer on the output may be necessary before utilizing the circuit.



$T_1 = R_1C_1 \ln\left(1 - \frac{V_{TH} - 0.7}{V_{CC}}\right)$ where $V_{TH} = V_{CC}\frac{R_B}{R_A + R_B}$

$T_2 = 1.1R_OC_O$ of IC-1
$T_3 = 1.1R_OC_O$ of IC-2

$\Delta V = \frac{(I_{O1})(1.1R_OC_O)}{C_2}$

see 4151/2 Data Sheet for Design Equations

Fig. 49 Staircase Generator Waveforms

Appendix
Signal Conditioning

Transducer Bridge

Low level transducer signals may be integrated and converted directly by the period measurement technique (see Figure 14).

Another technique is to amplify the signal with a low drift instrumentation amplifier before conversion. Transducers with bridge outputs lend themselves to this, with a differential output, allowing amplification with high noise rejection. Bridges require a reference (excitation) voltage to generate the differential output, readily supplied by the 7.3 volt reference output of the 4153. Figure 50 shows a typical transducer interface circuit using a 4153. A1 and Q1 buffer the reference output of the 4153 to supply a well regulated excitation voltage to te bridge. Changes in the value of the transducer (x) cause changes in the differential output voltage.

$$V_{DIFF} = \frac{V_{REF}}{2} - \frac{R}{X+R}(V_{REF})$$

This differential output is amplified by the instrumentation amplifier A2 and applied to the input of the VFC. Thus the VFC output frequency is proportional to the value of the transducer resistance. This circuit is only an illustrative example, as bridge configurations could be unipolar or bipolar, linear or nonlinear.

Absolute Value Circuit

Figure 51 is a schematic for an absolute value circuit for bipolar inputs.

When V_{IN} is positive the op amp is effectively out of the circuit; when its output goes Low the 1N914 turns off, and the signal passes without attenation to the VFC input. When V_{IN} is negative, the op amp inverts the signal (the 1N914 is biased through the zener), and the VFC receives a positive input. The zener diode ensures that the polarity indicating transistor is turned on. The polarity output may be used to drive the sign bit of the interface or display.

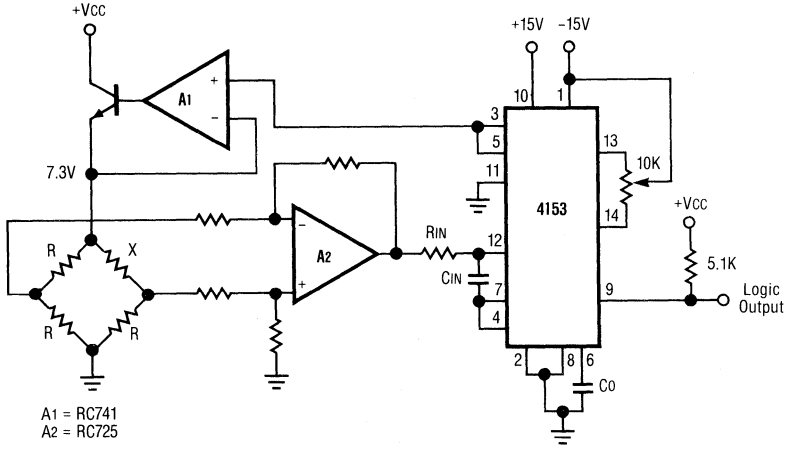


Fig. 50 Transducer Bridge

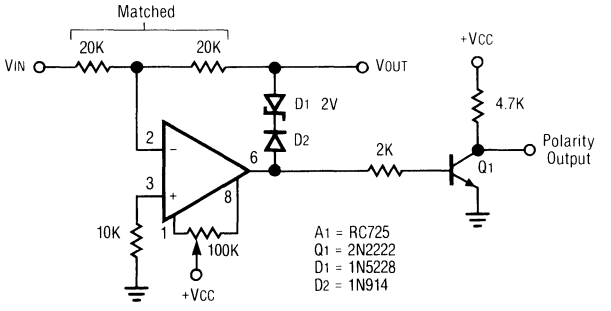


Fig. 51 Absolute Value Circuit

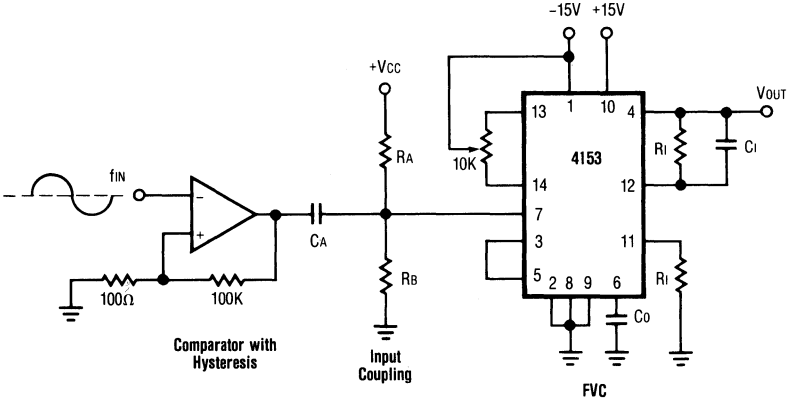


Fig. 52 FVC Input Conditioning

FVC Signal Conditioning

Frequency-to-voltage converters require the input waveform to have a sharp edge, and that the signal actually reaching the trigger input have less pulse width than the period of the one shot. This is to prevent the one shot from being retriggered, which would cause an erratic, nonlinear output. If the input is a sine wave, for instance, a Schmitt trigger or comparator should be used to square up the waveform before AC coupling to the FVC (see Figure 52).

The time constant $C_A(R_A//R_B)$ should be kept less than 15μS in most applications. For applications with a square wave input, the one shot time should be kept less that the minimum period of the square wave. This prevents the input from interfering with the timing waveform and affecting linearity. By keeping C_O small this problem can be avoided (see Figure 53).

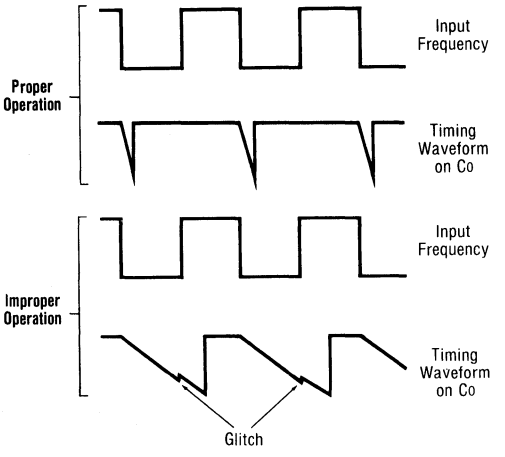


Fig. 53 FVC Timing Waveforms

Other Application Ideas

Here are some more application ideas:

- Audio Logic Level Indicator
- Automotive Cruise Control
- Frequency-to-Voltage →Gain→ Voltage-to-Frequency
- Pulse Width Modulators
- Pulse Frequency Modulated Audio Transmission
- FSK Demodulators
- Signal Conversion
  - Current-to-frequency
  - Temperature-to-frequency
  - Pressure-to-frequency
  - Frequency-to-current
  - Capacitance-to-frequency
  - Light-to-frequency
- Variometers
- Discriminators
- Tachometers and Flow Meters
- Multimeters and Panel Meters
- Linear Potentiometer Positioners

An Introduction to the Z Transform and its Derivation

INTRODUCTION TO THE Z TRANSFORM AND ITS DERIVATION

1. INTRODUCTION

Recent advances in the field of electronic computing machinery are due largely to the great strides made in IC technology. Specifically, improved speed and higher IC density have made practical the efficient digitization and subsequent processing of real world data. More complex processing with more accurate results can be performed with digital than with present analog data equipment. With scientific advancement in fields such as medicine and geophysics the need for complicated processing algorithms and large data storage capability points most singularly in favor of the digital approach.

The recognized potential of the digital computer as a signal processing tool has spawned rebirth in the field of discrete mathematics. The Z transform has proven itself to be a useful constituent in this field, and it is the intent of this paper to introduce the Z transform as a means of analysis and synthesis of purely discrete time and mixed (analog-digital) systems. Hopefully, those familiar with Z transform theory will find the presentation unique and clear; and newcomers to the field of DSP, especially those of an analog persuasion, will be spared the frustration of breaking into this new field which usually bears little resemblance to its analog counterpart. This is not to be an exhaustive treatise on digital processing mathematics but more of an introduction to the subject. It is designed especially to clarify or define some of the crucial points which the author finds are omitted from most introductory treatments of the subject. This attitude will hopefully give the reader a good intuitive foundation on which to build.

2. MOTIVATION FOR LAPLACE TRANSFORM

One frustrating aspect of an engineering education is that often the student is expected to accept a formula or concept at face value, use it, and build on it without knowing its origin. Some may reply, "Who cares?" and rejoice at the prospect of having to learn less material. On the other hand, the more inspired find it maddening to open to page 1 of their digital systems text and find the opening statement: "It is intuitively obvious to the casual observer that:

$$\sum_{n=0}^{\infty} h_n^2 = \frac{1}{2\pi j} \oint_{|Z|=1} H(Z)\, H\left(\frac{1}{Z}\right) Z^{-1}\, dZ \text{ "}$$

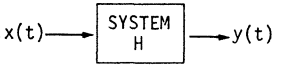
Clearly, this sort of thing may propagate and cause great confusion or misuse of the theory. For our purpose (that is, understanding discrete time systems) it is important that the fundamental theorems which apply to any linear system are well understood. A good place to start is with a derivation of the LaPlace transform and the motivation behind it. This will lay the groundwork for the Z transform discussion which follows:

All continuous realizable linear time invariant systems can be described in most general terms by the nth order differential equation 1.

$$a_n \frac{d^n y}{dt^n} + a_{n-1} \frac{d^{n-1} y}{dt^{n-1}} + \ldots a_1 \frac{dy}{dt} + a_0 y \qquad (1)$$

$$= b_m \frac{d^m u}{dt^m} + \ldots b_1 \frac{du}{dt} + b_0 u = x(t)$$

u and y are both functions of time and the a's and b's are constant for the time invariant case. From a system standpoint, y is the system output and the u's are the input terms. To simplify matters let x equal the sum of all the input terms are shown in equation 1.



For any given input x(t), a unique system output y(t) will result. Generally the output will be a complicated sum of individual time functions (not necessarily resembling input x). We arrive at the response via the tedious time domain solution of the differential equation for the given input x(t).

One input function to a linear system yields a conceptually trivial solution to the differential equation and hence simplifies the system description. The complex exponential time function e^{st} (where $s = \sigma + j\omega$) may be differentiated any number of times without destroying its original functional form.

That is,

$$\frac{de^{st}}{dt} = se^{st}$$

$$\vdots$$

$$\frac{d^n e^{st}}{dt^n} = s^n e^{st}$$

Successive differentiations yield the original time function e^{st} multiplied by a complex constant (e.g. s^n). For the present we will not be concerned with the meaning of e^{st} in a practical sense but note that is has a remarkable property particularly suited to differentiation. Returning to equation (1), we might logically question, "with the output of a system being e^{st} what must the input have been?"

Letting $y(t) = e^{st}$ (the output), differentiating and accumulating all the terms one finds:

$$(a_n s^n + a_{n-1} s^{n-1} + \ldots a_1 s + a_0)\, e^{st} = x(t) \quad (2)$$

The input function is shown to be the same function as the output function (e^{st}) but simply multiplied by the constant $a_n s^n + \ldots a_1 s + a_0$ which we will term $1/H(s)$ from this point on.

Conversely for an input $x(t) = e^{st}$ the output will be

$$y(t) = \frac{e^{st}}{a_n s^n + \ldots a_1 s + a_0} = e^{st} H(s)$$

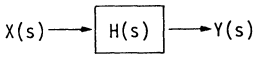
2.1 Eigenfunctions and Transfer Functions

Our starting point is the differential equation which is accepted as an accurate description of all linear invariant and continuous phenomena. For an input $x = e^{st}$ (where s may take on any complex value) the output function will also be e^{st} but multiplied by a constant H(s), that is $y = H(s) \cdot x$.

To denote that x and y are of identical functional form e^{st}, a more formal expression using capital letters for X and Y is adopted.

$$\frac{Y(s)}{X(s)} = H(s) \quad (3)$$

Also the time variable t is omitted for brevity.



Hence, function e^{st} will pass through a linear invariant system unaltered in functional form and merely modified by a constant, H(s). e^{st} are called the eigenfunctions of the system, and H(s) are the eigen-values or the transfer function. In general, any functions which undergo the linear operations of a given system and maintain their functional form (but are simply modified in amplitude or weight) are called eigenfunctions. Similar definitions relate to vectors which undergo linear transformation. The terms eigenvector and eigenvalue apply in these cases. The reader is reminded that H(s) is a function of the value of s alone and takes on unique values according to the value selected for s for the input.

Expanding briefly will solidify this point and also relate the practicality of the transfer function. First note that $e^{st} = e^{\sigma t}[\cos\omega t + j\sin\omega t]$; e^{st} has no time bound on it, and extends from t = minus to plus infinity. For $\sigma = 0$, $s = j\omega$ and $e^{st} = \cos\omega_0 t + j\sin\omega_0 t$.

As an example, choose

$$H_1(s) = \frac{a}{s + a} = \frac{Y(s)}{X(s)} \quad (4)$$

For $X(s) = e^{j\omega_0 t}$, $s = j\omega_0$

$$Y(s) = Y(j\omega_0) = \frac{a e^{j\omega_0 t}}{j\omega_0 + a} = \underbrace{\left[\frac{a}{\sqrt{\omega_0^2 + a^2}}\right]\left[e^{-j\phi}\right]}_{\text{Eigenvalue } H_1(o+j\omega_0)}$$

Amplitude

Phase

$$e^{j\omega_0 t} = \frac{a e^{-j\phi}}{\sqrt{\omega_0^2 + a^2}} \cdot X(j\omega)$$

$$\phi = -\tan^{-1}\left(\frac{\omega_0}{a}\right).$$

The complex eigenvalue is a complex multiplier. That is, it has the capability of scaling amplitude and also effecting a phase shift on $e^{j\omega t}$. From $H(j\omega)$ the complex frequency response is found.

In the laboratory real sinusoids are generated. These can be described mathematically by combining complex exponentials through Euler's identities as follows:

$$\cos\omega_o t = \frac{e^{j\omega_o t} + e^{-j\omega_o t}}{2}$$

$$\sin\omega_o t = \frac{e^{j\omega_o t} - e^{-j\omega_o t}}{2j}$$

The real sinusoid frequency response of the system described by $H_1(s)$ is found conceptually by forcing $H_1(s)$ separately with $e^{+j\omega_o t}/2$ and with $e^{-j\omega_o t}/2$ and then adding the responses.

$$Y(j\omega) + Y(-j\omega) = \left[\frac{ae^{-j\phi}}{\sqrt{\omega_o^2 + a^2}}\right]\frac{e^{j\omega_o t}}{2} + \left[\frac{ae^{+j\phi}}{\sqrt{\omega_o^2 + a^2}}\right]$$

$$\left[\frac{e^{-j\omega_o t}}{2}\right] = \frac{a}{\sqrt{\omega_o^2 + a^2}}\cos(\omega_o t - \phi)$$

It can be shown that the steady state response can be found directly from the transfer function. That is, for real sinusoid inputs $x = \cos(\omega t + \Theta)$, the output y is

$$|H(j\omega)|\cos(\omega t + \Theta + \phi_o)$$

where Θ is the input reference phase and ϕ_o is the phase imparted by the network transfer function. Details of this discussion can be found in The Analysis of Linear Circuits by C. Close.

Real exponentials and damped sinusoids are also special cases of the eigenfunction e^{st}. For $\omega = 0$, $e^{st} = e^{\sigma t}$. The transfer function is very general in that it gives the response for any input eigenfunction for any specified value of s.

For $x(t) = e^{-\alpha t}$, $\sigma = -\alpha$ and $\omega = 0$. The output will be of the form $e^{-\alpha t}$ but will have a coefficient $H(\sigma)$.

$$y(t) = \frac{a}{\sigma + a}e^{\sigma t} = \left[\frac{a}{a-\alpha}\right]e^{-\alpha t}$$

Eigenvalue coefficient

This method of system characterization has not attracted much interest probably because at $t = -\infty$, $e^{-\alpha t}$ is infinitely large. However, conceptually speaking, if one applies $e^{-\alpha t}$ to $H_1(s)$, $H(-\alpha)\,e^{-\alpha t}$ is the output response.

2.2 LaPlace Transform as a Convolution

The system transfer function can be found directly from its impulse or natural response by LaPlace transformation. The impulse response of a continuous system can be obtained by applying a unit impulse to the input of H. The impulse has the property of having unit area (i.e., volt-sec) while having infinitely high amplitude. It can be defined as a rectangular pulse whose width T approaches zero and whose amplitude 1/T approaches infinity (Figure 1).

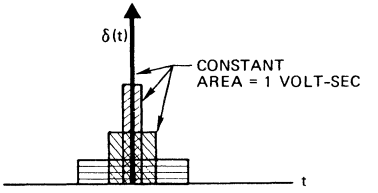


Figure 1. Generation of a Unit Impulse or Dirac Delta Function $\delta(t)$ (Area is a constant 1 volt-sec, and width and amplitude vary inversely)

Figure 2 shows the canonical representation for H. The application of an impulse imparts an initial value of 1 volt on the first integrator. The response which follows is the impulse response or natural response of the filter. It is equivalent to the homogeneous solution of the differential equation (1) (i.e., the solution for x = 0).

It is not possible for an ideal impulse to be generated in real life, but the theoretical effect of its application may be duplicated perfectly by placing an initial value on the system at t = 0, through any available means. The reader is advised to consult any book on circuit theory for an in-depth discussion on system impulse response and the homogeneous differential equation.

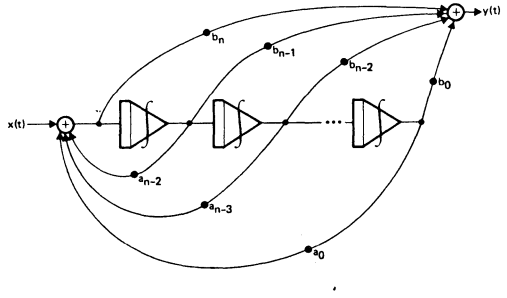


Figure 2. General Canonical Form

As a preliminary to the actual LaPlace integral derivation, an input function x(t) is approximated by a sequence of impulses weighted by T · x(t) (Figure 3).

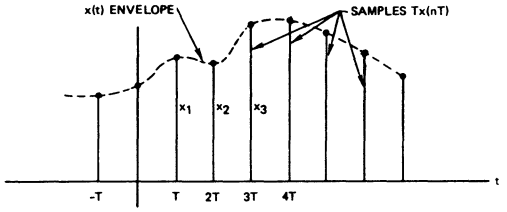


Figure 3. Discrete Time Approximation of x(t)

Hypothetical function x(t) shown approximated by impulses weighted by T · x(t) at T spacing; all impulses are actually infinitely high but have various weights.

The approximation is written in equation form:*

$$x(t) \simeq T \sum_{n=-\infty}^{\infty} x(t)\,\delta(t - nT) = x(nT) \qquad (5)$$

(function envelope (weight); impulses shifted in time by nT)

For T→0 the summation becomes an integral. T (the normalizing factor which maintains fairly constant energy for all values of T) becomes the differential increment dt, and nT becomes a continuous time variable τ. The integral

$$x(t) = \int_{-\infty}^{\infty} x(t)\,\delta(t - \tau)\,dt = \lim_{T\to 0} T\,x(nT) \qquad (6)$$

may be verified as correct.

Good insight is gained into the system behavior by applying one of the impulses from Figure 3, say x(-3T) δ(t + 3T), and observing the system response to it. For an impulse of unit weight applied at t = 0, a hypothetical impulse response is established (Figure 4).

Figure 4. Impulse Response h(t)

The system is casual or nonanticipatory in that the response does not precede the input.

Figure 5 shows the response for the system with x(-3T) δ(t + 3T) applied.

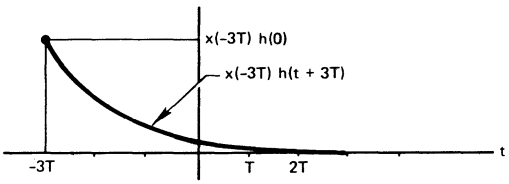


Figure 5. System Response to x(-3T)

The system output to the complete x(nT) string is found by accumulating all the individual impulse responses (Figure 6).

*The approximation for x(t) should include an integral, because in the strictest mathematical sense the shifting property of a dirac delta function is defined only under integration. The abbreviated form has been generally accepted in the engineering field, probably because it is more clear.

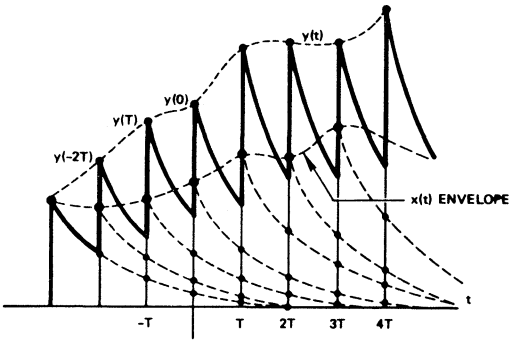


Figure 6. Superposition Sum of Individual Impulse Responses

For example, if x(t) began at t = -3T and were zero previously, then the output at t = -3T would be $T \cdot x(-3T) \cdot h(0) = y(-3T)$. The output at t = -2T has contributions from x(t) at -2T, namely $T \cdot x(-2T) \cdot h(0)$ and the tail of h(t+3T), i.e., $T \cdot x(-3T) \cdot h(-T + 2T)$. The outputs for various discrete times are listed below.

$$y(-3T) = T\, x_{-3}\, h(0)$$

$$y(-2T) = T[x_{-2}\, h_0 + x_{-3}\, h_1]$$

$$y(-T) = T[x_{-1}\, h_0 + x_{-2}\, h_1 + x_{-3}\, h_2]$$

$$\vdots$$

$$y(nT) = T[x_n\, h_0 + x_{n-1}\, h_1 + x_{n-2}\, h_2 + \cdots x_{-3} h_{n+3}]$$

In closed form

$$y(nT) = T \sum_{m=-3}^{n} x(mT)\, h(t-mT) \qquad (7)$$

For a continuous input, mT and nT become continuous variables τ and t, respectively, and for the most general case where x(t) begins at $t = -\infty$, the summation in equation (7) becomes the continuous convolution integral.

$$y(t) = \int_{-\infty}^{t} x(\tau)\, h(t-\tau)\, d\tau = \lim_{T \to 0} y(nT) \qquad (8)$$

The integral can be rearranged slightly to suit our purposes by making the following change of variables:

$$\alpha = t - \tau$$

It follows that $d\alpha = -d\tau$

Original Integral		New Integral	
Variable of Integration	Limit	Variable of Integration	Limit
τ	$-\infty$	α	$t-(-\infty)=\infty$
τ	t	α	t-t=0

The convolution is equivalently stated

$$y(t) = \int_{0}^{\infty} x(t-\alpha)\, h(\alpha)\, d\alpha \qquad (9)$$

Recalling that the transfer function H(s) relates the amount of e^{st} that will pass through the system for a given s, let $x(t) = X(s) = e^{st}$, then $x(t - \alpha) = e^{-s(t-\alpha)}$. It follows that

$$y(t) = \int_{0}^{\infty} e^{s(t-\alpha)}\, h(\alpha)\, d\alpha \qquad (10)$$

The exponential is separable yielding

$$y(t) = e^{st} \int_{0}^{\infty} h(\alpha) e^{-s\alpha} d\alpha = X(s) \int_{0}^{\infty} h(\alpha) e^{-s\alpha} d\alpha \qquad (11)$$

For $x(t) = e^{st}$ it was shown (starting with equation (1)) that Y(s) = H(s) X(s). Allowing H(s) X(s) to step in for Y(s) yields the well known LaPlace transform integral.

$$X(s)\, H(s) = X(s) \int_{0}^{\infty} e^{-s\alpha}\, h(\alpha)\, d\alpha \qquad (12)$$

and

$$H(s) = \int_{0}^{\infty} h(\alpha)\, e^{-s\alpha}\, d\alpha = \int_{0}^{\infty} h(t)\, e^{-st}\, dt \qquad (13)$$

2.3 Summary

Linear time invariant continuous systems are described by nth order differential equations.

In general, obtaining an expression for the output y(t) requires the time domain solution of the differential equation. The involved process may be tedious and yield unwieldy results for most inputs. For inputs of the form $x(t) = e^{st}$ the output is always of the same functional form and modified only by a coefficient. That is, $y(t) = H(s)e^{st}$. H(s) is called the transfer function of the system and it results from passing e^{st} through the differential equation. To denote that the input is specifically the eigenfunction* e^{st}, the input and output functions are more formally denoted by capital letters X(s) and Y(s). The time dependence of e^{st} is understood and the t is dropped for brevity. The H(s)'s corresponding to each X(s) are the eigenvalues. There are infinitely many eigenvalues since s may take on infinitely many values.

As implied, dealing with the differential equation and its solution can be a tiresome and often unrewarding experience. The transfer function is very useful for computing frequency response, assessing system stability, and doing complicated filter and system designs. It can also be used indirectly to compute the time response of a filter to inputs other than e^{st} without resorting to the differential equation.

When the impulse response of a system is given and the transfer function H(s) is desired, the LaPlace transform may be used. As illustrated in the derivation, the LaPlace transform is the convolutional solution of a system or differential equation whose input is the system eigenfunction. The convolution (or superposition) integral is employed to find the output for any input, but it yields a rather simplistic result when the eigenfunction is used as the input and the transfer function is implicitly described:

$$X(s)\,H(s) = Y(s)$$

The eigenfunctions are found to have practical significance, in that appropriate pairs yield physically realizable and usable waveforms. Specifically, allowing $\omega = 0$ yields $e^{st} = e^{\sigma t}$, and for $\sigma = 0$,

$$\frac{e^{j\omega t} + e^{-j\omega t}}{2} = \cos\omega t$$

is formed, or more generally

$$\frac{e^{st} + e^{s^*t}}{2} = e^{\sigma t}\cos\omega t$$

The transfer function representations of systems are classically termed as frequency domain descriptions, where differential equation solutions deal with the time or spatial domain. The variable s is the complex frequency variable which has real and imaginary parts, σ and $j\omega$, respectively. Technically, the response of a system to real frequency relates to its behavior in passing $e^{\sigma t}$. The response to imaginary frequency relates to "real world" sine or cosine waveforms.

3. Z TRANSFORM

The LaPlace and Z transforms belong to a class of linear time invariant transformations loosely termed as convolutional transforms. Their derivations stem from the superposition determination of a system output given that it is forced with the eigenfunction input.

The Z transform, which is the widely accepted tool to describe and design purely discrete time and mixed systems, provides similar information stability and frequency response as does the LaPlace transform for continuous systems. The Z transform and discrete transfer function relate to the frequency domain in a discrete time system.

The Z transform may be derived in the same manner as is the LaPlace transform, with the exception that the time variable is discrete. Before proceeding with the derivation, some opening remarks concerning discrete time or sampled data functions are in order.

As pointed out earlier, continuous functions are special cases of discrete time functions. Figure 3 and equation (6) indicate that decreasing sampling time T adds more and more samples on the waveform. As $T \to 0$ the sampled waveform becomes continuous.

One would expect that the continuous frequency domain could be interpreted as a special, or more specifically, limiting, case of the discrete frequency domain, just as continuous time functions are special cases of discrete time functions (i.e., $T = 0$). A mathematical description to this end would soften the absolute distinction which is usually made between sampled and continuous worlds. Alternating between the two without having to resort to separate time-to-frequency transforms is sometimes beneficial in a practical sense as well as a tutorial sense.

However, the Z transform is not designed to do this in its basic form; and consequently the

* As a rule, functions which pass through a linear system unaltered in functional form are termed eigenfunctions. The associated multipliers are called eigenvalues. This description is consistent with operations in linear vector spaces where a vector $\bar{x}$ undergoes a linear algebraic transformation A resulting in vector $\lambda\bar{x}$, where λ is a constant. $\bar{x}$ is commonly known as an eigenvector. The multiplier λ is an eigenvalue.

notion of the discrete frequency domain is usually held quite separate from that of the continuous frequency domain, and its related s plane. The next section briefly describes the effects of applying signals at arbitrary sampling rates to continuous elements. A smooth transition between the sampled and continuous frequency domains is thus provided. The following development ultimately leads to the Z transform.

3.1 Effects of Sampled Data on Continuous Elements

Figure 7 shows a continuous filter with impulse response h(t), subjected to an input waveform x(t), which is sampled by an impulse train. The train is normalized by T, the sampling interval.

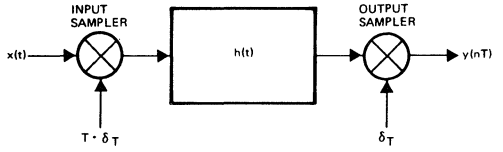


Figure 7. Continuous Filter with Sampled Input

The immediate output y(t) is jagged waveform depicted in Figure 6. Equation (7) describes the waveform at this point exactly for the sampled input denoted Tx(nT). If we are concerned with y(t) at the sample points, a fictitious sampler (synchronized with $T\delta_T$) may be added. The final output is then denoted y(nT). The discrete convolution sum describing y(nT) is given in equation (14).

$$y(nT) = T \sum_{m=-\infty}^{n} x(mT)\, h(nT-mT) \qquad (14)$$

It can be shown that when a continuous system is subjected to a sampled input the differential equation becomes a forward difference equation. The differentials are replaced with forward differences and the coefficients take on modified values.

The first forward difference denoted $(\Delta_f y_n/T)$ approximates dy/dt. It is defined below:

$$\frac{\Delta_f y_n}{T} = \frac{y(nT+T) - y(nT)}{T} \quad \text{and} \quad \lim_{T\to 0} \frac{\Delta y}{T} = \frac{dy}{dt} \qquad (15)$$

The difference operation is reminiscent of basic calculus, where the first derivative or slope of the function is approximated by the same. For sampled functions, derivatives are meaningless; and at least in this case* they are approximated by first differences.

Equation (16) in its discrete form is given.

$$a'_n \frac{\Delta^N y_n}{T^N} + a'_{n-1} \frac{\Delta^{N-1} y_n}{T^{N-1}} + \ldots a'_1 \frac{\Delta y_n}{T} + a'_0 y_n = \sum_{i=0}^{N} \frac{b'_i \Delta^i x_n}{T^i} \qquad (16)$$

Variables x and y are now discrete and denoted by x(nT) or x_n, etc.

The discrete version of e^{st} is the eigenfunction to equation (16). We can confirm this by observing its behavior under successive differencing. Maintaining the shortened notation:

$$\frac{y_{n+1} - y_n}{T} = \frac{e^{s(n+1)T} - e^{snT}}{T} = e^{snT} \frac{e^{sT} - 1}{T} \qquad (17)$$

Note that e^{snT} (the discrete eigenfunction) is preserved and is multiplied by a constant $(e^{sT} - 1)/T$.

The second difference yields:

$$\frac{\Delta}{T}\left[\frac{\Delta}{T} e^{snT}\right] = \left[\frac{e^{sT} - 1}{T}\right] \frac{\Delta}{T} e^{sT} = \left[\frac{e^{sT} - 1}{T}\right]^2 e^{snT} \qquad (18)$$

Similarly,

$$\boxed{\frac{\Delta_f^N}{T} e^{snT} = \left[\frac{e^{sT} - 1}{T}\right]^N e^{snT}}$$

*The field of numerical analysis deals with the approximation of derivatives and integrals by more sophisticated operations on discrete signals. The processes involved lead to various other discrete frequency domain variables such as the w or bilateral transform variable. The interested reader may find material on these subjects from many sources.

Recalling that for the continuous case

$$\boxed{\frac{d^N}{dt^N} e^{st} = s^N e^{st}} \qquad (19)$$

The reader should delight in knowing that the multiplying factor $(e^{sT} - 1)/T$ is exactly analogous to s. More specifically, it is the discrete version of s; e^{sT} can be expanded:

$$\left[\frac{e^{sT} - 1}{T}\right] = \frac{1}{T}\left\{\left[1 + sT + \frac{(sT)^2}{2!} + \frac{(sT)^3}{3!} + \ldots\right] - 1\right\} \qquad (20)$$

and it follows directly that

$$\boxed{\lim_{T\to 0}\left(\frac{e^{sT} - 1}{T}\right) = s}$$

Moreover, the resulting discrete transfer function $H([e^{sT} - 1]/T)$ becomes $H(s)$ as $T\to 0$.

Mathematically,

$$\lim_{T\to 0} H\left(\frac{Z-1}{T}\right) = H(s)$$

where $Z = e^{st}$

For convenience we assign the Greek letter $\beta = (Z - 1)/T$ for future use.

Following the same direction as with the LaPlace derivation, for $x(nT) = e^{snT}$ the same signals are denoted with capital letters and the time variable is dropped. Hence,

$$\left.\begin{matrix} x(nT) = X(\beta) \\ y(nT) = Y(\beta) \end{matrix}\right\} \text{ for } x(nT) = e^{snT} \qquad (21)$$

The two are related by the transfer function:

$$Y(\beta) = H(\beta)\, X(\beta)$$

Given that a system has a given impulse response h(t), its discrete transfer function is found directly through the convolution sum of equation (14) with $x(nT) = e^{snT}$.

The operation is trivial and leads ultimately to the Z transform.

$$y(nT) = T \sum_{m=-\infty}^{n} e^{smT}\, h(nT-mT) \qquad (22)$$

Letting $i = n - m$, a summation over i results with the modified limits as indicated.

$$y(nT) = T \sum_{i=0}^{\infty} e^{s(n-i)T}\, h(iT) \qquad (23)$$

The reader may check the substitution of variables and subsequent limit modifications using the LaPlace derivation as a guide.

$e^{s(n-i)T}$ separates, and using the frequency domain notation, equation (24) results.

$$Y(\beta) = H(\beta)\, X(\beta) = T \cdot e^{snT} \sum_{i=0}^{\infty} h(iT)\, e^{-siT}$$

$$H(Z) = T \sum_{i=0}^{\infty} h(iT) Z^{-i} \quad \text{or} \qquad (24a)$$

$$H(\beta) = T \sum_{i=0}^{\infty} h(iT)[T\beta + 1]^{-i} \qquad (24b)$$

where $Z = T\beta + 1$.

Because β and Z are related algebraically, $H(\beta)$ may be denoted $H(Z)$.

Equation (24a) with the normalizing T omitted is the accepted form of the Z transform. The effects of sampling on a continuous system are best illustrated through the normalized Z transform, and for the present the T will be included. In Section 4 the Z transform is used in the direct computer implementation of digital filters and the T is omitted.

3.2 Sampling Effects on First Order Systems

To illustrate the effects of sampling, a first order filter with $h(t) = e^{-at}$ is selected for the system in Figure 7.

The LaPlace transform of h(t) is:

$$H(s) = \frac{1}{s + a} \qquad (25)$$

The poles and zeros for a general H(s) are typically denoted in the complex s plane. The s plane may be used as an analytical tool for graphically computing frequency response or root locus plots. It symbolically describes the system relative performance and stability. That is, real poles plotted in the left half plane represent converging exponential impulse responses. Complex poles represent damped sinusoid components and right half plane poles represent an unstable system.

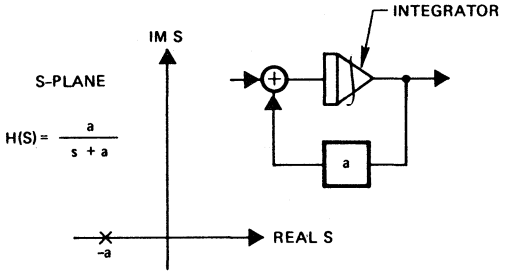


Figure 8. s Plane Showing Pole for H(s) at s = -a

Sampling x(t) bends the jω axis of the s plane into a circle of radius 1/T centered at -1/T as shown in Figure 9a. This can be verified by plotting β for s = jω. The term $(e^{j\omega T} - 1)/T$ maps out a circle whose arc length is the input signal frequency ω. The circle becomes infinitely large as T approaches zero, and the circle perimeter becomes the jω axis of the s plane. Equivalently, the jω axis may be considered a circle of infinite radius; corresponding to the fact that a continuous waveform is a sampled waveform with infinite sampling rate. The area outside the circle corresponds to the right half s plane. Poles in this region result in instability.

The real axis is a direct but not a linear mapping of the real s axis. -1/T in the sampled plane corresponds to negative infinity in the s plane. Hence, the effect of sampling on a continuous system is not just to bend the jω axis but also to modify the numerical value of the real pole positions by an exponential warping factor. This is illustrated by computing the normalized Z transform for e^{-anT}.

$$H(Z) = T \sum_{n=0}^{\infty} e^{-anT} Z^{-n} = T\left[1+e^{-aT} Z^{-1} + e^{-2aT} Z^{-2} + \ldots\right]$$

This converging infinite series can be expressed in closed form:

$$H(Z) = \frac{T}{1-e^{-aT} Z^{-1}} = \frac{TZ}{Z-e^{-aT}} \qquad (26)$$

Substituting $Z = T\beta + 1$

$$H(\beta) = \frac{T\beta+1}{\beta + \frac{1-e^{-aT}}{T}} \qquad (27a)$$

From equation (27) it is seen that sampling produces a pole of $\beta = -(1 - e^{-aT})/T$ and a zero at $\beta = -1/T$. As the sampling rate increases, the circle radius approaches infinity, and $-(1 - e^{-aT})/T$ approaches -a which is the correct pole location for $h(t) = e^{-at} \cdot -(1 - e^{-aT})/T$ is therefore the sampled system view of a continuous system singularity at -a. One may verify that taking the limit as T goes to zero yields -a, and

$$\lim_{T\to 0} \left[\frac{T\beta + 1}{\beta + \frac{1 - e^{-aT}}{T}}\right] = \frac{1}{s + a} \qquad (27)$$

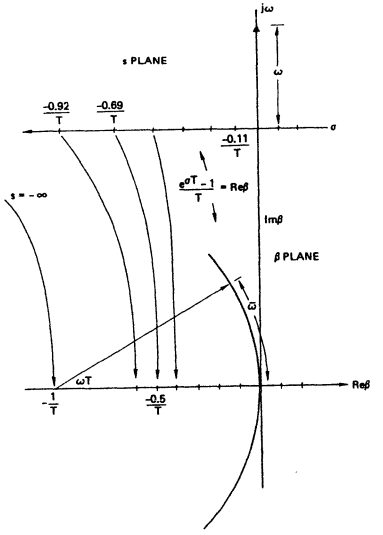
By expanding e^{-aT} into a power series this result is obtained:

$$e^{-aT} = 1 - aT + \frac{(aT)^2}{2} - \frac{(aT)^3}{3!} + \ldots$$

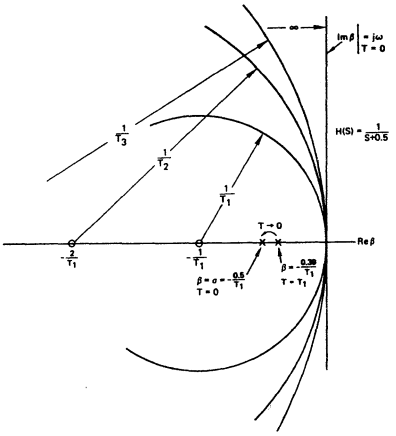
Figure 9b shows the pole zero plot in the β plane for three sampling intervals T_1, T_2 and T_3. In Figure 10 three implementations for the first order discrete filter are given. Each filter gives a sampled output with a continuous input, although theoretically the inputs may be sampled and synchronized with the input samplers. The frequency responses for all three will be identical at the sampling instants.

Figure 10b,c show purely discrete versions of the configuration. In b the accumulator or discrete integrator is shown within the enclosed area. It is mathematically equivalent to an analog integrator driven with a sampled input. The delay elements are intrinsic to implementation of any discrete function and may be formed with purely continuous elements (L-C distributed delay lines), or with discrete elements (digital registers or charge coupled devices) according to the nature of the signal inputs. For demonstrative reasons we have elected to simulate systems which apply to real continuous phenomena (such as integration, etc.). Even if this is the intent of the design, the system can always be described more simply with delays rather than with discrete integrators as the basic element. This is shown by example in Figure 10. The transfer functions for all three are shown to be equivalent with some algebraic shuffling of terms.

For purely digital filters where the data is sampled and quantized by an A/D converter, all the arithmetic operations are done digitally. The delays are implemented with memory (or shift registers), the summing points are realized with digital adders, and digital multipliers are employed to give the correct filter coefficients. Some useful digital filters are designed by directly substituting a discrete frequency variable for s in the analog transfer function. The resulting transfer function can be expressed ultimately in terms of Z or Z^{-1}, regardless of the discrete variable form. The configuration can always use delays directly rather than discrete integrators (whose functional elements are delays).

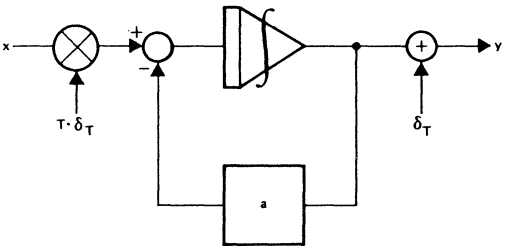


a) s and β Plane Correspondence

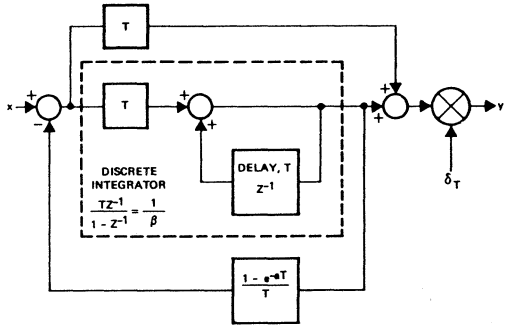


b) Pole Zero Migration

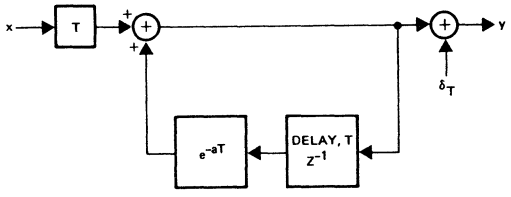
Figure 9. Pole Zero Plot for Various Sampling Rates. The discrete pole is located at $\beta = -0.39/T_1$ for $T = T_1$. The pole migrates to the left, asymptotically approaching $\sigma = -0.5/T_1$ as $T \rightarrow 0$.



a) Sampled Analog Configuration



b) Discrete Integrator Configuration



c) Simplified Delay Implementation

Figure 10. Three Implementations for Realizing H(Z) (All transfer functions become H(s) as T→0). The discrete integrator in b simulates the integration process by rectangular approximation.

Application Notes

Mathematically this is true because s is replaced with a discrete frequency variable which is always an algebraic function of Z. Using β as an example, one might approximate double integration $(1/s^2)$ by $1/\beta^2$.

In terms of Z this becomes

$$\frac{T^2}{(Z-1)^2} = \frac{T^2}{Z^2 - 2Z + 1} = \frac{T^2 Z^{-2}}{1 - 2Z^{-1} + Z^{-2}}$$

This function can be simulated easily with the signal flow graph in Figure 11.

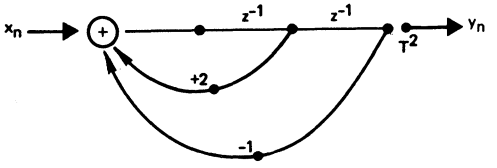


Figure 11. Approximation of $1/s^2$

Direct implementation with the delay elements simplifies computations in systems where analog filter functions are used as the baseline for the digital design (an example is given in Section 4 with the bilinear transform). Moreover, filters with impulse responses of finite duration (FIR filters) utilize the delay function directly. That is, these filters do not originate by replacing s with a discrete time frequency variable. They are used in applications where linear phase is a requirement and where erratic filter shapes are to be implemented. FIR filter structures are discussed in Section 4.

Figure 12 shows the Z plane which is a shifted normalized version of the β plane shown in Figure 10. The pole and zero for the first order discrete network are found easily from H(Z) in equation (26) by setting the denominator and numerator equal to zero and solving for the value of Z.

$$Z - e^{-aT} = 0$$

$$TZ = 0$$

A pole results at $Z = e^{-aT}$ and a zero at $Z = 0$.

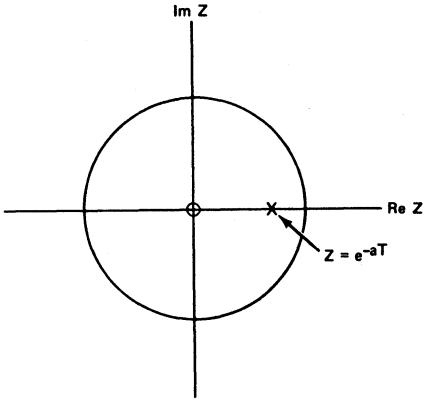


Figure 12. Z Plane Showing Pole Zero Locations for First Order Discrete Network

3.3 Second Order Effects

In this section, the frequency domain effects of a second order filter subjected to sampled data are investigated. The emphasis is on pole zero migrations in the β plane, and frequency response. The equivalent forward difference equation is also derived for the second order low pass.

An analog second order low pass filter has a transfer function

$$H(S) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} = \frac{\omega_n^2}{(s+\xi\omega_n)^2 + \omega_n^2[1-\xi^2]}$$

with s plane poles as shown in Figure 13. Its impulse response is found by inverse LaPlace to be

$$h(t) = K_o e^{-\xi\omega_n t} \sin \omega_o t \qquad (28)$$

$$= K_o e^{-at} \sin \omega_o t$$

where

$$K_o = \frac{\omega_n}{\sqrt{1-\xi^2}}$$

and

$$\omega_o = \omega_n\sqrt{1-\xi^2}$$

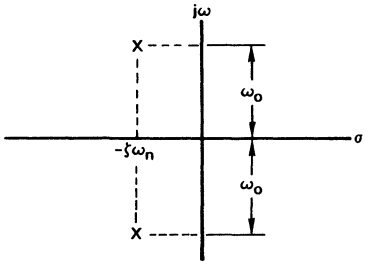


Figure 13. Low Pass Second Order Filter s Plane Plot. Poles

$$s = -\xi\omega_n \pm j\omega_n$$

To find the complex frequency response with a sampled input, the normalized sampled input $T \cdot e^{snT}$ is convolved with h(t). More simply stated, the normalized Z transform of h(t) is found.

$$H(Z) = T \sum_{n=o}^{\infty} \left(K_o\, e^{-anT} \sin \omega_o nT \right) Z^{-n} \quad (29)$$

First note that

$$e^{-anT} \sin \omega_o nT = \frac{e^{(j\omega_o - a)nT} - e^{-(j\omega_o + a)nT}}{2j}$$

and $Z\{e^{-anT} \sin \omega_o nT\}$

$$= \frac{T}{2j} \sum_{n=o}^{\infty} \left[e^{(j\omega_o - a)nT} - e^{-(j\omega_o + a)nT} \right] Z^{-n} \quad (30)$$

The two exponentials are complex, but this presents no difficulty and the two infinite sums can be expressed in closed form.

$$H(Z) = \frac{K_o T}{2j} \left(\frac{1}{1 - e^{-aT} e^{+j\omega_o T} Z^{-1}} - \frac{1}{1 - e^{-aT} e^{-j\omega_o T} Z^{-1}} \right)$$

$$= \frac{K_o (e^{-aT} \sin\omega_o T) TZ}{\left(Z - e^{-aT} e^{+j\omega_o T}\right)\left(Z - e^{-aT} e^{-j\omega_o T}\right)} \quad (31a)$$

$$= \frac{K_o (e^{-aT} \sin\omega_o T) TZ}{Z^2 - 2e^{-aT} \cos \omega_o TZ + e^{-2aT}} \quad (31b)$$

Now

$$\beta = \frac{Z - 1}{T}$$

and

$$H(\beta) = \frac{K_o e^{-aT} (\beta + \frac{1}{T}) \sin \omega_o T}{\left(\beta + \frac{1 - e^{-aT} e^{-j\omega_o t}}{T}\right)\left(\beta + \frac{1 - e^{-aT} e^{-j\omega_o T}}{T}\right)} \quad (32)$$

Equation (32) looks at first glance somewhat formidable. A closer look shows it to be very close to the second order analog system.

First observe that the two complex poles,

$$p_1, p_2 = -\frac{1 - e^{-aT \pm j\omega_o T}}{T},$$

are on the radii joining $\beta = -1/T$, and the points $\pm\omega_o$ units along the arc of the ω contour (Figure 14). The distance from the contour is $(1 - e^{-aT})/T$. The reader may note a generality for real and complex poles at this point. Recall that for a first order sampled system with time constant $\tau = 1/a$, the pole is on the real axis, $(1 - e^{-aT})/T$ units from the β plane origin (Figure 9).

In both cases the poles are at a distance of $(1 - e^{-aT})/T$ from the ω contour (circle). From equation 27b, as $T \to o$ and the ω contour becomes the jω axis, this distance becomes $a(=\xi\omega_n)$. For the second order filter $-\xi\omega_n$ is the real coordinate for the s plane poles (Figure 13).

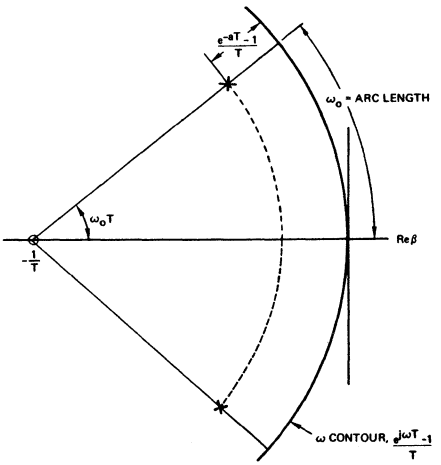


Figure 14. Poles in the β Plane for Second Order System

Applying Euler's expansion for $e^{\pm j\omega_o T}$ and using L'Hospital's rule from basic calculus:

$$\lim_{T\to 0} p_1, p_2 = -\frac{1 - e^{-aT}(\cos \omega_o T \pm j \sin \omega_o T)}{T} \quad (33)$$

$$= -a \pm j\omega_o$$

which comprise the analog pole pair. The complex pole locations for three T values are plotted in the β plane in Figure 15a. Figure 15b indicates a graphical means of computing frequency response in the β plane.

The impulse response for the filter is

$$h(t) = K_o e^{-\xi\omega_n t} \sin \omega_o t$$

$$\omega_o = \frac{\pi}{4T_1}$$

and

$$a = \xi\omega_n$$

$$= .5/T_1$$

The discrete time impulse response is

$$h(nT) = e^{-\xi\omega_n nT} \sin \omega_o nT$$

For the lowest sampling rate ($1/T_1$) the poles exist on the $\pm\omega_o T_1$ radii $(1 - e^{-aT})/T \cong .39/T_1$ units from the T_1 circle perimeter. When the sample rate is doubled the radius increases and the distance is $.44/T_1$ units from the new circle. Finally as $T\to 0$, the distance is "a" itself: $.5/T_1$.

In both first and second order examples, a zero occurs in the numerator at $\beta = -1/T$ (the center of the circle, Figure 15). As the sample rate increases the location of this zero moves toward β or $s = -\infty$. Zeros at infinity always accompany realizable analog transfer functions and these zeros are said to be implied. They provide no computational information and are not included in the transfer function. Thus $1/(s + a)$ is really $(s/\infty + 1)/(s + a)$.

If the reader has any doubt that such zeros exist, he can convince himself by taking a continuous system and sampling it! Sampling brings points of infinite frequency into a finite region as illustrated by both first and second order examples.

The forward difference equation related to H(β) is found from equation (32). Clearing the denominator, letting Y(β) and X(β) be output and input terms respectively, and recalling that β represents a first difference operator (equation 17), equation (34) results.

$$\frac{\Delta^2 y_n}{T^2} + 2\left[\frac{1 - e^{-aT}\cos \omega_o T}{T}\right]\frac{\Delta y_n}{T} + \left(\frac{1 - 2e^{-aT}\cos \omega_o T + e^{-2aT}}{T^2}\right) y_n$$

$$= e^{-aT} \sin \omega_o T \left(\frac{\Delta x_n}{T} + \frac{x_n}{T}\right) K_o \quad (34)$$

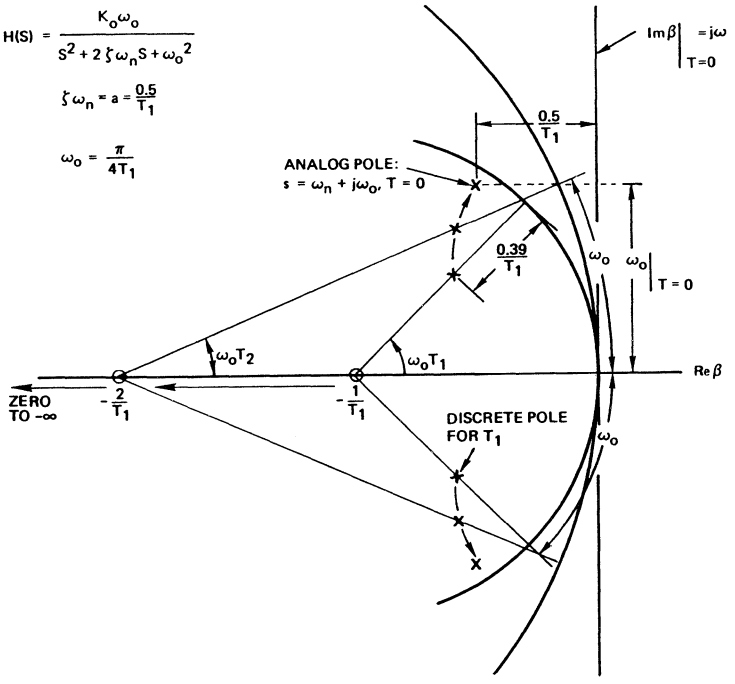
As $T\to 0$ the differences become differentials, d^2y/dt^2 etc. Note the presence of the difference term $\Delta x_n/T$, corresponding to the zero at $-1/T$, in the right-hand side of equation (33). In the limit, $\Delta x_n \to 0$ and

$$\lim_{T\to 0}\left(\frac{e^{-aT}\sin \omega_o T}{T}\right)(\Delta x_n + x_n) = \omega_o \cdot x(t)$$

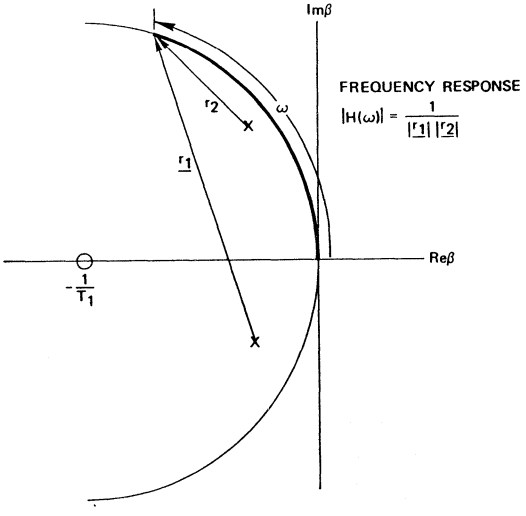
The reader can verify that equation (34) becomes

$$\frac{d^2y}{dt^2} + 2\xi\omega_n \frac{dy}{dt} + \omega_n{}^2 y(t) = \omega_o K_o x(t) \quad (35)$$

The canonical flow diagrams for equations (34) and (35) are given in Figure 16. The accumulator elements in Figure 16(a) can be expanded so that the second order discrete flow graph contains only delay elements, Z^{-1} and Z^{-2}.

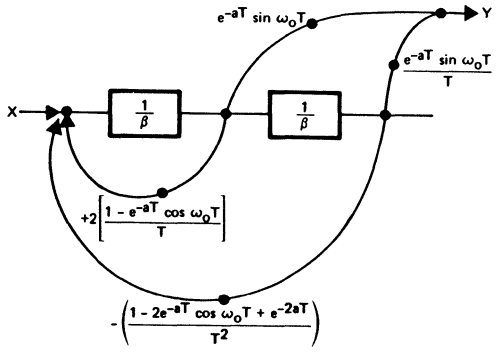


a) Pole Zero Plot

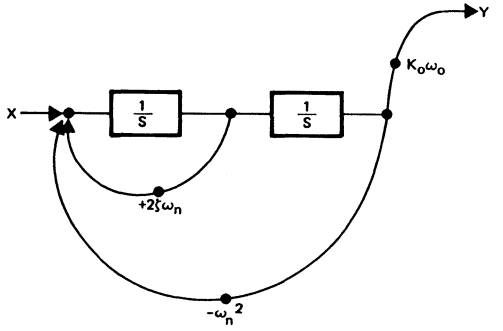


b) Graphical Computation of Frequency Response

Figure 15. β Plane for Second Order Low Pass Filter



a) The $1/\beta$ elements are discrete integrators (accumulators, see Figure 10b) with transfer function $TZ/(Z-1)$.



b) The feedback and feed forward coefficients of a) become those in b) as $T \rightarrow 0$ and $1/\beta \rightarrow 1/s$.

Figure 16. Canonical Second Order Forms

4. APPLICATION OF Z TRANSFORM TO FILTER SYNTHESIS

The preceding sections were devoted to presenting the Z transform in an systematic fashion. It was indicated that when analog elements are subjected to sampled waveforms their frequency domain representations are altered. The $j\omega$ axis of the s plane can be interpreted as a circle of infinite radius, and when systems are subjected to a finite sampled waveform this axis bends into a circle of radius $1/T$. This interpretation provides analytical insight into mixed systems and some digital systems which attempt to simulate purely analog systems.

However, digital filters are being used in areas where analog techniques do not apply. Digital filter theory has reached a level of sophistication where many designs could never be duplicated with analog techniques. Recently developed mathematical design techniques provide for digital filters with cutoff rates and bandwidths that can not be approached with analog filters.

Digital filters can be put into two main categories: infinite impulse response (IIR) and finite impulse response (FIR) filters. FIR filters are usually implemented with a finite length delay line with multiple taps. These filters are very flexible and especially useful in synthesizing erratic filter shapes. They are successfully utilized in very sharp cutoff and narrowband applications where linear phase is a requirement.

Butterworth, Chebyshev, and elliptical filters may be implemented with cascaded second order IIR filter sections in the same way as analog filters. The results in the digital world are analogous but more predicatable, because accuracy is dependent only on computer word length and not on component variations. As a result, very sophisticated filters may be built with much better results than analog filters could provide.

4.1 IRR Implementations

The most often used recursive element in filter synthesis is the second order canonical filter. This filter is the building block for very high order elliptic and Butterworth configurations as well as all-pass phase correcting filters.

A very effective technique for implementing elliptic and Butterworth filters is through analog transfer function. Because transfer functions for these filters are well documented, it is a simple matter to design the digital filter by replacing s in the analog transfer function with an appropriate discrete frequency variable. It was shown that differencing could be used as an approximation for differentiation in the differential equation. The resulting frequency variable was

$$\frac{e^{sT} - 1}{T}$$

which is analogous to s. Unfortunately, direct substitution of $(Z - 1)/T$ for s generally yields poor digital filter results except for very low frequency applications. However, excellent filters are obtained when s is replaced with

$$w = \frac{1}{T} \frac{Z - 1}{Z + 1}$$

The variable w results from approximating continuous integration by discrete trapezoidal integration as shown in Figure 17.

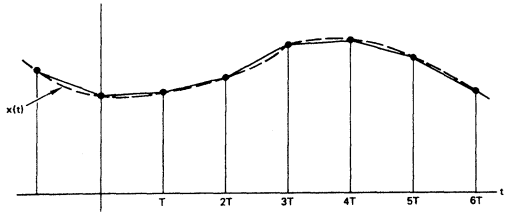


Figure 17. Integration Using Trapezoidal Approximation

The individual data points of x_n are connected by straight lines forming little contiguous trapezoidal sections. The area under the n^{th} section is given by s_n (Figure 18).

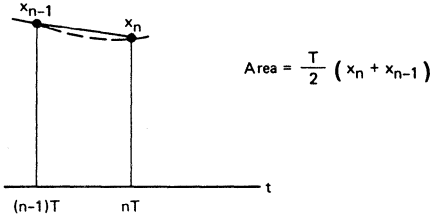


Figure 18. Trapezoid Section with Area S_n

The total accumulated area under x including s_n is given in equation (36).

$$^{*}\ s_n = s_{n-1} + \frac{T}{2}\left[x_n + x_{n-1}\right] \qquad (36)$$

The frequency domain representation for this integration process can be found by passing the discrete eigenfunction e^{snT} through equation(36), or simply Z* transforming the equation directly. Either way the result is given in equation (37).

$$^{**}\ \frac{S(Z)}{X(Z)} = \frac{T}{2}\left[\frac{1 + e^{-sT}}{1 - e^{-sT}}\right] = \frac{T}{2}\ \frac{1 + Z}{1 - Z}\ \frac{1}{s} \qquad (37)$$

Because s implies continuous differentiation

$$\frac{2}{T}\left[\frac{1 - Z}{1 + Z}\right]$$

replaces s in the desired analog transfer function. w has the remarkable property that its frequency contour ω coincides with the imaginary w axis just as ω corresponds to the imaginary s axis. This means that responses for digital and analog filters will be identical at corresponding points in frequency. The relationship between the analog and digital imaginary axes is not linear and so prewarping the critical frequencies in the analog filter is required before w is substituted for s in the analog transfer function. This is a simple matter and should become clear with the following discussion.

The ω contour in the w plane can be found by letting s = jω.

$$w|_{s=j\omega} = \frac{2}{T}\ \frac{e^{j\omega T} - 1}{e^{j\omega T} + 1} = j\ \frac{2}{T}\tan\frac{\omega T}{2} \qquad (38)$$

Figure 19 shows the frequency correspondence in the s and w planes.

For lower frequencies, the imaginary w axis becomes fairly linear with ω. That is for small Θ, tan Θ=Θ. Therefore,

$$\frac{2}{T}\tan\frac{\omega T}{2} \simeq \omega$$

and the imaginary w and s axes track very closely. If a very high sampling rate 1/T were provided and a relatively low frequency cutoff filter were needed, one would not have to prewarp critical frequencies for the desired filter. Of course, in the limit as T→0 the w plane becomes the s plane

$$\lim_{T\to 0} w = s$$

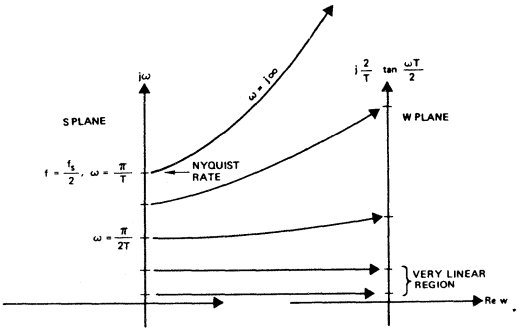


Figure 19. s and w Planes Showing Correspondence of Frequencies

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* In contrast, the reader should verify that 1/β implies rectangular integration and the accumulated area is $s_n = s_{n-1} + T\,[x_n]$ (Fig. 10b).

** The reader should consult any book on Z transforms or discrete time systems for an in-depth discussion on operations involving the Z transform.

Application Notes

It is evident from Figure 19 that a frequency of $f_S/2$ (i.e., $\omega = \pi/2$, one-half the sampling frequency) maps into j infinity in the w plane. Hence, traversing a relatively small span of frequencies close to the Nyquist frequency ($f_S/2$) results in a relatively large variation on the imaginary w axis. This fact provides advantage in the digital world for filters with sharp transitions. The following example illustrates this point.

Figure 20 shows the pole plot in the s plane for a fifth order* Butterworth filter whose cutoff frequency is at $\omega = \pi/2T$ or $f = f_S/4$ (1/4 the sampling frequency f_S). To get the same cutoff point for the digital filter the circular pole pattern has its radius widened according to $2/T \tan \omega T/2$. The pole pattern in both planes is exact other than normalization, because w is a direct substitution for s in the analog transfer function for the Butterworth filter.

The frequency response for the filter can be found graphically by drawing vectors from the imaginary frequency axes to the pole locations. The response at any point is the reciprocal of the product of the vector lengths. In the w plane a frequency of 3/8 f_S produces vectors which are proportionately longer on the Im w axis than on the $j\omega$ axis (Figure 19). The cutoff rate for the digital filter is therefore greater and provides a sharper filter than the corresponding analog filter.

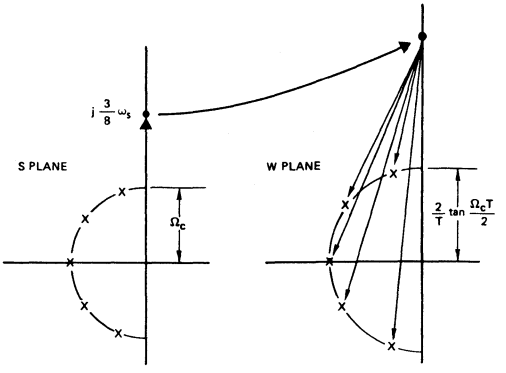

Figure 20. Pole Plots for Fifth Order Butterworth Filter Using Transform

*The reader should consult a book on filter theory for the actual details on the parameters for the Butterworth and elliptic filters.

The transfer function for the fifth order Butterworth is given in equation (39).

$$H(s) = \prod_{i=1}^{2} \frac{\Omega_c^2}{s^2 + 2\Omega_c \cos\frac{i\pi}{5}\, s + \Omega_c^2} \cdot \frac{\Omega_c}{s + \Omega_c} \tag{39}$$

The poles are situated in a circular contour at a radius of Ω_c (cutoff frequency) in the s plane. There are four complex conjugate poles and one real pole. The corresponding discrete domain cutoff frequency is ω_c. To show how the discrete transfer function is developed take one of the second order factors in equation (39) and replace s with $2/T \cdot (Z - 1/Z + 1)$

$$\frac{\Omega_c^2}{s^2 + 2\Omega_c \cos\frac{\pi}{5}\, s + \Omega_c^2} \rightarrow \tag{40}$$

$$\frac{\omega_c^2}{\left(\frac{2}{T}\frac{Z-1}{Z+1}\right)^2 + 2\omega_c \cos\frac{\pi}{5} \cdot \left(\frac{2}{T}\frac{Z-1}{Z+1}\right) + \omega_c^2}$$

Simplification yields a Z transfer function of the form

$$H_1(Z) = \frac{A\,(1 + Z^{-1})^2}{1 + BZ^{-1} + CZ^{-2}}$$

which can be implemented directly with delay elements (Figure 21).

It is not necessary to implement the integrator terms $T/2\ (1 + Z^{-1})/(1 - Z^{-1})$ because clearing equation (40) leaves just the delay terms with their corresponding modifiers. The complete filter is implemented by cascading the individual second order sections with the first order section.

The first order section transfer function is found and easily implemented (Figure 21).

$$\frac{\Omega_c}{S + \Omega_c} \rightarrow \frac{\omega_c}{\frac{2}{T}\left(\frac{Z-1}{Z+1}\right) + \omega_c} \tag{41a}$$

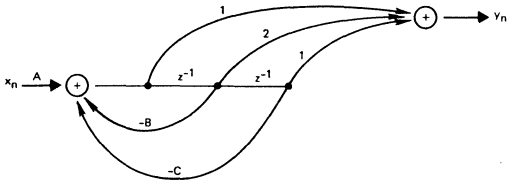

Figure 21. Canonical Form for Butterworth Second Order Section

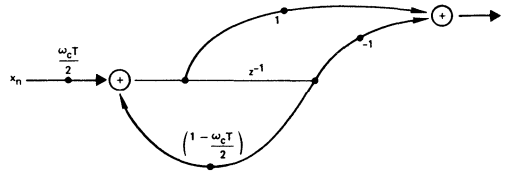

Figure 22. First Order Section

$$H(Z) = \frac{\frac{\omega_c T}{2}(Z+1)}{Z - \left(1 - \frac{\omega_c T}{2}\right)} \qquad (41b)$$

4.2 Introduction to FIR Structures

The previous section described in IIR digital filter using a discrete approximation to the analog frequency variable s. This technique follows naturally the Z transform development presented in the first section because the normalized Z transform was shown to result from the application of a sampled waveform (analog) to a continuous network. This effect resulted in replacing the derivatives of the differential equation with forward differences. The w (or bilinear) transform method uses a more complicated expression to approximate the derivative, and good filters result. This method is considered an indirect implementation because it is a mapping of an analog transfer whose form is based directly on some frequency response criteria.

Early digital filter work was based on contemporary analog theory. The realization came very early that poorly performing filters resulted when digital designs were based on simple and obvious features of analog designs (such as direct pole zero mappings into the Z plane).* As a result methods like the bilinear transform emerged as effective design techniques.

Finite impulse response digital filters are characterized by their time limited impulse responses. These filters may be implemented in the analog world through the use of LC type tapped delay lines or charge coupled delay lines. However, they are still discrete time filters in spite of their analog or semi-analog implementation. From a mathematical standpoint they have no real analog counterpart in that no expressed or implied attempt is made to simulate integrating or differentiating operators which are the elements of a true analog filter.

Practically speaking, the advantages of FIR filters cannot be truly realized because the time delay cannot be simulated in an analog fashion without some objectionable side effects. In a charge coupled device (CCD) amplitude errors accumulate as the signal propagates down the line. Noise is a problem, and limited dynamic range is attainable with currently available devices. LC delay lines (which only approximate time delay) are limited to medium frequency applications due to the large inductor capacitor sizes necessary for low frequency work. Both techniques have high frequency rolloff characteristics which make precision filter designs difficult. Time delays can be implemented in the digital machine to the accuracy of a crystal oscillator. There is no insertion loss problem, and dynamic range is dependent only on the word length of the computer (i.e., 12, 14, 16 bits).

In general IIR filters are more efficient than FIR filters. For a given order no FIR filter can achieve as sharp a transition as the best IIR filter with the same ripple error constraint. A typical FIR filter may take twice as much memory as an IIR filter with the same specification requirements.

In contrast, FIR filters are generally much easier to implement than IIR types and generally less susceptible to roundoff noise. The main feature of a FIR filter is its capability to

*Such techniques as the impulse invariant and matched Z transform methods are generally frowned upon in serious filter design applications. The reader is referred to Rabiner and Gold, "Theory and Application to Digital Signal Processing," for an in-depth discussion of these methods as well as the method of approximation by forward and backward differences.

achieve an exact linear phase response if desired. IIR filters are typified by the wild phase excursions through the transition regions which can cause severe distortion problems in image, radar, and speech processing systems.

Optimization techniques which are applied to analog and digital recursive filters can be applied successfully to nonrecursive structures to achieve very accurate approximations to a desired or ideal frequency response. Specifically, the Chebyshev criterion which minimizes the maximum error over a band of frequencies can be applied to FIR design to yield equiripple filters with the added attraction of linear phase.

To describe all the virtues and mathematical techniques behind the design of FIR filters is beyond the intent of this paper. The reader is directed to the sources named in the bibliography for the detailed research on the various design techniques. The signal flow graph for a general FIR filter is given in Figure 23.

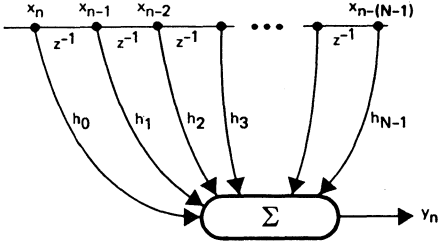

Figure 23. FIR Signal Flow Graph (z^{-1} terms represent data delays of one clock time T)

The filter output consists of input x_n and past samples x_{n-1}, x_{n-2}, ... x_{n-N} of various weights. The weights (h_0 - h_{N-1}) define the impulse response of the filter directly. Output y_n at any instant in time nT is given by equations (42a) and (42b).

$$y_n = h_o\, x_n + h_1 + h_2\, x_{n-2} + \ldots h_{N-1}\, x_{n-(N-1)} \qquad (42a)$$

$$y_n = \sum_{m=0}^{N-1} h_m\, x_{n-m} \qquad (42b)$$

Equation (42) is just the convolution sum for a finite duration impulse response with input x_n. The Z transform of h_n which relates X(z) and Y(z) is found by letting $x_n = e^{snT}$ as in Section 1. $(e^{snT})(e^{-smT}) = x_{n-m}$ and the Z transform is given in Equation (43a) and (43b).

$$\frac{Y(Z)}{X(Z)} = H(Z) = \sum_{n=0}^{N-1} h_n\, Z^{-n} \qquad (43a)$$

$$H(Z) = h_0 + h_1\, Z^{-1} + h_2\, Z^{-2} + \ldots h_{N-1}\, Z^{-(N-1)} \qquad (43b)$$

4.3 Constraints on h_n for Linear Phase

True linear phase filters have a phase function of the form

$$\phi(\omega) = \alpha\omega$$

The constraints on h_n can be indicated by examining the function in Figure 24 which is symmetric about the point t = 0. It is shown as a finite duration continuous function but may be piecewise linear or purely discrete.

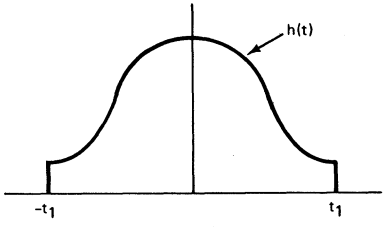

Figure 24. Symmetric Time Function

The function in Figure 25 is h(t) shifted by t_o and therefore symmetric about t_o.

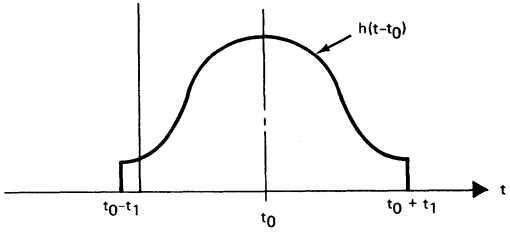

Figure 25. Shifted Symmetric Time Function

Without regard to realizability assume that $h(t-t_0)$ is the impulse response to some filter. We desire the frequency response or the network function of the filter. The Fourier transform may be used.

$$H(s)\Big|_{s=j\omega} = H(j\omega) = \int_{t_0-t_1}^{t_0+t_1} H(t - t_0)\, e^{-j\omega t}\, dt$$

Letting $\tau = t-t_0$ and with the appropriate limits gives

$$H(j\omega) = \int_{-t_1}^{t_1} h(\tau)\, e^{-j\omega t_0}\, e^{-j\omega\tau}\, d\tau \quad (44)$$

$h(\tau)$ is symmetric about $\tau = 0$ and therefore $h(\tau) = h(-\tau)$. Equation (44) can be rewritten.

$$H(j\omega) = \left[e^{-j\omega t_0}\right] \cdot \quad (45)$$

$$\left[\int_{-t_1}^{0} h(-\tau)\, e^{-j\omega\tau}\, d\tau + \int_{0}^{t1} h(\tau)\, e^{-j\omega\tau}\, d\tau\right]$$

Letting $\alpha = -\tau$ in the first integral gives

$$-\int_{t_1}^{0} h(\alpha)\, e^{j\omega\alpha}\, d\alpha = \int_{0}^{t_1} h(\tau)\, e^{+j\omega\tau} d\tau$$

With $e^{\pm j\theta}$ described as $\cos\theta \pm j \sin\theta$

$$H(j\omega) = e^{-j\omega t_0} \left[2\int_{0}^{t_1} h(\tau)\cos\omega\tau\, d\tau\right.$$

$$\left. - j\int_{0}^{t_1} h(\tau)\sin\omega\tau\, d\tau + j\int_{0}^{t_1} h(\tau)\sin\omega\tau\, d\tau\right]$$

The second and third integrals cancel each other. The first integral and a phase term $e^{-j\omega t_0}$ are left. Recall that in ganeral $H(j\omega)$ is a complex eigenvalue which modifies amplitude and imparts a pahse shift. $e^{-j\omega t_0}$ has amplitude unity and phase shift $\phi(\omega) = \omega t_0$. It is linear with ω and simply represents a constant throughput time delay of t_0 seconds. The integral

$$2\int_{0}^{t_1} h(\tau)\cos\omega\tau\, d\tau$$

is in general different for each ω but it is always a real number, and hence imparts no phase shift. Negation of the imaginary term

$$j\int_{-t_1}^{t_1} h(\tau)\sin\omega\tau\, d\tau$$

keeps the integral portion of the eigenvalue real and therefore ensures the phaseless transfer of eigenfunction $e^{j\omega t}$.

Before tabulating the purely discrete network characteristics based on these findings, the case of an antisymmetric impulse response is analyzed.

Figure 26 is a transfer function which exhibits antisymmetric behavior about $t = t_0$. Proceeding as before one finds that the real integral disappears leaving.

$$H(j\omega) = e^{-j\omega t_0} \left[-2j\int_{0}^{t_1} h(\tau)\sin\omega\tau\, d\tau\right] \quad (46)$$

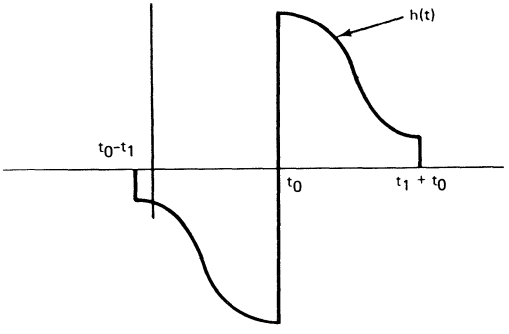

Figure 26. Antisymmetric Function

The integral is imaginary, implying an additional -90 degree phase delay added to the linear phase term.

These filters are usually considered linear phase, although strictly speaking

$\phi(\omega) = -\omega t_0 - \pi/2$ is not a linear function of ω. More accurately they are termed constant group delay filters since $d\phi/d\omega = -t_0 = \text{constant}$. Purely linear phase filters have constant group delay and constant phase delay.* These filters are used for differentiators and Hilbert transformers where a constant 90 degree pahse shift is needed.

4.4 Linear Phase Configurations for Discrete Filters

Four structures for the Nth order linear phase digital filters (Figure 23) are:

1) N odd, h_n symmetric

2) N even, h_n symmetric

3) N odd, h_n antisymmetric

4) N even, h_n antisymmetric

A case 1 configuration is shown in Figure 27. Because N is odd, h_n is symmetric about (N-1)/2; N is arbitrarily 7. If each mode were processed separately, N-1 multiplications would have to be performed. Because the impulse response is symmetric, the delay line outputs may be taken in groups of two, added together, and multiplied by the appppropriate co-efficient. Only half as many multiplications are necessary. As multiplication is usually the most time consuming operation, a significant savings in machine time can be realized.

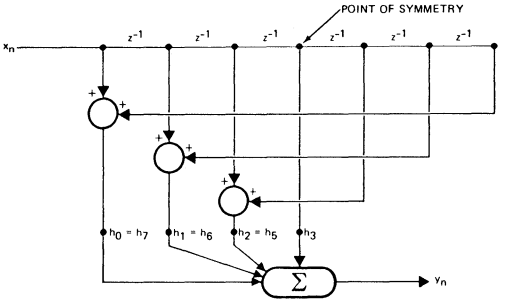

Figure 27. FIR Structure for N Odd, Symmetric Case

*Group delay is defined as the derivative of the phase function with respect to frequency ($D = d\phi(\omega)/d\omega$). Phase delay is defined as $2\pi\ \phi(\omega)/\omega$.

5.0 SUMMARY

The Z transform was introduced as the convolutional solution to a discrete time system whose input is the system eigenfunction. The derivation which was modeled after the LaPlace Transform in section one, provides an easy transition into the theory of discrete time signals. It was indicated that with the proper normalization, the Z transform becomes the LaPlace transform as the sampling rate approaches infinity. This presentation is useful in sample data control system work where it is essential to understand the effects of sampling on continuous elements.

In modeling digital filters after analog prototypes, this view point is also helpful. Such is the case with the w transform whose complex frequency variable arises from a trapezoidal approximation to continuous integration.

As signal processing tasks become progressively more challenging, the mathematical tools required to meet their demands become more powerful and complex. It is necessary for the engineer and scientist to develop a good intuitive feeling for these tools. A firm mathematical basis is therefore essential.

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Correlation ... A Powerful Technique for Digital Signal Processing

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1.0 CORRELATION THEORY

1.1 BACKGROUND

Correlation techniques are used widely in communications, instrumentation, computers, telemetry, sonar, radar, medical and other signal processing systems. Correlation has several desirable properties, including:

- The ability to detect a desired signal in the presence of noise or other signals.
- The ability to recognize specific patterns within analog or digital signals.
- The ability to measure time delays through various media, such as materials, the human body, RF paths, electronic circuits, etc.

As these properties indicate, correlation is essentially a comparison process. In fact, we use correlation daily when we compare sounds, images, or other sensations relative to other sounds, images or sensations stored in our brain. The key function of the human comparison process is to measure mentally the degree of similarity between two or more parameters. This comparison is generally made with good discrimination against extraneous forms of information and noise. The comparison can be made in real time, or we can mentally store the data until some later time.

The mental correlation process is fine where the decision-making process is not limited by time constraints. However, in electronic systems we do not usually have the luxury of performing correlation at our leisure. Correlation must be performed in real time, requiring the use of electronic circuits that are compatible with the system in question.

Electronic systems that perform correlation have been around for years, but they have been bulky and inefficient. The development of VLSI has changed this; now correlation can be performed efficiently with a minimum number of components. Before we look at some of these VLSI components, let's look at the theory behind correlation.

1.2 CORRELATION

The correlation between two functions is a measure of their similarity; loosely termed, it is a comparison process. This comparison can be expressed mathematically as the correlation between two functions $v_1(t)$ and $v_2(t)$:

$$R_{12}(\tau) \equiv \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} v_1(t)\, v_2(t+\tau)\, dt \qquad (1)$$

Here, $R_{12}(\tau)$ refers to the correlation between two signals, v_1 and v_2. It is determined by multiplying one signal, $v_1(t)$, by the other signal shifted in time, $v_2(t+\tau)$, and then taking the integral of the product. Thus, correlation involves multiplication, time shifting (or delay) and integration.

If the functions are periodic, the expression simplifies to:

$$R_{12}(\tau) = \frac{1}{T_o} \int_{-T_o/2}^{+T_o/2} v_1(t)\, v_2(t+\tau)\, dt \qquad (2)$$

where T_o is the period of the functions.

The effects of multiplication, time shifting and integration can be visualized graphically in Figure 1. This particular example shows two waveforms that have similar shapes and equal periodicity. The picture shows one particular time shift, τ_o, between $v_1(t)$ and $v_2(t+\tau_o)$. In this example, τ_o was chosen to yield a very low correlation between the two functions.

A value of τ_o selected to maximize the degree of overlap between the two functions would yield maximal correlation. As this example illustrates, the correlation of two functions is very sensitive to their relative phasing.

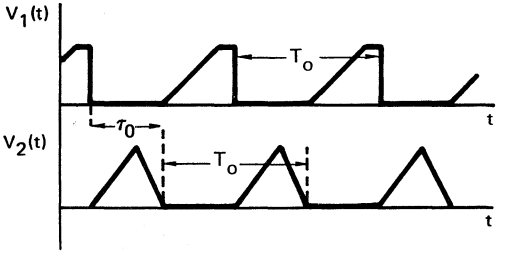


Figure 1. Two Related Waveforms. *The timing is such that the product* $v_1(t)\, v_2(t) = 0$ *for the value of* τ_o *shown.*

The correlation of a function with a time-delayed replica of itself is called autocorrelation. Thus $v_1(t) = v_2(t)$, and $R_{12}(\tau)$ becomes $R(\tau)$ and is given by:

$$R(\tau) = \frac{1}{T_o} \int_{-T_o/2}^{+T_o/2} v_1(t)\, v_1(t+\tau)\, dt \qquad (3)$$

1.3 CONVOLUTION

Closely related to correlation is the convolution of two functions, $v_1(t)$ and $v_2(t)$, which is defined as:

$$C(\tau) = \int_{-\infty}^{+\infty} v_1(t)\, v_2(\tau - t)\, dt \qquad (4)$$

Inspection of the arguments of functions v_1 and v_2 shows that correlation handles two functions "forward" in time, while convolution treats one forward and the other backward. Both procedures involve multiplying two functions together in some fashion, and then integrating the resulting product over the range of the common independent variable, "t". Mathematically, filtering involves the convolution of an input function, v(t) with the system's impulse response, h(t), yielding:

$$C(\tau) = \int_{-\infty}^{+\infty} v(t)\, h(\tau - t)\, dt \qquad (5)$$

where $C(\tau)$ is the functional output of the filter.

1.4 DIGITAL CORRELATION AND CONVOLUTION

Whereas all the functions discussed so far are continuous analog representations of physical variables, digital signal processing requires functions to be represented in discrete form, where the time scale and amplitude are quantized into discrete steps. The above integrals are changed into sums and the functions take on a finite number of discrete values. The convolution and correlation equations in discrete form become:

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)\, h(n-k)$$

and

$$R(n) = \sum_{k=-\infty}^{\infty} v_1(k)\, v_2(n+k) \qquad (6)$$

respectively. Here, the indices "k" and "n" measure out the variables denoted by "t" and "τ" in the earlier discussion. In practice, the summations will cover finite ranges of values of "k", rather than the infinite range shown here. The ranges selected will depend on the durations of the two functions and of their sampled portions, and on their periodicities (if any).

A digital correlator circuit can perform both correlation and convolution, operating according to the discrete summation equations. The remainder of this chapter describes a monolithic digital correlator that can perform digital correlation and convolution at a 20-MHz rate. Correlation and convolution will be discussed further in the other chapters, which discuss several applications of the monolithic correlator.

1.5 DIGITAL CORRELATOR

The major functions of an all-digital correlator are shown in Figure 2. A reference shift register stores the reference word, and the input word is applied to the input shift register. Both shift registers are n bits long, where "n" is any whole number. The respective bits of the two shift registers are connected to individual exclusive-NOR gates, whose outputs are applied to a summing network.

In operation, the correlator output is obtained by aligning the input word (in the shift register) relative to the reference word. The respective bits in the two shift registers are compared by the exclusive-NOR gates, whose outputs are summed. The shift registers, the exclusive-NOR gates, and the summer fulfill the three functions of correlation: time delay, multiplication, and integration, respectively.

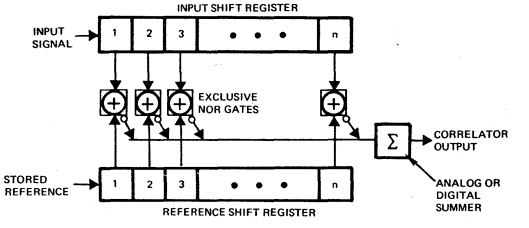


Figure 2. Basic Correlator

A new and first-of-its-kind monolithic digital correlator from TRW LSI Products is the 24-pin TDC1023J, which can perform 64-bit parallel correlation at 20 MHz. Its block diagram is shown in Figure 3.

To perform correlation with the TDC1023J, the input signal is serially shifted into the independently-clocked A-register and the reference word is serially-shifted into the independently-clocked B register. A +1 logic value at "clock R" copies the reference word from the B register into the R latch. The user can then serially load a new reference word into the B register while correlation takes place between the A register and the R latch.

Data in the A register and R latch are continually compared bit-for-bit by the exclusive-NOR gates, whose outputs are applied to the digital summer via AND gates. The output of the digital summer is a 7-bit word representing, in binary, the number of bit positions in the A register and R latch that are in agreement at any instant of time.

The M register is a 64-bit, independently-clocked mask register that permits the user to select bit positions where no comparisons are desired. This is accomplished by inserting a 64-bit serial word into the M register, with logical "0's" in the "no comparison" bit positions. Since the outputs from the M register are applied to the AND gates that also contain the outputs from the exclusive-NOR gates, masked bits are prevented from reaching the digital summer.

Either true or inverted binary outputs can be obtained from the TDC1023J through use of the INV control line, which operates on the outputs of the digital summer. The

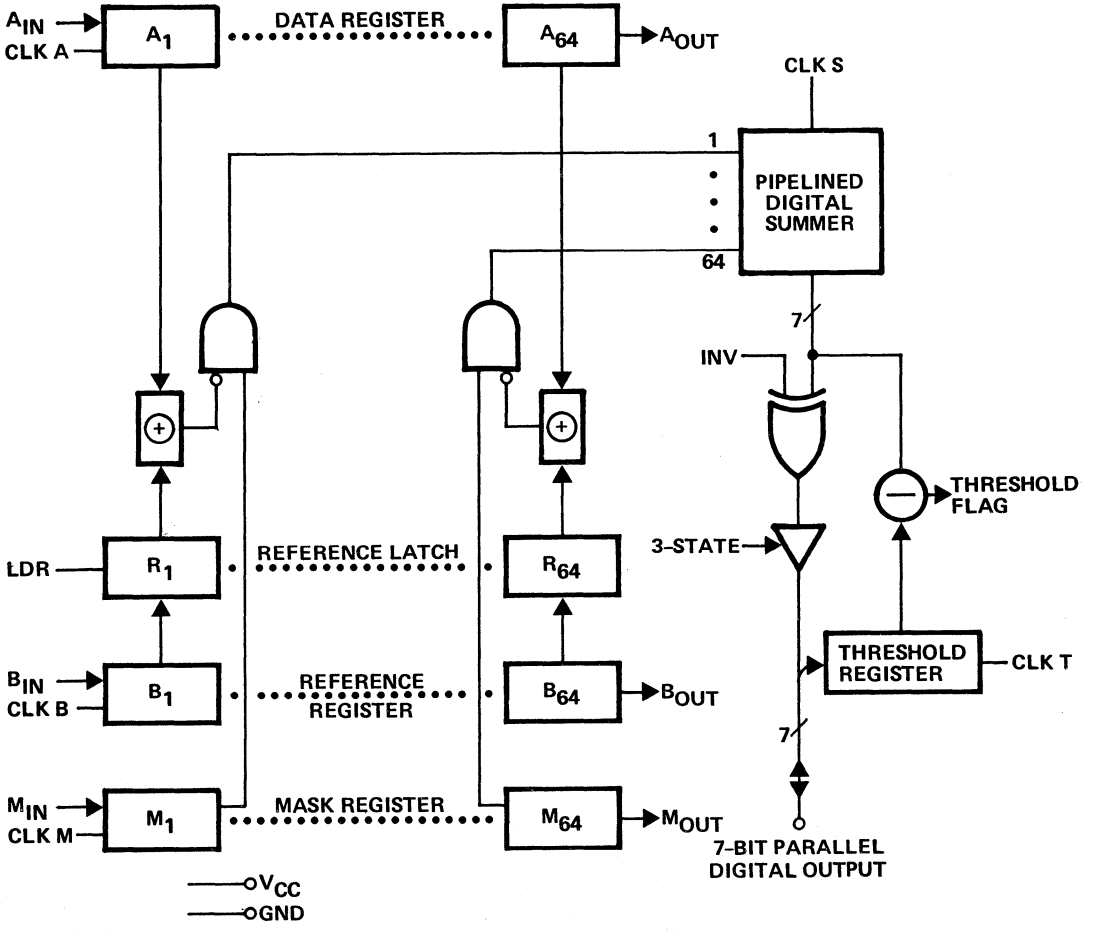


Figure 3. TDC1023J Digital Output Correlator

inverters' exclusive-OR gate outputs feed seven, 3-state output buffers controlled by signal TS. (Logical "1" on the TS disables the buffered outputs by placing them in a high impedance state.) When INV is a logical "1", the seven D_0-D_6 outputs are inverted; when INV is a logical "0", they are true.

The TDC1023J also has a 7-bit, independently-clocked T register, which is used to establish a correlation threshold. Exceeding the threshold causes a logical "1" on Flag T, the threshold flag. The threshold is set by first disabling the output buffers using the TS control line, then using outputs D_0-D_6 to parallel-load the desired threshold number into the T register. Flag T is activated when the binary number from the digital summer equals or exceeds the threshold stored in the T register.

2.0 BASIC CORRELATOR APPLICATIONS

A binary correlator compares, bit-by-bit, one sequence of binary digits against another. If these two binary sequences are derived from different sources, such as the phase patterns of a transmitted CW radar signal and its reflected return, the operation is cross-correlation. In contrast, auto correlation is the comparison of a single binary sequence against a time-shifted copy of itself. Cross-correlation applications include:

- Detection of differences (e.g., errors) between two data sequences;
- Determination of the time delay between two similar signals, such as a radar transmission and its returning reflection;
- Correction of errors in expanded-code (redundant) data streams;
- Multiplexing of data among several users;
- Recognition of specified patterns within a data stream; and
- Synchronization of a decoding process or analyzer (such as a TV receiver's scanning circuits) with an incoming data stream.

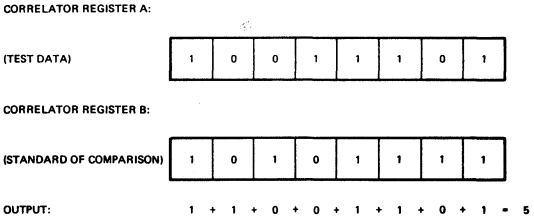
Autocorrelation is often employed to identify periodicities within a data stream, as a time-domain alternative to spectral analysis and the associated time domain – frequency domain transformations. Similarly, it can "extract" a periodic signal from its random noise background, since the signal will yield high autocorrelation levels, while the random interface will not.

The TDC1023J fits three broad classes of correlator applications:

- Direct autocorrelation or cross-correlation of non-redundant non-expanded data;
- Comparisons of expanded-code data sequences, in which extra bits have been added for error-rejecting redundancy or for other uses, such as multiplex addressing; and
- Synchronization of a receiver/analysis system with an incoming signal.

2.1 APPLICATIONS USING UNEXPANDED DATA

Many correlator applications involve comparing a given data sequence or pattern against a standard ("correct") sequence. As shown in Figure 4, when presented with two sequences of up to 64 bits each, the correlator counts the number of bits in one sequence that match the corresponding bits in the other sequence. The difference (E) between the total number of bits under comparison (N) and the correlator's output (R, the number of coincident bits) is the number of deviations (presumably errors) between the two sequences, i.e., E = N - R.



In this example, N = 8, R = 5, *and* E = 8 - 5 = 3. *The correlator's registers are filled serially with the two binary sequences shown; the correlator's output of* "5" *indicates that in* 5 *of the positions, the two sequences coincide.*

Figure 4. Correlation of a Data Sequence Against a Standard

2.1.1 Logic Analyzer

In principle, the TDC1023J correlator could be used in the automated testing of digital circuits. This trivial application is included as a tutorial example, to illustrate the correlator's function, rather than as a suggestion for a cost-effective, practical device. The other applications discussed in this paper use the correlator's unique capabilities far more efficiently. In this application the data values (logic levels) of a specified group of test points are entered serially into one of the correlator's registers. The remaining register is filled with the corresponding "correct" pattern for that device, test point(s), and test. The difference between the number of bits under comparison and the number of agreements is the number of errors detected.

Although this type of operation does not identify the exact location of a given error, it flags and counts errors rapidly and automatically. In the automatic testing of a complex device, the correlator can count agreements as they arise during a long test cycle. The resulting total number of agreements (correlation score) can be regarded as a figure of merit for the device under test. A maximum possible score throughout the test procedure indicates error-free performance. This application is suitable for assembly line testing, where parts exhibiting no errors are passed, those exhibiting one or more errors are rejected, and there is generally no need to describe or locate each error precisely.

A complication in this application is that the correlator can be loaded only with serial streams of data, whereas most test situations involve the simultaneous examination of data values at several parallel test points. Therefore, parallel-to-serial conversion of the data is often required. This requirement is a constraint primarily in high-speed multipoint testing, where the correlator's input must be rapidly multiplexed among several inputs (test points). Where higher speeds are required, two or more correlators may be employed in parallel, with each correlator monitoring a group of test points.

Since a typical TDC1023J correlator can accommodate a 20 MHz bit rate, the number of correlators required is at least N x R/20, where "N" is the number of test points to be examined and "R" is the rate at which they must be checked (in MHz).

Figure 5 is a simplified block diagram of a multiple-correlator system designed to perform high-speed error analysis of several test points simultaneously. For simplicity, a separate correlator is wired to each test point in the circuit. During the test, the sequence of data values appearing at each test point is clocked serially into the corresponding correlator's A register. At the end of the test, each correlator's output score is read.

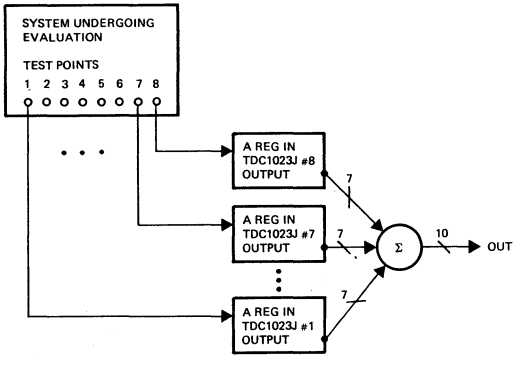


Figure 5. Multiple-Correlator Test Fixture Block Diagram

In this example, the test fixture includes a separate TDC1023J correlator for each test point. During testing, the values appearing at these test points are fed serially into the respective A register inputs. Each correlator's B register holds the "correct" pattern for its test point. When a full test sequence is stored in each A register, the correlator outputs are summed.

The TDC1023J 64-bit digital output correlator has three features that simplify actual implementation of the system in Figure 5. First, if fewer than 64 bits are required in a test sequence, the masking register can be used to select only the desired A register contents, ignoring all others. Second, the digital summer outputs and the register input and output ports facilitate serial connection of n correlators, allowing test sequences longer than 64 bits. Third, when set to the appropriate "pass" level, the threshold register will automatically activate a flag to distinguish between parts passing and failing the test sequence.

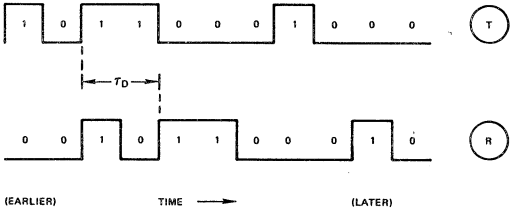
The correlator's input registers must be appropriately clocked, to ensure that they read the desired test data values, without omissions or duplications. This is particularly critical where parallel-to-serial conversion (multiplex switching) is employed to enable each correlator to evaluate several parts or test points. Furthermore, since its inputs feed directly into one-bit-wide serial shift registers, the correlator is limited to verifying high (logic "1") and low (logic "0") levels, rather than indeterminate, high-impedance, or rapidly oscillating levels. When properly timed, the correlator can process brief impulses, as long as its maximum shift rate of 20 MHz is not exceeded. Since the input register set up time is 25 nsec, each input signal must remain valid for at least this long, to ensure proper data handling. The minimum correlation clock time of 50 ns also limits the TDC1023J's real-time correlation rate to 20 MHz.

Two signals can be loaded into and across the A and B registers at a bit rate of 20 MHz for pre-correlation alignment. They can also be clocked at 20 MHz during real-time correlation, in which a correlation score is computed for each new alignment. Although the data can be re-aligned and correlated continuously at 20 MHz, the three steps of internal pipelining in the digital summation network imply that the "Nth" correlation score will be available while the "N + 3rd" alignment is being clocked into the A and B registers. The user's timing and control logic must allow for this pipelining latency period.

2.1.2 Time Delay Measurement

A simple correlator-based system can determine the time delay between two similar patterns of bits, such as a transmitted radar or sonar signal and its reflected return. In this example, the two signals appear similar in shape or bit pattern, but will exhibit a relative time shift of 2 D/C, where D is the antenna-target separation and C is

the speed of light (or the speed of sound, in sonar and ultrasound systems). Theoretically, this time delay will cause a low correlation between the two signals, even though without the delay, the two signals would correlate well. As shown in Figure 6, correlator-based time delay measurement entails gradually "eliminating" the time delay by shifting one signal with respect to the other. The highest correlation is obtained when the total shift just compensates for the original time delay between two signals. The transmitted signal can be a burst of energy which contains a particular phase or amplitude pattern, or it can be a continuous signal comprising periodic repetitions of a pattern.

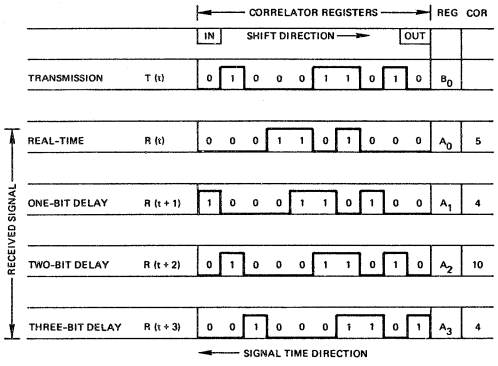


Signal "T" is the original transmission; "R" is the reflected return. In real time, R and T are separated by the time delay τ_D, which causes them to correlate poorly. Shifting R to eliminate the relative time delay will yield a high correlation. The time behaviors of both signals determine the correlation pattern. In this figure, earlier values are to the left of later ones.

Figure 6. Data Shifting for Time Delay Measurement

For time delay measurements, the TDC1023J's B register is fed the "original" signal, such as a transmitted radar (or sonar) pattern, while the A register is simultaneously filled with the (delayed) "return" signal. The two registers are clocked together, so that the time delay between the signals appears as a displacement in their relative register positions, as shown in Figure 7. After loading both registers, the system monitors the correlator output while continuing to clock the A register only. This loads progressively later return signal bits, while shifting the delayed pattern across the original pattern as in Figure 7. The number of bit shifts required for an acceptable correlation, times the signal's bit time (inverse of frequency) is the total time delay between the two signals.

For time delay measurement the transmitted code must be long and complex enough to avoid false or ambiguous alignments. For example, a code such as 101010101 would clearly be unsuitable for time delay measurement, since all shifts of 2N bits (where N = 1, 2, 3, ...) would yield high correlations, causing ambiguous results. In contrast, a code which repeats only once every 500 characters is much more likely to provide an unambiguous

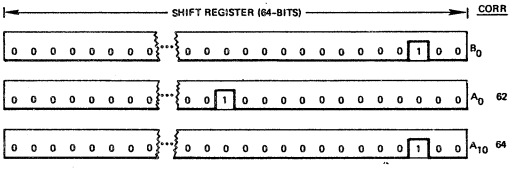


First, the original transmission and delayed reflection are loaded simultaneously into the B *and* A *registers, respectively. Next, the* B *register clock is stopped, while the* A *register clock continues to read in the return signal and shift it across the register. The highest correlation occurs when the "*A *register only" clock cycles have just compensated for the original delay between the signals.*

Figure 7. Time Delay Measurement with a Correlator

measure of any time delay of less than 500 bit times, although even this code would be unsuitable in some applications involving longer time delays.

When a nonrecurring code, such as a single burst of information, is employed in time delay measurement, the length and pattern of the transmitted code are still constrained. Under ideal circumstances where the only objective is to measure distance to a target, a simple isolated pulse, e.g., a single positive bit surrounded by negatives or zeroes, can be transmitted, as shown in Figure 8. The returning reflection of this signal contains a similar isolated pulse, delayed by the round-trip travel time between the antenna and the target. However, this is an insensitive



As in Figure 7, the original signal is loaded into the B *register. The return is clocked across the* A *register until a correlation of* 64 *is obtained. Note that the total correlation score is relatively insensitive to the imposed time delay, reaching* 64 *for perfect alignment, but* 62 *at all other times.*

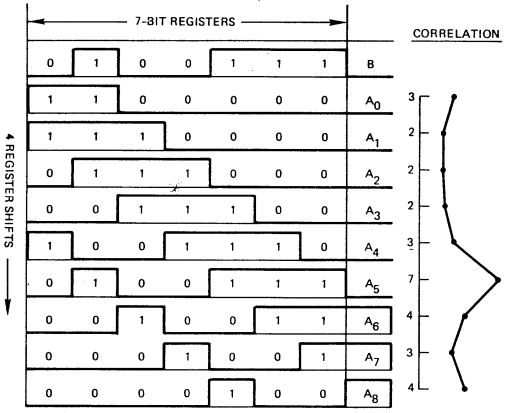
Figure 8. Single-Pulse Time-Delay Measurement

alignment test, with a total correlation score of 62/64 when the transmitted and received pulses are mis-aligned, versus 64/64 for perfect alignment.

In the presence of noise or interference, the return signal could contain one or more false positives, which could reduce the perfect-alignment correlation and generate other equally high correlations.

Longer codes are used to improve the accuracy and sensitivity of the time delay measurement, as shown in Figure 9. Here, a seven-bit "Barker code" is chosen for its low correlation with random noise and with time-shifted versions of itself. Although the longer pulse code cannot improve the 64/64 correlation score for perfect time alignment, in the presence of noise it will greatly reduce the chance of a burst of random noise causing a high correlation. For a given level of interference and concommitant bit errors, increasing the Barker code length tends to reduce the frequency and magnitude of false correlations, thereby enhancing the accuracy of the range measurement system. The interested reader can refer to the literature on Barker codes, which offer the lowest achievable error rates and highest sensitivity for these applications.

A caveat in time delay measurement is that the bit rate of the code must be high enough to permit precise measurement of the time delay, since the correlator can measure time delay only to within ±1 bit time. A higher bit rate permits a more precise determination of delay time, but increases the amount of data to be handled.



In this example, alignment within one bit time generates a significantly higher score than any other degree of relative timing between the two signals.

Figure 9. Time-Delay Measurement with a Seven-Bit Barker Code

2.1.3 Identification of Periodicities in a Data Stream

This autocorrelation application involves comparing a single data stream against a time-delayed replica of itself, in order to identify periodicities or patterns. First, as shown in Figure 10, the signal is loaded simultaneously into the A and B registers. Then, when the registers are full, the B register pattern is held stationary, while the incoming signal continues to be clocked sequentially through the A register, to simulate a steadily increasing time shift. Periodicities in the data pattern generate high correlations, which appear periodically as the A register contents slide past the B register. These correlation peaks are separated by low correlations, and the number of bits between sequential high correlations corresponds to the period of the repeating pattern. For example, the data sequence 100100100100 exhibits a high autocorrelation for every delay of 3N bit times, where N = 1, 2, 3,... .

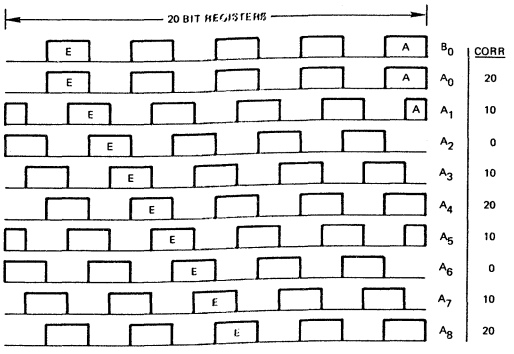
Random noise can make a periodic signal harder to detect, by reducing the contrast between the periodic correlation peaks and the low "residual" correlations between them. However, a correlator can still identify signal periodicities, in the presence of surprisingly high levels of random noise. If S(m) and S(m + n) are the original and time-shifted versions of the pure signals, and N(m) and N(m + n) are the corresponding additive noise values, then the correlator performs the following sum:

$$R(n) = \sum_{m=0}^{63} [S(m) + N(m)]\ [S(m+n) + N(m+n)] \quad (7)$$

where m and n are indices representing discrete steps in time. (In this example, the sum runs arbitrarily over 64 values only because this is the length of the TDC1023 correlator.) The function being summed comprises four terms:

S(m) . S(m + n)
N(m) . N(m + n)
S(m) . N(m + n)
N(m) . S(m + n)

Truly random noise does not correlate significantly with either S or with its time-shifted self; therefore only the term S(m) . S(m + n) contributes significantly to R, the overall sum. However, according to statistical theory, the noise products do not necessarily vanish if the summation is over a data set too short to constitute a statistically representative sample. When a short sample is considered, the noise can interfere significantly, masking the pattern of periodic high and low correlations. To handle a data sample longer than 64 bits, the user can increase the length of the summation by cascading two or more correlators in series.



The original signal is fed, in duplicate, into the A *and* B *registers, generating a perfect correlation. The* A *register copy is sequentially shifted, while the* B *register copy is held static. Periodicities in the data then cause periodic peaks in the correlation score.*

The letters "A" and "E" tag specific pulses of the signal, for the reader's convenience.

Figure 10. Autocorrelation and Signal Periodicities

2.2 EXPANDED CODE APPLICATIONS

The unexpanded data applications described in Section 2.1 involve direct use of data or data streams, without added redundancy or other expansion of the original code (pattern of bits). The following applications involve the comparison of expanded-code data streams against one another. Despite its increased length, which slows the transmission of useful information, expanded code is used for several purposes, including:

- Correction or flagging of errors;
- Multiplexing of code (when address information is included within the data stream); and
- Automatic recognition systems, which also involve incorporating address information within the data stream.

An "expanded code" is one which contains extra data bits, beyond those absolutely required to convey the information it contains. For example, since there are four possible 2-bit combinations: 00, 01, 10, and 11, up to four possible data values can be unambiguously represented by assigning each to one of these 2-bit combinations ("minimal codes"). In an expanded-code application, each of the four data values is assigned to one or more "expanded" codes longer than two bits, i.e., the original four values would be mapped into a space containing a larger number of possible values. The extra bits of an expanded code can be used either to add redundancy (for error detection) or to convey new information (such as addressing) in the data stream. Tables 1 and 2 present examples of these two types of code expansion. In Table 1, each of the four original 2-bit codes is replaced by one of four 6-bit codes, strictly to add redundancy for error protection. In Table 2, each code now bears a third bit, which assigns the coded information to one of two potential users. There is no redundancy in Table 2; every bit bears essential data or address information.

Table 1. Code Expansion for Redundancy

In this example, a single bit error in the original code will alter its meaning. In contrast, a single-bit error in the expanded code will not change its meaning, if the system can recognize the intended pattern from the five unaltered bits.

ORIGINAL CODE	EXPANDED CODE
0 0	0 0 0 0 0 0
0 1	0 1 0 1 0 1
1 0	1 0 1 0 1 0
1 1	1 1 1 1 1 1

Table 2. Code Expansion for Addressing

In this sample format, the first two bits bear the message, while the third identifies the intended receiver.

ORIGINAL MESSAGE	INTENDED RECEIVER 0	INTENDED RECEIVER 1
0 0	0 0 0	0 0 1
0 1	0 1 0	0 1 1
1 0	1 0 0	1 0 1
1 1	1 1 0	1 1 1

FORMAT:

MESSAGE	ADDRESS
X X	X

2.2.1 Error Correction

Error correction systems can operate only on expanded code, since it is data redundancy that enables them to detect and identify incorrect values. A maximum-efficiency code, such as ordinary binary numbers, can tolerate no errors. For example, if 1110 (14) is intended but 0110 (6) is sent, there is no way to determine whether the 0110 is actually a true "6" or an intended "14" or other value, with one or more erroneous bits.

However, by expanding the 16 possible 4-bit binary values into seven bits, a 7-bit "code alphabet" can be developed. A system using this expanded code can correct single errors and detect up to two simultaneous errors. With the ordinary (unexpanded) binary system, each code is separated by only one bit from its neighbor-

ing codes, such that a single 1-bit error transforms one allowable code into another, unintended code. In coding terminology, the "distance between codes" is 1 bit and the number of "tolerable simultaneous errors" is zero. Expanding from four bits to seven increases the total number of possible combinations of bits from $2^4 = 16$ to $2^7 = 128$, a factor of eight. Only 16 of these 128 codes are regarded as valid, whereas the remaining 7 x 16 = 112 codes each represent a one-bit deviation from one of the correct codes (Table 3). Since each true code is chosen to differ in at least three bits from all other correct codes, the "distance between codes" is now three bits, and each single-error code can be unambiguously associated with a particular correct code. Thus, each of the N = 16 original true values has been mapped into eight expanded codes, one representing the nominally correct expansion, the others each containing a single error in one of the seven bit positions of the expanded code. In this case, since the distance between adjacent codes is three bits, the system can positively identify and correct 1-bit errors. The system can detect 2-bit errors, but cannot distinguish between these and other single-bit errors.

Table 3. Seven-Bit Expansion of a 4-Bit Code

Note that the last four bits of each expanded code are merely the original four-bit code. Furthermore, if four-bit code "A" is the inverse of four-bit code "B," then their seven-bit expansions will exhibit the same inverse relationship.

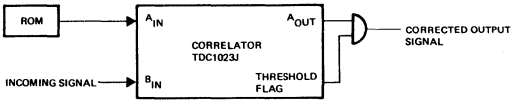
ORIGINAL	EXPANDED
0 0 0 0	0 0 0 0 0 0 0
0 0 0 1	0 1 1 0 0 0 1
0 0 1 0	1 1 0 0 0 1 0
0 0 1 1	1 0 1 0 0 1 1
0 1 0 0	1 1 1 0 1 0 0
0 1 0 1	1 0 0 0 1 0 1
0 1 1 0	0 0 1 0 1 1 0
0 1 1 1	0 1 0 0 1 1 1
1 0 0 0	1 0 1 1 0 0 0
1 0 0 1	1 1 0 1 0 0 1
1 0 1 0	0 1 1 1 0 1 0
1 0 1 1	0 0 0 1 0 1 1
1 1 0 0	0 1 0 1 1 0 0
1 1 0 1	0 0 1 1 1 0 1
1 1 1 0	1 0 0 1 1 1 0
1 1 1 1	1 1 1 1 1 1 1

Correlator-Based Error Correction System

An error-correction system can be designed with the TDC1023J correlator (Figure 11). In the 7-bit expanded code example, the correlator is set to compare seven consecutive bits of incoming signal sequentially against the 16 "correct" 7-bit codes. This is accomplished by reading seven signal bits into the correlator's B register, and then clocking in the first trial 7-bit "correct" code from a memory. If a low correlation is obtained, i.e., if fewer than six of the signal bits agree with their "paradigm" counterparts, then the next code is loaded into the register. If the second pattern also fails to produce a correlation score of 6/7 or 7/7, then the third pattern is loaded in, and the process continues until a correlation of 7 or 6 is obtained, presumably corresponding to a match (or near-match) between the correct code and the signal. When this high correlation is obtained, the correct code value (from the memory) is sent to the system output. If the correlation score is a perfect 7, the output will equal the input, with no change. In contrast, if the correlation score is 6, the output will be the error-free intended code, even though the input contained a 1-bit error. In this example, the correlator's output threshold level is set to 6, to flag only perfect and near-perfect correlations.

The threshold flag can also be used to restart the B register clock, if desired. This system can operate at a fixed rate, clocking in a new data word after each full cycle through all ROM combinations, or a new data word can be clocked in as soon as a high correlation is reached, effectively "short-cycling" the system. The TDC1023's unique architecture, with the serial A and B registers, plus the R latch, accommodates high-speed operation, by permitting the user to load each new data sample into the B register while the previous sample (in the R Latch) is compared sequentially against the paradigms being shifted across the A register.

This system must be modified for high-error rate applications. As described, it yields the wrong output when fed a code containing two errors, since any two-error version of a code is indistinguishable from a one-error version of another code. Thus, given correct codes of A = 1100110 and B = 0010110, a two-error version of



The incoming signal is loaded into the B *register, while the first paradigm code is loaded into the* A *register. If the resulting correlation is high, the threshold flag opens the output* (AND) *gate, sending out the correct code from* A_{OUT}. *If the correlation is too low, the next code is loaded in, etc., until a high correlation results.*

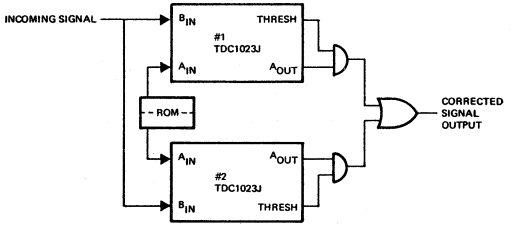
Figure 11. Correlator-Based Error Correction System

Application Notes

code A, e.g., 0000110, is indistinguishable from one single-error version of B, 0000110. The correlator mistakenly identifies the two-error A code as a one-error B code, and put out a false B code as its interpretation of the true data value. If a relatively high error rate is anticipated, then an even longer code expansion must be employed to increase the system's error tolerance. Using a carefully designed enhanced code, double, triple, or higher order errors can be accurately corrected. The maximum number of simultaneous errors that can be corrected is always less than half of the distance (number of bit changes) between codes. Since longer codes imply slower transmission of useful information, there is an obvious tradeoff between a code's efficiency and its error tolerance.

One disadvantage of correlator-based error correction is that the correlator must run through numerous comparisons for each segment of incoming signal code. With a 16-combination, 7-bit code, the correlator must compare the incoming data stream against each of 16 stored combinations.

Since each pattern is seven bits long, up to 7 x 16 = 112 clock cycles are required to test each 7-bit segment of incoming code. Thus, in this example the maximum permissible bit rate for incoming information is 1/16 of the correlator's maximum bit shift rate. If higher data handling speed is required, the incoming data stream can be fed into two or more correlators simultaneously (Figure 12). If two correlators are used, each correlates the incoming data segment against only half of the possible true values from the memory. When one correlator "finds" an acceptable high level of correlation between the data stream and one of its stored paradigm patterns, it then feeds the contents of its comparison register serially into the output.



Each correlator is fed paradigms from half of the ROM. *Since both operate simultaneously, the system speed is twice that of the single-*ROM *system. When one correlator finds a high correlation, its threshold flag allows its "A" register to feed through to the output. Since the correlator's output remains disabled, only the desired code reaches the output. Additional correlators will further increase the error correction system's speed, to a hardware-intensive, maximum-speed configuration of one correlator per paradigm pattern.*

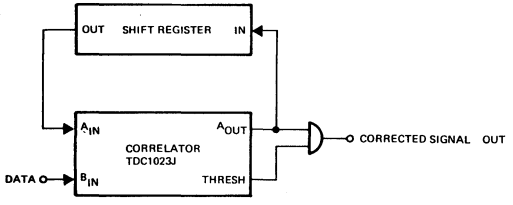
Figure 12. Higher Speed Error Correction System

The structure of the TDC1023J correlator suggests that the A register should be used for the paradigm patterns from the memory while the B register (and therefore the R latch) should hold the segmented incoming data stream. This configuration facilitates relatively rapid and efficient rotation of paradigms through the device. The error correction system concept must be augmented slightly to enable the TRW correlator to accommodate various data word lengths. If the desired word length is 64 bits, then the concept functions directly, as described, i.e., a test pattern is read into the comparison register during the 64 clock cycles, then compared against the stored 64-bit signal sample. If a high (greater than threshold) correlation is obtained, this register is then serially emptied into the desired output, for use by the remainder of the system. In contrast, if a shorter word length is used, then at each instant, the 64-bit correlator contains both the desired N-bit pattern and 64-N other bits irrelevant to the correlation. In this case, the simplest solution is to program the masking register to ignore the first (64-N) bits in computing the correlations, so that only the last N bits in the register are then compared to the incoming word sample. When a high correlation is obtained, the correct signal is in the last N positions of the paradigm register and can be shifted out serially. Although the test patterns can be read sequentially into the A register, without any spacing or delineation between words, synchronization data must be provided to tell the correlator when each new word is in position for testing. Otherwise, a chance agreement between an incoming signal segment and mis-synchronized pieces of two sequential paradigm codes will cause the output of an unwanted code.

In the actual system implementation, the paradigm codes can be read directly from a random-access memory (RAM), or they can be pipelined through a long shift register or a first-in/first-out stack (FIFO), depending on system timing requirements.

If the same fixed set of codes is always used, then a read-only memory (ROM) can be employed as the primary storage device. The only major requirement is that the correlator output be read only when one of the paradigm patterns is lined up exactly in the proper bit positions of the correlator's comparison register. Figure 13 illustrates a simple system in which a single shift register holds the paradigm codes. In this example, the contents of the external shift register and the correlator's A register are recirculated word-by-word, under control of the system clock. The A register's output is connected to the rest of the system when the threshold flag goes high.

The preceding discussion assumes that the incoming data stream is word-synchronized, i.e., that the receiver knows when each new 7-bit incoming data word starts and when it ends. A lack of synchronization leads to ambiguous or erroneous interpretation of the message.



In this application, the paradigm codes recirculate sequentially between the external register and the correlator's A *register. When a high level of correlation is obtained, the resulting threshold flag connects the* A *register output pin to the remainder of the system.*

Figure 13. Error Correction System Using a Correlator and a Shift Register

For example, if an incoming sequence is . . . 110011001 . . . and we know only that it comprises 2-bit words, there is no way to tell whether the actual message is . . . 11, 00, 11, 00. . . or . . . 10, 01, 10, 01 . . . Chapter 4 describes how a second correlator can be used to synchronize the receiver/analysis system with the incoming data.

ROM- (or RAM)-Based Error Correction

An alternative to correlator-based error correction is a ROM-based system in which each word of the incoming message is interpreted as a ROM address. The ROM contents corresponding to that address are then sent to the next portion of the system. In a ROM-based error correction system, several addresses, each representing a different error, contain the same correct data sequence. In this way, each of several slightly erroneous data sequences is mapped into the corresponding correct sequence.

The principal disadvantage of the ROM-based error correction system is that it requires a far larger ROM than does the correlator-based system. An error correction system for the previously-described 7-bit expanded code requires eight memory locations for each of the 16 correct codes . . . a total of 128 words. In contrast, the correlator-based system requires only one 7-bit word memory location for each of the 16 codes. In this case no ROM is needed. Instead, the 16 words can be stored sequentially in a shift register and shifted through the correlator and back to the shift register under control of the system clock (Figure 13). The speed of the ROM-based system is limited by the system's memory access time, whereas the speed of the correlator-based system depends primarily on the shift and correlation rates of the correlator.

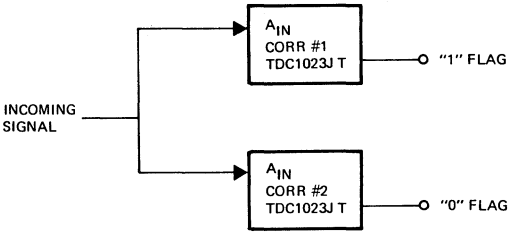
2.2.2 Interference Reduction

Code expansion can also be used to correct data errors encountered by a receiver in a high-noise or high-interference environment. In this case, the basic principle again is to add extra (redundant) bits to a message, thereby enhancing the error-tolerance of the system. For example, a specific 64-bit code can be assigned to the binary value "1" and the complement of this code to "0". Then, instead of a simple sequence of ones and zeroes, a much longer serial sequence can be transmitted that consists of the desired combination of expanded codes for "1" and "0". The resulting message contains the intended information, plus redundancy, which permits detection of errors in the transmission or reception of the data. The receiver can use two correlators, one holding the code for a "1", the other a "0", to reconstruct the intended message. Then, whenever an expanded code version of a one or zero is received, the appropriate correlator sends a "1" or "0" message to the output, from whence it can be fed to the remainder of the receiver system.

Figure 14 is a block diagram of such a system, showing the technique by which the appropriate "1" and "0" codes are to be sent. This basic technique can also be applied to a multiplexing system with multiple users, as discussed in the following section.

2.2.3 Code Multiplexing

The standard system of a time-division code multiplexing, which gives multiple users access to a single information transmission channel, involves a fixed-speed multiplexing switch that transfers the channel from user to user in a preset sequence. This system is somewhat inflexible: each user receives a fixed percentage use of the system. The TDC1023J correlator makes possible a flexible time sharing system, which adapts its switching rate and sequence according to the immediate needs of each user. Addressing information containing the intended receiver's unique code is attached as a prefix to each message. Each user has a correlator, one register of



The B *register of correlator #1 holds the expanded code for the message "1," while the* B *register of correlator #2 holds the expanded code for "0." If correlator #1 recognizes the expanded "1" code in the data stream, its threshold flag will go high. Conversely, an expanded "0" code will produce a high threshold flag from correlator #2.*

Figure 14. Interference Reduction System-Decoder

which is preloaded with the corresponding address code. When a user's correlator registers the proper address sequence, it switches the intended receiver from "standby" to "receive" mode. This addressing information ensures that the appropriate user(s) receive the correct information, which the other users ignore. If the next message is to be sent to a different user, it is preceded by his unique address code, which can be read only by his correlation receiver system. Each message, irrespective of its "audience", is terminated by a standard "end of message" code, which returns all receivers to "standby" to prevent them from reading messages immediately following their own.

In this system, useful information can be sent over the single transmission channel a large percentage of time. The only overhead information, the address/start-of-message and end-of-message flags, are sent periodically as the need arises. The percentage of "air time" occupied by these start and end codes is a function of the length of the individual messages being sent. The more frequently the channel must be switched from one receiver to another, the greater the percentage of air time that must be "wasted" on addressing and stop codes, and is therefore unavailable for the transmission of useful information.

An alternative system involves separate encoding of "1's" and "0's" for each user, as discussed in the previous section. Figure 15 compares the two coding formats. Unfortunately, separate encoding requires considerably greater code expansion, since every bit of useful information must be expanded into a sequence of several bits. However, this system is efficient for short messages, which involve frequent shifting from receiver to receiver. In this case, the separate "start of message/address" codes would occupy an unacceptably high percentage of the available message time. The choice between the "start-of-message" format and the "bit-by-bit" format depends heavily on the intended lengths of messages and the number of users of the system. Slower switching and longer messages tend to favor the "beginning of message" format, while shorter messages, frequently

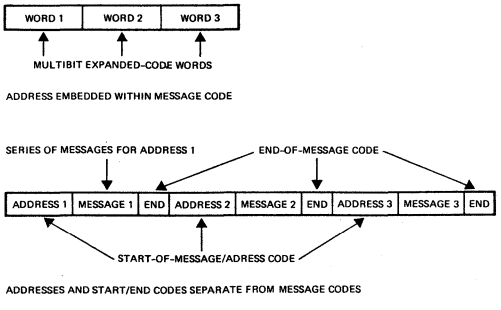


Figure 15. Alternative Coding Formats for Code Multiplex

switched, may favor the "bit-by-bit" format. If accurate word synchronization cannot be maintained over time, then the "beginning of message" format is recommended, since the "start message" codes can reset word synchronization. Synchronization is discussed in the next section.

A variation on the multiplexing theme is the automatic recognition system, in which the TDC1023J correlator's B register is preloaded with a key code. Whenever this key appears in the data stream (and therefore in the A register), the resulting high correlation score is used to energize a specific device. For example, in a remote warning system, the transmitter can send a key code each time a local emergency arises. At the receiver, the correlator's threshold flag is wired to turn on an alarm, which announces the emergency at the remote (transmitter) site. Only correlators that are programmed with this key code can cause the alarm to ring.

2.2.4 Use of the A and B Registers

Many cross-correlation applications involve the correlation of a data stream against a fixed pattern or a series of fixed patterns. In some cases, it is possible to leave a single fixed pattern in one register while clocking prestored or real time data through the other, as in the interference reduction and data multiplex of Sections 2.2.4 and 2.2.5. In other applications, however, it is more convenient to hold a data sample in one register while shifting a series of paradigm patterns through the other, as in the error correction applications of Section 2.1.

The TDC1023J correlator has been designed to accommodate all of these applications efficiently. Its A register is directly accessible for continuous input and shifting of data. In contrast, the R latch is parallel loaded from the B register, to permit "batched" changes of the entire 64-bit pattern. Holding its clock at a logical "1" puts the R latch into a transparent mode, in which its contents match and shift with those of the B register. Holding the R clock at a logical "0" permits the user to preload the B register with the next pattern while the A and R register patterns are being correlated. After the "current" A and R patterns have been correlated, a rising edge at CLOCK R replaces the R register's contents with those of the B register.

3.0 SYNCHRONIZATION

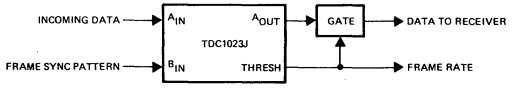
Synchronization is one of the most common uses of the TDC1023J correlator. In fact, many of the previous correlator applications require an additional correlator to maintain synchronization between the incoming data stream and the analytical system. Synchronization operations include frame synchronization, in which the correlator identifies the start of each new frame (or major group) of information; word synchronization, in which

the beginnings of individual data words are detected; and bit synchronization, involving the alignment of individual bits of incoming information with the receiver's bit-by-bit clock. The correlator is probably best suited to frame synchronization, although its use in word or even bit synchronization will also be described. The frame and word synchronization discussions immediately following tell how to establish and maintain frame and word synchronization if the bit rate is known, i.e., if bit synchronization can be assumed. These techniques are useful in situations where the data transmission (bit) rate is known and invariant, where the receiver's clock is triggered by the transmitter's or where the "receiver and transmitter" are part of the same system. In the more general case, to be discussed in Section 3.3, the receiver's clock is periodically retuned to maintain adequate bit synchronization, without which the data cannot be handled properly.

3.1 FRAME SYNCHRONIZATION

In general, a system can achieve and maintain frame synchronization only if the incoming data stream is interrupted periodically by a specific "start-of-frame" pattern. This pattern, transmitted at the beginning of each new frame, tells the receiver that a new frame will immediately enter the input register and must be handled accordingly. For example, in a video system, the "start-of-frame" pattern tells the receiver to return its scan to the beginning position, in preparation for the new picture (frame) that will follow the "start-of-frame" pattern. In a non-video data application, such as a data filing system, the "frame sync" pattern could denote the beginning of a new group of data, such as the data file for a particular individual.

In a frame synchronization system, one register (usually the B register of the TDC1023J) is pre-loaded with the standard synchronization pattern, while the incoming data stream is shifted serially through the other (A) register (Figure 16). When a frame sync pattern embedded in the incoming data stream aligns exactly with the stored sync pattern, the correlator's threshold flag reaches a logical "1", which in turn tells the receiver to start handling a new frame of data. The special start-of-frame pattern must be long and unusual to prevent false synchronization, which occurs when the correlator finds and locks onto a portion of the data stream resembling the desired synchronization pattern. The longer the sync pattern, the lower the chance of a false synchronization, but the larger the percentage of the total data stream that must be dedicated to synchronization and hence is unavailable for transmitting useful information.



In this application, the B *register is loaded with the frame sync pattern, so that each occurrence of a frame sync pattern within the data stream causes the threshold flag to go high. A train of pulses, spaced at the frame rate, appears at the correlator's threshold output.*

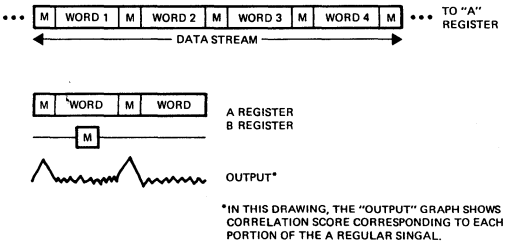
The optional gate is closed when the system is first activated, but is opened by the first threshold pulse from the correlator's output.

Figure 16. Frame Synchronizer System

The receiver-correlator system operates continuously, with the correlator producing a high threshold flag as it receives each successive frame sync pattern in the incoming data stream. The rate at which these high outputs are generated is the frame rate of the incoming data. As long as its scanning system (or data filing system, etc.) is reset at this rate, the receiver remains synchronized with the incoming data and continues to distinguish one frame or group of data from the next.

3.2 WORD SYNCHRONIZATION

When presented with a data stream comprising a series of individual words, a system must be able to decide where one word ends and the next begins, to facilitate accurate use of the data. One obvious technique for separating the words in a continuous bit stream is to insert a "start of word" marker pattern at the end of each word, before the start of the following word, as shown in Figure 17. If a correlator in the receiver system is programmed to identify this marker, it puts out a high correlation value whenever it encounters "start of word" in the incoming data stream. If the data word vocabulary and "start of word" marker code are carefully selected, the correlator's output reaches isolated high values at the word rate, with much lower correlation levels between



In this example, the data (words 1, 2, ...) *and the identical* "start of word" *markers* ("M") *are transmitted as a continuous series of pulses. Ideally, the marker is a fixed sequence of bits which never occurs within the data stream. Whenever a marker in the data stream passes the marker stored in the* B *register, a spike is generated in the output.*

Figure 17. "Start of Word" Marker Code

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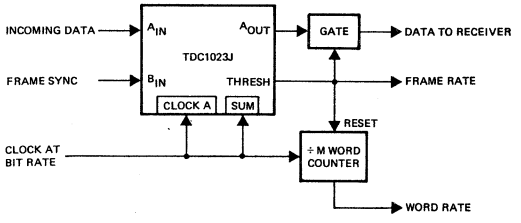
these spikes. If the signal processing system is programmed to begin handling a new word at each correlator spike, it remains word-synchronized with the incoming data and successfully distinguishes between individual incoming words.

The "start of word" marker code must be carefully selected to minimize the possibility of false triggering of the correlator by data or noise, rather than by a true sync pattern. The reader interested in selecting low-error sync patterns is referred to in the literature on shift register sequences, Barker codes, and spread spectrum signal theory, including Shift Register Sequences (S.W. Golomb, 1965) and Introduction to Communication Systems (F.G. Stremler, 1977). Most low-error sync patterns are "pseudo random noise" (PRN) sequences, which are chosen to correlate poorly with most likely data sequences. For example, a PRN sequence must contain roughly equal numbers of "1's" and "0's" to avoid high correlations with the data sequences, ". . . 000 . . ." and ". . . 11111 . . .". The length of the selected sync code represents a compromise between high efficiency, which requires a short correlation time, and low error rate, which requires a longer correlation time.

Although the preceding procedure can yield accurate word synchronization, it is inefficient if the markers occupy a significant percentage of the total data stream. Clearly, if the number or length of the markers can be reduced, then more useful data can be sent. If the data words are organized into fixed-length frames, and a frame sync marker pattern (Section 3.1) is provided, it is easy to derive word synchronization from frame synchronization. If there are always N words per frame, then the word rate is N times the frame rate. The frame-rate output spikes of the frame sync correlator can be frequency-multiplied upward to produce the needed word-sync spikes. Given a fixed word length, word synchronization can be established and maintained with a recirculating counter, operating at modulo n, where "n" is the number of bits per word. In this case (Figure 18), the



In this system, word length is a constant "n," and the counter therefore puts out a "start new word" spike at every nth clock pulse (therefore every nth bit). The frame pulses reset the counter, to reestablish word sync at the start of each frame.

Figure 18. Derivation of Word Sync from Frame Sync

counter is reset at each frame pulse, after which it continues to cycle through its states, returning to its "word start" position every n cycles. If it abruptly shifts or gradually drifts out of word synchronization, the counter readjusts automatically at the start of the next frame.

3.3 BIT SYNCHRONIZATION

The preceding discussion assumed that the transmitter's and receiver's clocks were synchronized, i.e., that each pulse of the receiver's clock would load in the data bit immediately following the one loaded on the previous clock cycle. As illustrated in Figure 19, if the transmitter clock runs faster than the receiver clock, the receiver will periodically miss a data bit of the message. In contrast, a fast receiver clock occasionally loads a single bit twice in succession. These "missed-bit" and "doubled-bit" errors can be avoided only if the two clocks are synchronized.

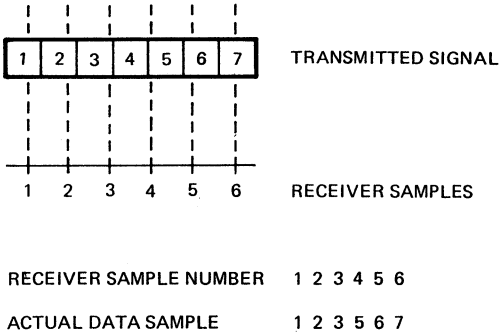
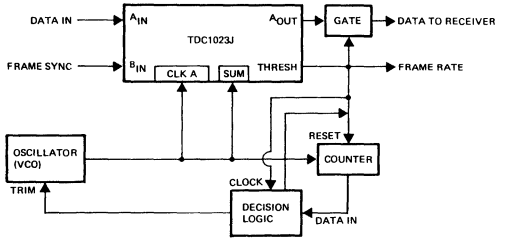


Figure 19. Loss of One Message Bit Due to a Slow Receiver Clock

In many transmit-receive systems, the receiver clock requires only minor periodic adjustments to maintain synchronism with the transmitter clock. As long as the two clocks are nearly synchronized at all times, the frame sync pulses are strong and regular, providing a periodic signal from which word and bit synchronization can be derived, as needed. Figure 20 shows how a correlator and a bit counter can be used to derive bit sync from the frame sync. The system continually readjusts the receiver's oscillator rate according to the number of bits received between frame sync patterns. For example, if the receiver identifies two frame pulses 1023 received bits apart, while the actual separation is 1024 transmitted bits, then the receiver clock, running too slowly, has missed one data bit. Since only 1023 receiver clock cycles have occurred in a time span intended for 1024, the receiver's clock rate must be multiplied by 1024 ÷ 1023 for the next frame of data. A typical clock and clock-adjustment hardware system comprises a voltage controlled oscillator, a counter, a digital-to-analog converter, and a simple voltage match-



The frame sync pulse tells the controller ("decision logic") *to read the counter and adjust the oscillator rate accordingly, i.e., if the count is too low, then the oscillator is to be accelerated. The controller must also reset the counter for the next frame of data.*

Figure 20. Bit Synchronizing System

ing circuit. In this simple servo system, the number of bits between frame sync pulses is counted and converted to a voltage, which is used to readjust the clock rate. If the number of receiver frame bits is smaller than the standard transmitted frame length, the clock is accelerated proportionately.

This synchronization system has several limitations, including:

- It can determine synchronization only to within ±1 bit time per frame. Given a frame length of N bits, this is a timing precision of 100%/N.
- It is applicable only to signals for which the data bits occupy a large percentage of the available time, i.e., signals with short inter-bit transition times. It would not be suitable for a "Morse Code"-like signal comprising a series of spaced impulses.
- As described, it cannot establish correct phasing between the incoming bit stream and the receiver. This is not a serious limitation for signals with short interpulse intervals, for which the receiver can clock in each data bit anytime during its valid state, i.e., at any phase within a fairly broad range.
- It is only applicable to signals whose frame size either is fixed or varies according to a pattern known to the receiver. Otherwise, the receiver's oscillator interprets variations in the frame length as though they are variations in the bit transmission rate, leading to synchronization errors.
- The signal used must include periodic frame sync patterns to "prompt" the correlator.
- The bit rate of the signal should be very stable, changing by less than one bit time per frame interval. Every rate change exceeding one bit per frame causes either a missed or an extra bit to appear at the receiver, and continuous high-speed change causes a steady stream of errors, in which the receiver either misses a bit or loads a single bit twice.

4.0 MULTIPLE CORRELATOR APPLICATIONS

Although a single TDC1023J correlator can handle only 64-bit-long sequences of single-bit data, several correlators can be connected in series to handle longer sequences. Similarly, several correlators can be connected in parallel to handle word widths of two or more bits. Finally, the correlator can be used with appropriate A to D converters to build an analog correlation system. This chapter outlines procedures for serial, parallel and analog extensions of the basic correlator circuit.

4.1 SERIAL CONNECTIONS FOR SEQUENCES OVER 64-BITS LONG

An extended-length correlator can be designed to handle data sequences 64N bits long, with N correlator IC's. First, as shown in Figure 21, the three input registers (A, B, and M) are connected serially, such that the A output of the first correlator directly feeds the A input of the second, etc. The corresponding register clocks of all correlators in the string are tied together to provide three master clock connections, A, B, and M. To this point, serial connection of the correlators is identical to serial connection of 3 x 64 shift registers. If the TDC1023J digital output correlator is used, the R clocks must also be tied together and an external digital summing

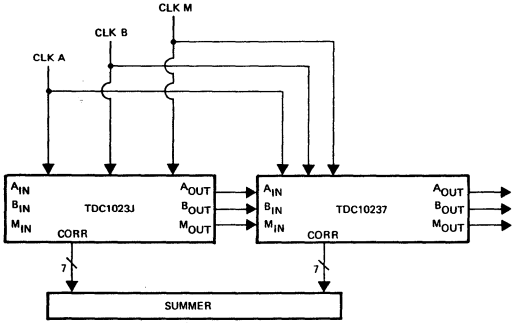


Figure 21. Serial Connection of Correlators for Long Data Strings

circuit must be provided to add the outputs of the individual correlators, thereby computing the total number of A - B bit agreements encountered within the string of correlators.

Serial connection of multiple correlators produces an efficient extended-length correlator with all of the original correlator features except output threshold flagging, which can be added to the external summing circuit, if needed. The external addition circuitry can be simplified somewhat by operating the TDC1023J as a 63-bit correlator, i.e., by masking one bit position. In this configuration, the most significant bit (MSB) of each correlator's output can be ignored.

The serial correlator systems depicted in Figure 21 also requires clock signals for the summing network in the correlators and for the external summing network. These clocks must be carefully phased to ensure that the external summer operates on valid correlation scores from the correlators. The separation of summing and shifting clock connections on the TDC1023J permits the user to shift the data through the comparison registers at 20 MHz, with or without simultaneous computation of the correlation sums.

4.2 PARALLEL CONNECTIONS FOR ANALOG OR MULTI-BIT WORDS

Many applications require correlations between multi-bit functions, instead of the simple bit streams discussed above. To handle multi-bit information, correlators are cascaded in parallel, just as parallel configurations of serial shift registers are used to store multi-bit information.

There are two principal hardware architectures for parallel cascading of correlators. The simpler of the two permits correlation between a multi-bit or analog signal and a single-bit binary standard, whereas the more complex scheme is used to correlate two multi-bit or analog functions. Chapter 5 tells how to modify the latter procedure to convolve two multi-bit or analog functions.

4.2.1 Positive/Negative Vs One/Zero Correlation

Single-bit and multi-bit correlation and convolution involve the multiplication of two functions, followed by summation of the resulting products. Depending on the application, the user requires either positive/negative (XNOR, exclusive-NOR) or one/zero (AND) multiplication logic, as depicted in Table 4. The XNOR logic is used where the two signal levels, "1" and "0", are to be handled as +1 and -1, respectively. There is also the type of logic required for comparison, since it produces a "1" whenever two corresponding bits agree and a "0" when they don't. The AND logic is appropriate in most multi-bit applications and in all cases in which the two "1" and "0" signal levels are to be interpreted at face value. This logic represents ordinary arithmetic multiplication.

Table 4. Optional Correlator Logic Structures

XNOR LOGIC – POSITIVE/NEGATIVE MULTIPLICATION OF "A" AND "B" REGISTERS

		A	
	M = 1	1	0
B	1	1	0
	0	0	1

AND LOGIC – ONE/ZERO MULTIPLICATION OF "A" AND "M" REGISTERS

		A	
	B = 1	1	0
M	1	1	0
	0	0	0

As shown in Table 5, the user can select XNOR multiplication logic by loading the two data streams into the A and B registers of the TDC1023J and filling all desired correlation positions of the M register with "1." For AND logic, the data streams are loaded into the A and M registers and the B register is filled with "1's." Selective masking of bit positions is not possible with AND logic. Note that correlation actually is between latch R and register A. Holding clock R high provides direct user access to latch R, by making its contents track those of register B.

The single-bit application outlined in Section 4.2.2 requires XNOR logic, whereas the multi-bit/multi-bit applications of Section 4.2.3 and Chapter 5 are based on AND logic. As discussed above, the AND logic is for

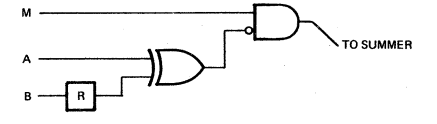
Table 5. Correlator Truth Table

Note that only the TDC1023J *digital output correlator includes the* R *latch which is parallel-loaded from the* B *register. The two basic operating modes are* A XNOR R, *enabled by mask* "M," *and* A AND M, *with* R = 1.

OVERALL LOGIC

REGISTER VALUE			BIT
M	A	B	OUTPUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

CORRELATOR LOGIC DIAGRAM



"1's" and "0's" (standard binary digits), whereas the XNOR logic is for positive and negatives or for comparisons of signals.

4.2.2 Correlation Between an Analog Signal and a Single-Bit Standard

In the presence of interference, a single-bit transmitted signal comprising a series of "1's" and "0's" may be received as a series of analog levels, as depicted in Figure 22. In this example, the noise and interference seen by the receiver have added randomly to the intended signal level, reducing or even eliminating the distinction between the "1's" and "0's". As the amount of noise increases, so does the probability of misinterpreting one or more data values.

One common way to handle the problem of additive noise is to quantize the incoming signal to 1 bit, by establishing a threshold halfway between the signal levels that would correspond to "1" (full scale) and "0". Every signal value exceeding this threshold is considered to be a "1", whereas every sub-threshold level is declared to be a "0". If the desired signal pattern is loaded into the B register and the 1 bit quantized incoming data sequence is fed through the A register, the correlator's output approximates the true correlation between the two patterns. This procedure is acceptable in low-noise applications where midscale (ambiguous) values are rare, but it can be unacceptably error-prone at higher noise levels. Its main limitation is that it assigns equal weighting to all received samples, whether they are near an extreme (and therefore very reliable) or near the midscale threshold (and therefore very unreliable). The further a signal level is from midscale, the more certain its true value. Therefore, a signal of 95% of full intensity (where 0% is a "0" and 100% is a "1") carries more information than one of 55%, even though both would be declared "1's". The architecture discussed next addresses this problem directly.

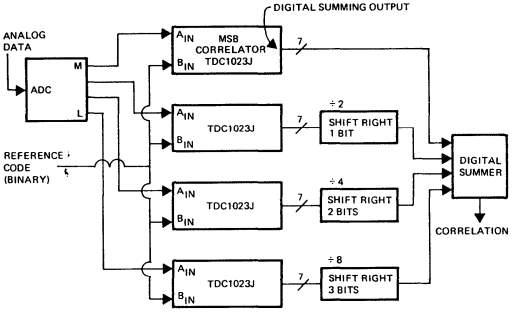
Instead of quantizing the incoming signal merely to a "1" or "0" (1-bit) value, an analog-to-digital converter can be used to quantize it to a precision of four (or more) bits. Although the resulting 4-bit word is not readily handled by a single correlator, it can be fed to four correlators, wired in parallel, as in Figure 23. As the figure suggests, each correlator handles a specific bit position of the incoming digitized signal. The dividers between the correlator's outputs and the summing network apply appropriate binary weighting, reflecting the relative importances of the correlation scores for the various bits. With the system illustrated, a true zero (A/D output "0000") or full scale (A/D output "1111") input signal which matched its B-register paradigm "0" or "1" causes outputs of "1" from all four correlators, producing a final weighted sum of 1/2 + 1/4 + 1/8 + 1/16 = 15/16. In contrast, a signal just above midscale, with an A/D output of "1000", produces an output only from the most-significant correlator, for a final weighted sum of 1/2.

Thus, the architecture illustrated not only correlates the analog input against the binary standard, but it also weights the computed correlation score to reflect the confidence with which the true value of each bit is known. The advantage of this treatment of the data is illustrated in the following example. Given matched paradigm and transmitted sequences of 1, 0, 0, 1 and a received (data plus interference) sequence of 1, .53, 0, 1, the single-bit, single-correlator system would interpret the received signal as 1, 1, 0, 1, for a total correlation of 3, instead of the true value of 4. In the 4-bit system, the computed correlation would be 7/8 + 3/8 + 7/8 + 7/8 = 24/8, out of a possible 28/8. Thus in this admittedly extreme example, the single-bit system would report 75% of the true correlation, while the more complex one would report 86% of it, thereby demonstrating reduced sensitivity to a noise-induced error.

----- INTENDED SIGNAL

——— ACTUAL SIGNAL

Figure 22. Binary Signal in the Presence of Noise



Note that all A *clocks must be tied together, as must all* B *clocks,* M *clocks,* R *clocks and summer clocks. This application uses the* XNOR *internal correlator logic, as in the single-bit correlation discussed earlier.*

Figure 23. Four-Bit Quantization and Correlation

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4.2.3 Correlation of Two Multi-Bit Functions

A different parallel correlation configuration is required where two multi-bit functions are to be correlated. Figure 24 depicts a 9-correlator matrix for computing the correlation between two 3-bit functions (or two analog functions quantized to 3 bits each). Each combination of bit positions of the two functions is fed to a separate correlator, the output of which is weighted accordingly. The configuration illustrated can be justified as follows:

1) The basic correlation equation is:

$$R(m) = \sum_{n=1}^{N} h(n) \times (m+n)$$

where m and n are indices for the serial values of the functions h and x.

2) Since h and x are three-bit quantities, they can be represented as $h \cdot 2^2 + j \cdot 2^1 + k \cdot 2^0 = 4h + 2j + k$ and $x \cdot 2^2 + y \cdot 2^1 + z \cdot 2^0 = 4x + 2y + z$, respectively.

3) Therefore, the correlation product h(n) x (m + n) can be re-expressed (dropping the arguments m and n, for convenience) as : 16 xh + 8 (xj + yh) + 4 (xk + yj + zh) + 2 (yk + zj) + zk.

The hardware implementation of this system is straightforward, requiring only the correlators and a summation network. The various divide-by-2^N blocks are merely rightward shifts of N bits. Thus, the outputs of the various correlators are loaded into different bit positions of the external summer, according to their weightings, as shown in Figure 25.

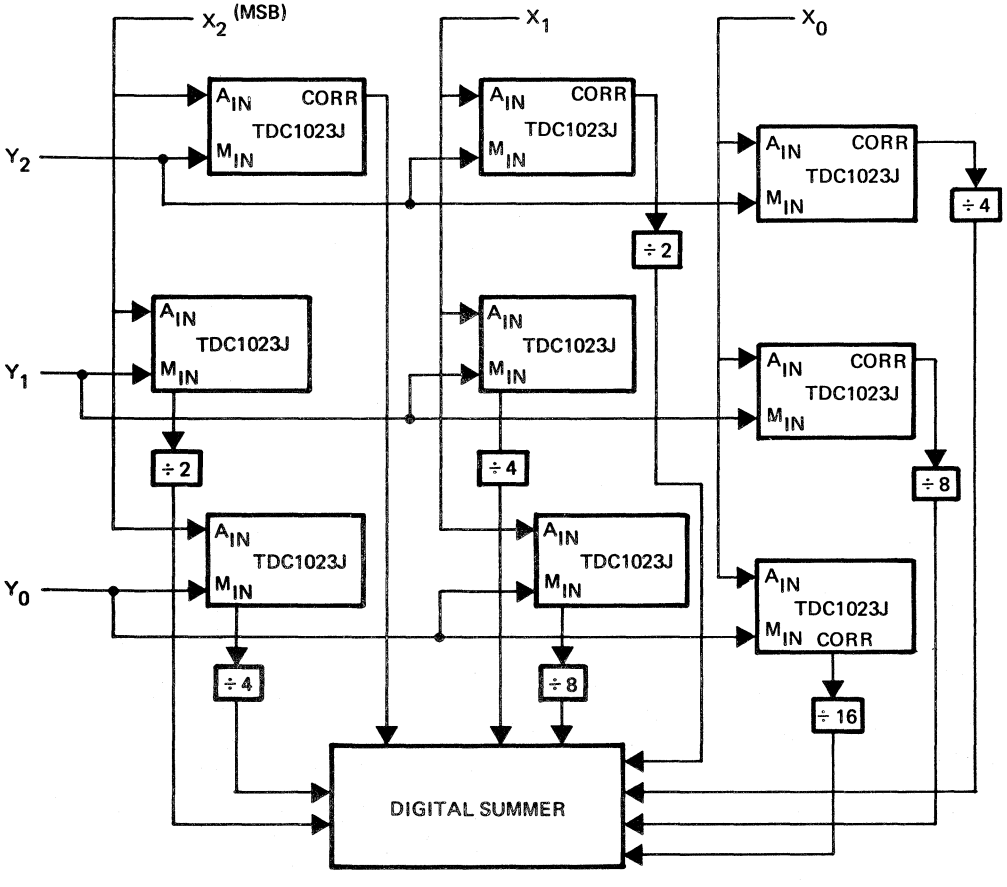
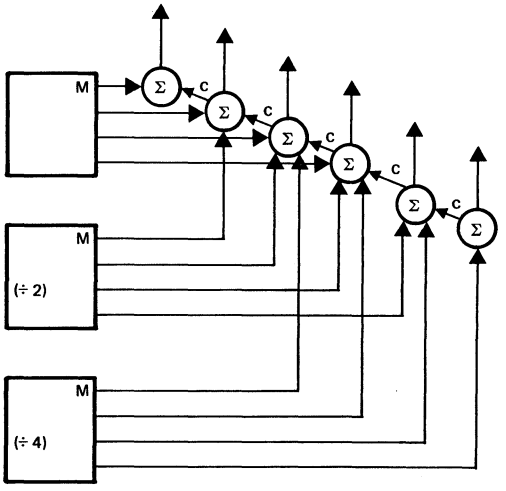


Figure 24. Correlation of Two Multi-bit Functions



Only the four MSBs *of each correlator's output are shown. In practice, all seven bits from each can be summed together, according to the pattern shown above.*

Figure 25. Weighted Summation of Multiple Correlator Outputs

5.0 CONVOLUTION

Convolution, the mathematical operation of multiplying two functions together and integrating their product across their common independent variable, is used extensively in digital signal processing. This section tells how to build a hardware convolver using one or more TDC1023 correlators.

The basic equation for digital convolution is:

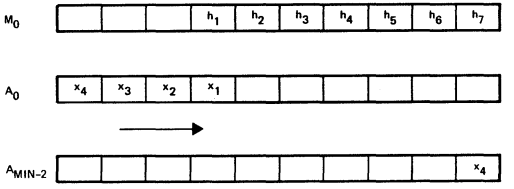
$$y(n) = \sum_{m=-\infty}^{\infty} h(m) \times (n - m)$$

where "h" and "x" are the two functions to be convolved and "m" and "n" are digital indices representing their common independent variable (generally time). The result of the convolution, y, is a function of the offset index "n", which measures the relative timing of the two functions. The equation for correlation,

$$R(n) = \sum_{m=-\infty}^{\infty} h(m) \times (m - n)$$

is identical, except that the argument of the function "x" has been inverted, i.e., that its sequence of values has been reversed. In both correlation and convolution, the successive values of two functions are multiplied together and the resulting products are summed. However, correlation operates on both functions in their natural sequences, whereas convolution operates forward on one function (h) and backward on the other (x), as shown in Figure 26.

To convolve two functions with a correlator, the function "h" is loaded into the A register, the function "x" into the "M" or B register, as discussed in Section 5.1. "H" is shifted in serially in the normal manner, while "x" must be shifted in backwards. The shifting of the two functions is coordinated so that h(m), the mth term of "h", lines up inside the correlator with x(n - m), the (n - m)th term of "x". The correlator then outputs y(n), the nth point of the convolution of h and x. Shifting the function h forward one "notch" in the correlator will then align h(m) against x(n + 1 - m), producing the next term of the convolution.



Step 1: Load register M *with function* "h" *(backward) to state* "M_0."

Step 2: Clock function "x" *forward through register* A *until* x_1 *and* h_1 *align.*

Step 3: Compute first convolution point, $y_1 = x_1 \cdot h_1$.

Step 4: Advance "A" *register contents one bit, compute* $y_2 = h_1x_2 + h_2x_1$.

Step 5: Continue until last step, x_4h_7 *in this case.*

Figure 26. Convolution with the Correlator

In convolution, the function "h" must be reversed, then loaded into register M, such that its last data point is the first into the register. "H" is clocked all the way across register M, until it just reaches the end of the register, i.e., its last data point (the first in) occupies the last position in the register, as shown in Figure 26. Register R must be preloaded with all "1's." Next, the function "x" is loaded forward into register A, so that its first data point is the first one into the register. It is clocked across the register until its first data point aligns with the first (last in) data point of "h." At this point, the two

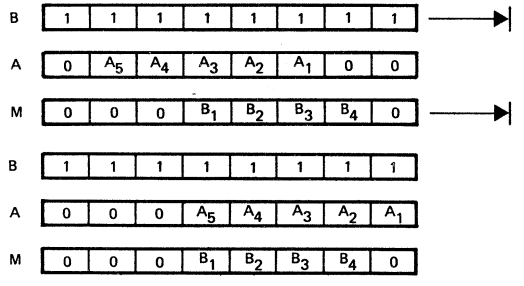
functions overlap by exactly one data point, and all A and M register locations not occupied by "x" or "h" are filled with zeros. The summation network is now clocked, causing the correlator to compute and output the first point of the convolution, which is simply the product of the first point of "h" and the first point of "x."

The remainder of the convolution operation involves shifting register A one position, computing and reading out the next correlation score (the next point in the convolution), and then repeating this shift/compute operation until the functions "h" and "x" no longer overlap. The last point of the convolution is thus the product of the last point of "x" and the last point of "h."

Digital filtering is a special form of convolution, in which "h" is the impulse response and "x" is the data stream. Digital filtering is performed exactly as described above, with the shift-and-compute operation continuing as long as data are available in "x". In a finite impulse response (FIR) filter, the impulse response is merely the sequence of coefficients.

5.1 "EXCLUSIVE-NOR" VERSUS "AND" LOGIC

Convolution requires standard binary multiplication (the logical AND function), not comparison (the logical XNOR function). As discussed in Section 4, the correlator AND function represents "one/zero" multiplication. The two data functions, "x" and "h," are loaded into the A and M registers and the B register is filled with "1's," as illustrated in Figure 27. In this mode,



Two finite functions, A *and* B, *have been loaded into the* A *and* M *registers, respectively. With these functions occupying the positions shown in the upper figure, the correlator will compute a single number, the value of the convolution for* $y(n=4) = \sum_m A(m)\,B(4-m) = A_1B_3 + A_2B_2 + A_3B_1$. *The value of the convolution for* $y(n=6) = \sum_m A(m)\,B(6-m) = A_1B_5 + A_2B_4 + A_3B_3 + A_4B_2 + A_5B_1$, *is computed using the lower configuration.*

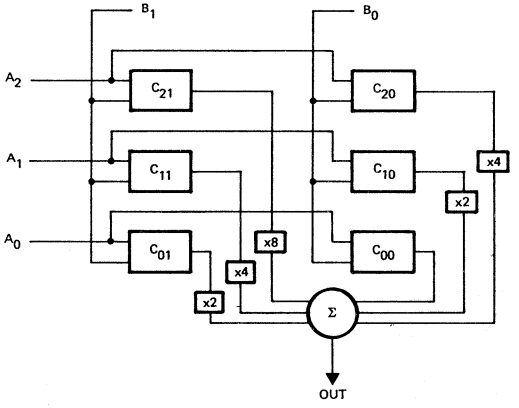
Figure 27. Convolution with the Correlator

each bit position yields an output of "1" only if both the A and M registers hold "1's" in that position; otherwise, the output for that bit is a "0". The 1023 correlator then performs the integration over time in its digital summer, putting out a single value, y(m), corresponding to the relative alignment of the functions "x" and "h" within the A and M registers.

5.2 HIGHER-PRECISION CONVOLUTION

Many types of data should be represented to two or more bits precision; however, the correlator can handle only a single bit level. An array of correlators can be assembled for multibit precision, as shown in Figure 28. As the figure suggests, each correlator multiplies and "integrates" a particular combination of bit levels in the two input functions. The outputs of the various correlators are then summed, with appropriate binary weightings, to yield the final result. The binary weightings are executed through shifts of one bit position for each factor of two. Thus, a "divide by four" is simply a two-bit rightward shift of the data. As in ordinary binary multiplication, the relative binary weighting for each correlator is merely the sum of the corresponding binary weightings of the multiplier and multiplicand bits fed into it.

The correlator and weighting configuration described in the previous paragraph is easily justified algebraically. Every binary number represents a sum of various powers of 2, some with a weighting of "1", others with a weighting of "0". If the two functions are represented as



C_{ij} *are correlator chips. Input functions for convolution are* $A = A_0 2^0 + A_1 2^1 + A_2 2^2$ and $B = B_0 2^0 + B_1 2^1$. *Correlators* C_{00}, C_{01} *and* C_{10} *can be eliminated, if lower-precision convolution is acceptable. "A" values are fed into the* A *registers, while* B*'s go to the* M *registers.*

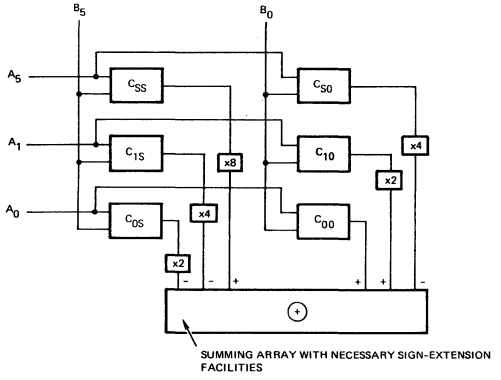
Figure 28. Block Diagram for 3-Bit and 2-Bit Convolution

$a_0 2^0 + a_1 2^2 + \ldots + a_m 2^m$ and $b_0 2^0 + b_1 2^1 + b_2 2^2 + \ldots + b_n 2^n$, then the product will comprise (m + 1) x (n + 1) terms, $a_0 b^0\ 2^{0+0} + a_1 b_0 2^{1+0} + a_2 b_0 2^{2+0} + \ldots + a_0 b_1 2^{0+1} + \ldots + a_m b_n 2^{m+n} \equiv p$. Mathematically, a digital convolution involves computing this total product separately for each instant of time, and then summing the products over time. Equivalently, the correlator system first sums (integrates) each individual sub-product (e.g., $a_0 b_0 2^0$) over time, and then combines all of these sums. Since only the sequence of additions is altered, the two operations are equivalent.

If only a single-precision product is required, the lowest-order bit combinations can be ignored, significantly reducing the number of correlators in the circuit. Note that this abbreviated format yields only 0 to -1 LSB precision, rather than the ±1/2 LSB obtainable from rounding a full double-precision product to single-precision. Since the abbreviated format constitutes an arithmetic truncation, the results are biased downward. This can be corrected by adding "1" to the bit immediately below the LSB to be retained in the final product.

5.3 HIGH PRECISION CONVOLUTION WITH NEGATIVE QUANTITIES

As outlined in Figure 29, the binary weighting scheme outlined above can be further extended to include multiple-precision negative numbers. Since the correlators perform their time integrations independently and before the summation of each individual product, caution should be exercised when designing multi-correlator convolvers to handle negative numbers. The arithmetic format best-suited to this application is two's complement binary, in which the most significant bit is the sign bit in both the multiplier and the multiplicand. The sign bits must be treated carefully, as discussed below. In two's complement arithmetic, all correlators are operated in AND logic (binary multiply) mode, with the "forward" function in the A register, the "backward" one in the M, and a string of "1's" in the B register. The outputs of the correlators that handle nonsign (positive) bits only are considered positive, as is the output of the correlator handling both sign bits. These outputs are all summed, each with its respective binary weighting, which is achieved simply through column shifting, as before. For example, upon receiving a 2^2 relative weighting, the quantity "101" becomes "10100."



The architecture illustrated can be extended readily to larger word sizes. Note that correlator outputs SI *and* IS, *where* I = 0, 1, . . ., *are considered negative. Subtraction is most easily accomplished by inverting the binary digits, adding* 1 *to the* LSB, *and adding.*

Figure 29. Convolution of Two's Complement Numbers

The correlators that multiply the sign bit of one function against any nonsign bit of the other must also be treated carefully. These correlators are operated in A register - M register AND logic, but the final outputs must be subtracted from those of the other correlators, to reflect the negative weighting of the sign bit. The values must also be shifted to provide proper binary weighting, and leftward sign extension must be applied as needed. In two's complement arithmetic, the digits of the quantity to be subtracted are inverted, then "1" is added to the LSB, and the resulting quantity is added to produce the subtraction. The summation algorithm parallels the accumulation logic of standard two's complement binary multiplication.

5.4 LONGER-SAMPLE CONVOLUTION

Although the convolution architecture just described is limited by the correlator's shift register length to 64-sample convolutions, it can be extended readily to 128-sample or even longer convolutions. Expanding the architecture to large-sample convolutions requires replacing each correlator with N/64 correlators, where N is the desired number of samples in the convolution, i.e., the length of the shorter of the two functions "x" and "h." The correlators within each set are wired serially, such that the A, B, and M register outputs of one device feed the A, B, and M inputs of the next, and all corresponding register clocks are tied together within each set. Finally, the digital outputs within each set must be combined in a digital summer, whose output is then shifted (for appropriate binary weighting) and added to the outputs of the other digital summers. Thus, the serial connections of correlators for extended-sample convolution and correlation are identical. The number of series-connected correlators required is L/64, where L is the length of the shorter of the two functions "x" and "h."

5.5 CONVOLUTION OF ANALOG SIGNALS

It is relatively simply to convert the multibit convolver into an analog convolver, using two A/D converters. Since many A/D converters operate over a range which does not cross zero, the simplest configuration would be unipolar (positive-only or negative-only), in the general format discussed in Section 5.2 above. Treating all incoming signal levels as same-signed would eliminate the need for two's complement arithmetic and its associated subtractions (Section 5.3). However, bipolar signals can be handled by offsetting the A/D converter's input so that an original signal of "0" produces a mid-scale ("1000 . . .") output, while positive signals produce higher outputs and negative signals produce lower outputs. To convert the output of the A/D converter into two's complement format, merely invert the MSB, leaving the other bits unchanged. The resulting two's complement binary code is then supplied bit-by-bit to the appropriate correlator inputs.

Note that this system represents the simplest, fastest, but not necessarily most cost-effective implementation of the analog convolver. If lower speed and increased control logic requirements are acceptable, the number of correlators and/or A/D converters can be reduced through the multiplexing of data inputs and outputs. The hardware architecture chosen depends on the data rate and the speed of the A/D converters that are used.

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An Introduction to Two Different Finite Impulse Response Structures

TP-31

Digital filtering is a rapidly expanding field; it provides improved stability, predictability, and performance over analog designs. The design process for digital filters is not dramatically different from design techniques for high-performance analog filters; however, due to the flexibility of the digital approach, additional design decisions are necessary.

One of these decisions is the choice between filters with (theoretically) infinite impulse responses and those with finite impulse responses. The advantages of Infinite Impulse Response (IIR) filters include ease of design without computer aid and efficiency (in terms of number of multiplications required per sample for a given rolloff rate, without specifying the phase response). The advantages of Finite Impulse Response (FIR) filters include: ease of design of complex frequency responses with computer aid, ability (within limits) to specify the phase response of the filter, ease of obtaining exact linear phase, and circuit simplicity.

The stages of filter design are:

1. Specification of all relevant parameters.
2. Generation of a transfer function which meets the requirements specified in step 1.
3. Selection of a signal flow diagram to give the transfer function obtained in step 2. This corresponds to the selection of a circuit configuration in analog filter design.
4. Selection of an architecture to carry out the calculations to give the signal flow graph.
5. Designing the circuit.

This application note discusses two different forms for Finite Impulse Response (FIR) digital filters. The theoretical development of each form precedes discussion of their merits. In the stages of filter design as discussed above, only steps 3 and 4 are discussed in this application note. The Z-transform is used heavily in the discussion of the use of Infinite Impulse Response forms to get a FIR overall response; some familiarity with the Z-transform is therefore assumed.

Development of the Tapped Delay Line Form for FIR Filters

1. An impulse is a finite-length sequence of length one.

2. When an impulse is fed into a finite impulse response filter, the result is a finite-length sequence.

3. The Z-transform of the impulse response of a FIR filter is the impulse response itself, since the Z-transform of a unit impulse is unity. This is shown in Figure 1.

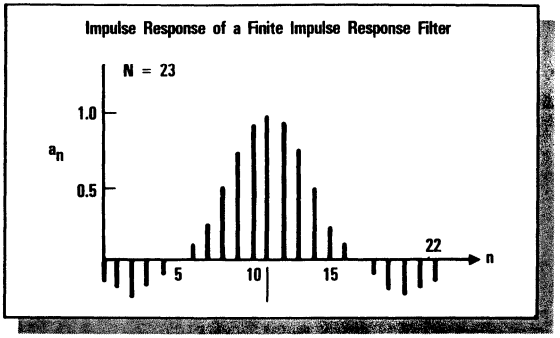

Figure 1

4. The Z-transform of a finite sequence, if written in terms of z^{-1}, can be translated into a signal flow diagram, as seen below in Figure 2.

$$H(z) = \sum_{n=0}^{N-1} h(n)z^{-n}$$ (definition of the Z transform of a finite sequence h(n) of length N)

where

$Y(z) = X(z)\,H(z)$

The summation is:

$$X(z) = h(0) + h(1)z^{-1} + h(2)z^{-2} + \ldots + h(n-1)z^{-(n-1)}$$

Since z^{-1} represents a single-sample delay, this becomes:

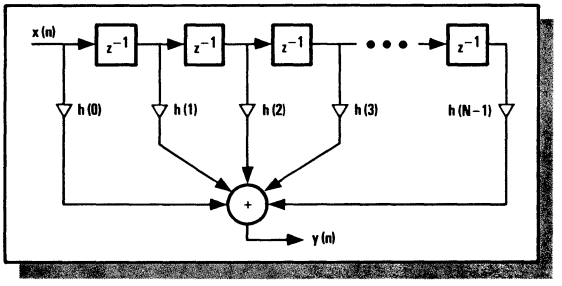

Figure 2.

5. Various techniques exist for determining the values of h(n) from the frequency response requirements. (See **Theory and Application of Digital Signal Processing** for more detail.)

6. The hardware for implementing this signal flow diagram can be represented by one of several block diagrams, as shown below in Figures 3a and 3b.

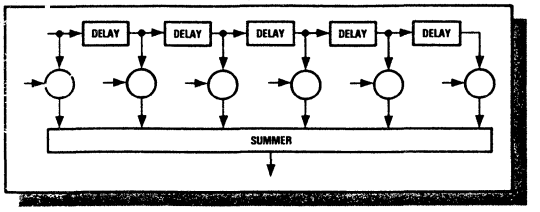

Figure 3a

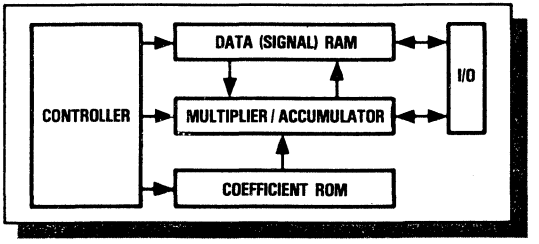

Figure 3b

Benefits of the Tapped Delay Line Form for FIR Filters

1. The configuration shown in Figure 3a requires the least amount of hardware. (The TRW LSI Products TDC1028 utilizes a variant on this block diagram.) Figure 3b requires the fewest ICs for a given filter length. With its large amount of parallel arithmetic hardware, implementation 3a offers very high operating speeds, with a maximum data rate equal to the cycle time of the arithmetic elements.

2. Since the coefficients used in filtering are simply the impulse response values, this form can be used for adaptive filtering.

Development of the Frequency–Sampling Form for FIR Filters

1. An impulse is a finite-length sequence of length one.

2. When an impulse is fed into a FIR filter, the result is a finite-length sequence, by definition.

3. The Z-transform of a finite-length sequence always has a region of convergence that includes the unit circle, and therefore can be discussed as the frequency reponse of a FIR filter.

4. Evaluating the Z-transform of a single period in a periodic sequence at equally-spaced points around the unit circle gives the same values as the Discrete Fourier Series of the periodic sequence.

   A periodic sequence can be composed of repetitions of a single aperiodic finite-duration sequence.

5. If the DFT (with the same number of points as the number of taps of the FIR filter) of the impulse response of a FIR filter is taken, the result is the frequency response of the filter, sampled at equal intervals between zero frequency and twice the Nyquist rate.

6. Therefore, the samples of the frequency response of a finite impulse response filter are identical to the Z-transform of the impulse response. In the notation below, $\tilde{X}(k) = X(k)$, where $\tilde{X}(k)$ is the DFT of the impulse response.

7. Designing a FIR filter is the same as obtaining its impulse response, which in turn is the same as taking its Z-transform, because the Z-transform of an impulse is unity.

   A FIR filter can be designed by taking the Z-transform of the impulse response, which has been obtained from the inverse DFT of the desired frequency response, sampled at N points between zero and twice the Nyquist frequency.

8. Expressed mathematically:

   $x(n) = Z^{-1}[X(z)]$ or $X(z) = Z[x(n)]$

   where

   $x(n) = \tilde{x}(n) = \text{IDFT}[\tilde{X}(k)]$

9. Elaborating on the mathematics:

$$X(z) = \sum_{n=0}^{N-1} x(n) z^{-n} \quad \text{(definition of the Z transform of a finite sequence of length N)}$$

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} \tilde{X}(k)\, e^{-j2\pi kn/N} \quad \text{(definition of N point DFT)}$$

10. Substituting the equation for x(n) into the Z-transform:

$$X(z) = \sum_{n=0}^{N-1} z^{-n} \left(\frac{1}{N} \sum_{k=0}^{N-1} \tilde{X}(k)\, e^{-j2\pi kn/N} \right)$$

11. Moving the $\frac{1}{N}$ term to the outside and interchanging the order of summation:

$$X(z) = \frac{1}{N} \sum_{k=0}^{N-1} \sum_{n=0}^{N-1} \tilde{X}(k)\, z^{-n}\, e^{-j2\pi kn/N}$$

12. Two quantities raised to the n^{th} power can be combined:

$$X(z) = \frac{1}{N} \sum_{k=0}^{N-1} \sum_{n=0}^{N-1} \tilde{X}(k) \left(z^{-1}\, e^{-j2\pi k/N} \right)^n$$

13. Since the $\tilde{X}(k)$ term has no dependence on n, it can be removed from the second summation:

$$X(z) = \frac{1}{N}\sum_{k=0}^{N-1}\tilde{X}(k)\sum_{n=0}^{N-1}\left(z^{-1}\, e^{-j2\pi\, k/N}\right)n$$

14a. To perform the second summation, a difference between two infinite series of the form is used:

$$S = \sum_{n=0}^{\infty} r^{-n} = \sum_{n=0}^{\infty} r^{-n} - \sum_{n=N}^{\infty} r^{-n}$$

where

$$r = e^{-j\,(2\pi)\,k/N}\, z^{-1}$$

14b. The infinite series sums to:

$$\sum_{n=1}^{\infty} r^{-n} = \frac{1}{1-r}$$

15. Therefore:

$$S = \frac{1}{1 - e^{-j\,(2\pi)\,k/N}\, z^{-1}} - \sum_{n=N}^{\infty}\left(e^{-j\,(2\pi)\,k/N}\, z^{-1}\right)n$$

16. A change of variables is performed: let n = m+N (m=n−N)

$$S = \frac{1}{1 - e^{-j\,(2\pi)\,k/N}\, z^{-1}} - \sum_{n=m+N}^{\infty}\left(e^{-j\,(2\pi)\,k/N}\, z^{-1}\right)m+N$$

17. Distributing the exponentiation over the multiplication:

$$S = \frac{1}{1 - e^{-j\,(2\pi)\,k/N}\, z^{-1}} - \sum_{n=m+N}^{\infty}\left(e^{-j\,(2\pi)\,N/N}\, e^{-j\,(2\pi)\,km/N}\, z^{-N}\, z^{-m}\right)$$

18. The first exponential has a value of unity, and z^{-N} does not depend on the index m; therefore:

$$S = \frac{1}{1 - e^{-j\,(2\pi)\,k/N}\, z^{-1}} - z^{-N}\sum_{m=0}^{\infty}\left(e^{-j\,(2\pi)\,km/N}\, z^{-m}\right)$$

19. The last summation is identical to that of #15, therefore:

$$S = \frac{1}{1 - e^{-j\,(2\pi)\,k/N}\, z^{-1}} - z^{-N}\,\frac{1}{1 - e^{-j\,(2\pi)\,k/N}\, z^{-1}}$$

20. Since the denominators are equal, the result is:

$$S = \frac{1}{1 - e^{-j\,(2\pi)\,k/N}\, z^{-1}}$$

21. Using this value in the #13 equation, which is:

$$X(z) = \frac{1}{N}\sum_{k=0}^{N-1}\tilde{X}(k)\sum_{n=0}^{N-1}\left(z^{-1}\, e^{-j2\pi\, k/N}\right)n$$

The result is:

$$X(z) = \left(1 - z^{-N}\right)\frac{1}{N}\sum_{k=0}^{N-1} X(k)\,\frac{1 - z^{-N}}{1 - e^{-j2\,k/N}\, z^{-1}}$$

22. To simplify:

$$S_k = \frac{1}{1 - e^{-j\,(2\pi)\,k/N}\, z^{-1}}$$

which gives –

$$X(z) = \left(1 - z^{-N}\right)\sum_{k=0}^{N-1}\tilde{X}(k)\, S_k$$

23. This can be shown in signal flow diagram form. (See Figure 4)

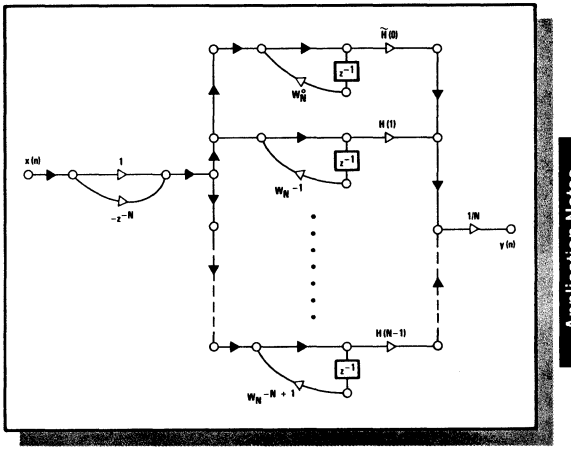

Figure 4.

24. Unfortunately, the poles of this circuit are exactly on the unit circle, which means that stability is only conditional. To avoid this problem, the poles are placed at a radius r, where r is just slightly less than unity. This guarantees stability at little variation in frequency response from the unity radius case. Therefore, the new values for the Z–transform of the impulse response are:

$$X(z) = \left(1 - r^N\, z^{-N}\right)\frac{1}{N}\sum_{k=0}^{N-1}\tilde{X}(k)\, S_k$$

where r is slightly less than unity. (See Gold and Rader, **Digital Processing of Signals**, p. 83.)

25. This signal flow diagram is that of a FIR filter cascaded with a set of IIR filter blocks in which the outputs are summed. The frequency response of a filter includes both amplitude and phase response; the $\tilde{X}(k)$ are complex numbers, as are the S_k.

26. There is no reason to allow the h(n) to be complex as virtually every desired magnitude and phase response can be obtained with real h(n). As a result, the complex first order loops can be grouped as complex conjugates and implemented as real-coefficient second order networks. This implementation is shown below in Figure 5.

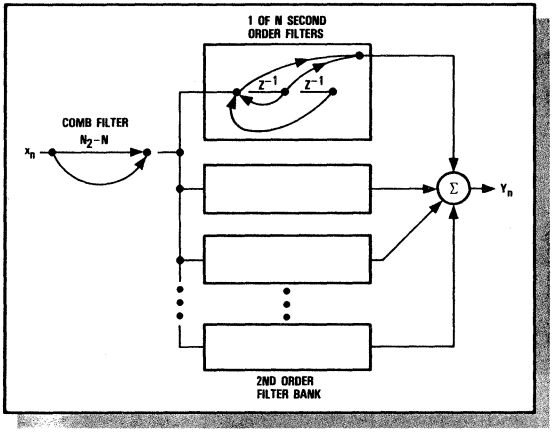

Figure 5

27. For further information on calculating the values for the coefficients of the second order sections, see Oppenheim and Shafer, **Digital Signal Processing**, p. 161-163.

28. The preceding development has been mathematical, with no physical motivation or description. Added understanding may come from examination of the operation of the frequency sampling structure in both the frequency (Z-plane) and time domains.

29. The second-order elementary sections have infinite impulse response characteristics which stem from the use of feedback. As a result, they have poles, which in general are complex conjugates in the Z-plane.

30. In order to get a finite impulse response characteristic for the overall circuit, the effects of the poles (and hence of the IIR-giving feedback) must be cancelled out. This can be done by cascading each elementary section with a circuit with zeros at exactly those frequencies where the elementary sections provide poles.

31. In the frequency domain, the finite impulse response pre-filter has the response $H(z)=(1 - z^{-n})$. This expression can be factored, and the result is:

$$H(z) = \prod_{k=0}^{n/2} (1 - z^{n/k})(1 + z^{n/k})$$

32. When viewed graphically in the Z-plane, this is a set of equally-spaced zeros on the unit circle. This is shown in Figure 6 below. Note that these are exactly superimposed on the pole locations given in (22).

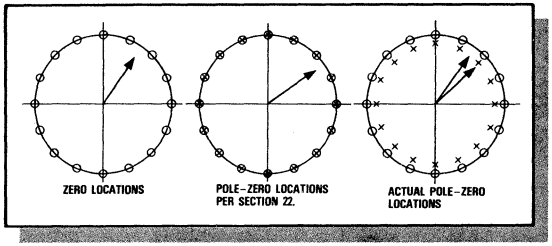

Figure 6

33. Actually, as mentioned in (24), the poles are designed to lie just within the unit circle, whereas the simple implementation of the FIR pre-filter gives zeros on the unit circle itself. As a result, there is an error term. This can be dealt with by changing the FIR pre-filter to move the zeros inward; however, the usual approach in practice is to ignore the problem, and treat the error as a small deviation from the desired frequency response.

34. While the frequency response analysis of the action of frequency sampling filters describes the operating mechanism as pole-zero cancellation, there is also a good description in the time domain.

35. Consider the impulse response of a single elementary section, in cascade with the FIR pre-filter. An impulse is applied to the FIR section, and is immediately passed through and applied to the elementary section. This elementary section starts to oscillate with a fixed magnitude because its pole is on the unit circle. N samples later (which is an integer number of cycles of oscillation), a negative impulse (of exactly the right value to stop the oscillations) is applied. This is shown in Figure 7.

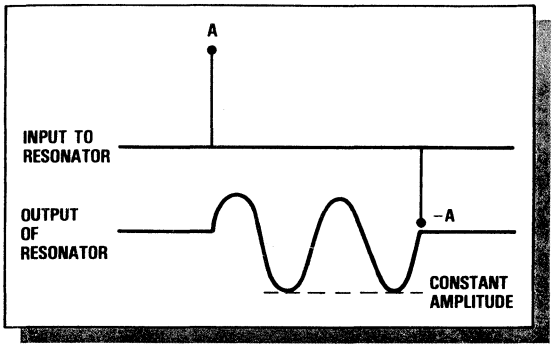

Figure 7

36. Again, as mentioned in (24), the poles of the elementary sections are moved inside the unit circle. The time-domain effect of this is that the second (countervailing) impulse is now just slightly larger than that necessary to stop the oscillations, with the net effect of reversing the phase of those oscillations. However, finite arithmetic precision may result in zero oscillations in many actual implementations.

Benefits of the Frequency-Sampling Form for FIR Filters

1. On first examination, the block diagram shown in Figure 5 seems to have a severe drawback: over twice the number of multiplications are required compared to the tapped delay line implementation.

2. If frequency selective filters (lowpass, highpass, bandpass, or bandstop) are being designed, many of the frequencies which are sampled will have a response of zero. Second order filters for these frequencies need not be implemented. This can reduce the number of multiplications significantly. In fact, it may require fewer multiplications than the delay line architecture. The cost is increased memory, since more values must be stored; however, at the present cost of memory chips, this is not a large penalty.

3. This signal flow diagram configuration might be implemented in the hardware block diagram shown in Figure 3. It is the same hardware block diagram used for Infinite Impulse Response Filters; thus, this configuration may be desirable for general-purpose programmable filter implementation, where either type of filter may be required. For further information about this hardware design, see TRW LSI Products Application Note TP-7A.

4. The frequency-sampled implementation requires greater design effort than the tapped delay line form. The availability of computer-aided design programs is easier for the tapped delay line form; however, programs to perform the frequency sampling design are easier to write.

Summary

Most present-day applications of FIR filters use the tapped delay line implementation, for its ease in design and adaptation. An alternative form has been described which may be more efficient, and which can be hardware time-multiplexed with Infinite Impulse Response filters, due to the similarities.

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Oppenheim, A., and R. W. Schafer, **Digital Signal Processing**, Englewood Cliffs, New Jersey, Prentice-Hall, 1975.

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TP-31

Using the TDC1034, TDC1018, TDC1141 and TDC1112 in a TTL Environment

Introduction

The TDC1018 and TDC1034 digital-to-analog converters (D/A) were designed for operation in systems that employ ECL logic families. The digital inputs to these devices are designed for direct ECL compatibility and a single power supply voltage of −5.2 Volts is all that is required for operation.

There are many TTL systems that require the use of high-speed D/A converters but have only +5 Volt power supplies available. The TDC1018 and TDC1034 can easily be used in a TTL environment and this application note suggests practical circuits and clarifies some of the issues that surface.

"Normal" Operation

The circuitry of the TDC1018 and TDC1034 has been partitioned on the chip into analog and digital functions. This is done in order to optimize noise and feedthrough performance of the D/A converter. Both devices have analog and digital ground inputs as well as analog and digital power inputs.

Since the TDC1018 was designed for ECL systems, its A_{GND} and D_{GND} inputs normally connect to 0.0 Volts (system ground) and the power supply pins, V_{EEA} and V_{EED}, connect to −5.2 Volts. The basic connections for the TDC1034 are the same but the analog and digital ground inputs have been renamed to more accurately reflect their functions. In normal ECL system operation, the V_{CCA} and V_{CCD} inputs of the TDC1034 connect to system analog and digital grounds respectively.

Power Supply Connections in a TTL System

As long as the correct polarity of the power supply inputs is maintained, the TDC1018 and TDC1034 can operate from a +5.0 Volt supply as well as a −5.2 Volt supply. The D/A converter is not affected by the nature of its power supply. To operate in TTL mode, the more positive power supply inputs (A_{GND} and D_{GND} on the TDC1018, V_{CCA} and V_{CCD} on the TDC1034) connect to +5 Volts. The negative power inputs (V_{EEA} and V_{EED}) connect to system ground. Table 1 summarizes the power and ground connections for the TDC1018 and TDC1034 in ECL and TTL operating modes.

Device, Power, Ground	ECL mode	TTL mode
TDC1018		
Positive Analog Power	–	A_{GND} Pin 17
Positive Digital Power	–	D_{GND} Pin 9
Analog Ground	A_{GND} Pin 17	V_{EEA} Pin 20
Digital Ground	D_{GND} Pin 9	V_{EED} Pin 5
Negative Analog Power	V_{EEA} Pin 20	–
Negative Digital Power	V_{EED} Pin 5	–
TDC1034		
Positive Analog Power	–	V_{CCA} Pin 13
Positive Digital Power	–	V_{CCD} Pin 6
Analog Ground	V_{CCA} Pin 13	V_{EEA} Pin 16
Digital Ground	V_{CCD} Pin 6	V_{EED} Pin 3
Negative Analog Power	V_{EEA} Pin 16	–
Negative Digital Power	V_{EED} Pin 3	–

Table 1. Power And Ground Connections For ECL And TTL System Operation.

Getting the TTL Data In

Since the TDC1018 and TDC1034 were designed for ECL systems, all of their digital inputs are optimized for ECL logic levels. The Operating Conditions Table of the Datasheet indicates the minimum voltage (with respect to D_{GND} or V_{CCD}) that can be applied to the D/A which will insure a logic "1" as V_{IH}. V_{IL} is the maximum voltage that can be applied which will insure a logic "0."

The V_{IL} specification can also be restated as: any voltage more negative than −1.49 Volts but more positive than V_{EED} is a logic "0." Similarly, V_{IH} can be restated as: any input voltage more positive than −1.045 Volts but more negative than D_{GND} is a logic "1." These interpretations of V_{IL} and V_{IH} are predicated on the connection of D_{GND} to 0 Volts and V_{EED} to −5.2 Volts.

Since the D/A converters can be operated from a positive power supply voltage, V_{IL} and V_{IH} input conditions must be translated into TTL equivalents. V_{IL} in a TTL environment becomes: any input voltage more negative than +3.51 Volts (V_{CC} − 1.49) is a logic "0." Similarly V_{IH} in a TTL environment becomes: any input voltage more positive than +3.955 Volts (V_{CC} − 1.045) is a logic "1." Table 2 summarizes the translation of V_{IL} and V_{IH} in TTL and ECL operating modes.

Digital Input	ECL mode	TTL mode
logic "1"	−1.045 to 0.0V	+3.955 to +5.0V
logic "0"	−1.49 to −5.2V	0.0 to +3.51V

Table 2. V_{IH} And V_{IL} Operating Conditions For ECL And TTL Operating Modes.

An appropriate way to drive the digital inputs of the TDC1018 or TDC1034 D/A converter from TTL devices is shown on the left-hand side of Figure 1. A resistor divider network between the TTL gate and D/A converter will insure proper input level for the D/A, with minimum V_{OH} for the TTL gate of 2.4 Volts and a maximum V_{OL} of 0.4 Volts.

Getting The Analog Out

The analog output structure for both the TDC1018 and TDC1034 is the same. Output current "sinks" (flows into) the complementary OUT+ and OUT- terminals. The compliance voltage limitations on these outputs are specified with respect to the positive power inputs.

In order to convert the D/A output current into a output voltage, a load resistor is connected between the output terminal and the positive power input. In a TTL system, this will create an output voltage that varies with respect to the +5 Volt supply. In some applications this is undesirable because of the variation and noise of the +5 Volt power supply.

Figure 1 is a suggested circuit that can be used to "turn around" the D/A output current and generate an output voltage that varies with respect to analog ground and is relatively insensitive to variations in power supply voltage. PNP transistors Q1 and Q2 are biased in a way that maintains a nearly constant voltage on the base of Q1. The current that flows in Q1 is the difference between the constant quiescent current set up by R1 and the voltage drop across U2, and the D/A output current flowing into the OUT- terminal.

A 1.2 Volt band-gap reference diode, U2, provides the reference voltage for the D/A converter and the bias voltage for output transistor Q1. Q2 is a diode-connected transistor which functions as temperature compensation for the emitter-base voltage of transistor Q1. Since a maximum of nearly 30 milliamps can flow through Q1, a monolithic dual PNP transistor is not recommended. Q1 and Q2 should be placed in close thermal contact.

Since the output transistor is biased with respect to the +5 Volt power supply, bypass capacitors on the base of Q1 are connected to +5 and not to ground. The sum of the currents from the outputs of the D/A converter is constant and should share a common path to V_{CC} that excludes the reference circuitry. This will reduce the possibility of creating a signal feedback path back into the D/A.

Two performance photographs are shown in Figures 2 and 3. The full 1-Volt p-p output of the circuit is shown in Figure 2. The ramp portion of the photo indicates the normal linear dynamic range of the D/A converter as it varies from black to white. Additionally, the SYNC input to the D/A converter is activated after the video range reaches full scale. Figure 3 shows the dynamic performance of the circuit when it puts out a 25 nanosecond full-scale video pulse. The small variable capacitor between base and collector of Q1 can be used to optimize the pulse response.

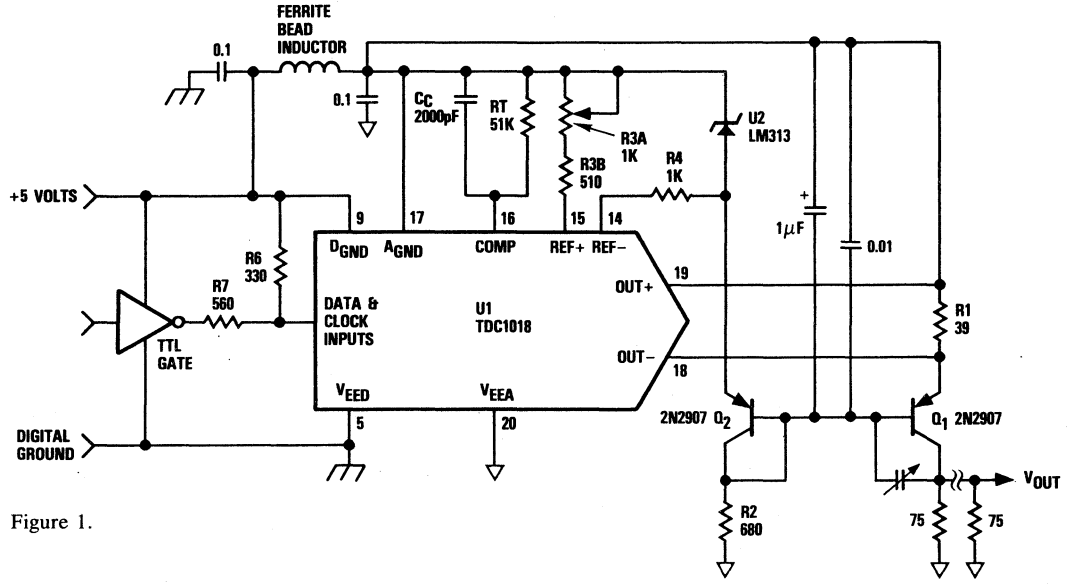

Figure 1.

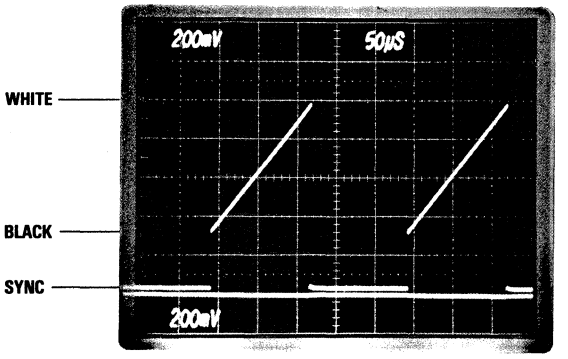

Figure 2

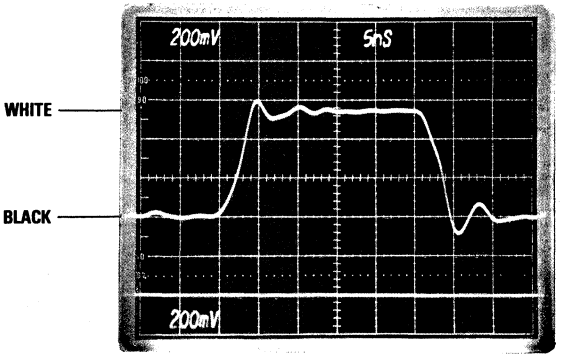

Figure 3

Analysis Of The Current "Turn–Around" Circuit

A set of equations is helpful in tailoring this circuit for a specific application. Equations 1, 2, and 3 show the derivation of the transfer function of the circuit. Equations 4, 5, and 6 come from information presented on the TDC1018 Datasheet. The relationship between the output voltage of the circuit to the current in Q1 is given by:

$$V_{OUT} = I_{EQ1} \times \frac{\beta 1}{\beta 1 + 1} \times R1 \quad (1)$$

where $\beta 1$ is the forward current gain of transistor Q1.

The current in Q1 as a function of D/A converter output current can be shown by:

$$I_{EQ1} = \left\{ \frac{V_{U2} + (V_{BE2} - V_{BE1})}{R1} \right\} - I_{D/A} \quad (2)$$

where V_{U2} is the forward voltage drop across band–gap reference device (1.22 Volts nominally) and $I_{D/A}$ is the D/A output current flowing into the OUT– terminal of the D/A converter.

The transfer function of the TDC1018 D/A converter in its linear range is given by:

$$I_{D/A} = \left\{ \left(\frac{\text{input data}}{256} \right) \times I_{REF} \times K1 \right\} + I_{BLK} \quad (3)$$

where I_{REF} is the reference current flowing into the REF+ terminal of the D/A converter, K1 is a constant derived from the datasheet, and I_{BLK} is the nominal D/A output current when the D/A converter outputs "black."

I_{REF}, I_{BLK}, and I_{SYNC} output current levels can be determined from the Operating Conditions Table and the Video Control Truth Table found on the datasheet for the TDC1018.

$$I_{REF} = \left(\frac{V_{U2}}{R3A + R3B} \right) = 1.115 \text{ mA nominally} \quad (4)$$

$$I_{BLK} = 19.4 \text{ mA nominally} \quad (5)$$

$$K1 = \frac{I_{SYNC} \text{ output current}}{I_{REF}} = \frac{28.57 \text{ mA}}{1.115 \text{ mA}} = 25.6 \quad (6)$$

Conclusion

The circuit described is a true single power supply voltage output D/A converter. The techniques discussed in this application note should help clarify the operation of TRW's high–speed eight and four–bit D/A converters in a TTL environment.

Non-Linear Operations with the TMC2301 Image Resampling Sequencer

John Eldon and John Watson

Non-Linear Operations with the TMC2301 Image Resampling Sequencer

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John Watson, U.C.S.D.

The TMC2301 Image Resampling Sequencer is used in an image filtering and resampling system both to map input address sequences to output address sequences (a geometric transformation) and to provide a set of local addresses (a "walk") with which to calculate each output point's intensity by interpolation of a selected number of input points' intensities. Both these functions and the associated control signals are described in TP-36 and TP-37. Here we will consider the use of pure and mixed second-order terms to achieve nonlinear geometric mappings. A general technique for approaching nonlinear transforms and two simple examples are included. Finally, a series of parameter sets is given to demonstrate the effect of second-order coefficients on a rectangular test image.

Review of Zero and First Order Terms

The TMC2301 implements the following "backward" mapping from (u, v), the output address, to (x, y), the input address (with the kernel = 0, i.e., with no pixel walk, since we are not yet concerned with interpolation here):

$$X = XO + u*DXUO + (u^2 - u)/2*DXUU + u*v*DXUV + v*DXVO + (v^2 - v)/2*DXVV$$

$$Y = YO + u*DYUO + (u^2 - u)/2*DYUU + u*v*DYUV + v*DYVO + (v^2 - v)/2*DYVV$$

Here we use the notation DXUO = dX/dUO, DXUU = d^2X/dU, DXUV = d^2 X/dUdV, etc. As described in TP-36 and TP-37, the lower-order coefficients operate as follows:

XO and YO translate the (u, v) image by shifting its origin.

DXUO copies, expands or compresses the (u, v) image horizontally, for the cases DXUO = 1, DXUO > 1, and 0 < DXUO < 1 respectively. DXUO < 0 constitutes a reflection (copied, compressed or expanded) about the vertical axis.

DXVO shears the curve in the horizontal direction, as shown in Figures 1 and 2:

Figure 1

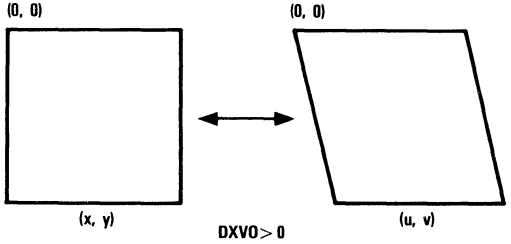
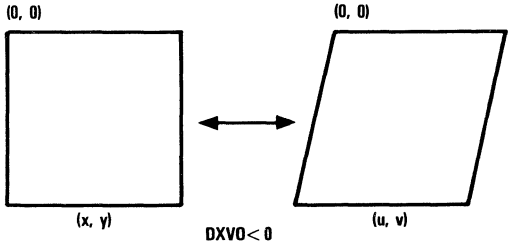


Figure 2



Note:

1. It is important to understand that these are "backward" mappings, which go from an "irregular" (x, y) input image to a rectangular (u, v) output image. This would be the direction of a typical distortion correction, for example. In the "Test Images" section below, coefficients are provided to go from a rectangular input (x, y) image to an "irregular" output (u, v) image.

DYUO copies, expands or compresses the (u, v) image vertically, for the cases DYUO - 1, DYUO > 1 AND DYUO < 1 respectively.

DYVO shears the image in the vertical direction, as shown in Figures 3 and 4:

Figure 3

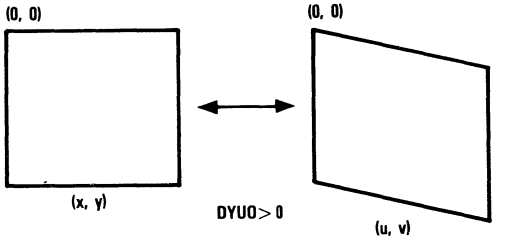
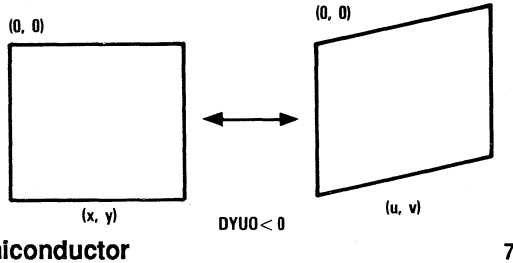


Figure 4



Meaning of Nonlinear Terms

There are two useful ways to look at the DXUU, DXUV, DYUU, DYVV, and DYUV expressions. On the one hand, they are the coefficients of U^2, U*V and V^2 for the separate X and Y equations (with a minor adjustment; see the next section). On the other hand, they can be thought of as second derivatives (or, more correctly, second-order finite differences). Thus, for example, the positive half of the parabola $y = 2*U^2$ has a positive second derivative $d^2Y/dU = 4$ and, indeed, setting DYUU = 4 and DXUO = 1 transforms the line U = 0 to $Y = 2*U^2$ (again, with the necessary coefficient adjustments). Likewise, $d^2X/dUV = c1$ (a constant) has the continuous solution X = c1*U*V + (terms in U and V alone), and with the TMC2301, setting DXUV = c1 results in a c1*U*V term in the solution for X (see above).

With either interpretation, the second-order inputs perform the following operations (again, we consider the "backward" mapping from the rectangular (u, v) ouput to the (x, y) input):

DXUU: Just as DXUO expands or compresses an image in the horizontal direction linearly, so DXUU expands or compresses it nonlinearly (with U^2). For example (again ignoring adjustments, i.e., in this example, DXUU is presumed to directly multiply U^2):

Figure 5

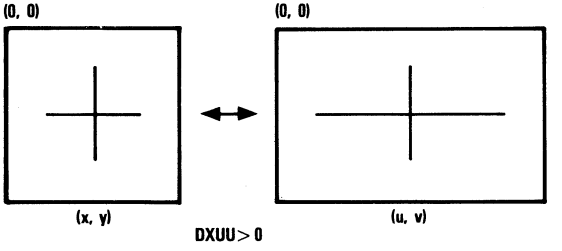
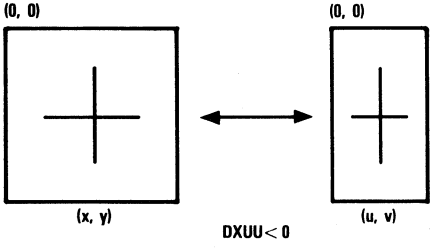


Figure 6



DXVV: This produces a nonlinear "warp" in the horizontal direction as one moves down a column, as in Figures 7 and 8:

Figure 7

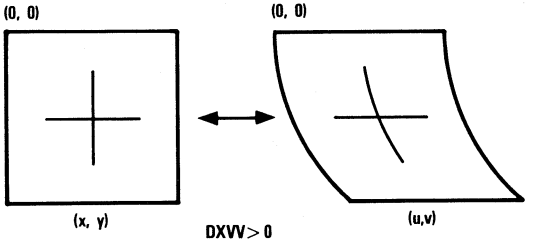
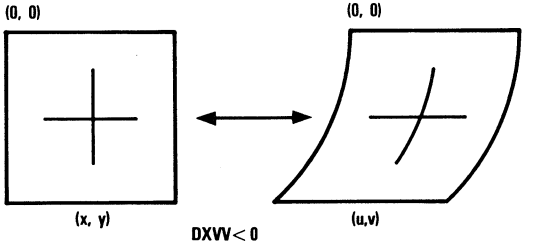


Figure 8



DXUV: This produces another horizontal warp, in which the lower righthand corner of the (u, v) image undergoes the maximum horizontal deflection, whereas the upper and left-side borders (where u and v are small) are warped least, as in Figures 9 and 10:

Figure 9

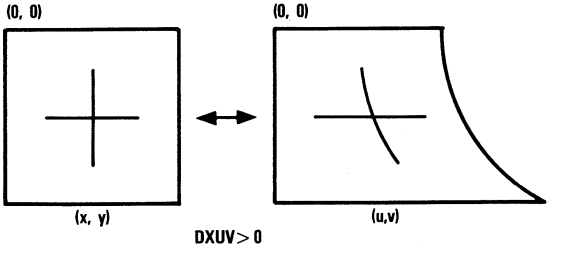
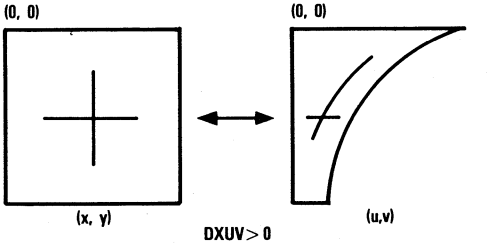


Figure 10



DYUU: This produces a nonlinear warp in the vertical direction, as in Figures 11 and 12:

Figure 11

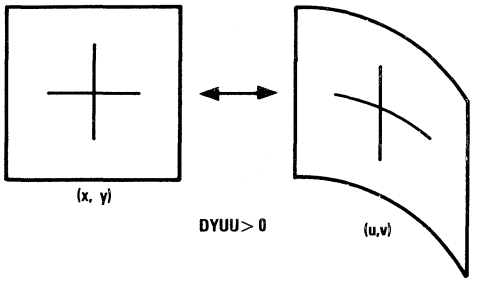
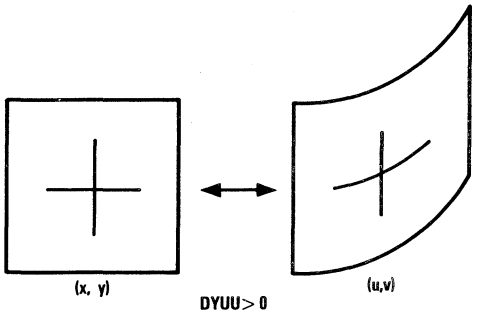


Figure 12



DYVV: This expands or compresses in the vertical direction non-linearly, as in Figures 13 and 14:

Figure 13

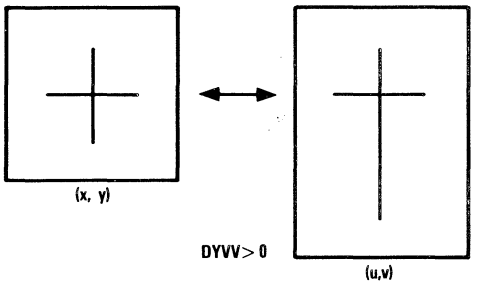
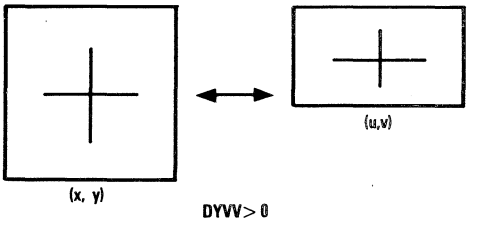


Figure 14



DYUV: This warps the curve in the vertical direction, in which the lower righthand corner undergoes the maximum vertical shift, as in Figures 15 and 16:

Figure 15

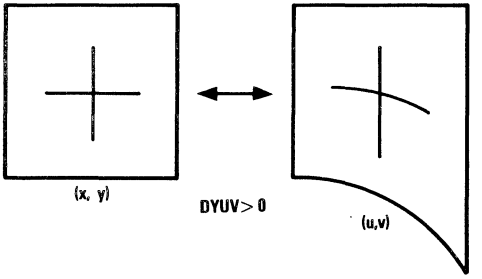
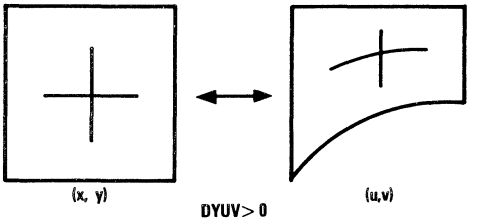


Figure 16



Compensating the Coefficients (Not Applicable to DXUV, DYUV)

The "pure" second-order terms are implemented by the TMC2301 with a double accumulation which results in the form (e.g.) Y = DYUU*(U^2 - U)/2. Thus, when we wish to implement a formula of the form Y = c1*U^2 + c2*U, we need the following coefficient transformation:

$$DYUU = 2*c1;\ DYUO = c1 + c2$$

The same (analogous) transformation holds for DXUU, DXVV, DYVV, DXUO, DXVO and DYVO. For examples, see below. DXUV and DYUV require no adjustment.

Technique

Each nonlinear situation requires a different treatment, mainly because the functional forms can be hard to identify, and nonlinear matrices cannot be cascaded as the linear operations such as translation, rotation and scaling can be (see TP-36). A possible generalized approach is as follows:

a. Superimpose the input and output images with the output (u, v) image aligned with an axis, if possible, so that the U and V functional forms are dimensionally separable in terms of the axes.

b. Estimate a functional form of the input (x, y) image. If necessary, define a new set of axes to help with this step.

c. Working from the image backwards, map the image into the intermediary axis set (if any), rotate the intermediary axes to the u, v axes (or the u', v' axes set), then express the desired U and V functional forms.

d. Remember to adjust the coefficient on any pure first and second-order terms (DXUU, DXVV, DYUU, DYVV, DXUO, DXVO, DYUO, DYVO).

Examples

I. Keystoning

Say that the image (in the x, y plane) is of the form illustrated in Figure 17, with "keystoning" distortion and horizontal curvature, and it is desired to correct the perspective and restore the picture to its rectangular form (Figure 18). (The keystoning is rather extensive, to make the example easy to follow.)

Figure 17

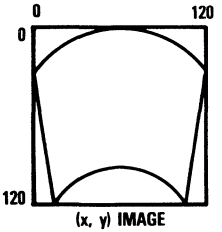


Figure 18

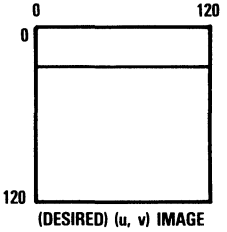
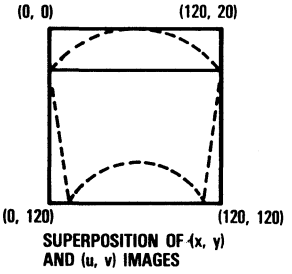


Figure 19



Step a, the superposition, is illustrated in Figure 19. Since the X and Y components are easily separable (the sides are a function of v, and the top and bottom are a function of u), no rotation is necessary.

Step b: To get the functional forms, consider the sides first. To map the vertical lines U = 0 and U = 120 into the x, y image, we need a horizontal shear to the right (DXVO > 0) for the U = 0 line and, then, a horizontal warp to the left (DXUV < 0) to correct the righthand side. Since both operations work as functions of the original u, v space, the horizontal warp will not affect the left edge.

The shear (DXDV) affects the mapping of the (u, v) rectangle, as in Figure 20:

Then, the warp (DXUV) brings the right edge back, as in Figure 21:

Figure 20

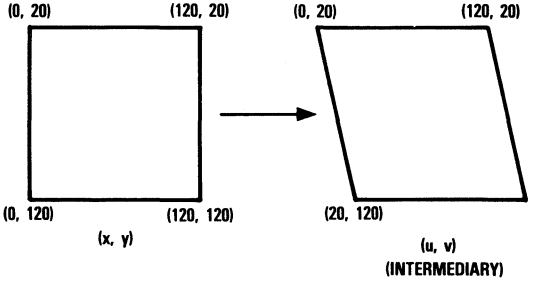
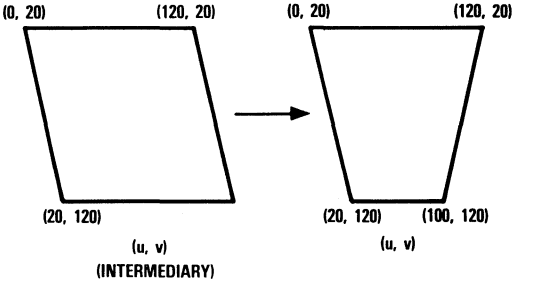


Figure 21



Taking as our functional form, then:

$$X = U + c1*V + c2*U*V;$$

Step c: Since the shear begins at V = 20 and is linear thereafter, we translate the starting point:

$$X = U + c1*(V - 20) + c2*U*(V - 20)$$

Since the lefthand side is not affected by c2 and needs a slope of 1/5, we know c1 = 0.2. Then, plugging in points, e.g., X(120, 120) = 100, we get c2 = −0.0333. Expanding:

X = 1.0667U + 0.2*V − 0.00333*V*U − 4; this can be checked by substituting in other test points, e.g., (U, V) = (0, 20), (60, 20), (120, 60), etc.

So DXUO = 1.0667, DXVO = 0.2, DXUV = 0.00333, XO = −4

II. Correcting the Horizontal Curvature

Turning to the top and bottom, one must choose a functional form. Unfortunately, one is limited to polynominal forms; a circle is not available, since Y will equal the square root of some polynominal function in U. However, an arc can be closely approximated by a parabolic form, and that is the obvious choice here. Since Y is positive going downwards, and the vertex of the parabola is translated along the u-axis by 60, we suppose a form:

$$Y = A*U^2 + B*U + C + V$$

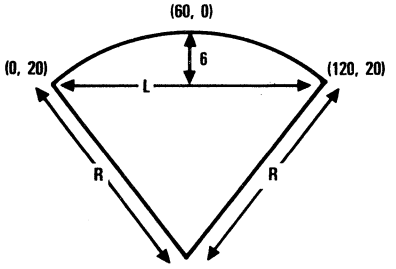
The point (U, V) = (0, 20) maps to Y = 20, and the points (U, V) = (60, 0) and (120, 20) mapping to Y = 0 and Y = 20 respectively. Substituting this yields:

$$Y = (1/180)*U^2 - (2/3)*U + V$$

But here the DYUU term requires coefficient transformation, as above. Since c1 = (1/180) and c2 = (-2/3),
DYUU = 2*c1 = 0.01111 and DYUO = c1 + c2 = -0.66111.
The "V" term requires DYVO = 1.

Inputting these 7 coefficients (with others equal to 0) will transform the x, y image to the rectangular boundary of U = 0 to 120, V = 20 to 120. Of course, if the original image weren't precisely parabolic, there would be some error. In this case, if the top and bottom were actually circular, we could easily calculate from Figure 22:

Figure 22



$R = (L/2)^2 + (R - abs(b))^2$
$R = (L/2)^2 + b^2) / 2*abs(b) = 100$, and thus

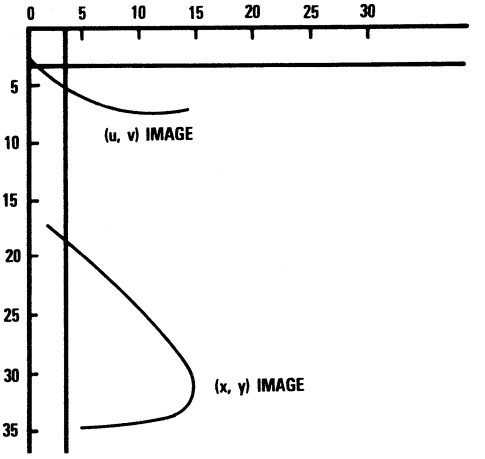
$(60 - X)^2 + (1100 - Y)^2 = 10000$. Comparing these values with the parabolic ones, one can determine the accuracy of the approximation. If you wish to make it even closer, you can use a least-squares curve fitting technique by taking more points from the "ideal" circle.

(NOTE: To get the functional form desired, of course, the user may employ any standard technique for translating a series of points into an explicit functional description. With only first and second-order terms available, however, something like the above approach is usually easiest.)

III. A Tutorial Example

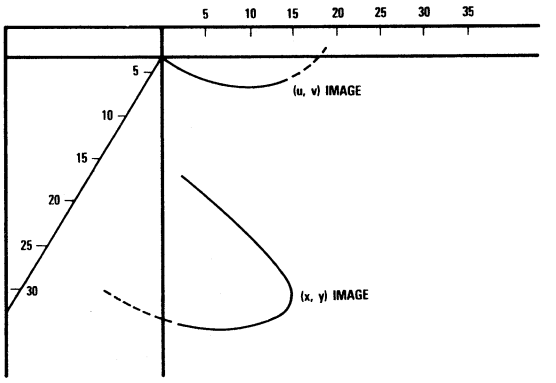
We will now consider a more complex example (with little practical significance) to illustrate the general technique. Say you were given the following input image (bottom curve of Figure 23) and desired output image (top curve of Figure 23):

Figure 23



Step a, to superimpose the images with the U and V functional forms aligned with an axis, is already done. Step b is to estimate a functional form of the input image. To help do this, we introduce intermediate axes Zx and Zy, extend the input image to be symmetrical, and measure distances from the new axes to some known image points (Figure 24):

Figure 24



Clearly, we can again estimate a parabolic form for the x, y image in terms of Zx and Zy:

$$Zy = A*(Zx - 20)^2 + B*(Zx - 20) + C$$

c. Using some points, e.g., (Zx, Zy) = (10, 10), (20, 30) and (30, 10), yields:

$$Zy = (1/5)Zx^2 + 8*Zx - 50,\ Zx = 10 \text{ to } 25.$$

Now, this axis (from 10 to 25) must be mapped to the eventual U axis, which can be done by the standard rotation matrix:

$$\begin{vmatrix} X' \\ Y' \end{vmatrix} = 1\ [Z,\ Z,\ 1] \begin{vmatrix} \cos 120° & -\sin 120° \\ \sin 120° & \cos 120° \end{vmatrix}$$

Substituting for Zy, we get:

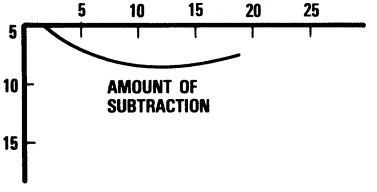
$$X' = 0.173*Zx^2 + 6.4287*Zx - 43.3$$
$$Y' = -.1*Zx^2 + 4.866*Zx - 25$$

Now, sweeping X' through 10 to 25 is the same as sweeping Zx through 10 to 25, so we have the x, y image as a function of the U-axis, U = 10 to 25. But we want to sweep U from 0 to 15, so we shift:

$$X = -0.173*(u + 10)^2 + 6.428*(u + 10) - 43.3$$
$$Y = 0.1*(U + 10)^2 + 4.8666*(U + 10) - 25$$

Now, we have the original (x, y) curve by tracking along the U-axis from 0 to 15. But we want to generate it by sweeping through the output curve, i.e., $V = -(1/30)*U^2 + (2/3)*U$. So that this translates into the desired (x, y) image, we need to add 1 to Y for each increment of V (a Y = V term, i.e., DYVO = 1, as is normal in a copy; see above) and, then, subtract the expression for V above from each Y point. (See Figure 25):

Figure 25



This yields (expanding) $Y = V - p.0666*U^2 + 2.2*U + 13.66$. The U values along the curve will be the same as those along the axis. Finally, we need to compensate for the DXUU and DYUU coefficients:

DXUU = 2*C1 = 2*(−0.173)= −0.346;
DXUO = C1 + C2 = 2.968 − 0.173 = 2.795;
DYUU = 2*(−0.0666) = −01333;
DYUO = 2.2 + (−0.0666) = 2.1333;

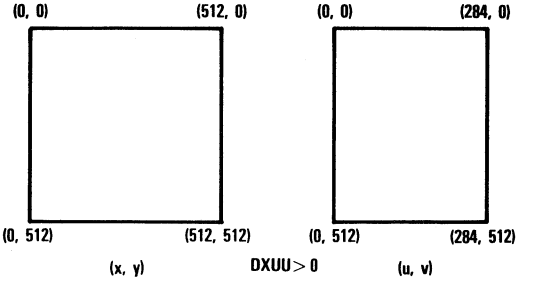
The other coefficients map directly: DYVO − 1, XO = 3.68; YO = 13.66.

Inputting these coefficients will indeed transform the given (x, y) input image to the given (u, v) output image.

Test Images

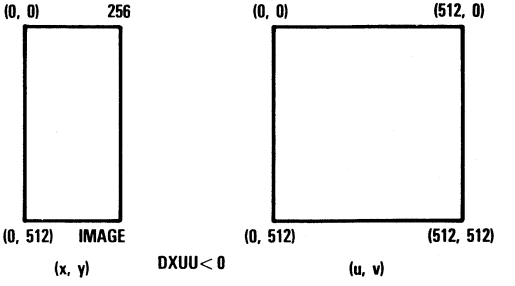
The above examples all take an "irregular" input (x, y) image and map it to a rectangular output (u, v) image. For the purposes of testing (or for intentional distortion of an image), the reverse process is useful: taking a rectangular (x, y) input and producing an "irregular" (u, v) output. Below are 12 examples (assuming a full-scale screen of 512x512 pixels) of using 1 coefficient at a time to transform a rectangular input. The pure second-order coefficients have been compensated, as described above (e.g., in the first example below, we achieve $X = 1/512\ U^2$ by setting DXUU = 2*C1 = 1/256 and DXUO = C1 + C2 = 1/512).

Figure 26



DXUU = 0.00694444
(0.0000 0001 1100 0111 0001)
DXUO = 0.00347222
(0.0000 0000 1110 0011 0101)
DYVO = 1

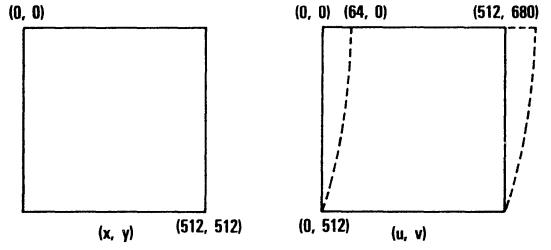
Figure 27



DXUU = 1/512 = -2^{-9}
(...111.1111 1111 1000)
DXUO = 1 − 1/1024 = 1023/1024
(0.1111 1111 1100 0000)
DYVO = 1

Figure 28

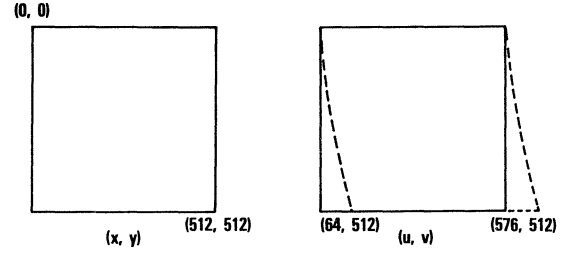
DXVV > 0 (WITH OFFSET)



DXVV = 1/2048 = 2^{-11}
(0.0000 0000 0010)
DXUO = 4097/4096
(1.0000 0000 0001 0000)
XO = −64
(...111000000.00...)

Figure 29

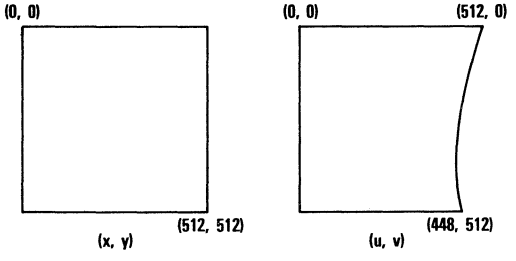
DXVV < 0



DXVV = −1/2048
(...111.1111 1111 1110 0000)
DXVO = −1/4096
(...111.1111 1111 1111 0000)
DXUO = 1
DYVO = 1

Figure 30

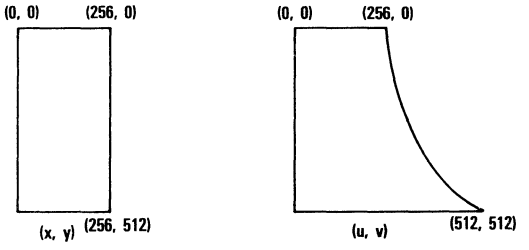
DXUV > 0



DXUV = 2.7902 10^{-4}
(0.0000000000100100100)
DXUO = 1
DYVO = 1

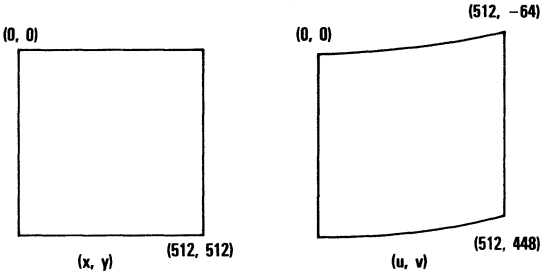
Figure 31

DXUV < 0



DXUV = 2^{-10}
(...111.1111 1111 1100)
DXUO = 1
DYVO = 1

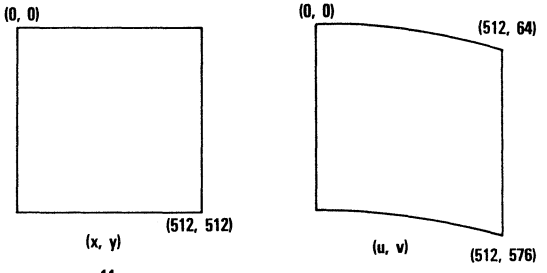
Figure 32



DYUU = 2^{-11}
(0.0000 0000 0010)
DYVO = 1
DXUO = 1

Figure 33

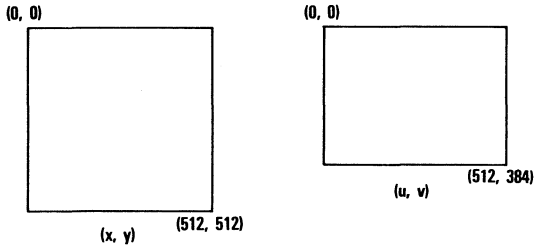
DYUU < 0



DYUU = -2^{-11}
(...111.1111111111100000)
DYUO = -2^{-12}
(...111.1111111111110000)
DYVO = 1
DXUO = 1

Figure 34

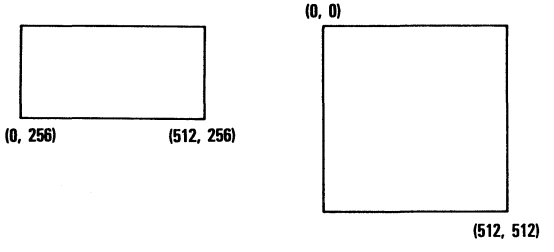
DYVV > 0



$DYVV = 6.94444X10^{-3}$
(0.0000000111000111001)
$DYVO = 3.472222X10^{-3}$
(0.0000000011100011110)
DXUO = 1

Figure 35

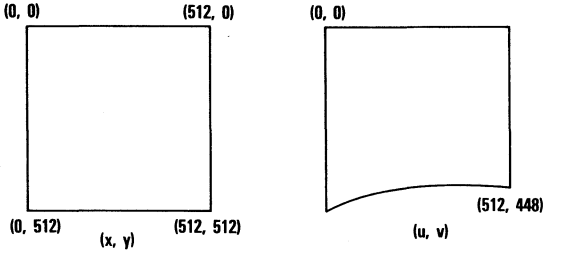
DYVV < 0



$DYVV = -1/512 = -2^{-9}$
(...111.111111111000)
DYVO = 511/512
(0.111111111000)
DXUO = 1

Figure 36

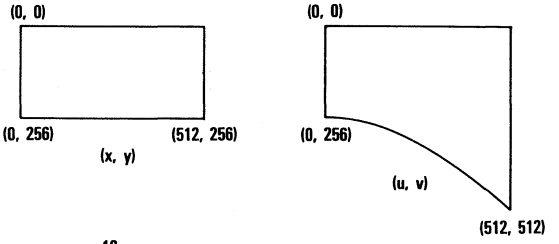
DYUV > 0



$DYUV = 3/2.7902X10^{-4}$
(0.0000000000100100)
DYVO = 1
DXYO = 1

Figure 37

DYUV < 0

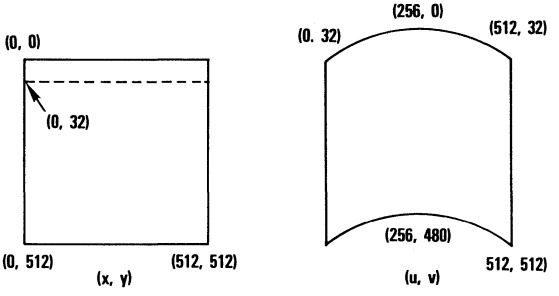


$DYUV = -2^{-10}$
(...111.111111111100)
DYVO = 1
DXUO = 1

Test Image for Keystoning

To use several parameters, we simply reverse the procedure given above, e.g., given a rectangular (x, y) input and wishing to create horizontally-curved (u, v) output (Figure 38):

Figure 38



$DYUU = -2^{-10}$
(111.1111 1111 1100)
$DYUO = 2^{-2} - 2^{-11}$
(0.0011 1111 1110 0000)
DYVO = 1
DXUO = 1

We can assume a parabolic form:

$$Y = Au^2 + Bu + V + C$$

Substituting points, e.g.:

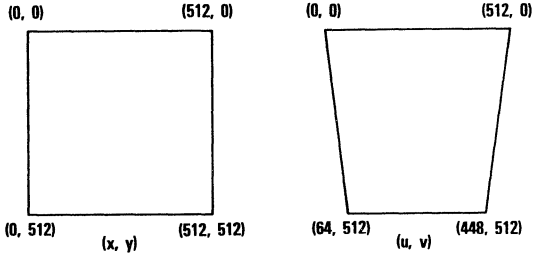
Y = 32, (U, V) = (0, 32)
Y = 32, (U, V) = (256, 0)
Y = 512, (U, V) = (512, 512)
Y = 512, (U, V) = (256, 480)

One arrives at $Y = 1/2048\ U^2 + 1/4\ U + V$, which leads to the parameter assignment listed on Figure 38 (DYUU = 2*(-1/2048); DYUO = -1/2048 + 1/4.

Test Image for Keystoning

Producing a keystoning effect from an input rectangle requires some approximation. When we mapped from a (u, v) rectangle to an (x, y) keystoned image, the sides u = 0 and u = 120 were constants and, thus, the equation
X = a*U + b*U*V + c*V + d became a linear function in V. If, however, we try to achieve the following transformation in Figure 39:

Figure 39



we find that the X = a constant = a*U + b*U*V + c*V does not allow U or V to be expressed as a linear function of the other. Nevertheless, we can perform a 4-point mapping to achieve a good approximation, as follows:

Mapping Points:

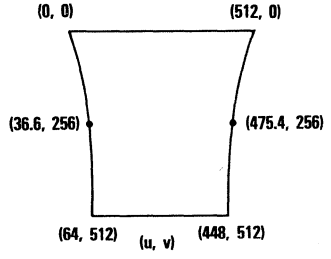
X (0, 0) = 0
X (512, 0) = 512
X (64, 512) = 0
X (448, 512) = 512

Solving four simultaneous equations by substituting these points into X = AU + BV +CUV + D, we arrive at:

A = DXUO = 1; B = DXVO = 1/6; C = DXUV = 1/1536; D = XO = 0

The result is a mapping with ideal (exact) values at the test points (corners) but a slight curvature along the vertical sides of the output image. This curvature amounts to a maximum of 4.6 pixels halfway between the top and bottom (see Figure 40).

Figure 40

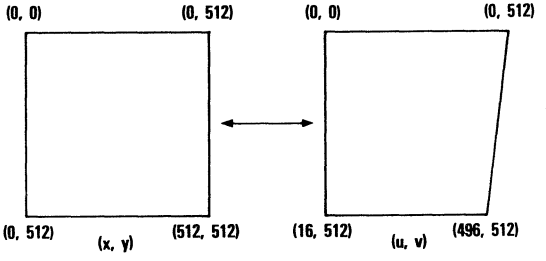


If one wishes for more linear sides at the cost of some error at the corner points, one can use a balanced mapping as follows:

X(21.333, 170.666) = 0
X(42.666, 341.333) = 0
X(490.666, 170.666) = 512
X(469.333, 341.333) = 512

The degree of curvature error improves for cases of milder keystoning and worsens for cases of more extreme keystoning. For example, in the transformation in Figure 41, a mapping of the four corners results in X = U - 1/30*V + 1/7680*U*V. Here the maximum curvature (again halfway down the output image) is only 0.26 pixels off from the ideal (linear) result. By contrast, if the keystoning extends to X = 128 and X = 384 on the bottom of the output, the maximum error (with corner mapping) can be as high as 20 pixels. For cases such as this, it is certainly advisable to use a balanced mapping, choosing points 1/3 and 2/3 of the way down both sides, in order to reduce the curvature.

Figure 41



The TMC2301's nonlinear terms can be put to use in a wide variety of application-specific ways. One can, e.g., flatten out curved surfaces by simply applying a pure second order term (with rotation, if necessary). The magnitude of the second-order coefficient can be calculated by mapping points estimated from the size and location of the original image on the screen, as above. Similarly, one could flatten out an object, which is tilted away from the camera by mapping the four corner points. In cases like these, the coefficients have to be estimated and adjusted according to the particulars of camera angle and image location.

TMC2302P5C Demonstration Board

The TMC2302P5C Demonstration Board

Introduction

The Raytheon TMC2302P5C Demonstration Board is designed to demonstrate some of the image manipulations possible with the TMC2302 Image Manipulation Sequencer. The Demonstration Board stores a source image up to 512 x 512 eight-bit pixels. The TMC2302 addresses the source image elements in a manner determined by the type of manipulation being performed. Each addressed pixel proceeds through a color look-up table (TMC0171) prior to display. The TMC0171 Color Palette maps each of the 256 possible color values to the 262,144 displayable pixel locations.

The TMC2302 can perform up to a third-order warp on the source image. The software for the Demonstration Board allows the user to individually edit the coefficients controlling the warp. The software can also generate coefficients based on mouse-driven parameters or pseudo-random sequences.

The Demonstration Board performs a few of the large number of image manipulations possible with the TMC2302. The Demonstration Board performs only nearest neighbor resampling on two-dimensional images. When used with a multiplier-accumulator (Raytheon's TMC2208 and TMC2210) or a multiplier-array (Raytheon's TMC2246, TMC2249 or TMC2250) the TMC2302 is capable of convolutions and bi-linear and bi-cubic interpolations. These interpolations produce much smoother images (fewer aliased artifacts, jagged edges) than the nearest neighbor resampling performed by the Demonstration Board.

Configurations

the Demonstration Board and its software are designed to run on an IBM-compatible PC, XT, AT, 386 or 486 personal computer. It will run in a PC bus-compatible slot, or from an IBM PC type parallel port. If a math coprocessor (8087, 80287, 80387 or the coprocessor section of an 80486) is present in the host computer, the supplied software will use it. If a math coprocessor is not found, the floating-point operations will be done by the host processor. This may cause the system to run more slowly than ti would if a math coprocessor was present.

Some of the demonstration software requires a three button mouse with MSmouse driver installed on the host computer. If the software can't find the driver or the mouse, it will indicate so and prevent those routines from executing.

The amount of main system memory required for the demonstration program is about 150K bytes.

There are two independent options for installation. The first option determines how the host PC communicates with the Demonstration Board. The second option determines how the monitor(s) are connected to the Demonstration Board and the host PC.

Host Connection

The Demonstration Board can be installed in a PC-compatible slot in the host computer, or run from a parallel port. The PC slot installation can be more convenient for long-term installations in one host computer. The parallel port installation does not require the PC case to be removed, but an additional cable and external power supply are required.

A Demonstration Board installed in the host computer will use I/O ports 300-307h and 310-317h. If any other devices in the system respond to these addresses, the board will not operate properly and system damage could result. Check the address ranges used by network or interface boards to ensure that there will be no conflict.

If the Demonstration Board is to be operated from the parallel port of the host computer, then an adapter cable is needed to connect the parallel port to the dual-row header on the Demonstration Board. This adapter cable is not supplied with the board, but is readily available from computer supply companies. An external power supply (+5 Volts at 2 Amperes) with a disk drive style power connector will be needed. The cable pin functions are shown in Section 4.

The board may respond faster when installed on the host computer AT bus, but this may not be apparent in a 12 MHz AT or 386 system.

Monitor Configurations

A single VGA monitor may be shared between host computer display (text) and Demonstration Board display (image). A separate monitor (VGA or an RS-170 block sync monitor) can be used for the Demonstration Board display.

If a single monitor is used, the VGA output from the host computer is routed through the Demonstration Board to the monitor. The Demonstration Board switches the monitor over to its output under software control.

If separate monitors are used for the Demonstration Board output, the VGA pass-through cable is not used. The monitor for the Demonstration Board can be either a VGA type

multisync monitor or an RS-170 compatible color or monochrome monitor. The RS-170 monitor must handle block sync, since no serration pulses are provided.

Cables for connecting monitor(s) are not supplied with the Demonstration Board. For the RS-170 block-sync option the green video output should be used (connector pin function information is provided in Section 4).

Board Installation

If the board is installed in an internal slot in the host computer, the Demonstration Board edge-connector provides all the signal and power required. The board can be installed in any free PC or AT bus slot. Plug the board in and tighten the bracket mount screw ensuring that the board is properly supported and that it cannot touch adjacent boards. The 26-pin parallel port header (marked "J3") and the four-pin power connector (marked "J4") must be disconnected while the Demonstration Board is installed in the host computer.

If the board is operated outside of the host computer, the 26-pin dual-row connector on the Demonstration Board should be connected to a parallel port with an appropriate adapter cable. The dual-row header end of the cable connects to J3 with pin 1 closest to the "J3" marking. The other end of the adapter cable connects to a standard parallel I/O port. A 5 Volt D.C. regulated power supply capable of supplying 2 Amperes should be connected to J4. The pin functions for both cable connections are shown in Section 4.

Monitor Installation

If a single monitor is used, then the 15-pin hi-density end (three rows of pins) of the VGA input cable should be connected to the output connector on the host computer VGA card. The 15-pin Sub-D end (two rows of pins) is then connected to the Demonstration Board.

If a VGA monitor is used (whether as a single monitor shared with the host or as an additional monitor to the host computer display), the monitor cable should connect to the 15-pin hi-density D connector on the Demonstration Board. For RS-170 operation, the monitor connects to the 15-pin hi-density D connector.

Batch Demonstration Operation

A simple batch program is provided that will run with any of the installation configurations. The disk marked "TRWDEMO" contains all the software needed to run the batch demonstration. Insert this disk in drive A: and type: A:DEMO to start the program, which will load an image and manipulate it. See Section 2.4 or Section 6.0 if the program does not execute. If the program is to run from a hard disk, use MKDIR to make a directory and copy the files to the hard disk directory.

Problems

The demonstration program will display diagnostic messages when it starts. If the message "Demonstration Board not found" is displayed, the program was unable to locate the board on the PC bus or on a parallel port. If the Demonstration Board is installed in the PC bus, this error may be caused by another board at the same bus I/O addresses as the Demonstration Board. Some network and interface boards use the same addresses. Conflicting boards should be removed from the system. If the Demonstration Board is connected to a parallel port and is not found by the software, check the board power by observing the lit LED. If the LED is not illuminated, check the power supply voltage. Additionally, it may be necessary to check the adapter cable connections.

Software

The Demonstration Board is supplied with programs to manipulate images and perform diagnostic tests. The following programs are included:

a. TRWDEMO.EXE - the main demonstration program
b. TRWDIAG.EXE - the diagnostic program
c. TRWOFF.EXE - a program to return the display to the VGA card
d. TRWSRC.C - a sample C program to run the Demonstration Board
e. DEMO.BAT - a batch file to run a short demo
f. TRWSCRPT.TXT - the script that is piped to TRWDEMO by DEMO.BAT

TRWDEMO

This program executes the various demonstrations. When initialized, it searches for the Demonstration Board on the parallel ports starting at the highest addressed parallel port. After checking the parallel ports, the PC bus is examined for the presence of the Demonstration Board. The test of a parallel port will disrupt any current print job on that port. The automatic port search can be overridden, if necessary, with the command line option /p:# which causes the parallel port at base address # to be used (i.e. "trwdemo/p:378" uses the parallel port that starts at address 378h). The command line option /i causes the program to only look for a Demonstration Board installed on the host computer bus.

All other configuration options are automatically sensed. Configuration and debugging messages are displayed as the program starts to help isolate problems.

There are four command line options. The /p and /i options were discussed above. The /s command line options causes the program to not wait for a key to be struck to stop the current sequence. This is useful for batch files, since the key wait routine will not see characters in the batch file. The /f option causes the program to use an optimized math coprocessor routine for some calculations. This results in faster execution, but requires the presence of a math coprocessor. This may be beneficial on slower machines that have a coprocessor installed such as an 80287 on a 286 system or an 8087 on an 8088

system. If the /f option is not specified, the program will automatically use the coprocessor, if present. If no coprocessor is found and the /f option is not specified, the host processor will do all computations. If the /f option is specified and no coprocessor is present, program operation is unpredictable.

After the program has determined the configuration and location of the Demonstration Board, a list of available commands is displayed. A command is invoked by entering the command number followed by [cr]. The commands are:

0 - Terminate

This command causes the program to terminate and returns to C:>.

1 - Load Image

This command loads an image into the Demonstration Board source image memory. The program will ask for the file name of the image to load. The main demonstration program can load images into the Demonstration Board from several image formats. The extent on the image file name is used to determine the type of image being loaded. The following are supported:

a. .GIF 'Graphics Interchange Format' is a trademark of CompuServe, Inc.
b. .PIC Mouse Systems PC Paint Picture File Format is limited to 4- and 8-bit version 2.00 images.
c. .MAP 768 bytes of lookup table information followed by a 512 x 512 image. The format may change.
d. .RGB 512 x 512 image data uses a lookup table that maps the top 3 bits to red, the next 3 bits to green, and the bottom two bits to blue.
e. .BW 512 x 512 image data uses a lookup table that maps the values to a grey scale.

2 - Edit Coefficients

This command allows individual coefficients to be edited. More than one coefficient can be specified on a line. The [cr] key will switch the monitor back to allow editing of more coefficients. If no coefficients are entered, the [cr] key will return to the main menu. The values entered are floating point. Note that the higher order coefficients have dramatic effect and should be kept quite small. Also note that the target (screen) origin is at the beginning of the back porch (during blanking). For a Demonstration Board with 20 MHz clock displaying VGA, this means that pixels less than U = 40 or V = 33 will be blanked. A good starting command is "a0 -100 b0 -50 a1 1 b4 1" which sets $X_0(A_0) = -100$, $Y_0(B_0) = -50$, $dX/dU(A_1) = 1$, and $dY/dV(B_4) = 1$.

3 - Rotate

This command rotates the image 360 degrees in one degree increments.

4 - Warped Rotate

This command executes a combined warped rotation.

5, 6, 11, 12, and 14 - Various Random Warps

These command selections cause the image to be warped under control of the host computer. Typing a key on the keyboard stops the warp at the end of the current pass.

7 - Other

This allows changing of options that affect the way the image wraps around at its edges. The submenu allows you to select one of the following:

0	Clips to the image border. This is the default mode.
1	Wraps the image around in all directions.
2	Wraps the image around in quadrant 4, relative to the source image.
3	Clear coefficients between commands. This is a default mode.
4	Do not clear coefficients between commands. This allows editing of coefficients created during other transformations.

8 - Mouse Corner Warp

The mouse is used for this control point warp that uses the four corners of the image as the control points. When no mouse buttons are depressed, the upper left corner of the source image is moved by moving the mouse. The left, middle and right buttons control the remaining three corners of the image. Pressing the left and right mouse buttons simultaneously returns to the main menu.

9 - Mouse Rotate and Zoom

The mouse controls rotation and scaling of the image. Moving the mouse while holding no buttons, one button or two buttons changes rotation and scaling parameters. Simultaneously pressing the left and right buttons returns to the main menu.

10 - MONG

A paddle game. This uses vertical mouse motion to move the paddle up and down.

13 - Spin Down

This selection spins the source image while expanding it from a reduced size. The the image is reduced in size by clipping without minifying.

TRWDIAG - Diagnostic Software

TRWDIAG allows the Color Palette and image memory to be tested. This program has a menu similar to the one in TRWDEMO. Selecting the number for an option causes that test to be run. The image memory tests take quite a bit longer over the parallel port then

they do with the Demonstration Board installed on the host computer bus. The options are:

0 - Quit

This section terminates the program.

1 - Parameter Select

This allows changes to the parameters used by the tests. The check parameter allows only the writing of the pattern to memory, only checking a pattern that is already in memory, or both writing the pattern and checking the pattern. The pattern parameter controls the pattern used to check the memory. The triple pattern is good for address testing. The random pattern uses a polynomial based pseudo-random number generator. The H ramp and V ramp patterns produce an incrementing pattern across or down the source memory. The seed is used as a starting value for all tests. A value of zero should not be used with the random pattern. The offset controls the starting phase of the triple pattern. The count controls the number of times the test is run. A count greater than one causes the seed to be changed for each pass of a test.

2 - Image RAM Test

This selection tests the source image memory.

3 - DAC Test

This selection tests the image Color Palette memory in the TMC0171. The mask is determined by initial testing when the program starts. If the DAC is determined to only be 6 bits, then only the lower six bits are checked.

4 - DAC Mask Test

This selection tests the mask register in the TMC0171. It tests 256 patterns for each count. If there are no errors encountered, the mask is restored to its initial value.

5 - DAC Mask Set

This selection shows the current value of the mask and allows a new value to be entered. If the mask is set to FFh and the Combo Test (selection 8) is run, the DAC RAM array will be tested for sensitivity to asynchronous pixel inputs.

6 - Print RAM Region

This selection allows a region of the image RAM to be displayed as hexadecimal numbers.

7 - Print DAC Region

This selection allows a region of the DAC Color Palette RAM to be displayed as hexadecimal numbers.

8 - Combo Test

This option puts a triple pattern in the image RAM and a random pattern in the DAC and checks them. A triple pattern is then loaded in the DAC and a random pattern in the image RAM. These patterns are then checked and the mask is checked.

9 - Clock

This option makes a rough measurement of the frequency of the oscillator on the Demonstration Board.

10 - Border Image

This option writes a test image to image RAM and sets the TMC0171. Use TRWDEMO to view the image. The left edge is red, the right edge is green, the top is blue, and the bottom edge is yellow. Inside this bounding box are some color check blocks. Since the box border is a single pixel wide, the aliasing in the nearest-neighbor sampling may cause a border not to appear when the image is minified.

TRWOFF

This program switches the system to the VGA display if it is chained through the Demonstration Board. This can be a useful program to run from the system AUTOEXEC.BAT file to ensure that the computer does not boot with the display switched to the Demonstration Board output. This program searches for a bus-installed card first. If it does not find the Demonstration Board on the bus, then the parallel ports are checked. To go directly to a Demonstration Board on a specific parallel port, the /p:# command line option can be given (similar to the TRWDEMO/p option).

The Demonstration Board Hardware

Memory Map

The following table describes the memory locations for the registers that are used to control the Demonstration Board. These addresses are for a bus installed Demonstration Board. Other sections describe the translation used for addressing these registers from the parallel port.

Memory Map for 2302 Demonstration Board

Address	Type	Function	Bits
300	RD	Status Register	0 - VFLAG 1 - Monitor Select 0 2 - Monitor Select 1 3 - Monitor Select 2 4 - VGA feedthrough 5 - Relay 6 - Collision 7 - Control bit 7
	WR	TMC2302 data lower byte	
301	RD	-	
	WR	TMC2302 data higher byte	
302	RD	Vertical Clear	
	WR	TMC2302 Address	
303	RD	-	
	WR	Control Register	0 - 2302 Init 1 - Download 2 - Download Write 3 - Wrap Source 4 - Reserved 5 - Relay 6 - Overlay Enable 7 - Reserved
304	RD	RAM data	
	WR	RAM data	
305	RD	-	
	WR	RAM address YA<9..6>	
306	RD	-	
	WR	RAM address XA<7..0>	
307	RD	-	
	WR	RAM address YA<5..0>,XA9,CA8	

TMC0171 Color Palette Addresses

Address	Function
310	Write Mode Address Register
311	Palette Data
312	Mask
313	Read Mode Address Register
314	Write Mode Overlay Address*
315	Overlay Data*
316	Reserved
317	Read Mode Overlay Address*

* the Overlay function is not present for TMC0171 Color Palette

Control Register Functions

The control register (Address 303h) sets the base mode for the Demonstration Board.

2302 INIT	Setting and then clearing the 2302 INIT bit will initialize the TMC2302s.
DOWNLOAD	Setting the Download bit allows the image memory to be read.
DOWNLOAD WRITE	Setting both the Download and the Download Write bits allows the image memory to be written.
WRAP SOURCE	The Wrap Source bit causes the source image space to wrap around in both dimensions.
RELAY	When the Relay bit is cleared, the VGA input is passed through. When the Relay bit is set, the Demonstration Board image is passed through to the output connector.
OVERLAY ENABLE	The Overlay Enable bit enables a special mode that is used for MONG. In this mode the TMC2302 TVAL signals are used to set an overlay, instead of controlling the blanking region at the edge of the screen.

The TMC2302 control registers are set by writing the desired address in the TMC2302 Address register. Next, the lower byte of the TMC2302 data is written to the TMC2302 Data Low Byte register. Finally, the higher byte is written to the TMC2302 Data High Byte register. Writing the high byte causes the data to be written to the selected TMC2302. Bit 7 of the TMC2302 Address register selects the X-coordinate TMC2302 when LOW, and the Y-coordinate TMC2302 when HIGH. The TMC2302 addresses are use coefficient bit 32 as the bottom bit of the X and Y image address. The sub-pixel bits below bit 32 are ignored and the bits above bit 40 (for a 512 squared source space) are also ignored.

The image RAM is written by setting the Download and Download Write bits in the control register, the desired address is set in the three RAM address registers, and the data is

written to the RAM Data register. To read the image RAM, set the Download bit in the control register. Then, set the desired address in the three RAM address registers. Finally, read the data from the RAM Data register. The TMC0171 Color Palette mask should be cleared prior to setting the Download bit. The mask should only be set back to 3Fh after the Download bit cleared.

Status Register Functions

The status register (Address 300h) reads back status from the Demonstration Board.

VFLAG	VFLAG is active if a vertical blanking interval has come along since the last time VFLAG was cleared. VFLAG is cleared by reading the Vert Clear location.
MONITOR SELECTS	The Monitor Select bits (0, 1, 2) reflect the state of the Monitor Select bits coming back from the VGA monitor.
VGA FEEDTHROUGH	The VGA Feedthrough bit is LOW if the VGA chaining cable is connected from the Demonstration Board to a VGA card. Otherwise this bit is HIGH.
RELAY	The Relay bit reflects the status of the elay bit in the Control register.
COLLISION	The Collision bit indicates that the image and the overlay were coincident when in Overlay Enable mode. This bit is cleared by reading the Vert Clear location. Status bit 7 reflects the state of bit 7 in the Control register.

Parallel Port Access

To access a Demonstration Board on a parallel port, bit 2 of the parallel port control register must be set LOW. The parallel port uses an additional register on the Demonstration Board. This register is loaded by outputting the data on the parallel port data register and taking bit 3 of the parallel port control register HIGH and then LOW. The bottom five bits of this additional Demonstration Board register are the same as the bottom five address bits when the board is installed in the system bus. Bit 5 should be left LOW. If bit 6 is taken from a LOW to a HIGH, the readback shift register is loaded.

The parallel port control bit 0 is taken HIGH for a read to the Demonstration Board. The readback data is read one bit at a time on bit 7 of the parallel port status register. The readback data starts with the last significant bit, and is advanced to the next bit by taking bit 3 of the parallel port control register HIGH and then LOW. Since this will also load the additional register described above, bit 6 on the parallel port output data should be kept HIGH to keep from reloading the readback shift register. The parallel port inverts the readback data. The parallel port control bit 1 is taken HIGH for a write to the Demonstration Board.

Connector Pin Functions

This section gives the pin functions for the VGA output connector, the VGA chaining input connector, the PC slot edge connector, the parallel port connector, the auxiliary power connector, and the two signal probe headers.

Hi-Density VGA Output Connector (J1) Pinout

Pin	Signal	Pin	Signal	Pin	Signal
1	Red	6	Ground	11	Monitor Select 0
2	Green	7	Ground	12	Monitor Select 1
3	Blue	8	Ground	13	Horizontal Sync
4	Monitor Select 2	9	SP1	14	Vertical Sync
5	Ground	10	Ground	15	SP2

VGA Chaining Input Connector (J2)

Pin	Signal	Pin	Signal
1	Red	9	SP1
2	Green	10	VGA Sense
3	Blue	11	Monitor Select 0
4	Monitor Select 2	12	Monitor Select 1
5	Ground	13	Horizontal Sync
6	Ground	14	Vertical Sync
7	Ground	15	SP2
8	Ground		

PC Slot Connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	NC	A16	NC	B1	Ground	B16	NC
A2	D(7)	A17	NC	B2	Reset	B17	NC
A3	D(6)	A18	NC	B3	+5 Volts	B18	NC
A4	D(5)	A19	NC	B4	NC	B19	NC
A5	D(4)	A20	NC	B5	NC	B20	NC
A6	D(3)	A21	NC	B6	IRQ2	B21	NC
A7	D(2)	A22	A(9)	B7	NC	B22	NC
A8	D(1)	A23	A(8)	B8	NC	B23	IRQ5
A9	D(0)	A24	A(7)	B9	NC	B24	IRQ4
A10	NC	A25	A(6)	B10	Ground	B25	IRQ3
A11	AEN	A26	A(5)	B11	NC	B26	NC
A12	NC	A27	A(4)	B12	NC	B27	NC
A13	NC	A28	A(3)	B13	IOW	B28	NC
A14	NC	A29	A(2)	B14	IOR	B29	+5 Volts
A15	NC	A30	A(1)	B15	NC	B30	NC
		A31	A(0)			B31	Ground

Parallel Port Adapter Cable

J3 Pin	Parallel Port Pin	Signal	Use	PC Port
1	1	Strobe	IOR	Control Bit 0
3	2	D(0)	D(0)	Data
5	3	D(1)	D(1)	Data
7	4	D(2)	D(2)	Data
9	5	D(3)	D(3)	Data
11	6	D(4)	D(4)	Data
13	7	D(5)	D(5)	Data
15	8	D(6)	D(6)	Data
17	9	D(7)	D(7)	Data
19	10	Ack	VGA Sense	Status Bit 6
21	11	Busy	Readback Data	Status Bit 7
23	12	P.End	VFLAG	Status Bit 5
25	13	Select	-	Status Bit 4
2	14	Auto Feed	IOW	Control Bit 1
4	15	Error	-	Status Bit 3
6	16	Init Prt	Enable	Control Bit 2
8	17	Select In	Control Strobe	Status Bit 3
10	18	Ground	Ground	-
12	19	Ground	Ground	-
14	20	Ground	Ground	-
16	21	Ground	Ground	-
18	22	Ground	Ground	-
20	23	Ground	Ground	-
22	24	Ground	Ground	-
24	25	Ground	Ground	-
26	-	-	-	-

Auxiliary Power Connector (J4)

Pin	Signal
1	No Connect
2	Ground
3	Ground
4	+5 Volts

X Probe Connector (X-coordinate TMC2302 Signals)

Pin	Signal	Pin	Signal
1	Ground	2	Ground
3	TVAL	4	ENDD
5	TADR(3)	6	DONE
7	TADR(0)	8	TADR(2)
9	KADR(0)	10	TADR(1)
11	TWR	12	KADR(1)
13	KADR(2)	14	KADR(3)
15	SADR(2)	16	SADR(0)
17	SADR(3)	18	SADR(1)
19	ACC	20	SVAL

Y Probe Connector (Y-coordinate TMC2302 Signals)

Pin	Signal	Pin	Signal
1	SYNC (pulled up)	2	Ground
3	NOOP (pulled up)	4	CLK
5	TVAL	6	ENDD
7	TADR(3)	8	TADR(2)
9	TADR(0)	10	TADR(1)
11	SADR(2)	12	SADR(0)
13	SADR(3)	14	SADR(1)
15	Ground	16	SVAL

Jumpers

The table below shows the jumper positions for a 512 x 512 source space. The board should be positioned so that the bracket is towards the right. The jumper on W1 is vertical (up means connect the middle and top pins with the jumper plug). The remaining jumpers are horizontal (up means connect the top two pins together with a jumper plug).

Jumper Positions

Jumper	Position	Jumper	Position
W1	Up	W2	Middle
W3	Middle	W4	Up
W5	Up	W6	Up
W7	Up	W8	Down
W9	Down	W10	None
W11	Left		

Hardware Description

The TMC2302 integrated circuits are designed to provide the capability to rapidly manipulate images. The TMC2302P5C Demonstration Board allows the user to become familiar with the types of manipulations possible with the TMC2302. It also provides test points for examining the timing and control sequencing of the TMC2302.

The board has three major blocks. The first of these is the warp address generator, which consists of two TMC2302s (identified in the block diagram as the X TMC2302 and Y TMC2302). The TMC2302s operate at video rate and generate the address sequences for the manipulation being performed. The second major block is the Image RAM where the source image is stored. The TMC0171 Color Palette is the third major block. It converts the digital pixel values from the Image RAM into red, green,and blue signal levels for display on a video monitor.

The warp address generator provides X and Y addresses to the Image RAM. The TMC2302 generate these addresses at video rate, and generate most of the video timing information as well. The Target Valid (TVAL*) signals from the X and Y TMC2302s are used for video sync and blanking, respectively. The TMC2302s operate continuously and the target windows are set up to provide the appropriate Target Valid timing. The X and Y addresses index the appropriate pixel for the location currently being refreshed on the video display.

The Image RAM provides the appropriate pixel value for the address being indexed. This RAM is static and operates at the video pixel rate. The TMC0171 Color Palette uses the pixel data to address it's on-chip RAM (color look-up table or color palette). The color palette provides the red, green, and blue values for the pixel being refreshed. These levels are sent to the video monitor.

Hardware Interface

The Demonstration Board supports operation in a personal computer card slot or from a PC-compatible parallel port. When the board is operated from a parallel port, the port signals are converted to the same signals that would be generated from an internal PC card slot. The parallel port decode register holds the value that is used to simulate the lower bits of the address that would normally come from the PC bus. The ENABLE signal is HIGH to enable PC bus operation, and LOW for parallel port operation. When using the parallel port, ENABLE tells the decode logic to ignore the upper address bits. Reading back from the parallel port involves loading the Readback Shift Register with a data byte and then shifting the data to a parallel port status line, one bit at a time.

The Video Out signals come from either the TMC0171 Color Palette or the VGA Video In connector. If a single display is shared between the Demonstration Board and a VGA display board, then the Video Source Relays switch the two sources to the monitor.

Downloading

Each of the major functional blocks contains data that must be downloaded. These are the coefficients for the address generators, the source image for the Image RAM, and the color palette RAM data for the TMC0171. The TMC2302s and TMC0171 can be loaded at any time. The Image RAM must be switched into a special download mode. The TMC2302s do not allow readback of coefficients. The Image RAM and TMC0171 both allow their data to be read. The download mode (with one variation) is used to upload the Image RAM. When downloading (or uploading) the decode logic converts the PC bus address into a strobe for the section of board being addressed. These strobes are used to load data into RAMs or registers, or to enable data out of RAM or the Status Buffer. The Data Bus Transceiver isolates the heavy loading of the local data bus from the PC data bus.

When downloading, the TMC2302 Address Register and TMC2302 Low Data Register must be loaded before sending the high byte data. Writing the high byte causes the transfer of the high and low data to the address contained in the TMC2302 Address Register.

Downloading (or uploading) to (or from) the Image RAM is more complex. The Control Register download bit (bit 1: referred to as "Download" in the Demonstration Board instructions but named "DNLOAD" on the schematic drawings)s) must be set. This control bit changes the source of the Image RAM X and Y address from the TMC2302s to the RAM Address Registers. To enable write data to the Image RAM and to disable the Image RAM output buffers, another Control Register bit ("Download Write" in the instructions and "DNWR" in the schematic drawings) must be set. After these control bits have been set, the desired X and Y Image RAM address must be written to the RAM Address Registers. Then the image data byte can be read or written.

Programmable Array Logic

There are two Programmable Array Logic (PAL) devices on the TMC2302P5C Demonstration Board. One is used exclusively for decoding the addresses used to access the board. The other handles a potpourri of video functions.

The Decode Logic consists of the decode PAL and a decoder IC. The decode PAL generates all the read strobes and just the write strobes for the decoder IC and the TMC0171. The decoder IC decodes the individual write strobes for the registers and the Image RAM. All of the decode signals are asynchronous. The decode PAL uses different equations for PC bus and parallel port operation. The ENABLE signal (abbreviated ENAB in the PAL code) is HIGH for bus operation and LOW for parallel port operation. It changes the decode from using PC bus address lines A9-A0 to using the Parallel Port Decode Register lines A4, A2, A1 and A0. PWR and PRD are the TMC0171 write and read strobes. MORE is the enable to the decode IC to further decode a write operation. RAMDAT is a decode for either reads or writes to the Image RAM. For an Image RAM write operation, both RAMDAT and MORE will be active. STATUS is a read decode to the Status Buffer. DEN enables the Data Bus Transceiver, and is active for PC bus reads to any of the Demonstration Board, for PC bus writes, for parallel port writes, or for cases where the bus is quiescent (to keep the local data bus quiet by preventing it from floating for long periods).

The Video Timing PAL generates some of the video monitor control signals and two status flags. BLANK is the blanking signal to the monitor. The equations define the inactive state of BLANK, which means they define the active video display region (BLANK is the compliment of active display for each individual dot clock interval). For operation without either overlays or source image wrapping (normal mode), the pixels of the warped image are displayed if the source X and Y pixels were valid and the Y TMC2302 target region is valid. The Target Valid (TVAL) signal from the Y TMC2302 defines the normal active display region for the monitor. When source image wrapping is enabled, the SVAL X and Y signals are not used to clip the displayed area to the source image bounds. This causes the source image to wrap around to fill the entire displayable area of the screen. In overlay mode (used for MONG), the source image is always assumed to be in a displayable screen area. SVAL X and Y determine the displayable area for the source image. TVAL Y (abbreviated TVY in the PAL source) determines the overlay region independently from the source image region. The OL0 signal is activated for overlay region (not supported by the
TMC0171.)

For VGA display operation, VCNT1, VCNT2, and VSYNC generate a two line sync interval. Horizontal sync comes from the TVAL X signal. For RS-170 block sync, the TVAL X region is programmed to generate composite sync.

The Video Timing PAL also generates two flags that are available through the status buffer. VFLG is set when the X TMC2302 is done with the video display refresh sequence. Both TMC2302s continue refreshing the screen using the coefficients in their respective control parameter preload buffers. VFLG indicates to software that there is a vertical interval available to change the contents of the control parameter preload buffers before the new coefficient set is used. VFLG is cleared by writing to the decode location that generates the VCLR strobe. The

COLL flag is used only in overlay mode (for MONG). It indicates that the source image region (defined by SVAL X and Y) and the overlay region (defined by TVY) are at least partially coincident on the screen. This is used by MONG to determine when the image hits the paddle. Seasoned MONG players will note that it is possible for the image to take a quantum jump through the paddle without a hit being detected. COLL is cleared the same way VFLG is cleared.

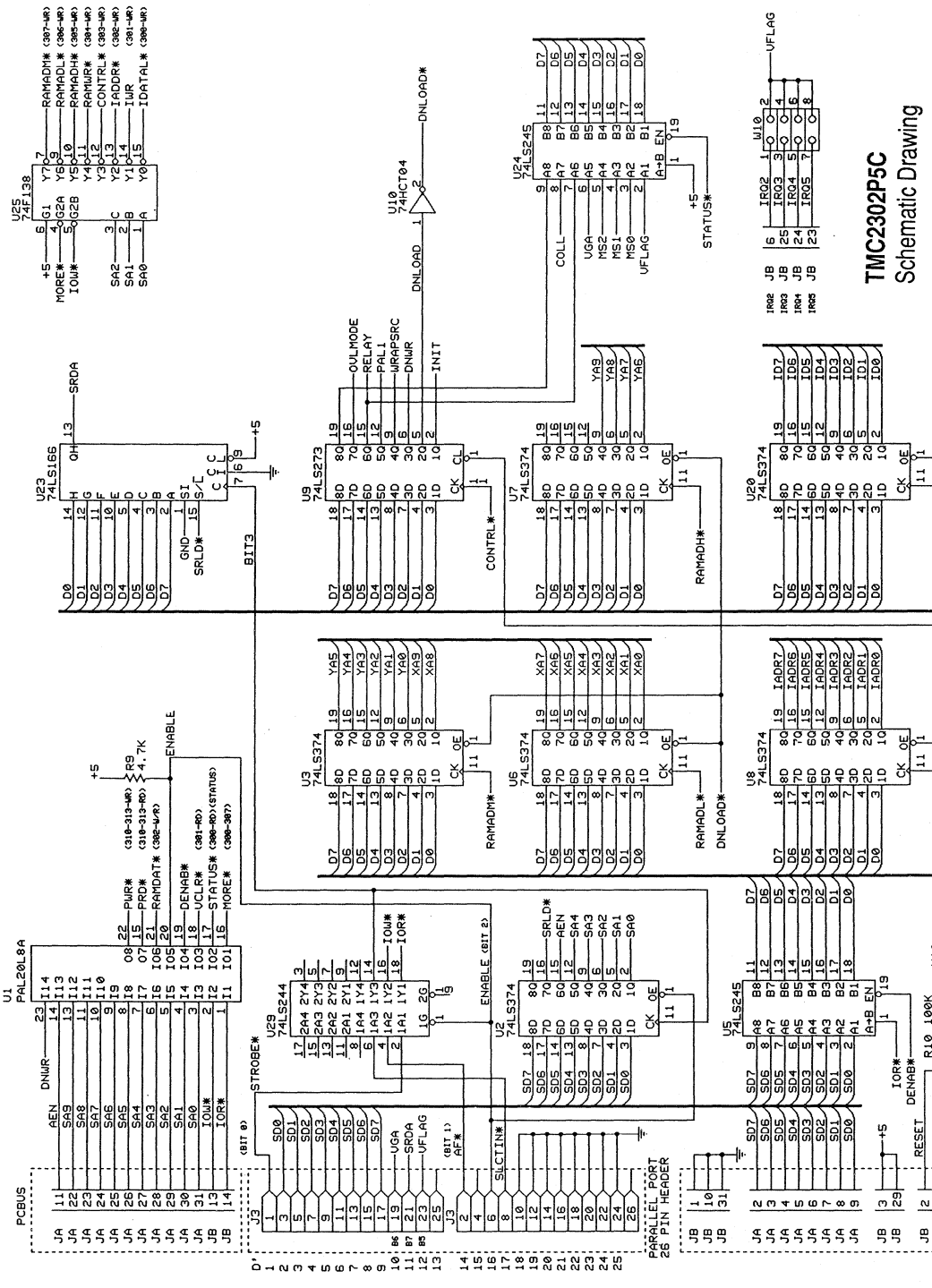
Each TMC2302 generates an independent target region valid signal (TVAL). Sync generally is the compliment of the TVAL signal from the X TMC2302, while blank generally comes from the compliment of the TVAL signal from the Y TMC2302. Blank is also used to blank the screen beyond the edge of the source image.

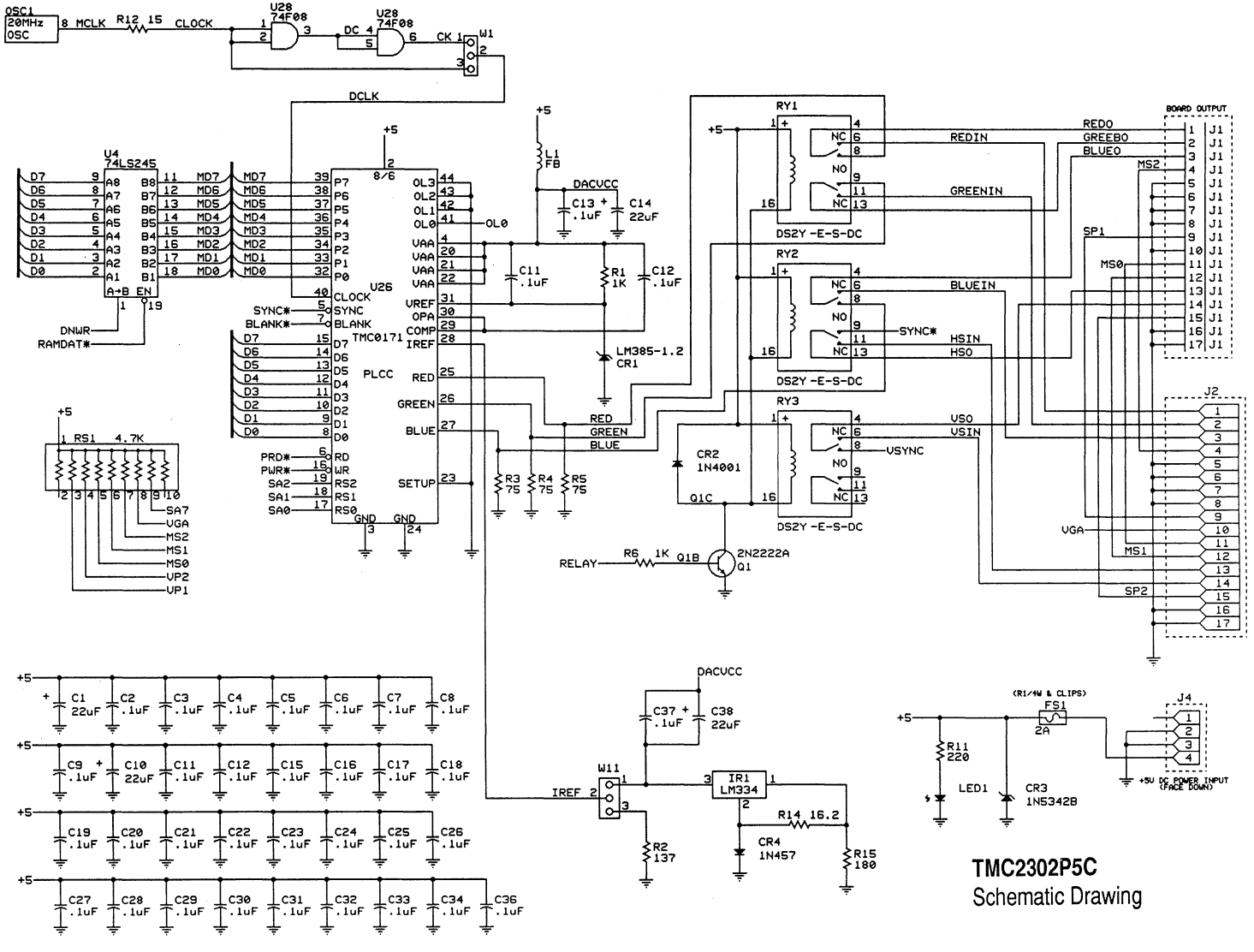
Listing for Decode PAL

```
MODULE trw2
TITLE 'TRW TMC2302P5C Decode PAL, 8-bit version'
trwu1  device  'P20L8';

A9,A8,A7,A6,A5,A4,A3,A2,A1,A0                pin 13,11,10,9,8,7,6,5,4,3;
AEN,!IOW,!IOR                pin 14,2,1;     "PC bus control lines
ENAB                         pin 20;         "high for PC bus, low for parallel port
                                             operation
DNWR                         pin 23;         "status bit, active for image download writes
!MORE,!PWR,!PRD,!RAMDAT      pin 16,22,15,21; "decode outputs
!DEN,!VCLR,!STATUS           pin 19,18,17;   " more decode outputs

HADDR =[A9,A8,A7,A6,A5,A4,A3,.x.,.x.,.x.];   "PC bus high address
ADDR  = [A9,A8,A7,A6,A5,A4,A3,A2,A1,A0];     "PC bus address
PADDR =[A4,.x.,A2,A1,A0];                    "Parallel port address
@radix 16;

EQUATIONS
PWR =     (HADDR == 310) & !AEN & IOW & ENAB          "310 - 317 Write
          # A4 & !AEN & IOW & !ENAB;                  "parallel port Write
PRD =     (HADDR == 310) & !AEN & IOR & ENAB          "310 - 317 Read
          # A4 & !AEN & IOR & !ENAB;                  "parallel port Read
MORE =    (HADDR == 300) & !AEN & IOW & ENAB          "300 - 307 Write to 2nd decode
          # !A4 & !AEN & IOW & !ENAB;                 "parallel port Write
RAMDAT =(ADDR == 304) & IOR & !DNWR & !AEN & ENAB "Image RAM Read
          # (ADDR == 304) & IOW & DNWR & !AEN & ENAB"Image RAM Write
          # (PADDR == 4) & IOR & !DNWR & !AEN & !ENAB"parallel port Read
          # (PADDR == 4) & IOW & DNWR & !AEN & !ENAB"parallel port Write
VCLR =    (ADDR == 302) & IOR & !AEN & ENAB           "Read to 302 clears the Vert Flag
          # (PADDR == 2) & IOR & !AEN & !ENAB;        "parallel port Read
STATUS =(ADDR == 300) & IOR & !AEN & ENAB             "Read to 300 returns status
          # (PADDR == 0) & IOR & !AEN & !ENAB;        "parallel port Read
DEN =     (HADDR == 300) & IOR & !AEN & ENAB          "Enable data to PC bus
          # (HADDR == 310) & IOR & !AEN & ENAB        "Enable RAMDAC data to PC bus
          # IOW & !IOR                                "IOR inactive term to prevent
                                                      parallel port fight
          # AEN & !IOR;                               "default - enable bus to prevent
                                                      float
END trw2
```

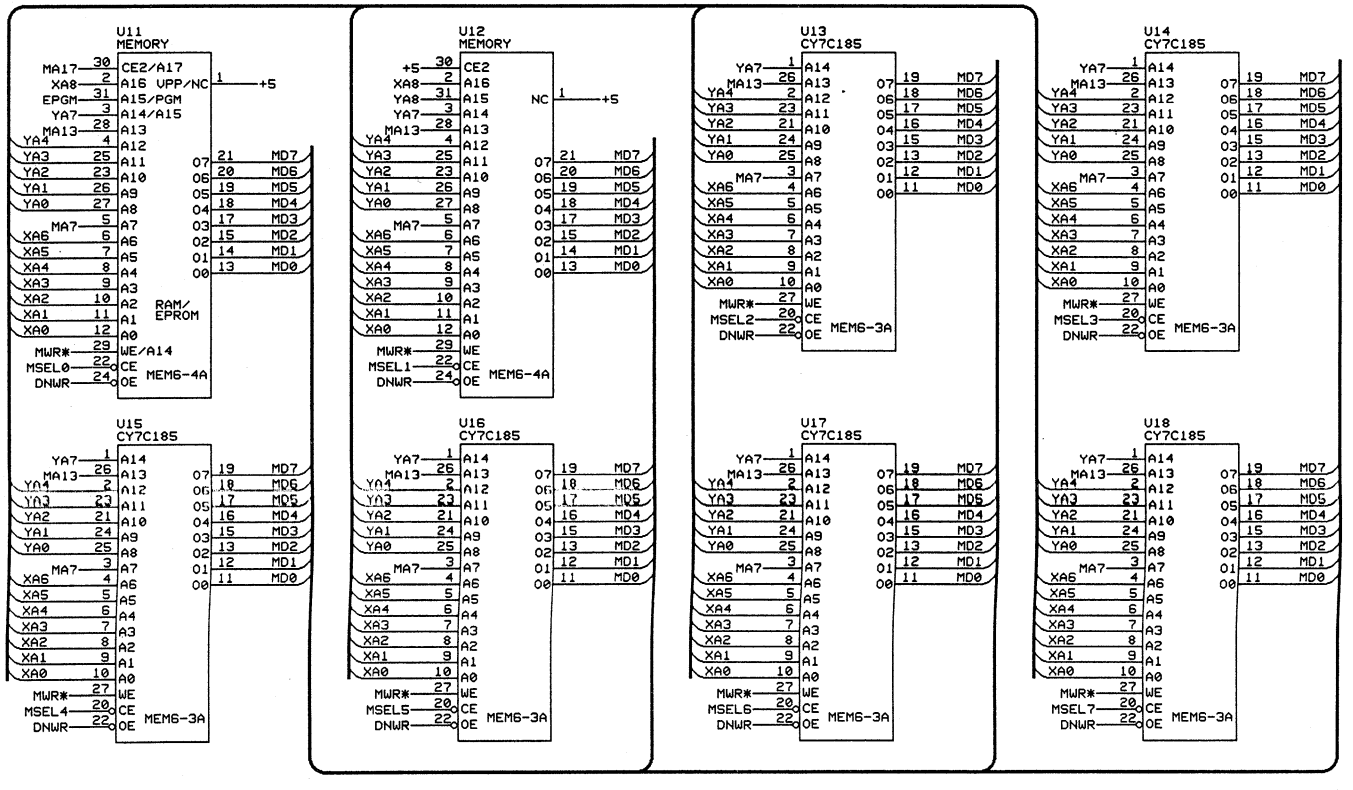
Listing for Sync PAL

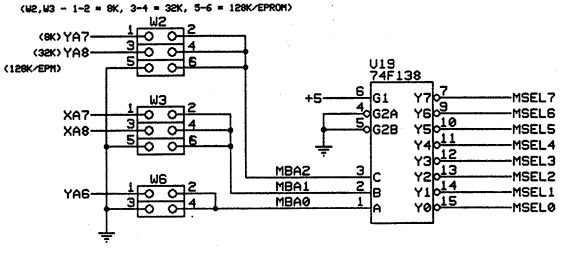
```
MODULE trw1  FLAG '-r2'
TITLE 'TRW TMC2302P5C Sync PAL'
trw2  device  'P20R6';

CLK          pin 1;     "Video dot clock
!OE          pin 13;    "Output enable
!SVALX       pin 2;     "Source Image Address Valid in X dimension
!SVALY       pin 3;     "Source Image Address Valid in Y dimension
!TVY         pin 4;     "Target Address Valid from Y 2302 (indicates active " video screen
                        region [versus blanking region])
WRAPSRC      pin 5;     "Wrap the source image by ignoring SVALX and SVALY
XDONE        pin 6;     "Done from X 2302 - sets VFLG
INIT         pin 7;     "Init from control register
ENDDX        pin 8;     "ENDD from X 2302, pulses during H-sync
ENDDY        pin 9;     "ENDD from Y 2302, active for last line
!VCLR        pin 10;    "Vertical Flag Clear
OVLMODE      pin 11;    "Overlay Mode bit from Control Register
!BLANK       pin 15;    "Video Blanking signal
VFLG         pin 16;    "Vertical Flag to status register
!VCNT2       pin 17;    "Counter bit 2 for VGA vertical sync
!VCNT1       pin 18;    "Counter bit 1 for VGA vertical sync
INITD        pin 19;    "Resynchronized Init to 2302's
COLL         pin 20;    "Collision Flag to status reister (for Overlay Mode)
VSYNC        pin 21;    "VGA Vertical Sync
OL0          pin 22;    "Overlay bit 0 to DAC

EQUATIONS
!BLANK =  SVALX & SVALY & TVY          "don't blank when source valid (& on screen)
          # WRAPSRC & TVY               "don't blank when Wrap Source mode set
          # OVLMODE & SVALX & SVALY    "don't blank source when in overlay mode
          # OVLMODE & TVY;             "don't blank for overlay region
VCNT1 :=  ENDDY                        "start VGA Vertical sync
          # VCNT1 & !ENDDX;            "and hold for next horizontal line
VCNT2 :=  VCNT1 & ENDDX;               "hold Vertical sync for all of second line
OL0 =     TVY & OVLMODE;               "in overlay mode, TVY indicates the overlay region
COLL :=   TVY & SVALX & SVALY          "set overlay mode collision - image & overlay hit
          # COLL & !VCLR;              "hold collision until Vertical Clear command
INITD :=  INIT;                        "synchronize INIT into 2302's
!VSYNC :=VCNT1 # VCNT2;                "VGA Vertical sync
VFLG :=   XDONE & !VCLR                "set Vertical Flag - end of 2302 screen refresh
                                       sequence
          # VFLG & !VCLR;              "hold Vertical Flag until Vertical Clear command
END trw1;
```

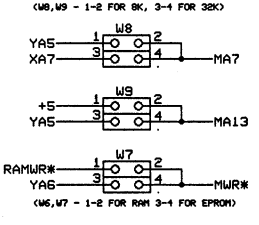


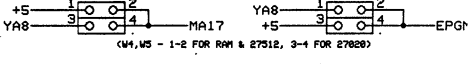


TMC2302P5C
Schematic Drawing

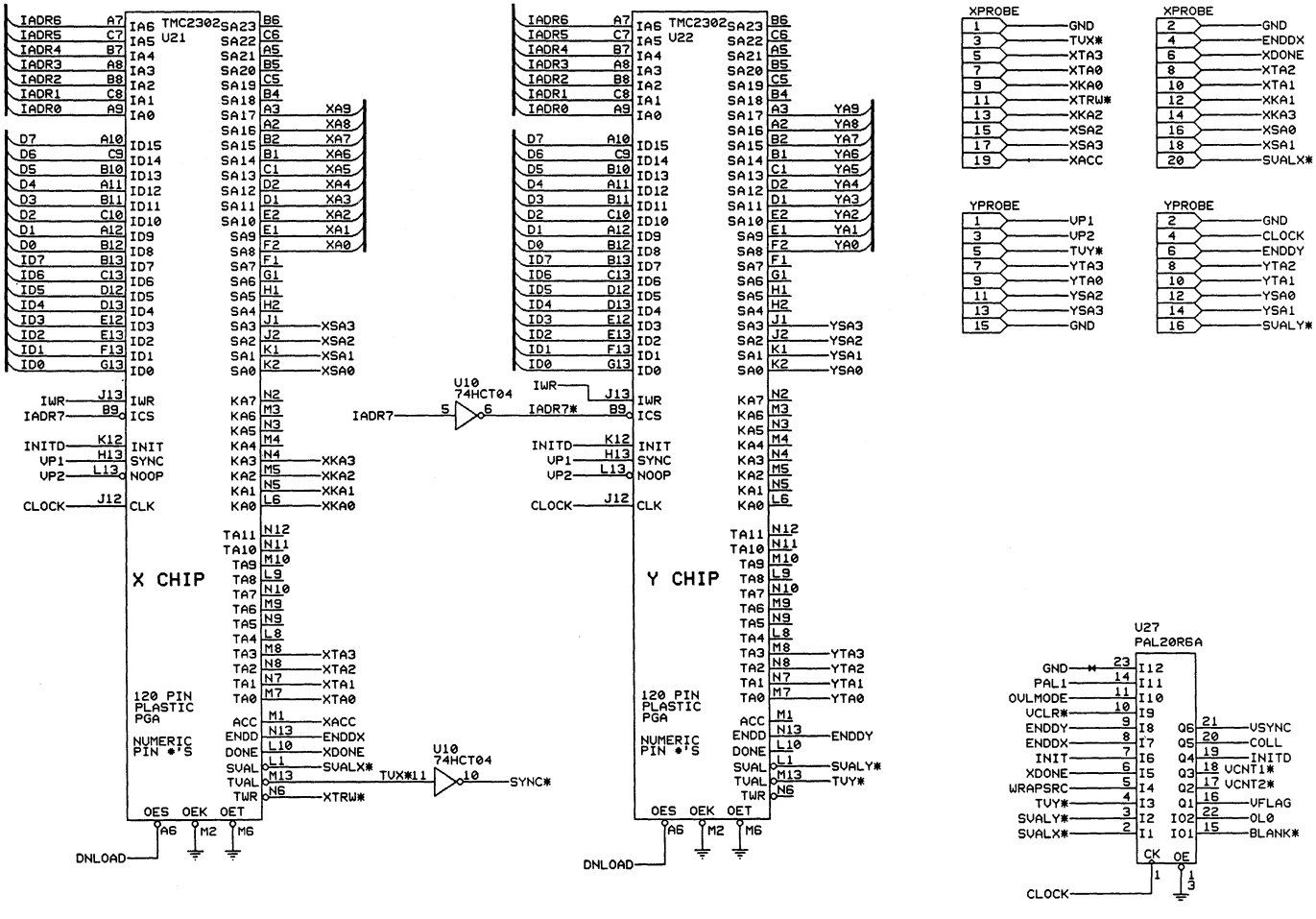








TMC2302P5C
Schematic Drawing

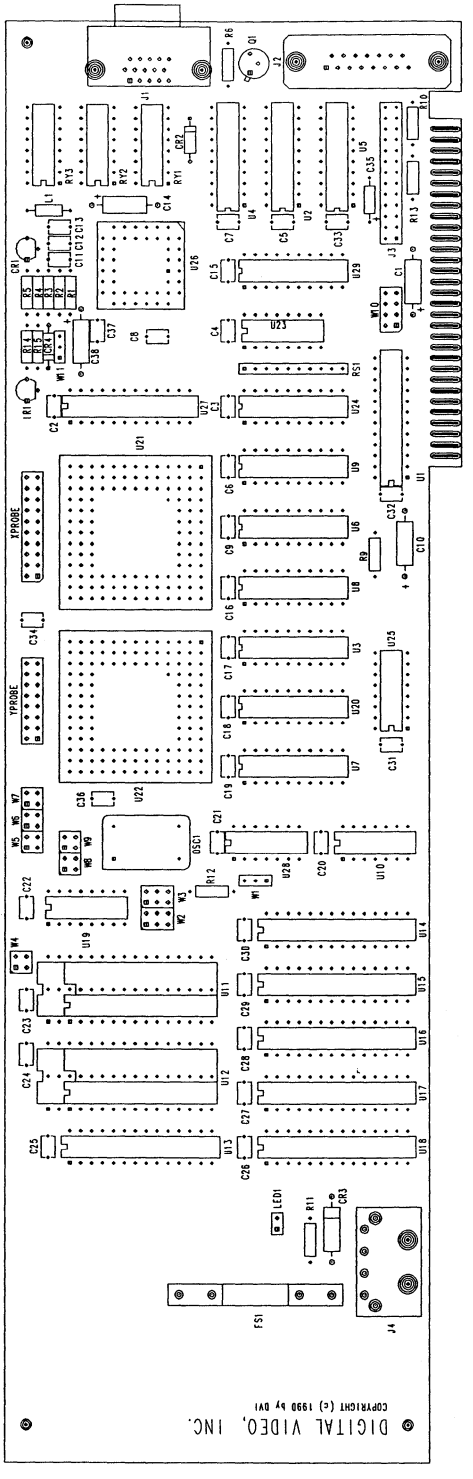


TMC2302P5C
Schematic Drawing

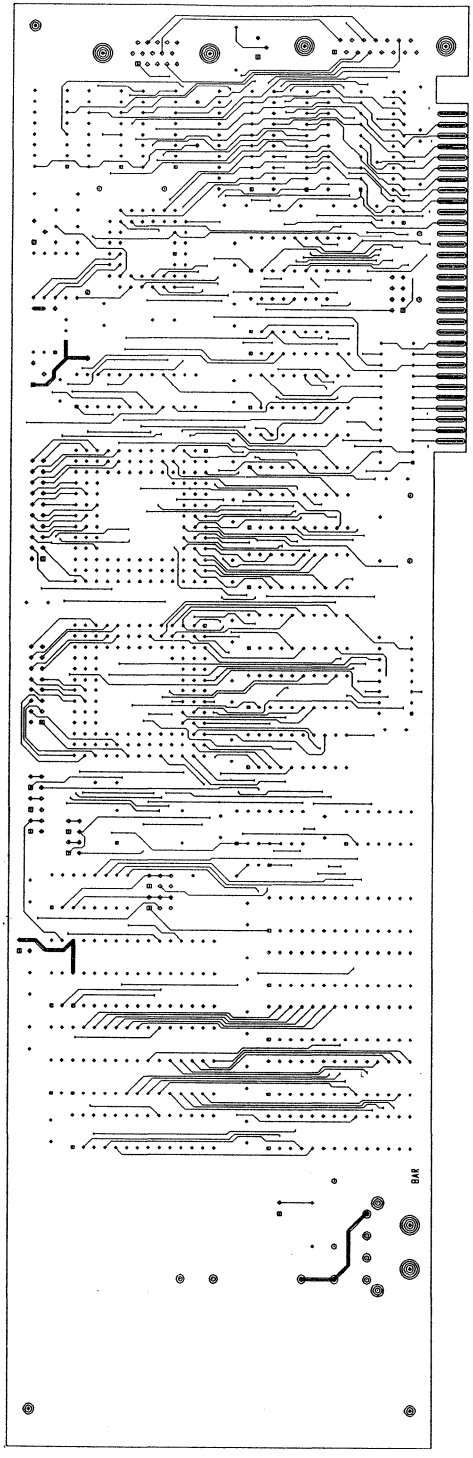
TP-47B

TMC0171

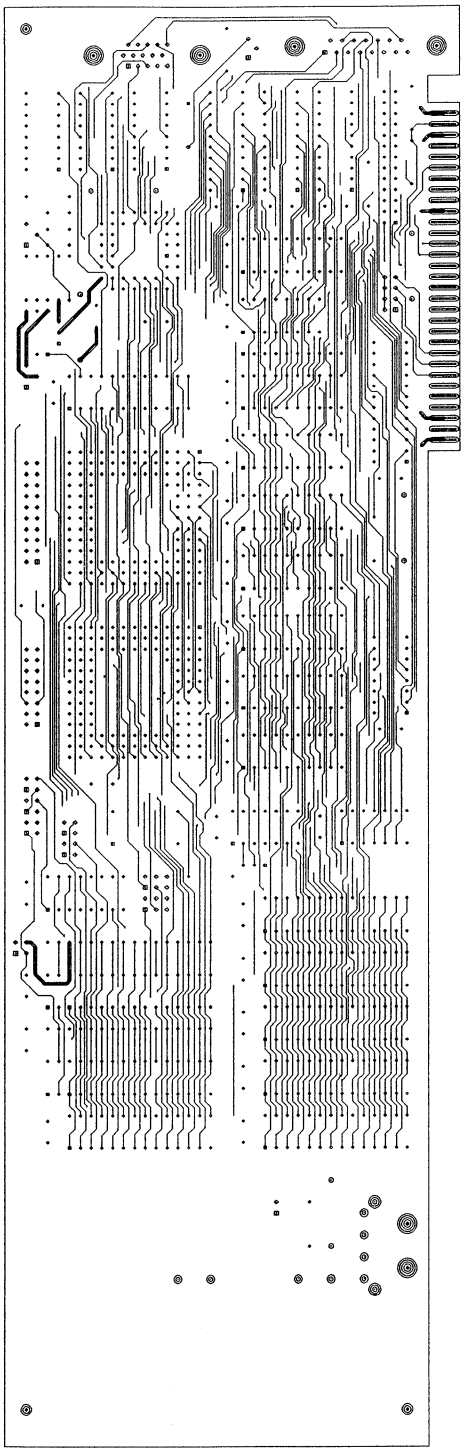
TMC2302P5C
Schematic Drawing



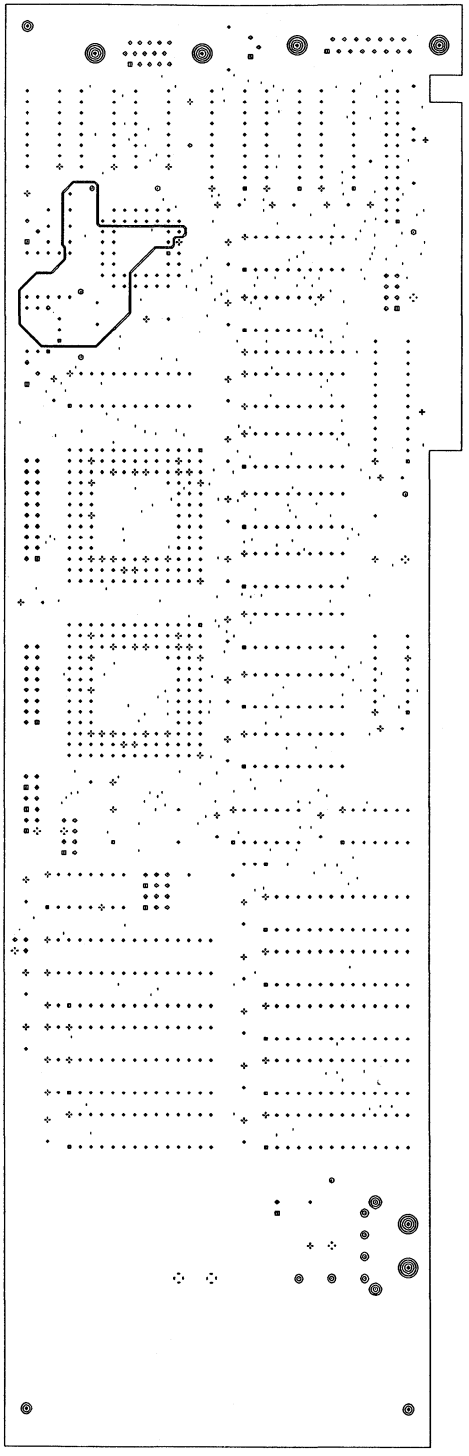
TMC2302P5C
Board Layout Drawing



TMC2302P5C
Board Layout Drawing



TMC2302P5C
Board Layout Drawing



TMC2302P5C
Board Layout Drawing

TMC2242 Topics: Operation with 8-bit I/O, Comparing with Analog Anti-Aliasing Filters and 3 dB Better SNR Through Oversampling

TMC2242 Topics:

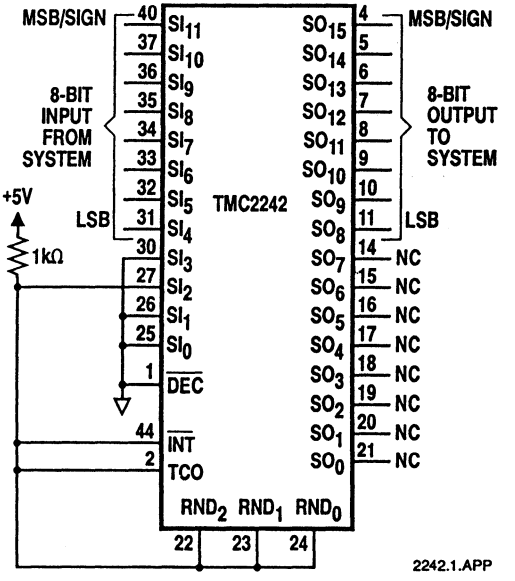
I. Operation with 8-bit I/O

II. Comparing with analog anti-aliasing filters

III. 3dB Better SNR Through Oversampling

The TMC2242 is a video-speed half-band anti-aliasing digital filter. It accepts 12-bit parallel input data and delivers 16 bits of parallel data. Its decimation mode is particularly useful for filtering data from analog-to-digital (A/D) converters, while its interpolation mode filters data prior to digital-to-analog (D/A) conversion. The TMC2242 greatly simplifies analog pre- or post-filters. In decimation mode, the output data rate is 1/2 the input data rate. In interpolation mode, the output data rate is twice the input data rate. The TMC2242's third mode, 1:1 filtering, is used for general purpose fixed-coefficient digital filtering.

Figure 1. Connecting the TMC2242 for 8-bit 2's complement format.



There are many possible connection methods (bit weight assignments) for applications where fewer than the full 12 input bits are used. Recommended connections for 8-bit applications are shown in Figures 1 through 12. For higher resolution inputs, expand data input and output connections in the direction of the LSBs, keeping MSB connections as shown.

Internal Limiting

The TMC2242's limiter restricts its output magnitude to $7FFF_h$ (most positive) and 8000_h (most negative) in two's complement output format (TCO = HIGH). In unsigned magnitude output format (TCO = LOW), the output magnitude is limited to 0000_h (most positive) and $FFFF_h$ (most negative). This limiting is not performed in the interpolation mode where the "gain" of the TMC2242 is approximately 0.5. In low input resolution applications (<12 bits), the full output range of the TMC2242 is not used and the on-chip limiting may not be effective.

Prevention of Overflow and Underflow

Sharp-cutoff analog and digital filters may exhibit minor overshoot and undershoot when driven with sharp step inputs. The output excursions of these filters will be greater than the peak-to-peak input signal excursion for full-scale input step transitions. Whereas analog filters usually have ample signal headroom for overshoot and undershoot transients, digital filters have a limited and well-defined output range and may clip when asked to filter full-scale input transients. The TMC2242 provides the extra output word width (16 bits) required to accommodate this potential signal growth.

If sharp, full-scale input transitions are anticipated, and the system cannot accommodate the extra dynamic range provided by the TMC2242 (as applied in an 8-bit system, for instance) then the input range should be limited slightly to prevent undesired overflow and underflow.

Tables 2 suggests input value limits for this kind of application. It applies for all input and output formats, however attention must be paid to the difference between the bit assignments of the TMC2242 and bit weighting of the system. The actual limiting values required in any particular application will vary according to the nature of expected signals and system configuration.

Table 1. Effect of on-chip limiting in 8-bit applications

Figure	Input Format	Mode	Output Format	Is on-chip limiting effective?
1	2's comp	decimate	2's comp	yes
2	2's comp	1:1 filter	2's comp	yes
3	2's comp	interpolate	2's comp	no
3a	2's comp	interpolate	inv 2's comp	no
4	2's comp	decimate	inv uns mag	yes
5	2's comp	1:1 filter	inv uns mag	yes
6	2's comp	interpolate	inv uns mag	no
7	uns mag	decimate	uns mag	no
8	uns mag	1:1 filter	uns mag	no
9	uns mag	interpolate	uns mag	no
10	uns mag	decimate	inv uns mag	no
11	uns mag	1:1 filter	inv uns mag	no
12	uns mag	interpolate	inv uns mag	no

Table 2. Suggested limits for 12-bit formats

Mode	SI_{11-0} limit values for unsigned magnitude Min	Max	SI_{11-0} limit values for 2's complement Min	Max
decimate	$8F8_h$	709_h	$07A_h$	783_h
1:1 filter	$8F8_h$	709_h	$07A_h$	783_h
interpolate	$9B7_h$	648_h	$0DC_h$	723_h

If less than 12 bits of input data are used in applications involving fast full-scale transitions, the input value must remain within these values. Table 3 suggests limiting values for 8-bit input data connected to SI_{11-4} for two's complement format (Figures 1 through 6) and connected to SI_{10-3} for unsigned magnitude format (Figures 7 through 12). Unless shown otherwise, unused input pins are connected to ground. Note that the connection of system data to SI_{11-0} depends upon the application, mode, and particular data format used.

In Figures 3, 3a, 7, 8, 9, 10, 11 and 12, the unused MSBs of the TMC2242 (SO_{15} and, in some cases, SO_{14}) may be used to indicate out-of-range conditions.

Table 3. Suggested input limits for 8-bit applications having sharp step inputs

Figure	Input Format	Mode	Output Format	Limit values for 8-bit data Min	Max
1	2's comp	decimate	2's comp	$8F_h$	70_h
2	2's comp	1:1 filter	2's comp	$8F_h$	70_h
3	2's comp	interpolate	2's comp	$9B_h$	64_h
3a	2's comp	interpolate	inv 2's comp	$9B_h$	64_h
4	2's comp	decimate	inv uns mag	$8F_h$	70_h
5	2's comp	1:1 filter	inv uns mag	$8F_h$	70_h
6	2's comp	interpolate	inv uns mag	$9B_h$	64_h
7	uns mag	decimate	uns mag	10_h	EF_h
8	uns mag	1:1 filter	uns mag	10_h	EF_h
9	uns mag	interpolate	uns mag	$1B_h$	$E4_h$
10	uns mag	decimate	inv uns mag	10_h	EF_h
11	uns mag	1:1 filter	inv uns mag	10_h	EF_h
12	uns mag	interpolate	inv uns mag	$1B_h$	$E4_h$

Full-Scale Sinewave Inputs

Filter coefficients were chosen to give an optimum filter shape, but yield a gain slightly above unity for 1:1 filtering and decimation, and 0.5 for interpolation. This extra gain is less than 0.03dB worst case. If pure full-scale sinewaves are expected, the input level will need to be reduced slightly. A gain of 0.03dB corresponds to three additional LSB-weights referred to full-scale in a 12-bit system, less than one LSB in a 10-bit system, and less than 1/4 LSB in an 8-bit system. In 8-bit applications the 0.03dB gain is therefore usually ignored. This additional gain contributes no linearity error or distortion, and the full input range may be used without fear of undershoot or overshoot.

Rounding

The TMC2242 has internal rounding circuitry which allows the output to be rounded to any of eight selectable precisions. Rounding is accomplished by adding an offset of 1/2 LSB to the digital result and then truncating. The $RND_{2\text{-}0}$ inputs select which of $SO_{0\text{-}7}$ is the system LSB. Setting $RND_{2\text{-}0}$ = 111 selects SO_7, and $RND_{2\text{-}0}$ = 000 selects SO_0. If SO_x is the system LSB, then set $RND_{2\text{-}0}$ = x. These selections apply to Figures 3, 3a, 6, 7, 8, 9, 10, 11 and 12.

Figures 1, 2, 4, and 5 use SO_8 as the LSB. Additional offset is required for correct rounding in applications where one of $SO_{15\text{-}8}$ is the LSB. in this case, an input is tied HIGH to add the additional offset that, when combined with the selected rounding bits of the TMC2242, results in a total offset of 1/2 LSB. In Figures 1, 2, 3, and 5, the internal rounding adds 1/4 LSB and input SI_2 is tied HIGH to add another 1/4 LSB for a total of 1/2 LSB, all referred to SO_8. It is less correct to set input bit SI_3 HIGH to provide all of the required 1/2 LSB because setting $RND_{2\text{-}0}$ = 000 selects SO_0 as the LSB which will add an additional undesired 1/512 LSB offset.

Figure 2.

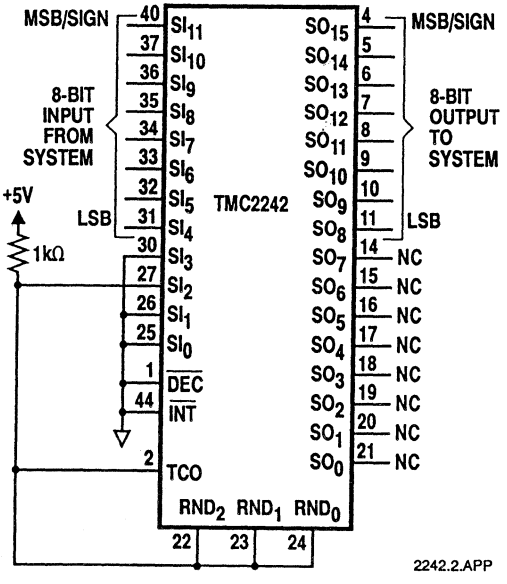
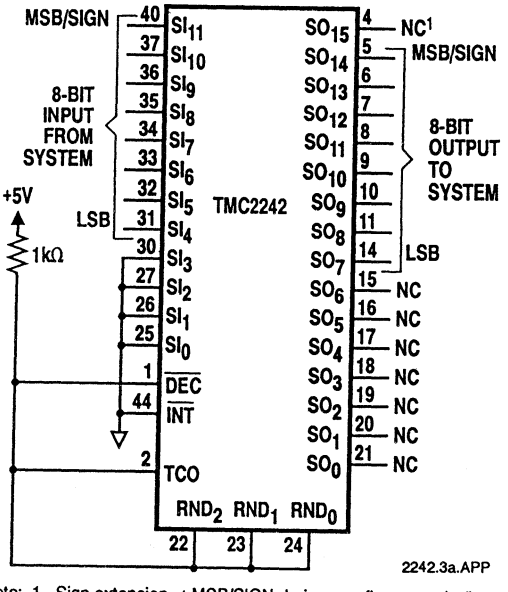


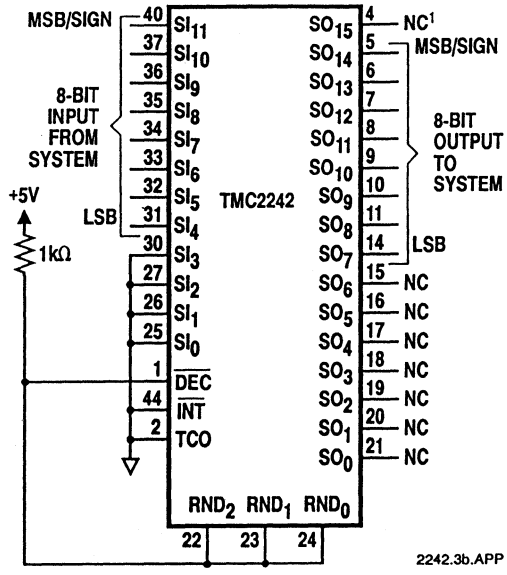
Figure 3.



Note: 1. Sign extension, ≠ MSB/SIGN during overflow or underflow.

Application Notes

Figure 3a.



Note: 1. Sign extension = MSB/SIGN during overflow or underflow.

Figure 4.

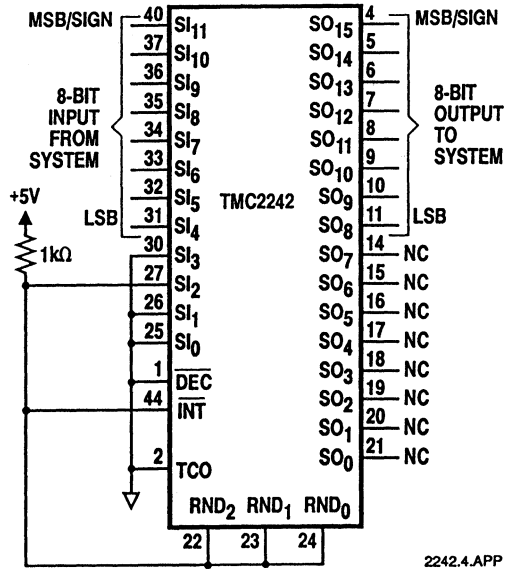


Figure 5.

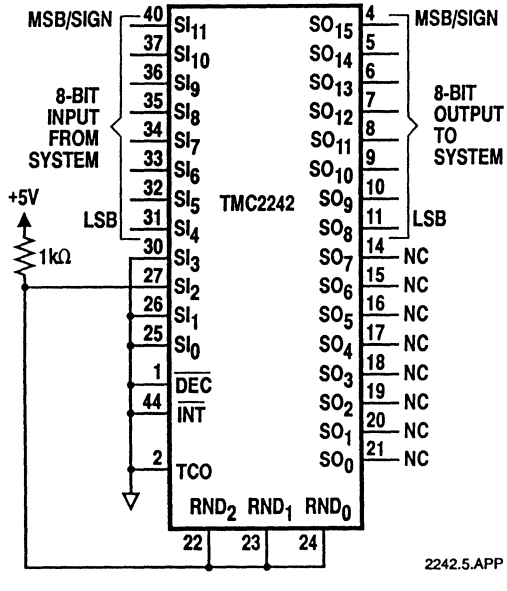


Figure 6.

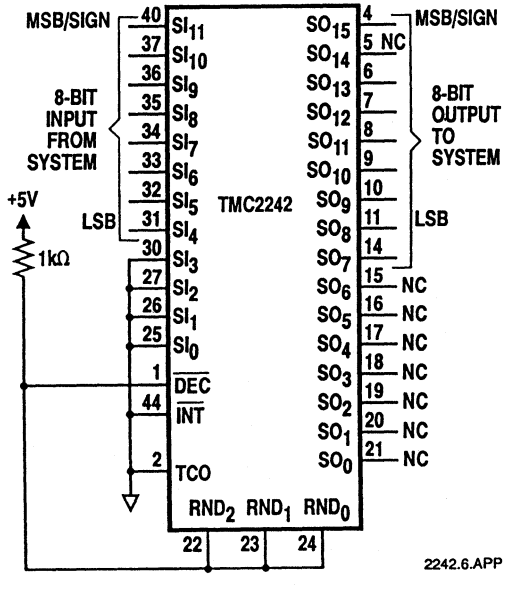
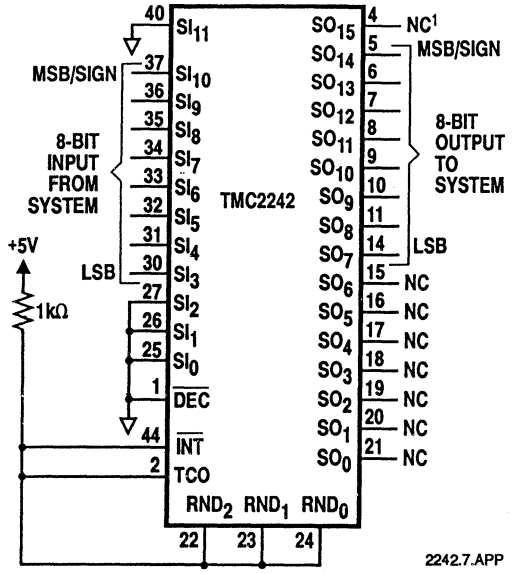
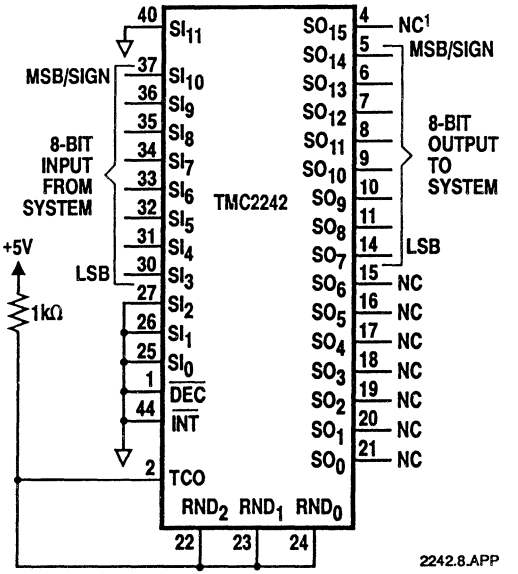


Figure 7.



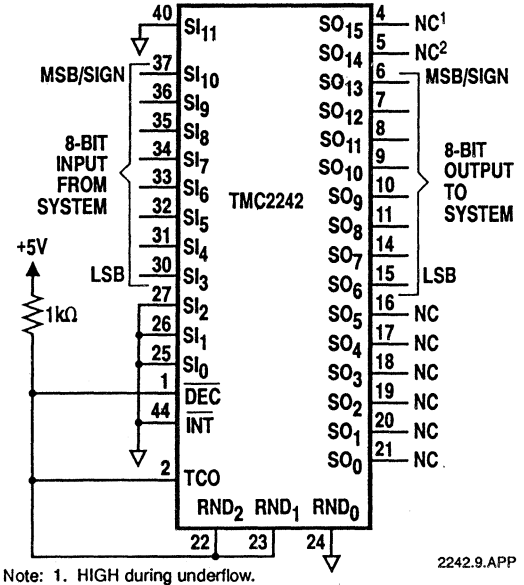
Note: 1. HIGH during overflow or underflow.

Figure 8.



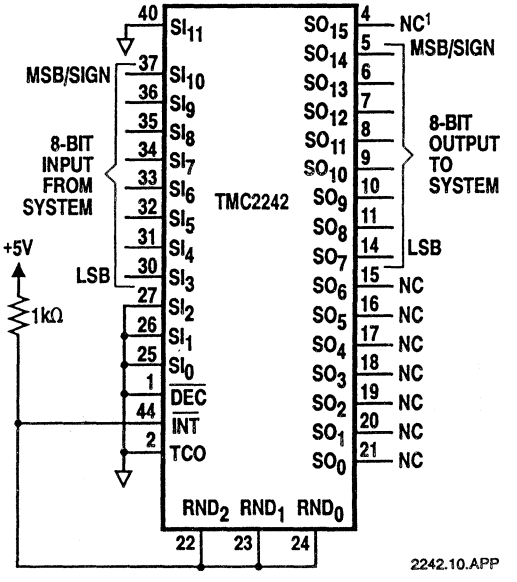
Note: 1. HIGH during overflow or underflow.

Figure 9.



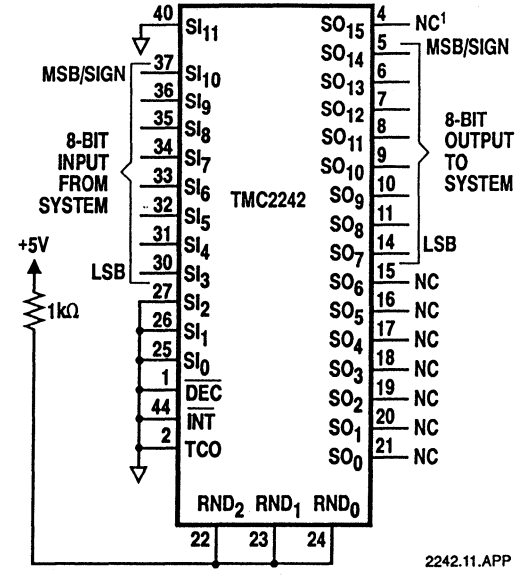
Note: 1. HIGH during underflow.
2. HIGH during overflow or underflow.

Figure 10.



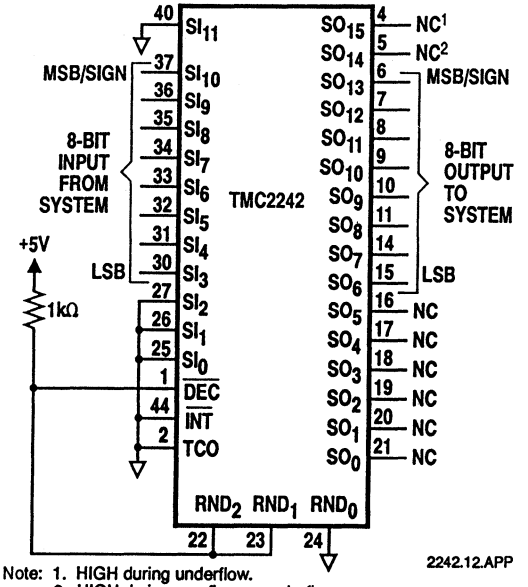
Note: 1. HIGH during overflow or underflow.

Figure 11.



Note: 1. HIGH during overflow or underflow.

Figure 12.



Note: 1. HIGH during underflow.
2. HIGH during overflow or underflow.

Table 4. Summary of connections shown in Figures 1 through 12.

Figure	Input Format	Mode	Output Format	Input Pins	SI_2 Pin	Output Pins	DEC\	INT\	TCO	RND_0
1	2's comp	decimate	2's comp	SI_{11-4}	HIGH	SO_{15-8}	LOW	HIGH	HIGH	HIGH
2	2's comp	1:1 filter	2's comp	SI_{11-4}	HIGH	SO_{15-8}	LOW	LOW	HIGH	HIGH
3	2's comp	interpolate	2's comp	SI_{11-4}	LOW	SO_{14-7}	HIGH	LOW	HIGH	HIGH
3a	2's comp	interpolate	inv 2's comp	SI_{11-4}	LOW	SO_{14-7}	HIGH	LOW	LOW	HIGH
4	2's comp	decimate	inv uns mag	SI_{11-4}	HIGH	SO_{15-8}	LOW	HIGH	LOW	HIGH
5	2's comp	1:1 filter	inv uns mag	SI_{11-4}	HIGH	SO_{15-8}	LOW	LOW	LOW	HIGH
6	2's comp	interpolate	inv uns mag	SI_{11-4}	LOW	SO_{15-7}, SO_{14}=NC	HIGH	LOW	LOW	HIGH
7	uns mag	decimate	uns mag	SI_{10-3}	LOW	SO_{14-7}	LOW	HIGH	HIGH	HIGH
8	uns mag	1:1 filter	uns mag	SI_{10-3}	LOW	SO_{14-7}	LOW	LOW	HIGH	HIGH
9	uns mag	interpolate	uns mag	SI_{10-3}	LOW	SO_{13-6}	HIGH	LOW	HIGH	LOW
10	uns mag	decimate	inv uns mag	SI_{10-3}	LOW	SO_{14-7}	LOW	HIGH	LOW	HIGH
11	uns mag	1:1 filter	inv uns mag	SI_{10-3}	LOW	SO_{14-7}	LOW	LOW	LOW	HIGH
12	uns mag	interpolate	inv uns mag	SI_{10-3}	LOW	SO_{13-6}	HIGH	LOW	LOW	LOW

Notes: 1. For unsigned magnitude input format, SI_{11}=LOW
2. In all cases, RND_1 and RND_2 = LOW.

II. Comparing with analog anti-aliasing filters

When a signal is sampled periodically, the frequency spectrum of that signal is "folded" in such a way as to superimpose frequencies in the primary band of DC to 1/2 the sampling rate with frequencies outside of that band. This effect is commonly called aliasing. To avoid having this effect destroy (by superimposing high frequency noise on the lower frequency signal) information of interest, an anti-aliasing filter must be used to remove the energy above $f_s/2$ from the signal before it is sampled.

Due to aliasing, the sampling rate must be at least twice the signal bandwidth. To account for real world filters, there must be ample headroom for the "skirts" of the anti-aliasing filter. When sampling a signal such as a video signal, the sampling rate chosen (often 4x the NTSC color subcarrier frequency) and the signal bandwidth define the anti-aliasing filter required. If, for example, the signal band is DC to 6 MHz, then the filter must pass DC to 6 MHz and attenuate 7.16 MHz (1/4 octave transition band) by 48 dB. Since realization of such a filter is very difficult, compromises are sometimes made in the signal bandwidth, or the amount of attenuation, or both.

An alternative is to increase the sample rate. If the sample rate is increased to 8x the NTSC color subcarrier frequency, then the stopband need not commence until 14.32 MHz, allowing 1.25 Octaves for the filter to transition from passband to stopband. The disadvantage of this is that the amount of data being generated has doubled, even though the information content has stayed the same.

A solution is to sample at a high rate with a simple anti-aliasing filter in front oft the A/D converter. Then digitally low-pass filter and decimate the data. This avoids the need to store or process more data than the information content of the signal would warrant. This is the purpose of the TMC2242 half-band filter.

The TMC2242 is a digital low-pass filter which passes frequencies from DC to 1/4 the sampling rate. As a result of aliasing, only the frequency spectrum from DC to 1/2 the sampling rate is unique. Since the TMC2242 passes 1/2 of the spectrum available to it, it is called a "half-band filter." The signal is then decimated so that the output data rate becomes 1/2 the input data rate.

The result is that the complexity of the anti-aliasing filter has been significantly reduced at the expense of having to sample the signal at twice the rate needed, plus the addition of a digital filter/decimator. It is reasonable to ask if this is a good tradeoff.

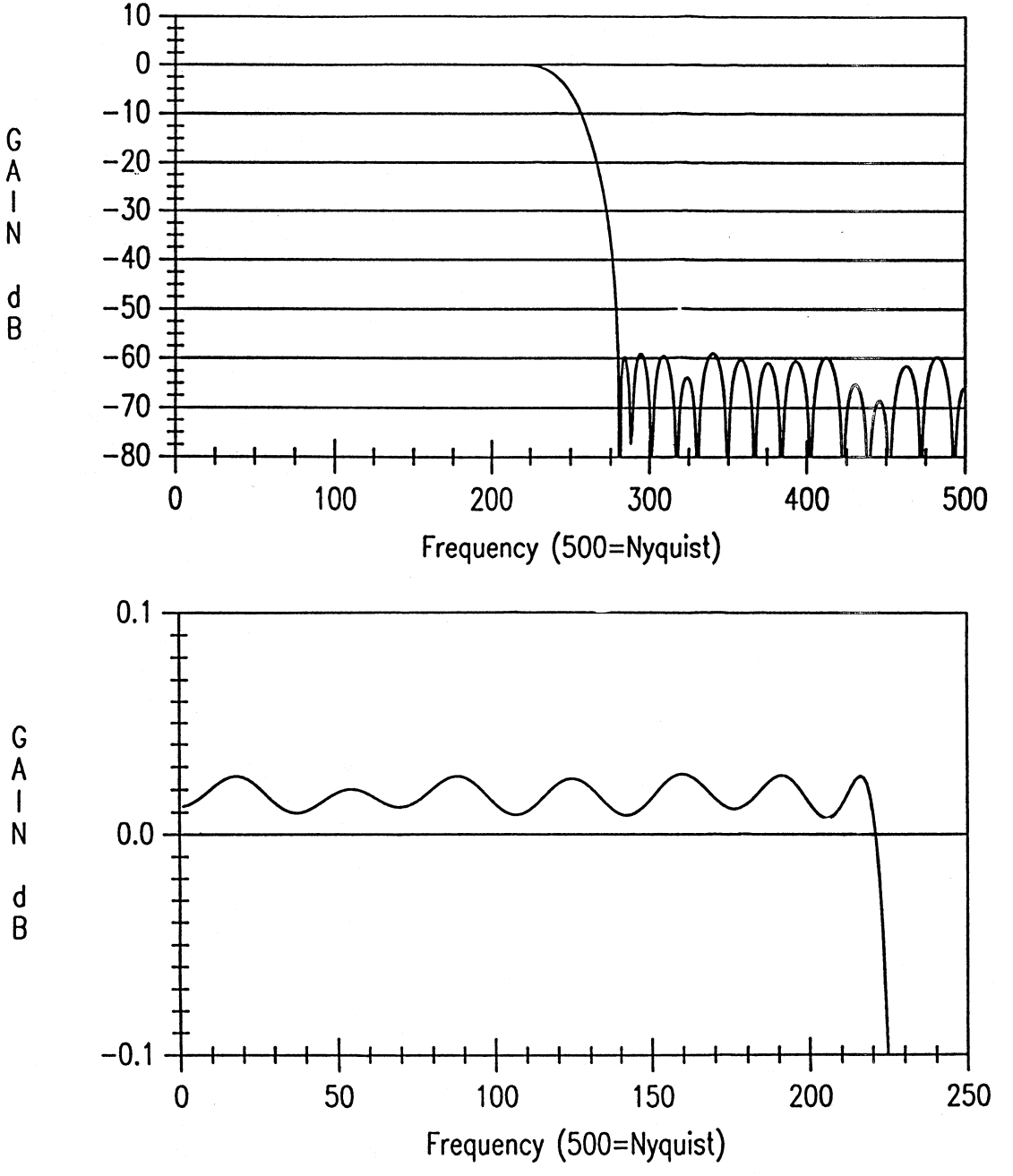
One performance advantage of the TMC2242 over the complex analog filter is that of group delay. Group delay is a measure of the differential propagation time of two sinewaves, of differing frequencies, through a circuit. The result of poor group delay is poor pulse response. The group delay of the digital filter is ZERO.

The use of the FIR filter structure in the TMC2242 guarantees stability, and insensitivity to component selection. The equivalent analog filter would require several high precision components (L and C), all matched precisely to achieve desired performance. This matching must be maintained over the operating temperature range for the circuit. The result is usually an analog filter design that requires hand tuning to achieve desired performance, making the filter expensive to manufacture. All TMC2242s have exactly the same characteristics, over the entire guaranteed temperature range, and the characteristics will not change with age.

The reliability of systems employing the TMC2242 should be greatly improved since there will be a greatly reduced component count.

The following pages show plots of the TMC2242, the vertical axis is in dB and the horizontal axis is frequency normalized so that the sampling rate is 1000.

Figure 13. TMC2242 Frequency Response Curves



III. 3dB Better SNR Through Oversampling

By operating an A/D converter at rates above the minimum required to meet the Nyquist criterion, it is possible to reduce quantization noise. Filtering and decimation return the original data bandwidth, but with improved SNR.

The TMC2242 is a half-band decimating filter. The input signal is low pass filtered, passing only the DC to $f_s/4$ band. The output is decimated so that the output data rate is 1/2 the input data rate. The primary reason for using the TMC2242 is to simplify the requirements imposed upon anti-aliasing filters which are normally placed just ahead of A/D converters. One beneficial side effect of using the TMC2242 is that by oversampling, the signal-to-quantizing noise ratio is increased by 3dB for each octave of oversampling. The result of using a TMC2242 after a 9-bit A/D converter (i.e. TDC1049) sampling at 8x the NTSC color subcarrier frequency is an equivalent 4x subcarrier sampling rate where the resolution of the output signal is 9.5 bits.

To explain where the additional 1/2 bit comes from, the digitizing process must be modeled. If the input to the A/D converter is a signal, f(t), and the digitized output of the signal is $f_d(t)$, then the digitization can be thought of as simply adding quantization noise of $f_d(t)$-f(t). This difference signal is called $\varepsilon(t)$. Therefore $f_d(t)=f(t)+\varepsilon(t)$. $\varepsilon(t)$ is the noise that is not wanted since it represents the error in the sample.

The probability density function of $\varepsilon(t)$ is close to that of white noise for most real signals. Its value is equally likely to fall between $+1/2\delta$ and $-1/2\delta$ where δ is a quantization step. If sampling is done at twice the required rate, followed by decimation, the noise in the decimated signal will be the sum of the two $\varepsilon(t)$s. The expected value of the sum of two variables equally distributed over a range of $\pm 1/2\delta$ is $\pm\sqrt{2}/2\ \delta$, hence the noise has increased by a factor of $\sqrt{2}$. In the mean time, the signal, having been sampled twice, has increased in value by a factor of 2. Since the signal strength grows more rapidly than the noise, there is an improvement in SNR by a factor of $2/\sqrt{2}$ (3dB) for each octave of oversampling.

Another way of looking at the process is in the frequency domain. The spectrum of $\varepsilon(t)$ is white and therefore its energy is equally distributed across the frequency band for DC to $f_s/2$. The half-band filter acts equally on the noise and the signal. Since the signal falls entirely within the passband, it is entirely passed. The noise, being evenly distributed, is cut in half, increasing the signal-to-noise ratio by 3dB.

The Evaluation Board for the TMC1175/TDC3310

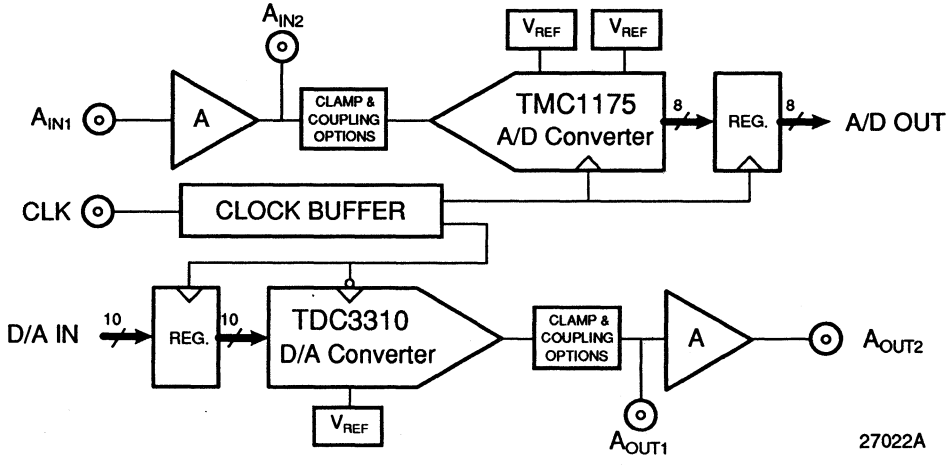
Application Note TP-50A
The Evaluation Board for the TMC1175/TDC3310

The TMC1175E1C Evaluation Board brings all of the circuitry together for evaluating Raytheon's TMC1175 CMOS A/D converter and the TDC3310 10-bit D/A converter. The A/D and D/A signal paths are independent but easily configurable at the edge connector for reconstruction of A/D converter data with the D/A converter. Data is registered after the A/D and before the D/A converters. A common clock signal will drive both A/D and D/A converters. A/D and D/A converters may also be clocked independantly via the edge connector.

The TMC1175E1C is a simple two-layer printed circuit board with 100 x 160 millimeter Eurocard dimensions. The component side of the board comprises mostly ground plane with only a few interconnections. A double row 64-pin DIN male connector gives access to all power and digital signals. Analog input and output signals are available from SMA connectors.

Variable voltage references are provided for the TMC1175 and TDC3310. Configurable input and output wideband video amplifiers are provided for signal conditioning. Signal path offsets may be adjusted at the input and output amplifiers.

Figure 1. Evaluation Board Block Diagram



Power Supply and Clock Input Requirements

Both the TMC1175 and TDC3310 require only +5 Volts for operation. The A/D converter voltage reference circuits and wideband amplifiers may be operated from voltages of ±5 to ±18 Volts.

A Clock Buffer circuit has been included on the board with a 50Ω terminated SMA input. The clock buffer circuit provides separate CONV signals to the A/D and D/A converters and their registers. Pull-up resistors on edge-connector CLK inputs enable the clock buffer when a common clock is used. If separate clocks are desired, edge-connector pins B2 and B24 may be used for the A/D and D/A converters, respectively. The TDC3310 clock input may be monitored on test point TP1.

TMC1175 A/D Converter Circuitry

The circuitry included on this evaluation board is not intended to represent the minimum design for A/d operation. It is designed with maximum flexibility for evaluating the TMC1175 in various configurations.

The input amplifier, U6, may be configured for inverting or non-inverting operation, with and without variable offset voltage. R39 is the potentiometer used for varying the offset of the signal applied to the A/D converter. The output of the input amplifier is monitored at SMA A_{IN2}. A_{IN2} may also be used as a signal input when AC-coupling to the A/D converter is used. The 75Ω input termination resistor and voltage gain of this amplifier are jumper selectable. Fixed amplifier gains of -4, -1, +2, and +5 are available.

AC- or DC-coupling directly to the TMC1175, is accomplished via input connector A_{IN2}. A "poor man's" diode clamp limits the negative going AC-coupled signal to the A/D converter to the voltage applied to R_T. The diode clamp and coupling method are jumper selectable. Silicon diodes are included on the board to prevent voltage excursions on the input to the A/D converter from going beyond the power supply range.

Two variable voltage reference circuits are provided on the board for driving the R_T and R_B inputs of the TMC1175. The A/D reference voltage inputs may be jumper configured for the internal reference divider of the TMC1175 using V_{R+} and V_{R-}. Other jumper options connect R_T to V_{CC} and R_B to GND. The reference inputs to the A/D converter may be monitored on test points TP5 and TP6.

Table 1 summarizes the function of each jumper and Table 2 indicates which jumpers are to be installed and removed for amplifier configurations.

Table 1. A/D Converter Jumpers

J14	Connects OFFSET control to inverting input of amplifier.
J15	Grounds inverting input of amplifier for non-inverting operation.
J16	Connects A_{IN1} to inverting amplifier input.
J17	Enables 75Ω termination resistor on A_{IN1}.
J18	Connects A_{IN1} to non-inverting amplifier input.
J19	Connects OFFSET control to non-inverting input of amplifier.
J20	Decreases feedback resistor of amplifier from 4.99kΩ to 1.0kΩ.
J21	Connects amplifier output to A/D input.
J22	D.C. couples amplifier output to A/D input.
J23	Enables 75Ω termination resistor on A_{IN2}.
J24	Enables diode clamp.
J25	Connects A/D R_T to V_{R+} pin.
J26	Connects A/D R_T to V_{CC}.
J27	Connects A/D R_T to variable voltage reference.
J28	Connects A/D R_B to ground.
J29	Connects A/D R_B to V_{R-} pin.
J30	Connects A/D R_B to variable voltage reference.

Table 2. Jumpers for A/D Input Configurations

	Configuration	Installed	Removed
1	Non-inverting, with offset control	**J14 J18**	**J15 J16 J19**
2	Inverting, with offset control	**J16 J19**	**J14 J15 J18**
3	Non-inverting, without offset control	**J15 J18**	**J14 J16 J19**
4	AC-coupled direct input on A_{IN2} (with termination and clamp)	**J23 J24**	**j21 j22**
5	DC-coupled direct input on A_{In2} (without termination and clamp)	**J22**	**J21 J23 J24**

TDC3310 D/A Converter Circuitry

The D/A converter circuitry included on the Evaluation Board is not intended to represent the minimum design for D/A operation. It is designed with maximum flexibility for evaluating the TDC3310 in configurations that work for various applications and implementations. Since the TDC3310 is a 10-bit D/A converter, its two LSBs are jumpered to ground, enabling 8-bit operation, matching the resolution of the TMC1175 A/D converter. The INVERT input to the TDC3310 is grounded by jumper J4.

A simple band-gap voltage reference and potentiometer R7 provide a variable reference to the TDC3310. Varying R7 will change the "gain" of the TDC3310 D/A converter. The reference is set to -1.0 Volts with respect to the +5 Volt power supply as part of the factory test procedure. The adjustment ranges from -0.4 to -1.2 Volts with respect to the +5 Volt power supply. The TDC3310 reference voltage may be monitored on test point TP2.

AC- or DC-coupling directly from the TDC3310 to the output amplifier is accomplished via jumper J6. SMA connector A_{OUT1} can be used as a monitor point for the input to the output amplifier or as an un-amplified D/A converter output. A "poor man's" diode clamp limits the negative going AC-coupled signal from the D/A converter to GND. The diode clamp is jumper selectable.

The wideband video output amplifier, U5, may be configured for inverting (A_V = -2) or non-inverting (A_V = +2) operation with variable offset voltage from R16. The amplifier has an output series resistor of 75Ω to ensure 1 Volt pk-pk video levels into 75Ω terminated cables.

Since the output voltage from the TDC3310 D/A converter if referred to the +5 Volt power supply, the output amplifier may be configured as a differential amplifier with one input referred to the +5 Volt power supply. This configuration reduces the effect of common-mode noise from the power supply at the input to the amplifier.

Table 3 summarizes the function of each jumper and Table 4 indicates which jumpers are to be installed and removed for output amplifier configurations.

Table 3. D/A Converter Jumpers

J1	Enables 51Ω termination resistor on D/A CLK.
J2	Grounds LSB of D/A converter for 8-bit operation.
J3	Grounds 2nd LSB of D/A converter for 8-bit operation.
J4	Grounds INVERT input to D/A.
J5	Enables 75Ω termination resistor on A_{OUT1} connector.
J6	D.C. couples output of D/A converter.
J7	Enables diode clamp.
J8	Connects inverting input of amplifier to V_{CC}.
J9	Connects AC-coupled output of D/A to amplifier.
J10	Grounds inverting input of amplifier.
J11	Connects non-inverting input of amplifier to V_{CC}.
J12	Connects non-inverting input of amplifier to D/A output.
J13	Connects non-inverting input of amplifier to ground.

Table 4. Jumpers for D/A Output Amplifier Configurations

	Configuration	Coupling	Referred	Installed			Removed				
1	Non-inverting	AC	GND	**J10**	**J12**		**J6**	**J8**	**J9**	**J11**	**J13**
2	Inverting	AC	GND	**J9**	**J13**		**J6**	**J8**	**J10**	**J11**	**J12**
3	Non-inverting	DC	GND	**J6**	**J10**	**J12**	**J8**	**J9**	**J11**	**J13**	
4	Inverting	DC	GND	**J6**	**J9**	**J13**	**J8**	**J10**	**J11**	**J12**	
5	Non-inverting	AC	V_{CC}	**J8**	**J12**		**J6**	**J9**	**J10**	**J11**	**J13**
6	Inverting	AC	V_{CC}	**J9**	**J11**		**J6**	**J8**	**J10**	**J12**	**J13**
7	Non-inverting	DC	V_{CC}	**J6**	**J8**	**J12**	**J9**	**J10**	**J11**	**J13**	
8	Inverting	DC	V_{CC}	**J6**	**J9**	**J11**	**J8**	**J10**	**J12**	**J13**	

The Edge Connector

The edge connector has been arranged to easily configure the board for reconstructing A/D data with the TDC3310 D/A converter. A./D data outputs are located exactly adjacent to D/A data inputs on the edge connector. Simply shorting these edge connector pins together will enable the direct transfer of data from one signal path to the other.

Table 5. Edge-connector Pin Assignments

A32	GND	B32	V- (-15V)
A31	GND	B31	V+ (+15V)
A30	GND	B30	N/C
A29	GND	B29	N/C
A28	GND	B28	N/C
A27	GND	B27	N/C
A26	GND	B26	N/C
A25	GND	B25	N/C
A24	GND	B24	D/A CONV Input
A23	GND	B23	N/C
A22	GND	B22	N/C
A21	D/A D_1 MSB	B21	A/D D_1 MSB
A20	D/A D_2	B20	A/D D_2
A19	D/A D_3	B19	A/D D_3
A18	GND	B18	V_{CC} (+5V)
A17	D/A D_4	B17	A/D D_4
A16	D/A D_5	B16	A/D D_5
A15	D/A D_6	B15	A/D D_6
A14	D/A D_7	B14	A/D D_7
A13	D/A D_8	B13	A/D D_8 LSB
A12	D/A D_9	B12	N/C
A11	D/A D_{10} LSB	B11	N/C
A10	N/C	B10	N/C
A9	N/C	B9	N/C
A8	N/C	B8	N/C
A7	N/C	B7	N/C
A6	N/C	B6	N/C
A5	N/C	B5	N/C
A4	GND	B4	N/C
A3	GND	B3	N/C
A2	GND	B2	A/D CONV Input
A1	GND	B1	V_{EE} (-5.2V)

Figure 2. A/D Converter Schematic Diagram

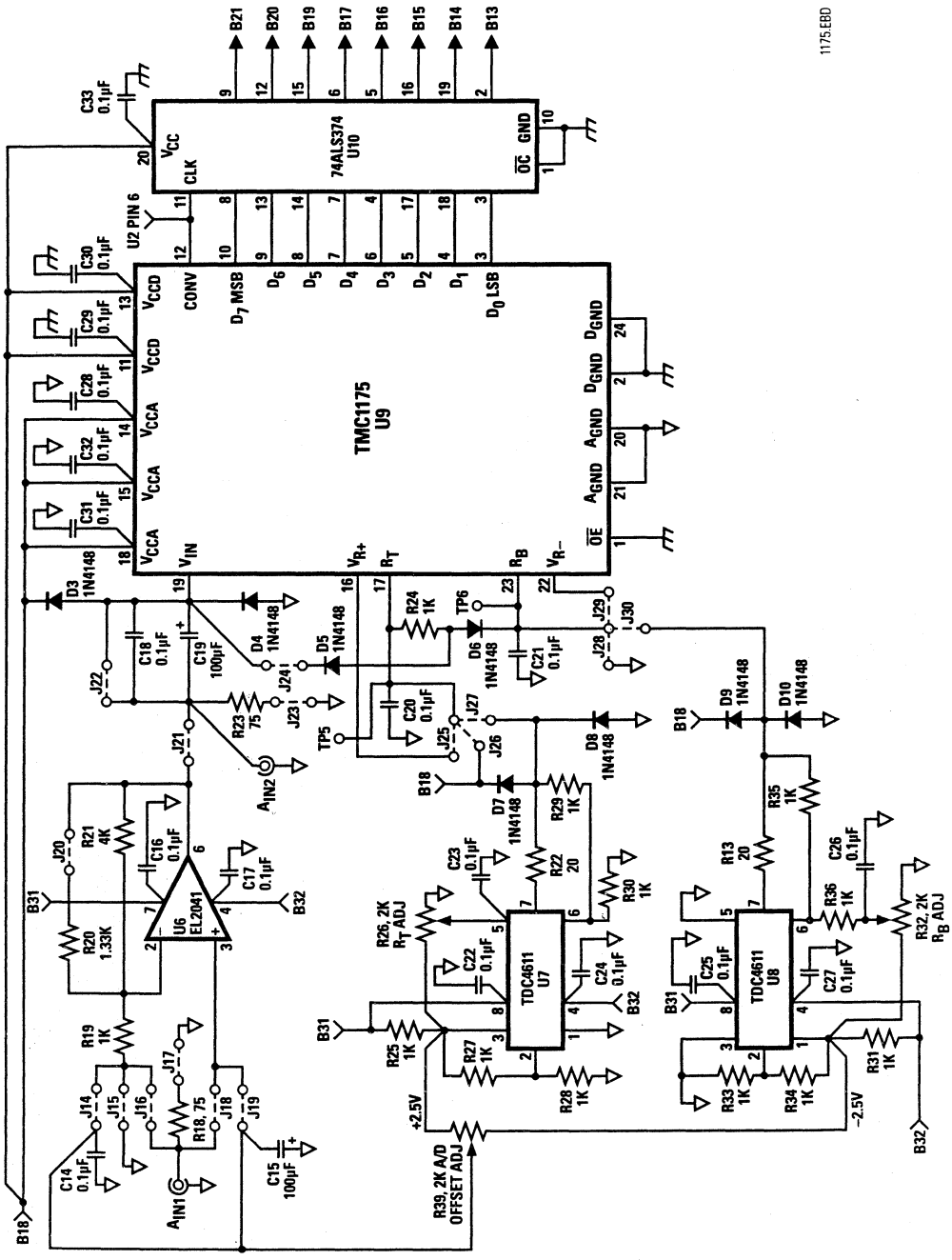


Figure 3. D/A Converter Schematic Diagram

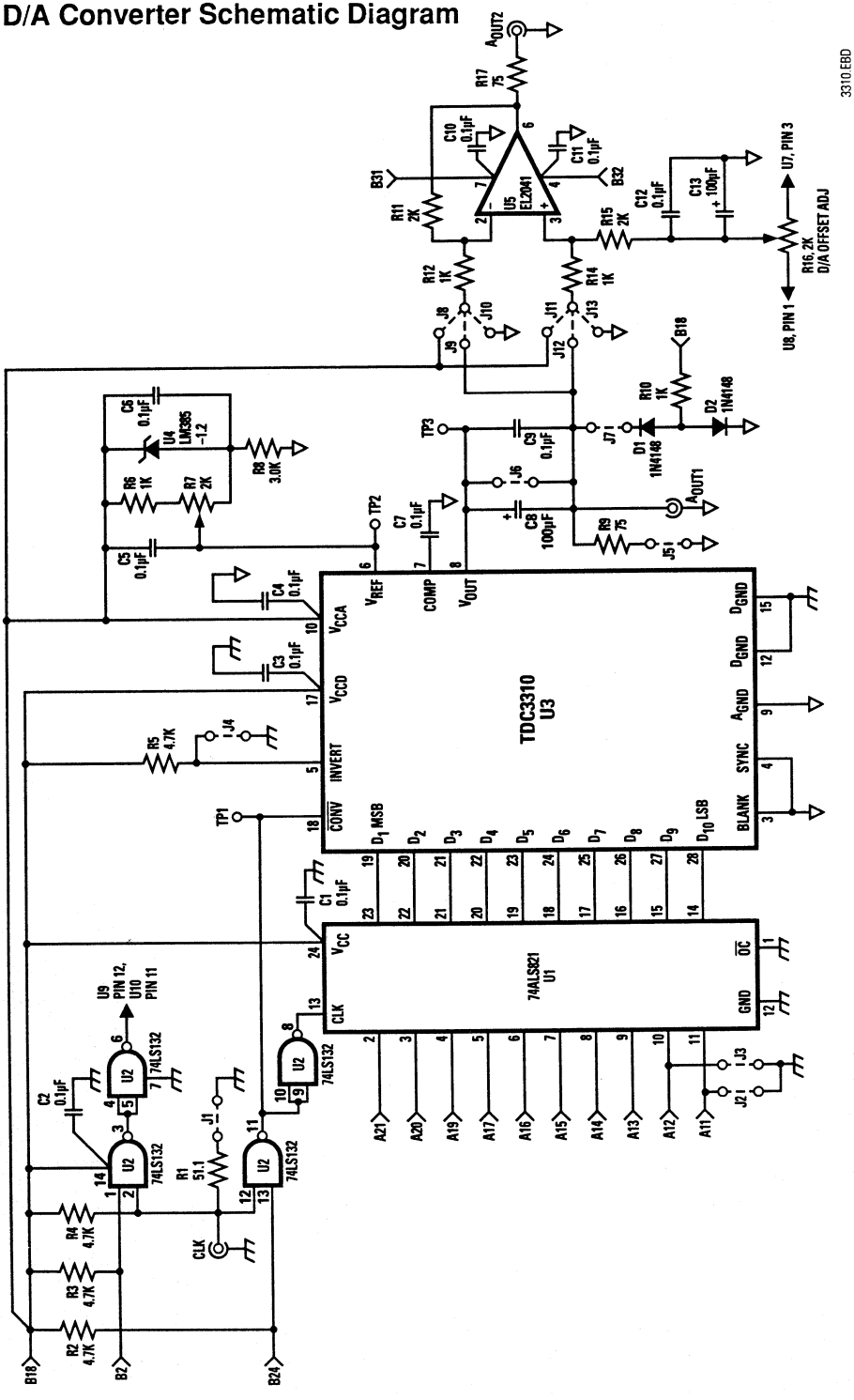


Table 6. Parts List

Item	Qty	Part/Value	Ref. Designator	Mfg. P/N
1	29	Ceramic capacitor, 0.1 µF	C1-C7, C9-C12, C14, C16-C18, C21-C33	MD015C104KAB, AVX
2	4	Tantalum capacitor, 100 µF	C8, C13, C15, C19	TAP107K035SCS, AVX
3	2	Resistor, 20Ω	R13, R22	RN50C20R0F
4	1	Resistor, 51.1Ω	R1	RN50C51R0F
5	4	Resistor, 75Ω	R9, R17, R18, R23	RN50C75R0F
6	17	Resistor, 1.0kΩ	R6, R10, R12, R14 R19, R24-R31, R33-R36	RN50C1001F
7	1	Resistor, 1.33kΩ	R20	RN50C1331F
8	2	Resistor, 2.0kΩ	R11, R15	RN50C2001F
9	1	Resistor, 3.0kΩ	R8	RN50C3001F
10	1	Resistor, 4.0kΩ	R21	RN50C4001F
11	4	Resistor, 4.7kΩ	R2-R5	RN50D4701F
12	1	Potintiometer, 2kΩ	R7	
13	4	Potentiometer, 2kΩ	R16, R26, R32, R39	
14	10	Silicon Diode	D1-D10	1N4148
15	1	10-bit register	U1	74ALS821
16	1	Quad 2-input NAND gate	U2	74LS132
17	1	10-bit D/A Converter	U3	TDC3310N6C, Raytheon Semiconductor
18	1	1.2 Volt bandgap diode	U40	LM385-1.2
19	2	Wideband op-amp	U5, U6	EL2041, Elantec
20	2	Voltage reference, op-amp	U7, U8	LM611, National Semiconductor
21	1	8-bit A/D Converter	U9	TMC1175N2C30, Raytheon Semiconductor
22	1	8-bit register	U10	74ALS374

Figure 4. PC Board Circuit-Side Layout

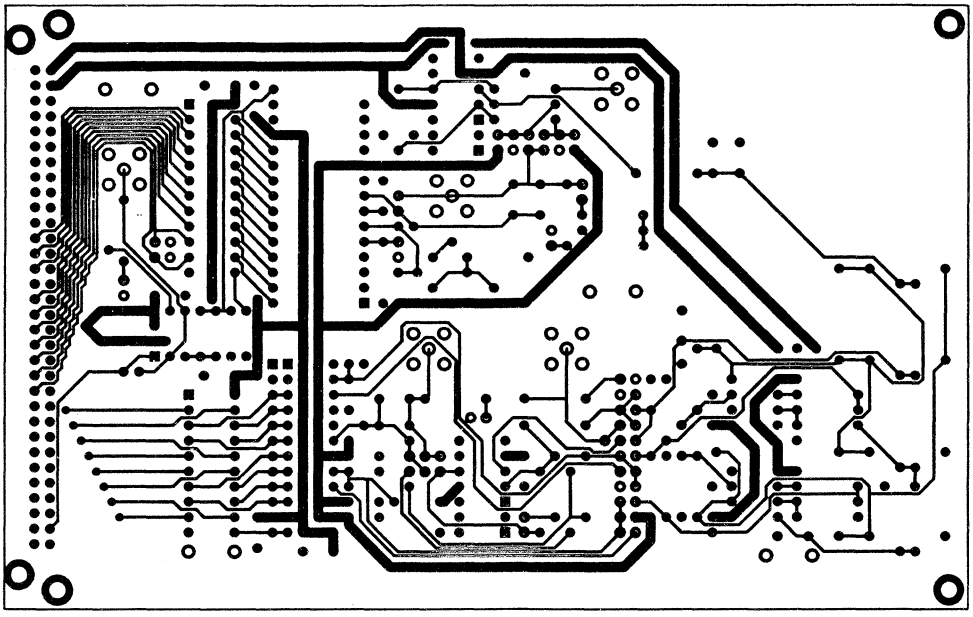


Figure 5. PC Board Component-Side Layout

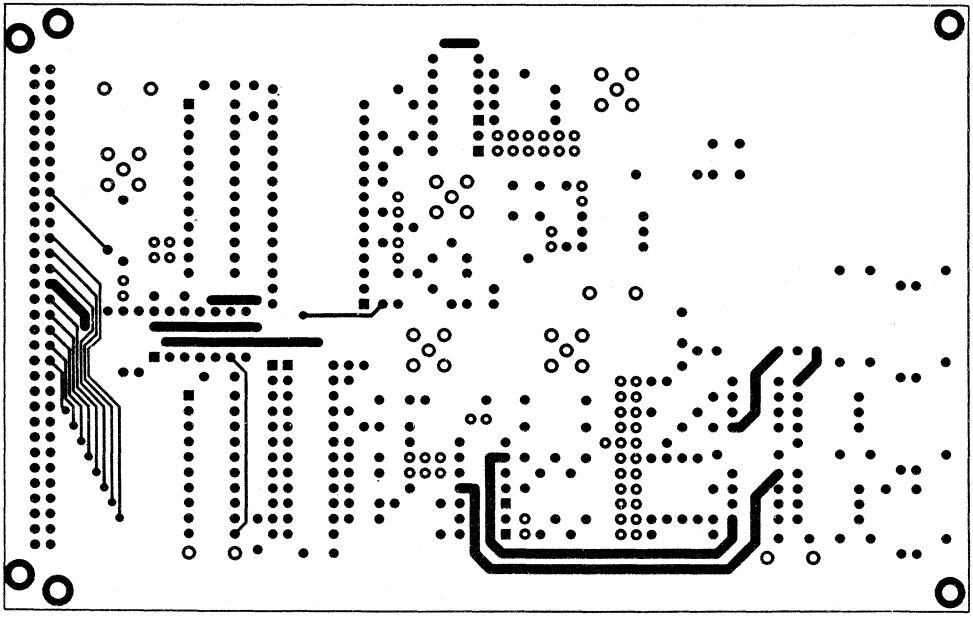
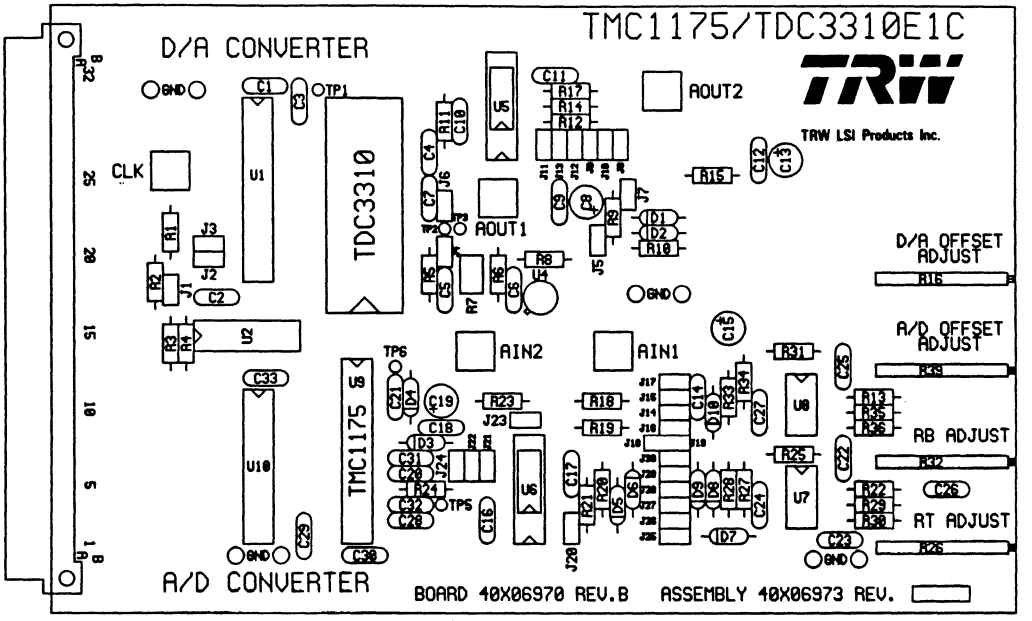


Figure 6. PC Board Silkscreen Layout



Application Notes

A Demonstration Board for the TMC22090 Digital Video Encoder

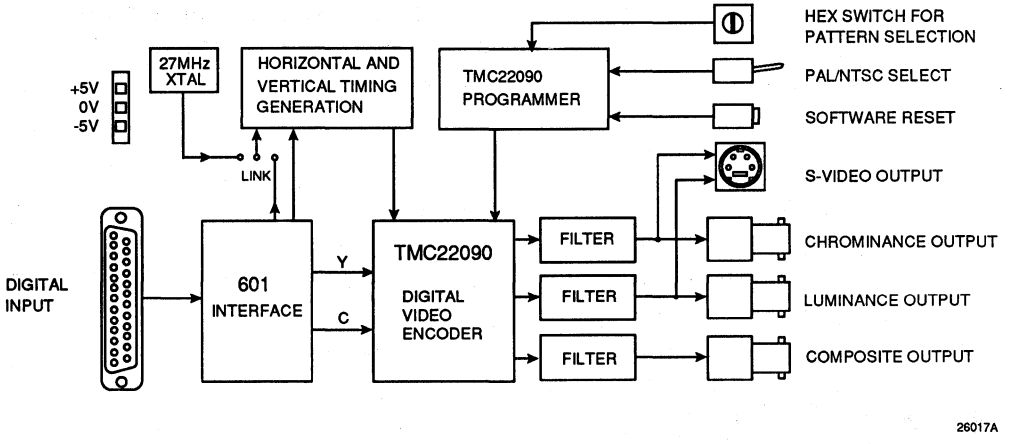
A Demonstration Board for the TMC22090 Digital Video Encoder

Dean Raby

The TMC22061P7C encoder demonstration board converts 8-bit digital component video, (CCIR rec 656 or SMPTE rp 125, a.k.a. "601") into analog composite video using the TMC22090 digital video encoder. The board is dual standard and will operate in both PAL and NTSC television standards.

A 27 MHz crystal oscillator is provided for cases where a CCIR-601 source is not available. In such a case only the internally generated color bars and modulated ramp can be produced.

Figure 1. Block diagram



CCIR-601 Interface

The CCIR-601 data stream is terminated into differential ECL-to-TTL converters. The translated data is latched through U23 at a 27 MHz rate and then to a YC demultiplexer. Here, the luminance and chrominance data words are separated into two data streams termed Y and C, respectively. This YC data goes directly into the TMC22090 which separates the color difference signals from the C data and interpolates the color difference signals to the same sample rate as Y data. This interpolation improves the horizontal color transitions.

The TRS decoder decodes the field (F), vertical blanking (V), and horizontal blanking (H) information for use in the timing signal generation on the board. The TRS decoder also produces the pixel counter reset and the LDV signal for latching the YC data into the TMC22090.

Horizontal and Vertical Timing

The pixel counter (U4, U5, and U1) is decoded to produce the VHSYNC\ and PDC signals required by the TMC22090 for horizontal synchronization. A 2x line rate clock, H/2_CLK, used in the VVSYNC\ generation, is also produced along with P_CLOCK and DATA_EN. P_CLOCK is used to clock the program counters and the DATA_EN signal used in the YC demultiplexing circuit.

A 4-bit counter embedded in U9 is started whenever V goes HIGH, which occurs at the beginning of each vertical blanking interval. This counter is clocked by H/2_CLK which enables the VVSYNC\ pulse to be produced at the same time as the first vertical sync pulse in each field. The PGM output signal ensures that the software reset signal, RES_OUT, goes HIGH 15 half-line periods before the program counter starts.

Software Reset

A software reset occurs whenever the pushbutton switch, S3, is depressed. The software reset is latched through U9 to ensure a known relationship between the internal pixel clock of the TMC22090 and the externally generated LDV, PDC, VHSYNC\, and VVSYNC\ signals. When S3 is depressed the internal state machines of the TMC22090 are reset and the outputs are disabled. When S3 is released the program counter is started at the beginning of the next vertical blanking period. Software Reset is required after power-up and after each functional change.

Programming the TMC22090

A 12-bit counter (U6, U7, and U8) is used to produce the addresses used in programming the TMC22090. U11 produces the required R/W\, $A_{1:0}$, and CS\ signals, while U12 contains 16 different pages of setup data for NTSC and another 16 pages for PAL (selected via switch S2). An additional 32 pages are unprogrammed, and available for user setups. They are accessed by addressing the Upper Memory Blocks (UMB) via selector E7. To ensure that the outputs of the programmable logic are correctly timed to transitions on the microprocessors data bus, they are addressed at four times the rate that U12 is addressed. The 16 pages of setup data are selected by the rotary switch S1, as shown in the table below.

Table 1. Board Operational Setups.

Rotary Switch Position	Board Function
0	Color bars test signal (8-bars).
1	Color bars test signal (9-bars).
2	Modulated ramp test signal.
3	Encodes CCIR-601 input data (normal operation)
4	Subcarrier data limited to 28-bit resolution.
5	Subcarrier data limited to 24-bit resolution.
6	Luminance data limited to 6-bit resolution.
7	Chrominance data limited to 6-bit resolution.
8	Luminance and chrominance data limited to 6-bit resolution.
9	Inverted luminance data.
A	Inverted luminance data and 180° phase shift to chrominance.
B	Chrominance data set to constant value in UV CLUTs.
C	Color burst phase advanced 10 degrees.
D	Color burst phase retarded 10 degrees.
E	Reduced active video line length.
F	Black burst (NTSC includes pedestal).

Output Reconstruction Filters

The 2x oversampling of internal digital data before the output D/A converters of the TMC22090 not only reduces the Sin(x)/x high-frequency roll-off but eliminates complicated reconstruction filters. This is particularly important as the frequency response of digital filters is dependent upon the sample rate while the frequency of the aliased subcarrier component is fixed. The filters are terminated on the board. If termination on the board is not required, simply remove the appropriate link behind the BNC connector (E4, E5, E6).

Operation Without a CCIR-601 Source

Only rotary switch positions 0, 1, and 2 are useful without a CCIR-601 digital video source available. These switch positions produce color bars and a modulated ramp These test patterns are inserted into the pixel data path after the CLUTs in RGB format and demonstrate 90% of the circuitry of the TMC22090. To provide a PXCK in the absence of a CCIR-601 source, switch E2 to internal.

Power Supply Requirements

The TMC22061P7C board requires 1.25 Amps from the +5 Volt power supply and 0.25 Amps from the -5 Volt power supply. The -5 Volt power supply powers ECL logic devices which have relatively good noise immunity. The +5 Volt power supply not only drives TTL logic devices but it also provides the power to the TMC22090. Therefore, it is recommended that a bench power supply is used with the cable lengths kept to a minimum. When operating in stand-alone mode, only +5 Volts is required.

On-Board Read-Only Memory

The table on the next page shows the content format of the EPROM which hold the 64 pages of setup data.

Table 2. EPROM Address Map

Address	Contents
0	
1	CLUT address pointer set to 00_h
2	Start of CLUT data
:	V_{n-1}
:	V_n
:	V_{n+1}
769	End of CLUT data
770	Control Register pointer set to 00_h
771	Start of Control Register data
:	
:	
851	End of Control Register data
852	Unused locations set to 00_h
:	
:	
1023	Unused locations set to 00_h

APPENDIX A. TMC22061 Parts List

Item	Qty	Part/Value	Ref. Designator	P/N, Mfg. No.
1	2	Ferrite Beads	L1, L2	2743001112, FAIR-RITE Prod. Corp.
2	3	Inductors, 1.8μH	L3, L5, L7	IMS-2 1.8μH +/- 5%, Dale
2	3	Inductors, 1.0μH	L4, L6, L8	IMS-2 1.0μH +/- 5%, Dale
3	33	Ceramic capacitor, 0.1 μF	C3-C5, C9-C14, C43 C17-C20,C22-C39,C41	MD015C104KAB, AVX
4	4	Ceramic capacitor, 0.01 μF	C1, C16, C40, C42	MD015C103KAB, AVX
5	3	Ceramic capacitor, 47 pF	C57, C59, C61	SR151A470JAA, AVX
7	3	Ceramic capacitor, 100 pF	C45, C49, C53	SR151A101JAA, AVX
7	6	Ceramic capacitor, 330 pF	C44, C47, C48, C51, C52, C55	SR133A561JAA, AVX
8	2	Tantalum capacitor, 0.47 μF	C2, C15	TAP474K035SCS, AVX
9	2	Tantalum capacitor, 22 μF	C7, C8	TAP226K035SCS, AVX
10	9	Resistor, 75Ω	R15-R20, R22-R24	RN50C75R0F
11	9	Resistor, 120Ω	R3, R5-R12	RN50D1200F
12	1	Resistor, 412Ω	R14	RN50C4120F
13	1	Resistor, 3.3kΩ	R1, R13, R21	RN50C3301F
14	1	Resistor, 4.7kΩ	R2	RN50D4701F
15	1	Resistor, 47kΩ	R4	RN50D4702F
16	1	SIP resistor, 3.3kΩ	RN1	4308R-101-332, Bourns
16A	1	SIP resistor, 3.3kΩ	RN2	4310R-101-332, Bourns
17	1	1N4148 Silicon Diode	CR1	1N4148
18	1	LT1004 Bandgap Reference	CR2	LT1004-1.2, Linear Technology
18A	2	1N4004 Silicon Diode	CR3, CR4	1N4004, Motorola
19	1	TMC22090 Encoder	U18	TMC22090R0C, Raytheon Semiconductor.
20	2	16R8 PAL	U9, U20	TIBPAL16R8-15CN, Texas Inst.
21	2	20R8 PAL	U10, U11	TIBPAL20R8-15CNT, Texas Inst.
22	1	27512 Eprom	U12	TMS27C512-120JL, Texas Inst.
23	3	10125 ECL-TTL Translator	U16, U19, U22	MC10125P, Motorola
24	1	74F08 Quad 2-input AND	U13	MC74F08N, Motorola or equiv.

APPENDIX A. TMC22061 Parts List (continued)

Item	Qty	Part/Value	Ref. Designator	P/N, Mfg. No.
25	1	74LS74 Dual D-type FF	U14	MC74LS74AN, Motorola or equiv.
26	3	74F163 4-bit counter	U1, U5, U4	MC74F163AN, Motorola or equiv.
27	3	74LS163 4-bit counter	U6, U7, U8	MC74LS163AN, Motorola or equiv.
28	1	74F174 Hex D-type FF	U2	MC74F174AN, Motorola or equiv.
29	2	74F374 Octal D-type FF	U17, U23	MC74F374N, Motorola or equiv.
30	1	74HCT374 Octal D-type	U15	MC74HCT374N, Motorola or equiv.
31	2	74F377 Octal D-type FF	U21, U24	MC74F377N, Motorola or equiv.
32	1	Crystal oscillator	Y1	MXO-55GA-2C-27MHz, CTS-Kyight F1100H-27MHz, Fxo
33	15	Test points	TP1-TP15	ME151-203-100, Mouser
34	4	Shorting block		ME151-8000, Mouser
35	4	Jumpers	E1, E4, E5, E6	NSH-36SB-S1-TR, Robinson-Nugent
36	1	Power Connector	J1	ELM033100, PCD
37	3	BNC connectors	J2, J3, J4	31-5431, Amphenol
38	1	S-VIDEO Connector	J5	749263-1, Amphenol
39	1	25-pin D-connector	P1	617BO25SAJ220, Amphenol
40	2	SPDT switch	E2, E7	090320102, Secma Inc.
41	1	SPDT switch	S2	ATIDG-RA-1, Alco Switch
42	1	SPDT switch	S3	TP11FG-RA-0, Alco Switch
43	1	HEX rotary switch	S1	350134GSV, EECO
44	1	PLCC socket		PLCCB-84-PS-T, Robinson-Nugent
45	1	Oscillator socket		ICA-143-SCO-TG30, Robinson-Nugent
46	2	20-pin DIP socket		ICA-203-S-TG30, Robinson-Nugent
47	2	24-pin DIP socket		ICA-243-S-TG30, Robinson-Nugent
48	1	28-pin DIP socket		ICA-286-S-TG30, Robinson-Nugent
49	1	Universal transistor mount		111-080, BIVAR
50	4	Standoff		1902F, Keystone
51	1	Bare PC Board		40X07140 Rev. B, Raytheon Semi.

APPENDIX B PAL Functions Listings

This appendix contains the programmable array logic listings of the devices used on the TMC22061P7C evaluation board. These listings are shown as ABEL_HDL source files. The following brief tutorial is provided and refers only to terms used for programming logic used on this board,.

Sets

A set is a collection of signals and constants that are operated on as one unit. Any operation applied to a set is applied to each element in the set. For example in U9,

```
count = [c3,c2,c1,c0]
```

Valid operations used on the TMC22061P7C are:

Operator	Example	Description
:=	A := [1,0,1]	registered assignment
!	!A	NOT: ones complement
&	A & B	AND
#	A # B	OR
==	A == B	equal
!=	A != B	not equal
<	A < B	less than
<=	A <= B	less than or equal
>	A > B	greater than
>=	A >= B	greater than or equal

The basic elements of a source file

Module The module statement names the module and indicates the presence of any dummy variables used.

Title The title statement can be used to give a title or description for the module.

Declarations Declarations associate names with devices, pins, nodes, constants, macros, and sets.

Equations It is possible to use equations, state diagrams, or truth tables to describe logic designs. All programmable devices in appendix A use equations.

End The end statement terminates the module. Comments begin with double quotation marks, " ", and end with either another double quotation mark or the end of line, whichever comes first.

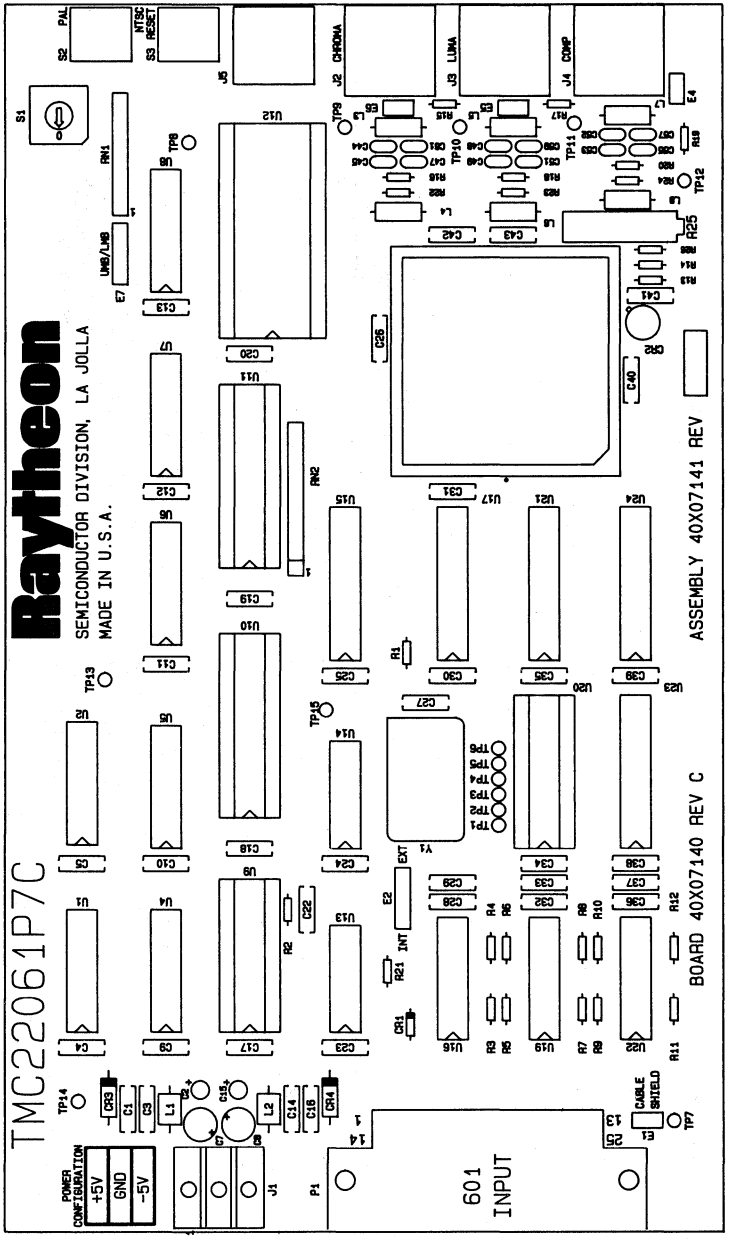
```
Board Reference Designator U9

Module    bd1_u9
Title     'VVSYNC generation and reset control logic'
Declarations
                    bd1_u9 device "P16R8';
    "inputs"
                    clk,v,pn,f                  pin 1,2,3,4;
                    s_reset                     pin 7;
    "outputs"
                    c0,c1,c2,c3                 pin 19,18,17,16;
                    fb,vvsync,pgmfb,pgm         pin 15,14,13,12;
    "notation"
                    count = [c3,c2,c1,c0];
                    t = (s_reset & !pgmfb) # pgm # (v & s_reset & !pgm &
                    pgmfb);
Equations
               !c0      := c0 & t & (count != 15)
                        #  !t;
               !c1      := !c0 & !c1 & t & (count != 15)
                        #  c0 & c1 & t (count != 15)
                        #  !t;
               !c2      := !c2 & !c0 & t & (count != 15)
                        #  !c2 & !c1 & t & (count != 15)
                        #  c2 & c1 & c0 & t & (count != 15)
                        #  !t;
               !c3      := !c3 & !c0 & t & (count != 15)
                        #  !c3 & !c1 & t & (count != 15)
                        #  !c3 & !c2 & t & (count != 15)
                        #  !t;
               !vvsync  := !fb & pn & ((count >= 3) & (count <= 5))
                        #  fb & ((count >= 4) & (count <= 5))
                        #  !fb & !pn & (count == 5)
                        #  ((count >= 6) & (count <= 7));
               !fb      := (!fb & v) # (f & !v);
               pgmfb    := s_reset;
               !pgm     := (count == 15)
                        #  s_reset & pgmfb & !pgm
                        #  !s_reset;
    End        bd1_u9
```

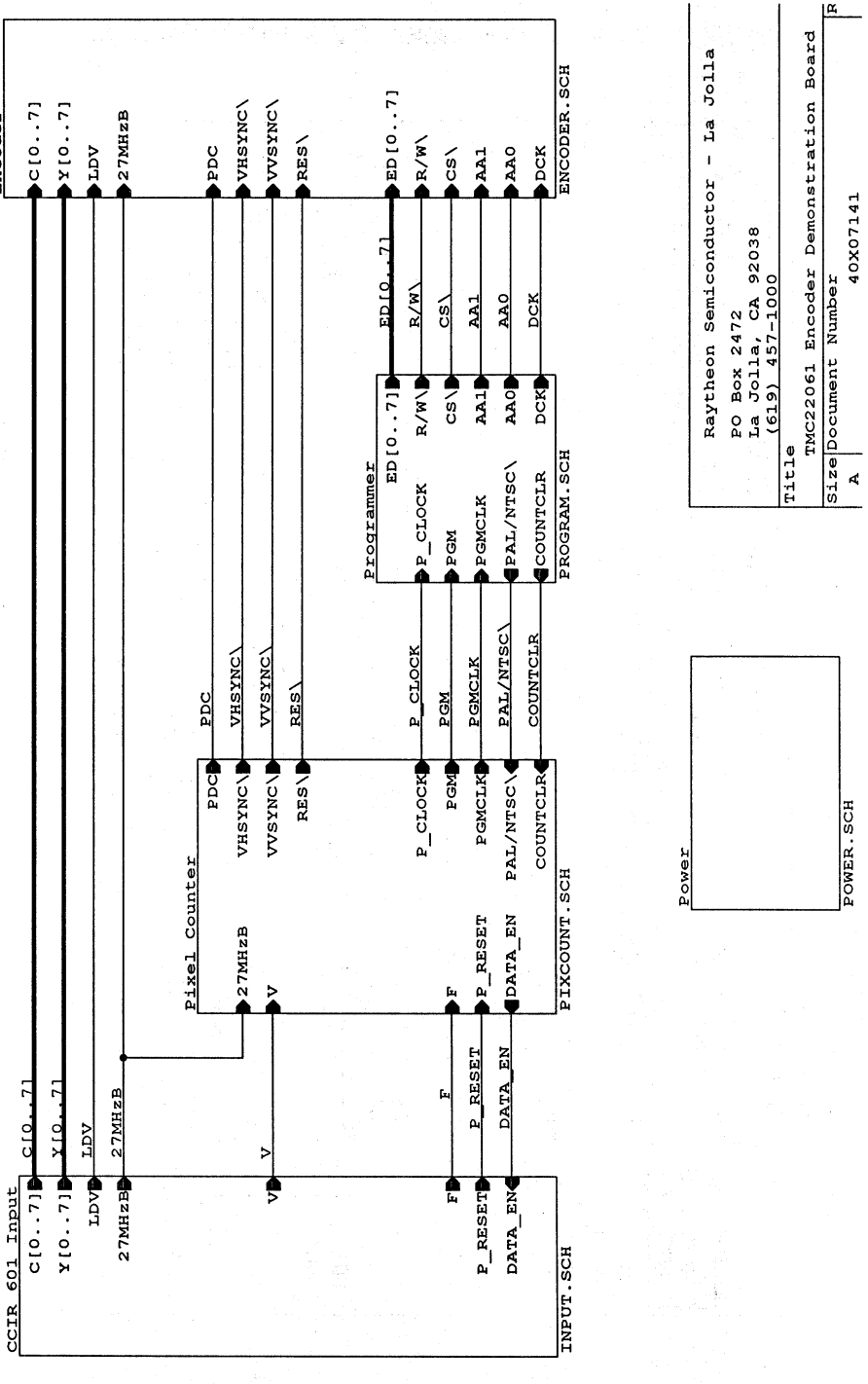
```
Board Reference Designator U10

Module     bd1_u10
Title      'VHSYNC generation and data control logic'
Declarations
                    bd1_u10 device "P20R8';
    "inputs"
                    a0,a1,a2,a3,a4,a5,a6        pin 2,3,4,5,6,7,8
                    a7,a8,a9,a0                 pin 9,10,11,14;
                    clk,pn                      pin 1,23;
    "outputs"
                    vhsync,pdc,hclk             pin 22,21,20;
                    h2clk,den,pclk              pin 19,18,17;
                    fb                          pin 16;
    "notation"
                    addr = [a10..a0];
Equations
               !vhsync  := ((addr >= 16) & (addr <= 256));
               !hclk    := ((addr >= 1712) & (addr <= 16));
               h2clk    := ((addr >= 15) & (addr < 256))
                           # !fb;
               !den     := a0;
               !pclk    := !a0;
               !fb      := ((addr >=766) & (addr < 1015);
    End
```

```
Board Reference Designator U11

Module     bd1_u11
Title      'TMC22090 programming control'
Declarations
                    bd1_u11 device "P20R8';
    "inputs"
                    clk                          pin 1;
                    a0,a1,a2,a3,a4,a5,a6         pin 2,3,4,5,6,7,8;
                    a7,a8,a9,a10,a11             pin 9,10,11,14,23;
    "outputs"
                    offset,zero,countclr         pin 22,21,20;
                    dck,rw,cs,aa1,aa0            pin 19,18,17,16,15;
    "notation"
                    addr = [a11..a0];
Equations
               !offset     := ((addr >= 3081) & (addr < 3265));
               !zero       := (addr == 0)
                           #  ((addr >= 3264) & (addr <= 3327));
               countclr    := (addr >= 3265);
               !dck        := !a1 & zero;
               !rw         := zero & (addr <= 3261);
               !cs         := (a1 & a0)
                           #  (!a1 & !a0)
                           #  (addr >= 3263)
                           #  !zero;
               !aa1        := (addr <= 9)
                           #  ((addr >= 3082) & (addr <= 3085))
                           #  !zero;
               !aa0        := !offset
                           #  (addr >= 3264)
                           #  !zero;
    End        bd1_u9
```

```
Board Reference Designator U20

Module    bd1_u20
Title     'TRS decode'
Declarations
                  bd1_u20 device "P16R8';
    "inputs"
                  d0,d1,d2,d3,d4,d5,d6,d7   pin 2,3,4,5,6,7,8,9;
    "outputs"
                  p1,p2,p3,f,v,h            pin 19,18,17,16,15,14;
                  p_reset,ldv               pin 13,12;
    "notation"
                  data = [d7..d0];
Equations
              !p1         := (data == ^hFF);
              !p2         := (data == ^h00) & !p1;
              !p3         := (data == ^h00) & !p2;
              !h          := (!h & p3) # (!d4 & !p3);
              !v          := (!v & p3) # (!d5 & !p3 & !d4)
                          #  (!v & !p3 & d4);
              !f          := (!f & p3) # (!d6 & !p3 & !d4)
                          #  (!f & !p3 & d4);
              !p_reset    := !p3 & d4;
              !ldv        := !p_reset # ldv;
    End       bd1_u9
```

APPENDIX C. Components Placement and Schematic Drawings

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PDC
VHSYNC\
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RES\
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R/W\
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PGM
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DCK
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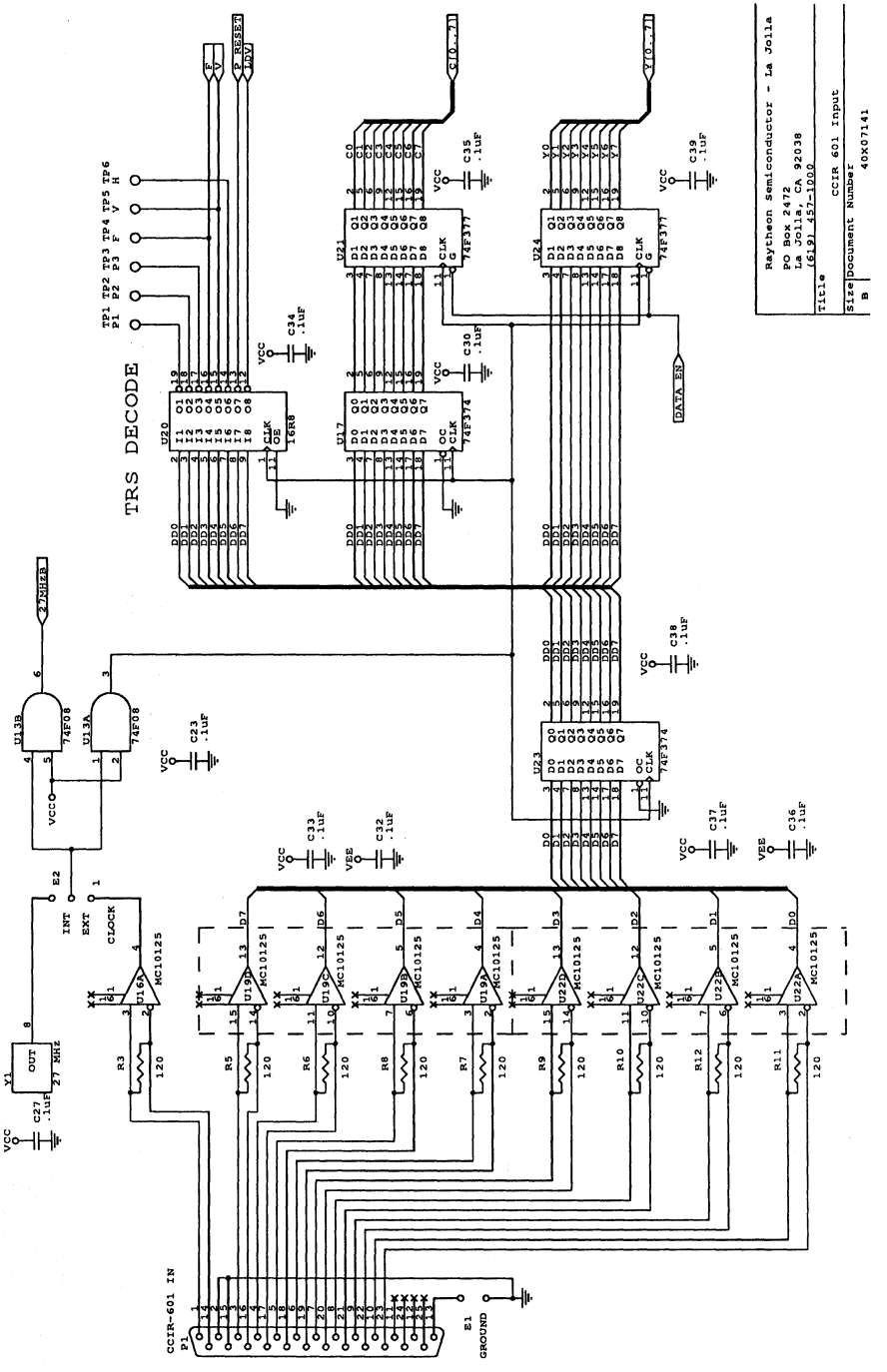
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INT
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CLOCK
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DATA EN
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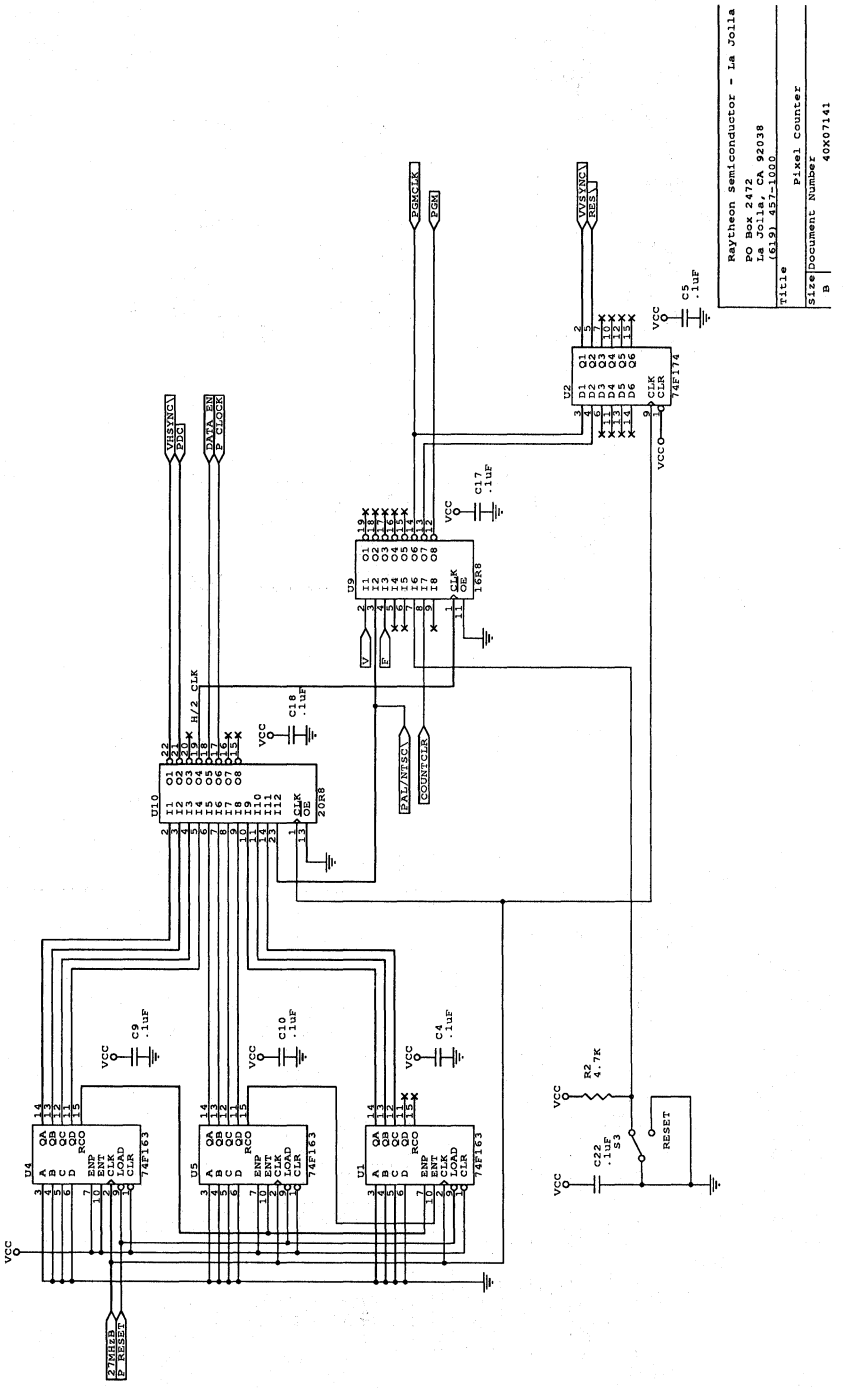
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H/2 CLK
PAL/NTSC\
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VCC
RESET
R2
4.7K
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C1
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C4
.1uF
C9
.1uF
C10
.1uF
C17
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U10
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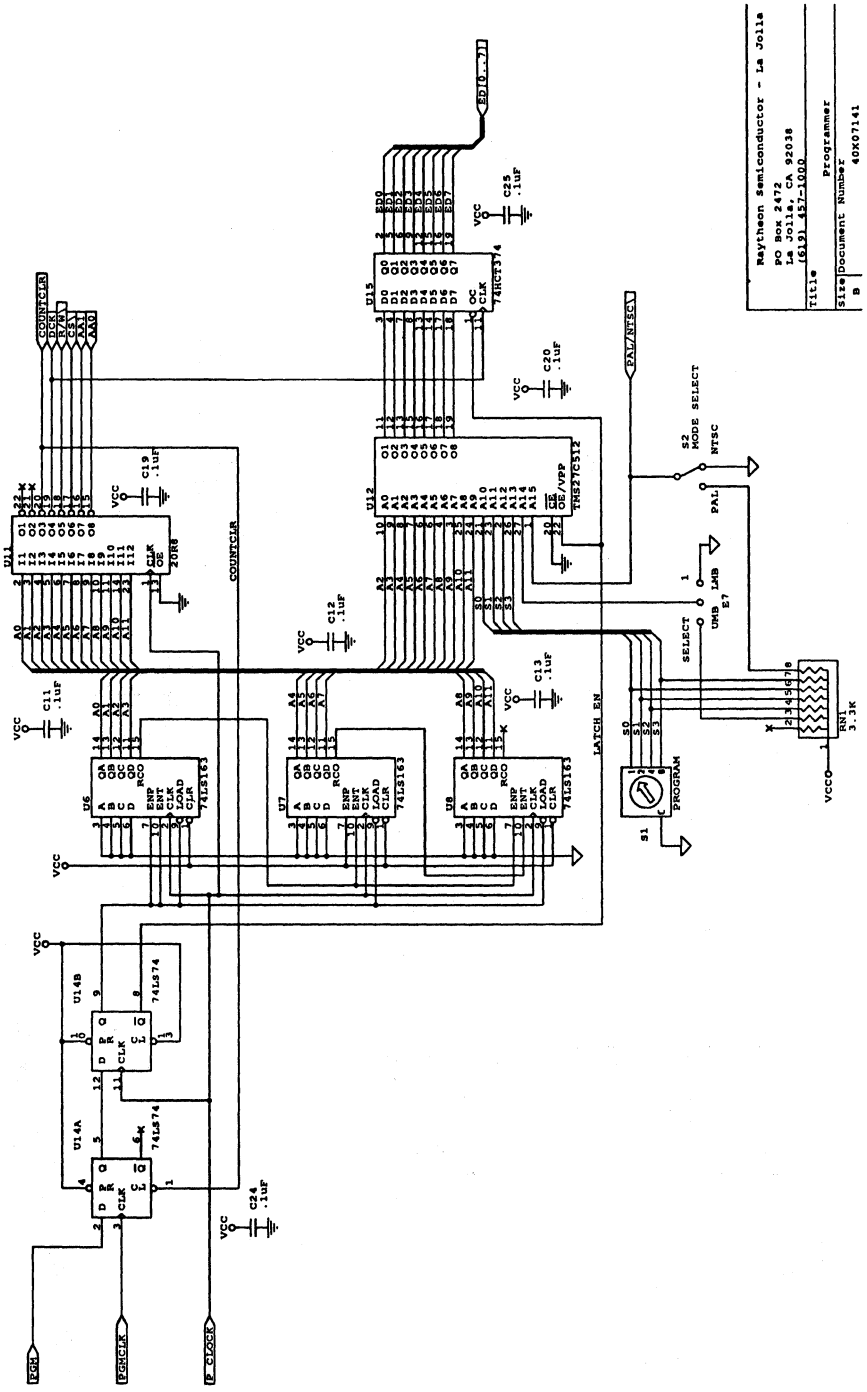
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La Jolla, CA 92038
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Size
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C13 .1uF
C11 .1uF
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U7
U8
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U14A
U14B
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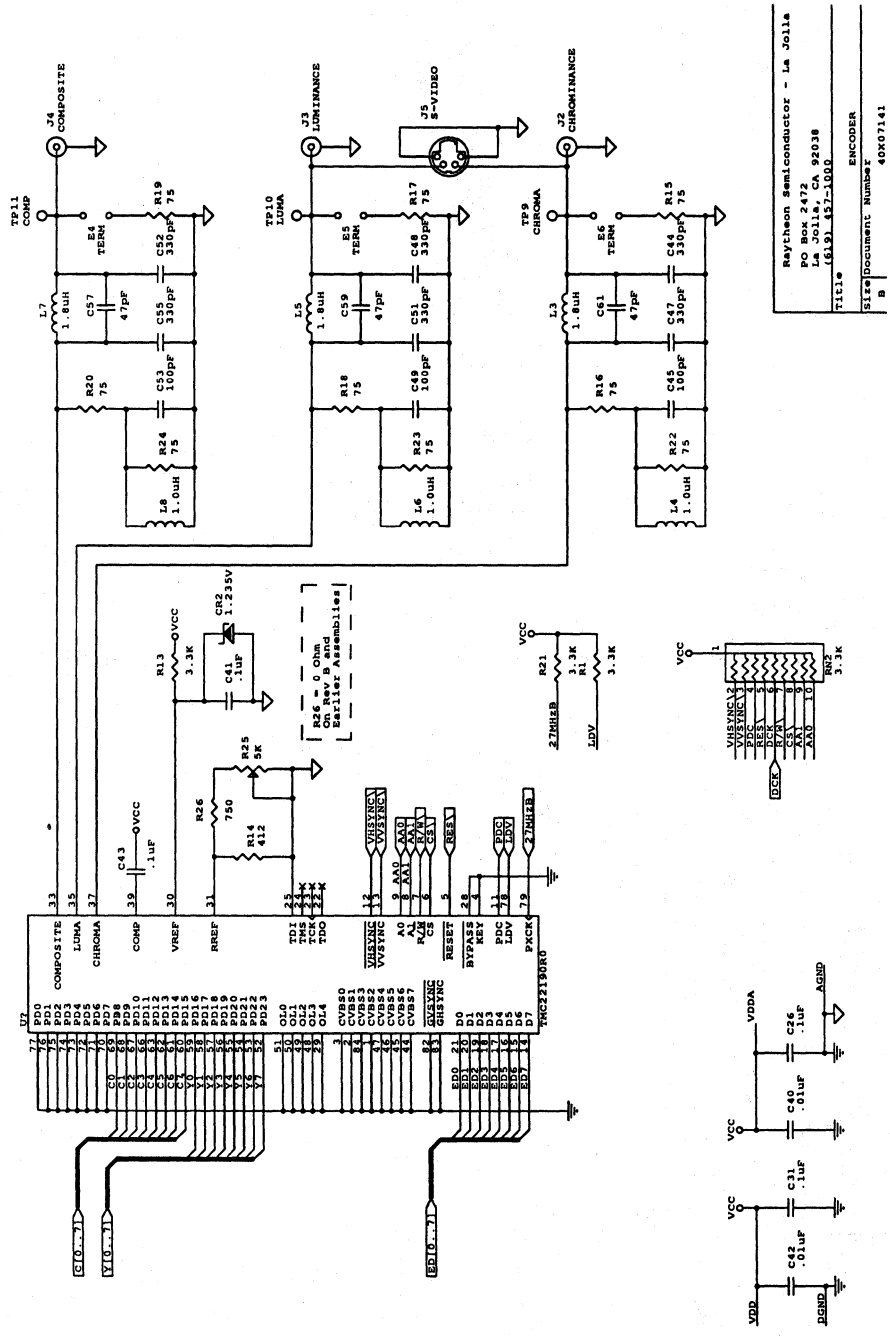
PAL/NTSC
S2
MODE SELECT
NTSC
PAL
SELECT
LAB
UNB
S7
LATCH EN
S0
S1
S2
S3
S1
PROGRAM
RN1
3.3K
VCCO
PGM
PGMCLK
P_CLOCK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J3 LUMINANCE
J5 S-VIDEO
J2 CHROMINANCE
TP11 COMP
TP10 LUMA
TP9 CHROMA
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E5 TERM
E6 TERM
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L5 1.8uH
L3 1.8uH
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C59 47pF
C61 47pF
C52 330pF
C55 330pF
C48 330pF
C51 330pF
C44 330pF
C47 330pF
R19 75
R17 75
R15 75
R20 75
R18 75
R16 75
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C49 100pF
C45 100pF
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R23 75
R22 75
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Raytheon Semiconductor - La Jolla
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(619) 457-1000
Title ENCODER
Size B
Document Number 40X07141
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COMPOSITE
LUMA
CHROMA
COMP
VREF
RREF
R13 3.3K
R25 5K
R26 750
R14 412
C41 .1uF
CR2 1.235V
C43 .1uF
R26 = 0 Ohm
On 24v B and
Delta Assemblies
R21 3.3K
R1 3.3K
27MHzB
LDV
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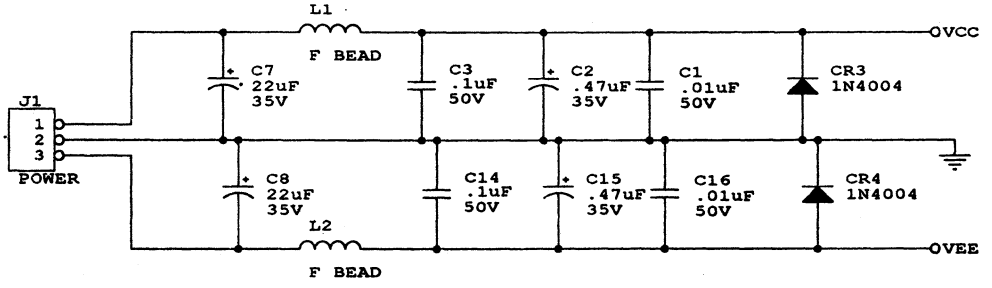

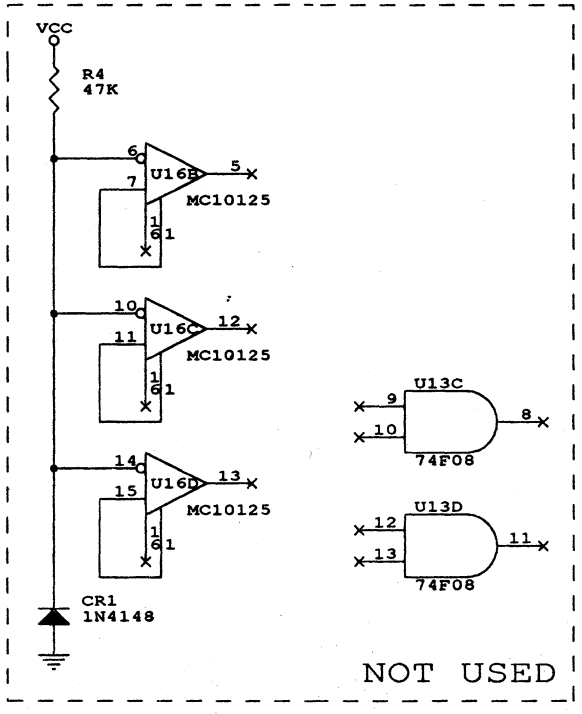

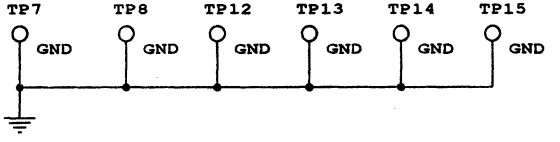

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Title: Power and Miscellaneous	
Size: A	Document Number: 40X07141

TP-51A

Additional Information

A schematic database is available in OrCAD[tm] format, along with PAL and EPROM Maps. Contact the factory.

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Bilinear Interpolation in Polar Coordinates

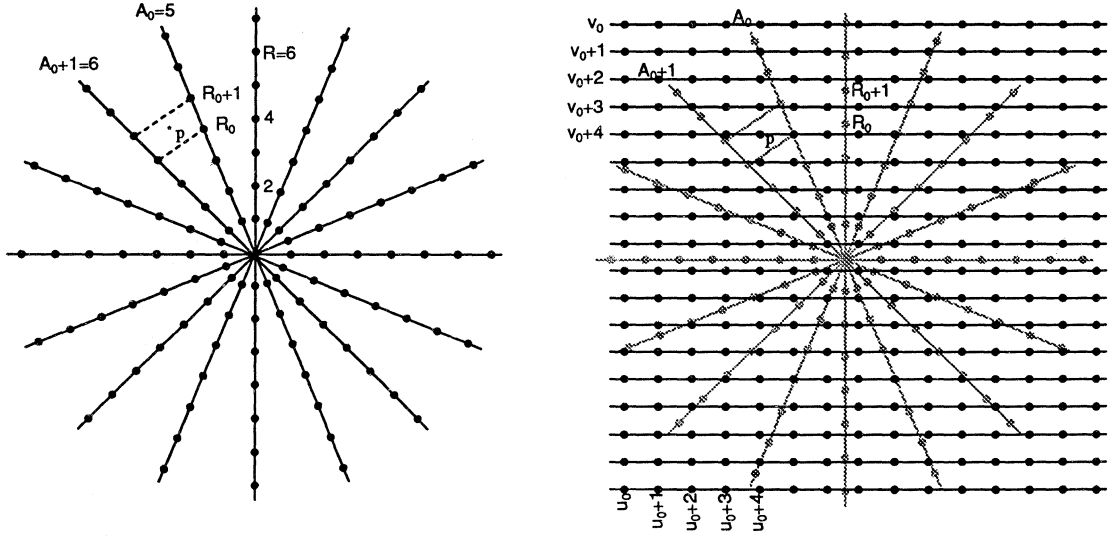
Bilinear Interpolation in Polar Coordinates

Dr. John A. Eldon

In many radar and medical scanner applications, data are collected in polar format at discrete range/azimuth positions, but displayed on a rectangular raster. To create a raster display or to prepare the data for manipulation, the user typically wants to locate, for every picture element (pixel) "p" with integer "target" Cartesian coordinates, the corresponding set of polar coordinates in the "source" data space.

In polar space, unless the transformed point p happens to coincide with one of the positions whose signal value is known, its value must be estimated from those of the surrounding points. As in conventional rectilinear resampling, one can interpolate the transformed point's value from those of the nearest one, four, or sixteen data points. This application brief provides some guidance for dealing with the geometric distortions inherent in polar-to-rectangular resampling. Although this application brief deals specifically with the problem of bilinear (four-point) resampling, the reader may extend it to other resampling kernel sizes.

Figure 1. Backmap from Raster to Polar



ORIGINAL DATA POINTS (BY AZIMUTH AND RANGE)

DESIRED DISPLAY RASTER GRID OF PIXELS

In Figure 1, the pixel "p," with raster coordinates ($u_0 + 4$, $v_0 + 4$) is found through a simple two-dimensional trigonometric transformation to lie at coordinates ($R_0 + f_R$, $A_0 + f_A$) in polar space. Assuming the polar coordinate center lies at (u_c , v_c) in the Cartesian raster, then for any point (u_p , v_p) in the raster, $R_p = ((u_p - u_c)^2 + (v_p - v_c)^2)^{1/2}$ and $A_p = \arctan ((v_c - v_p) / (u_p - u_c))$ for $x_p > x_c$ or $\pi + \arctan ((v_c - v_p) / (u_p - u_c))$ for $x_c > x_p$. If the length units of u and/or v differ from those of R, then the terms involving ($u_p - u_c$) and/or ($v_p - v_c$) need to be rescaled to make all length-dimension variables consistent in the above equations. In Figure 1, one unit of R corresponds to one unit of u, but 1.25 units of v. The polar coordinate origin lines at ($u_0 + 6.7$, $v_0 + 8.7$). The Pythagorean Theorem yields:

$$R_p = ((u_0 + 4 - u_0 - 6.7)^2 + 0.8^2 (v_0 + 4 - v_0 - 8.7)^2)^{1/2} = 4.34,$$

or $R_0 = 4$ and $f_R = 0.34$, separating the integer and fractional parts for later computational convenience. Since p is to the left of the polar center,

$$A_p = \pi + \arctan(0.8(v_0+8.7-v_0-4) / (u_0+4-u_0-6.7)) = 2.19 \text{ radians.}$$

Since the angular step in Figure 1's polar coordinates is $2\pi/16$ radians, $A_p = 2.19 / (2\pi/16) = 5.6$, or $A_0 = 5$ and $f_A = 0.6$.

In the example shown, the polar coordinates of the point "p," which lies at ($u_0 + 4$, $v_0 + 4$) in the display raster grid, are ($R_0 + f_R$, $A_0 + f_A$) = (4.34 , 5.6). Since the signal value at this precise location is not known, it is estimated from the values of the four nearest known data points, which define the dotted trapezoid surrounding p.

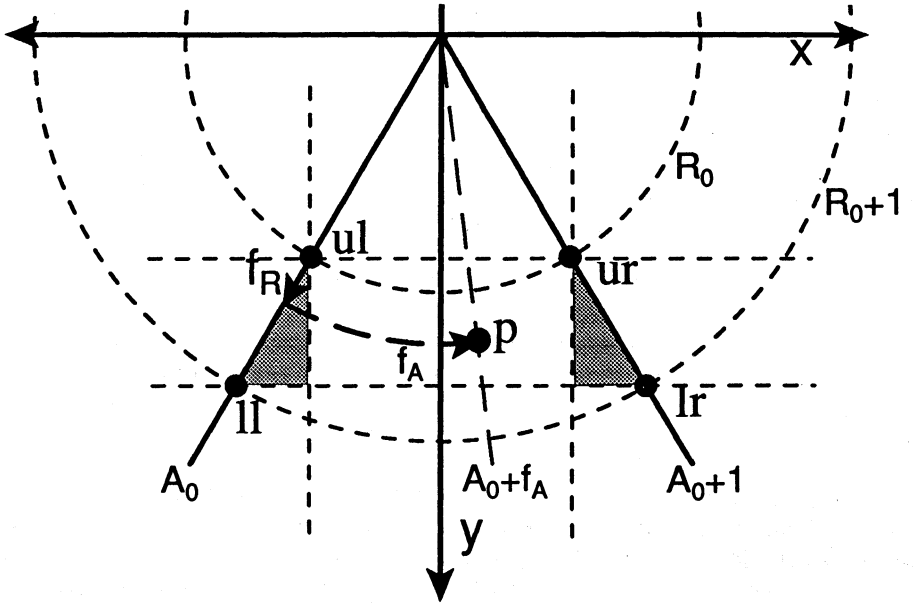
Figure 2 is an expanded and rotated view of transformed data point "p," whose coordinates in polar space are ($R_0 + f_R$, $A_0 + f_A$). The four surrounding known data values are "ul" (upper left) at (R_0 , A_0), "ll" at ($R_0 + 1$, A_0), "ur" at (R_0 , $A_0 + 1$), and "lr" at ($R_0 + 1$, $A_0 + 1$). Blindly and naively estimating the value at p from those at the four reference points according to the standard bilinear interpolation formula, would yield:

$$v (p) = ul (1 - f_A) (1 - f_R) + ur (f_A) (1 - f_R) + ll (1 - f_A) f_R + lr (f_A) f_R$$

For noncritical applications, this will produce acceptable results, particularly if the number of azimuthal bins is large and the number of range bins is small. However, many applications will demand at least some of the geometric corrections described below.

Since bilinear interpolation is a Cartesian procedure, an artificial rectangular grid, (x,y), is constructed with an origin coinciding with that of the polar data source space and with y-axis oriented at the angle $A_0 + 0.5$, halfway between p's four nearest neighboring data points. [Note that our point-specific local coordinates x and y, contrived strictly for convenience in the discussion which follows, are not generally aligned with the desired rectilinear display space.] If N represents the number of azimuthal rays per full circle, and A and F are defined as π/N and $A (2f_A - 1)$, respectively, then the rectangular coordinates of the transform point and its four surrounding data points are as listed in Table 1.

Figure 2. Bilinear Resampling with Polar Data



Here, the resampled point is again labeled "p," the four surrounding data points are labeled ul, ur, ll, and lr, the polar coordinate system has been rotated and local Cartesian coordinates x and y (not to be confused with display coordinates u and v) have been defined for convenience.

Table 1. Polar and Local Rectangular Coordinates

Point	Polar	Rectangular
p	$(R_0 + f_R , A_0 + f_A)$	$((R_0 + f_R) \sin (F) , (R_0 + f_R) \cos (F))$
ul	(R_0 , A_0)	$(-R_0 \sin (A) , R_0 \cos (A))$
ur	$(R_0 , A_0 + 1)$	$(R_0 \sin (A) , R_0 \cos (A))$
ll	$(R_0 + 1 , A_0)$	$(-(R_0 + 1) \sin (A) , (R_0 + 1) \cos (A))$
lr	$(R_0 + 1 , A_0 + 1)$	$((R_0 + 1) \sin (A) , (R_0 + 1) \cos (A))$

Having established the positions of the four reference points and the transform point in the new rectangular space, proceed with the bilinear interpolation, noting any distortions arising from the polar format of the data.

First, consider the y dimension. Each reference point's y coordinate is scaled by a factor of cos (A), whereas the y coordinate of p is scaled by cos (F), which can vary in value from 1 to

cos (A). The maximum distortion of p's y position occurs when p lies on the y axis, i.e., when f_A = 0.5. In this case, the positional distortion and thus the interpolation accuracy will be a function of radial position (range) and azimuthal step size, i.e., the number of data scan directions. For example, if there are 64 range bins and 128 scan angles spread over a full circle, then the maximum distortion will be 64 * (1 - cos (π/128)) = 0.02 range bins. This implies that if R_0 = 64 and f_A = 0.5, the point p will lie 0.02 range bin lower (farther from the origin) than indicated by f_R. To correct for this effect, the user would increase f_R by 0.02 before interpolating radially. Without this correction term, proceed with the first dimension of a conventional bilinear interpolation, multiplying the values at ul and ur by (1 - f_R) and the values at ll and lr by f_R. To apply the correction, replace f_R with f_R', where:

$$f_R' = f_R + (R_0 + f_R) (\cos (\pi (1 - 2f_A) / N) - \cos (\pi/N))$$

The correction term vanishes as the transformed point approaches one of the source data azimuthal axes, i.e, as f_A approaches 0 or 1.0. Furthermore, the error grows linearly with range. Perhaps the simplest way to handle this is to increase the size of the coefficient table, so that it can be addressed jointly by f_R, R_0, and f_A, instead of only f_R and f_A.

Using similar logic, examine distortion in the x direction, to compute the appropriate adjustment for f_A. The x coordinates of points ul and ur are - R_0 sin (π/N) and R_0 sin (π/N), respectively, whereas the x coordinate of p is (R_0 + f_R) sin (π(1 - 2f_A) / N), and the x coordinates of the two lower reference points are -(R_0 + 1) sin (π/N) and (R_0 + 1) sin (π/N). With no geometric correction, one would execute the second dimension of the bilinear interpolation by multiplying ul and ll by (1 - f_A) and ur and lr by f_A.

To apply a geometric correction to the second dimension of the bilinear interpolation, note first that the distance between the two lower reference points is L = 2 (R_0 + 1) sin (π/N), whereas the x coordinate of p is (R_0 + f_R) sin (π(1 - 2f_A) /N). The horizontal projections of the distances from ll to p and from p to lr are M = (R_0 + 1) sin (π/N) - (R_0 + f_R) sin (π(1 - 2f_A) /N) and N = (R_0 + 1) sin (π/N) + (R_0 + f_R) sin (π(1 - 2f_A) /N), respectively. Instead of multiplying ll by (1 - f_A), multiply it by N / L. Similarly, to apply the geometric correction to lr, multiply it by M/L instead of f_A.

Finally, the problem of horizontal interpolation between the two upper reference points, ul and ur, is addressed. With no geometric correction, ul is multiplied by (1 - f_A) and ur by f_A. If p's x coordinate falls between -R_0 sin (π/N) and +R_0 sin (π/N), then define l, m, and n following the development of L, M, and N in the previous paragraph, viz:

$$l = 2 (R_0) \sin (\pi/N),\ m = R_0 \sin (\pi/N) - (R_0 + f_R) \sin (\pi(1 - 2f_A) /N), \text{ and}$$
$$n = R_0 \sin (\pi/N) + (R_0 + f_R) \sin (\pi(1 - 2 f_A) /N).$$

Then, multiplying ul by n/l and ur by m/l will yield a geometrically corrected result.

The problem with this approach is that it doesn't satisfactorily address p's which fall near one of the azimuthal axes, such that x (p) is between x (ul) and x (ll) or between x (ur) and x (lr), as in the shaded regions of Figure 2. The denser our set of data - bearing azimuthal scanlines,

the less significant this problem is. One fairly clean way to handle the problem is to reduce the bilinear interpolation to a one - dimensional linear interpolation in such cases, taking advantage of the proximity of p to two known data points. Thus, as f_A approaches 0, compute the value of p as:

$$v(p) = ul(1 - f_R) + ll(f_R)$$

As f_A approaches 1.0, one would use a similar one - dimensional interpolation, substituting ur for ul and lr for ll.

To decide if and when to employ a geometric correction in polar data resampling, the user should run a series of test simulations with simple geometrical shapes as source data and watch for distortions and other artifacts during resampling. If present, artifacts will generally be most noticeable at the largest radii. Alternatively, the user can employ the geometric correction equations presented in this paper to calculate the worst - case spatial distortion and then judge whether this would be visually objectionable.

RC4193/4391 Switching Regulators

Table of Contents

Introduction

The RC4193 and RC4391 are low power switching regulator control ICs, complete with all the active components needed to build small power supplies. The 4193 is dedicated to step up applications ($V_{IN} < V_{OUT}$) and uses an internal NPN power transistor, while the 4391 is set up for step down ($V_{IN} > V_{OUT}$) and inverting (positive input, negative output) applications, and includes a PNP power transistor. More detailed information, such as pin out, specifications, and basic usage are contained in the RC4191/4192/4193 Data Sheet and the RC4391 Data Sheet. This application note is intended to supplement the data sheets; it provides extra application circuits plus additional design and troubleshooting aids.

First is a brief section with guidelines for determining whether these micropower regulators meet your application requirements. Next is a discussion of the internal oscillator. Limitations and characteristics of the oscillator are provided, along with some circuits that use the oscillator (C_X) pin for other purposes. After the oscillator section is a very basic 4391 application (step down) which was not included in the RC4391 Data Sheet. Following this step down application are some specifically tailored 4193 application circuits, with specifications and PC card layouts. These dual op amp supply applications give the reader good examples of the size, simplicity, and performance made practical by the RC4193 and RC4391.

Near the end of this application note is a section on designing a pot core inductor to fill the requirement for an external inductor. This inductor design guide was intended for engineers without a strong background in magnetics; it shows how to select a core and wind it properly without an excess of equations or complex calculations that confuse many first time switching regulator users. Included are design examples that start with the application requirements and end up with a finished pot core design.

Last is a troubleshooting chart listing common prototype breadboarding problems and possible causes and cures.

Application Suitability

Selecting the best switching regulator controller for a given application means reviewing the strengths and weaknesses of the controllers available and deciding which fits in your niche. The main strengths of Raytheon's 4193 and 4391 are their small size, low quiescent current, and versatility; the weaknesses are relatively low power transistor current rating (375mA), imprecise oscillator frequency, higher EMI (electromagnetic interference), and single ended output.

1. **Small Size**

   The Raytheon circuits are packaged in an 8-lead mini-DIP, and this combined with the low external component count reduces the amount of PC board area needed to about 1 inch^2 . Also, they work well up to 75kHz, reducing the size of the inductor core required. Therefore on card power supplies where the regulator is built on the same PC board with other circuitry are practical and cost effective. Competitive manufacturers' controllers usually come in 14 or 16 lead packages and require more external components.

2. **Efficiency**

   The efficiency depends on two major factors: The ratio of controller power consumption to load power, and the saturation voltage of the power switch transistor. First, 4193 and 4391 feature very low supply current, so the power consumed will be very low compared to the load power. If the load power is high then this feature loses importance, and controllers with milliamps of supply current become acceptable. Second, the saturation voltage of the power switch transistor will reduce efficiency at high switch currents. External switch transistors can help here, but add to circuit complexity and cost. Below are some general guidelines for efficiency and load power, showing the range of power that Raytheon's circuits are practical for.

	Efficiency		
Load Power	4193	4391	Comments
0 to 150mW	70 to 80%	60 to 70%	Ideal range
150 to 400mW	60 to 70%	50 to 60%	Somewhat reduced efficiency
400mW to 10W	50 to 80%	60 to 80%	External power transistor
>10W	Impractical for 4193/4391 due to imprecise oscillator frequency		

3. **Versatility**

   Between the 4193 and the 4391 all the standard switcher configurations can be built using a minimum of external components.

The 4193 is dedicated to step up applications and the 4391 covers inverting and step down applications. Also, a variety of other features are possible using the remote shutdown capability and low battery detection circuitry (see the applications in the 4191/4192/4193 Data Sheet and later in this publication for examples).

4. **Oscillator Tolerance**

   Because the oscillator is constructed with diffused resistors the initial accuracy and drift with temperature of the oscillator frequency is poor. Therefore, the application circuit must be overdesigned so that units with a higher than nominal frequency will meet the output load current drain, and units with a lower than nominal frequency do not overcurrent or overheat the power transistor or overcurrent and saturate the inductor. At high load power (> 10W) this variation becomes impractical, since an increase in component specifications tolerable at lower power becomes expensive and bulky at high power. See the section titled "Oscillator" for more information.

5. **EMI (Electromagnetic Interference)**

   The 4193 and 4391 use a variable duty cycle method of feedback control rather than pulse width modulation (PWM) control. Under reduced load current or no load conditions the duty cycle will be greatly reduced and the short pulses produced will cause greater RF radiation, due to the increased high frequency components of the voltage switching waveform at the switch transistor. This problem of somewhat greater EMI at low loads is offset by the benefit of variable duty cycle control having no minimum load required. PWM circuits usually require some minimum load current to maintain regulation.

Oscillator

Internal Design

The oscillator creates its square wave like the popular RC555 timer does: by the charge and discharge of a capacitor, controlled by two voltage level detectors and a current steering flip-flop. See Figure 1.

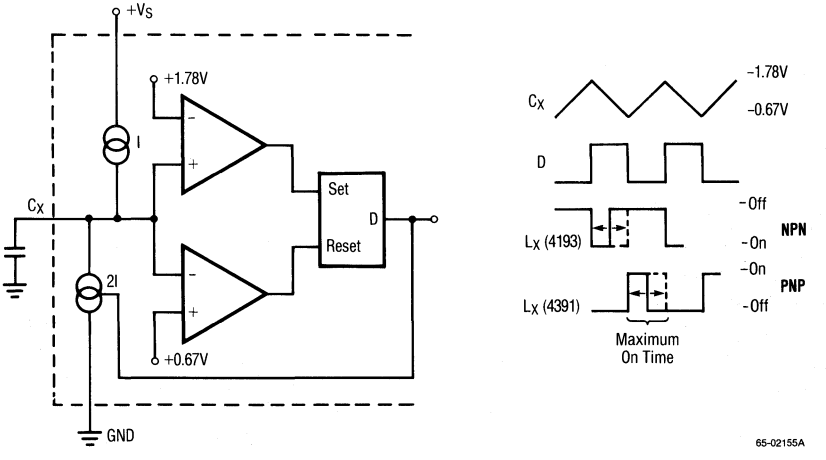


Figure 1. Oscillator Block Diagram and Waveforms

When power is first applied, the timing capacitor C_X charges up from a constant current source I, integrating the current into a linear voltage ramp. The voltage ramps up until it reaches the upper comparator threshold, at which time a current sink 2I which subtracts from I is switched in; the resultant negative current discharges C_X. The voltage on C_X then ramps downward, until it hits a lower threshold voltage, switching 2I out, and the voltage again ramps upward. This cycle repeats itself endlessly and the resultant triangular waveform can be observed at the C_X pin. The square wave output is internal and cannot be directly observed. Note also that the 10pF capacitance of a 10X scope probe will change the frequency of oscillation.

The internal power transistor switches at the peaks of the triangle wave. The two Raytheon parts switch at opposite phases of the triangle; when the power transistor of the 4193 is on and the triangle wave on C_X is ramping down, the 4391's transistor is off. This means that when power is first applied, the 4193's transistor is on, a hard start condition that can cause latch up and excess supply current (the 4391 starts up with its transistor off). This hard start condition is easily cured with the addition of one capacitor (see the section "Soft Start" for details).

Frequency Accuracy

The oscillator was designed to be simple and operate down at low supply voltages, and as a result the initial frequency accuracy and drift with temperature are poor. All application designs must take this variation into account. Use ±30% tolerance in figuring worst case component values and ratings, ensuring that the inductor value is low enough for those units with a high oscillator frequency, and that the inductor and power transistor have a high enough peak current rating to cover those units whose oscillator frequency is lower than nominal. This ±30% tolerance is most important to high power applications, especially when selecting external power transistors and inductor cores.

Synchronized Oscillator

If a TTL or CMOS square wave is available the internal oscillator may be slaved to the external signal. Figure 2 shows the one resistor interface.

In addition to its use in easing component tolerance problems this interface can help in troubleshooting switching problems on prototype breadboards. The truth table (Figure 3) shows what state the internal power transistor will be in for combinations of C_X pin and V_{FB} pin conditions.

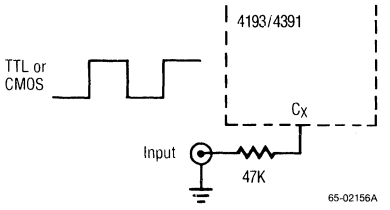


Figure 2. Synchronized Oscillator Interface

C_X	V_{FB}*	L_X (4193)	L_X (4391)
High	High	Off	Off
High	Low	On	Off
Low	High	Off	On
Low	Low	Off	Off

*"High" = tied to supply through 100K
"Low" = tied to ground through 100K
"Low" = tied to negative voltage through 100K (4391 only)

Figure 3. Truth Table for C_X and V_{FB} (Static Conditions)

Duty Cycle

There is a 5μS turn off delay of the 4193 power transistor (3μS for the 4391). When on, the transistor saturates and remains on 5μS after the oscillator (C_X) transition. This causes the maximum duty cycle to be greater than 50%, and increases with increasing oscillator frequency. For this reason application designs should be limited to 75kHz maximum operating frequency.

The duty cycle can be varied somewhat by connecting a high value resistor between the C_X pin and either ground or $+V_S$. Note the difference in polarity between the 4193 and 4391; a pull up resistor decreases the 4391 duty cycle and increases the 4193 duty cycle. Limit the current in this resistor to 0.5μA (2MΩ from C_X to ground).

The variable duty cycle method of feedback control used (as opposed to PWM) turns on the switch transistor only when the load demands current. This feedback system responds to a wide range of load currents, and regulates tightly from no load to full load where other systems require a minimum load. However, this on

demand system can make the oscillator appear "noisy," as its voltage waveform may not be in synchronization with the oscillator waveform. This is a normal operating condition, but may cause extra EMI (electromagnetic interference) under reduced output loading conditions.

Soft Start

At the moment power is applied the 4193 is fully on, and the resultant current spike can cause the supply voltage to sag or the inductor to saturate and complicate startup. Many of these problems can easily be cured by adding a capacitor to the startup circuit as shown in Figure 4.

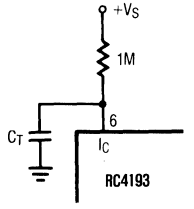


Figure 4. Soft Start Circuit

The delay introduced by the RC time constant at startup allows the output filter capacitor to charge up before the power transistor switches on, reducing the instantaneous supply current. A typical value for C is in the 0.1μF to 1.0μF range.

Delayed Start

A more sophisticated delay start feature may be added by use of the low battery detector. See Figure 5 for a schematic.

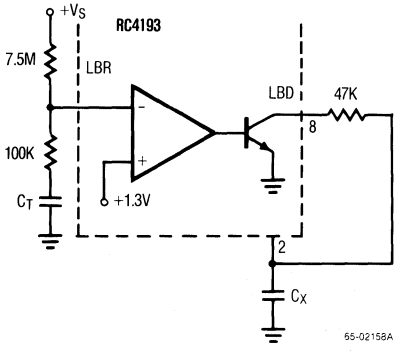


Figure 5. Delayed Startup Circuit

In this case the open collector LBD (Low Battery Detector) output clamps the oscillator pin (C_X) low and forces the power transistor off. Slowly the capacitor C will charge up to the LBR threshold. When the +1.3V threshold is reached, the LBD comparator will reverse its state and unclamp the oscillator, allowing it to run freely and toggle the power transistor. This can be used for much longer delays than the soft start circuit.

Current Limiting

The oscillator (C_X) pin can also be used to add short circuit protection in a method similar to the external sync interface. A transistor V_{BE} is used as a current sensing comparator which resets the oscillator upon sensing an overcurrent condition, thus providing cycle-by-cycle current limiting. Figure 6 shows how this is applied to the 4391 in an inverting application.

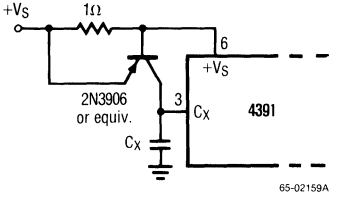


Figure 6. 4391 Short Circuit Current Limit

This idea is not as easy to implement with the 4193, because its C_X pin must be clamped low instead of high to force the output transistor off. The emitter of the output transistor is internally connected to ground, so putting a resistor in series is not possible. This idea will work for external transistors though, and a schematic is shown in Figure 7.

4391 Step Down

The next section describes a new 4391 application, using the 4391 to provide the step down or "buck" configuration instead of using a 4193 plus external transistor. This application is important because it eliminates the external transistor in low power step down applications (saving PC real estate and parts costs) and also extends the input voltage range.

Figures 8 and 9 show block diagrams of how this trick is done. In Figure 8 the ground pin of the device is connected to circuit ground, and the circuit regulates to a lower output voltage.

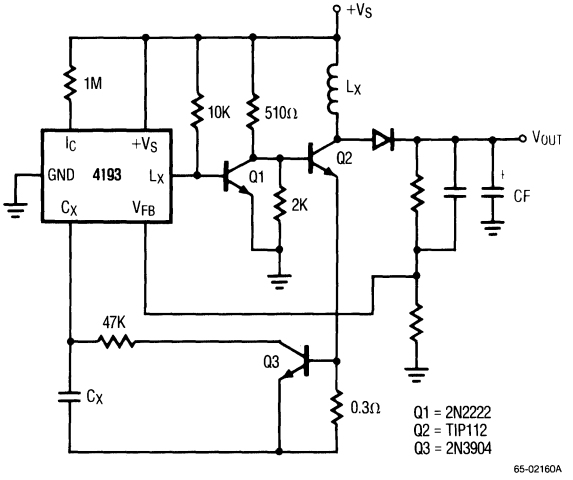


Figure 7. Typical High Power Interface With Current Limit (4193)

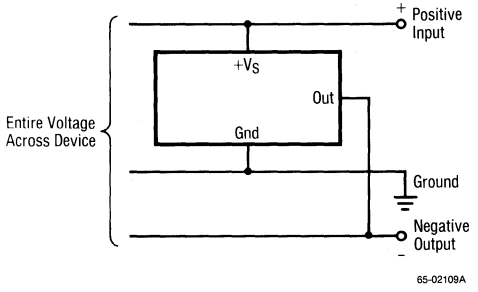


Figure 8. Normal 4391 Inverting Circuit

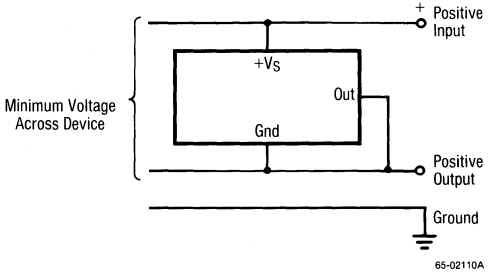


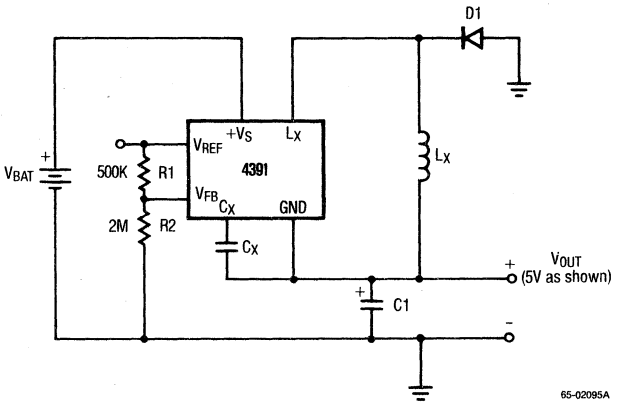
Figure 9. New 4391 Step-Down Circuit

Regulating to a voltage lower than ground provides the normal (positive input, negative output) inverting circuit. Figure 9 shows the ground pin of the device connected to a positive output voltage instead of circuit ground. This connection increases the supply voltage range, increases efficiency, and renders the 4193 step-down circuits obsolete.

The standard step-down application for the 4193 regulator requires the use of an extra external PNP transistor. The reason for this is that the power switch transistor internal to the 4193 is an open collector NPN with its emitter tied to ground, and the step-down mode needs a PNP with its emitter wired to the positive supply. The 4391 application shown in Figure 10 eliminates the extra transistor in step-down circuits.

The 4391, ordinarily an inverting regulator (positive in, negative out), requires that the output voltage sensed by the feedback resistor to be a negative voltage with respect to the ground pin of the device. In this step-down circuit the 4391 is tricked into believing that the output is negative by wiring its ground pin to the output filter capacitor and its feedback resistor to the negative terminal of the battery.

When power is first applied, the 4391 senses that the feedback point is not negative enough with respect to its ground. Therefore, the transistor



IMPORTANT NOTE: This circuit must have a minimum load current ≥ 1mA always connected.

Figure 10. Low Power Step-Down Supply

switches, and pumps charge into the filter capacitor, raising the ground pin with respect to the negative battery terminal until it starts to regulate. Thereafter the feedback system will maintain a programmed voltage across the capacitor [V_{OUT} = (1.3V)(R2/R1)].

A side benefit of this arrangement is increased efficiency, because the supply voltage applied across the 4391 is less than the battery voltage (applied voltage = $V_{BAT} - V_{OUT}$). This means that less power is consumed by the regulator and so it subtracts less from the efficiency.

Figure 11 shows how the supply voltage range can be extended using a zener diode connected in parallel with the device. This zener protects the 4391 from start up transients. When power is

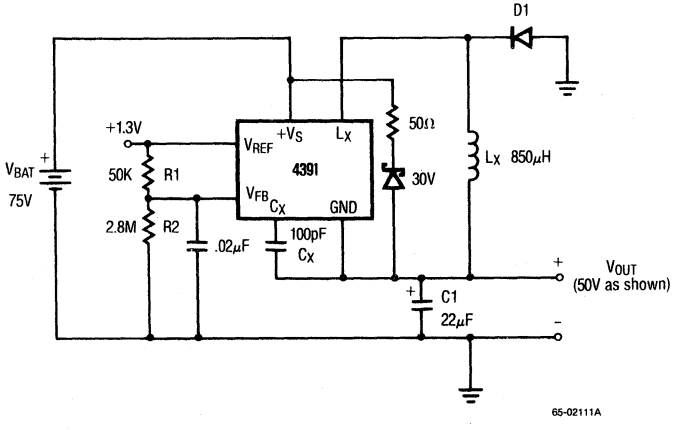


Figure 11. High Voltage Step-Down Supply

first applied the output filter capacitor is discharged, so the entire supply voltage is momentarily applied across the 4391. The zener diode provides a shunt path around the device so that the spike of current required to charge the output capacitor up to its regulated voltage does not flow through the 4391 and possibly damage it. Using this zener shunt gives the circuit capability to handle very high input voltages, provided the difference between input and output is within the 30V rating of the 4391. For example, a 75V supply could be safely regulated to 50V output, and could regulate to an even lower output voltage if a series zener (like the optional zener in Figure 12) is added.

4193 Low Voltage Start-Up

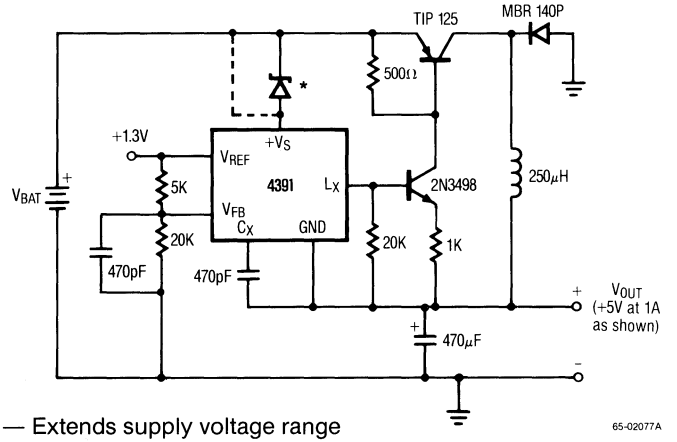
Figure 13 shows how the bootstrapped application can be "kicked on" using an extra capacitor and triple pole double throw switch. This connection allows the circuit to start up using a single Ni-Cad cell of 1.6 to 1.2V. When power is first applied the 1.2V battery does not provide enough voltage to meet the minimum 2.4V supply voltage requirement. The 22μF capacitor, when switched, temporarily doubles the battery voltage to bias up the 4193.

When the switch is in the down position, the capacitor charges up to the battery voltage.

Then, when the switch is changed to the up position, the capacitor is put in series connection with the battery, and the doubled voltage is applied directly to the positive power supply lead of the 4193. This voltage is enough to bias the junctions internal to the 4193 and gets it started. Then, when the stepped up output voltage reaches a high enough value, diode D1 is forward biased and the output voltage takes over supplying power to the 4193. The circuit is shown with component values for +5V output, but the circuit can be set up for other voltages.

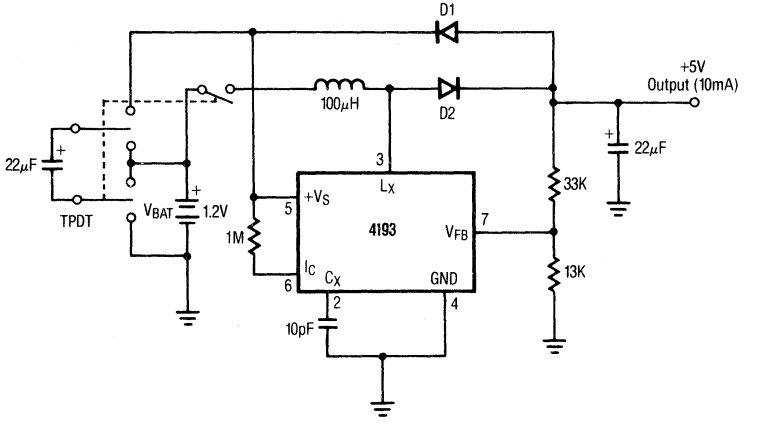
±12V Transformer Coupled Application

Transformer switching regulators have one great advantage over the standard single winding inductor applications: multiple windings can be taken from the secondary to produce multiple DC output voltages. Two output voltages are generated by the example below, the first being a well regulated +12V and the second being an unregulated -12V. The circuit could be built using two switching regulators (4391 and 4193) to provide two well regulated output voltages, but that approach requires two ICs, two inductor cores, and twice as much board space. The transformer coupled circuit eliminates much of this hardware at some expense of load and line regulation and winding complexity.



*Optional — Extends supply voltage range

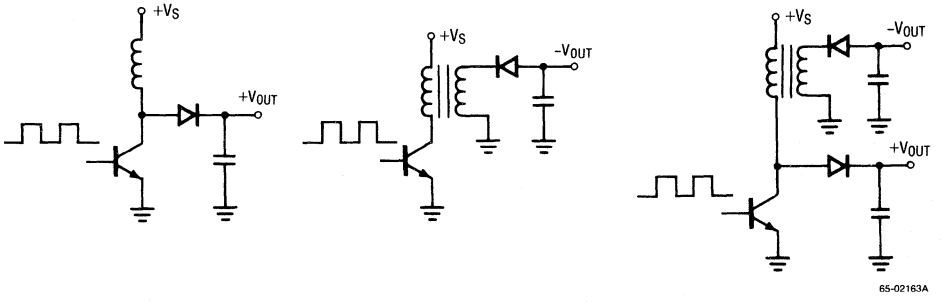
Figure 12. High Power Step-Down Supply



D1 = 1N914 or equivalent
D2 = Motorola MBR140P (power Schottky) or equivalent

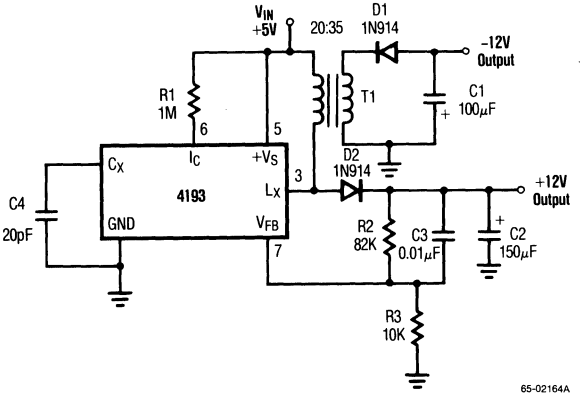
Figure 13. Low Voltage Start-Up (Bootstrapped Operation)

Transformer coupled 4193 circuits are necessarily single ended (as opposed to push-pull) because only one output transistor is included within the IC. This single ended output exaggerates one major disadvantage of transformer applications, the size of the core needed. Push-pull circuits utilize 100% of the flux capability of a given core, while single ended circuits utilize only 50%. Thus in single ended applications the core must be larger to meet the same output power requirement. So single ended transformer applications should be limited to lower load power applications (less than 10W). In this example a combination of step-up and transformer coupling is used in order to simplify the winding arrangement (only two windings needed). See Figure 14.



a) Simple Step-Up b) Simple Transformer c) Transformer Plus Step-Up

Figure 14. Circuit Topology



T1 = 14mm x 8mm power pot core with .012 inch air gap (use 28 gauge magnet wire)
NOTE: $+V_{OUT}$ must have a minimum load for proper operation (see Figure 16)

Figure 15. ±12V Transformer Coupled Power Supply

The power supply converts +5V TTL supply voltage into ±12V output voltages. Load and line regulation are traded away for simplicity and low cost; the negative output has no line regulation, and poor (but acceptable for many purposes) load regulation. In return this supply needs only a minimum of expensive components: a single 4193 and one inductor core constitute the majority of cost.

The positive output voltage exhibits the good regulation of other 4193 applications, because the feedback control is derived from the positive output, and changes in input voltage or load current are compensated for by adjusted duty cycle.

Line regulation at the negative output is 0dB; any change in input voltage is seen at the negative output. This is because of transformer coupling. The input/output relationship of a transformer is given by:

$$\frac{V_P}{V_S} = \frac{N_P}{N_S}$$

where: V_P = Primary DC Voltage
V_S = Secondary DC Voltage
N = Number of turns

In this case the DC voltage at the primary is the voltage applied when the switch transistor is off.

$$V_P = +V_{OUT} + V_D - V_{IN}$$

As the supply voltage V_{IN} is increased, V_S and, therefore, $-V_{OUT}$ will decrease in direct proportion. This means that a preregulated voltage supply, such as a +5V TTL supply, must be used (rather than a battery which will decay).

Load regulation at the negative output is a function of the current drawn from both outputs. Though obviously not a precision output, this negative voltage is good enough for many op amp type applications, and if necessary can be post regulated with a three terminal series voltage regulator. See Figure 16 for a graph of negative load regulation.

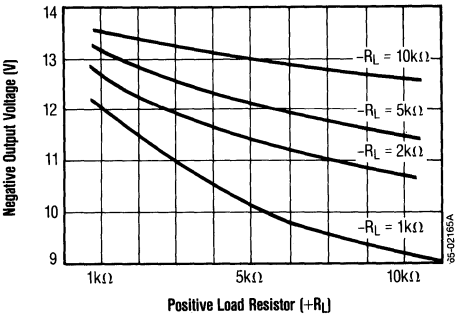


Figure 16. Negative Output Load Regulation

±12V Transformer Coupled Power Supply Specifications

Output Voltage ..... ±12 Volts
Input Voltage ..... +5 Volts
Output Current ..... ±12 Milliamps
Efficiency 60%
Ripple ..... $100mV_{p-p}$

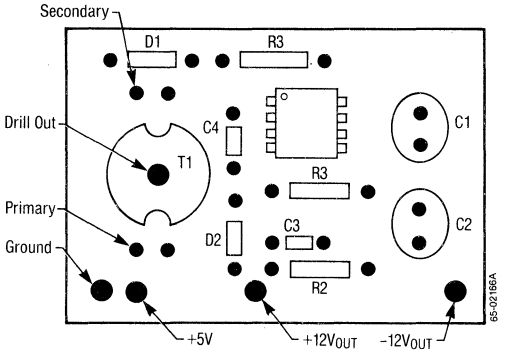


Figure 17. ±12V Power Supply Component Placement Diagram

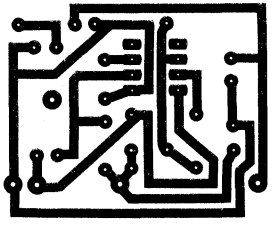


Figure 18. Transformer Coupled Supply 1X PC Board Layout (Component Side View)

Capacitor Coupled ±15V Power Supply

This application circuit is similar to the transformer coupled ±12V power supply in that it uses just a single 4193 IC and one inductor core, but in this case the negative output is created by a capacitor-diode inverting circuit tapping the L_X pin. So, the extra winding needed in the transformer coupled circuit is eliminated, and a simple off the shelf two terminal inductor is the only magnetic component required.

There is a tradeoff, however, resulting from using this capacitor coupled inverting circuit instead of an extra winding. Unbalanced output voltages result where the value of the negative output voltage is always a diode drop less than the positive. Therefore, a Raytheon 4195 series-pass dual tracking regulator IC is added after the 4193 in order to produce balanced outputs. Use of a linear series pass regulator reduces the efficiency greatly, so therefore the tradeoff for using the capacitor coupled circuitry is a loss of efficiency (reduced to about 35–40%). Because of this lowered efficiency battery applications are less suitable, but the circuits strong points (small size and low cost) make it useful for a range of on-card applications.

A side benefit from the 4195 linear regulator is reduced ripple and noise at the output. Also, both the positive and negative outputs are tightly regulated.

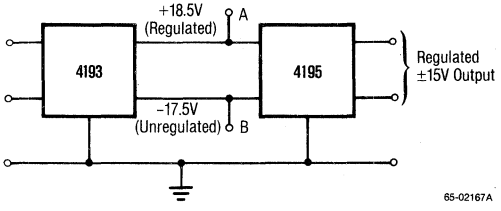
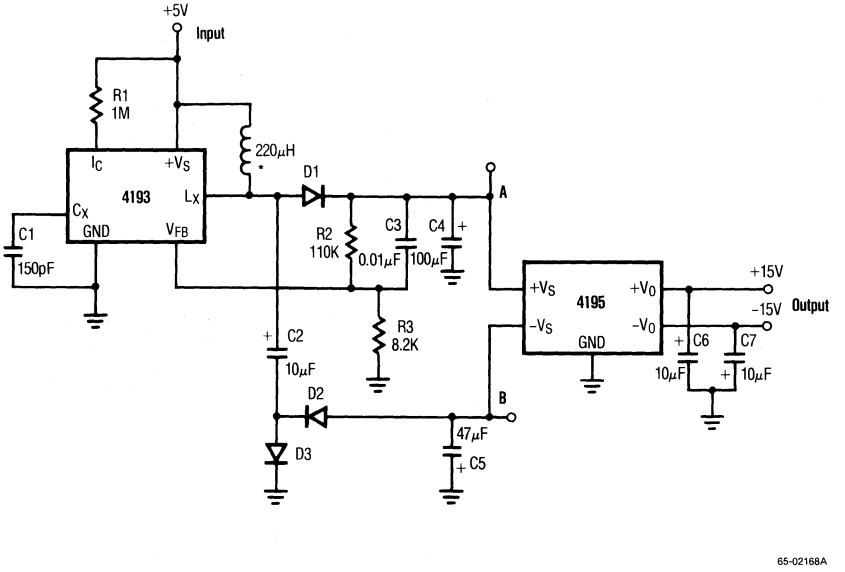


Figure 19. Capacitor Coupled Supply (Block Diagram)

Figure 20 shows a complete schematic of the capacitor coupled supply including the 4195 linear regulator.

The switching regulator portion of the circuit steps up and charges its positive output (Point A) normally through the flyback connection of D1. (NOTE: If the 4195 is removed point A can be used as a single +15V supply with an output current capability of 20mA at an efficiency of 60%.) The voltage at point A is regulated via a feedback signal set by R2 and R3 [V_A = (R2/R3 + 1) V_{REF}]. This +18.5V at point A is then stepped down to +15V by the 4195.

The negative voltage at point B is developed through the 10μF coupling capacitor and D2, D3. When the inductor is discharging into point A the L_X terminal rises to one diode drop above



* = 11mm x 7mm power pot core with 70 turns and .02 inch C.P. air gap
D1, 2, 3 = 1N914

Figure 20. ±15V Capacitor Coupled Supply

the voltage at point A. During this discharge time the coupling capacitor charges through D3, which is forward-biased. Then, when the next oscillator cycle starts the L_X terminal is forced nearly to ground by the internal power transistor, and the more positively charged side of the capacitor is held at close to ground potential. So D3 is then reverse-biased, D2 is forward-biased, and the capacitor discharges into point B. Thus point B is charged to a negative voltage (≅1V less than the magnitude of point A) with each oscillator cycle. This negative voltage is then stepped down to -15V by the 4195.

Specifications for ±15V Capacitor Coupled Power Supply

Output Voltage	+15V ±.5V
	-15V ±.5V
Output Current	±8mA
Input Voltage Range	+4.5V to +8.0V
Output Voltage Ripple	< $5mV_{pp}$
Load Regulation (no load to full load)	< 5mV
Operating Temperature Range	-35°C to +85°C

Application Notes

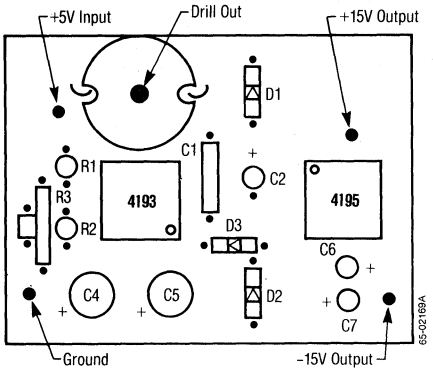


Figure 21. ±15V Power Supply 2X Component Placement Diagram (Component Side View)

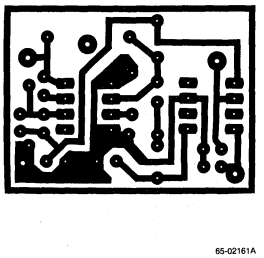
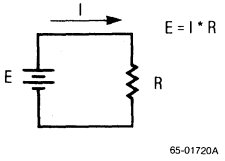


Figure 22. ±15V Power Supply 1X PC Card Layout (Component Side View)

Pot Core Inductor Design

Electrical Circuit



Magnetic Circuit

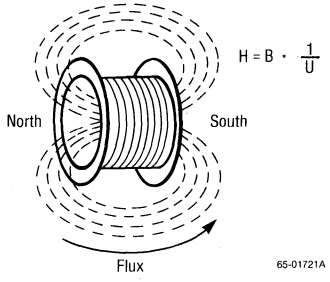


Figure 23. Electricity Versus Magnetism

Electricity Versus Magnetism

Electrically the inductor must meet just one requirement, but that requirement can be hard to satisfy. The inductor must exhibit the correct value of inductance (L, in Henrys) as the inductor current rises to its highest operating value (I_{MAX}). This requirement can be met most simply by choosing a very large core and winding it until it reaches the correct inductance value, but that brute force technique wastes size, weight and money. A more efficient design technique must be used.

Question: What happens if too small a core is used?

First, one must understand how the inductor's magnetic field works. The magnetic circuit in the inductor is very similar to a simple resistive electrical circuit (see Figure 23). There is a magnetizing force (H, in oersteds), a flow of magnetism, or flux density (B, in Gauss), and a resistance to the flux, called permeability (U, in Gauss per oersted). H is equivalent to voltage in the electrical model, flux density is like current flow, and permeability is like resistance (except for two important differences discussed below).

First Difference: Permeability, instead of being analogous to resistance, is actually more like conductance (1/R). As permeability increases, flux increases.

Second Difference: Resistance is a linear function. As voltage increases, current increases proportionally, and the resistance value stays the same. In a magnetic circuit the value of permeability varies as the applied magnetic force varies. This nonlinear characteristic is usually shown in graph form in ferrite core manufacturer's data sheets. See Figure 24.

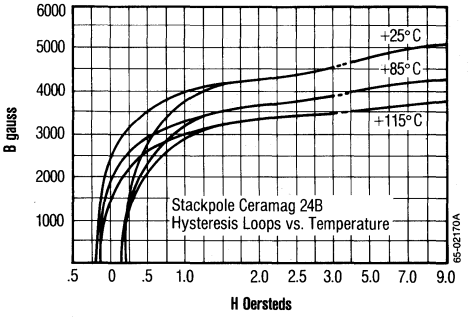


Figure 24. Typical Manufacturer's Curve Showing Saturation Effects

As the applied magnetizing force increases, at some point the permeability will start decreasing, and therefore the amount of magnetic flux will not increase any further, even as the magnetizing force increases. The physical reality is that, at the point where the permeability decreases, the magnetic field has realigned all of the magnetic domains in the core material. Once all of the domains have been aligned the core will then carry no more flux than just air; it becomes as if there were no core at all. This phenomenon is called saturation. Because the inductance value, L, is dependent on the amount of flux, core saturation will cause the value of L to decrease dramatically, in turn causing excessive and possibly destructive inductor current.

Pot Cores for 4193/4391

Pot core inductors are best suited for Raytheon's micropower switching regulators for several reasons:

1. **They are available in a wide range of sizes.** 4193/4391 applications are usually low power with relatively low peak currents (less than 500mA). A small inexpensive pot core can be chosen to meet the circuit requirements.
2. **Pot cores are easily mounted.** They can be bolted directly to the PC card adjacent to the regulator IC.
3. **Pot cores can be easily air-gapped.** The length of the gap is simply adjusted using different washer thicknesses. Cores are also available with predetermined air gaps.
4. **Electromagnetic interference is kept to a minimum.** The completely enclosed design of a pot core reduces stray electromagnetic radiation — an important consideration if the regulator circuit is built on a PC card with other circuitry.

Core Size

Question: Is core size selected according to load power?

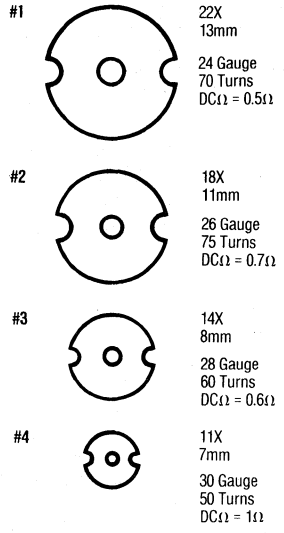
Not quite. Core size is dependent on the amount of energy stored, not on load power. Raising the operating frequency allows smaller cores and windings. Reduction of the size of the magnetics is the main reason switching regulator design tends toward higher operating frequency. Designs with the 4193/4391 should use 75kHz as a maximum running frequency, because the turn off delay of the power transistor and stray capacitive coupling begin to interfere. Most applications are in the 10 to 50kHz range, for efficiency and EMI reasons.

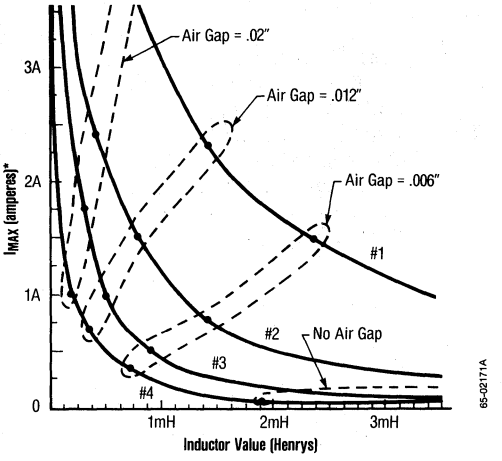
The peak inductor current (I_{MAX}) must reach a high enough value to meet the load current drain. If the operating frequency is increased, and simultaneously the inductor value is decreased, then the core can be made smaller. For a given core size and winding, an increase in air gap spacing (an air gap is a break in the material in the magnetic path, like a section broken off a doughnut) will cause the inductance to decrease and I_{MAX} (the usable peak current before saturation) to increase.

The curves shown in Figure 25 are typical of the ferrite manufacturer's power HF material, such as Siemens N27 or Stackpole 24B, which are usually offered in standard millimeter sizes including the sizes shown.

Use of the Design Aid Graph (Figure 25)

1. From the application requirement, determine the inductor value (L) and the required peak current (I_{MAX}).





*Includes safety margin (25%) to ensure nonsaturation.

Figure 25. Inductor Design Aid

2. Observe the curves of the design aid graph and determine the smallest core that meets both the L and I requirements.
3. Note the approximate air gap at I_{MAX} for the selected core, and order the core with the gap. (If the gapping is done by the user, remember that a washer spacer results in an air gap of twice the washer thickness, because two gaps will be created, one at the center post and one at the rim, like taking two bites from a doughnut.)
4. If the required inductance is equal to the indicated value on the graph, then wind the core with the number of turns shown in the table of sizes. The turns given are the maximum number for that gauge of wire that can be easily wound in the cores winding area.
5. If the required inductance is less than the value indicated on the graph, a simple calculation must be done to find the adjusted number of turns. Find A_L (inductance index) for a specific air gap.

$$\frac{L\ (\text{indicated})}{\text{Turns}^2} = A_L\ (\text{in Henrys/turn}^2)$$

Then divide the required inductance value by A_L to give the actual turns squared, and take the square root to find the actual turns needed.

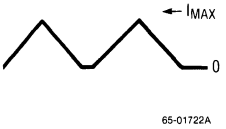
$$\text{Actual Turns} = \frac{L\ (\text{required})}{A_L}$$

If the actual number of turns is significantly less than the number from the table then the wire size can be increased to use up the left-over winding area and reduce resistive losses.

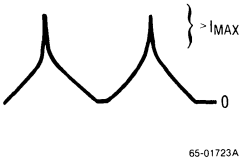
6. Wind and gap the core as per calculations, and measure the value with an inductance meter. Some adjustment of the number of turns may be necessary.

   The saturation characteristics may be checked with the inductor wired into the switching regulator application circuit. To do so, build and power up the circuit. Then clamp an oscilloscope current probe (recommend Tektronix P6042 or equivalent) around the inductor lead and monitor the current in the inductor. Draw the maximum load current from the application circuit so that the regulator is running at close to full duty cycle. Compare the waveform you see to those pictured in Figure 26.

   Check for saturation at the highest expected ambient temperature.



Proper Operation
(Waveform is Fairly Linear)



Improper Operation
(Waveform is Nonlinear, Inductor is Saturating)

Figure 26. Inductor Current Waveforms

7. After the operation in circuit has been checked, reassemble and pot the core using a potting compound recommended by the manufacturer.

If the core material differs greatly in magnetic characteristics from the standard power material shown in Figure 25, then the following general equation can be used to help in winding and gapping. This equation can be used for any core geometry, such as an E-E core.

$$L_X = \frac{(1.26)(N^2)(Ae)(10^{-8})}{g = (le/ue)}$$

Where: N = number of turns
Ae = core area from data sheet (in cm^2)
le = magnetic path length from data sheet (in cm)
ue = permeability of core from manufacturer's graph
g = center post air gap (in cm)

Manufacturers

Below is a list of several pot core manufacturers:

Ferroxcube Company
5083 Kings Highway
Saugerties, NY 12477

Indiana General Electronics
Keasley, NJ 08832

Siemens Company
186 Wood Avenue South
Iselin, NJ 08830

Stackpole Company
201 Stackpole Street
St. Mary, PA 15857

TDK Electronics
13-1, 1-Chome
Nihonbaski, Chuo-ku, Tokyo

Tohoku Metal Ind.
13-7, 6-Chome
Ginza, Chuo-ku, Tokyo

Design Examples

Design Example One: 25kHz 4391 Inverter

Application requirements:

$-V_{OUT}$ = 11.3V
$+V_S$ = 6V
I_{LOAD} = 50mA

Inductor Approximation (See Figure 27)

1. Find T_{ON}:

$$T_{ON} \cong \frac{1}{2fo} + 3\mu S = \frac{1}{(2)(25K)} + 3\mu S = 23\mu S$$

2. Find TI:

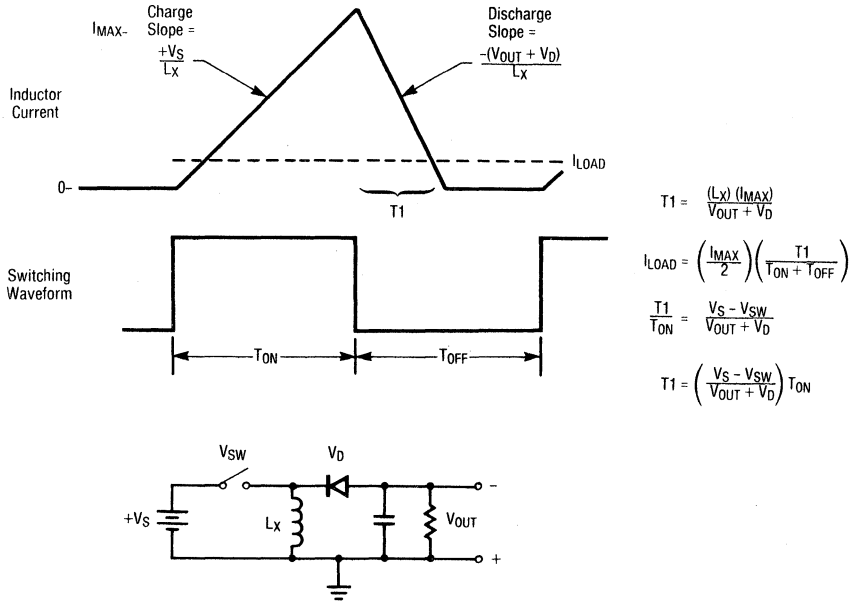
$$TI = \left(\frac{V_S}{V_{OUT} + Vd}\right) T_{ON} = \left(\frac{6V}{12V}\right) 23\mu S = 11.5\mu S$$

3. Find I_{MAX}:

$$I_{MAX} = \left(\frac{V_{OUT} + Vd}{I_{MAX}}\right) (2I_L) =$$

$$\left(\frac{40\mu S}{11.5\mu S}\right)(2)(50mA) = 348mA$$

Application Notes



$$T1 = \frac{(Lx)(I_{MAX})}{V_{OUT} + V_D}$$

$$I_{LOAD} = \left(\frac{I_{MAX}}{2}\right)\left(\frac{T1}{T_{ON} + T_{OFF}}\right)$$

$$\frac{T1}{T_{ON}} = \frac{V_S - V_{SW}}{V_{OUT} + V_D}$$

$$T1 = \left(\frac{V_S - V_{SW}}{V_{OUT} + V_D}\right) T_{ON}$$

Figure 27. 23kHz 4391 Inverting Design Example

4. Find Lx:

$$Lx = \left(\frac{V_{OUT} + Vd}{I_{MAX}}\right)(TI) = \left(\frac{12V}{348mA}\right)(11.5\mu S) = 396\mu H$$

5. Look up 400 μH and 350mA in Figure 25 — the point lies inside the #4 core area, so the smallest size core can be used. Estimate the air gap — at the 400μH 350mA point the air gap required is about .009". At .009" air gap, the inductance value is approximately 500μH with a full (50 turn) winding.

   So

$$A_L = \frac{L}{Turn^2} = \frac{500\mu H}{50^2} = .2\mu H/Turn^2$$

   The needed value of inductance is 400μH, so the actual number of turns =

$$\text{Turns (Actual)} = \sqrt{\frac{Lx}{A_L}} = \sqrt{\frac{400\mu H}{.2\mu H/N^2}}$$

   = 44.7 Turns

   Round up to the next highest number — use 45 turns.

Design Example Two: 10kHz Step-Up Regulator

Application requirements:

$+V_{OUT}$ = 15V
$+V_S$ = 5V
I_{LOAD} = 100mA

Inductor Approximation (See Figure 28)

1. Find T_{ON}:

$$T_{ON} \cong \frac{1}{2fo} + 5\mu S = \frac{1}{(2)(10K)} + 5\mu S = 55\mu S$$

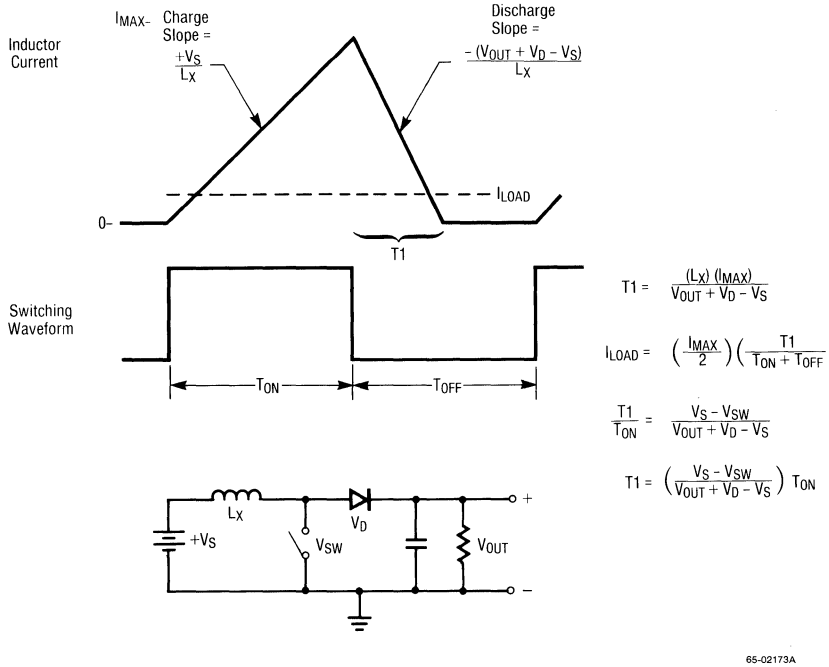
2. Find TI:

$$TI = \left(\frac{V_S}{V_{OUT} + Vd - V_S}\right)(T_{ON}) = \left(\frac{5V}{15.7V - 5V}\right)(55\mu S) = 26\mu S$$

3. Find I_{MAX}:

$$I_{MAX} = \left(\frac{T_{ON} + T_{OFF}}{TI}\right)(2I_L) =$$

$$\left(\frac{100\mu S}{26\mu S}\right)(2)(100mA) = 770mA$$



Idealized Schematic

Figure 28. 10kHz 4391 Step-Up Design Example

4. Find Lx:

$$Lx = \left(\frac{V_{OUT} + Vd - V_S}{I_{MAX}}\right)(TI) =$$

$$\left(\frac{10.7V}{770mA}\right)(26\mu S) = 360\mu H$$

5. Look up 360μH and 770mA in Figure 25 — the point lies between the #4 curve and the #3 curve, so the #3 core must be used. Estimate the air gap — by Figure 25 it is approximately .012". At .012", the inductance value with a full winding (60 turns) of 28 gauge wire is about 500μH.

   So

$$A_L = \frac{500\mu H}{60^2} = .138\mu H/N^2$$

   The needed value of inductance is 360μH, so

$$\text{Turns (Actual)} = \sqrt{\frac{Lx}{A_L}} = \sqrt{\frac{360\mu H}{.138\mu H/N^2}}$$

   = 51 Turns

   This leaves some extra winding space which could be filled by using the next larger wire size; in this case 26 gauge would work well.

Design Example Three: 20kHz Step-Down (4193)

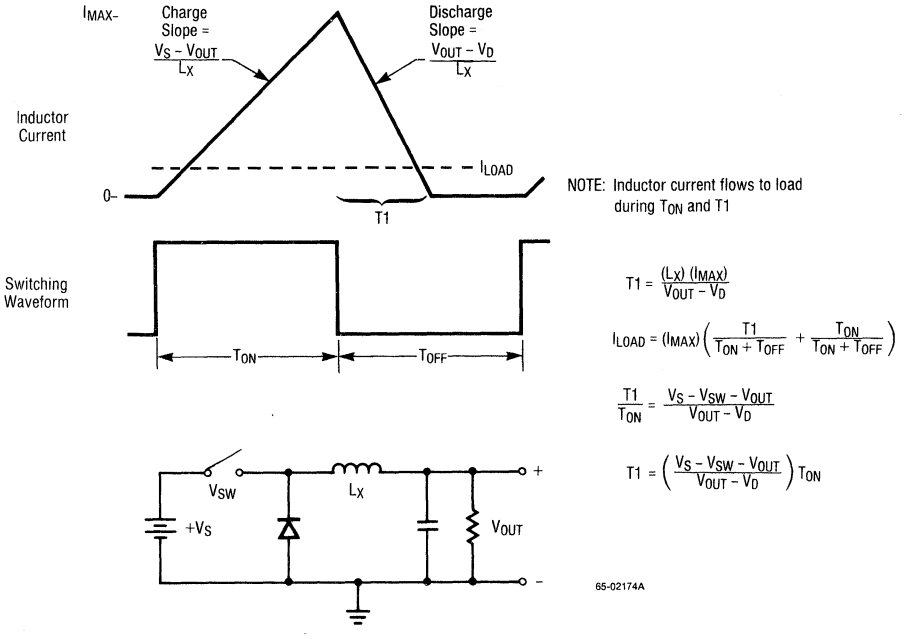
Application requirements:

$+V_{OUT}$ = 20V
$+V_S$ = 32V
I_{LOAD} = 200mA

Inductor Approximation (See Figure 29)

1. Find T_{ON}:

$$T_{ON} \cong \frac{1}{2fo} + 5\mu S \quad \frac{1}{(2)(20K)} + 5\mu S = 30\mu S$$



Idealized Schematic

Figure 29. 20kHz Step-Down Design Example

2. Find TI:

$$TI = \left(\frac{V_S - V_{OUT}}{V_{OUT} - Vd}\right)(T_{ON}) = \left(\frac{32V - 20V}{20V - .7V}\right) 30\mu S = 18.6\mu S$$

3. Find I_{MAX}:

$$I_{MAX} = \frac{2I_L}{fo(TI + T_{ON})} =$$

$$\frac{(2)(200mA)}{20K(18.6\mu S + 30\mu S)} = 389mA$$

4. Find Lx:

$$Lx = \left(\frac{V_{OUT} - Vd}{I_{MAX}}\right)(TI) =$$

$$\left(\frac{19.3V}{389mA}\right)(18.6\mu S) = 923\mu H$$

5. Look up 923μH and 389mA in Figure 25 — the point lies between #3 and #4 cores so the #3 core must be used. Estimate the air gap — by Figure 25 it is approximately .005". At .005", the inductance value with a full winding (60 turns) is about 1,000μH.

So

$$A_L = \frac{1{,}000\mu H}{60^2} = .277\mu H/Turn^2$$

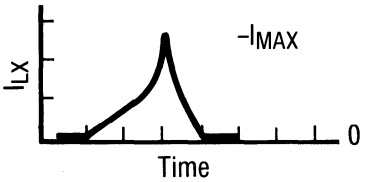
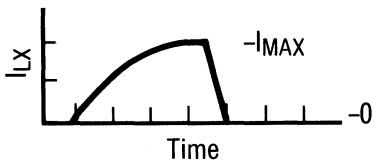
The needed value of inductance is 923μH, so

$$\text{Turns (Actual)} = \sqrt{\frac{Lx}{A_L}} = \sqrt{\frac{923\mu H}{.277\mu H/N^2}}$$

= 57.6 Turns

Use 58 turns.

Appendix: Troubleshooting Chart

Symptom	Possible Problems
Draws excessive supply current on start-up.	Battery not "stiff" — inadequate supply bypass capacitor. Inductance value too low. Operating frequency too low. Hard start condition — see "soft start".
Output voltage is low.	Inductance value too high for Fop or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
Lx pin appears noisy — scope will not synchronize.	Normal operating condition.
 Inductor current shows nonlinear waveform.	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
 Inductor current shows nonlinear waveform.	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
Poor efficiency.	Core saturating. Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high SAT). High series resistance. Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback capacitor.

Section 8
Glossary

Ambient Temperature (T_A)
Standard temperature range devices have their temperature range specified in terms of the ambient temperature (still air) surrounding the converter.

Analog Ground Voltage (V_{AGND})
Potential of the analog ground terminal with respect to the digital ground terminal.

Analog Input Impedance (R_{IN})
Although the input impedance of a flash A/D converter is largely capacitive, it does have a resistive component which is approximated with R_{IN}, the input resistance. R_{IN} varies with the input voltage.

Aperture Error (E_{AP})
Because there is an aperture of non-zero duration during which the A/D looks at a signal before conversion, there are errors introduced in the conversion. These errors are the effect of: aperture time (the amount of time during which the input signal is considered before conversion), aperture time uncertainty (the variation in aperture time) and aperture jitter which is the uncertainty in the starting instant of the aperture time. All of these effects are combined in a single parameter, Aperture Error (E_{AP}). Aperture Errors cause a degradation of the SNR of the A/D converter with higher analog input frequencies and are estimated based upon this SNR degradation.

Average Input Bias Current Drift (TC_{IB})
The ratio of change in input bias current to a change in ambient temperature, expressed in nanoamps per °C (nA/°C).

$$TC_{IB} = \frac{I_B @ T_{(1)} - I_B @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Average Input Offset Current Drift (TC_{IOS})
The ratio of change in input offset voltage to a change in ambient temperature, expressed in microvolts per degree C (µV/°C).

$$TC_{IOS} = \frac{I_{OS} @ T_{(1)} - I_{OS} @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Average Input Offset Voltage Drift (TC_{VOS})
The ratio of change in input offset voltage to a change in ambient temperature, expressed in microvolts per degree C (µV/°C).

$$TC_{VOS} = \frac{V_{OS} @ T_{(1)} - V_{OS} @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Bandwidth, reference (BWR)
BWR specifies the maximum frequency at which the reference (V_{REF}) may be exercised. It is a small signal parameter since in most cases the reference is only varied by a small portion of its full-scale value. Exceeding the BWR specification may result in the same types of coding errors encountered when the BW specification is violated.

Case Temperature (T_C)
For extended temperature range devices, the temperature range is specified in terms of the case temperature.

Channel Separation (CS)
The ratio of output voltage of an amplifier to the output voltage of an adjacent amplifier whose gain is 100, and whose inputs are grounded, expressed in decibels (dB). Channel separation is measured at the outputs of adjacent amplifiers:

$$\text{Channel Separation} = 20LOG_{10}\left(\frac{100V_{O(1)}}{V_{O(2)}}\right)$$

Where $V_{O(1)}$ and $V_{O(2)}$ are the independent and dependent amplifier output voltages.

Code Size (Q, CS)
Code size is the size of the individual codes, from code transition to code transition. It is often expressed as a percentage of the ideal code size. The ideal code size is given by:

$$\frac{\text{Input Voltage Range}}{2^N}$$

Where N is the number of bits of resolution of the A/D converter.

Q is also defined as the total number of quantizing levels or codes output by a converter (2^N).

Common Mode Rejection Ratio (CMRR)
The ratio of change of input common mode voltage (both inputs swing together over a specified voltage range) to a change in input offset voltage, expressed in decibels (dB).

$$CMRR = 20LOG_{10}\left(\frac{V_{IN(1)} - V_{IN(2)}}{V_{OS} @ V_{IN(1)} - V_{OS} @ - V_{IN(2)}}\right)$$

Where $V_{IN(1)}$ and $V_{IN(2)}$ are the upper and lower limits of the input common mode voltage range.

Compliance
The measure of the output impedance of a switch current source, given as a maximum current for a specified voltage change, in microamps (μA).

Differential Gain (DG)
Differential gain is defined as "The difference between (1) the ratio of the output amplitudes of a small high-frequency sine wave signal at two stated levels of a low frequency signal on which it is superimposed and (2) unity" **[1]**. Distortion-free processing of a color television signal demands that the amplitude of the chrominance signal not be affected by the luminance function. This is a relevant specification for the video industry since the saturation of the color being shown is represented by the amplitude of a small signal superimposed upon another signal which determines the brightness of the color. The standard method for measuring the differential gain of a device is by using a standardized test signal, known as a modulated ramp (refer to Figure 2). The output of the A/D is then reconstructed by a reference D/A and low pass filter; the resultant signal is displayed on a vectorscope which is defined in reference **[2]**. During DG measurements the vectorscope display will be fuzzy due to quantizing errors in the A/D and D/A. The measurement requires interpretation of the peak-to-peak curvature of the center of the waveform. There are theoretical bounds on differential gain performance described in **[3]**. The number specified on an A/D converter data sheet is the difference between the actual differential gain of the device and the theoretical performance. Figure 3 shows the typical test set-up that might be used in Differential Gain testing, which is described in more detail in reference **[2]**.

Differential Nonlinearity (DNL)
The incremental error from an ideal 1 LSB analog output change when the input is changed 1 LSB; guaranteed monotonicity requires the differential nonlinearity error to be less than 1 LSB. Differential nonlinearity is expressed as a percentage of the full scale output.

Differential Phase (DP)
Differential Phase is defined a "the difference in output phase of a small, high-frequency, sine wave signal at the two state levels of a low frequency signal on which it is superimposed" **[1]**. Distortion-free processing of a color television signal demands that the phase of the chrominance signal not be affected by the luminance function.

Differential phase errors appear on the T.V. screen as changes in the hue of the colors (tint) as the brightness changes. Differential phase testing is very similar to differential gain testing. The equipment shown in Figure 3 is identical for both tests. The results are analyzed in the same manner as Differential Gain. Reference **[2]** also includes differential phase testing of A/D converters.

Digital Input Capacitance (C_I)
The amount of capacitive loading present at a digital input. Digital input capacitance is measured with a capacitance bridge, applying a 1 MHz signal to the input.

Distortion (THD)
The large signal harmonic distortion between input and output under closed loop conditions, expressed in percent at a specified frequency.

Full Power Bandwidth (BW)
Bandwidth specified for a Flash Analog-to-Digital (A/D) converter is different from the bandwidth specification given for a purely analog device. Before attenuation becomes a significant factor in the performance of the converter, other problems may arise, leading to degraded performance. Spurious and missing codes might be encountered when the analog input frequency exceeds the bandwidth specification. Bandwidth for an A/D converter is the maximum frequency full-scale input sinewave that can be accurately quantized by the A/D converter without spurious or missing codes. A spurious

code is a code which is grossly inaccurate, such as when the input signal is near mid-scale and an output code which is a full-scale output is generated. When the signal is reconstructed with a D/A converter, this spurious code looks like a glitch, and is therefore sometimes referred to as a glitch. Bandwidth is measured with worst case power supply conditions and sampling at the maximum sampling rate. (F_S).

The test used to determine the bandwidth of an A/D converter is the "Beat Frequency Test." The principle behind this test is to use "aliasing" to convert a high-frequency input signal to a low-frequency output signal which is easier to analyze. This is done by providing the A/D converter with a high-frequency sine wave input, and then sampling the input at a rate offset by a small delta in frequency from an integral (N) multiple of the input frequency. A D/A converter is given every Nth A/D output; this produces an output signal of the A/D which is an aliased version of the input. In a typical set-up, the analog reconstruction (D/A output) is examined on an oscilloscope for spurious and missing codes. Figure 1 shows a typical test set-up. A spurious code is defined as a non-continuous change in the output of the A/D which is not affected in the input signal.

Full Scale Current (I_{FS})
The maximum current that can be obtained from the output, for a specified reference current, measured in milliamps (mA). A typical binary D/A produces its full scale output with all ones applied at the input.

Full Scale Frequency
A voltage-to-frequency converter can operate up to the guaranteed full scale frequency without violating any of the performance specs for this frequency range. Full scale frequency is expressed in Hertz (Hz).

Full Scale Symmetry
The difference between the full scale output values of the two outputs of a complementary output D/A, expressed in microamps (μA).

Gain Bandwidth Product (GBW)
The frequency at which the open loop gain equals unity, expressed in Hertz (Hz).

Gain Temperature Coefficient
The variation of full scale current measured over a specified temperature range, expressed in parts per million per degree C (ppm/°C).

$$\text{Gain TC} = \left(\frac{I_{FS} @ T_{(1)} - I_{FS} @ T_{(2)}}{T_{(1)} - T_{(2)}}\right)\left(\frac{10^6}{I_{FS}}\right)$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Integral Linearity Error (E_{LI})
Integral linearity is a measure of how the ideal and actual transfer functions of the A/D compare. The integral linearity error is the maximum difference between the actual and ideal quantization levels (the midpoint between adjacent threshold levels).

There are several methods for measuring integral linearity. A typical A/D transfer function showing different types of linearity errors is shown in Figure 6. Zero-based linearity is used mainly in bipolar systems with adjustments that allow the user to null any errors at the origin (the center of the transfer function). To measure zero-based integral linearity, a "straight line of best fit" is drawn through the origin. Then the maximum deviation of the actual transfer function from this line is determined. Terminal-based linearity measurements are similar to the zero-based; however, the line is drawn between the two end points of the transfer function. The same difference signal is generated, and the same method is used for interpreting the results. The other method for measuring independent integral linearity involves drawing the "straight line of best fit" through the transfer function, independent of the mid or end points, then calculating the error. A common method for measuring integral linearity is the subtractive ramp test. A low-frequency ramp is digitized by the A/D converter, then the signal is reconstructed with a D/A converter. The reconstructed signal is now subtracted from the original ramp with a differential amplifier and the difference (error signal) is displayed on an oscilloscope. The sawtooth wave displayed on the oscilloscope can be examined for integral non-linearities. Figure 7 shows the test set-up for the subtractive ramp test.

Input Bias Current (I_B)
The average of the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Current, Constant Bias[1] (I_{CB})
The current drawn by the input of the A/D converter is dependent upon frequency and voltage level of the analog input. The current is sometimes also dependent upon the phase of the convert signal. This dependence is explained under I_{SB}, synchronous bias current; however, neglecting all of these second order effects, the current drawn by the input of the A/D is I_{CB}. This can be thought of as the sum of the converter input bias currents which is dependent upon the input voltage level.

Input Current, Logic High[1] (I_{IH})
I_{IH} is the current drawn by a digital input to the device when the potential of the terminal is in the logic low state.

Input Current, Logic Low[1] (I_{IL})
I_{IL} is the current drawn by a digital input to the device when the potential of the terminal is in the logic low state.

Input Current, Synchronous Bias[1] (I_{SB})
In some flash converters, the current flowing into the analog input varies slightly depending upon the state of the CONV input varies slightly depending upon the state of the CONV signal. If the comparators are in the track mode (CONV low), then the input current is greater, and the amount of this current change is I_{SB}, synchronous bias current.

Input Equivalent Capacitance (C_{IN})
C_{IN} is an approximation of the largely capacitive input impedance of a flash A/D converter. The input capacitance is slightly dependent upon the DC level of the analog input voltage and the input frequency. The input equivalent capacitance must be taken into account when designing a buffer to drive a flash A/D.

The method used to test input capacitance involves sending a high-frequency signal through a transmission line to the analog input, and determining the input impedance by analysis of the reflected wave. This type of test is performed by an R.F. impedance analyzer.

Input Noise Current (I_{Np-p})
The peak-to-peak noise current within a specified frequency band, expressed in nanoamps or picoamps (nA or pA).

Input Noise Current Density (I_N)
The RMS noise current in a 1 Hertz band centered on a specified frequency, expressed in picoamps per root Hertz (pA/√Hz).

Input Noise Voltage (e_{np-p})
The peak-to-peak noise voltage within a specified frequency band, expressed in nanovolts or microvolts (nV or μV).

Input Noise Voltage Density (e_n)
The RMS noise voltage in a 1 Hertz band centered on a specified frequency, expressed in nanovolts per root Hertz (nV/√Hz).

Input Offset Current (I_{OS})
The difference between the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Offset Voltage (V_{OS})
The voltage that must be applied between the two inputs to obtain an output voltage in the center of the output swing range, expressed in millivolts or microvolts (mV or μV).

Input Resistance (Common Mode)
The ratio of input voltage change to the resulting change in input bias current, expressed in megaohms or gigaohms (MΩ or GΩ).

$$\text{Common Mode } R_{IN} = \frac{V_{(1)} - V_{(2)}}{I_B @ V_{(1)} - I_B @ V_{(2)}}$$

Where $V_{(1)}$ and $V_{(2)}$ are the upper and lower limits of the input voltage range.

Input Resistance (Differential Mode)
The ratio of small signal change in input offset voltage to a change in input current at either input terminal with the other grounded, expressed in megaohms (MΩ).

Input Voltage Range
The range of voltages at the inputs over which an amplifier or comparator operates within its common mode rejection ratio specification, expressed in volts (V).

Large Signal Voltage Gain (A_{VOL})
The ratio of a specified output voltage change to the change in input offset voltage required to effect the change under open loop conditions, expressed in volts per millivolt (V/mV) or decibels (dB).

$$AVOL = \left(\frac{V_{OUT(1)} - V_{OUT(2)}}{V_{OS(1)} - V_{OS(2)}} \right)$$

Where $V_{OUT(1)}$ and $V_{OUT(2)}$ are the specified upper and lower voltage limits for the change at the output.

Leakage Current (I_{LEAK})
The current that flows into the open collector output transistor when the logic output transistor is in the "off" state, as a result of the application of the maximum supply voltage to the output. Leakage current is measured in microamps (μA).

Least Significant Bit (LSB)
The digital input line which has the smallest effect on the analog output. LSB can also refer to the measure of the

analog output change when the input code is incremented; in that case, the ideal value of 1 LSB is calculated as:

$$1LSB = \left(\frac{1}{2^N}\right) \text{(Full Scale Range) in V or MA}$$

where N is the resolution of the converter.

Line Regulation
The ratio of change in output voltage to the change in supply (line) voltage affecting it, expressed as a percentage of the output voltage per volt change in supply voltage (%/V).

Linearity Error, Differential (E_{LD})
Differential non-linearity is a measure of the uniformity of the code midpoint spacing. Differential linearity is defined as the maximum of the difference between adjacent code midpoints and the width of one Least Significant Bit (LSBs). If there is a missing code, the center of that code is considered to be the transition which skips that code. A differential non-linearity calculation is shown if Figure 4. Another method that can be used to determine differential non-linearity is a subtractive ramp test which examines the difference between adjacent quantization levels (see E_{LI}). This method is shown in Figure 5. Differential non-linearity is sometimes measured with a statistical (histogram) test. In the histogram test the A/D converter is provided a full-scale sinusoidal analog input, and a large number of output samples is collected. The probability of obtaining each code is then calculated and the ratio of the actual number of samples at that code to the total number of samples represents the differential linearity error. An increase in code width results in a corresponding increase in the number of occurrences of that particular code.

Load Regulation
The ratio of change in output voltage to the change in load (output) current affecting it, measured in percent of output voltage per milliamp change in load current (%/mA).

Logic Input Current
The input current into the logic switch at specified applied voltage, expressed in microamps (μA).

Logic Input Levels
The range of voltages within which the logic trip level is guaranteed, expressed in volts (V).

Long Term Input Offset Voltage Stability
The averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation expressed in microvolts per month (μV/Mo).

Maximum Sampling Rate (F_S)
F_S is a sampling rate (samples per second) at which the converter is guaranteed to operate. Most flash A/D converter will operate reliably at any rate up to the maximum sampling rate, which is measured with worst case supply, worst case duty cycle conditions, and maximum full-power input frequency.

Monotonicity
For any one LSB increase in input code the D/A output either increases or remains constant.

Noise Power Ratio (NPR)
"NPR is the decibel ratio of the noise level in a measuring channel with the baseband fully noise loaded...to...the level in that channel with all of the baseband noise loaded except the measuring channel" [4]. To test NPR, the input of the A/D converter is presented with white noise having a frequency spectrum from low frequencies up to 1/2 the sampling rate. The power of the input noise is adjusted so that the converter is fully loaded, but not clipping excessively. The output of the A/D converter is then converted back into an analog signal with a D/A. The D/A output is passed through a very narrow band pass filter, and the output power of the signal is measured. The process is now repeated, but with a notch filter at the input of the A/D converter. The ratio of the two measured powers is the Noise Power Ratio, and is often expressed in dB:

$$NPR = 10 \log_{10} \text{(ratio)}$$

NPR is often used to determine how much noise will "bleed" into one channel from other channels in a broadband, frequency domain multiplexed system.

Nonlinearity
The difference between the actual analog output and an imaginary straight line drawn between the measured zero scale and full scale readings, for any code combination. Nonlinearity is expressed as a percentage of the full scale output.

Nonlinearity Error (N_L)
On a plot of input voltage versus output frequency, a straight line is drawn from the origin to the full scale point which is defined by the intersection of the maximum input voltage and maximum output frequency.

The actual plot of input versus output frequency should not deviate from this straight line by more than increment $\Delta F_{O(MAX)}$. Nonlinearity is defined here as $(\Delta F_O/\Delta F_S)$ x 100% where F_S is the maximum frequency for the range in question. For instance, when specifying nonlinearity

error for the 0.1 Hz to 10 kHz range, then F_S = 10 kHz. When specifying nonlinearity error for a frequency-to-voltage converter, nonlinearity error is defined as ($\Delta V/V_{FS}$) x 100%.

Offset Adjustment Range
The change in V_{OS} that can be produced using the specified external offset adjustment circuit, expressed in millivolts (mV).

Offset Errors, Sense Connected E_{OBS}, E_{OTS}
To minimize the effect of offset errors, some A/D converters have sense outputs. These allow the use of a sense pin, which carries minimal current to close a feedback path around the reference input, resulting in lower offset errors. Figure 9 shows a block diagram for an A/D converter which has sense connections. Figure 10 shows how a feedback path is closed around an operational amplifier to make use of the offset sense point. E_{OBS} and E_{OTS} are the residual offset errors when the sense leads are used.

Offset Voltage Bottom, Offset Voltage Top (E_{OB}, E_{OT})
Figure 8 shows the block diagram for a typical 6-bit flash A/D converter. There is a parasitic (R_P) resistance between the R_T lead and the first resistor. The voltage drop across this resistor is an offset voltage between the first code quantization level and the voltage applied to R_T. This offset is referred to as E_{OT}. The similar offset voltage at the bottom of the resistor chain is E_{OB}. E_{OT} and E_{OB} are measured by applying a known voltage to R_T and R_B and measuring the difference between these voltages and the voltages of the first and last code transitions of the A/D converter. In an ideal A/D, the first transition occurs at a point 1/2 LSB more negative than the top of the range. Therefore, if the input voltage to the device is set 1/2 LSB closer to R_B than zero, and V_{RT} is adjusted to get toggling between codes 0 and 1, then the voltage on R_T will be E_{OT}.

Open Loop Output Resistance (R_{OUT})
The resistance seen looking into the output with the output at the center of its swing, under small signal conditions, expressed in ohms (Ω)

Output Capacitance
The value of the internal parasitic capacitances, modelled as a single capacitor from the output to ground, expressed in picofarads (pF).

Output Current, Logic High[1] (I_{OH})
I_{OH} is the minimum current that is available (this is a negative value, there current flow is out of the device) to force an output terminal to the high state, while potential at the terminal is at the V_{OH} minimum specification.

Output Current, Logic Low[1] (I_{OL})
I_{OL} is the minimum current that is available to force output terminal to the low state, while the potential at the terminal is at the V_{OL} maximum specification.

Output Delay (t_D)
t_D is the time between the rising edge of the CONV signal and the time at which the output data from the A/D is guaranteed to be stable. On many TTL flash A/D converters, this delay can be reduced by the addition of pullup resistors from the data outputs of the device to the V_{CC} supply. This output delay is measured with the test load specified in the corresponding data sheet.

Output High Voltage (V_{OH})
The potential at an output terminal in the high state with respect to digital ground, when loaded with the test load defined in the data sheet. V_{OH} is measured with V_{CC} at a minimum.

Output Hold Time (tHO)
The time from the rising edge of the convert signal to the time when the output data lines begin to change.

Output Short Circuit Current[1] (I_{OS})
The current flowing from an output when the output is short circuited to ground while in the logic high state. This specification is indicated only on TTL compatible devices.

Output Leakage Current (I_{LEAK})
For open collector output types; the collector to emitter leakage current of the output transistor with the output in an off condition and a specified voltage applied, expressed in microamps (µA).

Output Low Voltage (V_{OL})
The potential at an output terminal in the low state with respect to digital ground, when loaded with the test load defined in the data sheet. V_{OL} is measured with V_{CC} set to the maximum value.

Output Sink Current (I_{SINK})
The current flowing into the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Source Current (I_{SOURCE})
The current flowing out of the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Voltage Compliance
The range of voltages over which the output can be driven while maintaining nonlinearity specifications, measured in volts (V).

Output Voltage Noise
Output voltage noise is the broadband noise over a specified range of frequencies, measured in microvolts peak-to-peak (μVp-p).

Output Voltage Swing (V_{OUT})
The peak output change, referred to ground, that can be obtained for a specified load resistance, expressed in volts (V).

Overshoot (OS)
The positive or negative going excursion that exceeds the final settled condition at the output of a closed loop unity gain amplifier, expressed as a percentage of the output step.

Phase Margin (PM)
The difference between the amplifier phase shift and 180° at the frequency where the open loop gain equals unity, expressed in degrees.

Phase Margin = 180° -ø

Where ø equals the input-output phase shift at $A_V = 1$.

Power Bandwidth
The maximum frequency at which a specified peak voltage sine wave may be obtained, measured in Hertz (Hz).

Power Supply Rejection Ratio (PSRR)
The ratio of change of supply voltage to a change in input offset voltage, expressed in decibels (dB).

$$PSRR = 20LOG_{10}\left(\frac{V_{S(1)} - V_{S(2)}}{V_{OS} @ V_{S(1)} - V_{OS} @ V_{S(2)}}\right)$$

Where $V_{S(1)}$ and $V_{S(2)}$ are the upper and lower limits of the specified change of supply voltage.

Power Supply Sensitivity
The ratio of change in the full scale output to a change in supply voltage, measured in percent of full scale per percent change in supply voltage (%ΔFS/%ΔV).

Propagation Delay
The time delay between a step input to all inputs and a change in the output, from the 5% point of TTL input swing to the 50% point of the final output value. Propagation delay is expressed in nanoseconds (ns).

Pulse Width High (t_{PWH})
t_{PWH} minimum is the minimum width high CONV pulse with which the A/D will accurately operate if all other specifications are met. t_{PWH} is measured from the 1.3 Volt level of the rising edge of the CONV signal to the 1.3 Volt level of the falling edge of the CONV signal on TTL compatible devices. If the CONV signal has a low portion of t_{PWH}, and a high portion of t_{PWH}, the device may be exceeding F_S in which case it may not operate properly.

Pulse Width Low (t_{PWL})
t_{PWL} is the low CONV pulse width with which the A/D will accurately operate if all other specs are met. t_{PWL} is measured from the 1.3 Volt level of the falling edge of the CONV signal to the 1.3 Volt level of the rising edge of the CONV signal on TTL compatible devices.

Reference Bias Current
The input current to the reference amplifier which subtracts from the reference current, expressed in microamps (μA).

Reference Bottom Voltage (V_{RB})
The potential of the R_B terminal with respect to analog ground.

Reference Current (I_{REF})
The current flowing through the reference resistor chain (in through R_T).

Reference Input Slew Rate
The average rate of change of the output current for a step change at the reference input, expressed in milliamps per microsecond (mA/μs).

Reference Middle Voltage (V_{RM})
The potential of the R_M terminal with respect to analog ground.

Reference Top Voltage (V_{RT})
The potential of the R_T terminal with respect to analog ground.

Reference Resistance (R_{REF})
R_{REF} is the total resistance of the entire reference resistor chain, including parasitics. It can be measured directly between R_T and R_B. Another method of testing R_{REF} is to calculate it from I_{REF} and (V_{RT} - V_{RB}).

Resolution
The number of inputs or bits. The number of discrete steps or states at the output is equal to 2^N, where N is the resolution of the converter.

Rise Time
The time required for an output voltage step to change from 10% to 90% of its final value, expressed in nanoseconds (ns).

Sampling Time Offset (t_{STO})
Sampling time offset is the time interval between the rising edge of the CONV signal and the actual instant at which the A/D samples the input signal.

Scale Factor (K)
Scale factor K is the ratio of F_O/V_{IN}.

Settling Time
The time delay between a 50% of TTL level change at all logic inputs to the point where the output settles within a specified error band of its final value, for either full scale to zero scale or zero scale to full scale changes. Settling time is measured in nanoseconds or microseconds (ns or µs).

Short Circuit Current (I_{SC})
The maximum output current available from a device with the output shorted to ground, expressed in milliamps (mA).

Signal-to-Noise Ratio (SNR)
The signal-to-noise ratio is the ratio of the value of the signal to that of the noise. The values of the signal and of the noise are usually expressed as RMS, but for some signals such as video, it is defined as peak-to-peak signal vs. RMS noise, because it is difficult to determine the RMS value of a video signal, and the meaning of peak-to-peak noise is not a useful parameter. The signal-to-noise ratio of an A/D converter provides a good figure of merit for the dynamic accuracy of the device. To test SNR, the A/D converter is given a high purity sine wave input. This is sampled at a non-harmonic sampling rate and the output of the A/D converter is stored in memory. The data from the A/D are then transformed into the frequency domain with a Fast Fourier Transform (FFT) and analyzed to determine the SNR. When analyzing the data, most of the "noise" will be located at the harmonic frequencies; therefore the SNR is a good estimate of total harmonic distortion. The analysis method takes the RMS or peak-to-peak voltage of the signal, and divides it by the RMS value of the noise. SNR is usually expressed in dB with the formula below:

$$SNR_{RMS} = 20 \log_{10} \frac{Signal_{RMS}}{Noise_{RMS}}$$

$$SNR_{Peak\text{-}RMS} = 20 \log_{10} \frac{Signal_{RMS}}{Noise_{RMS}} + 9.0$$

Sink Current (I_{SINK})
The amount of current that can be forced into the output with the reference still within ±3% regulation, expressed in milliamps (mA).

Supply Current[1] (I_{CC})
I_{CC} is the current drawn by the device from the V_{CC} supply. I_{CC} is a positive valued parameter. I_{CC} decreases with increasing temperatures in most A/D converters and is measured with V_{CC} at the maximum rated value.

Supply Current[1] (I_{EE})
I_{EE} is the current drawn by the device from the V_{EE} supply. Since I_{EE} is referenced to a negative supply, it is a negative valued parameter (current flows out of the device). In Raytheon Semiconductor's bipolar converters, I_{EE} decreases with increasing temperature and is measured with the maximum (most negative) rated V_{EE}.

Supply Current (I_{SY})
The current required from the power supply to operate a device under quiescent no-load conditions, expressed in milliamps (mA).

Supply Voltage (V_S)
The range of power supply voltages over which a device will operate, expressed in volts (V).

Supply Voltage (V_{EEA}, V_{EED}, V_{EE})
V_{EE} is the negative supply voltage. On converters with both digital and analog negative supplies, the analog supply is denoted V_{EEA}, and the digital supply is V_{EEA}.

Temperature Coefficient (T_C)
The change in the output voltage over specified temperature range in parts per million per °C (ppm/°C).

Temperature Coefficient (T_{CO})
T_{CO} is the factor which linearly approximates the variation with temperature of offset errors (E_{OT}, E_{OB}). This is a first order approximation and the actual temperature coefficient is a function of temperature which may exceed the maximum of T_{CO} in some temperature ranges.

Transient Response (t_{TR})
t_{TR} is the amount of time required for the converter to recover from a full-scale input transition, before valid data can be produced. The comparators in a flash A/D converter have a finite slew rate and a finite settling time. If a device is presented with a full-scale input change

(which exceeds that slew rate), it takes t_{TR} for the input circuit to recover and provide accurate data.

Unity Closed Loop Bandwidth (BW)
The frequency at which the small signal voltage gain is 3 dB below unity when operated as a closed loop unity gain follower, expressed in Hertz (Hz).

Zero Scale Current
The leakage current flowing into the D/A converter output with all logic inputs off and the output at a specified voltage range, expressed in microamps (μA).

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[1] *IEEE Standard Dictionary of Electrical and Electronic Terms*, IEEE Std 100-1977, p. 177.

[2] *IEEE Standard Definitions of Terms Relating to Television*, IEEE Std 201-1979.

[3] F.A. Williams and R.K. Olsen, "Quantization Effects on Differential Phase and Gain Measurements," *SMTE Journal*, November 1982.

[4] *The White Noise Book*, M.J. Kent.

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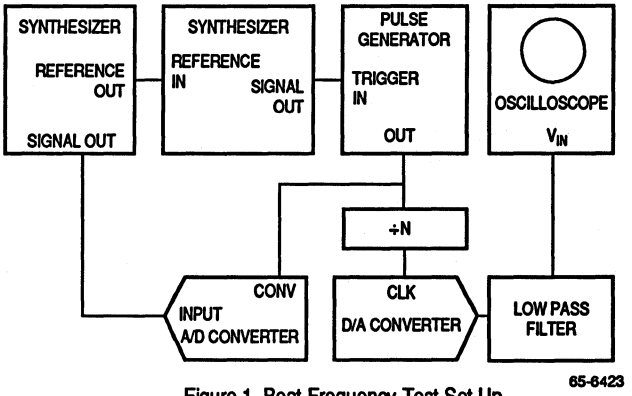


Figure 1. Beat Frequency Test Set Up

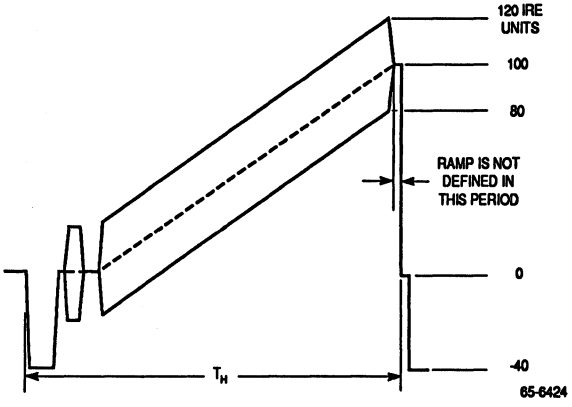


Figure 2. Modulated Ramp Test Signal

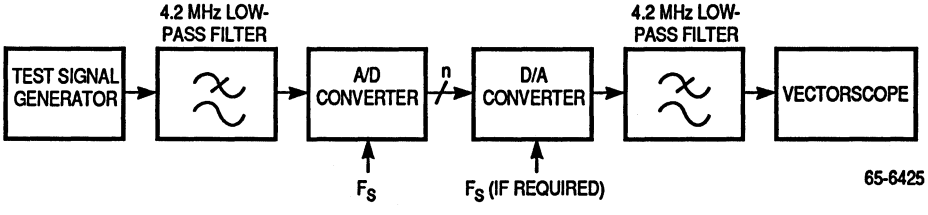


Figure 3. Differential Gain and Phase, Test Set Up

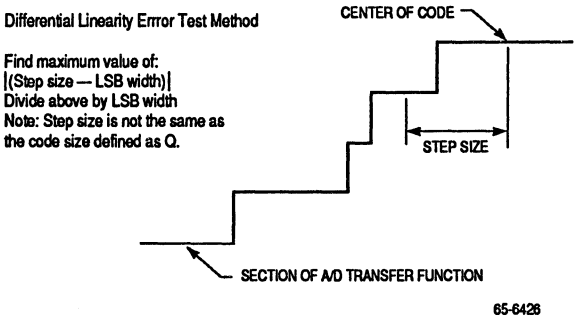


Figure 4. Differential Linearity Error

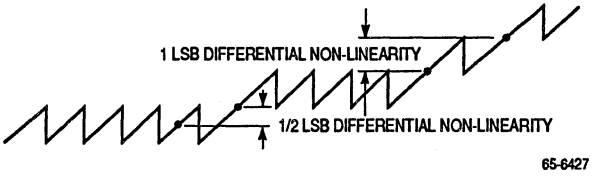


Figure 5. Differential Non-Linearity Measurement

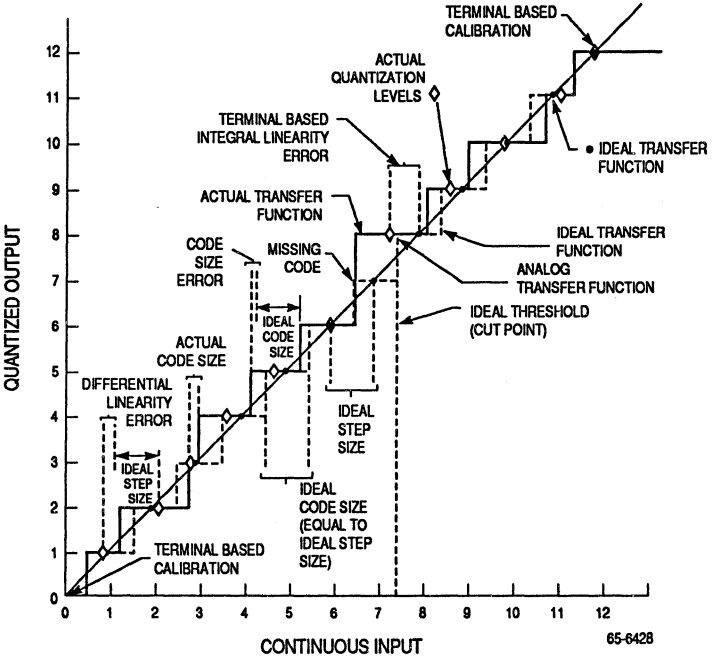


Figure 6. A/D Converter Transfer Function

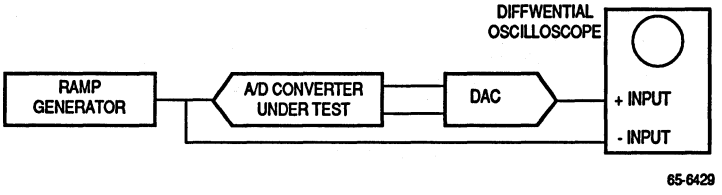


Figure 7. Subtractive Ramp Test Set-Up

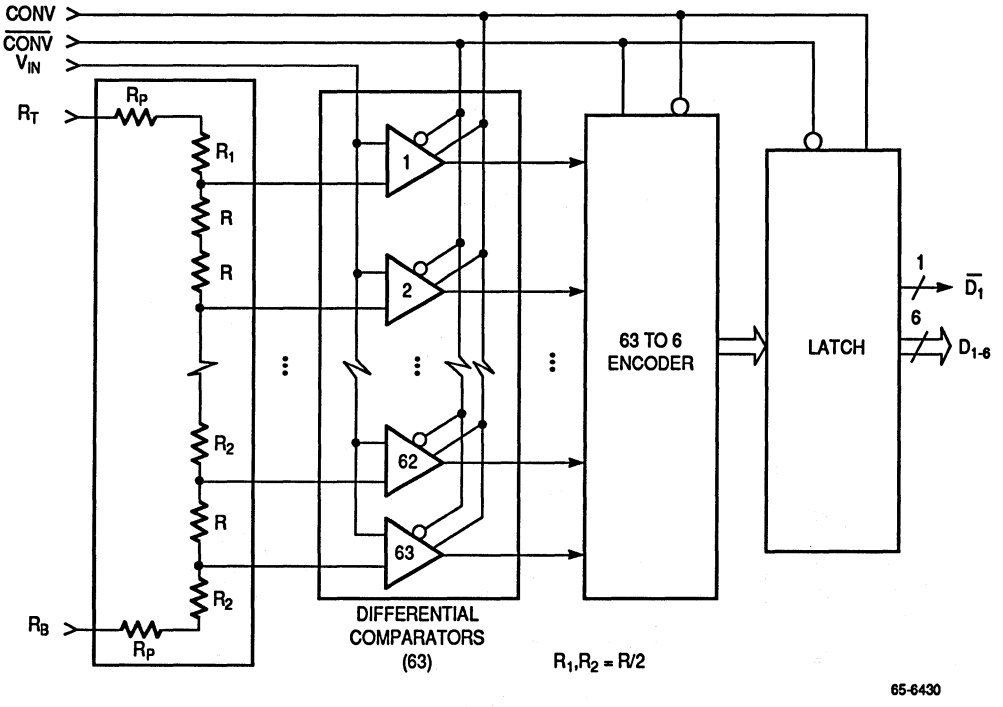


Figure 8. 6-Bit Flash A/D Block Diagram

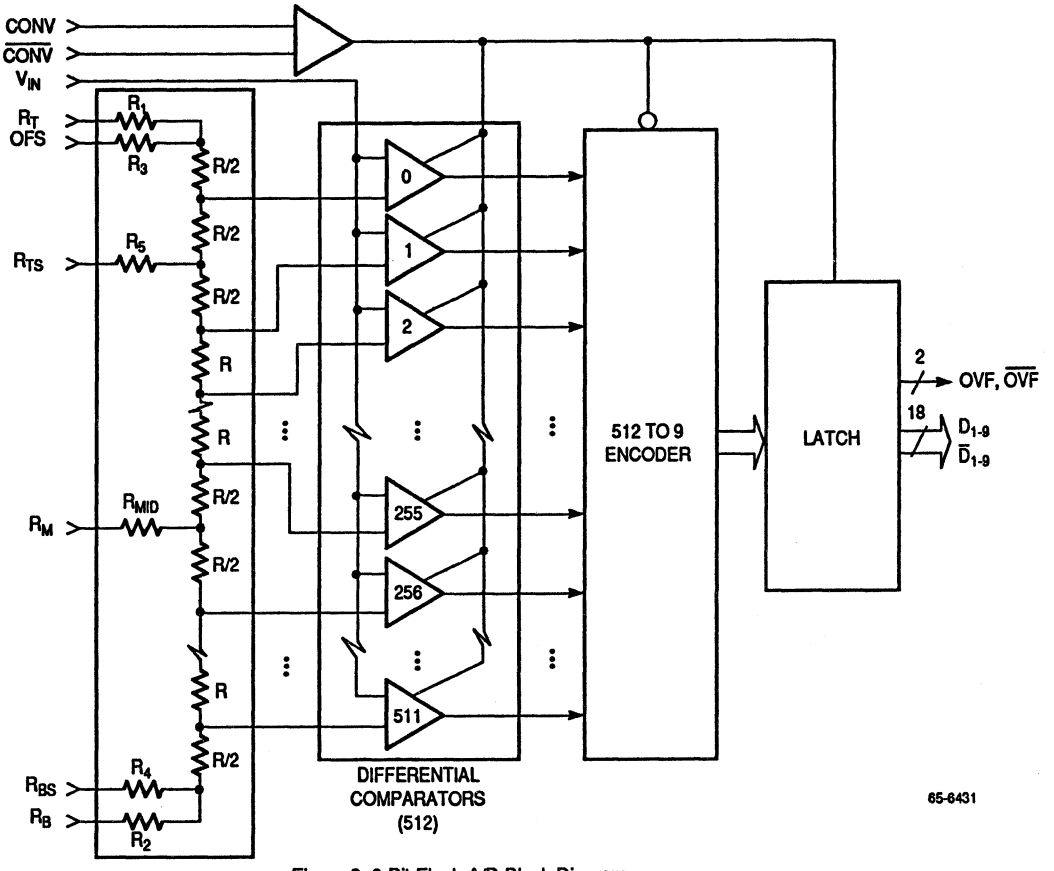


Figure 9. 9-Bit Flash A/D Block Diagram

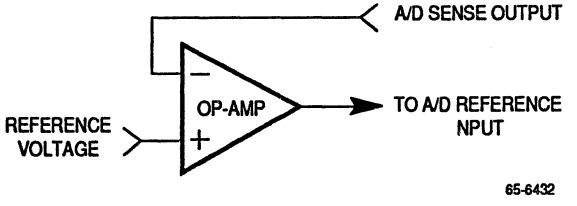


Figure 10. Driving a Reference with the Sense Connection

Video Terminology

AGC

Automatic **G**ain **C**ontrol in a video system is a circuit or subsystem that senses video amplitude and automatically adjusts amplifier gain to increase or decrease the video signal to the desired level.

ALPHA-channel

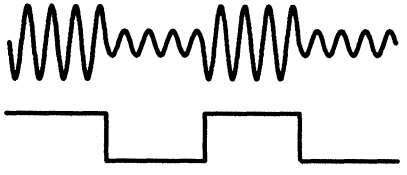
α is a digital value (usually 8- or 10-bits, normalized, and ranging from 0 to 1) that is associated with the mixing of two video sources. The value of α scales the magnitudes of input video in the following mixer equation:

Mixed video = (α)(Video #1) + (1-α)(Video #2)

α values are also associated with each RGB color pixel in graphics and imaging systems. α is used to scale the intensity an image on a pixel-by-pixel basis.

AM

Amplitude **M**odulation refers to adding low frequency information to a high-frequency signal by changing its amplitude in proportion to the low frequency information. Amplitude modulation of the color subcarrier frequency in video results in the variation of color intensity (saturation). Amplitude modulation of a carrier frequency is the way the video portion of a television signal is transmitted over an rf channel and is the basis of AM radio.



Anti-aliasing Filter

A low-pass analog filter preceding an A/D converter. The purpose of this kind of filter is to sufficiently attenuate frequency components above the signal band of interest. If not sufficiently attenuated, unwanted noise and high frequency components will alias (mix) themselves back into the critical frequency band, and degrade A/D conversion results. Since the unwanted frequencies become mixed with the wanted frequency band, it then becomes impossible to separate the two later in the system.

Aperture Delay, Error, Jitter, Uncertainty

Aperture is an analog-to-digital converter concept referring to the window of time when the A/D converter is sampling and its input signal.

Aperture delay is the absolute time between the clock edge that initiates the conversion cycle and the time when the input signal is actually sampled.

Aperture Error, Jitter, and Uncertainty are different terms for essentially the same thing. They refer to the changes in Aperture Delay exhibited on a sample-to-sample basis. Excessive Aperture Error, Jitter, and Uncertainty degrade A/D converter dynamic performance parameters such as SNR (signal-to-noise ratio).

APL

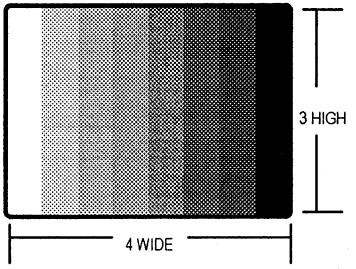
Average **P**icture **L**evel is a video term that refers to the variation in active video levels as the TV picture changes from very dark to very light scene content. Under normal operating conditions, APL can vary widely and quickly, burdening circuit elements such as AGC, clamps, and DC-restore.

Artifact

A video artifact is an unwanted characteristic of a television picture due to noise, improper image filtering, or timing errors.

Aspect Ratio

The ratio of picture width to picture height. For NTSC and PAL, the aspect ratio is 4:3. The aspect ratio for HDTV will be set at 16:9.



B-Y

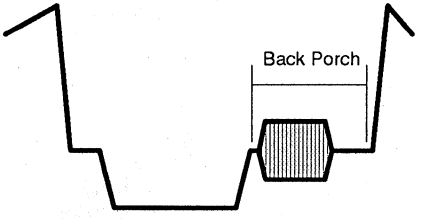
One of the "color-difference" signals derived from matrix multiplying RGB values by various constants. The other color-difference signal, (R-Y), is derived in conjunction with (B-Y).

B-Y = -0.299 R - 0.587 G + 0.866 B

Back Porch

The portion of the horizontal interval of a video line beginning with the rising edge of Horizontal Sync and ending with the beginning of active video.

Back porch includes Breezeway, Color Burst, and Color Back Porch.



Bandwidth

A range of frequencies over which a circuit or system works without degrading. The bandwidth of NTSC video is approximately 4.2 MHz and 5.5 MHz for PAL, meaning that frequency components from near-DC to the bandwidth limit are normally expected to be present. For an A/D converter, bandwidth refers to the range of input frequencies over which the A/D converter is to accurately work without degrading the result.

Bandwidth Flatness

The flatness of a frequency band is the measure of the variation of the amplitude of all frequencies in the band of interest. In the NTSC video band of 4.2 MHz, a flatness of +/-1 dB is considered to be acceptable.

Baseband

Composite video normally occupies a frequency span from near-DC to 4.2 MHz for NTSC and 5.5 MHz for PAL. When video is applied to an rf modulator for transmission on a television channel, the resulting AM modulated rf is no longer baseband.

BetaCam

A combination VCR and color TV camera, carried on one shoulder, used for recording local news events or other video productions. BetaCam offers much higher video quality than S-Video or VHS....but at a considerably higher price.

Black Balance

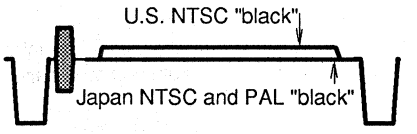
A color TV camera operation that examines the red, green, and blue analog signal values from the image sensor elements and adjust them so that a true black signal (no Chrominance) results when the camera is focused on a black object.

Black Burst

A composite video signal that carries with it all Horizontal and Vertical Sync, Color Burst, and Set-up (Pedestal) if applicable to the television standard in effect. No active video is allowed in Black Burst. See Black Level for waveform.

Black Level

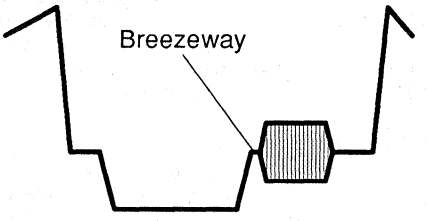
Black level is the active video amplitude of a black picture. In the NTSC television standard used in the U.S., the black level is defined to be 7.5 IRE units above that of the blanking level. The NTSC used in Japan and in PAL, the black level is defined to be exactly the same as blanking. The elevated black level is also known as "setup" or "pedestal."



Blanking
The video signal level of the Front Porch, Breezeway, and Color Back Porch. The term blanking refers to the shutting off of the red, green, and blue CRT electron beams at the end of each line and field allowing the sweep circuitry to retrace and set up for the next line or field.

Blooming
A TV camera term where one or more of the red, green, and blue image sensors overloads due to excess light and causes the image to clip at its maximum brightness. This was common before the use of solid-state CCD image sensors.

Breezeway
That portion of a video horizontal interval between the rising edge of Horizontal Sync and the beginning of Color Burst.



Broad Pulse
Another term used for the Vertical Sync pulses (between the strings of Equalizing Pulses) in the Vertical Sync interval.

Burst Gate
A video system signal that indicates the timing of the Color Burst in the Horizontal Blanking Interval.

CCD
Charge Coupled Devices are used for almost all TV camera image sensing applications. A single CCD is used in consumer quality CamCorders, sensing the three primary colors, red, green, and blue. In more expensive TV cameras, including studio cameras, three separate CCDs sensitive to red, green, and blue light capture the image.

CCIR
Comite Consultatif International des Radio-communications. The United Nations regulatory body covering all forms of radio communications.

Chrominance
That component of a composite video signal that contains only amplitude- and phase-modulated subcarrier. Chrominance carries with it no information about Sync or Luminance.

Chroma Bandwidth
Chrominance (the color component of video) comprises a phase and amplitude modulated subcarrier frequency. The span of frequencies generated by phase and amplitude modulation of the color subcarrier frequency is the chrominance bandwidth. The NTSC chrominance bandwidth is approximately 1.3 MHz on a 3.58 MHz subcarrier.

Chroma Demodulator
Chrominance comprises a phase and amplitude modulated subcarrier frequency that carrier with it all color information for a video signal. In video processing, it is often necessary to extract color information signals. A Chroma Demodulator circuit provides color difference signals from chrominance.

Chroma Key
Chroma key is a video special effect that allows one image to be superimposed over another. A foreground image is keyed over (switched in place of) a background image wherever there is a specific color (usually blue or green) found on the foreground image.

Chroma Trap
A band rejection filter specifically designed to reject the color subcarrier portion of a composite video signal without altering the luminance portion of the video.

Clamp
A circuit element in a video system that forces the Front and Back Porch blanking level of composite video to a specific desired voltage. Normal composite video requires that the Back Porch level be 0.0 Volts. Video transmission lines are usually AC-coupled, causing the DC reference to be lost. A/D Converters may require the Back Porch level to be at some other voltage. Clamp circuits force composite video to the prescribed levels.

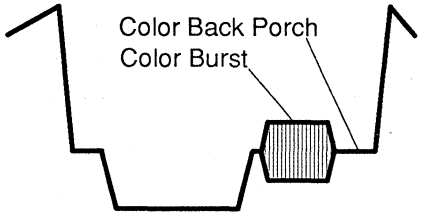
Clipping
Under certain light conditions the "white" level of composite video may exceed the maximum allowable for transmission or processing. Clipping circuits prevent video from exceeding these limits.

Closed Captioning
Closed Captioning data is inserted and transmitted on one of the Black Burst lines at the top of each field. A Closed Captioning decoder extracts that data, converts it to text, and superimposes that text over the video program.

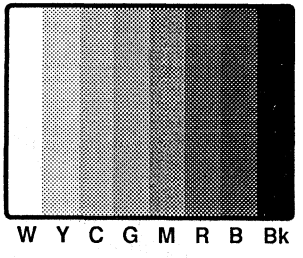
CLUT
A Color Look-Up Table is found on digital video encoders, mixers, and RAMDACs. The CLUT is a small block of high-speed RAM that maps pixel input data to a specific color. The CLUT of a typical VGA RAMDAC maps the 8-bit pixel data into 256 different colors made up of 18-bits each (6-bit red, 6-bit green, 6-bit blue).

Coaxial cable
The most common method of transporting composite or serial digital video around a system or studio is over a cable comprising a center conductor and a surrounding grounded shield. Low cost coaxial cables offer low loss, wide bandwidth, and low noise video performance.

Color Back Porch
That portion of the Horizontal Sync interval between the end of Color Burst and the beginning of active video



Color Bars
A video test signal that displays eight vertical bars of six fully-saturated colors plus black and white. The six colors are the three primary colors (red, green, and blue) and their three complements (cyan, magenta, yellow).



Color Burst
That portion of the Horizontal Sync interval after Breezeway and before Color Back Porch. From eight to eleven full cycles of color subcarrier frequency define the Color Burst. The Color Burst envelope has a specific shape, controlling the growth and decay of the color subcarrier waveform. Color Burst provides a subcarrier reference for color demodulation.

Color Decoder and Color Demodulator
See Chroma Demodulator

Color Difference
Components of color based upon a matrix multiplication operation on RGB values. (R-Y) and (B-Y) color difference components can also be visualized by mapping color vectors onto the 0^{o} and 90^{o} polar coordinate axes.

Color Encoder
The circuit element that outputs chrominance from the two color difference signals. This is the opposite function of the color decoder.

Color Framing
A color frame in NTSC consists of four sequential fields comprising all possible combinations of Color Burst phase and vertical sequences. PAL color framing is an 8-field sequence.

Color Killer
When incoming video in a video system does not contain color information (monochrome, without chrominance) there is no need to separate color difference components from chrominance. the color killer circuit detects the missing color burst and disables the color decoder accordingly, eliminating any color artifacts.

Color Purity
Color Purity is a measure of how close a specific color comes to its target saturation and hue. When displaying color bars on a vectorscope, each of the six color vectors should be centered in the graticule box that corresponds to its saturation (chrominance amplitude) and hue (chrominance phase angle with respect to color burst).

On a television screen, color purity is a subjective test. Color purity is best determined by painting the entire screen with fully-saturated red. Variations in the displayed color indicate mis-aligned electron guns or a magnetized shadow mask in the picture tube.

Color Space
The Chrominance component of composite video is usually divided further into components of color. The most common color components, or color spaces, are (B-Y)(R-Y), C_BC_R, IQ, UV, and HS.

Colour
With all due respects to the Queen, this word is simply misspelled. It should be 'color', and everybody knows what color is. Except, of course, those who are blind or color-blind, and then it really doesn't matter much, does it?

Comb Filter
A special filter used for separating chrominance from composite baseband video. A comb filter is a far better filter than a chrominance trap because it can pick out chrominance components that overlap into the luminance frequency band. When plotted, the frequency response of this kind of filter looks like the teeth of a comb.

Component
Composite video can be separated into components. Horizontal and Vertical Sync pulses, Luminance, and Chrominance information combine to make composite video. Chrominance can be further separated into color difference signals such as (B-Y)(R-Y), C_BC_R, IQ, UV, etc.

Composite Video
Composite video is the signal formed by combining Horizontal and Vertical Sync, Color Burst, Luminance, and Chrominance.

Contouring
An image artifact from limited gray-scale or color resolution. Instead of gradual changes in color shading, the image will have lines that resemble the isobars on a weather map. Contouring is usually not noticeable with 7-bit or greater gray-scale resolution.

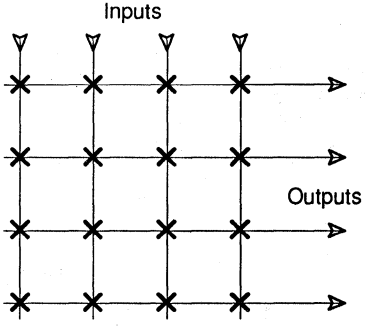
Contrast
The separation between the whitest white and blackest black of an image. Low contrast images look like they have a lot of gray in them.

Co-site Sampling
When video is digitized, decoded, and then transmitted in component form, pixels are decoded into a set of components corresponding to a single location on the displayed image. The Luminance of that pixel is represented by Y and the color components of that same location are C_BC_R. Therefore, it takes a complete set of YC_BC_R data to completely define one pixel.

Cross-Color Distortion
Luminance information that is inadvertently decoded as part of the Chrominance signal. For example, vertical stripes on a coat can be interpreted as subcarrier due to their relative spacing when compared to the period of the subcarrier frequency.

Cross-Luma Distortion
Chrominance information that is inadvertently decoded as Luminance.

Crosspoint Switch
A switching or networking element in a video system that interconnects any of x inputs to any of y outputs. The Crosspoint switch is a key element in a video production mixer or video routing system. A 4x4 crosspoint switch array is shown below.



Crosstalk
The unwanted noise or distortion on a signal that has been injected by other signals near the signal being measured.

CVBS
An abbreviation for **C**omposite **V**ideo **B**lank and **S**ync. The CVBS bus is a high-speed data path between video processors over which digital composite video data is sent. Sync pulses and blanking levels are later extracted from this data.

D-1
A digital video standard for $YC_BC_R4:2:2$ components sampled at 13.5 MHz. Digital video is transmitted serially at 270 Mbit per second or in 10-bit parallel format at 27 Mword per second. D1 is also known as CCIR-601.

D-2

A worldwide standard for digital composite video sampled at 4 x f_{SC} (14.318 Msps for NTSC and 17.732 Msps for PAL).

Data Key

Digital Video Encoders like the TMC22190 offer a feature that allows keying (pixel switching) by matching input RGB color combinations with pre-programmed colors stored in the data key register. When the input color does not match the stored color, RGB input data is encoded. Whenever the input color matches the stored color, the encoder outputs video corresponding to the data found on the CVBS bus.

DC-Restore

During video processing, the DC voltage level of blanking, 0.0 Volts, may have been modified. DC Restore circuits bring the blanking level back to 0.0 Volts for transmission. See also Clamp.

Decimating Filter

A digital filter that not only outputs data at a rate lower that data in input (1/2 the rate for 2:1 decimation) but also attenuates unwanted image artifacts caused by the decimation process.

Decoder

The process of extracting Luminance and color difference components such as (R-Y)(B-Y) or C_BC_R from composite video is the function of a decoder. Various filtering techniques are also employed in a decoder to accurately separate Chrominance information from Luminance and thereby improve picture quality.

Differential Gain

A video parameter that quantifies color accuracy over the black-to-white Luminance range. Dg is measured by superimposing a constant amplitude subcarrier on a linear ramp or stair-step Luminance signal. The variation in the amplitude of the subcarrier, dg, corresponds to variations in color saturation.

Differential Phase

A video parameter that quantifies color accuracy over the black-to-white luminance range. Dp is measured by superimposing a constant phase subcarrier on a linear ramp or stair-step Luminance signal. The variation in the phase of the subcarrier, dp, corresponds to variations in color hue.

Digitizer

Another term for Analog-to-Digital Converter (A/D) except that a digitizer will have circuit functions like clamps, amplifiers, and other elements necessary to complete the process of converting composite video to digital data.

Dissolve

A controlled transition between two video images. In a dissolve, the original image decreases in amplitude at the same time as the second image increases. The second image is gradually superimposed over the original until it dominates and there is no original image at all.

Doubly-Terminated

1. When terminating resistors are located at both source and destination ends of coaxial cable.
2. When too many terminating resistors are connected to a coaxial cable, attenuating the video signal.

Downstream Key

The last key source in a multilayer keyed composite image. The Downstream Key places the top-most image on the composite image.

Edge Rate

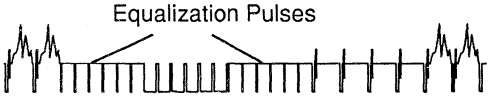
The rise and fall slopes of Horizontal and Vertical Sync pulses, Color Burst envelope, and the beginning and end of active video must be limited and controlled to keep high-frequency components from exceeding the channel bandwidth.

Encoder

Encoders assemble composite video from its components. For example, the inputs to an encoder are Horizontal and Vertical Sync, RGB or YC_BC_R component video, or color-index values. The output is complete baseband composite video including all H and V Sync timing.

Equalization Pulse

A series of pulses in the Vertical Sync interval just preceding and following the series of Vertical Sync pulses.



Even Field
One of the two fields that make up each frame of an interlaced video signal. Video "half-lines appear at the end of each even field. See Field, Odd Field

Fader
A video processing element that fades or dissolves a video image to black (or from black). Many consumer CamCorders have automatic faders that operate at the touch of a button.

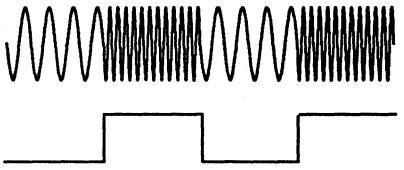
Field
In an interlace video system such as NTSC and PAL, each frame of 525 lines (625 for PAL) is made up of two fields of 262.5 line apiece (312.5 for PAL). In NTSC there are 59.94 fields per second while PAL produces 50. But PAL flickers, yes it does.

Field Sequence
The combination of Equalization Pulses, Vertical Sync pulses, video half-lines, and Black Burst lines (including VITS, SMPTE Time Code, Closed Captioning, etc.) found between the last active video line of one field and the first active video line of the next field.

Field Tilt
A video parameter that indicates the drift or change in blanking level from the beginning of a field to the end of that field. Field tilt is usually caused by inadequate back porch clamping of the blanking level to 0.0 Volts.

Flat Field
A video test signal for measuring field and line tilt. The flat field is either a full field of Black Burst or a full field of constant gray or white (no Chrominance).

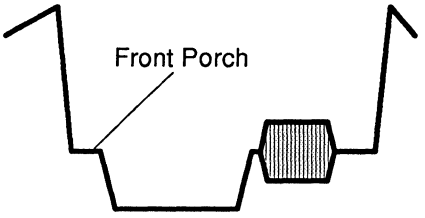
FM
Frequency Modulation refers to adding low-frequency information to a high-frequency signal by changing its frequency in proportion to the low frequency information. Modulation of the color subcarrier frequency in SECAM video systems results in changing the color intensity or saturation. Frequency modulation of a carrier frequency is the principle behind the transmission of the audio portion of television programs over an rf channel, and FM radio.



Frame
In an interlaced video system such as NTSC or PAL, a frame is made up of two interlaced fields. The frame rate for NTSC is 29.97 and 25.0 for PAL, exactly 1/2 of the field rate.

Frame Store
A digital Video system that captures by digitizing and writes into RAM all of the pixels comprising a frame of video.

Front Porch
That portion of the Horizontal Sync interval after the end of active video and before the falling edge of Horizontal Sync.



Gamma
A mathematical correction factor, γ, used to compensate video systems for non-linearity such as that found in optical image sensors and CRTs.

In the transfer function: Output = K (Input)$^{1/\gamma}\gamma$ introduces a non-linearity the compensates for non-linearity associated with the input. Typical values for γ in NTSC and PAL are 2.2 and 2.8, respectively.

Generations
When recording video on tape, each subsequent copy of a copy of a copy is a generation. Digital recording techniques and equipment permit many more generation to be produced without significantly degrading picture quality.

Genlocking
The video process of extracting Horizontal and Vertical Sync from composite video for the

purpose of synchronizing video cameras, recorders, and other video processing systems.

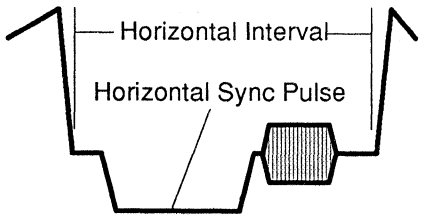
Group Delay
A video parameter that compares the relative propagation delay of different frequencies in the video band. If, for example, low frequencies such as 100 kHz have a significantly different delay through a video filter or amplifier than the color subcarrier frequency, 3.58 MHz (NTSC), Luminance features of a picture will not align themselves with the color of that feature. That will look bad.

GRS
The **G**enlock **R**eference **S**ignal includes subcarrier frequency, subcarrier phase, and field identification digital data. It is transmitted from the TMC22070 Genlocking Video Digitizer to the TMC22090 and 22190 Digital Video Encoders over the CVBS bus during Horizontal Sync.

HDTV
High **D**efinition **T**ele**V**ision is a video technology of the future which promises to dramatically improve image quality by increasing signal bandwidth as well as line and frame rates. HDTV will require high-speed A/D and D/A converters as well as very high speed digital video processors. Also know as "Advanced Television."

Horizontal Interval
The Horizontal Sync interval is the series of signals between the end of active video of one line and the start of video for the next line. It includes the Front Porch, Horizontal Sync, Breezeway, Color Burst, and Color Back Porch (all of Back Porch).

Horizontal Sync
A negative-going pulse at the end of every line. This pulse triggers CRT retrace and the beginning of the next line.



HSI
Hue, **S**aturation, and **I**ntensity color components. These correspond closely to the controls found on most TV sets: tint (hue), color (saturation), brightness and contrast (intensity).

Hue
That characteristic of color that differentiates Rosy Red from Vida Blue from Mellow Yellow. in a polar coordinate vector display, hue corresponds to the angle of the vector with respect to the Color Burst.

Hum Bars
Noise induced from AC power line voltages may appear as horizontal lines scrolling vertically in the displayed image in NTSC. In PAL, hum bars due to 50 Hz power will be stationary.

I^2C
A serial 3-wire interface between integrated circuits used to set-up and control those circuits.

Interlace
In NTSC and PAL video systems, an image is scanned in two passes. The scanned lines of the first pass (field) are interlaced with the lines of the second pass. The interlaced lines do not overlap each other, but rather fill in the space between lines of the next pass.

Interpolation Filter
A digital filter that doubles the sampling rate of the input data by calculating (interpolating) a new data point on the basis of two or more sequential input points. The new data point is inserted between the input data points used for its calculation.

IRE Units
The **I**nstitute for **R**adio **E**ngineers developed a scale for measuring video signal amplitudes. Sync pulses are to be 40 IRE units in amplitude and active video is limited to 100 IRE units. The entire range of 140 IRE units was defined to be 1 Volt peak-to-peak. NTSC waveform monitors usually have a graticule showing IRE units.

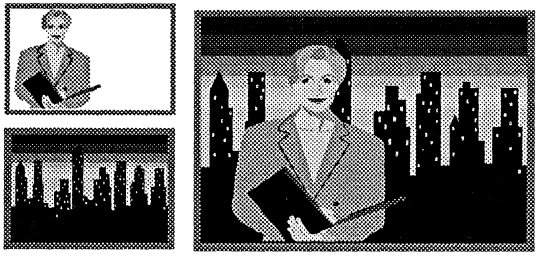
Jitter
See Aperture Jitter

JTAG
An integrated circuit test interface which allows board level testing of all interconnections to a large integrated circuit without testing the actual

function of the integrated circuit. See TMC22190 data sheet.

K-factor
A video parameter that is a measure of impulse response of a video system.

Key
A video processing method for superimposing one image over another. A key signal in the shape of the image to be superimposed is used to switch that image on in place of the background image. The newsreader is "keyed" over the city scene in the example below.



Lap Dissolve
Same as Dissolve. A controlled transition between images when one gradually overwrites (overlaps) the other.

Layer
When multiple key signals are used to build a multiple level composite image by keys, wipes, and dissolves, each component image is a layer.

Layering Engine
A circuit or system that accomplishes the layering (keying) of several images to form a single composite image. See TMC22190 data sheet.

Line
Video images are scanned by optical sensors from left to right, forming a line, repeating, one line at a time to build a complete two-dimensional image. Active video, Front Porch, Horizontal Sync, Color Back Porch, and Color Burst comprise each video line.

Line Rate
The number of video line scanned or displayed per second. In NTSC there are 15,734 lines per second, and 15,750 in PAL.

Line Tilt
A video parameter that indicates the drift or change in blanking or gray video level from the beginning of a line to the end of that line. Line tilt is usually caused by inadequate Back Porch clamping of the blanking level to 0.0 Volts or to short AC-coupling time constants.

Linear Key
Similar to digital keying except that the transition from background image to foreground image is a ramp, over which the foreground image gradually overwrites the background image. Same as "soft keying".

Linear Phase
A characteristic of a video filter or amplifier that ensures good group delay.

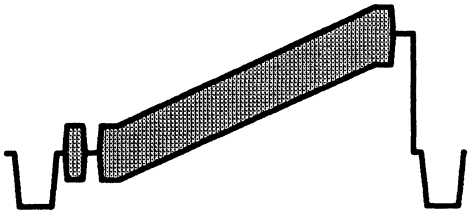
Linearity
A common system parameter that reflects the system's ability to closely follow and process input signals without adding errors and degrading results. In video, linearity sometimes relates to differential phase and differential gain performance.

Luminance
The black-and-white components of a video signal. When combined with Chrominance, the result is composite video.

Make-before-break
A term to describe the action of crosspoint switches. When a switch transition is made from one video source to another, it is important that there be no period of time during which the neither source is connected to the output. "Make-before-break" means that the new video source connection is made to the output just before the old video source disconnects.

Modulated Pulse
A video test waveform used in the testing of Group Delay and YC gain matching. A modulated pulse is a short period of subcarrier that grows and decays according to a specific pulse envelope.

Modulated Ramp
The video test waveform that is used in testing differential phase and differential gain.



Modulation

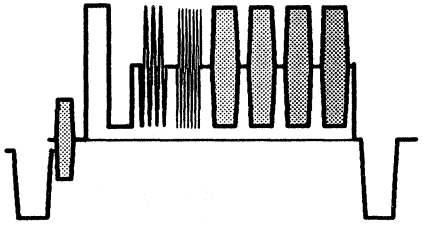
Adding information to a signal. For example, phase and amplitude modulation of the color subcarrier to make Chrominance. Adding Chrominance to Luminance is a Luminance modulation process. TV transmitters are AM modulated for video and FM modulated for audio.

Monitor

A television screen that accepts baseband composite video and displays the image. A monitor may be a subset of a TV receiver which can also detect and demodulate the rf signal from a television channel and display the image and amplify the sound.

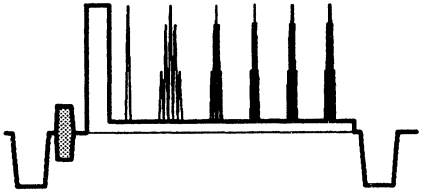
Multiburst

A video test waveform that includes short bursts of several frequencies (1.0, 2.0 MHz etc.) spanning the video band. When displayed on a waveform monitor, Multiburst offers a quick look at system frequency response by observing the relative amplitude of each frequency burst with respect to the others.



Multipulse

A video test waveform that includes series of short modulated envelope pulses of varying amplitudes, duration, and subcarrier frequency. When displayed on a waveform monitor, Multipulse offers a quick look at system pulse response and group delay.



Noise

Any part of a video signal that is not desirable and degrades the quality of the picture. Hum bars, speckles, ghosts, zits, etc. combine to reduce picture quality.

NTSC

A color television system developed by the National Television Standards Committee that is used in North America, Japan, and other parts of the world. NTSC is an interlaces system, characterized by 59.94 fields and 29.97 frames per second and 525 line per frame.

Odd Field

One of the two fields that make up each frame of an interlaced video signal. See Field, Even Field

Overlay

A computer graphics operation where colored text or patterns are written on top of a displayed image without modifying that image. Most RAMDACs and digital video encoders have additional overlay color RAM annexed to the CLUT for this purpose. Overlay is enabled on a pixel-by-pixel basis and the color of the overlay depends only upon the overlay RAM location addressed and the color value stored in that address.

Oversampling

Whenever a Digitizer of A/D Converter is clocked at a rate that is far in excess of the Nyquist criteria (>2x required bandwidth) the system is said to be oversampled. Oversampling in video systems relaxes the anti-alias filter cut-off requirements and reduces system cost. An oversampling A/D converter may be followed by a decimation filter to minimize the data bandwidth.

PAL

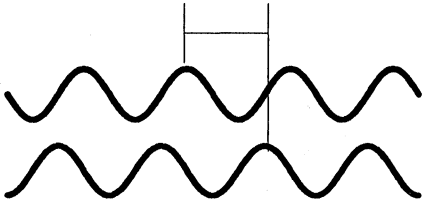
A color television system (Phase Alternate Line) used in Europe and other parts of the world. PAL is an interlaces system, characterized by 50 fields and 25 frames per second and 625 line per frame.

Pedestal

In NTSC systems, the blanking level of composite video is 0.0 Volts while the "**black**" color level is defined at +7.5 IRE units (+53 mV). This small difference between blanking and black is intended to completely cut off the CRT beam in the TV during retrace. PAL systems do not employ Pedestal (same as Setup).

Phase

The offset in time between two sinewaves of exactly the same frequency. Phase is usually expressed in degrees with 360 degrees of phase between sine peaks.



Phase-Lock Loop

In general, a phase-lock loop is a frequency synthesizer whose output is continuously compared to and varied according to some incoming reference frequency.

In video applications, phase-lock loops are used to generate a stable subcarrier frequency using incoming color burst as the phase and frequency reference signal. They are also used to generate A/D converter clock frequencies using the line scan frequency as the reference.

Pipeline Latency

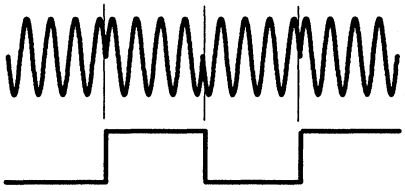
In a digital system or processor, there is a period of time between the entering of data into the system and the emerging of processed data corresponding to that data. This time interval is usually divided into discrete time elements or clock periods which control the processing operations. Latency is the number of clock cycles between the input and the result based upon the inputs.

Pixel

The most basic element of an image. When digitized, each video line is divided into discrete elements, pixels, which are characterized only by position and color. Images are a collection of a number of pixels per line and lines per frame.

PM

Phase **M**odulation refers to adding low frequency information to a high-frequency signal by changing its relative phase in proportion to the low frequency information. Phase modulation of the color subcarrier frequency in video results in changing the color hue.



Pulse Bar

A video test waveform that includes short pulses and black-to-white transitions.

QAM

In video processing, **Q**uadrature **A**mplitude **M**odulation is the process of applying the color component signals (U and V) to amplitude and phase modulate the color subcarrier, producing Chrominance.

Raster

A term used to describe the horizontal and vertical scanning of the electron beams in a TV or other CRT display.

R-Y

One of the "color-difference" signals derived from matrix multiplying RGB values by various constants. The other color-difference signal, (B-Y), is derived in conjunction with (R-Y).

R-Y = 0.701 R - 0.587 G - 0.114 B

Reconstruction Filter

An analog filter used to smooth the transitions between discrete analog voltages produced by a Digital-to-Analog converter (D/A) when reconstructing wideband signals such as video. The filter must have good group delay characteristics as well as adequate attenuation of frequencies beyond the video band.

RGB

The most base components of color, the primary colors **R**ed, **G**reen, and **B**lue. Combining all possible intensities of red, green, and blue light sources produces an infinite number of visible colors.

Routing
The interconnection and distribution of video signals throughout a video system such as a production studio or television station. Video sources and destinations are usually routed through the use of crosspoint switches.

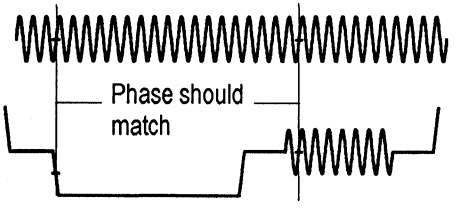
RS-170A
A Television Standard specification that defines and describes the signal characteristics of NTSC. See SMPTE 170M.

S-Video
A baseband video standard that keeps Luminance
separate from Chrominance. S-Video connectors and cables carry two video signals, one for Luminance and the other for Chrominance.

Sample-and-Hold
A circuit element that acquires an analog signal by sampling that signal and then holds the DC level of that signal at the time it was sampled. A sample-and-hold is usually found at the front end or internal to A/D converters. They hold the A/D input steady while the digital equivalent to the held DC level is determined.

Saturation
The characteristic of color that differentiates Navy Blue from Baby Blue, Blood Red from Pink, and Kelly Green from Mint Green.

SCH Phase
SCH is the **S**ub**C**arrier phase relationship between the falling edge of **H**orizontal Sync and the phase angle of the Color Burst. Whenever video signals are mixed, it is very important that the SCH characteristics of the two video signals be matched. If SCH errors are present, the mixed video will suffer from incorrect colors and horizontal spatial shifts.



SECAM
A television system primarily used in France, China, Soviet Union (R.I.P.), and the middle East. SECAM is similar to PAL except that the color subcarrier is frequency modulated instead of phase modulated for varying color hue. This renders SECAM completely incompatible with PAL and NTSC.

Serial Digital
A digital communication standard that sends digitized video (and audio) through 75 Ohm cables at 270 Mbits per second conforming to CCIR-601 specifications. Serial Digital is becoming the studio interconnection standard.

Serration
The series of Equalization and Vertical Sync pulses found between fields in the vertical interval.

Setup
In NTSC systems, the blanking level of composite video is 0.0 Volts while the **"black"** color level is defined at +7.5 IRE units (+53 mV). This small difference between blanking and black is intended to completely cut off the CRT beam in the TV during retrace. PAL systems do not employ Setup (same as Pedestal).

Short time Distortion
SD is a video parameter that describes the character of fast changing Luminance in video. Rise time, fall time, overshoot, undershoot, ringing, and damping of fast edges are compared to ideal transitions for the measurement.

Sine-Squared Pulses
A pulse and fast edge video test signal that is bandlimited within the limits of the baseband composite video. In NTSC systems, rise and fall times of Sine-squared pulses are limited to 125 nanoseconds. The limits are 100 nanoseconds in PAL.

Skew
The actual difference in time of two or more events that are ideally supposed to be simultaneous. For example, the data sent out from an A/D converter are ideally supposed to change simultaneously, but may not. Luminance and Chrominance outputs of encoders and RGB outputs of RAMDACs are ideally supposed to be simultaneous. There may be, however, a small skew between these signals.

SMPTE
Society for **M**otion **P**icture and **T**elevision **E**ngineers.

SMPTE-170M
An NTSC video standard developed by SMPTE that replaces RS-170A.

SMPTE Time Code
A digitally coded set of data usually found in vertical interval line 19 that indicates the hour, minute, second, and frame number of video. SMPTE Time Code is extensively used in videotape editing and in record keeping. It may also be encoded on the audio track of videotape (linear time code).

SNR
Signal-to-Noise Ratio is the ratio in decibels (dB) of the wanted signal amplitude to the unwanted noise in a video signal.

Soft Key
A key transition between a foreground image and a background image during which there is a controlled gradual transition instead of a switched instantaneous transition. See also Key, Layer

Square Pixel
When a video line is digitized and divided into discrete picture elements that have equal horizontal and vertical dimension with respect to the displayed image, the pixels are "square." A circle displayed 100 pixels high and 100 pixels wide will be round, not egg shaped.

Stair Step
A video test signal that ramps Luminance from black to white using 5 or 10 discrete DC levels (steps). Stairstep waveforms with constant amplitude and phase subcarrier added are sometimes used in differential gain and differential phase measurements.

Subcarrier
A high-frequency signal, added to the Luminance component of video that carries with it all color information. In NTSC, the subcarrier frequency is 3.579545 MHz and in PAL the frequency is 4.433618 MHz. Amplitude modulation (AM) of the subcarrier results in changes in color saturation while phase modulation (PM) of the subcarrier results in changes in hue.

Subcarrier Phase
The phase of subcarrier with respect to a reference subcarrier (i.e. color burst).

SVGA
Super **VGA** is a computer CRT display standard that employs 600 or more horizontal lines and 800 or more pixels per line. It is contrasted with VGA which employs 480 lines and 640 pixels per line. SVGA offers higher CRT resolution than VGA. The common SVGA resolutions are: 600 x 800, 768 x 1024, and 1024 x 1280.

SVHS
Super **VHS** is a VCR recording standard that separates the Luminance (Y) from Chrominance (C) and records both of these signals on tape. SVHS cassettes are similar to VHS cassettes but SVHS will not playback on regular VHS VCRs.

Sweep
A term used to describe the horizontal and vertical scanning of the electron beams in a TV or other CRT display. Sweep can also refer to the change or span of frequency in a video test signal.

Sync
An abbreviation that refers to the set of horizontal and vertical synchronizing pulses that indicate beginning of image lines and fields.

Sync Separator
A video processor that detects composite sync pulses and outputs separate horizontal and vertical sync pulses.

Sync Tear
An undesirable effect when a monitor input is switched between two asynchronous video sources. Sync tear occurs when video sources that are not genlocked are mixed or switched.

Sync Tip
The most negative voltage level of the video signal during the Horizontal and Vertical Sync pulses.

Termination
The resistive load placed at the source and/or destination end of a coaxial cable to ensure maximum signal integrity, proper impedance matching, and amplitude.

Tilt
See Field Tilt and Line Tilt

Time-Base Corrector
A video processing system that corrects variations in line and field timing due to video

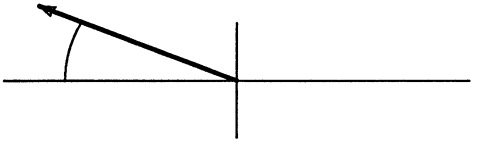
tape recorder head speed variations. These systems are also known as TBCs.

Tint

Same as Hue. That characteristic of color that differentiates Rosy Red from Ira Blue from Mellow Yellow. In a polar coordinate vector display, hue corresponds to the angle of the vector with respect to the Color Burst.

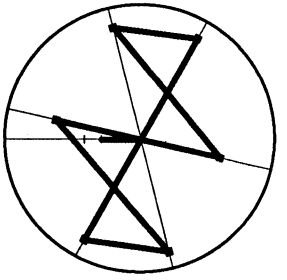
Vector

A vector is a quantity that has both magnitude and direction. In video, colors are represented by vectors in polar coordinates. Magnitude corresponds with the level of saturation and the direction of the vector corresponds to hue.



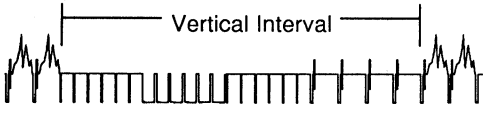
Vectorscope

A video test instrument that analyzes color subcarrier characteristics by displaying them on a polar coordinate scale as vectors. A Vectorscope can also display color components such as (R-Y) (B-Y), YIQ, RGB etc.



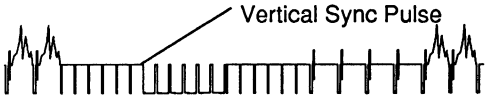
Vertical Interval

The combination of Equalization pulses, Vertical Sync pulses, video half-lines, and Black Burst lines (including VITS, SMPTE Time Code, Closed Captioning, etc.) found between the last active video line of one field and the first active video line of the next field.



Vertical Sync

A series of negative-going pulses at the end of every field. These pulses trigger CRT vertical retrace and the beginning of the next field.



VGA

A common computer video display characterized by 480 line per frame and 640 pixels per line, non-interlaced.

VITS

Vertical Interval Test Signals may have many purposes, primarily in-service studio and transmitter testing and automatic receiver adjustment. VITS information is inserted in place of the Black Burst lines at the top of each frame.

VM700

A video measurement test instrument made by Tektronix. This instrument is the industry-standard for measuring video parameters.

Waveform monitor

A video test instrument that displays the line and field waveforms of video signal.

White

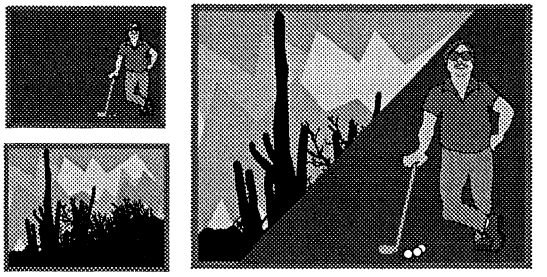
The on-screen color resulting from the red, green, and blue color components being active and at their full-scale value. White is the brightest value of Luminance.

White Balance

A color TV camera operation that examines the red, green, and blue analog signal values from the image sensor elements and adjust them so that a true white signal (no Chrominance) results when the camera is focused on a white object.

Wipe

A wipe is a video production term that refers to the transition from one video source to another. During a wipe operation, the screen is split in various patterns, uncovering the new video source while covering the old source. In the example below , the golfer shares a split-screen wipe with a desert scene.



Y

The Luminance component of video. For example, the Y in YC_BC_R, YIQ, YUV all refer to the Luminance or black-and-white component of the color video signal. Y is calculated from red, green, and blue values by:

$$Y = 0.299\ R + 0.587\ G + 0.114\ B$$

YC

A video component set which separates Luminance (Y) from Chrominance (C). S-Video is based on YC components. The Luminance signal is all that is displayed on a black-and-white TV or monitor.

YC_BC_R

A common color component set derived from Y(B-Y)(R-Y) components which, in turn, are derived from RGB values. YC_BC_R is the component set used in CCIR-601 and D-1 video standards.

YIQ

Another color component set similar to YC_BC_R except rotated through a different vector baseline. YIQ is most commonly associated with NTSC.

YUV

A modified video component set, similar to YC_BC_R. In YUV, UV are scaled in order to prevent overmodulation of the subcarrier modulator in an encoder.

2:1:1

Similar to 4:2:2 except at 1/2 the data rate. 2:1:1 is used in teleconferencing where video is sent over telephone lines.

25 Hz Offset

In most PAL standards, the subcarrier frequency, f_{SC} and the horizontal line frequency, f_H, are related by:

$$f_{SC} = ((1135 / 4) + (1 / 625)) f_H$$

The factor (1/625) adds 25 Hz the PAL subcarrier frequency. This offset masks the residual subcarrier dot pattern (sometimes seen on black-and-white displays) by causing the dot pattern to move, making it less visible..

4-field sequence

A complete field sequence for NTSC which includes all Color Burst phase and vertical interval sequences consists of 4 fields.

4x subcarrier sampling

Digitizing composite video at a rate (frequency) equal to exactly four time the color subcarrier frequency (14.318181 MHz for NTSC and 17.734472 MHz for PAL).

4:1:1

This suffix, when added to YC_BC_R ($YC_BC_R4:1:1$) indicates that for every 4 samples of Luminance data (Y) there is only one sample of C_B and C_R data available.

4:2:2

This suffix, when added to YC_BC_R ($YC_BC_R4:2:2$) indicates that for every 4 samples of Luminance data (Y) there are 2 samples of C_B and 2 samples of C_R data interleaved.

4:4:4

This suffix, when added to YC_BC_R or RGB ($YC_BC_R4:4:4$, RGB4:4:4) indicates that for every 4 samples of Luminance data (Y) or R there are 4 samples of C_B or G and 4 samples of C_R or B data.

601

Refers to the CCIR Recommendation 601-1, which describes and defines "Encoding Parameters of Digital Television for Studios."

8-field sequence

A complete field sequence for PAL which includes all Color Burst phase and vertical interval sequences consists of 8 fields.

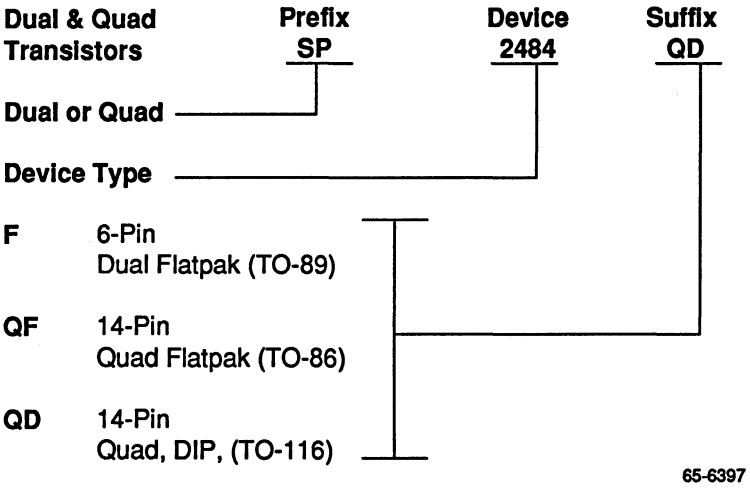
For further reading and study on VIDEO:

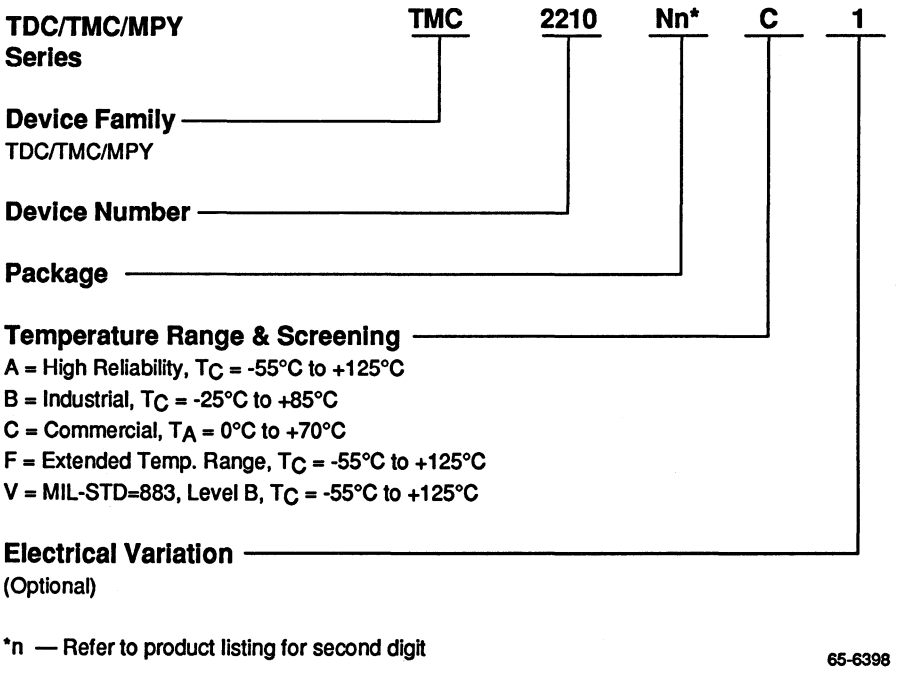
- CCIR 601-1 "Encoding Parameters of Digital Television for Studios"
- CCIR 624-3 "Television Systems"
- Craig, Margaret, "Television Measurements - NTSC Systems", Tektronix 1780R instrument literature
- Craig, Margaret, "Television Measurements - PAL Systems", Tektronix 1781R instrument literature
- Hutson, G.H., Shepherd, P.J., Brice, W.S., "Colour Television", McGraw-Hill Berkshire, England (1990)
- IEEE Standard Dictionary of Electrical and Electronic terms", John Wiley & Sons, New York (1972)
- Jack, Keith, "Video Demystified", High Text Publications, Solano Beach, California (1993)
- Roberts, R.S., "Television Engineering - Broadcast, Cable, and Satellite Part 1: Fundamentals", Pentech Press, London (1985)
- Roberts, R.S., "Television Engineering - Broadcast, Cable, and Satellite Part 2: Applications", Pentech Press, London (1985)
- SMPTE 170M Proposed SMPTE Standard for television - Composite analog video signal - NTSC for studio applications.
- Stafford, R.H., "Digital Television", John Wiley & Sons, New York (1980)
- Watkinson, John, "The Art of Digital Television", Focal Press, Oxford (1990)

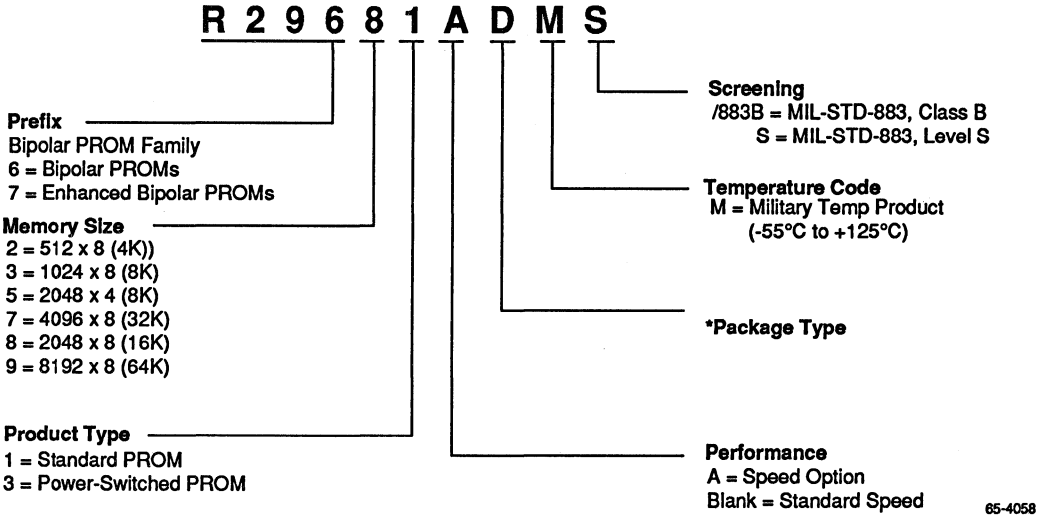
Section 9
Ordering Information & Packages

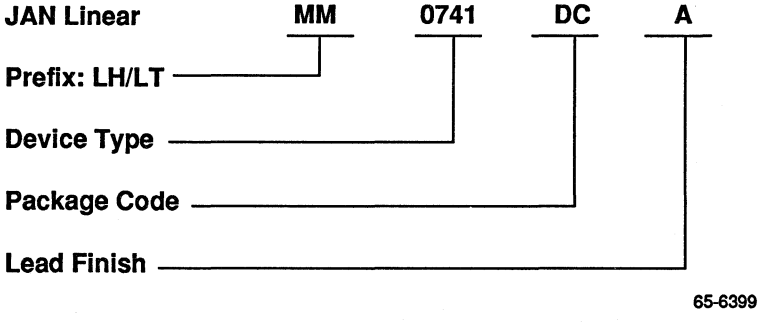
Contents

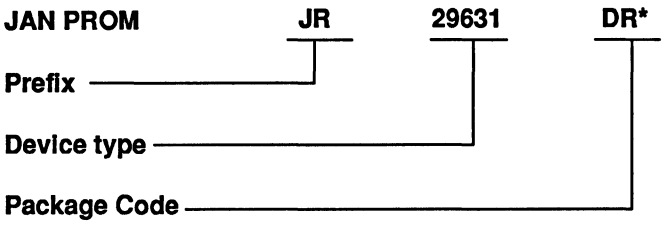
Product Ordering Information





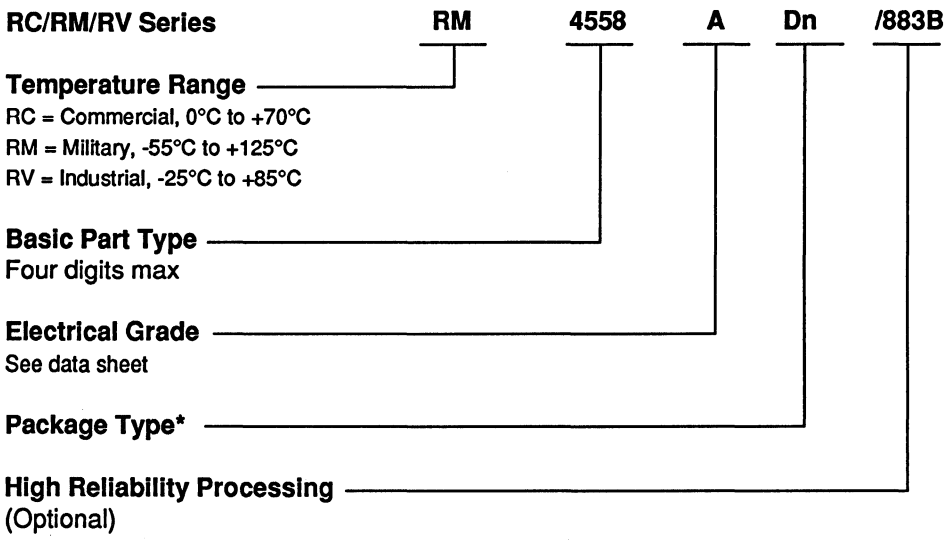

R 2 9 6 8 1 A D M S
Prefix
Bipolar PROM Family
6 = Bipolar PROMs
7 = Enhanced Bipolar PROMs
Memory Size
2 = 512 x 8 (4K))
3 = 1024 x 8 (8K)
5 = 2048 x 4 (8K)
7 = 4096 x 8 (32K)
8 = 2048 x 8 (16K)
9 = 8192 x 8 (64K)
Product Type
1 = Standard PROM
3 = Power-Switched PROM
Screening
/883B = MIL-STD-883, Class B
S = MIL-STD-883, Level S
Temperature Code
M = Military Temp Product
(-55°C to +125°C)
*Package Type
Performance
A = Speed Option
Blank = Standard Speed
65-4058


JAN Linear
MM
0741
DC
A
Prefix: LH/LT
Device Type
Package Code
Lead Finish
65-6399



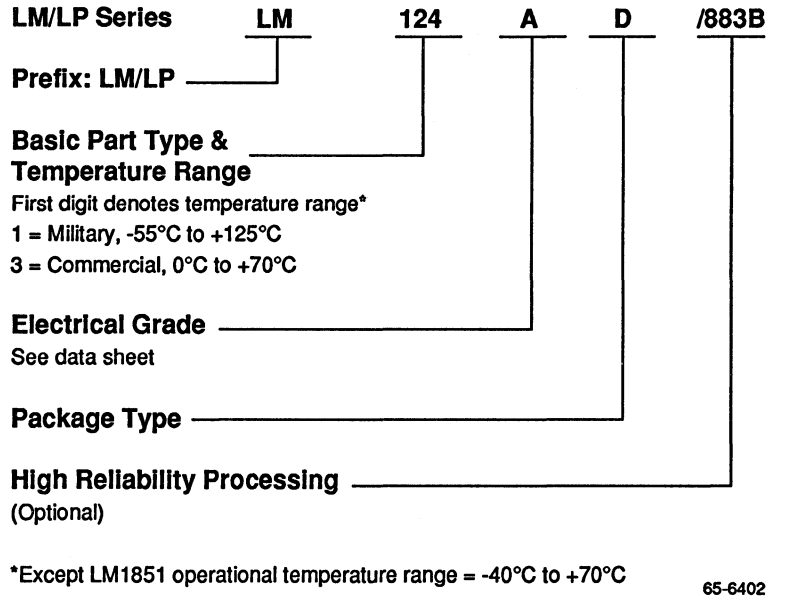
*All devices supplied with solder dip lead finish

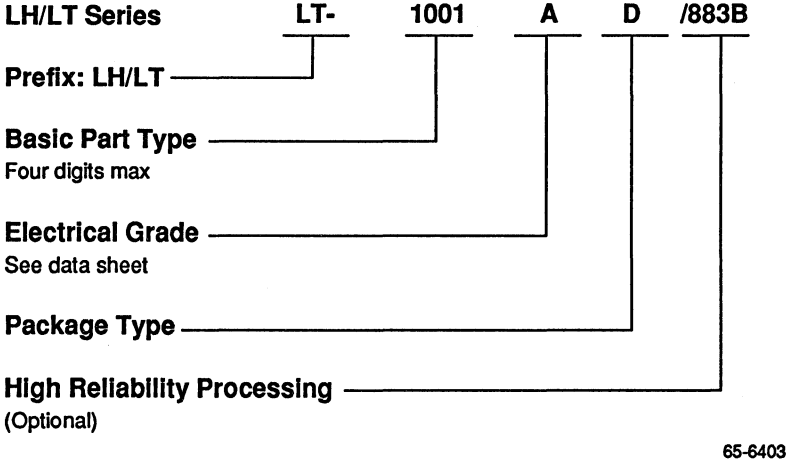
65-6400

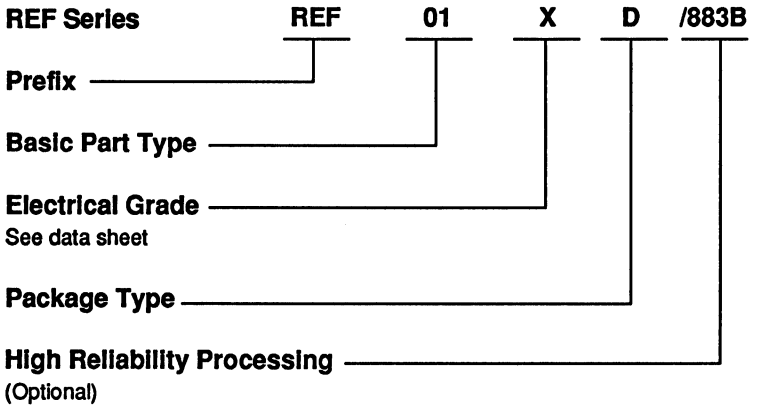


*Second digit is optional. Refer to product listing.

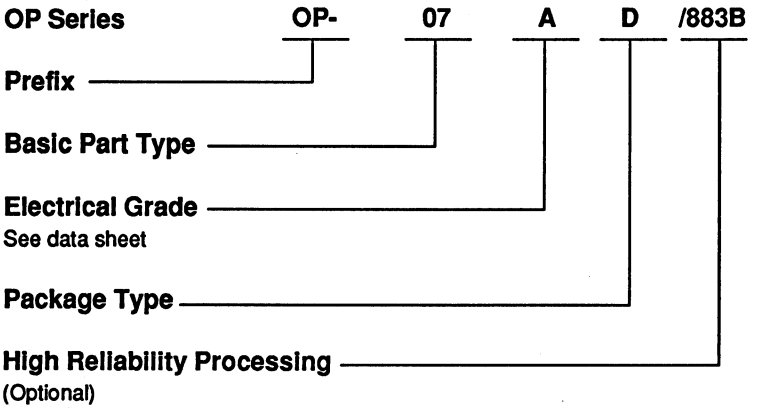
65-6401


LM/LP Series
LM
124
A
D
/883B
Prefix: LM/LP
Basic Part Type &
Temperature Range
First digit denotes temperature range*
1 = Military, -55°C to +125°C
3 = Commercial, 0°C to +70°C
Electrical Grade
See data sheet
Package Type
High Reliability Processing
(Optional)
*Except LM1851 operational temperature range = -40°C to +70°C
65-6402

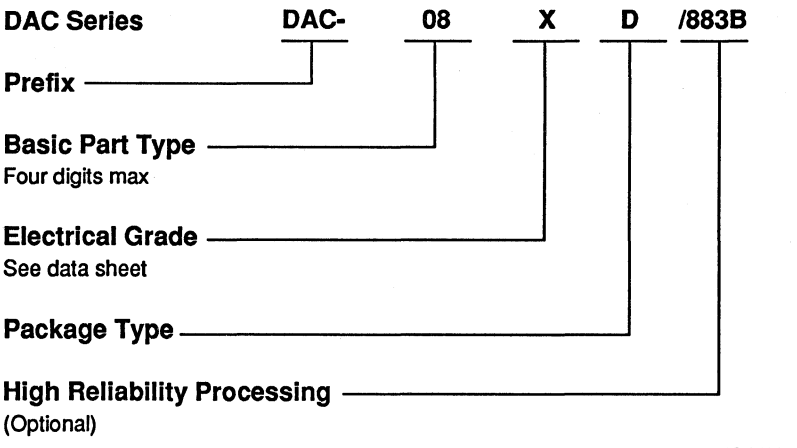

LH/LT Series
LT-
1001
A
D
/883B
Prefix: LH/LT
Basic Part Type
Four digits max
Electrical Grade
See data sheet
Package Type
High Reliability Processing
(Optional)
65-6403



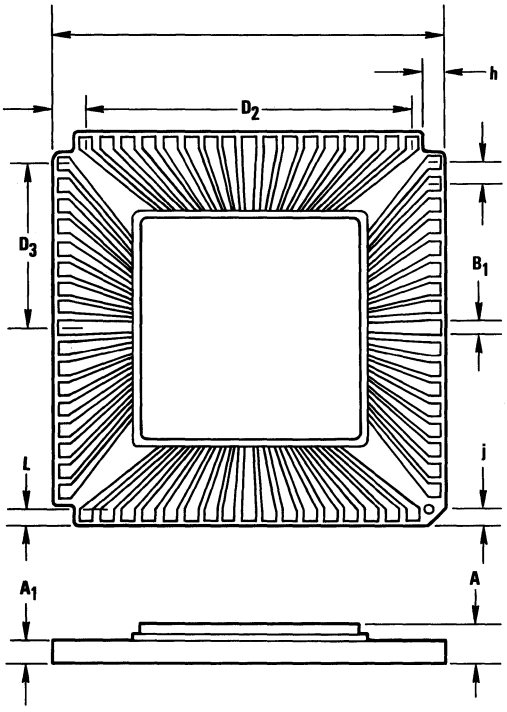
65-6404



65-6405


DAC Series
DAC-
08
X
D
/883B
Prefix
Basic Part Type
Four digits max
Electrical Grade
See data sheet
Package Type
High Reliability Processing
(Optional)
65-6406

A1 68-Lead Hermetic Ceramic Chip Carrier JEDEC Type A

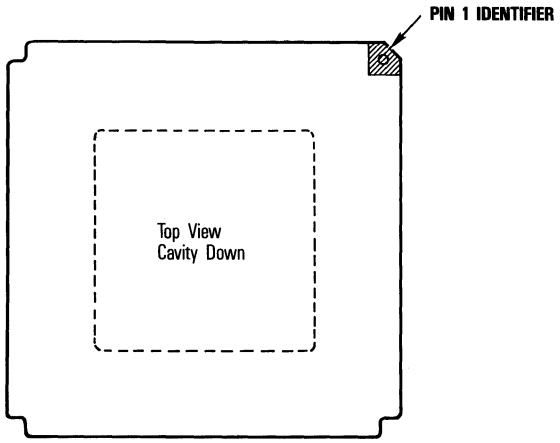


Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.075 (1.90)	.110 (2.79)	
A_1	.050 (1.27)	.070 (1.78)	
B_1	.033 (0.84)	.039 (0.99)	
D	.940 (23.88)	.960 (24.38)	Note 3
D_1			.075 (1.90) Ref.
D_2			.800 (20.32) Basic
D_3			.400 (10.16) Ref.
e			.050 (1.27) Basic
h			.050 (1.27) Ref.
j			.040 (1.02) Ref.
L	.040 (1.02)	.055 (1.40)	
N			68, Note 4
ND			17, Note 5

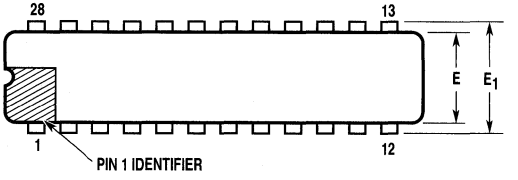
Ref. 90X00181

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.



B2 24-Lead Ceramic Dual In-Line Package

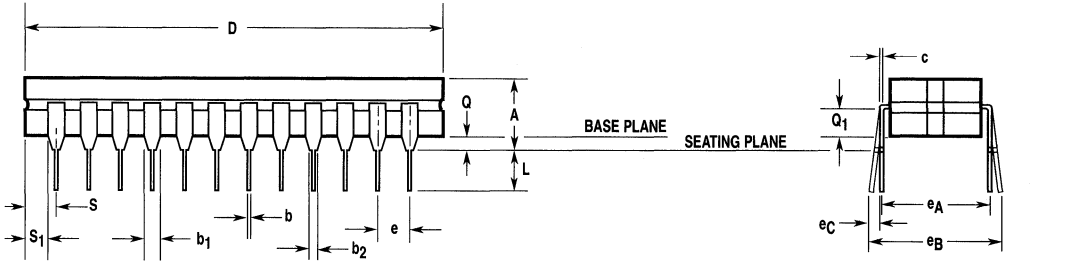
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.070 (1.78)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	1.235 (31.37)	1.280 (32.51)	
E	.280 (7.11)	.305 (7.75)	
E_1	.300 (7.62)	.320 (8.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			24, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181



20102A

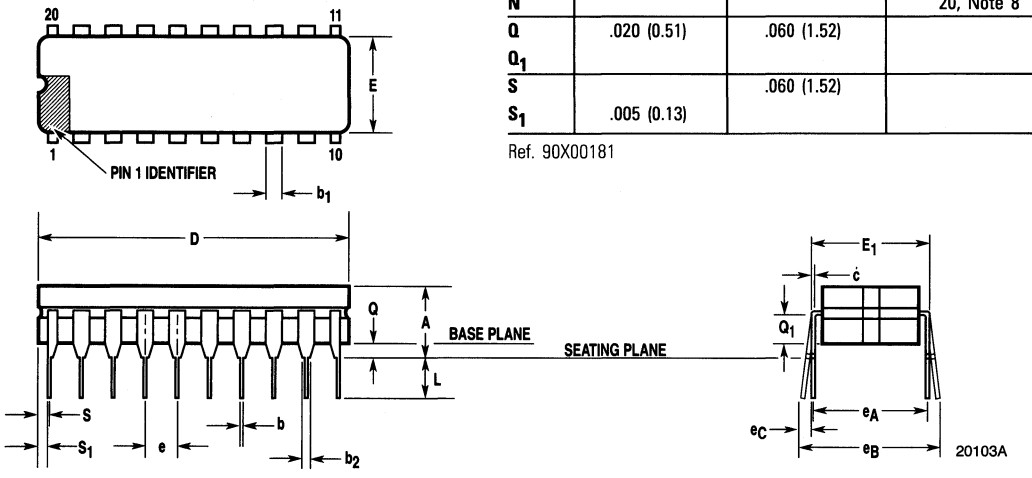
B3 20-Lead Ceramic Dual In-Line Package

Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.150 (3.81)	.200 (5.08)	
b	.015 (0.38)	.021 (0.53)	
b_1	.050 (1.27)	.060 (1.52)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.012 (0.31)	
D		.985 (25.02)	
E	.220 (5.59)	.310 (7.87)	
E_1	.290 (7.37)	.320 (8.13)	
e	.090 (2.29)	.110 (2.79)	
e_A			.300 (7.62) Basic
e_B	.310 (7.78)	.410 (10.41)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			20, Note 8
Q	.020 (0.51)	.060 (1.52)	
Q_1			
S		.060 (1.52)	
S_1	.005 (0.13)		

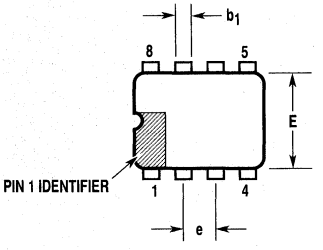
Ref. 90X00181

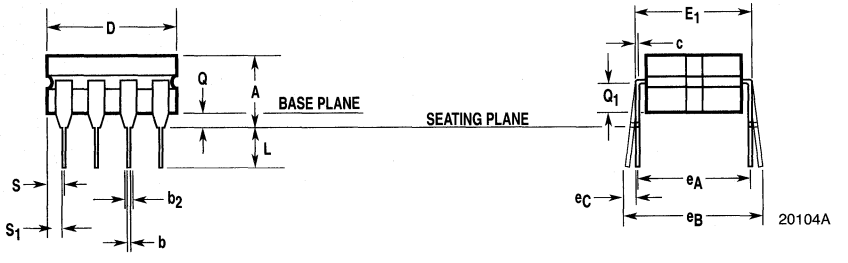
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.



B4 8-Lead Dual In-Line Package

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N=lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.





Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.150 (3.81)	.200 (5.08)	
b	.015 (0.38)	.021 (0.53)	
b_1	.030 (0.76)	.070 (1.78)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.012 (0.31)	
D		.400 (10.16)	
E	.220 (5.56)	.291 (7.39)	
E_1	.290 (7.37)	.320 (8.13)	
e	.090 (2.29)	.110 (2.79)	
e_A			.300 (7.62) Basic
e_B		.310 (7.78)	.410 (10.41)
e_C			
L	.125 (3.17)	.200 (5.08)	
N			8, Note 8
Q	.020 (0.51)	.060 (1.52)	
Q_1			
S		.055 (1.40)	
S_1	.015 (0.38)		

Ref. 90X00181

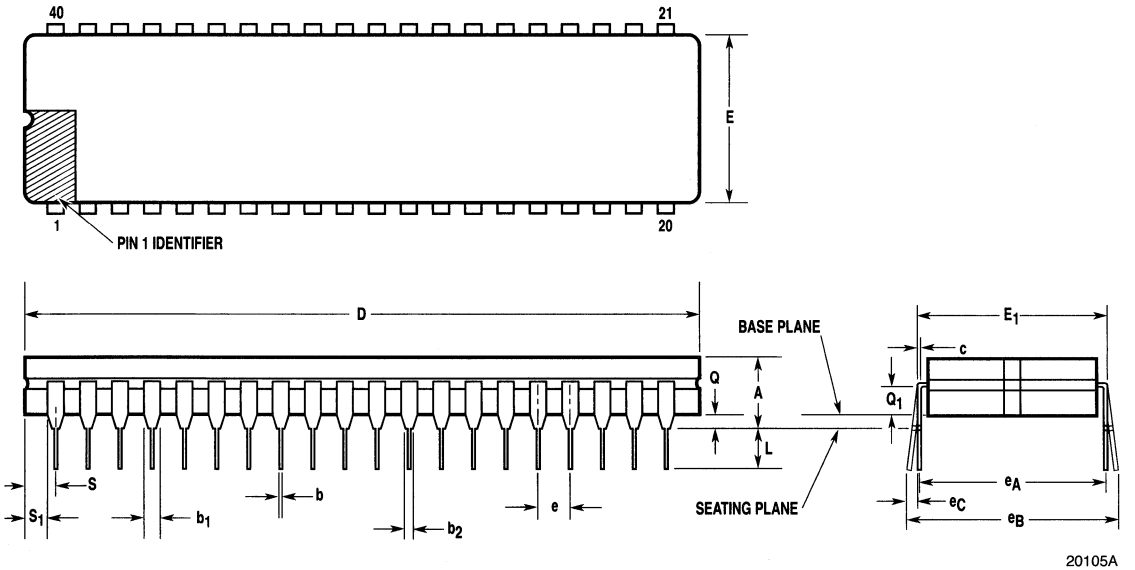
B5 40-Lead Ceramic Dual In-Line Package

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.225 (5.72)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.065 (1.65)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	2.030 (51.56)	2.096 (53.24)	
E	.510 (12.95)	.600 (15.24)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			40, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

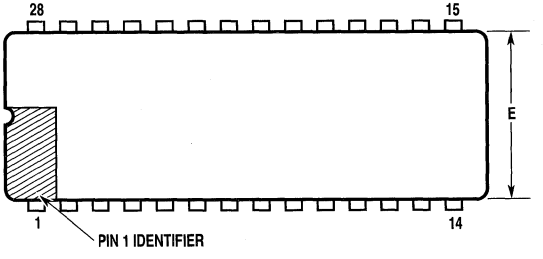
Ref. 90X00181



20105A

B6 28-Lead Ceramic Dual In-Line Package

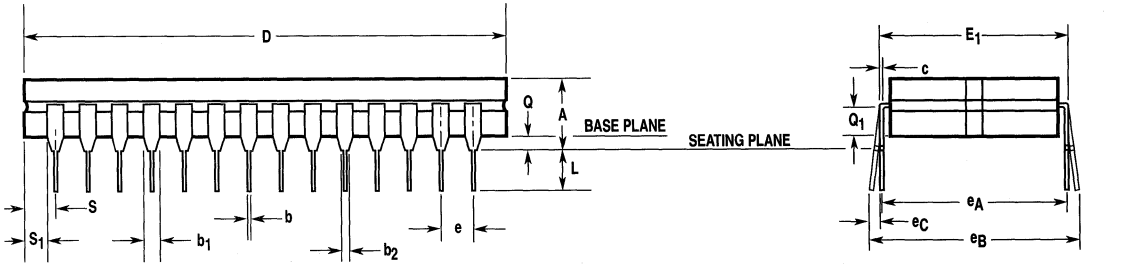
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N=lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.070 (1.78)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	1.435 (36.45)	1.480 (37.59)	
E	.500 (12.70)	.600 (15.24)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			28, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181



20106A

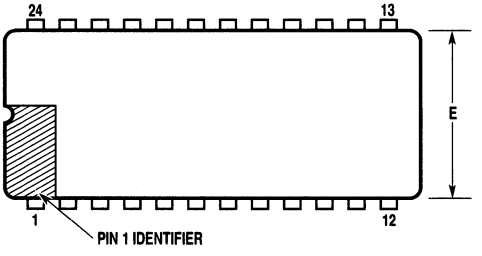
B7 24-Lead Ceramic Dual In-Line Package

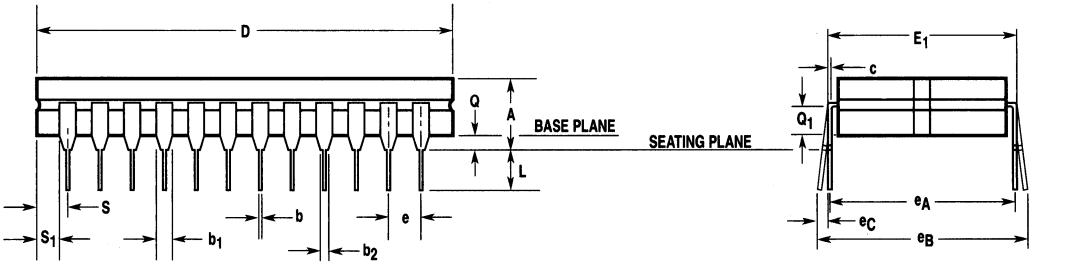
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N=lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.070 (1.78)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	1.235 (31.40)	1.280 (32.51)	
E	.510 (12.95)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			24, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181





20107A

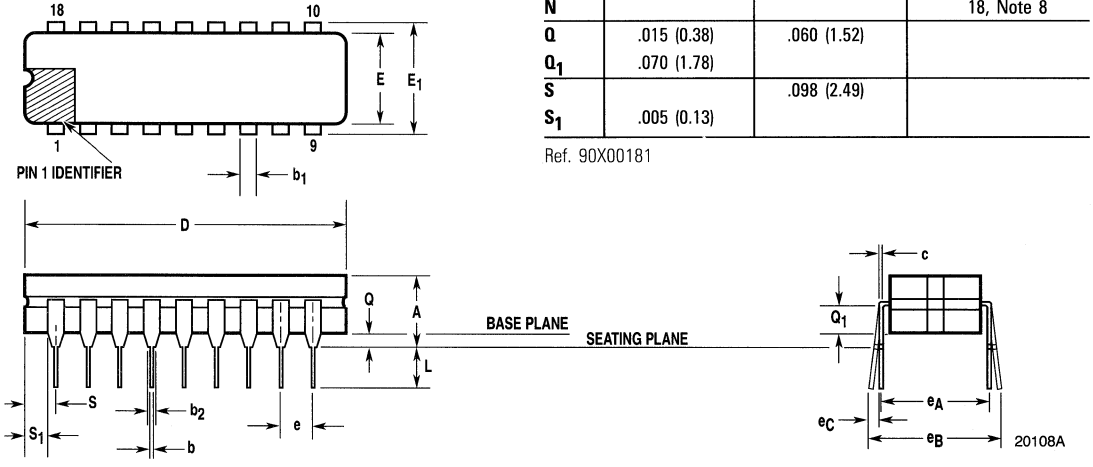
B8 18-Lead Ceramic Dual In-Line Package

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N=lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.065 (1.65)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	.875 (22.22)	.920 (23.37)	
E	.280 (7.11)	.305 (7.75)	
E_1	.290 (7.37)	.320 (8.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			18, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181



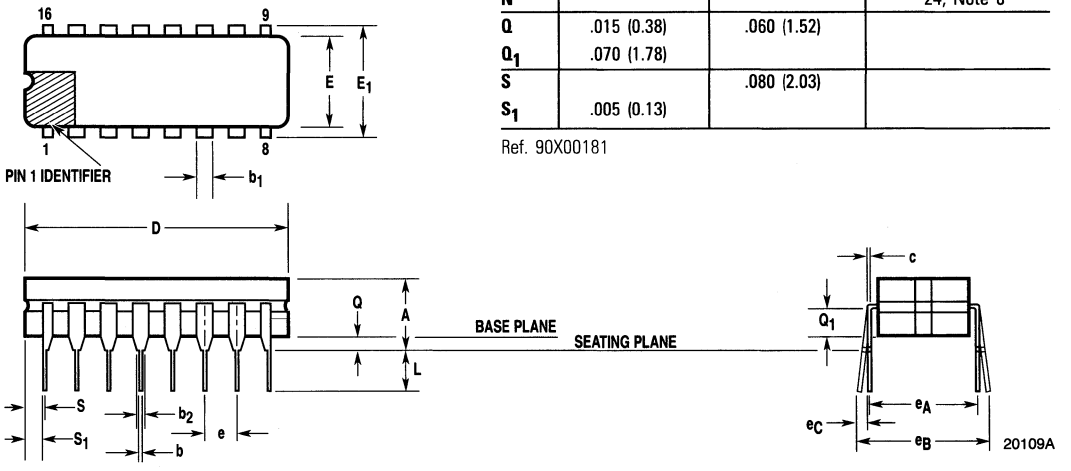
B9 16-Lead Ceramic Dual In-Line Package

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.

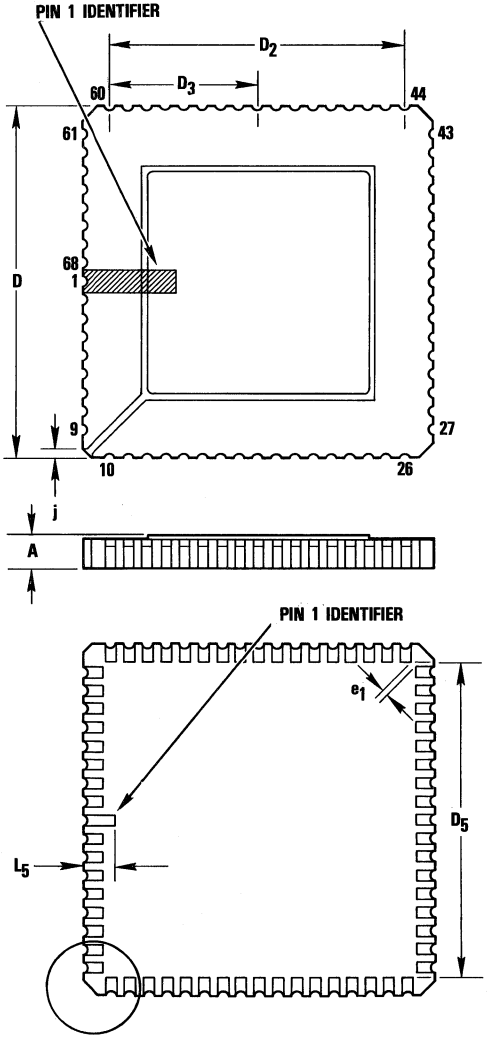
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.065 (1.65)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	.750 (19.05)	.820 (20.83)	
E	.240 (7.11)	.305 (7.75)	
E_1	.290 (7.37)	.320 (5.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			24, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.080 (2.03)	
S_1	.005 (0.13)		

Ref. 90X00181



C1 68-Contact Hermetic Ceramic Chip Carrier

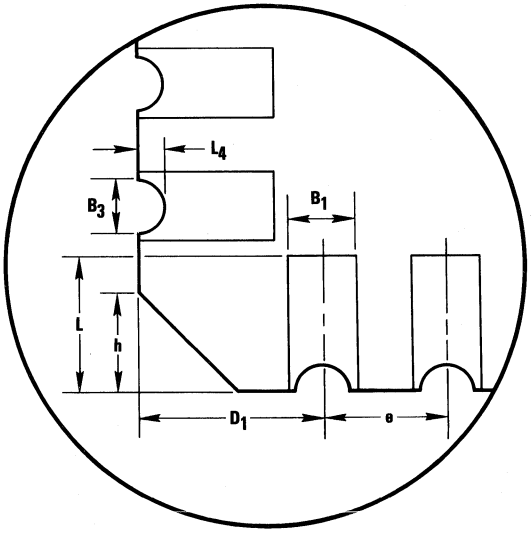


Dimensions

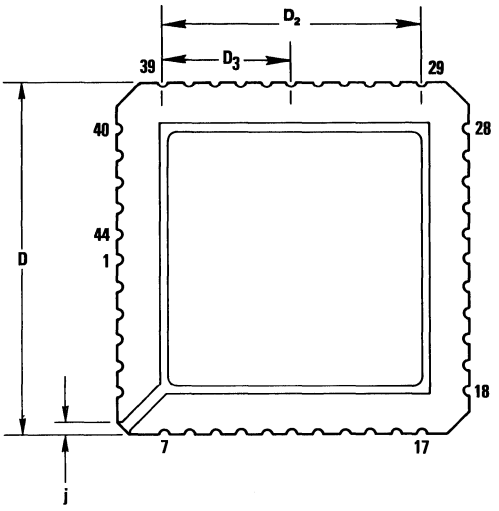
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.082 (2.08)	.110 (2.79)	
B_1	.022 (0.56)	.028 (0.71)	
B_3	.006 (0.15)	.022 (0.56)	
D	.938 (23.82)	.962 (24.43)	
D_1			.075 (1.90) Ref.
D_2			.800 (20.32) Basic
D_3			.400 (10.16) Basic
D_5			.850 (21.59) Ref.
e			.050 (1.27) Basic
e_1	.015 (0.38)		
h			.040 (1.02) Ref.
j			.020 (0.51) Ref.
L	.045 (1.14)	.055 (1.40)	
L_4	.003 (0.08)	.015 (0.38)	
L_5	.075 (1.91)	.095 (2.41)	
N			68, Note 4
ND			17, Note 5

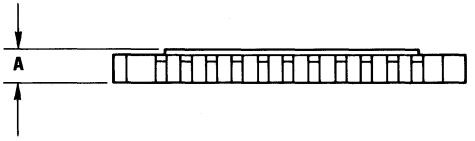
Ref. 90X00181

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.



C2 44-Contact Hermetic Ceramic Chip Carrier



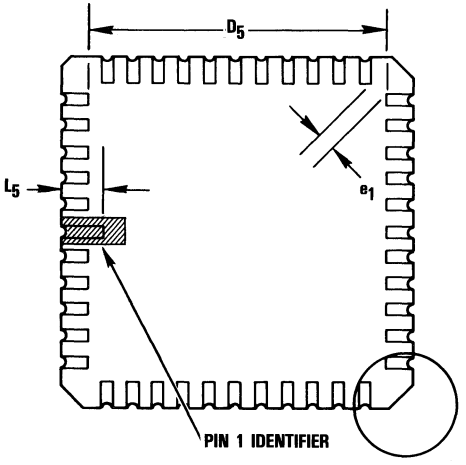


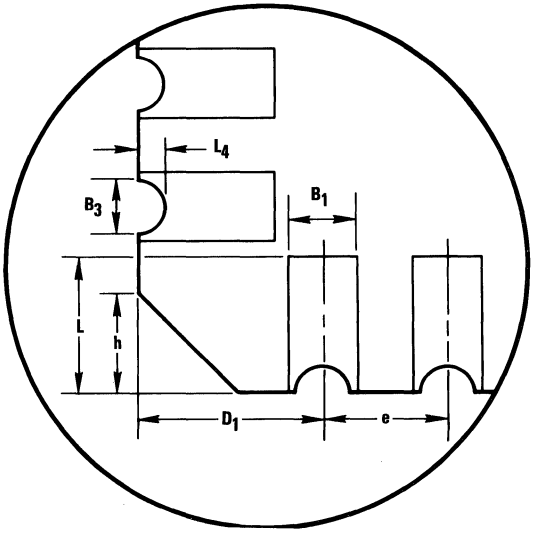
Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.064 (1.62)	.110 (2.79)	
B_1	.022 (0.56)	.028 (0.71)	
B_3	.006 (0.15)	.022 (0.56)	
D	.640 (16.26)	.660 (16.76)	
D_1			.075 (1.90) Ref.
D_2			.500 (6.35) Basic
D_3			.250 (6.35) Basic
D_5			.550 (13.97) Ref.
e			.050 (1.27) Basic
e_1	.015 (0.38)		
h			.040 (1.02) Ref.
j			.020 (0.51) Ref.
L	.045 (1.14)	.055 (1.40)	
L_4	.003 (0.08)	.015 (0.38)	
L_5	.075 (1.91)	.095 (2.41)	
N			44, Note 4
ND			11, Note 5

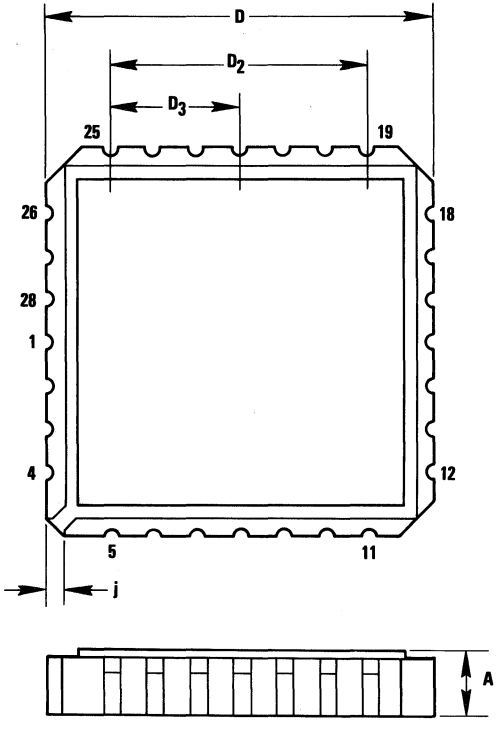
Ref. 90X00181

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.





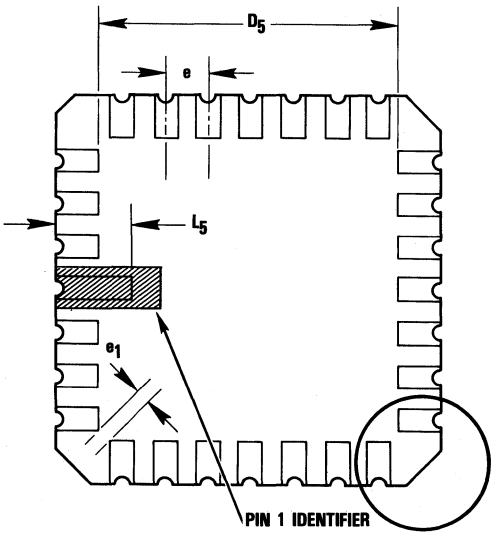
C3 28-Contact Hermetic Ceramic Chip Carrier

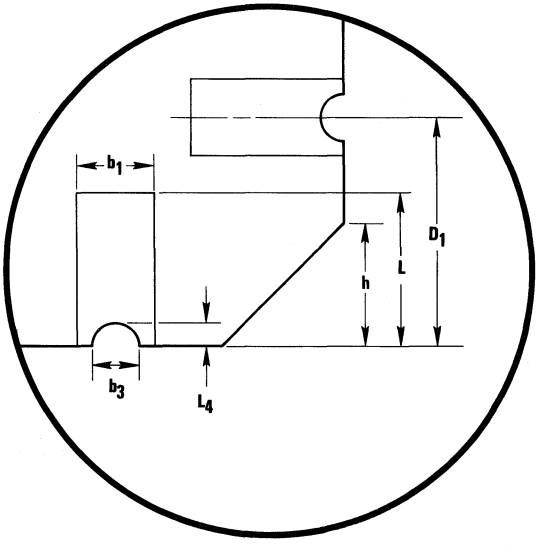


Sym	Inches (Millimeters) Min	Max	Notes
A	.064 (1.62)	.100 (2.54)	
B_1	.022 (0.56)	.028 (0.71)	
B_3	.006 (0.15)	.022 (0.56)	
D	.442 (11.23)	.460 (11.68)	
D_1			.075 (1.90) Ref.
D_2			.300 (7.62) Basic
D_3			.150 (3.81) Basic
D_5			.350 (8.89) Ref.
e			.050 (1.27) Basic
e_1	.015 (0.38)		
h			.040 (1.02) Ref.
j			.020 (0.51) Ref.
L	.045 (1.14)	.055 (1.40)	
L_4	.003 (0.08)	.015 (0.38)	
L_5	.075 (1.91)	.095 (2.41)	
N			28, Note 4
ND			7, Note 5

Ref. 90X00181

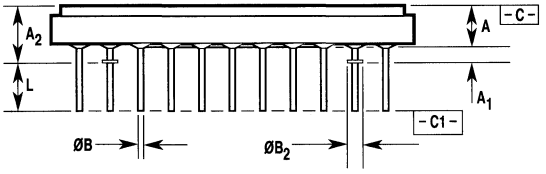
Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.





G0 68 Pin Grid Array
Cavity Down with Flat Heat Sink

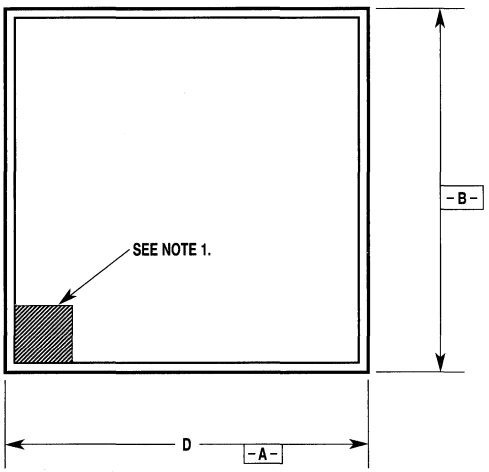
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Dimension M: defines matrix size.
3. Dimension N: defines pin count.
4. Controlling dimension: inch.
5. Optional (TRW option) index pin.

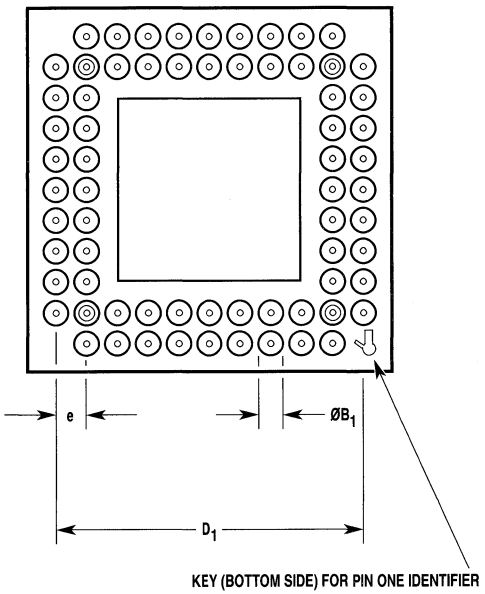


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.120 (3.05)	.185 (4.70)	
A_1	.025 (0.63)	.060 (1.52)	
A_2	.150 (3.81)	.240 (6.10)	
ϕB	.017 (0.43)	.020 (0.51)	
ϕB_1		.080 (2.03)	
ϕB_2			.050 (1.27) Nominal
D	1.140 (28.96)	1.180 (29.97)	
D_1			1.000 (25.40) Basic
e			.100 (2.54) Basic
L	.120 (3.05)	.140 (3.56)	
M			11, Note 2
N			68, Note 3

Ref. 90X00181

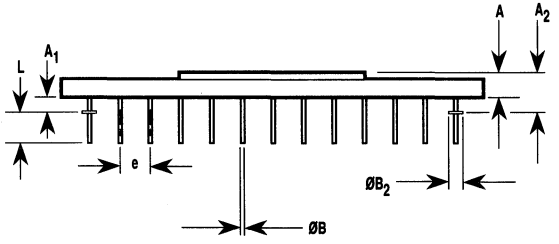




20125A

G5 89 Pin Grid Array

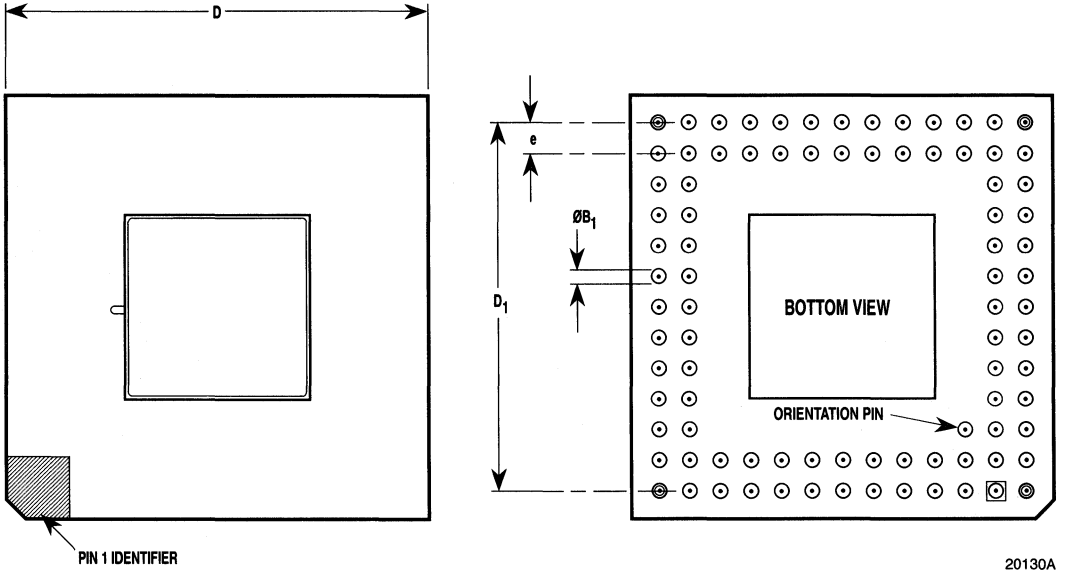
Notes: ..1. Pin one identifier shall be within shaded area shown.
2. Dimension M: defines matrix size.
3. Dimension N: defines pin count.
4. Controlling dimension: inch.
5. Optional (TRW option) index pin.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.125 (3.18)	
A_1	.040 (1.02)	.060 (1.52)	
A_2	.115 (2.92)	.190 (4.83)	
ϕB	.017 (0.43)	.020 (0.51)	
ϕB_1		.080 (2.03)	
ϕB_2			.050 (1.27) Nominal
D	1.340 (34.04)	1.380 (35.05)	
D_1			1.200 (30.48) Basic
e			.100 (2.54) Basic
L	.120 (3.05)	.150 (3.81)	
M			13, Note 2
N			88, Note 3

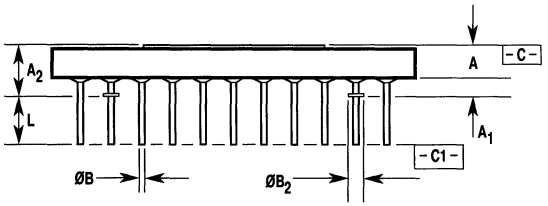
Ref. 90X00181



20130A

G8 68 Pin Grid Array

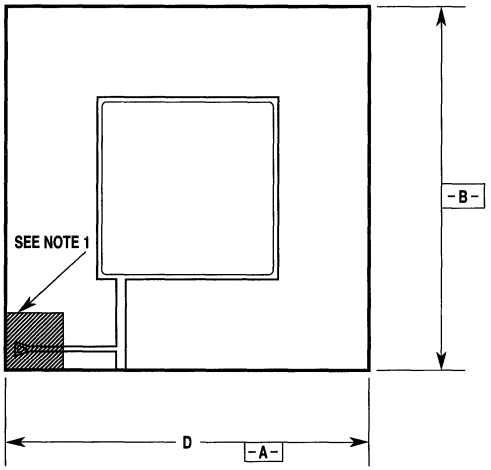
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Dimension M: defines matrix size.
3. Dimension N: defines pin count.
4. Controlling dimension: inch.
5. Optional (TRW option) index pin.

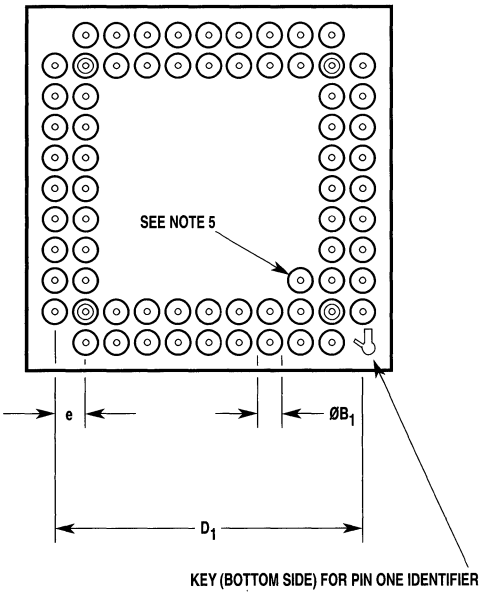


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.125 (3.18)	
A_1	.040 (1.02)	.060 (1.52)	
A_2	.115 (2.92)	.190 (4.83)	
ϕB	.017 (0.43)	.020 (0.51)	
ϕB_1		.080 (2.03)	
ϕB_2			.050 (1.27) Nominal
D	1.140 (28.96)	1.180 (29.97)	
D_1			1.00 (25.4) Basic
e			.100 (2.54) Basic
L	.120 (3.05)	.150 (3.81)	
M			11, Note 2
N			68, Note 3

Ref. 90X00181

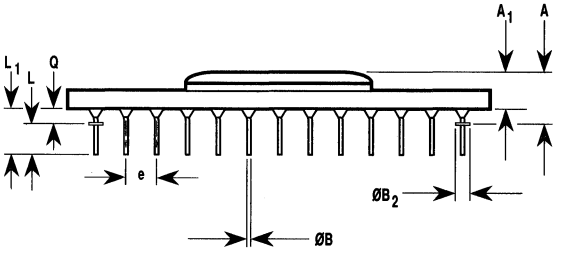




20133A

H5 121 Printed Circuit Board Pin Grid Array
Cavity Up

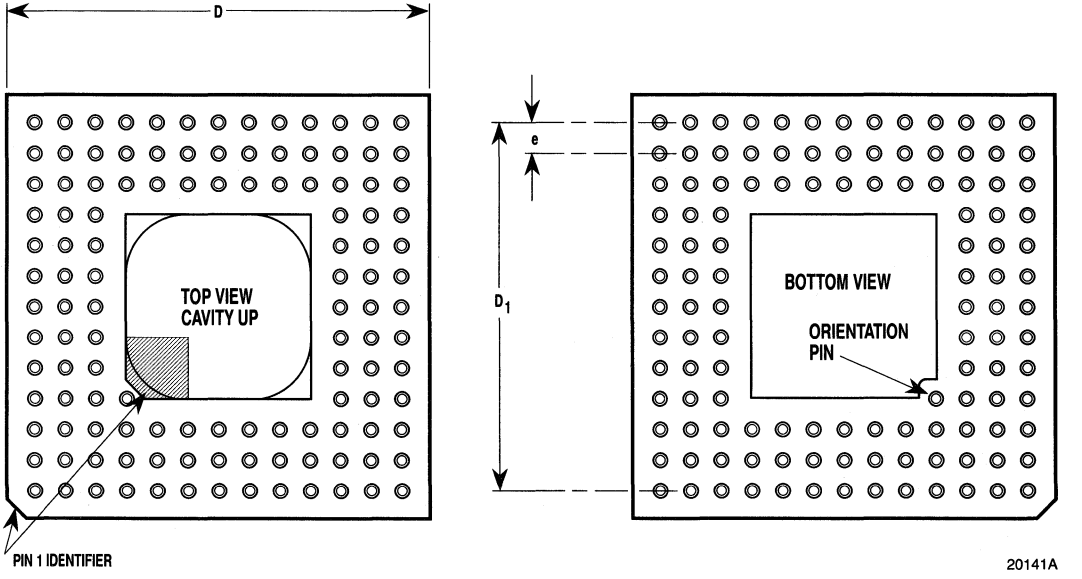
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension M: defines matrix size.
4. Dimension N: defines the maximum possible number of pins. Orientation pin is at supplier's option.
5. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A	.125 (3.17)	.215 (5.46)	
A_1	.080 (2.03)	.160 (4.06)	
ϕB	.016 (0.41)	.020 (0.51)	Note 2
ϕB_2			.050 (1.27) Nominal, Note 2
D	1.340 (34.04)	1.380 (35.05)	Square
D_1			1.200 (30.48) Basic
e			.100 (2.54) Basic
L	.110 (2.79)	.145 (3.68)	
L_1	.170 (4.32)	.190 (4.83)	
M			13, Note 3
N			120, Note 4
Q	.040 (1.02)	.060 (1.52)	

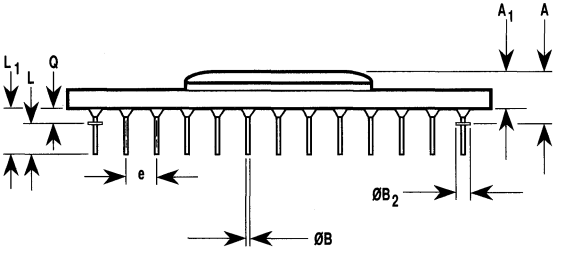
Ref. 90X00181



20141A

H7 89 Printed Circuit Board Pin Grid Array
Cavity Up

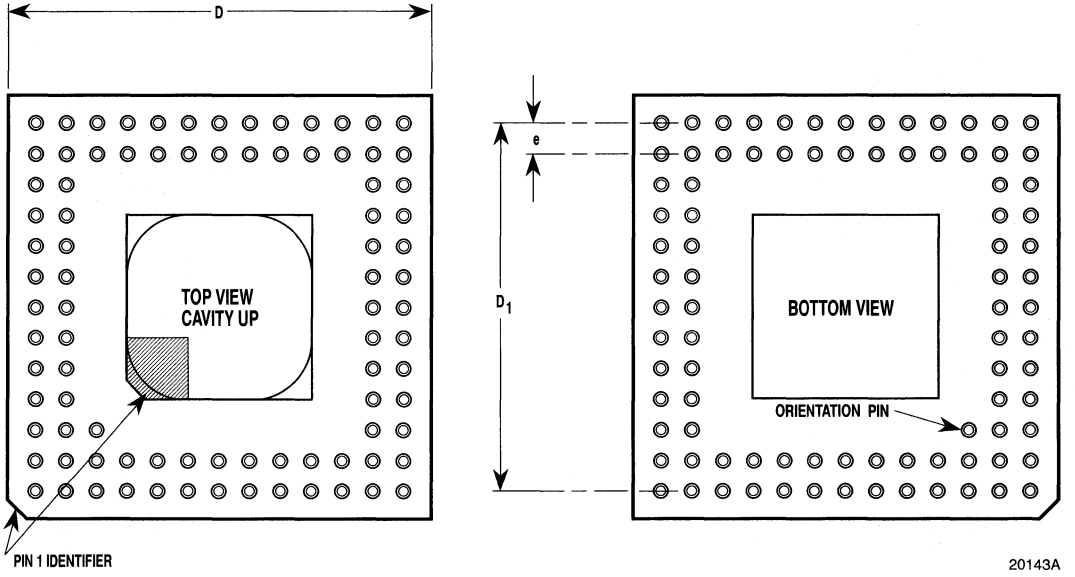
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension M: defines matrix size.
4. Dimension N: defines the maximum possible number of pins. Orientation pin is at supplier's option.
5. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.125 (3.17)	.215 (5.46)	
A_1	.080 (2.03)	.160 (4.06)	
ϕB	.016 (0.41)	.020 (0.51)	Note 2
ϕB_2			.050 (1.27) Nominal, Note 2
D	1.340 (34.04)	1.380 (35.05)	Square
D_1			1.200 (30.48) Basic
e			.100 (2.54) Basic
L	.110 (2.79)	.145 (3.68)	
L_1	.170 (4.32)	.190 (4.83)	
M			13, Note 3
N			88, Note 4
Q	.040 (1.02)	.060 (1.52)	

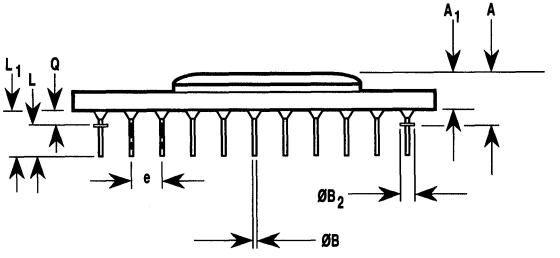
Ref. 90X00181



20143A

H8 69 Printed Circuit Board Pin Grid Array
Cavity Up

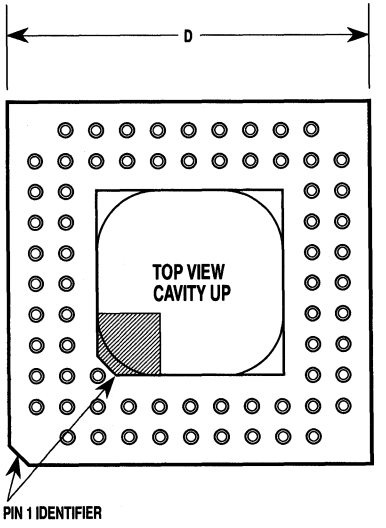
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension M: defines matrix size.
4. Dimension N: defines the maximum possible number of pins. Orientation pin is at supplier's option.
5. Controlling dimension: inch.

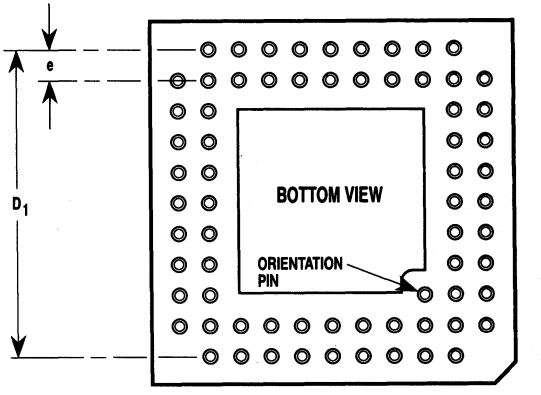


Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A	.125 (3.17)	.215 (5.46)	
A_1	.080 (2.03)	.160 (4.06)	
ϕB	.016 (0.41)	.020 (0.51)	Note 2
ϕB_2			.050 (1.27) Nominal, Note 2
D	1.140 (28.96)	1.180 (29.97)	Square
D_1			1.000 (25.40) Basic
e			.100 (2.54) Basic
L	.110 (2.79)	.145 (3.68)	
L_1	.170 (4.32)	.190 (4.83)	
M			11, Note 3
N			68, Note 4
Q	.040 (1.02)	.060 (1.52)	

Ref. 90X00181

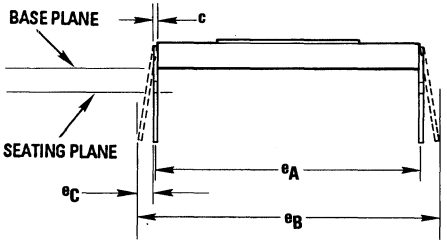




20144A

J0 64-Lead Hermetic Ceramic Dual In-Line Package

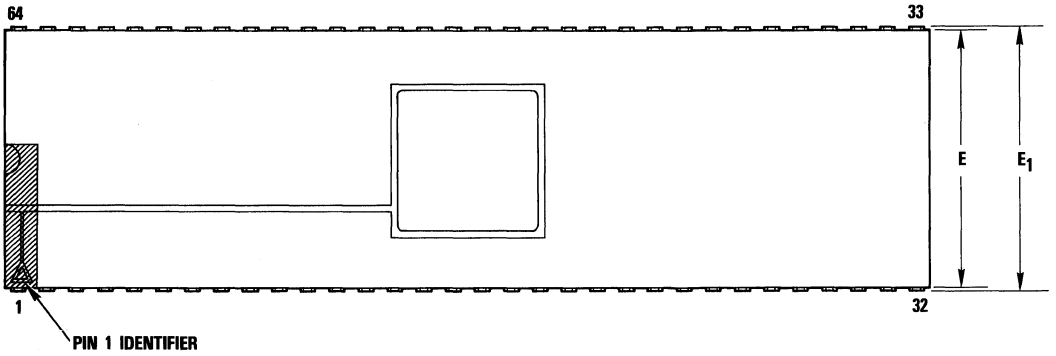
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1, E_3 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimensions E_3 and e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.

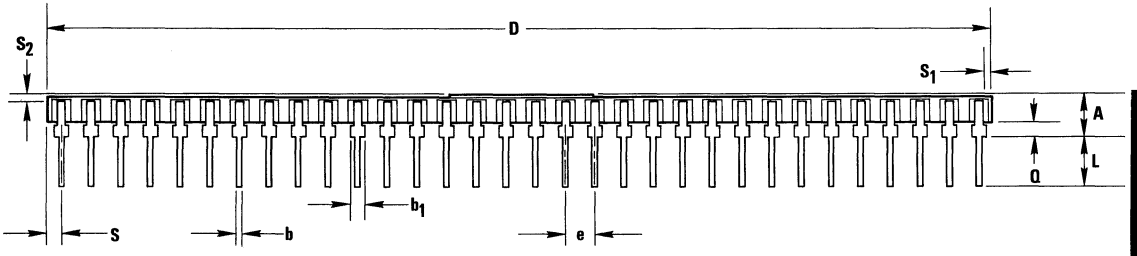


Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A	.120 (3.05)	.175 (4.44)	
b	.015 (0.38)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	3.170 (80.52)	3.240 (82.30)	
E	.880 (22.35)	.910 (23.11)	
E_1	.890 (22.61)	.930 (23.62)	
e			.100 (2.54) Basic
e_A			.900 (22.86) Basic
e_B		1.000 (25.40)	
e_C			
L	.125 (3.17)	.175 (4.44)	
N			64, Note 7
Q	.025 (0.63)	.065 (1.65)	
S		.100 (2.54)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

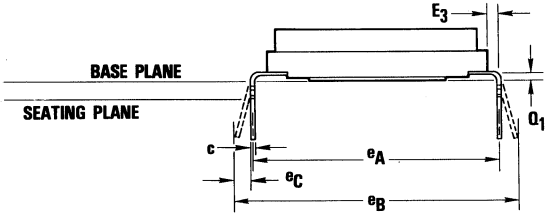
Ref. 90X00181





J1 64-Lead Hermetic Ceramic Dual In-Line Package Bottombraze with Heat Sink

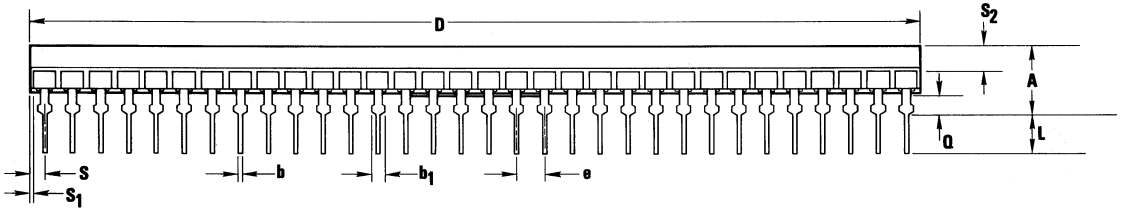
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1, E_3 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimensions E_3 and e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Controlling dimension: inch.
8. Dimension Q_1: measured from lead braze/ceramic interface.
9. Dimension N: defines pin count.

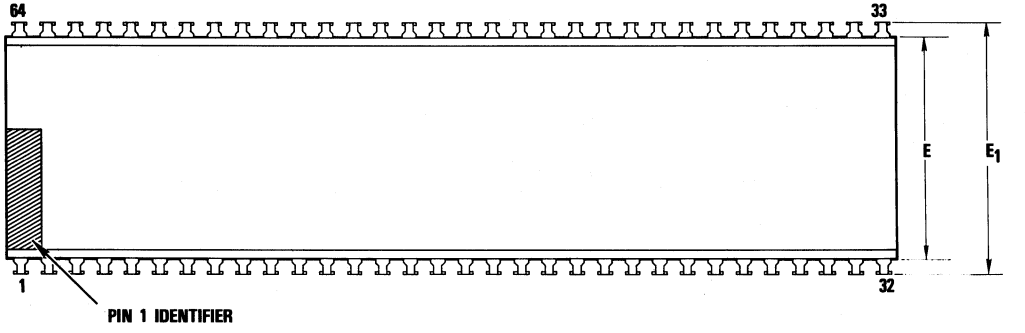


Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A	.190 (4.83)	.275 (6.99)	
b	.015 (0.38)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	3.170 (80.52)	3.240 (82.30)	
E	.790 (20.07)	.810 (20.57)	
E_1	.880 (22.35)	.930 (23.62)	
E_3	.025 (0.63)		
e			.100 (2.54) Basic
e_A			.900 (22.86) Basic
e_B		1.050 (26.67)	
e_C	.000 (0.00)		
L	.125 (3.17)	.175 (4.44)	
N			64, Note 9
Q	.050 (1.27)	.100 (2.54)	
Q_1	.026 (0.66)		
S		.100 (2.54)	
S_1	.005 (0.13)		
S_2	.060 (1.52)		

Ref. 90X00181





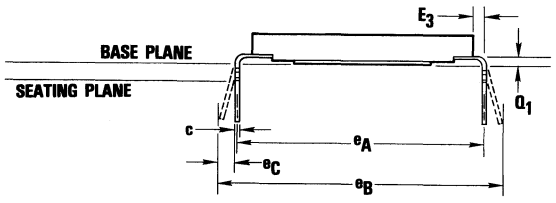
J3 64-Lead Hermetic Ceramic Dual In-Line Package Bottombraze

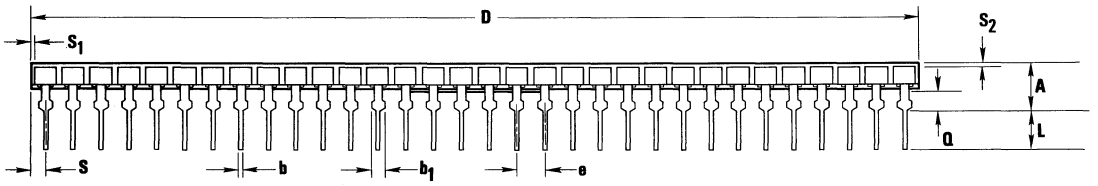
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1, E_3 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimensions E_3 and e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Controlling dimension: inch.
8. Dimension Q_1: measured from lead braze/ceramic interface.
9. Dimension N: defines pin count.

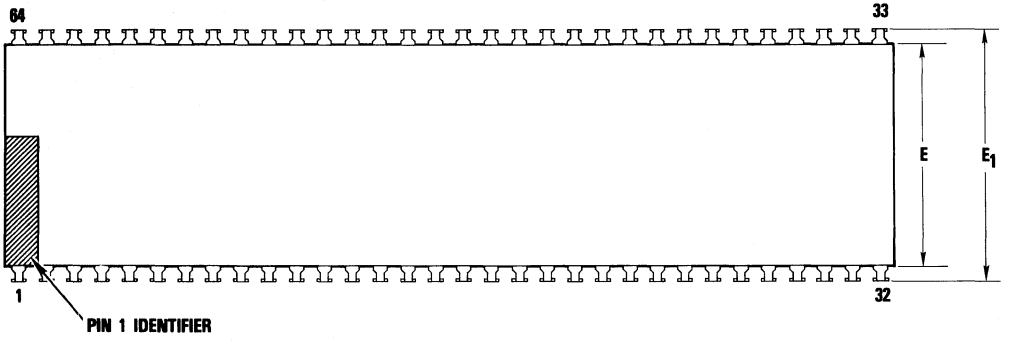
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.125 (3.17)	.200 (5.08)	
b	.015 (0.38)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	3.170 (80.52)	3.240 (82.30)	
E	.790 (20.07)	.810 (20.57)	
E_1	.880 (22.35)	.930 (23.62)	
E_3	.025 (0.63)		
e			.100 (2.54) Basic
e_A			.900 (22.86) Basic
e_B		1.050 (26.67)	
e_C			
L	.125 (3.17)	.175 (4.44)	
N			64, Note 9
Q	.050 (1.27)	.100 (2.54)	
Q_1	.026 (0.66)		
S		.100 (2.54)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181

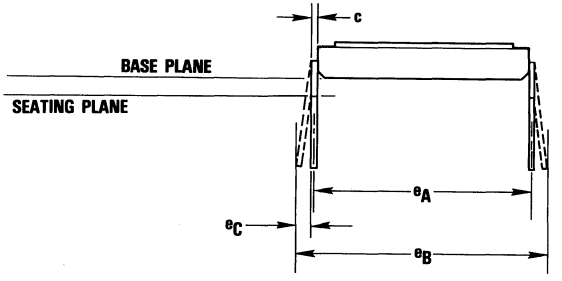






J4 48-Lead Hermetic Ceramic Dual In-Line Package

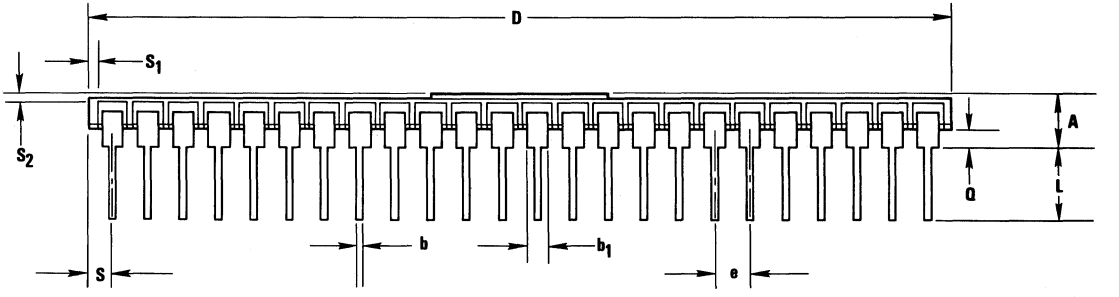
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N=leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.

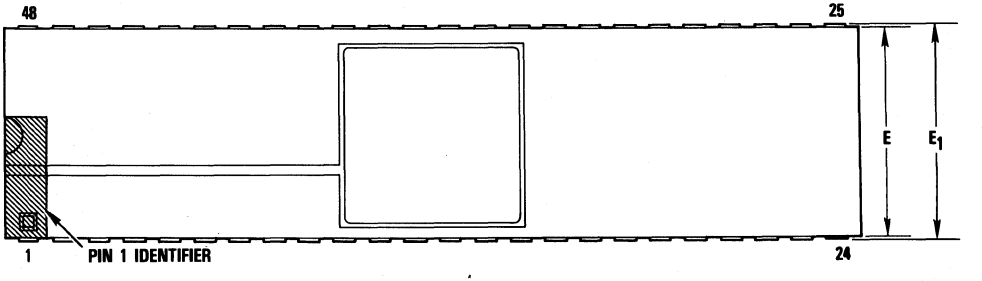


Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.120 (3.05)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	2.370 (60.20)	2.435 (61.85)	
E	.575 (14.60)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			48, Note 7
Q	.025 (0.63)	.060 (1.52)	
S		.100 (2.54)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181





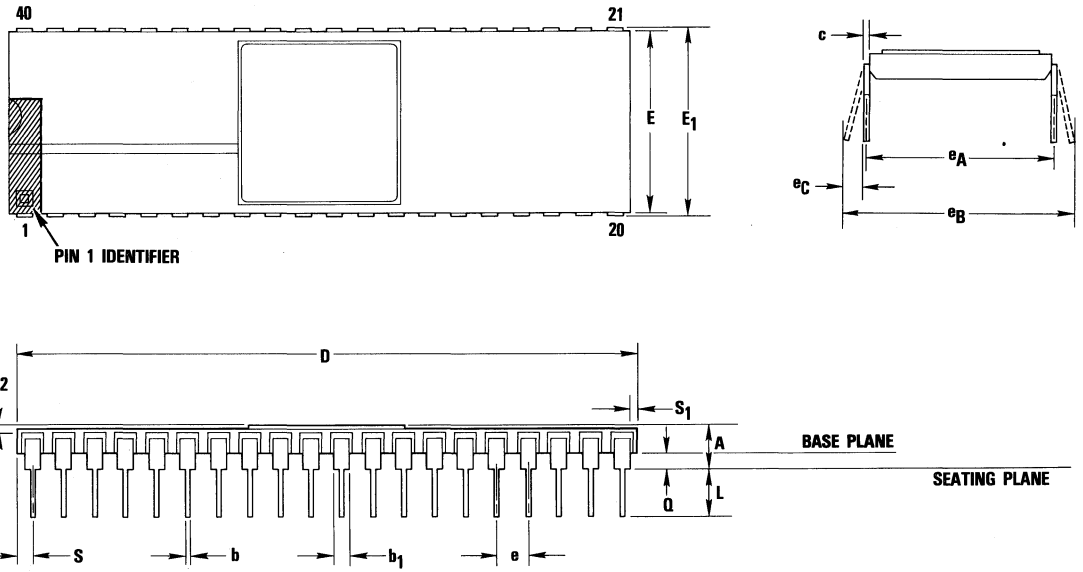
J5 40-Lead Hermetic Ceramic Dual In-Line Package

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.120 (3.05)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	1.970 (50.04)	2.030 (51.56)	
E	.575 (14.60)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			40, Note 7
Q	.025 (0.63)	.060 (1.52)	
S		.098 (2.49)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181



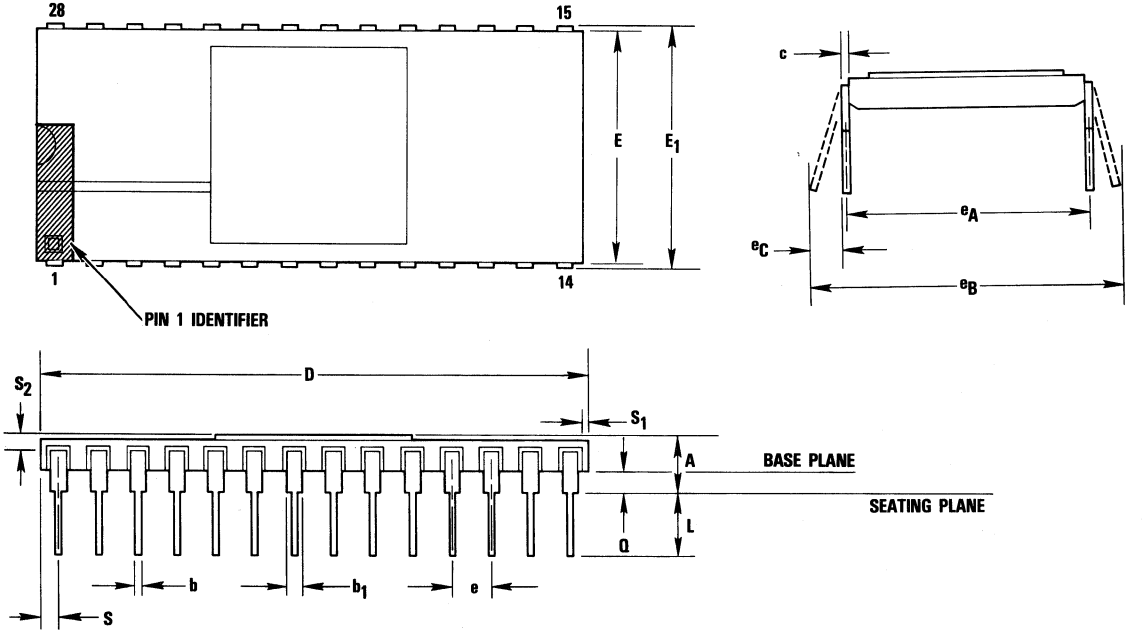
J6 28-Lead Hermetic Ceramic Dual In-Line Package

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.

Dimensions

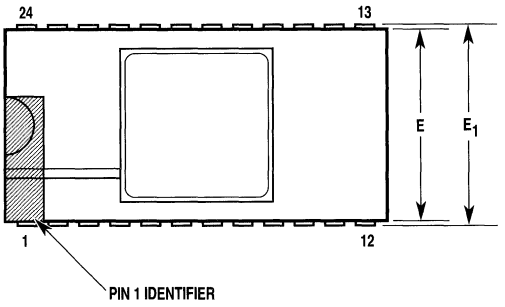
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.120 (3.05)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	1.380 (35.05)	1.420 (36.07)	
E	.575 (14.60)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			28, Note 7
Q	.025 (0.63)	.060 (1.52)	
S		.098 (2.49)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181



J7 24-Lead Hermetic Ceramic Dual In-Line Package

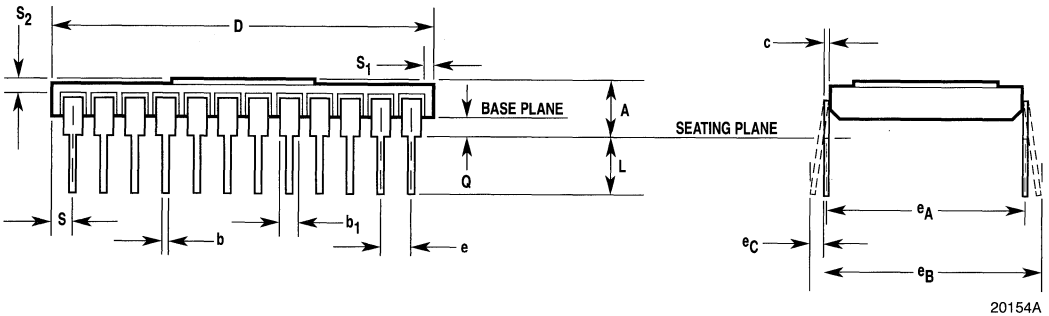
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.120 (3.05)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	1.180 (29.97)	1.220 (30.99)	
E	.575 (14.60)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			24, Note 7
Q	.025 (0.63)	.060 (1.52)	
S		.098 (2.49)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

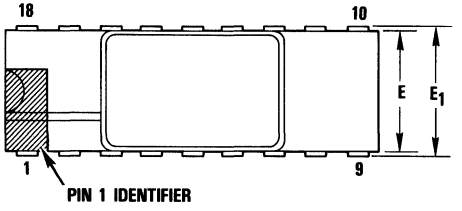
Ref. 90X00181



20154A

J8 18-Lead Hermetic Ceramic Dual In-Line Package

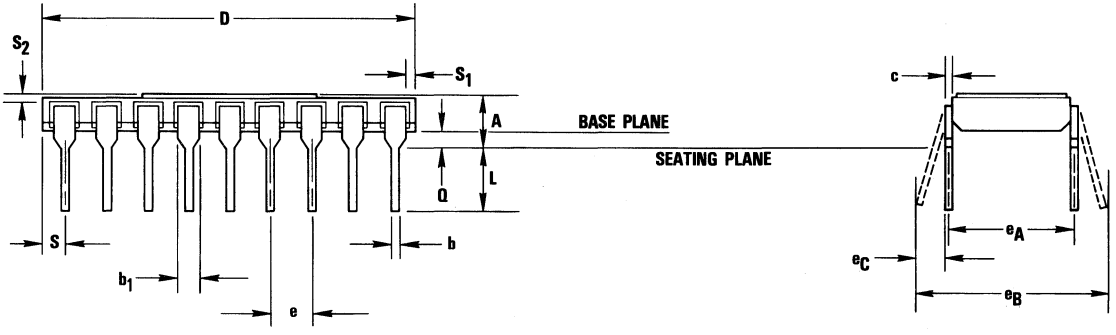
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.



Dimensions

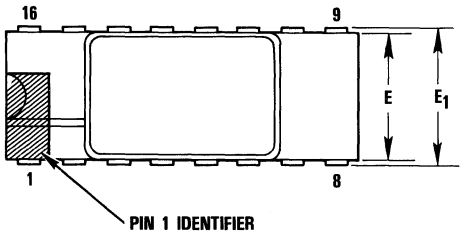
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.100 (2.54)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	.885 (22.48)	.915 (23.24)	
E	.285 (7.24)	.305 (7.75)	
E_1	.290 (7.37)	.320 (8.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			18, Note 7
Q	.015 (0.38)	.060 (1.52)	
S		.098 (2.49)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181



J9 16-Lead Hermetic Ceramic Dual In-Line Package

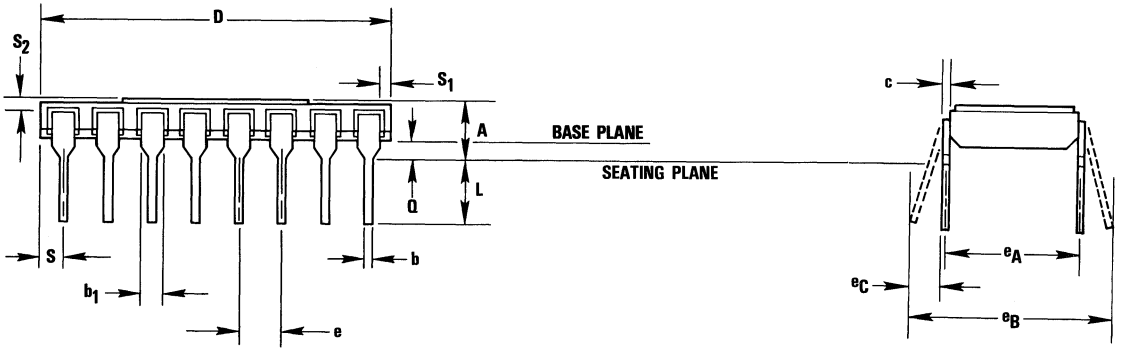
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.



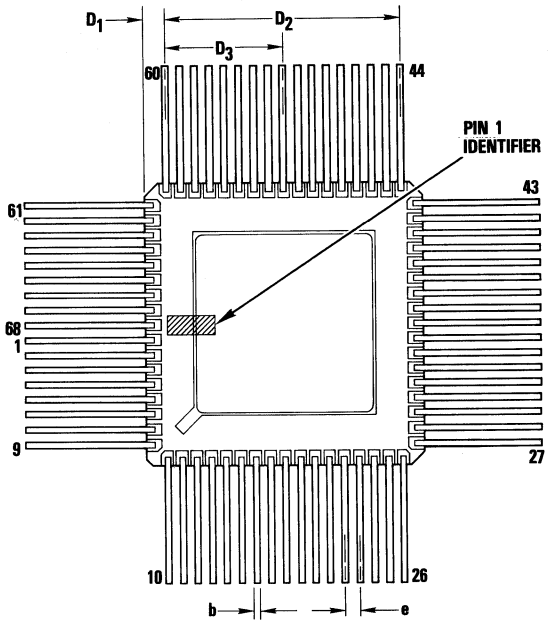
Dimensions

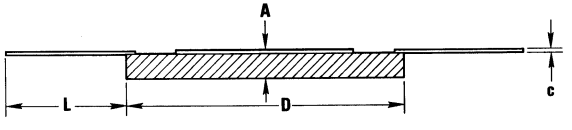
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.100 (2.54)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	.790 (20.07)	.810 (20.57)	
E	.285 (7.24)	.305 (7.75)	
E_1	.290 (7.37)	.320 (8.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			16, Note 7
Q	.015 (0.38)	.060 (1.52)	
S		.080 (2.03)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181



L1 68 Leaded Hermetic Ceramic Chip Carrier



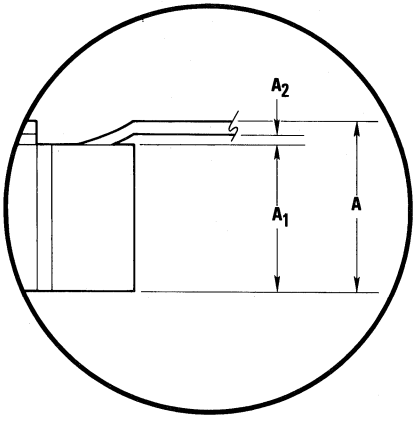


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.115 (2.92)	
A_1	.070 (1.78)	.100 (2.54)	
A_2	.005 (0.13)	.015 (0.38)	
b	.016 (0.41)	.022 (0.56)	
c	.009 (0.23)	.012 (0.30)	
D	.935 (23.75)	.970 (24.64)	
D_1			.075 (1.91) Ref.
D_2			.800 (20.32) Basic
D_3			.400 (10.16) Basic
e			.050 (1.27) Basic
L	.350 (8.98)	.400 (10.16)	
N			68, Note 4
ND			17, Note 5

Ref. 90X00181

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.



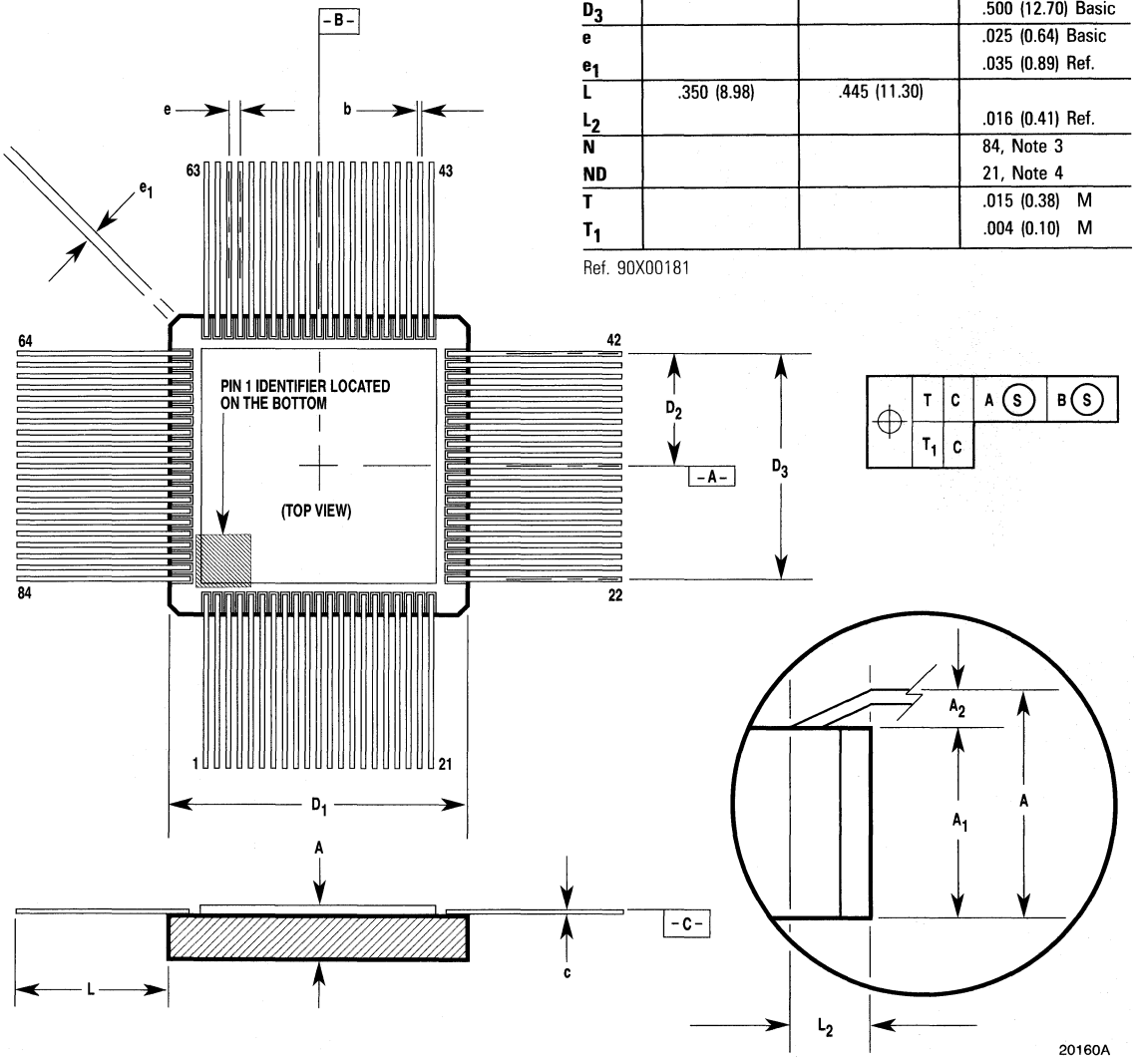
L3 84 Leaded Hermetic Ceramic Chip Carrier

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension D_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
3. Dimension N: number of terminals.
4. Dimension ND: number of terminals per package edge.
5. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.060 (1.52)	.100 (2.54)	
A_1	.055 (1.40)	.075 (1.91)	
A_2	.005 (0.13)	.025 (0.64)	
b	.008 (0.20)	.012 (0.30)	
c	.005 (0.13)	.009 (0.23)	
D_1	.640 (16.25)	.660 (16.76)	
D_2			.250 (6.35) Basic
D_3			.500 (12.70) Basic
e			.025 (0.64) Basic
e_1			.035 (0.89) Ref.
L	.350 (8.98)	.445 (11.30)	
L_2			.016 (0.41) Ref.
N			84, Note 3
ND			21, Note 4
T			.015 (0.38) M
T_1			.004 (0.10) M

Ref. 90X00181



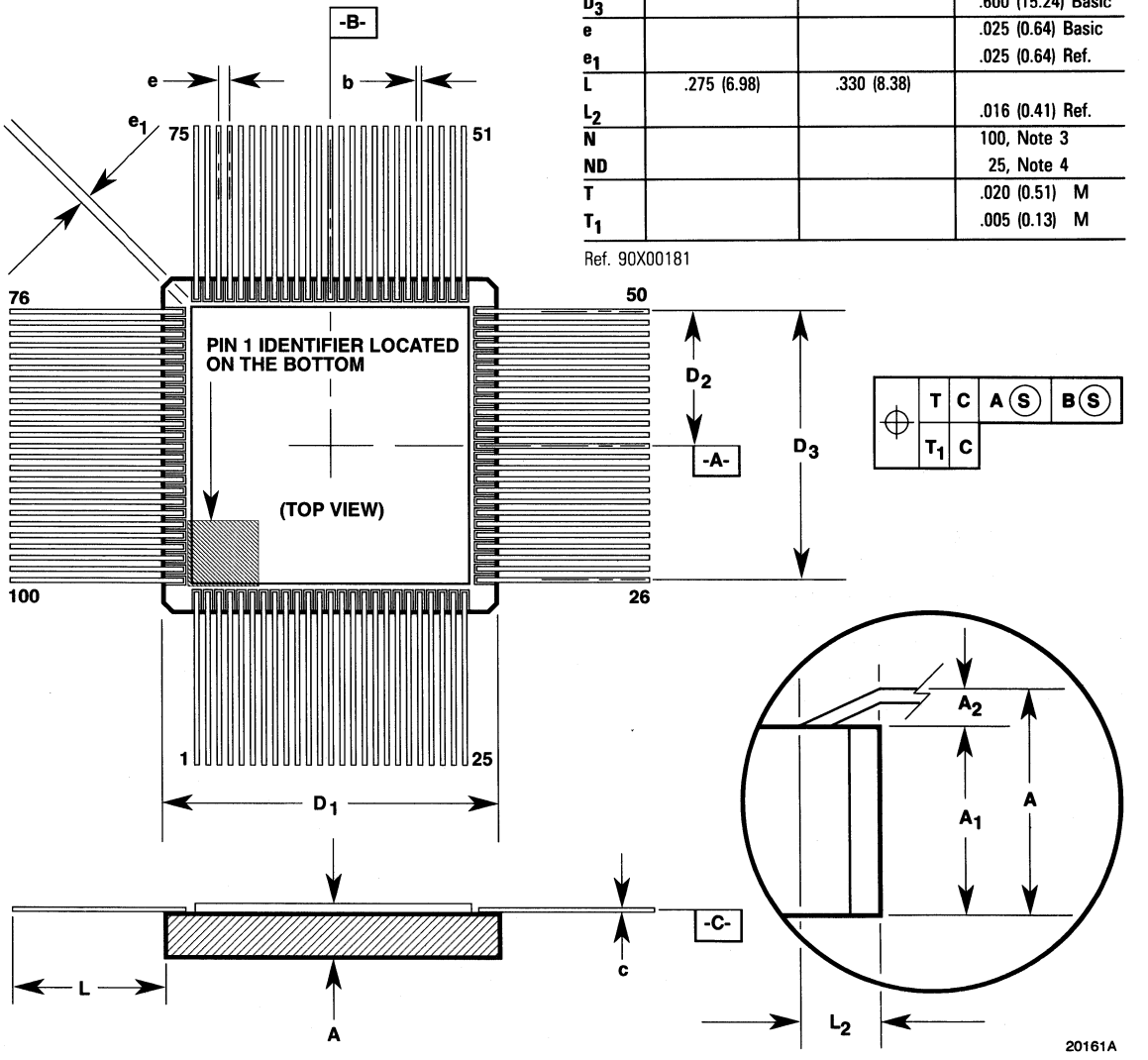
L4 100 Leaded Hermetic Ceramic Chip Carrier

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension D_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
3. Dimension N: number of terminals.
4. Dimension ND: number of terminals per package edge.
5. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.120 (3.05)	
A_1	.075 (1.91)	.095 (2.41)	
A_2	.005 (0.13)	.025 (0.64)	
b	.008 (0.20)	.012 (0.30)	
c	.005 (0.13)	.009 (0.23)	
D_1	.740 (18.80)	.760 (19.30)	
D_2			.300 (7.62) Basic
D_3			.600 (15.24) Basic
e			.025 (0.64) Basic
e_1			.025 (0.64) Ref.
L	.275 (6.98)	.330 (8.38)	
L_2			.016 (0.41) Ref.
N			100, Note 3
ND			25, Note 4
T			.020 (0.51) M
T_1			.005 (0.13) M

Ref. 90X00181



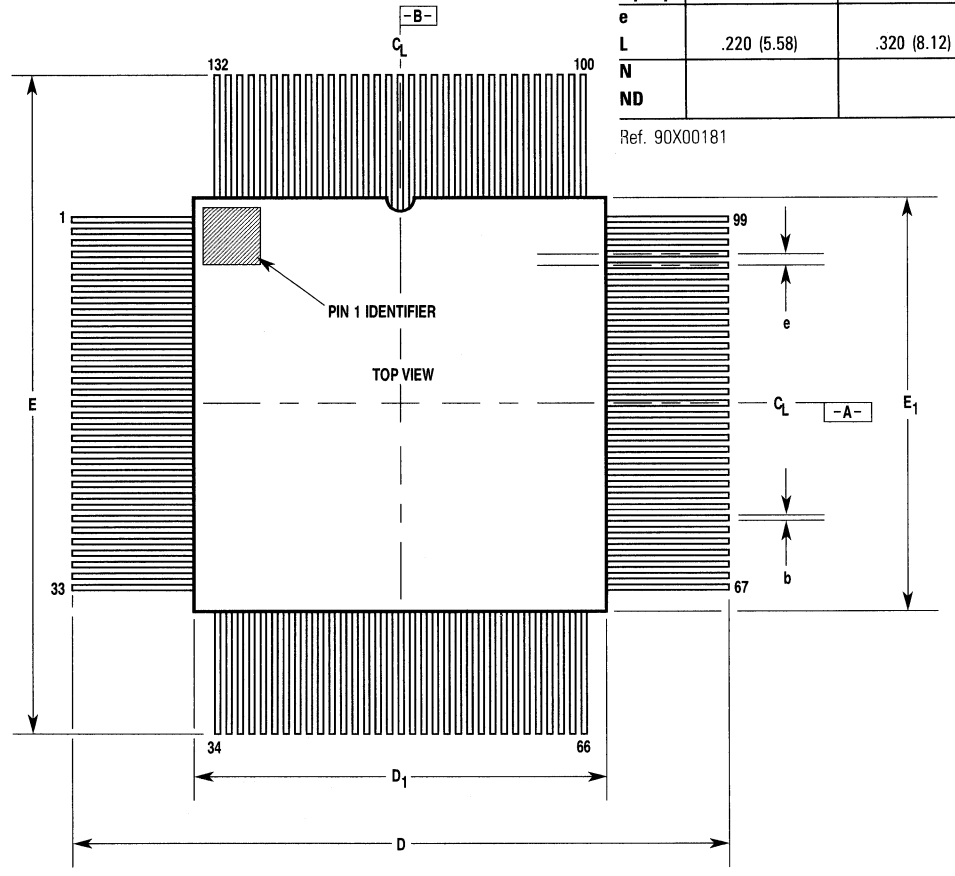
L5 132 Leaded Cerquad

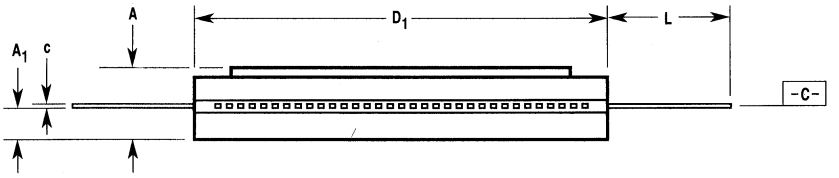
Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimensions D_1 and E_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
3. Dimension N: number of terminals.
4. Dimension ND: number of terminals per package edge.
5. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.114 (2.89)	.154 (3.91)	
A_1	.055 (1.40)	.075 (1.90)	
b	.008 (0.20)	.012 (0.30)	
c	.005 (0.13)	.009 (0.23)	
D, E			1.415 (35.94) Ref.
D_1, E_1	.860 (21.83)	.900 (22.84)	
e			.025 (0.64) Basic
L	.220 (5.58)	.320 (8.12)	
N			132, Note 3
ND			33, Note 4

Ref. 90X00181





20162A

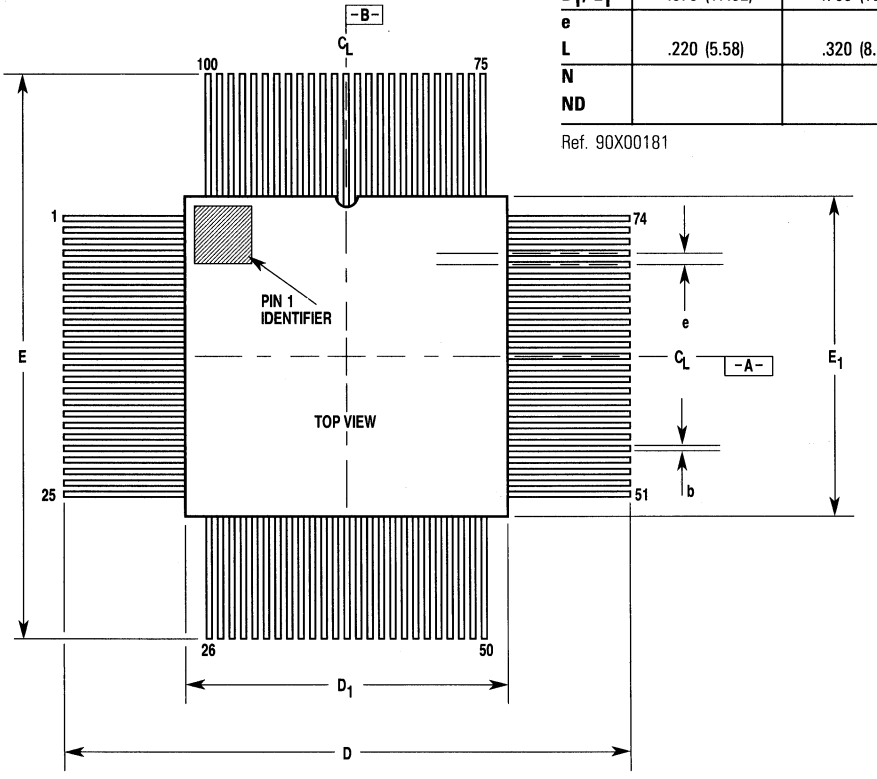
L6 100 Leaded Cerquad

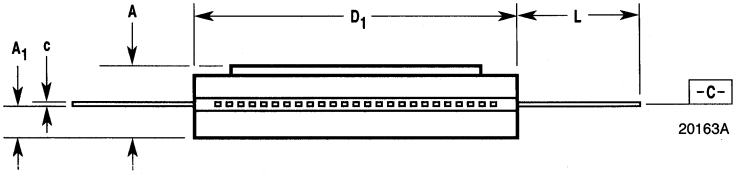
Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimensions D_1 and E_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
3. Dimension N: number of terminals.
4. Dimension ND: number of terminals per package edge.
5. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.114 (2.89)	.154 (3.91)	
A_1	.055 (1.40)	.075 (1.90)	
b	.008 (0.20)	.012 (0.30)	
c	.005 (0.13)	.009 (0.23)	
D, E			1.300 (32.95) Ref.
D_1, E_1	.670 (17.02)	.760 (19.30)	
e			.025 (0.64) Basic
L	.220 (5.58)	.320 (8.12)	
N			100, Note 3
ND			25, Note 4

Ref. 90X00181



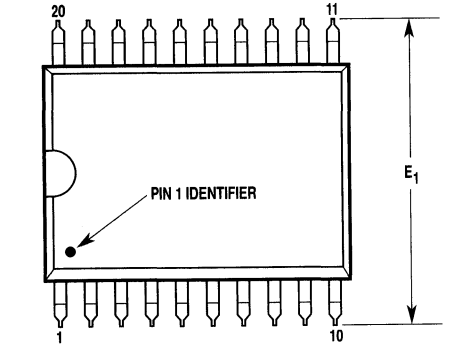


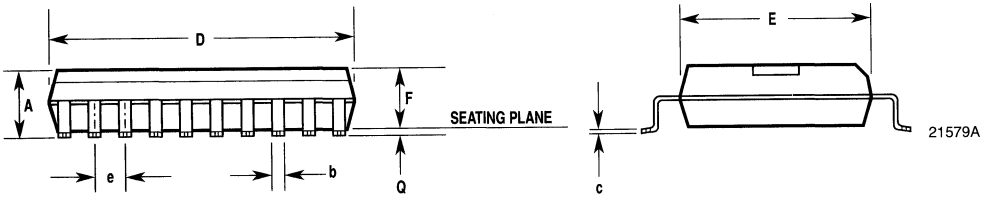
M3 20-Lead Plastic SOIC, .300"

Dimensions

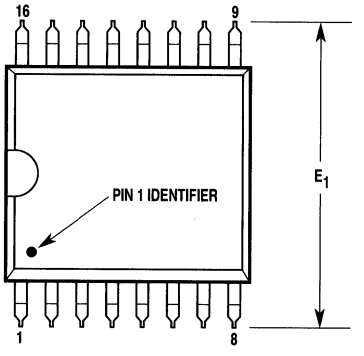
Sym	Inches (Millimeters) Min	Max	Notes
A	.093 (2.36)	.104 (2.64)	
b	.014 (0.36)	.019 (0.48)	
b_1			
c	.009 (0.23)	.013 (0.33)	
D	.496 (12.60)	.512 (13.01)	
E	.291 (7.39)	.299 (7.60)	
E_1	.394 (10.01)	.419 (10.64)	
e			.050 (1.27) Typ.
L			
N			20
Q	.004 (0.10)	.012 (0.30)	

Ref. 90X00181





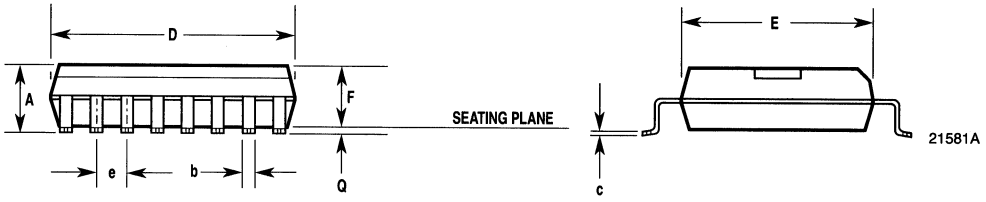
M9 16-Lead Plastic SOIC, .300"



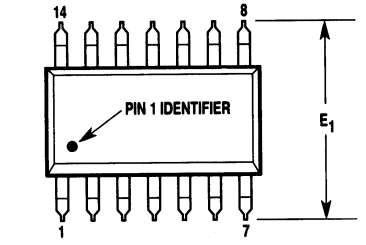
Dimensions

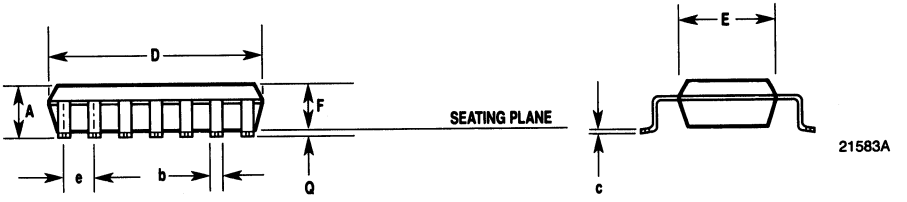
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.093 (2.36)	.104 (2.64)	
b	.014 (0.36)	.020 (0.51)	
b_1			
c	.009 (0.23)	.013 (0.33)	
D	.398 (10.11)	.413 (10.50)	
E	.291 (7.39)	.299 (7.60)	
E_1	.394 (10.01)	.419 (10.64)	
e			.050 (1.27) Typ.
F	.089 (2.26)	.092 (2.34)	
L			
N			16
Q	.004 (0.10)	.012 (0.30)	
α			

Ref. 90X00181



ME 14-Lead Plastic SOIC, .150"





Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.053 (1.35)	.069 (1.75)	
b	.014 (0.36)	.020 (0.51)	
b_1			
c	.008 (0.20)	.010 (0.25)	
D	.335 (8.51)	.344 (8.74)	
E	.150 (3.81)	.157 (3.99)	
E_1	.228 (5.79)	.244 (6.20)	
e			.050 (1.27) Typ.
F	.049 (1.25)	.059 (1.50)	
L			
N			14
Q	.004 (0.10)	.010 (0.25)	
α			

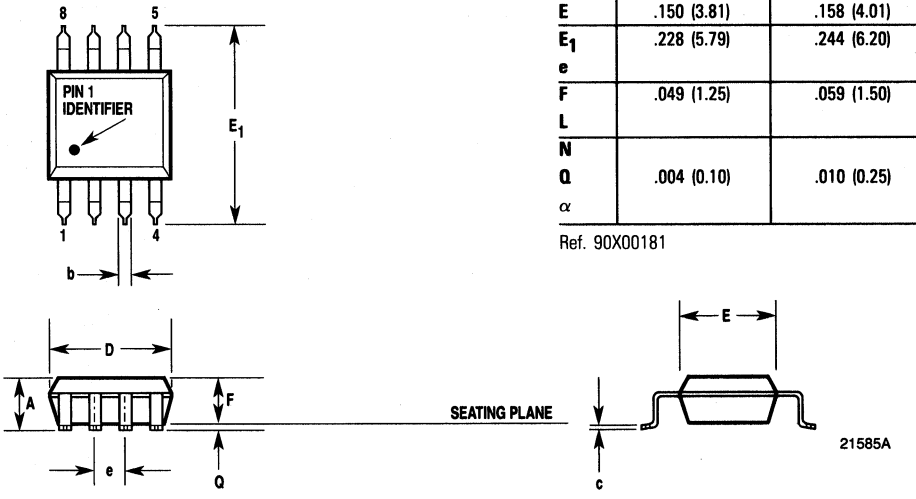
Ref. 90X00181

MH 8-Lead Plastic SOIC, .150"

Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.053 (1.35)	.069 (1.75)	
b	.014 (0.36)	.019 (0.48)	
b_1			
c	.007 (0.18)	.010 (0.25)	
D	.188 (4.78)	.196 (4.98)	
E	.150 (3.81)	.158 (4.01)	
E_1	.228 (5.79)	.244 (6.20)	
e			.050 (1.27) Typ.
F	.049 (1.25)	.059 (1.50)	
L			
N			8
Q	.004 (0.10)	.010 (0.25)	
α			

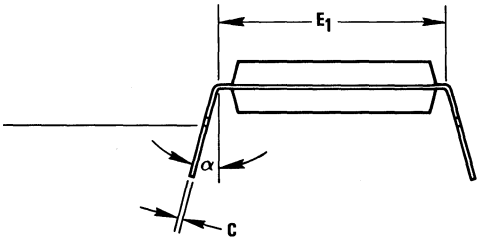
Ref. 90X00181



N0 64-Lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

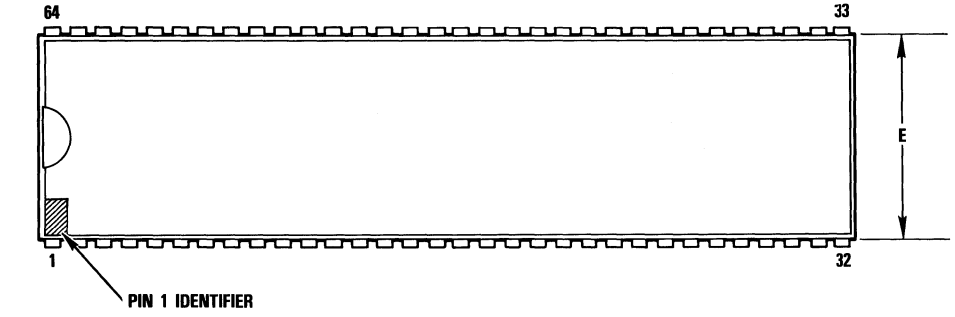
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.

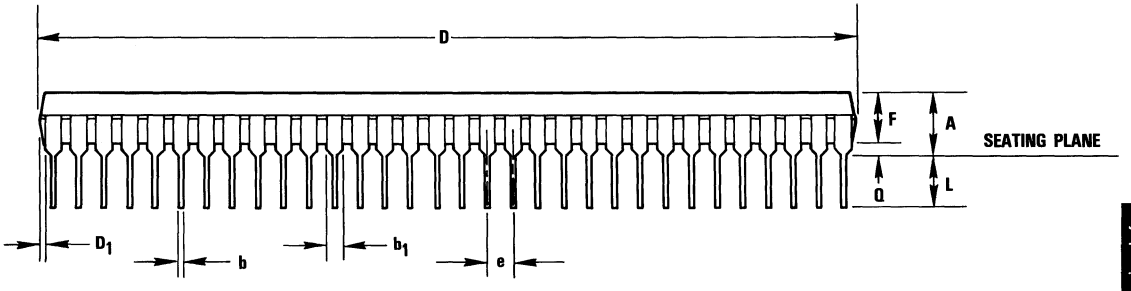


Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A		.250 (6.35)	
b	.014 (0.35)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	3.05 (77.47)	3.245 (82.42)	
D_1	.005 (0.13)		
E	.745 (18.92)	.840 (21.34)	
E_1	.900 (22.86)	.925 (23.50)	
e			.100 (2.54) Basic
F	.125 (3.18)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

Ref. 90X00181

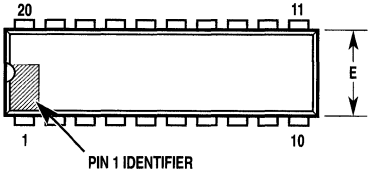




N1 20-Lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

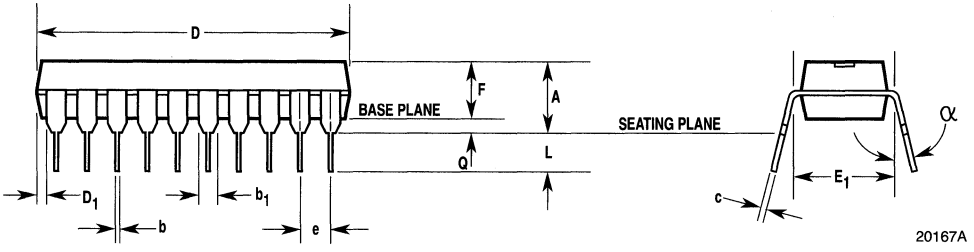
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

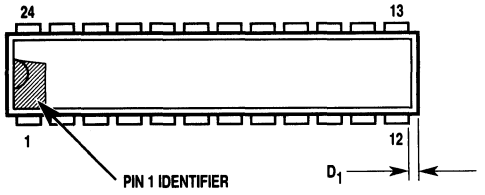
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.145 (3.68)	.200 (5.08)	
b	.015 (0.38)	.021 (0.53)	
b_1			.060 (1.52) Typ.
C	.009 (0.23)	.015 (0.38)	
D	1.013 (25.73)	1.040 (26.42)	
D_1	.005 (0.13)		
E	.255 (6.48)	.265 (6.73)	
E_1	.310 (7.87)	.363 (9.27)	
e	.090 (2.29)	.110 (2.79)	
F	.125 (3.18)	.135 (3.43)	
L	.125 (3.18)	.140 (3.56)	
Q	.020 (0.51)		
α	0°	15°	

Ref. 90X00181



N2 24-Lead Plastic Dual In-Line Package, .300"

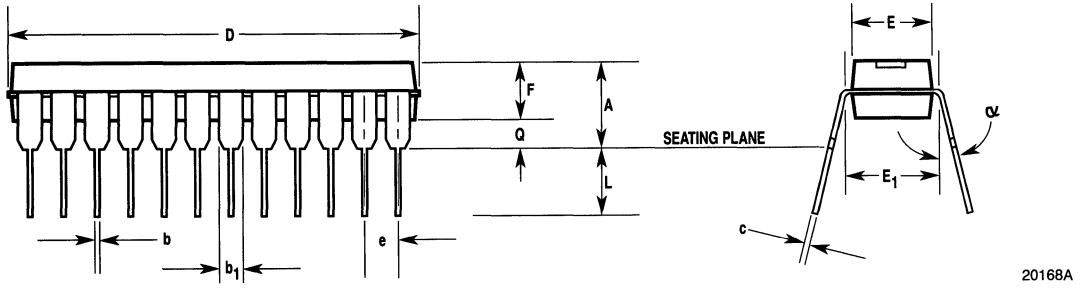
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.130 (3.30)	.230 (5.84)	
b	.014 (0.35)	.023 (0.58)	
b_1	.045 (1.14)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	1.180 (29.97)	1.285 (32.64)	
D_1	.005 (0.13)		
E	.240 (6.10)	.310 (7.87)	
E_1			.300 (7.62) Basic
e			.100 (2.54) Basic
F	.115 (2.92)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

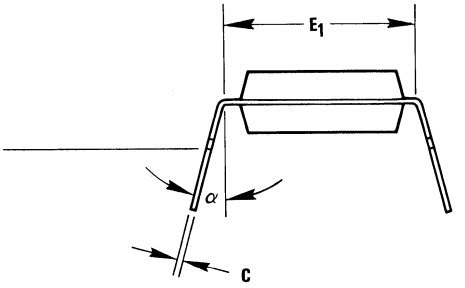
Ref. 90X00181



N4 48-Lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

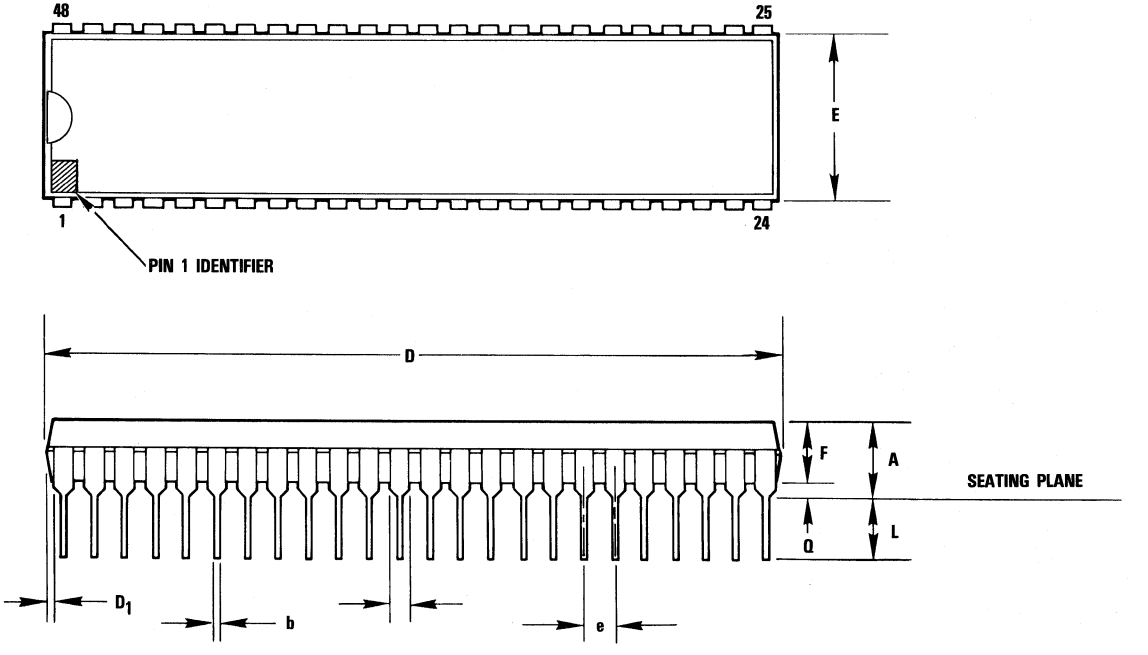
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A		.250 (6.35)	
b	.014 (0.35)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	2.375 (60.32)	2.490 (63.25)	
D_1	.005 (0.13)		
E	.485 (12.32)	.580 (14.73)	
E_1	.600 (15.24)	.625 (15.87)	
e			.100 (2.54) Basic
F	.125 (3.18)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

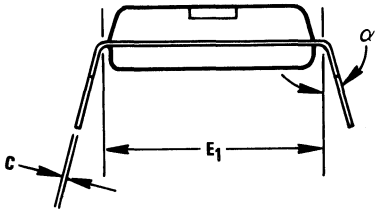
Ref. 90X00181



N5 40-Lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

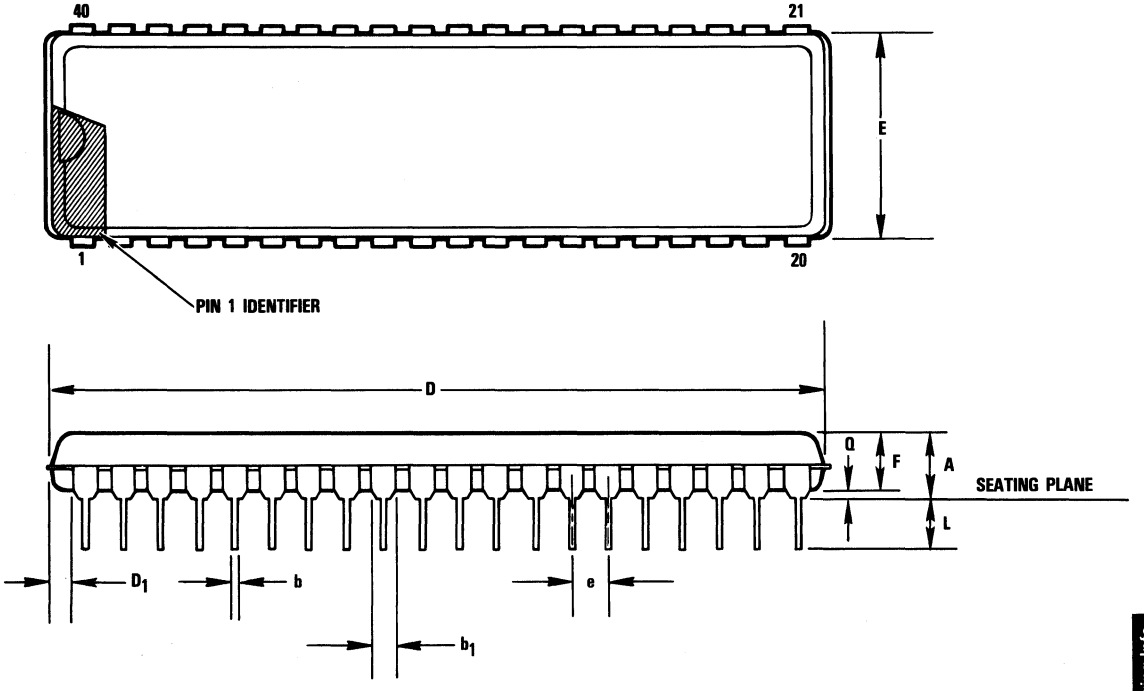
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A		.250 (6.35)	
b	.014 (0.35)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	1.980 (50.29)	2.095 (53.21)	
D_1	.005 (0.13)		
E	.485 (12.32)	.580 (14.73)	
E_1	.600 (15.24)	.625 (15.87)	
e			.100 (2.54) Basic
F	.125 (3.18)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

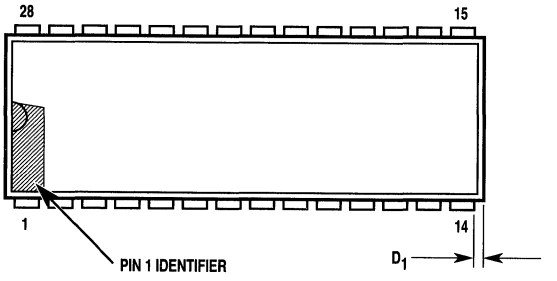
Ref. 90X00181



N6 28-Lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

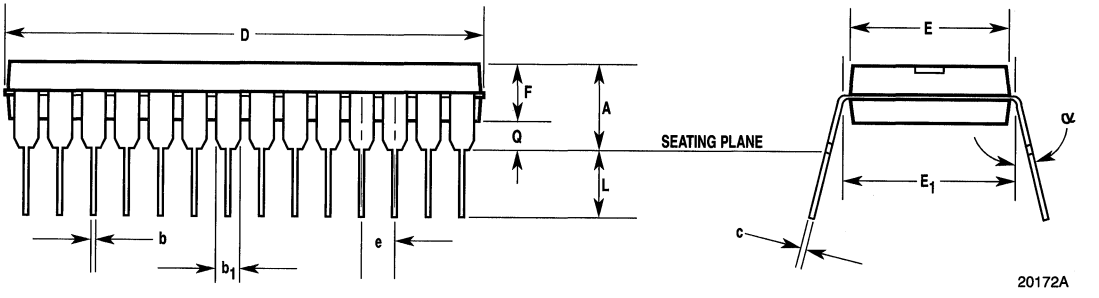
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A		.250 (6.35)	
b	.014 (0.36)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	1.380 (35.05)	1.565 (39.75)	
D_1	.005 (0.13)		
E	.485 (12.32)	.580 (14.73)	
E_1	.600 (15.24)	.625 (15.88)	
e			.100 (2.54) Basic
F			
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

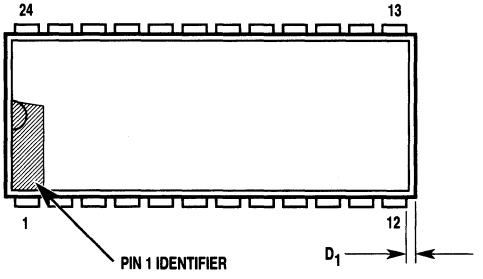
Ref. 90X00181



N7 24-Lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

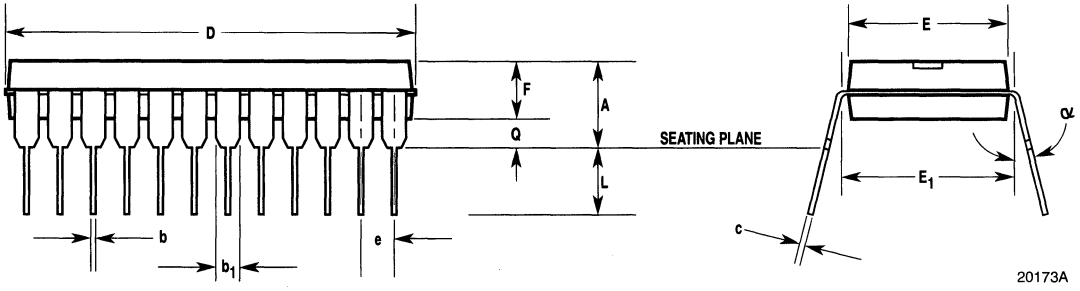
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A		.250 (6.35)	
b	.014 (0.35)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	1.150 (29.21)	1.290 (32.77)	
D_1	.005 (0.13)		
E	.485 (12.32)	.580 (14.73)	
E_1	.600 (15.24)	.625 (15.88)	
e			.100 (2.54) Basic
F	.125 (3.18)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

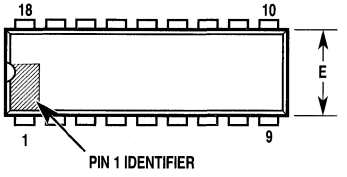
Ref. 90X00181



N8 18-Lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

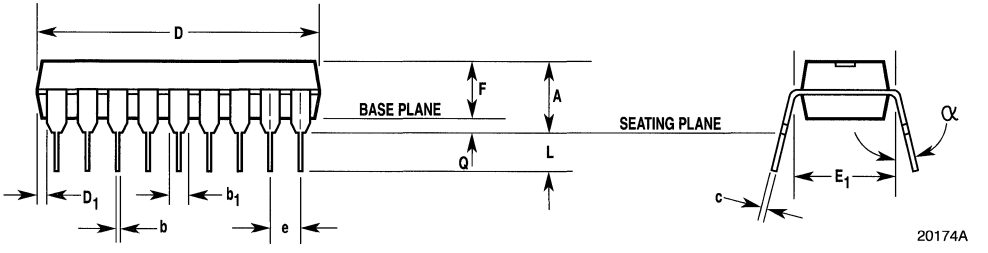
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.210 (5.33)	
b	.014 (0.36)	.022 (0.56)	
b_1	.045 (1.14)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	.845 (21.46)	.925 (23.50)	
D_1	.005 (0.13)		
E	.240 (6.10)	.280 (7.11)	
E_1	.300 (7.62)	.325 (8.25)	
e			.100 (2.54) Basic
F	.115 (2.92)	.195 (4.95)	
L	.115 (2.92)	.160 (4.06)	
Q	.015 (0.38)		
α	0°	15°	

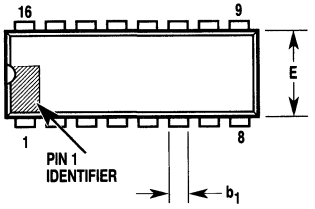
Ref. 90X00181



N9 16-lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

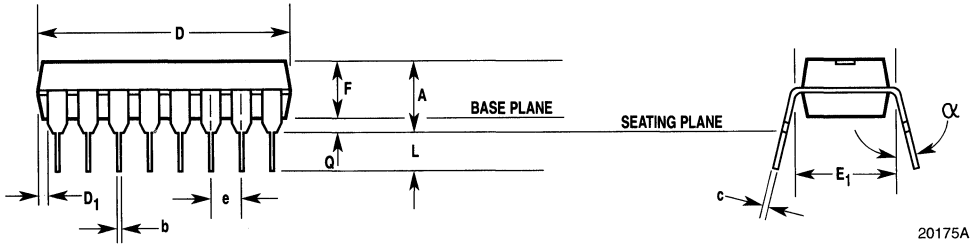
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.210 (5.33)	
b	.014 (0.35)	.022 (0.56)	
b_1	.045 (1.14)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	.745 (18.92)	.840 (21.34)	
D_1	.005 (0.13)		
E	.240 (6.10)	.280 (7.11)	
E_1	.300 (7.62)	.325 (8.25)	
e			.100 (2.54) Basic
F	.115 (2.92)	.195 (4.95)	
L	.115 (2.92)	.160 (4.06)	
Q	.015 (0.38)		
α	0°	15°	

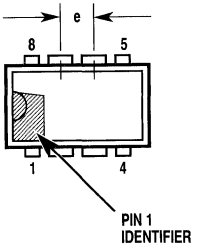
Ref. 90X00181



NH 8-Lead Plastic Dual In-Line Package

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

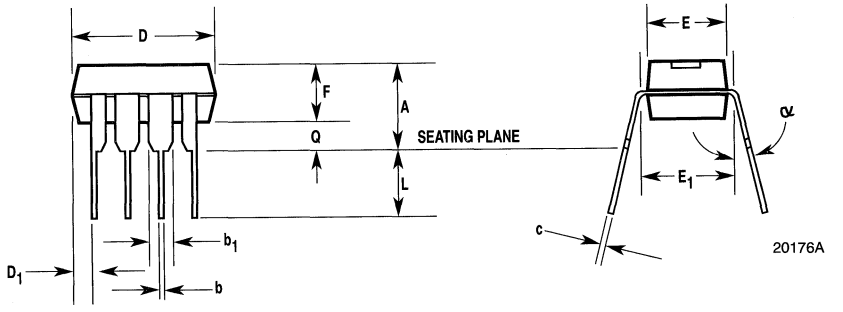
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A	.145 (3.68)	.200 (5.08)	
b	.015 (0.38)	.021 (0.53)	
b_1			.060 (1.52) Typ.
C	.009 (0.23)	.015 (0.38)	
D	.373 (9.47)	.400 (10.16)	
D_1	.005 (0.13)		
E	.245 (6.22)	.255 (6.48)	
E_1	.310 (7.87)	.365 (9.27)	
e	.090 (2.29)	.110 (2.79)	
F	.125 (3.18)	.135 (3.43)	
L	.125 (3.18)	.140 (3.56)	
Q	.020 (0.51)		
α	0°	15°	

Ref. 90X00181



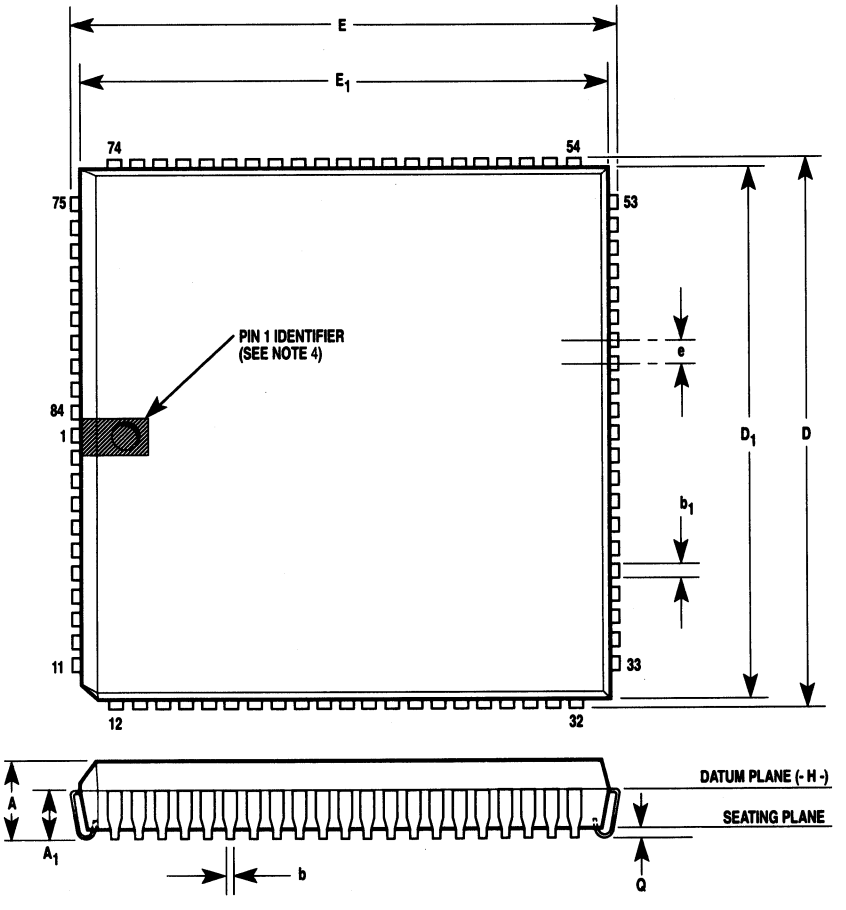
R0 84-Lead Plastic J-Leaded Chip Carrier

Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.165 (4.20)	.200 (5.08)	
A_1	.090 (2.29)	.130 (3.30)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	1.185 (30.10)	1.195 (30.35)	
D_1	1.150 (29.21)	1.158 (29.41)	Note 3
E	1.185 (30.10)	1.195 (30.35)	
E_1	1.150 (29.21)	1.158 (29.41)	Note 3
N			84, Note 5
ND			21, Note 6
Q	.020 (0.51)		

Ref. 90X00181

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **(–H–)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (0.25mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.



20180A

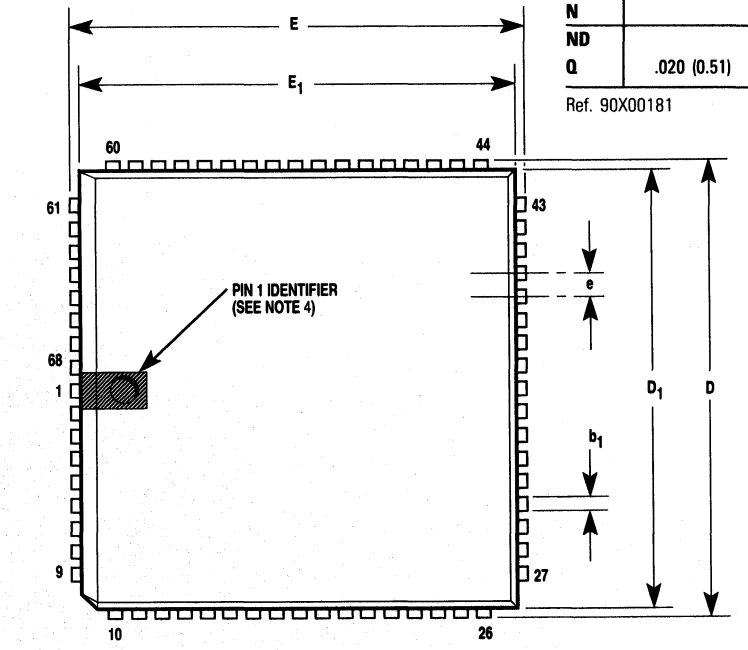
R1 68-Lead Plastic J-Leaded Chip Carrier

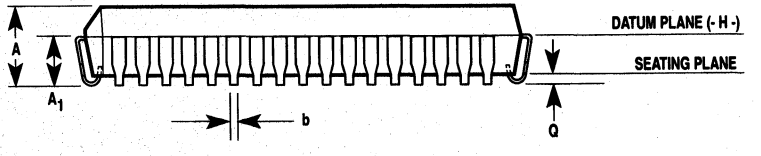
Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **(–H–)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (0.25mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.165 (4.20)	.200 (5.08)	
A_1	.090 (2.29)	.130 (3.30)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	.985 (25.02)	.995 (25.27)	
D_1	.950 (24.13)	.958 (24.33)	Note 3
E	.985 (25.02)	.995 (25.27)	
E_1	.950 (24.13)	.958 (24.33)	Note 3
e			.050 (1.27) Basic
N			68, Note 5
ND			17, Note 6
Q	.020 (0.51)		

Ref. 90X00181

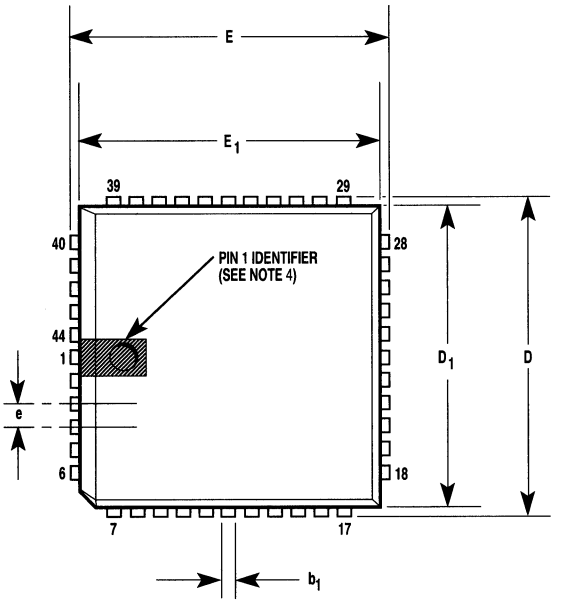


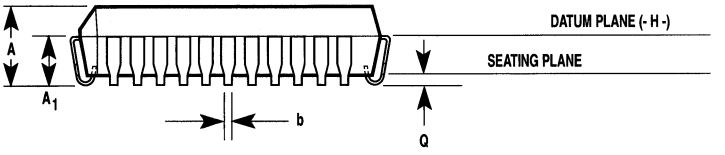


20181A

R2 44-Lead Plastic J-Leaded Chip Carrier

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **(–H–)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (0.25mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.





20182A

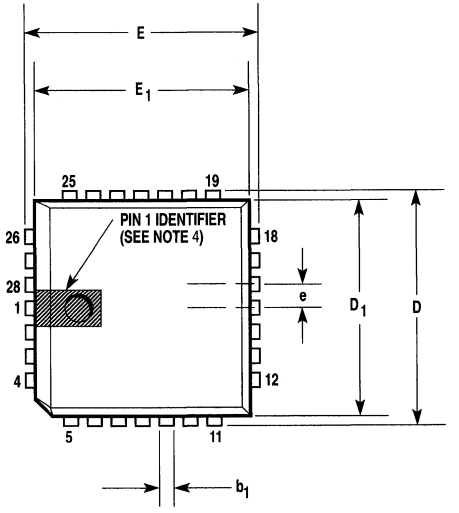
Dimensions

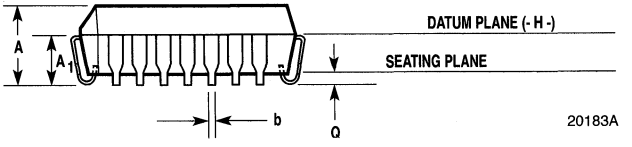
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.165 (4.20)	.180 (4.57)	
A_1	.090 (2.29)	.120 (3.04)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	.685 (17.40)	.695 (17.65)	
D_1	.650 (16.51)	.656 (16.66)	Note 3
E	.685 (17.40)	.695 (17.65)	
E_1	.650 (16.51)	.656 (16.66)	Note 3
e			.050 (1.27) Basic
N			44, Note 5
ND			11, Note 6
Q	.020 (0.51)		

Ref. 90X00181

R3 28-Lead Plastic J-Leaded Chip Carrier

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **(-H-)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (.245mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.





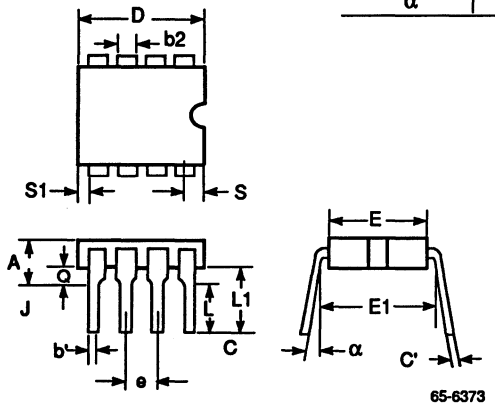
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.165 (4.20)	.180 (4.57)	
A_1	.900 (2.29)	.120 (3.04)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	.485 (12.32)	.495 (12.57)	
D_1	.450 (11.43)	.456 (11.58)	Note 3
E	.485 (12.32)	.495 (12.57)	
E_1	.450 (11.43)	.456 (11.58)	Note 3
e			.050 (1.27) Basic
N			28, Note 5
ND			7, Note 6
Q	.020 (0.51)		

Ref. 90X00181

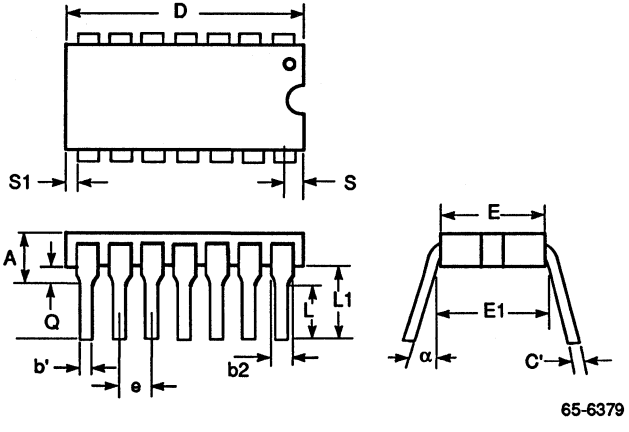
D-8 8-Lead Ceramic Dual In-Line Package

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
b1	.014	.023	.36	.58
b2	.045	.065	1.14	1.65
C1	.008	.015	.20	.38
D		.405		10.29
E	.220	.310	5.59	7.87
E1	.290	.320	7.37	8.13
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	.140		3.56	
Q	.015	.060	.38	1.52
S		.055		1.35
S1	.005		.13	
α	0°	15°	0°	15°



D-14 14-Lead Ceramic Dual In-Line Package

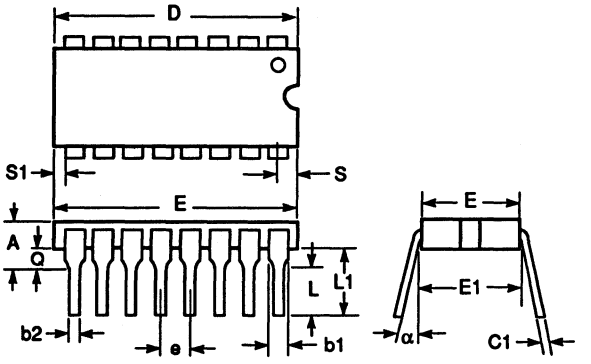
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
b1	.014	.023	.36	.58
b2	.045	.065	1.14	1.65
C1	.008	.015	.20	.38
D		.785		19.94
E	.220	.310	5.59	7.87
E1	.290	.320	7.37	8.13
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	.140		3.56	
Q	.015	.060	.38	1.52
S		.098		2.49
S1	.005		.13	
α	0°	15°	0°	15°



65-6379

D-16 16-Lead Ceramic Dual In-Line Package

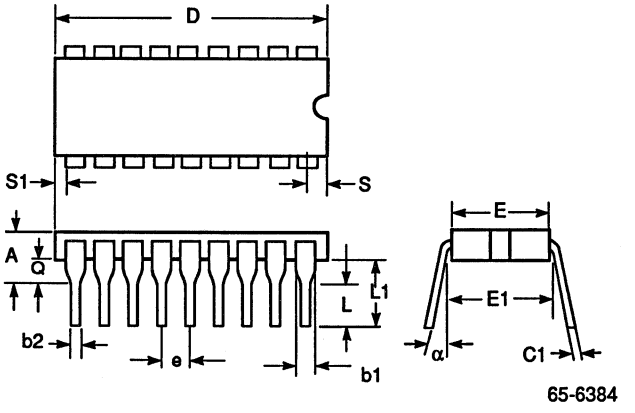
Dimension	Inches			Millimeters		
	Min		Max	Min		Max
A			.200			5.08
b1	.014		.023	.36		.58
b2	.045		.065	1.14	1.65	
C1	.008		.015	.20		.38
D			.840			21.34
E	.220		.310	5.59		7.87
E1	.290		.320	7.37		8.13
e	.100 BSC			2.54 BSC		
L	.125		.200	3.18		5.08
L1	.140			3.56		
Q	.015	.060	.38	1.52		
S			.098			2.49
S1	.005			.13		
α	0°		15°	0°		15°



65-6382

D-18 18-Lead Ceramic Dual In-Line Package

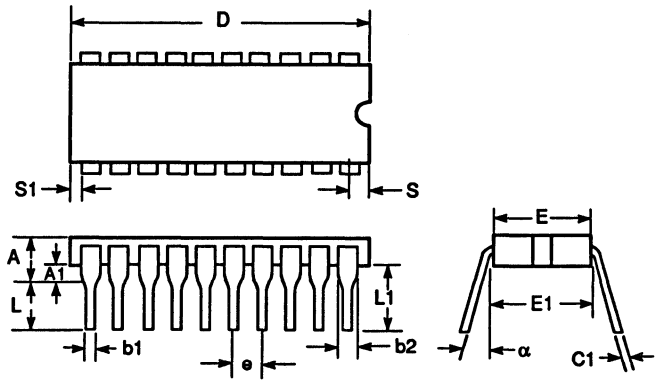
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
b1	.014	.023	.36	.58
b2	.045	.065	1.14	1.65
C1	.008	.015	.20	.38
D		.840		21.34
E	.220	.310	5.59	7.87
E1	.290	.320	7.37	8.13
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	.140		3.56	
Q	.015	.060	.38	1.52
S		.098		2.49
S1	.005		.13	
α	0°	15°	0°	15°



65-6384

D-20 20-Lead Ceramic Dual In-Line Package

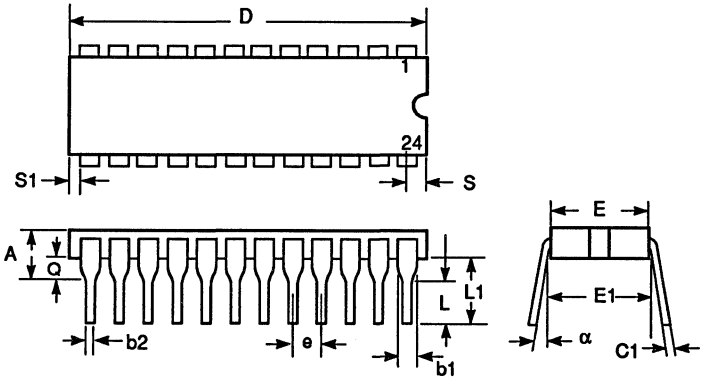
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
b1	.014	.023	.36	.58
b2	.045	.065	1.14	1.65
C1	.008	.015	.20	.38
D		1.060		26.92
E	.220	.310	5.59	7.87
E1	.290	.320	7.37	8.13
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	.125		3.56	
Q	.015	.070	.38	1.78
S		.080		2.03
S1	.005		.13	
α	0°	15°	0°	15°



65-6386

D-24 24-Lead Ceramic Dual In-Line Package (0.3" Wide)

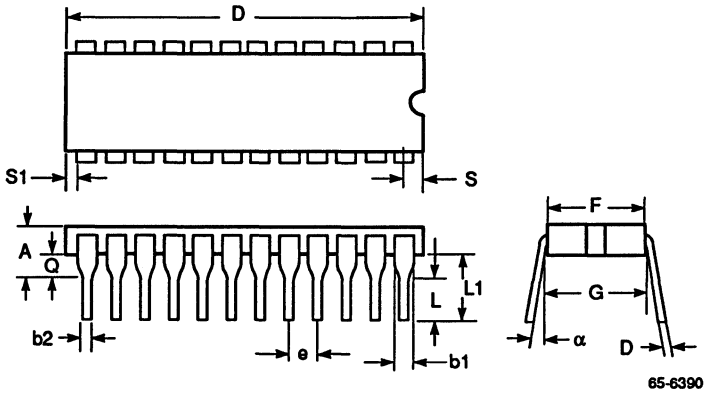
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
b1	.014	.023	.36	.58
b2	.045	.065	1.14	1.65
C1	.008	.015	.20	.38
D		1.280		32.51
E	.220	.310	5.59	7.87
E1	.290	.320	7.37	8.13
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	.140		3.56	
Q	.015	.060	.38	1.52
S		.080		2.03
S1	.005		.13	
α	0°	15°	0°	15°



65-6391

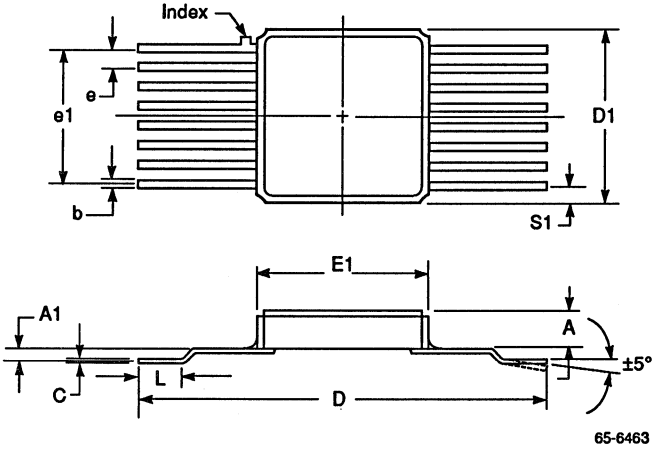
D-24W 24-Lead Ceramic Dual In-Line Package (0.6" Wide)

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.225		5.72
b1	.014	.023	.36	.58
b2	.045	.065	1.14	1.65
C1	.008	.015	.20	.38
D		1.290		32.77
E	.500	.610	12.70	15.47
E1	.590	.620	14.99	15.75
e	.100 BSC		2.54 BSC	
L	.120	.200	3.05	5.08
L1	.135		3.43	
Q	.015	.075	.38	1.91
S		.098		2.49
S1	.005		.13	
α	0°	15°	0°	15°



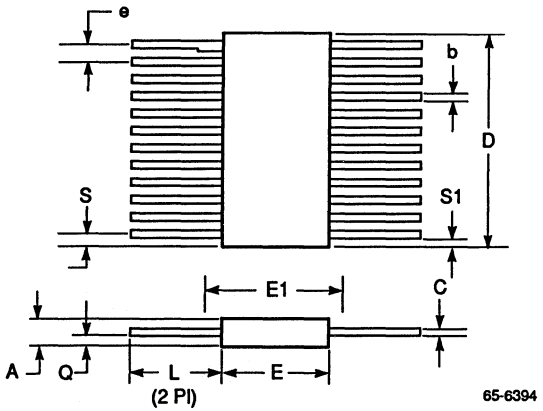
F-16 16-Lead Ceramic Gull Wing Flat Pack

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.090	.133	2.28	3.38
A1	.023	.033	0.58	0.84
b	.013	.017	0.33	0.43
C	.007	.010	0.178	0.25
D	.675	.685	17.15	17.40
D1/E1	.442	.458	11.23	11.63
e	.05 BSC		1.27 BSC	
L	.050	.065	1.27	1.65



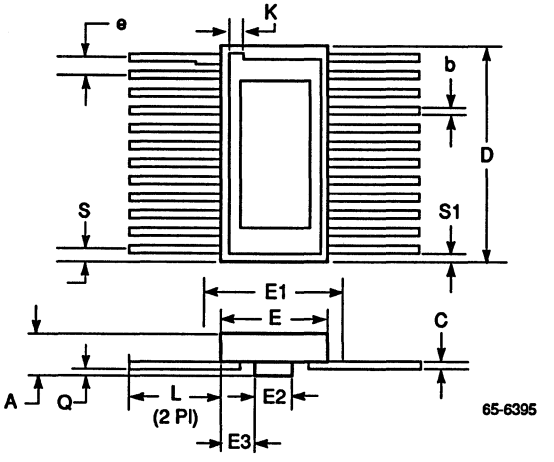
F-24 24-Lead Ceramic Flat Pack (Cerpak) Package

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.063	.090	1.6-0	2.29
b	.015	.019	.38	.48
C	.003	.006	.08	.15
D	.584	.621	14.83	15.77
E	.363	.377	9.22	10.03
e	.050 BSC		1.27 BSC	
L	.250	.370	6.35	9.40
Q	.026	.040	.66	1.02
S		.045		1.14
S1	.005		.13	



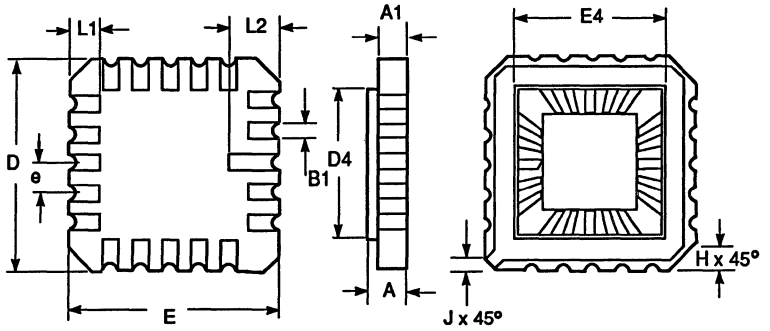
F-24B 24-Lead Ceramic Bottom-Brazed Flat Pack Package

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.045	.115	1.14	2.92
b	.015	.019	.38	.48
C	.003	.006	0.08	0.15
D		.640		16.26
E	.350	.420	9.14	10.67
E1		.450		11.43
E2	.180		4.57	
E3	.030		0.76	
e	.050 BSC		1.27 BSC	
L	.250	.370	6.35	9.40
Q	.026	.045	0.66	1.14
S		.045		1.14
S1	.005		0.13	



L-20 20-Pad Leadless Chip Carrier

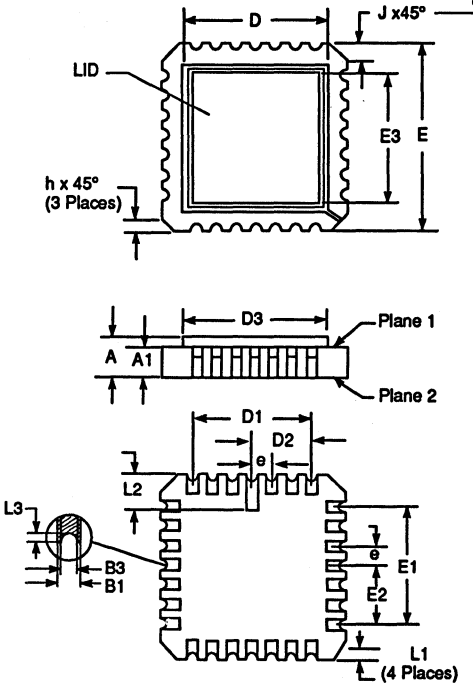
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.064	0.086	1.63	2.18
A1	0.054	0.066	1.37	1.68
B1	0.022	0.028	0.56	0.71
B3	.006	.022	0.15	0.56
D/E	0.342	0.358	8.69	9.09
D1/E1	.200 BSC			
D2/E2	.100 BSC			
D3/E3		.358		9.09
e	0.050 BSC		1.27 BSC	
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L1	.045	.055	1.14	1.40
L2	.075	.095	1.91	2.41
L3	.003	.015	.008	0.38
ND/NE	5		5	



65-6388

L-28 28-Terminal Ceramic Leadless Chip Carrier

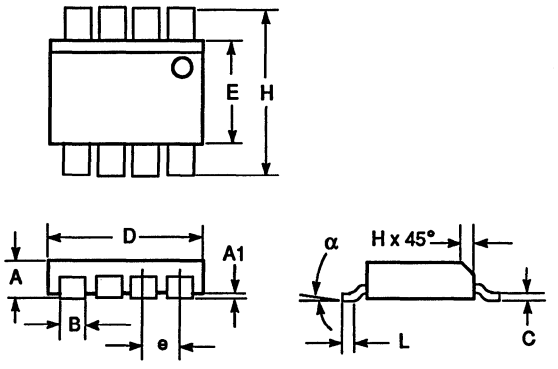
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.060	.100	1.52	2.54
A1	.050	.088	1.27	2.24
B1	.022	.028	0.56	0.71
B3	.006	.022	.015	.056
D/E	.442	.460	11.23	11.68
D1/E1	.300 BSC		7.62 BSC	
D2/E2	.150 BSC		3.81 BSC	
D3/E3		.460	10.21	11.68
e	.050 BSC		1.27 BSC	
h	.040 REF		1.02 REF	
j	.020 REF		0.51 REF	
L1	.045	.055	1.14	1.40
L2	.075	.095	1.91	2.41
L3	.003	.015	0.08	0.38
ND/NE	7		7	



65-6393

M-8 8-Lead Plastic Small Outline Dual In-Line Package

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.053	.069	1.35	1.75
A1	.004	.009	.10	.20
B	.014	.020	.350	.450
C	.007	.010	.19	.22
D	.188	.197	4.80	5.00
E	.150	.158	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
L	.020	.045	.508	1.14
α	0°	8°	0°	8°
h	.010	.020	.25	.50

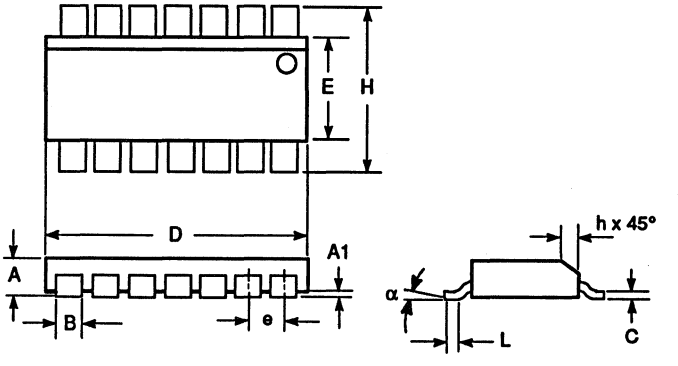


65-6375

M-14 14-Lead Plastic Small Outline Dual In-Line Package

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.053	.069	1.35	1.75
A1	.004	.008	0.10	0.20
B	.014	.019	0.36	0.48
C	.007	.009	0.18	0.23
D	.336	.344	8.54	8.74
E	.150	.158	3.81	4.01
e	.050 BSC		1.27 BSC	
H	.228	.244	5.79	6.20
h	.010	.020	0.25	0.50
L	.020	.045	0.51	1.14
0C	0°	8°	0°	8°

Dimensions conform to JEDEC Specification MS-012-AB for SO packages.

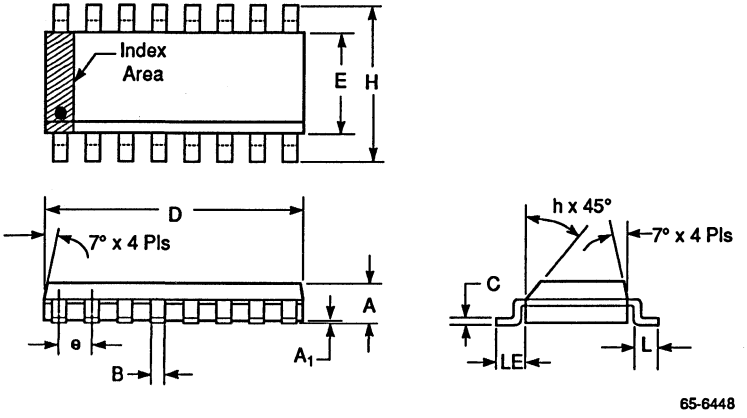


65-6380

M-16 16-Lead Plastic Small Outline Dual In-Line Package

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.013	.020	0.33	0.51
C	.0075	.0098	0.19	0.25
D	.3859	.3937	9.80	10.00
E	.1497	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.2284	.2440	5.80	6.20
h	.0099	.0196	0.25	0.50
L	.016	.050	.40	1.27
LE	.030	—	.76	—
Y	—	.004	—	0.10
O	0°	8°	0°	8°

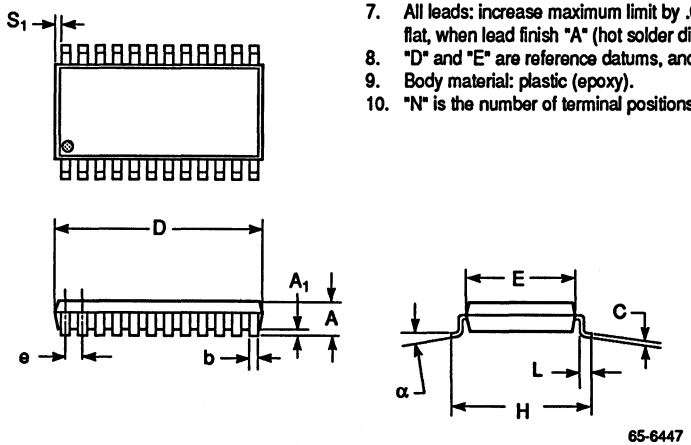
Notes:
1. Refer to applicable symbol list.
2. Dimension "D" does not include mold flash, protrusions of gate burrs. Mold flash, protrusions and gate burrs shall not exceed .006 in. (.15 mm) per side.
3. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed .101 in. (.25 mm) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the hatched area.
5. "L" is the length of terminal for soldering to a substrate.
6. The lead width "B" as measured .014 in. (.36 mm) or greater above the seating plane, shall not exceed a maximum value of .024 in. (.61 mm).



M-24 24-Lead Plastic Small Outline Dual In-Line Package

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.092	.105	2.34	2.67
A1	.003	.012	0.08	0.30
B	.014	.020	0.35	0.51
C	.009	.013	0.23	0.32
D	.598	.614	15.19	16.70
E	.290	.299	7.37	7.60
e	.050 BSC		1.27 BSC	
H	.393	.420	9.98	10.67
L	.015	.050	0.38	1.27
S1	.005	—	0.13	—
α	0°	8°	0°	8°
N	24		24	

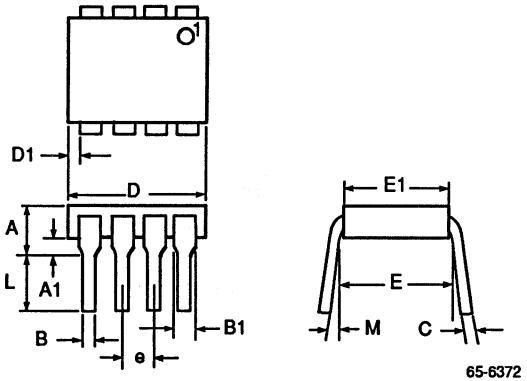
Notes:
1. Dimensions and tolerancing per ANSI Y14.5 - 1982
2. Controlling dimension: millimeter
3. Index area; a notch or a pin one identification marks hall be located adjacent to pin one. The manufacturers' identification shall not be used as a pin one identification mark.
4. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located within .005 (0.13 mm) of its exact longitudinal position relative to pins 1 and 24.
5. Applies to all four corners (leads number 1, 12, 13 and 24)
6. Twenty-two spaces.
7. All leads: increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish "A" (hot solder dip) is applied.
8. "D" and "E" are reference datums, and do not include mold flash.
9. Body material: plastic (epoxy).
10. "N" is the number of terminal positions.



65-6447

N-8 8-Lead Plastic Dual In-Line Package

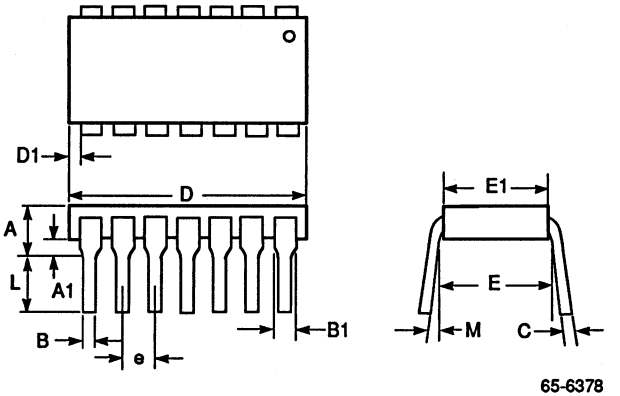
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	0.36	0.58
B1	.030	.070	0.76	1.78
C	.008	.013	0.20	0.30
D	.330	.375	8.38	9.40
E1	.240	.260	6.09	6.60
E	.300	.325	7.37	7.87
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
A1	.015	.060	0.38	1.52
D1	.005		0.13	
M	0°	15°	0°	15°



65-6372

N-14 14-Lead Plastic Dual In-Line Package

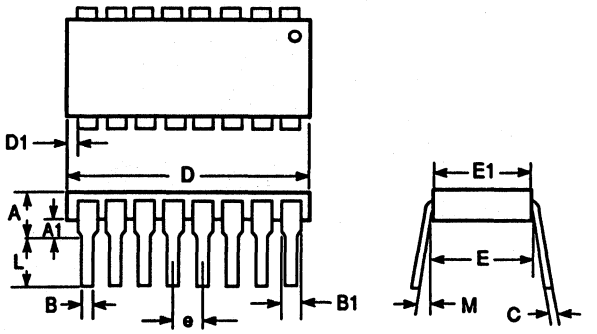
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	0.36	0.58
B1	.030	.070	0.76	1.78
C	.008	.013	0.20	0.30
D	.740	.760	18.92	19.18
E1	.240	.262	6.10	6.60
E	.300	.325	7.37	7.87
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
A1	.015	.060	0.38	1.52
D1		.005	.013	
M	0°	15°	0°	15°



65-6378

N-16 16-Lead Plastic Dual In-Line Package

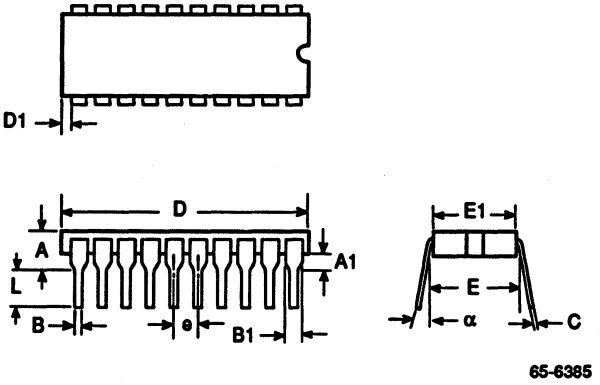
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	0.36	0.58
B1	.030	.070	0.76	1.78
C	.008	.013	0.20	0.30
D	.740	.760	18.80	19.30
E1	.240	.262	6.10	6.60
E	.300	.325	7.37	7.87
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
A1	.015	.060	0.38	1.52
D1	.005		0.13	
M	0°	15°	0°	15°



65-6381

N-20 20-Lead Plastic Dual In-Line Package

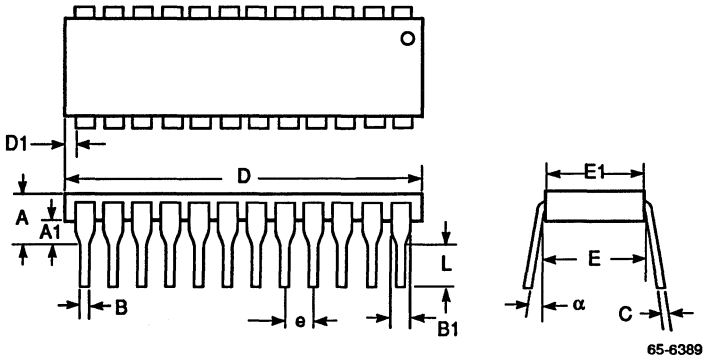
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.210		5.33
B1	.014	.023	.36	.58
C	.008	.012	.20	.30
D	.995	1.065	5.27	27.05
E1	.245	.310	6.22	7.87
E	.290	.320	7.37	8.13
L	.115	.150	2.92	3.81
e	.100 BSC		2.54 BSC	
A1	.015		0.38	
D1	.005		.13	
M	0°	15°	0°	15°



65-6385

N-20W 20-Lead Plastic Dual In-Line Package (0.6" Wide)

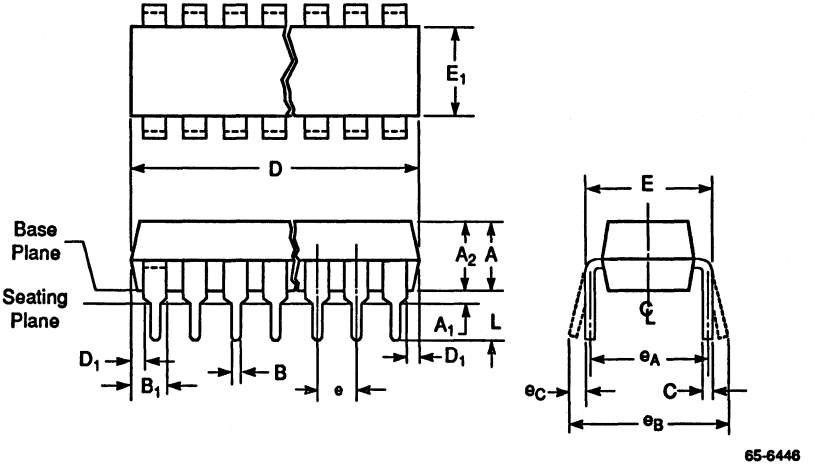
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.225		5.72
B	.014	.023	0.36	0.58
B1	.030	.070	0.76	1.78
C	.008	.012	0.20	0.30
D	1.24	1.26	31.5	32.0
E1	.530	.550	13.46	13.97
E	.590	.620	14.99	15.78
e	.100 BSC		2.54 BSC	
L	.120	.200	3.05	5.08
A1	.015	.075	0.38	1.91
D1	.005		0.13	
M	0°	15°	0°	15°



N-24N 24-Lead Plastc Dual In-Line Package (0.3" Wide)

Notes
1. Controlling dimensions are in "inches"
2. Dimesioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions "A", "A1" and "L" are measured with the package seated in the Seating Plane.
4. "D" an d "E1" dimensions for plastic packages, do not include modl flash or protrusions. Mold flash or protursions shall not exceed .010 inch (0.25 mm).
5. "E" and "eA" measured with the leads constrained to be perpendicular to the base plan.
6. "eB" and "eC" are measured at the lead tips with the leads unconstrained. "eC" must be zero or greater.
7. The basic pin spacing os .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within ±010 inch (0.25 mm) of its exact longitudinal position relative to pins 1 and 24.
8. All leads: increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat, when lead finish "A" (hot solder dip) is applied.
9. "N" is the maximum number of lead positions.
10. Eleven spaces.

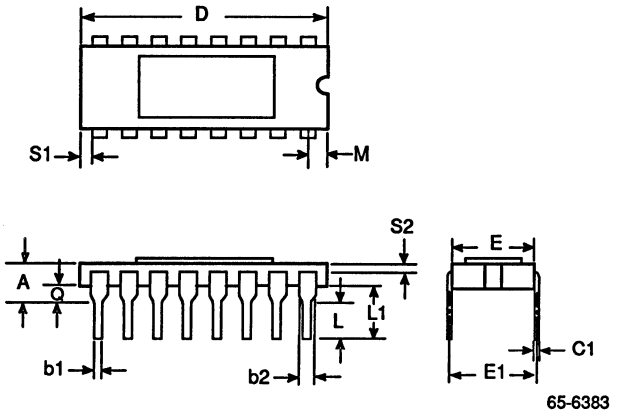
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.210		5.33
A1	.015		0.38	
A2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D	1.125	1.275	28.58	32.39
D1	.005	0.13		
E	.300	.325	7.62	8.26
E1	.240	.280	6.1	7.11
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB		.430		10.92
L	.115	.160	2.92	4.06
N		24		24



65-6446

S-16 16-Lead Ceramic Sidebraze Dual In-Line Package

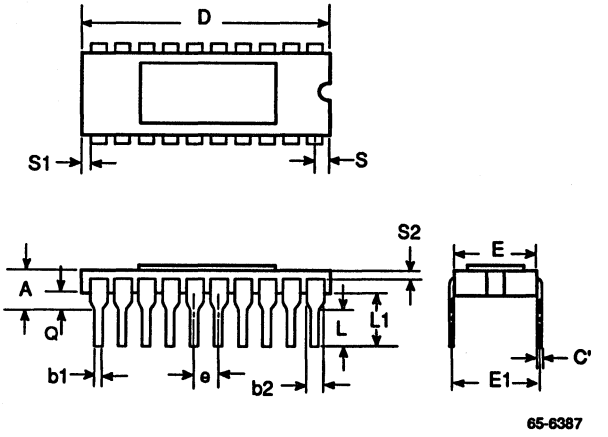
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
b1	.014	.023	.36	.58
b2	.045	.065	1.14	1.65
C1	.008	.015	.20	.38
D		.840		21.33
E	.200 .310	5.59	7.87	
E1	.290	.320	7.37	8.13
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	.140		3.57	
Q	.015	.060	.33	1.52
S		.098		2.49
S1	.005		.13	
S2	.005		.13	



65-6383

S-20 20-Lead Ceramic Sidebraze Dual In-Line Package

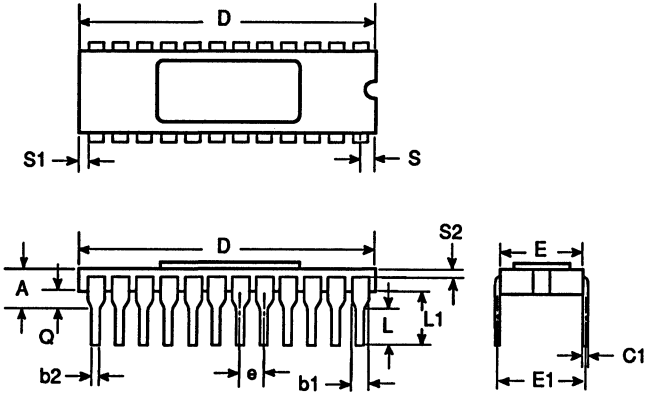
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
b1	.014	.023	.36	.58
b2	0.45	.065	1.14	1.65
C1	.008	.015		.38
D		1.060		26.92
E	.220	.310	5.59	7.87
E1	.290	.320	7.37	8.13
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	1.40		3.57	
Q	.015	.070	.38	1.78
S		.080		2.03
S1	.005		.13	
S2	.005		.13	



65-6387

S-24 24-Lead Ceramic Sidebraze Dual In-Line Package (0.3" Wide)

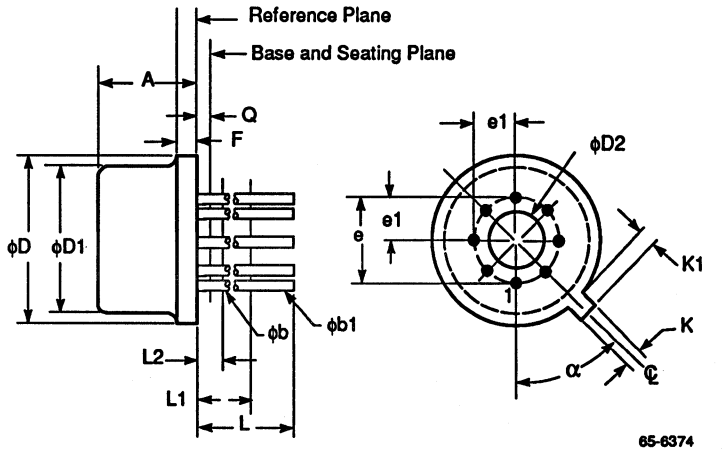
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.225		5.08
b1	.014	.023	.36	.58
b2	.045	.065	1.14	1.65
C1	.008	.015	.20	.38
D		1.280		32.51
E	.220	.310	5.59	7.87
E1	.290	.20	7.37	8.13
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	.125		3.56	
Q	.015	.060	.38	1.52
S		.080		2.03
S1	.005		.13	
S2	.005		.13	



65-6392

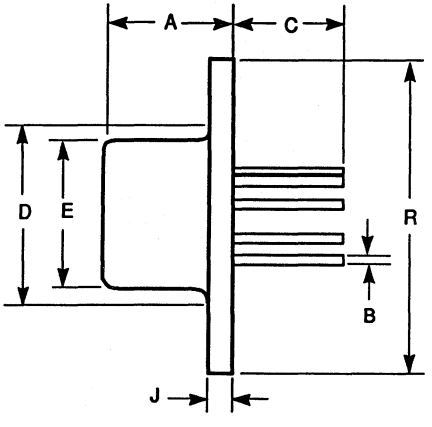
T-8 8-Lead TO-99 Metal Can

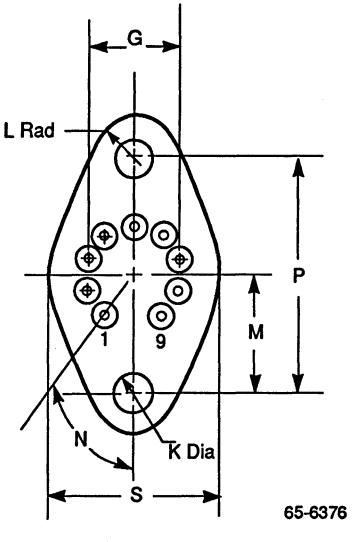
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.165	.185	4.19	4.70
b	.016	.019	.41	.48
b1	.016	.021	.41	.53
D	.335	.375	8.51	9.53
D1	.305	.335	7.75	8.51
/D2	.110	.160	2.79	4.06
e	.200 BSC		5.08 BSC	
e1	.100 BSC		2.54 BSC	
F		.040		1.02
K		.034	.69	.86
K1	.027	.045	.69	1.14
L	.500	.750	12.7	19.05
L1		.050		1.27
L2	.250		6.35	
Q	.010	.045	.25	1.14
α	450 BSC		450 BSC	



T-9 9-Lead TO-66 Metal Can

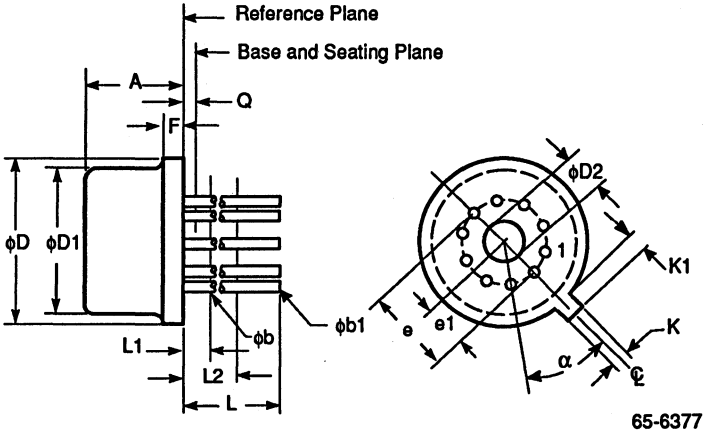
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.250	.340	6.35	8.63
B	.028	.034	.71	.863
C	.360		9.14	
D		.620		15.748
E	.300	.500	7.62	12.70
G	.325 BSC		5.84 BSC	
J	.050	.075	1.27	1.90
K	.142	.152	3.60	3.86
L		.145		3.68
M	.477	.483	12.11	12.26
N	36° Typ		36° Typ	
P	.958	.962	24.33	24.43
R		1.252		31.80
S		.700		17.80

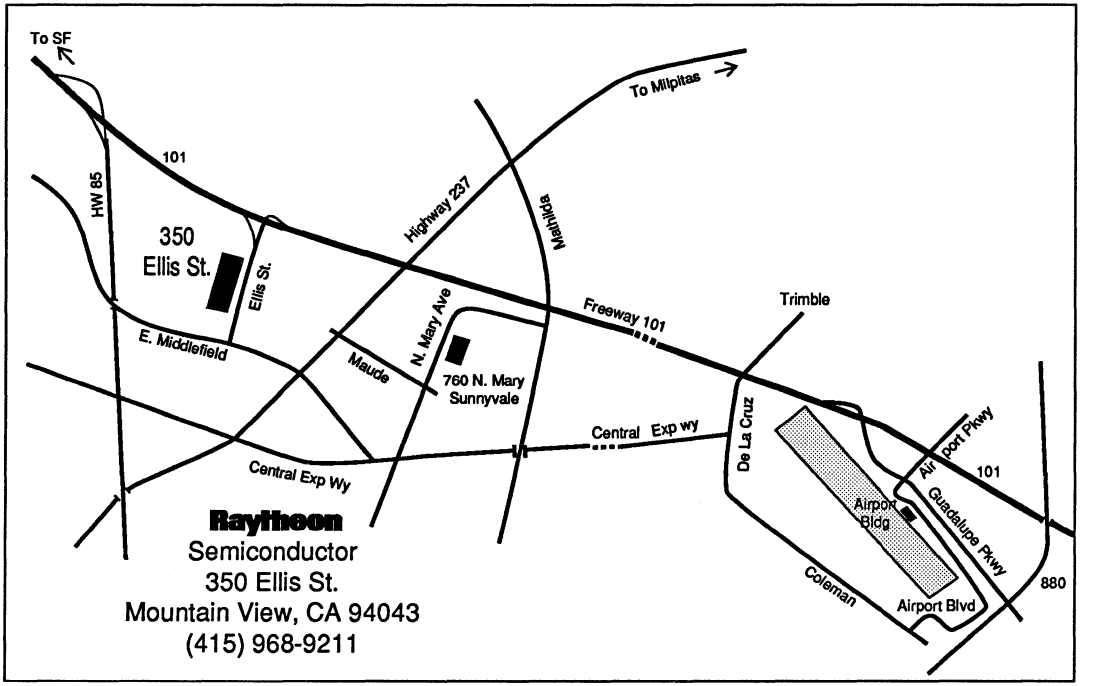




T-10 10-Lead TO-100 Metal Can

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.165	.185	4.19	4.70
b	.016	.019	.41	.48
b1	.016	.021	.41	.53
D	.335	.375	8.51	9.53
D1	.305	.335	7.75	8.51
D2	.110	.160	2.79	4.06
e	.230 BSC		5.84 BSC	
e1	.115 BSC		2.92 BSC	
F		.040		1.02
K	.027	.034	.69	.86
K1	.027	.045	.69	1.14
L	.500	.750	12.70	19.05
L1		.050		1.27
L2	.250		6.35	
Q	.010	.045	.25	1.14
α	36° BSC		36° BSC	





From San Jose Airport:
Take 101 North to Ellis Street Exit.
Left on Ellis. Raytheon Semiconductor is on the right side of the street.
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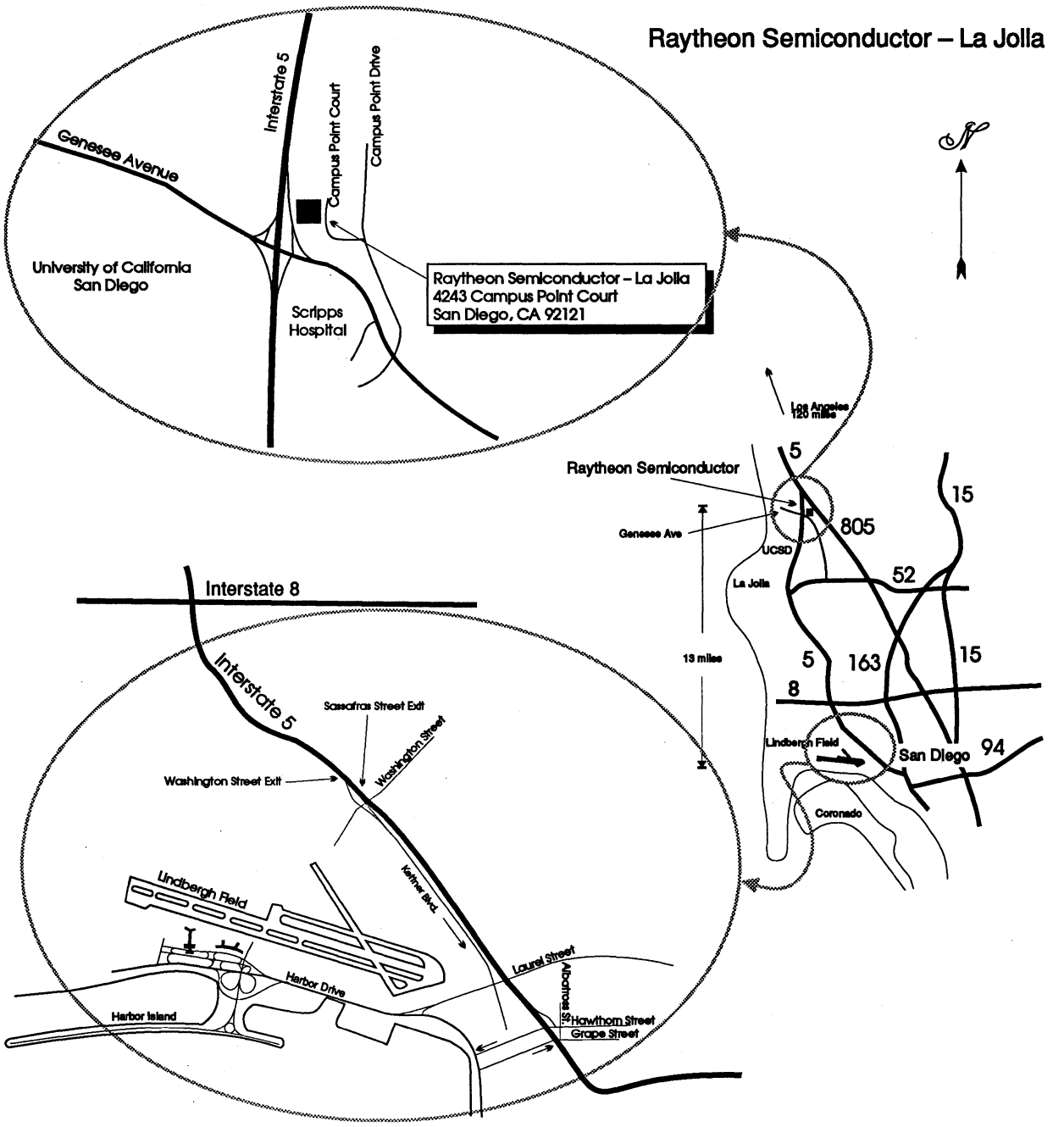
Raytheon Semiconductor – La Jolla



To Raytheon Semiconductor from Lindbergh Field (San Diego Airport): Exit the Airport going TOWARD SAN DIEGO. Go North on Interstate 5 (follow Harbor Drive - LEFT on Grape, LEFT on Albatross (under Freeway), cross Hawthorn and enter the freeway). Exit Interstate 5 at the Genesee Ave offramp (13 miles north of San Diego) and turn right (East). Proceed up the hill to Campus Point Drive (second stoplight) and turn left. Go to Campus Point Court (the first street) and turn left. Raytheon Semiconductor is on the left side of the street. Park in front of the building (first driveway) at the far end of the lot in visitors' parking and enter the front lobby.

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24413A

Notes

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- ❑ Digital Signal Processing
- ❑ Linear
- ❑ PROM
- ❑ Small Signal Transistors
- ❑ 32 Volt Linear Arrays
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- ❑ Precision Complementary BiCMOS Standard Cell Family (RSC4000)

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- ❑ Linear
- ❑ PROM
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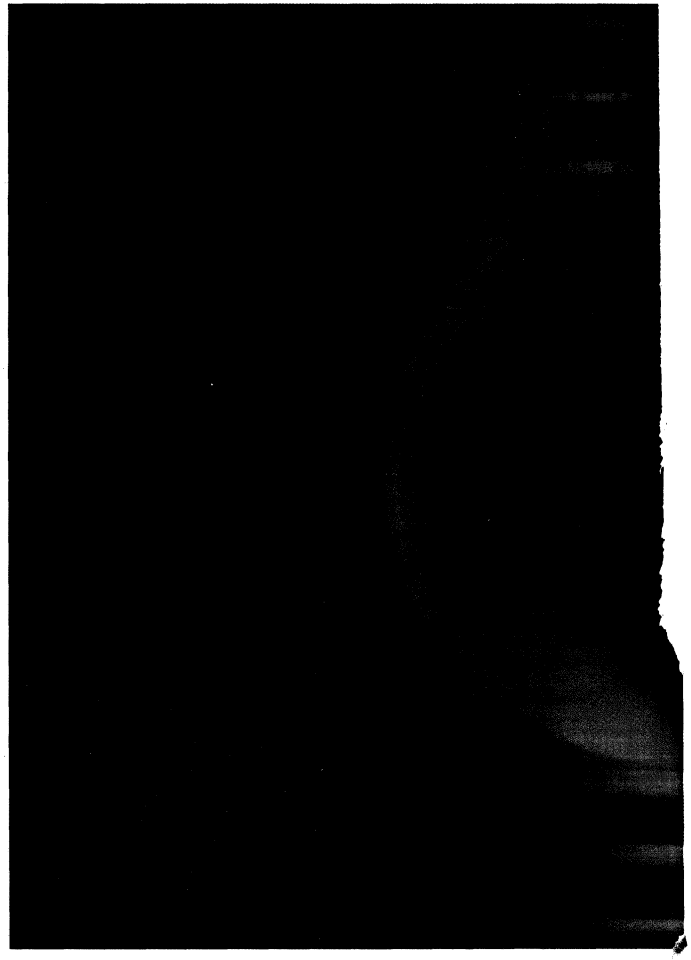

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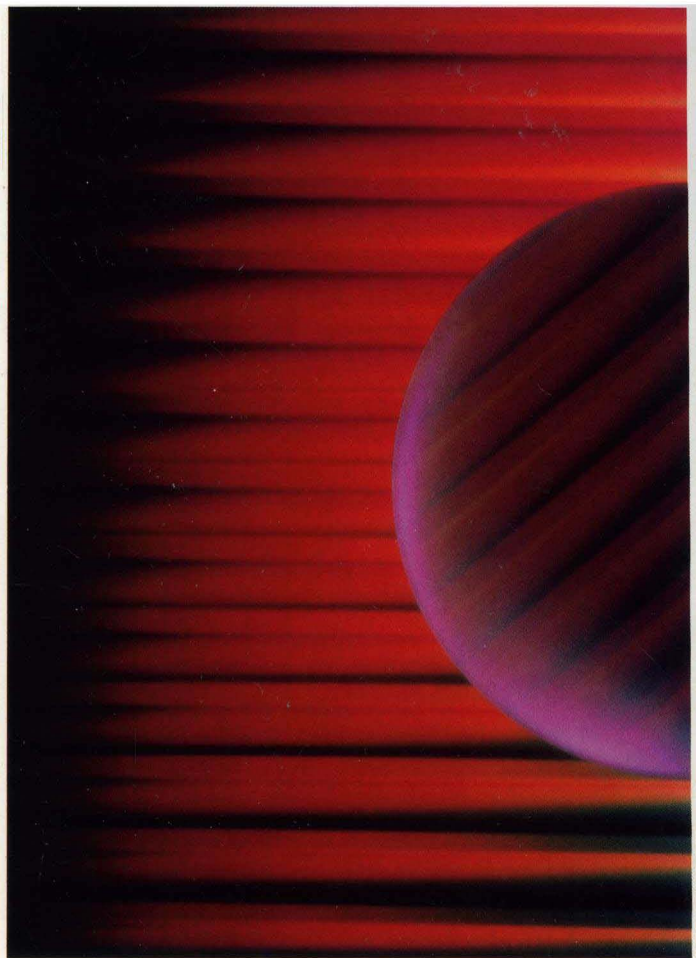

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