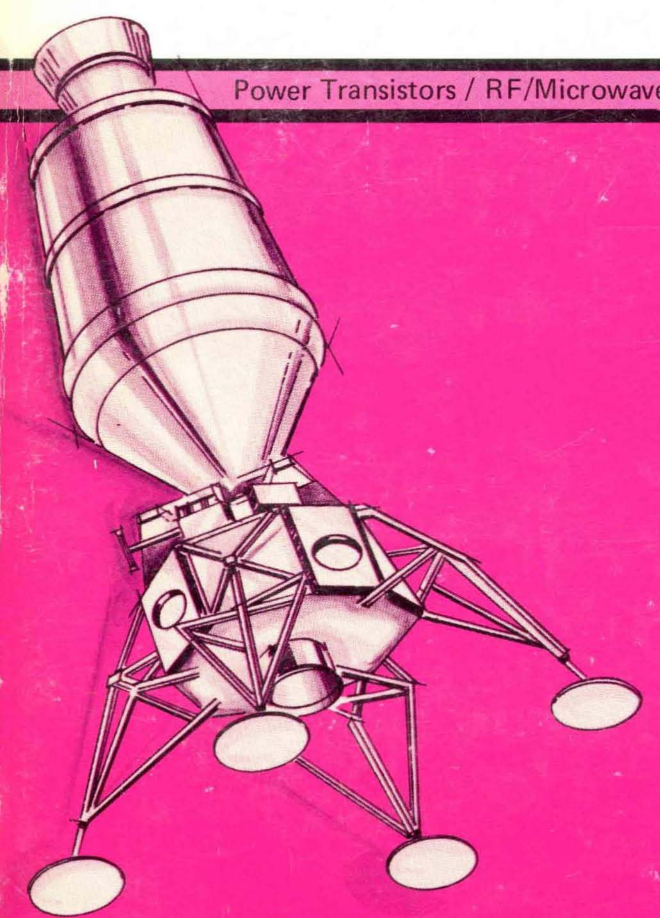
RCA

High-Reliability Devices

Power Transistors / RF/Microwave Devices / Integrated Circuits



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RCA
High-Reliability Devices

This DATABOOK contains descriptive text, data, and related application notes on high-reliability power transistors, rf power transistors, thyristors, and integrated circuits presently available from RCA Solid State Division as either standard or custom products. For ease of type selection, a complete index to these high-reliability devices is given on pages 6-10. Text material and data are then grouped according to type of devices: (a) power transistors, (b) rf power transistors, (c) thyristors, (d) linear and COS/MOS integrated circuits.

For ease of reference, data sheets in each category are arranged as nearly as possible in order of type-number sequence. Because some data sheets include more than one type number, however, some types may be out of sequence. If you don't find the number you're looking for where you expect it to be, please refer to the Index to Devices on pages 6-10.

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The RCA Solid State DATABOOKS are supplemented throughout the year by a comprehensive data service system that keeps you aware of all new device announcements and lets you obtain as much or as little product information as you need — when you need it.

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A ☐ Broadcast
B ☐ Communication
C ☐ Instrumentation/Control
D ☐ Computer/Data Processing
E ☐ Computer, Peripheral
F ☐ Automotive
G ☐ Industrial
H ☐ Medical
I ☐ Research
J ☐ Transportation
K ☐ Consumer, Electronic
L ☐ Consumer, Appliance
M ☐ Space
N ☐ Ordnance
O ☐ Avionics
P ☐ Electronic Warfare

Product Interest: (Indicate order of interest if more than one is marked)

A ☐ Linear IC's
B ☐ Digital IC's, COS/MOS
C ☐ Digital IC's, Bipolar
D ☐ Thyristors/Rectifiers
E ☐ Liquid Crystals
F ☐ Semiconductor Diodes
G ☐ RF Power Semiconductors
H ☐ MOSFETS
I ☐ Power Transistors
J ☐ Power Hybrid Circuits

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2N683*	212	SCR	25-A silicon controlled rectifier
2N684*	212	SCR	25-A silicon controlled rectifier
2N685*	212	SCR	25-A silicon controlled rectifier
2N686*	212	SCR	25-A silicon controlled rectifier
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2N688*	212	SCR	25-A silicon controlled rectifier
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2N690*	212	SCR	25-A silicon controlled rectifier
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2N3898*	217	SCR	35-A silicon controlled rectifier
2N3899*	217	SCR	35-A silicon controlled rectifier
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2N5446*	200	Triac	40-A silicon triac
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2N5568*	201	Triac	10-A silicon triac
2N5569*	201	Triac	10-A silicon triac
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*High-reliability versions of these types are available on a custom basis.

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JAN2N5039	35	PWR	High-speed n-p-n power transistor
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JAN2N5416	35	PWR	High-voltage n-p-n power transistor
JAN2N5671	34	PWR	High-speed n-p-n power transistor
JAN2N5672	34	PWR	High-speed n-p-n power transistor
JAN2N5838	36	PWR	High-speed n-p-n power transistor
JAN2N5839	36	PWR	High-voltage n-p-n power transistor
JAN2N5840	37	PWR	High-voltage n-p-n power transistor
JAN2N5918	83	RF	VHF/UHF n-p-n power transistor
JAN2N5919A	84	RF	VHF/UHF n-p-n power transistor
JAN2N6211	37	PWR	High-voltage p-n-p power transistor

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Type	Page	Product Line	Description
JAN2N6212	37	PWR	High-voltage p-n-p power transistor
JAN2N6213	37	PWR	High-voltage p-n-p power transistor
JANTX2N1479	30	PWR	Hometaxial-base n-p-n power transistor
JANTX2N1480	30	PWR	Hometaxial-base n-p-n power transistor
JANTX2N1481	30	PWR	Hometaxial-base n-p-n power transistor
JANTX2N1486	30	PWR	Hometaxial-base n-p-n power transistor
JANTX2N2857	80	RF	UHF n-p-n power transistor
JANTX2N3055	80	PWR	Hometaxial-base n-p-n power transistor
JANTX2N3375	81	RF	VHF/UHF n-p-n power transistor
JANTX2N3439	32	PWR	High-voltage n-p-n power transistor
JANTX2N3440	32	PWR	High-voltage n-p-n power transistor
JANTX2N3441	33	PWR	High-voltage n-p-n power transistor
JANTX2N3442	33	PWR	High-voltage n-p-n power transistor
JANTX2N3553	81	RF	VHF/UHF n-p-n power transistor
JANTX2N3585	34	PWR	High-voltage n-p-n power transistor
JANTX2N3771	34	PWR	High-current n-p-n power transistor
JANTX2N3772	34	PWR	High-current n-p-n power transistor
JANTX2N4440	81	RF	VHF/UHF n-p-n power transistor
JANTX2N5038	35	PWR	High-speed n-p-n power transistor
JANTX2N5039	35	PWR	High-speed n-p-n power transistor
JANTX2N5071	82	RF	VHF n-p-n power transistor
JANTX2N5109	83	RF	VHF/UHF n-p-n power transistor
JANTX2N5415	31	PWR	High-voltage n-p-n power transistor
JANTX2N5416	31	PWR	High-voltage p-n-p power transistor
JANTX2N5671	36	PWR	High-speed n-p-n power transistor
JANTX2N5672	36	PWR	High-speed n-p-n power transistor
JANTX2N5840	36	PWR	High-voltage n-p-n power transistor
JANTX2N5919A	84	RF	VHF/UHF n-p-n power transistor
JANTX2N6211	37	PWR	High-voltage p-n-p power transistor
JANTX2N6212	37	PWR	High-voltage p-n-p power transistor
JANTX2N6213	37	PWR	High-voltage p-n-p power transistor
JANTXV2N3375	81	RF	VHF/UHF n-p-n power transistor
ANTXV2N3553	81	RF	VHF/UHF n-p-n power transistor
ANTXV2N3584	34	PWR	High-voltage n-p-n power transistor
JANTXV2N3585	34	PWR	High-voltage n-p-n power transistor
JANTXV2N4440	81	RF	VHF/UHF n-p-n power transistor
S2400A*	218	SCR	4.5-A silicon controlled rectifier
S2400B*	218	SCR	4.5-A silicon controlled rectifier
S2400D*	218	SCR	4.5-A silicon controlled rectifier
S2400M*	218	SCR	4.5-A silicon controlled rectifier
S2600B*	219	SCR	7-A silicon controlled rectifier
S2600D*	219	SCR	7-A silicon controlled rectifier
S2600M*	219	SCR	7-A silicon controlled rectifier
S2610B*	219	SCR	3.3-A silicon controlled rectifier
S2610D*	219	SCR	3.3-A silicon controlled rectifier
S2610M*	219	SCR	3.3-A silicon controlled rectifier
S2620B*	219	SCR	7-A silicon controlled rectifier
S2620D*	219	SCR	7-A silicon controlled rectifier
S2620M*	219	SCR	7-A silicon controlled rectifier
S3700B*	220	SCR	5-A silicon controlled rectifier
S3700D*	220	SCR	5-A silicon controlled rectifier
S3700M*	220	SCR	5-A silicon controlled rectifier
S3701MI	221	SCR	5-A silicon controlled rectifier
S3704A*	222	SCR	5-A silicon controlled rectifier
S3704B*	222	SCR	5-A silicon controlled rectifier
S3704D*	222	SCR	5-A silicon controlled rectifier
S3704M*	222	SCR	5-A silicon controlled rectifier
S3704S*	222	SCR	5-A silicon controlled rectifier
S3714A*	222	SCR	5-A silicon controlled rectifier
S3714B*	222	SCR	5-A silicon controlled rectifier
S3714D*	222	SCR	5-A silicon controlled rectifier
S3714M*	222	SCR	5-A silicon controlled rectifier
S3714S*	222	SCR	5-A silicon controlled rectifier
S6400N*	217	SCR	35-A silicon controlled rectifier
S6410N*	217	SCR	35-A silicon controlled rectifier
S6420A*	217	SCR	35-A silcion controlled rectifier
S6420B*	217	SCR	35-A silicon controlled rectifier
S6420D*	217	SCR	35-A silicon controlled rectifier
S6420M*	217	SCR	35-A silicon controlled rectifier
S6420N*	217	SCR	35-A silicon controlled rectifier
S6431M*	224	SCR	35-A silicon controlled rectifier
S7430M*	214	SCR	35-A silicon controlled rectifier
S7432M*	215	SCR	35-A silicon controlled rectifier
T2300A*	204	Triac	2.5-A silicon triac
T2300B*	204	Triac	2.5-A silicon triac
T2300D*	204	Triac	2.5-A silicon triac
T2302A*	204	Triac	2.5-A silicon triac
T2302B*	204	Triac	2.5-A silicon triac
T2304B*	205	Triac	0.5-A silicon triac
T2304D*	205	Triac	0.5-A silicon triac
T2305B*	205	Triac	0.5-A silicon triac
T2305D*	205	Triac	0.5-A silicon triac
T2310A*	204	Triac	1.6-A silicon triac
T2310B*	204	Triac	1.6-A silicon triac
T2310D*	204	Triac	1.6-A silicon triac
T2312A*	204	Triac	1.9-A silicon triac
T2312B*	204	Triac	1.9-A silicon triac
T2312D*	204	Triac	1.9-A silicon triac
T2313A*	204	Triac	1.9-A silicon triac
T2313B*	204	Triac	1.9-A silicon triac
T2313D*	204	Triac	1.9-A silicon triac
T2313M*	203	Triac	1.9-A silicon triac
T2700B*	206	Triac	6-A silicon triac
T2700D*	206	Triac	6-A silicon triac
T2710B*	206	Triac	3.3-A silicon triac
T2710D*	206	Triac	3.3-A silicon triac
T4100M*	201	Triac	15-A silicon triac

* High-reliability versions of these types are available on a custom basis.

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T4101M*	201	Triac	10-A silicon triac
T4103B*	207	Triac	15-A silicon triac
T4103D*	207	Triac	15-A silicon triac
T4104B*	207	Triac	10-A silicon triac
T4104D*	207	Triac	10-A silicon triac
T4105B*	207	Triac	6-A silicon triac
T4105D*	207	Triac	6-A silicon triac
T4110M*	202	Triac	15-A silicon triac
T4111M*	202	Triac	10-A silicon triac
T4113B*	207	Triac	15-A silicon triac
T4113D*	207	Triac	15-A silicon triac
T4114B	207	Triac	10-A silicon triac
T4114D*	207	Triac	10-A silicon triac
T4115B*	207	Triac	6-A silicon triac
T4115D*	207	Triac	6-A silicon triac
T4120B*	202	Triac	15-A silicon triac
T4120D*	202	Triac	15-A silicon triac
T4120M*	202	Triac	15-A silicon triac
T4121B*	201	Triac	10-A silicon triac
T4121D*	201	Triac	10-A silicon triac
T4121M*	201	Triac	10-A silicon triac
T6401B*	208	Triac	30-A silicon triac
T6401D*	208	Triac	30-A silicon triac
T6401M*	208	Triac	30-A silicon triac
T6404B*	209	Triac	40-A silicon triac
T6404D*	209	Triac	40-A silicon triac
T6405B*	209	Triac	25-A silicon traic
T6405D*	209	Triac	25-A silicon triac
T6411B*	208	Triac	30-A silicon triac
T6411D*	208	Triac	30-A silicon triac
T6411M*	208	Triac	30-A silicon triac
T6414B*	209	Triac	40-A silicon triac
T6414D*	209	Triac	40-A silicon triac
T6415B*	209	Triac	25-A silicon triac
T6415D*	209	Triac	25-A silicon triac
T6421B*	208	Triac	30-A silicon triac
T6421D*	208	Triac	30-A silicon triac
T6421M*	208	Triac	30-A silicon triac
T8401B*	210	Triac	60-A silicon triac
T8401D*	210	Triac	60-A silicon triac
T8401M*	210	Triac	60-A silicon triac
T8411B*	210	Triac	60-A silicon triac
T8411D*	210	Triac	60-A silicon triac
T8411M*	210	Triac	60-A silicon triac
T8421B*	210	Triac	60-A silicon traic
T8421D*	210	Triac	60-A silicon triac
T8421M*	210	Triac	60-A silicon triac
T8430B*	211	Triac	80-A silicon traic
T8430D*	211	Triac	80-A silicon traic
T8430M*	211	Triac	80-A silicon triac
T8440B*	211	Triac	80-A silicon triac
T8440D*	211	Triac	80-A silicon triac
T8440M*	211	Triac	80-A silicon triac
T8450B*	211	Triac	80-A silicon triac
T8450D*	211	Triac	80-A silicon triac
T8450M*	211	Triac	80-A silicon triac

*High-relaibility versions of these types are available on a custom basis.

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Introduction to High-Reliability Solid-State Devices

The advent of the transistor in 1948 marked a dramatic step forward in the potential reliability of electronic equipment. Much of this solid-state reliability potential has been realized and, without doubt, has played a key role in the phenomenal growth and diversification of electronics over the past two decades. In spite of this achievement, however, the demand and need for greater reliability assurance in solid-state devices continues to grow.

Electronic systems continue to grow more complex as more comprehensive functions are provided. In the process, greater quantities, or more sophisticated and complex devices are used. The development cycle for systems continues to decrease so that less and less time is available for component reliability testing in operating systems. Electronics systems are becoming interlocked with huge dollar investments, with the social and political fabric of society, and with vital national security to such a degree that a system failure may have immediate and visible impact. Consumers are demanding better warranties at a time when service costs are rising rapidly. Further, a dynamic solid-state technology rapidly generates new devices that offer even greater functional and reliability potential.

Solid-state devices classified as high-reliability types have come to be primarily associated with military and aerospace applications. In many ways, this association is misleading because the commercial equipment market is probably the largest user of high-reliability products, but not necessarily by that label. Military and aerospace agencies, however, have been largely responsible for establishment of comprehensive published reliability specifications and standards which have been accepted by the solid-state industry. MIL standards dominate the procedures used to specify high-reliability solid-state devices and represent a common reference point frequently used by commercial users to define their requirements.

Commercial High-Reliability Requirements

The dominant market for solid-state devices today is commercial. The bulk of the parts produced are initially designed, developed, and manufactured to meet specific functional, quality, and reliability needs of a class of commercial electronic equipment. Commercial equipment tends to be evolutionary and to be produced continuously over longer periods and in larger quantities than is the case with equipment for military and aerospace systems. At the outset, the commercial user is more likely, than is the military and aerospace user, to be involved in influencing the solid-state device manufacturer to his particular functional and economic requirements. His opportunity to evaluate early devices and influence corrective measures for his application is greater. All these factors enhance the ability of both the solid-state manufacturer and the user to reach a balance between reliability and economics which matches a particular need.

One of the most important factors, which brings lower cost to the commercial user without sacrifice in reliability, is his ability, together with that of the manufacturer, to identify accurately over a period of time a few relatively simple controls and/or screens which can be used to effectively eliminate potential failures in his particular application. This ability is possible because his application is specific and continuous, and device volumes are considerable. The commercial user generally achieves the reliability he requires without elaborate specifications and with a minimum of administrative procedures.

Military and Aerospace High-Reliability Requirements

Military and aerospace requirements for high-reliability solid-state devices are extremely large and diverse, not only in terms of performance, operating conditions, and reliability, but also in terms of logistics and procurement. As a result of these requirements, the military services have jointly developed specifications and standards under which most military end-use solid-state devices are procured. To simplify procurement, logistics, and the development of reliability data, MIL specs are not issued for the full spectrum of devices manufactured; rather, they are restricted to those devices for which significant need is demonstrated and are specified so that the device can have as wide applicability as possible. Although the limits for operating conditions may exceed those required for some applications, they simplify procurement and assure a supply of devices for the majority of military equipment. These standards also cover a wide range of requirements for the manufacturer on such things as:

(a) The procedure and requirements for a manufacturer to become certified to manufacture MIL-spec parts.
(b) The requirements for qualifying parts.
(c) Product-assurance provisions in such areas as quality control, inspection procedures, personnel training, cleanliness, failure analysis, and documentation.
(d) Test methods and procedures.
(e) Marking and identification of product.
(f) Preservation and packing.

A large number of transistor types are covered by published military specifications. Specifications for microcircuits (integrated circuits) are relatively new, and only a limited number of military specifications have been approved and issued. Many types of devices, both transistors and integrated circuits, are not covered by military specifications, either because they are too new

or are not used in sufficient quantities. Many of these devices offer the most recent technological advances or have special performance characteristics which offer advantages to the designer of high-reliability equipment. RCA cooperates with the users of such devices in establishment of high-reliability specifications, patterned after MIL standards, which allow these devices to be approved for use in military and aerospace systems, as well as commercial equipment. If the use warrants, these specifications may be submitted by RCA, or the user, to the cognizant military specification agency as candidates for MIL approval as a standard type.

Most procurements of solid-state devices for military systems are made by the equipment contractor from the MIL-STD parts list as awards are received for electronic equipment. Some military and aerospace programs, because of their size, duration, or special requirements (Minuteman and Apollo are two examples), require that special specifications and process methods, or even special production lines, be established and tailored to the particular functional, reliability, and economic needs of the program. RCA Solid State Division has frequently used the resources of its laboratories, production facilities, and expert technical staff to contribute to the success of such programs.

Military Specifications

There are two major military specifications used for the procurement of standard solid-state devices by the military. These specifications are MIL-S-19500, which covers devices such as discrete transistors, thyristors, and diodes, and MIL-M-38510, which covers microcircuits, both hybrid and monolithic.

MIL-S-19500 is the specification for the familiar "JAN" transistors. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center. At present, approximately five hundred detailed electrical specifications are included in the MIL-S-19500 system.

Three levels of reliability, JAN, TX, and TXV, are defined by MIL-S-19500. Devices designated as JAN types receive lot screening only and are the least expensive. Devices designated as TX receive some 100-per-cent screening (primarily burn-in) and a tight lot-sampling plan. Not all detailed specifications include TX requirements. Devices designated as TXV are tested the same as TX devices; however, they receive an additional visual inspection prior to sealing the package. Only a few detailed specifications include TXV testing.

The Defense Electronic Supply Center maintains a "Qualified Products List" of all vendors qualified to produce devices in accordance with MIL-S-19500. This list is published periodically and is available to manufacturers of military equipment. NASA, to date, has not been a heavy user of MIL-S-19500, preferring instead to procure devices to their own specifications.

MIL-M-38510 is the relatively new military specification for microcircuits. This specification is far more demanding than MIL-S-19500 and presently only a few vendors have parts on the Qualified Products List. MIL-M-38510 also defines three levels (classes A, B, and C) of reliability testing. These levels, however, are markedly different from those defined by MIL-S-19500. Class A, the highest level, is intended primarily for flight and other highly critical applications. Class A devices undergo a lengthy list of 100-per-cent screens, plus a tight lot-sampling plan. Class B devices are intended for general military usage and undergo less (but still extensive) 100-per-cent testing than Class A units. Class C devices undergo the least amount of 100-per-cent testing and are, of course, the least expensive.

Approximately 40 detailed specifications are currently included in the MIL-M-38510 system. A Qualified Products List for these devices is maintained by the Defense Electronic Supply Center. NASA is now starting to use MIL-M-38510 specifications.

Both MIL-M-38510 and MIL-S-19500 attempt to make available to the designer of military equipment a list of standard, qualified, general-purpose parts which are acceptable to the military. Although MIL-S-19500 and MIL-M-38510 do not cover every solid-state device available on the market, and do not attempt to do so, enough devices are available to build the majority of military equipment. Use of these devices makes the job of spare-parts inventory far simpler for the military and the job of specification negotiations far easier for the equipment manufacturer.

Special Terms and Definitions

Acceptable Quality Level (AQL) is the maximum percent defective (or the maximum number of defects per hundred units) that for purposes of sampling inspection, can be considered satisfactory as a process average.

Acceptable Reliability Level (ARL) is a nominal value expressed in terms of percent failures per 1000 operating hours specified for acceptance of parts or equipment. It is the level of reliability that will be accepted at some confidence level by a reliability sampling plan.

Acceptance/Rejection Criteria is the extent of defectiveness allowed in a sample of tested product which will assure the quality level specified.

Assignable Causes of Variation are other-than-chance causes, such as unexpected and abnormal variations in material and machines, lack of skill or carelessness in manual operations, abnormal changes in power supply, rough handling, etc. These causes normally can be identified and eliminated economically.

Average is the arithmetic mean of a set of **n** numbers. The average is obtained by dividing the sum of the numbers by **n.**

Average Outgoing Quality (AOQ) is the average outgoing quality of product after 100 percent inspection of rejected lots, with replacement by good units of all defective units found in inspection.

Average Outgoing Quality Limit (AOQL) (in outgoing product after inspection) is the maximum value of the AOQ that a sampling plan will assure over a long period of time, no matter how defective the product may be when submitted for inspection.

Indifference Quality Level (IQL) is the product quality which will be accepted as often as it is rejected. It has a 0.50 probability of acceptance.

Burn-in is a process of "shakedown" operation of each item of finished product that is performed prior to placing the item in use.

Catastrophic Failure is a sudden change in the operating characteristics of the product which would cause the item to be inoperative (e.g., circuit opens or shorts, structural failure, etc.).

Chance or Random Failure is a failure that occurs at random within the operational time of the product after all efforts have been made to eliminate design and before wear-out becomes the predominant cause of failure.

Characteristic is a trait, property, or feature of a specified item, type of item, or group of items.

Confidence Level is the degree of desired trust or assurance in a given result. A confidence level, which always is associated with some assertion, measures the probability that a given assertion is true.

Confidence Interval is a range of values that is believed to include, with a preassigned degree of confidence (confidence level), the true value of a characteristic of the lot or universe for a given percentage of the time. For example, 95% confidence limits for a sample of 10 with a ratio of successes to total number tested of 0.9 (9 successes and 1 failure) would be 0.54 and 1.0; that is, even with an observed success ratio of 0.9 (90%), the best that can be said is that the true ratio lies between 0.54 (54%) and 1.0 (100%) as estimated 95% of the time.

Consumer's (Beta, β) Risk is the probability that a sampling plan will accept unsatisfactory material. Consumer's risk normally is associated with the lot tolerance percent defective (LTPD) having a probability of acceptance of 0.10.

Control Chart (Quality) is a chart identifying the expected level of a characteristic and statistical control limits placed above and/or below this level. Successive values of some quality measure (e.g., defects-per-unit, defectives, percent defective, averages, etc.) are plotted on this chart for judging patterns and significant variations in the characteristic.

Control Limits (Quality) are the statistical limits (usually designated in multiples of the standard deviation) of the characteristic measured, such as defects per unit, defectives, percent defective, averages, etc., about the expected level. Values fluctuating within the control limits are considered comparable to the expected quality level. Value falling outside these limits indicate a significant change in the measured characteristic.

Defect is the occurrence, in an individual element or part, of a characteristic which fails to meet the specified standard.

Defective is the status of an individual article that contains one or more defects.

Degradation Failure is a failure that results from a gradual change in performance characteristics with time to a value outside the specified limits of the product but would not cause the item to be inoperative.

Environment is the aggregate of all the conditions and influences that can affect the operation of the product (e.g., temperature, humidity, acceleration, shock, vibration, radiation, etc.).

Failure Mechanism is the basic physical or chemical cause for failure.

Failure Mode is the characteristic which was observed to fail.

Failure Rate is defined as the number of failures within a time interval. In the case of exponentially distributed times-to-failure, the failure rate is defined as the reciprocal of mean-time-to-failure (i.e., failure rate equals 1/m, where m is the mean time between failures).

Heterogeneity is a state or conditions of dissimilarity of nature, kind, or degree.

Homogeneity is a state or condition of similarity of nature, kind, or degree.

Inherent Reliability is maximum reliability attainable with an item of a particular design.

Inspection (Final) is the application of an inspection act, just prior to shipment of the product. Shipment in this case may be to the customer, to a storage area, or to assembly shops within RCA, where the product in question becomes a component of a larger unit of product.

Inspection (Process) is the application of an inspection act at various stages in the manufacturing process prior to the final stage.

Inspection Act is the determination of conformance to specified requirements and general standards of acceptable workmanship.

Inspection Item is any specific requirement, characteristic, or feature for which inspection is made.

Inspection Lot, for purposes of acceptance–sampling inspection, is defined as an aggregation of articles submitted for inspection at one time that has been produced, as far as practicable, under what are judged to be essentially the same conditions.

Inspection Point is a designated position within the manufacturing process at which inspection effort is applied.

Inspection by Attributes is the determination of conformance of a particular inspection item without reference to degree or magnitude. For example, go/no-go testing.

Inspection by Variables consists of a determination of the magnitude of the characteristic covered by the inspection item and use of approved statistical quality control techniques to determine conformance to specifications.

Lambda, λ (Life Test Failure Rate) is defined as the lot tolerance percent defective (LTPD) per 1000 hours.

Lot Tolerance Percent Defective (LTPD) is the percent defective of a sampling plan for which the probability of acceptance is low (commonly 10% probability of acceptance unless otherwise stated).

Mean Time Between Failures (MTBF) is the average time between failures.

Operating Time is the time during which power is applied to an item.

Parameter is a quantity or value that remains constant within a given set of conditions (i.e., is subject to change only if the conditions change).

Population (Universe) is the total collection of units from a common source.

Precision is the degree to which repeated observations of a class of measurements conform to themselves.

Process Average is the average percent defective or average number of defects per hundred units of product found during initial inspection. Initial inspection is the first inspection of product (as distinguished from inspection of product resubmitted after prior rejections) and includes only first sample results where multiple sampling plans are used.

Producer's (Alpha, α) Risk is the probability that a sampling plan will reject satisfactory material. Producers risk normally is associated with a percent defective which has a probability of rejection of 0.05.

Random Selection is the selection of items from a population in a manner such that each item has an equal and independent chance of being elected.

Range is the difference between the greatest and the least of a set of variate values.

Real Time Control is a continuous acceptance and interpolation of data against established criteria.

Redundancy is the existence of more than one means for accomplishing a given task in which more than one means must fail before there is an overall failure of the system.

Reliability (Mathematical) is the probability of an item performing its intended purpose for a specified period of time under given conditions.

Sample is a group of items chosen by random selection.

Sampling Inspection is a random and representative selection of a portion of the units from a lot in accordance with the specified sampling plan. Each unit in the selected sample is inspected to determine whether or not each unit conforms to specification requirements.

Sampling Plan is an inspection plan that specifies sample sizes and criteria for accepting or rejecting an inspection lot based on the results of inspecting the sample.

Shelf Life is the length of time an item can be stored under specified conditions and still meet specified requirements with a specified level of assurance.

Specification is a detailed description of the characteristics of a product and of the criteria that must be used for determining whether the product conforms to the description.

State of the Art is the level at which technology has been developed at any period of time.

Stratified Sample is a group of items selected from sublots so that the number of items included in the sample from each sublot is proportional to the size of the sublot. Random selection of items from within each sublot is required.

Tolerance is the allowable variation in measurements within which an item is judged acceptable.

Useful Life is the total operating time between burn-in and wear-out.

Variables Testing is a test procedure in which the items under test are classified according to quantitative, rather than qualitative, measure of characteristics.

High-Reliability Power Transistors

High-Reliability Power Transistors

A number of factors such as second breakdown, power dissipation, current and voltage ratings, maximum operating areas, temperature, and thermal-fatigue considerations affect the performance and reliability of power transistors in various circuit applications. These factors define the maximum limits of reliable transistor operation for both steady-state and pulsed conditions. Each of these factors must be given careful consideration in the development and production of power transistors for military, aerospace, and critical industrial applications for which high reliability is a prime objective. In such applications, replacement of defective parts is often difficult or impossible or may result in considerable expense. Care must be taken to assure that field failure rates are held to an absolute minimum. The following guidelines should be followed in an effort to achieve this objective.

Electrical Considerations:

Voltage Breakdowns	Device voltages should be limited to 70 per-cent of the maximum rates values.
Current Gain	A margin of 15 to 20 per cent above the required values should be provided to allow for degradation.
Second-Breakdown Energy Tests	Sufficient $I_{S/b}$ protection must be provided for forward-bias conditions and sufficient $E_{S/b}$ protection must be provided for inductive circuits.

Reliability Considerations:

High-Temperature Tests	Such tests are required to guarantee high-temperature performance.
Low-Level Leakage Tests	Test for stability.
Delta Temperature Tests	Adequate heat sinks must be provided so that case temperature is held to a minimum.
Operating Temperature	Device operating temperatures should be limited to 50 to 75 per cent of maximum rated values.
Transistor Protection	Circuits should include provisions to protect power transistors against electrical transients.

Second Breakdown

Second breakdown is a potentially destructive phenomenon that can occur in all power transistors within the maximum current and voltage ratings of the device. A simplified explanation is that localized thermal regeneration occurs, and the transistor exhibits a lower value of breakdown voltage, referred to as the "second breakdown". The lower value of voltage results from thermal generation of charge-carrier pairs (holes and electrons) at high localized temperatures which alter the conductivity of the semiconductor in that vicinity. This localized effect reduces the ability of the transistor to support the applied voltage. Fig. 2-1 shows qualitatively what happens under primary or second breakdown.

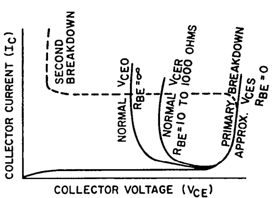

Fig. 2-1–Primary and secondary breakdown voltages.

Reverse-Bias Second Breakdown—Reverse-bias second breakdown is a phenomenon that may occur when the collector current continues to flow under reverse-bias conditions and causes the injected current to be concentrated in the central portions of the emitter, in contrast to the normal edge injection of the current. If the injected current is severely restricted to a very small central area by a large reverse emitter-base bias, the current density can rise to very large levels—in the order of thousands of amperes per square centimeter. If the collector of the transistor is of high-resistivity silicon, the high current density may inject a density of charge carriers that is equal to or greater than the collector impurity density. In this local region, the base widens and the collector depletion layer expands until the injected current density is smaller than the collector impurity density. If the current density is sufficiently high, the collector depletion layer expands to a more heavily doped collector region, such as an epitaxial substate. When the collector depletion layer expands, the collector breakdown voltage is governed by the impurity gradient related to the base doping and the heavily doped collector. The collector breakdown voltage normally supports only a fraction of the original

voltage, and the second-breakdown voltage results. The thermal effects from the large current densities also contribute to the regeneration process. Fig. 2-2 shows the process of reverse-bias second breakdown.

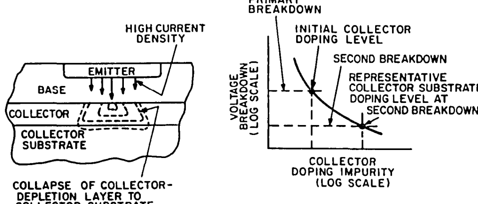

Fig. 2-2– Reverse-bias second breakdown.

In an inductive circuit, a situation exists such that collector current flows in the forward direction while the transistor is being turned off, and a high voltage is induced across the device. As a result, the transistor enters the sustaining region. The hot spot that forms during reverse-bias second breakdown may then be generated by current crowding in the depletion region, as shown in Fig. 2-3.

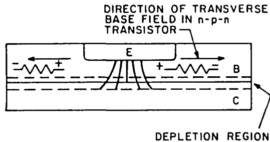

Fig. 2-3– Cross section showing current crowding that occurs during reverse-bias second breakdown.

The reverse base current that flows laterally through the base region creates an electric field. For an n-p-n transistor, electrons flow from the emitter to the collector across the base region. The field causes these carriers to flow mainly from the center of the emitter, because the emitter-base forward bias is greatest at this point. Because the device is in the sustaining region as a result of circuit conditions, a depletion region is present. Carriers (electrons) that flow across this region, which resembles two plates of a capacitor, decrease in potential. Therefore, energy is transformed to heat and causes a hot spot and possibly reverse-bias second breakdown ($E_{S/b}$). Typical examples of this situation are circuits, such as those shown in Fig. 2-4, in which an unclamped inductive load or a non-commutated leakage inductance is present.

Anything that increases the transverse base field aggravates hot-spot formation. Therefore, higher reverse base currents that result from decreased base-drive resistance or higher reverse voltages diminish $E_{S/b}$ capability, as shown in Fig. 2-5. This figure shows the effect of variations in the external base-to-emitter resistance R_{BE}, the reverse base-to-emitter voltage V_{BE}, and the load inductance L.

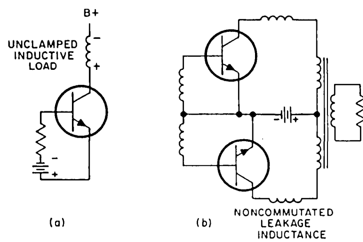

Fig. 2-4– Examples of (a) unclamped inductive loads and (b) uncommutated leakage inductance.

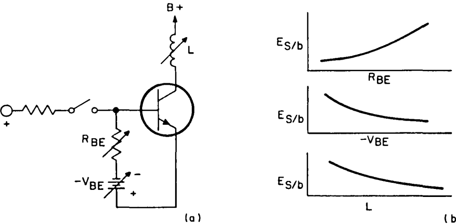

Fig. 2-5– (a) Typical inductive-load circuit and (b) variation of second-breakdown capability as a function of circuit parameters.

A test set which makes the measurement of reverse-bias second breakdown possible and also protects the transistor being tested is shown in Fig. 2-6. A test cycle includes the following steps:

1. The transistor is driven to the desired collector-current level in saturation.
2. The transistor is reverse-biased.
3. The transistor enters the sustaining region, VCEX(sus).
4. Energy is absorbed by the transistor.

If failure occurs, high-frequency noise is sensed at the base of the transistor. A "crowbar" (transistor) in parallel with the transistor being tested is then turned on, and energy is shunted through this "crowbar" to protect the transistor undergoing the test. Fig. 2-7 shows the voltage-current relationship during the reverse-bias second-breakdown ($E_{S/b}$) test.

Forward-Bias Second Breakdown—Forward-bias second breakdown is somewhat different from reverse-bias second breakdown. As shown in Fig. 2-8, the localized heating results because the current density J crosses the depletion region (collector field) V_c to yield a power density P. As P increases, more current

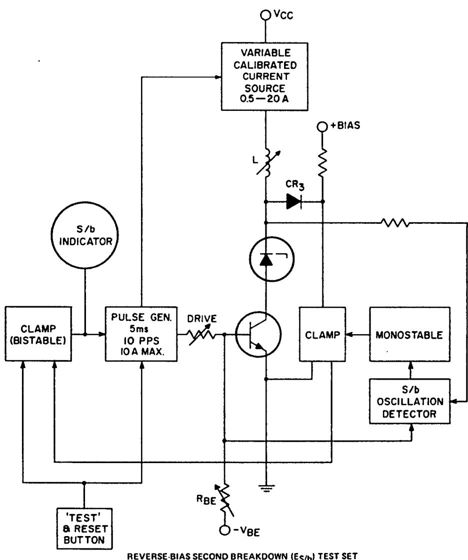

Fig. 2-6– Reverse-bias second-breakdown ($E_{S/b}$) test set.

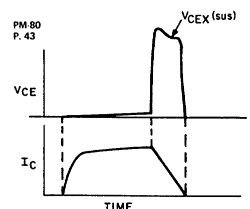

Fig. 2-7– Waveforms during second-breakdown ($E_{S/b}$) test.

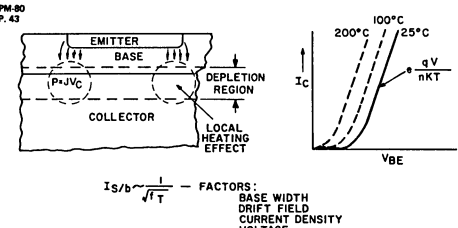

Fig. 2-8– Forward-bias second breakdown.

is injected into the localized area. The increase in current is caused by a decrease in the localized V_{BE}, at an approximate rate of 2 millivolts per °C. The local system becomes regenerative as more heat from the increased power density reduces V_{BE} and thereby increases the current injection.

The forward-bias second-breakdown current, $I_{S/b}$, is defined as the current at the onset of second breakdown, and is closely related to the collector field V_C, the current density J, and other properties of the transistor. Forward-bias second breakdown is also related to charge-carrier transit time across the base region, and is controlled by base width and any accelerating fields that exist in the base. The longer the transit time required for the charge carrier to cross the base, the more lateral diffusion of the charge and thus the greater the reduction in the current density at the edge of the collector depletion layer. This diffusion effect, referred to as "fan-out," is enhanced by wide base widths and homogeneously doped bases. Because the forward-bias second breakdown is related to the base width, it is also related to frequency response. For a given structure, this frequency relationship is expressed by the following empirical equation:

$$I_{S/b} \approx \left(\frac{1}{\sqrt{f_T}}\right)^K$$

Operation in the forward-bias region subjects the transistor to simultaneous current and voltage. This condition causes current concentrations as previously discussed. This type of rating must be considered for all linear applications of transistors.

The block diagram of a nondestructive second-breakdown test set is shown in Fig. 2-9. The transistor under test is in series with a pass transistor and is driven by a differential amplifier at a current level selected by the operator. The level selected is independent of transistor current-transfer ratio. The pass transistor is operated out of saturation, so that fast turn-off is possible. A second differential amplifier senses the voltage across the pass transistor and the 1-ohm resistor in series with it. This voltage is held constant throughout the test to improve the accuracy of the second-breakdown voltage reading. The circuit is arranged so that only the collector current of the transistor under test passes through the 1-ohm resistor. The voltage across this resistor, therefore, provides an accurate indication of collector current.

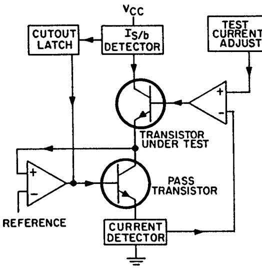

Fig. 2-9– Block diagram of test set for forward-bias second-breakdown current ($I_{S/b}$).

The onset of second breakdown is detected by use of the primary of a pulse transformer connected in series with the collector of the transistor under test. Under second-breakdown conditions, the rapid rate of rise of collector current induces a voltage L(di/dt) in the transformer secondary which is coupled to the input circuit of the series pass transistor. This voltage turns off the series pass transistor in one microsecond. Simultaneously, a voltage is developed across the transformer primary of a polarity that immediately reduces the voltage across the transistor under test. The inductance of the transformer also aids in limiting immediate current rise in the transistor being tested.

The test-set characteristics, together with the protective cutout circuit, prevent damage to the transistor during the second-breakdown test. The complete cutout time of the actual test set is approximately one microsecond; this value is sufficient to prevent destruction of any transistor currently available.

The pulse width of the voltage and current applied to the transistor under test can be varied from 0.5 millisecond to several seconds. For dc second-breakdown tests, a pulse width of 0.5 to 2 seconds is required because the thermal time constant of the power-transistor pellet and mounting block may be several tenths of a second.

A comparison of energy-handling capability for several transistor structures is shown in Table 2-1.

Table 2-1-Comparison of Energy-Handling Capability

	I_C x V_{CEO} (1-Second pulse)	Forward Bias Energy Handling at V_{CEO} Limit J	Reverse-Bias Energy $E_{S/b}$ mJ
	Doped - $\pi\nu$		
2N5240	0.08 x 300	24	1.6
2N5840	0.02 x 350	7.0	0.45
	Double-diffused, double-epitaxial		
2N5038	0.25 x 90	22.5	13
2N5672	0.12 x 120	14.4	20
2N6032	0.05 x 120	6	40
2N3879	0.09 x 75	6.85	1.0
	Hometaxial- Base		
2N5578	1.5 x 70	105	800
2N3055	1.9 x 60	115	170
2N3773	0.6 x 140	84	310

Inductive Voltage-Breakdown Testing

In most practical applications of transistors, the highest voltage that appears across the transistor results from the turn-off of the transistor, because the transistor switches from a high-current "on" state to a "cut-off" state. Inductive testing simulates this condition very closely, as shown in Fig. 2-10. Curve-tracer testing, on the other hand, subjects the transistor to an increasing voltage until the required current is achieved; i.e., the

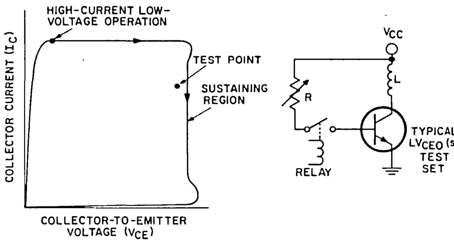

Fig. 2-10– Inductive voltage-breakdown testing of a transistor: (a) load line; (b) test circuit.

high-current, high-voltage measuring point is approached from the other direction with the collector current I_C lagging the collector-to-emitter voltage V_{CE}, as shown in Fig. 2-11. Unless sufficient current is supplied to the place the transistor in the sustaining region, the breakdown voltage measured is artificially high. If this high current is passed through a transistor with a high breakdown voltage, a high dissipation results. This dissipation is not uniformly distributed over the whole junction, but tends to concentrate in the spots with the lowest breakdown. This concentration is further aggravated when the base-to-emitter junction is reverse-biased. The small areas that break down first form hot spots. These hot spots result in further current concentration with time, and possible device destruction. Fig. 2-12 shows the test circuit used in the curve-tracer test.

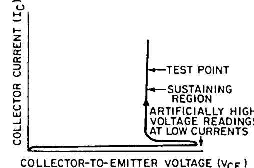

Fig. 2-11– Load line for curve-tracer voltage-breakdown testing.

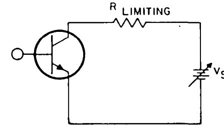

Fig. 2-12– Test setup for curve-tracer voltage-breakdown testing.

The 8-millisecond sweep of a curve tracer is relatively slow compared to inductive sweeping. This sweep allows time for the current to concentrate and to deliver an appreciable and variable amount of energy. Inductive testing, on the other hand, delivers a relatively fixed amount of energy in a short time (0.6 millisecond maximum for the 2N4348 transistor). Less concentration of current is allowed, and the test is potentially less destructive and provides a more realistic rating. Curve-

tracer testing may reject transistors that will operate satisfactorily in any practical application because the opportunity for the occurrence of hot spots is increased, and lower values of V_{CEO} are measured.

Effect of Temperature on Silicon Transistors

The characteristics of transistors vary with changes in temperature. In view of the fact that most circuits operate over a wide range of environments, a good circuit design should compensate for such changes so that operation is not adversely affected by the temperature dependence of the transistors.

Current Gain—The effect of temperature on the gain of a silicon transistor is dependent upon the level of the collector current, as shown in Fig. 2-13. At the lower current levels, the current-gain parameter h_{FE} increases with temperature. At higher currents, however, h_{FE} may increase or decrease with a rise in temperature because it is a complex function of many components.

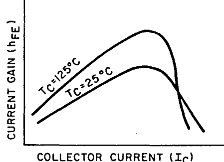

Fig. 2-13– Current gain as a function of collector current at different temperatures.

Base-to-Emitter Voltage—Fig. 2-14 shows the effect of changes in temperature on the base-to-emitter voltage (V_{BE}) of silicon transistors. Two factors, the base resistance ($r_{bb'}$) and the height of the potential barrier at the base-emitter junction ($V_{BE'}$), influence and behavior of the base-to-emitter voltage. As the temperature rises, material resistivity increases; as a result, the value of the base resistance $r_{bb'}$ becomes greater. The barrier potential $V_{BE'}$ of the base-emitter junction, however, decreases with temperature. The following equation shows the relationship between the base-to-emitter voltage and the two temperature-dependent factors:

$$V_{BE} = I_B r_{bb}' + V_{BE}'$$

$$= \frac{I_C}{h_{FE}} r_{bb}' + V_{BE}'$$

As indicated by this equation, the base-to-emitter voltage diminishes with a rise in temperature for low values of collector current, but tends to increase with a rise in temperature for higher values of collector current.

Collector-to-Emitter Saturation Voltage—The collector-to-emitter saturation voltage $V_{CE}(sat)$ is affected primarily by collector resistivity (ρ_C) and the

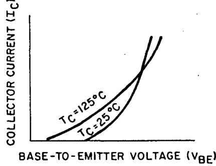

Fig. 2-14– Collector current as a function of base-to-emitter voltage at different temperatures.

amount by which the natural gain of the device (h_{FE}) exceeds the gain with which the circuit drives the device into saturation. This latter gain is known as the forced gain (h_{FEf}).

At lower collector currents, the natural h_{FE} of a transistor increases with temperature, and the IR drop in the transistor is small. The collector-to-emitter saturation voltage, therefore, diminishes with increasing temperature if the circuit continues to maintain the same forced gain. At higher collector currents, however, the IR drop increases, and gain may decrease. This decrease in gain causes the collector-to-emitter saturation voltage to increase and possibly to exceed the room-temperature (25°C) value. Fig. 2-15 shows the effect of temperature on the collector-to-emitter saturation voltage.

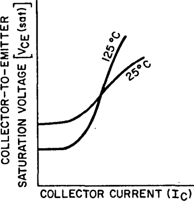

Fig. 2-15– Collector current as a function of collector-to-emitter saturation voltage at different temperatures.

Collector Leakage Currents—Reverse collector current is a resultant of three components, as shown by the following equation:

$$I_R = I_D + I_G + I_S$$

Fig. 2-16 shows the variations of these components with temperature.

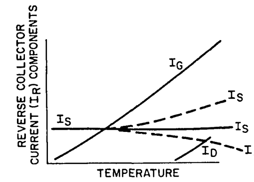

Fig. 2-16– Reverse collector current as a function of temperature.

The diffusion or saturation current I_D is a result of carriers that diffuse to the collector-base junction and are accelerated across the depletion region. This component is small until temperatures near 175°C are reached. The component I_G results from charge-generated carriers that are created by the flow of diffusion carriers across the depletion region. This component increases rapidly with temperature. I_D and I_G are referred to as bulk leakages. The term I_S represents surface leakage which is caused by local inversion, channeling, ions, and moisture. This leakage component is dependent on many factors, and its variations with changes in temperature are difficult to predict.

At low temperatures, either surface or bulk leakage can be the dominant leakage factor, particularly in transistors that employ a mesa structure. At high temperatures, charge-generated carriers and diffusion current are the major causes of leakage in both mesa and planar transistor structures; the current I_G, therefore, is the dominant leakage component. Because of the dominance of surface leakage I_S at low temperatures and the fact that this leakage may vary either directly or inversely with temperature, it is not possible to define a constant ratio of the leakage current at low temperatures to that at high temperatures. In view of the fact that power transistors are normally operated at high junction temperatures, it is more meaningful to compare the leakage characteristics of both mesa and planar transistors at high temperatures. The relative reliability of different types of power transistors, which is in no way related to the magnitude of low-temperature leakage current, is also best compared at high temperatures.

Pulsed Safe-Area Systems

On the basis of the heat storage in the thermal mass of the silicon chip and its mounting system, the peak power-handling capability of transistors increases with decreases in pulse duration. Fig. 2-17 shows normalized thermal resistance N_R as a function of time for a specific transistor and indicates that power substantially higher than rated steady-state values may be applied for short periods of time without exceeding the maximum rated junction temperature. These values of increased power correspond to $(1/N_R)\ P_{(dc)}$, where $1/N_R$ is the normalized power multiplier and $P_{(dc)}$ is the steady-state power rating at the case temperature of interest.

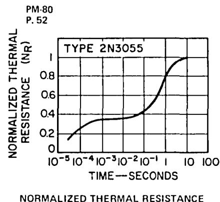

Fig. 2-17– Normalized thermal resistance.

The dissipation-limited region of the pulsed safe-area rating chart shown in Fig. 2-18 is prepared by use of the normalized thermal resistance from the following equation:

$$P_{diss} = [T_J(max) - T_C] / \theta_{J-C}(N_R)$$

This equation indicates a constant-power curve which can be represented on a log-log volt-ampere graph by a straight line that has a slope of -1 (from $I = PV^{-1}$).

The pulsed power curves are usually calculated and then verified by nondestructive tests along the constant-power curves from low to higher voltages. When dissipation is the only limiting factor, the -1 slope is continued to the transistor forward-biased avalanche breakdown voltage rating, at which point $V_{aM} = 1$ and may be approximated by $V_{CEO}(sus)$. When second breakdown ($I_{S/b}$) is the limiting factor, the slope changes from -1 to a higher value, usually between -1.5 and -4, according to the following relationship:

$$I_{S/b} = PV^{-N}$$

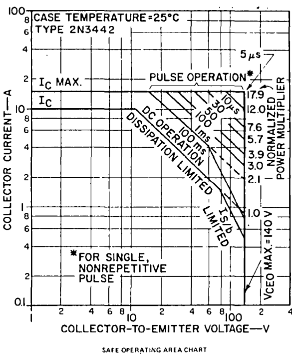

Fig. 2-18– Safe-operating-area chart.

Fig. 2-19 shows the derating curve for operation of a power transistor at case temperatures above 25°C. The $I_{S/b}$ limit is derated less with increasing temperature than the dissipation limit because the concentration of current that results in circuit breakdown is less severe than dissipation factors as temperature increases.

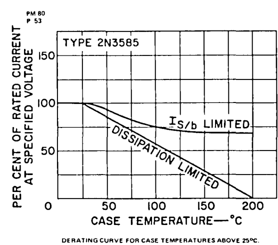

Fig. 2-19– Derating curve for case temperatures above 25°C.

For pulsed operation, the derating factor shown in Fig. 2-19 must be applied to the appropriate curve on the safe-area rating chart. For the derating, the effective case temperature T_C(eff) may be approximated by the average junction temperature T_j(av). The average junction temperature is determined as follows:

$$T_j(av) = T_C + P_{AV} (\theta_{J\text{-}C})$$

This approach results in a conservative rating for the pulsed capability of the transistor. A more accurate determination can be made by computation of actual instantaneous junction temperatures.

Depending upon whether time markers can be placed along the load line, two methods are available to determine whether a transistor will be operated within its safe-area limits in a given circuit.

1. Without Time Markers: The energy of the load line is concentrated at a single point (I_W, V_W) at which the greatest load-line penetration outside the safe area occurs. Multiplication of the waveforms of collector current I_C and the collector-to-emitter voltage V_{CE} yields a waveform of instantaneous power as a function of time. Integration of one cycle of this instantaneous-power waveform results in an energy E. The width (t_p) of an equivalent pulse may be determined as follows:

$$t_p = E/V_W I_W$$

The voltage V_W, the current I_W, and the pulse width t_p are compared to the corresponding values of the pulsed safe area on the derated curves.

2. With Time Markers: If time-marked load lines are available, either through the use of dual-trace waveforms of collector-to-emitter voltage and collector current as a function of time or Z-axis modulation of oscilloscope traces, an alternative approach may be used. The marked load line is sketched on the derated curves. If the transistor is being operated in the safe area, the trace time of the portion of the load line that extends outside a given pulsed safe area should not be greater than the specified pulsed width for that safe area. For example, the load line should not spend more than 1 millisecond outside the 1-millisecond safe area.

Thermal Fatigue

Significant temperature variations occur in power transistors because of changes in ambient temperature and in the power dissipation during operation. These variations in temperature result in cyclic mechanical stresses at the interface of the semiconductor pellet and the metal header to which the pellet is bonded because of the difference in the thermal expansions of these parts. These stresses are a function of the difference in the coefficients of thermal expansion of the semiconductor and metallic materials, of the change in temperature at the interface, and of the dimensions of the interface.

Power transistors are subjected to thermal-cycling stresses in all practical applications. Table 2-2 lists examples of the thermal cycling that a power transistor may be required to withstand in several typical applications. These data show that the thermal-cycling requirements may be very severe even in some of the more common types of applications. The cyclic stresses produced by the continuous thermal cycling may result in dislocation "pile-ups" at points of discontinuity such as may be produced by voids and impurities. Such dislocations cause localized hardening and cracks that may eventually lead to transistor failures. This type of failure

Table 2-2 — Thermal-Cycling Requirements, for Typical Applications of Power Transistors.

Application	Circuit	P_T (W)	ΔT_C (°C)	Minimum Equipment Life Required (years)	Typical Thermal-Cycling Rating Required (cycles)
Auto radio audio output	Class A	8	75	5	5,000
	Class AB	2	45	5	5,000
Power supply	Series regulator	50	65	5	5,000
	Switching regulator	15	65	5	5,000
Hi-Fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series regulator	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^8
Television	Vertical output	10	75	5	5,000
	Audio output	8	75	5	5,000
Sonar modulator	Linear amplifier	100	55	10	144×10^3

may be considered simply as fatigue wearout that results from continuous flexing of materials during thermal cycling.

Effect of Assembly Methods and Package Material on Thermal-Cycling Capability—The thermal-cycling stresses set up at the interface of two dissimilar materials because of the difference in the coefficients of thermal expansion of the materials can be reduced by insertion of a material that has an intermediate expansion coefficient between them. Fig. 2-20(a) illustrates the use of a molybdenum slab as an expansion matcher in a silicon power transistor to reduce the cyclic thermal stresses between the silicon pellet and the copper header. Use of this technique can result in significant improvement in the thermal-cycling capability of power transistors.

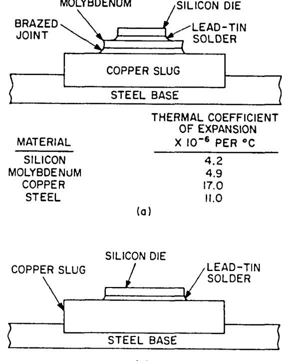

Fig. 2-20–Cross section of a transistor that uses a molybdenum expansion matcher between pellet and header; (b) cross section of a transistor in which pellet is soldered directly to copper.

Use of silicon-gold eutectic bonding to attach the semiconductor pellet to the header results in a pellet-to-header joint that can withstand a very large number of number of thermal cycles. When this type of hard-solder bonding is used, however, the stress generated because of a thermal mismatch is transmitted to the pellet, which in most power transistors is made of silicon. Because silicon is relatively weak in tensile strength and is highly "notched sensitive," the cyclic thermal stresses may result in the propagation of cracks in the silicon pellet unless either the pellet is very small or an expansion matcher is used.

In most silicon power transistors, lead solder is used to bond the pellet to the header. The cyclic thermal stresses produced at the mounting interface are then absorbed by non-elastic deformation of the soft solder material, and very little stress is transmitted to the pellet. The continuous flexing of the solder, however, may eventually lead to fatigue failure in this material. Any impurities in the solder results in dislocation pile-ups that accelerate the failure. RCA has developed a process that significantly reduces the impurities introduced into the lead solder. Use of this proprietary "controlled solder process" (CSP) makes it possible to avoid microcracks that propagate to cause fatigue failures in power transistors and, therefore, greatly increases the thermal-cycling capability of these devices.

Thermal-Cycling Rating Chart—An equipment manufacturer should make certain that power-transistor circuits are designed so that cyclic thermal stresses are mild enough to assure that no transistor fatigue failures occur during the required operating life of this equipment. Experimental results indicate that the thermal-cycling capability of a power transistor can be predicted by use of the following mechanical-activation energy equation:

$$N = Ae^{\gamma_\phi}/\Delta T$$

where N is the number of cycles to failure, A is a system constant, γ_ϕ is a constant proportional to the mechanical-activation energy required to produce a failure, and ΔT is proportional to the energy supplied as a result of the change in temperature at the mounting interface.

The above equation, together with empirical data, forms the basis for a new thermal-cycling rating system developed by RCA. This rating system, which is the first of this type in the industry, shows the relationship between total transistor power dissipation, the change in case temperature, and the number of thermal cycles that the transistor is rated to withstand.

Fig. 2-21 shows a typical thermal-cycling rating chart. This chart is provided in the form of a log-log presentation in which total transistor power dissipation is denoted by the ordinate and the thermal-cycling capability (number of cycles to failure) is indicated by the abscissa. Rating curves are shown for various magnitudes of change in case temperature. Use of this chart makes it possible for a circuit designer to avoid transistor thermal-fatigue failures during the operating life of this equipment. In general, power dissipation is a fixed system requirement. The designer also knows the number of thermal cycles that a power transistor will be subjected

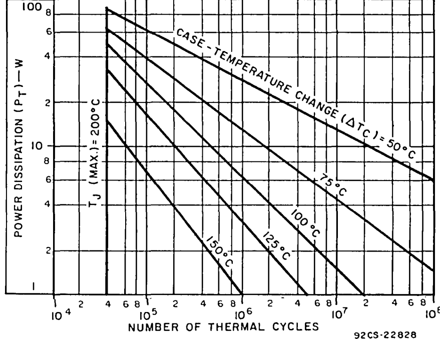

Fig. 2-21—Thermal-cycling rating chart for an RCA hermetic power transistor.

to during the minimum required life of the equipment. For these conditions, the chart indicates the maximum allowable change in case temperature. (If the rating point does not lie exactly on one of the rating curves, the allowable change in case temperature can be approximated by linear interpolation.) The designer can then determine the minimum size of heat sink required to restrict the change in case temperature within this maximum value.

Thermal-cycling ratings are included in the technical data for all RCA silicon power transistor announced since January 1, 1971. Similar ratings are being added for earlier power transistors as sufficient date are accumulated.

RCA experience in determining thermal-cycling rating has shown that package material is also a very important consideration in relation to thermal fatigue. Comparison data on the RCA steel packages and aluminum packages are given in the RCA Reliability Report, "Evaluation of Aluminum TO-3 Packages Under Thermal-Cycling Conditions" (AN-6071), shown later in the section *Application Notes on Power Transistors*.

These data show that the thermal-cycling capability of RCA's steel package with its glass-to-stem seal, welded cap, and controlled solder process is far superior (more than an order of magnitude better) to that of a similar type aluminum package and hard-solder mounting system.

Thermal-Fatigue Testing—The RCA thermal-cycling ratings allow a circuit designer to use power transistors with assurance that fatigue failures of these devices will not occur during the minimum required life of his equipment. These ratings provide valid indications of the thermal-cycling capability of power transistors for all types of operating conditions. On the basis of these ratings, limiting conditions can be established during circuit design so that the possibility of transistor thermal-fatigue failures are avoided.

Obviously, all individual power transistors cannot be tested to determine their thermal-cycling capability because such tests are expensive, time consuming, and destructive. The validity of the RCA thermal-cycling ratings results from the application of stringent process controls at each step in the manufacture of power transistors and from the testing of a statistically significant number of samples. Thermal-cycling ratings for power transistors provide the same type of assurance that a device will not fail when operated within ratings as that provided by the more familiar voltage, current, and second-breakdown ratings.

During thermal-fatigue testing of power transistors, the operating power for the device is usually equivalent to that expected to be applied during normal operation. The transistor is operated until the rise in case temperature is equal to the maximum value anticipated in the intended application. The case temperature is then reduced to the initial value by use of forced-air or water cooling. The cycle is repeated until failure occurs, as indicated by a significant increase in the transistor thermal resistance. The transistor heat sink and the timing of the temperature-cycling are selected to simulate as closely as possible the actual conditions that the transistor will be subjected to in the actual application. Table 2-3 shows the results of thermal-fatigue tests on several RCA transistors.

Effect of Radiation on RCA Power Transistors

There has been an increasing requirement for modern military systems to be "radiation hard", i.e., resistant to the effects of nuclear radiation. The electronic equipment in these systems must be carefully designed to achieve the required hardness. Solid-state devices have been the subject of particularly close attention.

Nuclear radiation has two major effects on power transistors. First, photocurrents generated by high-intensity irradiation can cause transistor saturation and possible circuit malfunction during the exposure. Second, prolonged exposure to bombardment by heavy particles such as neutrons can cause permanent changes in the transistor characteristics. These changes, which are caused by displacement damage to the semiconductor crystal, are primarily manifested as a decrease in transistor gain and an increase in saturation voltages. Table 2-4 summarizes the basic considerations relative to both displacement damage and photocurrents.

Power transistors must be optimally designed to minimize these radiation effects and maintain the required power-handling capability. The key design parameters are a thin low resistivity, low volume base, and a collector as thin and as low in resistivity as possible consistent with voltage breakdown requirements. Trans-

Table 2-3 — Thermal-Fatigue Performance of some Typical RCA Power Transistors

Type	Pellet Size Mils x Mils		Mounting Material	Material to which Die is Attached	CSP	Change in Case Temp. °C	Power Dissipation Watts	No. of Cycles to 10% Failure
2N3773*	250	250	Lead	Copper	No	42	85	1,000
2N3773	250	250	Lead	Molybdeum	No	42	85	9,600
2N3772	250	250	Lead	Copper	Yes	90	16	34,500**
2N3055	180	180	Lead	Copper	No	65	50	3,500
2N3055	180	180	Lead	Copper	Yes	90	6.7	40,000***
2N6032	230	230	Silicon Gold	Molybdeum	No	53	105	12,793***
2N5298	130	130	Lead	Copper	No	50	18	10,000
2N5240	130	130	Lead	Copper	Yes	42	51	8,500***
2N5039	145	183	Lead	Copper	Yes	73	59	10,000***

* Early design. ** Test still operating. *** Test terminated—less than 10% failure.

Table 2-4 — Effect of Nuclear Radiation on Power Transistors

Displacement Damage		Photocurrents	
Cause	Heavy particles, such as neutrons, bombarding the transistor and creating defects in the semiconductor material. Decreases lifetime in the base and increases collector resistivity.	**Cause**	High-intensity, high-energy radiation such as gamma, X-rays, electrons, neutrons, etc. generating electron-hole pairs.
Result	Semipermanent gain degradation and Increase in $V_{CE(sat)}$, leakage, and V_{CE}. These changes are referred to as semipermanent because annealing at several hundred degrees centigrade for a few hours recovers most of the degradation.	**Result**	Relatively large currents lasting as long as the transistor is exposed to radiation.
Radiation Parameter	Particles per square centimeter, called fluence, designated by the symbol Φ. The commonly used unit for this parameter is neutrons per square centimeter (n/cm^2).	**Radiation Parameter**	Radiation is usually defined in terms of rad(Si), where one rad(Si), identified by the symbol γ (gamma) is the amount of radiation required to deposit 100 ergs in one gram of silicon. $\dot{\gamma}$ (gamma dot) is defined as the dose rate in rad(Si) per second.
Relationship at Different Radiation Levels	Formula commonly used to extrapolate gain degradation results from one fluence level to another. $1/h_{FE2} = (1/h_{FE1}) + K^1\Phi$ where h_{FE2} = post-radiation gain h_{FE1} = pre-radiation gain K^1 = damage constant in cm^2/n Φ = fluence in n/cm^2	**General**	Collector-base photocurrents (I_{pp}) and emitter-base photocurrents (I_{cc}) are variously plotted as amperes versus $\dot{\gamma}$, or coulombs versus γ (coul/rad). At low dose rates, photocurrents are generally quite well-behaved and reasonably predictable from the formula $I=G\gamma$ where G is a function of the effective volume of the junction. (At relatively high dose rates, some transistors exhibit a departure from the assumed linear dose-rate dependence.)

istors that meet these design criteria are typified by high f_T, fast switching speeds, and moderate breakdown voltages.

RCA has developed power transistors which offer an optimized performance trade-off of radiation hardness, voltage, safe area, and power capability. For example, both photocurrent and voltage breakdown increase with increased collector resistivity because carrier lifetime is a function of resistivity. Collector resistivity, therefore, is fine-tuned to provide the maximum voltage breakdown possible with acceptable photocurrent performance. Post-radiation beta degradation is a function of base width, as is the frequency cutoff. Both of these characteristics are enhanced with decreasing base width. However, the safe-area capability is also a function of base width. Consequently, this parameter is fine-tuned to achieve optimum electrical performance and radiation hardness. Other techniques can be employed to enhance safe-area capability, such as the introduction of various amounts of ballasting.

Manufacturing Controls

RCA high-reliability power transistors are processed in accordance with the provisions of MIL-S-19500. These provisions include the following items:

1. A clearly defined procedure for the conversion of a customer specification into an RCA internal specification with built-in safeguards to assure the customer that the delivered parts meet or exceed his specification requirements.
2. A formalized personnel training and testing program which assures that each operation is performed correctly.
3. A complete inspection of incoming materials, utilities, and work in process using on-site facilities such as scanning-electron-microscope, and X-ray equipment.
4. Maintenance of cleanliness in work areas.
5. Rigorous control over changes in design, materials, and processes with documentation kept in active files for a minimum of three years.
6. Tool and test equipment maintenance and calibration in strict accordance with MIL-C-45662, "Calibration System Requirements."
7. A quality-assurance program in accordance with MIL-Q-9858, "Quality Program Requirements."

Detailed processing and screening requirements for RCA high-reliability power transistors are defined in the following paragraphs.

Processing and Screening

RCA offers a number of power transistors that have been qualified as JAN, JANTX, and/or JANTXV de-

vices in accordance with MIL-S-19500. These devices, which include hometaxial-base types, high-voltage types, and high-speed types, together with the detailed electrical (slash-sheet) specification number for them, are listed in Table 2-5.

Fig. 2-22 shows the processing requirements specified by MIL-S-19500 for JAN, JANTX, and JANTXV power transistors.

In addition to JAN, JANTX, and JANTXV types, many other RCA power transistors that are subjected to high-reliability preconditioning and screening in accordance with the Group A, B, and C Sampling Tests as specified in MIL-STD-750 or special customer requirements can be obtained on a custom basis. These power transistors can be supplied to four basic reliability levels. The preconditioning and screening for Level 1 is the same as that for JANTXV devices and, in addition, includes X-ray inspection. Level 2 corresponds directly to the JANTXV level. Level 3 devices are equivalent to JANTX devices. For RCA Level 4 devices, the preconditioning consists of burn-in only.

Fig. 2-23 shows the basic processing steps required for RCA high-reliability power transistors for each reliability level, and Table 2-6 lists the screening tests to which these devices are subjected. Tables 2-7, 2-8, and 2-9 list the Groups A, B, and C Sampling Tests and the

Table 2-5 — JAN and JANTX RCA Power Transistors

Basic Device Type Nos.	Detailed Electrical Specification
Hometaxial-Base Types	
2N1479, 2N1480, 2N1481, 2N1482	MIL-S-19500/207
2N1483, 2N1484, 2N1485, 2N1486	MIL-S-19500/180
2N1487, 2N1488, 2N1489, 2N1490	MIL-S-19500/208
2N2015, 2N2016	MIL-S-19500/248
2N3055	MIL-S-19500/407
2N3441	MIL-S-19500/369
2N3442	MIL-S-19500/370
2N3771, 2N3772	MIL-S-19500/413
High-Voltage Types	
2N3584, 2N3585	MIL-S-19500/384
2N6211, 2N6212, 2N6213	MIL-S-19500/461*
2N3439, 2N3440	MIL-S-19500/368
2N5415, 2N5416	MIL-S-19500/485
2N5838, 2N5839, 2N5840	MIL-S-19500/487
High-Speed Types	
2N5038, 2N5039	MIL-S-19500/439
2N5671, 2N5672	MIL-S-19500/488

*** In process of Qualification by RCA**

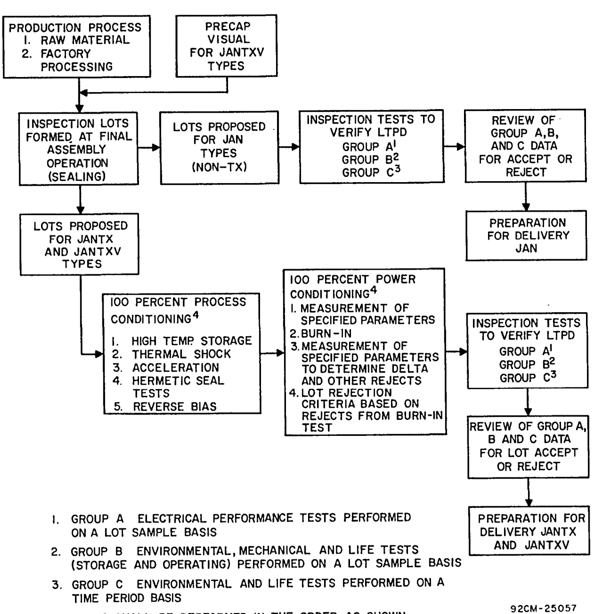

Fig. 2-22—Order of procedure diagram for JAN, JANTX, and JANTXV power transistors.

test methods specified by MIL-STD-750. The lot-sampling plans used for RCA high-reliability power transistors, as defined by MIL-S-19500 and MIL-STD-105D, are shown in Tables 2-10, 2-11, and 2-12.

The electrical ratings and characteristics and special features of JAN, JANTX, and JANTXV types and of other RCA power transistors for which high-reliability versions can be obtained are shown in the data charts at the end of this section.

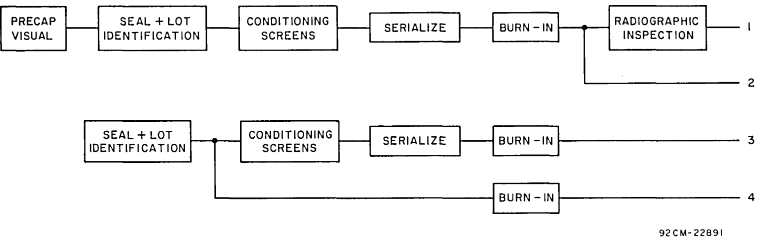

Fig. 2-23– Process-flow chart for four reliability levels of RCA high-reliability power transistors.

Table 2-6— Screening Tests for RCA High-Reliability Power Transistors

Test	Conditions	MIL-STD-750 Method	MIL-STD-750 Conditions	Screening Levels 1	2	3	4
1. Precap Visual		2072		X	X		
2. Seal and Lot Identification				X	X	X	X
3. High Temp Storage	24 hrs at 200°C			X	X	X	
4. Temperature Cycling	10 cycles	1051	C	X	X	X	
5. Acceleration	Y_1 direction	2006		X	X	X	
6. Fine Leak		1071	G or H	X	X	X	
7. Gross Leak		1071	A,C,D or F	X	X	X	
8. Reverse Bias	24 hrs at 150°C	1039	A	X	X	X	
9. Serialize				X	X	X	
10. Pre Burn-in Electrical				X	X	X	
11. Burn-in	168 hrs at 25°C	1039	B	X	X	X	X
12. Post Burn-in Electrical				X	X	X	
13. Final Electrical				X	X	X	X
14. Radiographic Inspection		2076		X			
15. External Visual		2071		X	X	X	

Specific test conditions and limits determined by each type of transistor.

Table 2-7 — Group A Inspections

Subgroup	Test	MIL-STD-750 Method
1	Visual & Mech Examination	2071
2	BV_{CEO}, BV_{CER}, or BV_{CEX}	3011
	I_{CEO}, I_{CER}, or I_{CEX}	3041
	I_{EBO}	3061
3	h_{FE}	3076
	$V_{CE(sat)}$	3071
	V_{BE}	3066
4	h_{FE}	3306
	C_{obo}	3236
	t_{on}	3251
	t_{off}	3251
5	150°C I_{CEX}	3041
	−65°C h_{FE}	3076

Table 2-8 — Group B Inspections

Subgroup	Test	MIL-STD-750 Method
1	Physical dimensions	2066
2	Solderability	2026
	Temperature Cycling	1051
	Moisture Resistance	1021
3	Shock	2016
	Vibration, Variable Frequency	2056
	Constant Accleration	2066
4	Safe Operating Area	3051
5	High Temperature Life	1031
6	Steady-State Operation Life	1026

Table 2-9 — Group C Inspections

Subgroup	Test	MIL-STD-750 Method
1	Barometric Pressure	1001
2	Salt Atmosphere	1041

TABLE 2-10 — LTPD sampling plans 1/ 2/ 3/

Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample).

Max. Percent Defective (LTPD) or λ	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3
Acceptance Number (c) (r = c + 1)	Minimum Sample Sizes (For device-hours required for life test, multiply by 1000)											
0	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)
1	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)
2	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)
3	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)
4	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)
5	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)
6	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)
7	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)
8	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)
9	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)
10	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)

1/ Sample sizes are based upon the Poisson exponential binomial limit.
2/ The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.
3/ This sampling plan is derived from Table C-1 in Appendix C of MIL-S-19500.

TABLE 2-11 — Sample Size Code Letters*

Lot or batch size			General inspection levels I	II	III
2	to	8	A	A	B
9	to	15	A	B	C
16	to	25	B	C	D
26	to	50	C	D	E
51	to	90	C	E	F
91	to	150	D	F	G
151	to	280	E	G	H
281	to	500	F	H	J
501	to	1200	G	J	K
1201	to	3200	H	K	L
3201	to	10000	J	L	M
10001	to	35000	K	M	N
35001	to	150000	L	N	P
150001	to	500000	M	P	Q
500001	and	over	N	Q	R

* Derived from Table I of MIL-STD-105D

TABLE 2-12 — Single Sampling Plans for Normal Inspection*

Sample size code letter	Sample size	Acceptable Quality Levels (normal inspection) 0.010 Ac Re	0.015 Ac Re	0.025 Ac Re	0.040 Ac Re	0.065 Ac Re	0.10 Ac Re	0.15 Ac Re	0.25 Ac Re	0.40 Ac Re	0.65 Ac Re	1.0 Ac Re	1.5 Ac Re	2.5 Ac Re	4.0 Ac Re	6.5 Ac Re	10 Ac Re	15 Ac Re	25 Ac Re
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2
B	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3
C	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4
D	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6
E	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8
F	20	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11
G	32	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15
H	50	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22
J	80	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑
K	125	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑
L	200	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑
M	315	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑
N	500	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑
P	800	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑
Q	1250	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑
R	2000	↑	↑	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑

↓ = Use first sampling plan below arrow. If sample size equals, or exceeds, lot or batch size, do 100 percent inspection.
↑ = Use first sampling plan above arrow.

Ac = Acceptance number.
Re = Rejection number.

* Derived from Table II-A of MIL-STD-105D

JAN2N1479 – JAN2N1482

Hometaxial-Base Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/207
Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military

Package: JEDEC TO-5
Maximum Ratings: P_T = 1 W; V_{CEO} = 40 V (2N1479, 2N1481)
= 55 V (2N1480, 2N1482)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 5 mA, V_{CE} = 28 V	600	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 200 mA, V_{CE} = 4 V	35	100	2N1489 2N1490
			20	60	2N1479 2N1480
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 200 mA	–	25	μs
Turn-off	t_{OFF}	I_C = 200 mA	–	25	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 135.

JAN2N1483 – JAN2N1486 JANTX2N1483 – JANTX2N1486

Hometaxial-Base Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/180
Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military

Package: JEDEC TO-8
Maximum Ratings: P_T = 1.75 W; V_{CEO} = 40 V (2N1483, 2N1485)
= 55 V (2N1484, 2N1486)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 5 mA, V_{CE} = 28 V	600	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 750 mA, V_{CE} = 4 V	35	100	2N1485 2N1486
			20	60	2N1483 2N1484
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 750 mA	–	25	μs
Turn-off	t_{OFF}	I_C = 750 mA	–	25	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 137.

JAN2N1487–JAN2N1490 Hometaxial-Base Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/208
Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military

Package: JEDEC TO-3
Maximum Ratings: P_T = 75 W; V_{CEO} = 40 V (2N1487, 2N1489)
= 55 V (2N1488, 2N1490)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 100 mA, V_{CE} = 12 V	500	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1.5 A, V_{CE} = 4 V	25	75	2N1489 2N1490
			15	45	2N1487 2N1488
Saturated Switching Time: Turn-on	t_{ON}	I_C = 1.5 A	–	25	μs
Turn-off	t_{OFF}	I_C = 1.5 A	–	25	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 139.

JAN2N2015 JAN2N2016 Hometaxial-Base Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/ 248
Structuer: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military

Package: JEDEC TO-36
Maximum Ratings: P_T = 150 W; V_{CEO} = 50 V (2N2015)
= 65 V (2N2016)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 5 A, V_{CE} = 4 V	800	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 5 A, V_{CE} = 4 V	15	50	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 5 A, I_B = 0.5 A	–	1.25	V

For characteristics curves and test conditions, refer to published data for basic type in File No. 12.

JAN2N3055
JANTX2N3055

Hometaxial-Base Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/407
Structure: Hometaxial-base
Applications: Power-switching, amplifiers

System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: P_T = 117 W; V_{CEO} = 70 V

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 4 V	800	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 4 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4 A, I_B = 0.4 A	–	0.75	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 70 V, t = 1 s	1.67	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 4 A	–	6	μs
Turn-off	t_{OFF}	I_C = 4 A	–	12	μs
Thermal-Cycling Rating		P_T = 20 W, ΔT_C= 50°C	3×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 524.

JAN2N3439, JAN2N3440
JANTX2N3439, JANTX2N3440

High-Voltage Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/368
Structure: Double-diffused epitaxial
Applications: High-voltage amplifiers, inverters, regulators
System Usage: Military

Package: JEDEC TO-39 (2N3439S) or JEDEC TO-5 (2N3439L)
Maximum Ratings: P_T = 0.8 W; V_{CEO} = 350 V (2N3439)
= 250 V (2N3440)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 20 mA, V_{CE} = 10 V	40	160	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 50 mA, I_B = 4 mA	–	0.5	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 200 V, t = 1 s	50	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 20 mA	–	1	μs
Turn-off	t_{OFF}	I_C = 20 mA	–	10	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 64.

JAN2N3441
JANTX2N3441

High-Voltage Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/369
Structure: Hometaxial-base
Applications: High-voltage power switching, amplifiers

System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: P_T = 25 W; V_{CEO} = 140 V

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 4 V	400	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 0.5 A, V_{CE} = 4 V	25	100	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 0.5 A, I_B = 0.05A	–	1	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 30 V, t = 1 s	833	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 0.5 A	–	8	μs
Turn-off	t_{OFF}	I_C = 0.5 A	–	15	μs
Thermal-Cycling Rating		P_T = 4 W, ΔT_C = 50°C	5×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 529.

JAN2N3442

High-Voltage Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/370
Structure: Hometaxial-base
Applications: High-voltage power switching, amplifiers

System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: P_T = 117 W; V_{CEO} = 140 V

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 3 A, V_{CE} = 4 V	100	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 3 A, V_{CE} = 4 V	20	70	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 3 A, I_B = 0.3 A	–	1	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	$V_{CE} \geqslant 8$ V, t = 1 s	1.5	–	A
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	3×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 528.

JAN2N3584, JAN2N3585 JANTX2N3584, JANTX2N3585 JANTXV2N3584, JANTXV2N3585

High-Voltage Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/384
Structure: Double-diffused epitaxial collector
Applications: High-voltage amplifiers, inverters, regulators
System Usage: Military

Package: JEDEC TO-66
Maximum Ratings: P_T = 35 W; V_{CEO} = 250 V (2N3584)
= 300 V (2N3585)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 10 V	25	100	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 1 A, I_B = 0.125 A	–	0.75	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 2 A, L = 100 μH R_{BE} = 20Ω	200	–	μJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 100 V, t = 1 s	350	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 1 A	–	3	μs
Turn-off	t_{OFF}	I_C = 1 A	–	7	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 138.

JAN2N3771, JAN2N3772 JANTX2N3771, JANTX2N3772

High-Current Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/413
Structure: Hometaxial-base
Applications: Power-switching, amplifiers, inverters
System Usage: Military

Package: JEDEC TO-3
Maximum Ratings: P_T = 150 W; V_{CEO} = 40 V (2N3771)
= 60 V (2N3772)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 4 V	600	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 A, V_{CE} = 4 V	15	60	2N3772
		I_C = 15 A; V_{CE} = 4V	15	60	2N3771
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 5 A, L = 40 mH, R_{BE} = 100Ω	500	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 60 V, t = 1 s	2.5	–	A
Saturated Switching Time:		2N3772 2N3771		2N3771 2N3772	
Turn-on	t_{ON}	I_C = 10A I_C = 15A	–	10 8	μs
Turn-off	t_{OFF}	I_C = 10 A I_C = 15 A	–	12 10	μs
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	4×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 525.

JAN2N5038, JAN2N5039 / JANTX2N5038, JANTX2N5039 High-Speed Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/439
Structure: Multiple-emitter sites, double-diffused epitaxial collector
Applications: Switching regulators, inverters, amplifiers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: P_T = 140 W; V_{CEO} = 90 V (2N5038)
= 75 V (2N5039)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 2 A, V_{CE} = 10 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 12 A, V_{CE} = 5 V	20	–	2N5038
		I_C = 10 A, V_{CE} = 5 V	20	–	2N5039
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 12 A, L = 180 μH, R_{BE} = 20Ω	13	–	mJ
Second Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 45 V, t = 1 s	0.9	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 12 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = 12 A	–	2	μs
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	4×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 367.

JAN2N5415, JAN2N5416 / JANTX2N5415, JANTX2N5416 High-Voltage Silicon P-N-P Power Transistors

JAN Electrical Specification: MIL-S-19500/485
Structure: Double-diffused epitaxial
Applications: High-voltage amplifiers, inverters, regulators
System Usage: Military
Package: JEDEC TO-5
Maximum Ratings: P_T = 0.75 W; V_{CEO} = -200 V (2N5415)
= -300 V (2N5416)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = –10 mA, V_{CE} = –10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –50 mA, V_{CE} = –10 V	30	120	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –50 mA, I_B = –5 mA	–	–2	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = –100V, t = 1 s	–100	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = –50 mA	–	1	μs
Turn-off	t_{OFF}	I_C = –50 mA	–	10	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 336.

JAN2N5671, JAN2N5672 JANTX2N5671, JANTX2N5672 High-Speed Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/488
Structure: Double-diffused epitaxial collector
Applications: Switching regulators, amplifiers
System Usage: Military

Package: JEDEC TO-3
Maximum Ratings: P_T = 140 W; V_{CEO} = 90 V (2N5671)
= 120 V (2N5672)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 2 A, V_{CE} = 10 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 15 A, V_{CE} = 2 V	20	100	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 15 A, I_B = 1.2 A	–	0.75	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 15 A, L = 180 μH R_{BE} = 20Ω	20	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 45 V, t = 1 s	0.9	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 15 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = 15 A	–	2	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 383.

JAN2N5838–JAN2N5840 JANTX2N5838–JANTX2N5840 High-Voltage Silicon N-P-N Power Transistors

JAN Electrical Specification: MIL-S-19500/487
Structure: Double-diffused, epitaxial-base
Applications: High-voltage switching regulators, inverters
System Usage: Military

Package: JEDEC TO-3
Maximum Ratings: P_T = 100 W; V_{CEO} = 250 V (2N5838)
= 275 V (2N5839)
= 350 V (2N5840)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Procuct	f_T	I_C = 0.2 A, V_{CE} = 10 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 2 A, V_{CE} = 3 V	10	50	2N5840 2N5839
		I_C = 3 A, V_{CE} = 2 V	8	40	2N5838
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 3 A, L = 100 μH R_{BE} = 50Ω	0.45	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 40 V, t = 1 s	2.5	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 2 A	–	1.75	μs
Turn-off	t_{OFF}	I_C = 2 A	–	4.5	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 410.

JAN2N6211 - JAN2N6213
JANTX2N6211 - JANTX2N6213

High-Voltage Silicon P-N-P Power Transistors

JAN Electrical Specification: MIL-S-19500/461
Structure: Double-diffused epitaxial collector
Applications: High-voltage amplifiers, inverters, regulators
System Usage: Military

Package: JEDEC TO-66
Maximum Ratings: P_T = 35 W; V_{CEO} = 225 V (2N6211)
= 300 V (2N6212)
= 350 V (2N6213)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -0.2 A, V_{CE} = -10 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -1 A, V_{CE} = -4 V	10	100	2N6213
		I_C = -1 A, V_{CE} = -3.2 V	10	100	2N6212
		I_C = -1 A, V_{CE} = -2.8 V	10	100	2N6211
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = -40 V, t = 1 s	-0.875	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = -1 A	–	0.6	μs
Turn-off	t_{OFF}	I_C = -1 A	–	3.1	μs
Thermal-Cycling Rating		P_T = 2 W, ΔT_C = 50°C	7×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 507.

2N2102

High-Speed, Medium-Power Silicon N-P-N Power Transistor

Structure: Planar, Double-diffused epitaxial collector
Applications: Small-signal and medium-power general usage
System Usage: NASA SATURN
Package: JEDEC TO-39 (2N2102S) or JEDEC TO-5 (2N2102L)
Maximum Ratings: V_{CEO} = 65 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 10 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 150 mA, V_{CE} = 10 V	40	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	1.5	V

For characteristics curves and test conditions, refer to published data for basic type in File No. 106.

2N3054

Hometaxial-Base Silicon N-P-N Power Transistor

Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = 55 V, P_T = 25 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 4 V	800	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 0.5 A, V_{CE} = 4 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 0.5 A, I_B = 0.05 A	–	1	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 55 V, t = 1 s	0.455	–	A
Thermal-Cycling Rating		P_T = 4 W, ΔT_C = 50°C	5×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 527.

2N3263 High-Power, High-Speed, High-Current Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: High-speed switching, amplifiers, inverters
System Usage: Minuteman, SRAM
Package: Radial, hermetic
Maximum Ratings: V_{CEO} = 90 V, P_T = 84 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 3 A, V_{CE} = 10 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 15 A, V_{CE} = 3 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 15 A, I_B = 1.2 A	–	0.75	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 10 A, L = 40 μH R_{BE} = 20Ω	2	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 75 V, t = 250 μs	350	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 15 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = 15 A	–	2	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 54.

2N3265 High-Power, High-Speed, High-Current Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: High-speed switching, amplifiers, inverters
System Usage: Minuteman, SRAM
Package: JEDEC TO-63
Maximum Ratings: V_{CEO} = 90 V, P_T = 125 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 3 A, V_{CE} = 10 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 15 A, V_{CE} = 3 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 15 A, I_B = 1.2 A	–	0.75	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 10 A, L = 40 μH R_{BE} = 20Ω	2	–	mJ
Second Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 75 V, t =250 μs	350	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 15 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = 15 A	–	2	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 54.

2N3773

High-Voltage Silicon N-P-N Power Transistor

Structure: Hometaxial-base
Applications: High-voltage inverters, amplifiers, hammer drivers
System Usage: VIKING
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 140 V, P_T = 150 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 4 V	200	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 8 A, V_{CE} = 4 V	15	–	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 8 A, I_B = 0.8 A	–	1.4	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 2.5 A, L = 40 mH R_{BE} = 100Ω	0.125	–	J
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 100 V, t = 1 s	1.5	–	A
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	4×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 526.

2N3879

High-Current, High-Speed Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: High-current, high-speed switching
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = 75 V, P_T = 35 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 10 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 5 V	20	–	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 4 A, I_B = 0.4 A	–	1.2	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 4 A, L = 125 μH R_{BE} = 50Ω	1	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 40 V, t = 1 s	500	–	mA
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 4 A	–	440	ns
Turn-off	t_{OFF}	I_C = 4 A	–	1200	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 299.

2N4036

Medium-Power Silicon P-N-P Power Transistor

Structure: Planar, double-diffused epitaxial collector
Applications: Small-signal, medium-power amplifiers
System Usage: Military
Package: JEDEC TO-39 (2N4036S) or JEDEC TO-5 (2N4036L)
Maximum Ratings: V_{CEO} = -65 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -50 mA, V_{CE} = -10 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -150 mA, V_{CE} = -10 V	40	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = -150 mA, I_B = -15 mA	–	-0.65	V
Saturated Switching Time: Turn-on	t_{ON}	I_C = -150 mA	–	110	ns
Turn-off	t_{OFF}	I_C = -150 mA	–	700	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 216.

2N5240

High-Voltage, High-Power Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: Series regulators, power amplifiers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 300 V, P_T = 100 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 2 A, V_{CE} = 10 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 2 A, I_B = 0.25 A	–	2.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 4 A, L = 0.2 mH, R_{BE} = 50Ω	1.6	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 150 V, t = 1 s	0.67	–	A

For characteristics curves and test conditions, refer to published data for basic type in File No. 321.

2N5262

High-Speed Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial
Applications: Core drivers, high-speed amplifiers
System Usage: AEGIS
Package: Low-profile TO-39
Maximum Ratings: V_{CEO} = 50 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 10 V	250	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 1 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1 A, I_B = 0.1 A	–	0.8	V
Saturated Switching Time: Turn-on	t_{ON}	I_C = 1 A	–	30	ns
Turn-off	t_{OFF}	I_C = 1 A	–	60	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 313.

2N5320

High-Speed Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: Small-signal and medium-power amplifiers
System Usage: Military
Package: JEDEC TO-39 (2N5320S) or JEDEC TO-5 (2N5320L)
Maximum Ratings: V_{CEO} = 75 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 500 mA, V_{CE} = 4 V	30	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 500 mA, I_B = 50 mA	–	0.5	V
Saturated Switching Time: Turn-on	t_{ON}	I_C = 500 mA	–	80	ns
Turn-off	t_{OFF}	I_C = 500 mA	–	800	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 325.

2N5322

High-Speed Silicon P-N-P Power Transistor

Structure: Double-diffused epitaxial collector
Applications: Small-signal, medium-power amplifiers
System Usage: Military
Package: JEDEC TO-39 (2N5322S) or JEDEC TO-5 (2N5322L)
Maximum Ratings: V_{CEO} = -75 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -50 mA, V_{CE} = -4 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -500 mA, V_{CE} = -4 V	30	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = -500 mA, I_B = -50 mA	–	-0.7	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = -500 mA	–	100	ns
Turn-off	t_{OFF}	I_C = -500 mA	–	1000	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 325.

2N5578

High-Current, High-Power Silicon N-P-N Power Transistor

Structure: Multiple-emitter sites, hometaxial-base
Applications: High-current, high-power amplifiers and switching
System Usage: TOW, Sonobuoy
Package: JEDEC TO-3 with 0.060-inch-diameter pins
Maximum Ratings: V_{CEO} = 70 V, P_T = 300 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 10 A, V_{CE} = 4 V	400	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 40 A, V_{CE} = 4 V	10	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 40 A, I_B = 4 A	–	1.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 7A, L = 33 mH, R_{BE} = 10Ω	0.8	–	J
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 25 V, t = 1 s	12	–	A

For characteristics curves and test conditions, refer to published data for basic type in File No. 359.

2N5781

High-Speed Silicon P-N-P Power Transistor

Structure: Epitaxial-base
Applications: Medium-power switching and amplifiers
System Usage: Military
Package: JEDEC TO-5
Maximum Ratings: V_{CEO} = -65 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -0.1 A, V_{CE} = -2 V	8	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -1 A, V_{CE} = -2 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = - 1 A, I_B = -0.1 A	–	-0.5	V
Saturated Switching Time: Turn-on	t_{ON}	I_C = -1 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = -1 A	–	2.5	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 413.

2N5784

Hometaxial-Base Silicon N-P-N Power Transistor

Structure: Hometaxial-base
Applications: Medium-power switching, amplifiers
System Usage: Military
Package: JEDEC TO-5
Maximum Ratings: V_{CEO} = 65 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.1 A, V_{CE} = 2 V	1	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 2 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1 A, I_B = 0.1 A	–	0.5	V
Saturated Switching Time: Turn-on	t_{ON}	I_C = 1A	–	5	μs
Turn-off	t_{OFF}	I_C = 1A	–	15	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 413.

2N5954

High-Speed, Medium-Power Silicon P-N-P Power Transistor

Structure: Epitaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = -80 V, P_T = 40 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -1 A, V_{CE} = -4 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -2 A, V_{CE} = -4 V	20		
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = -2 A, I_B = -0.2 A	–	-1	V

For characteristics curves and test conditions refer to published data for basic type in File No. 675.

2N6033

High-Current, High-Speed, High-Power Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: High-current, fast switching
System Usage: SAFEGUARD
Package: JEDEC TO-3 with 0.060-inch-diameter pins
Maximum Ratings: V_{CEO} = 120 V, P_T = 140 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 2 A, V_{CE} = 10 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 40 A, V_{CE} = 2 V	10	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 40 A, I_B = 4 A	–	1	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 20 A, L = 310 μH, R_{BE} = 5Ω	62	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 40 V, t = 1 s	0.9	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 40 A	–	1	μs
Turn-off	t_{OFF}	I_C = 40 A	–	2	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 462.

2N6056

Darlington
Silicon N-P-N Power Transistor

Structure: Monolithic, epitaxial-base
Applications: Power-switching, amplifiers, hammer drivers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 80 V, P_T = 100 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 3 A, V_{CE} = 3 V	4	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 3 V	750	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4 A, I_B = 16 mA	–	2	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 5 A, L = 12 mH, R_{BE} = 100Ω	150	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 40 V, t = 1 s	2	–	A
Thermal-Cycling Rating		P_T = 10 W, ΔT_C = 50°C	8×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 563.

2N6079

High-Voltage, High-Power
Silicon N-P-N Power Transistor

Structure: Multiple-emitter sites, double-diffused epitaxial
Applications: High-voltage inverters
System Usage: SAFEGUARD
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = 350 V, P_T = 45 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	1	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1.2 A, V_{CE} = 1 V	12	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1.2 A, I_B = 0.2 A	–	0.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 3 A, L = 100 μH, R_{BE} = 50Ω	0.45	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 50 V, t = 1 s	0.9	–	A

For characteristics curves and test conditions, refer to published data for basic type in File No. 492.

2N6248

High-Speed, High-Power Silicon P-N-P Power Transistor

Structure: Epitaxial-base
Applications: Power-switching
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = -100 V, P_T = 125 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -1 A, V_{CE} = -4 V	10	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -5 A, V_{CE} = -4 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = -5 A, I_B = -0.5 A	–	-1.3	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = -42 V, t = 1 s	-1.25	–	A
Thermal-Cycling Rating		P_T = 10 W, ΔT_C = 50°	1.5×10^6	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 541.

2N6251

High-Voltage Silicon N-P-N Power Transistor

Structure: Multiple-epitaxial
Applications: High-voltage inverters
System Usage: MARK-48, P-3-C
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 350 V, P_T = 175 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 10 V	2.5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 A, V_{CE} = 3 V	6	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 10 A, I_B = 1.67 A	–	1.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 10 A, L = 50 μH R_{BE} = 100Ω	2.5	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 30 V, t = 1 s	5.8	–	A
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	2×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 523.

2N6385

Darlington Silicon N-P-N Power Transistor

Structure: Monolithic, epitaxial-base
Applications: Power-switching, amplifiers, hammer drivers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 80 V, P_T = 100 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 5 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 5 A, V_{CE} = 3 V	1000	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 5 A, I_B = 0.01 A	–	2	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 4.5 A, L = 12 mH R_{BE} = 100Ω	120	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 75 V, t = 1 s	0.22	–	A
Thermal-Cycling Rating		P_T = 10 W, ΔT_C = 50°C	8×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 609.

2N6479 2N6481 2N6480 2N6482

Radiation-Hardened Silicon N-P-N Power Transistor

Epitaxial-Planar Types for Aerospace and Military Applications

Rated for Operation in Radiation Environments with Neutron Fluence Levels to 1 x 10^{14} Neutrons/cm^2 and Gamma Exposure up to 1×10^8 Rad (Si)/s

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*
PRE-RADIATION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc V_{CB}	V_{CE}	V_{EB}	CURRENT A dc I_E	I_B	I_C	LIMITS 2N6479 2N6481 MIN.	MAX.	2N6480 2N6482 MIN.	MAX.	UNITS
Collector Cutoff Current: With emitter open	I_{CBO}	100						–	1	–	1	mA
* With base-emitter junction reverse-biased	I_{CEV}		100	0				–	1	–	1	mA
* At T_C = 100°C			60	0				–	1	–	1	
* Emitter Cutoff Current	I_{EBO}			6				–	2	–	2	mA
Emitter-to-Base Voltage	V_{EBO}				0.002			6	–	6	–	V
Collector-to-Emitter Sustaining Voltage: * With base open	$V_{CEO}(sus)$						0.2[a]	60	–	80	–	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$						0.2[b]	80	–	100	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					1.2	12[a]	–	0.75	–	0.75	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					1.2	12[a]	–	1.5	–	1.5	V
* DC Forward Current Transfer Ratio	h_{FE}		2				12[a]	20	300	20	300	
Second Breakdown Collector Current: With base forward-biased, t = 1 s	$I_{S/b}$		12					7.3	–	7.3	–	A
* Saturated Switching Time												
Rise	t_r		V_{CC} = 30			1.2[c]	12	–	400	–	400	ns
Storage	t_s					1.2[c]	12	–	800	–	800	
Fall	t_f					1.2[c]	12	–	200	–	200	
* Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (f = 10 MHz)	$\|h_{fe}\|$		5				1	10	–	10	–	
								2N6479 2N6480		2N6481 2N6482		
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$		10				5	–	2	–	1.5	°C/W

* In accordance with JEDEC registration data format JS-6 RDF-1.

[a] Pulsed; pulse duration ≤ 350 μs, duty factor ≤ 2%.

[c] $I_{B_1} = I_{B_2}$

POST-NEUTRON-RADIATION ELECTRICAL CHARACTERISTICS
AFTER EXPOSURE TO 5 x 10^{13} NEUTRONS/cm^2 (1 MeV equiv.), *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		VOLTAGE V dc			CURRENT A dc		For all Types		
		V_{CE}	V_{BE}	V_{EB}	I_C	I_B	MIN.	MAX.	
* Collector Cutoff Current: With base-emitter junction reverse-biased	I_{CEV}	100	0				–	1.2	mA
* Emitter Cutoff Current	I_{EBO}			5			–	2.2	mA
* Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$				0.2 0.2	0.05 0.05	80[b] 60[c]	– –	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				7[a]	1.4	–	1.5	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				7[a]	1.4	–	1.5	V
* DC Forward Current Transfer Ratio	h_{FE}	5			7[a]		12	–	
Magnitude of Common Emitter, Small-Signal Short Circuit Forward Current Transfer Ratio (f = 10 MHz)	$\|h_{fe}\|$	5			1		10	–	
* Damage Constant	K▲						–	9×10^{-16}	

* In accordance with JEDEC registration data format JS-6 RDF-1.

a Pulsed; pulse duration ≤ 350 μs, duty factor ≤ 2%.

b For types 2N6480, 2N6482.

c For types 2N6479, 2N6481.

$$\blacktriangle\text{Damage constant } K = \frac{\frac{1}{h_{FE_2}} - \frac{1}{h_{FE_1}}}{\phi}$$

Where h_{FE_1} = Beta prior to exposure
h_{FE_2} = Beta after exposure
ϕ = Neutron fluence (1 MeV equiv.)

Knowing K, h_{FE_2} may be calculated for other fluences using the relationship:

$$h_{FE_2} = \frac{1}{K\phi + \frac{1}{h_{FE_1}}}$$

TYPICAL CHARACTERISTIC DURING GAMMA EXPOSURE FOR DOSE RATES OF LESS THAN 1 x 10^8 RAD(Si)/sec

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS	UNITS
		VOLTAGE – V dc		For all Types	
		V_{CB}	V_{BE}	TYPICAL	
Collector-to-Base Charge Generation Constant	(C)	20	0	5×10^{-8}	Coulomb / Rad

The charge generated in the depletion region of a transistor is proportional to the volume of the depletion region, the total dose, and the energy of the gamma radiation.

The primary base-collector photo current $[I_{pp(base)}] = (C)\dot{\gamma}$, where $\dot{\gamma}$ is the gamma dose rate in Rad(Si)/s.

Solid State Division

Power Transistors Application Notes

AN-6071

Evaluation of Hermeticity of Aluminum TO-3 Packages Under Thermal-Cycling Conditions (Reliability Report)

A program that continually upgrades product and develops meaningful rating systems is a requirement in the power-semiconductor business. RCA's program has played a major role in the development of products and has led to the specification of IS/b, ES/b, and thermal-cycling ratings. RCA's experience in determining the thermal-cycling ratings of power transistors has shown that package material and assembly systems must be looked at very carefully from a thermal-fatigue viewpoint. This report evaluates the thermal capabilities of our competitors' aluminum TO-3 package with soldered-in leads against the RCA steel TO-3 package with glass-sealed leads.

Failure Data

In conjunction with its ongoing thermal-cycling rating program, RCA continually evaluates product from its major competitors. The results of this evaluation are quite significant in the case of the aluminum TO-3 package. Type 2N3055 product in the aluminum TO-3 package from three major competitors has been evaluated and the results compared to those achieved with RCA's steel TO-3 package. None of the competitors' product tested passed RCA's thermal-cycling criteria, and, in addition, all of the product demonstrated early failures in thermal-fatigue tests for hermeticity. It is RCA's opinion that the aluminum package as it is now manufactured is unacceptable, and that, in addition, it has some fundamental engineering problems that indicate that it may never be a viable hermetic-package system. Tables I and II show typical examples of the data gathered during tests of Type 2N3055 devices in aluminum TO-3 packages. Tables III and IV show additional data on a second, recently announced transistor type housed in the aluminum TO-3 package. Note that most failures occurred before 5000 cycles.

Failure Analysis

Helium Leak Test — Before and after each test, all units were checked by submitting them to a four-hour helium bomb and then to a helium-leak detector.

Freon Bubble — The freon-bubble test is a gross-leak test in which the units are freon-bombed overnight (in FC-78 helium) and then submerged in hot freon (FC-43) and checked for bubble exodus. Analysis of the leakers showed that the devices lost hermeticity at the glass eyelet assemblies (emitter and base leads) that are soldered into the aluminum header after the number of thermal cycles indicated. Note that no RCA devices failed the thermal-cycling test. RCA steel TO-3 devices were included in these tests only as controls; the life of the RCA steel-packaged 2N3055 on the 16-W thermal-cycling test is typically well beyond 100,000 cycles before first failures.

Table I — Results of 16-W Thermal-Cycling Test of 2N3055 — 10,000 Cycles
(T_C = 40 to 130°C, No. of Units = 10

TEST	NO. OF FAILURES ALUM. TO-3			STEEL TO-3 RCA
	Mfr. A	Mfr. B	Mfr. C	
Helium Leak — Fine	8	4	3	0
Freon Bubble — Gross	2	5	0	0
Total	10	9	3	0
Cumulative Electrical Failures for 10,000 Cycles	7 Short	5 Short 1 θ_{jc}*	1 Open 4 Short	0

* θ_{jc} increased more than 25 percent

Table II — Results of Temperature-Cycling Test of 2N3055 — 75 Cycles
(T_C = −65 to +150°C, No. of units = 15)

TEST	NO. OF FAILURES ALUM. TO-3			STEEL TO-3 RCA
	Mfr. A	Mfr. B	Mrf. C	
Helium Leak — Fine	9	14	5	0
Freon Bubble — Gross	0	1	1	0
Total	9	15	6	0

Table III – Results of 16-W Thermal-Cycling Test on Second Device – 3000 Cycles

(T_C = 40 to 130°C, No. of units = 12)

TEST	NO. OF FAILURES ALUM. TO-3 MANUFACTURER A
Helium Leak – Fine	0
Freon Bubble – Gross	9
Total	9

Table IV – Results of Temperature Cycling Test on Second Device – 25 Cycles

(T_C = –65 to +150°C, No. of units = 12)

TEST	NO. OF FAILURES ALUM. TO-3 MANUFACTURER A
Helium Leak – Fine	0
Freon Bubble – Gross	3
Total	3

Engineering Problem

Fig. 1 shows an exploded view of the aluminum TO-3 package; all three competitors use lead eyelet assemblies that are soldered into the aluminum flange. The cyclic heating and cooling of the aluminum package cause expansion and contraction of the flange with respect to the eyelet assembly and propagate microcracks that ultimately cause leaks. Contamination of the solder holding the eyelet assembly probably initiates the problem.

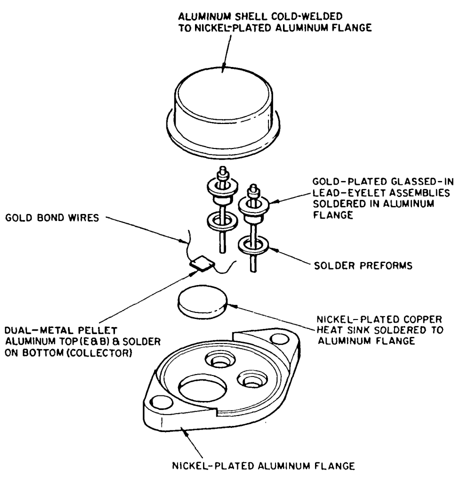

Fig. 1– Aluminum TO-3 package.

Fig. 2 shows the RCA steel TO-3 package. Note the glass-to-stem seal with no solder interface. This configuration is possible with the steel package because the melting point of steel is far higher than the melting point of glass. It is not possible to use the same system with the aluminum header because the melting point of aluminum is below that of the glass used in the seal. Consequently, manufacturers who use aluminum packages are forced to use a soldered-in assembly.

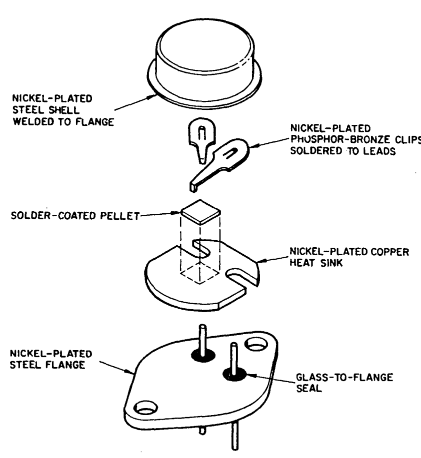

Fig.2– RCA steel TO-3 package.

Conclusion

RCA's competitors have proclaimed the attributes of aluminum packages and hard-solder power (the power available from a package in which the pellet has been mounted by the use of a hard-solder method). We believe that the soldered-in eyelet associated with the aluminum package has serious reliability and fundamental engineering problems. This is also true of their so-called "hard-solder" packages, which use the same type of soldered-in eyelet assemblies. RCA's steel package with its glass-to-stem seal, welded cap, and controlled solder process, is far superior to the aluminum package and hard-solder mounting system-over an order of magnitude better. The aluminum package has a long way to go to compete. The customer who buys a device in a TO-3 package may think he is buying long-term hermeticity; he may have a serious problem if it's aluminum.

Solid State
Division

Power Transistors

Application Note
AN-6249

Real-Time Controls of Silicon Power-Transistor Reliability

L. J. Gallace and V. J. Lukach

This Note compares the traditional, classical approach to the reliability-assurance testing of power transistors with a newer classification of testing: Real-Time Control, RTC. The classical approach is commonly referred to as Group B, and involves a series of mechanical, environmental, and life stress tests. RTC is a continuous, systematic evaluation and control in "real time" of basic, potential failure mechanisms. It is an important supplement to a **total** program intended to assure the reliable performance of power transistors.

Classical Method of Determining Reliability

When examining semiconductor reliability, the term "reliability" itself must first be defined and understood. Because "reliability" means different things to different people, it becomes necessary to define the degree or level of reliability required in the classical and universal language of statistics. The procedure of accumulating life-test data under conditions which may be application-oriented to obtain MTF (mean-time-to-failure) data is an oversimplified way of demonstrating reliability when one desires millions of device hours with a small number of failures. Unless one is interested in demonstrating only modest levels of reliability, this procedure will be totally inadequate for determining how well the manufacturing process produces devices that meet the intended design criteria.

Table I indicates the enormous sample sizes required to demonstrate very low failure rates by the classical method. The equally enormous expenditures in facilities and time required to test samples of the sizes shown is obvious.

Table I – Sample Size Required for 1000-Hour Life Test

Failure Rate %/ 1000 Hrs.	With Zero Failures at 90% Confidence	With One Failure at 90% Confidence	With Three Failures at 90% Confidence
1.0	231	390	668
0.1	2,303	3,891	6,681
0.01	23,026	38,980	66,808
0.001	230,000	389,000	668,000

Fig. 1(a) shows the "bathtub curve" used in the classical method to characterize the random failure region; this curve is an oversimplification of the three curves shown in Fig. 1(b) representing various failure modes. Clearly, the bathtub-curve method of determing a region which by its very definition is random and largely unpredictable is unsatisfactory.

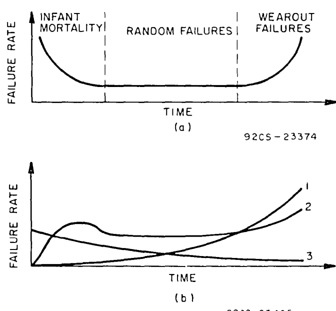

Fig. 1 – (a) Generalized "bathtub" failure-rate curve, (b) family of curves from which the "bathtub" curve in (a) is derived.

Comparison of Group B and RTC

The classical approach was developed years ago because some over-all protection in the form of reliability assurance was needed by customers. These Group B tests, performed under standardized MIL-STD-750 conditions, were necessary and useful. However, times have changed. Reliability engineers have overstress-tested devices to destruction; in addition, a wealth of customer field information is available. Failure analysis performed on a routine basis has added even more knowledge. The net result is a greater understanding and appreciation of categories of potential failure mechanisms associated with different product designs than was previously possible; RTC is a reliability-assurance testing system that takes advantage of all this information.

Reliability-assurance data published per specific customers' requests has traditionally consisted of Group-B test results. In general, the summation of data shows large sample sizes with near zero total failures. RTC, with its accelerated test conditions, may not show zero failures. Therefore, when RTC data is published externally, customers must be educated in its interpretation. This education usually consists of personal contact and a qualitative explanation of each report.

The foundation of RTC is accelerated testing, tests performed at higher than normal stress levels to increase the failure rate and shorten the time to wearout. There is almost no mechanical, environmental, life, or combined stress test for which accelerated test conditions cannot be achieved. Table II lists the various tests with recommended directions for acceleration. The reliability tests of the future will use accelerated testing techniques that are associated with real-time-control theory to provide meaningful, quick appraisals and predictions of the reliability of solid-state components.

Table III describes some of the most important differences that exist between the classical form of testing and RTC. The power and advantages of RTC are clearly visible.

Table II – Tests and Acceleration Directions

Test	Direction of Stress Acceleration
Mechanical	
Lead fatigue	Increase bends to package destruction
Lead pull	Increase weight to package destruction
Lead torque	Increase torque to package destruction
Centrifuge	Increase G-force
Impact shock	Increase G-force
Vibration	Equipment limited
Solderability	Increase preconditioning stress, e.g., 3 hrs. in steam
Environmental	
Moisture resistance/ relative humidity	Increase time; use pressure cooker/ autoclave; use moisture with bias
Salt atmosphere	Increase time
Temperature cycling	Increase cycles; increase ΔT ambient
Thermal shock	Increase cycles; increase ΔT liquid
Life	
Operating life	Increase T junction
Storage life	Increase T ambient
Thermal fatigue	Increase ΔT_{case}; increase cycles
Reverse bias	Increase T ambient; increase voltage

Real-Time Controls

Real-time controls are accelerated tests used to control reliability – a design and process parameter. In the real-time method of determining reliability, a continuous flow of data is interpolated into established criteria to provide an indication of how well the manufacturing process is producing product that meets the criteria. By comparing actual to historical data, changes required in the manufacturing process to improve the reliability of the product can be made on a day-to-day basis.

The tests used as real-time controls are selected on the basis of extensive reliability-engineering work done during the design

Table III – Differences Between Classical Group-B Tests and Real-Time Controls

APPROACH	GROUP-B TESTS	REAL-TIME CONTROLS
1. Test Considerations	At maximum device ratings or less	Overstress many times to destruction
2. Overall	General, multi-subgroups, "shotgun" approach	Specific, predetermined reliability engineering experimentation necessary, "rifle" approach.
3. Types of Failure	Non-predictable multi-failure modes; read 6 to 15 electrical parameters	Visually one failure mode; i.e., look for evidence of one specific failure mechanism. Many times electrical readings not required.
4. Frequency	Usually once per month	Weekly – Daily – Hourly
5. Product Stage	Completed, electrically tested product	All stages of product
6. Sample Size	Large (approximately 150 per each subgroups)	Small (approximately 40), taken more frequently
EFFECTIVENESS		
1. Decisions	Very poor, after the fact	Immediate and Direct
2. Reliability Predictability	Poor, considering current low level failure rates	Excellent, considering protection from accelerated conditions
3. Problem Detection, Feedback, Corrective Action	Poor	Excellent, quick response on today's product with measurable quick evaluation of corrective action
4. Efficiency of One Test Rack	8 tests/rack/year (1000 hr. test and down period)	90 tests/rack/year (3 day max. and 1 day for changing product)
5. Test Duration	Approximately 6 weeks	Minutes to three days maximum

of a new product. Reliability, design, and applications engineers work together to develop an integrated matrix of mechanical, electrical, thermal, and environmental stress tests that will provide information concerning allowable margins of materials, process, and structure in the manufacturing process. Failure mechanisms detected during the manufacturing process can then be continually controlled even though they occur under accelerated conditions, and the product reliability margin, as shown in Fig. 2, can be maintained. Very often a two- or three-day accelerated life test can be used to predict the performance of a product in an actual application over a five-to

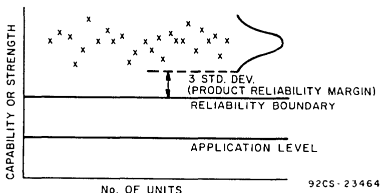

Fig. 2 – Curve demonstrating product-reliability margin.

seven-year period. For this reason, a major effort is made to correlate accelerated-test data to use conditions.

Information generated by the RTC method has unquestionable validity because tests are well controlled, and all ambiguties have been removed. Not only is the stress application and duration known for acceptable product, but, in most cases, RTC may be used to evaluate and control individual failure mechanisms. Current as well as historical and projected operating information is generated for analysis.

Real-Time Control Programs

Thermal Cycling

The first real-time control was developed by RCA to control the thermal-cycling capability of silicon power transistors in plastic packages.[1,2,3] The thermal-cycling capability is determined from a system of rating curves which defines cycle life in terms of power and changes in case temperature. RTC tests are designed to produce information in three days for use in process-control. Table IV shows the sampling plan and test conditions for real-time control of thermal-cycling capability of VERSAWATT transistors. Fig. 3 shows the

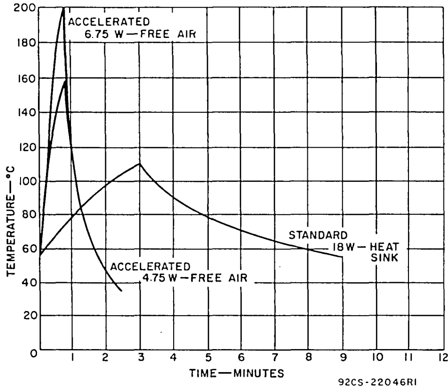

Fig. 3 – Difference in thermal-cycling tests for the standard-quality, Group-B method and the accelerated RTC method.

differences in the thermal-cycling tests for the standard-quality, group-B method and the accelerated RTC method. The thermal-cycling test circuit, Fig. 4, includes an indicator

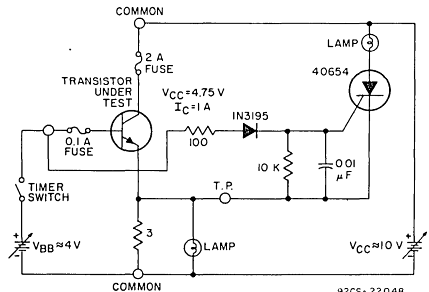

Fig. 4 – The thermal cycle test circuit used to obtain the data in Table IV.

Table IV – Sampling Plan and Test for Real-Time-Control of VERSAWATT TO-220 Thermal-Cycling Capability

OBJECTIVES

1. Provide a Meaningful Control for Critical Thermal-Cycling Capability.
2. Detect Lot-to-Lot Differences.
3. Initiate Corrective Actions and/or Holding Actions.

TEST CONDITIONS AND ACCEPTANCE CRITERIA

Accelerated Thermal Cycling – Free Air, 4.75 W, $\Delta T_C = 125^oC$, $t_{ON} = 50$ Sec., $t_{OFF} = 100$ Sec., n = 40:
c = 0 @ 1700 cycles, or
c = 1 @ 3000 cycles

FAILURES – Check for Opens on Rack, in Addition to Group B Tests End Points Including Top-Contact and Bottom-Contact Electrical Parameters.

NOTE: In No Way Does This Real-Time-Control De-Emphasize An Existing Disciplined And Total In-Process Quality-Control Program–From Incoming Inspection Through Warehousing.

circuit for open-emitter or open-base contacts. The failure-rate data for VERSAWATT product tested under the RTC accelerated conditions is shown in Table V.

Table V – Failure-Rate Data for 1972 for VERSAWATT Product Tested Under RTC

No. of Lots	No. of Units	No. Lots Failed	No. of Units Failed	Per cent Failed
104	4,150	1	6	0.144

Pull Strength

RTC may be practiced either on a lot-by-lot or shift basis. For example, each day, 30 samples per shift of power transistors are subjected to the following sequence of tests immediately after the soldering of the emitter, base, and collector contacts, i.e., just before the units are plastic encapsulated:

1. Autoclave (121°C, 30 psia, 4 hours)
2. Pull test on emitter-base contacts

The purpose of the autoclave is to age the unprotected soldered joint so that poor solder contacts are more easily detected. A typical distribution for the pull-strength test is shown in Fig. 5. A contact that cannot withstand at least

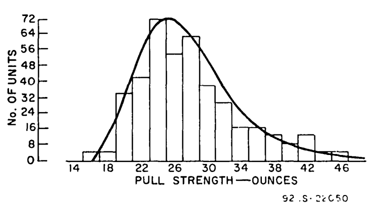

Fig. 5 – A typical pull-strength distribution after autoclave at 30 psia, T = 121°C, 4 hours.

10 ounces of pull is a failure. The autoclave-plus-pull-test RTC checks only the mechanical strength of the solder joint, and provides a direct measure of the success of the soldering process on a real-time basis. Deficiencies discovered as a result of the pull-strength test are corrected in subsequent shifts.

Wire-Bond Test

A thermal shock test of plastic product using wire bonds for emitter-base connections is performed weekly, and is very effective in monitoring a major failure mechanism which manifests itself as intermittent opens under thermal operation. The sampling plan and test conditions for the thermal-shock RTC are as follows:

Sample Size	Conditions	Cycles	Dwell Time
40	–65°C to 150°C	100	30 sec. at each extreme

The test proceeds as follows:

1. Perform end-point test for hot intermittent opens.
2. Make curve-tracer measurement with power applied; allow device to heat to 125°C.
3. Criticize data for stability criteria ("jitter").
4. Reject all unstable product and confirm rejects by failure analysis.

Aluminum-Gold Bonding

The aluminum-gold bonding RTC was developed to detect the failure mechanism of bond lifts in gold bonds caused by the presence of impurities in the gold. The failure mechanism occurs after life testing at high temperatures (200°C) without any apparent force being applied. The test is performed on a lot basis according to the following sampling plan, test conditions, and procedures:

1. Sample size is 15 devices with at least 30 wire bonds, pull-test one half of the wire bonds on each unit.
2. Bake 1 hour at 390°C.
3. Perform pull-test on remaining wires.
4. Observe number of bond-lift failures.

Fig. 6 is a graphical representation of the results of the aluminum-gold bonding test is performed on gold-plated parts for four different lots.

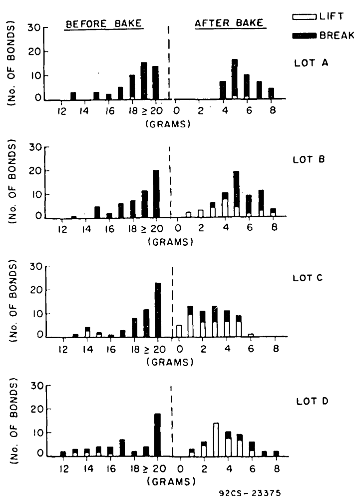

Fig. 6 – Bond-pull test results before and after 390°C bake.

Additional Tests

Additional real-time controls for maintaining the thermal-cycling capability of both hermetic- and plastic-packaged power transistors are shown in Table VI. These tests were developed because of the success of earlier RTC tests on the TO-220 plastic-packaged silicon power devices. RTC tests have developed for all silicon power transistors because of demands for increased reliability by automotive and consumer-product manufacturers.

Table VI — Real-Time Thermal-Cycling Test Conditions

PACKAGE	POWER (WATTS)	T_C(°C)	ΔT_C(°C)	t_{on}	t_{off}	HEAT SINK
TO-220 VERSAWATT	18	55 to 110	55	3 min.	3 min.	3°C/W
	4.75	35 to 155	125	50s	100s	Free Air
TO-3 Hermetic	16	40 to 130	90	50s	100s	Free Air
	56	70 to 120	50	15s	25s	6.3°C/W
TO-66 Hermetic	8.5	35 to 155	120	50s	100s	Free Air
RCA "TO-5" Plastic	1.5	35 to 135	100	60s	90s	Free Air
TO-5 Hermetic	1.5	30 to 115	85	60s	90s	Free Air

RTC Used to Achieve a Higher Reliability Level

Real-time controls not only maintain an acceptable reliability level as intended by the design of the product, but, because they are most often highly accelerated tests that show the difference in lot capability or margin of acceptability of the product manufactured, they tend to force the level of reliability higher. Fig. 7 shows how reliability levels are distributed with and without RTC.

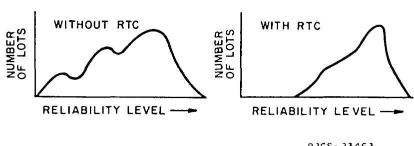

Fig. 7 — Distribution of reliability levels with and without RTC.

Conclusion

The accelerated tests of the real-time-control method of realiability determination are invaluable tools in attaining the most reliable silicon power transistors. These tests, used in conjunction with or as substitutes for the tests of the Group B or classical method, have been proven more effective than previous tests or applications-oriented derated conditions in predicting and assuring reliability levels. The success of the RTC method is directly related to a complete understanding of device and manufacturing-process capability.

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Solid State Division

Power Transistors

Application Note AN-6320

Radiation-Hardness Capability of RCA Silicon Power Transistors

R. B. Jarl

Because all military systems and weaponry may at one time be exposed to nuclear radiation, the effects of this radiation on the electronic system components must be determined and allowed for in the design. This Note describes the types of radiation damage that might be experienced by a power device and the tests used to determine the design most effective in preventing this damage.

"RADIATION HARDNESS"

In reality there is no such thing as a "radiation hard" transistor. A circuit or a device is considered "radiation hard" for a given application; the criteria is whether the entire circuit will perform its intended function after being exposed to a given radiation condition. There are several levels of nuclear radiation for which equipment is designed. For example, a hand-carried transceiver is designed for a radiation level of possibly one thousand times less than the guidance electronics in an ICBM warhead because, in its environment, the transceiver would be destroyed by a nuclear-weapon blast effect while the radiation level was still very low. An ICBM, on the other hand, flies outside the earth's atmosphere; hence, the destructive mechanism might not be blast effect but, more likely, neutron, gamma, and X-ray effects from the defensive missile burst. The levels of radiation from which manned aircraft, weapons stores, missile launch systems and the like have to be protected lie somewhere between the levels for the transceiver and the ICBM.

All transistors suffer degradation in gain, saturation, and leakage when exposed to nuclear radiation. The problem is to acquire sufficient knowledge of the transistor behavior after such exposure to allow the circuit designer to adjust the design for any undesirable changes that may occur in the device characteristics. The transistor designer may optimize a power device for radiation characteristics, but usually at the expense of its dc operating capability.

DAMAGE CLASSIFICATION

The types of radiation damage that may be inflicted upon a power device are classified as follows:

1. Physical Damage
2. Displacement Damage
3. Transient Radiation Energy Effect (TREE)
4. Ionizing Electromagnetic Pulse Effects (IEMP)

Physical Damage is inflicted on a device by "flash X-rays" from a nearby nuclear explosion. The X-rays produce a thermo-mechanical shock-wave in the dense material to which the transistor die is attached, usually molybdenum, copper, or gold. This shockwave then propagates into the transistor die and, if strong enough, will cause visible fracturing of the device.

Displacement Damage refers to changes in the atomic structure of the silicon crystal caused primarily by the disruption of the crystal lattice by impacting neutrons. The result of this damage is an increased recombination rate in the base and increased collector-body series resistance. The combined effect is manifest by a decrease in current gain and an increase in collector-emitter saturation voltage.

Transient Radiation Energy Effects (TREE) are caused mainly by gamma rays which produce large numbers of whole electron pairs in the collector-base and emitter-base junctions and cause large photo-currents to flow in the associated circuits. Intense gamma radiation may also cause current-gain degradation similar to that caused by neutron exposure, but the effect is modest compared to neutron effects.

Ionizing Electromagnetic Pulse (IEMP) Effects are the result of an intense ionization of the surroundings of an aircraft or space vehicle that produces a voltage gradient over the hull of several hundred thousand volts. Wherever there is a gap in the metal skin, such as access doors, windows, or antenna feedthroughs, the field will redistribute itself and follow the path of least resistance, possibly down into the vehicle electronics. Should the IEMP suppression be insuffi-

cient, high-current pulses may be induced in the system electronics. In most cases, the protection of the small signal and logic circuits will dictate IEMP suppression well below the capabilities of the power devices. Where a power device will be exposed to an IEMP condition, a pulsed safe-area test may be applied to simulate the situation and verify the device durability.

This Note is confined to the discussion of displacement damage (neutron effects) and transient-radiation effects (photocurrents), the main cause of failure of power devices exposed to nuclear radiation.

DEVICES TESTED

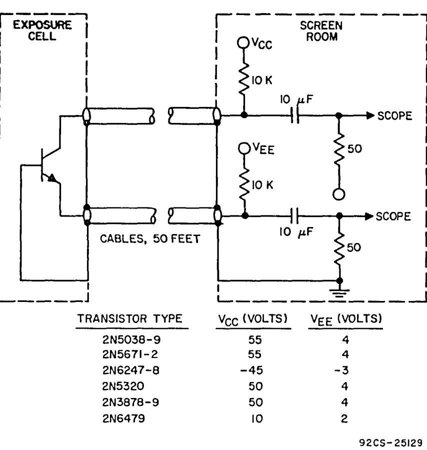
Recently, six different RCA power-transistor structures, as detailed in Table I, were subjected to fission spectrum neutron exposure and gamma radiation to determine their tolerance to nuclear and space radiation. Each sample consisted of 20 units. Except for the 2N6479, which was designed as a radiation tolerant device, these are standard commercial power transistors. The devices were evaluated for tolerance to neutron exposure and primary and secondary photocurrent generation as a function of gamma-ray intensity. Fig. 1 shows the circuit configuration and biasing used in measuring photocurrent.

TABLE I
IRRADIATED POWER-TRANSISTOR SWITCHES

Transistor	Description	Size (mils)	V_{CEO} (volts)	f_T (MHz)
2N6479	15A pwr sw. n-p-n	155 x 155	≃60-80	100-140
2N5671	30A pwr sw. n-p-n	210 x 220	100-140	60-90
2N5038	20A pwr sw. n-p-n	143 x 182	100-140	70-100
2N3878	7A pwr sw. n-p-n	103 x 103	75-110	60-90
2N5320	1A ampl. & sw. n-p-n	42 x 42	70-120	120-180
2N6247	10A ampl. p-n-p	150 x 150	60-80	4-10

Neutron Testing

Each unit tested for neutron tolerance received five fission-spectrum neutron exposures; the total fluence was sufficient to produce almost a total degradation in current gain (H_{FE}). Before and after each exposure, 5-volt, H_{FE}, appropriate V_{CE}(sat), V_{BE}(sat), I_{CBO}, I_{EBO} and switching speed data were taken. Only H_{FE} and V_{CE}(sat) degradation showed themselves to be of primary concern. I_{CBO} and I_{EBO} increased by only small and relatively manageable amounts.



TRANSISTOR TYPE	V_{CC} (VOLTS)	V_{EE} (VOLTS)
2N5038-9	55	4
2N5671-2	55	4
2N6247-8	-45	-3
2N5320	50	4
2N3878-9	50	4
2N6479	10	2

92CS-25129

Fig. 1. Circuit and biasing arrangement for measuring photocurrent.

V_{CEO} increased, as did f_T (current gain bandwidth product), while switching times decreased. V_{BE}(sat) increased somewhat but was still very manageable.

It is possible to predict H_{FE} after neutron exposure as a function of an empirically determined damage coefficient, K_D:

empirically determined damage coefficient, K_D:

$$K_D \Phi = \frac{1}{H_{FE\Phi}} - \frac{1}{H_{FEo}} \quad (1)$$

or

$$H_{FE\phi} = \frac{1}{K_D \Phi + \frac{1}{H_{FEo}}} \quad (2)$$

Where:

$H_{FE\phi}$ = Current gain after neutron exposure
H_{FEo} = Current gain before neutron exposure
Φ = Cumulative neutron fluence
K_D = Recombination-rate damage coefficient

(The derivation of Equations 1 and 2 is given in the Appendix.) The more common form of this relationship is:

$$K \Phi \left(\frac{1}{2\pi f_T}\right) = \frac{1}{H_{FE\phi}} - \frac{1}{H_{FEo}} \quad (3)$$

The factor $\frac{1}{2\pi f_T}$, the gain-bandwidth product, is an approximation of the base transit time. Eq. 3 works well with small signal-devices, where f_T may be easily and repeatedly measured at the same collector current and voltage levels as the other parameters of concern. The measurement of f_T at currents greater than 1 ampere is extremely difficult owing to junction-temperature problems. Furthermore, because of the low output impedances which exist, and the difficulty of obtaining a load impedance which must be even lower, the f_T results are only qualitative in

nature. The gain-bandwidth product within members of a given device design are generally uniform; therefore, for this study, $\frac{1}{2\pi f_T}$ was merged with K (the recombination-rate damage coefficient) such that:

$$K_D = \frac{K}{2\pi f_T} = \text{composite } H_{FE} \text{ damage coefficient.}$$

Figs.2, 3(a) through 3(m),and 4(a) through 4(f) present the following typical information on the devices tested:

V_{CE}(sat) vs cumulative neutron fluence (Φ) at a forced gain of 4 (I_C/I_B=4).

V_{CE}(sat) vs cumulative neutron fluence (Φ) at a forced gain of 8 (I_C/I_B=8).

H_{FE} vs I_C prior to radiation

Recombination-rate damage coefficient (K_D) vs I_C.

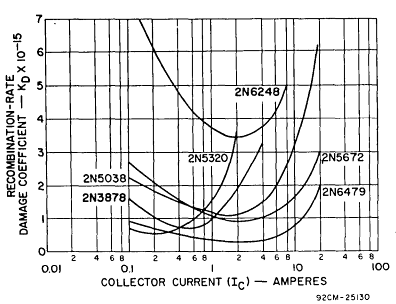
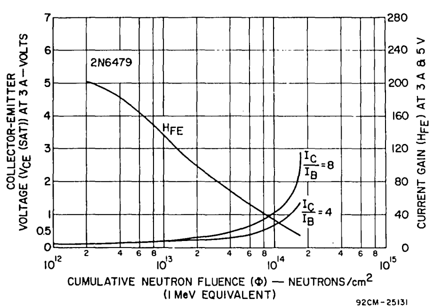
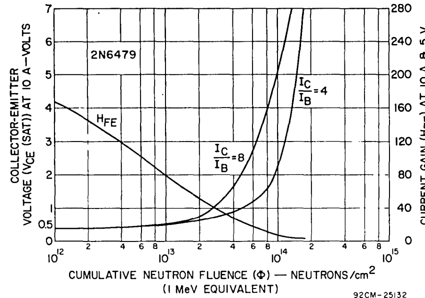


Fig. 2. Composite graph of recombination-rate damage coefficient as a function of collector current for the power transistors discussed in this Note.

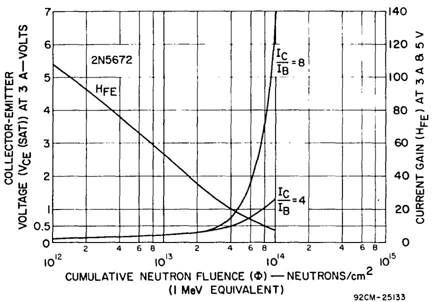


(a) 2N6479 (3A)

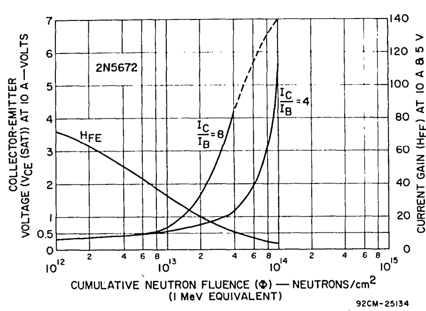
Fig. 3. Collector-emitter saturation voltage and current gain as a function of cumulative neutron fluence for the power transistors discussed in this Note.



(b) 2N6479 (10A)

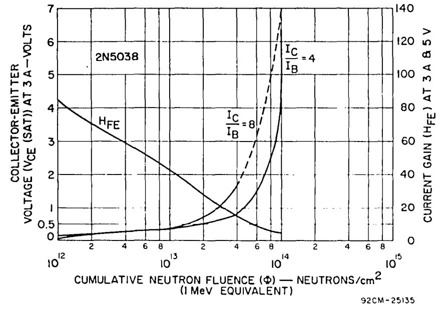


(c) 2N5672 (3A)

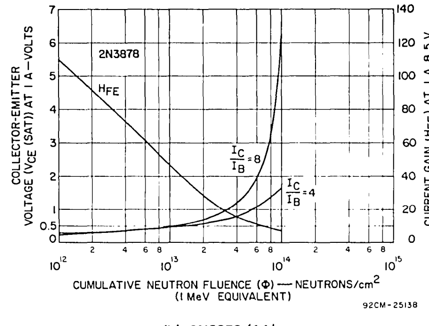


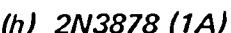
(d) 2N5672 (10A)

Fig. 3. Collector-emitter saturation voltage and current gain as a function of cumulative neutron fluence for the power transistors discussed in this Note.

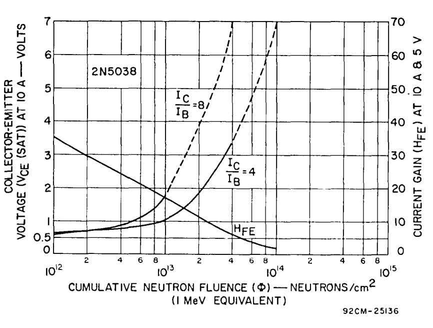


(e) 2N5038 (3A)

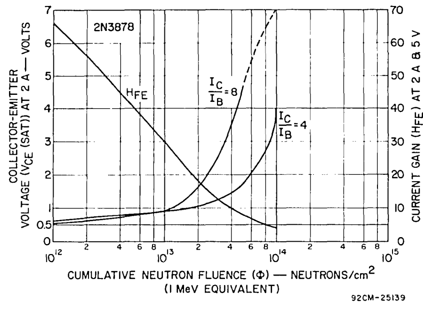




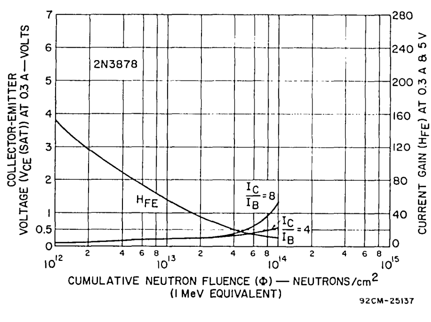
(h) 2N3878 (1A)



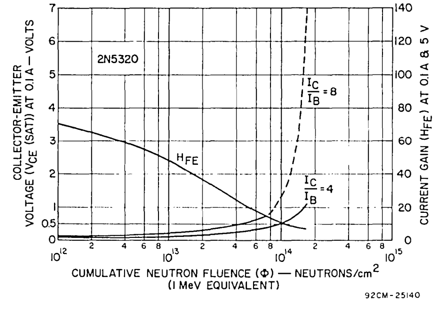
(f) 2N5038 (10A)



(i) 2N3878 (2A)



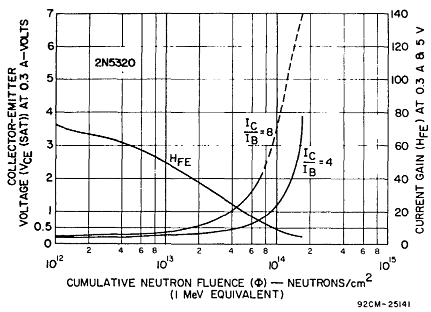
(g) 2N3878 (0.3A)



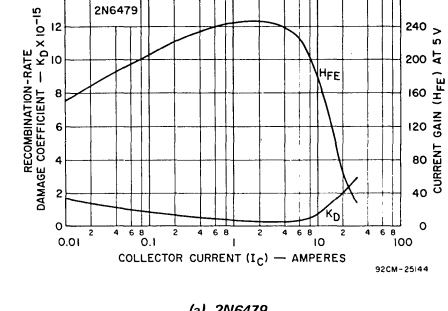
(j) 2N5320 (0.1A)

Fig. 3. Collector-emitter saturation voltage and current gain as a function of cumulative neutron fluence for the power transistors discussed in this Note.

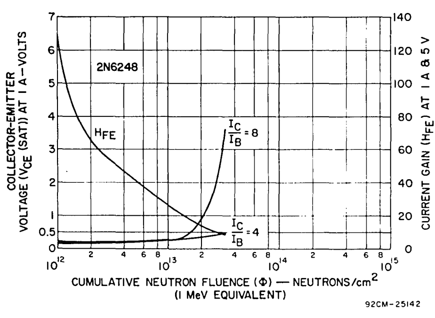
Fig. 3. Collector-emitter saturation voltage and current gain as a function of cumulative neutron fluence for the power transistors discussed in this Note.



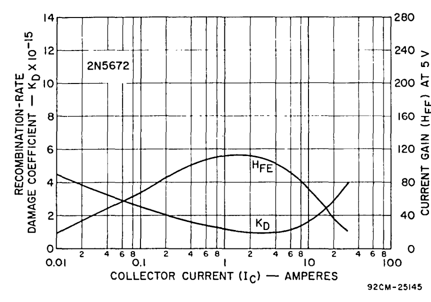
(k) 2N5320 (0.3A)



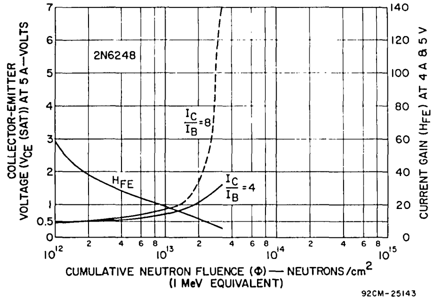
(a) 2N6479



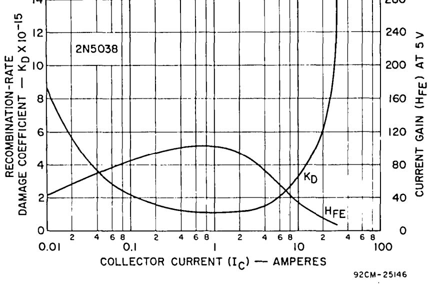
(l) 2N6248 (1A)



(b) 2N5672



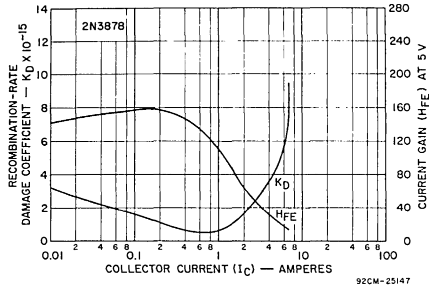
(m) 2N6248 (5A, V_{CE}; 4A, H_{FE})



(c) 2N5038

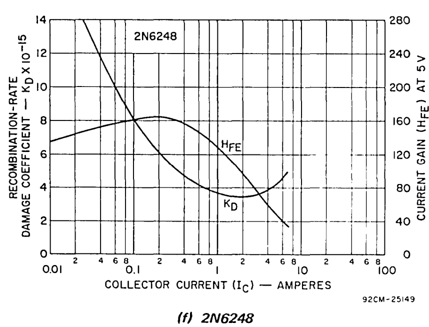
Fig. 3. Collector-emitter saturation voltage and current gain as a function of cumulative neutron fluence for the power transistors discussed in this Note.

Fig. 4. Recombination-rate damage coefficient and current gain as a function of collector current for the power transistors discussed in this Note.



(d) 2N3878

(e) 2N5320



(f) 2N6248

Fig. 4. Recombination-rate damage coefficient and current gain as a function of collector current for the power transistors discussed in this Note.

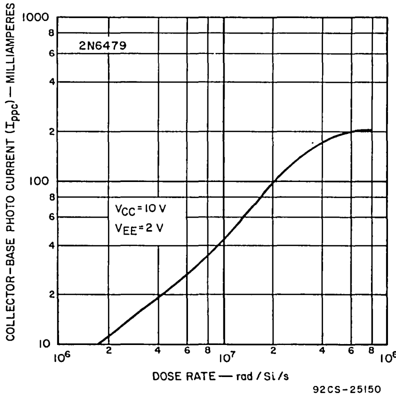
Photocurrent Testing

The effect on power transistors of high-intensity radiation, such as high-energy electrons, gamma rays, and X-rays, is ionization in the collector-base and emitter-base depletion layers that produces primary photocurrents proportional to the electrical volumes of the junctions. When these photocurrents flow through the biasing networks and are sufficient to produce the appropriate IR drops in the circuit extrinsic to the base-emitter circuit, the device may become forward biased, producing what is known as "secondary photocurrent" by means of conventional H_{FE} amplification. Primary photocurrent production is predictable and can be stated as a coefficient of 6.4 μA/rad(Si)/cm^3. The expression for the collector-base photocurrent, I_{ppc}, may be written as

$$I_{ppc} = 6.4 \times 10^{-6} \times A \times W$$

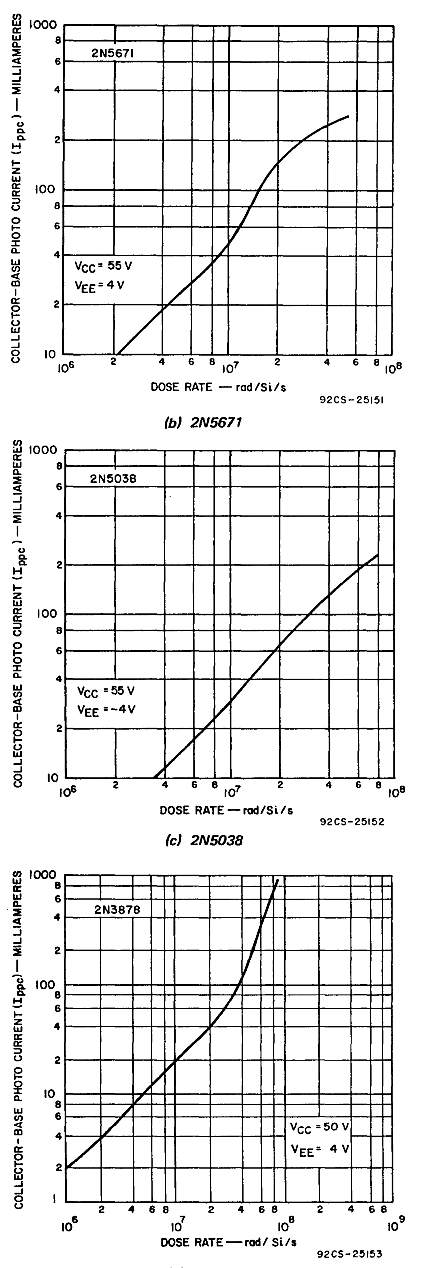
where A is the area of the base in cm^2 and W is the width of the collector-base depletion layer in centimeters. Note that W is to some degree voltage dependent; therefore, I_{ppc} will also be voltage dependent to the extent that the collector depletion layer widens according to the collector voltage and the impurity ratio between the base and collector layers.

Fig. 1 shows the circuit used for obtaining the photocurrent data in this Note; it is not entirely satisfactory for the levels of photocurrent that may occur in large power devices. Because the photocurrent is measured by monitoring the voltage across a 50-ohm termination resistor, the arrangement saturates at a photocurrent of $\frac{V_{CC}}{50}$ thus, the amount of current measured is not a true indication of I_{ppc} at the higher exposure levels. The curves of Figs. 5(a) through 5(f) should be evaluated with this fact in mind.



(a) 2N6479

Fig. 5. Collector-base photocurrent as a function of dose rate for the power transistors discussed in this Note.

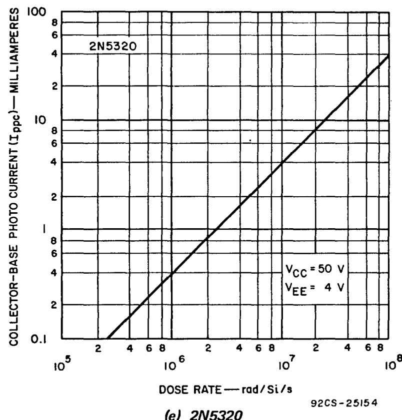


(b) 2N5671

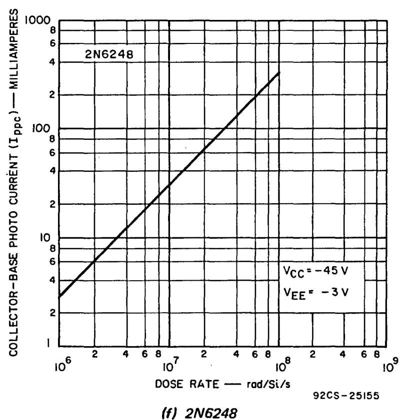
(c) 2N5038

(d) 2N3878

Fig. 5. Collector-base photocurrent as a function of dose rate for the power transistors discussed in this Note.



(e) 2N5320



(f) 2N6248

Fig. 5. Collector-base photocurrent as a function of dose rate for the power transistors discussed in this Note.

Characterization of the devices tested consisted of measuring the primary photocurrents in the transistors and plotting these as functions of radiation dose rate. Tests were performed at the 25 MeV linear-accelerator facility at the White Sands Missile Range, New Mexico. Radiation pulse widths of 5 to 6 microseconds were used to attain equilibrium photocurrent. All testing was performed with the accelerator in the electron-beam mode of operation. Variations in dose rate were obtained by positioning the test device at different distances from the beam port. Dose rates ranged from about 5 x 10^5 to 2 x 10^8 rad(Si)/s and were determined from the responses of a calibrated diode. The radiation response of the diode was, in turn, calibrated against lithium fluoride, Tiny Thermoluminescent Dosimetry Discs (TTDD's), and calcium fluoride impregnated Teflon chips, both of which were positioned in the area normally occupied by the device under test.

The photocurrent characteristics of the various devices evaluated are shown in Table II and described below.

TABLE II
DEVICE PHOTOCURRENT CHARACTERISTICS

Transistor Type	TOTAL GAMMA DOSE (rads-silicon x 10^3)				
Test No.	1	2	3	4	5
2N6479	.93	2.2	4.2	33.2	79.2
2N5671	1.2	2.3	3.7	26.7	58
2N5038	1.5	2.7	4.1	25.1	38
2N3878	.93	2.13	3.63	24.6	49.6
2N5320	.85	2.0	3.4	32	73
2N6247	.83	1.68	2.68	6.1	26.3

2N6479. Relatively linear collector-base photocurrents were observed. The emitter-base plot was non-linear. Secondary photocurrent began at 3 x 10^7 rad/s. The primary photocurrent generation rates in amperes per rad per second are:

collector-base 5×10^{-9} A/rad/s
emitter-base 1×10^{-11} A/rad/s (approx.) non-linear

2N5671-2. Both the collector-base and emitter-base junctions exhibit a linear relationship between the photocurrent and the dose rate. However, this transistor type switched into the secondary-photocurrent mode from 5 x 10^6 to 2 x 10^7 rad/s, so that the points of the emitter plot are accordingly reduced in quantity. The plot in Fig. 5(b) yields a primary photocurrent generation rate of:

collector-base 4.8×10^{-9} A/rad/s
emitter-base 2×10^{-10} A/rad/s

2N5038-9. Linear relationships between the photocurrent and dose rate for both collector-base and emitter-base junctions were obtained. The onset of secondary photocurrent was observed at dose rates of 2 x 10^7 to 2 x 10^8 rad/s. The primary photocurrent generation rates taken from Fig. 5(c) are:

collector-base 3.1×10^{-9} A/rad/s
emitter-base 6.5×10^{-11} A/rad/s

2N3878-9. The collector-base junction shows a linear relationship between photocurrent and dose rate, whereas the emitter base is very non-linear. The non-linearity holds even though data is plotted from 5 x 10^5 to 10^8 rad/s, and secondary photocurrent did not begin until the dose rate was 3 x 10^7 rad/s. The primary photocurrent-generation rates are:

collector-base 2.4×10^{-9} A/rad/s
emitter-base 1×10^{-11} A/rad/s (approx.) non-linear

2N5320. Linear results. Secondary photocurrent is not observed for this device for dose rates as high as 3 x 10^7 rad/s. The collector-base photocurrent generation rate is 4 x 10^{-10} A/rad/s.

2N6247-8. Linear relationship between photocurrent and dose rate for both junctions were seen. Secondary photocurrent was observed at about 3 x 10^7 rad/s. Primary-photocurrent generation rates are:

collector-base 2.9×10^{-9} A/rad/s
emitter-base 2.1×10^{-10} A/rad/s

APPENDIX
DERIVATION OF THE NEUTRON-DAMAGE COEFFICIENT

The common-emitter current gain at a constant voltage may be expressed as:

$$H_{FE} = \frac{1}{t_b R} - 1 \qquad \text{(A-1)}$$

where:

t_b = base transit time
R = base recombination rate

The recombination rate (R) is proportional to the number of defects produced in the base by neutron radiation. The number of defects is proportional to the total exposure. Therefore, R may be expressed as:

$$R = R_o + K\Phi \qquad \text{(A-2)}$$

where:

K = a damage coefficient
Φ = total neutron fluence

The base transit time, (t_b), may be approximated by the relationship:

$$t_b = \frac{1}{2\pi f_T} \qquad \text{(A-3)}$$

Manipulation of Eqs. A-1 and A-2 yields the expression:

$$K\Phi = \frac{1}{t_b}\left(\frac{1}{H_{FE\phi}+1} - \frac{1}{H_{FEo}+1}\right) \qquad \text{(A-4)}$$

where:

H_{FEo} = H_{FE} prior to neutron exposure[1]
$H_{FE\phi}$ = H_{FE} after neutron exposure[2]

Simplifying,

$$H_{FEo} + 1 = H_{FEo} \qquad \text{(A-5)}$$

Eq. A-4 now becomes

$$K\Phi = \frac{1}{t_b}\left(\frac{1}{H_{FE\phi}+1} - \frac{1}{H_{FEo}}\right) \qquad \text{(A-6)}$$

A reorganization yields:

$$1 + H_{FE} = \frac{1}{t_b K\Phi + \frac{1}{H_{FEo}}} \qquad \text{(A-7)}$$

If Eq. A-3 is then substituted in Eq. A-7, the expression becomes:

$$1 + H_{FE} = \frac{1}{\frac{K\Phi}{2\pi f_T} + \frac{1}{H_{FEo}}} \qquad \text{(A-8)}$$

As described in the main text, f_T and K may be merged as:

$$\frac{K}{2\pi f_T} = K_D \qquad \text{(A-9)}$$

$1 + H_{FE\phi}$ is usually expressed as $H_{FE\phi}$, and the expression becomes:

$$H_{FE\phi} = \frac{1}{K_D\Phi + \frac{1}{H_{FEo}}} \qquad \text{(A-10)}$$

REFERENCES

1. Larin, Radiation Effects in Semiconductors, pp. 17, eq. 2.19, 2.20, John Wiley, New York, 1968
2. Same as ref. 1, pp. 14, eq. 2.11
3. Rockwell International, Internal letter 73-551-012-79, October 15, 1973

High-Reliability RF Power Transistors

High-Reliability RF Power Transistors

During the past several years, the RCA Solid State Division has conducted intensive programs to improve the quality and reliability of rf power transistors. The significant technological improvements that have resulted from these programs have advanced rf power transistors to the point that such devices are now used with confidence in numerous equipments in which high reliability is a prime requisite.

Design Features

The recent technological advances in RCA rf power transistors are extensions of the RCA overlay-transistor concept. Table 3-1 summarizes some of the major design features of RCA rf power transistors.

Overlay Transistor Structure—The RCA overlay design,* the basic type of structure used for RCA high-reliability rf power transistors, employs a unique emitter construction that makes possible exceptional power-frequency capabilities. The emitter is separated into many discrete sites that are connected in parallel to provide the increased current-handling capability required at high power levels. This type of emitter structure provides the high ratio of emitter periphery to base area that is essential to the generation of high power levels at high frequencies. In addition, the overlay construction makes possible current densities in the emitter mentallizing fingers that are significantly less than those in other high-frequency transistor structures. The adverse effect of high current density on transistor reliability, particularly with respect to failures caused by aluminum migration, is discussed subsequently.

The reduced emitter current density in overlay transistors can be attributed primarily to the relatively broad metal fingers used to interconnect the discrete emitter sites. These fingers are typically an order of magnitude wider than the ones used in interdigitated or mesh types of transistor structures. In addition, the separation between the emitter and base metallized fingers is 3 to 4 times greater than that in other types of high-frequency transistor structures. This increased separation permits the deposition of thicker metallizing layers and, therefore, results in a further reduction in current densities.

Emitter-Site Ballasting—A major technological development in the evolution of rf power transistors is a unique process in which an integral series resistor is introduced directly above each emitter site of an overlay transistor structure. RCA uses this process, which is referred to as emitter-site ballasting, to achieve rugged and reliable fine-line precise-geometry rf power transistors without sacrifice in high-frequency performance.

In overlay transistors, additional conducting and insulating layers can be readily introduced between the aluminum metallization and the shallow diffused emitter sites (shallow emitter diffusion is a requirement for good microwave performance). RCA has developed a technique in which a polycrystalline silicon layer (PSL) is interspersed between these regions. This interlayer, the resistivity of which can be accurately controlled by impurity doping, is used as the medium for the emitter-site ballasting of RCA microwave power transistors. Fig. 3-1 shows top and cross-sectional views of the emitter-finger structure of an overlay transistor that includes the polycrystalline silicon layer.

The resistivity of the polycrystalline silicon layer and the geometry of the contacting aluminum are controlled to form a ballast resistor in series with each emitter site. This ballasting has proved very effective in the reduction of hot spots, i.e., localized heated areas that result when the emitter-to-collector current is allowed to concentrate within small regions of the transistor pellet. Such current concentrations may occur when a large number of transistor elements are interconnected electrically, but are not coupled thermally. The formation of such hot spots can result in a regenerative condition that leads to localized thermal runaway and the consequent destruction of the transistor.

* U.S. Patent No. 3,434,019, March 18, 1969

Table 3-1 — Design Features

Feature	Advantages
Overlay structure	Reduces current density Minimizes aluminum migration
Emitter-site ballasting	Reduces formation of isolated hot spots Improves safe operating area Improves transistor resistance to failure under high VSWR conditions
Polycrystalline silicon layer (PSL)	Minimizes "alloy spike" failures Minimizes dielectric failures
Glass-passivated aluminum metallizing	Minimizes aluminum migration
Hermetic package	Improves resistance to moisture Results in rugged mechanical construction Features low inductances and low parasitic capacitances Provided in both stripline and coaxial configurations

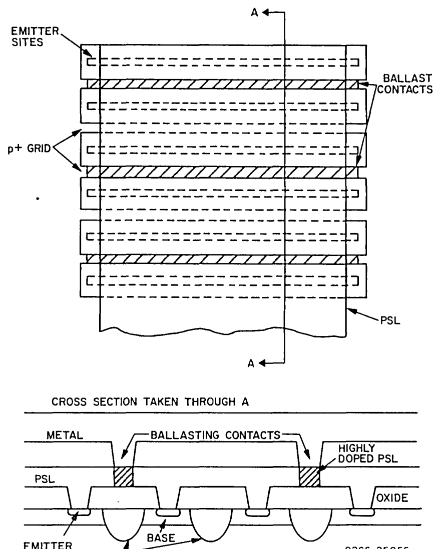


Fig. 3-1—Emitter-finger structure of an overlay transistor that contains the polycrystalline silicon layer (PSL).

The ballast resistors connected in series with each emitter site provide internal biasing control to prevent excessive current in any portion of the transistor. The formation of hot spots is thereby significantly reduced. Because the overlay construction results in an emitter that is segmented into many separate sites connected in parallel, each hot spot may be isolated and controlled so that the injection of charge carriers across the transistor chip is made more uniform.

The emitter-site ballasting results in a more uniform current distribution and, therefore, makes possible more effective utilization of emitter periphery. Consequently, transistor power-output and overdrive capabilities are increased, and the forward-bias safe-operating area (determined by infrared measurements) is enlarged. This latter factor is important for linear applications of high-frequency power transistors.

The formation of transistor hot spots under rf conditions increases as the output VSWR increases. Transistor failures caused by high VSWR conditions are often related to forward-bias second breakdown, which is characterized by extremely high localized currents. Emitter-site-ballasted transistors, therefore, have a substantially greater immunity to failure produced by high VSWR conditions such as those encountered in some broadband amplifiers. This immunity is particularly demonstrated by the RCA 2-GHz series of microwave power transistors. For example, the RCA-2N6265, 2N6266, RCA2003, and RCA2005 2-GHz transistors are characterized to withstand an infinite VSWR at rated power levels and the specified frequency. Higher-power types included in the 2-GHz series, such as the 2N6267 and the RCA2010, are characterized to withstand a VSWR of 10 to 1 at rated power levels and the specified frequency.

Polycrystalline Silicon Layer—In addition to its use as a medium for emitter-site ballasting, the polycrystalline silicon layer (PSL) also helps to minimize two other thermally induced failure modes that occur in high-frequency power transistors. As shown in Fig. 3-1, this layer forms a barrier between the aluminum metallization and the shallow diffused emitter region and, therefore, substantially reduces the possibility of "alloy spike" failures, i.e., emitter-to-base shorts caused by intermetallic formations of silicon and aluminum that may occur under severe hot-spot conditions.

The polycrystalline silicon layer also provides a barrier between the aluminum emitter finger and the silicon-dioxide insulating layer over the base. This barrier minimizes the possibility of emitter-to-base shorts caused by dielectric failures that result from an interaction between the aluminum and the silicon dioxide.

Recent reliability studies of high-frequency transistors operated under overstress conditions (i.e., at junction temperatures greater than 200°C) demonstrated an order of magnitude improvement in the mean time between failures for types that contain the polycrystalline silicon layer over that of similar types in which this layer is not used. These results verify that the PSL technique contributes substantially to over-all device reliability and therefore is an important feature in the construction of high-frequency power transistors.

Glass-Passivated Aluminum—In RCA rf power transistors, a silicon dioxide layer is deposited over the aluminum metallization. This deposition results in an increase of 40 per cent in the activation energy required for the initiation of aluminum migration. The mean time between failure of large crystalline aluminum passivated in this way is increased by approximately four times at a current density of 1×10^5 amperes/centimeter^2. The silicon dioxide layer also protects the aluminum from contamination and from damage that may result because of scratches or smears during device assembly.

RCA has recently concluded a study on electron-migration failure mechanisms in rf power transistors. The RCA-2N6267, a 10-watt, 2-GHz transistor that has the highest current density of any RCA microwave power type, was used as the test device in this study. The median time to failure (MTF) was determined for more than one-hundred 2N6267 transistors that were dc-biased to simulate high-current-density and high-junction-temperature operating conditions. The effects of hot-spot junction temperatures over the range from 230°C to 300°C, as determined from infrared scanning,

and of current densities in the metallization of 1 x 10^5 amperes/centimeter^2 to 3 x 10^5 amperes/centimeter^2 were observed. On the basis of the results obtained, the MTF of the transistors at the typical operating current density of 1 x 10^5 amperes/centimeter and the typical operating junction temperature of 150°C was predicted to be 100 years. Even at an operating junction temperature equal to twice the typical value (i.e., at 2 x 10^5 amperes/centimeter^2), an MTF of 12 years is predicted for operation of the transistors at a junction temperature of 150'C. These results indicate that, under normal conditions, migration failures should not be a factor for RCA rf power transistors.

Gold Metallization—In some RCA microwave power transistors, particularly those intended for military phased-array-radar applications, gold metallization is employed to meet government specifications. These transistors use a metallization system that was developed by RCA for a high-volume, high-reliability military application. In this system, the contacting layer is a noble-metal, silicide upon which successive layers of titanium, platinum, and gold are superimposed. Tests of transistors operated under extreme overstress conditions (i.e., at current densities equal to twice the typical value and a hot-spot junction temperature of 285°C) showed that transistors that use the gold metallization have a median time to failure 11 times that of transistors with the same geometry that use glass-passivated aluminum metallization. The MTF data given in the preceding paragraph for overlay transistor structures that use glass-passivated aluminum metallization, however, show that this type of metallization is more than adequate for most applications.

Hermetic Transistor Packages—The package of a power transistor used in microwave applications becomes an integral circuit element that has a critical bearing on over-all circuit performance. A suitable package for a microwave power transistor should have good thermal properties and low parasitic reactances. Package parasitic reactances and resistive losses significantly affect circuit performance characteristics such as power gain, bandwidth, and stability. The most critical parasitics are the inductances of the emitter and base leads. The higher the power capabilities of the transistor, the lower the device impedances, particularly at the input. For high-power high-frequency transistors, the input impedance is determined primarily by the package, rather than by the transistor pellet. Consequently, such transistors should be encased in well-designed and well-constructed packages.

All RCA high-reliability of power transistors are supplied in metal-ceramic or laminated-ceramic packages. These packages, which are sealed with metallized ceramic interfaces, provide a true hermetic enclosure that can withstand thermal cycling from 65°C to + 200°C and power cycling such as may be encountered in transmitter service. In addition, these packages are mechanically rugged and are essentially impervious to moisture and other external contaminants.

Fig. 3-2 shows photographs of packages used for RCA high-reliability rf power transistors. These RCA hermetic transistor packages are specially designed to have extremely good thermal properties. For example, in the metal-ceramic packages, such as the HF-11, HF-21, and HF-28, the transistor pellet is mounted on a silver block or stud which is connected to the collector terminal. In the HF-46, a laminated-ceramic package, the pellet is mounted directly on a beryllium-oxide substrate. In each case, the initial heat spreader, i.e., the silver block or beryllium-oxide substrate, is a material that has a high thermal conductivity.

The RCA microwave-transistor packages, in addition to being mechanically rugged hermetic designs with excellent thermal properties, also have very low values of parasitic reactances and excellent isolation between input and output.

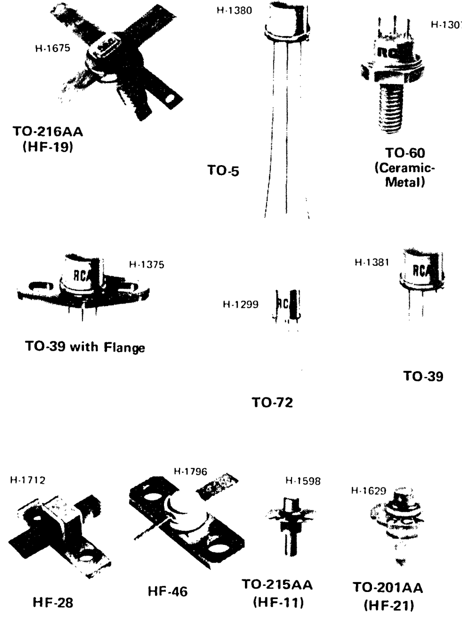


Fig. 3-2– Packages used for RCA high-reliability rf power transistors

Special Rating Concepts

Unlike low-frequency high-power transistors, many rf devices can fail within the dissipation limits set by the classical junction-to-case thermal resistance during operation under conditions of high load VSWR, high collector supply voltage, or linear (Class A or AB) operation. Failure can be caused by hotspotting, which results

from local current concentration in the active areas of the device, and may appear as a long-term parameter degradation. Localized hotspotting can also lead to catastrophic thermal runaway.

The presence of hotspots can make virtually useless the present method of calculating junction temperature by measurements of average thermal resistance, case temperature, and power dissipation. However, by use of an infrared microscope, the spot temperature of a small portion of an rf transistor pellet can be determined accurately under actual or simulated device operating conditions. The resultant peak-temperature information is used to characterize the device thermally in terms of junction-to-case hotspot thermal resistance, θ_{JS-C}.

The use of hotspot thermal resistance improves the accuracy of junction temperature and related reliability predictions, particularly for devices involved in linear or mismatch service.

DC Safe Area—The safe area determined by infrared techniques represents the locus of all current and voltage combinations within the maximum ratings of a device that produce a specified spot temperature (usually 200°C) at a fixed case temperature. The shape of this safe area is very similar to the conventional safe area in that there are four regions, as shown in Fig. 3-3: constant current, constant power, derating power, and constant voltage.

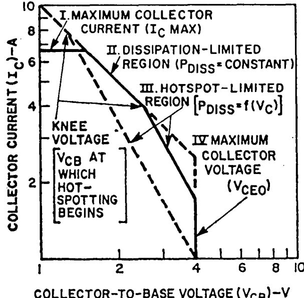


Figure 3-3. Safe-area curve for an rf power transistor determined by infrared techniques.

Regions I and IV, the constant-current and constant-voltage regions, respectively, are determined by the maximum collector current and V_{CEO} ratings of the device. Region II is dissipation-limited; in the classical safe area curve, this region is determined by the following relationship:

$$P_{max} = \frac{T_J(max) - T_C}{\theta_{J-C}}$$

where T_C is the case temperature.

This relationship holds true for the infrared safe area; P_{max} may be slightly lower because the reference temperature $T_{J(max)}$ is a peak value rather than an average value. The hotspot thermal resistance (θ_{JS-C}) may be calculated from the infrared safe area by use of the following definition:

$$\theta_{JS-C} = \frac{T_{JS} - T_C}{P}$$

where T_{JS} is highest spot temperature [$T_{J(max)}$ for the safe area] and P is the dissipated power (= I × V product in Region II).

The collector voltage at which regions II and III intersect, called the knee voltage V_K, indicates the collector voltage at which power constriction and resulting hotspot formation begins. For voltage levels above V_K, the allowable power decreases. Region III is very similar to the second-breakdown region in the classical safe area curve except for magnitude. For many rf power transistors, the hotspot-limited region can be significantly lower than the second-breakdown locus. Generally V_K decreases as the size of the device is increased.

Fig. 3-4 shows the temperature profiles of two transistors with identical junction geometrics that operate at the same dc power level. If devices are operated on the dissipation-limited line of their classical safe areas, the profiles show that the temperature of the unballasted device rises to values 130°C in excess of the 200°C rating. Temperatures of this magnitude, although not necessarily destructive, seriously reduce the lifetime of the device.

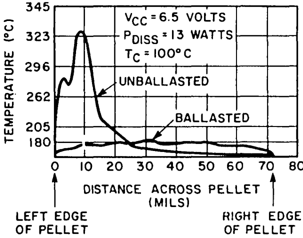


Figure 3-4. Thermal profiles of a ballasted and an unballasted power transistor during dc operation.

Effect of Emitter Ballasting—The profiles shown in Fig. 3-4 also demonstrate the effectiveness of emitter ballasting in the reduction of power (current) constriction. In the ballasted device, a biasing resistor is introduced in series with each emitter or small groups of emitters. If one region draws too much current, it will be biased towards cutoff, allowing a redistribution of current to other areas of the device.

The amount of ballasting affects the knee voltage, V_K, as shown in Fig. 3-5. A point of diminishing returns is reached as V_K approaches V_{CEO}.

RF Operation—In normal class C rf operation, the hotspot thermal resistance is approximately equal to the classical average thermal resistance. If the proper collector loading (match) is maintained, θ_{JS-C} is independent of output power at values below the saturated- or

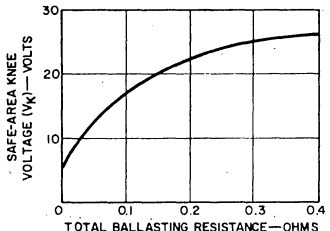
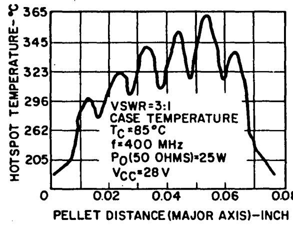


Figure 3-5. Safe-area voltage for an rf power transistor as a function of total ballasting resistance.

slumping-power level, and is independent of collector supply voltage at values within + 30 per cent of the recommended operating level.

Power constriction in rf service normally occurs only for collector load VSWR's greater than 1.0. A transistor that has a mismatched load experiences temperatures far in excess of device ratings, as shown in Fig. 3-6(a) for VSWR = 3.0. For comparison, the temperature profile for the matched condition is shown in Fig. 3-6(b).

Fig. 3-7 is a typical family of thermal-resistance curves that indicate the response of a device to various



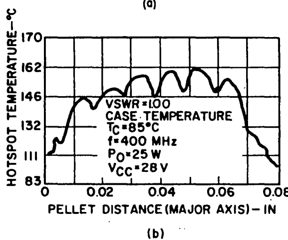


Figure 3-6. Thermal profile of a power transistor during rf operation: (a) under mismatched conditions; (b) under matched conditions.

levels of VSWR and collector supply voltage. $\theta_{S\text{-}C}$ responds to even slight increases in VSWR above 1.0 and saturates at a VSWR in the range of 3 to 6. The saturated level increases with increasing supply voltage. Devices with high knee voltages tend to show smaller changes of $\theta_{S\text{-}C}$ with VSWR and supply voltage. $\theta_{S\text{-}C}$ under mismatch is independent of frequency and power level, and reaches its highest values at load angles that produce maximum collector current. Power level does, however, influence the temperature rise and probability of failure.

Device failure can also occur at a load angle that produces minimum collector current. Under this condition, collector voltage swing is near its maximum, and an avalanche breakdown can result. This mechanism is sensitive to frequency and power level, and becomes predominant at lower frequencies because of the decreasing rf-breakdown capability of the device.

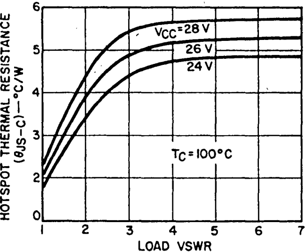


Figure 3-7. Mismatch-stress thermal characteristics for the 2N5071.

Collector mismatch can be caused by the following conditions:

1. Antenna loading changes in mobile applications when the vehicle passes near a metallic structure.
2. Antenna damage.
3. Transmission-line failure because of line, connector, or switch defects.
4. Variable loading caused by nonlinear input characteristics of a following transistor (particularly broadband) or varactor stage.
5. Supply-voltage changes that reflect different load-line requirements in class C.
6. Tolerance variations on fixed-tuned or stripline circuits.
7. Matching network variations in broadband service.

Case-Temperature Effects—The thermal resistance of both silicon and beryllium oxide, two materials that are commonly used in rf power transistors, increases about 70 per cent as the temperature increases from 25 to 200°C. Other package materials such as steel, kovar, copper, or silver, exhibit only minor increases in thermal resistance (about 5 per cent). The over-all increase in $\theta_{S\text{-}C}$ of a device depends on the relative amounts of these materials used in the thermal path of the device; typically the increase of $\theta_{S\text{-}C}$ ranges from 5 per cent to 70 per cent. Fig. 3-8 shows the rf and dc thermal resistance coefficients for a typical rf transistor. For both cases, the coefficient is referenced to a 100°C case and is defined as follows:

$$K_{\theta 100} = \frac{\theta_{JS-C}}{\theta_{JS-C} \text{ at } T_C = 100°C}$$

The rf coefficient changes more than the dc coefficient, because of the power constriction that occurs in rf operation at elevated case temperature.

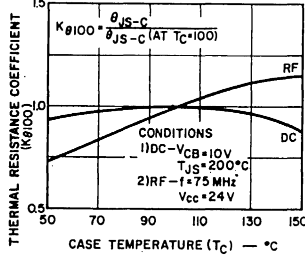


Figure 3-8. Thermal-resistance coefficient for the 2N5071.

RF Avalanche Breakdown Voltage—The voltage breakdown mechanism is a time dependent phenomenon; and, therefore, breakdown voltages under pulsed and rf conditions are higher than the dc values. This is obviously true when the time during which the device is subject to fields of breakdown intensity is short with respect to the mechanism time constant and the off-time is sufficiently long to permit the relaxation of this mechanism. Under these conditions, a catastrophic level cannot be reached during a single pulse, and the accumulative effect of several pulses is prevented by the off-time relaxation. Tests have demonstrated that a device that has a dc breakdown voltage (BV_{CBO}) of between 60 and 80 volts can often withstand about 135 volts (collector to base) under pulse lengths shorter than 0.25 microsecond. RF performance (particularly classes B and C) is analogous to pulsed operation in the sense that the instantaneous rf voltages are at their peak value for only a fraction of the cycle. (For example, at 1.3 GHz, the period of a cycle is 0.77 nanosecond and the voltage is peaked for less than ¼ cycle. Therefore, the high-intensity fields exist for less than 0.19 nanosecond.

The increased rf breakdown-voltage capability has been shown empirically. RF breakdown voltages approximately twice that at low frequencies have been achieved. One possible theoretical explanation is based on the following relationship between rf breakdown and current gain which in effect expresses the relationship at one operating frequency in terms of the alpha and beta cut-off frequencies of the device.

$$\frac{V_{CBO}^{(RF)}}{V_{CBO}} = \left\{\left[1 + \left(\frac{\omega}{\omega_\beta}\right)^2\right] \times \left[1 + 2M\left(\frac{\omega}{\omega_\beta}\right)^2\right]\right\}^{1/2n}$$

where M = "excess phase" factor, ω_β = beta cut-off frequency = ω_T / β, η = empirical constant ranging from 2 to 10, and ω = operating frequency

In reality ω_0/ω_β is a relationship between the device transit times (i.e., time constants) and the operating frequency, for example:

$$\frac{\omega_o}{\omega_\beta} = \frac{2\pi f_o}{\frac{1}{\tau_\beta}} = \frac{2\pi}{} \frac{\tau_\beta}{\tau_o}$$

$$\text{where } \tau = \frac{1}{\omega_\beta} = \text{beta transit time}$$

$$\text{and } \tau_o = \frac{1}{f_o} = \text{period (time of one cycle)}$$

The ratio $\omega/\omega\beta$, therefore, normalizes the time (duration) of voltage stress to the time of transit of the device.

The curve of this function is shown in Fig. 3-9. This curve indicates that a transistor operating at its cutoff frequency ω_t could theoretically have a breakdown voltage equal to six times the dc breakdown voltage. More typically, two to three times the dc breakdown voltage has been observed. A further increase in safety factor is obtained from the fact that the V_{CEsat} is greater under rf conditions because the instantaneous peak voltage is given by

$$\begin{aligned} V \text{ inst.} &= V_{CC} + (V_{RF} \text{ peak}) \\ &= V_{CC} + (V_{CC} - V_{CE}sat) \\ &= 2\,V_{CC} - V_{CE}sat \end{aligned}$$

$V_{CE}sat$ increases with operating frequency; the maximum instantaneous voltage, therefore, is lower at the higher frequencies further increasing the safety factor.

Both theoretical and empirical evidence support the contention that rf breakdown voltage can be considerably higher than BV_{CBO} (static). Therefore, reliable operation can be obtained even though V_{CC} is more than one-half BV_{CBO} (static).

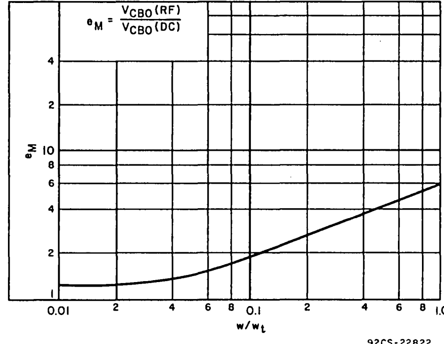


Fig. 3-9–Relationship of rf voltage breakdown to dc voltage breakdown as a function of frequency.

Reliability as a Function of Current Density and Junction Temperature

Questions are frequently asked concerning the life of rf power transistors that use an aluminum metallization system in connection with electromigration-related failure modes. Electromigration of the aluminum has been shown to occur in the presence of high current densities and elevated temperatures. This condition results from the mass transport of metal by momentum exchange between thermally activated metal ions and conducting electrons. As a consequence, the original uniform aluminum film is reconstructed to form thin conductor regions and extruded appearing hilocks.

The process can be accompanied by the solid-state dissolution of silicon in the aluminum. This latter effect usually occurs to a limited extent in transistor-manufacturing heat treatments until the aluminum-silicon saturation point is reached. As a result, only a very small additional amount of silicon dissolves during normal operation of the device. At high current densities and elevated temperatures, however, the electromigration process can act to transport the thermally diffused silicon ions away from the silicon-aluminum interface, and silicon diffusion into the aluminum is then allowed to continue until eventually failure of the transistor junctions occurs.

Test Conditions—The effects of electromigration on the lifetime of RCA rf power transistors in relation to various current densities and junction temperatures were evaluated in an accelerated-operating-life test program. DC current-voltage conditions were used because electromigration is responsive to the dc components of the total wave form used in rf applications, i.e., electromigration is effected by the unidirectional components of the field. Tests were conducted at three different emitter stripe current densities (J_E). The tests at each current density, in turn, were conducted at three different peak junction temperatures (T_j), all of which were accelerated above normal use conditions. Peak junction temperature was determined by infrared scanning of the transistor pellet at each life-test condition. Table 3-2 shows the matrix of test conditions. The sample size per test condition ranged from 10 to 15 units.

Test Vehicle—The RCA 2N6267 was used as the test vehicle because it is required to withstand one of the highest current of densities of any RCA rf power transistor (this transistor, therefore, represents a "worst-case" candidate). All the transistors used in the test were standard-product commercial devices, i.e., they were not subjected to conventional high-reliability screening prior to life testing.

Failure Mode—The accelerated test conditions produced failures that resulted from electromigration of aluminum and silicon. The failure indicator was degradation of the transistor junctions. RF power output measured at frequent life-test down periods prior to device junction failure exhibited only slight degradation (typically 8%); this degradation is extremely small in view of the severity of the test conditions.

Test Data—An Arrhenious plot (1/T-log scale) of the log-normal median time to failure (MTF) obtained from each test is shown in Fig. 3-10. The curves shown are extrapolated down from the data points in order to enable prediction of the MTF at operating junction temperatures below the maximum rated value of 200°C. An MTF of 9.5 x 10^5 hours (or greater than 100 years) is estimated for the 2N6267 test vehicle at its typical application current density of 8.5 x 10^4 A/cm^2 and junction temperature of 150°C.

Points from each curve in the Arrhenious plot were taken in the temperature range of 200°C to 100°C and replotted on a log-log scale, shown in Fig. 3-11, for extrapolation over various current densities. Fig. 3-11 represents general curves of MTF as a function of emitter current density and peak junction temperature. These curves can be used to estimate the MTF of an rf power transistor at its typical operating current density. Table 3-3 lists several RCA transistors designed to operate at microwave frequencies and shows the predicted MTF of these devices for typical application values of collector current, emitter stripe current density, and peak junction temperature. The microwave transistors are glass-passivated devices. It has been shown that the MTF of devices in which the glass passivation is not used is reduced by a factor of 10. Table 3-4 shows the MTF for non-glass-passivated rf devices predicted by use of this acceleration factor.

Table 3-2 Accelerated Life-Test Conditions

Collector Current (A)	Emitter Current (A)	Emitter Stripe Current Density (A/cm^2)	Peak Junction Temperature in Degrees Centigrade*		
			T_j1	T_j2	T_j3
1	1.02	8.5 x 10^4	300	280	154
2	2.07	1.7 x 10^5	283	258	230
3	3.22	2.7 x 10^5	300	273	240

* Represents peak temperature as averaged over several devices at each life-test condition. External heat-sink size is adjusted to achieve the differences in junction temperature on the life test.

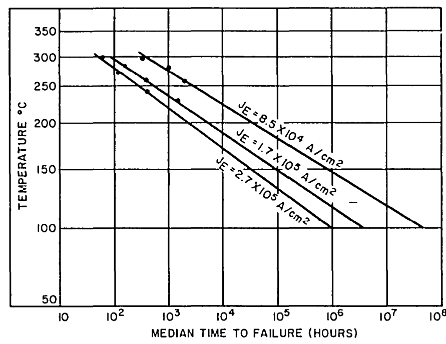


Fig. 3-10–Arrhenious plot showing extrapolation to lower temperatures from the life-test MTF points.

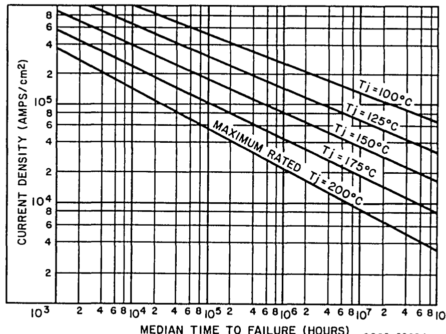


Fig. 3-11–MTF as a function of current density and junction temperature.

Table 3-3 — Estimated MTF for Glass-Passivated RF Power Transistors at Typical-Application Current Densities

Type	IE(Amps)	JE (104A/CM²)	MTF (10⁶ Hours) Tj=150°C
2N5470	0.119	5.2	4
2N5920	0.180	5.5	3.5
2N5921	0.450	3.5	12
2N6265	0.215	6.5	2
2N6266	0.540	4.2	7
2N6267	1.10	8.5	.95
2N6268	0.275	8.3	1
2N6269	0.920	7.2	1.5
RCA2001	0.120	3.8	10
RCA2003	0.300	9	.8
RCA2005	0.540	4.2	7
RCA2010	1.10	8.5	.95
RCA3001	0.120	3.8	10
RCA3003	0.300	9	.8
RCA3005	0.540	8	1.1
40915	0.0015	4.2	7
41039	0.030	1	300

Table 3-4 — Estimated MTF for Non-Glass-Passivated Devices at Typical-Application Current Densities.

Type	Typical IE (mA)	JE (10⁴ amps/cm²)	MTF Tj = 150°C (10⁶ hours)
2N1493	25	2.5	3.5
2N2631	375	2.7	2.5
2N2857	1.5	0.72	15.0
2N2876	500	3.5	1.3
2N3118	50	5.1	0.4
2N3375	350	2.4	2.8
2N3553	150	1.0	12.0
2N3632	600	2.1	6.0
2N3866	70	3.8	1.0
2N5016	900	4.5	.6
2N5071	1300	3.7	1.2
2N5090	85	4.6	.58
2N5109	50	2.7	2.5
2N5916	120	5.7	0.3
2N5918	480	5.7	0.3
2N5919A	800	4.0	0.8
2N5994	2400	7.2	0.15
2N6093	5100	4.8	.5
2N6105	1350	4.4	.7
41024	100	5.4	.35

RCA JAN, JANTX, and JANTXV RF Power Transistors

RCA can supply a number of rf power transistors that have been qualified as JAN, JANTX, and/or JANTXV types in accordance with MIL-S-19500. These transistors, together with the MIL-S-19500 detailed electrical (slash-sheet) specifications for them, are listed below:

Basic Device Type No.	Electrical Specification No.*
2N918	MIL-S-19500/301
2N1493	MIL-S-19500/247
2N2857	MIL-S-19500/343
2N3375, 2N3553, 2N4440	MIL-S-19500/341
2N3866	MIL-S-19500/398
2N5071	MIL-S-19500/442
2N5109	MIL-S-19500/453
2N5918	MIL-S-19500/473
2N5919A	MIL-S-19500/475

* MIL-S-19500 detailed electrical specifications for JAN, JANTX, and JANTXV devices can be obtained from the *Naval Publications and Forms Center,* 5801 Tabor Avenue, Philadelphia, Pa.

RCA HR-Series RF Power Transistors—Processing and Screening

RCA HR-series types are high-reliability rf and microwave power transistors intended for applications in aerospace, military, and industrial equipment. These transistors are supplied to three screening levels (/1, /2, /3) which meet the electrical mechanical, and environmental test, methods, and procedures established for power transistors in MIL-STD-750. Table 3-5 defines

these reliability levels in terms of system-application usage.

RCA can provide on request SEM (Scanning Electron Microscope) inspection photographs to NASA-Goddard Specification GSFC-S-311-P-12A for each wafer lot tested to level /1. Precap Visual Inspection is conducted in conformance with Method 2072 of MIL-STD-750.

Table 3-5— Reliability Levels for RCA High-Reliability RF and Microwave Transistor

RCA Level	Application	Description
/1	Satellite and Aerospace	For devices intended for applications in which maintenance and replacement are extremely difficult or impossible, and Reliability is imperative.
/2	Military and Industrial (For example in Airborne Electronics)	For devices intended for applications in which maintenance and replacement can be performed, but are difficult and expensive.
/3	Military and Industrial (For example in Ground Based Electronics)	For devices intended for applications in which replacement can readily be accomplished.

HR-series transistors are available in RCA HF-28 and HF-46 and JEDEC TO-60, TO-201AA, TO-215AA, TO-216AA TO-5, TO-39, and TO-72 packages. The product-flow diagram shown in Fig. 3-12 lists a summary of processing, screening, tests, and sampling procedures followed in the manufacture of these transistors.

Table 3-6 provides detailed information for the screening tests included in the product-flow diagram. Table 3-7 gives pre-burn-in and post-burn-in electrical tests and delta limits for critical test parameters.

When ordering HR-series types, the appropriate reliability level should be indicated by addition of the suffix /1, /2, or /3 to the type number. For example, the 2N6265 processed to level /3 requirements should be marked HR2N6265/3.

The parameters listed in Table 3-7 are tested before and after burn-in, and the data are recorded for all devices in the lot. The parameters measured shall not have changed during burn-in from the initial value by more than the specified delta (Δ) limit or beyond the end-point limits given in Table 3-7.

All devices that exceed these limits are removed from the inspection lot, and the quality removed are noted in the lot history. If the quantity removed after burn-in exceeds 10 per cent of the devices subjected to burn-in, the entire lot is rejected.

Table 3-6— Description of Total Lot Screening for HR-Series rf power transistors*

Test	Conditions	MIL-STD-750 or -202 Method	Cond.	Screening Levels• /1	/2	/3
Wafer Lot Identification	—	—	—	X	—	—
SEM Inspection	—	GSFC-S-311-P-12A▪		S	—	—
Precap Visual	—	2072	—	X	X	—
Seal and Lot Identification	—	—	—	X	X	X
Stabilization Bake	24 hrs min at 200°C	—	—	X	X	X
Temperature Cycling	10 cycles	1051/107C	—	X	X	X
Centrifuge	20,000G, Y_1 direction	2006	—	X	X	X
Fine Leak	—	112	CIII	X	X	X
Gross Leak	—	112	A or B	X	X	X
HTRB (High-Temperature Reverse Bias)	80% V_{CB}, 150°C min	—	—	X	X	X
Serialize	—	—	—	X	X	X
Pre-Burn-in Electrical	See detail Specification			X	X	X
Burn-In	See detail Specification			X	X	X
Post-Burn-in Electrical	See detail Specification			X	X	X
Final Group A	See detail Specification			X	X	X

* Data on specific HR-Series types given in following pages show test conditions and limits.
• × = 100% Testing; S = Sample of 5 (random selection from each wafer); — = not performed.
▪ This specification, which was written by NASA Goddard Space Flight Center, is the industry standard.

Table 3-7— Burn-In Test Measurements

Test	MIL-STD-750 Method	Conditions & Limits	Symbol	Δ Limits
Collector cutoff current	3041	Per Detailed Electrical Specification	—	100% of pre-burn-in value or 10% of Group -A Limit whichever is greater
Forward-current transfer ratio	3076		h_{FE}	± 20% of pre-burn-in value
Power output	—		P_{out}	

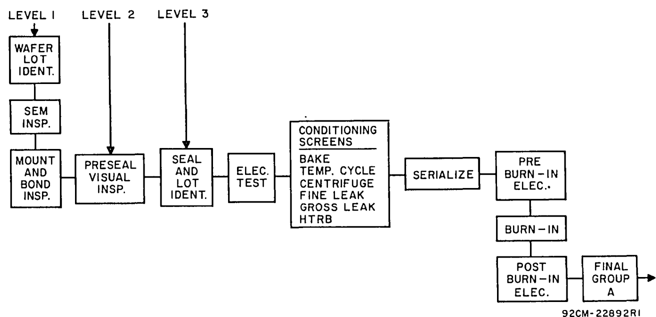


Fig. 3-12–Product Flow Diagram for RCA HR-Series rf power transistors (See Tables 3-6 and 3-7 for additional details)

RCA Premium- and Ultra-High-Reliability RF Power Transistors

RCA also supplies several transistors referred to as premium- or ultra-high-reliability types. Processing and screening requirements and ratings and electrical characteristics for these transistors are included in the technical data for these types at the end of this section.

Quality Assurance Program

In addition to the prescribed screening requirements, RCA maintains a general Quality Assurance Program for high-reliability rf transistors which includes the following functions:

1. A system for controlling the conversion of a customer specification into an internal RCA specification which assures complete compliance with customer requirements. Also, this system provides for control of documentation regarding changes in design, processes, materials, and electrical characteristics. All processes, work instructions, and quality inspections are clearly defined and documented.
2. Maintenance of test equipment and tools kept in strict compliance with MIL-C-45662, "Calibration System Requirements."
3. Quality Inspection in accordance with MIL-I-45208. Specifically, this program incorporates the following quality inspections:
   (a) A thorough inspection of incoming raw parts and materials.
   (b) Wafer-processing visual inspections and bond-pull tests to check metallization-to-wafer adherence.
   (c) Pellet visual inspection after wafer dicing (SEM inspection of pellets when required by purchase order).
   (d) Package-assembly visual inspection.
   (e) In-process bond-pull test to monitor pellet-to-package adherence.
   (f) In-process bond-pull test to monitor integrity of bond-wire contact.

(g) Precap visual inspection.
(h) Package cap-seal visual inspection.
(i) Hermeticity (fine and gross) leak-test audit performed after 100% testing.
(j) Group A electrical-test audit performed after 100% testing.
(k) Completed-unit external visual inspection
(l) Group B reliability test sampling from parent types in accordance with MIL-STD-750 test methods.

4. Quality-control sampling procedures in accordance with MIL-STD-105 and MIL-S-19500.
5. Thorough records kept on all inspections. All data kept on active file for a minimum of 3 years.

Technical Data

Significant electrical ratings and characteristics and special features of RCA JAN, JANTX, and JANTXV rf power transistors; HR-series rf power transistors; and premium- and ultra-high-reliability rf power transistors are given in the data charts on the following pages.

JAN2N918 — Silicon Epitaxial Planar VHF Transistor

JAN Electrical Specifications: MIL-S-19500/301A
Package: JEDEC TO-72

Maximum Ratings

P_T		V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_J	T_{stg}
$T_C = 25°C$ [1]	$T_A = 25°C$ [2]						
mW	mW	Vdc	Vdc	Vdc	mAdc	°C	°C
300	200	30	3	15	50	+200	-65 to +200

[1] Derate linearly 1.71 mW/°C for $T_C > 25°C$.
[2] Derate linearly 1.14 mW/°C for $T_A > 25°C$.

Primary Electrical Characteristics

Limits	h_{FE} $I_C = 3$ mAdc $V_{CE} = 1$ Vdc	h_{fe} $I_C = 4$ mAdc $V_{CE} = 10$ Vdc f = 100 MHz	$r_b' C_c$ $I_E = -4.0$ mAdc $V_{CB} = 10$ Vdc f = 79.8 MHz	C_{obo} $V_{CB} = 10$ Vdc $I_E = 0$ 100 kHz ⩽ f ⩽ 1 MHz	NF $V_{CE} = 6$ Vdc $I_C = 1$ mAdc f = 60 MHz $g_s = 2.5$ mmho	G_{PE} $V_{CB} = 12$ Vdc $I_C = 6.0$ mAdc f = 200 MHz
			psec	pF	dB	dB
Min	20	6.0	–	–	–	15
Max	200	–	25	1.7	6.0	–

For characteristic curves and test conditions, refer to data on basic type in File No. 83.

JAN2N1493 — Silicon N-P-N VHF Transistor

JAN Electrical Specification: MIL-S-19500/247
Package: JEDEC TO-39

Maximum Ratings

P_T [1]	V_{CBO}	V_{CEX}	V_{EBO}	$R_{\theta JC}$	T_J	T_{stg}
W	Vdc	Vdc	Vdc	°C/W	°C	°C
3.5	100	100	4.5	50	+200	-65 to +200

[1] This power-dissipation rating is for 1,000 hours expected life at $T_A = +25° \pm 3°C$.

Primary Electrical Characteristics

Limits	PG (at: f = 70 MHz $V_{CC} = 50$ Vdc $I_C = 25$ mAdc	h_{fe} f = 70 MHz $V_{CC} = 20$ Vdc $I_C = 15$ mAdc	h_{FE} $V_{CE} = 20$ Vdc $I_E = 10$ mAdc	C_{ob} f = 0.1 to 1.0 MHz $V_{CB} = 20$ Vdc $I_E = 0$	$r_b' C_c$ $V_{CC} = 20$ Vdc $I_C = 10$ mAdc
	dB	–	–	pF	psec
Min.	10	2.5	50	–	–
Max.	–	–	200	5.0	100

For characteristic curves and test conditions, refer to data on basic type in File No. 10.

JAN2N2857, JANTX2N2857

Silicon N-P-N Epitaxial Planar UHF Transistor

JAN Electrical Specifications: MIL-S-19500/343A
Service: For UHF
Package: JEDEC TO-72

Maximum Ratings

P_T[1] $T_A = 25°C$	P_T[2] $T_C = 25°C$	V_{CBO}	V_{CEO}	V_{EBO}	T_A	I_C
mW	mW	Vdc	Vdc	Vdc	°C	mAdc
200	300	30	15	3	-65 to +200	40

[1] Derate linearly 1.14 mW/°C for $T_A > 25°C$.
[2] Derate linearly 1.71 mW/°C for $T_C > 25°C$.

Primary Electrical Characteristics

	h_{FE}	$\|h_{fe}\|$	C_{cb}	NF	G_{PE}	$r_b' C_c$
Limits	V_{CE} = 1 Vdc, I_C = 3 mAdc	V_{CE} = 6 Vdc, I_C = 5 mAdc, f = 100 MHz	V_{CB} = 10 Vdc, I_E = 0, 100 kHz ≤ f ≤ 1 MHz	V_{CE} = 6 Vdc, I_C = 1.5 mAdc, f = 450 MHz, R_g = 50 ohms	V_{CE} = 6 Vdc, I_C = 1.5 mAdc, f = 450 MHz	V_{CB} = 6 Vdc, I_E = 2 mAdc, f = 31.9 MHz
			pF	dB	dB	psec
Min	30	10	–	–	12.5	4
Max	150	19	1.0	4.5	21	15

For characteristic curves and test conditions, refer to data on basic type in File No. 61.

JAN2N3375, JANTX2N3375, JANTXV2N3375 JAN2N3553, JANTX2N3553, JANTXV2N3553 JAN2N4440, JANTX2N4440, JANTXV2N4440

Silicon N-P-N Overlay VHF-UHF Transistors

JAN Electrical Specifications: MIL-S-19500/341
Package: JEDEC TO-39-2N3553
JEDEC TO-60-2N3375, 2N4440

Maximum Ratings

Type	P_T $T_A = 25°C$	P_T $T_C = 25°C$	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_{stg}	T_J
	W	W	Vdc	Vdc	Vdc	Adc	°C	°C
2N3375, 2N4440	2.6 [1]	11.6 [3]	65	40	4	1.5	-65 to +200	+200
2N3553	1.0 [2]	7.0 [4]	65	40	4	1.0	-65 to +200	+200

[1] Derating linearly at 14.86 mW/°C for $T_A > 25°C$.
[2] Derate linearly at 5.71 mW/°C for $T_A > 25°C$.
[3] Derate linearly at 0.066 W/°C for $T_C > 25°C$.
[4] Derate linearly at 0.04 W/°C for $T_C > 25°C$.

Primary Electrical Characteristics

Limits	$V_{CE}(sat)$ [1] $I_C = 500$ mAdc, $I_B = 100$ mAdc, 2N3375 2N4440	$V_{CE}(sat)$ [1] $I_C = 250$ mAdc, $I_B = 50$ mAdc, 2N3553	C_{obo} $I_E = 0$, $V_{CB} = 30$ Vdc, 100 kHz $\leq f \leq$ 1 MHz	$\lvert h_{fe} \rvert$ $V_{CE} = 28$ Vdc, $I_C = 125$ mAdc, f = 100 MHz	h_{FE} $V_{CE} = 5$ Vdc[1], $I_C = 150$ mAdc
	Vdc	Vdc	pF		
Min	–	–	–	3.5	15
Max	0.7	0.6	10	–	150

Limits	P_{OE} $P_{IE} = 1.0$ W, f = 100 MHz, 2N3375	P_{OE} $P_{IE} = 1.0$ W, f = 400 MHz, 2N3375	P_{OE} $P_{IE} = 0.25$ W, f = 175 MHz, 2N3553	P_{OE} $P_{IE} = 1.0$ W, f = 100 MHz, 2N4400	P_{OE} $P_{IE} = 1.0$ W, f = 400 MHz, 2N4400
	W	W	W	W	W
Min	7.5	3.0	2.5	10	4.0
Max	14	6.0	5.0	16	8.0

[1] Pulsed test

For characteristic curves and test conditions, refer to data on basic type in File No. 386.

JAN2N3866, JANTX2N3866

Silicon N-P-N Overlay VHF-UHF Transistors

JAN Electrical Specification: MIL-S-19500/398
Package: JEDEC TO-39

Maximum Ratings

P_T[1/] $T_A = 25°C$	V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_{stg}	T_J
W	Vdc	Vdc	Vdc	Adc	°C	°C
1.0	60	3.5	30	0.4	-65 to +200	+200

[1/]Derate linearly at 5.71 mW/°C for $T_A > 25°C$.

Primary Electrical Characteristics

Limits	h_{FE} $V_{CE} = 5.0$ Vdc $I_C = 50$ mAdc	$\|h_{fe}\|$ $V_{CE} = 15$ Vdc $I_C = 50$ mAdc f = 200 MHz	C_{obo} $V_{CB} = 28$ Vdc $I_E = 0$ 100 kHz ≤ f ≤ 1 MHz	$V_{CE}(sat)$ $I_C = 100$ mAdc $I_B = 10$ mAdc	P_{OE} $V_{CC} = 28$ Vdc $P_{IE} = 0.15$ W f = 400 MHz	P_{OE} $V_{CC} = 28$ Vdc $P_{IE} = 0.075$ W f = 400 MHz
			pF	Vdc	W	W
Min	15	2.5	–	–	1.0	0.5
Max	200	8.0	3.0	1.0	2.0	–

For characteristic curves and test conditions, refer to data on basic type in File No. 80.

JAN2N5071, JANTX2N5071

Silicon N-P-N Emitter-Ballasted Overlay VHF Transistor

JAN Electrical Specification: MIL-S-19500/442
Package: JEDEC TO-60

Maximum Ratings

P_T[1/] $T_A = 25°C$	P_T[2/] $T_C = 25°C$	V_{CEO}	V_{EBO}	V_{CEX}	I_C	$T_{Oper.}$ & $T_{stg.}$
W	W	Vdc	Vdc	Vdc	Adc	°C
2.6	70	35	4	65	10	-65 to +200

[1/] Derate linearly at 15 mW/°C for $T_A > 25°C$ [2/] Derate linearly at 400 mW/°C for $T_C > 25°C$

Primary Electrical Characteristics

Limits	h_{FE} $V_{CE} = 5$ Vdc $I_C = 3$ Adc	C_{obo} $V_{CB} = 30$ Vdc $I_E = 0$ 100kHz ≤ f ≤ 1MHz	P_{OE} $P_{IE} = 3$ W f = 76 MHz	VSWR f = 30 MHz $P_{OE} = 30$ W	$R_{\theta JC}$
		pF	W		°C/W
Min.	15		24		
Max.	100	85	34	3:1 All Phases	2.5

For characteristic curves and test conditions, refer to data on basic type in File No. 269.

JAN2N5109, JANTX2N5109

Silicon N-P-N Overlay VHF-UHF Transistors

JAN Electrical Specification: MIL-S-19500/453
Package: JEDEC TO-39

Maximum Ratings

P_T[1/] T_A = 25°C	V_{CBO}	V_{EBO}	V_{CEO}	V_{CER}	I_C	T_{stg}	T_J
W	Vdc	Vdc	Vdc	Vdc	Adc	°C	°C
1.0	40	3.0	20	40	0.4	-65 to +200	+200

[1/] Derate linearly 5.71 mW/°C for T_A > 25°C.

Primary Electrical Characteristics

Limits	h_{FE} V_{CE} = 15 Vdc I_C = 50 mAdc	$\|h_{fe}\|$ V_{CE} = 15 Vdc I_C = 50 mAdc f = 200 MHz	C_{obo} V_{CB} = 28 Vdc I_E = 0 100 kHz ≤ f ≤ 1 MHz	$V_{CE}(sat)$ I_C = 100 mAdc I_B = 10 mAdc	G_{Pe} V_{CE} = 15 Vdc P_{IE} = 10 dBM I_C = 10 mAdc f = 200 MHz
			pF	Vdc	dB
Min	40	6.0	–	–	11.0
Max	120	9.0	3.5	0.5	–

For characteristic curves and test conditions, refer to data on basic type in File No. 281.

JAN2N5918

Silicon N-P-N Emitter-Ballasted VHF-UHF Transistor

JAN Electrical Specification: MIL-S-19500/473
Package: JEDEC TO-216AA

Maximum Ratings

P_T[1/] T_A = 25°C	P_T[2/] T_C = 75°C	V_{CEO}	V_{EBO}	V_{CEX}	I_C	T_J
W	W	Vdc	Vdc	Vdc	Adc	°C
2.4	10	30	4	60	0.75	-65 to +200

[1/] Derate linearly 13.7 mW/°C for T_A > 25°C
[2/] Derate linearly 80 mW/°C for T_C > 75°C

Primary Electrical Characteristics

Limits	$V_{CE}(sat)$ I_C = 2 Adc I_B = 400 mAdc	h_{FE} V_{CE} = 4 Vdc I_C = 0.5 Adc	C_{obo} V_{CB} = 30 Vdc I_E = 0 100 kHz ≤ f ≤ 1 MHz	P_{OE} P_{IE} = 1.59 W f = 400 MHz
	Vdc		pF	W
Min	–	15	–	10
Max	–	200	13	13

For characteristic curves and test conditions, refer to data on basic type in File No. 448.

JAN2N5919A
JANTX2N5919A

Silicon N-P-N Emitter-Ballasted Overlay VHF/UHF Transistor

JAN Electrical Specifications: MIL-S-19500/475
Service: For UHF
Package: JEDEC TO-216AA

Maximum Ratings

P_T [1] $T_A = 25°C$	P_T [2] $T_C = 25°C$	V_{CEO}	V_{EBO}	V_{CEX}	I_C	T_A
W	W	Vdc	Vdc	Vdc	Adc	°C
2.6	25	30	4	65	4.5	-65 to +200

[1] Derate linearly 15 mW/°C for $T_A > 25°C$.

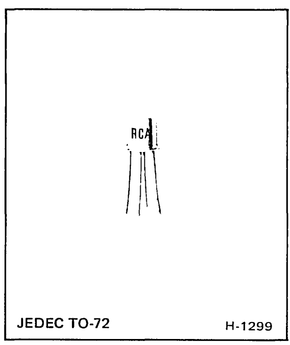
[2] Derate linearly 200 mW/°C for $T_C > 75°C$.

Primary Electrical Characteristics

Limits	$V_{CE}(sat)$ $I_C = 2$ Adc $I_B = 400$ mAdc	h_{FE} $V_{CE} = 4$ Vdc $I_C = 0.5$ Adc	C_{obo} $V_{CB} = 30$ Vdc $I_E = 0$ 100 khz $\leqslant f \leqslant$ 1 MHz	P_{out} $P_{in} = 4$ W f = 400 MHz
	Vdc		pF	W
Min	---	10	---	16
Max	2	200	22	22

For characteristic curves and test conditions, refer to data on basic type in File No. 505.

Solid State
Division



JEDEC TO-72 H-1299

Silicon N-P-N Epitaxial Planar Transistor

For UHF Applications in Industrial and Military Equipment

Features:

- **High gain-bandwidth product — f_T = 1000 MHz min.**
- **High converter (450-to-30-MHz) gain — G_c = 15 dB typ. for circuit bandwidth of approximately 2 MHz**
- **High power gain as neutralized amplifier — G_{pe} = 12.5 dB min. at 450 MHz for circuit bandwidth of 20 MHz**
- **High power output as uhf oscillator —**
  P_o = { 30 mW min., 40 mW typ. at 500 MHz; 20 mW typ., at 1 GHz }
- **Low device noise figure —**
  NF = { 4.5 dB max. as 450 MHz amplifier; 7.5 dB typ. as 450-to-30-MHz converter }
- **Low collector-to-base time constant — $r_b' C_c$ = 7 ps typ.**
- **Low collector-to-base feedback capacitance — C_{cb} = 0.6 pF typ.**

The RCA-HR2N2857 is a high-reliability version of the RCA-2N2857. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N2857 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N2857 transistor in RCA data bulletin file No. 61.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	30	V
COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	15	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	2.5	V
COLLECTOR CURRENT	I_C	40	mA
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 25° C		300	mW
At case temperatures above 25° C		Derate at 1.72	mW/°C
At ambient temperatures up to 25° C		200	mW
At ambient temperatures above 25° C		Derate at 1.14	mW/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. from seating surface for 10 s max.		265	°C

II. GROUP A TESTS, *at Ambient Temperature (T_A) = 25° C*

CHARACTERISTIC	Symbol	TEST CONDITIONS							LIMITS		Units
		Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Emitter-to-Base Voltage V_{EB}	DC Emitter Current I_E	DC Base Current I_B	DC Collector Current I_C			
		MHz	V	V	V	mA	mA	mA	Min.	Max.	
* Collector Cutoff Current	I_{CBO}		15			0			–	10	nA
Collector-to-Base Breakdown Voltage	BV_{CBO}					0		0.001	30	–	V
Collector-to-Emitter Breakdown Voltage	BV_{CEO}						0	3	15	–	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}					–0.01		0	2.5	–	V
* Static Forward Current Transfer Ratio	h_{FE}			1				3	30	150	
Small-Signal Forward Current Transfer Ratio	h_{fe}	0.001[c] 100[c]		6 6				2 5	50 10	220 19	
Collector-to-Base Feedback Capacitance	C_{cb}	0.1 to 1[b]	10			0			–	1.0	pF
Collector-to-Base Time Constant	$r_b' C_c$	31.9[c]	6			–2			4	15	ps
Small-Signal Common-Emitter Power Gain in Neutralized Amplifier Circuit	G_{pe}	450[c]		6				1.5	12.5	19	dB
Power Output as Oscillator	P_o	⩾500[a]	10			–12			30	–	mW
UHF Device Noise Figure	NF	450[c, d, f]		6				1.5	–	4.5	dB
UHF Measured Noise Figure	NF	450[c, d]		6				1.5	–	5.0	dB

[a] Fourth lead (case) not connected.

[b] Three-terminal measurement: Lead No. 1 (Emitter) and lead No. 4 (Case) connected to guard terminal.

[c] Fourth lead (case) grounded.

[d] Generator resistance R_g = 50 ohms.

[e] Generator resistance R_g = 400 ohms.

[f] Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test circuit (0.25 dB) and the contribution of the following stages in the test setup (0.25 dB).

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

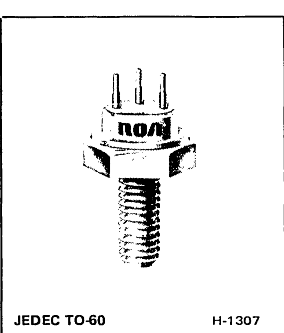
V_{CB} = 15 V

P_T = 0.2 W

Solid State Division

RF Power Transistors

HR2N3375



JEDEC TO-60 H-1307

Silicon N-P-N Overlay Transistor

For VHF/UHF Applications

Features:

- **7.5 W (MIN) output at 100 MHz Class C**
- **3.0 W (MIN) output at 400 MHz Class C**
- **2.5 W (Typ) output at 500 MHz, Oscillator**
- **High Voltage Ratings**
- **Hermetic stud-type package**
- **All electrodes isolated from stud**

The RCA-HR2N3375 is a high-reliability version of the RCA-2N3375. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N3375 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N3375 transistor in RCA data bulletin file No. 386.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter voltage V_{BE} = −1.5 V	V_{CEV}	65	V
With base open	V_{CEO}	40	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.5	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		11.6	W
At case temperatures above 25°C	Derate linearly at	0.066	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/16 in. (1.58 mm) from insulating wafer for 10 s max.		230	°C

II. GROUP A TESTS. At Case Temperature (T_C) = 25°C.

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
			DC Collector Volts		DC Base Volts	DC Current (Milliamperes)					
			V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector-Cutoff Current	I_{CEO}		30			0		–	.1	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$				0		0.1	65	–	V
	Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$					0	0 to 200[a]	40[b]	–	V
		$V_{(BR)CEV}$			−1.5			0 to 200[a]	65[b]	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0.1		0	4	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					100	500	–	1	V
*	DC Forward Current Transfer Ratio	h_{FE}		5				150	10	–	

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		DC Collector Volts		DC Base Volts	DC Current (Milliamperes)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-to-Base Capacitance Measured at 1 MHz	C_{obo}	30			0			–	10	pF
RF Power Output Amplifier, Unneutralized At 100 MHz	P_{OE}		28					7.5[c]	–	W
400 MHz			28					3.0[d]	–	

[a]Pulsed through an inductor (25 mH); duty factor = 50%.
[b]Measured at a current where the breakdown voltage is a minimum.
[c]For P_{IE} = 1.0 W; minimum efficiency 65%.
[d]For P_{IE} = 1.0 W minimum efficiency 40%.
*Recorded before and after burn-in for each device (serialized).

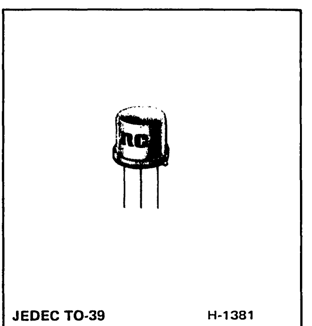
III. BURN-IN CONDITIONS

T_A = 25°C
V_{CB} = 30 V
P_T = 2.6 W

Solid State
Division

RF Power Transistors

HR2N3553



JEDEC TO-39 H-1381

Silicon N-P-N Overlay Transistor

For VHF/UHF Applications

Features:

- **2.5 W (MIN) output at 175 MHz, Class C Amplifier**
- **1.5 W (Typ) output at 500 MHz, Oscillator**
- **High Voltage Ratings**

The RCA-HR2N3553 is a high-reliability version of the RCA-2N3553. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N3553 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N3553 transistor in RCA data bulletin file No. 386.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter voltage V_{BE} = −1.5 V	V_{CEV}	65	V
With base open	V_{CEO}	40	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.33	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		7	W
At case temperatures above 25°C	Derate linearly at	0.04	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/16 in. (1.58 mm) from seating plane for 10 s max.		230	°C

II. GROUP A TESTS. At Case Temperature (T_C) = 25°C.

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		DC Collector Volts		DC Base Volts	DC Current (Milliamperes)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
* Collector-Cutoff Current	I_{CEO}		30			0		–	.1	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$				0		0.3	65	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$					0	0 to 200[a]	40[b]	–	V
	$V_{(BR)CEV}$			−1.5			0 to 200[a]	65[b]	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0.1		0	4	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					50	250	–	1	V
* DC Forward Current Transfer Ratio	h_{FE}		5				150	10	–	

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		DC Collector Volts		DC Base Volts	DC Current (Milliamperes)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-to-Base Capacitance Measured at 1 MHz	C_{obo}	30			0			–	10	pF
RF Power Output Amplifier, Unneutralized At 175 MHz	P_{OE}		28					2.5[c]		W

[a]Pulsed through an inductor (25 mH); duty factor = 50%.
[b]Measured at a current where the breakdown voltage is a minimum.
[c]For P_{IE} = 2.5 W; minimum efficiency = 50%.
*Recorded before and after burn-in for each device (serialized).

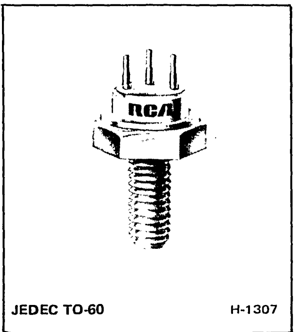
III. BURN-IN CONDITIONS

T_A = 25°C
V_{CE} = 30 V
P_T = 1 W

Solid State
Division

RF Power Transistors

HR2N3632



JEDEC TO-60 H-1307

Silicon N-P-N Overlay Transistor

For VHF Applications

Features:

- **13.5 W (MIN) output at 175 MHz Class C**
- **10.0 W (Typ) output at 260 MHz Class C**
- **High Voltage Ratings**
- **Hermetic stud-type package**
- **All electrodes isolated from stud**

The RCA-HR2N3632 is a high-reliability version of the RCA-2N3632. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N3632 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N3632 transistor in RCA data bulletin file No. 386.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter voltage V_{BE} = −1.5 V	V_{CEV}	65	V
With base open	V_{CEO}	40	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	1.0	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		23	W
At case temperatures above 25°C	Derate linearly at	0.13	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During soldering):			
At distances ⩾ 1/16 in (1.58 mm) from insulating wafer for 10 s max.		230	°C

II. GROUP A TESTS. At Case Temperature (T_C) = 25°C.

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
			DC Collector Volts		DC Base Volts	DC Current (Milliamperes)					
			V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector-Cutoff Current	I_{CEO}		30			0		–	0.25	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$				0		0.5	65	–	V
	Collector-to-Emitter	$V_{(BR)CEO}$					0	0 to 200[a]	40[b]	–	V
	Breakdown Voltage	$V_{(BR)CEV}$			−1.5			0 to 200[a]	65[b]	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				.25		0	4	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					100	500	–	1	V
*	DC Forward Current Transfer Ratio	h_{FE}		5				300	10	–	

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		DC Collector Volts		DC Base Volts	DC Current (Milliamperes)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-to-Base Capacitance Measured at 1 MHz	C_{obo}	30			0			–	20	pF
RF Power Output Amplifier, Unneutralized At 175 MHz	P_{OE}		28					13.5[c]		W
260 MHz			28					10[d]		

[a]Pulsed through an inductor (25 mH); duty factor = 50%.
[b]Measured at a current where the breakdown voltage is a minimum.
[c]For P_{IE} = 3.5 W; minimum efficiency = 70%.
[d]For P_{IE} = 3.0 W; typical efficiency = 60%.
*Recorded before and after burn-in for each device (serialized).

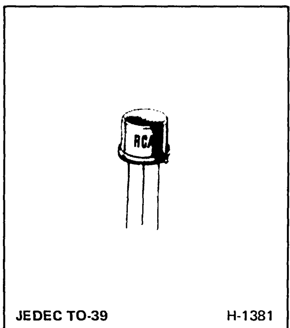
III. BURN-IN CONDITIONS

T_A = 25°C
V_{CB} = 30 V
P_T = 2.6 W

Solid State
Division

RF Power Transistors

HR2N3866


JEDEC TO-39 H-1381

Silicon N-P-N Overlay Transistor

High-Gain Driver for VHF/UHF Applications
in Military and Industrial Communications Equipment

Features:

- **High power gain, unneutralized Class C amplifier**
  - **1-W output at 400 MHz (10-dB gain)**
  - **1-W output at 250 MHz (15-dB gain)**
  - **1-W output at 175 MHz (17-dB gain)**
  - **1-W output at 100 MHz (20-dB gain)**
- **Low output capacitance**
  C_{obo} = 3 pF max.

The RCA-HR2N3866 is a high-reliability version of the RCA-2N3866. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N3866 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N3866 transistor in RCA data bulletin file No. 80.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	55	V
With base open	V_{CEO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.4	A
CONTINUOUS BASE CURRENT	I_B	0.4	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 25° C		5	W
At case temperatures above 25° C		Derate at 0.0286	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE:			
At distances ≥ 1/16 in. (1.58 mm) from seating plane for 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature $(T_C) = 25^{o}$ C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC VOLTAGE (V)		TEST CONDITIONS: DC CURRENT (mA)			LIMITS		UNITS
		V_{CE}	V_{EB}	I_E	I_B	I_C	MIN.	MAX.	
Collector Cutoff Current: Base-emitter junction reverse biased	I_{CEX}	55	1.5				–	0.1	mA
* Base open	I_{CEO}	28			0		–	20	μA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	55	–	V
Collector-to-Emitter Breakdown Voltage: With base open	$V_{(BR)CEO}$				0	5	30	–	V
With base connected to emitter through 10-ohm resistor	$V_{(BR)CER}$		0			5	55	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
Emitter-Cutoff Current	I_{EBO}		3.5				–	0.1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				20	100	–	1.0	V
* DC Forward-Current Transfer Ratio	h_{FE}	5				50	10	200	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						–	35	^{o}C/W

DYNAMIC

TEST AND CONDITIONS	SYMBOL	FREQUENCY MHz	LIMITS		UNITS
			MIN.	MAX.	
Power Output (V_{CC} = 28 V): P_{IE} = 0.1 W	P_{OE}	400	1.0	–	W
Large-Signal Common-Emitter Power Gain (V_{CC} = 28 V): P_{IE} = 0.1 W	G_{PE}	400	10	–	dB
Collector Efficiency (V_{CC} = 28 V): P_{IE} = 0.1 W, P_{OE} = 1 W, Source Impedance = 50 Ω	η_C	400	45	–	%
Magnitude of Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio: I_C = 50 mA, V_{CE} = 15 V	$\lvert h_{fe} \rvert$	200	2.5	–	
Available Amplifier Signal Input Power, P_{OE} = 1 W, Source Impedance = 50 Ω	P_i	400	–	0.1	W
Common-Base Output Capacitance (V_{CB} = 28 V)	C_{obo}	1	–	3	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

$T_A = 25^{o}$ C

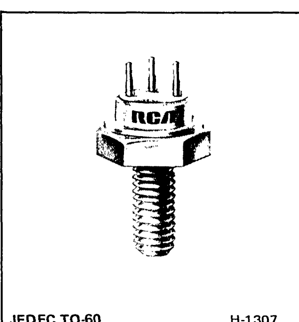
V_{CB} = 28 V

P_T = 1 W

Solid State
Division

RF Power Transistors

HR2N5071



JEDEC TO-60 H-1307

24-W (CW), 76-MHz Emitter-Ballasted Overlay Transistor

Silicon N-P-N Device for 24-Volt Applications in VHF Communications Equipment

Features:

- **For class B or class C amplifiers**
- **For 24-V FM (30 to 76 MHz) communications**
- **24 W output at 76 MHz with 9 dB gain (Min.)**
- **Low thermal resistances**

The RCA-HR2N5071 is a high-reliability version of the RCA-2N5071. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5071 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5071 transistor in RCA data bulletin file No. 269.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
COLLECTOR CURRENT:			
Continuous	I_C	3.3	A
Peak		10	A
CONTINUOUS BASE CURRENT	I_B	1	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		70	W
At case temperatures above 25°C	Derates linearly at	0.4	W/°C
TEMPERATURE RANGE:			
Storage and operating (junction)		−65 to 200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. (0.8 mm) from insulating wafer for 10 s max.		230	°C

II. GROUP A TESTS. At Case Temperature (T_C) = 25°C.

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		DC Collector Voltage-V		DC Base Voltage-V	DC Current mA					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	MIN.	MAX.	
Collector-Cutoff Current:										
* With base open	I_{CEO}		30			0		–	5	mA
With emitter open	I_{CBO}	60						–	10	
Collector to Emitter Sustaining Voltage:										V
With base open	$V_{CEO}(sus)$					0	200[a]	30	–	
With external base-to-emitter resistance (R_{BE}) = 5 Ω	$V_{CER}(sus)$						200[a]	40	–	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$					10	0	4	–	V
* DC Forward Current Transfer Ratio	h_{FE}		5				1 A	20	–	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$							–	2.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS		UNITS
		DC Collector Supply (V_{CC})–V	Input Power (P_{IE})–W	Frequency (f) - MHz	MIN.	MAX.	
Power Output	P_{OE}	24	3	76	24	–	W
Power Gain	G_{PE}	24	3	76	9	–	dB
Available Amplifier Signal Input Power	P_i	Source impedance (Zg) = 50	P_{OE} = 24 W	76	–	3	W
Collector Efficiency	η_C	24	3	76	60	–	%
Load Mismatch	LM	24	1.2	30	GO/NO GO VSWR = 3:1		
Collector-to-Base Capacitance	C_{obo}	V_{CB} = 30 V	–	1	–	85	pF

[a]Pulsed through a 25-mH inductor; duty factor = 50%; repetition rate > 60 Hz.
*Recorded before and after burn-in for each device (serialized).

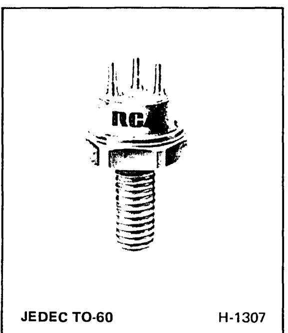
III. BURN-IN CONDITIONS

T_A = 25°C
V_{CB} = 28 V
P_T = 2.6 W

Solid State
Division

RF Power Transistors

HR2N5090



JEDEC TO-60 H-1307

High-Power Silicon N-P-N Overlay Transistor

High-Gain Type for Class A, B, or C Operation in VHF/UHF Circuits

Features:

- **Maximum-safe-area-of-operation curve**
- **1.2-W (min.) output at 400 MHz (7.8-dB gain)**
- **1.6-W (typ.) output at 175 MHz (12-dB gain)**
- **Hermetic stud-type package**
- **All electrodes isolated from stud**

The RCA-HR2N5090 is a high-reliability version of the RCA-2N5090. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5090 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5090 transistor in RCA data bulletin file No. 270.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

Rating	Symbol	Value	Unit
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	55	V
With base open	V_{CEO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.4	A
CONTINUOUS BASE CURRENT	I_B	0.4	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 100° C		4	W
At case temperatures above 100° C		Derate linearly at 0.04	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During Soldering):			
At distances ≥ 1/16 in. (1.58 mm) from insulating wafer for 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR VOLTAGE V	DC BASE VOLTAGE V	DC CURRENT mA			LIMITS		UNITS
		V_{CE}	V_{BE}	I_E	I_B	I_C	MIN.	MAX.	
* Collector Cutoff Current: With base open	I_{CEO}	28			0		–	0.02	mA
With base-emitter junction reverse-biased	I_{CEV}	55	–1.5				–	0.1	mA
Emitter Cutoff Current	I_{EBO}		3.5			0	–	0.1	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	55	–	V
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$				0	5	30	–	V
With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$					5	55[a]	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				20	100	–	1.0	V
* DC Forward-Current Transfer Ratio	h_{FE}	5				50	10	200	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						–	25	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR VOLTAGE V	OUTPUT POWER (P_{OE}) W	INPUT POWER (P_{IE}) W	COLLECTOR CURRENT (I_C) mA	FREQUENCY (f) MHz	LIMITS: MIN.	MAX.	UNITS
Power Output (Class C amplifier, unneutralized)	P_{OE}	V_{CC} = 28		0.2		400	1.2	–	W
Gain-Bandwidth Product	f_T	V_{CE} = 15			50		500	–	MHz
Magnitude of Common Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio	$\|h_{fe}\|$	V_{CE} = 15			50		2.5	–	
Available Amplifier Signal Input Power	P_i		1.2			400	–	0.2	W
Collector Efficiency	η_C		1.2				45	–	%
Collector-to-Base Capacitance	C_{obo}	V_{CB} = 30				1	–	3.5	pF

[a] Pulse through a 25-mH inductor; duty factor = 0.05.

* Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

V_{CB} = 28 V

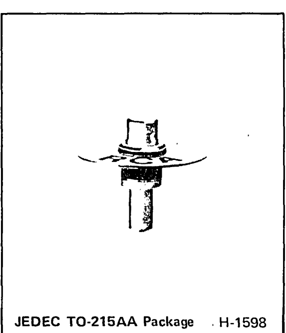
P_T = 1.75 W

Solid State
Division

RF Power Transistors

HR2N5470

Silicon N-P-N Overlay Transistor



JEDEC TO-215AA Package H-1598

For UHF/Microwave Power Amplifiers,
Microwave Fundamental-Frequency Oscillators,
and Frequency Multipliers

Features:

- **1-W output with 5-dB gain (min.) at 2 GHz**
- **2-W output with 10-dB gain (typ) at 1 GHz**
- **Ceramic-metal hermetic package with low inductance and low parasitic capacitances**

The RCA-HR2N5470 is a high-reliability version of the RCA-2N5470. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5470 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5470 transistor in RCA data bulletin file No. 350.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	55	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
PEAK COLLECTOR CURRENT		0.4	A
CONTINUOUS COLLECTOR CURRENT	I_C	0.2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25° C		3.5	W
At case temperatures above 25° C		Derate at 0.02	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC Collector Voltage (V)		DC Current (mA)			LIMITS		UNITS
		V_{CB}	V_{CE}	I_E	I_B	I_C	Min.	Max.	
* Collector Cutoff Current	I_{CES}		50				–	1	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	55	–	V
Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$					5	55	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				10	100	–	1.0	V
Collector-to-Base Capacitance (Measured at 1 MHz)	C_{cb}	30		0			–	3.0	pF
RF Power Output (Common-Base Amplifier): At 2 GHz[a]	P_{OB}	28					1.0	–	W
* Forward Current Transfer Ratio	h_{FE}		5			50	30	150	

[a] For P_{IB} = 0.316 W; minimum efficiency = 30%.

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

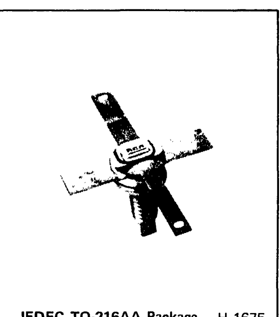
V_{CB} = 15 V

P_T = 1 W

Solid State
Division

RF Power Transistors

HR2N5916



JEDEC TO-216AA Package H-1675

High-Gain Silicon N-P-N Overlay Transistor

For VHF/UHF Communications Equipment

Features:

- **Radial leads for microstripline circuits**
- **2-W (min.) output at 400 MHz (10-dB gain)**
- **2-W (typ.) output at 1 GHz (5-dB gain)**
- **Low-inductance, ceramic-metal hermetic package**
- **All electrodes isolated from stud**

The RCA-HR2N5916 is a high-reliability version of the RCA-2N5916. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5916 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5916 transistor in RCA data bulletin file No. 425.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	24	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 100° C		4	W
At case temperatures above 100° C		Derate linearly at 0.04	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		DC Collector Voltage	DC Base Voltage	DC Current mA					
		V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
* Collector-to-Emitter Cutoff Current: Base-emitter junction shorted	I_{CES}	30	0				–	1	mA
Collector-to-Emitter Breakdown Voltage:	$V_{(BR)CES}$		0			5[a]	55	–	V
With base open	$V_{(BR)CEO}$					5[a]	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				10	100	–	0.5	V
* Forward Current Transfer Ratio	h_{FE}	5				50	30	150	
Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$						–	25	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
		DC Collector Supply (V_{CC}) – V	Output Power (P_{OE}) – W	Input Power (P_{IE}) – W	Frequency (f) – MHz	Min.	Max.	
Power Output	P_{OE}	28		0.2	400	2.0	–	W
Power Gain	G_{PE}	28	2		400	10	–	dB
Collector Efficiency	η_C	28		0.2	400	50	–	%
Collector-Base Capacitance	C_{cb}	30 (V_{CB})			1	–	4.5	pF

a Pulsed through a 25-mH inductor; duty factor = 50%

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

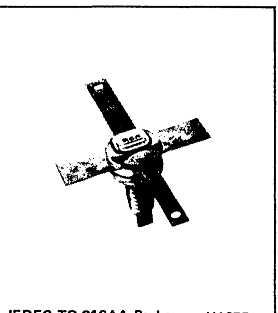
V_{CB} = 16 V

P_T = 1.3 W

Solid State
Division

RF Power Transistors

HR2N5918



JEDEC TO-216AA Package H1675

10-W, 400-MHz High-Gain Silicon N-P-N Emitter-Ballasted Overlay Transistor

For VHF/UHF Communications Equipment

Features:

- **10-W output at 400 MHz (8-dB min. gain)**
- **Emitter-ballasting resistors**
- **Broadband performance (225–400 MHz)**
- **Low-inductance ceramic-metal hermetic package**
- **All electrodes isolated from stud**
- **Radial leads for stripline circuits**

The RCA-HR2N5918 is a high-reliability version of the RCA-2N5918. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5918 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5918 transistor in RCA data bulletin file No. 448.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	30	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.75	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 75° C		10	W
At case temperatures above 75° C		Derate linearly at 0.08	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector Voltage	DC Base Voltage	DC Current mA					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector-to-Emitter Cutoff Current: Base-emitter junction shorted	I_{CES}	30	0				–	5	mA
	Collector-to-Emitter Breakdown Voltage:	$V_{(BR)CES}$		0			100[a]	60	–	V
	With base open	$V_{(BR)CEO}$					100[a]	30	–	
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			1		0	4	–	V
*	Forward Current Transfer Ratio	h_{FE}	4				500	10	200	
	Thermal Resistance, (Junction to Case)	$R_{\theta JC}$						–	12.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
		DC Collector Supply (V_{CC}) – V	Output Power (P_{OE}) – W	Input Power (P_{IE}) – W	Frequency (f) – MHz	Min.	Max.	
Power Output	P_{OE}	28		1.59	400	10	–	W
Power Gain	G_{PE}	28	10		400	8	–	dB
Collector Efficiency	η_C	28	10		400	60	–	%
Collector-to-Base Output Capacitance	C_{obo}	30 (V_{CB})			1	–	13	pF

[a]Pulsed through a 25-mH inductor; duty factor = 50%.

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

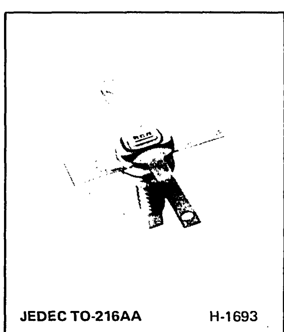
V_{CB} = 28 V

P_T = 2.4 W

Solid State
Division

RF Power Transistors

HR2N5919A



JEDEC TO-216AA H-1693

16-W, 400-MHz, Silicon N-P-N Emitter-Ballasted Overlay Transistor

Overdrive Capability of 20 W Output

Features:

- **6-dB gain (min.) at 400 MHz with 16-W (min.) output**
- **Integral emitter-ballasting resistors**
- **Broadband performance (225—400 MHz)**
- **Low-inductance ceramic-metal hermetic package**
- **Radial leads for microstripline circuits**
- **All electrodes isolated from the stud**

The RCA-HR2N5919A is a high-reliability version of the RCA-2N5919A. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5919A are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5919A transistor in RCA data bulletin file No. 505.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	30	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	4.5	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 75° C		25	W
At case temperatures above 75° C		Derate at 0.2	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		DC Collector Voltage-V	DC Base Voltage-V	DC Current mA					
		V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
* Collector-to-Emitter Cutoff Current: With base connected to emitter	I_{CES}	30	0				–	10	mA
Collector-to-Emitter Breakdown Voltage: With base connected to emitter	$V_{(BR)CES}$		0			200[a]	65	–	V
With base open	$V_{(BR)CEO}$				0	200[a]	30	–	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			5		0	4	–	V
* Forward Current Transfer Ratio	h_{FE}	4				500	10	200	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						–	5.0	°C/W

[a]Pulsed through a 25-mH inductor; duty factor = 50%

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
		DC Collector Supply (V_{CC})-V	Input Power (P_{IE})-W	Output Power (P_{OE})-W	Frequency (f) MHz	Min.	Max.	
Output Power	P_{OE}	28	4.0		400	16	–	W
Overdrive Objective Test	P_{OE}	28	7.0		400	20	–	W
Power Gain	G_{PE}	28		16	400	6	–	dB
Collector Efficiency	η_C	28	4.0		400	65	–	%
Collector-to-Base Output Capacitance	C_{obo}	30 (V_{CB})			1	–	22	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

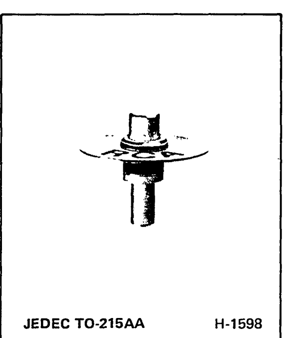
V_{CB} = 28 V

P_T = 2.6 W

Solid State
Division

RF Power Transistors

HR2N5920


JEDEC TO-215AA H-1598

2-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **2-W output with 10-dB gain (min.) at 2 GHz**
- **3-W output with 12-dB gain (typ.) at 1 GHz**
- **Ceramic-metal hermetic package with low inductance and low parasitic capacitances**
- **Stable common-base operation**
- **For coaxial, microstripline, and lumped-constant circuit applications**
- **Integral emitter-ballasting resistors**

The RCA-HR2N5920 is a high-reliability version of the RCA-2N5920. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5920 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5920 transistor in RCA data bulletin file No. 440.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω, sustaining	$V_{CER}(sus)$	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
DC COLLECTOR CURRENT (Continuous)	I_C	0.25	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75° C		3.5	W
At case temperatures above 75° C, derate linearly		0.028	W/° C
For point of measurement of temperature (on collector terminal), see dimensional outline.			
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector or Base Voltage (V)		DC Current (mA)					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector Cutoff Current	I_{CES}	45	0				–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		1	50	–	V
	Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					5	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				10	100	–	1	V
*	Forward Current Transfer Ratio	h_{FE}	5				100	20	200	
	Thermal Resistance (Junction-to-collector terminal)	$R_{\theta JCT}$						–	30	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	POWER INPUT P_{IB}(W)	POWER OUTPUT P_{OB}(W)	SUPPLY VOLTAGE V_{CC}(V)	FREQUENCY (f) GHz	LIMITS		UNITS
						Min.	Max.	
Power Output	P_{OB}	0.2		28	2	2	–	W
Power Gain	G_{PB}	0.2	2.0	28	2	10	–	dB
Collector Efficiency	η_C	0.2	2.0	28	2	40	–	%
Collector-to-Base Capacitance	C_{obo}			30 (V_{CB})	1 MHz		3	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

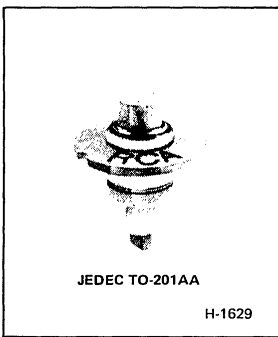
V_{CB} = 15 V

P_T = 2 W

Solid State
Division

RF Power Transistors

HR2N5921



JEDEC TO-201AA

H-1629

5-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **5-W output with 5.5-dB gain (typ.) at 2.3 GHz**
- **5-W output with 7-dB gain (min.) at 2 GHz**
- **10-W output with 11-dB gain (typ.) at 1.2 GHz**
- **Integral emitter-ballasting resistors**
- **Ceramic-metal hermetic package with low inductance and low parasitic capacitances**

The RCA-HR2N5921 is a high-reliability version of the RCA-2N5921. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5921 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5921 transistor in RCA data bulletin file No. 427.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
DC COLLECTOR CURRENT (Continuous)	I_C	0.7	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25° C		14.5	W
At case temperatures above 25° C, derate linearly		0.083	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		DC Collector or Base Voltage (V)		DC Current (mA)					
		V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
* Collector Cutoff Current	I_{CES}	45	0				–	2	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	50	–	V
Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					10	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				20	100	–	1	V
* Forward Current Transfer Ratio	h_{FE}	5				500	20	200	
Thermal Resistance (Junction-to-Flange)	$R_{\theta JF}$						–	12	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
		Frequency (f) – GHz	DC Collector Supply Voltage (V_{CC}) – V	Min.	Max.	
Output Power P_{IB} = 1 W	P_{OB}	2	28	5	–	W
Power Gain P_{OB} = 5 W	G_{PB}	2	28	7	–	dB
Collector Efficiency P_{OB} = 5 W	η_C	2	28	40	–	%
Collector-to-Base Capacitance V_{CB} = 30 V	C_{obo}	1 MHz	–	–	8.5	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_C = 125° C

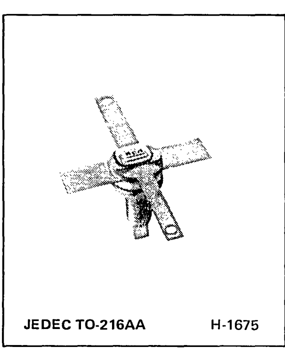
V_{CB} = 8 V

P_T = 3.2 W

Solid State
Division

RF Power Transistors

HR2N6105



JEDEC TO-216AA H-1675

30-W, 400-MHz Broadband Emitter-Ballasted Silicon N-P-N Overlay Transistor

Features:

- **5-dB gain (min.) at 400 MHz with 30 watts (min.) output**
- **Emitter-ballasting resistors**
- **Broadband performance (225—400 MHz)**
- **Low-inductance ceramic-metal hermetic package**
- **Radial leads for microstripline circuits**
- **All electrodes isolated from the stud**

The RCA-HR2N6105 is a high-reliability version of the RCA-2N6105. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6105 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N6105 transistor in RCA data bulletin file No. 504.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	30	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	4.5	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 75° C		36	W
At case temperatures above 75° C		Derate linearly at 0.288	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS DC Voltage V		DC Current mA		LIMITS		UNITS
		V_{CE}	V_{BE}	I_E	I_C	Min.	Max.	
* Collector-to-Emitter Cutoff Current: Base connected to emitter	I_{CES}	30	0			–	10	mA
Collector-to-Emitter Breakdown Voltage: With base connected to emitter	$V_{(BR)CES}$		0		200[a]	65	–	V
With base open	$V_{(BR)CEO}$				200[a]	30	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			5	0	4	—	V
* Forward Current Transfer Ratio	h_{FE}	4			500	10	200	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						3.5	°C/W

[a]Pulsed through a 25-mH inductor; duty factor = 50%.

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS DC Collector Supply (V_{CC}) – V	Input Power (P_{IE}) – W	Output Power (P_{OE}) – W	Frequency (F) – MHz	LIMITS Min.	Max.	UNITS
Output Power	P_{OE}	28	9.5		400	30	–	W
Overdrive Test	P_{OEO}	28	12.0		400	34	–	W
Power Gain	G_{PE}	28		30	400	5	–	dB
Collector Efficiency	η_C	28	9.5		400	65	–	%
Collector-to-Base Output Capacitance	C_{obo}	30 (V_{CB})			1	–	35	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

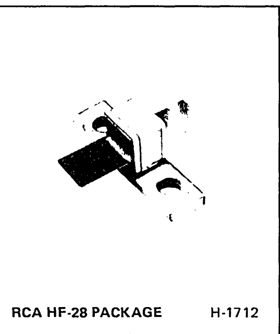
V_{CB} = 28 V

P_T = 2.6 W

Solid State
Division

RF Power Transistors

HR2N6265



RCA HF-28 PACKAGE H-1712

2-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **VSWR capability of ∞: 1 at 2 GHz**
- **2-W output with 8.2-dB gain (min.) at 2 GHz**
- **3-W output with 12-dB gain (typ.) at 1 GHz**
- **Ceramic-metal hermetic stripline package with low inductance and low parasitic capacitances**
- **For microstripline and lumped-constant circuit applications**

The RCA-HR2N6265 is a high-reliability version of the RCA-2N6265. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6265 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N6265 transistor in RCA data bulletin file No. 543.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.275	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75° C		6.25	W
At case temperature above 75° C		Derate linearly at 0.05	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC Collector or Base Voltage (V)		TEST CONDITIONS: DC Current (mA)			LIMITS		UNITS
		V_{CE}	B_{BE}	I_E	I_B	I_C	Min.	Max.	
* Collector Cutoff Current	I_{CES}	45	0				–	2	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
Collector-to-Emitter Breakdown Voltage: External base-to-emitter resistance R_{BE} = 10 Ω	$V_{(BR)CER}$					10	50	–	V
* Forward Current Transfer Ratio	h_{FE}	5				100	10	200	
Thermal Resistance (Junction-to-Flange)	$R_{\theta JF}$						–	20	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	POWER INPUT P_{IB}(W)	POWER OUTPUT P_{OB}(W)	SUPPLY VOLTAGE V_C(V)	FREQUENCY (f) GHz	LIMITS Min.	LIMITS Max.	UNITS
Power Output	P_{OB}	0.3		28	2	2	–	W
Power Gain	G_{PB}	0.3	2.0	28	2	8.2	–	dB
Collector Efficiency	η_C	0.3	2.0	28	2	33	–	%
Collector-to-Base Capacitance	C_{obo}			30 (V_{CB})	1 MHz	–	5	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

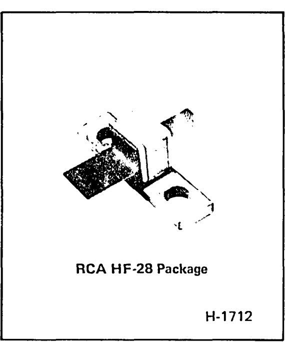
V_{CB} = 15 V

P_T = 2 W

Solid State
Division

RF Power Transistors

HR2N6266



RCA HF-28 Package

H-1712

5-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators,and Frequency Multipliers

Features:

- **Emitter-ballasting resistors**
- **VSWR capability of ∞: 1 at 2 GHz**
- **5-W output with 7-dB gain (min.) at 2 GHz**
- **13.5-W output with 11-dB gain (typ.) at 1 GHz**
- **Ceramic-metal hermetic stripline package with low inductance and low parasitic capacitances**
- **Stable common-base operation**
- **For microstripline, stripline, and lumped-constant circuit applications**

The RCA-HR2N6266 is a high-reliability version of the RCA-2N6266. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6266 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N6266 transistor in RCA data bulletin file No. 544.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	1	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75° C		14.8	W
At case temperature above 75° C		Derate linearly at 0.118	W/°C
TEMPERATURE RANGE:			
Storage and operaging (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector or Base Voltage (V)		DC Current (mA)					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector Cutoff Current	I_{CES}	45	0				–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	50	–	V
	Emitter-to-Base Breakdown Voltage	$B_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Breakdown Voltage With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					10	50	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				20	100	–	1	V
*	Forward Current Transfer Ratio	h_{FE}	5				100	15	200	
	Thermal Resistance (Junction-to-Flange)	$R\theta_{JF}$						–	8.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
		Frequency (f) – GHz	DC Collector Supply Voltage (V_{CC}) – V	Min.	Max.	
Output Power, P_{IB} = 1 W	P_{OB}	2	28	5	–	W
Power Gain, P_{OB} = 5 W	G_{PB}	2	28	7	–	dB
Collector Efficiency, P_{OB} = 5 W	η_C	2	28	33	–	%
Collector-to-Base Capacitance V_{CB} = 30 V	C_{obo}	1 MHz		–	10	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_C = 135° C

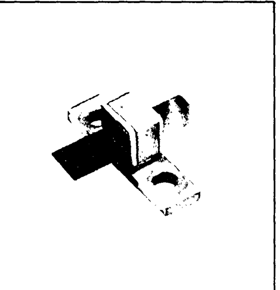
V_{CB} = 8 V

P_T = 3.2 W

RCA Solid State Division

RF Power Transistors

HR2N6267



RCA HF-28 PACKAGE H-1712

10-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **Emitter-ballasting resistors**
- **10-W output with 7-dB gain (min.) at 2 GHz (28 V)**
- **8-W output with 6-dB gain (typ.) at 2.3 GHz (28 V)**
- **VSWR capability of 10:1 at 2 GHz**
- **Ceramic metal hermetic stripline package with low inductance and low parasitic capacitances**
- **Stable common-base operation**
- **For microstripline, stripline, and lumped-constant circuit applications**

The RCA-HR2N6267 is a high-reliability version of the RCA-2N6267. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6267 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N6267 transistor in RCA bulletin file No. 545.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	1.5	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75° C		21	W
At case temperature above 75° C		Derate linearly at 0.168	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC Collector or Base Voltage (V)		TEST CONDITIONS: DC Current (mA)			LIMITS		UNITS
		V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
* Collector Cutoff Current	I_{CES}	45	0				–	2	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					10	50	–	V
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)				20	100	–	1	V
* Forward Current Transfer Ratio	h_{FE}	5				100	15	200	
Thermal Resistance (Junction-to-Flange)	$R_{\theta JF}$						–	6	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: Frequency (f) – GHz	TEST CONDITIONS: DC Collector Supply Voltage (V_{CC}) – V	LIMITS Min.	LIMITS Max.	UNITS
Output Power, P_{IB} = 2 W	P_{OB}	2	28	10	–	W
Power Gain, P_{OB} = 10 W	G_{PB}	2	28	7	–	dB
Collector Efficiency, P_{OB} = 10 W	η_C	2	28	35	–	%
Collector-to-Base Capacitance, V_{CB} = 30 V	C_{obo}	1 MHz		–	13	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

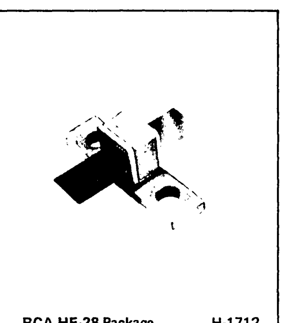
T_C = 145° C

V_{CB} = 8 V

P_T = 3.2 W

Solid State
Division

HR2N6268 HR2N6269



RCA HF-28 Package H-1712

6.5- and 2-W, 2.3-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistors

For Use in Microwave Power Amplifiers, Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **Designed for 20 to 24-V equipment**
- **Emitter-ballasting resistors**
- **VSWR capability of 10:1 at 2.3 GHz**
- **2-W output with 7-dB gain (min.) at 2.3 GHz (HR2N6268)**
- **6.5-W output with 5-dB gain (min.) at 2.3 GHz (HR2N6269)**
- **Stable common-base operation**

The RCA-HR2N6268 and RCA-HR2N6269 are high-reliability versions of the RCA-2N6268 and RCA-2N6269. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6268 and HR2N6269 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic 2N6268 and 2N6269 transistors in RCA data bulletin file No. 546.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

		HR2N6268	HR2N6269	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	45	45	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	45	45	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.350	1.5	A
TRANSISTOR DISSIPATION:	P_T			
At case temperature up to 75° C		6.25	21	W
At case temperature above 75° C ... Derate linearly at		0.05	0.168	W/°C
TEMPERATURE RANGE:				
Storage and operating (Junction)		−65 to +200		°C
CASE TEMPERATURE (During Soldering):				
For 10 s max.		230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR OR BASE VOLTAGE (V)		TEST CONDITIONS: DC CURRENT (mA)			LIMITS: HR2N6268		LIMITS: HR2N6269		UNITS
			V_{CE}	V_{BE}	I_E	I_B	I_C	MIN.	MAX.	MIN.	MAX.	
*	Collector Cutoff Current	I_{CES}	40	0				–	2	–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	45	–	45	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	3.5	–	V
	Collector-to-Emitter Breakdown Voltage With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					10	45	–	45	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				10 20	100 100	– –	1 –	– –	– 1	V
	Thermal Resistance (Junction-to-Flange)	$R_{\theta JF}$						–	20	–	6	°C/W
*	Forward Current Transfer Ratio	h_{FE}	5				100	10	200	15	200	

DYNAMIC

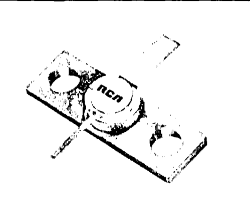
CHARACTERISTIC	SYMBOL	TEST CONDITIONS: FREQUENCY (f) – GHz	TEST CONDITIONS: DC COLLECTOR SUPPLY VOLTAGE (V_{CC}) – V	LIMITS: HR2N6268		LIMITS: HR2N6269		UNITS
				MIN.	MAX.	MIN.	MAX.	
Output Power, P_{IB} = 0.4 W = 2 W	P_{OB}	2.3 2.3	22 22	2 –	– –	– 6.5	– –	W
Power Gain, P_{OB} = 2 W = 6.5 W	G_{PB}	2.3 2.3	22 22	7 –	– –	– 5	– –	dB
Collector Efficiency, P_{OB} = 2 W = 6.5 W	η_C	2.3 2.3	22 22	33 –	– –	– 32	– –	%
Collector-to-Base Capacitance V_{CB} = 30 V	C_{obo}	1 MHz		–	5.5	–	13	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

	HR2N6268	HR2N6269	
T_A	25	–	°C
T_C	–	145	°C
V_{CB}	15	8	V
P_T	2	3.2	W

Solid State
Division



RCA HF-46

(RCA HF-46 can also be supplied without flange upon request.)

H-1796

1-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For Use in Microwave Power Amplifiers, Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- 1-W output with 7-dB gain (min.) at 2 GHz, 28 V
- Load VSWR capability of 10:1 at 2 GHz
- Emitter-ballasting resistors
- Stable common-base operation
- Ceramic-metal hermetic stripline package with low inductance and low parasitic capacitances
- For stripline, microstripline, and lumped-constant circuits

The RCA-HR2001 is a high-reliability version of the RCA-2001. It is specially processed and screened for high reliability in accordance with the basic scheduies outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2001 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic RCA-2001 transistor in RCA data bulletin file No. 759.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
EMITTER-TO-BASE VOLTAGE.	V_{EBO}	3.5	V
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75°C		5	W
At case temperature above 75°C . . . . . Derate linearly at		0.04	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≥ 0.02 in. (0.5 mm) from seating plane for 10 s max.		230	°C

ELECTRICAL CHARACTERISTICS, *at Case Temperature (T_C) = 25°C*

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
			Voltage V dc		Current mA dc		RCA2001		
			V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	
*	Collector Cutoff Current: With emitter open	I_{CBO}		28	0		–	0.5	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0	5	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1	0	3.5	–	V
	Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	25	°C/W
*	Forward Current Transfer Ratio	h_{FE}	5			100	15	120	

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
		VOLTAGE V dc	FREQUENCY GHz	POWER W		RCA2001		
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	
Output Power	P_{OB}	28	2	0.2		1	–	W
Large-Signal Common-Base Power Gain	G_{PB}	28	2		1	7	–	dB
Collector Efficiency	η_C	28	2		1	30	–	%
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	3	pF

* Recorded before and after burn-in for each device (serialized).

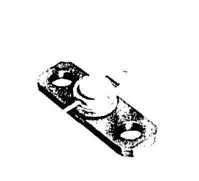
III. BURN-IN CONDITIONS

T_C = 130°C
V_{CB} = 15 V
P_T = 1.9 W

Solid State
Division

RF Power Transistors

HR2003 HR2N6390



RCA HF-46
(RCA HF-46 can also be supplied without flange upon request.)
H-1796

2.5- and 3-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistors

For Use in Microwave Power Amplifiers, Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **2.5-W output with 7-dB gain (min.) at 2 GHz, 28 V (HR2003)**
- **3-W output with 8-dB gain (min.) at 2 GHz, 28 V (HR2N6390)**
- **Load-VSWR capability of ∞: 1 at 2 GHz**
- **Emitter-ballasting resistors**
- **Stable common-base operation**

The RCA-HR2003 and RCA-HR2N6390 are high-reliability versions of the RCA 2003 and RCA 2N6390. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2003 and HR2N6390 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic RCA 2003 and 2N6390 transistors in RCA data bulletin file No. 626.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

		HR2003	HR2N6390	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	50	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	1	1	A
TRANSISTOR DISSIPATION:	P_T			
At case temperature up to 75° C		8.34	8.34	W
At case temperature above 75° C ... Derate linearly at		0.067	0.067	W/°C
TEMPERATURE RANGE:				
Storage and operating (Junction)		−65 to +200		°C
LEAD TEMPERATURE (During Soldering):				
At distances ⩾ 0.02 in. (0.5 mm) from seating plane for 10 s max.		230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Voltage V dc		Current mA dc		LIMITS HR2003		HR2N6390		UNITS
		V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	MIN.	MAX.	
* Collector Cutoff Current: With emitter open	I_{CBO}		28	0		–	0.5	–	–	mA
With emitter connected to base	I_{CES}	45				–	–	–	2	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0 0	1 2	50 –	– –	– 50	– –	V
Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$				5	50	–	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			1	0	3.5	–	3.5	–	V
* Forward Current Transfer Ratio	h_{FE}	10			50	20	120	20	120	
Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	15	–	15	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS VOLTAGE V dc	FREQUENCY GHz	POWER W		LIMITS HR2003		HR2N6390		UNITS
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	MIN.	MAX.	
Output Power	P_{OB}	28 28	2 2	0.5 0.475		2.5 –	– –	– 3	– –	W
Large-Signal Common-Base Power Gain	G_{PB}	28 28	2 2		2.5 3	7 –	– –	– 8	– –	dB
Collector Efficiency	η_C	28 28	2 2		2.5 3	30 –	– –	– 30	– –	%
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	5	–	5	pF

***Recorded before and after burn-in for each device (serialized).**

III. BURN-IN CONDITIONS

T_A = 25° C

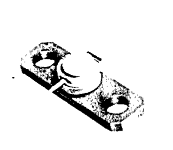
V_{CB} = 15 V

P_T = 2 W

Solid State Division

RF Power Transistors

HR2005 HR2N6391



RCA HF-46
(RCA HF-46 can also be supplied without flange upon request.)
H-1796

5-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistors

For Use in Microwave Power Amplifiers, Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **5-W output with 7-dB gain (min.) at 2 GHz, 28 V for both types**
- **Load-VSWR capability of ∞: 1 at 2 GHz**
- **Emitter-ballasting resistors**
- **Stable common-base operation**

The RCA-HR2005 and RCA-HR2N6391 are high-reliability versions of the RCA2005 and RCA-2N6391. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2005 and HR2N6391 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic RCA2005 and 2N6391 transistors in RCA data bulletin file No. 627.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

		HR2005	HR2N6391	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	50	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	2.5	2.5	A
TRANSISTOR DISSIPATION:	P_T			
At case temperature up to 75° C		16.7	16.7	W
At case temperature above 75° C ... Derate linearly at		0.133	0.133	W/°C
TEMPERATURE RANGE:				
Storage and operating (Junction)		–65 to +200		°C
LEAD TEMPERATURE (During Soldering):				
At distances ≥ 0.02 in. (0.5 mm) from seating plane for 10 s max.		230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS				UNITS
		Voltage V dc		Current mA dc		HR2005		HR2N6391		
		V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	MIN.	MAX.	
* Collector Cutoff Current: With emitter open	I_{CBO}		28	0		–	0.5	–	–	mA
With emitter connected to base	I_{CES}	45				–	–	–	3	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0	1	50	–	–	–	V
				0	5	–	–	50	–	
Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$				5	50	–	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			1	0	3.5	–	3.5	–	V
* Forward Current Transfer Ratio	h_{FE}	10			200	20	120	20	120	
Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	7.5	–	7.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS				UNITS
		VOLTAGE V dc	FREQUENCY GHz	POWER W		HR2005		HR2N6391		
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	MIN.	MAX.	
Output Power	P_{OB}	28	2	1		5	–	5	–	W
Large-Signal Common-Base Power Gain	G_{PB}	28	2		5	7	–	7	–	dB
Collector Efficiency	η_C	28	2		5	30	–	30	–	%
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	9	–	9	pF

*Recorded before and after burn-in for each device (serialized).

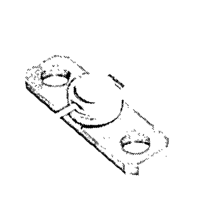
III. BURN-IN CONDITIONS

T_C = 135° C
V_{CB} = 8 V
P_T = 3.2 W

Solid State
Division

RF Power Transistors

HR2010 HR2N6392 HR2N6393



RCA HF-46
(RCA HF-46 can also be supplied without flange upon request.)

H-1796

10-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistors

For Use in Microwave Power Amplifiers,
Fundamental-Frequency Oscillators,
and Frequency Multipliers

Features:

- **10-W output with 7-dB gain (min.) at 2 GHz, 28 V (HR2N6393)**
- **10-W output with 5-dB gain (min.) at 2 GHz, 28 V (HR2010, HR2N6392)**
- **Load-VSWR capability of 10:1 at 2 GHz**
- **Emitter-ballasting resistors**
- **Stable common-base operation**

The RCA-HR2010, RCA-HR2N6392, and RCA-HR2N6393 are high-reliability versions of the RCA 2010, RCA-2N6392, and RCA-2N6393. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2010, HR2N6392, and HR2N6393 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic RCA 2010, 2N6392, and 2N6393 transistors in RCA data bulletin file No. 628.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*		HR2010	HR2N6392	HR2N6393	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	50	45	V
COLLECTOR-TO-EMITTER VOLTAGE:					
With external base-to-emitter resistance, $R_{BE} = 10\ \Omega$	V_{CER}	50	50	45	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	3.5	3.5	3.5	A
TRANSISTOR DISSIPATION:	P_T				
At case temperature up to 75° C		21	21	21	W
At case temperature above 75° C . . . Derate linearly at		0.167	0.167	0.167	W/°C
TEMPERATURE RANGE:					
Storage and operating (Junction)			−65 to +200		°C
LEAD TEMPERATURE (During Soldering):					
At distances ⩾0.02 in. (0.5 mm) from seating plane for 10 s max.			230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS						UNITS
		Voltage V dc		Current mA dc		HR2010		HR2N6392		HR2N6393		
		V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
* Collector Cutoff Current: With emitter open	I_{CBO}		28			–	0.5	–	–	–	–	mA
With emitter connected to base	I_{CES}	45				–	–	–	3	–	–	mA
		40				–	–	–	–	–	3	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0	5	50	–	50	–	45	–	V
Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V'_{(BR)CER}$				5	50	–	50	–	45	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			1	0	3.5	–	3.5	–	3.5	–	V
* Forward Current Transfer Ratio	h_{FE}	10			500[a]	20	120	20	120	20	120	
Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	6	–	6	–	6	°C/W

[a] Pulse test: pulse duration = 80 μs

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS						UNITS
		VOLTAGE V dc	FREQUENCY GHz	POWER W		HR2010		HR2N6392		HR2N6393		
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output Power	P_{OB}	28	2	2		–	–	–	–	10	–	W
		28	2	3		10	–	10	–	–	–	W
Large-Signal Common-Base Power Gain	G_{PB}	28	2		10	5	–	5	–	7	–	dB
Collector Efficiency	η_C	28	2		10	33	–	33	–	35	–	%
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	10	–	11	–	11	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_C = 145° C

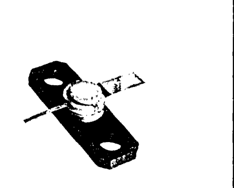
V_{CB} = 8 V

P_T = 3.2 W

Solid State
Division

RF Power Transistors

HR3001 HR3003 HR3005



RCA HF-46
(RCA HF-46 can also be supplied without flange upon request.)
H-1796

1-W, 2.5-W, and 4.5-W, 3-GHZ, Emitter-Ballasted N-P-N Transistors

Features:

- **1-W output with 7-dB gain (min.) at 3 GHz (HR3001)**
- **2.5-W output with 5-dB gain (min.) at 3 GHz (HR3003)**
- **4.5-W output with 5-dB gain (min.) at 3 GHz (HR3005)**
- **Emitter-ballasting resistors**
- **Stable common-base operation**
- **Hermetic stripline package with low inductances and low parasitic capacitances**
- **Load-VSWR capability of 10:1 at 3 GHz**

The RCA-HR3001, RCA-HR3003, and RCA-HR3005 are high-reliability versions of the RCA3001, RCA3003, and RCA3005. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR3001, HR3003, and HR3005 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic RCA3001, RCA3003, and RCA3005 transistor in RCA data bulletin file No. 657.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*		HR3001	HR3003	HR3005	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	50	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	3.5	V
TRANSISTOR DISSIPATION:	P_T				
At case temperature up to 75° C		5	8.34	14.7	W
At case temperature above 75° C ... Derate linearly at		0.04	0.067	0.118	W/°C
TEMPERATURE RANGE:					
Storage and operating (Junction)			−65 to +200		°C
LEAD TEMPERATURE (During Soldering):					
At distances ≥ 0.02 in. (0.5 mm) from seating plane for 10 s max.			230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS						UNITS
			Voltage V dc		Current mA dc		HR3001		HR3003		HR3005		
			V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
*	Collector Cutoff Current: With emitter open	I_{CBO}		28	0		–	0.5	–	0.5	–	0.5	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0	5	50	–	50	–	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1	0	3.5	–	3.5	–	3.5	–	V
*	Forward Current Transfer Ratio	h_{FE}	5			100	15	120	15	120	15	120	
	Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	25	–	15	–	8.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS						UNITS
		VOLTAGE V dc	FREQUENCY GHz	POWER W		HR3001		HR3003		HR3005		
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output Power	P_{OB}	28 28 28	3 3 3	0.2 0.8 1.4		1.0 – –	– – –	– 2.5 –	– – –	– – 4.5	– – –	W
Large-Signal Common-Base Power Gain	G_{PB}	28 28 28	3 3 3		1.0 2.5 4.5	7 – –	– – –	– 5 –	– – –	– – 5	– – –	dB
Collector Efficiency	η_C	28 28 28	3 3 3		1.0 2.5 4.5	30 – –	– – –	– 30 –	– – –	– – 30	– – –	%
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	3	–	5	–	7	pF

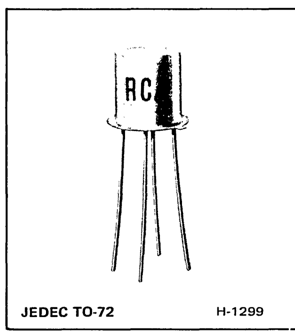
*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

	HR3001	HR3003	HR3005	
T_A	–	25	–	°C
T_C	130	–	145	°C
V_{CB}	15	15	8	V
P_T	1.9	2.0	3.2	W

Solid State
Division

HR40915



JEDEC TO-72 H-1299

0.2-to-1.4-GHz Low-Noise Silicon N-P-N Transistor

For High-Gain Small-Signal Applications

Features:

- **Low noise figure:**
  NF = 2.5 dB (max.) with 11 dB gain at 450 MHz
  = 3.0 dB (typ.) at 890 MHz
  = 4.5 dB (typ.) at 1.3 GHz
- **High gain (tuned, unneutralized):**
  G_{PE} = 14 dB (min.) at 450 MHz
  = 6.5 dB (typ.) at 1.3 GHz
- **High gain-bandwidth product**
- **Large dynamic range**
- **Low distortion**

The RCA-HR40915 is a high-reliability version of the RCA-40915. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR40915 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 40915 transistor in RCA data bulletin file No. 574.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	35	V
COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	15	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	40	mA
TRANSISTOR DISSIPATION:	P_T		
At ambient temperatures up to 25°C		200	mW
At ambient temperatures above 25°C	Derate linearly at	1.14	mW/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to + 200	°C

II. GROUP A TESTS, At Ambient Temperature (T_A) = 25°C.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		DC COLLECTOR VOLTAGE (V)		DC CURRENT (mA)					
		V_{CB}	V_{CE}	I_E	I_B	I_C	MIN.	MAX.	
STATIC									
* Collector Cutoff Current	I_{CBO}	10		0			–	20	nA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.01	35	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$				0	0.1	15	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.01		0	3.5	–	V
* DC Forward-Current Transfer Ratio	h_{FE}		10			3	20	–	–
Thermal Resistance: (Junction-to-Ambient)	$R_{\theta JA}$						–	880	°C/W
DYNAMIC									
Device Noise Figure (f = 450 MHz)	NF		10			1.5	–	2.5	dB
Small-Signal Common-Emitter Power Gain (f = 450 MHz) Unneutralized Amplifier	G_{PE}		10			1.5	14	–	dB
At minimum noise figure	G_{PE}		10			1.5	11.0	–	dB
Collector-to-Base Output Capacitance (f = 1 MHz)	C_{obo}	10		0			–	1.0	pF

*Recorded before and after burn-in for each device (serialized).

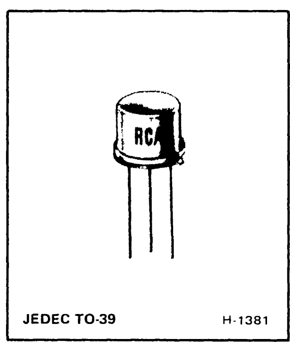
III. BURN-IN CONDITIONS

T_A = 25°C
V_{CB} = 15 V
P_T = 0.2 W

Solid State
Division

RF Transistors

HR41039


JEDEC TO-39 H-1381

Silicon N-P-N Overlay Transistor

For VHF Broadband Amplifiers in CATV and MATV Equipment

Features:

- **Low Device Noise Figure:**
  200-MHz narrow-band (30 mA) = 3 dB max.
  60-MHz narrow-band (30 mA) = 2.2 dB max.
  50-250-MHz broadband = 6.5 dB typ.
- **High Gain:**
  G_{PE} (200 MHz, 30 mA) = 15 dB min.
  G_{VE} (50-250 MHz, broadband) = 10 dB typ.
  f_T (30 mA) = 1.8 GHz min.
- **Low Distortion:**
  Cross-modulation (40 dBmV, 17 V, 60 mA) = −67 dB typ.
  IMD (50 dBmV, 17 V, 60 mA) = −55 dB typ.
- **Collector-to-Base Time Constant:**
  (f = 31.9 MHz) = 7.0 ps typ.

The RCA-HR41039 is a high-reliability version of the RCA-41039. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR41039 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 41039 transistor in RCA data bulletin file No. 764.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	40	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	25	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.25	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 75°C		2.5	W
At case temperatures above 75°C	Derate linearly at	0.02	W/°C
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		230	°C

II. GROUP A TESTS, At Case Temperature (T_C) = 25°C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS DC Voltage V		DC Current mA			LIMITS		UNITS
			V_{CB}	V_{CE}	I_E	I_B	I_C	Min.	Max.	
*	Collector-Cutoff Current	I_{CBO}	18			0		–	100	μA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		1	40	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Sustaining Voltage: With base open	$V_{VEO}(sus)$				0	20	25	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				10	100	–	0.25	V
*	DC Forward-Current Transfer Ratio	h_{FE}		15			50	60	350	
	Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$						–	50	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS DC Voltage V		DC Current mA			LIMITS		UNITS
		V_{CB}	V_{CE}	I_E	I_B	I_C	Min.	Max.	
Small-Signal, Common-Emitter Power Gain (f = 200 MHz)	G_{PE}		15			30	15	–	dB
Noise Figure (Measured) (f = 200 MHz)	NF		15			30	–	3.2[a]	dB
Wideband Voltage Gain (f = 50-250 MHz)	G_{VE}		17			60	9.5	–	dB
12-Channel Cross Modulation Distortion (f = 50-250 MHz; output level = 40 dBmV)	CMD		17			60	–62	–	dB
Gain-Bandwidth Product (f = 200 MHz)	f_T		15 15			30 60	1.8 2	– –	GHz
Collector-to-Base Capacitance (f = 1 MHz)	C_{obo}	30					–	2.5	pF

[a]Because of insertion loss of input test circuit, device noise figure is approximately 0.2 dB less than measured.

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25°C
V_{CB} = 15 V
P_T = 1 W

Solid State Division

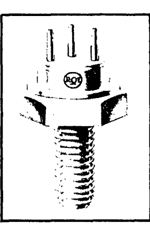
RF Power Transistors

40279

The RCA-40279 is the ultra-high reliability version of the RCA-2N3375 epitaxial silicon N-P-N planar transistor intended for class-A, -B, or -C amplifier, frequency multiplier, or oscillator operation. This device is subjected to special preconditioning tests for selection in ultra-high-reliability, large-signal, high-power, VHF-UHF applications in Space, Military, and Industrial communications equipment.

- **Ultra–High Reliability**
- **Complete Qualification Testing**

High-Power VHF-UHF Amplifier



JEDEC TO-60

RF SERVICE, Maximum Ratings (Absolute-Maximum Values)

Collector-To-Base Voltage, V_{CBO}	65	volts
Collector-To-Emitter Voltage:		
With base open, V_{CEO}	40	volts
With V_{BE} =-1.5 volts, V_{GEV}	65	volts
Emitter-To-Base Voltage, V_{EBO}	4	volts
Collector Current, I_C	1.5	amps.

Transistor Dissipation, P_T:		
At T_C up to 25°C	11.6	watts
At T_C above 25°C	Derate linearly to 0 watts at 200°C	
Temperature Range:		
Storage	-65 to 200	°C
Operating (Junction)	-65 to 200	°C
Lead Temperature (During soldering):		
At distances 1/32" from insulating wafer for 10 sec. max.	230	°C

ELECTRICAL CHARACTERISTICS – Case Temp. = 25°C (Unless Otherwise Specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR VOLTS		DC BASE VOLTS	DC CURRENT (MILLIAMPERES)			LIMITS		UNITS
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-Cutoff Current	I_{CEO}	–	30	–	–	0	–	–	0.1	μa
Collector To-Base Breakdown Voltage	BV_{CBO}	–	–	–	0	–	0.1	65	–	Volts
Collector-To-Emitter Breakdown Voltage	BV_{CEO}	–	–	–	–	0	0 to 200*	40**	–	Volts
Collector-To-Emitter Breakdown Voltage	BV_{CEV}	–	–	–1.5	–	–	0 to 200*	65**	–	Volts
Emitter-To-Base Breakdown Voltage	BV_{EBO}	–	–	–	0.1	–	0	4	–	Volts
Collector-To-Emitter Saturation Voltage	$V_{CE}(sat)$	–	–	–	–	100	0.5 amp	–	1	Volt
Output Capacitance	C_{ob}	30	–	–	0	–	–	–	10	pf
RF Power Output Amplifier, Unneutralized										
At 100 Mc (See Fig. 1)	P_{OUT}	–	28	–	–	–	–	7.5°	–	Watts
At 400 Mc (See Fig. 2)		–	28	–	–	–	–	3▲	–	Watts
Forward Current Transfer Ratio	h_{FE}	–	5	–	–	–	150	10	–	–

* Pulsed through an inductor (25 mh); duty factor = 50%
** Measured at a current where the breakdown voltage is a minimum.
● For P_{IN} = 1.0 w; minimum efficiency = 65%
▲ For P_{IN} = 1.0 w; minimum efficiency = 40%

TO-60 DIMENSIONAL OUTLINE

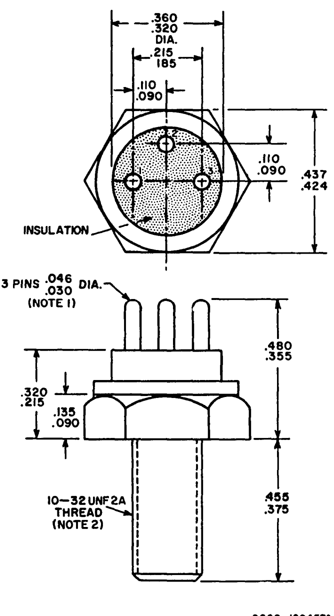
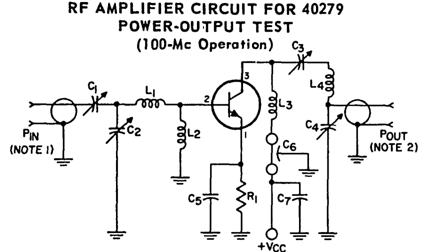


FIGURE 1

RF AMPLIFIER CIRCUIT FOR 40279 POWER-OUTPUT TEST (100-Mc Operation)



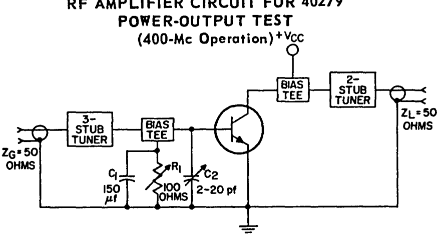
NOTE 1: GENERATOR IMPEDANCE = 50 OHMS.
NOTE 2: LOAD IMPEDANCE = 50 OHMS.

FOR 100-MC OPERATION

C_1, C_2: 7-100 PF
C_3, C_4: 4-40 PF
C_5: 330 PF, DISC CERAMIC
C_6: 1500 PF
C_7: 0.005 μF, DISC CERAMIC
L_1: 3 TURNS NO. 16 WIRE, 1/4" ID, 5/16" LONG
L_2: FERRITE CHOKE, Z = 750 ($\pm$20 %) OHMS
L_3: 2.4-μH CHOKE
L_4: 5 TURNS NO. 16 WIRE, 5/16" ID, 7/16" LONG
R_1: 1.35 OHMS, NON-INDUCTIVE

FIGURE 2

RF AMPLIFIER CIRCUIT FOR 40279 POWER-OUTPUT TEST (400-Mc Operation)



RELIABILITY TESTING

Electrically, the RCA-40279 is similar to the RCA-2N3375; the exception being the 40279 I_{CEO} is 100 nanoamperes maximum. In addition to Preconditioning and Group A tests, a Qualification Approval test series (Group B Tests) is performed on a semi-annual basis. All units are tested to assure freedom from second breakdown in Class-A applications.

Preconditioning (100 Per Cent Testing of Each Transistor)

1. Serialization
2. Record I_{CEO}, h_{FE}, V_{CE}(sat)
3. Temperature Cycling-Method 102A of MIL-STD-202, 5 cycles, -65°C +200°C
4. Bake, 72 hours minimum, +200°C
5. Constant Acceleration-Method 2006 of MIL-STD-750, 10, 000G, Y_1 and Y_2 axes
6. Record I_{CEO}, h_{FE}, V_{CE}(sat)
7. Reverse Bias Age, T_A = 150°C, V_{CB} = 28 V, t = 168 hours

*8. Record I_{CEO}, h_{FE}, V_{CE}(sat)

9. Power Age, T_A = 25°C, V_{CB} = 28 V, t = 500 hours, P_D = 2.6 W, free air

*10. Record I_{CEO}, h_{FE}, V_{CE}(sat) at 168 hours and 500 hours

11. Helium Leak, 1 x 10^{-8} cc/sec. max.
12. Methanol Bomb, 70 psig, 18 to 24 hours
13. X-Ray, RCA spec. 1750326
14. Record Subgroups 2 and 3 of Group A Tests

*

Delta criteria after 168 hours Reverse Bias Age and after 168 hours and 500 hour Power Age

ΔI_{CEO}	+100% or +10 nanoamperes whichever is greater
Δh_{FE}	±30%
ΔV_{CE}(sat)	±0.1 V

Group A Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD	SYMBOL	LIMITS		UNITS
					MIN.	MAX.	
	Subgroup 1		10				
2071	Visual and Mechanical Examination	–	–	–	–	–	–
	Subgroup 2		5				
3036D	Collector-To-Emitter Cutoff Current	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	100	namps
3001D	Collector-To-Base Breakdown Voltage	I_C = 100 μa, I_E = 0	–	BV_{CBO}	65	–	Volts
3026D	Emitter-To-Base Breakdown Voltage	I_E = 100 μa, I_C = 0	–	BV_{EBO}	4	–	Volts
3011D	Collector-To-Emitter Breakdown Voltage	I_C = 0 to 200 ma (Inductive) I_B = 0	–	BV_{CEO}	40	–	Volts
3011A	Collector-To-Emitter Breakdown Voltage	I_C = 0 to 200 ma (inductive) V_{BE} = -1.5 V	–	BV_{CEV}	65	–	Volts
3071	Collector-To-Emitter Saturation Voltage	I_C = 500 ma, I_B = 100 ma	–	V_{CE}(sat)	–	1	Volt
3076	Forward Current Transfer Ratio	I_C = 150 ma V_{CE} = 5 V	–	h_{FE}	10	–	
	Subgroup 3		5				
3236	Output Capacitance	f = 140 Kc, V_{CB} = 30 V, I_E = 0	–	C_{ob}	–	10	pf
See Fig. 1	R.F. Power Output (Min. Eff. = 65%)	V_{CE} = 28 V P_i = 1 W, f = 100 mc	–	P_{OUT}	7.5	–	Watts
See Fig. 2	R.F. Power Output (Min. Eff. = 40%)	V_{CE} = 28 V, P_i = 1 W, f = 400 mc	–	P_{OUT}	3	–	Watts
	Subgroup 4		15				
3036D	Collector Cutoff Current	T_A = 150°C ± 3°C, V_{CB} = 30 V, I_E = 0	–	I_{CBO}	–	100	μamp
3076	Forward Current Transfer Ratio	T_A = 150°C ± 3°C, I_C = 150 ma, V_{CE} = 5 V	–	h_{FE}	–	200	–

Group B Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD*	SYMBOL	LIMITS MIN.	MAX.	UNITS
	Subgroup 1 (10 samples)	–	7	–	–	–	–
2066	Physical Dimensions	TO-60	–	–	–	–	–
202/102A	Temperature Cycle	5~, -65°C, 200°C	–	–	–	–	–
1056B	Thermal Shock	0°C, 100°C	–	–	–	–	–
1021	Moisture Resistance	Omit lead fatigue	–	–	–	–	–
2036D	Torque-To-Stud	1 minute, 12 inch pounds	–	–	–	–	–
	Subgroup 2 (10 samples)		7				
2016	Impact Shock	500G, 5 blows X_1, Y_1, Z_1, 1 msec.	–	–	–	–	–
2046	Vibration Fatigue	–	–	–	–	–	–
2056	Vibration Var. Freq.	–	–	–	–	–	–
	Subgroup 3 (10 samples)		7				
2026	Solderability	–	–	–	–	–	–
1066	Dew Point	25°C, -65°C read I_{CEO}	–	–	–	–	–
1001	Barometric Pressure	100,000 ft. read I_{CEO}	–	–	–	–	–
	Subgroup 4 (25 samples)		7				
1031	Storage Life	200°C, 1000 hr	–	–	–	–	–
2006	Constant Acceleration	20,000G, Y_1, Y_2	–	–	–	–	–
	Subgroup 5 (25 samples)		7				
1026	Operating Life	1000 hrs T_C = 140°C, V_{CB} = 28 V, P_D = 4 W	–	–	–	–	–
	End Points Subgroups 1, 2, 3, 4, 5						
3036D	Collector-Cutoff Current	V_{CE} = 30, I_B = 0	–	I_{CEO}	–	1	μamp
3011A	Collector-To-Emitter Breakdown Voltage	I_C = 0 to 200 ma (inductive) V_{BE} = −1.5 V	–	BV_{CEV}	60	–	Volts
	R.F. Power Output (See Fig. 1)	f = 100 mc, V_{CE} = 28 V, P_i = 1 W	–	P_{OUT}	6.5	–	Watts
3076	Forward Current Transfer Ratio	I_C = 150 ma, V_{CE} = 5 V	–	h_{FE}	9	–	–
3026D	Emitter-To-Base Breakdown Voltage	I_E = 100 μa, I_C = 0	–	BV_{EBO}	3.5	–	Volts

* Acceptance/Rejection Criteria of Group B tests: For an LTPD plan of 7% the total sample size is 80 for which the maximum number of rejects allowed is 2. Acceptance is also subject to a maximum of one (1) reject per Subgroup.

Group B tests are performed once every six months as part of Qualification Approval.

Solid State
Division

RF Power Transistors

40294

RCA-40294 is an ultra-high-reliability double-diffused, epitaxial planar transistor of the silicon NPN type for low-noise amplifier, mixer, and oscillator applications at frequencies up to 500 MHz (common-emitter configuration), and up to 1200 MHz (common-base configuration).

This transistor is electrically and mechanically like RCA-2N2857, but is specially processed, preconditioned, and tested for critical aerospace and military applications.

The 40294 utilizes a hermetically sealed JEDEC TO-72 package. All active transistor elements are insulated from the case, which may be grounded by a fourth lead in applications requiring shielding of the device.

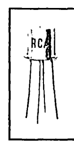
The curves of Typical Characteristics shown in the technical bulletin for RCA-2N2857 also apply for RCA-40294.

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	30 max.	V
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15 max.	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	2.5 max.	V
COLLECTOR CURRENT, I_C	40 max.	mA
TRANSISTOR DISSIPATION, P_T:		
For operation with heat sink:		
At case temperatures* up to 25°C	300 max.	mW
At case temperatures* above 25°C	Derate at 1.72 mW/°C	
For operation in free air:		
At ambient temperatures up to 25°C	200 max.	mW
At ambient temperatures above 25°C	Derate at 1.14 mW/°C	
TEMPERATURE RANGE:		
Storage and Operating (Junction)	-65 to +200	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds maximum	265 max.	°C

* Measured at center of seating surface.

ULTRA-HIGH-RELIABILITY SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR



JEDEC TO-72

For UHF Applications in Critical Aerospace and Military Equipment

Features

- Meets performance requirements of TX2N2857 MIL-S-19500/343 USAF, 7 March 1966
- Extra-rigorous control and inspection of all parts, materials, and internal assemblies before sealing
- 100% thermal and mechanical preconditioning after sealing
- complete electrical and mechanical QUALITY CONFORMANCE test program
- 100% RELIABILITY ASSURANCE testing
- 100% PERFORMANCE-REQUIREMENTS testing
- 100% Noise Figure and Power Gain Tests at 450 MHz
- high gain-bandwidth product — f_T = 1000 MHz min.
- very low Device Noise Figure — NF = 4.5 dB max. at 450 MHz
- high power gain as neutralized amplifier — G_{pe} = 12.5 dB min. at 450 MHz for circuit bandwidth of 20 MHz
- high power output as uhf oscillator — P_o = 30 mW min. at 500 MHz
- low collector-to-base time constant — $r_b'C_c$ = 15 ps max.

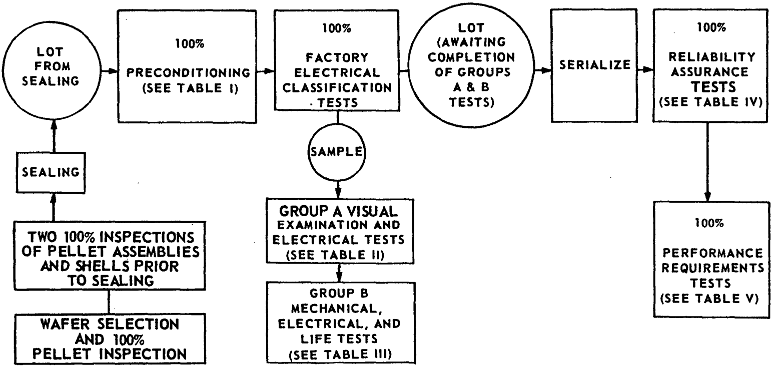
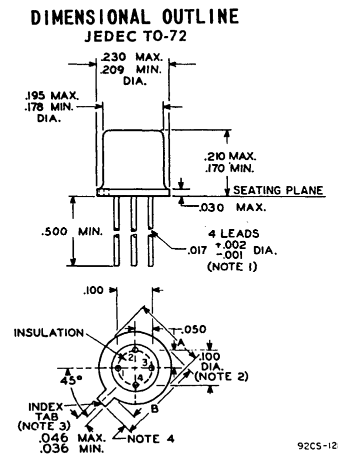


Fig. 1 - High-Reliability Testing Process Flow Diagram

TABLE I 100% PRECONDITIONING BEFORE FACTORY, QUALITY, RELIABILITY-ASSURANCE AND PERFORMANCE REQUIREMENTS TESTS

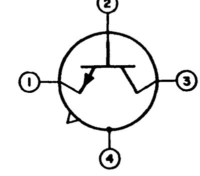
Test	Condition
STABILIZATION BAKE	48 hours minimum at 200° C
TEMPERATURE CYCLING (PER MIL-STD-750 METHOD 1051, COND. C)	5 complete cycles from -65° C to +200° C, each including 15 minutes at -65° C, 15 minutes at +200° C, and 5 minutes at 25° C
HELIUM-LEAK TEST (PER MIL-STD-202, METHOD 112 COND. C, PROC.IIIA)	Leakage may not exceed 10^{-8} atm cc/s
BUBBLE TEST (PER MIL-STD-202, METHOD 112 COND. A)	150° C minimum, 1 minute, ethylene glycol
CONSTANT-ACCELERATION (CENTRIFUGE) TEST (PER MIL-STD-750, METHOD 2006)	20,000 G's; Y_1 plane, 1 minute

DIMENSIONAL OUTLINE
JEDEC TO-72



TERMINAL DIAGRAM
Bottom View

LEAD 1 – EMITTER
LEAD 2 – BASE
LEAD 3 – COLLECTOR
LEAD 4 – CONNECTED TO CASE



NOTE 1: THE SPECIFIED LEAD DIAMETER APPLIES IN THE ZONE BETWEEN 0.050" AND 0.250" FROM THE SEATING PLANE. FROM 0.250" TO THE END OF THE LEAD A MAXIMUM DIAMETER OF 0.021" IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIAMETER IS NOT CONTROLLED.

NOTE 2: MAXIMUM DIAMETER LEADS AT A GAUGING PLANE 0.054" + 0.001" – 0.000" BELOW SEATING PLANE TO BE WITHIN 0.007" OF THEIR TRUE LOCATION RELATIVE TO MAX. WIDTH TAB AND TO THE MAXIMUM 0.230" DIAMETER MEASURED WITH A SUITABLE GAUGE. WHEN GAUGE IS NOT USED, MEASUREMENT WILL BE MADE AT SEATING PLANE.

NOTE 3: FOR VISUAL ORIENTATION ONLY.

NOTE 4: TAB LENGTH TO BE 0.028" MINIMUM – 0.048" MAXIMUM, AND WILL BE DETERMINED BY SUBTRACTING DIAMETER A FROM DIMENSION B.

TABLE II

GROUP A TESTS

Sub-group	Lot Tolerance Per Cent Defective	Characteristic Test	Symbol	MIL-STD 750 Reference Test Method	TEST CONDITIONS: Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B	LIMITS RCA 40294 Min.	Max.	Units
					°C	MHz	V	V	mA	mA	mA	Min.	Max.	
1	5	Visual and Mechanical Examination	--	2071	--	--	--	--	--	--	--	--	--	
2	3	Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0		--	10	nA
		Collector-Cutoff Current	I_{CES}	3041 Bias Condition C	25±3	--		16				--	100	nA
		Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0		30	--	V
		Collector-to-Emitter Breakdown Voltage	$BV_{CEO(sus)}$	3011 Test Condition D	25±3	--			3*		0	15	--	V
		Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	-0.001		2.5	--	V
		Base-to-Emitter Voltage	V_{BE}	3066 Test Condition A	25±3	--			10		1	--	1	V
		Collector-to-Emitter Voltage	V_{CE}	3071	25±3	--			10		1	--	0.4	V
		Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3			30	150	
3	10	Small-Signal Power Gain▲	G_{pe}		25±3	450		6	1.5			12.5	19	dB
		Device Noise Figure⊕: Generator Resistance (R_G) = 50 Ω	NF		25±3	450		6	1.5			--	4.5	dB
		Measured Noise Figure Generator Resistance R_G = 50Ω	NF		25±3	450		6	1.5			--	5.0	dB
		Collector-to-Base Time Constant▲	$r_b'C_c$		25±3	31.9		6		-2		4	15	ps
		Oscillator Power Output	P_o		25±3	≥500	10			-12		30	--	mW
		Collector-to-Base Feedback Capacitance ●	C_{cb}		25±3	≥0.1 ≤1	10			0		--	1	pF
4	10	Static Forward Current Transfer Ratio (Low Temperature)	h_{FE}	3076	-55±3	--		1	3			10	--	
		Collector-Cutoff Current (High Temperature)	I_{CBO}	3036 Bias Condition D	150^{+0}_{-5}	--	15			0		--	1	μA
		Small-Signal, Short Circuit Forward Current-Transfer Ratio▲	h_{fe}	3206	25±3	0.001		6	2			50	220	
		Magnitude of Small-Signal, Short-Circuit Forward Current Transfer Ratio▲	$\|h_{fe}\|$	3206	25±3	100		6	5			10	19	

* Pulse Test

▲ Lead No. 4 (Case) Grounded

⊕ Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test amplifier and the contribution of the following stages in the test setup.

● Three-terminal measurement with emitter and case leads guarded.

TABLE III
GROUP B TESTS

Subgroup	Test	MIL-STD 750 Reference	Lot Tolerance Per Cent Defective %	INITIAL AND ENDPOINT CHARACTERISTICS TESTS: Characteristic Test	MIL-STD 750 Reference	Test Conditions	RCA-40294 Initial Values Min.	Initial Values Max.	End Point Values Min.	End Point Values Max.	Units
1	PHYSICAL DIMENSIONS (See Dimensional Outline Drawing on page 7)	2066	20	--	--	--	--	--	--	--	
2	SOLDERABILITY Solder Temp. = 260±5°C	2026	10	I_{CBO}	3036D	T_A =25±3 °C V_{CB}=15 V	--	10	--	10	nA
	TEMPERATURE-CYCLING TEST (Condition C)	1051									
	THERMAL-SHOCK TEST: $T_{min} = 0^{+5}_{-0}$ °C $T_{max} = 100^{+0}_{-5}$ °C	1056 Test Condition A		h_{FE}	3076	T_A =25±3 °C V_{CE}=1 V I_C=3 mA	30	150	30	150	
	MOISTURE-RESISTANCE TEST	1021									
3	SHOCK TEST: NON-OPERATING 1500 G's, 0.5 ms 5 blows each in X_1, Y_1, Y_2, and Z_1 planes	2016	10	I_{CBO}	3036D	T_A =25±3 °C V_{CB}=15 V	--	10	--	10	nA
	VIBRATION FATIGUE TEST: NON-OPERATING 60 ±20 Hz, 20 G's	2046		h_{FE}	3076	T_A =25±3°C V_{CE}=1 V I_C=3 mA	30	150	30	150	
	VIBRATION VARIABLE-FREQUENCY TEST	2056									
	CONSTANT-ACCELERATION TEST: 20,000 G's	2006									
4	TERMINAL STRENGTH TEST	2036 Test Condition E	20	Helium Leak Test	MIL-STD 202 Method 112 Condition C Procedure III A		--	--	--	10^{-8}	atm cm^3/s
				Bubble Test	MIL-STD 202 Condition A	T_A=150°C (min.) 1 minute					
5	SALT-ATMOSPHERE TEST	1041	20	I_{CBO}	3036D	T_A =25±3 °C V_{CB}=15 V	--	10	--	10	nA
				h_{FE}	3076	T_A =25±3°C V_{CE}=1 V I_C=3 mA	30	150	30	150	
6	HIGH-TEMPERATURE LIFE TEST (NON-OPERATING): T_A =200±10°C Duration=1000 hrs.	1031	λ= 7%	I_{CBO}	3036D	T_A =25±3° C V_{CB}=15 V	--	10	--	20	nA
				h_{FE}	3076	T_A =25±3°C V_{CE}=1 V I_C=3 mA	30	150	24	180	
7	STEADY-STATE OPERATION LIFE TEST: Common-Base Circuit T_A =25±3° C V_{CB}=12.5±0.5 V P_T=200 mW Duration=1000 hrs.	1026	λ= 7%	I_{CBO}	3036D	T_A=25±3 °C V_{CB}=15 V	--	10	--	20	nA
				h_{FE}	3076	T_A =25±3 °C V_{CE}=1 V I_C=3 mA	30	150	24	180	

TABLE IV

100% RELIABILITY ASSURANCE TEST

THE CUMULATIVE REJECTS OF TABLES IV AND V SHALL NOT EXCEED 10% OF THE LOT

Test	MIL-STD 750 Reference	INITIAL AND ENDPOINT CHARACTERISTICS TESTS				
		Characteristic Test	RCA-40294		MIL-STD 750 Reference	Test Conditions
			Initial Value	Endpoint Value		
POWER BURN-IN: Common-Base Circuit $T_A = 25 \pm 3\,^{\circ}C$ $V_{CB} = 12.5 \pm 0.5$ V $P_T = 200$ mW Duration=340 hours	1026	ΔI_{CBO}	10 max. nA	$\Delta = \pm 5$ nA	3036 Bias Condition D	$T_A = 25 \pm 3\,^{\circ}C$ $V_{CB} = 15$ V
		Δh_{FE}	30 min. 150 max.	$\Delta = \pm 15\%$	3076	$T_A = 25 \pm 3\,^{\circ}C$ $V_{CE} = 1$ V $I_C = 3$ mA

TABLE V

100% PERFORMANCE REQUIREMENTS TESTS

THE CUMULATIVE REJECTS OF TABLES IV AND V SHALL NOT EXCEED 10% OF THE LOT

Test	Symbol	MIL-STD 750 Reference	TEST CONDITIONS							LIMITS		Units
			Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B	RCA 40294		
			°C	MHz	V	V	mA	mA	mA	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0		--	10	nA
Collector-Cutoff Current	I_{CES}	3041 Bias Condition C	25±3	--		16				--	100	nA
Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0		30	--	V
Collector-to-Emitter Breakdown Voltage	BV_{CEO} (sus)	3011 Test Condition D	25±3	--			3*		0	15	--	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	−0.001		2.5	--	V
Base-to-Emitter Voltage	V_{BE}	3066 Test Condition A	25±3	--			10		1	--	1	V
Collector-to-Emitter Voltage	V_{CE}	3071	25±3	--			10		1	--	0.4	V
Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3			30	150	
Device Noise Figure▲: Generator Resistance (R_G)=50 Ohms	NF	--	25±3	450		6	1.5			--	4.5	dB
Measured Noise Figure Generator Resistance $R_G = 50\,\Omega$ ▲	NF		25±3	450		6	1.5			--	5.0	dB
Visual Examination (External) Under 20-Power Magnification		Examine leads, header, and shell for visual defects.										

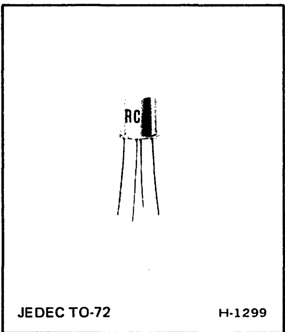
* Pulse Test

▲ Lead No. 4 (Case) Grounded

Solid State
Division

RF Power Transistors

40296



JEDEC TO-72 H-1299

Ultra-High-Reliability Silicon N-P-N Epitaxial Planar Transistor

For UHF Applications in Critical Aerospace and Military Equipment

Features:

- **Meets performance requirements of TX2N2857 MIL-S-19500/343 USAF, 7 March 1966**
- **Extra-rigorous control and inspection of all parts, materials, and internal assemblies before sealing**
- **100% thermal and mechanical preconditioning after sealing**
- **Complete electrical and mechanical QUALITY CONFORMANCE test program**
- **100% RELIABILITY ASSURANCE testing**
- **100% PERFORMANCE-REQUIREMENTS testing**
- **100% noise figure and power gain tests at 450 MHz**

RCA-40296 is an ultra-high-reliability double-diffused, epitaxial planar transistor of the silicon n-p-n type for low-noise amplifier, mixer, and oscillator applications at frequencies up to 500 MHz (common-emitter configuration), and up to 1200 MHz (common-base configuration).

This transistor is electrically and mechanically like RCA-2N2857, but is specially processed, preconditioned, and tested for critical aerospace and military applications.

The 40296 utilizes a hermetically sealed JEDEC TO-72 package. All active transistor elements are insulated from the case, which may be grounded by a fourth lead in applications requiring shielding of the device.

The curves of Typical Characteristics shown in the technical bulletin for RCA-2N2857 also apply for RCA-40296.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	2.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	40	mA
TRANSISTOR DISSIPATION	P_T		
With heat sink, at case* temperatures up to 25°C		300	mW
With heat sink, at case* temperatures above 25°C		Derate linearly 1.72	mW/°C
At ambient temperatures up to 25°C		200	mW
At ambient temperatures above 25°C		Derate linearly 1.14	mW/°C
TEMPERATURE RANGE:			
Storage & Operating (Junction)		-65 to +200	°C
CASE TEMPERATURE (During soldering):			
At distances ⩾ 1/32 in. (0.8 mm) from seating surface for 10 seconds max.		265	°C

* Measured at center of seating surface.

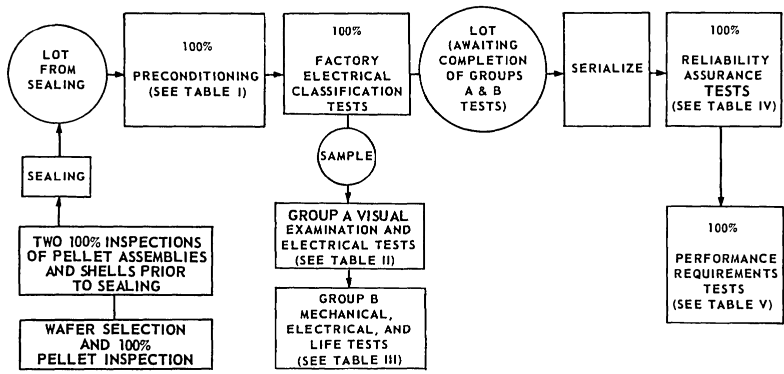
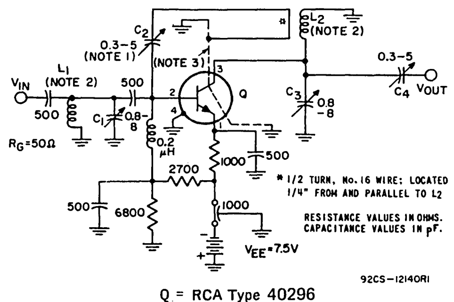


Fig. 1 - High-Reliability Testing Process Flow Diagram



NOTE 1: (NEUTRALIZATION PROCEDURE): (A) CONNECT A 450-MHz SIGNAL GENERATOR (WITH R_g = 50 OHMS) TO THE INPUT TERMINALS OF THE AMPLIFIER. (B) CONNECT A 50-OHM RF VOLTMETER ACROSS THE OUTPUT TERMINALS OF THE AMPLIFIER. (C) APPLY V_{EE}, AND WITH THE SIGNAL GENERATOR ADJUSTED FOR 5 mV OUTPUT FROM THE AMPLIFIER, TUNE C_1, C_3, AND C_4 FOR MAXIMUM OUTPUT. (D) INTERCHANGE THE CONNECTIONS TO THE SIGNAL GENERATOR AND THE RF VOLTMETER. (E) WITH SUFFICIENT SIGNAL APPLIED TO THE OUTPUT TERMINALS OF THE AMPLIFIER, ADJUST C_2 FOR A MINIMUM INDICATION AT THE INPUT. (F) REPEAT STEPS (A), (B), AND (C) TO DETERMINE IF RETUNING IS NECESSARY.

NOTE 2: L_1 & L_2–SILVER-PLATED BRASS ROD, 1-1/2" LONG x 1/4" DIA. INSTALL AT LEAST 1/2" FROM NEAREST VERTICAL CHASSIS SURFACE.

NOTE 3: EXTERNAL INTERLEAD SHIELD TO ISOLATE THE COLLECTOR LEAD FROM THE EMITTER AND BASE LEADS.

Fig. 2 - Neutralized Amplifier Circuit Used to Measure 450-MHz Power Gain and Noise Figure.

TABLE I 100% PRECONDITIONING BEFORE FACTORY, QUALITY, RELIABILITY-ASSURANCE AND PERFORMANCE REQUIREMENTS TESTS

Test	Condition
STABILIZATION BAKE	48 hours minimum at 200° C
TEMPERATURE CYCLING (PER MIL-STD-750 METHOD 1051, COND. C)	5 complete cycles from -65° C to +200° C, each including 15 minutes at -65° C, 15 minutes at +200° C, and 5 minutes at 25° C
HELIUM-LEAK TEST (PER MIL-STD-202, METHOD 112 COND. C, PROC.IIIA)	Leakage may not exceed 10^{-8} atm cc/s
BUBBLE TEST (PER MIL-STD-202, METHOD 112 COND. A)	150° C minimum, 1 minute, ethylene glycol
CONSTANT-ACCELERATION (CENTRIFUGE) TEST (PER MIL-STD-750, METHOD 2006)	20,000 G's; Y_1 plane, 1 minute

TABLE II

GROUP A TESTS

Sub-group	Lot Tolerance Per Cent Defective	Characteristic Test	Symbol	MIL-STD 750 Reference Test Method	TEST CONDITIONS: Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B	LIMITS RCA 40296: Min.	Max.	Units
					°C	MHz	V	V	mA	mA	mA	Min.	Max.	
1	5	Visual and Mechanical Examination	--	2071	--	--	--	--	--	--	--	--	--	
2	3	Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0		--	10	nA
		Collector-Cutoff Current	I_{CES}	3041 Bias Condition C	25±3	--		16				--	100	nA
		Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0		30	--	V
		Collector-to-Emitter Breakdown Voltage	BV_{CEO} (sus)	3011 Test Condition D	25±3	--			3*		0	15	--	V
		Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	0.001		2.5	--	V
		Base-to-Emitter Voltage	V_{BE}	3066 Test Condition A	25±3	--			10		1	--	1	V
		Collector-to-Emitter Voltage	V_{CE}	3071	25±3	--			10		1	--	0.4	V
		Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3			30	150	
3	10	Small-Signal Power Gain▲	G_{pe}		25±3	450		6	1.5			11.5	16.5	dB
		Device Noise Figure⊕: Generator Resistance $(R_G) = 50\ \Omega$	NF		25±3	450		6	1.5			--	3.4	dB
		Measured Noise Figure Generator Resistance $R_G = 50\Omega$	NF		25±3	450		6	1.5				4.2	dB
		Collector-to-Base Time Constant▲	$r_{b'}C_c$		25±3	31.9		6		-2		4	15	ps
		Oscillator Power Output	P_o		25±3	≥500	10			-12		30	--	mW
		Collector-to-Base Feedback Capacitance ●	C_{cb}		25±3	≥0.1 ≤1	10			0		--	1	pF
4	10	Static Forward Current Transfer Ratio (Low Temperature)	h_{FE}	3076	-55±3	--		1	3			10	--	
		Collector-Cutoff Current (High Temperature)	I_{CBO}	3036 Bias Condition D	150^{+0}_{-5}	--	15			0		--	1	µA
		Small-Signal, Short Circuit Forward Current-Transfer Ratio▲	h_{fe}	3206	25±3	0.001		6	2			50	220	
		Magnitude of Small-Signal, Short-Circuit Forward Current Transfer Ratio▲	$\|h_{fe}\|$	3206	25±3	100		6	5			10	20	

* Pulse Test

▲ Lead No. 4 (Case) Grounded

⊕ Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test amplifier and the contribution of the following stages in the test setup.

● Three-terminal measurement with emitter and case leads guarded.

TABLE III
GROUP B TESTS

Subgroup	Test	MIL-STD 750 Reference	Lot Tolerance Per Cent Defective (%)	Charac-teristic Test	MIL-STD 750 Reference	Test Conditions	RCA-40296 Initial Values Min.	RCA-40296 Initial Values Max.	RCA-40296 End Point Values Min.	RCA-40296 End Point Values Max.	Units
1	PHYSICAL DIMENSIONS (See Dimensional Outline Drawing on page 7)	2066	20	--	--	--	--	--	--	--	
2	SOLDERABILITY Solder Temp. = 260±5°C	2026	10	I_{CBO}	3036D	T_A = 25±3°C, V_{CB} = 15 V	--	10	--	10	nA
2	TEMPERATURE-CYCLING TEST (Condition C)	1051	10								
2	THERMAL-SHOCK TEST: $T_{min} = 0^{+5}_{-0}$ °C, $T_{max} = 100^{+0}_{-5}$ °C	1056 Test Condition A	10	h_{FE}	3076	T_A = 25±3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	30	150	
2	MOISTURE-RESISTANCE TEST	1021	10								
3	SHOCK TEST: NON-OPERATING 1500 G's, 0.5 ms 5 blows each in X_1, Y_1, Y_2, and Z_1 planes	2016	10	I_{CBO}	3036D	T_A = 25±3°C, V_{CB} = 15 V	--	10	--	10	nA
3	VIBRATION FATIGUE TEST: NON-OPERATING 60 ±20 Hz, 20 G's	2046	10								
3	VIBRATION VARIABLE-FREQUENCY TEST	2056	10	h_{FE}	3076	T_A = 25±3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	30	150	
3	CONSTANT-ACCELERATION TEST: 20,000 G's	2006	10								
4	TERMINAL STRENGTH TEST	2036 Test Condition E	20	Helium Leak Test	MIL-STD 202 Method 112 Condition C Procedure III A		--	--	--	10^{-8}	atm cm^3/s
4	TERMINAL STRENGTH TEST	2036 Test Condition E	20	Bubble Test	MIL-STD 202 Condition A	T_A = 150°C (min.) 1 minute					
5	SALT-ATMOSPHERE TEST	1041	20	I_{CBO}	3036D	T_A = 25±3°C, V_{CB} = 15 V	--	10	--	10	nA
5	SALT-ATMOSPHERE TEST	1041	20	h_{FE}	3076	T_A = 25±3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	30	150	
6	HIGH-TEMPERATURE LIFE TEST (NON-OPERATING): T_A = 200±10°C Duration = 1000 hrs.	1031	λ = 7%	I_{CBO}	3036D	T_A = 25±3°C, V_{CB} = 15 V	--	10	--	20	nA
6	HIGH-TEMPERATURE LIFE TEST (NON-OPERATING): T_A = 200±10°C Duration = 1000 hrs.	1031	λ = 7%	h_{FE}	3076	T_A = 25±3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	24	180	
7	STEADY-STATE OPERATION LIFE TEST: Common-Base Circuit T_A = 25±3°C V_{CB} = 12.5±0.5 V P_T = 200 mW Duration = 1000 hrs.	1026	λ = 7%	I_{CBO}	3036D	T_A = 25±3°C, V_{CB} = 15 V	--	10	--	20	nA
7	STEADY-STATE OPERATION LIFE TEST: Common-Base Circuit T_A = 25±3°C V_{CB} = 12.5±0.5 V P_T = 200 mW Duration = 1000 hrs.	1026	λ = 7%	h_{FE}	3076	T_A = 25±3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	24	180	

TABLE IV

100% RELIABILITY ASSURANCE TEST

THE CUMULATIVE REJECTS OF TABLES IV AND V SHALL NOT EXCEED 10% OF THE LOT

Test	MIL-STD 750 Reference	INITIAL AND ENDPOINT CHARACTERISTICS TESTS				
		Characteristic Test	RCA-40296 Initial Value	RCA-40296 Endpoint Value	MIL-STD 750 Reference	Test Conditions
POWER BURN-IN: Common-Base Circuit T_A =25±3°C V_{CB}=12.5±0.5 V P_T=200 mW Duration=340 hours	1026	ΔI_{CBO}	10 max. nA	Δ= ±5 nA	3036 Bias Condition D	T_A =25±3 °C V_{CB}=15 V
		Δh_{FE}	30 min. 150 max.	Δ=±15%	3076	T_A =25±3 °C V_{CE}=1 V I_C=3 mA

TABLE V

100% PERFORMANCE REQUIREMENTS TESTS

THE CUMULATIVE REJECTS OF TABLES IV AND V SHALL NOT EXCEED 10% OF THE LOT

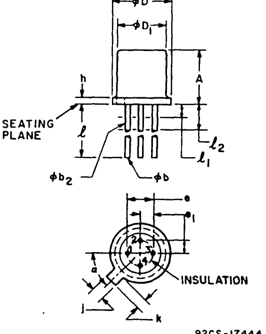
Test	Symbol	MIL-STD 750 Reference	TEST CONDITIONS							LIMITS RCA 40296		Units
			Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B			
			°C	MHz	V	V	mA	mA	mA	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0		--	10	nA
Collector-Cutoff Current	I_{CES}	3041 Bias Condition C	25±3	--		16				--	100	nA
Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0		30	--	V
Collector-to-Emitter Breakdown Voltage	BV_{CEO} (sus)	3011 Test Condition D	25±3	--			3*		0	15	--	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	0.001		2.5	--	V
Base-to-Emitter Voltage	V_{BE}	3066 Test Condition A	25±3	--			10		1	--	1	V
Collector-to-Emitter Voltage	V_{CE}	3071	25±3	--			10		1	--	0.4	V
Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3			30	150	
Device Noise Figure▲: Generator Resistance (R_G)=50 Ohms (See Fig. 3 for Test Circuit)	NF	--	25±3	450		6	1.5			--	3.9	dB
Visual Examination (External) Under 20-Power Magnification		Examine leads, header, and shell for visual defects.										

* Pulse Test

▲ Lead No. 4 (Case) Grounded

DIMENSIONAL OUTLINE

JEDEC TO–72



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.50 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.50 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter 0.019 in. (0.484 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.025 mm) – 0.000 (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

Note 6: Tab centerline.

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector
Lead 4 – Connected to case

Solid State
Division

RF Power Transistors

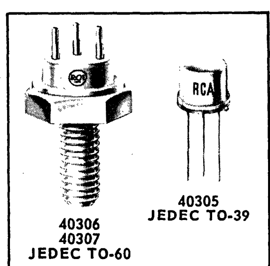
40305
40306
40307

RCA-40305, 40306, and 40307 are high-reliability variants of RCA-2N3553, 2N3375, and 2N3632 epitaxial silicon n-p-n overlay transistors. They are intended for Class-A▲, -B, or -C amplifier, frequency multiplier, or oscillator operation.

These devices are subjected to special preconditioning tests for selection in high-reliability, large-signal, high-power, VHF-UHF applications in Space, Military, and Industrial communications equipment.

High Reliability

High-Power VHF-UHF Amplifier



40306
40307
JEDEC TO-60

40305
JEDEC TO-39

FEATURES

- High-Reliability Assured By Seven (7) Preconditioning Steps
- Data Recorded Before and After "Power-Age Test" and Held to Critical Delta Criteria
- High Voltage Ratings —
  V_{CBO} = 65 volts max.
  V_{CEV} = 65 volts max.
  V_{CEO} = 40 volts max.
- 100 Per-Cent Tested to Assure Freedom from Second Breakdown for Operation in Class-A Applications
- High Power Output, P_{OUT}, Unneutralized Class-C Amplifier —
  At 400 Mc, 3 w min. (40306)
  175 Mc { 13.5 w min. (40307); 2.5 w min. (40305) }
  100 Mc, 7.5 w min. (40306)

RF SERVICE▲

Maximum Ratings, *Absolute-Maximum Values*

	40305	40306	40307	
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	65	65	65	volts
COLLECTOR-TO-EMITTER VOLTAGE:				
With base open, V_{CEO}	40	40	40	volts
With V_{BE} = -1.5 volts, V_{CEV}	65	65	65	volts
EMITTER-TO-BASE VOLTAGE, V_{EBO}	4	4	4	volts
COLLECTOR CURRENT, I_C	1.0	1.5	3.0	amperes
TRANSISTOR DISSIPATION, P_T▲:				
At case temperatures up to 25° C	7.0	11.6	23	watts

	40305	40306	40307	
At case temperatures above 25° C	Derate linearly to 0 watts at 200° C			
TEMPERATURE RANGE:				
Storage	-65 to 200			°C
Operating (Junction)	-65 to 200			°C
PIN OR LEAD TEMPERATURE (During soldering):				
At distances ≥ 1/32" from insulating wafer (TO-60 package) or from seating plane (TO-39 package) for 10 sec. max.	230			°C

▲Secondary breakdown considerations limit maximum DC operating conditions—contact your RCA representative for specific data.

ELECTRICAL CHARACTERISTICS
Case Temperature = 25° C

Characteristic	Symbol	TEST CONDITIONS						LIMITS						Units
		DC Collector Volts		DC Base Volts	DC Current (Milliamperes)			40305		40306		40307		
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current	I_{CEO}		30			0		-	0.1	-	0.1	-	0.25	µamp
Collector-to-Base Breakdown Voltage	BV_{CBO}				0 0 0		0.1 0.3 0.5	- 65 -	- - -	65 - -	- - -	- - 65	- - -	volts
Emitter-to-Base Breakdown Voltage	BV_{EBO}				0.1 0.25		0 0	4 -	- -	4 -	- -	- 4	- -	volts
Collector-to-Emitter Breakdown Voltage	BV_{CEO}					0	0 to 200[a]	40[b]	-	40[b]	-	40[b]	-	volts
	BV_{CEX}			-1.5			0 to 200[a]	65[b]	-	65[b]	-	65[b]	-	volts
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					100 50	500 250	- -	- 1	- -	1 -	- -	1 -	volt
DC Forward-Current Transfer Ratio	h_{FE}		5 5				150 300	10 -	- -	10 -	- -	- 10	- -	
Collector-to-Base Capacitance Measured at 1 Mc	C_{ob}	30			0			-	10	-	10	-	20	pf
RF Power Output Amplifier, Unneutralized At 100 Mc 175 Mc 175 Mc 400 Mc	P_{OUT}		28 28 28 28					- 2.5[d] - -	- - - -	7.5[c] - - 3[f]	- - - -	- - 13.5[e] -	- - - -	watts

[a] Pulsed through an inductor (25 mh); duty factor = 50%.

[b] Measured at a current where the breakdown voltage is a minimum.

[c] For P_{IN} = 1.0 w; minimum efficiency = 65%.

[d] For P_{IN} = 1/4 w; minimum efficiency = 50%.

[e] For P_{IN} = 3.5 w; minimum efficiency = 70%.

[f] For P_{IN} = 1.0 w; minimum efficiency = 40%.

RELIABILITY TESTING

RCA types 40305, 40306, and 40307 are electrically similar to RCA-2N3553, 2N3375, and 2N3632 respectively; but they differ in that they have substantially lower collector-cutoff current. I_{CEO} for the 40305 and 40306 is 100 nanoamperes maximum and I_{CEO} for the 40307 is 250 nanoamperes maximum.

Preconditioning (100 Per-Cent Testing of Each Transistor)

1. Helium Leak, 1 x 10^{-8} cc/sec. max.
2. Temperature Cycling-Method 102A of MIL-STD-202, 3 cycles, -65° C to +200° C
3. Methanol Bomb, 70 psig, 16 hours minimum
4. Bake, 72 hours minimum, +200° C
5. Constant Acceleration-Method 2006 of MIL-STD-750, 10,000 G, Y_1 axis
6. Serialization
7. Record I_{CEO}, h_{FE}, $V_{CE}(sat)$
8. Power Age, T_A = 25° C, V_{CB} = 28 V, t = 168 hours, free air
   P_D(40305) = 1 watt
   P_D(40306, 40307) = 2.6 watts
9. * Record I_{CEO}, h_{FE}, $V_{CE}(sat)$
10. X-Ray Inspection, RCA Spec. 1750326
11. Record Subgroups 2 and 3 of Group A Tests.

* Delta criteria after 168 hours Power Age

I_{CEO}	40305 40306	+100% or +10 nanoamperes whichever is greater
I_{CEO}	40307	+100% or +25 nanoamperes whichever is greater
h_{FE}		±30%
$V_{CE}(sat)$		±0.1 V

Group A Tests

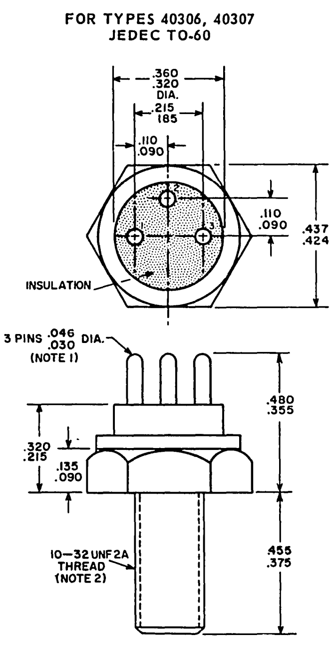
TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	SYMBOL	CONDITIONS	LTPD	LIMITS						UNITS
					40305		40306		40307		
					Min.	Max.	Min.	Max.	Min.	Max.	
	Subgroup 1			10							
2071	Visual and Mechanical Examination	-	-	-	-	-	-	-	-	-	-
	Subgroup 2			5							
3041D	Collector-To-Emitter Cutoff Current	I_{CEO}	V_{CE} = 30 V, I_B = 0	-	-	0.1	-	0.1	-	0.25	μamp
3001D	Collector-To-Base Breakdown Voltage	BV_{CBO}	I_C = 300 μa, I_E = 0	-	65	-	-	-	-	-	volts
			I_C = 100 μa, I_E = 0	-	-	-	65	-	-	-	volts
			I_C = 500 μa, I_E = 0	-	-	-	-	-	65	-	volts
3026D	Emitter-To-Base Breakdown Voltage	BV_{EBO}	I_E = 100 μa, I_C = 0	-	4	-	4	-	-	-	volts
			I_E = 250 μa, I_C = 0	-	-	-	-	-	4	-	volts
3011D	Collector-To-Emitter Breakdown Voltage	BV_{CEO}	I_C = 0 to 200 ma[a], I_B = 0	-	40[b]	-	40[b]	-	40[b]	-	volts
3011A	Collector-To-Emitter Breakdown Voltage	BV_{CEX}	I_C = 0 to 200 ma[a], V_{BE} = -1.5 V	-	65[b]	-	65[b]	-	65[b]	-	volts
3071	Collector-To-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 250 ma, I_B = 50 ma	-	-	1	-	-	-	-	volts
			I_C = 500 ma, I_B = 100 ma	-	-	-	-	1	-	1	volts
3076	Forward Current Transfer Ratio	h_{FE}	I_C = 150 ma, V_{CE} = 5 V	-	10	-	10	-	-	-	
			I_C = 300 ma, V_{CE} = 5 V	-	-	-	-	-	10	-	
	Subgroup 3			5							
3236	Open Circuit Output Capacitance	C_{ob}	f = 1 Mc, V_{CB} = 30 V, I_E = 0	-	-	10	-	10	-	20	pf
	R. F. Power Output	P_{OUT}	V_{CE} = 28 V, P_{IN} = 0.25 watt, f = 175 Mc, Min. Effic. = 50%	-	2.5	-	-	-	-	-	watts
			V_{CE} = 28 V, P_{IN} = 1 watt, f = 100 Mc, Min. Effic. = 65%	-	-	-	7.5	-	-	-	watts
			V_{CE} = 28 V, P_{IN} = 3.5 watts, f = 175 Mc, Min. Effic. = 70%	-	-	-	-	-	13.5	-	watts
			V_{CE} = 28 V, P_{IN} = 1 watt, f = 400 Mc, Min. Effic. = 40%	-	-	-	3	-	-	-	watts
	Subgroup 4			15							
3036D	Collector Cutoff Current	I_{CBO}	T_A = 150°C ± 3°C, V_{CB} = 30 V, I_E = 0	-	-	100	-	100	-	250	μamp
3076	Forward Current Transfer Ratio	h_{FE}	T_A = 150°C ± 3°C, I_C = 150 ma, V_{CE} = 5 V	-	-	200	-	200	-	-	
			T_A = 150°C ± 3°C, I_C = 300 ma, V_{CE} = 5 V	-	-	-	-	-	-	200	

[a] Pulsed through an inductor (25 mh); duty factor = 50%.

[b] Measured at a current where the breakdown voltage is a minimum.

DIMENSIONAL OUTLINES

FOR TYPES 40306, 40307
JEDEC TO-60



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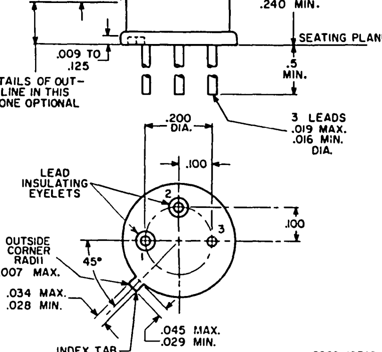
Dimensions in Inches

FOR TYPE 40305
JEDEC TO-39



92CS-12742

Dimensions in Inches

NOTE 1: THE PIN SPACING PERMITS INSERTION IN ANY SOCKET HAVING A PIN-CIRCLE DIAMETER OF 0.200" AND CONTACTS WHICH WILL ACCOMMODATE PINS HAVING A DIAMETER OF 0.035" MIN., 0.045" MAX.

NOTE 2: THE TORQUE APPLIED TO A 10-32 HEX NUT ASSEMBLED ON THE THREAD DURING INSTALLATION SHOULD NOT EXCEED 12 INCH-POUNDS.

NOTE 3: THIS DEVICE MAY BE OPERATED IN ANY POSITION.

TERMINAL CONNECTIONS

Pin or Lead No.1 - Emitter

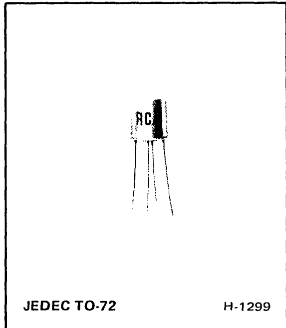
Pin or Lead No.2 - Base

Pin or Lead No.3 - Collector (For 40306, 40307)
Collector, Case (For 40305)

Solid State
Division

RF Power Transistors

40414



JEDEC TO-72 H-1299

High-Reliability Silicon N-P-N Epitaxial Planar Transistor

For UHF Applications in Industrial and Military Equipment

Features:

- **High gain-bandwidth product: f_T = 1000 MHz min.**
- **High converter (450-to-30 MHz) gain: G_c = 15 dB typ. for circuit bandwidth of approximately 2 MHz**
- **High power gain as neutralized amplifier: G_{PE} = 12.5 dB min. at 450 MHz for circuit bandwidth of 20 MHz**
- **High power output as uhf oscillator: P_{OE} = { 30 mW min., 40 mW typ. at 500 MHz; 20 mW typ., at 1 GHz }**
- **Low device noise figure: NF = { 4.5 dB max. as 450 MHz amplifier; 7.5 dB typ., as 450-to-30 MHz converter }**
- **Low collector-to-base time constant: $r_b'C_c$ = 7 ps typ.**
- **Low collector-to- base feedback capacitance: C_{cb} = 0.6 pF typ.**

RCA-40414 is a double-diffused epitaxial planar transistor of the silicon n-p-n type. It is extremely useful in low-noise-amplifier, oscillator, and converter applications at frequencies up to 500 MHz in the common-emitter configuration, and up to 1200 MHz in the common-base configuration.

The 40414 is electrically and mechanically like the RCA-2N2857, but each shipment of the RCA-40414 is accompanied by a certified summary of the results of the Group A Electrical Tests and the Group B Environmental Tests shown in Tables I and II, respectively. The Test Data Summary and Certification shown in the Specimen Copy on page 5 are the results of the acceptance tests for the production lot from which the shipment is made.

RCA–40414 utilizes a hermetically sealed 4-lead JEDEC TO-72 package. All active elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead in applications requiring shielding of the device.

The curves of Typical Characteristics shown in the Technical Bulletin for RCA-2N2857 also apply for RCA-40414.

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	2.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	40	mA
TRANSISTOR DISSIPATION	P_T		
At case temperatures* up to 25°C		300	mW
At case temperatures* above 25°C		Derate linearly 1.71	mW/°C
At ambient temperatures up to 25°C		200	mW
At ambient temperatures above 25°C		Derate linearly 1.14	mW/°C
TEMPERATURE RANGE:			
Storage & Operating (Junction)		–65 to +200	°C
CASE TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. (0.8 mm) from seating surface for 10 seconds max.		265	°C

* Measured at center of seating surface.

TABLE I – GROUP A TESTS

Sub-group	Lot Tolerance Per Cent Defective	Characteristic Test	Symbol	MIL-STD 750 Reference Test Method	TEST CONDITIONS: Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	LIMITS RCA 40414: Min.	Max.	Units
					°C	MHz	V	V	mA	mA	Min.	Max.	
1	10	Visual and Mechanical Examination	--	2071	--	--	--	--	--	--	--	--	
2	5	Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0	--	10	nA
		Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0	30	--	V
		Collector-to-Emitter Breakdown Voltage	BV_{CEO} (sus)	3011 Test Condition D	25±3	--			3*	I_B = 0	15	--	V
		Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	-0.01	2.5	--	V
		Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3		30	150	
3	15	Small-Signal Power Gain▲	G_{pe}		25±3	450		6	1.5		12.5	19	dB
		Device Noise Figure⊗ Generator Resistance (R_G) = 50 Ω	NF		25±3	450		6	1.5		--	4.5	dB
		Measured Noise Figure: Generator Resistance (R_G) = 50 Ω ▲	NF		25±3	450		6	1.5		--	5.0	dB
		Collector-to-Base Time Constant▲	$r_{b'}C_c$		25±3	31.9	6		2		4	15	ps
		Oscillator Power Output (See Fig.4 for Test Circuit)	P_o		25±3	≥500	10			-12	30	--	mW
		Collector-to-Base Feedback Capacitance●	C_{cb}		25±3	≥0.1 ≤1	10			0	--	1	pF
4	15	Static Forward Current Transfer Ratio (Low Temperature)	h_{FE}	3076	-55±3	--		1	3		10	--	
		Collector-Cutoff Current (High Temperature)	I_{CBO}	3036 Bias Condition D	150 +0 -5	--	15			0	--	1	µA
		Small-Signal, Short Circuit Forward Current-Transfer Ratio▲	h_{fe}	3206	25±3	0.001		6	2		50	220	
		Magnitude of Small-Signal, Short-Circuit Forward Current-Transfer Ratio▲	$\|h_{fe}\|$	3206	25±3	100		6	5		10	19	

* Pulse Test

▲Lead No.4 (Case) Grounded

●Three-terminal measurement with emitter and case leads guarded.

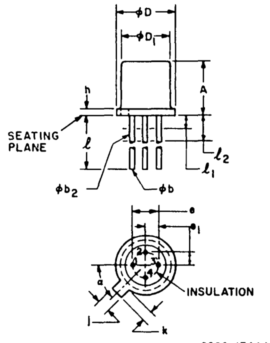
⊗Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test amplifier and the contribution of the following stages in the test setup.

TABLE II – GROUP B TESTS

Subgroup	Test	MIL-STD 750 Reference	Lot Tolerance Per Cent Defective	INITIAL AND ENDPOINT CHARACTERISTICS TESTS							Units
				Charac-teristic Test	MIL-STD 750 Reference	Test Conditions	RCA-40414				
							Initial Values		End Point Values		
			%				Min.	Max.	Min.	Max.	
1	PHYSICAL DIMENSIONS (See Dimensional Outline Drawing on page 6)	2066	20	--	--	--	--	--	--	--	
2	SOLDERABILITY Without Aging	2026	20	I_{CBO}	3036D	T_A = 25 ± 3°C, V_{CB} = 15 V	--	10	--	30	nA
	TEMPERATURE-CYCLING TEST (Condition C)	1051									
	THERMAL-SHOCK TEST: $T_{min} = 0^{+5}_{-0}$ °C, $T_{max} = 100^{+0}_{-5}$ °C	1056 Test Condition A		h_{FE}	3076	T_A = 25 ± 3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	18	--	
	MOISTURE-RESISTANCE TEST	1021									
3	SHOCK TEST: NON-OPERATING 1500 G's, 0.5 ms 5 blows each in X_1, Y_1, Y_2 and Z_1 planes	2016	20	I_{CBO}	3036D	T_A = 25 ± 3°C, V_{CB} = 15 V	--	10	--	30	nA
	VIBRATION FATIGUE TEST: NON-OPERATING 60 ± 20 Hz, 20 G's	2046									
	VIBRATION VARIABLE-FREQUENCY TEST	2056		h_{FE}	3076	T_A = 25 ± 3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	18	--	
	CONSTANT-ACCELERATION TEST: 20,000 G's	2006									
4	TERMINAL STRENGTH TEST	2036 Test Condition E	20	--	--	--	--	--	--	--	
				--	--	--	--	--	--	--	
5	SALT-ATMOSPHERE TEST	1041	20	I_{CBO}	3036D	T_A = 25 ± 3°C, V_{CB} = 15 V	--	10	--	30	nA
				h_{FE}	3076	T_A = 25 ± 3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	18	--	
6	HIGH-TEMPERATURE LIFE TEST (NON-OPERATING): T_A = 200 ± 10°C Duration = 1000 hrs.	1031	λ= 10%	I_{CBO}	3036D	T_A = 25 ± 3°C, V_{CB} = 15 V	--	10	--	30	nA
				h_{FE}	3076	T_A = 25 ± 3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	18	--	
7	STEADY-STATE OPERATION LIFE TEST: Common-Base Circuit T_A = 25 ± 3°C V_{CB} = 12.5 ± 0.5 V P_T = 200 mW Duration = 1000 hrs.	1026	λ= 10%	I_{CBO}	3036D	T_A = 25 ± 3°C, V_{CB} = 15 V	--	10	--	30	nA
				h_{FE}	3076	T_A = 25 ± 3°C, V_{CE} = 1 V, I_C = 3 mA	30	150	18	--	

DIMENSIONAL OUTLINE

JEDEC TO–72



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.50 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.50 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter 0.019 in. (0.484 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.025 mm) – 0.000 (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

Note 6: Tab centerline.

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector
Lead 4 – Connected to case

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40577

HIGH-RELIABILITY TRANSISTOR

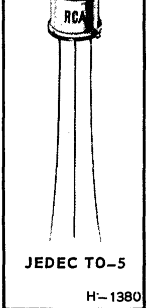
High-Gain Device for Class A or C Operation in VHF Circuits

RCA–40577* is a high-reliability variant of the RCA–2N3118, a triple-diffused transistor. It is especially processed for high reliability. It is intended for Class A and C amplifier, frequency multiplier or oscillator operation in high-reliability, large-signal, high-power VHF applications in Space, Military, and Industrial communications equipment.

High reliability is assured by eight preconditioning steps, including drift temperature measurements after the High Temperature Reverse Bias and Power Age tests. The 40577 also features complete qualification and lot acceptance testing.

*Formerly RCA-Dev. No. TA7079

- 8 Preconditioning Steps
- Complete Qualification and Lot Acceptance Testing
- 1.0 Watt Output Min. at 50 MHz
- 0.4 Watt Output Min. at 150 MHz



JEDEC TO-5

H-1380

RATINGS

Maximum Ratings, ***Absolute-Maximum Values:***

COLLECTOR-TO-EMITTER VOLTAGE:			
With V_{BE} = −1.5 volts	V_{CEV}	85	V
With base open	V_{CEO}	60	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
COLLECTOR CURRENT	I_C	0.5	A
TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 25° C		3	W
At free-air temperatures up to 25° C		0.5	W
At case temperatures above 25° C		See *Fig.4*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. from insulating wafer for 10 s max.		230	°C

TYPICAL POWER OUTPUT vs. POWER INPUT

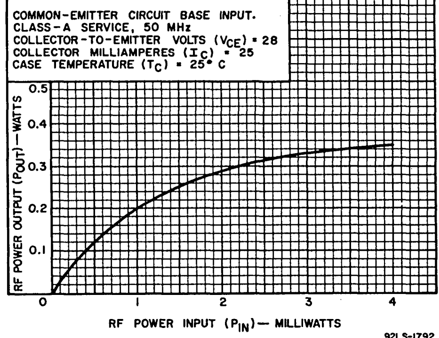


Fig. 1

ELECTRICAL CHARACTERISTICS
Case Temperature = 25° C
Except As Indicated

Characteristics	Symbols	TEST CONDITIONS							LIMITS		Units
		Frequency (MHz)	DC Collector-to-Base Voltage (volts)	DC Collector-to-Emitter Voltage (volts)	DC Base Volts	DC Current (Milliamperes)					
		f	V_{CB}	V_{CE}	V_{BE}	I_C	I_E	I_B	Min.	Max.	
Collector-Cutoff Current 25 °C[a] 150 °C[a]	I_{CBO}		30 30				0 0			10 5	nA µA
Emitter-to-Base Breakdown Voltage	BV_{EBO}					0	0.1		4		volts
Collector-to-Emitter Breakdown Voltage (Sustaining)	$BV_{CEO}(sus)$					10 pulsed[b]		0	60		volts
Reverse Collector-to-Emitter Breakdown Voltage	BV_{CEX}				−1.5	0.1			85		volts
Output Capacitance	C_{ob}	1	28			0				6	pF
$r_{bb}'C_{b}'_{c}$ Product	$r_{bb}'C_{b}'_{c}$	50		28		25				60	ps
DC Forward-Current Transfer Ratio[b]	h_{FE}			5		100			50	275	
Small-Signal Forward-Current Transfer Ratio	h_{fe}	50		28		25			5		
Real Part of Short-Circuit Input Impedance	$h_{ie(real)}$	50		28		25			25	75	ohms
Real Part of Short-Circuit Output Impedance	$1/Y_{22(real)}$	50		28		25			500	1000	ohms
Output Power Class-C Service Pin = 0.1 watt (with heat sink)	P_{OUT}	50 150		28 28					1.0 0.4		watt watt
Power Gain Class-A Service P_{out} = 0.2 watt (with heat sink)	PG	50		28		25			18		dB

[a] T_{FA} = free air temperature.
[b] Pulse duration 300 µs; duty factor, less than 1.8%.

TYPICAL LARGE-SIGNAL OPERATION, CLASS–C SERVICE

150 MH:

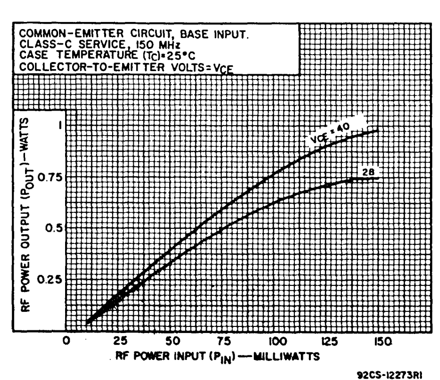


Fig. 2

DISSIPATION DERATING CURVE

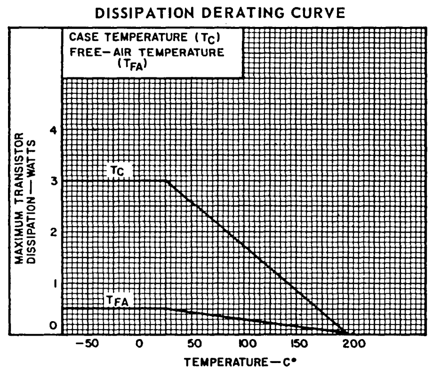


Fig. 3

RELIABILITY SPECIFICATIONS . . . .

In addition to Preconditioning and Group A tests, a Qualification Approval test series (Group B tests) is performed on each lot.

Preconditioning (100 Per Cent Testing of Each Transistor)

1. Serialization
2. Record I_{CBO}, h_{FE}
3. Temperature Cycling-Method 107B, Cond. C of MIL-STD-202, 5 cycles, -65° C to 200° C
4. Bake, 72 hours minimum, 200° C
5. Constant Acceleration-Method 2006 of MIL-STD-750, 10,000g, Y_1 and Y_2 axes
6. X-Ray
7. Record I_{CBO}, h_{FE}
8. Reverse Bias Age, $T_A = 175^{\circ}$ C, $V_{CB} = 60$ V, t = 96 hours
9. [d] Record I_{CBO}, h_{FE}.
10. Power Age, $T_A = 25^{\circ}$ C, $V_{CB} = 28$ V, t = 340 hours, $P_T = 1$ W, free air
11. [d] Record I_{CBO}, h_{FE} at 340 hours
12. Helium Leak, 1×10^{-7} cc/sec. max.
13. Gross Leak, MIL-STD-202, Method 112
14. Record Subgroups 2 and 3 of Group A Tests

[d] Delta criteria after 96 hours Reverse Bias Age and 340 hours Power Age.

ΔI_{CBO} +100% or +5 nanoamperes whichever is greater

Δh_{FE} ±20%

Definitions

Delta (Δ): Delta shall be determined by subtracting the parameter value measured before application of stress from the value measured after the application of stress.

Group A Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD	SYMBOL	LIMITS Min.	LIMITS Max.	UNITS
	Subgroup 1		10				
2071	Visual and Mechanical Examination	–	–	–	–	–	–
	Subgroup 2		5				
3036D	Collector-Cutoff Current	$V_{CB} = 30V$, $I_E = 0$	–	I_{CBO}	–	10	nA
3001D	Collector-to-Emitter Breakdown Voltage	$I_C = 100$ µA, $V_{BE} = -1.5$ V	–	BV_{CEV}	85[g]	–	volts
3026D	Emitter-to-Base Breakdown Voltage	$I_E = 100$ µA, $I_C = 0$	–	BV_{EBO}	4	–	volts
3011D	Collector-to-Emitter Breakdown Voltage	$I_C = 10$ mA[f] $I_B = 0$	–	V_{CEO}	60[g]	–	volts
3076	DC Forward-Current Transfer Ratio	$I_C = 100$ mA, $V_{CE} = 5V$	–	h_{FE}	50	275	
	Subgroup 3		5				
3236	Output Capacitance	f = 0.1 to 1.0 MHz, V_{CB}=28V, $I_E = 0$	–	C_{ob}	–	6.0	pF
	Power Output	f = 50 MHz, $V_{CE} = 28V$ Pin = 0.1 W	–	P_{OUT}	1.0	–	watts
	RF Power Output (Min. Eff. = 45%)	$V_{CE} = 28$ V, $P_{IN} = 0.1$ W f = 150 MHz	–	P_{OUT}	0.4	–	watts
3306	Small-Signal Forward-Current Transfer Ratio	$I_C = 25$ mA, $V_{CE} = 28$ V f = 50 MHz	–	h_{fe}	–	5.0	
	Subgroup 4		15				
3036D	Collector-Cutoff Current	$T_A = 150^{\circ}$C, $V_{CB} = 30$ V	–	I_{CBO}	–	5	µA
3201	Input Impedance	$V_{CE} = 28$ V, $I_C = 25$ mA f = 50 MHz	–	h_{ie}	25	75	ohms
3231	Output Admittance	$V_{CE} = 28$ V, $I_C = 25$ mA f = 50 MHz	–	Y_{22}	1	2	mmho

[f] Pulsed through an inductor (25 µH); duty factor = 50%.

[g] Measured at a current where the breakdown voltage is a minimum.

General Reliability Specifications that are applicable to all rf power transistors are given in booklet RFT–701 and must be used in conjunction with the specific Preconditioning, Group A Tests, and Group B Tests shown below.

Group B Tests[h]

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS
	Subgroup 1	(13 Samples)
2066	Physical Dimensions	JEDEC TO-5 Pkg.
	Subgroup 2	(13 Samples)
2026	Solderability	Omit aging, Dwell time = 10 s ± 1 s
1051	Thermal Shock (Temp. Cycling)	Test Condition C
1056	Thermal Shock (Glass Strain)	Test Condition B
	Seal (Leak Rate)	Method 112 of MIL-STD-202 Test Cond. C, procedure III; Test Cond. A for gross leaks
1021	Moisture Resistance	
	Subgroup 3	(13 Samples)
2016	Shock	1,500 g, 0.5 ms, 5 blows each orientation: X_1, Y_1, Y_2, Z_1
2046	Vibration Fatigue	Nonoperating
2056	Vibration Var. Freq.	–
2006	Constant Acceleration	20,000 G Y_1, Y_2
	Subgroup 4	(13 Samples)
2036	Terminal Strength (Lead Fatique)	Test Cond. E
	Subgroup 5	(13 Samples)
1041	Salt Atmosphere	
	Subgroup 6	(25 Samples)
1031	High Temperature Life (Non-operating)	$T_{storage}$ = 200° C, t = 1000 hrs.
	Subgroup 7	(25 Samples)
1026	Steady-State Operation	P_T = 1.5 W, T_C = 100° C, t = 1000 hrs. V_{CB} = 40 V

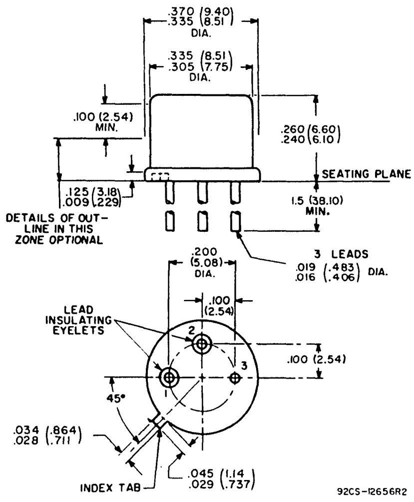
TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	SYMBOL	LIMITS		UNITS
				Min.	Max.	
	End Points Subgroups (2, 3, 5, 6)					
3036D	Collector Base Cutoff Current	V_{CB} = 30 V, I_E = 0	I_{CBO}		1.0	µA
3001D	Collector Base Breakdown Voltage	V_{BE} = −1.5 V, I_C= 100 µA	BV_{CEV}	80		
3076	DC Forward-Current Transfer Ratio	I_C =100 mA, V_{CE} = 5 V	h_{FE}	35	325	–

[h]Acceptance/Rejection Criteria of Group B tests: For an LTPD plan of 7% the total sample size is 115 for which the maximum number of rejects allowed is 4. Acceptance is also subject to a maximum of one (1) reject per Sub-group. Group B tests are performed on each lot for Qualification or Lot Acceptance.

[i]Pulsed through an inductor (25 mH); duty factor = 50%.

[k]Measured at a current where the breakdown voltage is a minimum.

DIMENSIONAL OUTLINE
JEDEC No.TO-5



Note *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector,
Case

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RF Power Transistors

40578

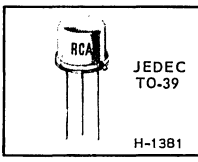
HIGH-RELIABILITY TRANSISTOR

RCA–40578* is a high-reliability variant of the RCA–2N3866, an epitaxial n-p-n planar transistor of "overlay" emitter electrode construction. It is especially processed for high reliability. It is intended for Class A, B, and C amplifier, frequency multiplier, or oscillator operation in high-reliability, driver or predriver stages, VHF-UHF applications in Space, Military, and Industrial communications equipment.

High reliability is assured by eight preconditioning steps, including drift temperature measurements after the High Temperature Reverse Bias and Power Age tests. The 40578 also features complete qualification and lot acceptance testing.

* Formerly RCA–Dev. No. TA7080

High-Gain Device for Class A,B, or C Operation in VHF-UHF Circuits



- 8 Preconditioning Steps
- Complete Qualification and Lot Acceptance Testing
- High Power Gain, Unneutralized Class C Amplifier
  At 400 MHz, 1 W output with 10 dB gain (min.)
  250 MHz, 1 W output with 15 dB gain (typ.)
  175 MHz, 1 W output with 17 dB gain (typ.)
  100 MHz, 1 W output with 20 dB gain (typ.)

RATINGS

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance (R_{BE} = 10 ohms)	V_{CER}	55	V
With base open	V_{CEO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
COLLECTOR CURRENT	I_C	0.4	A
TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 25° C		5	W
At free-air temperatures up to 25° C		1.0	W
At temperatures above 25° C		See *Fig. 1*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		–65 to 200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≧ 1/32 in. from seating plane for 10 s max.		230	°C

DISSIPATION DERATING CURVE

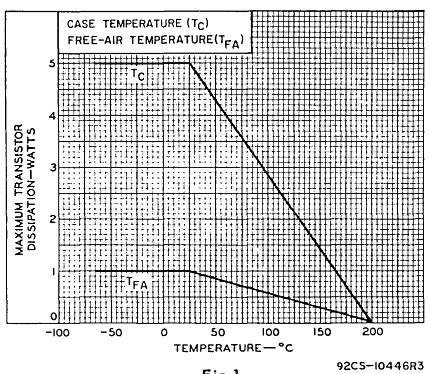


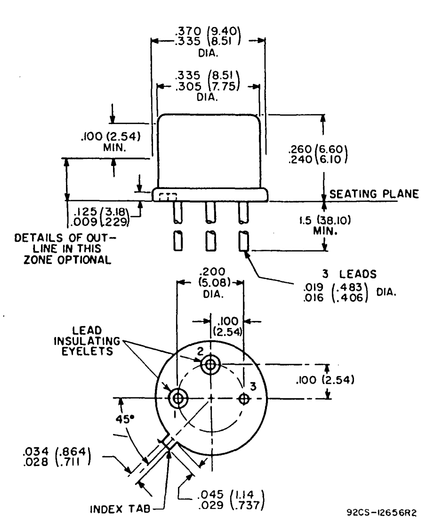
Fig.1

ELECTRICAL CHARACTERISTICS
Case Temperature = 25° C

Characteristic	Symbol	TEST CONDITIONS						LIMITS		Units
		DC Collector Volts		DC Base Volts	DC Current (mA)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-Cutoff Current	I_{CEO}		28			0		-	100	nA
Collector-to-Base Breakdown Voltage	BV_{CBO}				0		0.1	55	-	V
Collector-to-Emitter Voltage (Sustaining)	$V_{CER}(sus)^a$						5	55	-	V
	$V_{CEO}(sus)$					0	5	30	-	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}				0.1		0	3.5	-	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					20	100	-	1.0	V
Collector-to-Base Capacitance (Measured at 1 MHz)	C_{ob}	30			0			-	3.0	pF
RF Power Output Class-C Amplifier, Unneutralized At 100 MHz At 250 MHz At 400 MHz	P_{OUT}		28^b 28^b 28^b					1.8 (typ.)[c] 1.5 (typ.)[d] 1.0[e]		W
Gain-Bandwidth Product	f_T		15				50	800 (typ.)		MHz

[a]With external base-emitter resistance (R_{BE}) = 10 Ω.
[b]V_{CC} value.
[c]For P_{IN} = 0.05 W; minimum efficiency = 60%.
[d]For P_{IN} = 0.1 W; minimum efficiency = 50%.
[e]For P_{IN} = 0.1 W; minimum efficiency = 45%.

DIMENSIONAL OUTLINE
JEDEC TO-39



TERMINAL CONNECTIONS

Lead No. 1 – Emitter
Lead No. 2 – Base
Case, Lead No. 3 – Collector

DIMENSIONS IN INCHES AND MILLIMETERS

Note: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

RELIABILITY SPECIFICATIONS . . . .

In addition to Preconditioning and Group A tests, a Qualification Approval test series (Group B tests) is performed on each lot.

Preconditioning (100 Per Cent Testing of Each Transistor)

1. Serialization
2. Record I_{CEO}, h_{FE}
3. Temperature Cycling-Method 107B Cond. C of MIL-STD-202, 5 cycles, -65° C to 200° C
4. Bake, 72 hours minimum, 200° C
5. Constant Acceleration-Method 2006 of MIL-STD-750, 10,000g, Y_1 and Y_2 axes
6. X-Ray
7. Record I_{CEO}, h_{FE}
8. Reverse Bias Age, $T_A = 200^{o}$ C, $V_{CB} = 50$ V, t = 96 hours
9. [d] Record I_{CEO}, h_{FE}
10. Power Age, $T_A = 25^{o}$ C, $V_{CB} = 28$ V, t = 340 hours, $P_T = 1$ W, free air
11. [d] Record I_{CEO}, h_{FE}, V_{CE} at 340 hours
12. Helium Leak, 1×10^{-7} cc/sec. max.
13. Gross Leak, MIL-STD-202, Method 112
14. Record Subgroups 2 and 3 of Group A Tests

[d]Delta criteria after 96 hours Reverse Bias Age and 340 hours Power Age

ΔI_{CEO}	+100% or +20 nanoamperes whichever is greater
Δh_{FE}	±20%

Definitions

Delta (Δ): Delta shall be determined by subtracting the parameter value measured before application of stress from the value measured after the application of stress.

Group A Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD	SYMBOL	LIMITS Min.	LIMITS Max.	UNITS
	Subgroup 1		10				
2071	Visual and Mechanical Examination	–	–	–	–	–	–
	Subgroup 2		5				
3041D	Collector-Cutoff Current	$V_{CE} = 28$ V	–	I_{CEO}	–	100	nA
3001D	Collector-to-Base Breakdown Voltage	$I_C = 100$ µA	–	BV_{CBO}	55	–	volts
3026D	Emitter-to-Base Breakdown Voltage	$I_E = 100$ µA	–	BV_{EBO}	3.5	–	volts
3011D	Collector-to-Emitter Breakdown Voltage	$I_C = 0$ to 5 mA[f]	–	BV_{CEO}	30[g]	–	volts
3011B	Collector-to-Emitter Breakdown Voltage	$I_C = 0$ to 5 mA[f], $R_{BE} = 10\ \Omega$	–	BV_{CER}	55[g]	–	volts
3071	Collector-to-Emitter Saturation Voltage	$I_C = 100$ mA, $I_B = 20$ mA	–	$V_{CE}(sat)$	–	1	volt
3076	DC Forward-Current Transfer Ratio	$I_C = 100$ mA, $V_{CE} = 5$ V	–	h_{FE}	10	–	–
	Subgroup 3		5				
3236	Output Capacitance	$V_{CB} = 30$ V	–	C_{ob}	–	3.0	pF
3261	Extrapolated Unity Gain Frequency	$I_C = 50$ mA, $V_{CE} = 15$ V, f = 200 MHz	–	f_T	500	–	MHz
	RF Power Output (Min. Eff. = 45%)	$V_{CE} = 28$ V, $P_{IN} = .1$ W, f = 400 MHz	–	P_{OUT}	1.0	–	watts
	Subgroup 4		15				
3036D	Collector-Cutoff Current	$T_A = 150^{o}$ C ± 3° C, $V_{CB} = 30$ V	–	I_{CBO}	–	100	µA
3076	DC Forward-Current Transfer Ratio	$T_A = -55^{o}$ C ± 3° C, $I_C = 100$ mA, $V_{CE} = 5$ V	–	h_{FE}	5	–	–

[f]Pulsed through an inductor (25 µH); duty factor = 50%.
[g]Measured at a current where the breakdown voltage is a minimum.

General Reliability Specifications that are applicable to all rf power transistors are given in booklet RFT-701 and must be used in conjunction with the specific Preconditioning, Group A Tests, and Group B Tests shown below.

Group B Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS
	Subgroup 1	(13 Samples)
2066	Physical Dimensions	
	Subgroup 2	(13 Samples)
2026	Solderability	
1051	Thermal Shock (Temp. Cycling)	Test Condition C
1056	Thermal Shock (Glass Strain)	Test Condition B
2036	Terminal Strength (Tension)	Test Condition A, weight = 5 lbs. time = 15 s each terminal
	Seal (Leak Rate)	Method 112 of MIL-STD-202 Test Cond. C, procedure IIIa, Test Cond. A for gross leaks
1021	Moisture Resistance	10^{-8} cc/s
	Subgroup 3	(13 Samples)
2016	Shock	1,500 g, 0.5 ms, 5 blows each orientation: X_1, Y_1, Z_1, (15 blows total)
2046	Vibration Fatigue	Nonoperating
2056	Vibration Var. Freq.	–
2006	Constant Acceleration	20,000 G Y_1, Y_2
	Subgroup 4	(13 Samples)
2036E	Terminal Strength (Lead Fatigue)	
	Subgroup 5	(13 Samples)
1041	Salt Atmosphere	
	Subgroup 6	(25 Samples)
1031	High Temperature Life (Nonoperating)	$T_{storage}$ = 200° C
	Subgroup 7	(25 Samples)
1026	Steady-State Operation	T_{FA} = 25° C t = 1000 hrs. P_T = 1 W, V_{CB} = 28 V free air, no heat sink

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	SYMBOL	LIMITS Min.	LIMITS Max.	UNITS
	End Points Subgroups (2, 3, 5, 6, 7)					
3041D	Collector-to-Emitter Cutoff Current	V_{CE} = 28 V	I_{CEO}	–	1.0	µA
3011B	Collector-to-Emitter Breakdown Voltage	I_C = 5 mA (Inductive)[i] R_{BE} = 10	BV_{CER}	50[k]	–	volts
	RF Power Output (Min. Eff. = 45%)	V_{CE} = 28 V, P_{IN} = 0.1 W, f = 400 MHz	P_{OUT}	0.95	–	watts
3076	DC Forward-Current Transfer Ratio	I_C = 100 mA V_{CE} = 5 V	h_{FE}	9	–	–
3026D	Emitter-to-Base Breakdown Voltage	I_E = 100 mA	BV_{EBO}	3.0	–	volts

[h] Acceptance/Rejection Criteria of Group B tests: For an LTPD plan of 7% the total sample size is 115 for which the maximum number of rejects allowed is 4. Acceptance is also subject to a maximum of one (1) reject per Sub-group. Group B tests are performed on each lot for Qualification or Lot Acceptance.

[i] Pulsed through an inductor (25 mH); duty factor = 50%.

[k] Measured at a current where the breakdown voltage is a minimum.

Solid State
Division

RF Power Transistors

40605

RCA-40605* is an epitaxial silicon n-p-n planar transistor featuring "overlay" emitter electrode construction. It is intended for class-A, -B, or -C amplifier, frequency multiplier, and oscillator service in VHF/UHF equipment.

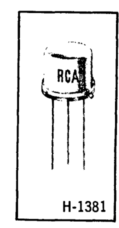
Premium high-reliability type 40605 is identical to RCA-2N3553 but is preconditioned and tested for use in critical aerospace and industrial equipment.

*Formerly RCA Dev. Type No. TA7361.

SILICON N-P-N "overlay" TRANSISTOR

"Premium" High-Reliability Type

For Class-A,-B, or -C Service in VHF/UHF Military, Industrial, and Commercial Equipment



JEDEC TO-39

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65 V
COLLECTOR-TO-EMITTER VOLTAGE:		
With -1.5 volts (V_{BE}) of reverse bias & external base-to-emitter resistance (R_{BE}) = 33 Ω	V_{CEX}	65 V
With base open	V_{CEO}	40 V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4 V
CONTINUOUS COLLECTOR CURRENT	I_C	0.33 A
PEAK COLLECTOR CURRENT	I_{Cpk}	1 A
TRANSISTOR DISSIPATION:	P_T	
At case temperatures up to 25°C		7 W
At case temperatures above 25°C derate linearly at		0.04 W/°C
At ambient temperatures up to 25°C		1 W
At ambient temperatures above 25°C derate linearly at		5.71 mW/°C
TEMPERATURE RANGE:		
Storage & Operating (Junction)		-65 to +200°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		230°C

FEATURES:

- **High Power Output**
  - **Class-C Amplifier . . .** **2.5-W (min.) at 175 MHz**
  - **Oscillator . . .** **1.5-W (typ.) at 500 MHz**

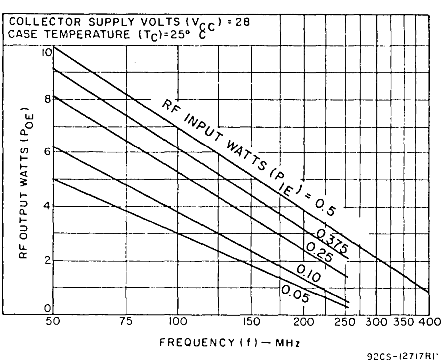


Fig.1 - Typical power output vs. frequency.

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C
STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		DC Collector Volts	DC Base Volts	DC Current mA					
		V_{CE}	V_{BE}	I_E	I_B	I_C	MIN.	MAX.	
Collector-Cutoff Current	I_{CEO}	30			0		–	0.1	μA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.3	65	–	V
Collector-to-Emitter Breakdown Voltage: *(See Fig. 2.)* With base open	$V_{(BR)CEO}$				0	200[a]	40[b]	–	V
With base-emitter junction reverse biased & external base-to-emitter resistance (R_{BE}) = 33 Ω	$V_{(BR)CEX}$		−1.5			200[a]	65[b]	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	4	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				50	250	–	1	V

[a] Pulsed through a 25-mH inductor; duty factor = 50%
[b] Measured at a current where the breakdown voltage is a minimum.

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS		UNITS
		DC Collector Supply (V_{CC}) – V	Input Power (P_{IE}) – W	Frequency (f) – MHz	MIN.	TYP.	
Power Output	P_{OE}	28	0.25	175	2.5[c]	–	W
Collector-to-Base Capacitance	C_{obo}	V_{CB} = 30 V, I_C = 0	–	1	–	10	pF
Gain-Bandwidth Product	f_T	V_{CE} = 28 V, I_C = 125 mA	–	–	350	–	MHz

[c] Minimum efficiency = 50%

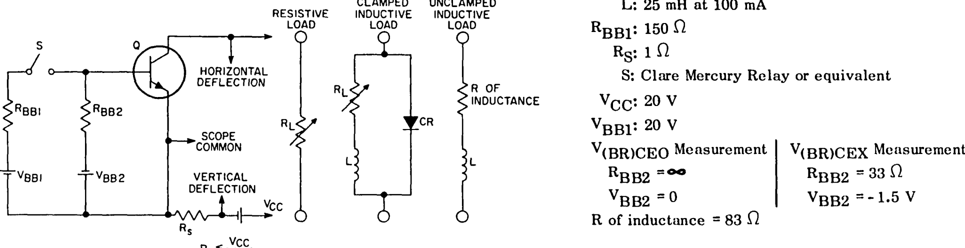


Fig.2 - Circuit used to measure voltages $V_{(BR)CEO}$ and $V_{(BR)CEX}$ (unclamped).

RELIABILITY SPECIFICATIONS . . .

General Reliability Specifications that are applicable to all rf power transistors are given in booklet RFT-701 and must be used in conjunction with the specific lot screening, Group A Tests, and Group B Tests shown below.

Lot Acceptance Data

Conditioning Screens (100% Testing, see Table I)		
a) Attributes Data on Burn-In	b) Attributes Data on Radiographic Inspection	c) Variables Data on Burn-In
Group A (Lot Sampling, see Table II)	**Group B** (Lot Sampling, see Table III)	
a) Variables Data	a) Attributes Data (From a member of the family)	

Table 1. Description of Total Lot Screening – 100% Testing

TEST	CONDITIONS	MIL-STD-750		MIL-STD-202	
		METHOD	CONDITIONS	METHOD	CONDITIONS
1. Lot identification	–	–	–	–	–
2. Pre-seal visual inspection	In accordance with RCA's RFT-701 (See note 1)	–	–	–	–
3. Temp. cycling	5 cycles	1051	C	–	–
4. High Temp. storage	72 hrs. min. at $T_A = 200^0$ C	–	–	–	–
5. Acceleration	20,000 g min.; Y_1 direction only	2006	–	–	–
6. Fine ieak	–	–	–	112	C
7. Gross leak	Fluorocarbon bubble test (See note 2)	–	–	–	–
8. Serialize	–	–	–	–	–
9. Pre burn-in electrical	See Table 1 A	–	–	–	–
10. Burn-in	(See note 3)	–	–	–	–
11. Post burn-in electrical	Delta requirements See table 1 A	–	–	–	–
12. Radiographic inspection	–	–	–	–	–

Note 1: Complete title of RFT-701 is: "General Reliability Specifications of RCA RF Power Transistors".

Note 2: Immersed in fluorochemical FC 78 at 65 psig for 4 hrs, unit is than placed in fluorochemical FC 48 at 80^0 C (nominal) and observed for bubbles.

Note 3: Burn-in tests:
Reverse bias age – all transistors shall be operated for 96 hrs at $T_A = 150^0$ C, $V_{CB} = 50$ V
Power age – all transistors shall be operated for 340 hrs at $T_A = 25^0$ C $\pm 3^0$ C, $V_{CB} = 30$ V, $P_T = 1$ W.

Table 1 A. Pre Burn-In & Post Burn-In Tests and Delta (Δ) Limits

TEST	SYMBOL	MIL-STD-750		LIMITS		UNITS
		METHOD	CONDITIONS	MIN.	MAX.	
Collector-Cutoff Current	I_{CEO}	3041	V_{CE} = 30 V, bias cond. D	–	0.1	μA
DC Forward-Current Transfer Ratio	h_{FE}	3076	V_{CE} = 5 V, I_C = 150 mA pulsed	15	150	—

Delta (Δ) Limits:

I_{CEO} and h_{FE} of Table 1A shall be retested after each burn-in test and the data recorded for all devices in the lot. The tests measured shall not have changed during each burn-in test from the initial value by more than the specified amount as follows:

ΔI_{CEO} = ± 100% or 10 nA, whichever is greater
Δh_{FE} = ± 20%

All transistors that exceed the delta (Δ) limits or the limits of Table 1A after each burn-in test shall be removed from the lot and the quantity removed shall be recorded in the lot history.

Table II. Group A Electrical Sampling Inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD	SYMBOL	LIMITS		UNITS
	METHOD	CONDITIONS			MIN.	MAX.	
Subgroup 1			10				
Visual and Mechanical Examination	2071	–	–	–	–	–	–
Subgroup 2			5				
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	100	nA
Collector-to-Base Breakdown Voltage	3001D	I_C = 0.3 mA	–	$V_{(BR)CBO}$	65	–	V
Emitter-to-Base Breakdown Voltage	3026D	I_E = 0.1 mA	–	$V_{(BR)EBO}$	4	–	V
Collector-to-Emitter Breakdown Voltage	3011D See Fig. 2.	I_C = 200 mA[a]	–	$V_{(BR)CEO}$	40[b]	–	V
Collector-to-Emitter Breakdown Voltage	3011B See Fig. 2.	I_C = 200 mA[a], V_{BE} = -1.5 V, R_{BE} = 33 Ω	–	$V_{(BR)CEX}$	65[b]	–	V
Collector-to-Emitter Saturation Voltage	3071	I_C = 250 mA, I_B = 50 mA	–	V_{CE} (sat)	–	1	V
DC Forward-Current Transfer Ratio	3076	I_C = 150 mA, V_{CE} = 5 V	–	h_{FE}	15	150	–
Subgroup 3			5				
Output Capacitance	3236	V_{CB} = 30 V, I_C = 0	–	C_{obo}	–	10	pF
Extrapolated Unity Gain Frequency	3261	I_C = 125 mA, V_{CE} = 28 V, f = 100 MHz	–	f_T	350	–	MHz
RF Power Output (Min. Eff. = 50%)	See Fig. 3.	V_{CE} = 28 V, P_{IE} = 0.25 W, f = 175 MHz	–	P_{OE}	2.5	–	W
Subgroup 4			15				
Collector-Cutoff Current	3036D	T_A = 150° C ± 3° C, V_{CB} = 30 V	–	I_{CBO}	–	100	μA
DC Forward-Current Transfer Ratio	3076	T_A = -55° C ± 3° C, I_C = 150 mA, V_{CE} = 5 V	–	h_{FE}	10	–	–

[a] Pulsed through a 25 mH inductor; duty factor = 50%

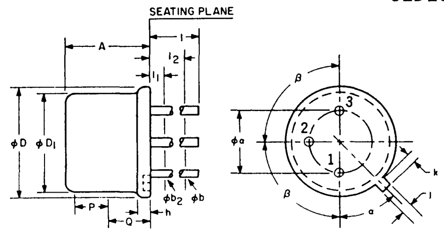
[b] Measured at a current where the breakdown voltage is a minimum

Table III. Group B Environmental Sampling Inspection

EXAMINATION OR TEST	MIL-STD-750 METHOD	MIL-STD-750 CONDITIONS	LTPD	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
Subgroup 1			20				
Physical Dimensions	2066	–		–	–	–	–
Subgroup 2			15				
Solderability	2026	–		–	–	–	–
Thermal Shock (Temp. Cycling)	1051	Test Condition C		–	–	–	–
Thermal Shock (Glass Strain)	1056	Test Condition B		–	–	–	–
Seal (Leak Rate)	–	Method 112 of MIL-STD-202 Test Cond. C, procedure III a		–	–	1×10^{-7}	atmcc/s
		For Gross Leaks, Refer to Note 1 in Lot Screening sequence		–	–	–	–
Moisture Resistance	1021	–		–	–	–	–
End Points:							
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0		I_{CEO}	–	100	nA
Collector-to-Emitter Breakdown Voltage	3011D See Fig. 2.	I_C = 200 mA[a]		$V_{(BR)CEO}$	40	–	V
DC Forward-Current Transfer Ratio	3076	I_C = 150 mA, V_{CE} = 5 V		h_{FE}	12	–	–
RF Power Output (Min. Eff = 50%)	See Fig. 3	V_{CE} = 28 V, P_{IE} = 0.25 W, f = 175 MHz		P_{OE}	2.5	–	W
Subgroup 3			15				
Shock	2016	1,500 g, 0.5 ms, 5 blows each orientation: X_1, Y_1, Z_1, Y_2,(15 blows total)		–	–	–	–
Vibration Fatigue	2046	Nonoperating		–	–	–	–
Vibration, Variable Frequency	2056	–		–	–	–	–
Constant Acceleration	2006	20,000 g Y_1, Y_2		–	–	–	–
End Points: (Same as Subgroup 2)							
Subgroup 4			15				
Terminal Strength (Lead Fatigue)	2036E	–		–	–	–	–
Subgroup 5			15				
Salt Atmosphere	1041	–		–	–	–	–
Subgroup 6							
High Temperature Life (Nonoperating)		T_{stg} = + 200° C, t = 1000 hrs.	–	–	–	–	–
End Points:							
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	1	μA
Collector-to-Emitter Breakdown Voltage	3011D See Fig. 2.	I_C = 200 mA[a]	–	$V_{(BR)CEO}$	40	–	V
DC Forward-Current Transfer Ratio	3076	I_C = 150 mA, V_{CE} = 5 V	–	h_{FE}	12	–	–
RF Power Output (Min. Eff. = 50%)	See Fig. 3	V_{CE} = 28 V, P_{IE} = 0.25 W, f = 175 MHz	–	P_{OE}	2.3	–	W

[a] Pulsed through a 25 μH inductor; duty factor = 50%

DIMENSIONAL OUTLINE
JEDEC No.TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	.190	.210	4.83	5.33	
A	.240	.260	6.10	6.60	
ϕb	.016	.021	.406	.533	2
ϕb_2	.016	.019	.406	.483	2
ϕD	.350	.370	8.89	9.40	
ϕD_1	.315	.335	8.00	8.51	
h	.009	.125	.229	3.18	
j	.028	.034	.711	.864	
k	.029	.040	.737	1.02	3
l	.500		12.70		2
l_1		.050		1.27	2
l_2	.250		6.35		2
P	.100		2.54		1
Q					4
α	45^0 NOMINAL				
β	90^0 NOMINAL				

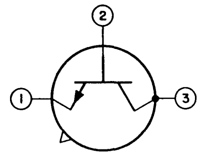
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010 in (.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and .5 in (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond .5 in (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL DIAGRAM

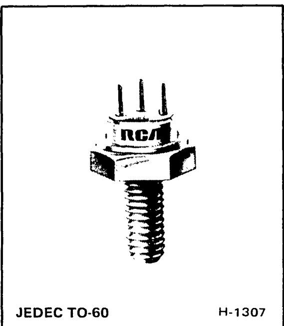


LEAD 1 – EMITTER
LEAD 2 – BASE
CASE, LEAD 3 – COLLECTOR

Solid State
Division

RF Power Transistors

40606



JEDEC TO-60 H-1307

High-Reliability Silicon N-P-N Overlay Transistor

For Large-Signal, High-Power VHF/UHF Applications in Military and Industrial Communications Equipment

Features:

- **High power output, unneutralized class C amplifier**
- **High voltage ratings**
- **100 per cent tested to assure freedom from second breakdown for operation in class A applications**
- **All three electrodes electrically isolated from case for design flexibility**

RCA-40606 is an epitaxial silicon n-p-n planar transistor. This device is intended for class A, B, C amplifier, frequency multiplier, or oscillator operation. The device was developed for vhf/uhf applications.

The transistor employs the overlay concept in emitter-electrode design — an emitter electrode consisting of many microscopic areas connected together through the use of a diffused-grid structure and an overlay of metal which is applied on the silicon wafer by means of a photo-etching technique. This arrangement provides the very high emitter periphery-to-emitter area ratio required for high efficiency at high frequencies.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base-emitter junction reverse-biased (V_{BE} = -1.5 V)	V_{CEV}	65	V
With base open	V_{CEO}	40	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
COLLECTOR CURRENT	I_C	3	A
TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 25°C		23	W
At case temperatures above 25°C		Derate linearly to 0 watts at 200°C	
TEMPERATURE RANGE:			
Storage and operating (junction)		-65 to 200	°C
TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. (0.8 mm) from insulating wafer for 10 s max.		230	°C

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C

Characteristic	Symbol	TEST CONDITIONS						LIMITS		Units
		DC Collector Volts		DC Base Volts	DC Current (Milliamperes)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-Cutoff Current	I_{CEO}		30			0		–	0.25	mA
Collector-to-Base Breakdown Voltage	BV_{CBO}				0		0.5	65	–	volts
Collector-to-Emitter Breakdown Voltage	BV_{CEO}					0	0 to 200*	40**	–	volts
	BV_{CEV}			−1.5			0 to 200*	65**	–	volts
Emitter-to-Base Breakdown Voltage	BV_{EBO}				0.25		0	4	–	volts
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					100	500	–	1	volt
Collector-to-Base Capacitance Measured at 1 MHz	C_{ob}	30			0			–	20	pF
RF Power Output Amplifier, Unneutralized At 260 MHz 400 MHz	P_{OE}		V_{CC} = 28 28					14.5• (typ.) 10▲	–	watts
Gain-Bandwidth Product	f_T		28				150	400 (typ.)		MHz
Base-Spreading Resistance Measured at 200 MHz	$r_{bb'}$		28				250	6.5 (typ.)		ohms
Collector-to-Case Capacitance	C_s							–	6	pF
DC Forward-Current Transfer Ratio	h_{FE}		5				300	10	–	
Second-Breakdown Collector Current[a] (Base forward-biased)	$I_{S/b}$		28					0.33	–	A

* Pulsed through an inductor (25 mh); duty factor = 50%.
** Measured at a current where the breakdown voltage is a minimum.
• For P_{IE} = 4.0 w; minimum efficiency = 60%.
▲ For P_{IE} = 4.0 w; minimum efficiency = 45%.
a Pulse duration = 1 s.

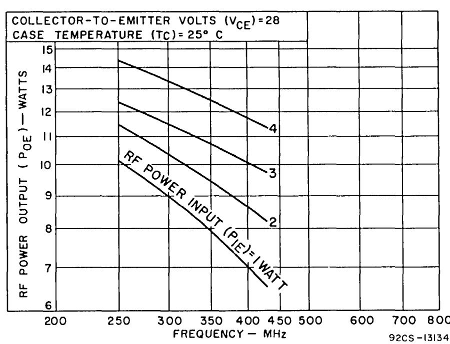


Fig. 1—Power output vs. frequency.

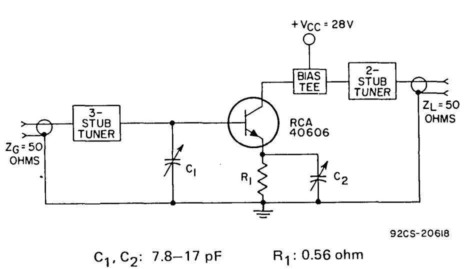


Fig. 2—RF amplifier circuit for power-output test at 400 MHz.

RELIABILITY SPECIFICATIONS:

Lot Acceptance Data

Conditioning Screens (100% Testing, see Table I) (a) Attributes Data on Burn-In	(b) Attributes Data on Radiographic Inspection	(c) Variables Data on Burn-In
Group A (Lot Sampling, see Table II) (a) Variables Data		**Group B** (Lot Sampling, see Table III) (a) Attributes Data (From a member of the family)

Table 1. Description of Total Lot Screening — 100% Testing

TEST	CONDITIONS	MIL-STD-750		LIMITS		UNITS
		METHOD	CONDITIONS	MIN.	MAX.	
1. Read: Collector-to-Emitter Current DC Forward-Current Transfer Ratio	 V_{CE} = 30 V, I_B = 0 I_C = 300 mA, V_{CE} = 5 V	 – –	 – –	 – 10	 250 –	 nA
2. Temp. Cycling	5 cycles, –65°C to +200°C	1051C	–	–	–	
3. High-Temp. Storage	T_A = 200°C, t = 72 hrs.	–	–	–	–	
4. Acceleration	20,000 g; Y_1, Y_2	2006	–	–	–	
5. Helium Leak		–	–	–	–	
6. Gross Leak	Ethylene Glycol, Temp. = 150°C, t = 15 s min.	–	–	–	–	
7. Serialization		–	–	–	–	
8. Radiographic Inspection		–	–	–	–	
9. Read and Record: Collector-to-Emitter Current DC Forward-Current Transfer Ratio	 V_{CE} = 30 V, I_B = 0 I_C = 300 mA, V_{CE} = 5 V	 – –	 – –	 – 10	 250 –	 nA
10. Reverse-Bias Age	T_A = 150°C, V_{CB} = 50 V, t = 96 hrs.	–	–	–	–	
11. Read and Record Reverse-Bias End Points	See Table 1A.	–	–	–	–	
12. Power Age	T_A = 25°C, V_{CB} = 30 V, t = 340 hrs. P_D = 2.6 W free air Interim down period = 168 hrs.	–	–	–	–	
13. Read and Record Power-Age End Points	See Table 1A.	–	–	–	–	
14. Read and Record Subgroups 2, 3 of Group A; Sample Subgroup 4 of Group A		–	–	–	–	

Table 1A. Power Age and Reverse-Bias Age

TEST	SYMBOL	MIL-STD-750		LIMITS		UNITS
		METHOD	CONDITIONS	MIN.	MAX.	
Collector-Cutoff Current	I_{CEO}	3041	V_{CE} = 30 V, I_B = 0	–	250	nA
DC Forward-Current Transfer Ratio	h_{FE}	3076	V_{CE} = 5 V, I_C = 300 mA pulsed	10	–	–

Delta (Δ) Limits:

I_{CEO} and h_{FE} of Table 1A shall be retested after each burn-in test and the data recorded for all devices in the lot. The tests measured shall not have changed during each burn-in test from the initial value by more than the specified amount as follows:

ΔI_{CEO} = ± 100% or 25 nA, whichever is greater

Δh_{FE} = ± 20%

All transistors that exceed the delta (Δ) limits or the limits of Table 1A after each burn-in test shall be removed from the lot and the quantity removed shall be recorded in the lot history.

Table II. Group A Electrical Sampling Inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD	SYMBOL	LIMITS		UNITS
	METHOD	CONDITIONS			MIN.	MAX.	
Subgroup 1			10				
Visual and Mechanical Examination	2071	–	–	–	–	–	–
Subgroup 2			5				
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	250	nA
Collector-to-Base Breakdown Voltage	3001D	I_C = 0.5 mA, I_E = 0	–	$V_{(BR)CBO}$	65	–	V
Emitter-to-Base Breakdown Voltage	3026D	I_E = 0.25 mA, I_C = 0	–	$V_{(BR)EBO}$	4	–	V
Collector-to-Emitter Breakdown Voltage	3011D	I_C = 200 mA[a], I_B = 0	–	$V_{(BR)CEO}$	40[b]	–	V
Collector-to-Emitter Breakdown Voltage	3011A	I_C = 200 mA[a], V_{BE} = -1.5 V, R_{BE} = 33 Ω	–	$V_{(BR)CEV}$	65[b]	–	V
Collector-to-Emitter Saturation Voltage	3071	I_C = 500 mA, I_B = 100 mA	–	V_{CE} (sat)	–	1	V
DC Forward-Current Transfer Ratio	3076	I_C = 300 mA, V_{CE} = 5 V	–	h_{FE}	10	–	–
Second Breakdown Collector Current	–	V_{CE} = 28 V, t = 1 s pulse	–	$I_{S/b}$	0.33	–	A
Subgroup 3			5				
Output Capacitance	3236	V_{CB} = 30 V, I_B = 0	–	C_{obo}	–	20	pF
Common-Emitter, Small-Signal Short Circuit Forward Current Transfer Ratio	–	I_C = 250 mA, V_{CE} = 28 V, f = 100 MHz	–	h_{fe}	2.4	–	–
RF Power Output (Min. Eff. = 45%)	See Fig. 3.	V_{CE} = 28 V, P_{IE} = 4 W, f = 400 MHz	–	P_{OE}	10	–	W
Subgroup 4			15				
Collector-Cutoff Current	3036D	T_A = 150° C ± 3° C, V_{CE} = 30 V	–	I_{CBO}	–	250	μA
DC Forward-Current Transfer Ratio	3076	T_A = -55° C ± 3° C, I_C = 300 mA, V_{CE} = 5 V	–	h_{FE}	10	–	–

[a] Pulsed through a 25 mH inductor; duty factor = 50%

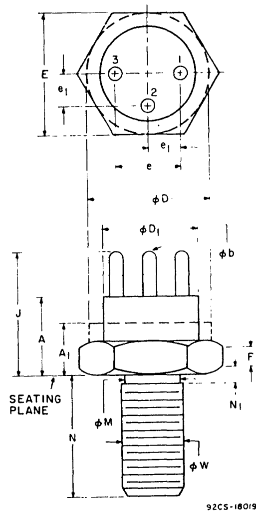
[b] Measured at a current where the breakdown voltage is a minimum

Table III. Group B Environmental Sampling Inspection

EXAMINATION OR TEST	MIL-STD-750 METHOD	MIL-STD-750 CONDITIONS	LTPD	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
Subgroup 1			20				
Physical Dimensions	2066	–		–	–	–	–
Subgroup 2			15				
Solderability	2026	–		–	–	–	–
Thermal Shock (Temp. Cycling)	1051	5 cycles −65°C to +200°C		–	–	–	–
Seal (Leak Rate)	1071			–	–	1×10^{-7}	atm cc/s
Terminal Strength	2036			–	–	–	–
Moisture Resistance	1021	–		–	–	–	–
End Points:							
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0		I_{CEO}	–	250	nA
Collector-to-Emitter Breakdown Voltage	3011D	I_C = 200 mA[a], I_B = 0		$V_{(BR)CEO}$	40	–	V
DC Forward-Current Transfer Ratio	3076	I_C = 300 mA, V_{CE} = 5 V		h_{FE}	10	–	–
RF Power Output (Min. Eff = 45%)	See Fig. 3	V_{CE} = 28 V, P_{IE} = 4 W, f = 400 MHz		P_{OE}	10	–	W
Subgroup 3			15				
Shock	2016	500 g, 1.0 ms, 5 blows each orientation: X_1, Y_1, Z_1, Y_2, (20 blows total)		–	–	–	–
Vibration Fatigue	2046	Nonoperating		–	–	–	–
Vibration, Variable Frequency	2056	–		–	–	–	–
Constant Acceleration	2006	20,000 g Y_1, Y_2		–	–	–	–
End Points: (Same as Subgroup 2)							
Subgroup 6							
High Temperature Life (Nonoperating)	1031	T_{stg} = + 200° C, t = 1000 hrs.	–	–	–	–	–
End Points:							
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	2.5	μA
Collector-to-Emitter Breakdown Voltage	3011D	I_C = 200 mA[a], I_B = 0	–	$V_{(BR)CEO}$	40	–	V
DC Forward-Current Transfer Ratio	3076	I_C = 300 mA, V_{CE} = 5 V	–	h_{FE}	9	–	–
RF Power Output (Min. Eff. = 45%)		V_{CE} = 28 V, P_{IE} = 4 W, f = 400 MHz	–	P_{OE}	10	–	W
Subgroup 7							
Operating Life							
Steady-State DC	1026	V_{CB} = 28 V, P_D = 4 W, T_A = 170°C	–	–	–	–	
End Points: (Same as Subgroup 6)							

[a] Pulsed through a 25 μH inductor; duty factor = 50%

DIMENSIONAL OUTLINE JEDEC TO-60



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.215	0.320	5.46	8.13	
A_1	–	0.165	–	4.19	2
ϕb	0.030	0.046	0.762	1.17	4
ϕD	0.360	0.437	9.14	11.10	2
ϕD_1	0.320	0.360	8.13	9.14	
E	0.424	0.437	10.77	11.10	
e	0.185	0.215	4.70	5.46	
e_1	0.090	0.110	2.29	2.79	
F	0.090	0.135	2.29	3.43	1
J	0.355	0.480	9.02	12.19	
ϕM	0.163	0.189	4.14	4.80	
N	0.375	0.455	9.53	11.56	
N_1	–	0.078	–	1.98	
ϕW	0.1658	0.1697	4.212	4.310	3, 5

NOTES:

1. Dimension does not include sealing flanges
2. Package contour optional within dimensions specified
3. Pitch diameter – 10-32 UNF 2A thread (coated)
4. Pin spacing perimts insertion in any socket having a pin-circle diameter of 0.200 in. (5.08 mm) and contacts which will accommodate pins with a diameter of 0.030 in. (0.762 mm) min., 0.046 in. (1.17 mm) max.
5. The torque applied to a 10-32 hex nut assembled on the thread during installation should not exceed 12 inch-pounds.

TERMINAL CONNECTIONS

Mounting Stud, Case, Pin No. 1 – Emitter
Pin No. 2 – Base
Pin No. 3 – Collector

Solid State Division

RF Power Transistors

Application Note AN-6229

Microwave Power-Transistor Reliability as a Function of Current Density and Junction Temperature

by S. Gottesfeld

Questions concerning the effect of electromigration-related failure modes on the life of microwave power transistors using an aluminum metallization system are frequently asked. This Note answers these questions as they pertain to RCA microwave power transistors. First, the design aspects of these transistors which aid in reducing the incidence of electromigration failure to a negligible level under normal operating conditions are discussed. Second, supporting life-test data on commercial-level RCA microwave power transistors is presented. The lifetime of the products in this line can be predicted from the data as a function of current density and junction temperature – the two main factors involved in electromigration failure modes.

Electromigration

Electromigration of the aluminum in the presence of high-current densities and elevated temperatures is well known[1] and results from the mass transport of metal by momentum exchange between thermally activated metal ions and conducting electrons. As a consequence, the original uniform aluminum film reconstructs to form thin conductor regions and extruded-appearing hillocks that may cause device degradation.

The electromigration process can be accompanied by the dissolution of silicon into the aluminum. This dissolution usually occurs during heat treatments employed in transistor manufacturing until the aluminum-silicon saturation point is reached. Therefore, little silicon can dissolve when the device is in *normal* operation. At high-current densities and elevated temperatures, however, the silicon ions which were diffused into the aluminum during the manufacturing process can be transported along with the aluminum ions undergoing electromigration away from the silicon-aluminum interface and into the aluminum. This situation allows further diffusion of silicon into the aluminum and leads to the eventual failure of the transistor junctions[2].

RELIABILITY DESIGN FEATURES

Overlay-Transistor Construction

The basic transistor construction used by RCA for rf power transistors is the "overlay" design. The emitters in this type of device are separated into many discrete sites which are paralleled for high-power performance. The overlay configuration provides the high ratio of effective emitter periphery to base area[3] needed for high-power generation at microwave frequencies. In addition, this structure has the advantage of permitting lower current densities in the emitter metallizing stripes than other high-frequency structures. This advantage results from the relatively broad emitter-metal stripes which interconnect the discrete emitters. These stripes are typically 35 microns wide compared to 3 to 5 microns for other interdigitated or matrix designs. Furthermore, the separation of the emitter- and base-metal fingers is 3 to 4 times greater in the overlay structure than competitive structures. This separation permits the deposition of thicker metal layers with greater cross-sectional areas; and further reduces current densities.

Polycrystalline Silicon Layer (PSL)

Another advantage of the overlay transistor structure with its broad emitter fingers and non-critical metal-definition is that it is readily adaptable to the introduction of additional conducting and insulating layers between the aluminum metallization and the shallow diffused emitter sites required for microwave performance. RCA has developed a polycrystalline silicon layer (PSL), shown in Fig.1, which is deposited over the emitter sites and under the aluminum metallization. The PSL forms a barrier between the aluminum emitter finger and the oxide insulating layer over the base; the barrier minimizes failures caused by the interaction of aluminum with silicon dioxide. In addition, the PSL layer helps to minimize thermally induced failure modes by providing a barrier between the aluminum and the shallow-emitter diffused region to prevent "alloy spike" failures; PSL also increases the distance that the silicon ions must travel from emitter-site region to metallization, Fig.1. Therefore, the amount of silicon that can be diffused into the aluminum is limited, and the possibility of device failure as a result of the electromigration of the silicon in the aluminum is reduced.

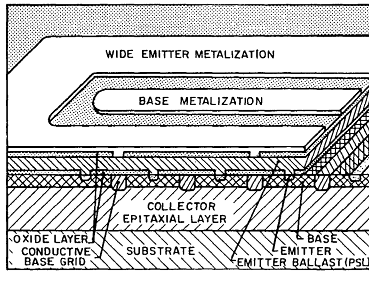


Fig.1 — Cross section of an overlay transistor showing the polysilicon layer (PSL) between the metallization and emitter sites, and how emitter ballasting may be placed in series with each emitter site by controlling the doping and contacting geometry of the PSL.

Emitter-Site Ballasting

RCA has utilized the PSL technology as a medium to introduce emitter-site ballasting into its microwave power transistors. Emitter-site ballasting permits more uniform injection across the transistor chips by reducing hot-spotting. By controlling the resistivity of the PSL and restricting the contacting geometry of the aluminum to the PSL layer, a ballast resistor is placed in series with each emitter site, as shown in Fig.1. These resistors function as negative-feedback elements to control that portion of the transistor that is drawing excessive current. Since the overlay construction results in an emitter that is segmented into many sites which are connected in parallel, each hot-spot may be isolated and controlled. Furthermore, the large number of resistors in parallel minimize the effects of excessive emitter resistance on input impedance and gain. In fact, one microwave transistor, the type 2N5921, which had low levels of emitter-site ballasting added to its structure, exhibited a 35-percent improvement in power output for the same drive level. At the same time, the measurement of the dc safe-operating area, as defined by a 200°C hot-spot junction temperature (infrared measurement), indicated an approximate doubling of the allowable current at 15 volts (see Fig.2).

It is also known that hot-spotting under rf conditions increases as the VSWR increases[4]. Device failures which occur under high VSWR conditions at the output are often related to a forward-bias second-breakdown failure mechanism which is characterized by extremely high localized currents. Thus, it could be expected that an emitter-ballasted transistor would have greater resistance to failure under high VSWR conditions, such as those encountered in some broadband amplifiers. In fact, the 2-gigahertz power transistors which are site-ballasted, types 2N6265 and 2N6266, have been characterized for their ability to withstand ∞:1 VSWR at all phases at rated power; the 2N6267 has been characterized at a 10:1 VSWR. The 3-gigahertz chain of microwave power devices are also site-ballasted, and are also rated at a 10:1 VSWR capacity.

Glass-Passivated-Aluminum Metallization

The standard metallization system used on all commercial RCA microwave power transistors consists of an evaporated aluminum-silicon film which is defined by means of photolithographic and chemical-etching techniques. The addition of silicon to the aluminum brings the state of the metallization closer to the aluminum-silicon saturation point and retards the electromigration of silicon into the aluminum. Aluminum electromigration is also significantly retarded by the deposition of a glass passivation layer over the aluminum film subsequent to the definition procedures. It has been shown[1] that the use of glass passivation results in a 40-percent increase in the activation energy required before electromigration can begin. The silicon-dioxide layer also protects the aluminum from contamination and from scratches or smears that may occur during device assembly.

OPERATING-LIFE-TEST PROGRAM

Test Conditions

An accelerated operating-life-test program was undertaken to study the effects of electromigration at various current densities on the lifetime of RCA microwave power transistors. DC current-voltage conditions were used since electromigration is responsive to the dc components of the total waveform used in rf applications, i.e., electromigration is effected by the unidirectional components of the field. Tests were run at three different emitter-stripe current densities (J_E) with each current density in turn run at three different peak junction temperatures (T_j); all tests represented stress levels above normal-

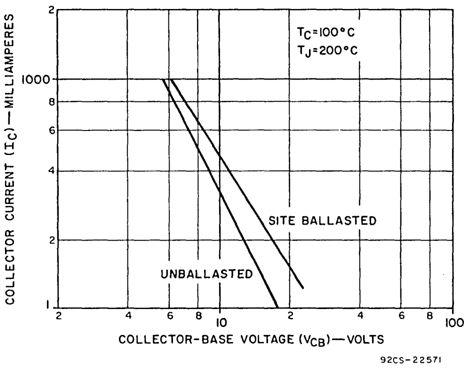


Fig.2 — DC infrared safe-area for ballasted and unballasted microwave transistor (2N5921 coaxial packaged).

use conditions. Peak junction temperature was determined by infrared scanning of the transistor pellet at each life-test condition. Table I shows the matrix of test conditions. The sample size per test condition ranged between 10 and 15 units. A total of 114 units were tested.

TABLE I – ACCELERATED LIFE-TEST CONDITIONS

Collector Current (Amperes)	Emitter Current (Amperes)	Emitter Stripe Current Density (A/cm^2)	Peak Junction Temperature* (°C) T_j1	T_j2	T_j3
1	1.02	8.5×10^4	300	280	254
2	2.07	1.7×10^5	283	258	230
3	3.22	2.7×10^5	300	273	240

* Represents peak temperature as averaged over several devices at each life-test condition. External heat-sink size was adjusted to achieve the differences in junction temperature on the life test.

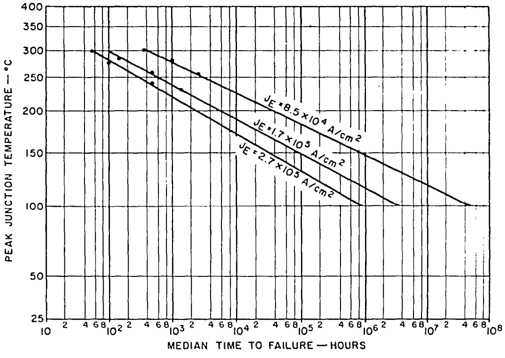


Fig.3 – Arrhenius plot showing extrapolation to lower temperatures from the life-test MTF points for the 2N6267.

Test Vehicle

A type 2N6267 device manufactured by RCA was used as the test vehicle because it operates at one of the highest current densities in the microwave family. This device incorporates all the design features described in the prior sections of this Note, and is considered representitive of the microwave family. All the transistors used on test were commercial-level devices, i.e., they were not subjected to conventional hi-rel screening prior to life testing.

Failure Mode

The accelerated test conditions produced failures due to electromigration of aluminum and silicon as described in the introductory section. The failure indicator was degraded or shorted transistor junctions. RF power output measured at frequent life-test down-periods prior to device junction failure exhibited only slight degradation (typically 8 percent); this performance is excellent considering the severity of the test conditions.

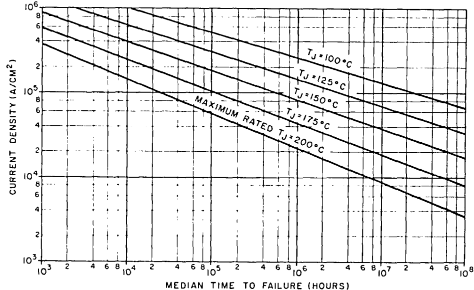


Fig.4 – MTF as a function of current density and junction temperature. In applying this chart, it is recommended that no device be used above its maximum ratings as specified in the published data sheet.

Data

An Arrhenius plot (1/T, log scale) of the log-normal median-time-to-failure (MTF) obtained from each test is shown in Fig.3. The curves are extrapolated down from the data points to enable prediction of MTF at operating junction temperatures below the maximum rated 200°C. An estimated MTF of 9.5×10^5 hours (or greater than 100 years) is predicted for the 2N6267 device under test at its typical-application current density of 8.5×10^4 A/cm^2 and junction temperature of 150°C.

Points from each curve in the Arrhenius plot were taken in the temperature range of 200°C to 100°C and replotted on a log-log scale, Fig.4, for extrapolation over various current densities. Fig.4 shows the general plot of MTF as a function of emitter-current density and peak-junction temperature. This chart can be used to estimate the MTF for each microwave transistor at its typical operating-current density. Table II lists the transistor types currently in the microwave family, and shows the predicted MTF for typical-application values of emitter current, emitter-stripe current density, and peak junction temperature.

TABLE II – ESTIMATED MTF FOR MICROWAVE FAMILY AT TYPICAL APPLICATION CURRENT DENSITIES

Package	Operating Frequency (GHz)	Type	Typical Operating Conditions I_E (Amperes)	J_E (10^4 A/cm^2)	Estimated MTF (10^6 hours) @ T_j = 150°C
HF-11 Coaxial	1	2N5470	0.119	5.2	4.0
	2	2N5920	0.180	5.5	3.5
HF-21 Coaxial	2	2N5921	0.450	3.5	12.0
HF-28 Stripline	2	2N6265	0.215	6.5	2.0
	2	2N6266	0.540	4.2	7.0
	2	2N6267	1.02	8.5	0.95
	2.3	2N6268	0.275	8.3	1.0
	2.3	2N6269	0.920	7.2	1.5
HF-46 Stripline	2	RCA2003	0.300	9.0	0.80
	2	RCA2005	0.540	4.2	7.0
	2	RCA2010	1.02	8.5	0.95
	3	RCA3001	0.120	3.8	10.0
	3	RCA3003	0.300	9.0	0.80
	3	RCA3005	0.540	8.0	1.1

CONCLUSIONS

The life-test data presented in this Note shows that the design features of RCA microwave-power transistors assure reliable operation at the current densities and junction temperatures normally encountered in typical applications. Under these operating conditions, the lifetime of these devices in terms of failure due to electromigration is estimated at approximately 100 years.

ACKNOWLEDGMENT

The author acknowledges the assistance of D. S. Jacobson in providing information concerning the transistor design descriptions, C. B. Leuthauser in providing microwave-transistor application information, and L. J. Gallace for his comments regarding the reliability aspects of this Application Note.

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2. J. R. Black,"RF Power Transistor Metallization Failure," IEEE Trans. Electron Devices, Vol. ED-17, No. 9, pp. 800–803, September 1970.
3. D. S. Jacobson, "What are the Trade-Offs in RF Transistor Design?," Microwaves, Vol. 11, No.7, July 1972.
4. C. B. Leuthauser,"Hotspotting in RF Power Transistors," RCA Application Note AN-4774.

Solid State Division

Power Hybrid Circuits
High-Reliability Slash (/) Series HC2000H/ . . .

Metal Hermetic Package

H-1777

High-Reliability Multi-Purpose 7-Ampere Operational Amplifier

For Aerospace, Military, and Critical Industrial Applications

Features:

- 30-kHz bandwidth at 60 W
- High output power: up to 100 W (rms)
- High output current: 7 A (peak)
- Built-in load-line limiting to protect amplifier from short-circuit at output terminals
- Stability with resistive or reactive loads
- Reactive-load fault protection
- Single or split power supply (30 to 75 V, total)
- Provision for feedback control
- Direct coupling to load
- Class B output stage
- Rugged package with heavy leads
- Light weight: 100 grams
- Low crossover distortion

The RCA-HC2000H "Slash" (/) Series types are complete solid-state hybrid operational amplifiers in metal hermetic packages, especially designed for critical applications in aerospace, military, and industrial equipment. These types are electrically and mechanically interchangeable with the RCA-HC2000H, but are specially processed and tested to meet the aerospace and military electrical, environmental, and physical test methods and procedures established for microelectronic devices in MIL-STD-883.

These units can be supplied to four screening levels; the number following the slash (/) mark in the type designation, e.g. HC2000H/1, indicates the screening level employed by RCA to achieve the quality and reliability commensurate with the intended application. A description of these levels (/1, /2, /3, and /4) is given in Table 1.

Types HC2000H/. . . employ a quasi-complementary-symmetry class B output circuit with built-in load-fault protection and hometaxial output transistors. They can be operated from single or split power supplies.

These amplifiers are recommended for the following applications: servo amplifiers (ac, dc, PWM); deflection amplifiers; power operational amplifiers; audio amplifiers; voltage regulators; and driven inverters.

- Examinations and tests performed in accordance with MIL-STD-883, "Test Methods and Procedures for Microelectronics"
- Total Lot Screening (100% testing) "Group A" (electrical) and "Group B" (environmental) sampling test program
- Choice of 4 distinct screening levels
- Internal visual (precap) inspection performed on all 4 screening levels in accordance with Method 2017 of MIL-STD-883

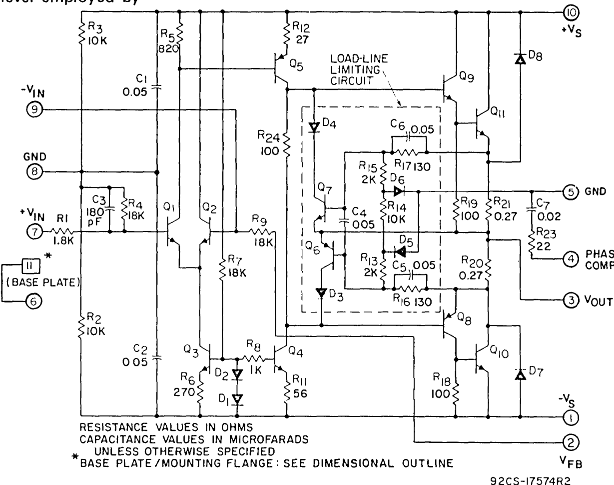


Fig. 1—Schematic diagram of type HC2000H/. . . power hybrid circuit operational amplifier.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE:
Between leads 1 & 10 . . . . . 75 V
OUTPUT CURRENT (PEAK) . . . . . 7 A
TOTAL DISSIPATION:
Per Output Device . . . . . See Fig. 2 & 3
TEMPERATURE RANGE:
Storage . . . . . −55 to +125°C
Output-Transistor Junction . . . . . −55 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance ⩾ 1/8 in. (3.17 mm) from case for 10 s max. . . . . . 235°C
LEAD-BENDING RADIUS (MIN.)
At distance ⩾ 0.075 (1.91 mm) from case . . . . . 0.04 in. (1.02 mm)

Table 1 — Descriptions of RCA Screening Levels

RCA Level	Approximates MIL-STD-883	Application	Description
/1	Class A with Condition B Precap Visual Inspection	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **impossible and reliability is imperative**
/2	Class A with Condition B Precap Visual Inspection. Centrifuge and Radiographic Inspection Omitted	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **extremely difficult or impossible and reliability is imperative**
/3	Class B	Military and Industrial; For example, in Airborne Electronics	For devices intended for use where maintenance and replacement **can be performed but are difficult and expensive**
/4	Class C	Military and Industrial; For example, in Ground-Based Electronics	For devices intended for use where replacement **can readily be accomplished**

Total Lot Screening Flow Chart

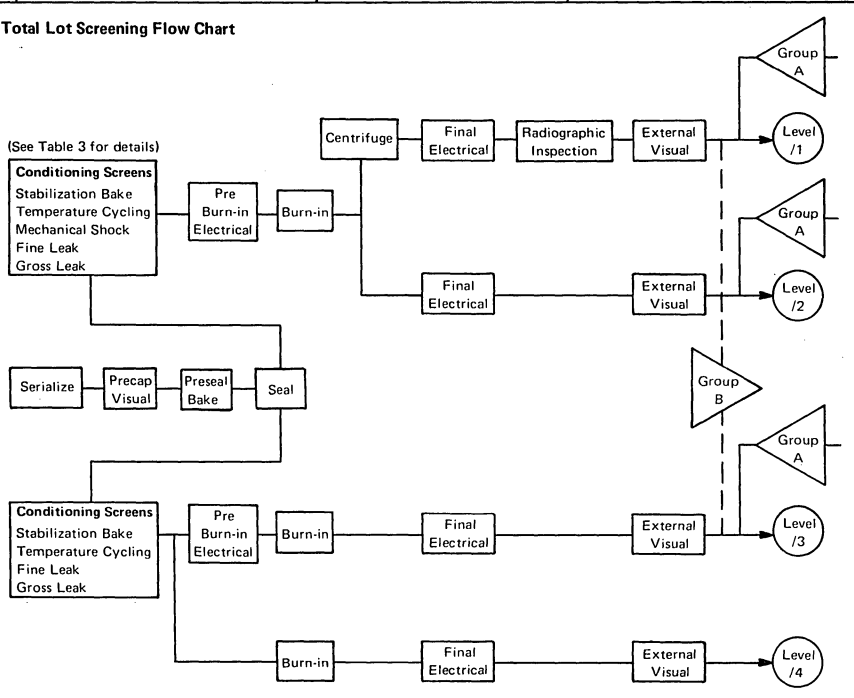


Table 2 – Lot Acceptance Data

	Levels	Included With Order	On Request
Conditioning Screens (100% Testing; see Table 3)			
a) Final electrical test data	/1, /2, /3, /4	√	–
b) Radiographic inspection	/1	√	–
c) Pre-burn-in electrical test data	/1, /2	–	√
d) Precap visual by customer's inspector	/1, /2	–	√
Group A (Lot Sampling; see Table 7)	/1, /2, /3	–	√
Group B (Lot Sampling; see Table 8)	/1, /2, /3	–	√

Note: If several shipments are made from a specific production lot, Group A and B data will be supplied for only the first shipment.

Table 3 – Description of Total Lot Screening (X indicates 100-per-cent testing)

Test	Conditions	MIL-STD-883		Screening Levels			
		Method	Conditions	/1	/2	/3	/4
1. Serialize	–	–	–	X	X	X	X
2. Precap Visual	–	2017	–	X	X	X	X
	Semiconductor Die	2010	–	X	X	X	X
3. Preseal Bake	2 hrs. min. at 150°C min.			X	X	X	X
4. Seal	–	–	–	X	X	X	X
5. Stabilization Bake	16 hrs. at 150°C min.	1008	C	X	X	X	X
6. Temperature Cycling	10 cycles	1010	C	X	X	X	X
7. Mechanical Shock	5 pulses, Y1 direction	2002	B	X	X		
8. Centrifuge	Y1 direction only	2001	1500 g	X			
9. Fine Leak	–	1014	A	X	X	X	X
10. Gross Leak	–	1014	C	X	X	X	X
11. Pre-Burn-In Electrical	See Table 4	–	–	X	X	X	
12. Burn-In (Accelerated thermal fatigue)	4 hrs. See Fig. 17	–	–	X	X	X	X
13. Final Electrical							
25°C	See Table 6	–	–	X	X	X	X
–55 and +125°C	See Table 6	–	–	X	X		
14. Radiographic Inspection	X2, Y2, Z1	2012	–	X			
15. External Visual	–	2009	–	X	X	X	X

Table 4 – Pre-Burn-In Electrical Tests at case temperature (T_C) = 25°C

Characteristic	Symbol	Test Conditions					Limits		Units
		Supply Voltage (V_S)-V	Freq. (f)-kHz	Output Power (P_O)-W	Load Resist. (R_L)-Ω	Test Circuit (Fig.)	Min.	Max.	
Open-Loop Voltage Gain	$\frac{V_{OUT}}{V_{IN}}$	±37.5	1	25	4	16	2400	–	V/V
Bandwidth	f_H	±37.5	–	1	4	19	43	–	kHz
Quiescent Current	I_O	±37.5	–	–	–	18	–	±30	mA
Offset Voltage	V_{offset}	±37.5	–	–	4	18	–	±250	mV
Maximum Voltage Swing	V_{OUT}	±26	1	100	4	19	±28	–	V
Short-Circuit Current	I_S	±37.5	1	–	0.5	19	–	±3.5	A

Table 5 – Characteristics not Measured in Screening Procedures

Characteristic	Symbol	Test Condition	Limits		Units
		Supply Voltage (V_S) - V	Max.	Typical	
Signal-to-Noise Ratio (Source impedance 600 Ω)	S/N	±37.5	–	+78	dB
Thermal Resistance per output device (junction-to-case)	$R_{\theta JC}$	–	2	–	°C/W
Common-Mode Input Voltage Range		–	–	$+V_S - 5$ V $-V_S + 5$ V	V

Table 6 – Final Electrical Tests (Post-Burn-in)

Characteristic	Symbol	Test Conditions					Limits At Indicated Temperatures						Units
		Supply Voltage (V_S)-V	Freq. (f)-kHz	Output Power (P_O)-W	Load Resist. (R_L)-Ω	Test Circuit (Fig.)	Minimum			Maximum			
							–55°C	+25°C	+125°C	–55°C	+25°C	+125°C	
Open-Loop Voltage Gain	$\frac{V_{OUT}}{V_{IN}}$	±37.5	1	25	4	16	2000	2400	2000*	–	–	–	V/V
Closed-Loop Voltage Gain	$\frac{V_{OUT}}{V_{IN}}$	±37.5	1	1	4	19	26	26	26	–	–	–	V/V
Bandwidth	f_H	±37.5	–	1	4	19	–	43	–	–	–	–	kHz
Quiescent Current	I_O	±37.5	–	–	–	18	–	–	–	–	±30	–	mA
Offset Voltage	V_{offset}	±37.5	–	–	4	18	–	–	–	±350	±250	±350	mV
Total Harmonic Distortion	THD	±37.5	1	60	4	19	–	–	–	–	0.5	–	%
Maximum Voltage Swing	V_{OUT}	±37.5	1	100	4	19	24	28	24*	–	–	–	V
Short-Circuit Current	I_S	±26	1	–	0.5	19	–	–	–	–	3.5	–	A
Input Impedance	Z_{IN}	±37.5	–	–	–	15	–	16	–	–	–	–	kΩ
Slew Rate	SR	±37.5	1	100	4	19	–	5	–	–	–	–	V/μs
Maximum Power	P_{max}	±37.5	1	100	4	19	72	100	72*	–	–	–	W

* Pulse test; duration $<$ 500 ms.

Table 7 – Group A Electrical Sampling Inspection MIL-M-38510 A

LTPD.●					
Screening Level					
/1, /2			/3, /4		
Temp °C					
−55	+25	+125	−55	+25	+125
7%	5%	7%	10%	5%	10%

Characteristic	Symbol	Test Circuit (Fig.)	Limits At Indicated Temperatures: Minimum −55°C	Minimum +25°C	Minimum +125°C	Maximum −55°C	Maximum +25°C	Maximum +125°C	Units
Open-Loop Voltage Gain	V_{OUT}/V_{IN}	16	2000	2400	2000*	–	–	–	V/V
Closed-Loop Voltage Gain	V_{OUT}/V_{IN}	19	26	26	26	–	–	–	V/V
Bandwidth	f_H	19	–	43	–	–	–	–	kHz
Quiescent Current	I_O	18	–	–	–	–	±30	–	mA
Offset Voltage	V_{offset}	18	–	–	–	±350	±250	±350	mV
Total Harmonic Distortion	THD	19	–	–	–	–	0.5	–	%
Maximum Voltage Swing	V_{OUT}	19	24	28	24*	–	–	–	V
Short-Circuit Current	I_S	19	–	–	–	–	3.5	–	A
Input Impedance	Z_{IN}	15	–	16	–	–	–	–	kΩ
Slew Rate	SR	19	–	5	–	–	–	–	V/μs
Maximum Power	P_{max}	19	72	100	72*	–	–	–	W

● Lot Tolerance Percent Defectives

* Pulse test; duration $<$ 500 ms

Table 8 – Group B Environmental Sampling Inspection

Subgroup	Test	MIL-STD-883		Lot Tolerance % Defectives	
		Reference	Conditions	Levels /1, /2	Levels /3, /4
1	Visual and Mechanical and Marking Permanency	2008	Test Cond. B 10X mag.	10	15
	Physical Dimensions	2008	Test Cond. A per Dimen. Outline		
2	Solderability	2003	Temperature 230 ± 5°C	10	15
3	Temperature Cycling	1010	Test Cond. C, 25 cycles		
4	Mechanical Shock	2002	Test Cond. B,0.5 ms,5 blows Y1 direction only	10	15
	Constant Acceleration	2001	Test Level 1500 g Y1 direction only		
5	Lead Fatigue	2004	Test Cond. B, per Fig. 20	10	15
	Fine Leak	1014	Test Cond. A, 5 x 10^{-7} min.		
	Gross Leak	1014	Test Cond. C		
6	High Temp. Storage	1008	Test Cond. C, 1000 hrs.	7	15
7	Operating Life	1005	T_A=25°C, 1000 hrs. Test Circuit–see Fig. 17	7	10
8	Bond Strength	2011	Test Cond. D	10 devices ⩽ 1% def.	10 devices ⩽ 1% def.

Table 9 – Group B Electrical Test Limits

Characteristic	Symbol	Test Circuit (Fig.)	Limits		Units
			Min.	Max.	
Offset Voltage	V_{offset}	18	–275	+275	mV
Maximum Power	P_{max}	19	90	–	W
Voltage Gain (Open Loop)	$\frac{V_{out}}{V_{in}}$	16	2000	–	V/V
Total Harmonic Distortion	THD	19	–	0.6	%
Short-Circuit Current	I_S	19	±1.5	±4.0	A

TYPICAL CURVES

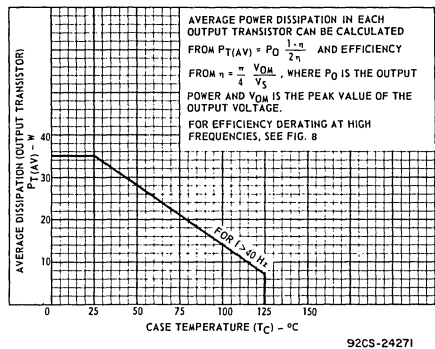


Fig. 2—Dissipation (average) derating curve for each output transistor (for symmetrical waveforms with f > 40 Hz).

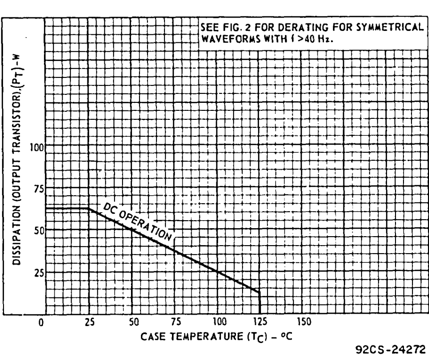


Fig. 3—Dissipation (dc) derating curve for each output transistor.

TEST ARRANGEMENTS AND PROCEDURES

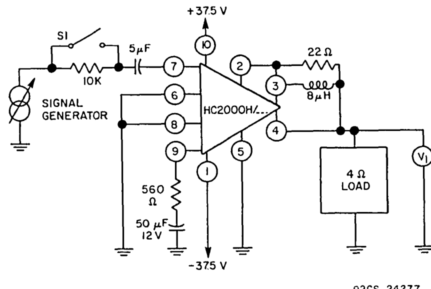


Fig. 4—Circuit for measurement of common-mode input impedance.

PROCEDURE FOR MEASUREMENT OF COMMON-MODE INPUT IMPEDANCE

a) Insert unit
b) Apply ±37.5 V
c) Close S1
d) Adjust signal generator for 1 V on voltmeter V1
e) Open S1
f) Read voltmeter V1
g) Input impedance = $(10\text{ k}) \times \frac{V1}{1 - V1}$

Note: Circuit under test must have a heat sink so that $T_C \approx 25^oC$, unless otherwise noted.

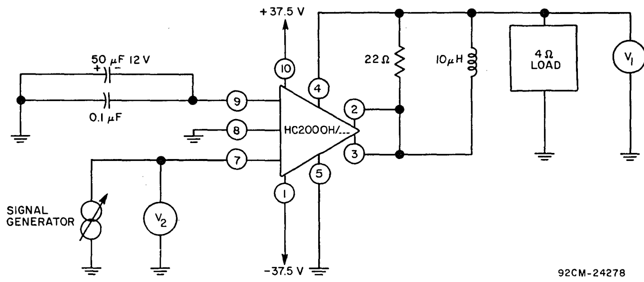


Fig. 5— Circuit for measurement of open-loop gain.

PROCEDURE FOR MEASUREMENT OF OPEN-LOOP GAIN

a) Insert unit
b) Apply ±37.5 V
c) Set generator at 1 kHz and adjust until V1 = 10 V rms
d) Read V2
e) Open-loop gain = V1/V2

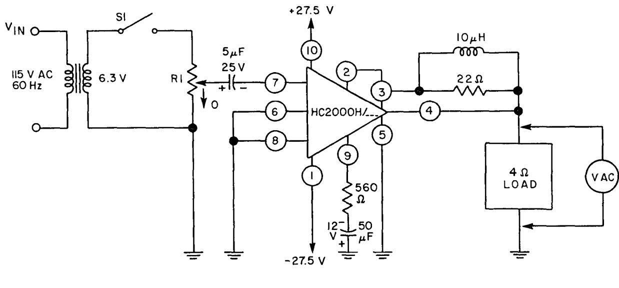


Fig. 6— Circuit for burn-in and life test.

1. BURN-IN (ACCELERATED THERMAL FATIGUE) PROCEDURE

a) Set R1 = 0, close S1
b) Insert unit
c) Apply ±27.5 V
d) Adjust R1 for 13.0 V AC across load
e) Monitor flange temperature and adjust R1 (if necessary) so that flange temperature stabilizes at 135°C ±5°C
f) Total power dissipation ≈35 W
g) Cycle switch S1: time on = 2.5 min., time off = 2.5 min.
h) Cool flange during off-cycle to 45°C ± 2°C in moving air.

2. LIFE-TEST PROCEDURE

a) Set R1 = 0, close S1
b) Insert unit
c) Apply ±27.5 V
d) Adjust R1 so that flange temperature stabilizes at 75°C max.
e) Cycle switch S1: time on = 2.5 min., time off = 2.5 min.
f) Cool flange during off-cycle to 45°C ± 2°C in moving air.

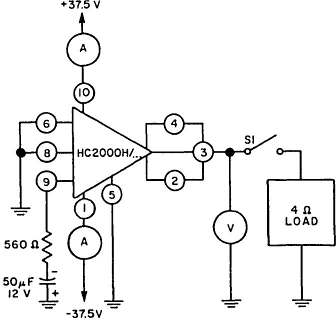


Fig. 7— Circuit for measurement of offset voltage and quiescent current.

PROCEDURE FOR MEASUREMENT OF OFFSET VOLTAGE AND QUIESCENT CURRENT

A = DC ammeter 100 mA range
V = DC voltmeter ± 250 mV range
a) Close S1
b) Insert unit
c) Apply ± 37.5 V
d) Read offset voltage on voltmeter. Change polarity if required.
e) Open S1
f) Read positive and negative quiescent current on ammeter.

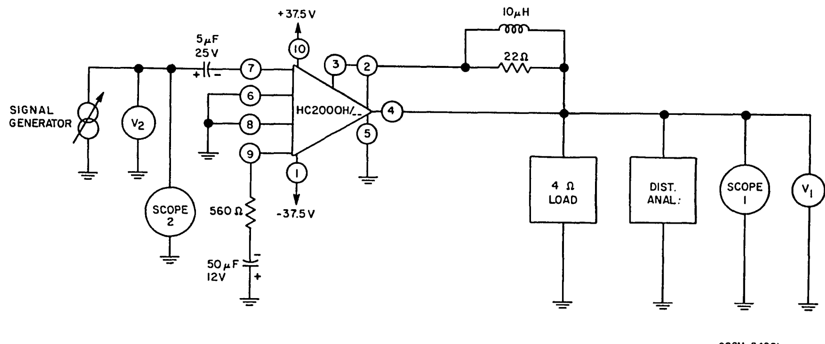


Fig. 8— Circuit for measurement of closed-loop voltage gain, total harmonic distortion, maximum voltage swing, maximum power, short-circuit current, bandwidth, and slew-rate.

1. PROCEDURE FOR MEASUREMENT OF CLOSED-LOOP VOLTAGE GAIN

a) Insert unit
b) Adjust signal generator to 1 kHz, V2 = 0
c) Apply ± 37.5 V
d) Adjust signal generator for 2 V rms on voltmeter V1
e) Read voltmeter V2
f) Voltage gain $= \frac{V1}{V2}$

2. **PROCEDURE FOR MEASUREMENT OF TOTAL HARMONIC DISTORTION**
   a) Adjust signal generator for 15.5 V rms on V1
   b) Adjust distortion analyzer. Record the meter reading as Total Harmonic Distortion (THD).

3. **PROCEDURE FOR MEASUREMENT OF MAXIMUM VOLTAGE SWING AND MAXIMUM POWER**
   a) Adjust signal generatoı for maximum output on scope No. 1 with no clipping. Read peak voltage as maximum voltage swing.
   b) Read V1
   c) Maximum power = $\frac{V1^2}{4}$

4. **PROCEDURE FOR MEASUREMENT OF SHORT-CIRCUIT CURRENT**
   a) Lower power supply to ± 26 V
   b) Momentarily replace 4-ohm load with 0.5-ohm load
   c) Scope No. 1 must show symmetrical square wave of less than ± 1.75 V

5. **PROCEDURE FOR MEASUREMENT OF BANDWIDTH**
   a) Raise power supply to ± 37.5 V
   b) Adjust signal generator at 43 kHz to 2 V rms on V1
   c) Adjust distortion analyzer and verify that THD < 0.5%

6. **PROCEDURE FOR MEASUREMENT OF SLEW RATE**
   a) Replace signal generator with square-wave generator.
   b) Adjust generator for 500 Hz and V1 = 40 V peak-to-peak.
   c) Read time required for swing from peak to peak.
   d) Slew rate = $\frac{40\ V}{\text{Measured time}}$

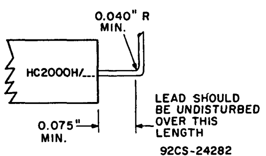


Fig. 9— Recommended lead-bending specification.

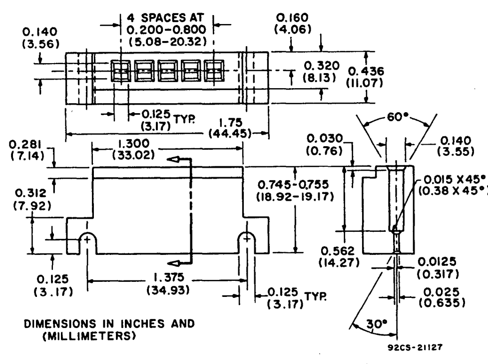


Fig. 10—Socket for use with HC2000H/. . . .

DIMENSIONAL OUTLINE

2 (50.8)
1 (25.4)
BASE PLATE
0.65 (16.5) (TYP.)
0.10 (2.54)
0.040(1.02) DIA. ON 0.200(5.08) CENTERS
3 (76.2)
2.1 (53.3)
TOP VIEW
2.5 (63.5)
0.280 (7.11)
0.260 (6.60)
0.320 (8.12)
0.310 (7.87)
1 (25.4) (TYP.)
0.275 (6.99) (TYP.)

DIMENSIONS IN INCHES AND (MILLIMETERS)

92CS-18037R2

*TERMINALS 6 AND 11 ARE CONNECTED INTERNALLY

TERMINAL CONNECTIONS

Pin No.	Connection	
1	$-V_S$	Negative supply voltage
2	V_{FB}	Feedback voltage
3	V_{OUT}	Output voltage
4	PC	Phase compensation
5	GND	Ground
6	BP	Base plate (internal connection)
7	$+V_{IN}$	Non-inverting input
8	GND	Ground
9	$-V_{IN}$	Inverting input
10	$+V_S$	Positive supply voltage

High-Reliability Thyristors

High-Reliability Thyristors

RCA offers, on a custom basis, high-reliability versions of a variety of standard-product thyristors (triacs and SCR's). These devices may be processed and screened to any of four different reliability levels that are approximately equivalent to, or exceed, the reliability classes (JAN, JANTX and JANTXV) defined by MIL-S-19500. They are supplied in hermetic packages that meet the stringent mechanical and environmental requirements of military, aerospace, and critical industrial applications. Fig. 4-1 shows the package options available for RCA high reliability triacs and SCR's.

Basic Reliability Considerations

RCA high-reliability thyristors are the result of careful design and screening and of careful adherence to basic reliability-assurance techniques.

A good basic design is essential for devices for which an assured high degree of reliability is a prime requirement. Any standard-product RCA triac or SCR selected to undergo high-reliability processing, therefore, is subjected to extensive design evaluations. RCA assesses the inherent reliability of each device type under conditions that simulate the types of service for which the device may be employed in recommended applications.

Testing to failure is one method that RCA uses for device reliability evaluations. The natural boundaries of any life-test program used to evaluate device reliability, however, are time and the number of available samples. Accelerated testing is an accepted technique used to obtain meaningful information in a reasonable time from a limited number of samples. In this testing, the sample devices are subjected to stresses that exceed rated or normal operating conditions for relatively short periods in order to generate failures that would normally occur under typical conditions over longer stress periods. If true acceleration exists, the results can be extrapolated to predict the mean time to failure under typical operating conditions. A device that survives the abnormal stresses of accelerated life tests is presumed to be very reliable when subjected to the less stringent conditions encountered in actual use. RCA uses accelerated life tests in evaluation of high-reliability thyristors.

The operating conditions that a device is subjected to in an actual system application have an important bearing on its reliability. A numerical expression of reliability is meaningless unless the prevailing electrical, mechanical, and environmental conditions under which the reliability was assessed are also specified, because if these conditions are altered, the numerical value may also be changed. Reliability specifications, therefore, must define limit values for the electrical, mechanical, and environmental conditions that affect the life or behavior of a device.

RCA defines the limiting operating conditions and requirements of the system and of the circuit in which a device is to be used and specifies in detail the necessary device parameters.

The equipment manufacturer must select devices for his system that can safely withstand the mechanical and environmental conditions they may be expected to encounter in the application. In addition, he must design his circuits so that the system does not impose any excess electrical strains that may adversely affect the life or performance of the devices and thereby reduce over-all system reliability. Special care must be taken to assure that no maximum rating of a device is exceeded under any condition of equipment operation. The equipment designer should also realize that the maximum and minimum ratings specified for the devices are worst-case limits. **A reliable equipment design should be conservative so that devices are not operated at or near maximum ratings.**

In the design of equipment and circuits that use RCA high-reliability triacs and SCR's, the designer should adhere strictly to the specifications that govern the use of such devices.

Failure Analysis

The various problems encountered with thyristors may be categorized in two large groups, as indicated in the following listings:

1. Manufacturing defects
2. Application faults
   a. Overvoltage, surface or bulk
   b. di/dt, overvoltage turn-on
      (1) di/dt turn-on
      (2) Gated turn-on
      (3) Gate noise turn-on
   c. Gate dissipation, forward-reverse interchanged cathode
   d. Surge
   e. Overload
   f. Hermeticity

Manufacturing defects, and the required corrective actions, are clearly the responsibility of the device manufacturer. In application defects, the user and the manufacturer have a joint responsibility. Experience has shown that, in general, application defects outnumber design or manufacturing defects by at least an order of magnitude. Such problems can usually be solved, however, through careful analysis and close communication between manufacturer and user.

Applications faults fall into several general categories. The first and most prevalent is that arising from overvoltage. Overvoltage damage can be either in the bulk of the device, at defects in the crystal, at diffusion irregularities, or at localized spots on the surface. The concentration of power dissipation at these small areas causes material degradation in either the silicon or the encapsulating materials at the edge. Closely associated with overvoltage turn-on, is a di/dt stress that results from turn-on initiated by the overvoltage. If overvoltage turn-on is accomplished without damage within the chip, a danger is still present in that the current

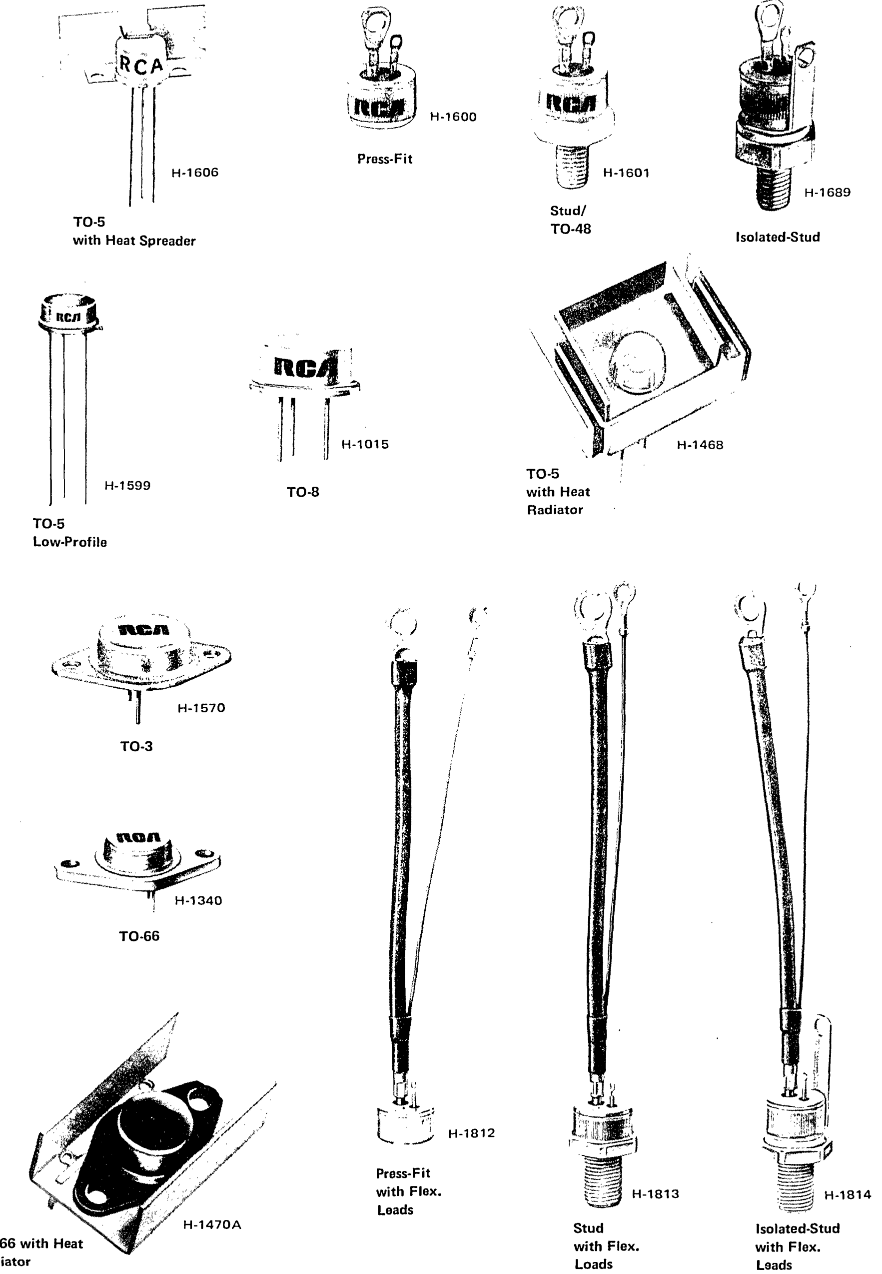


Fig. 4-1—Packages used for RCA high-reliability triacs and SCR's.

resulting from the thyristor turn-on is concentrated in the small area within which turn-on began. Such localized current conduction can result in over-temperature in a small area. In turn-on initiated from overvoltage, the mechanism to cause spreading of the current is not present. The di/dt capability for a thyristor turned on from overvoltage is much lower than the di/dt capability of the thyristor turned on by a gate signal. As a result, even though the di/dt in a circuit might be at a very comfortable level for gated turn-on, it may exceed the overvoltage turn-on di/dt capability. Often, during an examination of the damaged area of the chip, it is difficult to determine whether the failure is caused by the initial overvoltage or the initial rise of current. Both types of faults result in small burnt areas through the chip bulk or at the edge.

The di/dt capability for gated turn-on is high but it can still be exceeded, particularly with very low values of gate drive. A gated di/dt failure in RCA devices always occurs at the inside edge of the n-type emitter, which is the area at which conduction begins. This type of failure results in a small area of molten silicon. Such a failure mechanism is easily seen in the chip. Most users today are conscious of the fact that adequate gate signal must be provided, particularly in applications involving fast rising pulses of large magnitude. Frequently, analyses are made of devices from such circuits in which adequate gate signal is provided and yet di/dt failures that stem from inadequate gate signal are found. The conclusion is that turn-on is initiated by noise in the gate circuit somewhere, and the designer of the equipment must correct these unwanted signals.

Failure may also result because of gate over-dissipation. RCA thyristors have relatively large gates and robust gate leads, so that a good deal of dissipation is acceptable. The dissipation limit, however, can be exceeded. A triac will operate as a triac when the gate lead is inadvertently interchanged with the Main Terminal No. 1. The gate area is much smaller than the Main Terminal No. 1 area, and if full current flows, the gate will be damaged. Triac gate damage often destroys blocking voltage in the first quadrant without damage to the blocking voltage in the third quadrant. A consistent failure of first quadrant blocking voltage, therefore, suggests gate damage.

Short-time surge failure generally results from a gross melting of silicon over much of the cathode or main terminal areas. In some RCA packages for lower-current devices, the internal leads fuse at several hundred amperes of short-circuit current. Consequently if a device fails because the internal leads of a device are fused, it may be assumed that a momentarily shorted load condition existed. Overload results from a long duration of current in excess of the steady-state rated current which causes a gradual heat build up. The first area to be attacked is the ohmic contact system. In an overload failure, the high-temperature solder used on the chip melts and flows out from under the chip. This flow, which occurs prior to a resulting gross degradation of the ohmic contact system and pellet, characterizes overload failure.

Hermeticity failures on hermetic devices generally lead to the presence of ionizable material in the encapsulated resin next to the surface. This condition leads to surface current, surface inversion layers, a reduction in a device blocking-voltage capability, and increased blocking leakage current because of the high surface current. Therefore, it is particularly important to maintain hermeticity on hermetically sealed devices. For device failure because of degraded blocking characteristic, a gross and time leak check is performed before any inspection for other possible defects.

The most significant factor in the control failures is careful process control in the factory and communication between users and manufacturers in application defects.

Basic Reliability Testing

The most important factors in the control of manufacturing defects arise through knowledge of the device design and tight process control in manufacture. Nothing that can be done in terms of statistics or testing comes close to the importance of good process control in manufacture. This control is complemented by reliability testing to monitor product capability. During the development phase, various reliability tests are conducted by the product development group. During the early production phase, the device capability is monitored by an engineering reliability group. During normal production, the manufacturing-plant quality-control department regularly performs various mechanical, environmental, and life tests. Fig. 4-2 outlines the basic tests and analyses performed in reliability evaluations of RCA thyristors.

The high-temperature blocking test exposes the device to the maximum blocking voltage and the maximum operating temperature. The blocking test is followed by thermal-fatigue testing during which the rated current is passed through the thyristor, and the resulting power dissipation is used to heat the device to the maximum junction temperature. The current is then interrupted, and the thyristor is cooled rapidly. Thousands of thermal cycles are accumulated to verify the mechanical soundness of the pellet and its mounting system.

During the operating life tests, synthetic switching circuits simultaneously apply maximum current and maximum voltage to the device at the normal line frequency and maximum rated case temperature. This type of testing simulates actual operating conditions. High-temperature storage is used to accentuate instability that may exist at the surface of the device. Temperature cycling, surge, vibration, and shock are the familiar environmental tests used to assess the mechanical robustness of the package, the pellet, and the lead-attachment system. Surge testing stresses the ohmic contact system of the device to assure that low thermal resistance and an even distribution is maintained under the surge condition.

During the development phase, these tests are generally performed on a step-stress basis. During the quality control phase, they are conducted at rated conditions.

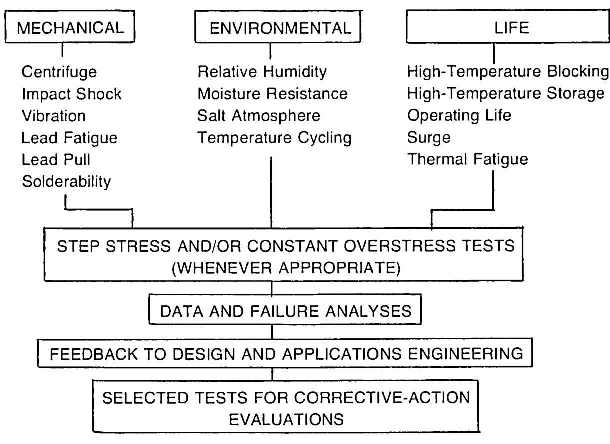


Fig. 4-2—Outline of reliability evaluations performed on RCA thyristors.

The data obtained from life testing can provide some statistical representation of failure rate. Fig. 4-3 shows an example of a method used to represent failure rate in the United States Military Handbook on "Reliability of Electronic Components." The curves shown present

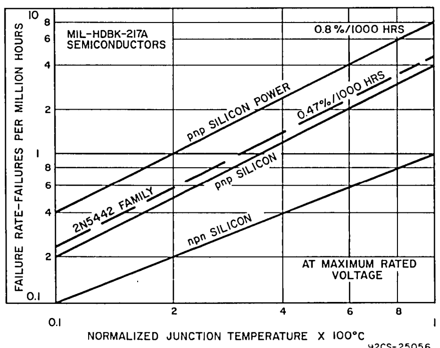


Fig. 4-3—Failure rates (in failures per 10^6 hours) for MIL-S-19500 transistors, (for power transistors, 1 watt or greater at T_A = 25°C multiply values shown by two) and for the RCA-2N5442 40-ampere triac (dashed line).

failure rates for transistors as a function of temperature. However, because the blocking junctions in thyristors typically form a p-n-p transistor structure, use of these derating curves for thyristors is justified when sufficient test data are available. Different failure rates have been projected from the statistical summing of experimental data. A derating curve that describes the failure rate of an RCA-2N5442 40-ampere triac is superimposed (dashed line) on the family of transistor derating curves shown in Fig. 4-3. As indicated by this curve, the failure rate of the 2N5442 triac (and of other thyristors that have been studied) is similar to that for other silicon power devices.

Processing and Screening

RCA high-reliability thyristors that are subjected to high-reliability preconditioning and screening in accordance with the Group A, B, and C Sampling Tests as specified in MIL-STD-750 or special customer requirements can be obtained on a custom basis. These thyristors can be supplied to four basic reliability levels that are approximately equivalent to, or exceed, the reliability classes (JAN, JANTX, JANTXV) defined by MIL-S-19500.

Fig. 4-4 shows the basic processing steps required for RCA high-reliability thyristors for each reliability level, and Table 4-1 lists the screening tests to which these devices are subjected. Tables 4-2, 4-3, and 4-4 list the Groups A, B, and C Sampling Tests and the test methods specified by MIL-STD-750.

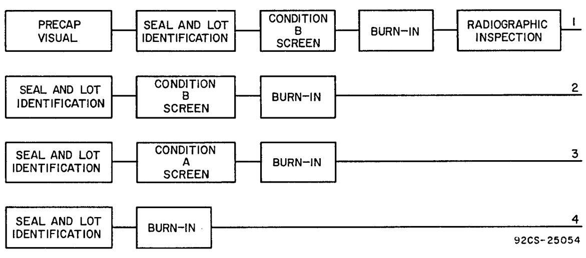


Fig. 4-4—Basic processing and screening required for RCA high-reliability triacs and SCR's.

Table 4-1— Screening Tests for High-Reliability Thyristors

Test	Condition	MIL-STD-750 Method	MIL-STD-750 Conditions	Screening Levels 1	2	3	4
1. Precap visual	20 power			X			
2. Seal and lot identification				X	X	X	X
3. High-temperature Storage	24 hrs. at 150°C	1031		X	X		
4. Temperature cycling	Low temperature per device	1051	F	X	X		
5. Acceleration	Y_1 direction	2006		X	X		
6. Hermeticity-fine leak		1071	H	X	X	X	
7. Hermeticity-gross leak		1071	D	X	X		
8. Serialize				X			
9. Preburn-in electrical-record				X			
10. Preburn-in electrical					X	X	X
11. Burn-in	24 to 168 hrs.; 100°C to 125°C			X	X	X	X
12. Post burn-in electrical					X	X	X
13. Post burn-in electrical-record Δ's				X			
14. Final electrical				X	X		
15. Hermeticity-fine leak				X	X		
16. Hermeticity-gross leak				X			
17. Radiographic		2076		X			
18. External visual		2071		X			

Table 4-2— Group A Tests

Subgroup	Test	MIL-STD-750 Method
1	Visual	2071
2	Forward blocking current	4206.1
2	Reverse blocking current	4211.1
3	High-temp. forward blocking current	
3	High-temp. reverse blocking current	
3	High-temp. gate-trigger voltage or gate-trigger current	4221.1
3	Exponential rate of voltage rise	4231.2
4	Gate-trigger voltage or gate-trigger current at 25°C	
4	Gate-controlled turn-on time	4223
4	Circuit-commutated turn-off time	4224
4	Gate-controlled turn-off time	4225
4	Forward "on" voltage	4226.1
4	Holding current	4201.2

Technical Data

Electrical ratings and gate or turn-off-time characteristics for RCA triacs and SCR's for which high-reliability versions can be obtained are shown in the data charts on the following pages.

Table 4-3— Group B Tests

Test	MIL-STD-750 Method
Reverse gate current	4219
Surge current	4066
Temperature cycling	1051
Thermal shock (glass strain)	1056
Terminal strength	2036
Moisture resistance	1021
AC blocking voltage	–

Table 4-4— Group C Tests

Subgroup	Test	MIL-STD-750 Method
1	Physical dimensions	2066
2	Shock	2016
2	Vibration, variable-frequency	2056
2	Constant acceleration	2006
3	Barometric pressure	1001
4	Salt atmosphere	1041
5	Solderability	2026
6	Intermittent life	–

Solid State Division

Thyristors

2N5441-2N5446 T6400 T6410 T6420 Series

40-A Silicon Triacs

BASIC RATINGS *For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.*		2N5441 2N5444 T6420B	2N5442 2N5445 T6420D	2N5443 2N5446 T6420M	T6400N T6410N T6420N	
*REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open, T_J = −65 to 110°C	V_{DROM}	200	400	600	800	V
RMS ON-STATE CURRENT (Conduction angle = 360°): Case temperature	$I_{T(RMS)}$					
* T_C = (2N5441–2N5443, T6400N)		40				A
* = (2N5444–2N5446, T6401N)		40				A
= (T6420B, D, M, N)		40				A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied principal voltage	I_{TSM}					
* 60 Hz (sinusoidal)		300				A
50 Hz (sinusoidal)		265				A
RATE OF CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.1 μs	di/dt	100				A/μs
FUSING CURRENT (for Triac Protection): T_J = −65 to 110°C, t = 1.25 to 10 ms	I^2t	450				A^2s
*PEAK GATE-TRIGGER CURRENT:■ For 1 μs max.	I_{GTM}	12				A
*GATE POWER DISSIPATION: PEAK (For 10 μs max., $I_{GTM} \leq$ 4 A)	P_{GM}	40				W
*TEMPERATURE RANGE: Storage	T_{stg}	−65 to 150				°C
Operating (Case)	T_C	−65 to 110				°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■ For v_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	I^+	positive	positive	I_{GT}	15	50	mA
	III^-	negative	negative		20	50	
	I^-	positive	negative		30	80	
	III^+	negative	positive		40	80	
DC Gate-Trigger Voltage:● ■ For v_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	1.35	2.5	V

PACKAGE: Press-Fit (2N5441-2N5443, T6400N)
Stud (2N5444-2N5446, T6401N)
Isolated-Stud (T6420 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 593.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.
* In accordance with JEDEC registration data format (JS-14, RDF2) filed for the JEDEC (2N-Series) types.

Solid State
Division

Thyristors
2N5567-2N5570
T4101 T4111 T4121 Series

10-A Silicon Triacs

BASIC RATINGS: *For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.*		2N5567 2N5569 T4121B	2N5568 2N5570 T4121D	T4101M T4111M T4121M	
*REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open, T_J = −65 to 100°C	V_{DROM}	200	400	600	V
*RMS ON-STATE CURRENT (Conduction angle = 360°): Case temperature (T_C) = 85°C	$I_{T(RMS)}$		10		A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied prinicpal voltage	I_{TSM}				
* 60 Hz (sinusoidal)			100		A
50 Hz (sinusoidal)			85		A
RATE-OF-CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{DROM}$, I_{GT} = 160 mA, t_r = 0.1 μs	di/dt		150		A/μs
FUSING CURRENT (for Triac Protection): T_J = −65 to 100°C, t = 1.25 to 10 ms	I^2t		50		A^2s
PEAK GATE-TRIGGER CURRENT:■ For 1 μs max.	I_{GTM}		4		A
*GATE POWER DISSIPATION: PEAK (For 1 μs max., $I_{GTM} \leq 4$ A	P_{GM}		16		W
*TEMPERATURE RANGE: Storage	T_{stg}		−65 to 150		°C
Operating (Case)	T_C		−65 to 100		°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	I+	positive	positive	I_{GT}	10	25	mA
	III−	negative	negative		10	25	
	I−	positive	negative		20	40	
	III+	negative	positive		20	40	
DC Gate-Trigger Voltage:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	1	2.5	V

PACKAGE: Press-Fit (2N5567, 2N5568, T4101M)
Stud (2N5569, 2N5570, T4111M)
Isolated-Stud (T4121B, D, M)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 457.

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N Series) types.
● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State Division

Thyristors

2N5571-2N5574 T4100 T4110 T4120 Series

15-A Silicon Triacs

BASIC RATINGS: *For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.*		2N5571 2N5573 T4120B	2N5572 2N5574 T4120D	T4100M T4110M T4120M	
*REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open, T_J = −65 to 100°C	V_{DROM}	200	400	600	V
*RMS ON-STATE CURRENT (Conduction angle = 360°): Case temperature	$I_{T(RMS)}$				
T_C = 80°C (2N5571–2N5574, T4100M, T4110M)			15		A
= 75°C (T4120 Series)			15		
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied prinicpal voltage	I_{TSM}				
* 60 Hz (sinusoidal)			100		A
50 Hz (sinusoidal)			85		A
RATE OF CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{DROM}$, I_{GT} = 160 mA, t_r = 0.1 μs	di/dt		150		A/μs
FUSING CURRENT (for Triac Protection): T_J = −65 to 100°C, t = 1.25 to 10 ms	I^2t		50		A^2s
PEAK GATE-TRIGGER CURRENT:■ For 1 μs max.	I_{GTM}		4		A
*GATE POWER DISSIPATION: Peak (For 1 μs max., $I_{GTM} \leq 4$ A	P_{GM}		16		W
*TEMPERATURE RANGE:					
Storage	T_{stg}		−65 to 150		°C
Operating (Case)	T_C		−65 to 100		°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■ For V_D = 12 V (dc),	I+	positive	positive	I_{GT}	20	50	mA
R_L = 30 Ω,	III−	negative	negative		20	50	
T_C = 25°C	I−	positive	negative		35	80	
	III+	negative	positive		35	80	
DC Gate-Trigger Voltage:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	1	2.5	V

PACKAGE: Press-Fit (2N5571, 2N5572, T4100M)
Stud (2N5573, 2N5574, T4110M)
Isolated-Stud (T4120B, D, M)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 458.

* In accordance with JEDEC registration data format (JS-14, RDF2) filed for the JEDEC (2N-Series) Types.
● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State
Division

Thyristors
2N5754-2N5757
T2303 T2313 Series

2.5-A Silicon Triacs

BASIC RATINGS:
For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

	Symbol	2N5754 T2313A	2N5755 T2313B	2N5756 T2313D	2N5757 T2313M	
*REPETITIVE PEAK OFF-STATE VOLTAGE:●	V_{DROM}					
Gate open, T_J = −65 to 100°C		100	200	400	600	V
RMS ON-STATE CURRENT (Conduction angle = 360°):	$I_{T(RMS)}$					
Case temperature						
* T_C = 70°C (T2303 Series)			2.5			A
Ambient temperature						
T_A = 25°C (T2313 Series)			1.9			A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}					
For one cycle of applied principal voltage						
* 60 Hz (sinusoidal)			25			A
50 Hz (sinusoidal)			21			A
RATE OF CHANGE OF ON-STATE CURRENT:						
$V_{DM} = V_{DROM}$, I_{GT} = 50 mA, t_r = 0.1 μs	di/dt		100			A/μs
FUSING CURRENT (for Triac Protection):						
T_J = −65 to 100°C, t = 1.25 to 10 ms	I^2t		3			A^2s
*PEAK GATE-TRIGGER CURRENT:■	I_{GTM}					
For 1 μs max.			1			A
*GATE POWER DISSIPATION:	P_{GM}					
PEAK (For 10 μs max.)			10			W
*TEMPERATURE RANGE:						
Storage	T_{stg}		−65 to 150			°C
Operating (Case)	T_C		−65 to 100			°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■							
For V_D = 12 V (dc)	I+	positive	positive	I_{GT}	5	25	mA
R_L = 30 Ω	III−	negative	negative		5	25	
T_C = 25°C	I−	positive	negative		10	40	
	III+	negative	positive		10	40	
DC Gate-Trigger Voltage:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	0.9	2.2	V

PACKAGE: Modified JEDEC TO-5 (2N5754-2N5757)
Modified JEDEC TO-5 with Heat Radiator (T2313 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 414.

* In accordance with JEDEC registration data format (JS-14, RDF-2 filed for the JEDEC (2N Series) types.
● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State Division

Thyristors

T2300 T2302 T2310 T2312 Series

2.5-Ampere Sensitive-Gate Silicon Triacs

BASIC RATINGS

For Operation with 50/60-Hz, Sinusoidal Supply Voltage and Resistive or Inductive Load

		Symbol	Value	Units
REPETITIVE PEAK OFF-STATE VOLTAGE● (Gate Open):		V_{DROM}		
T_J = -40°C to +90°C:	T2300A, T2310A		100	V
	T2300B, T2310B		200	V
	T2300D, T2310D		400	V
T_J = -40°C to +100°C:	T2302A, T2312A		100	V
	T2302B, T2312B		200	V
	T2302D, T2312D		400	V
RMS ON-STATE CURRENT (Conduction Angle = 360°):		$I_{T(RMS)}$		
T_C = 60°C:	T2300 series		2.5	A
T_C = 70°C:	T2302 series		2.5	A
T_A = 25°C:	T2300 series		0.35	A
	T2302 series		0.40	A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:		I_{TSM}		
For one full cycle of applied principal voltage				
60 Hz sinusoidal			25	A
50 Hz sinusoidal			21	A
PEAK GATE-TRIGGER CURRENT■:		I_{GTM}		
For 1 μs max.			0.5	A
GATE POWER DISSIPATION:■				
Peak (For 1 μs max.)		P_{GM}	10	W
Average:	T_C = 60°C	$P_{G(AV)}$	0.15	W
	T_A = 25°C		0.05	W
TEMPERATURE RANGE:				
Storage			-40 to +150	°C
Operating (case):	T2300 Series		-40 to +90	°C
	T2302 Series		-40 to +100	°C
	T2310, T2312 Series (From –40°C) Upper limits		See RCA data bulletin File No. 470	

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■ For V_D = 12 V (DC), R_L = 30 Ω, and T_C = 25°C	I^+	positive	positive	I_{GT}	3.5	10	mA
	III^-	negative	negative		3.5	10	
	I^-	positive	negative		7	10	
	III^+	negative	positive		7	10	
DC Gate-Trigger Voltage:●■ For V_D = 12 V (DC) and R_L = 30 Ω At T_C = 25°C				V_{GT}	1	2.2	V

PACKAGES: Modified JEDEC TO-5 (T2300, T2302 Series)
Modified JEDEC TO-5 with Heat Radiator (T2310, T2312 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 470.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State Division

Thyristors T2304 T2305 Series

400-Hz, 0.5-A Sensitive-Gate Silicon Triacs

BASIC RATINGS:
For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

	Symbol	T2304B T2305B	T2304D T2305D	Units
REPETITIVE PEAK OFF-STATE VOLTAGE:●	V_{DROM}			
Gate open, T_J = −65 to 100°C		200	400	V
RMS ON-STATE CURRENT (Conduction angle = 360°):	$I_{T(RMS)}$			
Case temperature T_C = 70°C		0.5		A
Ambient temperature T_A = 25°C (without heat sink)		0.4		A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}			
For one cycle of applied prinicpal voltage				
400 Hz (Sinusoidal)		50		A
60 Hz (Sinusoidal)		25		A
RATE OF CHANGE OF ON-STATE CURRENT:				
$V_{DM} = V_{DROM}$, I_{GT} = 60 mA, t_r = 0.1 μs	di/dt	100		A/μs
FUSING CURRENT (for Triac Protection):				
T_J = −65 to 100°C t = 1.25 to 10 ms	I^2t	2		A^2s
PEAK GATE-TRIGGER CURRENT:■	I_{GTM}			
For 1 μs max.		1		A
GATE POWER DISSIPATION:	P_{GM}			
Peak (For 1 μs max.)		10		W
TEMPERATURE RANGE:				
Storage	T_{stg}	−50 to 150		°C
Operating (Case)	T_C	−50 to 100		°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■							
For V_D = 12 V (dc)	I+	positive	positive	I_{GT}	5	25	mA
R_L = 30 Ω	III−	negative	negative		5	25	
T_C = 25°C	I−	positive	negative		10	40	
	III+	negative	positive		10	40	
DC Gate-Trigger Voltage:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	1	2.2	V

PACKAGE: Modified JEDEC TO-5

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 441.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State Division

Thyristors
T2700 T2710 Series

6-Ampere Silicon Triacs

BASIC RATINGS

For Operation with Sinusoidal Supply Voltage at Frequencies of 50/60 Hz, and with Resistive or Inductive Load.

		T2700B T2710B	T2700D T2710D	
REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate Open, for T_J = −65 to +100°C	V_{DROM}	200	400	V
RMS ON-STATE CURRENT For case temperature (T_C) of +75°C and a conduction angle of 360°	$I_{T(RMS)}$	6	6	A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied prinicpal voltage	I_{TSM}	100	100	A
FUSING CURRENT (for triac protection): T_J = −65 to 100°C, t = 1.25 to 10 ms	I^2t	50	50	A^2s
PEAK GATE-TRIGGER CURRNET:■ For 1 μs max.	I_{GTM}	4	4	A
GATE POWER DISSIPATION:■ Peak (For 1 μs max., $I_{GTM} \leqslant 4$ A (peak)	P_{GM}	16	16	W
TEMPERATURE RANGE:				
Storage	T_{stg}	−65 to +150		°C
Operating (Case)	T_C	−65 to +100		°C

GATE CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current: ● ■ For V_D = 12 volts (DC), R_L = 12 Ω T_C = +25°C, and specified triggering mode:	I_{GT}			mA
I+ Mode: positive V_{MT2}, positive V_{GT}		15	25	
III- Mode: negative V_{MT2}, negative V_{GT}		15	25	
I- Mode: positive V_{MT2}, negative V_{GT}		25	40	
III+ Mode: negative V_{MT2}, positive V_{GT}		25	40	
DC Gate-Triggering Volgate: ● ■ For V_D = 12 volts (DC) and R_L = 12 Ω At T_C = +25°C	V_{GT}	1	2.2	V

PACKAGE: JEDEC TO-66 (T2700 Series)
JEDEC TO-66 with Heat Radiator (T2710 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 351.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_{GT}) with reference to main terminal 1.

Solid State
Division

Thyristors
T4103 T4104 T4105
T4113 T4114 T4115
Series

400-Hz, 6,10, & 15-A Silicon Triacs

BASIC RATINGS:
For Operation with Sinusoidal Supply Voltage at Frequencies up to 400 Hz and with Resistive or Inductive Load.

		T4103B T4104B T4105B	T4113B T4114B T4115B	T4103D T4104D T4105D	T4113D T4114D T4115D	
REPETITIVE PEAK OFF-STATE VOLTAGE:●	V_{DROM}					
Gate open, T_J = −50 to 100°C		200		400		V
RMS ON-STATE CURRENT (Conduction angle = 360°):	$I_{T(RMS)}$					
Case temperature						
T_C = 90°C (T4105B, T4105D, T4115B, T4115D)		6				A
= 85°C (T4104B, T4104D, T4114B, T4114D)		10				A
= 80°C (T4103B, T4103D, T4113B, T4113D)		15				A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}					
For one cycle of applied principal voltage						
400 Hz (Sinusoidal)		200				A
60 Hz (Sinusoidal)		100				A
RATE OF CHANGE OF ON-STATE CURRENT:						
$V_{DM} = V_{DROM}$, I_{GT} = 160 mA, t_r = 0.1 μs	di/dt	150				A/μs
FUSING CURRENT (for triac protection):	I^2t					
T_J = −50 to 100°C, t = 1.25 to 10 ms		3				A^2s
PEAK GATE-TRIGGER CURRENT:■	I_{GTM}					
For 1 μs max.		4				A
GATE POWER DISSIPATION:	P_{GM}					
Peak (For 1 μs max., $I_{GTM} \leq 4$ A)		16				W
TEMPERATURE RANGE:						
Storage	T_{stg}	−50 to 150				°C
Operating (Case)	T_C	−50 to 100				°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■							
For V_D = 12 V (dc),	I^+	positive	positive	I_{GT}	20	50	mA
R_L = 30 Ω,	III−	negative	negative		20	50	
T_C = 25°C	I−	positive	negative		35	80	
	III+	negative	positive		35	80	
DC Gate-Trigger Voltage:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	1	2.5	V

PACKAGE: Press-Fit (T4103, T4104, T4105 Series)
Stud (T4113, T4114, T4115 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 443.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State Division

Thyristors

T6401 T6411 T6421 Series

30-A Silicon Triacs

BASIC RATINGS:
For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

		T6401B T6411B T6421B	T6401D T6411D T6421D	T6401M T6411M T6421M	
REPETITIVE PEAK OFF-STATE VOLTAGE:●	V_{DROM}				
Gate open, T_J = −50 to 100°C		200	400	600	V
RMS ON-STATE CURRENT (Conduction angle = 360°):	$I_{T(RMS)}$				
Case temperature					
T_C = 65°C (T6401 Series)			30		A
= 60°C (T6411 Series)			30		A
= 55°C (T6421 Series)			30		A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}				
For one cycle of applied principal voltage					
60 Hz (Sinusoidal)			300		A
50 Hz (Sinusoidal)			265		A
RATE OF CHANGE OF ON-STATE CURRENT:	di/dt				
$V_{DM} = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.1 μs			100		A/μs
FUSING CURRENT (for triac protection):	I^2t				
T_J = −40 to 100°C, t = 1.25 to 10 ms			450		A^2s
PEAK GATE-TRIGGER CURRENT:■	I_{GTM}				
For 1 μs max.			12		A
GATE POWER DISSIPATION:	P_{GM}				
Peak (For 1 μs max., $I_{GTM} \leq 4$ A)			40		W
TEMPERATURE RANGE:					
Storage	T_{stg}		−65 to 150		°C
Operating (Case)	T_C		−65 to 100		°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	I+	positive	positive	I_{GT}	15	50	mA
	III−	negative	negative		20	50	
	I−	positive	negative		30	80	
	III+	negative	positive		40	80	
DC Gate-Trigger Voltage:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	1.35	2.5	V

PACKAGES: Press-Fit (T6401 Series)
Stud (T6411 Series)
Isolated-Stud (T6421 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 459.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State
Division

Thyristors

T6404 T6405 T6414 T6415 Series

400-Hz, 25 & 40-A Silicon Triacs

BASIC RATINGS, *Absolute-Maximum Values:*
For Operation with Sinusoidal Supply Voltage at 400 Hz and with Resistive or Inductive Load.

	Symbol	T6404B T6405B T6414B T6415B	T6404D T6405D T6414D T6415D	
REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open, T_J = −50 to 110°C	V_{DROM}	200	400	V
RMS ON-STATE CURRENT (Conduction Angle = 360°): Case temperature	$I_{T(RMS)}$			
T_C = 85°C (T6405 Series)		25		A
= 80°C (T6415 Series)		25		A
= 70°C (T6404 Series)		40		A
= 65°C (T6414 Series)		40		A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied principal voltage	I_{TSM}			
400 Hz (Sinusoidal)		600		A
60 Hz (Sinusoidal)		300		A
RATE OF CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.1 μs	di/dt	100		A/μs
FUSING CURRENT (for Triac Protection): T_J = −50 to 110°C, t = 1.25 to 10 ms	I^2t	270		A^2s
PEAK GATE-TRIGGER CURRENT:■ For 1 μs max.	I_{GTM}	12		A
GATE POWER DISSIPATION: Peak (For 10 μs max., $I_{GTM} \leq$ 4 A (peak)	P_{GM}	42		W
TEMPERATURE RANGE: Storage	T_{stg}	−50 to 150		°C
Operating (Case)	T_C	−50 to 110		°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■							
For V_D = 12 V (dc),	I+	positive	positive	I_{GT}	20	80	mA
R_L = 30 Ω,	III−	negative	negative		50	80	
T_C = 25°C	I−	positive	negative		80	120	
	III+	negative	positive		80	120	
DC Gate-Trigger Voltage:● ■ For V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	2	3	V

PACKAGE: Press-Fit (T6404, T6405 Series)
Stud (T6414, T6415 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 487.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State Division

Thyristors

T8401B T8411B T8421B
T8401D T8411D T8421D
T8401M T8411M T8421M

60-A Silicon Triacs

BASIC RATINGS *For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.*		T8401B T8411B T8421B	T8401D T8411D T8421D	T8401M T8411M T8421M	
REPETITIVE PEAK OFF-STATE VOLTAGE:●	V_{DROM}				
Gate open, T_J = –40 to 110°C		200	400	600	V
RMS ON-STATE CURRENT (Conduction angle = 360°):	$I_{T(RMS)}$				
Case Temperature					
T_C = 85°C (T8401 Series)			60		A
= 80°C (T8411 Series)			60		A
= 75°C (T8421 Series)			60		A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}				
For one cycle of applied principal voltage					
60 Hz (sinusoidal)			600		A
50 Hz (sinusoidal)			500		A
RATE OF CHANGE OF ON-STATE CURRENT:					
$V_{DM} = V_{DROM}$, I_{GT} = 300 mA, t_r = 0.1 μs	di/dt		300		A/μs
FUSING CURRENT (for Triac Protection):					
T_J = –40 to 100°C, t = 1.25 to 10 ms	I^2t		1800		A^2s
PEAK GATE-TRIGGER CURRENT:■					
For 10 μs max.	I_{GTM}		7		A
GATE POWER DISSIPATION					
Peak (For 10 μs max., $I_{GTM} \leqslant$ 7 A (peak)	P_{GM}		42		W
TEMPERATURE RANGE:					
Storage	T_{stg}		–40 to 150		°C
Operating (Case)	T_C		–40 to 110		°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■							
For v_D = 12 V (dc)	I^+	positive	positive	I_{GT}	20	75	mA
R_L = 30 Ω	III^-	negative	negative		40	75	
T_C = 25°C	I^-	positive	negative		40	150	
	III^+	negative	positive		100	150	
DC Gate-Trigger Voltage:● ■ For v_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	1.35	2.8	V

PACKAGE: Press-Fit with Flexible Leads (T8401 Series)
Stud with Flexible Leads (T8411 Series)
Isolates-Stud with Flexible Leads (T8421 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 725.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State
Division

Thyristors

T8430 T8440 T8450 Series

80-A Silicon Triacs

BASIC RATINGS *For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.*		T8430B T8440B T8450B	T8430D T8440D T8450D	T8430M T8440M T8450M	
REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open, T_J = −40 to 110°C	V_{DROM}	200	400	600	V
RMS ON-STATE CURRENT (Conduction Angle = 360°): Case temperature	$I_{T(RMS)}$				
T_C = 75°C (T8430 Series)			80		A
= 65°C (T8440 Series)			80		A
= 55°C (T8450 Series)			80		A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied principal voltage	I_{TSM}				
60 Hz (sinusoidal)			850		A
50 Hz (sinusoidal)			720		A
RATE-OF-CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{DROM}$, I_{GT} = 300 mA, t_r = 0.1 μs	di/dt		300		A/μs
FUSING CURRENT (for Triac Protection): T_J = −40 to 110°C, t = 1.25 to 10 ms	I^2t		3600		A^2s
PEAK GATE-TRIGGER CURRENT:■ For 10 μs max.	I_{GTM}		7		A
GATE POWER DISSIPATION: Peak (For 10 μs max., $I_{GTM} \leq$ 7 A (peak)	P_{GM}		40		W
TEMPERATURE RANGE:					
Storage	T_{stg}		−40 to 150		°C
Operating (Case)	T_C		−40 to 110		°C

GATE CHARACTERISTICS	Mode	V_{MT2}	V_G	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current:● ■ For v_D = 12 V (dc) R_L = 30 Ω T_C = 25°C	I^+	positive	positive	I_{GT}	20	75	mA
	III^-	negative	negative		40	75	
	I^-	positive	negative		40	150	
	III^+	negative	positive		100	150	
DC Gate-Trigger Voltage:● ■ For v_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C				V_{GT}	1.35	2.5	V

PACKAGE: Press-Fit (T8430 Series)
Stud (T8440 Series)
Isolated-Stud (T8450 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 549.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Solid State
Division

Thyristors

2N681-2N690

25-A Silicon Controled Rectifiers

BASIC RATINGS:

	Symbol	2N681	2N682	2N683	2N684	2N685	2N686	2N687	2N688	2N689	2N690	Units
*NON-REPETITIVE PEAK REVERSE VOLTAGE:● Gate open	V_{RSOM}	35	75	150	225	300	350	400	500	600	720	V
NON-REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open	V_{DSOM}	35	75	150	225	300	350	400	500	600	720	V
*REPETITIVE PEAK REVERSE VOLTAGE:● Gate open	V_{RROM}	25	50	100	150	200	250	300	400	500	600	V
REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open	V_{DROM}	25	50	100	150	200	250	300	400	500	600	V

	Symbol	All types	Units
ON-STATE CURRENT: T_C = 65°C, conduction angle = 180°: RMS	$I_{T(RMS)}$	25	A
* Average	$I_{T(AV)}$	16	A
*PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one full cycle of applied principal voltage	I_{TSM}	150	A
RATE OF CHANGE OF ON-STATE CURRENT: $V_D = V_{DROM}$, I_{GT} = mA, t_r = 0.5 µs	di/dt		A/µs
FUSING CURRENT (for SCR protection): T_J = −65 to 125°C, t = 1 to 8.3 ms	I^2t		A^2s
*GATE POWER DISSIPATION:■ Peak Forward (for 10 µs max.)	P_{GM}	5	W
Average (averaging time = 10 ms max.)	$P_{G(AV)}$	0.5	W
*TEMPERATURE RANGE:■ Storage	T_{stg}	−65 to 150	°C
Operating (Case)	T_C	−65 to 125	°C

GATE CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNITS
DC Gate Trigger Current: V_D = 12 V (dc), R_L = 30 Ω, T_C = 125°C	I_{GT}	–	–	25	mA
* DC Gate Trigger Voltage: V_D = 12 V (dc), R_L = 30 Ω, T_C = 125°C	V_{GT}	0.25	–	–	V
= −65 to 125°C		–	–	3	V

PACKAGE: JEDEC TO-48

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 96.

* In accordance with JEDEC registration data format filed for the JEDEC (2N Series) types.
● These values do not apply if there is a positive gate signal. Gate must be open or negatively biased.
■ Any product of gate current and gate voltage which results in a gate power less than the maximum is permitted.

Solid State
Division

Thyristors

2N3228 2N3528
2N3525 2N3529
2N4101 2N4102

5-A Silicon Controlled Rectifiers

<table>
<tr><th>BASIC RATINGS:</th><th></th><th>2N3228</th><th>2N3525</th><th>2N4101</th><th>2N3528</th><th>2N3529</th><th>2N4102</th><th></th></tr>
<tr><td>NON-REPETITIVE PEAK REVERSE VOLTAGE .....</td><td>V_{RSOM}</td><td>330</td><td>660</td><td>700</td><td>330</td><td>660</td><td>700</td><td>V</td></tr>
<tr><td>REPETITIVE PEAK REVERSE VOLTAGE ....</td><td>V_{RROM}</td><td>200</td><td>400</td><td>600</td><td>200</td><td>400</td><td>600</td><td>V</td></tr>
<tr><td>REPETITIVE PEAK OFF-STATE VOLTAGE ....</td><td>V_{DROM}</td><td>200</td><td>400</td><td>600</td><td>200</td><td>400</td><td>600</td><td>V</td></tr>
<tr><td>ON-STATE CURRENT:
For case temperature (T_C) of +75°C,
and unit mounted on heat sink</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Average dc value at a conduction angle of 180° ...</td><td>$I_{T(AV)}$</td><td colspan="3">3.2</td><td>—</td><td>—</td><td>—</td><td>A</td></tr>
<tr><td>RMS Value ....</td><td>$I_{T(RMS)}$</td><td colspan="3">5.0</td><td>—</td><td>—</td><td>—</td><td>A</td></tr>
<tr><td>For free-air temperature (T_{FA}) of 25°C,
and with no heat sink employed</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Average dc value at a conduction angle of 180° ...</td><td>$I_{T(AV)}$</td><td>—</td><td>—</td><td>—</td><td colspan="3">1.3</td><td>A</td></tr>
<tr><td>RMS Value ....</td><td>$I_{T(RMS)}$</td><td>—</td><td>—</td><td>—</td><td colspan="3">2.0</td><td>A</td></tr>
<tr><td>PEAK SURGE CURRENT:
For one cycle of applied voltage ....</td><td>I_{TSM}</td><td colspan="6">60</td><td>A</td></tr>
<tr><td>FUSING CURRENT (For SCR protection)
For a period of 1 ms to 8.3 ms ....</td><td>I^2t</td><td colspan="6">15</td><td>A^2s</td></tr>
<tr><td>RATE OF CHANGE OF ON-STATE CURRENT
$V_{FB} = V_{BOO}$ (Min. value)
I_{GT} = 200 mA, 0.5 μs rise time</td><td>di/dt</td><td colspan="6">200</td><td>A/μs</td></tr>
<tr><td>GATE POWER:*
Peak, Forward or Reverse, for 10 μs duration ....</td><td>P_{GM}</td><td colspan="6">13</td><td>W</td></tr>
</table>

GATE CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current At T_C = +25°C	I_{GT}	8	15	mA (dc)
DC Gate-Trigger Voltage At T_C = 25°C	V_{GT}	1.2	2.0	V (dc)

PACKAGE: JEDEC TO-66 (2N3228, 2N3525, 2N4101)
JEDEC TO-8 (2N3528, 2N3529, 2N4102)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in RCA data bulletin No. 114.

*In accordance with JEDEC registration data format (JS-14, RDF-1) filed for the JEDEC (2N series) types.
•These values do not apply if there is a positive gate signal. Gate must be open or negatively biased.
▪Any product of gate current and gate voltage which results in a gate power less than the maximum is permitted.

Solid State Division

Thyristors

2N3650-2N3653, S7430M

35-A Silicon Controlled Rectifiers

BASIC RATINGS:		2N3650	2N3651	2N3652	2N3653	S7430M	
*NON-REPETITIVE PEAK REVERSE VOLTAGE: Gate open	V_{RSOM}	150	300	400	500	700	V
NON-REPETITIVE PEAK FORWARD VOLTAGE: Gate open	V_{DSOM}	150	300	400	500	700	V
*REPETITIVE PEAK REVERSE VOLTAGE: Gate open	V_{RROM}	100	200	300	400	600	V
*REPETITIVE PEAK OFF-STATE VOLTAGE: Gate open	V_{DROM}	100	200	300	400	600	V
*PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied principal voltage (60 Hz, sinusoidal)	I_{TSM}			180			A
ON-STATE CURRENT: For case temperature (T_C) = 25°C							
* Average DC value, conduction angle of 180°	$I_{T(AV)}$			25			A
RMS value	$I_{T(RMS)}$			35			A
*RATE OF CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{(BO)O}$, I_{GT} = 200 mA, t_r = 0.1 μs	di/dt			400			A/μs
*GATE POWER DISSIPATION: Peak Forward (for 10 μs max.)	P_{GM}			40			W
TEMPERATURE RANGE:							
Storage	T_{stg}			−65 to 150			°C
Operating (Case)	T_C			−65 to 120			°C

GATE CHARACTERISTICS	SYMBOL	Types 2N3650, 2N3651, 2N2652, 2N3653			Type S7430M			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
DC GATE TRIGGER CURRENT:								
V_D = 6 V (dc), R_L = 4 Ω, T_C = 25°C	I_{GT}	–	80	180	–	80	180	mA
V_D = 6 V (dc), R_L = 2 Ω, T_C = −65°C	I_{GT}	–	150	500*	–	150	500	mA
DC GATE TRIGGER VOLTAGE:								
V_D = 6 V (dc), R_L = 4 Ω, T_C = 25°C	V_{GT}	–	1.5	3	–	1.5	3	V
$V_D = V_{DROM}$, R_L = 200 Ω, T_C = 120°C	V_{GT}	0.25*	–	–	0.25	–	–	V
V_D = 6 V (dc), R_L = 2 Ω, T_C = −65°C	V_{GT}	–	2	4.5*	–	2	4.5	V

PACKAGE: JEDEC TO-48

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 408.

* In accordance with JEDEC registration data format (JS-14, RDF 1)—applies to the JEDEC (2N Series) types only.

Solid State Division

Thyristors

2N3654-2N3658, S7432M

35-A Silicon Controlled Rectifiers

BASIC RATINGS:		2N3654	2N3655	2N3656	2N3657	2N3658	S7432M	
*NON-REPETITIVE PEAK REVERSE VOLTAGE:● Gate open	V_{RSOM}	75	150	300	400	500	700	V
NON-REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open	V_{DSOM}	75	150	300	400	500	700	V
*REPETITIVE PEAK REVERSE VOLTAGE:● Gate open	V_{RROM}	50	100	200	300	400	600	V
*REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open	V_{DROM}	50	100	200	300	400	600	V
ON-STATE CURRENT: $T_C = 40°C$, conduction angle = 180°:								
RMS	$I_{T(RMS)}$	35						A
* Average	$I_{T(AV)}$	25						A
*PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one full cycle of applied principal voltage 60 Hz (sinusoidal)	I_{TSM}	180						A
*RATE OF CHANGE OF ON-STATE CURRENT: $V_D = V_{DROM}$, $I_{GT} = 200$ mA, $t_r = 0.1\ \mu s$	di/dt	400						A/µs
FUSING CURRENT (for SCR protection): $T_J = -65$ to 120°C, t = 1 to 8.3 ms	I^2t	165						A^2s
*GATE POWER DISSIPATION:■ Peak Forward (for 10 µs max.)	P_{GM}	40						W
*TEMPERATURE RANGE:								
Storage	T_{stg}	−65 to 150						°C
Operating (Case)	T_C	−65 to 120						°C

(Values in rows with a single entry apply to all types.)

TURN-OFF TIME CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNITS
*Circuit Commutated Turn-Off Time: (Sinusoidal Pulse) $V_{DX} = V_{DROM}$, $I_T = 100$ A, pulse duration = 1.5 µs, dv/dt = 200 V/µs, $V_{RX} = 30$ V min., $V_{GK} = 0$ V (at turn-off), $T_C = 115°C$	t_q	–	–	10	µs

PACKAGE: JEDEC TO-48

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 724.

* In accordance with JEDEC registration data format (JS-14, RDF-1) filed for the JEDEC (2N Series) types.
● These values do not apply if there is a positive gate signal. Gate must be open or negatively biased.
■ Any product of gate current and gate voltage which results in a gate power less than the maximum is permitted.

Solid State
Division

Thyristors

2N3668-2N3670 2N4103

12.5-A Silicon Controlled Rectifiers

BASIC RATINGS:		2N3668	2N3669	2N3670	2N4103	
NON-REPETITIVE PEAK REVERSE VOLTAGE	V_{RSOM}	150	300	660	700	V
REPETITIVE PEAK REVERSE VOLTAGE	V_{RROM}	100	200	400	600	V
REPETITIVE PEAK OFF-STATE VOLTAGE	V_{DROM}	100	200	400	600	V
ON-STATE CURRENT:						
For case temperature (T_C) of +80°C at conduction angle of 180°C,						
Average	$I_{T(AV)}$		8			A
RMS value	$I_{T(RMS)}$		12.5			A
PEAK SURGE CURRENT:						
For one cycle of applied voltage	I_{TSM}		200			A
FUSING CURRENT (for SCR protection)						
For a period of 1ms to 8.3ms	I^2t		165			A^2s
RATE OF CHANGE OF ON-STATE CURRENT..............	di/dt		200			A/μs
$V_{FB} = V_{BOO}$ (min. value) I_{GT} = 200 mA, 0.5μs rise time						
GATE POWER*						
Peak, Forward or Reverse, for 10μs duration	P_{GM}		40			W
TEMPERATURE:						
Storage	T_{stg}		−40 to +125			°C
Operating (Case)	T_C		−40 to +100			°C

GATE CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNITS
DC Gate-Trigger Current At T_C = +25°C	I_{GT}	1	20	40	mA (dc)
Gate-Trigger Voltage At T_C = +25°C	V_{GT}	–	1.5	2	V (dc)

PACKAGE: JEDEC TO-3

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in RCA data bulletin File No. 116.

*Any values of peak gate current or peak gate voltage to give the maximum gate power is permissible.

Solid State Division

Thyristors

2N3870-2N3873 2N3896-2N3899 S6400 S6410 S6420 Series

35-A Silicon Controlled Rectifiers

BASIC RATINGS		2N3870 2N3896 S6420A	2N3871 2N3897 S6420B	2N3872 2N3898 S6420D	2N3873 2N3899 S6420M	S6400N S6410N S6420N	
*NON-REPETITIVE PEAK REVERSE VOLTAGE:▲ Gate Open	V_{RSOM}	150	330	660	700	900	V
NON-REPETITIVE PEAK OFF- STATE VOLTAGE:▲ Gate Open	V_{DSOM}	150	330	660	700	900	V
*REPETITIVE PEAK REVERSE VOLTAGE:▲ Gate Open	V_{RROM}	100	200	400	600	800	V
*REPETITIVE PEAK OFF-STATE VOLTAGE:▲ Gate Open	V_{DROM}	100	200	400	600	800	V
ON-STATE CURRENT: T_C = 65°C♦, conduction angle = 180°:							
RMS	$I_{T(RMS)}$			35			A
* Average	$I_{T(AV)}$			22			A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one full cycle of applied principal voltage	I_{TSM}						
* 60 Hz (sinusoidal)				350			A
50 Hz (sinusoidal)				300			A
RATE OF CHANGE OF ON-STATE CURRENT: $V_D = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.5 μs	di/dt			200			A/μs
FUSING CURRENT (for SCR protection): T_J = −40 to 100°C, t = 1 to 8.3 ms	I^2t			300			A^2s
GATE POWER DISSIPATION:● Peak Forward (for 10 μs Max.)	P_{GM}			40			W
*TEMPERATURE RANGE:							
Storage	T_{stg}			−40 to 125			°C
Operating (Case)	T_C			−40 to 100			°C

GATE CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNITS
DC Gate Trigger Voltage:					
V_D = 12 V (dc), R_L = 30 Ω, T_C = -40°C	V_{GT}	–	1.5	3*	V
V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C		–	1.1	2	
DC Gate Trigger Current:					
V_D = 12 V (dc), R_L = 30 Ω, T_C = -40°C	I_{GT}	–	46	80*	mA
V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C		1	25	40	

PACKAGE: Press-Fit (2N3870-2N3873, T6400N)
Stud (2N3896-2N3899, T6410N)
Isolated-Stud (S6420A, B, D, M, N)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 578.

* In accordance with JEDEC registration data filed for the JEDEC (2N-series) types.
▲ These values do not apply if there is a positive gate signal. Gate must be open or negatively biased.
♦ T_C = 60° for isolated-stud package types.
● Any product of gate current and gate voltage which results in a gate power less than the maximum is permitted.

Solid State
Division

Thyristors

S2400 Series

4.5-A Silicon Controlled Rectifiers For Capacitive-Discharge Systems

BASIC RATINGS:		S2400A	S2400B	S2400D	S2400M	
NON-REPETITIVE PEAK REVERSE VOLTAGE:▲ Gate open	V_{RSOM}	100	200	400	600	V
NON-REPETITIVE PEAK FORWARD VOLTAGE:▲ Gate open	V_{DSOM}	150	250	500	700	V
REPETITIVE PEAK REVERSE VOLTAGE:▲ Gate open	V_{RROM}	100	200	400	600	V
REPETITIVE PEAK OFF-STATE VOLTAGE:▲ Gate open	V_{DROM}	100	200	400	600	V
ON-STATE CURRENT: T_C = 75°C, conduction angle = 180°:						
RMS	$I_{T(RMS)}$		4.5			A
Average	$I_{T(AV)}$		3.3			A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied principal voltage	I_{TSM}					
50 Hz, (Sinusoidal)			170			A
60 Hz, (Sinusoidal)			200			A
RATE OF CHANGE OF ON-STATE CURRENT: $V_D = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.5 μs	di/dt		200			A/μs
FUSING CURRENT (for SCR Protection): T_J = −40 to 100°C, t = 1.5 to 10 ms	I^2t		150			A^2s
GATE POWER DISSIPATION:● Peak forward (for 1 μs max.)	P_{GM}		40			W
TEMPERATURE RANGE:■						
Storage	T_{stg}		−40 to 150			°C
Operating (Case)	T_C		−40 to 100			°C

GATE CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Voltage: V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	V_{GT}	1.1	2	V
DC Gate-Trigger Current: V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	I_{GT}	8	15	mA

PACKAGE: JEDEC TO-8

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 567.

▲These values do not apply if there is a positive gate signal. Gate must be open or negatively biased.
● Any product of gate current and gate voltage which results in a gate power less than the maximum is permitted.
■Temperature measurement point is shown on the DIMENSIONAL OUTLINE.

Solid State
Division

Thyristors

S2600 S2610 S2620 Series

7-Ampere "Low-Profile" Silicon Controlled Rectifiers

BASIC RATINGS		S2600B S2610B S2620B	S2600D S2610D S2620D	S2600M S2610M S2620M	
NON-REPETITIVE PEAK REVERSE VOLTAGE:● Gate open	V_{RSOM}	250	500	700	V
NON-REPETITIVE PEAK FORWARD VOLTAGE:● Gate open	V_{DSOM}	250	500	700	V
REPETITIVE PEAK REVERSE VOLTAGE:● Gate open	V_{RROM}	200	400	600	V
REPETITIVE PEAK OFF-STATE VOLTAGE:● Gate open	V_{DROM}	200	400	600	V
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied principal voltage	I_{TSM}				
60 Hz (sinusoidal)		100	100	100	A
50 Hz (sinusoidal)		85	85	85	A
PEAK REPETITIVE ON-STATE CURRENT:† Duty factor = 0.1%, T_C = 75°C Pulse duration = 5 μs (min.), 20 μs (max.)		100	100	100	A
RATE OF CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.5 μs	di/dt		200		A/μs
FUSING CURRENT (for SCR protection): T_J = −65 to 100°C, t = 1 to 8.3 ms	I^2t		40		A^2s
GATE POWER DISSIPATION:▲ Peak Forward (for 1 μs max.)	P_{GM}	40	40	40	W
TEMPERATURE RANGE: Storage	T_{stg}		−65 to +150		°C
Operating (Case)	T_C		−65 to +100		°C

GATE CHARACTERISTICS	SYMBOLS	S2600 Series		S2610 Series S2620 Series		UNITS
		TYP.	MAX.	TYP.	MAX.	
DC GATE TRIGGER CURRENT: V_D = 12 V (DC), R_L = 30 Ω, T_C = +25°C	I_{GT}	6	15	6	15	mA
DC GATE TRIGGER VOLTAGE: V_D = 12 V (DC), R_L = 30 Ω, T_C = +25°C	V_{GT}	0.65	1.5	0.65	1.5	V

PACKAGE: Low-Profile TO-5 (S2600 Series)
Low-Profile TO-5 with Heat Radiator (S2610 Series)
Low-Profile TO-5 with Heat Spreader (S2620 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 496.

† When rms current exceeds 4 amperes (maximum rating for the anode lead), connection must be made to the case.
● These values do not apply if there is a positive gate signal. Gate must be open, terminated, or have negative bias.
▲ Any values of peak gate current or peak gate voltage that yeild the maximum gate power are permissible.

Solid State Division

Thyristors

S3700 Series

5-Ampere All-Diffused Silicon Controlled Rectifiers for Inverter Applications

BASIC RATINGS		S3700B	S3700D	S3700M	
NON-REPETITIVE PEAK REVERSE VOLTAGE:	V_{RSOM}				
Gate Open		330	660	700	V
REPETITIVE PEAK REVERSE VOLTAGE:	V_{RROM}				
Gate Open		200	400	600	V
REPETITIVE PEAK OFF-STATE VOLTAGE:	V_{DROM}				
Gate Open		200	400	600	V
ON-STATE CURRENT:					
For case temperature of +60°C and 60 Hz:					
Average DC value at a conduction angle of 180°	$I_{T(AV)}$	3.2	3.2	3.2	A
RMS value	$I_{T(RMS)}$	5	5	5	A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}				
TEMPERATURE RANGE:					
Storage	T_{stg}		−40 to +150		°C
Operating (Case)	T_C		−40 to +100		°C

TURN-OFF TIME CHARACTERISTICS	SYMBOLS	S3700B		S3700D		S3700M		UNITS
		Typ.	Max.	Typ.	Max.	Typ.	Max.	
Circuit-Commutated Turn-Off Time, (Reverse Recovery Time + Gate Recovery Time) $V_{DX} = V_{(BO)O}$ rated value, I_{TM} = 2A, 50μs min. pulse width, V_{RX} = 80 V min., rise time = 0.1μs, dv/dt = 100 V/μs, di_R/dt = 10 A/μs, I_{GT} = 100 mA at turn-on, V_{GT} = 0 V at turn-off, and T_C = +80°C	t_q	4	6	4	6	4	6	μs

PACKAGE: JEDEC TO-66

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 306.

Solid State
Division

Thyristors

S3701M

5-Ampere Silicon Controlled Rectifier

BASIC RATINGS:

REPETITIVE PEAK OFF-STATE VOLTAGE:	V_{DROM}		
Gate open		600	V
RMS ON-STATE CURRENT (Conduction angle = 180°):	$I_{T(RMS)}$	5	A
REPETITIVE PEAK ON-STATE CURRENT (0.2 μs Pulse Width):	I_{PM}		
Free-air cooling, f = 500 Hz		75	A
Free-air cooling, f = 5000 Hz		40	A
Infinite heat sink, f - 10,000 Hz		40	A
Infinite heat sink, f = 1,000 Hz		75	A
GATE POWER DISSIPATION:	P_{GM}		
Peak (for 10 μs pulse)		25	W
TEMPERATURE RANGE:			
Storage	T_{stg}	−40 to 125	°C
Operating (Case)	T_C	−40 to 100	°C

GATE CHARACTERISTICS	SYMBOL	MAX.	UNITS
DC Gate-Trigger Current: T_C = 25°C	I_{GT}	35	mA
DC Gate-Trigger Voltage: T_C = 25°C	V_{GT}	4	V

PACKAGE: JEDEC TO-66

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 476.

Solid State
Division

Thyristors

S3704 S3714 Series

5-A Silicon Controlled Rectifiers

BASIC RATINGS:

		S3704A S3714A	S3704B S3714B	S3704D S3714D	S3704M S3714M	S3704S S3714S	
NON-REPETITIVE PEAK REVERSE VOLTAGE:■ Gate open	V_{RSOM}	150	300	500	700	800	V
NON-REPETITIVE PEAK OFF-STATE VOLTAGE:■ Gate open	V_{DSOM}	150	300	500	700	800	V
REPETITIVE PEAK REVERSE VOLTAGE:■ Gate open	V_{RROM}	100	200	400	600	700	V
REPETITIVE PEAK OFF-STATE VOLTAGE:■ Gate open	V_{DROM}	100	200	400	600	700	V
ON-STATE CURRENT: T_C = 60°C, conduction angle = 180°:							
RMS	$I_{T(RMS)}$			5			A
Average	$I_{T(AV)}$			3.2			A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one full cycle of applied prinicpal voltage 60 Hz (Sinusoidal)	I_{TSM}			80			A
RATE OF CHANGE OF ON-STATE CURRENT: $V_D = V_{DROM}$, I_G = 50 mA, t_r = 0.1 μs	di/dt			200			A/μs
FUSING CURRENT (for SCR protection): T_J = −40 to 100°C, t = 1 to 8.3 ms	I^2t			25			A
GATE POWER DISSIPATION:●							
Peak Forward (for 10 μs max.)	P_{GM}			13			W
Peak Reverse (for 10 μs max.)	P_{RGM}			13			W
Average (averaging time = 10 ms max.)	$P_{G(AV)}$			0.5			W
TEMPERATURE RANGE:							
Storage	T_{stg}			−40 to 150			°C
Operating (Case)	T_C			−40 to 100			°C

TURN-OFF TIME CHARACTERISTIC	SYMBOL	TYP.	MAX.	UNITS
Circuit Commutated Turn-Off Time: $V_{DX} = V_{DROM}$, I_T = 2 A, pulse duration = 50 μs, dv/dt = 100 V/μs, −di/dt = −10 A/μs, I_{GT} = 100 mA, V_{GT} = 0 V (at turn-off), T_C = 80°C	t_q	4	8	μs

PACKAGE: JEDEC TO-66 (S3704 Series)
JEDEC TO-66 with Heat Radiator (S3714 Series)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 690.

■ These values do not apply if there is a positive gate signal. Gate must be open or negatively biased.
● Any product of gate current and gate voltage which results in a gate power less than the maximum is permitted.

Solid State
Division

Thyristors

S6200 S6210 S6220 Series

20-Ampere Silicon Controlled Rectifiers

BASIC RATINGS:		S6200A S6210A S6220A	S6200B S6210B S6220B	S6200D S6210D S6220D	S6200M S6210M S6220M	
NON-REPETITIVE PEAK REVERSE VOLTAGE: Gate open	V_{RSOM}	100	200	400	600	V
NON-REPETITIVE PEAK FORWARD VOLTAGE: Gate open	V_{DSOM}	150	250	500	700	V
REPETITIVE PEAK REVERSE VOLTAGE: Gate open	V_{RROM}	100	200	400	600	V
REPETITIVE PEAK OFF-STATE VOLTAGE: Gate open	V_{DROM}	100	200	400	600	V
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}					
For one cycle of applied principal voltage						
50 Hz (Sinusoidal)		170				A
60 Hz (Sinusoidal)		200				A
ON-STATE CURRENT:						
For case temperature (T_C) = 75°C, conduction angle of 180°:						
Average DC value	$I_{T(AV)}$	12.5				A
RMS value	$I_{T(RMS)}$	20				A
RATE OF CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{(BO)O}$, I_{GT} = 200 mA, t_r = 0.5 μs	di/dt	200				A/μs
FUSING CURRENT (for SCR protection): T_J = −65 to 100°C, t = 1 to 8.3 ms	I^2t	170				A^2s
GATE POWER DISSIPATION: Peak Forward (for 10 μs max.)	P_{GM}	40				W
TEMPERATURE RANGE:						
Storage	T_{stg}	−65 to 150				°C
Operating (Case)	T_C	−65 to 100				°C

GATE CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current: V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	I_{GT}	8	15	mA
DC Gate-Trigger Voltage: V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	V_{GT}	1.1	2	V

PACKAGE: Press-Fit (S6200)
Stud (S6210)
Isolated-Stud (S6220)

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in the RCA data bulletin File No. 418.

Solid State
Division

Thyristors

S6431M

35-A Silicon Controlled Rectifiers

BASIC RATINGS:

NON-REPETITIVE PEAK REVERSE VOLTAGE	V_{RSOM}	720	V
REPETITIVE PEAK REVERSE VOLTAGE	V_{RROM}	600	V
REPETITIVE PEAK OFF-STATE VOLTAGE	V_{DROM}	600	V
ON-STATE CURRENT:			
For case temperature of +65°C			
RMS value	$I_{T(RMS)}$	35	A
PEAK PULSE CURRENT		900	A
DYNAMIC DISSIPATION:			
For case temperature of +65°C		30	W
GATE POWER:*			
Peak, Forward or Reverse, for 10 μs duration	P_{GM}	40	W
TEMPERATURE:			
Storage	T_{stg}	−65 to +150	°C
Operating (Case)	T_C	−65 to +125	°C

GATE CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNITS
DC Gate-Trigger Current At T_C = +25°C	I_{GT}	25	80	mA (dc)
DC Gate-Trigger Voltage At T_C = +25°C	V_{GT}	1.1	2	V (dc)

PACKAGE: JEDEC TO-48

The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are given in RCA data bulletin No. 247.

*Any values of peak gate current or peak gate voltage to give the maximum gate power is permissible.

High-Reliability Integrated Circuits

High-Reliability Integrated Circuits

RCA offers high-reliability versions of a broad range of standard COS/MOS and linear integrated circuits that are processed in accordance with MIL-STD-883 (Military Standard for Test Methods, Microelectronics). In addition, twenty-seven COS/MOS integrated circuits are currently being "qualified" to meet the requirements of MIL-M-38510 (Military Standard for Microelectronics or Integrated Circuits). RCA plans to qualify a number of its more than 100 standard linear integrated circuits in accordance with MIL-M-38510 in the future.

RCA also offers a broad line of high-reliability integrated-circuit chips for use in hybrid circuits. Standard chips are normally inspected to MIL-STD-883, Method 2010.1, Condition B Visual. Chips subjected to the more critical Condition A Visual inspections and to SEM (scanning-electron-microscope) inspections are also available.

General Considerations

RCA high-reliability integrated circuits are supplied in hermetically sealed packages that are specially engineered and developed to meet the requirements of military, aerospace, and critical industrial applications. Most COS/MOS devices are supplied in either the dual-in-line package shown in Fig. 5-1(a) or the flat pack shown in Fig. 5-1(b). These packages feature a ceramic body with a welded cap. They are light in weight and can safely withstand the thermal shock levels specified by MIL-STD-883, Method 1011, Condition C. The flat pack and dual-in-line package have been in use since 1964, and the excellent reliability exhibited by these packages has been firmly established. Many currently available RCA high-reliability linear integrated circuits are supplied in the TO-5 style package shown in Fig. 5-1(c).

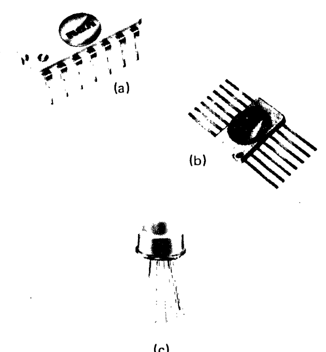


Fig. 5-1– Packages used for RCA high-reliability integrated circuits: (a) dual-in-line ceramic package; (b) ceramic flat pack; (c) TO-5-style package.

For all COS/MOS and many linear integrated circuits, the package in which a particular type is supplied is identified by the letter "D" (dual-in-line ceramic), "K" (ceramic flat pack), or "T" (TO-5 style in the device type-number designation. The charts shown in Figs. 5-2 and 5-3 illustrate how the device type number may be used to define the basic device, the reliability class, the type of package, and the lead finish for RCA high-reliability integrated circuits processed in accordance with MIL-STD-883 or MIL-M-38510, respectively.

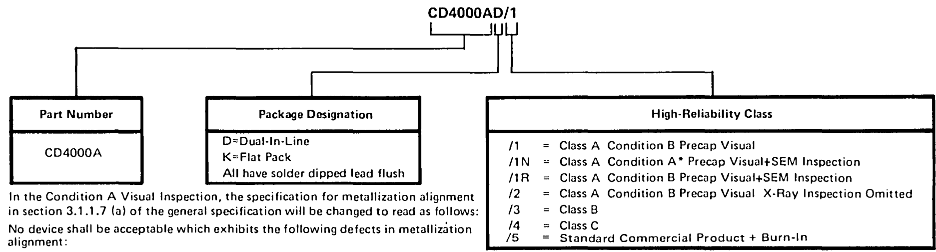
RCA high-reliability integrated-circuit products are currently being used for a broad variety of functions in military, aerospace, and critical industrial applications. Table 5-1 lists a few typical examples of the use of RCA high-reliability COS/MOS and linear integrated circuits in satellite and military systems.

Manufacturing Controls

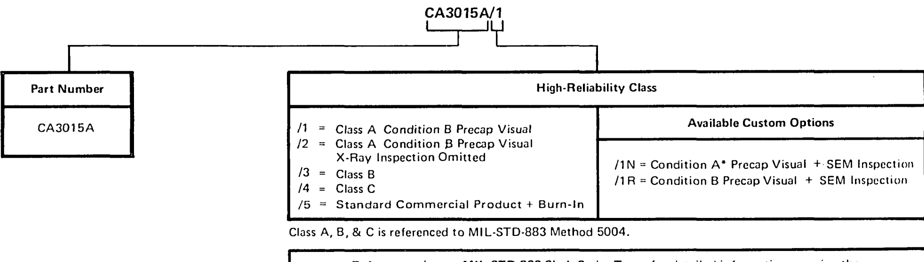
RCA high-reliability integrated circuits are processed in accordance with the Product Assurance Program defined in Appendix A of MIL-M-38510. The program includes the following items:

1. A clearly defined procedure for the conversion of a customer specification into an RCA internal specification with built-in safeguards to assure the customer that the delivered parts meet or exceed his specification requirements.
2. A formalized personnel training and testing program which assures that each operation is performed correctly.
3. A complete inspection of incoming materials, utilities, and work in process using on-site facilities such as scanning-electron-microscope, gas-chromatography, atomic-absorption, and X-ray equipment.
4. Maintenance of cleanliness in work areas, e.g., all critical operations are performed in a Class 100 environment.
5. Rigorous control over changes in design, materials, and processes with documentation kept in active files for a minimum of three years and in inactive files for a minimum of 20 years.
6. Tool and test equipment maintenance and calibration in strict accordance with MIL-C-45662, "Calibration System Requirements".
7. A quality-assurance program in accordance with MIL-Q-9858, "Quality Program Requirements".

Detailed processing and screening requirements for RCA high-reliability integrated circuits are defined subsequently in the discussions of MIL-STD-883 and MIL-M-38510 Requirements.



(a) COS/MOS Integrated Circuits



(b) Linear Integrated Circuits

Fig. 5-2– Guide to the reliability class, package, and lead finish of RCA high-reliability (slash-number series) integrated circuits processed in accordance with MIL-STD-883.

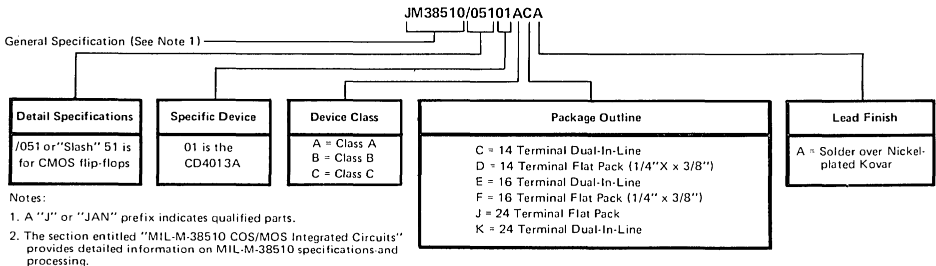


Fig. 5-3– Guide to the reliability class, package, and lead finish of RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-M-38510.

Table 5-1— A Few Typical Examples of Satellite and Military Applications of RCA High-Reliability Integrated Circuits.

RCA High Reliability COS/MOS integrated circuits are now being used in, or are being designed into the following systems:	
Satellites	**Military Equipment**
Pioneer F Experimental	Airborne Control
ATS – Series F and G	Data Buoy Platform
NIMBUS	Atmospheric Digital Equipment
HELIOS	F-15 Aircraft Equipment
ITOS	Ground Digital Equipment (Tanks)
HEOS	Oceanographic Digital Equipment
APOLLO-15	Army Digital Equipment
Atmospheric Explorer, AE (Experimenters and Flight-Hardware Usage, Several Thousand)	Navy Digital Equipment
Classified Satellites	Fuze and Arming Equipment
UK 4 (British/American)	AWAC Program
IMP Satellites	Navy Sonobuoy
Earth Resources Technical Satellite, ERTS	TAC Fire-Control System
Dual Air-Density Satellite (DADS)	PRC-85
AIRS Program	Aircraft Ground Control
Tenley Program	
SATCOM	
Space Shuttle	
LANS Program	

RCA High-Reliability Linear Integrated Circuits are now used in, or are being designed into, the following systems:	
Military Communications	**AFGIS Radar (Navy)**
ARC-150	**Missiles**
ARC-164	SAM-D
PRC-85	BULL-DOG
PRC-25	CONDOR
PRC-77	NIKE-X
F-15 Aircraft Equipment	**Other Classified Equipments**
AEGIS Program	
B-1 Bomber	

MIL-STD-833 Requirements

RCA Solid State Division offers a broad range of COS/MOS and linear integrated circuits processed and screened in accordance with MIL-STD-883, Method 5004, Class A, B, or C requirements. These devices are used in satellities and other aerospace, military, and critical industrial applications in which maintenance is extremely difficult. RCA high-reliability integrated circuits are provided in four basic screening levels (/1, /2, /3, and /4), as shown in Table 5-2. The basic /1 level has been subdivided to include two higher screening levels (/1N and /1R) as indicated in the table. These levels, which are marked on the device package following the type-number designation, meet the mechanical and electrical screening requirements of MIL-STD-883, imposed before the devices are sealed, and the screening tests required on packaged parts. RCA offers a /2 part which meets Class A requirements of MIL-STD-883 less radiographic inspection since the aluminum metallization and bonding wires do not show up under this inspection.

The product flow for RCA high-reliability integrated circuits processed in accordance with MIL-STD-883 is shown in Fig. 5-4. After wafer processing, special visual inspections are performed to MIL-STD-883, Method 2010.1, Condition B or A at both chip and pre-seal inspections to assure a packaged chip of high reliability. In the case of Class A product (RCA levels /1 and /2), parts are tested functionally, and then receive a dc parameter test; significant parameters are recorded.

A 240-hour burn-in at 125°C is performed on all parts. All readings are repeated, and delta shifts calculated. The customer is provided with print-outs of these parameters identified by the serial number on the part. The parts then go through 100-per-cent high- and low-temperature testing under functional and dc operating conditions. Next, 100-per-cent ac testing is accomplished followed by Group A sampling of all test conditions. The Class A product is branded, visually inspected, and retested both functionally and to dc parameters prior to packaging and shipment to the customer. The screening tests for Class B (RCA level /3) and Class C (RCA level /4) devices are reduced as shown in Table 5-3 in which X designates that a test is performed 100 per cent and S indicates that the test is a screen. For Class-B devices, the main difference is that burn-in is for 168 hours with GO-NO/GO parameter readings made before and after burn-in. Temperature testing is done on a sampling basis, and visual inspection prior to sealing is not as critical. Class-C devices are tested similarly to Class-B devices less the burn-in, temperature, and ac tests.

COS/MOS Integrated Circuits—All RCA high-reliability COS/MOS products are subjected to 100-per-cent production electrical tests after group A, quality testing and branding. Table 5-4 shows the test criteria for all product series. At a temperature of 25°C, all product series are 100-per-cent functionally tested at voltage extremes to guarantee 3- and 15-volt operation. Parametric tests are performed at 5 and 10 volts. High and low temperature plus dynamic (ac) testing is performed on high-reliability products.

Table 5-5 presents the group A electrical sampling criteria which are used to retest a portion of the product to assure that the 100-per-cent or other test parameters

Table 5-2— RCA Integrated-Circuit Screening Levels

Screening Levels▲		Application	Description
RCA Levels	Equivalent to MIL-STD-883, Method 5004.1		
For Packaged Devices			
/1N	Class A with SEM* Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **impossible and reliability is imperative**
/1R	Class A with SEM* Inspection and Condition B Precap Visual Inspection		
/1	Class A with Condition B Precap Visual Inspection		
/2	Class A with Condition B Precap Visual Inspection. Radiographic Inspection Omitted	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **extremely difficult or impossible and reliability is imperative**
/3	Class B	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement **can be performed but are difficult and expensive**
/4	Class C	Military and Industrial For example, in Ground-Based Electronics	For devices intended for use where replacement **can readily be accomplished**
/5 Standard commercial plus burn-in	—	Commercial and Industrial	For devices intended for use where a higher level of reliability is required than can be provided by product without a burn-in
For Chips■			
/N	SEM* Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For hybrid applications where maintenance and replacement **are extremely difficult and reliability is imperative**
/R	SEM* Inspection and Condition B Precap Visual Inspection		
/M	Condition B Precap Visual Inspection	Military and Industrial	For general applications

*SEM – Scanning Electron Microscope Inspection per NASA Specification GSFC-S-311-P-12
▲For details on Condition A and Condition B Precap Visual Inspection, refer to MIL-STD-883 Method 2010.1
■ Lot acceptance testing for chips is available on a custom basis

meet guaranteed limits. The prime factor is LTPD (Lot-Tolerance-Per Cent-Defective); the referenced numbers specify the required sample size. Again, for special tests of temperature extremes and dynamic (ac) tests, either small quantities are tested, or high-reliability test data are used as judgment information.

Table 5-6 lists pre-burn-in and post-burn-in tests and delta limits for critical device parameters.

Group B and C testing is similar to that of MIL-STD-883 for all COS/MOS product series. The purpose of Group B and C tests is to show quality conformance of the product being manufactured over specific periods of time. Tables 5-7 and 5-8 present the ten subgroup tests referenced to MIL-STD-883, the test conditions, and acceptance criteria for all high-reliability COS/MOS products.

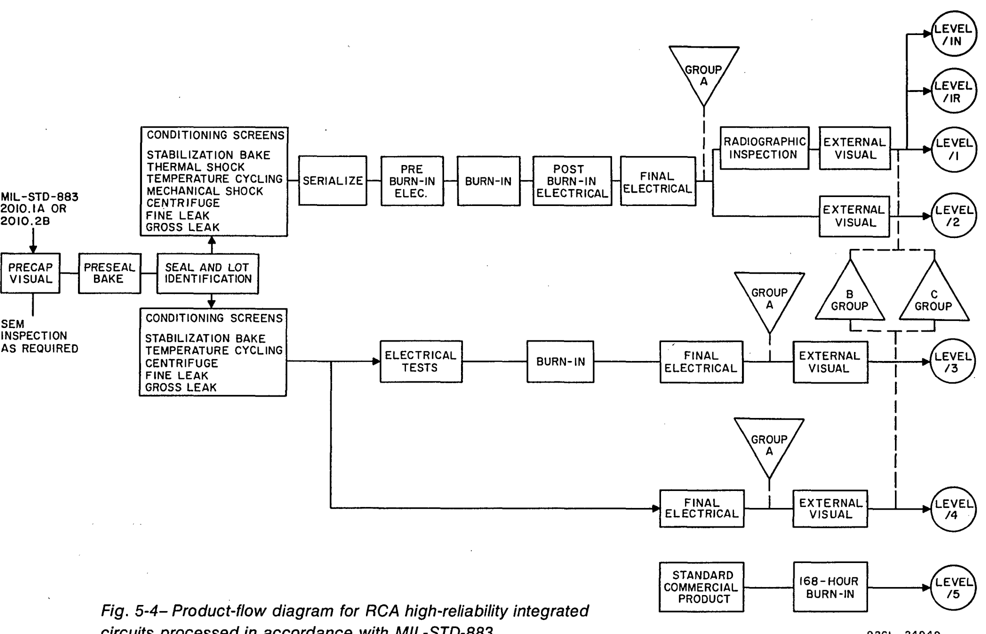


Fig. 5-4– Product-flow diagram for RCA high-reliability integrated circuits processed in accordance with MIL-STD-883.

Table 5-2— Description of RCA Integrated-Circuit Screening Levels

Test	Conditions	MIL-STD-883		RCA Screening Levels*					
		Method	Conditions	/1N	/1R	/1	/2	/3	/4
SEM Inspection	NASA Per GSFC-S-311-P-12	–	–	X	X	–	–	–	–
Precap Visual	–	2010.1	A	X	–	–	–	–	–
Precap Visual	–	2010.1	B	–	X	X	X	X	X
Preseal Bake	16 to 32 hrs at 200°C	–	–	X	X	X	X	X	X
Seal & Lot Identification	–	–	–	X	X	X	X	X	X
Stabilization Bake	48 hrs. at 150°C	1008	C	X	X	X	X	X	X
Thermal Shock	15 cycles	1011	C	X	X	X	X	–	–
Temperature Cycling	10 cycles	1010	C	X	X	X	X	X	X
Mechanical Shock	5 pulses, Y_1 direction	2002	B	X	X	X	X	–	–
Centrifuge	Y_2, Y_1 direction	2001	E	X	X	X	X	–	–
	Y_1 direction only	2001	E	–	–	–	–	X	X
Fine Leak	–	1014	A	X	X	X	X	X	X
Gross Leak	–	1014	C	X	X	X	X	X	X
Electrical Tests	See Note 1	–	–	X	X	X	X	X	–
Serialize	–	–	–	X	X	X	X	–	–
Pre Burn-in Electrical	See Note 2	–	–	X	X	X	X	–	–
Burn-in	240 hours	1015	B, D or E	X	X	X	X	–	–
	168 hours	1015	B, D or E	–	–	–	–	X	–
Post Burn-in Electrical	Delta Requirements	–	–	X	X	X	X	–	–

Table 5-3— Description of Total Lot Screening (X = 100% Testing) (cont'd)

Test	Conditions	MIL-STD-883		RCA Screening Levels*					
		Method	Conditions	/1N	/1R	/1	/2	/3	/4
Final Electrical	–	–	–	–	–	–	–	–	–
a) 25°C	see Table 4	–	–	X	X	X	X	X	X
b) -55 and +125°C	see Table 4	–	–	X	X	X	X	X	S
Radiographic Inspection	1 view	2012	–	X	X	X	–	–	–
External Visual	–	2009	–	X	X	X	X	X	X

Note 1: See specific type Slash (/) Series type data bulletin for test conditions and limits

* RCA screening level /5 consists of a 168-hour burn-in screen performed on standard commercial product. The ambient test temperature is the maximum possible without exceeding device thermal ratings. After burn-in, /5 devices meet all of the electrical requirements specified in the appropriate commercial data bulletin, Reference: RCA DATABOOK SSD-201.

Table 5-4— Final Electrical Tests

TEMPERATURE (T_A)	TEST	TEST CRITERIA		
		LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
+25°C	Selected Static Parameters	100%	100%	100%
+125°C	Selected Static Parameters	100%	100%	–
-55°C	Selected Static Parameters	100%	100%	–
+25°C	Selected Dynamic Parameters	100%	100%	–

Table 5-5— Group A Electrical Sampling Inspection

SUBGROUP	TEST	CONDITION	LTPD		
			LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Selected Static Parameters	T_A = +25°C	5	5	5
2	Selected Static Parameters	T_A = +125°C	5	7	10
3	Selected Static Parameters	T_A = -55°C	5	7	10
4	Selected Dynamic Parameters	T_A = +25°C	5	5	5

Table 5-6— Pre and Post Burn-In Electrical Tests and Delta Limits (T_A = 25°C)

CRITICAL PARAMETERS (at V_{DD} = 10 V)	SYMBOLS	LIMIT VALUES: For specific CD4000A Series Types and corresponding Δ limits for High-Reliability Versions *									
QUIESCENT DEVICE CURRENT	Total I_L(max)	0.1	0.5	1	2	5	10	15	25	50	Unit µA
	ΔI_L	0.05	0.2	0.3	0.5	1.0	1.3	1.5	2.5	5.0	µA
THRESHOLD VOLTAGE: "N" Channel	ΔV_{TH}"N"	←±0.3→									V
"P" Channel	ΔV_{TH}"P"	←±0.3→									V

CRITICAL PARAMETERS (at V_{DD} = 10 V)	SYMBOLS							Unit
DEVICE DRAIN CURRENT: Total	Total I_{DS}(min)	-0.1 - 0.5	0.5 - 2	2 - 5	5 - 10	10 - 25	25 - 50	mA
"N" Channel	ΔI_{DS}"N"	±0.1	±0.5	±0.75	±1	±2	±5	mA
"P" Channel	ΔI_{DS}"P"	±0.1	±0.5	±0.75	±1	±2	±5	mA

* For example, if a specific CD4000A Series type has a maximum quiescent device current of 0.5 µA at T_A = 25°C, RCA will test to a Δ limit of 0.2 µA for the high-reliability version of that type. In a similar manner, if a type has a quiescent device current rating of 5 µA, RCA will test to a Δ limit of 1.0 µA.

Table 5-7— Group B Environmental Sampling Inspection (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Physical Dimensions	2008	Test Cond. A per applicable data sheet	10	15	20
2	Marking Permanency	2008	Test Cond. B per Par. 3.2.1	← 4 devices (no failures) →		
	Visual and Mechanical	2008	Test Cond. B 10 X mag.	← 1 device (no failure) →		
	Bond Strength	2011	Test Cond. D 10 Devices minimum	5	15	20
3	Solderability	2003		10	15	15
4	Lead Fatigue	2004	Test Cond. B2 any 5 leads	10	15	15
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			

Note 1: Group B tests are performed on each inspection lot per requirements of MIL-M-38510.
Note 2: Operating life circuits are included in specific type high-reliability data bulletins.

Table 5-8— Group C Environmental Sampling Inspection (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Thermal Shock	1011	Test Cond. C	10	15	15
	Temperature Cycling	1010	Test Cond. C			
	Moisture Resistance	1004	No Voltage Applied			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests – Note 3					
2	Mechanical Shock	2002	Test Cond. B, 0.5 ms	10	15	15
	Vibration, Var. Freq.	2007	Test Cond. A			
	Constant Acceleration	2001	Test Cond. E			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Test – Note 3					
3	Salt Atmosphere	1009	Test Cond. A Omit Initial Conditioning	10	15	15
4	High Temp. Storage Critical Post Tests – Note 3	1008	Test Cond. C 1000 hours	7	7	7
5	Operating Life Critical Post Tests – Notes 2 and 3	1005	$T_A = 125°C$, 1000 hrs. Test Circuit (Note 2)	5	5	5
6	Steady State Bias Critical Post Tests – Note 3	1015	Test Cond. A, 72 hrs. At $T_A = 150°C$ (Note 3)	7	–	–

Note 1: Group C tests are performed at 3-month intervals for reliability history.
Note 2: Operating life circuits are included in specific type high-reliability data bulletins.
Note 3: Static parameters and limits are shown in High-Reliability Devices DATABOOK SSD-207, and in specific type high-reliability data bulletins.

Linear Integrated Circuits—Table 5-9 is a general guide to parameters that are tested for broad classifications of RCA high-reliability linear integrated circuits.

For RCA levels 1 and 2 (Class A) devices, the Table indicates the typical parameters that are recorded before and after burn-in. A device is rejected for failure to comply with these limits. The column headed MAX Δ shows the maximum change permitted in selected device parameters during burn-in. In installations where replacement is difficult or impossible, any readjustment to components for drifting is equally difficult or impossible.

For RCA level 3 (Class B) devices, only the minimum and/or maximum limits apply for burn-in. No values are recorded, and the tests are go/no-go.

RCA level 4 (Class C) devices are not subjected to burn-in.

Table 5-9— Pre- and Post-Burn-In Electrical-Test and Delta Limits for RCA High-Reliability Linear Integrated Circuits* (Typical Parameters)

OPERATIONAL AMPLIFIERS

Characteristics	Symbol	Test Conditions	Limits					Units
			Standard		Premium			
			Min.	Max.	Min.	Max.	MaxΔ	
Operational Transconductance Amplifiers (Example: CA3080A)								
Input Offset Voltage	V_{IO}	I_{ABC} = 500 mA**	–	5	–	2	±2	mV
Input Offset Current	I_{IO}	I_{ABC} = 500 mA**	–	0.5	–	0.5	±0.05	μA
Input Bias Current	I_I	I_{ABC} = 500 mA**	–	5	–	5	±0.25	μA
Transconductance	gm	I_{ABC} = 500 mA**	6700	13000	7700	12000	±3000	μmho
Operational Voltage Amplifiers (Example: CA3015A)								
Input Offset Voltage	V_{IO}	–	–	5	–	2	±1	mV
Input Offset Current	I_{IO}	–	–	5	–	1.6	±1	μA
Input Bias Current	I_I	–	–	24	–	6	±1	μA
Device Dissipation	P_D	No Load	110	240	110	240	±25	mW
		Output Shorted	320	600	320	600	±50	mW

DIFFERENTIAL AMPLIFIERS (Example: CA3028B)

Characteristics	Symbol	Limits			Units
		Min.	Max.	MaxΔ	
Input Bias Current	I_I	–	80	±8	μA
Input Offset Voltage	V_{IO}	–	5	±2	mV
Quiescent Operating Current (I_Q)	I_6 or I_8	2.5	4	±0.4	mA
Input Current (term. 7)	I_7	1	2.1	±0.2	mA
Device Dissipation	P_D	120	220	±24	mW

Table 4-9 — Pre- and Post-Burn-In Electrical-Test and Delta Limits for RCA High-Reliability Linear Integrated Circuits* (Typical Parameters) (Continued)

DEVICE ARRAYS

Characteristics	Symbol	Test Conditions	Limits			Units
			Min.	Max.	MaxΔ	
Diode Arrays (Example: CA3039)						
Forward Voltage Drop	V_F (Any Diode)	I_F = 0.2 ma		720	±10	mV
Forward Voltage Drop	V_F (Any Diode)	I_F = 1 ma		780	±10	mV
Forward Voltage Drop	V_F (Any Diode)	I_F = 20 ma		950	±10	mV
Transistor Arrays (Example: CA3018A)						
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μa, I_C = 0	5		±0.5	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		0.5	±0.15	μA
Input Current	I_I	I_C = 1 ma, V_{CE} = 3 V	5	25	±3	μA
Base-to-Emitter Voltage	V_{BE}	I_C = 1 ma, V_{CE} = 3 V	0.6	0.8	±0.10	V

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests and delta limits. Level %3 requires pre-burn-in electrical tests only.
** Programming Current

MIL-M-38510 Requirements for High-Reliability COS/MOS Integrated Circuits

Since 1970, RCA has been working closely with various aerospace and military agencies to qualify and provide COS/MOS devices to MIL-M-38510 specifications. Among these agencies are the NASA Goddard Space Flight Center, NASA Marshall Space Flight Center, NASA Headquarters Center in Washington, Rome Air Development Center, and the Defense Electronic Supply Center (DESC) at Dayton, a branch of the Defense Supply Agency.

MIL-M-38510 is the general specification for integrated circuits and the top document for MIL-STD-883. This general specification, introduced a year after MIL-STD-883 was in existence, adds a number of quality constraints not included in MIL-STD-883, which is a specification of test methods, procedures, and screening tests. Parts are provided to MIL-M-38510 under a series of /050 numbers of which nine are in existence. These nine numbers cover twenty-seven COS/MOS types. Parts meet requirements similar to those of Classes A, B, and C of MIL-STD-883, Method 5004 screening, except that additional requirements, including more test conditions and tightened limits, are imposed. The additional criteria for each class of product are designated by an X in Table 5-10. Also provided in MIL-M-38510 tests are PDA's (Per-Cent Defective Allowed) of 10 per cent for the three burn-in operations performed on Class-A product, and 10 per cent for the one burn-in of Class-B product. Table 5-11 provides a list of the COS/MOS devices for which MIL-M-38510 /050-number specification sheets have been written.

Table 5-10 — MIL-M-38510 requirements in addition to those of MIL-STD-883

Requirements	Class A	Class B	Class C
Product assurance plan	X	X	X
Manufacturing Certification	X	X	X
Line certification	X		
SEM inspection GSFC-S-311-P-12	X		
Radiographic NHB5300.4(3E)	X		
Two bias burn-in 36 hrs	X		–
Tighter DC electrical	X	X	X
Tighter AC electrical	X	X	X

Table 5-11 — COS/MOS devices for which specification sheets have been written.

Detailed Electrical Specification, MIL-M-38510	Device Covered
MIL-M-38510/050	
01	CD4011A
02	CD4012A
03	CD4023A
MIL-M-38510/051	
01	CD4013A
02	CD4027A
MIL-M-38510/052	
01	CD4000A
02	CD4001A
03	CD4002A
04	CD4025A
MIL-M-38510/053	
01	CD4007A
02	CD4019A
MIL-M-38510/054	
01	CD4008A
MIL-M-38510/055	
01	CD4009A
02	CD4010A
03	CD4049A
04	CD4050A
MIL-M-38510/056	
01	CD4017A
02	CD4018A
03	CD4020A
04	CD4022A
05	CD4024A
MIL-M-38510/057	
01	CD4006A
02	CD4014A
03	CD4015A
04	CD4021A
05	CD4031A
MIL-M-38510/058	
01	CD4016A

No other detailed electrical specifications have been defined by NASA or military agencies at this time. RCA plans to qualify most of the COS/MOS product line in the future.

Fig. 5-5 shows a product-flow diagram for RCA COS/MOS integrated circuits processed in accordance with MIL-M-38510.

Table 5-12 compares the general processing requirements for COS/MOS integrated circuits of MIL-STD-883 and MIL-M-38510, and Table 5-13 compares

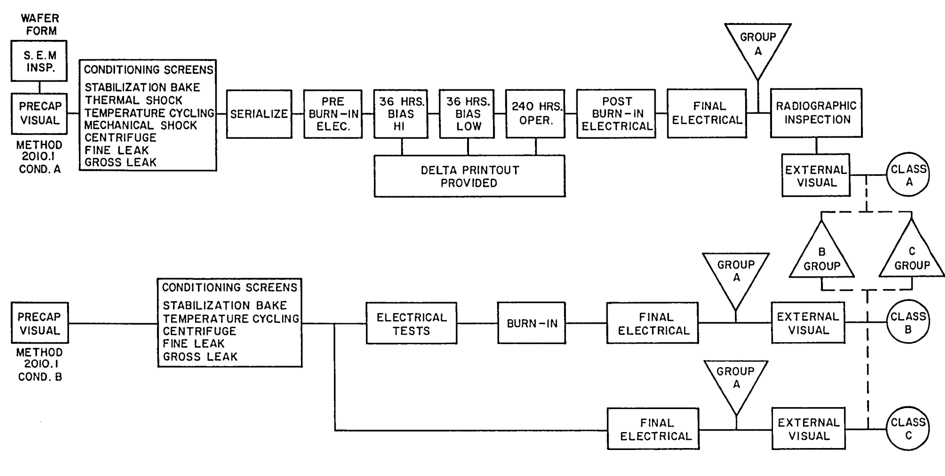


Fig. 5-5– Product flow diagram for RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-M-38510.

Table 5-12 – Comparison of MIL-STD-883 and MIL-M-38510 Processing and Screening Requirements for RCA High-Reliability COS/MOS Integrated Circuits.

	MIL-STD-883 METHOD	RCA MIL-STD-883 LEVEL						MIL-M-38510 CLASS		
		1N	1R	1	2	3	4	A	B	C
• Wafer										
SEM Inspection	GSFC-S-311-P-12*	X	X	–	–	–	–	X	–	–
• Assembly										
Precap Visual (Cond. A)	2010.1A	X	–	–	–	–	–	X	–	–
Precap Visual (Cond. B)	2010.1B	–	X	X	X	X	X	–	X	X
• Preconditioning										
Thermal Shock	1011C	X	X	X	X	–	–	X	–	–
Temperature Cycle	1010C	X	X	X	X	X	X	X	X	X
Mechanical Shock	2002B	X	X	X	X	–	–	X	–	–
Centrifuge Y1	2001E	–	–	–	–	X	X	–	X	X
Centrifuge Y1 & Y2	2001E	X	X	X	X	–	–	X	–	–
Fine Leak	1014A	X	X	X	X	X	X	X	X	X
Gross Leak	1014C	X	X	X	X	X	X	X	X	X
• Test and Burn-In										
Initial Test		X	X	X	X	X	–	X	X	–
Serialize		X	X	X	X	–	–	X	–	–
Bias Burn-In, Two 36-Hr. Deltas		–	–	–	–	–	–	X	–	–
Operating Burn-In, 240-Hr. Deltas	1015D, E	X	X	X	X	–	–	X	–	–
Operating Burn-In 168 Hrs.	1015D, E	–	–	–	–	X	–	–	X	–
Final Electrical DC 25°C		X	X	X	X	X	X	X	X	X
Final Electrical AC 25°C		X	X	X	X	X	S	X	X	S
Final Electrical DC −55°C		X	X	X	X	X	S	X	X	S
Final Electrical AC −55°C		–	–	–	–	–	–	S	S	S
Final Electrical DC +125°C		X	X	X	X	X	S	X	X	S
Final Electrical AC +125°C		–	–	–	–	–	–	S	S	S
• X-ray Inspection										
One View	2012	X	X	X	–	–	–	–	–	–
Two Views	NHB53004(3E)*	–	–	–	–	–	–	X	–	–

S = Sample X = 100% Testing – = Not Performed
*These specifications, developed by NASA, are required by MIL-M-38510.

the detailed screening requirements of these specifications for Class A COS/MOS integrated circuits.

In the processing of high-reliability COS/MOS integrated circuits, the wafer processing and metallization steps, the wafer finishing operations, and the wafer testing are the same as for standard-product COS/MOS devices. The major difference is that, for Class A parts, an SEM inspection step is inserted after the wafer processing and metallization, as shown in Fig. 5-6. After these four basic operations are completed, the tested wafer is subjected to the special high-reliability processing. As shown in Fig. 5-7, thirty-five additional processing and screening operations are required for Class A COS/MOS parts.

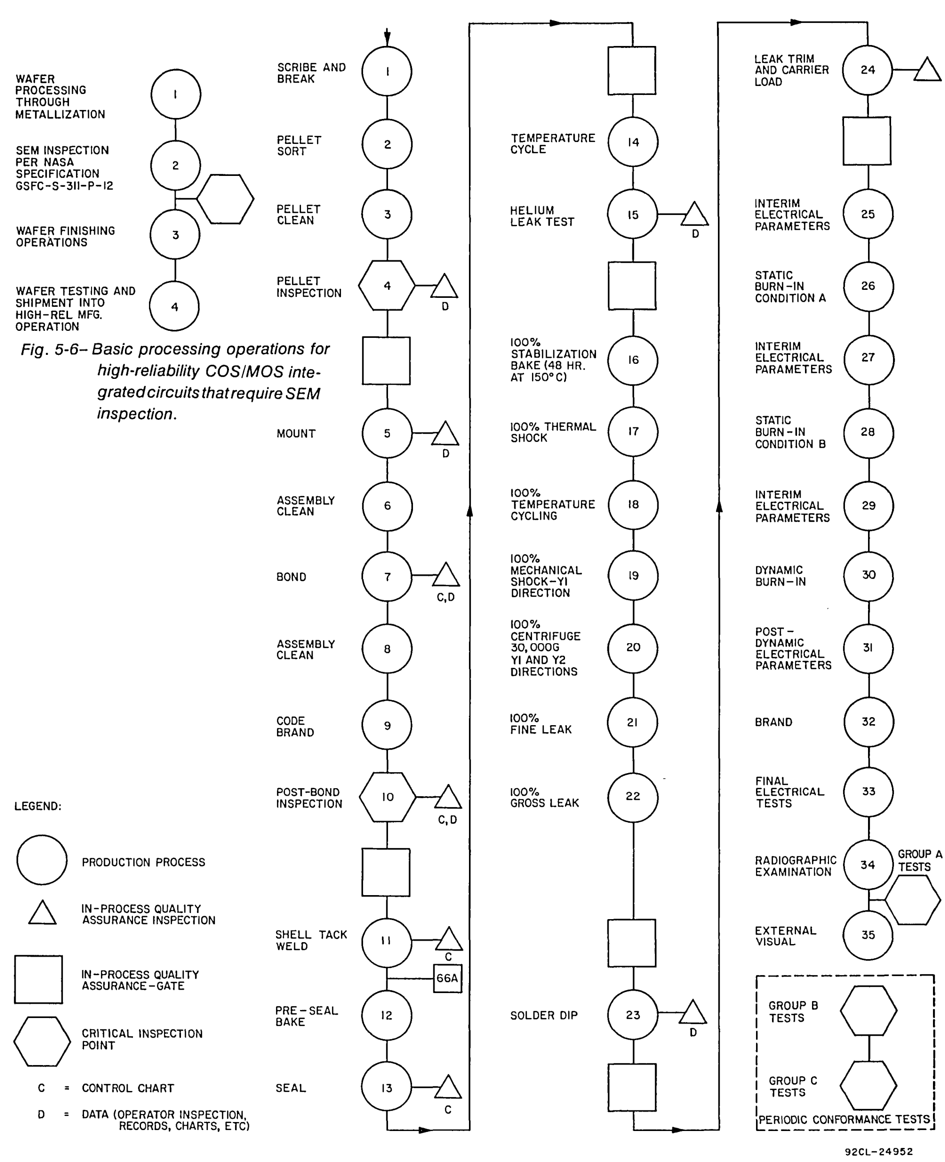


Fig. 5-6– Basic processing operations for high-reliability COS/MOS integrated circuits that require SEM inspection.

Fig. 5-7– COS/MOS High-Reliability Flow Chart for Flat Pack MIL-M-38510 Class A Devices.

Table 5-13— Comparison of MIL-STD-883 and MIL-M-38510 Detailed Screening Requirements for RCA Level /1N COS/MOS Devices

SCREENING PROCEDURES	RCA LEVEL /1N (PER MIL-STD-883)	CLASS A MIL-M-38510
1. SEM Inspection	Yes	Yes
2. Visual, Precap	2010.1 Cond. A	2010.1 Cond. A
3. Pre-conditioning	MIL-STD-883	MIL-STD-883
4. Bias Burn-in High	None	36 hrs @ 150°C, Δ(2) PDA(1)
5. Bias Burn-in Low	None	36 hrs @ 150°C, Δ(2) 5%
6. Operating Burn-in 240 hrs @ 125°C	Cirteria 10% Lot Reject Max; If Exceeded, Repeat Allowed	PDA 5% Max; if over 5% Reject Entire Lot Δ(2)
7. DC Elect. Tests	Measurements on Selected Inputs and Outputs	Measurements on all Inputs and Outputs
8. DC Test-Limit Resolution	50 nA Minimum; 10 mV Minimum	1 nA Minimum; 1 mV Minimum
9. AC Dynamic Tests	Measurements on Selected Inputs and Outputs	Measurements on all Inputs and Outputs
10. AC Test Limits	At 15-pF Load	AT 50-pF Load
11. Radiographic	View in One Dimension	View in Two Dimensions
12. Parts Qualification Requirement		9 Detailed Electrical Specifications
13. Group B and C Qualification Conformance	10 Generic Families for 50 COS/MOS Types	9 Generic Families for 27 COS/MOS Types

(1)PDA = Per-Cent Defective Allowable

(2)Δ = Delta Variables, Data Required

COS/MOS Life-Test Data

Table 5-14 provides a summary of Group B 125°C operating-life data for 1972 on RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-STD-883. These high-reliability COS/MOS devices were processed to meet RCA level /2 require-

Table 5-14— Operating-Life Data on RCA High-Reliability COS/MOS Integrated Circuits.

Device Tested:	1,122 from the CD4000A Family	
Specification:	High-reliability per RCA COS/MOS Reliability Report RIC-102 (MIL-STD-883, METHOD 5004)	
Test Hours:	1,000 hours each device**	
Total Device Hours:	1,055,372 hours	
Inoperable Failures:	Zero	
125°C Failure Rate =	0.086%/1000 hours	At 60% confidence
MTTF =	1,150,000 hours	
55°C Failure Rate* =	0.0126%/1000 hours	At 60% confidence
MTTF =	7,900,000 hours	
25°C Failure Rate =	0.0037%/1000 hours	At 60% confidence
MTTF =	26,800,000 hours	

*Actual tests conducted at 125°C. Failure rates derived for a 55°C operating temperature were obtained using acceleration factors of 6.8 and 23 for the 25°C operating temperature.

Acceleration factors were obtained from Report AD 614103, "Reliability of Integrated Circuits used in Missile Systems", Clearing House for Federal Scientific and Technical Information.

**231 units had less than 1000 hours.

Table 5-15 shows long-life reliability data for RCA of the life capability of 1972 shipments of RCA high-reliability COS/MOS integrated circuits.

Table 4-15 shows long-life reliability data for RCA high-reliability COS/MOS integrated circuits that have

Table 5-15— Long Life Reliability Data on RCA COS/MOS Integrated Circuits (Data obtained from 75 CD4001A integrated circuits tested at 125°C in a ring-counter application.)

Specification:	RCA commercial, full military-temperature range (−55°C to +125°C) per RCA COS/MOS Reliability Report RIC-101A	
Test Hours:	24,000 hours (AS OF MAY 1973)	
Total Device Hours:	1,784,000 hours**	
Inoperable Failures:	Zero	
125°C Failure Rate =	0.051%/1000 hours	At 60% confidence
MTTF =	1,940,000 hours	
55°C Failure Rate* =	0.0075%/1000 hours	At 60% confidence
MTTF =	13,300,000 hours	
25°C Failure Rate* =	0.0022%/1000 hours	At 60% confidence
MTTF =	46,000,000 hours	

Notes:

*Actual tests conducted at 125°C. Failure rates derived for a 55°C operating temperature were obtained using acceleration factors of 6.8 and 23 for the 25°C operating temperature.

Acceleration factors were obtained from Report AD 614103, "Reliability of Integrated Circuits used in Missile Systems", Clearing House for Federal Scientific and Technical Information.

**Two parts were destroyed at the 16,000-hour point as a result of operator error. Only 73 parts, therefore, were operated to 24,000 hours.

been operating continuously since 1970 in a ring-counter application that exercises the circuits in a functional mode. The data obtained from this test, which is still underway, indicate the long-term reliability of RCA COS/MOS integrated circuits.

High-Reliability Terms and Definitions

MIL-STD-883 — Military Standard for Test Methods, Microelectronics. This standard defines the best methods used to achieve three classes of reliability: Class A, Class B, and Class C. This specification defines standard test methods and procedures for high-reliability testing and processing.

Class A (MIL-STD-883) — The highest reliability category or level. RCA levels /1 and /2 follow MIL-STD-883 Class A; level /2 is the same as level /1 with the exception that X-ray inspection is omitted.

Class B (MIL-STD-883) — The intermediate reliability category or level. This class is the most widely used. RCA level /3 corresponds to MIL-STD-883, Class B.

Class C (MIL-STD-883) — The lowest reliability category or level. RCA level /4 follows MIL-STD-883, Class C. Level /4 or Class C parts have no burn-in.

MIL-M-38510 — Military Standard for Microelectronics or Integrated Circuits, first issued in 1969. MIL-M-38510 also defines three classes of reliability, Class A, Class B, and Class C, which are patterned after the MIL-STD-883 format. The MIL-M-38510 requirements differ from the MIL-STD-883 requirements in two significant ways.

MIL-M-38510 has detailed electrical specifications, or "slash sheets".

MIL-M-38510 requires Manufacturer's Certification for Class B and C devices and both Manufacturer's and Line Certification for Class A devices. Although the general specification has been available since 1969, the detailed electrical specifications have just recently been issued for various technologies, including COS/MOS.

The general specification includes basic material, such as definition of classes and general requirements common to all slash sheets.

Slash Sheets — Detailed electrical specifications that define exact test conditions and limits. Approved parts are shipped against exact nomenclature specified in the specification. The term slash sheet is derived from the fact that the part number is MIL-M-38510/XXXXX, or "MIL-M-38510 SLASH XXXXX".

Slash sheets must have a governmental sponsor. The COS/MOS sponsor is NASA, who has developed the detailed specifications for nine generic families that include 27 COS/MOS circuits.

Manufacturing Certification (Appendix A) — MIL-M-38510 specification requires that the supplier's Product-Assurance Program Requirements are being adhered to. This certification is conducted by DESC (Defense Electronic Supply Center) and is one of the prerequisites for qualification approval.

Line Certification — This certification is conducted by NASA to insure that the requirements of NHB 5300.4 (3C) "Line Certification Requirements for Microcircuits" are being adhered to. Line certification is one of the prerequisites for obtaining Class A qualification approval.

QPL (General Definition) — Qualified Parts List. High-reliability users often develop a QPL which tells designers within the company which parts are qualified and can be used.

Interim Qualification or Part-II Qual for MIL-M-38510 — Before any supplier is fully qualified to supply a part, it is possible to obtain Interim Qualifications. Interim, or Part-II, Qualification is obtained by receiving Manufacturing Certification (and Line Certification for Class A parts) and submitting a sample of tested parts with data. It is not necessary to go through the entire processing and burn-in cycle to obtain Interim Qualification. (RCA has received Part II Qualification for a number of COS/MOS circuits.) When any supplier receives Final Qualification (i.e., submits approved parts that have received the complete processing and testing per the slash sheet), Interim, Part II, Qualification

for that part is withdrawn, and only fully qualified parts can be supplied against the specification.

Final Qualification or QPL I for MIL-M-38510 Final Qualification is obtained when all requirements of both the general and detailed specifications are met.

SEM Scanning Electron Microscope. SEM inspection is a requirement for MIL-M-38510 Class A parts. (RCA has SEM facilities at both the Somerville, N.J., and Findlay, Ohio, locations.)

SEM Specification GSFC-S-311-P12 SEM inspection procedure including accept-reject criteria. This specification was written by NASA Goddard Space Flight Center and is the industry standard.

PDA Per-Cent Defective Allowed. If this per cent is exceeded, a lot fails. This term usually applies to burn-in.

Condition B Visual Refers to MIL-STD-883, Method 2010.1, Precap Inspection. Used for RCA 883/1, 2, 3, 4 and MIL-M-38510 Class B and C parts.

Condition A Visual Used for MIL-M-38510, Class A parts. The criteria for metallization, foreign matter, oxide and diffusion faults, and bonding is considerably tighter than Condition B. Condition A

Visual is a requirement for MIL-M-38510 Class A parts.

Group A Tests Quality audit of test parameters prior to shipment to the warehouse, in accordance with MIL-STD-883, Method 5005.

Group B Tests These tests are designed to test the mechanical quality of the packaged devices in accordance with MIL-STD-883, Method 5005. The tests include:

- Physical dimensions
- Marking permanency
- Visual and mechanical
- Bond strength
- Solderability
- Lead fatigue
- Hermeticity

Group C Tests These tests are designed to test both the mechanical and electrical characteristics of the packaged device as an indicator of long-term stability. The tests, which are conducted in accordance with MIL-STD-883, Method 5005, include:

- Thermal shock
- Temperature cycling
- Moisture resistance
- Mechanical shock
- Vibration, variable-frequency
- Constant acceleration
- Salt atmosphere
- High-temperature storage
- Operating life test
- Steady-state reverse bias

Delta Tests or Limits Refers to specifications that define the maximum shift of key parameters during burn-in.

MTTF or MTBF MTTF — Mean Time to Failure
MTBF — Mean Time between Failure
Both terms are interchangeable and define reliability. Reciprocal of failure rate. Expressed in hours.

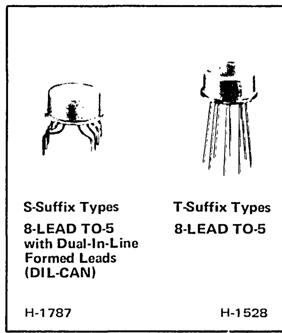
LTPD Lot Tolerance Per Cent Defective—sampling-plan term. An LTPD of 5 means that a lot 5-per-cent bad will pass incoming inspection only 10% of the time.

Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series CA101/ . . ., CA101A/ . . .



High-Reliability Operational Amplifiers

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Short-circuit protection and latch-free operation**
- **Unity-gain phase compensation with a single 30-pF capacitor**

	CA101	CA101A	
Max. V_{IO} (T_A = 25°C)	5	2	mV
Max. I_{IO} (T_A = 25°C)	200	10	nA
Min. A_{OL} (T_A = 25°C)	50	50	V/mV
T_A Range (Operating)	−55 to +125	−55 to +125	°C
Slew Rate (Summing ampl.)	–	10	V/μs

The RCA-CA101, CA101A, "Slash" (/) Series are high-reliability general-purpose, high-gain operational amplifiers intended for applications in aerospace, military and industrial equipment. They are electrically and mechanically identical with the standard types CA101, CA101A described in Data Bulletin File No. 786 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

These types, which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain; unity-gain compensation can be obtained with a single 30-pF capacitor.

Type CA101A has all the desirable features and characteristics of the CA101 plus superior input-offset characteristics, and improved noise performance

The packaged types can be supplied to screening levels — /1N, /1R, /1, /2, /3, and /4 — which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels — /M, /N, and /R.

These screening levels and detailed information on test methods, procedures and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

The CA101 and CA101A are supplied in either the standard 8-lead TO-5 package (T suffix), in the 8-lead TO-5 dual-in-line formed-lead "DIL-CAN" package (S suffix), or in chip form (H suffix).

The CA101T, S, and CA101AT, AS are direct replacements for industry types 101 and 101A in packages with similar terminal arrangements.

Applications:

- **Long-interval integrator**
- **Timers**
- **Sample and hold circuits**
- **Summing amplifiers**
- **Multivibrators**
- **Comparators**
- **Instrumentation**
- **AC/DC converters**
- **Inverting amplifiers**
- **Sine- & square-wave generators**
- **Capacitance multipliers & simulated inductors**

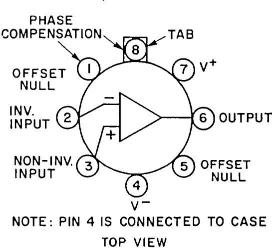


Fig. 1—Functional diagram.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C*

Parameter	Value	Unit
DC SUPPLY VOLTAGE (between V^+ and V^- terminals):		
CA101, CA101A	44	V
DC INPUT VOLTAGE	±15	V
(For supply voltage less than ±15 V, the Input Voltage rating is equal to the DC Supply Voltage)		
DIFFERENTIAL INPUT VOLTAGE	±30	V
OUTPUT SHORT-CIRCUIT DURATION	Indefinite*	
DEVICE DISSIPATION:		
Up to T_A = 75°C	500	mW
Above T_A = 75°C	derate linearly at 6.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Operating—		
CA101, CA101A	−55 to +125°C	
Storage (All types)	−65 to +150°C	
LEAD TEMPERATURE (During Soldering):		
At a distance 1/16" ±1/32 (1.59 ±0.79 mm) from case for 10 seconds max.	+265°C	

* At $T_A \leqslant 70°C$ and $T_C \leqslant 125°C$ (CA101);
$T_A \leqslant 75°C$ and $T_C \leqslant 125°C$ (CA101A)

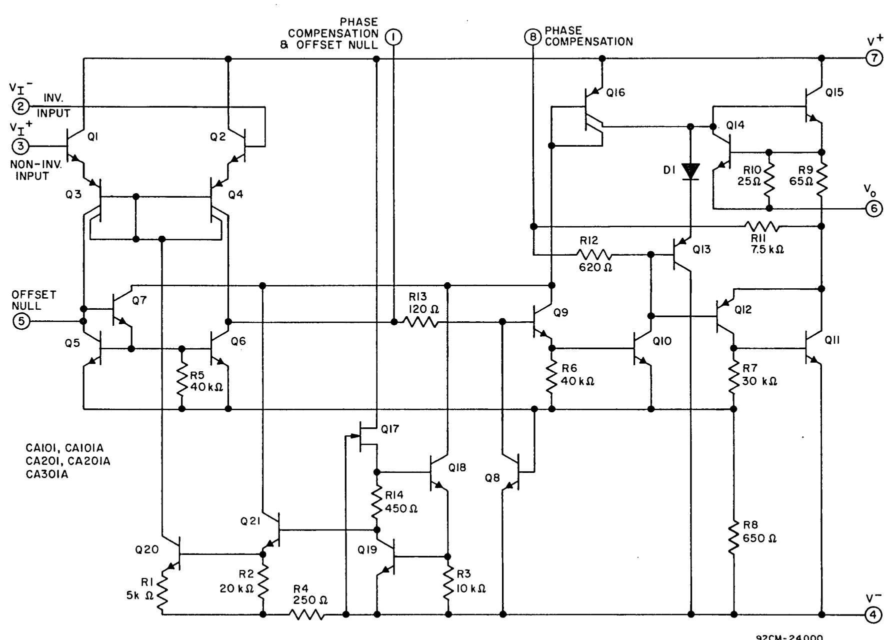


Fig. 2—Schematic diagram.

ELECTRICAL CHARACTERISTICS
For Design Guidance Only

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Supply Voltage (V±) = 5 to 15 V		LIMITS CA101 Typ.	LIMITS CA101A Typ.	UNITS
Input Offset Voltage	V_{IO}	T_A = 25°C	$R_S \leq 10k\Omega$	1	–	mV
			$R_S \leq 50k\Omega$	–	0.7	
Average Temperature Coefficient of Input Offset Voltage	αV_{IO}	T_A = –55 to +125°C	$R_S \leq 10k\Omega$	6	–	μV/°C
			$R_S \leq 50\Omega$	3	–	
				–	3	
Average Temperature Coefficient of Input Offset Current	αI_{IO}	–55°C to+25°C		–	0.02	nA/°C
		+25°C to +125°C		–	0.01	
Input Offset Current	I_{IO}	T_A = 25°C		40	1.5	nA
Input Bias Current	I_{IB}	T_A = 25°C		0.12	0.03	μA
Supply Current	$I^{\pm}$	T_A = 25°C	$V^{\pm}$ = 20V	1.8	1.8	mA
		T_A = 125°C	$V^{\pm}$ = 20V	1.2	1.2	
Open-Loop Differential Voltage Gain	A_{OL}	T_A = 25°C, V_O = ±10V	$V^{\pm}$ = 15V, $R_L \geq 2k\Omega$	160	160	V/mV
Input Resistance	R_I	T_A = 25°C		0.8	4	MΩ
Output Voltage Swing	V_{OPP}	$V^{\pm}$ = 15V	R_L = 10kΩ	±14	±14	V
		$V^{\pm}$ = 15V	R_L = 2kΩ	±13	±13	
Common-Mode Rejection Ratio	CMRR	T_A = –55 to +125°C	$R_S \leq 10k\Omega$	90	–	dB
			$R_S \leq 50k\Omega$	–	96	
Supply-Voltage Rejection Ratio	PSRR	T_A = –55 to +125°C	$R_S \leq 10k\Omega$	90	–	dB
			$R_S \leq 50k\Omega$	–	96	

Table I. Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C, V^+ = +15V, V^- = –15V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	LIMITS MAX.Δ	UNITS
Input Offset Voltage	V_{IO}	$R_S \leq 10k\Omega$	CA101	–	5	±1	mV
		$R_S \leq 50k\Omega$	CA101A	–	2	±0.5	
Input Offset Current	I_{IO}		CA101	–	200	±20	nA
			CA101A	–	10	±2	
Input Bias Current	I_I		CA101	–	500	±50	nA
			CA101A	–	75	±8	

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 19.

Table II. Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS▲ Supply Voltage ($V^{\pm}$) = 15V unless otherwise specified	LIMITS CA101 MINIMUM −55	+25	+125	CA101 MAXIMUM −55	+25	+125	CA101A MINIMUM −55	+25	+125	CA101A MAXIMUM −55	+25	+125	UNITS
Input Offset Voltage	V_{IO}	$R_S \leqslant 10k\Omega$	–	–	–	6	5	6	–	–	–	–	–	–	mV
		$R_S \leqslant 50k\Omega$	–	–	–	–	–	–	–	–	–	3	2	3	
Average Temperature Coefficient of Input Offset Voltage	αV_{IO}	$R_S \leqslant 50\Omega$	–	–	–	–	–	–	–	–	–	–	15	–	µV/°C
Average Temperature Coefficient of Input Offset Current	αI_{IO}	−55°C to +25°C	–	–	–	–	–	–	–	–	–	–	0.2	–	nA/°C
		+25°C to +125°C	–	–	–	–	–	–	–	–	–	–	0.1	–	
Input Offset Current	I_{IO}		–	–	–	500	200	200	–	–	–	20	10	20	nA
Input Bias Current	I_{IB}		–	–	–	1500	500	500	–	–	–	100	75	100	nA
Supply Current	$I^{\pm}$	$V^{\pm}$ = 20V	–	–	–	4	3	2.5	–	–	–	4	3.0	2.5	mA
Open-Loop Differential Voltage Gain	A_{OL}	$V_O = \pm 10V$ $R_L \leqslant 2k\Omega$	25	50	25	–	–	–	25	50	25	–	–	–	V/mV
Input Resistance	R_I		–	0.3	–	–	–	–	–	1.5	–	–	–	–	MΩ
Output Voltage Swing	V_{OPP}	R_L = 10kΩ	±12	±12	±12	–	–	–	±12	±12	±12	–	–	–	V
		R_L = 2kΩ	±10	±10	±10	–	–	–	±10	±10	±10	–	–	–	
Common-Mode Input-Voltage Range	V_{ICR}	$V^{\pm}$ = 15V	±12	±12	±12	–	–	–	–	–	–	–	–	–	V
		$V^{\pm}$ = 20V	–	–	–	–	–	–	±15	±15	±15	–	–	–	
Common-Mode Rejection Ratio	CMRR	$R_S \leqslant 10k\Omega$	70	70	70	–	–	–	–	–	–	–	–	–	dB
		$R_S \leqslant 50k\Omega$	–	–	–	–	–	–	80	80	80	–	–	–	
Supply-Voltage Rejection Ratio	PSRR	$R_S \leqslant 10k\Omega$	70	70	70	–	–	–	–	–	–	–	–	–	dB
		$R_S \leqslant 50k\Omega$	–	–	–	–	–	–	80	80	80	–	–	–	

▲Ambient temperature range T_A = −55 to +125°C unless otherwise specified.

Table III. Group C Electrical Characteristics Sampling Tests

T_A = +25°C V^+ = +15 V V^- = −15 V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS		LIMITS MIN.	MAX.	UNITS
Input Offset Voltage	V_{IO}	$R_S \leqslant 10k\Omega$	CA101	–	5	mV
		$R_S \leqslant 50k\Omega$	CA101A	–	2	
Input Offset Current	I_{IO}		CA101	–	200	nA
			CA101A	–	10	
Input Bias Current	I_I		CA101	–	500	nA
			CA101A	–	75	
Large-Signal Voltage Gain	A_{OL}	$V_O = \pm 10V$ $R_L = \geqslant 2k\Omega$		50	–	V/mV

TYPICAL STATIC CHARACTERISTICS

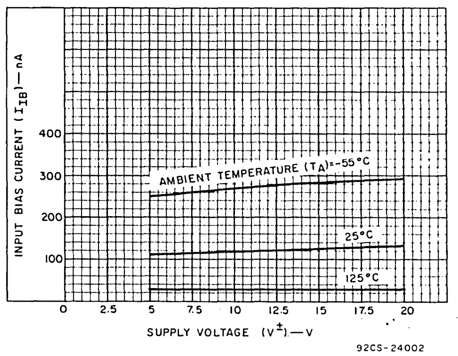


Fig. 3—Input bias current vs. supply voltage for CA101.

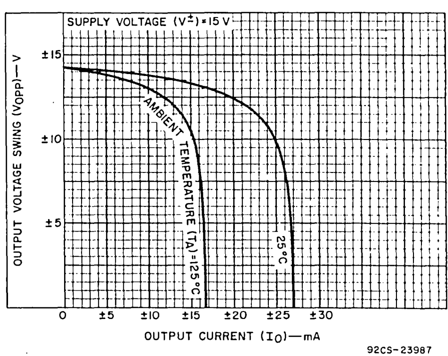


Fig. 4—Output characteristics for CA101, CA101A.

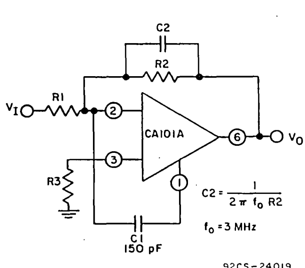


Fig. 5—Test circuit employing feedforward compensation.

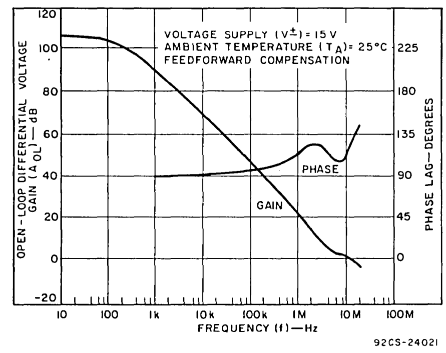


Fig. 6—Voltage gain and phase lag vs. frequency.

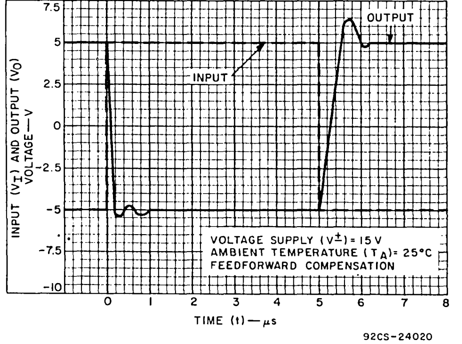


Fig. 7—Inverter pulse response.

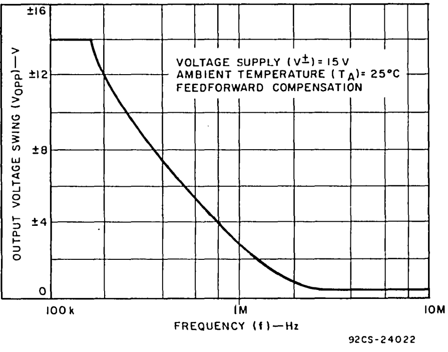


Fig. 8—Output voltage swing vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA101A

Single-Pole Compensation

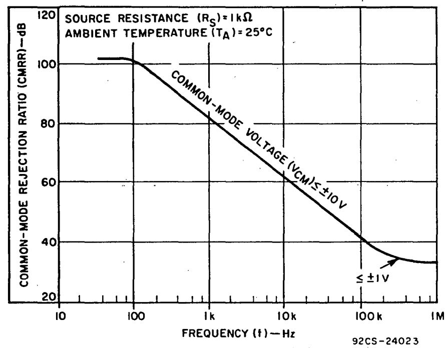


Fig. 9—Common-mode rejection ratio vs. frequency for CA101A.

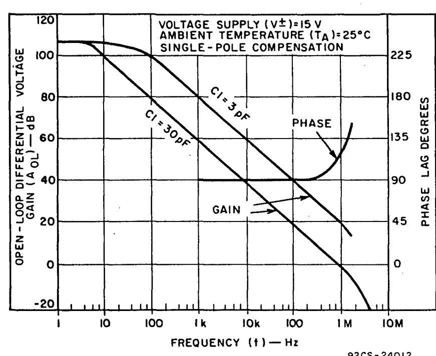


Fig. 10—Voltage gain and phase lag vs. frequency.

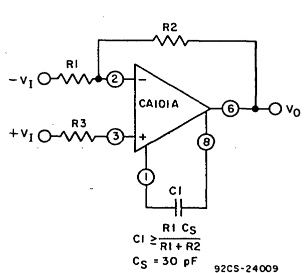


Fig. 11—Test circuit employing single-pole compensation.

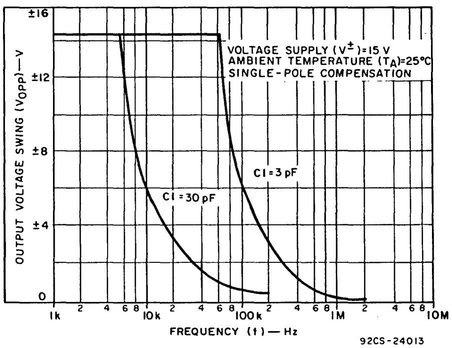


Fig. 12—Output voltage swing vs. frequency.

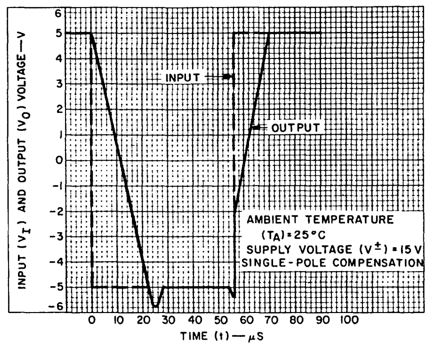


Fig. 13—Voltage follower (V_I, V_O) pulse response.

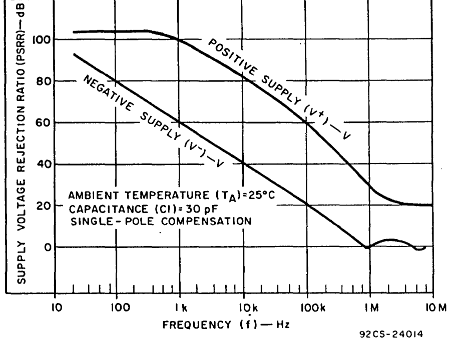


Fig. 14—Supply voltage rejection ratio vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA101A

Two-Pole Compensation

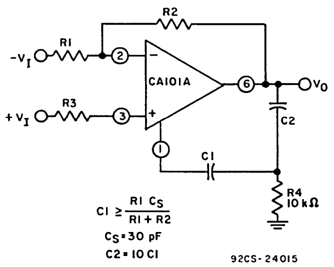


Fig. 15—Test circuit employing two-pole compensation.

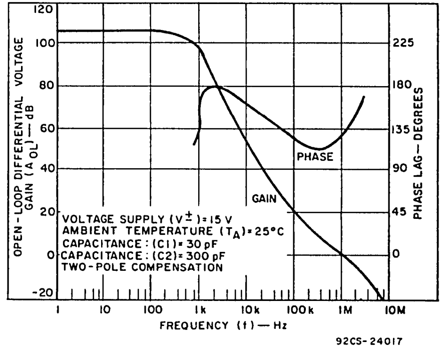


Fig. 16—Voltage gain and phase lag vs. frequency.

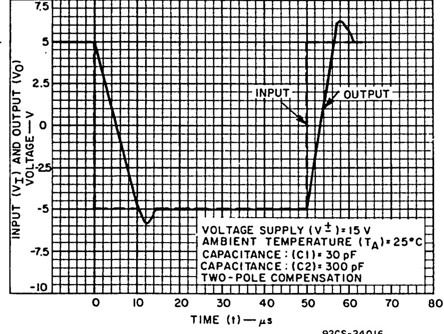


Fig. 17—Voltage follower pulse response.

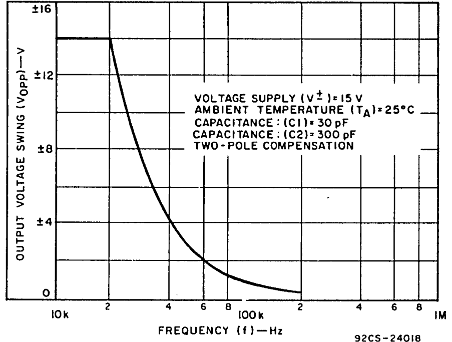


Fig. 18—Output voltage swing vs. frequency.

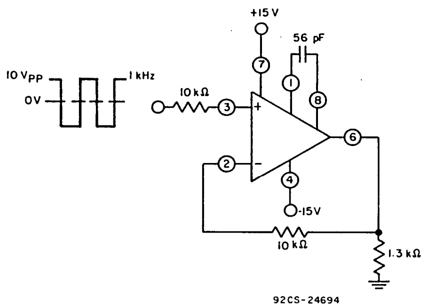


Fig. 19—Burn-in and operating life test circuit for CA101 and CA101A.

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPE CA101

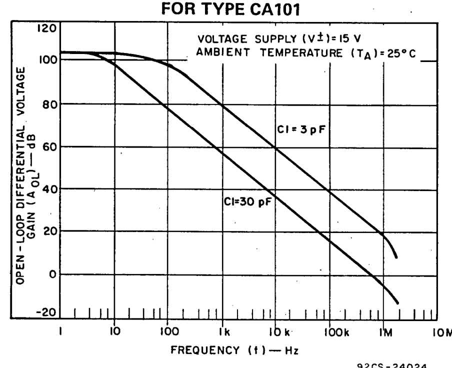


Fig. 20—Voltage gain vs. frequency.

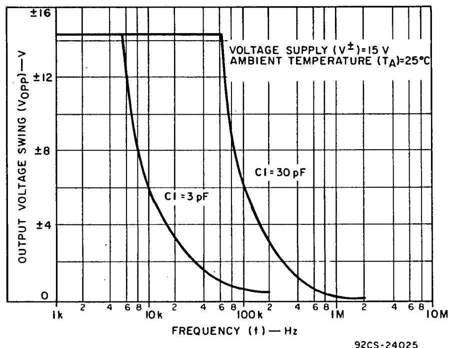


Fig. 21—Output voltage swing vs. frequency.

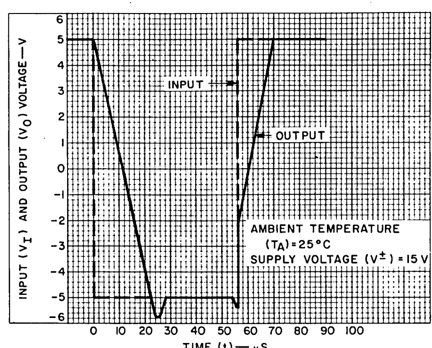


Fig. 22—Voltage follower pulse response.

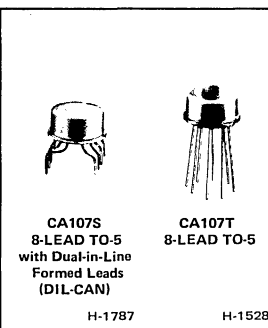
Lead Finish:
In accordance with MIL-M-38510, paragraph 3.6.2.5, lead finish "A".

Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series CA107/ . . .



CA107S
8-LEAD TO-5
with Dual-in-Line
Formed Leads
(DIL-CAN)
H-1787

CA107T
8-LEAD TO-5
H-1528

High-Reliability Operational Amplifiers

For Applications in Aerospace, Military, and Critical Industrial Equipment

- **Low input current over temperature range (100 mA max)**
- **30-pF on-chip capacitor provides internal frequency compensation**

Feature / Type	Max. V_{IO} (mV)	Max. I_{IO} (nA)	Max. I_{IB} (nA)	Temp. Range (T_A) °C
CA107	3	20	100	–55 to +125

The RCA-CA107 "Slash" (/) Series type is a high-reliability linear integrated circuit operational amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA107A described in Data Bulletin File No. 785 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The CA107 features a 30-pF on-chip capacitor to provide internal frequency compensation. Low input current over temperature range (100 nA max.) for the CA107 make this type especially well suited for applications such as long interval timers and sample-and-hold circuits.

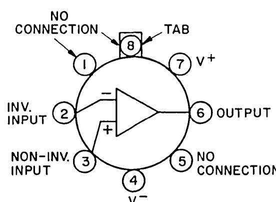
The packaged type can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /M, /N, and /R.

These screening levels and detailed information on test methods, procedures and test sequence are given in Reliability Report RIC202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

The CA107 is supplied in the standard 8-lead TO-5 style package ("T" suffix), the 8-lead TO-5 style with dual-in-line formed leads ("S" suffix), and in chip form ("H" suffix). It is a direct replacement for industry type 107 in packages with similar terminal arrangements.

Applications:

- **Long-interval integrators**
- **Timers**
- **Sample-and-hold circuits**
- **Summing amplifiers**
- **Multivibrators**



Functional diagram for TO-5 style packages

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DC SUPPLY VOLTAGE (Between V+ and V− Terminals):		
CA107	44	V
DC INPUT VOLTAGE	±15	V
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)		
DIFFERENTIAL INPUT VOLTAGE	±30	V
OUTPUT SHORT-CIRCUIT DURATION	Indefinite	
DEVICE DISSIPATION UP TO T_A = 70°C	500	mW
Above T_A = 70°C Derate linearly at	6.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Operating	−55°C to +125°C	
Storage	−65°C to +150°C	
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	+265°C	

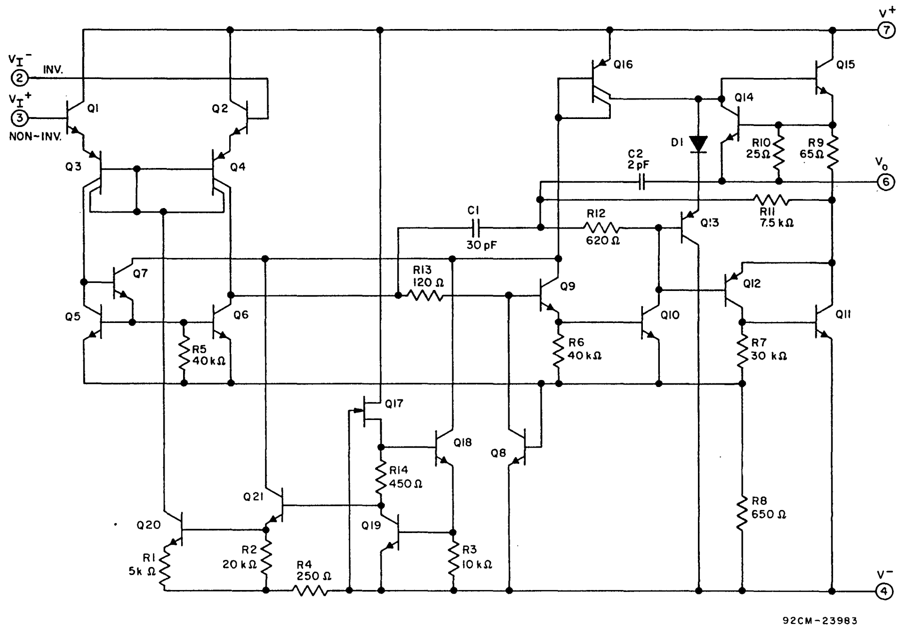


Fig. 1–Schematic diagram of CA107.

ELECTRICAL CHARACTERISTICS For Design Guidance Only

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Supply Voltage ($V^{\pm}$) = 5 V to 15 V	TYPICAL VALUES	UNITS
Input Offset Voltage	V_{IO}	T_A = 25°C, $R_S \leqslant$ 50 kΩ	0.7	mV
Average Temperature Coefficient of Input Offset Voltage	V_{IO}	−55 to +125°C	3	μV/°C
Input Offset Current	I_{IO}	T_A = 25°C	1.5	nA
Average Temperature Coefficient of Input Offset Current	I_{IO}	+25 to +125°C	0.01	nA/°C
		−55 to +25°C	0.02	
Input Bias Current	I_{IB}	T_A = 25°C	30	nA
Supply Current	$I^{\pm}$	T_A = +125°C, $V^{\pm}$ = 20 V	1.2	mA
		T_A = 25°C, $V^{\pm}$ = 20 V,	1.8	
Open-Loop Differential Voltage Gain	A_{OL}	$V^{\pm}$ = 15 V, V_O = ±10 V $R_L \geqslant$ 2 kΩ, T_A = 25°C	160	V/mV
Input Resistance	R_I	T_A = 25°C	4	MΩ
Output Voltage Swing	V_{OPP}	$V^{\pm}$ = 15 V, R_L = 10 kΩ	±14	V
		$V^{\pm}$ = 15 V, R_L = 2 kΩ	±13	
Common-Mode Rejection Ratio	CMRR	$R_S \leqslant$ 50 kΩ	96	dB
Supply-Voltage Rejection Ratio	PSRR	$R_S \leqslant$ 50 kΩ	96	dB

Table I. Pre Burn-in Electrical and Post Burn-in Electrical Tests, and Delta Limits *

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, V^+ = +15 V, V^- = −15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX.△	
Input Offset Voltage	V_{IO}		–	2	±0.5	mV
Input Offset Current	I_{IO}		–	10	±2	nA
Input Bias Current	I_I		–	75	±8	nA

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 4.

Table II Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Supply Voltage (V±) = 5 V to 15 V	LIMITS MINIMUM			LIMITS MAXIMUM			UNITS
			-55	+25	+125	-55	+25	+125	
Input Offset Voltage	V_{IO}	T_A = 25°C, $R_S \leq 50$ kΩ	–	–	–	3	2	3	mV
Average Temperature Coefficient of Input Offset Voltage	aV_{IO}		–	–	–	15	15	15	μV/°C
Input Offset Current	I_{IO}		–	–	–	20	10	20	nA
Average Temperature Coefficient of Input Offset Current	aI_{IO}		–	–	–	0.2	–	0.1	nA/°C
Input Bias Current	I_{IB}		–	–	–	100	75	100	nA
Supply Current	$I^{\pm}$		–	–	–	4	3	2.5	mA
Open-Loop Differential Voltage Gain	A_{OL}	$V^{\pm}$ = 15 V, V_O = ±10V $R_L \geq 2$ kΩ, T_A = 25°C	25	50	25	–	–	–	V/mV
Input Resistance	R_I		–	1.5	–	–	–	–	MΩ
Output Voltage Swing	V_{OPP}	$V^{\pm}$ = 15 V, R_L = 10 kΩ	±12	±12	±12	–	–	–	V
		$V^{\pm}$ = 15 V, R_L = 2 kΩ	±10	±10	±10	–	–	–	
Input Voltage Range	V_{ICR}	$V^{\pm}$ = 20 V	±15	±15	±15	–	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 50$ kΩ	80	80	80	–	–	–	dB
Supply-Voltage Rejection Ratio	PSRR	$R_S \leq 50$ kΩ	80	80	80	–	–	–	dB

Table III. Group C Electrical Characteristics Sampling Tests

T_A = +25°C V^+ = +15 V V^- = –15 V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Input Offset Voltage	V_{IO}	–	–	3	mV
Input Offset Current	I_{IO}	–	–	15	nA
Input Bias Current	I_I	–	–	85	nA
Large-Signal Voltage Gain	A_{OL}	V_O = ±10 V $R_L = \geq 2$kΩ	40	–	V/mV

TYPICAL CHARACTERISTICS

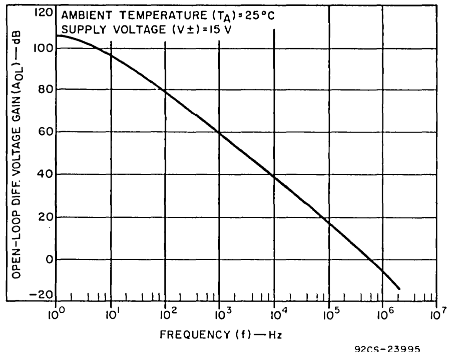


Fig. 2—Open-loop differential voltage gain vs. frequency.

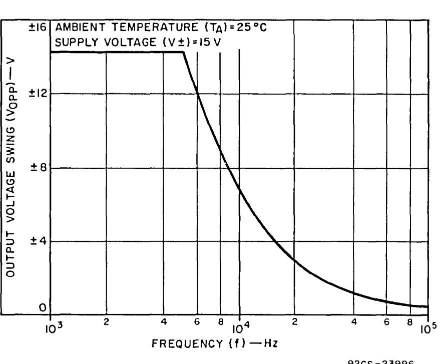


Fig. 3—Output voltage swing vs. frequency.

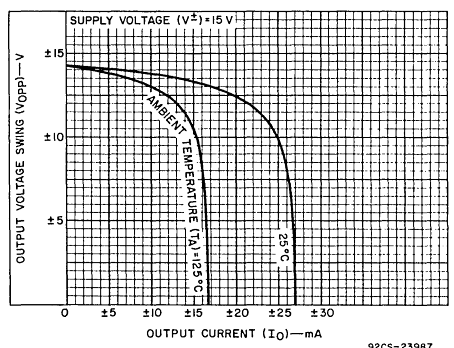


Fig. 3—Output voltage swing vs. output current.

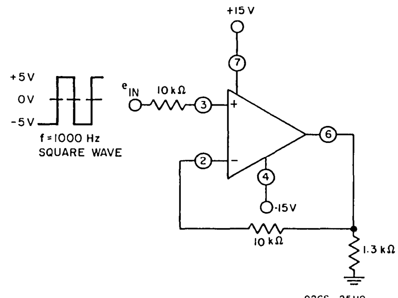


Fig. 4—Burn-in and operating life test circuit.

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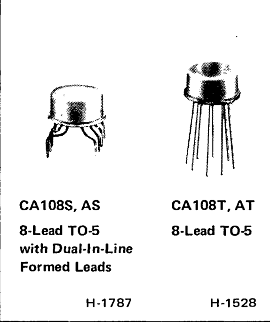
Monolithic Silicon

High-Reliability Slash (/) Series CA108/ . . ., CA108A/ . . .



CA108S, AS
8-Lead TO-5
with Dual-In-Line
Formed Leads
H-1787

CA108T, AT
8-Lead TO-5
H-1528

High-Reliability Precision Operational Amplifiers

For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Maximum input bias current – 2 nA**
- **Maximum input offset current – 0.2 nA**
- **Supply current of only 300 μA, even in saturation**
- **Maximum input offset voltage of 0.5 mV for "A" suffix types**

The RCA-CA108 and CA108A Slash (/) Series types are uncompensated precision operational amplifiers using super-beta transistors and feature very low offset parameters, high input impedance, and defined drift rates with temperature change. They are intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard type CA108 Series described in Data Bulletin File No. 621 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged type can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. the chip version can be supplied to three screening levels – /M, /N, and /R. These screening levels and detailed information on test methods, procedures and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The "A" versions have all the desirable features and characteristics of their prototypes plus exceptionally low input offset voltage characteristics. The CA108, CA108A, are direct replacements for industry types 108 and 108A in packages with similar terminal arrangements. The CA108 and CA108A are supplied in standard 8-lead TO-5 packages, 8-lead TO-5 packages with dual-in-line formed leads ("DIL-CAN"), or in chip form (H suffix).

Applications:

- **Instrumentation**
- **Summing amplifier**
- **Comparator**
- **Multivibrators**
- **Band-pass filters**
- **Sample and hold**

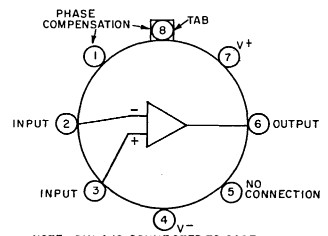


Fig. 1–Functional Diagram

ELECTRICAL CHARACTERISTICS, MAXIMUM VALUES AT T_A = 25°C	CA108T CA108S	CA108AT CA108AS
Input Offset Voltage (V_{IO})	2 mV	0.5 mV
Input Offset Current (I_{IO})	0.2 nA	
Input Bias Current (I_{IB})	2 nA	
Average Temperature Coefficient of Input Offset Voltage ($\Delta V_{IO}/\Delta T$)	15 μV/°C	5 μV/°C
Ambient Operating-Temperature Range	–55 to +125°C	

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$*

DC SUPPLY VOLTAGE (Between V+ and V− Terminals):		
CA108, CA108A	40	V
DC INPUT VOLTAGE	±15	V
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)		
DIFFERENTIAL INPUT CURRENT	±10	mA
OUTPUT SHORT-CIRCUIT DURATION	Indefinite	
DEVICE DISSIPATION	500	mW
AMBIENT TEMPERATURE RANGE:		
Operating	−55° to +125	°C
Storage	−65° to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+300	°C

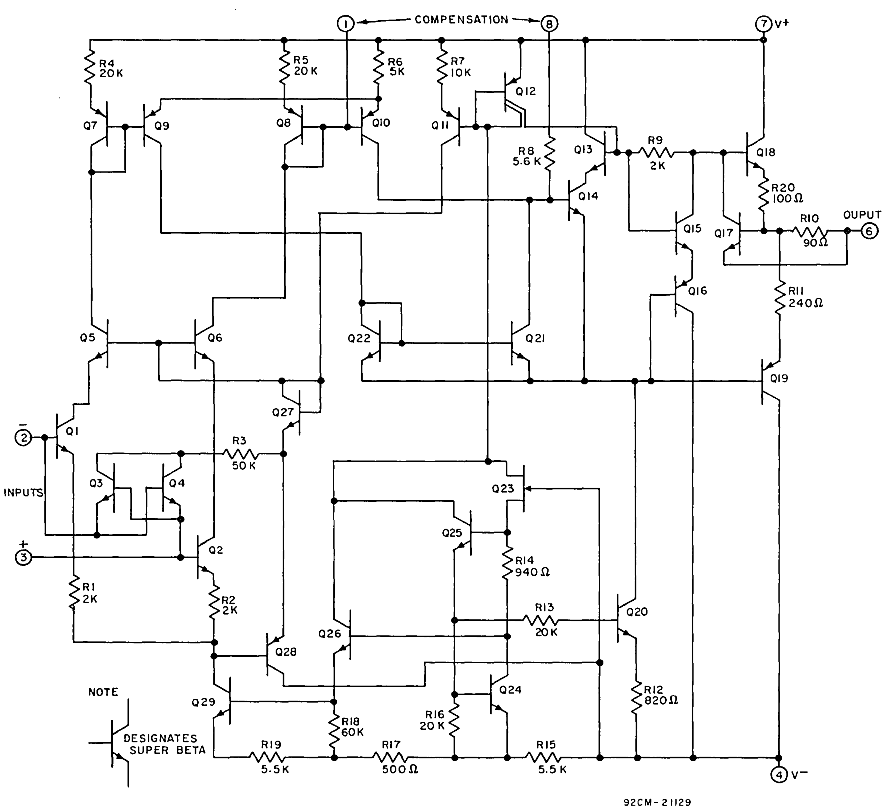


Fig. 2—Schematic diagram for CA108 and CA108A.

ELECTRICAL CHARACTERISTICS For Design Guidance Only

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: Supply Voltage (V) = ±5 V to ±15 V, Ambient Temperature T_A = 25°C	CA108 Typ.	CA108A Typ.	UNITS
Input Offset Voltage	V_{IO}		0.7	0.7	mV
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{IO}}{\Delta T}$		3	1	µV/°C
Input Offset Current	I_{IO}		0.05	0.05	nA
Average Temperature Coefficient of Input Offset Current	$\frac{\Delta I_{IO}}{\Delta T}$		0.5	0.5	pA/°C
Input Bias Current	I_{IB}		0.8	0.8	nA
Supply Current	I_Q	T_A = +125°C	0.15	0.15	mA
		T_A = 25°C	0.3	0.3	
Large-Signal Voltage Gain	A_V	V = ±15 V, V_O = ±10 V, R_L ≥10 kΩ	300	300	V/mV
Input Resistance R_I			70	70	MΩ
Output Voltage	V_O	V = ±15 V, R_L = 10 kΩ	±14	±14	V
Common-Mode Rejection Ratio	CMRR		100	110	dB
Supply-Voltage Rejection Ratio	V_{RR}		96	110	dB

TABLE I Pre Burn-In Electrical and Post Burn-In Electrical Tests and Delta Limits*

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, V^+ = +15 V, V^- = −15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	LIMITS MAX.Δ	UNITS
Input Offset Voltage	V_{IO}	CA108	–	2	±1	mV
		CA108A	–	0.5	±0.25	
Input Offset Current	I_{IO}		–	0.2	±0.05	nA
Input Bias Current	I_I		–	2	±0.2	nA

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 8.

Table II Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	Test Conditions Supply Voltage (V) ±15 Volts	LIMITS CA108 MINIMUM -55	+25	+125	CA108 MAXIMUM -55	+25	+125	CA108A MINIMUM -55	+25	+125	CA108A MAXIMUM -55	+25	+125	UNITS
Input Offset Voltage	V_{IO}		–	–	–	3	2	3	–	–	–	1	0.5	1	mV
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{IO}}{\Delta T}$		–	–	–	15	15	15	–	–	–	5	5	5	μV/°C
Input Offset Current	I_{IO}		–	–	–	0.4	0.2	0.4	–	–	–	0.4	0.2	0.4	nA
Average Temperature Coefficient of Input Offset Current	$\frac{\Delta I_{IO}}{\Delta T}$		–	–	–	2.5	2.5	2.5	–	–	–	2.5	2.5	2.5	pA/°C
Input Bias Current	I_{IB}		–	–	–	3	2	3	–	–	–	3	2	3	nA
Supply Current	I_Q		–	–	–	0.8	0.6	0.4	–	–	–	0.8	0.6	0.4	mA
Large-Signal Voltage Gain	A_V	V = ±15 V, V_O = ±10 V, $R_L \geqslant 10\ k\Omega$	25	50	25	–	–	–	48	80	40	–	–	–	V/mV
Input Resistance	R_I		–	30	–	–	–	–	–	30	–	–	–	–	MΩ
Output Voltage	V_O	V = ±15 V, R_L = 10 kΩ	±13	±13	±13	–	–	–	±13	±13	±13	–	–	–	V
Input Voltage Range	V_I	V = ±15 V	±13.5	±13.5	±13.5	–	–	–	±13.5	±13.5	±13.5	–	–	–	V
Common-Mode Rejection Ratio	CMRR		85	85	85	–	–	–	96	96	96	–	–	–	dB
Supply-Voltage Rejection Ratio	V_{RR}		80	80	80	–	–	–	96	96	96	–	–	–	dB

Table III Group C Electrical Characteristics Sampling Tests

T_A = +25°C V^+ = +15 V V^- = –15 V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS		LIMITS MIN.	MAX.	UNITS
Input Offset Voltage	V_{IO}		CA108	–	3	mV
			CA108A	–	1	
Input Offset Current	I_{IO}			–	0.4	nA
Output Voltage	V_O	R_L = 10 kΩ		–	±13	V
Large-Signal Voltage Gain	A_{OL}	V_O = 10 V, $R_L \geqslant 10\ k\Omega$	CA108	40	–	V/mV
			CA108A	70	–	

TYPICAL CHARACTERISTICS FOR TYPES CA108 AND CA108A

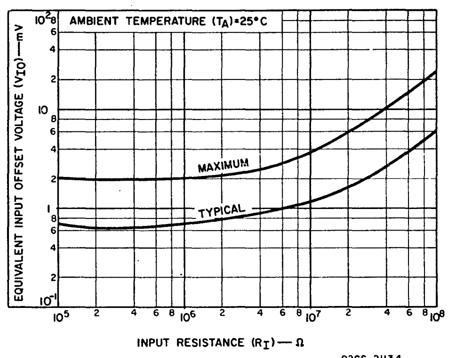


Fig. 3—Input offset voltage vs. input resistance.

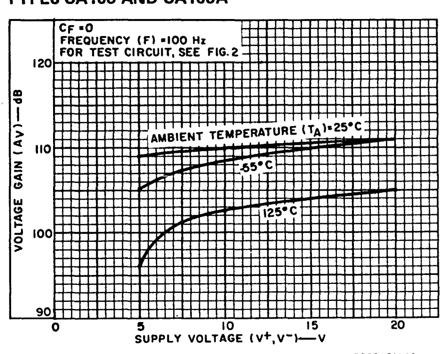


Fig. 4—Voltage gain vs. supply voltage.

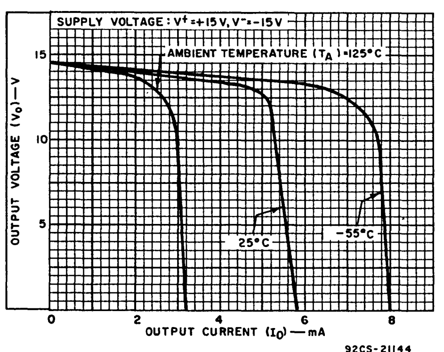


Fig. 5—Output voltage vs. output current for CA108 and CA108A.

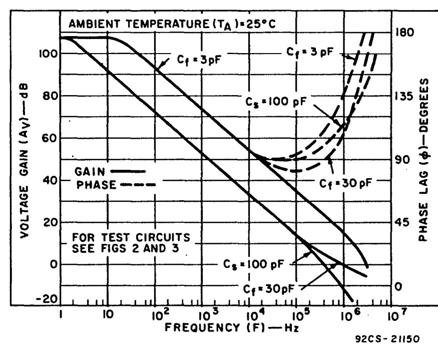


Fig. 6—Open-loop frequency response.

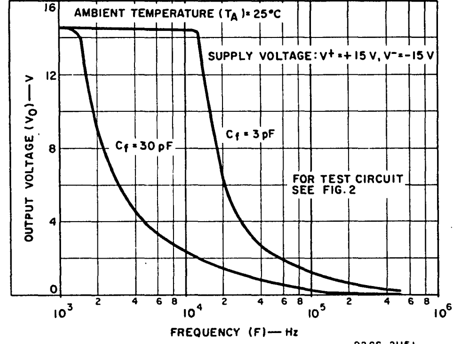


Fig. 7—Large-signal frequency response.

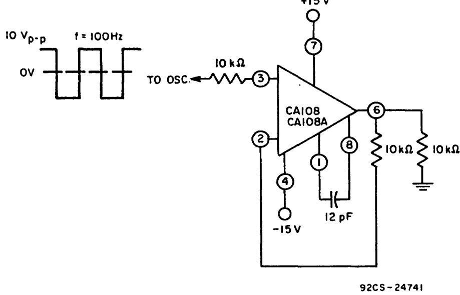


Fig. 8—Burn-in and operating life test circuit.

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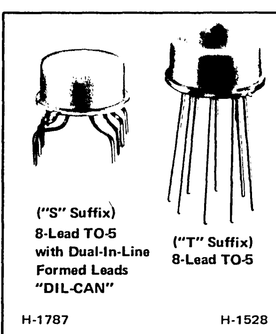
Monolithic Silicon

High-Reliability Slash (/) Series CA111/ . . .



("S" Suffix) 8-Lead TO-5 with Dual-In-Line Formed Leads "DIL-CAN" H-1787

("T" Suffix) 8-Lead TO-5 H-1528

High-Reliability Voltage Comparators

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

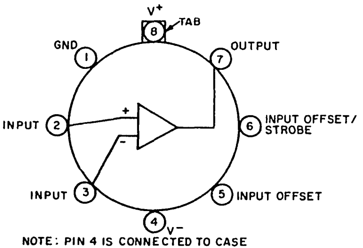
- Single- or dual-supply operation
- Power consumption — 135 mW at ±15 V
- Strobe capability
- Low input-offset current — 4 nA (typ.)
- Differential input-voltage range — ±30 V

Applications:

- Multivibrators
- Positive and negative peak detectors
- Crystal oscillators
- Zero-crossing detectors
- Solenoid, relay, and lamp drivers

The RCA-CA111 "Slash" (/) Series type is a high-reliability linear-integrated-circuit voltage comparator intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA111 described in Data Bulletin File No. 797 but is specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."



Functional Diagram

The CA111 Slash (/) Series types are supplied in 8-lead TO-5 style packages ("T" suffix), and in "DIL-CAN" packages, 8-lead TO-5 style packages with dual-in-line formed leads ("S" suffix). The CA111 is also supplied in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC SUPPLY VOLTAGE (Between V^+ and V^- terminals) . . . . . . 36 V
DC INPUT VOLTAGE* . . . . . . ±15 V
DIFFERENTIAL INPUT VOLTAGE . . . . . . ±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE (V_{7-4}) . . . . . . 50 V
GROUND TO NEGATIVE SUPPLY VOLTAGE (V_{1-4}) . . . . . . 30 V
OUTPUT SHORT-CIRCUIT DURATION . . . . . . 10 s
DEVICE DISSIPATION:
Up to T_A = 25°C . . . . . . 500 mW
Above T_A = 25°C . . . . . . derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating . . . . . . −55 to +125°C
Storage . . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . . . +265°C

*This rating applies for ± 15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

ELECTRICAL CHARACTERISTICS For Design Guidance Only

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: SUPPLY VOLTAGE ($V^{\pm}$) = 15 V, AMBIENT TEMPERATURE (T_A) = 25°C Unless Otherwise Specified	TYPICAL VALUES	UNITS
Input Offset Voltage*	V_{IO}	$R_S \leqslant 5\ k\Omega$	0.7	mV
Saturation Voltage		$V_I = -5$ mV, $I_O = 50$ mA	0.75	V
Input Voltage Range	V_{IPP}	$T_A = -55$ to +125°C	±14	V
Input Offset Current*	I_{IO}		4	nA
Input Bias Current*	I_{IB}		60	nA
Positive Supply Current	I^+		5.1	mA
Negative Supply Current	I^-		4.1	mA
Output Leakage Current		$V_I \geqslant 5$ mV, $V_O = 35$ V	0.2	nA
Strobe On Current			3	mA
Voltage Gain	A		200	V/mV
Response Time		100 mV Input Step with 5 mV Overdrive Voltage	200	ns

Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: SUPPLY VOLTAGE ($V^{\pm}$) = 15 V Unless Otherwise Specified	MAXIMUM LIMITS			UNITS
			–55	+25	+125	
Input Offset Voltage*	V_{IO}	$R_S \leqslant 5\ k\Omega$	4	3	4	mV
Saturation Voltage		$V_I = -5$ mV, $I_O = 50$ mA	–	1.5	–	V
		$V^+ \geqslant 4.5$ V, $V^- = 0$, $V_I \leqslant -6$ mV, $I_{SINK} \leqslant 8$ mA	0.4	0.4	0.4	V
Input Offset Current*	I_{IO}		20	10	20	nA
Input Bias Current*	I_{IB}		150	100	150	nA
Positive Supply Current	I^+		–	6	–	mA
Negative Supply Current	I^-		–	5	–	mA
Output Leakage Current		$V_I \geqslant 5$ mV, $V_O = 35$ V	500	10	500	nA

* The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1-mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ±15 V dual supply.

Table III. Pre Burn-in Electrical and Post Burn-in Electrical Tests, and Delta Limits* For All Types

ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = +15 V, V^- = −15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX.Δ	
Input Offset Voltage	V_{IO}	$R_S \leqslant 5\ k\Omega$	–	3	±1	mV
Input Offset Current	I_{IO}		–	10	±2	nA
Input Bias Current	I_I		–	100	±10	nA

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 9.

Table IV. Group C Electrical Characteristics Sampling Tests

T_A = +25°C, $V^{\pm}$ = 15 V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	V_{IO}	$R_S \leqslant 5\ k\Omega$	–	3	mV
Input Offset Current	I_{IO}		–	14	nA
Input Bias Current	I_I		–	110	nA

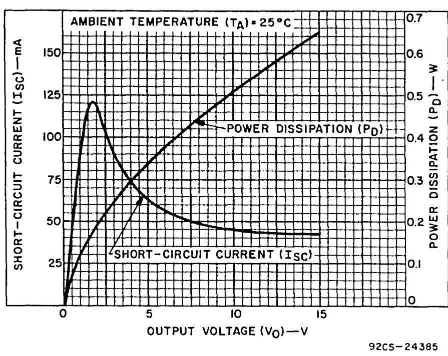


Fig. 1—Output limiting characteristics.

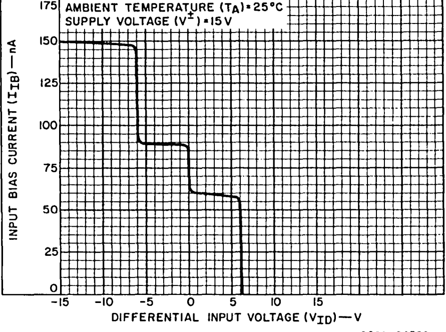


Fig. 2—Input characteristics.

NOTE: ALL RESISTANCES ARE IN OHMS

Fig. 3—Schematic diagram for CA111.

92CM-24380

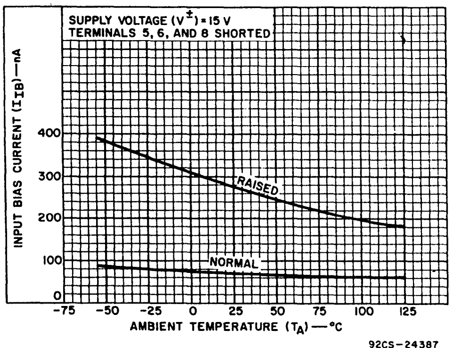


Fig. 4—Input bias current vs. ambient temperature.

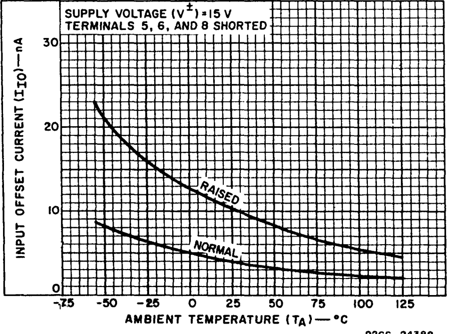


Fig. 5—Input offset current vs. ambient temperature.

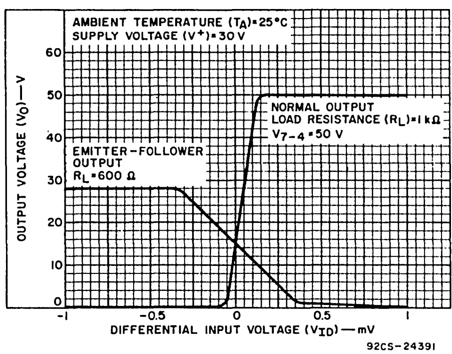


Fig. 6—Transfer function.

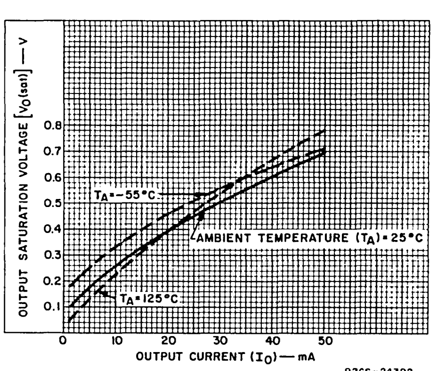


Fig. 7—Output saturation voltage vs. output current.

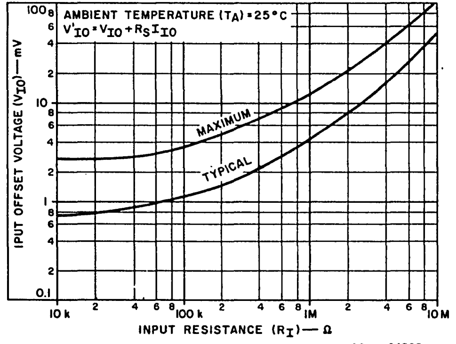


Fig. 8—Offset error.

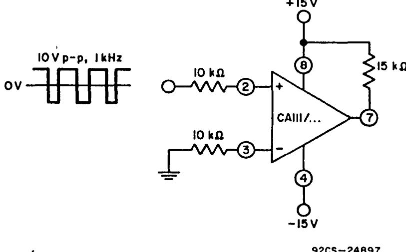


Fig. 9—Burn-in and operating life test circuit.

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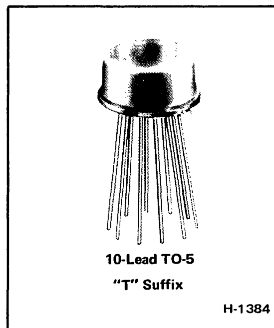
Monolithic Silicon
High-Reliability Slash (/) Series
CA723T/ . . .



10-Lead TO-5
"T" Suffix

H-1384

High-Reliability Voltage Regulators

For Regulated Output Voltages Adjustable from 2 V to 37 V at Currents up to 150 mA Without External Pass Transistors In Aerospace, Military, and Critical Industrial Equipment

Features:

- **Up to 150 mA output current**
- **Positive and negative voltage regulation**
- **Regulation in excess of 10 A with suitable pass transistors**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.03%**
- **Direct replacement for 723 industry types**
- **Adjustable output voltage: 2 to 37 V**

The RCA-CA723 Slash (/) Series types are high-reliability silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2 to 37 volts at currents up to 150 milliamperes. These devices are intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard type CA723 described in Data Bulletin File No. 788 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150 milliamperes and in excess of 10 amperes with the use of suitable n-p-n or p-n-p external pass transistors.

The packaged type can be supplied to six screening levels — /1N, /1R, /1, /2, /3, and /4 — which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels — /M, /N, /R.

These screening levels and detailed information on test methods, procedures and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

The CA723 is supplied in the 10-Lead TO-5 style ceramic package (T suffix), and is a direct replacement for industry type 723 in packages with similar terminal arrangements. It is also available in chip form (H suffix).

Applications

- **Series and shunt voltage regulator**
- **Floating regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Temperature controller**

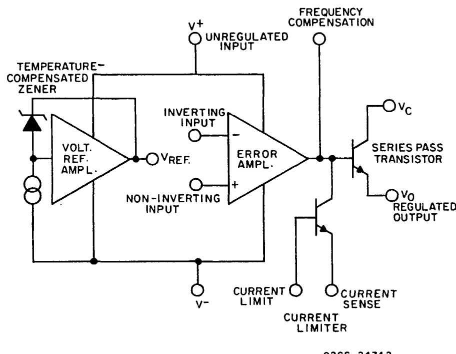


Fig. 1—Functional diagram of the CA723.

MAXIMUM RATINGS, *Absolute Maximum Values*

DC SUPPLY VOLTAGE		
(Between V+ and V− Terminals)	40	V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH		
(Between V+ and V− Terminals)	50	V
DIFFERENTIAL INPUT-OUTPUT VOLTAGE	40	V
DIFFERENTIAL INPUT VOLTAGE:		
Between Inverting and Non-Inverting Inputs	±5	V
Between Non-Inverting Input and V−	8	V
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF})	15	mA

DEVICE DISSIPATION:		
Up to T_A = 25°C		
CA723T	800	mW
Above T_A = 25°C		
CA723T	Derate linearly 6.3 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At a distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max.	+265	°C

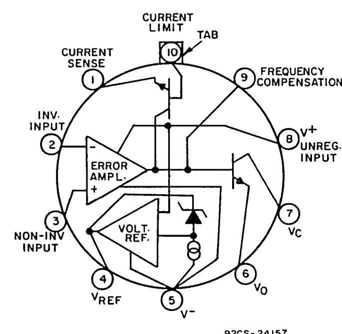


Fig. 2–Terminal arrangement of the CA723T in the TO-5 style package.

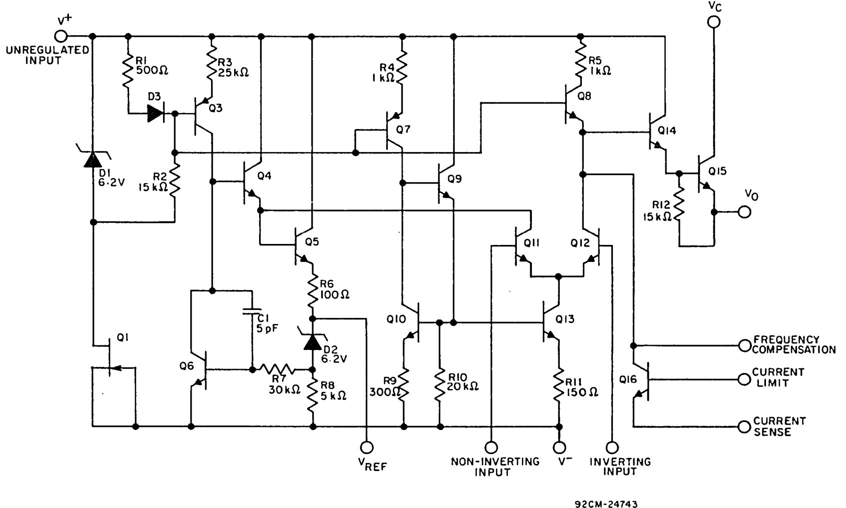


Fig. 3–Equivalent schematic diagram of the CA723.

ELECTRICAL CHARACTERISTICS *For Design Guidance Only*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (See Note) T_A = 25°C, V_I = V^+ = V_C = 12V, V^- = 0, V_O = 5V, I_L = 1 mA, C_I = 100 pF, $Z_{DIVIDER} \leq$ 10 kΩ (into error amplifier as shown in Fig. 14) unless otherwise indicated	CA723 Typ.	UNITS
Quiescent Regulator Current	I_Q	I_L = 0, V_I = 30 V	2.3	mA
Reference Voltage	V_{REF}		7.15	V
Line Regulation		V_I = 12 to 40 V	0.02	%V_O
		V_I = 12 to 15 V	0.01	
Load Regulation		I_L = 1 to 50 mA	0.03	%V_O
Output-Voltage Temperature Coefficient	ΔV_O	T_A = −55 to +125°C	0.002	%/°C
Ripple Rejection		f = 50 Hz to 10 kHz	74	
		f = 50 Hz to 10 kHz, C_{REF} = 5 µF	86	dB
Short-Circuit Limiting Current	I_{LIM}	R_{SCP} = 10 Ω V_O = 0	65	mA
Equivalent Noise Output Voltage	V_{NOISE}	BW = 100 to 10 kHz, C_{REF} = 0	20	
		BW = 100 to 10 kHz, C_{REF} = 5 µF	2.5	µV_{RMS}

Note: Line and load regulation specifications are given for condition of a constant chip temperature for high dissipation conditions, temperature drifts must be separately taken into account.

Table I. Pre Burn-In Electrical Post Burn-In Electrical Tests, and Delta Limits*

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX.Δ	
Reference Voltage	V_{REF}		6.95	7.35	±0.05	V
Quiescent Regulator Current	I_Q	I_L = 0 V_I=30V	–	3.5	±0.5	mA

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits
Level 3 requires pre burn-in test only. The burn-in and operating life test circuit is shown in Fig. 13

Table II. Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (See Note) $T_A=25°C, V_I=V^+=V_C=12V, V^-=0, V_O=5V, I_L=1mA, C_I=100pF, Z_{DIVIDER} \leqslant 10k\Omega$ (into error amplifier as shown in Fig. 14) unless otherwise indicated	LIMITS MINIMUM −55	LIMITS MINIMUM +25	LIMITS MINIMUM +125	LIMITS MAXIMUM −55	LIMITS MAXIMUM +25	LIMITS MAXIMUM +125	UNITS
Quiescent Regulator Current	I_Q	$I_L = 0, V_I = 30$ V	–	–	–	–	3.5	–	mA
Input Voltage Range	V_I		–	9.5	–	–	40	–	V
Output Voltage Range	V_O		–	2.0	–	–	37	–	V
Differential Input-Output Voltage	V_I-V_O		–	3.0	–	–	38	–	V
Reference Voltage	V_{REF}		–	6.95	–	–	7.35	–	V
Line Regulation		$V_I = 12$ to 40 V	–	–	–	–	0.2	–	$\%V_O$
		$V_I = 12$ to 15 V	–	–	–	0.3	0.1	0.3	$\%V_O$
Load Regulation		$I_L = 1$ to 50 mA	–	–	–	0.6	0.15	0.6	$\%V_O$

Note: Line and load regulation specifications are given for condition of a constant chip temperature: for high dissipation conditions, temperature drifts must be separately taken into account.

Table III. Group C Electrical Characteristics Sampling Tests
($T_A = 25°C, V_{CC} = +6$ V, $V_{EE} = -6$ V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Reference Voltage	V_{REF}		6.95	7.35	V
Line Regulation		$V_I = 12$ to 15 V	–	0.15	$\%V_O$
Load Regulation		$I_L = 1$ to 50 mA	–	0.2	$\%V_O$
Quiescent Regulator Current	I_Q	$I_L = 0$ $V_I = 30$ V	–	3.5	mA

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

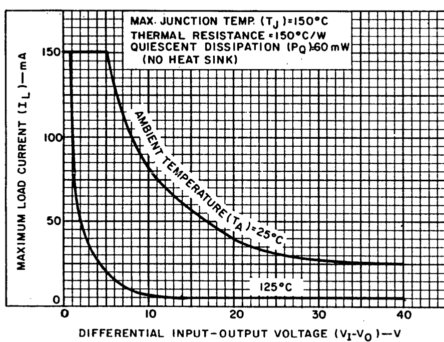


Fig. 4—Max. load current vs. differential input-output voltage.

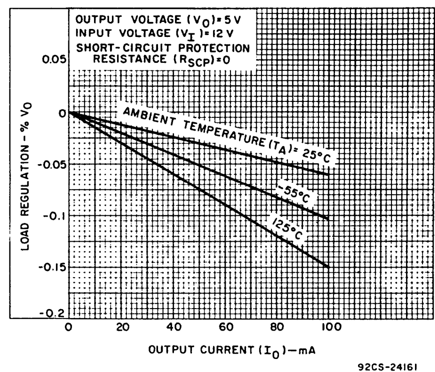


Fig. 5—Load regulation without current limiting.

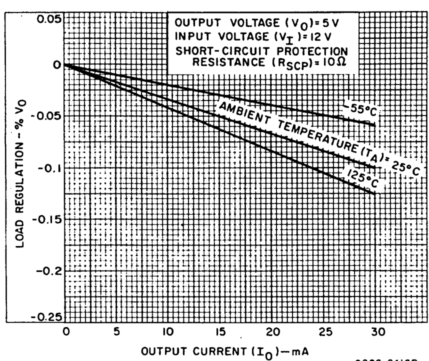


Fig. 6—Load regulation with current limiting.

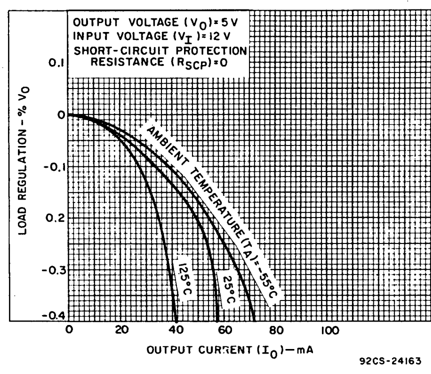


Fig. 7—Load regulation with current limiting.

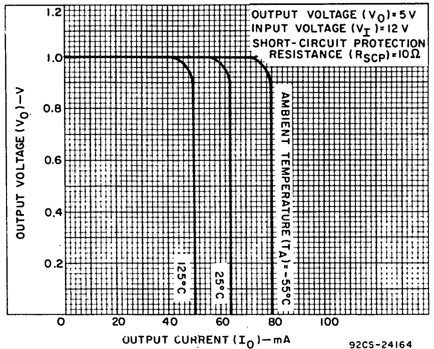


Fig. 8—Current limiting characteristics.

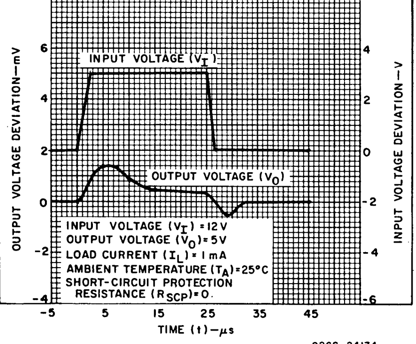


Fig. 9—Line transient response.

TYPICAL CHARACTERISTICS CURVES (Cont'd)

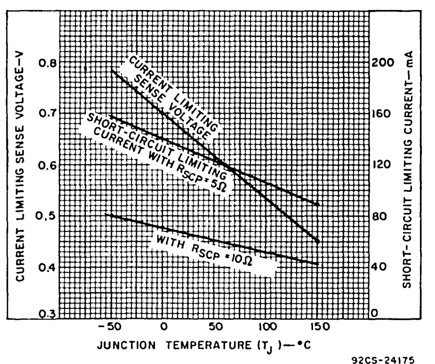


Fig. 10—Current limiting characteristics vs. junction temperature.

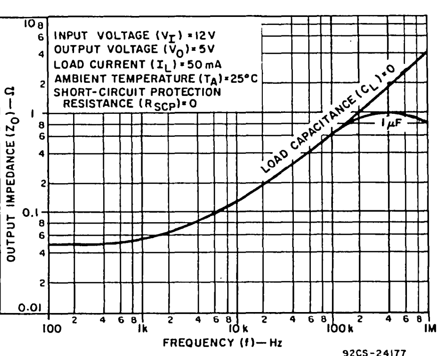


Fig. 11—Output impedance vs. frequency.

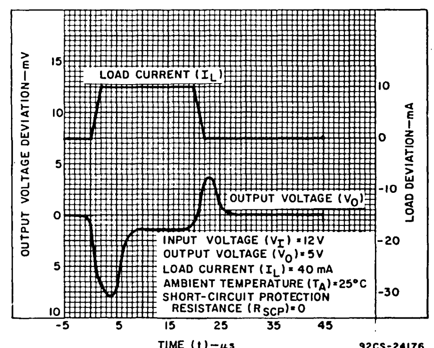


Fig. 12—Load transient response.

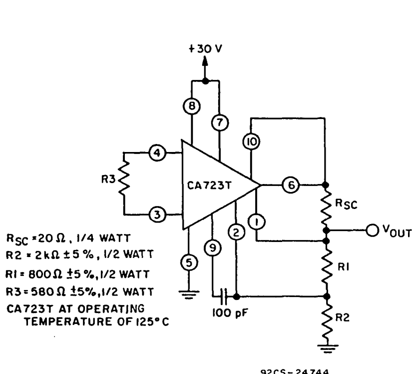


Fig. 13—Burn-in and operating life test circuit.

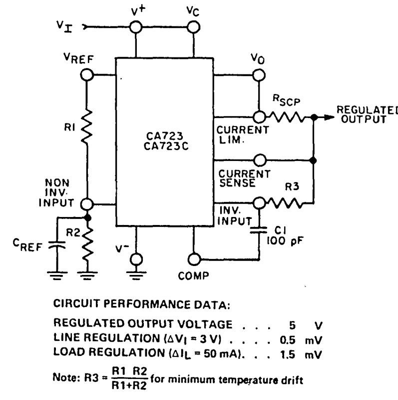


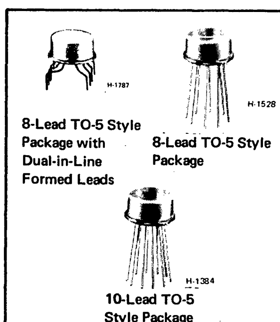
Fig. 14—Low-voltage regulator circuit (V_O = 2 to 7 volts).

Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CA741/..., CA747/..., CA748/..., CA1558/...



8-Lead TO-5 Style Package with Dual-in-Line Formed Leads

8-Lead TO-5 Style Package

10-Lead TO-5 Style Package

High-Reliability Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers

For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Input bias current (all types): 500 nA max.**
- **Input offset current (all types): 200 nA max.**

RCA-CA741, CA747, CA748, and CA1558 "Slash" (/) Series types are high-reliability linear integrated circuit High-Gain Single and Dual Operational Amplifiers intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard types described in Data Bulletin File No. 531 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

Applications:

- **Comparator**
- **DC amplifier**
- **Integrator or differentiator**
- **Multivibrator**
- **Narrow-band or band-pass filter**
- **Summing amplifier**

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA741, CA748, and CA1558 Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix) and in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN ("S" suffix). The CA747 is supplied in the 10-lead TO-5 style package ("T" suffix). All the types are also available in chip form ("H" suffix).

RCA TYPE NO.	NO. OF AMPLI.	PHASE COMP.	PACKAGE TYPE	OFFSET VOLT. NULL	A_{OL} (MIN.)	V_{IO} (MAX.)	T_A OPERATING RANGE	COMPATIBLE WITH INDUSTRY TYPE(S)
CA1558T	dual	internal	8-lead TO-5	no	50,000	5 mV	−55 to 125°C	MC1558, S5558
CA741	single	internal	8-lead TO-5	yes	50,000	5 mV	−55 to 125°C	µA741
CA747	dual	internal	10-lead TO-5	no	50,000	5 mV	−55 to 125°C	µA747
CA748	single	external	8-lead TO-5	yes	50,000	5 mV	−55 to 125°C	µA748

9-74

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC SUPPLY VOLTAGE (between V+ and V− terminals):

- CA741T, CA747T, CA748T, CA1558T . . . . 44 V

Differential Input Voltage . . . . ±30 V

DC Input Voltage* . . . . ±15 V

Output Short-Circuit Duration . . . . Indefinite

DEVICE DISSIPATION:

- Up to 75°C (CA741T, CA748T) . . . . 500 mW
- Up to 30°C (CA747T) . . . . 800 mW
- Up to 30°C (CA1558T) . . . . 680 mW

- Above Indicated Temperatures . . . . Derate linearly 6.67 mW/°C

Voltage between Offset Null and V−CA741T . . . . ±0.5 V

TEMPERATURE RANGE:

- Operating . . . . -55 to +125°C
- Storage . . . . -65 to +150 °C

LEAD TEMPERATURE (During Soldering)

- At distance 1/16±1/31 inch (1.59±0.79 mm) from case for 10 seconds max . . . . 300 °C

*If Supply voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.
▲Voltage values apply for each of the dual operational amplifiers.

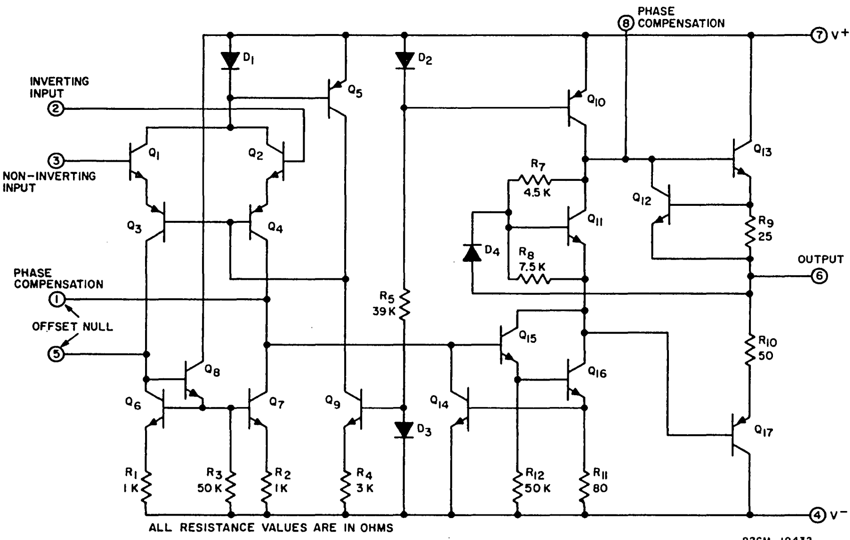
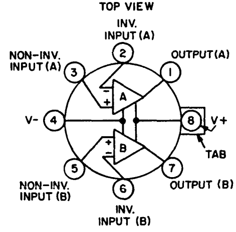


Fig. 1 — Schematic diagram of operational amplifier with external phase compensation for CA748T.

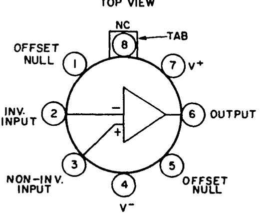
ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$*

CHARACTERISTICS	SYMBOLS	SUPPLY VOLTS $V^+ = +15$ V $V^- = -15$ V	TYP.	UNITS
Input Offset Voltage	V_{IO}	$R_S \leq 10$ kΩ	1	mV
Input Offset Current	I_{IO}		20	nA
Input Bias Current	I_{IB}		80	nA
Input Resistance	R_I		2	MΩ
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2$ kΩ, $V_O = \pm10$ V	200,000	
Common-Mode Input Voltage Range	V_{ICR}		±13	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10$ kΩ	90	dB
Supply Voltage Rejection Ratio	V_{RR}	$R_S \leq 10$ kΩ	30	μV/V
Output Voltage Swing	V_O(P-P)	$R_L \geq 10$ kΩ	±14	V
		$R_L \geq 2$ kΩ	±13	
Supply Current			1.7	mA
Device Dissipation	P_D		50	mW
Input Capacitance	C_I		1.4	pF
Offset Voltage Adjustment Range			±15	mV
Output Resistance	R_O		75	Ω
Output Short-Circuit Current			25	mA
Transient Response Risetime	t_r	Unity Gain $V_I = 20$ mV	0.3	μs
Overshoot		$R_L = 2$ kΩ, $C_L \leq 100$ pF	5.0	%
Slew Rate: Closed Loop	SR	$R_L \geq 2$ kΩ	0.5	V/μs
Open Loop▲			40	

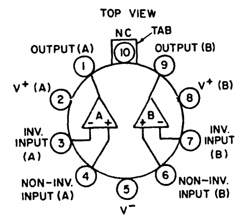
•Values apply for each of the dual operational amplifiers.



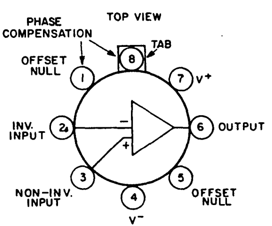
(a) — Functional diagram of CA1558T with internal phase compensation.



(b) — Functional diagram of CA741T with internal phase compensation.



(c) — Functional diagram of CA747T with internal phase compensation.



(d) — Functional diagram of CA748T with external phase compensation

Fig. 2—Functional diagrams of operational amplifiers.

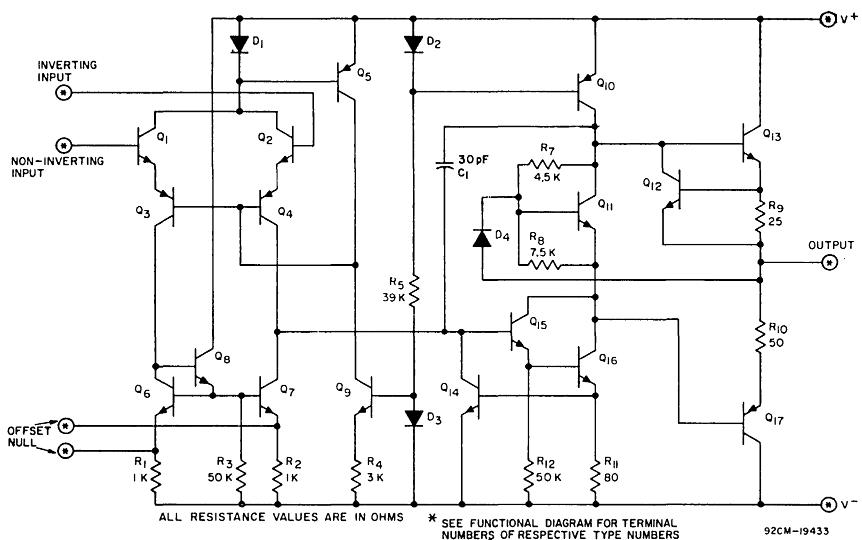


Fig. 3 – Schematic diagram of operational amplifiers with internal phase compensation for CA741T and for each amplifier of the CA748T and CA1558T.

Table I – Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits For All Types*

ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$, $V^+ = +15V$, $V^- = -15$ V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Offset Voltage	V_{IO}		–	5	±1	mV
Input Offset Current	I_{IO}		–	200	±24	nA
Input Bias Current	I_I		–	500	±60	nA
Device Dissipation	P_D			85	±18	mW

*Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 5.

Table II – Final Electrical and Group A. Electrical Sampling Inspection for All Types

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V	LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM			MAXIMUM			UNITS
			−55	+25	+125	−55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	6	5	6	mV
Input Offset Current	I_{IO}	–	–	–	–	500	200	200	nA
Input Bias Current	I_I	–	–	–	–	1500	500	500	nA
Supply Current		–	–	–	–	3.8	3.3	2.8	mA
Device Dissipation	P_D	–	–	–	–	100	85	75	mW
DYNAMIC									
Open-Loop Differential Voltage Gain	A_{OL}	$R_L = 2$ k, $V_O = \pm 10$ V	25000	50000	25000	–	–	–	
Common-Mode Rejection Ratio	CMRR	–	70	70	70	–	–	–	dB
Maximum Output-Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	±12 ±10	±12 ±10	±12 ±10	– –	– –	– –	V
Input Resistance	R_I	–	–	0.3	–	–	–	–	MΩ
Common-Mode Input-Voltage Range	V_{ICR}	$R_S \leqslant 10$ kΩ	±12	±12	±12	–	–	–	V
Supply Voltage Rejection Ratio	V_{RR}	$R_S \leqslant 10$ kΩ				150	150	150	μV/V

Table III – Group C. Electrical Characteristics Sampling Tests

$T_A = +25°C$ $V^+ = +15$ V, $V^- = -15$ V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS MIN.	MAX.	UNITS
Input Offset Voltage	V_{IO}	–	–	8	mV
Input Offset Current	I_{IO}	–	–	240	μA
Input Bias Current	I_I	–	–	800	μA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L = 2$ k, $V_O = \pm 10$ V	33000	–	
Supply Current			–	3	mA

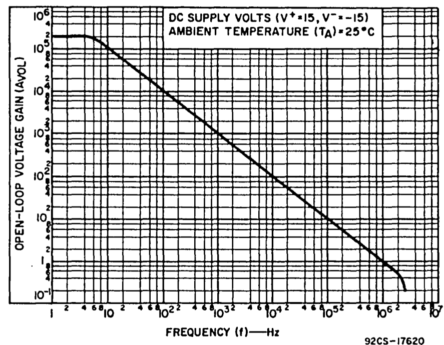


Fig.4 — Open-loop voltage gain vs. frequency for all types.

▲ THESE RESISTORS MAY BE ADJUSTED TO GIVE REQUIRED DRIVE UNDER DIFFERENT LOAD CONDITIONS

92CM-22837

TERMINAL No'S IN CIRCLES ARE FOR UNIT No. 1
TERMINAL No'S IN SQUARES ARE FOR UNIT No. 2

Fig.5 — Burn-in and operating life test circuit for CA741, CA747, CA748, CA1558.

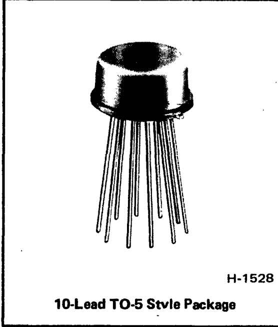
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3000/. . .



H-1528

10-Lead TO-5 Style Package

High-Reliability DC Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Input Impedance** .... **195 KΩ typ.**
- **Voltage Gain** .... **37 dB typ.**
- **Common-Mode Rejection Ratio** .... **98 dB typ.**
- **Input Offset Voltage** .... **1.4 mV typ.**
- **Push-Pull Input and Output**
- **Frequency Capability**
  DC to 30 MHz (with external C and R)
- **Wide AGC Range** .... **90 dB typ.**

Applications

- **Schmitt Trigger**
- **RC-Coupled Feedback Amplifier**
- **Mixer**
- **Comparator**
- **Modulator**
- **Crystal Oscillator**
- **Sense Amplifier**
- **See Companion Application Note ICAN-5030 "Applications of RCA-CA3000 IC DC Amplifier."**

RCA-CA3000 "Slash" (/) Series type is a high-reliability linear integrated circuit DC Amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3000 described in Data Bulletin File No. 121 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3000 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

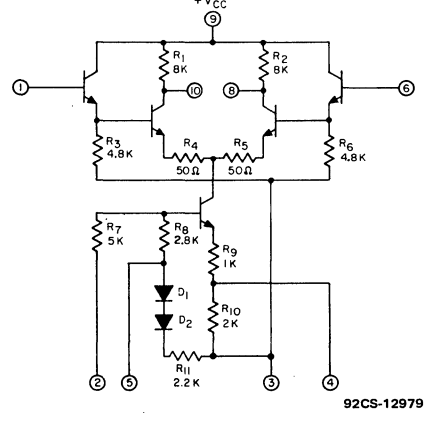


Fig. 1 — Schematic diagram

Maximum Ratings, Absolute-Maximum Values

OPERATING TEMPERATURE RANGE . . . . . . -55°C to +125°C
STORAGE-TEMPERATURE RANGE. . . . . -65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16" ±1/32"
(1.59 mm ±0.79 mm)
from case for 10 s max. 265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE . . ±2 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE . . ±2 V
MAXIMUM DEVICE DISSIPATION. . . . . 300 mW

Absolute Maximum Voltage and Current Limits at T_A = 25° C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 9 is 0 to −12 volts.

Terminal No.	1	2	3	4	5	6	7	8	9	10
1		*	+16▲ 0	*	*	+4 -4	Internal Connection Do not use	*	0 -12	+1 -12
2			+16 -5	*	*	*		*	0 -16	*
3				+5 -5	+5 -10	0 -16		*	0 -16	*
4					*	*		*	0 -16	*
5						*		*	0 -16	*
6								+1 -12	0 -12	*
7	Internal Connection Do not use									
8									0 -16	*
9										+16 0
10										
Case	Connected to Terminal #3 – Do Not Ground									

Maximum Current Ratings

Terminal No.	I_{IN} mA	I_{OUT} mA
1	1	0.1
2	–	–
3	–	–
4	–	–
5	1	0.1
6	–	–
7	–	–
8	–	–
9	–	–
10	–	–

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ This rating applies to the more positive of Terminals #1 or #6.

ELECTRICAL CHARACTERISTICS, *at $T_A = 25^oC$, $V^+ = +6$ V, $V^- = -6$V, unless otherwise specified*

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		LIMITS TYPE CA3000 Typ.	Units
STATIC CHARACTERISTICS					
Input Offset Voltage	V_{IO}			1.4	mV
Input Offset Current	I_{IO}			1.2	μA
Input Bias Current	I_I			23	μA
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS			
		4	5		
		NC	NC	2.6	V
		NC	V^-	4.2	V
		V^-	NC	-1.5	V
		V^-	V^-	0.6	V
Device Dissipation	P_T	NC	NC	30	mW
DYNAMIC CHARACTERISTICS					
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz		32	dB
		Double-Ended Output f = 1 kHz		37	dB
Bandwidth at -3 dB Point	BW			650	kHz
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz		6.4	V(P-P)
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		98	dB
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz		195K	Ω
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz		8K	Ω
Total Harmonic Distortion	THD	f = 1 kHz		0.2	%
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz		90	dB

Table I — Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions $V^+ = +6$ V, $V^- = -6$ V		Limits for Indicated Temp. (°C) Minimum -55	Minimum +25	Minimum +125	Maximum -55	Maximum +25	Maximum +125	Units
STATIC										
Input Offset Voltage	V_{10}	–		–	–	–	6.5	5	6.5	mV
Input Offset Current	I_{IO}	–		–	–	–	20	10	20	µA
Input Bias Current	I_I	–		–	–	–	70	36	25	µA
Quiescent Operating Voltage	V_8 or V_{10}	Terminal 4	Terminal 5							
		NC	NC	1.5	1.5	1.5	3.2	3.2	3.2	V
Device Dissipation	P_T	Terminal 4	Terminal 5							
		NC	NC	30	25	20	60	60	50	mW
		NC	-V	25	20	15	55	55	50	mW
		-V	NC	55	50	45	105	105	90	mW
		-V	-V	35	35	25	70	70	65	mW
DYNAMIC All tests at 1 kHz, except BW										
Differential Voltage Gain	A_{Diff}		Single-Ended Output	–	28	–	–	–	–	dB
Maximum Output Voltage	V_{OUT} (p-p)	f = 1 kHz		–	5	–	–	–	–	V_{p-p}
Bandwidth at -3 dB Point	BW	$V_I = 10$ mV, $R_S = 1$ kΩ		–	600	–	–	–	–	kHz
Common-Mode Rejection Ratio	CMR	f = 1 kHz		–	70	–	–	–	–	dB
Single-Ended Input Impedance	Z_{IN}			–	70 k	–	–	–	–	Ω
Single-Ended Output Impedance	Z_{OUT}			–	5.5 k	–	–	10.5 k	–	Ω
Total Harmonic Distortion	THD			–	–	–	–	5	–	%
AGC Range (Maximum Voltage Gain to Complete Cut-off)	AGC	f = 1 kHz		–	80	–	–	–	–	dB

Table II – *Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits**

Electrical Characteristics, at T_A = 25° C, V^+ = +6 V, V^- = -6 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	LIMITS MAX. Δ	UNITS
Input Offset Current	I_I	–	–	36	±4	μA
Quiescent Operating Voltage	V_8 or V_{10}	Terminal 4: NC Terminal 5: NC	1.5	3.2	±0.3	V
Device Dissipation	P_T	Terminal 4: NC Terminal 5: NC	25	60	±6	mW

*Levels 1 and 2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level 3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 7.

Table III – *Final Electrical Tests*

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = +6 V, V^- = -6 V	LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM			MAXIMUM			UNITS
				−55	+25	+125	−55	+25	+125	
Static	Input Offset Voltage	V_{IO}	–	–	–	–	6.5	5	6.5	mV
Static	Input Offset Current	I_{IO}	–	–	–	–	20	10	20	μA
Static	Input Bias Current	I_I	–	–	–	–	70	36	25	μA
Static	Quiescent Operating Voltage	V_8 or V_{10}	Terminals 4 and 5 No connection	1.5	1.5	1.5	3.2	3.2	3.2	V
Static	Device Dissipation	P_T	Terminals 4 and 5 No Connection	30	25	20	60	60	50	mW
Dynamic	Differential Voltage Gain Single Ended Output	A_{Diff}	f = 1 kHz	–	28	–	–	–	–	dB

Table IV – *Group C Electrical Characteristics Sampling Tests* (T_A = 25°C)

Characteristic	Symbol	TEST CONDITIONS V^+ = +6 V, V^- = -6 V	Limits Min.	Limits Max.	Units
Input Offset Voltage	V_{IO}		–	5	mV
Input Offset Current	I_{IO}		–	10	μA
Input Bias Current	I_I		–	36	μA
Quiescent Operating Voltage	V_8 or V_{10}		1.5	3.2	V
Device Dissipation	P_T		25	60	mW
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single Ended Output f = 1 kHz	28	–	dB

STATIC CHARACTERISTICS

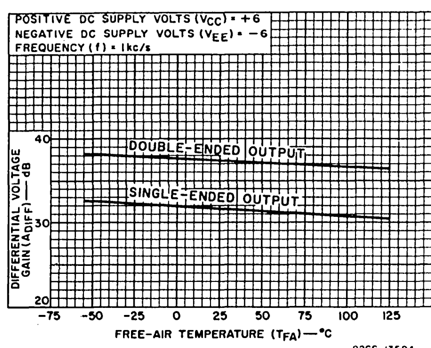


Fig.2— Differential voltage gain vs temperature

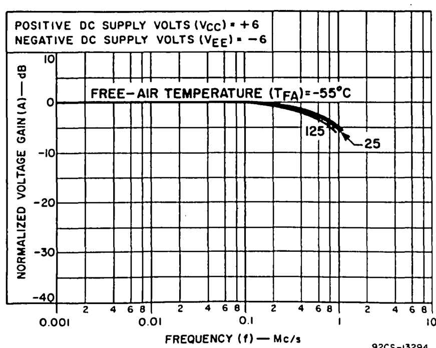


Fig.3— Bandwidth at -3 dB point vs temperature

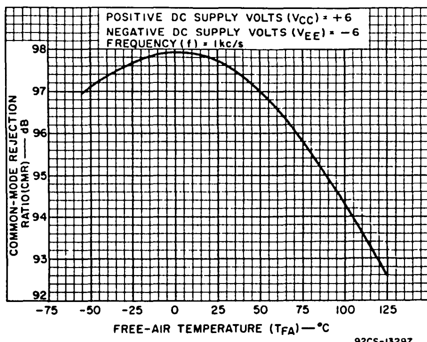


Fig.4— Common-mode rejection ratio vs temperature

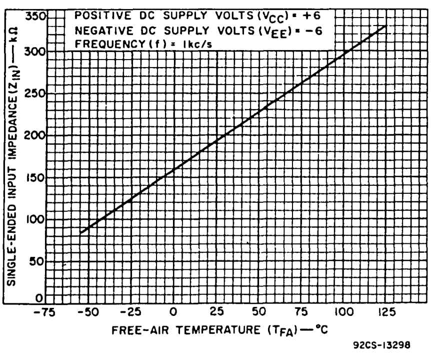


Fig.5—Single-ended input impedance vs temperature

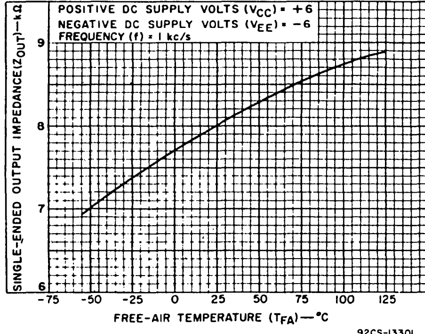


Fig.6— Single-ended output impedance vs temperature

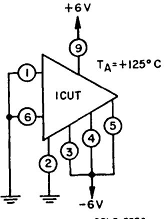


Fig.7— Burn-in and operating life test circuit

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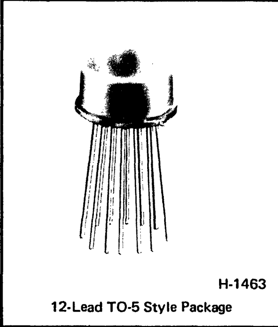
High-Reliability Slash(/) Series CA3001/. . .



H-1463
12-Lead TO-5 Style Package

High – Reliability Video Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Push-Pull Input & Output**
- **AGC Range . . . . 60 dB typ.**
- **Bandwidth . . . . 29 MHz**
- **Input Resistance . . . . 150 kΩ typ.**
- **Output Resistance . . . . 45 Ω typ.**
- **Voltage Gain . . . . 19 dB typ.**
- **Input Offset Voltage . . . . 1.5 mV typ.**

RCA-CA3001 "Slash" (/) Series type is a high-reliability linear integrated circuit Video Amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3001 described in Data Bulletin File No. 122 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3001 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications

- **DC, IF, & Video Amplifier**
- **Schmitt Trigger**
- **Mixer**
- **Modulator**
- **See Companion Application Note ICAN-5038 "Applications of the RCA-CA3001 IC Video Amplifier"**

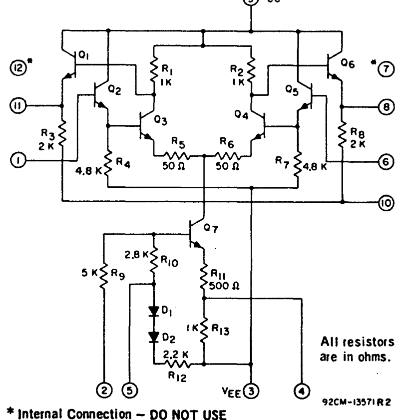


Fig. 1 – Schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values*

OPERATING TEMPERATURE RANGE	−55°C to +125°C
STORAGE TEMPERATURE RANGE	−65°C to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max.	265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±2.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	±2.5 V
MAXIMUM DEVICE DISSIPATION	300 mW

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS *at $T_A = 25°C$*

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals. All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10&No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Not Connected Unless Specified			LIMITS TYPE CA3001 Typ.	Units
STATIC CHARACTERISTICS:						
Input Offset Voltage	V_{IO}				1.5	mV
Input Offset Current	I_{IO}				1	μA
Input Bias Current	I_I				16	μA
Output Offset Voltage	V_{OO}				54	mV
		TERMINALS				
		MODE	4	5		
Quiescent Operating Voltage	V_8 OR V_{11}	A	NC	NC	4.4	V
		B	NC	V_{EE}	4.8	V
		C	V_{EE}	NC	2.7	V
		D	V_{EE}	V_{EE}	4	V
Device Dissipation	P_T	A	NC	NC	78	mW
		B	NC	V_{EE}	71	mW
		C	V_{EE}	NC	110	mW
		D	V_{EE}	V_{EE}	86	mW
DYNAMIC CHARACTERISTICS:						
Differential Voltage Gain (Single-ended input and output)	A_{DIFF}	f = 1.75 MHz f = 20 MHz			19 14	dB dB
Bandwidth at -3 dB Point	BW				29	MHz
Maximum Output Voltage Swing	$V_{OUT}(P\text{-}P)$	f = 1.75 MHz			5	$V_{P\text{-}P}$
Noise Figure	NF	f = 1.75 MHz, R_S = 1 KΩ			5	dB
		f = 11.7 MHz, R_S = 1 KΩ			7.7	dB
Common-Mode Rejection Ratio	CMR	f = 1 KHz			88	dB
Input Impedance Components:						
Parallel Input Resistance	R_{IN}	f = 1.75 MHz			140	KΩ
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz			3.4	pF
Output Resistance	R_{OUT}	f = 1.75 MHz			45	Ω
AGC Range (Maximum voltage gain to complete cutoff)	AGC	f = 1.75 MHz			60	dB

Table I. Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions V_{CC} = +6V, V_{EE} = -6V		Limits for Indicated Temp. (°C) Minimum			Maximum			Units
				-55	+25	+125	-55	+25	+125	
Static										
Input Unbalance Current	I_{IU}	–		–	–	–	23	10	5	μA
Input Bias Current	I_I	–		–	–	–	66	36	22	μA
Output Offset Voltage	V_{oo}	–		–	–	–	420	300	260	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4	Terminal 5							
		NC	NC	3.8	3.8	3.8	4.8	4.8	4.8	V
Device Dissipation	P_T	Terminal 4	Terminal 5							
		NC	NC	60	60	50	125	115	110	mW
		NC	$-V_{EE}$	55	55	45	120	105	105	mW
		$-V_{EE}$	NC	80	80	70	175	160	155	mW
		$-V_{EE}$	$-V_{EE}$	60	60	50	135	125	125	mW
Dynamic										
Differential Voltage Gain (single-ended input and output)	A_{Diff}	f = 1.75 MHz		–	16	–	–	–	–	dB
		f = 20 MHz		–	10	–	–	–	–	dB
Bandwidth at -3 dB Point	BW			–	16	–	–	–	–	MHz
Maximum Output Voltage Swing	V_{OUT} (p-p)	f = 1.75 MHz		–	4	–	–	–	–	V_{p-p}
Noise Figure	NF	f = 1.75 MHz, R_s = 1kΩ		–	–	–	–	8	–	dB
Common-Mode Rejection Ratio	CMR	f = 1 kHz		–	70	–	–	–	–	dB
Common Mode Input Voltage Range	V_{CMR}	f = 1 kHz		–	-.35 to +2.5	–	–	–	–	V
Parallel Input R	R_{IN}	f = 1.75 MHz		–	50	–	–	–	–	kΩ
Parallel Input C	C_{IN}	f = 1.75 MHz		–	–	–	–	7	–	pF
Output Resistance	R_{OUT}	f = 1.75 MHz		–	–	–	–	70	–	Ω
AGC Range (max. voltage gain to complete cutoff)	AGC	f = 1.75 MHz		–	55	–	–	–	–	dB

*Table II. Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits**

Electrical Characteristics, at T_A = 25°C, V^+ = +6 V, V^- = −6 V

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Max.	Max.Δ	
Input Offset Current	I_{IO}	–	–	10	±2	μA
Input-Bias Current	I_I	–	–	36	±4	μA
Output Offset Voltage	V_{OO}	–	–	300	±100	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4: NC Terminal 5: NC	3.8	4.8	±0.5	V
Device Dissipation	P_T	Terminal 4: NC Terminal 5: NC	60	115	±12	mW

*Level /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 5.

Table III. Final Electrical Tests

	Characteristic	Symbol	Test Conditions V^+ = +6 V, V^- = −6 V	Limits for Indicated Temp. (°C)						Units
				Minimum			Maximum			
				-55	+25	+125	-55	+25	+125	
Static	Input Offset Current	I_{IO}	–	–	–	–	–	10	–	μA
Static	Input Bias Current	I_I	–	–	–	–	66	36	22	μA
Static	Output Offset Voltage	V_{OO}	–	–	–	–	420	300	260	mV
Static	Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4: NC Terminal 5: NC	3.8	3.8	3.8	4.8	4.8	4.8	V
Static	Device Dissipation	P_T	Terminal 4: NC Terminal 5: NC	–	60	–	–	115	–	mW
Dynamic	Differential Voltage Gain (single-ended input & output)	A_{Diff}	f = 1.75 MHz	–	16	–	–	–	–	dB

Table IV. Group C Electrical Characteristics Sampling Tests (T_A = 25°C, V_C = +6V, V_{EE} = −6 V)

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Input Bias Current	I_I	–	–	36	μA
Output Offset Voltage	V_{OO}	–	–	300	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4 5: NC NC	3.8	4.8	V
Device Dissipation	P_T	Terminal 4 5: NC NC	60	115	mW
Voltage Gain	A_{Diff}	f = 1.75 MHz	16	–	dB

TYPICAL DYNAMIC CHARACTERISTICS

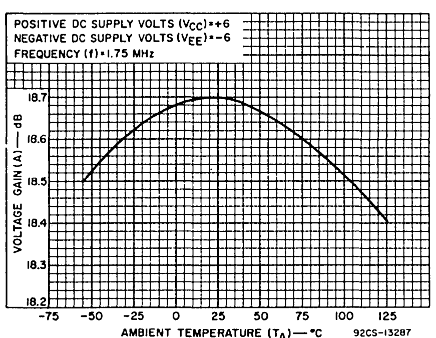


Fig. 2 — Differential voltage gain vs. temperature.

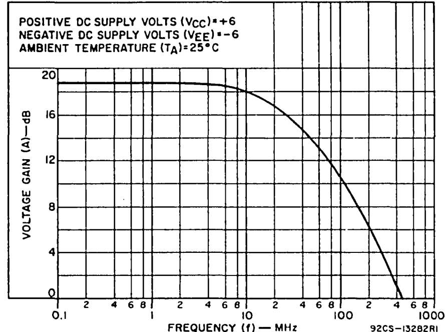


Fig. 3 — Differential voltage gain vs. frequency.

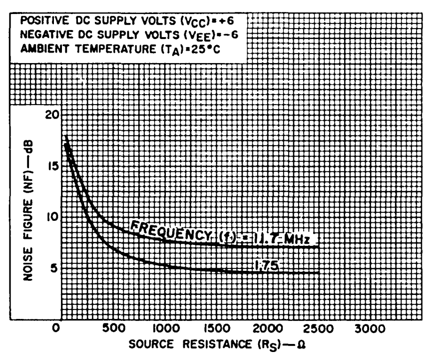


Fig. 4 — Noise figure vs. source resistance and frequency.

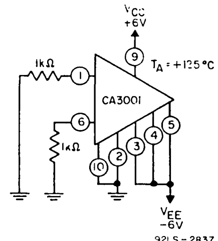


Fig. 5 — Burn-in and operating life test circuit.

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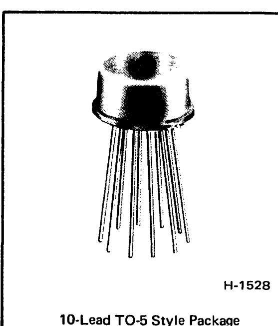
High-Reliability Slash(/) Series CA3002/. . .



H-1528

10-Lead TO-5 Style Package

High-Reliability IF Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Input Resistance — 100 kΩ typ.**
- **Output Resistance — 70 Ω typ.**
- **Voltage Gain — 24 dB typ. @ 1.75 MHz**
- **Push-Pull Input, Single-Ended Output**
- **-3 dB Bandwidth — 11 MHz typ.**
- **AGC Range — 80 dB typ.**
- **Useful Frequency Range DC to — 15 MHz**

RCA-CA3002 Slash (/) Series type is a high-reliability integrated-circuit IF Amplifier intended for applications in aerospace, military, and critical industrial equipment. It is electrically and mechanically identical with the standard type CA3002 described in Data Bulletin File No. 123 but is specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3002 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix), or in chip form ("H" suffix).

- **Product Detector**
- **AM Detector**
- **IF & Video Amplifier**
- **Schmitt Trigger**
- **See Companion Application Note ICAN-5038 "Application of RCA-3002 IC IF Amplifier"**

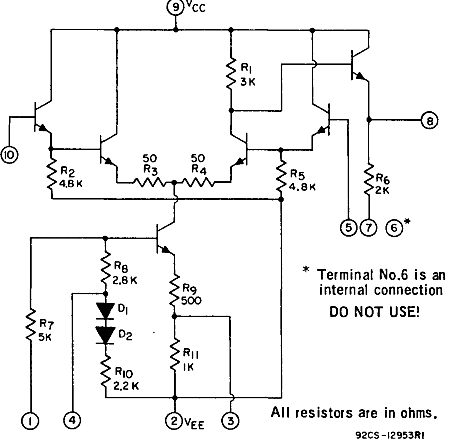


Fig. 1 Schematic Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

OPERATING TEMPERATURE RANGE . . . . -55°C to +125°C
STORAGE-TEMPERATURE RANGE . . . . -65°C to +150°C
MAXIMUM INPUT-SIGNAL VOLTAGE . . . . ±3.5 V
MAXIMUM DEVICE DISSIPATION . . . . 300 mW

LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32"
(1.59 mm ± 0.79 mm)
from case for 10 s max. . . . . 265°C

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, at $T_A = 25°C$

Indicated voltage or current limits for each terminal can be applied under the specified operating conditions for other terminals.

All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$) or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-8 V	0 V	2, 7 5, 10 9	-8 0 +6
2	-10 V	0 V	1, 5, 10 9	0 +6
3	-8.5 V	0 V	1, 5, 10 7 9	0 -6 +6
4	-8 V	0 V	1, 5, 10 2, 7 9	0 -8 +6
5	-3.5 V	+3.5 V	1, 10 2, 7 9	0 -6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL No.2 (SUBSTRATE) DO NOT GROUND			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
6	INTERNAL CONNECTION DO NOT USE			
7	-12 V	0 V	1, 5, 10 2 9	0 -6 +6
8	20 mA		1, 5, 7, 10 2 9 200 Ω Resistor Between Terminals 7 & 8	0 -6 +6
9	0 V	+10 V	1, 5, 10 2, 3, 7	0 -6
10	-3.5 V	+3.5 V	1, 5 2, 7 9	0 -6 +6

*Table 1 — Pre-Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT $T_A = 25°C$, $V^+ = +6$ V, $V^- = -6$ V	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Bias Current	I_I	$V^+ = +6$ V, Terminal No. 2 = -6 V, Terminal No. 1 to ground	—	31	±10	μA
Total Drain Current	I_T	$I_2 = I_9 = I_T$	5.0	15.8	±1.5	mA

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 7.

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C,* V^+ = +6 V, V^- = −6 V

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS TERMINALS No.3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED			LIMITS CA3002 Typ.	Units
STATIC CHARACTERISTICS:						
Input Unbalance Voltage	V_{IU}				2.2	mV
Input Unbalance Current	I_{IU}				2.2	μA
Input Bias Current	I_I				20	μA
Quiescent Operating Voltage		MODE	TERMINAL 2	TERMINAL 4		
		A	V_{EE}	NC	2.8	V
		B	V_{EE}	V_{EE}	3.9	V
Device Dissipation	P_T				55	mW
DYNAMIC CHARACTERISTICS:						
Differential Voltage Gain (Single-Ended Input and Output)	A_{DIFF}	f = 1.75 MHz			24	dB
Bandwidth at -3 dB Point	BW	-			11	MHz
Maximum Output Voltage Swing	$V_{OUT}(P\text{-}P)$	-			5.5	$V_{P\text{-}P}$
Noise Figure	NF	f = 1.75 MHz R_S = 1 kΩ			4	dB
Input Impedance Components: Parallel Input Resistance	R_{IN}	f = 1.75 MHz			100k	Ω
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz			4	pF
Output Resistance	R_{OUT}	f = 1.75 MHz			70	Ω
3rd Harmonic Inter-modulation Distortion	IMD	-			-40	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff	AGC	f = 1.75 MHz			80	dB

Table II – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6$ V, $V^- = -6$ V	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Input Unbalance Current	I_{IU}	$I_{10} - I_5 = I_{IU}$	–	–	–	35	10	10	μA
Input Bias Current	I_I		–	–	–	85	35	30	μA
Total Drain Current	I_T	$I_2 + I_9 = I_T$	–	–	–	167	15.8	15.0	mA

Table III – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6$ V, $V^- = -6$ V	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Static									
Input Unbalance Current	I_{IU}	$I_{10} - I_5 = I_{IU}$	–	–	–	35	10	10	μA
Input Bias Current	I_I		–	–	–	85	35	30	μA
Total Drain Current	I_T	$I_2 + I_9 = I_T$	–	–	–	16.7	15.8	15.0	mA
Max Output Voltage	$+V_{OM}$		–	4.6	–	–	5.4	–	V
Min. Output Voltage	$+V_{OM}$	Terminal No. 1 Ground	–	–	–	–	0.05	–	V
Dynamic									
Noise Figure	NF	f = 1.75 MHz, R_S = 1 kΩ	–	–	–	–	8	–	dB
Voltage Gain	A	f = 1.75 MHz, single-ended input and output	–	19	–	–	–	–	dB
AGC Range (Maximum Voltage gain to complete cutoff)	AGC	f = 1.75 MHz	–	60	–	–	–	–	dB

Table IV – Group C Electrical Characteristics Sampling Tests ($T_A = 25^oC$)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6$ V, $V^- = -6$ V	LIMITS		UNITS
			MIN.	MAX.	
Input Unbalance Current	I_{IU}	$I_{10} - I_5 = I_{IU}$	–	10	μA
Input Bias Current	I_I		–	35	μA
Total Drain Current	I_T	$I_2 + I_9 = I_T$	5.0	15.8	mA
Voltage Gain	A	f = 1.75 MHz, single-ended input and output	19	–	dB

DYNAMIC CHARACTERISTICS

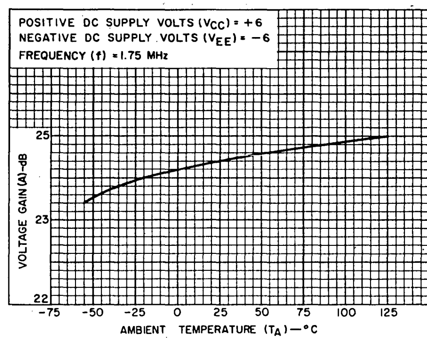


Fig.2 — Differential voltage gain vs temperature.

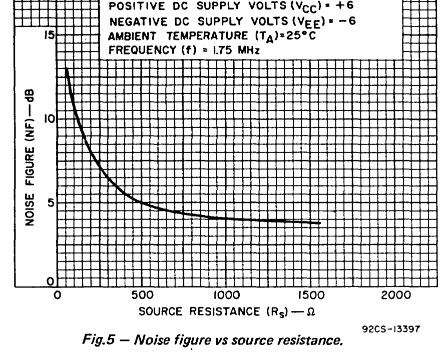


Fig.5 — Noise figure vs source resistance.

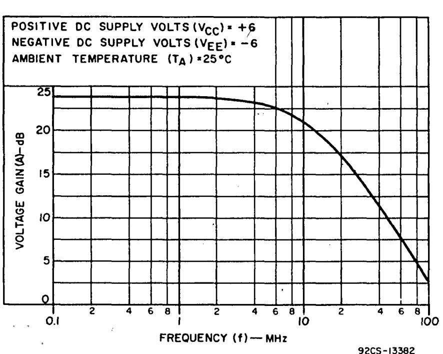


Fig.3 — Differential voltage gain vs frequency.

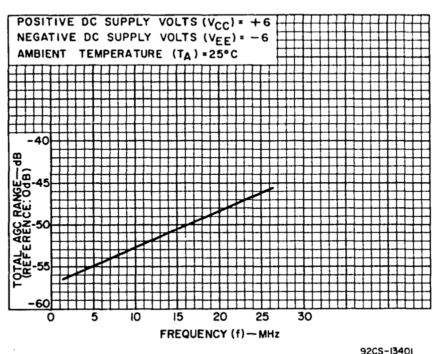


Fig. 6 — AGC range vs frequency.

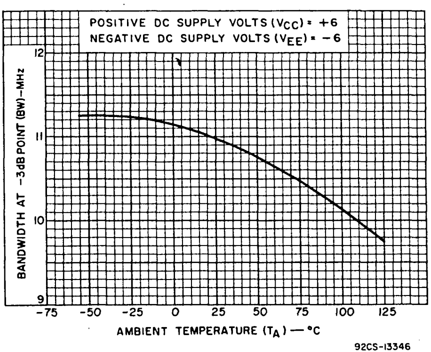


Fig.4 — Bandwidth at -3 dB point vs temperature.

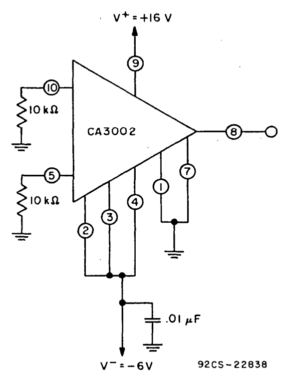


Fig. 7 — Burn-in and operating life test circuit.

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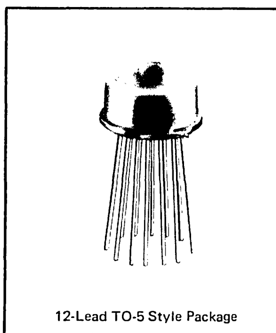
High-Reliability Slash(/) Series CA3004/. . .



12-Lead TO-5 Style Package

High-Reliability RF Amplifier

For Aerospace, Military and Critical Industrial Equipment

Features:

- **Operation from DC to 100 MHz**
- **RF, IF, and Video frequency capability**
- **Balanced differential amplifier configuration with controlled constant-current source**

Applications:

- **Detector**
- **Push-Pull Input and Output**
- **Wide and Narrow-Band Amplifier**
- **AGC**
- **Mixer**
- **Limiter**
- **Modulator**
- **Companion Application Note ICAN-5022 "Applications of RCS-CA3004, CA3005, and CA3006 IC RF Amplifiers"**

RCA-CA3004 "Slash" (/) Series type is a high-reliability linear integrated circuit RF Amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3004 described in Data Bulletin File No. 124 but is specially processed and tested to meet the electrical, mechanical and enviromental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3004 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

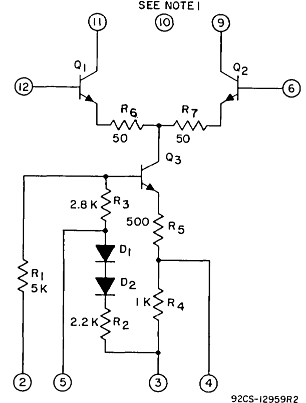


Fig. 1 — Schematic Diagram

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at $T_A = 25°C$

Voltage limits shown for each terminal can be applied under the indicated circuit conditions for other terminals.
All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	NO CONNECTION			
2	-9.5	0	6 12 3 9 10 11	0 0 -9.5 +6 +6 +6
3	-12	0	2 6 9 10 11 12	0 0 +6 +6 +6 0
4	-12	0	2 6 9 10 11 12	0 0 +6 +6 +6 0
5	-6	0	2,6,12 3 9 10 11	0 -6 +6 +6 +6
6	-3.5	+3.5	2 3 9 10 11 12	0 -6 +6 +6 +6 0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
7	NO CONNECTION			
8	NO CONNECTION			
9	0	+12	2 3 6 10 11 12	0 -6 0 +6 +6 0
10	0	+12	2 3 6 9 11 12	0 -6 0 +6 +6 0
11	0	+12	2 3 6 10 11 12	0 -6 0 +6 +6 0
12	-3.5	+3.5	2 3 6 9 10 11	0 -6 0 +6 +6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL NO.3 (SUBSTRATE) DO NOT GROUND			

MAXIMUM RATINGS, *Absolute-Maximum Values*

MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±3.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	−2.5 V, +3.5 V
MAXIMUM DEVICE DISSIPATION	300 mW
OPERATING-TEMPERATURE RANGE	−55°C to +125°C
STORAGE-TEMPERATURE RANGE	−65°C to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max.	265°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V^+ = +6V, V^- = -6 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Terminals No.4 and No.5 Open Unless Otherwise Specified		LIMITS TYPE CA3004 Typ.	Units
STATIC CHARACTERISTICS					
Input Offset Voltage	V_{IO}			1.7	mV
Input Offset Current	I_{IO}			0.125	μA
Input Bias Current	I_I			21	μA
		TERMINALS 4	TERMINALS 5		
Quiescent Operating Current	I_9 or I_{11}	NC	NC	1	mA
		V^-	NC	2.7	mA
		NC	V^-	0.45	mA
		V^-	V^-	1.25	mA
Quiescent Operating Current Ratio	I_9/I_{11}			1.1	–
Device Dissipation	P_T			26	mW
DYNAMIC CHARACTERISTICS					
Power Gain	G_P	f = 100 MHz		12	dB
Noise Figure	NF	f = 100 MHz		6.3	dB
Common Mode Rejection Ratio	CMRR	f = 1 kHz		98	dB
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz		–	dB

*Table I – Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS T_A = 25°C, V^+ = +6 V, V^- = –6 V	LIMITS MIN.	MAX.	MAX. Δ	UNITS
Input Offset Voltage	V_{IO}		–	5	±2	mV
Input Bias Current	I_I		–	40	±4	μA
Device Dissipation	P_D		–	45	±5	mW

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 4.

Table II – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6V, V^- = -6V$	LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM			MAXIMUM			UNITS
			−55	+25	+125	−55	+25	+125	
STATIC									
Device Dissipation	P_D		–	16	–	–	45	–	mW
Input Offset Current	I_{IO}		–	–	–	9	5	7	μA
Input Bias Current	I_I		–	–	–	60	40	40	μA
DYNAMIC									
Power Gain	G_P	Diff. Amp., f = 100 MHz	–	10	–	–	–	–	dB
Noise Figure	NF	Diff. Amp., f = 100 MHz	–	–	–	–	9	–	dB

Table III – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $T_A = 25°C, V^+ +6V, V^- = -6V$	LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM			MAXIMUM			UNITS
			−55	+25	+125	−55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}		–	–	–	5	5	5	mV
Input Offset Current	I_{IO}		–	–	–	9	5	7	μA
Input Bias Current	I_I		–	–	–	60	40	40	μA
Device Dissipation	P_D	Terminals 4 & 5 NC	16	16	14	50	45	45	mW
DYNAMIC									
Power Gain	G_P	f = 100 MHz	–	10	–	–	–	–	dB
Noise Figure	NF	f = 100 MHz	–	–	–	–	9	–	dB
AGC Range (Max. Voltage gain to Complete Cutoff)	AGC		–	-60	–	–	–	–	dB

Table IV – Group C Electrical Characteristics Sampling Tests ($T_A = 25^oC$)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6V, V^- = -6V$	LIMITS MIN.	MAX.	UNITS
Device Dissipation	P_D		–	45	mW
Power Gain	G_P	f = 100 MHz	10	–	dB
Input Bias Current	I_I		–	40	μA
Input Offset Voltage	V_{IO}		–	5	mV
Input Offset Current	I_{IO}		–	5	μA

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPE CA3004

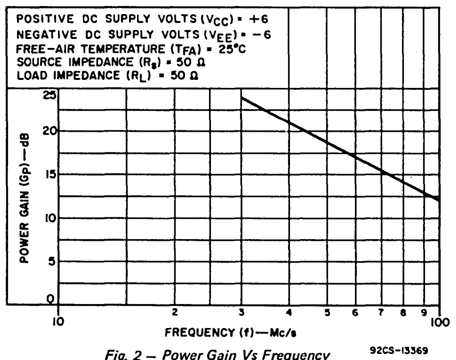


Fig. 2 – Power Gain Vs Frequency

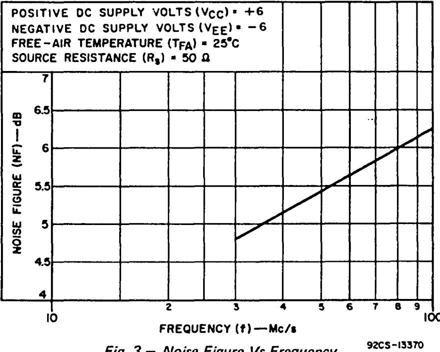


Fig. 3 – Noise Figure Vs Frequency

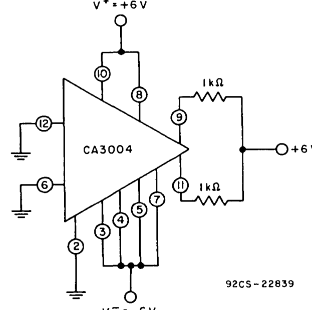


Fig. 4 – Burn-In and Operating Life Test Circuit

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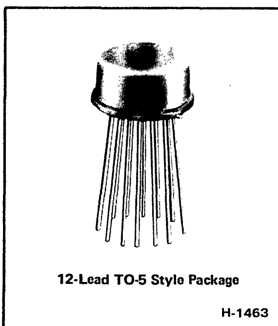


12-Lead TO-5 Style Package

H-1463

High-Reliability RF Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Input offset voltage (V_{IO}) = 1 mV (max.)**
- **AGC range = 60 dB (min.) at 1.75 MHz**
- **Cascode power gain = 20 dB (typ.) at 100 MHz**
- **Operation from dc to 100 MHz**
- **Sharp limiting characteristics**
- **Balanced input and output**
- **Uncommitted bases and collectors**

V⁺=6 V
T_A = +125°C
1K 1K
CA3006
V⁻=6V
92CS-15381R2

Burn-in and operating life test circuit.

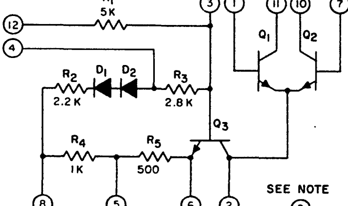
RCA-CA3006 "Slash" (/) Series types are high-reliability linear integrated circuits intended for a wide variety of applications in aerospace, military, and critical industrial equipment operating at frequencies up to 100 MHz. They are electrically and mechanically identical with the standard type CA3006 described in Data Bulletin File No.125 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

Applications:

- **Wide and narrow band amplifiers**
- **Detectors**
- **Mixers**
- **Limiters**
- **Modulators**
- **Cascode Amplifiers**

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3006 Slash (/) Series types are supplied in the 12-lead TO-5 style package ("T" suffix), and in chip form ("H" suffix).



NOTE: Connect Terminal No.9 to most positive dc supply voltage used for circuit.

Fig.1 – Schematic diagram of CA3006.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C:

DEVICE DISSIPATION	300	mW
SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±3.5	V
COMMON-MODE INPUT-SIGNAL VOLTAGE	−2.5 to +3.5	V

AMBIENT TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+300	°C

Maximum Voltage Ratings at T_A = 25°C

This chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 9 with respect to terminal 5 is 0 to +18 volts.

9	10	11	12	1	2	3	4	5	6	7	8	TERM-INAL No.
	*	*	+18 0	*	*	+18 0	+18 0	+18 0	+18 0	*	+18 0	9
		*	*	*	+12 0	*	*	*	*	+12 −1	+18 0	10
			*	+12 −1	+12 0	*	*	*	*	*	+18 0	11
				*	*	+18 −18	+18 −18	*	*	*	+18 −5	12
					+1 −4	*	*	*	+10 −4	+4 −4	*	1
						+12 −1	*	*	+10 0	+4 −1	*	2
							*	*	+1 −4	*	+10 −5	3
								*	*	*	+10 −5	4
									*	*	*	5
										+4 −10	*	6
											*	7
											REF. SUB- STRATE	8

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Maximum Current Ratings

TERM-INAL No.	I_{IN} mA	I_{OUT} mA
9	–	–
10	+20	+0.1
11	+20	+0.1
12	–	–
1	+2	+0.1
2	+20	+20
3	–	–
4	–	–
5	–	–
6	–	–
7	+2	+0.1
8	+0.1	+20

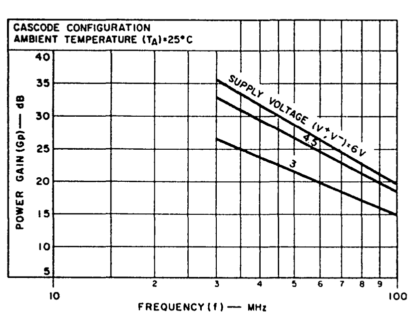


Fig.2 – Power gain vs. frequency, cascode configuration.

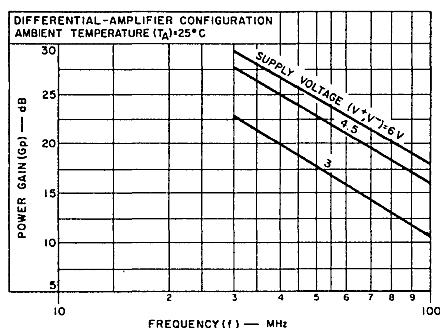


Fig.3 – Power gain vs. frequency, differential amplifier configuration.

Table I – Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V^+ = 6 V, V^- = 6 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS Min.	Max.	Max.Δ	UNITS
Input-Bias Current	I_{IB}	–	–	40	±4	μA
Quiescent Operating Current	I_{10} or I_{11}	Terminal 4: NC Terminal 5: NC	0.6	1.6	±0.2	mA
Device Dissipation	P_D	Terminal 4: NC Terminal 5: NC	16	45	±5.4	mW

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits. Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown on page 298.

ELECTRICAL CHARACTERISTICS, **Typical Values Intended Only For Design Guidance**

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS Terminals No.3,4,5, and 6 Not Connected Except Where Noted		LIMITS TYPE CA3006 Typ.	UNITS
STATIC					
Input Offset Voltage	V_{IO}			0.8	mV
Input Offset Current	I_{IO}			1.4	μA
Input Bias Current	I_{IB}			19	μA
Quiescent Operating Current	I_{10} or I_{11}	TERMINALS 4	TERMINALS 5		
		NC	NC	1	mA
		NC	V−	2.7	mA
		V−	NC	0.45	mA
		V−	V−	1.25	mA
Quiescent Operating Current Ratio	$\frac{I_{10}}{I_{11}}$			1.05	–
Device Dissipation	P_D			26	mW
DYNAMIC					
Power Gain	G_p	f = 100 MHz	Cascode Configuration	20	dB
			Differential-Ampl. Configuration	16	dB
Noise Figure	NF	f = 100 MHz	Cascode Configuration	7.8	dB
			Differential Ampl. Configuration	7.8	dB
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		101	dB
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz		–	dB

Table II – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = 6$ V, $V^- = 6$ V		LIMITS FOR INDICATED TEMPERATURE (°C) Minimum −55	Minimum +25	Minimum +125	Maximum −55	Maximum +25	Maximum +125	UNITS
STATIC										
Input Offset Current	I_{IO}			–	–	–	–	2	–	μA
Input Bias Current	I_{IB}			–	–	–	60	40	30	μA
Quiescent Operating Current	I_{10} I_{11}	Terminal 4 NC	Terminal 5 NC	0.6	0.6	0.5	1.7	1.6	1.4	mA
Device Dissipation	P_D	Terminal 4 NC	Terminal 5 NC	–	16	–	–	45	–	mW
DYNAMIC										
Power Gain	G_P	f = 100 MHz	Diff. Amplifier	–	14	–	–	–	–	dB
Noise Figure	NF	f = 100 MHz	Configuration	–	–	–	–	9	–	dB

Table III – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = 6$ V, $V^- = 6$ V		Limits for Indicated Temp. (°C) Minimum −55	Minimum +25	Minimum +125	Maximum −55	Maximum +25	Maximum +125	UNITS
STATIC										
Input Offset Voltage	V_{IO}	–		–	–	–	2	1	1.5	mV
Input Offset Current	I_{IO}	–		–	–	–	4	2	1	μA
Input Bias Current	I_{IB}	–		–	–	–	60	40	30	μA
Quiescent Operating Current	I_{10} I_{11}	Terminal 4	Terminal 5							
		NC	NC	0.6	0.6	0.5	1.7	1.6	1 4	mA
		NC	V^-	1.6	1.6	1.4	4.5	4.4	4	mA
		V^-	NC	0.25	0.25	0.25	0.8	0.75	0.85	mA
		V^-	V^-	0.7	0.8	0.75	2.3	2.4	2.2	mA
Device Dissipation	P_D	Terminal 4	Terminal 5							
		NC	NC	16	16	14	50	45	45	mW
		NC	V^-	45	45	40	125	120	110	mW
		V^-	NC	10	10	9	30	30	30	mW
		V^-	V^-	20	25	20	70	70	70	mW
DYNAMIC										
Power Gain	G_p	f = 100 MHz	Cascode Configuration	–	16	–	–	–	–	dB
			Differential Amplifier Configuration	–	14	–	–	–	–	dB
Noise Figure	NF	f = 100 MHz	Cascode Configuration	–	–	–	–	9	–	dB
			Differential Amplifier Configuration	–	–	–	–	9	–	dB
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz		–	−60	–	–	–	–	dB

Table IV – Group C Electrical Characteristics Sampling Tests ($T_A = 25$°C, $V^+ = 6$ V, $V^- = 6$ V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS Min.	Max.	Max.Δ	UNITS
Input Bias Current	I_{IB}	–	–	40	±4	μA
Quiescent Operating Current	I_{10} or I_{11}	Terminal 4: NC, 5: NC	0.6	1.6	±0.2	mA
Device Dissipation	P_D	Terminal 4: NC, 5: NC	16	45	±5.4	mW
Power Gain (Differential)	G_P	f = 100 MHz	14	–	±2	dB

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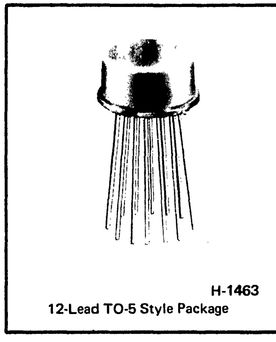
High-Reliability Slash(/) Series CA3015A/...



H-1463
12-Lead TO-5 Style Package

High-Reliability Operational Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

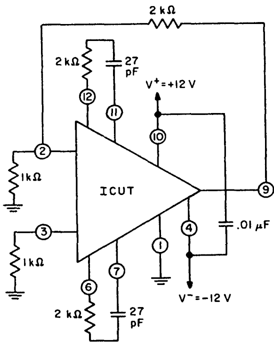
Features:

- Open-loop voltage gain .... 70 dB typ.
- Common-mode rejection ratio .... 103 dB typ.
- Input impedance .... 10 kΩ typ.
- Input offset voltage .... 1 mV typ.
- Input offset current .... 0.5 μA typ.
- Input bias current .... 4.7 μA typ.
- Static power drain at ± 12 V .... 175 mW typ.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Operating-Temperature Range .... -55°C to +125°C
Storage-Temperature Range .... -65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max. .... 265°C
Maximum Input-Signal Voltage .... -8 V, +1 V
MAXIMUM DEVICE DISSIPATION:

At Ambient Temperatures	Up to 70°C	700 mW
	Above 70°C	Derate at 6.7 mW/°C
At Case Temperatures	Up to 125°C	830 mW



Burn-in and operating life test circuit.

Applications:

- Narrow-band and band-pass amplifier
- Operational functions
- Feedback amplifier
- DC and video amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo driver
- Scaling adder
- Balanced modulator-driver

RCA-CA3015A "Slash" (/) Series type is a high-reliability linear integrated circuit operational amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3015A described in Data Bulletin File No. 310 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3015A Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Maximum Voltage Ratings at $T_A = 25°C$

The following chart gives the range of voltages wnich can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 12 with respect to terminal 10 is 0 to -15 volts.

TERMINAL No.	12	1	2	3	4▲	5	6	7	8	9	10	11
12		*	+15 -1	*	*	*	+5 -5	*	*	*	0 -15	+1 -15
1			*	*	+20 -5	*	*	*	*	*	*	*
2				+5 -5	+18 -5 Note 2	*	*	*	*	*	*	*
3					+18 -5 Note 2	*	+1 -15	*	*	*	*	*
4▲						0 -30 Note 3	*	*	0 -30	0 -30	0 -32	*
5							*	*	*	*	0 -30	*
6								+1 -15	*	*	0 -20	*
7									+20 -5	*	0 -20	*
8										+1 -5	0 -30	*
9											0 -32	*
10												+20 0
11												

Maximum Current Ratings

TERMINAL No.	I_{IN} mA	I_{OUT} mA
12	1	1
1	–	–
2	1	0.1
3	1	0.1
4▲	–	–
5	–	–
6	1	1
7	3	3
8	3	3
9	30	30
10	–	–
11	3	3

▲ CA3015A Case is internally connected to the substrate (Terminal Lead #4), DO NOT GROUND.

Note 1: For normal circuit operation, external voltages should not be applied to terminals 5,6,8, and 12.

Note 2: This rating applies only to the more positive terminal of terminals 2 or 3.

Note 3: Carefully observe maximum dissipation ratings.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

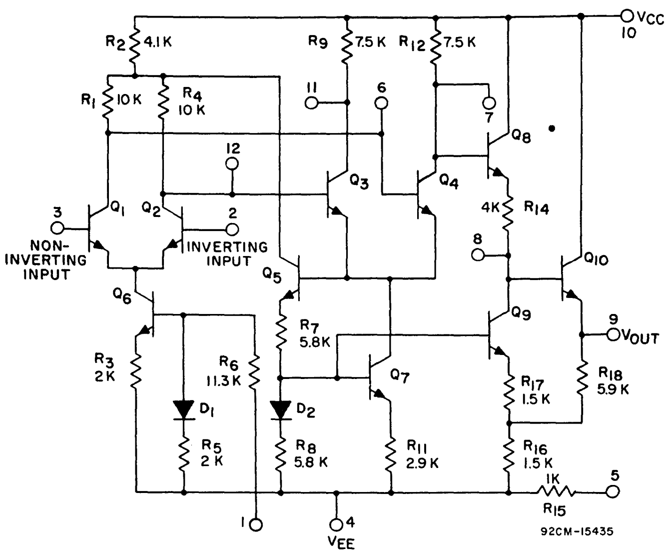


Fig. 1 — Schematic diagram.

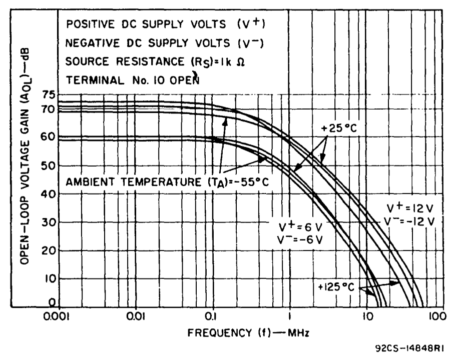


Fig. 2 — Open loop voltage gain vs. frequency

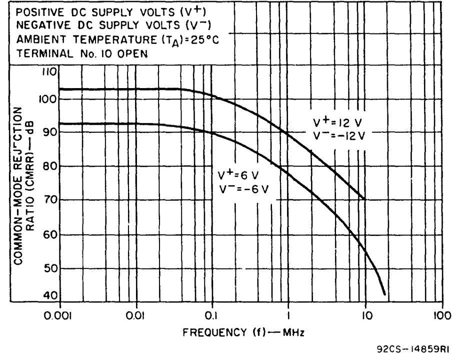
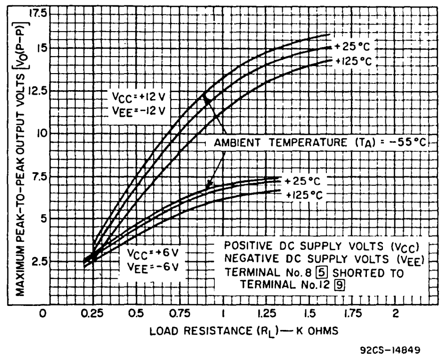


Fig. 3 — Common-mode rejection ratio vs. frequency

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V^+ = +12 V, V^- = −12 V TERMINAL NO. 5 NOT CONNECTED UNLESS OTHERWISE SPECIFIED	CA3015A TYP.	UNITS
STATIC CHARACTERISTICS:				
Input Offset Voltage	V_{IO}		1	mV
Input Offset Current	I_{IO}		0.5	μA
Input Bias Current	I_I		4.7	μA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$		0.096	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$		0.156	
Device Dissipation	P_T		175	mV
		Terminal 8 shorted to Terminal 12	500	
DYNAMIC CHARACTERISTICS:				
Open-Loop Differential Voltage Gain	A_{OL}		70	dB
Open-Loop Bandwidth at -3 dB Point	BW_{OL}		320	kHz
Slew Rate	SR	R_S = 1 kΩ	7	V/μs
Common-Mode Rejection Ratio	CMRR		103	dB
Maximum Output-Voltage Swing	$V_{O(P-P)}$		14	V_{P-P}
Input Impedance	Z_{IN}		10	kΩ
Output Impedance	Z_{OUT}		85	Ω
Common-Mode Input-Voltage Range	V_{CMR}		+0.65 -8	V
Noise Figure	NF	R_S = 1 kΩ	11	dB



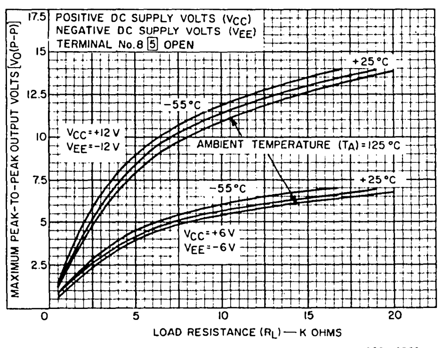


Fig. 4 — Maximum peak-to-peak output voltage vs. load resistance.

Table I

Pre Burn-In and Post Burn-In Electrical Tests, and Delta Limits*

ELECTRICAL CHARACTERISTICS, at T_A = V^+ = +12V, V^- = -12V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max.Δ	
Input Offset Voltage	V_{IO}		–	2	±1	mV
Input Offset Current	I_{IO}		–	1.6	±1	μA
Input Bias Current	I_I		–	6	±1	μA
Device Dissipation	P_T		110	240	±25	mW
		5 shorted to 9	320	600	±50	mW

*Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown on page 302.

Table II

Final Electrical Tests

CHARACTERISTICS	SYMBOL	TEST CONDITIONS V^+ = +12V, V^- = -12 V	LIMITS FOR INDICATED TEMP. (°C)						UNITS
			Minimum			Maximum			
			-55	+25	+125	-55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	3	2	3	mV
Input Offset Current	I_{IO}	–	–	–	–	3	1.6	2	μA
Input Bias Current	I_I	–	–	–	–	14	6	8	μA
Device Dissipation	P_T		115	110	95	280	240	235	mW
		5 shorted to 9	330	320	–	700	600	–	mW
DYNAMIC									
Open-Loop Differential Voltage Gain	A_{OL}	f = 1 kHz	–	66	–	–	–	–	dB

Table III

Group C Electrical Sampling Tests

T_A = +25°C V^+ = +12 V V^- = -12V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	V_{IO}	–	–	2	mV
Input Offset Current	I_{IO}	–	–	1.6	μA
Input Bias Current	I_I	–	–	6	μA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	–	–	0.5	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	–	–	0.5	mV/V
Device Dissipation	P_T	–	110	240	mW
		Terminal 5 shorted to 9	320	600	mW
Open-Loop Differential Voltage Gain	A_{OL}	f = 1 kHz	66	–	dB
Common-Mode Rejection Ratio	CMR	f = 1 kHz	80	–	dB

Table IV

Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions $V^+ = +12$ V, $V^- = -12$ V	Limits for Indicated Temperature (°C) Minimum -55	Minimum +25	Minimum +125	Maximum -55	Maximum +25	Maximum +125	Units
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	3	2	3	mV
Input Offset Current	I_{IO}	–	–	–	–	3	1.6	2	μA
Input Bias Current	I_I	–	–	–	–	14	6	8	μA
Input Offset Voltage Sensitivity Positive	$\frac{\Delta V_{IO}}{\Delta V^+}$	–	–	–	–	–	0.5	–	mV/V
Negative	$\frac{\Delta V_{IO}}{\Delta V^-}$	–	–	–	–	–	0.5	–	mV/V
Device Dissipation	P_T	–	115	110	95	280	240	235	mW
		5 shorted to 9	330	320	–	700	600	–	mW
DYNAMIC All tests are at 1 kHz except BW_{OL}									
Open-Loop Differential Voltage Gain	A_{OL}	–	–	66	–	–	–	–	dB
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	–	–	200	–	–	–	–	kHz
Common-Mode Rejection Ratio	CMR	–	–	80	–	–	–	–	dB
Maximum Output-Voltage Swing	$V_O(P\text{-}P)$	–	–	12	–	–	–	–	$V_{P\text{-}P}$
Input Impedance	Z_{IN}	–	–	7.5	–	–	–	–	kΩ
Output Impedance	Z_{OUT}	–	–	–	–	–	120	–	Ω
Common-Mode Input-Voltage Range	V_{CMR}	–	–	+0.35 to -8	–	–	–	–	V
Noise Figure	NF	$R_S = 1$ K	–	–	–	–	16	–	dB

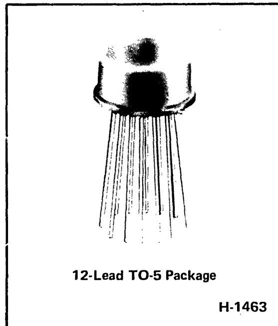
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3018A/ . . .



12-Lead TO-5 Package

H-1463

High-Reliability General-Purpose Transistor Array

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- Matched monolithic general-purpose transistors
- H_{FE} matched ± 10%
- V_{BE} matched ± 2 mV
- Operation from DC to 120 MHz
- Wide operating current range
- CA3018A performance characteristics controlled from 10 μA to 10 mA
- Low noise figure — — 3.2 dB typical at 1 kHz

RCA-CA3018A "Slash" (/) Series types are high-reliability linear integrated circuits intended for a wide variety of applications in aerospace, military, and critical industrial equipment. It consists of four general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the four transistors are connected in the Darlington configuration, and the substrate is connected to a separate terminal for maximum flexibility. The CA3018A is electrically and mechanically identical with the standard type CA3018A described in Data Bulletin File No. 338 but is specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic device in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3018A Slash (/) Series types are supplied in the 12-lead TO-5 style package ("T" suffix), and in chip form ("H" suffix).

Applications:

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers

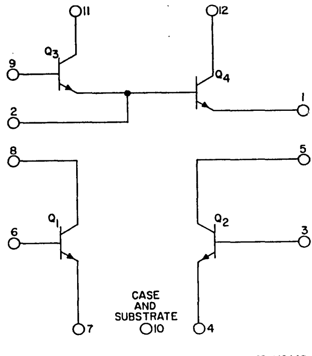


Fig. 1 – Schematic diagram for CA3018A.

MAXIMUM RATINGS, *Absolute Maximum Values at $T_A = 25^{\circ}C$*

DEVICE DISSIPATION:
- Any one transistor .... 300 mW
- Total package .... 450 mW
- $T_A > 85^{\circ}C$ .... derate linearly at 5 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating .... −55 to + 125°C
- Storage .... −65 to + 150°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	30	V
Collector-to-Substrate Voltage, V_{CIO}*	40	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +300 °C

* The collector of each transistor of the CA3018A/ is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

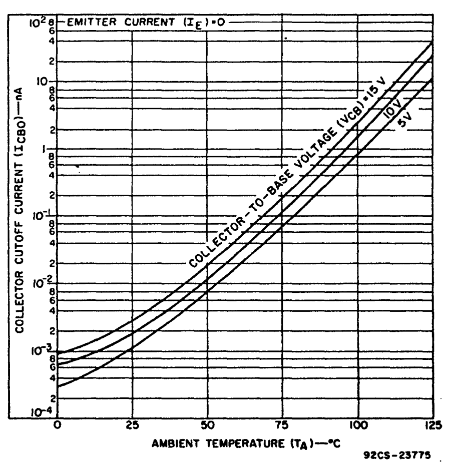
ELECTRICAL CHARACTERISTICS (For Each Transistor) Intended For Design Guidance

CHARACTERISTICS AT $T_A = 25^{\circ}C$	SYMBOL	SPECIAL TEST CONDITIONS	CA3018A LIMITS Typ.	UNITS
STATIC CHARACTERISTICS				
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	0.002	nA
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	See Curve	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	24	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$	60	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ μA, $I_C = 0$	7	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ μA, $I_{CI} = 0$	60	V
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1$ mA, $I_C = 10$ mA	0.23	V
Static Forward Current Transfer Ratio	h_{FE}	$V_{CE} = 3$ V, $I_C = 10$ mA $I_C = 1$ mA $I_C = 10$ μA	100 100 54	– – –
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		$V_{CE} = 3$ V, $I_{C1} = I_{C2} = 1$ mA	0.97	–
Static Forward Current Transfer Ratio Darlington Pair (Q_3 and Q_4)	h_{FED}	$V_{CE} = 3$ V, $I_C = 1$ mA $I_C = 100$ μA	5400 2800	–
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3$ V, $I_E = 1$ mA $I_E = 10$ mA	0.715 0.800	V
Input Offset Voltage	$\|V_{BE1} - V_{BE2}\|$	$V_{CE} = 3$ V, $I_E = 1$ mA	0.48	mV
Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	$\frac{\|\Delta V_{BE}\|}{\Delta T}$	$V_{CE} = 3$ V, $I_E = 1$ mA	-1.9	mV/°C
Base (Q_3)-to Emitter (Q_4) Voltage Darlington Pair	V_{BED} (V_{9-1})	$V_{CE} = 3$ V, $I_E = 10$ mA $I_E = 1$ mA	1.46 1.32	V
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3, Q_4	$\frac{\|\Delta V_{BED}\|}{\Delta T}$	$V_{CE} = 3$ V, $I_E = 1$ mA	4.4	mV/°C
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\|V_{BE1} - V_{BE2}\|}{\Delta T}$	$V_{CC} = +6$ V, $V^- = 6$ V $I_{C1} = I_{C2} = 1$ mA	10	mV/°C

TYPICAL CHARACTERISTICS, (Cont'd)

DYNAMIC CHARACTERISTICS	SYMBOL	SPECIAL TEST CONDITIONS	CA3018A TYP.	UNITS
Low Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source resistance = 1 KΩ	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:				
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	110	–
Short-Circuit Input Impedance	h_{ie}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	3.5	KΩ
Open-Circuit Output Impedance	h_{oe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	15.6	μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	1.8×10^{-4}	–
Admittance Characteristics:				
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	31-j1.5	mmho
Input Admittance	Y_{ie}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	0.3 + j0.04	mmho
Output Admittance	Y_{oe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	0.001 + j0.03	mmho
Reverse Transfer Admittance	Y_{re}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	See Curve	mmho
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	500	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	0.6	pF
Collector-to-Base Capacitance	C_{CI}	V_{CB} = 3 V, I_C = 0	0.58	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 3 V, I_C = 0	2.8	pF

STATIC CHARACTERISTICS



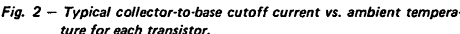


Fig. 2 – Typical collector-to-base cutoff current vs. ambient temperature for each transistor.

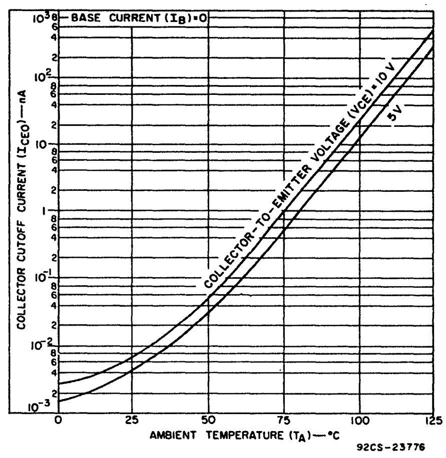


Fig. 3 – Typical collector-to-emitter cutoff current vs. ambient temperature for each transistor.

TABLE I – PRE BURN-IN ELECTRICAL AND POST BURN-IN ELECTRICAL TESTS, AND DELTA LIMITS*
ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS Min.	LIMITS Max.	LIMITS Max.Δ	UNITS
Emitter-to-Base Breakdown Volts, Q_1, Q_2	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	5	–	±0.5	V
Collector Cutoff Current, Q_1, Q_2	I_{CEO}	$V_{CE} = 10\ V$, $I_B = 0$	–	0.5	±0.15	μA
Collector Cutoff Current, Q_3, Q_4	$I_{CEO(D)}$	$V_{CE} = 10\ V$, $I_B = 0$	–	5	±1	μA
Input Current Q_1, Q_2	I_{IN}	$I_C = 1\ mA$, $V_{CE} = 3\ V$	–	16.7	±2	μA
Input Current Darlington Pair, Q_3, Q_4	$I_{IN(D)}$	$I_C = 1\ mA$, $V_{CE} = 3\ V$	–	0.5	±0.1	μA
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	$I_E = 1\ mA$, $V_{CE} = 3\ V$	0.6	0.8	±0.1	V
Base-to-Emitter Voltage, Darlington Pair, Q_3, Q_4	$V_{BE(D)}$ ($V_{9\text{-}1}$)	$I_E = 1\ mA$, $V_{CE} = 3\ V$	1.1	1.5	±0.1	V

* Levels/1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level/3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 12.

TABLE II – FINAL ELECTRICAL TESTS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURE (°C)						UNITS
			Minimum			Maximum			
		STATIC	–55	+25	+125	–55	+25	+125	
Collector Cutoff Current, Q_1, Q_2, Q_3, Q_4	I_{CBO}	$V_{CB} = 10\ V$, $I_E = 0$	–	–	–	–	40	–	nA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$	–	30	–	–	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	–	5	–	–	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\ \mu A$, $I_{CI} = 0$	–	40	–	–	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\ mA$, $I_B = 0$	–	15	–	–	–	–	V
Collector Cutoff Current Q_1, Q_2	I_{CEO}	$V_{CE} = 10\ V$, $I_B = 0$	–	–	–	–	0.5	100	μA
Collector Cutoff Current Q_3, Q_4	$I_{CEO(D)}$	$V_{CE} = 10\ V$, $I_B = 0$	–	–	–	–	5	2000	μA
Static Forward Current Transfer Ratio, Q_1, Q_2	h_{FE}	$V_{CE} = 3\ V$, $I_C = 1\ mA$	29	60	70	–	–	–	–
		$V_{CE} = 3\ V$, $I_C = 10\ mA$	–	50	–	–	–	–	–
		$V_{CE} = 3\ V$, $I_C = 10\ \mu A$	–	30	–	–	–	–	–
Static Forward Current Transfer Ratio, Q_3, Q_4	$h_{FE(D)}$	$V_{CE} = 3\ V$, $I_C = 1\ mA$	1000	2000	2300	–	–	–	–
		$V_{CE} = 3\ V$, $I_C = 100\ \mu A$	–	1000	–	–	–	–	–
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	$V_{CE} = 3\ V$, $I_E = 1\ mA$	0.7	0.6	0.4	1	0.8	0.7	V
		$V_{CE} = 3\ V$, $I_E = 10\ mA$	–	–	–	–	0.9	–	V
Input Offset Voltage	$\lvert V_{BE1} - V_{BE2} \rvert$	$V_{CE} = 3\ V$, $I_E = 1\ mA$	–	–	–	–	2	–	mV
Base-to-Emitter Voltage, Q_3, Q_4	$V_{BE(D)}$	$V_{CE} = 3\ V$, $I_E = 1\ mA$	–	1.1	–	–	1.5	–	V
		$V_{CE} = 3\ V$, $I_E = 10\ mA$	–	–	–	–	1.6	–	V
Collector-to-Emitter Saturation Voltage Q_1, Q_2	V_{CES}	$I_B = 1\ mA$, $I_C = 10\ mA$	–	–	–	–	0.5	–	V

TABLE III – GROUP A ELECTRICAL SAMPLING INSPECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMP. (°C) MINIMUM			MAXIMUM			UNITS
			−55	+25	+125	−55	+25	+125	
STATIC									
Collector Cutoff Current, Q_1, Q_2, Q_3, Q_4	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	–	40	–	nA
Collector-to-Base Breakdown Voltage, Q_1, Q_2, Q_3, Q_4	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	30	–	–	–	–	V
Emitter-to-Base Breakdown Voltage, Q_1, Q_2, Q_3, Q_4	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	–	–	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{C1} = 0	–	40	–	–	–	–	V
Collector-to-Emitter Breakdown Voltage, Q_1, Q_2, Q_3, Q_4	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	–	–	–	–	V
Collector Cutoff Current, Q_1, Q_2	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	–	0.5	100	μA
Collector Cutoff Current, Q_3, Q_4	$I_{CEO(D)}$	V_{CE} = 10 V, I_B = 0	–	–	–	–	5	2000	μA
Static Forward Current Transfer Ratio, Q_1, Q_2	h_{FE}	I_C = 1 mA, V_{CE} = 3 V	29	60	70	–	–	–	–
Static Forward Current Transistor Ratio, Darlington Pair	$h_{FE(D)}$	I_C = 1 mA, V_{CE} = 3 V	1000	2000	2300	–	–	–	–
Base-to-Emitter Voltage Voltage, Q_1, Q_2	V_{BE}	I_E = 1 mA, V_{CE} = 3 V	0.7	0.6	0.4	1.0	0.8	0.7	V
Static Forward Current Transfer Ratio, Q_1, Q_2	h_{FE}	I_C = 10 mA, V_{CE} = 3 V I_C = 10 μA, V_{CE} = 3 V	– –	50 30	– –	– –	– –	– –	– –
Static Forward Current Transfer Ratio, Darlington Pair	$h_{FE(D)}$	I_C = 100 μA, V_{CE} = 3 V	–	1000	–	–	–	–	–
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	I_E = 10 mA, V_{CE} = 3 V	–	–	–	–	0.9	–	V
Input Offset Voltage	$\|V_{BE1} - V_{BE2}\|$	I_E = 1 mA, V_{CE} = 3 V	–	–	–	–	2	–	mV
Base-to-Emitter Voltage, Darlington Pair	$V_{BE(D)}$ [V_{9-1}]	I_E = 10 mA, V_{CE} = 3 V I_E = 1 mA, V_{CE} = 3 V	– –	– 1.1	– –	– –	1.6 1.5	– –	V V
Magnitude of Static Beta Ratio, Q_1, Q_2		$I_{C1} = I_{C2}$ = 1 mA V_{CE} = 3 V	–	0.9	–	–	1.11	–	–
Collector-to-Emitter Saturation Voltage, Q_1, Q_2	V_{CES}	I_B = 1 mA, I_C = 10 mA	–	–	–	–	0.5	–	V
Static Forward Current Ratio, Darlington Pair	$h_{FE(D)}$	I_C = 10 mA, V_{CE} = 3 V	–	3000	–	–	–	–	–
DYNAMIC									
Gain Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA f = 100 MHz	–	300	–	–	–	–	MHz

TABLE IV – GROUP C ELECTRICAL CHARACTERISTICS SAMPLING TESTS (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Emitter-to-Base Breakdown Volts, Q_1, Q_2, Q_3, Q_4	$V_{(BR)EBO}$	I_E = 10 mA, I_C = 0	5	–	V
Collector-to-Emitter Breakdown Volts, Q_1, Q_2, Q_3, Q_4	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	–	V
Collector Cutoff Current, Q_1, Q_2	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.5	μA
Collector Cutoff Current, Q_3, Q_4	$I_{CEO(D)}$	V_{CE} = 10 V, I_B = 0	–	5	μA
Input Current, Q_1, Q_2	I_{IN}	I_C = 1 mA, V_{CE} = 3 V	–	25	μA
Input Current, Darlington Pair, Q_3, Q_4	$I_{IN(D)}$	I_C = 1 mA, V_{CE} = 3 V	–	1	μA
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	I_E = 1 mA, V_{CE} = 3 V	0.6	0.8	V
Base-to-Emitter Voltage, Darlington Pair, Q_3, Q_4	$V_{BE(D)}$	I_E = 1 mA, V_{CE} = 3 V	1.1	1.5	V

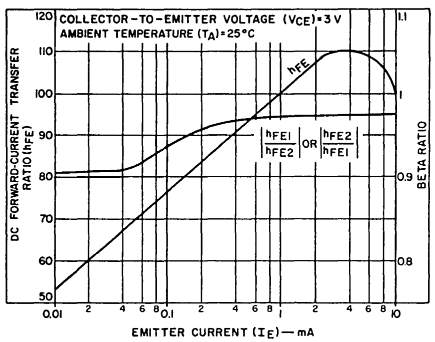


Fig. 4 – Typical static forward-current transfer ratio and beta ratio for transistors Q, and Q_2 vs. emitter current.

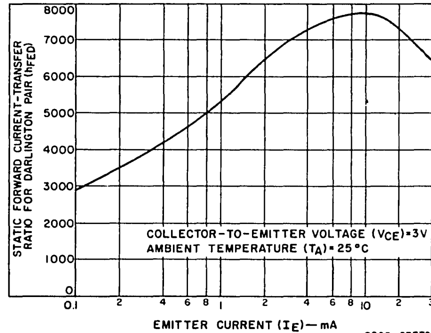


Fig. 5 – Typical static forward-current transfer ratio for Darlington-connected transistors Q_3 and Q_4 vs. emitter current.

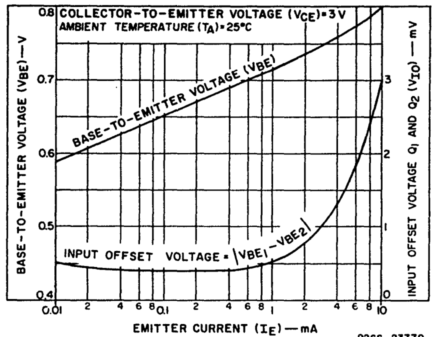


Fig. 6 – Typical static base-to-emitter voltage characteristic and input offset voltage for Q_1 and Q_2 vs. emitter current.

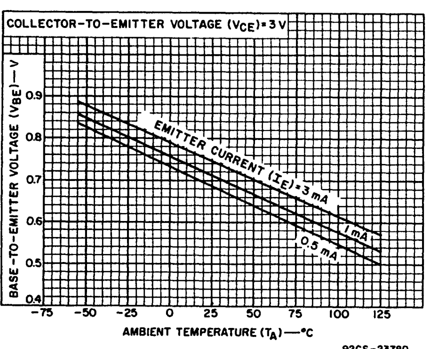


Fig. 7 – Typical base-to-emitter voltage characteristics for each transistor vs. ambient temperature.

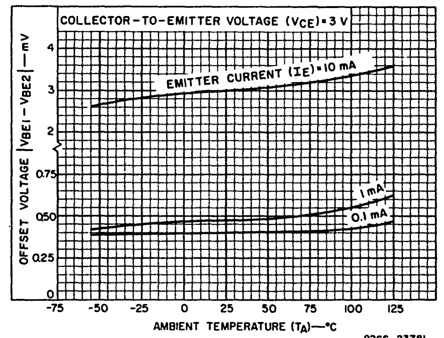


Fig. 8 – Typical offset voltage characteristics vs. ambient temperature.

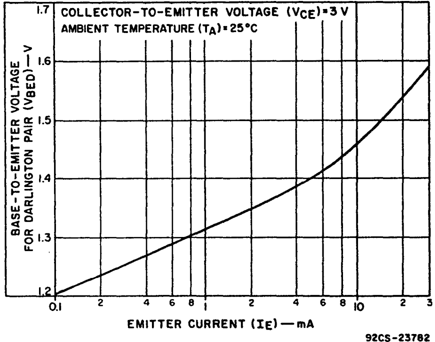


Fig. 9 – Typical static input voltage characteristics for Darlington pair (Q_3 and Q_4) vs. emitter current.

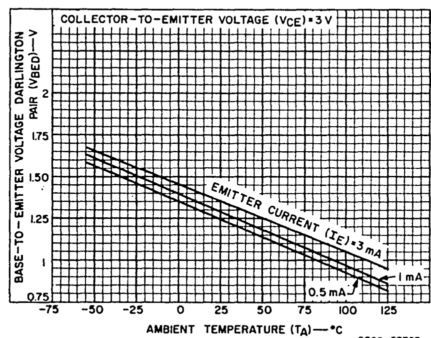


Fig. 10 – Typical static input voltage characteristics for Darlington pair (Q_3 and Q_4) vs. ambient temperature.

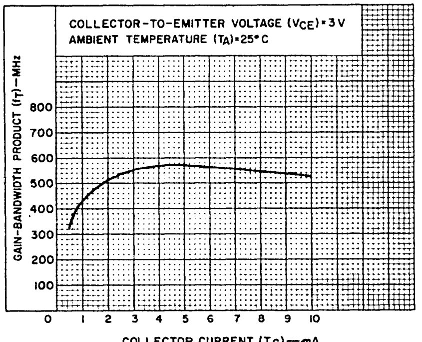


Fig. 11 – Typical gain-bandwidth product (f_T) vs. collector current.

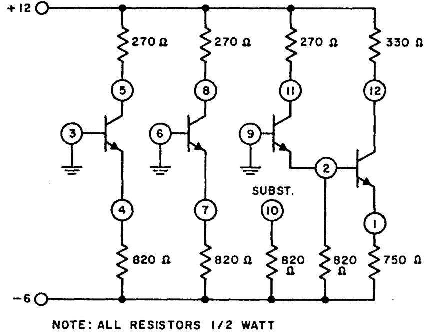


Fig. 12 – Burn-in and operating life test circuit.

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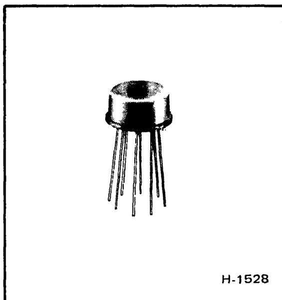
High-Reliability Slash(/) Series

CA3019/...



H-1528

10-LEAD TO-5 STYLE PACKAGE I

High-Reliability Diode Array Diode Quad and Two Individual Diodes

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Excellent diode match**
- **Low leakage current**
- **Low pedestal voltage when gating**

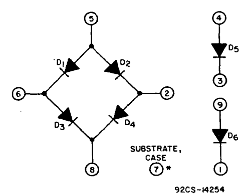
RCA-CA3019 "Slash" (/) Series type is a high-reliability linear integrated circuit Diode Array consisting of a diode quad and two individual diodes. It is intended for telemetry, data processing, instrumentation and communications applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3019 described in Data Bulletin File No. 236 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence, are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3019 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications:

- **Modulator**
- **Mixer**
- **Balanced modulator**
- **Analog switch**
- **Diode gate for chopper-modulator applications**
- **See companion application note ICAN-52911 application of the RCA CA3019 IC Diode Array**



* Connect to most negative circuit potential.

Fig. 1 — Schematic diagram.

*Table I – Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	MAX.	MAX. Δ	UNITS
Each Diode: DC Forward Voltage Drop	V_F	I_F = 1 mA	–	0.78	±0.010	V
		I_F = 0.2 mA	–	0.72	±0.010	V
		I_F = 20 mA	–	0.95	±0.010	V

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 5.

TYPICAL CHARACTERISTICS

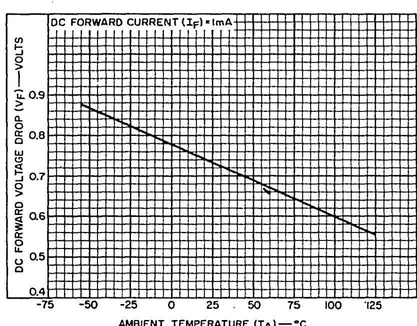


Fig. 2 – DC Forward Voltage Drop (any Diode) vs Temperature for CA3019.

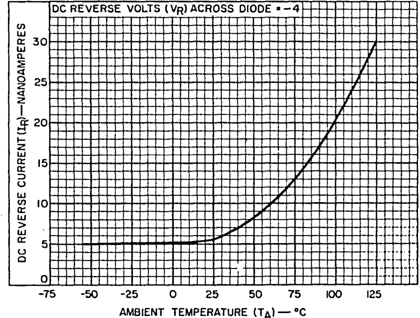


Fig. 3 – Reverse (Leakage) Current (any Diode) vs Temperature for CA3019.

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

Any one diode unit	20 max.	mW
Total for device	120 max.	mW

TEMPERATURE RANGE:

Storage	−65 to +150	°C
Operating	−55 to +125	°C

LEAD TEMPERATURE *(During Soldering)*:

At distance 1/16″ ±1/32″ (1.59 mm ±0.79 mm) from case for 10 s max. .... 265°C

Absolute-Maximum Voltage Limits at $T_A = 25^oC$

TERMINAL	VOLTAGE LIMITS NEGATIVE	POSITIVE	CONDITIONS TERMINAL	VOLTAGE
1	-3	+12	7	-6
2	-3	+12	7	-6
3	-3	+12	7	-6
4	-3	+12	7	-6
5	-3	+12	7	-6
6	-3	+12	7	-6
7	-18	0	1, 2, 3, 6, 8	0
8	-3	+12	7	-6
9	-3	+12	7	-6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

ELECTRICAL CHARACTERISTICS, at an Ambient Temperature, T_A, of 25°C
CHARACTERISTICS APPLY FOR EACH DIODE UNIT, UNLESS OTHERWISE SPECIFIED.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3019	
			Typ.	Units
DC Forward Voltage Drop	V_F	DC Forward Current (I_F) = 1 mA	0.73	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	DC Reverse Current (I_R) = -10 μA	6	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	DC Reverse Current (I_R) = -10 μA	80	V
DC Reverse (Leakage) Current	I_R	DC Reverse Voltage (V_R) = -4 V	0.0055	μA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	DC Reverse Voltage (V_R) = -4 V	0.010	μA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\|V_{F1} - V_{F2}\|$	DC Forward Current (I_F) = 1 mA	1	mV
Single Diode Capacitance	C_D	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = -2 V	1.8	pF
Diode Quad-to-Substrate Capacitance	C_{DQ-I}	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = -2 V		
		Terminal 2 or 6 to Terminal 7	4.4	pF
		Terminal 5 or 8 to Terminal 7	2.7	pF
Series Gate Switching Pedestal Voltage	V_S		10	mV

TYPICAL CHARACTERISTICS

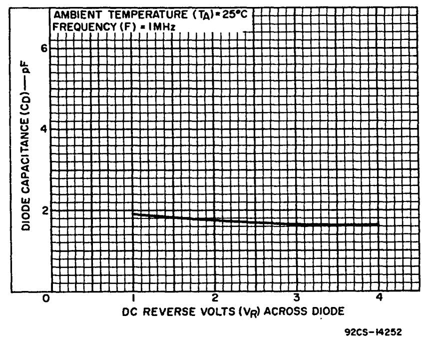


Fig. 4 — Diode capacitance (any diode) vs reverse voltage for CA3019.

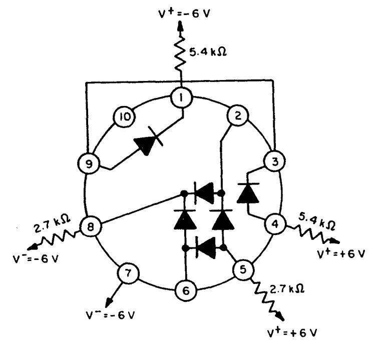


Fig. 5 — Burn-In and operating life test circuit

Table II – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Each Diode:									
DC Forward Voltage Drop	V_F	I_F = 0.2 mA	–	–	–	–	0.72	–	V
		I_F = 1 mA	0.76	–	0.41	0.97	0.79	0.60	V
		I_F = 20 mA	–	–	–	–	0.95	–	V
DC Reverse Leakage Current	I_R	V_R = −4 V	–	–	–	–	10	–	μA
DC Reverse Leakage Current To Substrate	I_R	V_R = −4 V	–	–	–	–	10	–	μA
Between Any Two Diodes: Diode Offset Voltage	$\|V_{F1} - V_{F2}\|$	I_F = 1 mA	–	–	–	–	5	–	mV
Isolation-to-Substrate Breakdown Voltage		−50 V through a 25 KΩ to terminal 7. Ground terminal 1 through 6, 8 and 9. Measure voltage at terminal 7	–	50	–	−25	−25	−25	V

Table III – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Each Diode:									
DC Forward Voltage Drop	V_F	I_F = 0.2 mA	–	–	–	–	0.72	–	V
		I_F = 1 mA	0.76	–	0.41	0.97	0.78	0.60	V
		I_F = 20 mA	–	–	–	–	0.95	–	V
DC Reverse Leakage Current	I_R	V_R = −4 V	–	–	–	–	10	–	μA
DC Reverse Leakage Current To Substrate	I_R	V_R = −4 V	–	–	–	–	10	–	μA
Between Any Two Diodes: Diode Offset Voltage	$\|V_{F1} = V_{F2}\|$	I_F = 1 mA	–	–	–	–	5	–	mV
Isolation-to-Substrate Breakdown Voltage		−50 V through a 25 KΩ to terminal 7. Ground terminal 1 through 6, 8 and 9. Measure voltage at terminal 7	–	50	–	−25	−25	−25	V

Table IV – Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Each Diode:					
DC Forward Voltage Drop	V_F	I_F = 0.2 mA	0.39	0.73	V
		I_F = 1 mA	0.49	0.79	V
		I_F = 20 mA	0.59	0.96	V
DC Reverse Leakage Current	I_R	V_R −4 V	–	10	μA
DC Reverse Leakage Current To Substrate	I_R	V_R = −4 V	–	10	μA
Between Any Two Diodes: Diode Offset Voltage	$V_{F1} - V_{F2}$	I_F = 1 mA	–	5	mV
Isolation-to-Substrate Breakdown Voltage		−50 V through a 25 KΩ to terminal 7.Ground terminal 1 through 6, 8 and 9. Measure voltage at terminal 7	–	−25	V

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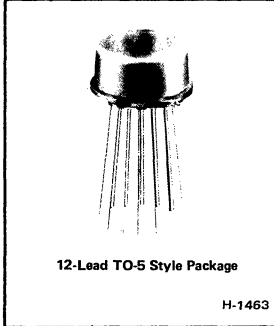
CA3020A/...



12-Lead TO-5 Style Package

H-1463

High-Reliability Multipurpose Wide-Band Power Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

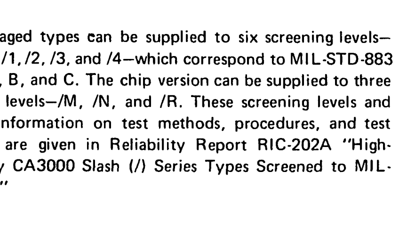
- High power output – class B amplifier. . . 1.0 W typ. at V^{+} = +12 V
- Wide frequency range. . . Up to 8 MHz with resistive loads
- High power gain. . .75 dB typ.
- Single power supply for class B operation with transformer. . . 3 to 12 V
- Built-in temperature-tracking voltage regulator provides stable operation over –55°C to +125°C temperature range

Applications:

- AF power amplifiers for portable and fixed sound and communications systems
- Servo-control amplifiers
- Wide-band linear mixers
- Video power amplifiers
- Transmission-line driver amplifiers (balanced and unbalanced)
- Fan-in and fan-out amplifiers for computer logic circuits
- Lamp-control amplifiers
- Motor-control amplifiers
- Power multivibrators
- Power switches
- Companion Application Note, ICAN-5766, "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers"

RCA-CA3020A "Slash" (/) Series types are high-reliability linear integrated circuits intended for a wide variety of applications in aerospace, military, and critical industrial equipment. They employ a highly versatile and stable direct-coupled circuit configuration featuring wide frequency range (dc to 8 MHz), high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020A extremely useful for a wide variety of applications, particularly as class B power amplifiers. It can provide a maximum power output of 1 watt from a 12-volt dc supply with a typical power gain of 75 db.

The CA3020A is electrically and mechanically identical with the standard type CA3020A described in Data Bulletin File No. 339 but is specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.



The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3020A Slash (/) Series types are supplied in the 12-lead TO-5 style package ("T" suffix), and in chip form ("H" suffix).

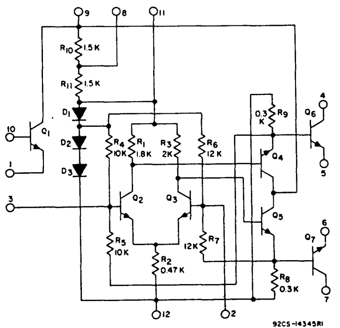


Fig.1 – Schematic diagram.

MAXIMUM RATINGS, *Absolute Maximum Values at $T_A = 25^oC$:*

	Without Heat Sink	With Heat Sink
DEVICE DISSIPATION:		
At $T_A = 25^oC$	1 W	At $T_C = 25^oC$ . . . 2 W
Above $T_A = 25^oC$	derate linearly 6.7 mW/^oC	At $T_C = 25^oC$ to $T_C = 55^oC$ . . . 2 W
		Above $T_C = 55^oC$ . . . derate linearly 16.7 mW/^oC

AMBIENT TEMPERATURE RANGE:

Operating . . . −55^oC to +125^oC

Storage . . . −65^oC to +150^oC

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. . . . +300 ^oC

Maximum Voltage Ratings at $T_A = 25^oC$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

Terminal No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	0 −12	+3 Note 1		+10 0
2			*	*	*	*	*	*	*	*	*	+2 −2
3				*	*	*	*	*	*	*	*	+2 −2
4					+25 0	*	*	*	*	*	*	+25 0
5						*	*	*	*	*	*	+3 Note 2
6							0 −25	*	*	*	*	+3 Note 2
7								*	*	*	*	+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+12 0
10											*	+10 0
11												*
12												Ref. Sub- Strate

Maximum Current Ratings

Terminal No.	I_{In} mA	I_{Out} mA
1	–	20
2	–	–
3	–	–
4	300	–
5	–	300
6	–	300
7	300	–
8	–	–
9	20	–
10	1	–
11	20	–
12	–	–

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

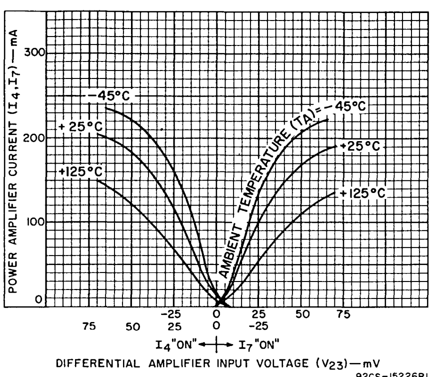


Fig.2 — Typical transfer characteristics with R_{10} shorted out.

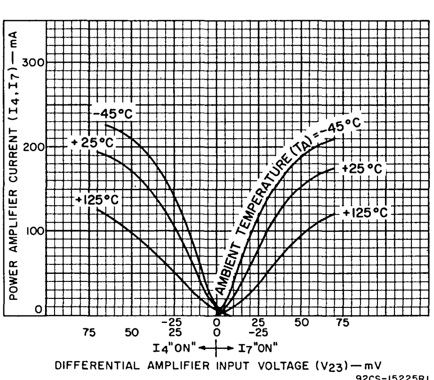


Fig.3 — Typical transfer characteristics with R_{10} in circuit.

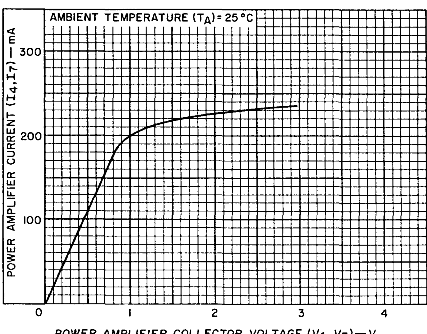


Fig.4 — "Minimum drive" typ. current-voltage saturation curve.

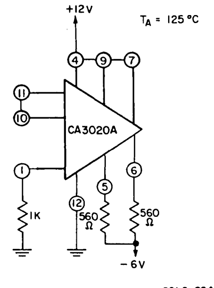


Fig.5 — Burn-in and operating life test circuit.

TABLE I – PRE BURN-IN ELECTRICAL AND POST BURN-IN ELECTRICAL TESTS, AND DELTA LIMITS*

Electrical Characteristics at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
		V^+_1▲	V^+_2▲	Min.	Max.	Max.Δ	
Peak Output Currents, Q_6 & Q_7	I_4PK, I_7PK	9 V	2 V	180	–	±15	mA
Cutoff Currents, Q_6 & Q_7	I_4 Cutoff I_7 Cutoff	9 V	2 V	–	1	±0.1	mA
Differential Amplifier Current Drain	I^+_1	9 V	9 V	6.3	12.5	±1.3	mA
Total Current Drain	$I^+_1 + I^+_2$	9 V	9 V	14	30	±3	mA

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 5.

▲ V^+_1 is the collector voltage applied to Q_1 through Q_5
V^+_2 is the collector voltage applied to Q_6 and Q_7

ELECTRICAL CHARACTERISTICS AT T_A = 25°C
Intended Only For Design Guidance

CHARACTERISTIC	SYMBOL	TEST CONDITIONS DC SUPPLY VOLTAGE		LIMITS CA3020A			UNITS
		V^+_1▲	V^+_2▲	MIN.	TYP.	MAX.	
Idle Currents, Q_6 & Q_7	I_4 IDLE, I_7 IDLE	9	2	–	5.5	–	mA
Differential Amplifier Current Drain	I^+_1	9	9	6.3	9.4	12.5	mA
Total Current Drain	$I^+_1 + I^+_2$	9	9	14	21.5	30	mA
Differential Amplifier Input Terminal Voltages	V_2, V_3	9	2	–	1.11	–	V
Regulator Terminal Voltage	V_{11}	9	2	–	2.35	–	V
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	6	–	30	75	–	
Bandwidth at –3 dB Point	BW	6	6	–	8	–	MHz
Maximum Power Output	$P_{O(MAX)}$	6	6	200	300[a]	–	mW
		9	9	400	550[a]	–	
		9	12	800	1000[b]	–	
Sensitivity for P_{OUT} = 800 mW	e_{IN}	9	12	–	50[b]	100	mV
Input Resistance – Terminal 3 to Ground	R_{IN3}	6	6	–	1000	–	Ω

[a] R_{CC} = 130 Ω
[b] R_{CC} = 200 Ω

TABLE II – FINAL ELECTRICAL TESTS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS FOR INDICATED TEMP.(°C) MINIMUM			MAXIMUM			UNITS
		V^+_1▲	V^+_2▲	–55	+25	+125	–55	+25	+125	
STATIC										
Peak Output Currents, Q_6 & Q_7	I_4PK, I_7PK	9 V	2 V	–	180	–	–	–	–	mA
Cutoff Currents, Q_6 & Q_7	I_4Cut, I_7Cut	9 V	2 V	–	–	–	–	1	–	mA
Differential Amplifier Current Drain	I^+_1	9 V	9 V	5.5	6.3	3.5	16.5	12.5	10	mA
DYNAMIC										
Total Current Drain	$I^+_1 + I^+_2$	9 V	9 V	6	14	8	51	30	25	mA
Sensitivity for P_{OUT} = 800 mW	e_{In}	9 V	12 V	–	–	–	–	100	–	mV

▲ V^+_1 is the collector voltage applied to Q_1 through Q_5
V^+_2 is the collector voltage applied to Q_6 and Q_7

TABLE III – GROUP A ELECTRICAL SAMPLING INSPECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS DC SUPPLY VOLTAGE		LIMITS FOR INDICATED TEMP.(°C)						UNITS
				MINIMUM			MAXIMUM			
		V^+_1▲	V^+_2▲	−55	+25	+125	−55	+25	+125	
STATIC										
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	–	–	–	25	–	–	–	–	V
	$V_{(BR)CEO}$	–	–	–	21	–	–	–	–	
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	–	–	–	10	–	–	–	–	V
Peak Output Currents, Q_6 & Q_7	I_{4PK} I_{7PK}	9 V	2 V	–	180	–	–	–	–	mA
Cutoff Currents, Q_6 & Q_7	$I_{4Cutoff}$ $I_{7Cutoff}$	9 V	2 V	–	–	–	–	1	–	mA
Differential Amplifier Current Drain	I^+_1	9 V	9 V	5.5	6.3	3.5	16.5	12.5	10	mA
Total Current Drain	$I^+_1 + I^+_2$	9 V	9 V	6	14	8	51	30	25	mA
Q_1 Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	10 V	–	–	–	–	–	100	–	µA
Emitter-to-Base	I_{EBO}	3 V	–	–	–	–	–	0.1	–	µA
Collector-to-Base	I_{CBO}	3 V	–	–	–	–	–	0.1	–	µA
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	6 V	–	–	30	–	–	–	–	
DYNAMIC										
Maximum Power Output, R_{CC} = 200 Ω	$P_{O(Max.)}$	9 V	12 V	–	800	–	–	–	–	mW
Sensitivity for P_{OUT} = 800 mW	e_{In}	9 V	12 V	–	–	–	–	100	–	mV

TABLE IV – GROUP C ELECTRICAL CHARACTERISTICS SAMPLING TESTS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
		V^+_1▲	V^+_2▲	MIN.	MAX.	
Peak Output Currents, Q_6 & Q_7	I_{4PK} I_{7PK}	9 V	2 V	180	–	mA
Cutoff Currents, Q_6 & Q_7	$I_{4Cutoff}$ $I_{7Cutoff}$	9 V	2 V	–	1	mA
Differential Amplifier Current Drain	I^+_1	9 V	9 V	6.3	12.5	mA
Total Current Drain	$I^+_1 + I^+_2$	9 V	9 V	14	30	mA
Sensitivity for P_{OUT} = 800 mW	e_{IN}	9 V	12 V	–	100	mV

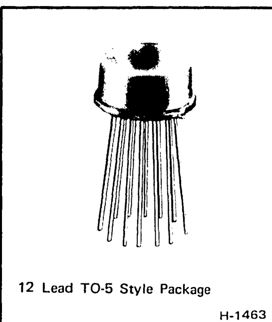
▲ V^+_1 is the collector voltage applied to Q_1 through Q_5
V^+_2 is the collector voltage applied to Q_6 and Q_7

Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CA3026/. . .



12 Lead TO-5 Style Package

H-1463

High-Reliability Transistor Array Dual Independent Differential Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Maximum input offset voltage — ±5 mV**
- **Full military temperature range capability — -55°C to +125°C**

RCA-CA3026 "Slash" (/) Series type is a high-reliability linear integrated circuit Dual Independent and Differential Amplifier is intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3026 described in Data Bulletin File No. 388 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3026 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications:

- **Dual sense amplifiers**
- **Dual Schmitt triggers**
- **Multifunction combinations — RF/Mixer/Oscillator; Converter/IF**
- **IF amplifiers (differential and/or cascode)**
- **Product detectors**
- **Doubly balanced modulators and demodulators**
- **Balanced quadrature detectors**
- **Cascade limiters**
- **Synchronous detectors**
- **Pairs of balanced mixers**
- **Synthesizer mixers**
- **Balanced (push-pull) cascode amplifiers**

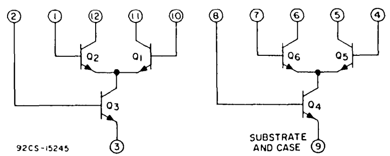


Fig. 1 — Schematic Diagram

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, *Absolute-Maximum Values, at $T_A = 25°C$*

POWER DISSIPATION,

Any one transistor	300	mW
Total package	600	mW
For $T_A > 55°C$	Derate at 5 mW/°C	

TEMPERATURE RANGE:

Operating	−55 to +125	°C
Storage	−65 to +200	°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1 and horizontal terminal 3 is +15 to −5 volts.

CA3026→ TERMINAL No. ↓	10	11	12	1	2	3	4	5	6	7	8	Note 1 9
10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*
11			*	*	*	+20 0	*	*	*	*	*	+20 0
12				+20 0	*	+20 0	*	*	*	*	*	+20 0
1					*	+15 -5	*	*	*	*	*	*
2						+1 -5	*	*	*	*	*	*
3							*	*	*	*	*	*
4								0 -20	*	+5 -5	*	+15 -5
5									*	*	*	+20 0
6										+20 0	*	+20 0
7											*	+15 -5
8												+1 -5
9												*
9												Ref Sub-strate

Maximum Current Ratings

CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
10	5	0.1
11	50	0.1
12	50	0.1
1	5	0.1
2	5	0.1
3	0.1	-50
4	5	0.1
5	50	0.1
6	50	0.1
7	5	0.1
8	5	0.1
9	0.1	50

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No. 9 is connected to the emitter of Q4, the reference substrate, and the case; therefore, should not be grounded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3026 LIMITS TYP.	UNITS
STATIC CHARACTERISTICS				
For Each Differential Amplifier				
Input Offset Voltage	V_{IO}	V_{CB} = 3 V, $I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	0.45	mV
Input Offset Current	I_{IO}		0.3	μA
Input Bias Current	I_I		10	μA
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$		0.98 to 1.02	-
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		1.1	μV/°C
For Each Transistor				
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V, I_C = 50 μA	0.630	V
		1 mA	0.715	
		3 mA	0.750	
		10 mA	0.800	
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-1.9	mV/°C
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	0.002	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	24	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	60	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	60	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	7	V
DYNAMIC CHARACTERISTICS				
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V, V_{EE} = -6 V, V_x = -3.3 V, f = 1 kHz	100	dB
AGC Range, One Stage	AGC		75	dB
Voltage Gain, Single Stage Double-Ended Output	A		32	dB
AGC Range, Two Stage	AGC		105	dB
Voltage Gain, Two Stage Double-Ended Output	A		60	dB

ELECTRICAL CHARACTERISTICS at T_A = 25°C – Cont'd.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3026 LIMITS TYP.	UNITS
DYNAMIC CHARACTERISTICS (Cont'd.)				
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)				
Forward Current-Transfer Ratio	h_{fe}	$f = 1$ kHz, $V_{CE} = 3$ V, $I_C = 1$ mA	110	-
Short-Circuit Input Impedance	h_{ie}		3.5	kΩ
Open-Circuit Output Impedance	h_{oe}		15.6	μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		1.8×10^{-4}	-
1/f Noise Figure (For Single Transistor)	NF	$f = 1$ kHz, $V_{CE} = 3$ V	3.25	dB
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 3$ V, $I_C = 3$ mA	550	MHz
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)				
Forward Transfer Admittance	y_{21}	$V_{CB} = 3$ V Each Collector $I_C \approx 1.25$ mA $f = 1$ MHz	-20+j0	mmho
Input Admittance	y_{11}		0.22+j0.1	mmho
Output Admittance	y_{22}		0.01+j0	mmho
Reverse Transfer Admittance	y_{12}		-0.003 +j0	mmho
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)				
Forward Transfer Admittance	y_{21}	$V_{CB} = 3$ V Total Stage $I_C \approx 2.5$ mA $f = 1$ MHz	68-j0	mmho
Input Admittance	y_{11}		0.55+j0	mmho
Output Admittance	y_{22}		0+j0.02	mmho
Reverse Transfer Admittance	y_{12}		0.004-j0.005	μmho
Noise Figure	NF	$f = 100$ MHz	8	dB

Table I. Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	LIMITS MAX. Δ	UNITS
Input Bias Current For Each Transistor Q1, Q2, Q5, and Q6	I_I	$V_{CE} = 3$V, $I_E = 2$mA	–	24	±6.0	μA
Base-to-Emitter Voltage For Each Transistor Q3 and Q4	V_{BE}	$V_{CE} = 3$V, $I_E = 1$mA	0.7	0.8	±0.1	V
Input Offset Voltage For Each Differential Amplifier	V_{IO}	$V_{CE} = 3$V, $I_E = 2$mA	–	5	±2	mV

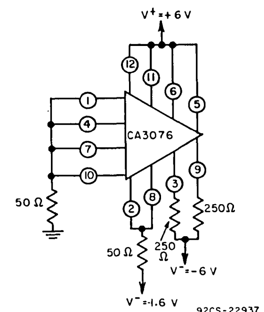
*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown on page 329.

Table II. Group A Electrical Sampling Inspection Tests and Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
For Each Transistor:									
Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	0.1	0.1	20	μA
Collector To-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E= 0	–	20	–	–	–	–	V
Emitter-To-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	–	5	–	–	–	–	V
Collector-To-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μ A, I_{C1} = 0	–	20	–	–	–	–	V
Collector-To-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	–	–	–	–	V
Input Bias Current For Transistors Q3 and Q4	I_I	V_{CE} = 3 V, I_E = 2mA	–	–	–	50	25	20	μA
Input Bias Current For Transistors Q1, Q2, Q5, and Q6	I_I	V_{CE} = 3 V, I_E = 2mA	–	–	–	50	25	20	μA
Base-To-Emitter Voltage For Transistors Q3 and Q4	V_{BE}	V_{CE} = 3 V, I_E = 1mA	0.7	0.7	0.4	1.05	0.8	0.75	V
For Each Differential Amplifier									
Input Offset Current	I_{IO}	V_{CE} = 3 V, I_E = 2mA	–	–	–	–	2	–	μA
Input Offset Voltage	V_{IO}	V_{CE} = 3 V, I_E = 2mA	–	–	–	–	5	–	mV

Table III. Group C Electical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
For Each Transistor: Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.2	μA
Input Bias Current For Transistors Q1, Q2, Q5, & Q6	I_I	V_{CE} = 3 V, I_E = 2mA	–	28	μA
Base-to-Emitter Voltage For Transistors Q3 and Q4	V_{BE}	V_{CE} = 3 V, I_E = 1mA	0.65	0.85	V
For Each Differential Amplifier: Input Offset Voltage	V_{IO}	V_{CE} = 3 V, I_E = 2mA	–	6	mV



Burn-in and operating life test circuit.

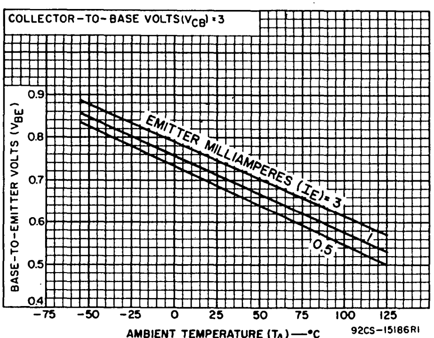


Fig. 2 — Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

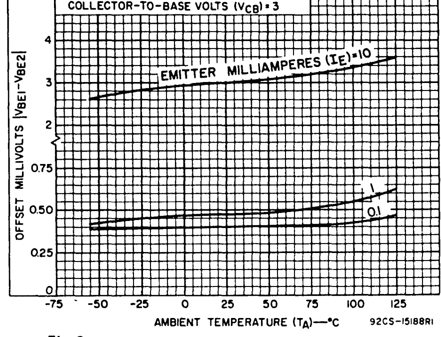


Fig. 3 — Offset voltage characteristic vs ambient temperature for differential pairs.

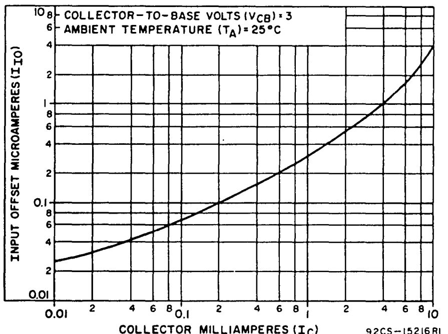


Fig. 4 — Input offset current for matched differential pairs vs collector current.

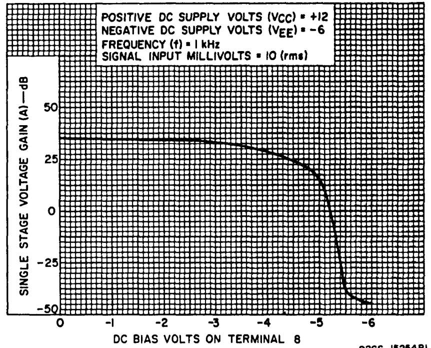


Fig. 5 — Single-stage voltage gain

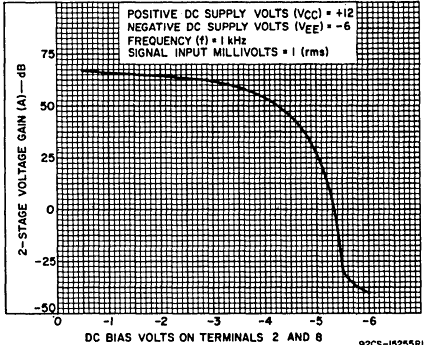


Fig. 6 — Two-stage voltage gain.

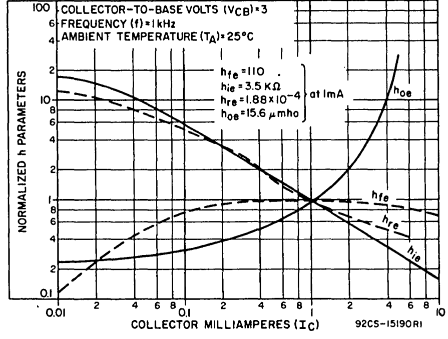


Fig. 7 — Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

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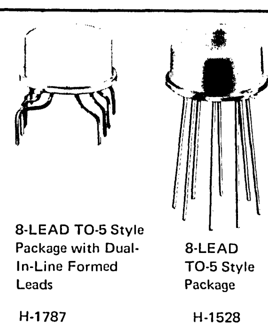
High-Reliability Slash(/) Series CA3028B/. . .



8-LEAD TO-5 Style Package with Dual-In-Line Formed Leads

H-1787

8-LEAD TO-5 Style Package

H-1528

High-Reliability Differential/Cascode Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Controlled for input offset voltage, input offset current, and input bias current**
- **Balanced differential amplifier configuration with controlled constant-current source to provide unexcelled versatility**
- **Single- and dual-ended operation**
- **Operation from DC to 120 MHz**
- **Balanced-AGC capability**
- **Wide operating-current range**

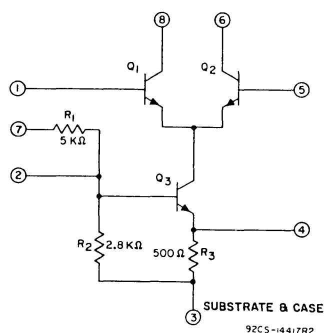


Fig. 1 – Schematic diagram.

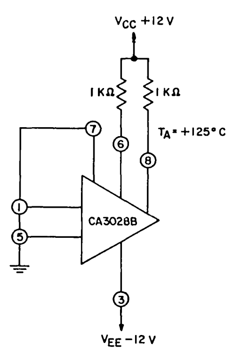


Fig. 2– Burn-in and operating life test circuit.

Applications:

- **RF and IF amplifiers (differential or cascode)**
- **DC, audio, and sense amplifiers**
- **Converter in the Commerical FM Band**
- **Oscillator** ■ **Mixer** ■ **Limiter**
- **See Application Note, ICAN 5337 "Application of the RCA CA3028 integrated circuit amplifier in the HF and VHF ranges."**

RCA-CA3028B "Slash" (/) Series type is a high-reliability linear integrated circuit Differential/Cascode Amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3028B described in Data Bulletin File No. 382 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3028B Slash (/) Series type is supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- At T_A up to 85°C . . . . 450 mW
- At T_A > 85°C derate linearly . . . . 5 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating . . . . −55 to +125°C
- Storage . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max. . . . . 265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15	0 to -15	0 to -15	+5 to -5	*	*	+20 to 0
2			+5 to -11	+5 to -1	+15 to 0	*	+15 to 0	*
3‡				+10 to 0	+15 to 0	+30● to 0	+15 to 0	+30● to 0
4					+15 to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

● Limit is +24V

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS TYP.	UNITS
STATIC CHARACTERISTICS					
		V^+	V^-		
Input Offset Voltage	V_{IO}	6 V 12 V	6 V 12 V	0.98 0.89	mV
Input Offset Current	I_{IO}	6 V 12 V	6 V 12 V	0.56 1.06	μA
Input Bias Current	I_I	6 V 12 V	6 V 12 V	16.6 36	μA
Quiescent Operating Current	I_6 or I_8	6 V 12 V	6 V 12 V	1.25 3.3	mA
Input Current (Terminal No. 7)	I_7	6 V 12 V	6 V 12 V	0.85 1.65	mA
Device Dissipation	P_T	6 V 12 V	6 V 12 V	36 175	mW

ELECTRICAL CHARACTERISTICS AT T_A = 25°C – Cont'd.

CHARACTERISTIC		SYMBOL	TEST CONDITIONS		LIMITS Typ.	UNITS
DYNAMIC CHARACTERISTICS						
Power Gain		G_P	f = 100 MHz, V_{CC} = +9V	Cascode	20	dB
				Diff.-Ampl.	17	
			f = 10.7 MHz, V_{CC} = +9V	Cascode	39	dB
				Diff.-Ampl.	32	
Noise Figure		NF	f = 100 MHz, V_{CC} = +9V	Cascode	7.2	dB
				Diff.-Ampl.	6.7	
Input Admittance		Y_{11}	f = 10.7 MHz, V_{CC} = +9V	Cascode	0.6 + j 1.6	mmho
				Diff.-Ampl.	0.5 + j 0.5	
Reverse Transfer Admittance		Y_{12}		Cascode	0.0003 - j0	mmho
				Diff.-Ampl.	0.01 - j0.0002	
Forward Transfer Admittance		Y_{21}		Cascode	99 - j18	mmho
				Diff.-Ampl.	-37 + j0.5	
Output Admittance		Y_{22}		Cascode	0. + j0.08	mmho
				Diff.-Ampl.	0.04 + j0.23	
Power Output (Untuned)		P_o	f = 10.7 MHz	Diff.-Ampl. 50 Ω Input-Output	5.7	μW
AGC Range (Max.Power Gain to Full Cutoff)		AGC	V_{CC} = +9V	Diff.-Ampl.	62	dB
Voltage Gain	at f = 10.7 MHz	A	f = 10.7 MHz, V_{CC} = +0V, R_L = 1 kΩ	Cascode	40	dB
				Diff.-Ampl.	30	
	Differential at f = 1 kHz		V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		38	dB
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		42.5	
Max. Peak-to-Peak Output Voltage at f = 1 kHz		V_o(P-P)	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		11.5	V_{P-P}
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		23	
Bandwidth at -3 dB point		BW	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		7.3	MHz
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		8	
Common-Mode Input-Voltage Range		V_{CMR}	V_{CC} = +6V, V_{EE} = -6V		(-3.2 - 4.5)	V
			V_{CC} = +12V, V_{EE} = -12V		(-7 - 9)	
Common-Mode Rejection Ratio		CMR	V_{CC} = +6V, V_{EE} = -6V		110	dB
			V_{CC} = +12V, V_{EE} = -12V		90	
Input Impedance at f = 1 kHz		Z_{IN}	V_{CC} = +6V, V_{EE} = -6V		5.5	kΩ
			V_{CC} = +12V, V_{EE} = -12V		3	
Peak-to-Peak Output Current		I_{P-P}	V_{CC} = +9V	f = 10.7 MHz, e_{in} = 400 mV, Diff.-Ampl.	4	mA
			V_{CC} = +12V		6	

TABLE I. GROUP A ELECTRICAL SAMPLING INSPECTION

Characteristics	Symbol	Test Conditions				Limits for Indicated Temp. (°C)						Units
						Minimum			Maximum			
		V_{CC}	V_{EE}	Freq. kHz	R_L kΩ	-55	+25	+125	-55	+25	+125	
Static												
Input Offset Voltage	V_{IO}	+6	-6			–	–	–	7	5	7.5	mV
		+12	-12			–	–	–	5	5	6	
Input Offset Current	I_{IO}	+6	-6			–	–	–	10	5	7.5	μA
		+12	-12			–	–	–	12	6	9	
Input Bias Current	I_I	+6	-6			–	–	–	70	40	35	μA
		+12	-12			–	–	–	130	80	55	
Quiescent Oper. Current	I_6 or I_8	+6	-6			0.5	1.0	0.5	2.0	1.5	2.0	mA
		+12	-12			2.0	2.5	1.5	4.5	4.0	4.0	
Input Current (terminal 7)	I_7	+6	-6			0.5	0.5	0.35	1.5	1.0	1.2	mA
		+12	-12			1.0	1.0	0.75	2.5	2.1	2.0	
Device Dissipation	P_T	+6	-6			20	24	20	45	42	45	mW
		+12	-12			120	120	105	230	220	210	
Dynamic												
Power Gain	G_P	V_{CC} = +9V, f = 10.7 MHz	Cascode			–	35	–	–	–	–	dB
			Diff-Ampl			–	28	–	–	–	–	
		V_{CC} = +9V, f = 100 MHz	Cascode			–	16	–	–	–	–	
			Diff-Ampl			–	14	–	–	–	–	
Noise Figure	NF	V_{CC} = +9V, f = 100 MHz	Cascode			–	–	–	–	9	–	dB
			Diff-Ampl			–	–	–	–	9	–	
Voltage Gain (Differential)	A	+6	-6	1	2	–	35	–	–	42	–	dB
		+12	-12		1.6	–	40	–	–	45	–	
Max. Peak-to-Peak Output Voltage	$V_{O(P-P)}$	+6	-6	1	2	–	7	–	–	–	–	$V_{(P-P)}$
		+12	-12		1.6	–	15	–	–	–	–	
Common-Mode Input-Voltage Range	V_{CMR}	+6	-6			–	-2.5 to +4	–	–	–	–	V
		+12	-12			–	-5 to +7	–	–	–	–	
Common-Mode Rejection Ratio	CMRR	+6	-6			–	60	–	–	–	–	dB
		+12	-12			–	60	–	–	–	–	

Table II. PRE BURN-IN ELECTRICAL AND POST BURN-IN ELECTRICAL TESTS, AND DELTA LIMITS*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max Δ	
Input Bias Current	I_I		-	80	± 8	µA
Input Offset Voltage	V_{IO}		-	5	± 2	mV
Quiescent Oper. Current	I_6 or I_8		2.5	4	± 0.4	mA
Input Current (term. 7)	I_7		1.0	2.1	± 0.2	mA
Device Dissipation	P_T		120	220	± 24	mW

*Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 2.

Table III. FINAL ELECTRICAL TESTS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS FOR INDICATED TEMPERATURE (°C)						UNITS
		V^+	V^-	Minimum			Maximum			
				-55	+25	+125	-55	+25	+125	
STATIC										
Input Offset Voltage	V_{IO}	+6	-6	-	-	-	-	5	-	mV
		+12	-12	-	-	-	5	5	6	
Input Offset Current	I_{IO}	+6	-6	-	-	-	-	5	-	µA
		+12	-12	-	-	-	12	6	9	
Input Bias Current	I_I	+6	-6	-	-	-	-	40	-	µA
		+12	-12	-	-	-	130	80	55	
Quiescent Oper. Current	I_6 or I_8	+6	-6	-	1	-	-	1.5	-	mA
		+12	-12	2.0	2.5	1.5	4.5	4.0	4.0	
Input Current (terminal 7)	I_7	+6	-6	-	0.5	-	-	1.0	-	mA
		+12	-12	1.0	1.0	0.75	2.5	2.1	2.0	
Device Dissipation	P_T	+6	-6	-	24	-	-	42	-	mW
		+12	-12	120	120	105	230	220	210	
DYNAMIC										
Power Gain	G_P	V_{CC} = +9V, f = 10.7 MHz Diff.-Ampl. Config.		-	28	-	-	-	-	dB
		V_{CC} = +9V, f = 100 MHz Cascode Ampl. Config.		-	16	-	-	-	-	dB
Noise Figure	NF	V_{CC} = +9V, f = 100 MHz Cascode Ampl. Config.		-	-	-	-	9	-	dB
Voltage Gain (Diff.)	A	V_{CC} = +12V, f = 1 kHz R_L = 1.6 kΩ		-	40	-	-	45	-	dB

Table IV. GROUP C ELECTRICAL CHARACTERISTICS SAMPLING TESTS (T_A = 25°C, V^+ = + 12V, V^- = -12V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Input Offset Voltage	V_{IO}		-	5	mV
Input Bias Current	I_I		-	80	µA
Quiescent Oper. Current	I_6 or I_8		2.5	4.0	mA
Input Current (term. 7)	I_7		1.0	2.1	mA
Device Dissipation	P_T		120	220	mW
Power Gain	G_P	V_{CC} = +9V, f = 10.7 MHz Diff.-Ampl. Config.	28	-	dB

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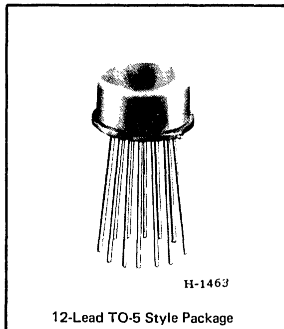
High-Reliability Slash(/) Series

CA3039/. . .



12-Lead TO-5 Style Package

High-Reliability Diode Array

Six Ultra - Fast Low - Capacitance Matched Diodes

For Applications in Communications and Switching Systems of Aerospace, Military and Critical Industrial Equipment

RCA-CA3039 "Slash" (/) Series type is a high-reliability linear integrated circuit Diode Array intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3039 described in Data Bulletin File No. 343 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3039 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Features:

- **Excellent reverse recovery time — 1 ns typ.**
- **Matched monolithic construction — V_F matched within 5 m V**
- **Low diode capacitance — C_D = 0.65 pF typical at V_R = – 2 V**

Applications:

- **Balanced modulators or demodulators**
- **Ring modulators**
- **High speed diode gates**
- **Analog switches**

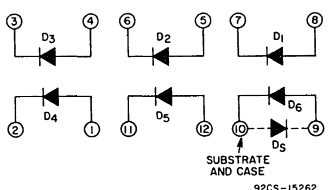


Fig. 1 - Schematic Diagram

ABSOLUTE MAXIMUM RATINGS at T_A = 25 °C

DISSIPATION:

Any one diode unit	100 mW
Total for device	600 mW
For T_A > 55 °C	derate linearly 5.7 mW/°C

TEMPERATURE RANGE

Operating	-55 to + 125 °C
Storage	-65 to + 150 °C

Peak Inverse Voltage, PIV for: D_1-D_5	5 V
D_6	0.5 V
Peak Diode-to-Substrate Voltage, V_{DI} for D_1-D_5 (term. 1,4,5,8 or 12 to term. 10)	+20, - 1 V
DC Forward Current, I_F	25 mA
Peak Recurrent Forward Current, I_f	100 mA
Peak Forward Surge Current, I_f (surge)	100 mA

LEAD TEMPERATURE (During Soldering): At distance 1/6" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max .... 265°C

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS TYP.	UNITS
DC Forward Voltage Drop	V_F	I_F = 50 μA	0.65	V
		1 mA	0.73	V
		3 mA	0.76	V
		10 mA	0.81	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 40μA	7	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = −10 μA	–	V
DC Reverse (Leakage) Current	I_R	V_R = −4 V	0.016	nA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = −10 V	0.022	nA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F1} - V_{F2} \rvert$	I_F = 1 mA	0.5	mV
Temperature Coefficient of $\lvert V_{F1} - V_{F2} \rvert$	$\frac{\Delta \lvert V_{F1} - V_{F2} \rvert}{\Delta T}$	I_F = 1 mA	1	μV/°C
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	−1.9	mV/°C
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	0.65	V
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	1	ns
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	30	Ω
Diode Capacitance	C_D	V_R = −2 V, I_F = 0	0.65	pF
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	3.2	pF

*Table I — Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25° C	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Each Diode DC Forward Voltage Drop	V_F	I_F = 3 mA	0.69	0.81	±0.010	V

* Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 7.

Table II — Final Electrical Tests and Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Each Diode: DC Forward Voltage Drop	V_F	I_F = 3 mA	0.82	0.69	0.47	1.0	0.86	0.63	V
DC Reverse Leakage Current	I_R	V_R = −4 V	–	–	–	–	100	–	nA
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 40 μA	–	5	–	–	–	–	V
Between Any Two Diodes: Diode Offset Voltage	$\|V_{F1} - V_{F2}\|$	I_F = 1 mA	–	–	–	–	8	–	mV
Breakdown Voltage Isolation-to-Substrate		−50 V through a 25 kΩ resistor to terminal 10. Ground terminals 1 through 9, 11 and 12. Measure voltage at terminal 10.	–	–	–	−25	−25	−25	V

Table III — Group C Electrical Characteristics Sampling Tests (T_A = 25° C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Each Diode: DC Forward Voltage Drop	V_F	I_F = 3 mA	0.69	0.81	V
DC Reverse Leakage Current	I_R	V_R = −4 V	–	100	nA
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 40 μA	5	–	V
Between Any Two Diodes: Diode Offset Voltage	$\|V_{F1} - V_{F2}\|$	I_F = 1 mA	–	8	mV

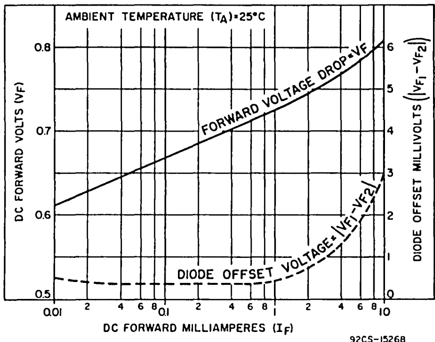


Fig. 2 – DC forward voltage drop (any diode) and diode offset voltage vs DC forward current.

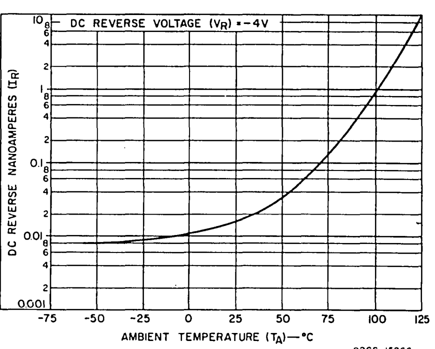


Fig. 3 – DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature.

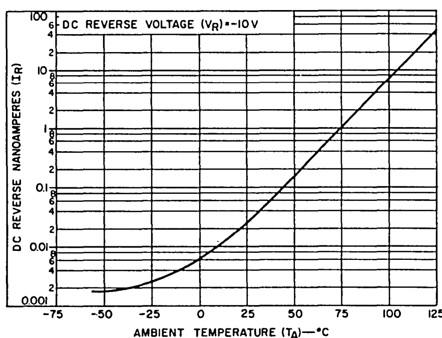


Fig. 4 – DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature.

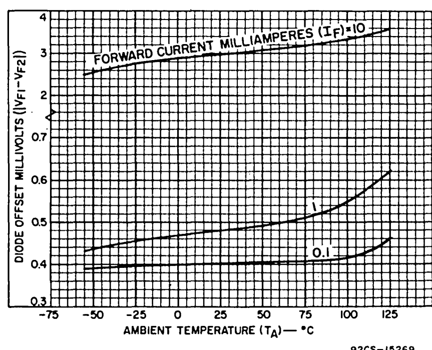


Fig. 5 – Diode offset voltage (any diode) vs temperature.

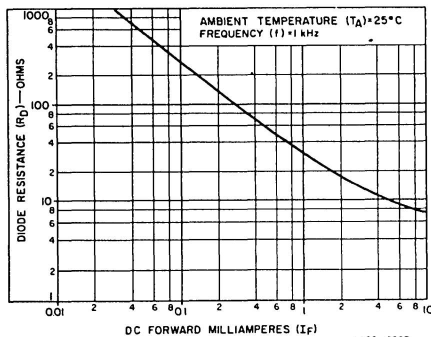


Fig. 6 – Diode resistance (any diode) vs DC forward current.

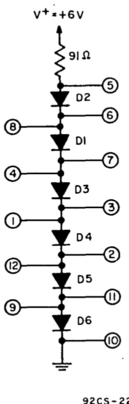


Fig. 7 – Burn-in and operating life test circuit.

Solid State
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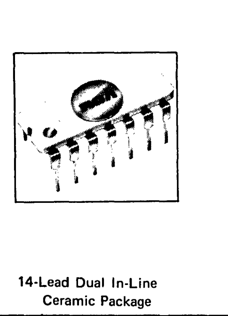
Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3045/. . .



14-Lead Dual In-Line
Ceramic Package

High-Reliability General-Purpose Transistor Array

Three Isolated Transistors and One Differentially-Connected Transistor Pair

For Low-Power Applications at Frequencies Through the VHF Range

In Aerospace, Military, and Critical Industrial Equipment

Features:

- **Two matched pairs of transistors**
  V_{BE} matched ±5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- **5 general purpose monolithic transistors**
- **Operation from DC to 120 MHz**
- **Wide operating current range**
- **Low noise figure – 3.2 dB typ. at 1 kHz**
- **Full military temperature range for CA3045 -55 to +125°C**

RCA-CA-3045 "Slash" (/) Series type is a high-reliability linear integrated circuit general-purpose transistor array intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3045 described in Data Bulletin File No. 341 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3045 Slash (/) Series type is supplied in the 14-lead dual-in-line ceramic package ("D" suffix) or in chip form ("H" suffix).

Applications:

- **General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF**
- **Custom designed differential amplifiers**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

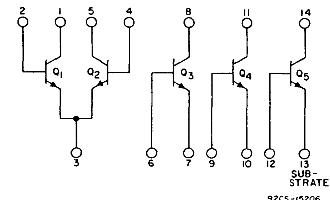


Fig. 1 – Schematic diagram.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C:

	EACH TRANSISTOR	TOTAL PACKAGE	
POWER DISSIPATION:			
At T_A up to 75°C	300	750	mW
At T_A > 75°C		Derate at 8 mW/°C	
Collector-to-Emitter Voltage, V_{CEO}	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	V
Collector Current, I_C	50	–	mA
TEMPERATURE RANGE:			
Operating		-55 to +125	°C
Storage		-65 to +150	°C
LEAD TEMPERATURE (During Soldering):			
At distance 1/16" ± 1/32" (1.59 mm ±0.79 mm) from case for 10 s max.			265°C

*The collector of each transistor of the CA3045 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 TYP.	UNITS	CHARAC-TERISTIC CURVES FIG.
STATIC CHARACTERISTICS					
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	60	V	-
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	24	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	60	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	7	V	-
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	0.002	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	See curve	μA	3
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V: I_C = 10 mA I_C = 1 mA I_C = 10 μA	100 100 54	- - -	4
Input Offset Current for Matched Pair Q_1 and Q_2. $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	0.3	μA	5
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V: I_E = 1 mA I_E = 10 mA	0.715 0.800	V	6
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	0.45	mV	6,8
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	0.45	mV	6,8
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	−1.9	mV/°C	7
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	0.23	V	-
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	1.1	μV/°C	8

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 TYP.	UNITS	CHARAC-TERISTIC CURVES FIG.
DYNAMIC CHARACTERISTICS					
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source Resistance = 1 kΩ	3.25	dB	10(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:					
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	110	-	11
Short-Circuit Input Impedance	h_{ie}		3.5	kΩ	
Open-Circuit Output Impedance	h_{oe}		15.6	μmho	
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		1.8×10^{-4}	-	
Admittance Characteristics:					
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	31-j1.5	-	
Input Admittance	Y_{ie}		0.3+j0.04	-	
Output Admittance	Y_{oe}		0.001+j0.03	-	
Reverse Transfer Admittance	Y_{re}		See curve	-	
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	550	-	9
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	0.6	pF	-
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	0.58	pF	-
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	2.8	pF	-

*Table I — Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits**

Electrical Characteristics, at T_A = 25°C For Each Transistor (Except where otherwise indicated)						
Characteristics	Symbol	Test Conditions	Limits			Units
			Min.	Max.	Max.Δ	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0 (Except Q_5)	5	-	±0.5	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	-	0.5	±0.15	μA
Input Current	I_I	I_C = 1mA, V_{CE} = 3V	5	25	±3	μA
Base-to-Emitter Voltage	V_{BE}	I_C = 1mA, V_{CE} = 3V	0.6	0.8	±0.10	V

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits. Level 3 requires pre burn-in test only. The burn-in and operating life test circuit is shown in Fig. 6.

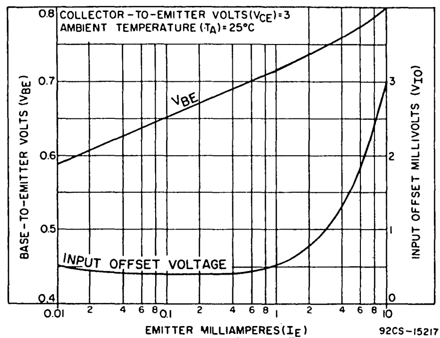


Fig. 2—Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

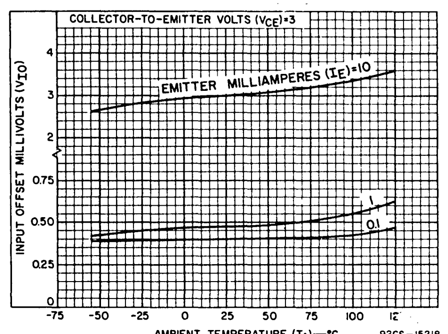


Fig. 3—Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

Table II – Final Electrical Tests (For each transistor unless otherwise indicated)

Characteristics	Symbol	Test Conditions	Limits For Indicated Temperature (°C) Minimum -55	Minimum +25	Minimum +125	Maximum -55	Maximum +25	Maximum +125	Units
STATIC									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	-	20	-	-	-	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	-	15	-	-	-	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$	-	20	-	-	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$ (Except Q5)	-	5	-	-	-	-	V
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	-	-	-	40	-	nA
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	-	-	-	0.5	100	μA
Static Forward Current-Transfer Ratio	h_{FE}	$V_{CE} = 3V$, $I_C = 10mA$	-	30	-	-	-	-	–
		$V_{CE} = 3V$, $I_C = 1mA$	18	40	45	-	-	-	
		$V_{CE} = 3V$, $I_C = 10\mu A$	-	15	-	-	-	-	
Input Offset Current for Differential Pair	$\|I_{IO_1} - I_{IO_2}\|$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	2	-	μA
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 10mA$					1.0		V
		$V_{CE} = 3V$, $I_C = 1mA$	0.7	0.6	0.4	1.0	0.8	0.7	
Input Offset Voltage for Differential Pair	$\|V_{BE_1} - V_{BE_2}\|$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Input Offset Voltage for Isolated Transistors	V_{IO}	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1mA$, $I_C = 10mA$	-	-	-	-	0.5	-	V

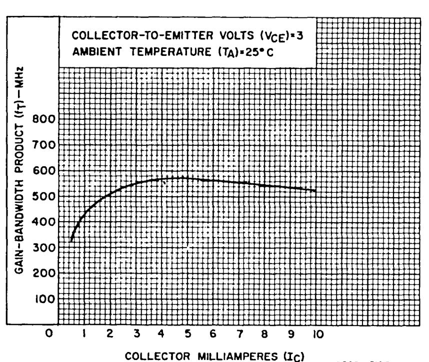


Fig. 4 — Typical gain-bandwidth product vs collector current.

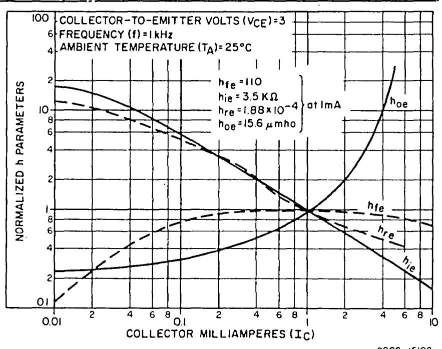


Fig. 5 — Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

Table III — Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions	Limits for Indicated Temperature (°C)						Units
			Minimum			Maximum			
			-55	+25	+125	-55	+25	+125	
STATIC									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	-	20	-	-	-	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	-	15	-	-	-	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$	-	20	-	-	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$ (Except Q_5)	-	5	-	-	-	-	V
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	-	-	-	40	-	nA
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	-	-	-	0.5	100	µA
Static Forward Current-Transfer Ratio	h_{FE}	$V_{CE} = 3V$, $I_C = 10mA$	-	30	-	-	-	-	—
		$V_{CE} = 3V$, $I_C = 1mA$	18	40	45	-	-	200	—
		$V_{CE} = 3V$, $I_C = 10\mu A$	-	15	-	-	-	-	—
Input Offset Current for Differential Pair, (Q_1, Q_2)	$\lvert I_{IO_1} - I_{IO_2} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	-	2	µA
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 1mA$	0.7	0.6	0.4	1.0	0.8	0.70	V
		$V_{CE} = 3V$, $I_C = 10mA$	-	-	-	-	1.0	-	V
Input Offset Voltage for Differential Pair, (Q_1, Q_2)	$\lvert V_{BE_1} - V_{BE_2} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Input Offset Voltage for Isolated Transistors $\lvert Q_3 - Q_4 \rvert, \lvert Q_4 - Q_5 \rvert, \lvert Q_5 - Q_3 \rvert$	V_{IO}	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1mA$, $I_C = 10mA$	-	-	-	-	0.5	-	V
DYNAMIC									
Gain-Bandwidth Product (Q_3)	f_T	$V_{CE} = 3V$, $I_C = 3mA$, $f = 100$ MHz	-	300	-	-	-	-	MHz

Table IV — Group C Electrical Characteristics Sampling Tests
($T_A = 25°C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V)

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$ (Except Q5)	5	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	15	-	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	-	0.5	µA
Input Current	I_I	$V_{CE} = 3$ V, $I_C = 1$ mA	5	25	µA
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3$ V, $I_C = 1$ mA	0.6	0.8	V

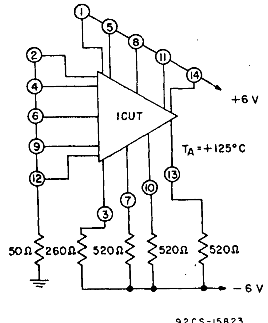


Fig. 6 — Burn-in and operating life test circuit.

Solid State
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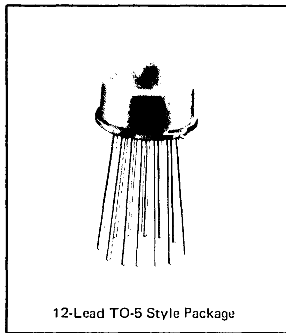
High-Reliability Slash(/) Series
CA3049/. . .



12-Lead TO-5 Style Package

High-Reliability Dual High-Frequency Differential Amplifier

For Low-Power Applications at Frequencies up to 500 MHz in Aerospace, Military and Critical Industrial Equipment

Features:
- Power Gain 23 dB (typ.) at 200 MHz
- Noise Figure 4.6 dB (typ.) at 200 MHz
- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs

RCA-CA3049 "Slash" (/) Series type is a high-reliability linear integrated circuit dual high-frequency differential amplifier intended for low-power applications at frequencies up to 500 MHz in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3049 described in Data Bulletin File No. 611 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3049 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications
- VHF amplifiers
- VHF mixers
- Multifunction combinations – RF/Mixer/Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Balanced mixers
- Synthesizers
- Balanced (push-pull) cascode amplifiers
- Sense amplifiers

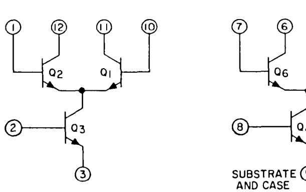


Fig. 1 - Schematic Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

POWER DISSIPATION, P:

Any one transistor	300
Total package	600
For T_A > 55°C Derate at:	5 mW/°C

TEMPERATURE RANGE:

Operating	−55 to +125°C
Storage	−65 to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max. .... 265°C

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

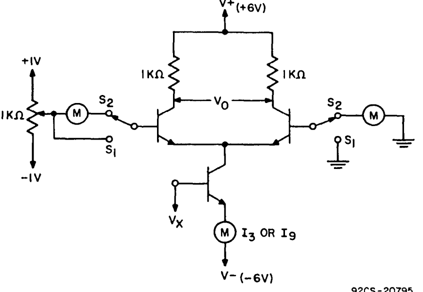
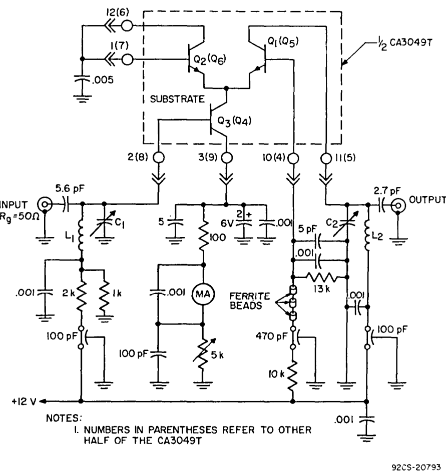


Fig. 2 — Static characteristics test circuit



L_1, L_2 — Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.
C_1, C_2 — 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)
All Capacitors in μF Unless Otherwise Indicated
All Resistors in Ohms Unless Otherwise Indicated

Fig. 3 — 200 MHz cascode power gain and noise figure test circuit.

*Table I — Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS at T_A = 25°C	LIMITS MIN.	MAX.	MAX. Δ	UNITS
Input Bias Current Q1, Q2, Q5, Q6	I_I	$I_3 = I_9$ = 2mA, V^+ = +6 V	–	25.2	±6	μA
Input Bias Current Q3, Q4	I_I	$I_3 = I_9$ = 2mA, V^+ = +6 V	–	50.4	±12	μA
Emitter-to Base Breakdown Voltage Q3, Q4	V_{EBO}	I_E = 10μA, I_C = 0	-5.3	–	±1.0	V
Collector Cutoff Current Q1 to Q6	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	95	±50	nA

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 9.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CA3049T TYP.	UNITS
STATIC CHARACTERISTICS					
For Each Differential Amplifier					
Input Offset Voltage	V_{IO}			0.25	mV
Input Offset Current	I_{IO}	$I_3 = I_9 = 2$ mA		0.3	μA
Input Bias Current	I_{IB}			13.5	μA
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$			1.1	μV/°C
For Each Transistor					
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$ V, $I_C = 1$ mA		774	mV
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 6$ V, $I_C = 1$ mA		-0.9	mV/°C
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		0.0013	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		24	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$		60	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ μA, $I_B = 0$, $I_E = 0$		60	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ μA, $I_C = 0$		7	V
DYNAMIC CHARACTERISTICS					
1/f Noise Figure (For Single Transistor)	NF	f = 100 KHz, $R_S = 500\ \Omega$, $I_C = 1$ mA		1.5	dB
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6$ V, $I_C = 5$ mA		1.35	GHz
Collector-Base Capacitance	C_{CB}	$I_C = 0$	$V_{CB} = 5V$	0.28 0.28	pF pF
Collector-Substrate Capacitance	C_{CI}	$I_C = 0$	$V_{CI} = 5V$	1.65	pF
For Each Differential Amplifier					
Common-Mode Rejection Ratio	CMR	$I_3 = I_9 = 2$ mA		100	dB
AGC Range, One Stage	AGC	Bias Voltage = -6V		75	dB
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		22	dB
Insertion Power Gain	G_P	f = 200 MHz	Cascode	23	dB
Noise Figure	NF	$V_{CC} = 12V$	Cascode	4.6	dB
Input Admittance	Y_{11}	For Cascode Configuration	Cascode	1.5 + j 2.45	mmho
		$I_3 = I_9 = 2$ mA	Diff.Amp.	0.878 + j 1.3	
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration	Cascode	0 - j 0.008	mmho
		$I_3 = I_9 = 4mA$	Diff.Amp.	0 - j 0.013	
Forward Transfer Admittance	Y_{21}	(each collector	Cascode	17.9 - j 30.7	mmho
		$I_C \simeq 2mA$)	Diff. Amp.	- 10.5 + j 13	
Output Admittance	Y_{22}		Cascode	- 0.503 - j 15	mmho
			Diff.Amp.	0.071 + j 0.62	

Table II — Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
STATIC (Each Differential Amplifer)									
Input Offset Voltage	V_{IO}		–	–	–	7	5	7.5	mV
Input Offset Current	I_{IO}	$I_3 = I_9 = 2mA$ $V^+ = +6$ V	–	–	–	9	3	3	μA
Input Bias Current	I_I	$I_3 = I_9 = 2mA$ $V^+ = +6$ V	–	–	–	41	25.2	18	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	–	–	–	100	–	nA
Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6V$, $I_C = 1mA$	–	–	–	–	874	–	mV
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	–	15	–	–	–	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	–	20	–	–	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_B = I_E = 0$	–	20	–	–	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	–	5	–	–	–	–	V

Table III — Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
These tests are the same as the Final Electrical Tests except for the addition of the Dynamic test shown below									
Dynamic Voltage gain (Single-Ended Output)	A	Bias Voltage = 4.2V, f = 10 MHz	–	18	–	–	–	–	dB

Table IV — Group C Electrical Characteristics Sampling Tests ($T_A = 25°C$)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	V_{IO}		–	5	mV
Input Bias Current Q_1, Q_2, Q_5, Q_6	I_I	$I_3 = I_9 = 2$ mA, $V+ = +6$ V	–	25.2	μA
Input Bias Current Q_3, Q_4	I_I	$I_3 = I_9 = 2$ mA, $V+ = +6$ V	–	50.4	μA
Power Gain	P_G		19	26	dB

TYPICAL CHARACTERISTICS

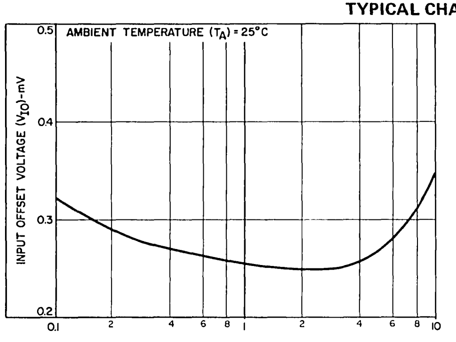


Fig. 4 — Input offset voltage vs. emitter current.

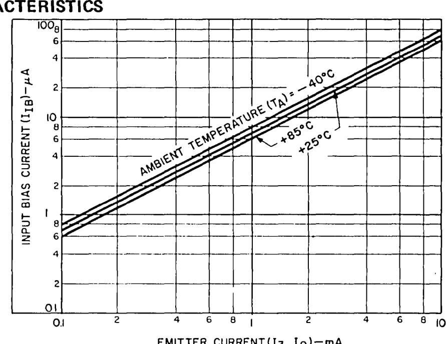


Fig. 5 — Input bias current vs. emitter current.

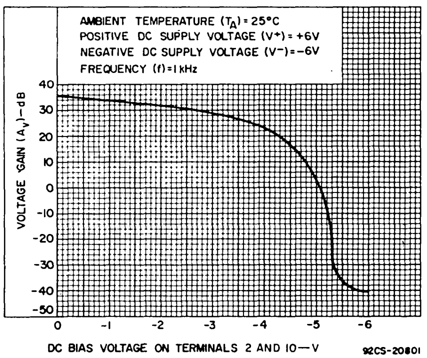


Fig. 6 — Voltage gain vs. dc bias voltage.

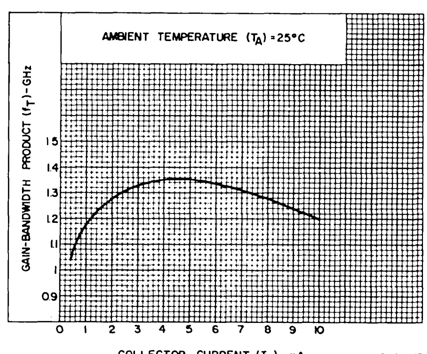


Fig. 7 — Voltage gain vs. frequency.

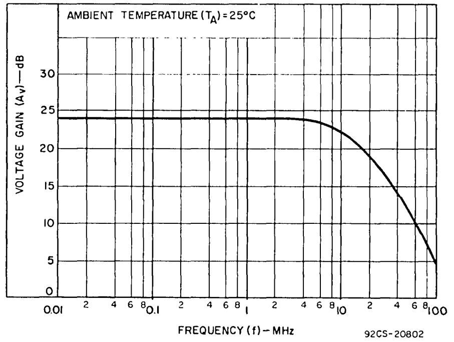


Fig. 8 — Gain-bandwidth product vs. collector current.

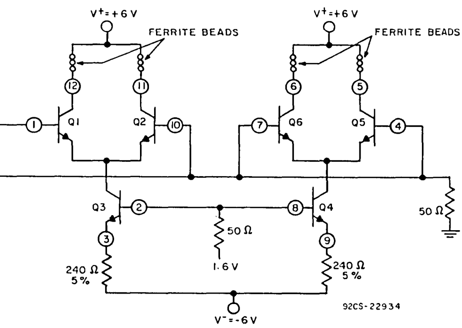


Fig. 9 — Burn-in and operating life test circuit.

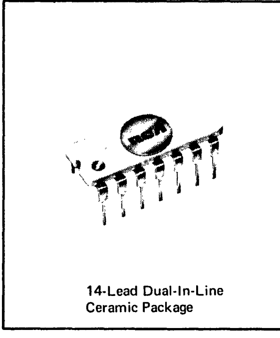
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3058/. . .



14-Lead Dual-In-Line Ceramic Package

High-Reliability Zero - Voltage Switch

For 50/60 and 400-Hz Thyristor Control Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **24 V, 120 V, 208/230 V, 277 V at 50 60, or 400 Hz operation**
- **Differential input**
- **Low balance input current (max.) 1 μA**
- **Built-in protection circuit for opened or shorted sensor (term. 14)**
- **Sensor range (R_X) - 2 to 100 kΩ**
- **DC mode (term 12)**
- **External trigger (term. 6)**
- **External inhibit (term. 1)**
- **DC supply volts (max.) 14**

RCA-CA3058 "Slash" (/) Series type is a high-reliability linear integrated circuit Zero-Voltage Switch designed to control a thyristor in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. It is intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3058 described in Data Bulletin File No. 490 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels— /1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3058 Slash (/) Series type is supplied in the 14-Lead dual-in-line ceramic package ("D" suffix), or in chip form ("H" Suffix).

AC Input Voltage (50/60 to 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

Applications

- **Relay control**
- **Heater control**
- **Photosensitive control**
- **Valve control**
- **Lamp control**
- **Power one-shot control**
- **Synchronous switching of flashing lights**
- **On-off motor switching**
- **Differential comparator with self-contained power supply for industrial applications**
- **For detailed application information, see application note 1CAN-6182 "Applications of RCA Integrated Circuit Zero-Votlage Switches (CA3058, CA3059, CA3079)"**

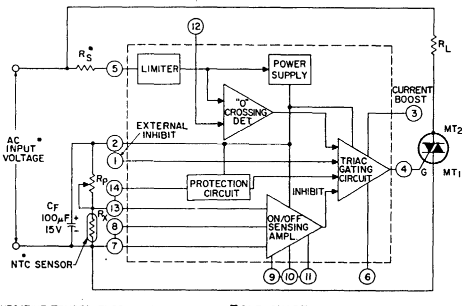


Fig. 1—Functional block diagram.

MAXIMUM RATINGS, *Absolute Maximum Values, at T_A = 25°C*

DC Supply Voltage (between Terms. 2 and 7) . . . 14 V

DC Supply Voltage (between Terms. 2 and 8) . . . 14 V

Peak Supply Current (Terms. 5 and 7) . . . . ±50 mA

Output Pulse Current (Term. 4) . . . . 150 mA

Power Dissipation:

Up to T_A = 75°C . . . . 700 mW

Above T_A = 75°C . . . . Derate Linearly 8 mW/°C

Ambient Temperature Range:

Operating . . . . -55 to +125°C

Storage . . . . -65 to +150°C

Lead Temperature (During soldering)

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max. 265 °C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C / **MAXIMUM CURRENT RATINGS**

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3	I_{IN} mA	I_{OUT} mA
1 Note 3		*	*	*	*	15 / 0	10 / −2	*	*	*	*	*	*	*	10	0.1
2			0 / −15	0 / −15	2 / −14	0 / −14	0 / −14	0 / −14	0 / −14	0 / −14	0 / −14	*	0 / −14	0 / −14	150	10
3				0 / −15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 / −10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 / −7	*	*	*	*	*	*	*	50	10
6 Note 3							14 / 0	*	*	*	*	*	*	*	*	*
7								*	14 / 0	*	20 / 0	2.5 / −2.5	14 / 0	6 / −6	*	*
8									10 / 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to −10 volts.

Note 1 – Resistance should be inserted between Term. 5 and external supply or line voltage for limiting current into Term. 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Term. 14 and external supply for limiting current into Term. 14 to less than 2 mA.

NOTE 3: For the CA3079 indicated terminal is internally connected and therefore, should not be used.

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

*Table I — Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS at T_A = 25°C	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
DC Supply Voltage	V_S	R_S = 10 kΩ, I_L = 0	6.0	7.0	±0.2	V
Output Leakage Current (Inhibit Mode)	I_4		–	10	±0.5	μA
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM}(4)	Terminal 3 Open, V_{GT}=0	50	–	±10	mA
Input Bias Current	I_I		–	1.0	±0.2	μA

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 8.

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $T_A = 25^oC$ (Unless Indicated Otherwise)	LIMITS Typ.	UNITS
For Operating at 120V rms, 50-60 Hz (AC Line Voltage)•				
DC Supply Voltage: Inhibit Mode At 50/60 Hz	V_S	$R_S = 10\ k\ \Omega$, $I_L = 0$	6.5	V
At 400 Hz		$R_S = 10\ k\ \Omega$, $I_L = 0$	6.8	V
At 50/60 Hz		$R_S = 5\ k\ \Omega$, $I_L = 2\ mA$	6.4	V
Pulse Mode At 50/60 Hz		$R_S = 10\ k\ \Omega$, $I_L = 0$	6.4	V
At 400 Hz		$R_S = 10\ k\ \Omega$, $I_L = 0$	6.7	V
At 50/60 Hz		$R_S = 5\ k\ \Omega$, $I_L = 2\ mA$	6.3	V
Gate Trigger Current	I_{GT} (4)	Terms 3 and 2 connected, V_{GT}=1V	105	mA
Peak Output Current (Pulsed): With Internal Power Supply	I_{OM} (4)	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	84	mA
		Terms.3 and 2 connected, Gate Trigger Voltage (V_{GT}) = 0	124	mA
With External Power Supply	I_{OM} (4)	Term. 3 open, V^+ = 12V, V_{GT} = 0	170	mA
		Terms 3 and 2 connected V^+ = 12V, V_{GT} = 0	240	mA
Inhibit Input Ratio:	V_9/V_2	Voltage Ratio of Term. 9 to 2	0.485	–
Total Gate Pulse Duration: For positive dv/dt 50-60 Hz	t_P	$C_{EXT} = 0$	100	µs
400 Hz	t_P	$C_{EXT} = 0$, $R_{EXT} = \infty$	12	µs
For negative dv/dt 50-60 Hz	t_N	$C_{EXT} = 0$	100	µs
400 Hz	t_N	$C_{EXT} = 0$, $R_{EXT} = \infty$	10	µs
Pulse Duration After Zero Crossing (50-60Hz): For positive dv/dt	t_{P1}	$C_{EXT} = 0$	50	µs
For negative dv/dt	t_{N1}	$R_{EXT} = \infty$	60	µs
Output Leakage Current Inhibit Mode:	I_4		0.001	µA
Input Bias Current:	I_I		220	nA
Common-Mode Input Voltage Range	V_{CMR}	Terms. 9 and 13 connected	1.5 to 5	V
Sensitivity ≠ (Pulse Mode)	ΔV_{13}	Term. 12 open	6	mV

≠Required voltage change at Term.13 to either turn OFF the triac when ON or turn ON the triac when OFF.

•The values given in the Electrical Characteristics Chart at 120V also apply for operation at input voltages of 24V, 208/230V, and 277V, except for Pulse Duration. However, the series reistor (R_S) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

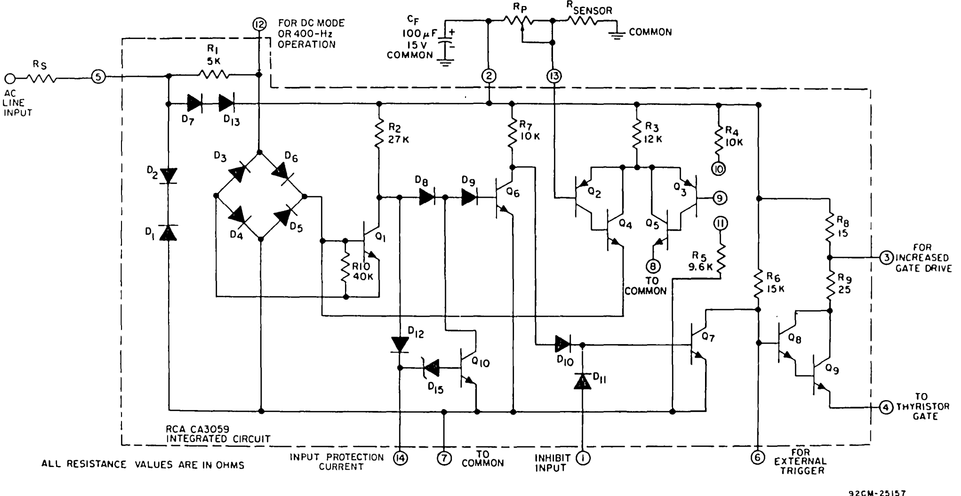


Fig. 2–Schematic diagram of CA3058 zero-voltage switch. For functional block diagram see Fig. 1.

Table II – Final Electrical Tests and Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS f = 50/60 Hz	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
DC Supply Voltage	V_S	R_S = 10 kΩ, I_L = 0	5.5	6.0	5.5	7.5	7.0	7.5	V
Output Leakage Current (Inhibit Mode)	I_4		–	–	–	20	10	20	µA
Input Bias Current	I_I		–	–	–	1.0	1.0	1.0	µA
Inhibit Input Ratio	V_G/V_Z	Voltage ratio of terminal 9 to terminal 2.	0.450	0.465	0.450	0.520	0.520	0.520	
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM} (4)	Terminal 3 open, V_{GT} = 0	–	50	–	–	–	–	mA
		Terminals 2 and 3 shorted, V_{GT} = 0	–	90	–	–	–	–	mA

Table III – Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS f = 50/60 Hz	LIMITS		UNITS
			MIN.	MAX.	
DC Supply Voltage	V_S	R_S = 10 kΩ, I_L = 0	5.9	7.1	V
Output Leakage Current (Inhibit Mode)	I_4		–	11	µA
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM} (4)	Terminal 3 Open, V_{GT} = 0	45	–	mA
Input Bias Current	I_I		–	1.2	µA

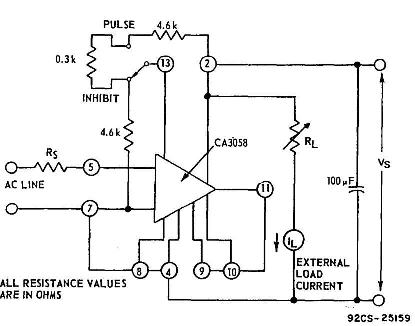


Fig. 3a—DC supply voltage test circuit

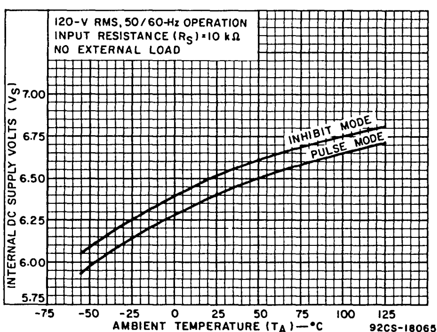


Fig. 3b—DC supply voltage vs. T_A

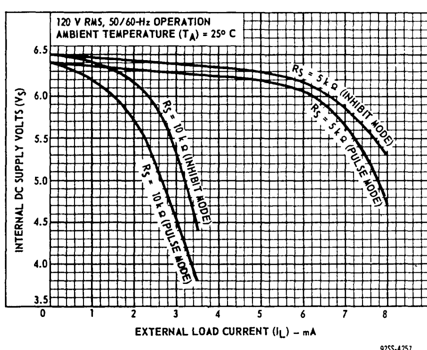


Fig. 3c—DC supply voltage vs. external load current

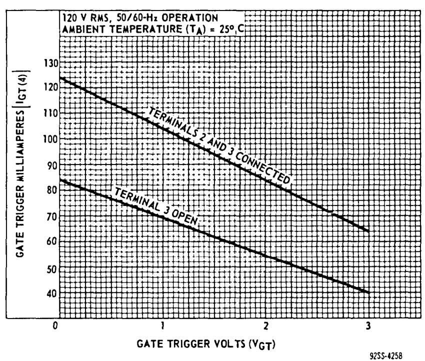


Fig. 4—Gate trigger current vs. gate trigger voltage

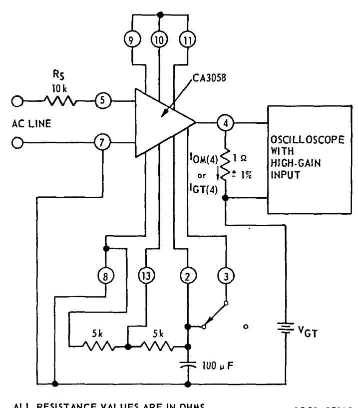


Fig. 5a—Peak output (pulsed) and gate trigger current with internal power supply test circuit

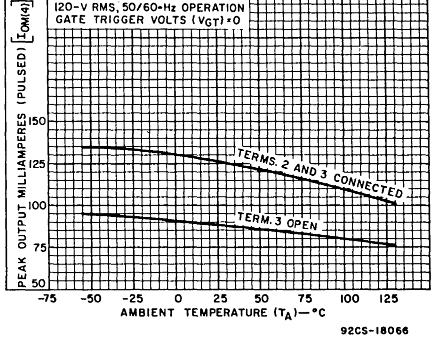


Fig. 5b—I_{OM} vs. T_A

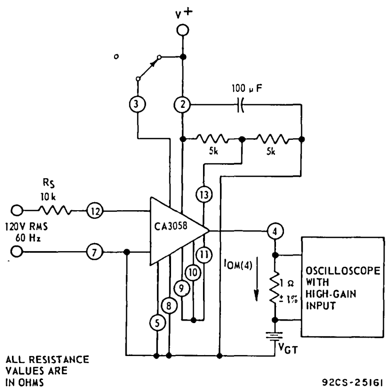


Fig. 6a—Peak output current (pulsed) with external power supply test circuit

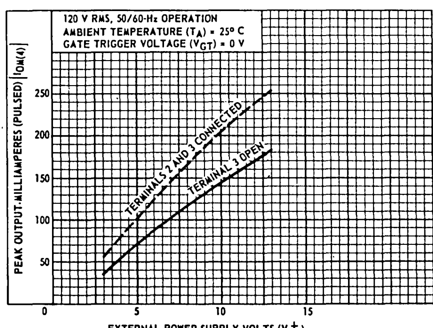


Fig. 6b—I_{OM} vs. external power supply voltage

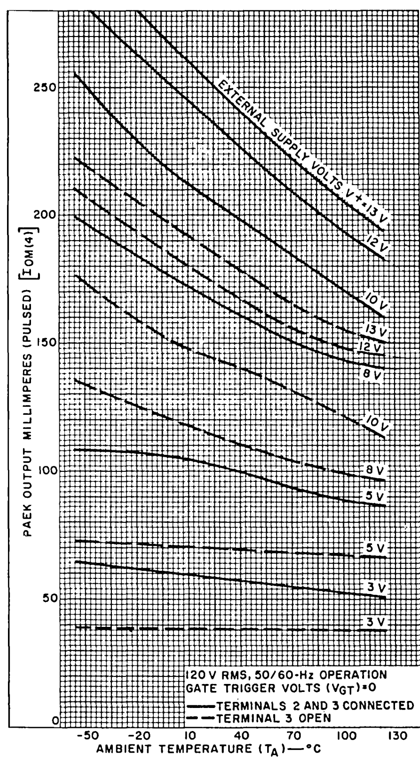


Fig. 6c—I_{OM} with external power supply vs. T_A

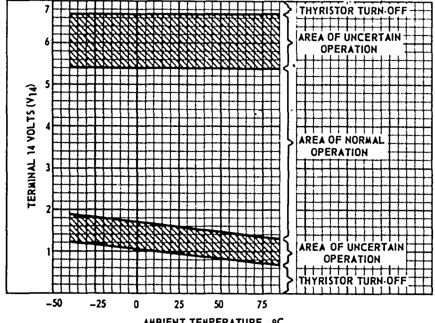


Fig. 7—Operating regions for built-in protection circuit

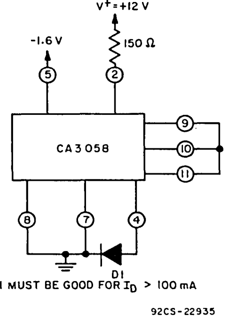


Fig. 8—Burn-in and operating life test circuit.

Solid State
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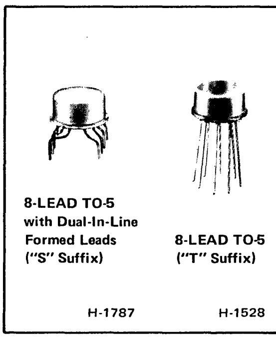
Monolithic Silicon

High-Reliability Slash (/) Series
CA3078A/ . . .



High-Reliability
Micropower Operational Amplifier

For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Low standby power: as low as 700 nW**
- **Wide supply voltage range: ±0.75 to ±15 V**
- **High peak output current: 6.5 mA min.**
- **Adjustable quiescent current**
- **Output short-circuit protection**

Applications:

- **Portable electronics**
- **Medical electronics**
- **Instrumentation**
- **Telemetry**

The CA3078A "Slash" (/) Series types are high-reliability linear integrated circuit operational amplifiers intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3078A described in Data Bulletin File No. 535 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, and /4 — which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels — /M, /N, and /R. These screening levels and detailed information on test methods, procedures and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3078AS and CA3078AT can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078AS and CA3078AT provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The CA3078A is supplied in the standard 8-lead TO-5 package ("T" suffix), the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix), or in chip form ("H" suffix).

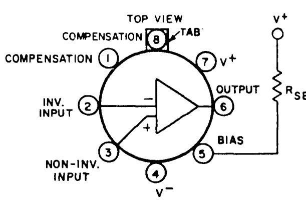


Fig. 1—Functional diagram of the CA3078AS and CA3078AT.

MAXIMUM RATINGS,

Absolute Maximum Values at $T_A = 25°C$

DC SUPPLY VOLTAGE (Between V+ and V− terminal)	36V
DIFFERENTIAL INPUT VOLTAGE	±6V
DC INPUT VOLTAGE	V+ to V−
INPUT SIGNAL CURRENT	0.1 mA
OUTPUT SHORT-CIRCUIT DURATION*	No Limitation
DEVICE DISSIPATION	250 mW (up to 125°C)
TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max.	+300°C

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS, *at $T_A = 25^oC$*
Typical Values Intended Only for Design Guidance

CHARACTERISTIC SYMBOLS	TYPICAL VALUES CA3078A $V^+ = +1.3V$, $V^- = -1.3V$, $R_{SET} = 2\ M\Omega$, $I_Q = 10\ \mu A$	TYPICAL VALUES CA3078A $V^+ = +0.75\ V$, $V^- = -0.75\ V$, $R_{SET} = 10\ M\Omega$, $I_Q = 1\ \mu A$	CHARACTERISTICS CURVES Fig.	UNITS
V_{IO}	0.7	0.9	–	mV
I_{IO}	0.3	0.054	–	nA
I_{IB}	3.7	0.45	4, 10	nA
A_{OL}	84	65	–	dB
I_Q	10	1	–	μA
P_D	26	1.5	–	μW
V_{OPP}	1.4	0.3	–	V
V_{ICR}	–0.8 to +1.1	–0.2 to +0.5	–	V
CMRR	100	90	–	dB
$I_{OM}^{\pm}$	12	0.5	7	mA
$\Delta V_{IO}/\Delta V^{\pm}$	20	50	–	μV/V

Typical Values Intended Only for Design Guidance, *at $T_A = 25^\circ C$ and $V^+ = +6\ V$, $V^- = -6\ V$*

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	CA3078A $R_{SET} = 5.1\ M\Omega$, $I_Q = 20\ \mu A$	CA3078A $R_{SET} = 1\ M\Omega$, $I_Q = 100\ \mu A$	UNITS
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leqslant 10\ K\Omega$	5	6	μV/°C
Input Offset Current Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leqslant 10\ K\Omega$	6.3	70	pA/°C
Open-Loop Bandwidth	BW_{OL}	3dB pt.	0.3	2	kHz
Slew Rate: Unity Gain	SR	See Fig. 11	0.027	0.04	V/μs
Slew Rate: Comparator	SR	See Fig. 11	0.5	1.5	V/μs
Transient Response	–	10% to 90% Rise Time	3	2.5	μs
Input Resistance	R_I		7.4	1.7	MΩ
Output Resistance	R_O		1	0.8	KΩ
Equiv. Input Noise Voltage	e_N(10 Hz)	$R_S = 0$	40	–	nV/√Hz
Equiv. Input Noise Current	i_N(10 Hz)	$R_S = 1\ M\Omega$	0.25	–	pA/√Hz

Table I. Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits•
ELECTRICAL CHARACTERISTICS, *at $T_A = 25^oC$, $V^+ = +6\ V$, $V^- = -6\ V$*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	LIMITS MAX.△	UNITS
Input Offset Voltage	V_{IO}	$R_S = \leqslant 10K$	–	3.5	±1	mV
Input Offset Current	I_{IO}		–	2.5	±0.4	nA
Input Bias Current	I_I		–	12	±1.5	nA
Maximum Output Current	I_{OM}^+ or I_{OM}^-		6.5	–	±1	mA

• Levels /1 and /2 require pre burn-in electrical post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 18.

Table II Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS						UNITS
					Rset = 5.1 MΩ I_Q = 20 µA						
		V+ & V-	R_S KΩ	R_L KΩ	MINIMUM			MAXIMUM			
					-55	+25	+125	-55	+25	+125	
Input Offset Voltage	V_{IO}	↑	≤10	–	–	–	–	4.5	3.5	4.5	mV
Input Offset Current	I_{IO}		–	–	–	–	–	5	2.5	5	nA
Input Bias Current	I_{IB}		–	–	–	–	–	50	12	50	nA
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	90	92	90	–	–	–	dB
Total Quiescent Current	I_Q		–	–	–	–	–	45	25	45	µA
Device Dissipation	P_D		–	–	–	–	–	540	300	540	µW
Maximum Output Voltage	V_{OM}	6	–	≥10	±5	±5.1	±5	–	–	–	V
Common-Mode Input Voltage Range	V_{ICR}		≤10	–	-5 to +5	-5 to +5	-5 to +5	–	–	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	–	80	–	–	–	–	dB
Maximum Output Current	I_{OM}^+ or I_{OM}^-		–	–	6.5	6.5	6.5	30	30	30	mA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$		≤10	–	–	76	–	–	–	–	µV/V
Negative	$\Delta V_{IO}/\Delta V^-$	↓		–	–	76	–	–	–	–	
						R_{SET} = 13MΩ, I_Q = 20 µA					
Input Offset Voltage	V_{IO}	↑	≤10	–	–	–	–	4.5	3.5	4.5	mV
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	88	92	88				dB
Total Quiescent Current	I_Q	15	–	–	–	–	–	50	30	50	µA
Device Dissipation	P_D		–	–	–	–	–	1350	750	1350	µW
Maximum Output Voltage	V_{OM}		–	≥10	±13.5	±14.1	±13.5	–	–	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	–	80	–	–	–	–	dB
Input Bias Current	I_{IB}		–	–	–	–	–	55	14	55	nA
Input Offset Current	I_{IO}	↓	–	–	–	–	–	5.5	2.7	5.5	nA

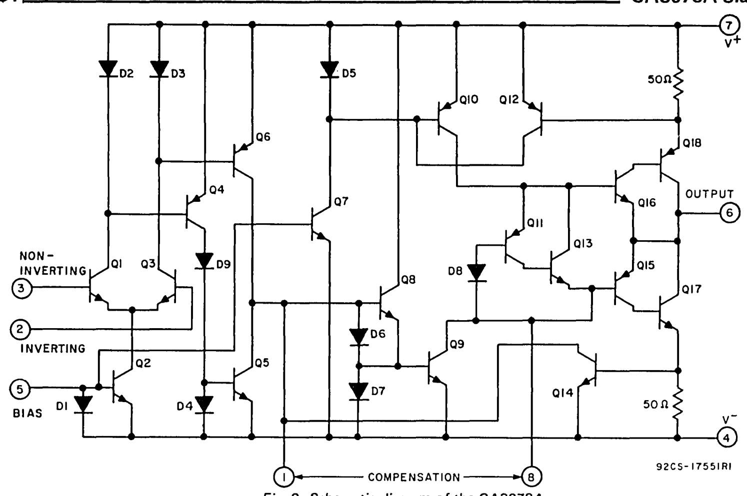


Fig. 2—Schematic diagram of the CA3078A.

Table III. Group C Electrical Characteristics Sampling Tests at T_A = +25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: V+ and V−	TEST CONDITIONS: R_S	TEST CONDITIONS: R_L	LIMITS (R_{SET} = 5.1 MΩ, I_Q = 20 μA): MIN.	LIMITS (R_{SET} = 5.1 MΩ, I_Q = 20 μA): MAX.	UNITS
Input Offset Voltage	V_{IO}	↑	≤ 10 KΩ		–	4.5	mV
Input Offset Current	I_{IO}				–	4	nA
Input Bias Current	I_I	6			–	28	nA
Open-Loop Differential Voltage Gain	A_{OL}			≥ 10 KΩ	84	–	dB
Maximum Output Voltage	V_{OM}	↓		≥ 10 KΩ	±4.0	–	V
		R_{SET} = 13 mΩ		I_Q = 20 μA			
Input Offset Voltage	V_{IO}	↑	≤ 10 KΩ		–	4.5	mV
Large-Signal Voltage Gain	A_{OL}	15		≥ 10 KΩ	84	–	dB
Maximum Output Voltage	V_{OM}	↓		≥ 10 KΩ	±10	–	V

TYPICAL CHARACTERISTICS

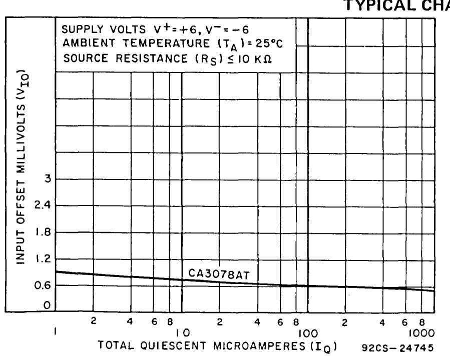


Fig. 3—Input offset voltage vs. total quiescent current.

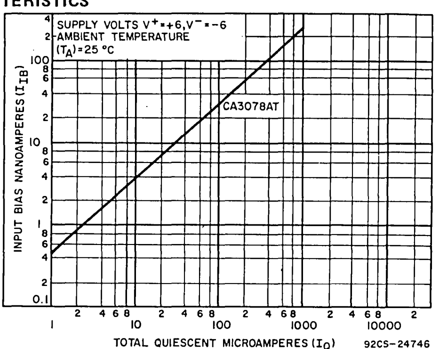


Fig. 4—Input bias current vs. total quiescent current.

TYPICAL CHARACTERISTICS (Cont'd)

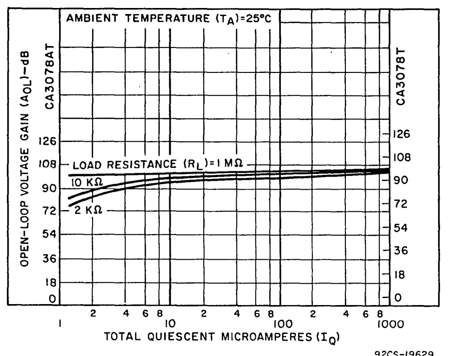


Fig. 5—Open-loop voltage gain vs. total quiescent current.

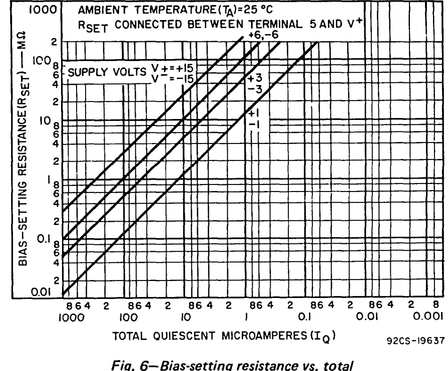


Fig. 6—Bias-setting resistance vs. total quiescent current.

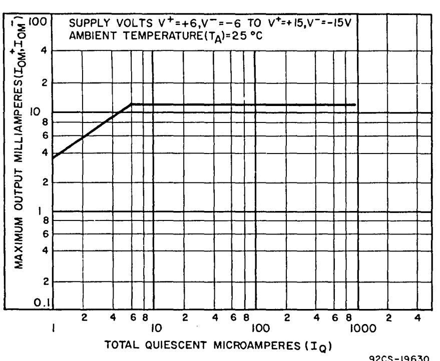


Fig. 7—Maximum output current vs. total quiescent current.

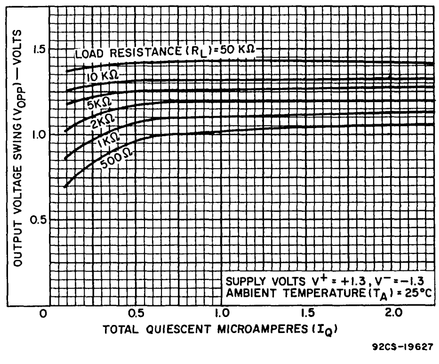


Fig. 8—Output voltage swing vs. total quiescent current.

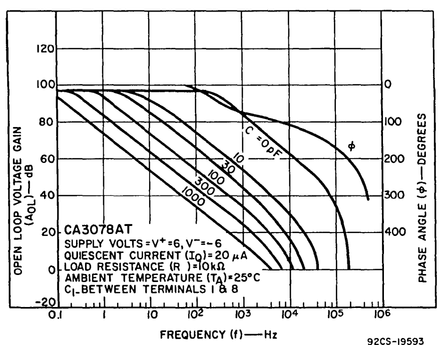


Fig. 9—Open-loop voltage gain vs. frequency for I_Q = 20 μA — CA3078A.

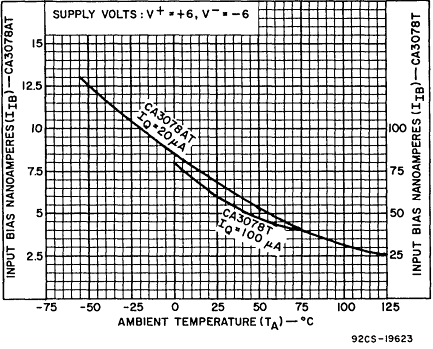


Fig. 10—Input bias current vs. temperature.

TYPICAL CHARACTERISTICS (Cont'd)

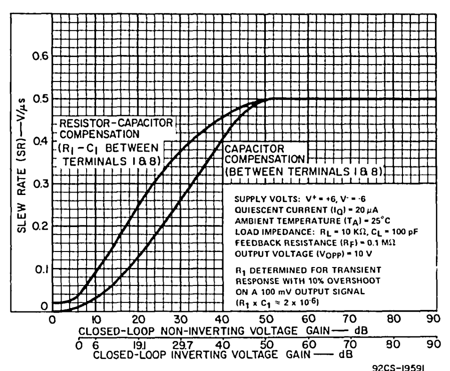


Fig. 11—Slew rate vs. closed-loop gain for I_Q = 20 µA – CA3078A.

Fig. 12—Phase compensation capacitance vs. closed-loop gain – CA3078AT.

OPERATING CONSIDERATIONS

Compensation Techniques

The CA3078A can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Fig. 12. These curves represent the compensation necessary at quiescent currents of 20 µA and 100 µA, respectively, for a transient response with 10% overshoot. Fig. 11 shows the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output.

Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table 4 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 20 µA and 100 µA.

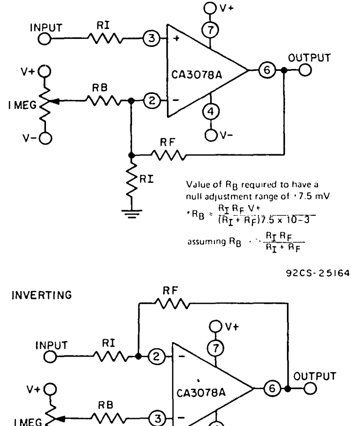


Fig. 13—Offset voltage null circuits.

Fig. 14—Inverting 20-dB amplifier circuit.

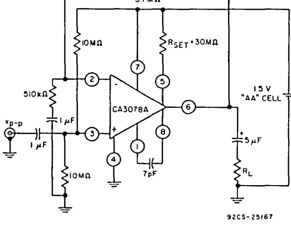


Fig. 15—Non inverting 20-dB amplifier circuit.

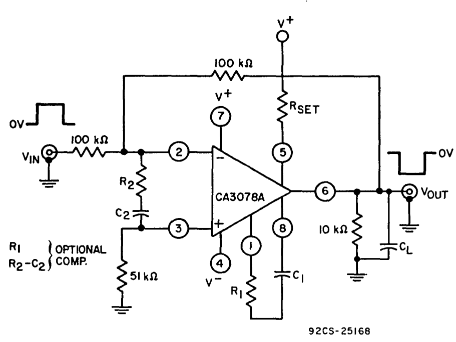


Fig. 16—Transient response and slew-rate, unity gain (inverting) test circuit.

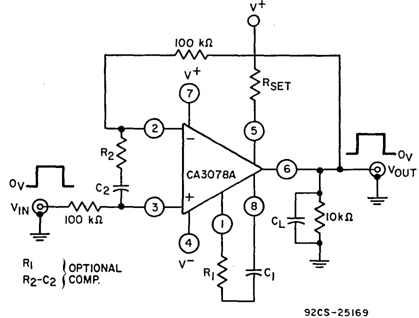


Fig. 17—Slew-rate, unity gain (non-inverting) test circuit.

Table IV. Unity-gain slew rate vs. compensation — CA3078A

SUPPLY VOLTS: $V^+ = 6$, $V^- = -6$
TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE OF 100 mV
OUTPUT VOLTAGE (V_O) = ±5V
AMBIENT TEMPERATURE (T_A) = 25°C
LOAD RESISTANCE (R_L) = 10 kΩ

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 16					UNITY GAIN (NON-INVERTING) Fig. 17				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078AT — I_Q = 20 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

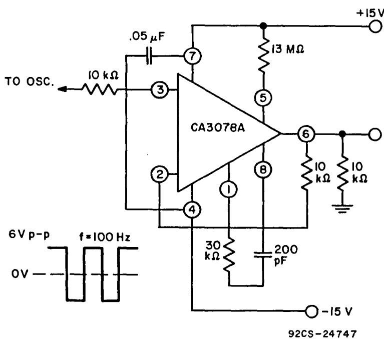


Fig. 18—Burn-in and operating life test circuit.

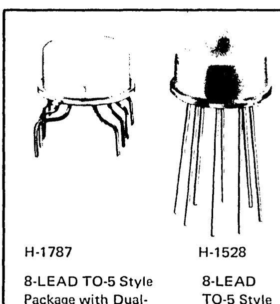
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3080/. . ., CA3080A/. . .



H-1787 8-LEAD TO-5 Style Package with Dual-In-Line Formed Leads

H-1528 8-LEAD TO-5 Style Package

High-Reliability Operational Transconductance Amplifiers Gateable-Gain Blocks

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Slew rate (unity gain, compensated): 50 V/μs**
- **Adjustable power consumption: 10 μW to 30 mW**
- **Flexible supply voltage range: ±2 V to ±15 V**
- **Fully adjustable gain: 0 to g_mR_L limit**
- **Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)**
- **Extended g_m linearity: 3 decades**
- **Hermetic package: 8-lead TO-5 style**

Applications:

- **Sample and hold**
- **Multiplex**
- **Voltage follower**
- **Multiplier**
- **Comparator**

RCA-CA3080 and CA3080A "Slash" (/) Series types are high-reliability linear integrated circuit Operational Transconductance Amplifiers. These gateable-gain blocks, which utilize the same unique OTA (Operational Transconductance Amplifier) concept first introduced in the RCA-CA3060, are intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard types CA3080 and CA3080A described in Data Bulletin File No. 475 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3080 and CA3080A Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Parameter	Value
DC Supply Voltage (between V^+ and V^- terminals)	36 V
Differential Input Voltage	±5 V
DC Input Voltage	V^+ to V^-
Input Signal Current	1 mA
Amplifier Bias Current	2 mA
Output Short-Circuit Duration	Indefinite
Device Dissipation	125 mW
Temperature Range:	
Operating	
CA3080	0 to 70 °C
CA3080A	–55 to + 125 °C
Storage	65 to +150 °C
Lead Temperature (During Soldering):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+ 300 °C

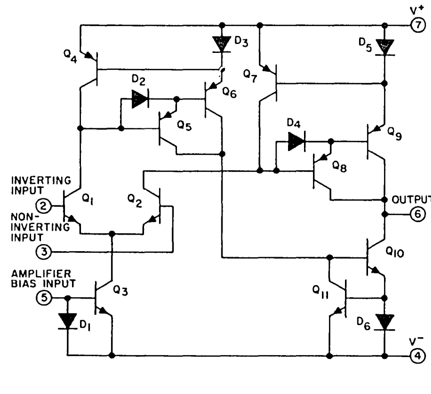


Fig. 1 – Schematic diagram for CA3080 and CA3080A.

ELECTRICAL CHARACTERISTICS
For Equipment Design CA3080

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS $V^+ = 15V$, $V^- = -15V$, $I_{ABC} = 500\mu A$, $T_A = 25^oC$ (unless indicated otherwise)	LIMITS TYP.	UNITS
Input Offset Voltage	V_{IO}		0.4	mV
Input Offset Current	I_{IO}		0.12	μA
Input Bias Current	I_I		2	μA
Forward Transconductance (large signal)	g_m		9600	μmho
Peak Output Current	$\mid I_{OM} \mid$	$R_L = 0$	500	μA
Peak Output Voltage: Positive	V^+_{OM}	$R_L = \infty$	13.5	V
Peak Output Voltage: Negative	V^-_{OM}	$R_L = \infty$	−14.4	V
Amplifier Supply Current	I_A		1	mA
Device Dissipation	P_D		30	mW
Common-Mode Rejection Ratio	CMRR		110	dB
Common-Mode Input-Voltage Range	V_{CMR}		13.6 to −14.6	V
Input Resistance	R_I		26	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only For Design Guidance CA3080

Characteristic	Symbol	Test Conditions	CA3080	Units
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\mu A$	0.3	mV
Input Offset Voltage Change	$\mid \Delta V_{IO} \mid$	Change in V_{IO} between $I_{ABC} = 500\mu A$ and $I_{ABC} = 5\mu A$	0.2	mV
Peak Output Current	I_{OM}	$I_{ABC} = 5\mu A$	5	μA
Peak Output Voltage: Positive	V^+_{OM}	$I_{ABC} = 5\mu A$	13.8	V
Peak Output Voltage: Negative	V^-_{OM}	$I_{ABC} = 5\mu A$	−14.5	V
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36V$	0.3	nA
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4V$	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate: Maximum (uncompensated)	SR	–	75	V/μs
Slew Rate: Unity Gain (compensated)	SR	–	50	V/μs
Open-Loop Bandwidth	BW_{OL}	–	2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF

ELECTRICAL CHARACTERISTICS
For Equipment Design — **CA3080A**

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS $V^+ = 15\,V$, $V^- = -15\,V$, $I_{ABC} = 500\,\mu A$, $T_A = 25^oC$ (unless indicated otherwise)	LIMITS Typ.	UNITS
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\,\mu A$	0.3	mV
			0.4	
Input Offset Voltage Change	$\lvert \Delta V_{IO} \rvert$	Change in V_{IO} between $I_{ABC} = 500\,\mu A$ and $I_{ABC} = 5\,\mu A$	0.1	mV
Input Offset Current	I_{IO}		0.12	μA
Input Bias Current	I_I		2	μA
Forward Transconductance (large signal)	g_m		9600	μmho
Peak Output Current	$\lvert I_{OM} \rvert$	$I_{ABC} = 5\,\mu A$, $R_L = 0$	5	μA
		$R_L = 0$	500	
Peak Output Voltage: Positive	V^+_{OM}	$I_{ABC} = 5\,\mu A$	13.8	V
Negative	V^-_{OM}	$R_L = \infty$	−14.5	
Positive	V^+_{OM}	$R_L = \infty$	13.5	
Negative	V^-_{OM}		−14.4	
Amplifier Supply Current	I_A		1	mA
Device Dissipation	P_D		30	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$		–	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36\,V$	0.3	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4\,V$	0.008	nA
Common-Mode Rejection Ratio	CMRR		110	dB
Common-Mode Input-Voltage Range	V_{CMR}		13.6 to − 14.6	V
Input Resistance	R_I		26	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Ony For Design Guidance — **CA3080A**

Characteristics	Symbols	Test Conditions	Typ.	Units
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate: Maximum (uncompensated)	SR		75	V/μs
Unity Gain (compensated)		—	50	
Open-Loop Bandwidth	BW_{OL}	–	2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF

Table I— Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +15$ V, $I_{ABC} = 0.5$ mA, $V^- = -15$ V		LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM			MAXIMUM			UNITS
				−55	+25	+125	−55	+25	+125	
Input Offset Voltage	V_{IO}		CA3080	–	–	–	6	5	6	mV
			CA3080A	–	–	–	5	2	5	
Input Offset Current	I_{IO}		CA3080	–	–	–	1.2	0.6	0.7	μA
			CA3080A	–	–	–	1.2	0.6	0.7	
Input Bias Current	I_I		CA3080	–	–	–	8	5	8	μA
			CA3080A	–	–	–	8	5	8	
Forward Transconductance	g_m		CA3080	5400	6700	5400	13000	13000	20000	umho
			CA3080A	4000	7700	4000	9000	12000	18000	
Peak Output Voltage Positive	$+V_{OM}$	$R_L = \infty$	CA3080, CA3080A	11.6	12	12	–	–	–	V
Peak Output Voltage Negative	$-V_{OM}$	$R_L = \infty$	CA3080, CA3080A	11.8	12	12	–	–	–	
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	CA3080	350	350	320	750	650	750	μA
			CA3080A	350	350	320	750	650	750	
Amplifier Supply Current	I_A		CA3080	0.7	0.8	0.7	1.4	1.2	1.4	mA
			CA3080A	0.7	0.8	0.7	1.4	1.2	1.4	
Common-Mode Rejection Ratio	C_{MRR}		CA3080	80	80	80	–	–	–	dB
			CA3080A	80	80	80	–	–	–	
Supply Voltage Rejection Ratio	V_{RR}		CA3080	–	–	–	150	150	150	μV/V
			CA3080A	–	–	–	150	150	150	

Table II— Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^- = -15$ V, $V^+ = +15$ V, $I_{ABC} = 0.5$ mA		LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM			MAXIMUM			UNITS
				−55	+25	+125	−55	+25	+125	
Input Offset Voltage	V_{IO}		CA3080	–	–	–	6	5	6	mV
			CA3080A	–	–	–	5	2	5	
Input Offset Current	I_{IO}		CA3080	–	–	–	1.2	0.6	0.7	μA
			CA3080A	–	–	–	1.2	0.6	0.7	
Input Bias Current	I_I		CA3080	–	–	–	8	5	8	μA
			CA3080A	–	–	–	8	5	8	
Forward Transconductance	g_m		CA3080	5400	6700	5400	13000	13000	20000	umho
			CA3080A	4000	7700	4000	9000	12000	18000	
Peak Output Voltage Positive	$+V_{OM}$	$R_L = \infty$	CA3080, CA3080A	11.6	12	12	–	–	–	V
Peak Output Voltage Negative	$-V_{OM}$	$R_L = \infty$	CA3080, CA3080A	11.8	12	12	–	–	–	
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	CA3080	350	350	320	750	650	750	μA
			CA3080A	350	350	320	750	650	750	
Amplifier Supply Current	I_A		CA3080	0.7	0.8	0.7	1.4	1.2	1.4	mA
			CA3080A	0.7	0.8	0.7	1.4	1.2	1.4	
Common-Mode Rejection Ratio	C_{MRR}		CA3080	80	80	80	–	–	–	dB
			CA3080A	80	80	80	–	–	–	
Supply Voltage Rejection Ratio	V_{RR}		CA3080	–	–	–	150	150	150	μV/V
			CA3080A	–	–	–	150	150	150	
Differential Input Current		$I_{ABC} = 10$ mA, $V_{DIFF} = 4$ V	CA3080	–	–	–	–	7	–	nA
			CA3080A	–	–	–	–	5	–	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	CA3080	–	–	–	–	7	–	nA
			CA3080A	–	–	–	–	5	–	
		$I_{ABC} = 0$, $V_{TP} = 36$	CA3080	–	–	–	–	7	–	nA
			CA3080A	–	–	–	–	5	–	

*Table III– Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25° C V^+ = +15 V, V^- = −15 V I_{ABC} = 0.5 mA	LIMITS MIN.	MAX.	MAX. Δ	UNITS
Input Offset Voltage	V_{IO}	CA3080	–	5	±0.2	mV
		CA3080A	–	2	±0.15	
Input Offset Current	I_{IO}	CA3080	–	0.6	±0.05	μA
		CA3080A	–	0.6	±0.05	
Input Bias Current	I_I	CA3080	–	5	±0.25	μA
		CA3080A	–	5	±0.25	
Forward Transconductance	g_m	CA3080	6700	13000	±3000	umho
		CA3080A	7700	12000	±3000	

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 12.

Table IV– Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = +15 V, V^- = −15 V	LIMITS MIN.	MAX.	UNITS
Input Offset Voltage	V_{IO}	CA3080	–	6.5	mV
		CA3080A	–	5.5	
Input Offset Current	I_{IO}	CA3080	–	1.2	μA
		CA3080A	–	1.2	
Input Bias Current	I_I	CA3080	–	10	μA
		CA3080A	–	10	
Forward Transconductance to Terminal No. 1	g_m	CA3080	6500	14000	umho
		CA3080A	7000	13000	
Peak Output Current	$\lvert I_{OM} \rvert$	CA3080	300	700	μA
		CA3080A	300	700	
Peak Output Voltage	$+V_{OM}$	CA3080	11	–	V
		CA3080A	11	–	
	$-V_{OM}$	CA3080	−11	–	
		CA3080A	−11	–	

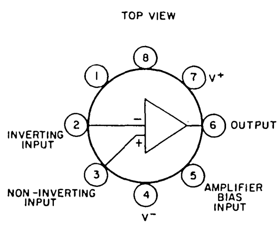


Fig. 2 – Functional diagram of CA3080 and CA3080A.

Typical Characteristics Curves for the CA3080 and CA3080A

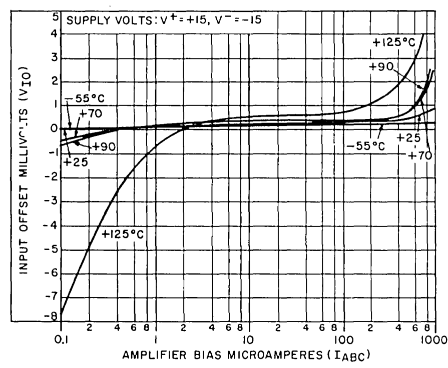


Fig. 3 – Input offset voltage vs. amplifier bias current.

Typical Characteristics Curves for the CA3080 and CA3080A (Cont'd.)

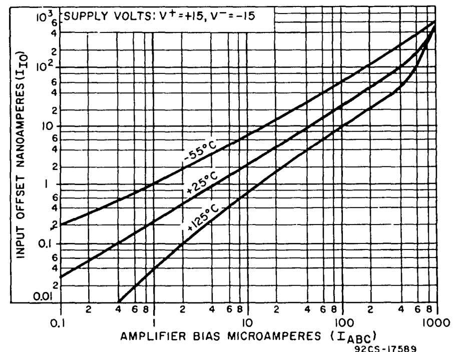


Fig. 4 — Input offset current vs. amplifier bias current.

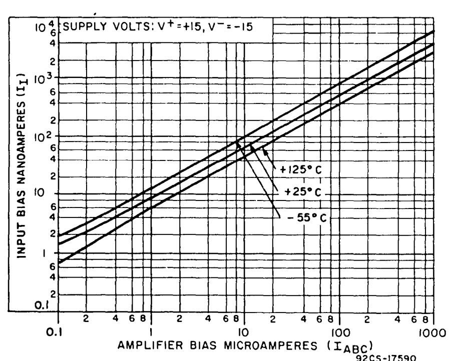


Fig. 5 — Input bias current vs. amplifier bias current.

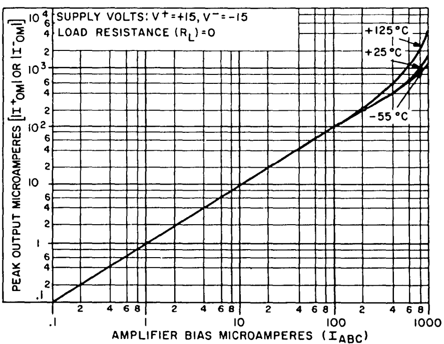


Fig. 6 — Peak output current vs. amplifier bias current.

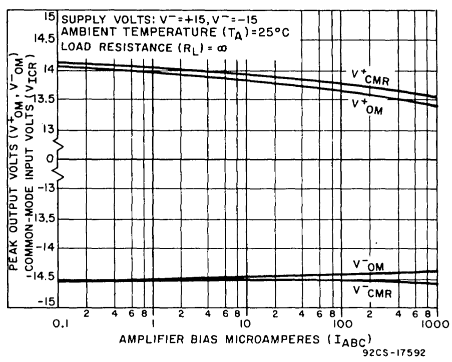


Fig. 7 — Peak output voltage vs. amplifier bias current.

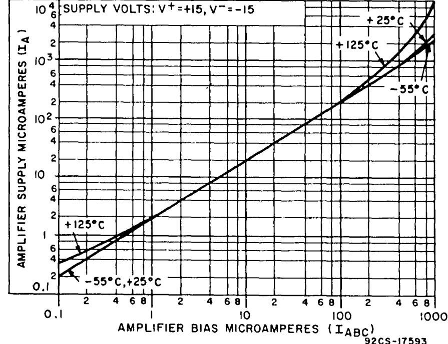


Fig. 8 — Amplifier supply current vs. amplifier bias current.

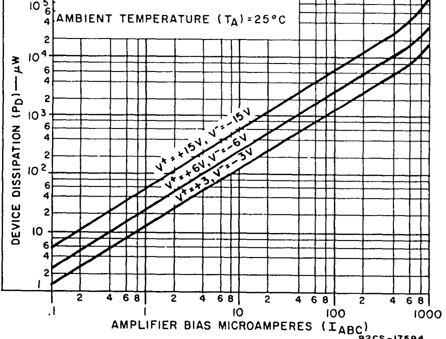
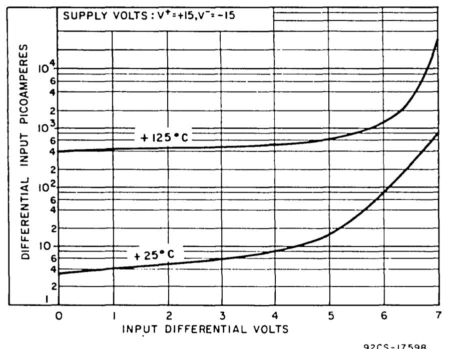


Fig. 9 — Total power dissipation vs. amplifier bias current.

Typical Characteristics Curves for CA3080 and CA3080A – Cont'd.



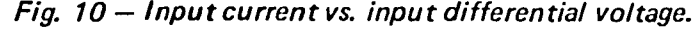


Fig. 10 – Input current vs. input differential voltage.

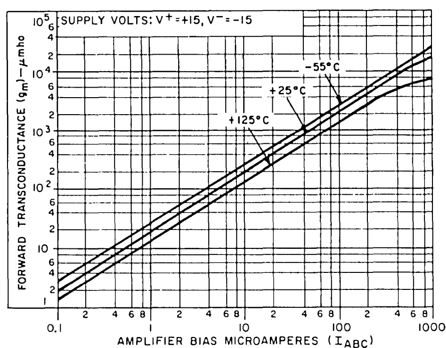


Fig. 11 – Transconductance vs. amplifier bias current.

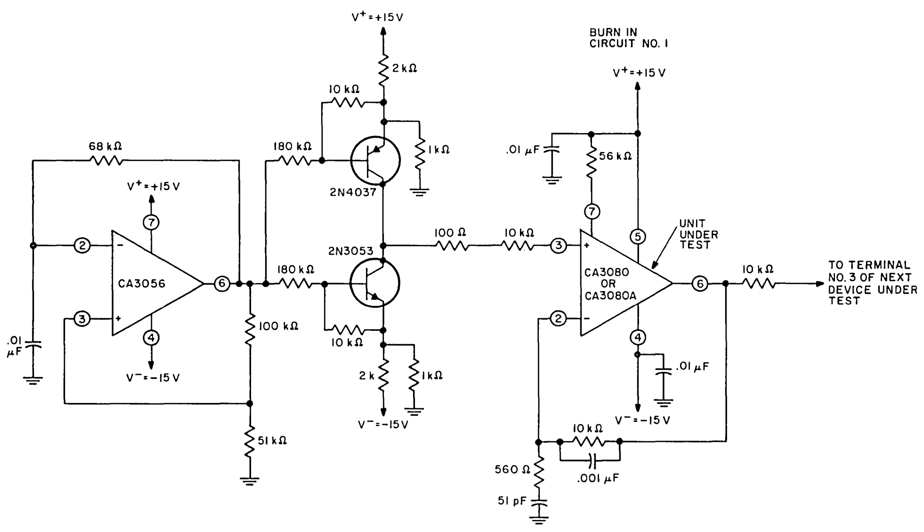


Fig. 12 – Burn-in and operating life test circuit.

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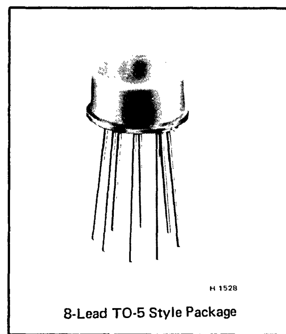
High-Reliability Slash(/) Series CA3085/..., CA3085A/..., CA3085B/...



8-Lead TO-5 Style Package

High-Reliability Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V at Currents up to 100 mA

For Application in Aerospace, Military and Critical Industrial Equipment

Features

- **Up to 100 mA output current**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.025%**
- **Pin compatible with LM100 Series**
- **Adjustable output voltage**

Applications

- **Shunt voltage regulator**
- **Current regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Combination positive and negative voltage regulator**
- **Dual tracking regulator**

RCA-CA3085, CA3085A, and CA3085B "Slash" (/) Series types are high-reliability linear integrated circuits designed specifically for voltage service as voltage regulators at output voltages ranging from 17 to 46 volts at currents up to 100 milliamperes. They are intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard types CA3085, CA3085A and CA3085B described in Data Bulletin File No. 491 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3085, CA3085A, and CA3085B Slash (/) Series type are supplied in the 8-lead TO-5 style package ("T" suffix) in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

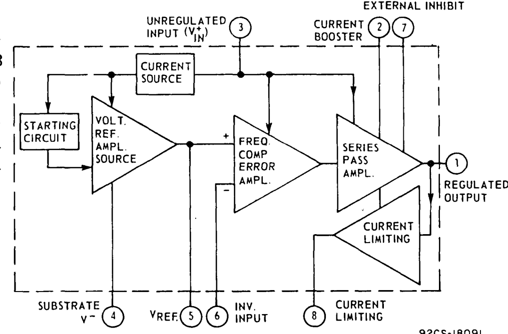


Fig.1—Block diagram of CA3085 Series. For schematic diagram see Fig.2.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

Power Dissipation:

Without Heat Sink		With Heat Sink	
up to T_A = 55°C	630 mW	up to T_C = 55°C	1.6 W
above T_A = 55°C	derate linearly @6.67 mW/°C	above T_C = 55°C	derate linearly at 16.7 mW/°C

Unregulated Input Voltage:

CA3085 . . . . 30 V
CA3085A . . . . 40 V
CA3085B . . . . 50 V

TEMPERATURE RANGE
Operating . . . . . . −55 to +125°C
Storage . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max. . . . .265°C

Maximum Voltage Ratings
The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERM-INAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	*	*	*	*	*	+10 0
6	–	–	*	*	*	*	*	*
7	–	–	–	+3 −10	+3 −10	*	*	+‡ 0
8	–	–	–	–	+5 −1	*	*	*
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERM-INAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

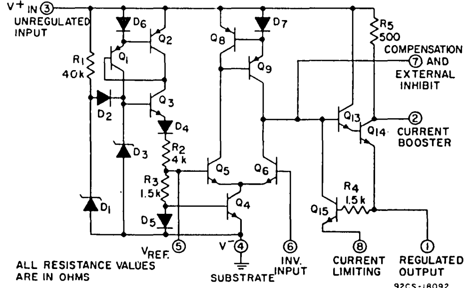


Fig.2—Schematic diagram of CA3085 Series.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$ [Unless indicated otherwise]		LIMITS CA3085 TYP.	CA3085A TYP.	CA3085B TYP.	UNITS
Reference Voltage	V_{REF}	$V^+_{IN} = 15V$		1.6	1.6	1.6	V
Quiescent Regulator Current	$I_{quiescent}$	$V^+_{IN} = 30V$		3.3	–	–	mA
		$V^+_{IN} = 40V$		–	3.65	–	
		$V^+_{IN} = 50V$		–	–	4.05	
Input Voltage Range	$V_{IN}(range)$	–		–	–	–	V
Maximum Output Voltage	$V_O(max.)$	$V^+_{IN} = 30, 40, 50V$#; $R_L = 365\,\Omega$; Term. No. 6 to Gnd.		27	37	47	V
Minimum Output Voltage	$V_O(min.)$	$V^+_{IN} = 30V$		1.6	1.6	1.6	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–		–	–	–	V
Limiting Current	I_{LIM}	$V^+_{IN} = 16V$, $V^+_{OUT} = 10V$ R_{SCP}* = $6\,\Omega$		96	96	96	mA
Load Regulation●	–	I_L = 1 to 100mA, $R_{SCP} = 0$		–	0.025	0.025	$\%V_{OUT}$
		I_L = 1 to 100mA, $R_{SCP} = 0$ $T_A = 0^oC$ to $+70^oC$		–	0.035	0.035	
		I_L = 1 to 12mA, $R_{SCP} = 0$		0.003	–	–	
Line Regulation▲	–	I_L = 1 mA, $R_{SCP} = 0$		0.025	0.025	0.025	%/V
		I_L = 1mA, $R_{SCP} = 0$ $T_A = 0^oC$ to $+70^oC$		0.04	0.04	0.04	
Equivalent Noise Output Voltage	V_{NOISE}	$V^+_{IN} = 25V$	$C_{REF} = 0$	0.5	0.5	0.5	mV p-p
			$C_{REF} = 0.22\mu F$	0.3	0.3	0.3	
Ripple Rejection	–	$V^+_{IN} = 25V$ f = 1kHz	$C_{REF} = 0$	50	50	50	dB
			$C_{REF} = 2\mu F$	56	56	56	
Output Resistance	r_o	$V^+_{IN} = 25V$, f = 1kHz		0.075	0.075	0.075	Ω
Temperature Coefficient of Reference and Output Voltages	ΔV_{REF}, ΔV_o	$I_L = 0$, $V_{REF} = 1.6V$		0.0035	0.0035	0.0035	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	$V^+_{IN} = 25V$, +50mA Step		1	1	1	μs
Turn Off	t_{OFF}	$V^+_{IN} = 25V$, –50mA Step		3	3	3	μs
Line Transient Recovery Time: Turn On	t_{ON}	$V^+_{IN} = 25V$, f = 1kHz, 2V Step		0.8	0.8	0.8	μs
Turn Off	t_{OFF}			0.4	0.4	0.4	μs

30 (CA3085), 40V(CA3085A), 50V(CA3085B)

* R_{SCP}: Short-circuit protection resistance

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{(V_{OUT(initial)})\ (\Delta V_{IN})} \times 100\%$

*Table I — Pre Burn-In and Post Burn-In Electrical Test and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $T_A = 25°C$	LIMITS MIN.	LIMITS MAX.	LIMITS MAX.	UNITS
Reference Voltage	V_{REF}	CA3085A, B	1.5	1.7	±0.05	V
		CA3085	1.4	1.8	±0.05	V
Output Voltage	$V_{O(min.)}$	V_{IN} +7.5 V or +50 CA3085B	–	1.7	±0.1	V
		V_{IN} +7.5 V or +40 V CA3085A	–	1.7	±0.1	V
		V_{IN} +7.5 V or +30 V CA3085	–	1.8	±0.1	V
	$V_{O(max.)}$	V_{IN} = 50 V CA3085/B	46	–	±0.5	V
		V_{IN} = 40 V CA3085/A	36	–	±0.5	V
		V_{IN} = 30 V CA3085	26	–	±0.5	V
Limiting Current	I_{LIM}	V_{IN}=7.5V R_{SCP}=7 Ω, R_L=10 Ω	–	115	±10	mA

* Levels/1N,/1R,/1, and/2 require pre and post burn-in electrical tests and delta limits
Level/3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 7.

Table II — Final Electrical Tests and Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM –55	MINIMUM +25	MINIMUM +125	MAXIMUM –55	MAXIMUM +25	MAXIMUM +125	UNITS
Reference Voltage	V_{REF}			1.4	1.4	1.3	1.9	1.8	1.8	V
Output Voltage Minimum Value	$V_{O(min.)}$	V_{IN} = 7.5V or 50V CA3085/B		–	–	–	1.8	1.7	1.7	V
		V_{IN} = 7.5V or 40V CA3085/A		–	–	–	1.8	1.7	1.7	V
		V_{IN} = 7.5 V or 30V CA3085		–	–	–	1.9	1.8	1.8	V
Maximum Value	$V_{O(max.)}$	V^+_{IN} = 30V, CA3085		25	26	24	–	–	–	
		V^+_{IN} = 40V, CA3085A		35	36	34	–	–	–	V
		V^+_{IN} = 50V, CA3085B		45	46	44	–	–	–	
Load Regulation		I_L = 1 to 100 mA	CA3085A	–	–	–	0.75	0.15	0.75	$\%/V_{OUT}$
		R_{SCP} = 0	CA3085B	–	–	–	0.75	0.15	0.75	$\%/V_{OUT}$
		I_L = 1 to 12 mA	CA3085	–	–	–	0.15	0.10	0.15	$\%/V_{OUT}$
Line Rgulation		I_L = 1 mA	CA3085	–	–	–	0.2	0.1	0.2	%/V
		R_{SCP} = 0	CA3085A	–	–	–	0.15	0.075	0.15	%/V
			CA3085B	–	–	–	0.12	0.04	0.12	%/V

Table III — Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Reference Voltage	V_{REF}			1.4	1.8	V
Minimum Output Voltage	$V_{O(min)}$	V^+_{IN} = 30 V, CA3085		–	1.9	V
		V^+_{IN} = 40 V, CA3085A		–	1.9	V
		V^+_{IN} = 50 V, CA3085B		–	2.0	V
Load Regulation		I_L = 1 to 100 mA	CA3085A	–	0.3	$\%/V_{OUT}$
		R_{SCP} = 0	CA3085B	–	0.75	
		I_L = 1 to 12 mA	CA3085	–	0.15	
Line Regulation		I_L = 1 mA	CA3085	–	0.25	%/V
		R_{SCP} = 0	CA3085A	–	0.1	
			CA3085B	–	0.05	

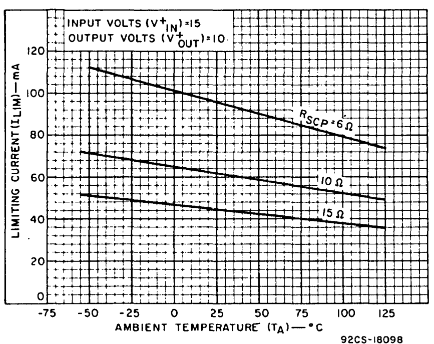


Fig. 3— I_{LIM} vs. T_A.

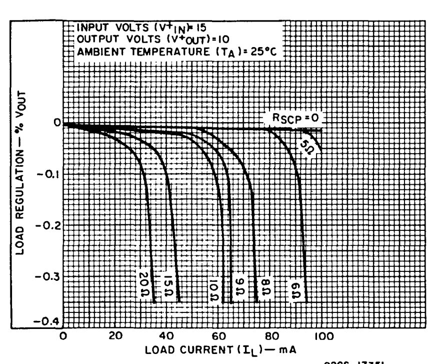


Fig. 4— Load regulation characteristics.

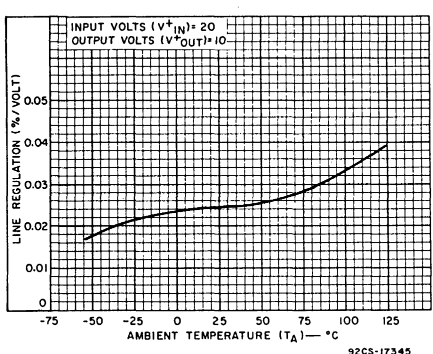


Fig. 5— Line regulation temperature characteristics.

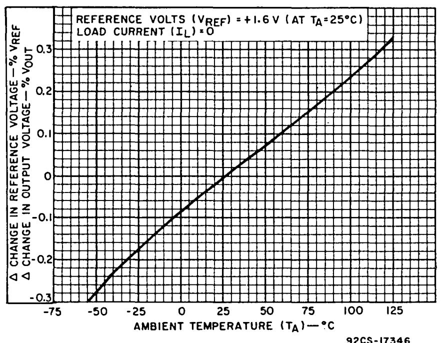


Fig. 6— Temperature coefficient of V_{REF} and V_{OUT}.

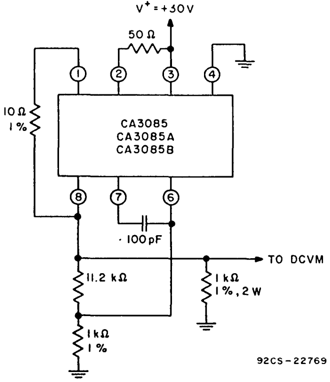


Fig. 7— Burn-in and operating life test circuit.

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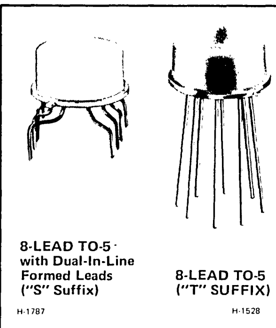
High-Reliability Slash (/) Series

CA3094/... CA3094A/... CA3094B/...



High-Reliability Programmable Power Switch/Amplifiers

For Control & General-Purpose Applications

In Aerospace, Military, and Critical Industrial Equipment

Features:

- Designed for *single* or dual power supply
- Programmable: strobing, gating, squelching, AGC capabilities
- Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)
- High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)
- Total harmonic distortion (THD) @ 0.6 W in class A operation — 1.4% typ.
- High current-handling capability — 100 mA (avg.), 300 mA (peak)
- Sensitivity controlled by varying bias current
- Output: "sink" or "drive" capability

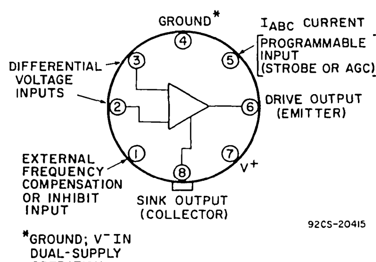
RCA-CA3094, CA3094A, and CA3094B "Slash" (/) Series are high-reliability linear integrated circuit differential-input power-control switch amplifiers with auxiliary circuit features for ease of programmability. They are intended for use in a variety of control and general-purpose applications for aerospace, military and industrial equipment. These devices are electrically and mechanically identical with standard types CA3094, CA3094A and CA3094B described in Data Bulletin File No. 598, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. The CA3094 is intended for operation up to 24 volts. The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

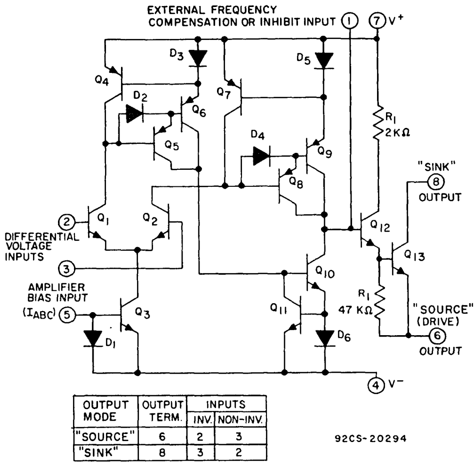
The CA3094, CA3094A, and CA3094B "Slash" (/) Series types are supplied in the 8-lead TO-5 style ceramic package ("T" Suffix), in 8-lead TO-5 style ceramic package with dual-in-line formed leads — ("S" Suffix DIL-CAN) — or in chip form ("H" Suffix).

Applications:

- Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor
- Over-current, over-voltage, over-temperature protectors
- Dual-tracking power supply with RCA-CA3085
- Wide-frequency-range oscillator
- Analog timer
- Level detector
- Alarm systems
- Voltage follower
- Ramp-voltage generator
- High-power comparator
- Ground-fault interrupter (GFI) circuits



Terminal Connections (Bottom View, Terminal End)



OUTPUT MODE	OUTPUT TERM.	INPUTS	
		INV.	NON-INV.
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig.1 – Schematic diagram of CA3094, CA3094A, and CA3094B Slash (/) Series Types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3094/Series	CA3094A/Series	CA3094B/Series	
DC Supply Voltage:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC Differential Input Voltage (Terminals 2 and 3)		± 5*		V
DC Common-Mode Input Voltage		Pin 4 ≤ Pins 2 & 3 ≤ Pin 7		
Peak Input Signal Current (Terminals 2 and 3)		± 1		mA
Peak Amplifier Bias Current (Terminal 5)		2		mA
Output Current:				
Peak		300		mA
Average		100		mA
Device Dissipation:				
Up to T_A = 55°C:				
Without heat sink		630		mW
With heat sink		1.6		W
Above T_A = 55°C:				
Without heat sink derate linearly		6.67		mW/°C
With heat sink derate linearly		16.7		mW/°C
Thermal Resistance (Junction to Air)		140		°C/W
Ambient Temperature Range:				
Operating		−55 to +125		°C
Storage		−65 to +150		°C
Lead Temperature (During Soldering): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.		+ 300		°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

ELECTRICAL CHARACTERISTICS $T_A = 25^oC$

Typical Values Intended Only for Design Guidance

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: Single Supply $V^+ = 30$ V, Dual Supply $V^+ = 15$ V, $V^- = 15$ V, $I_{ABC} = 100\ \mu A$ Unless Otherwise Specified	LIMITS Typ.	UNITS
INPUT PARAMETERS				
Input Offset Voltage	V_{IO}		0.4	mV
Input-Offset-Voltage Change	$\lvert \Delta V_{IO} \rvert$	Change in V_{IO} Between $I_{ABC} = 100\ \mu A$ and $I_{ABC} = 5\ \mu A$	1	mV
Input Offset Current	I_{IO}		0.02	μA
Input Bias Current	I_I		0.2	μA
Device Dissipation	P_D	$I_{out} = 0$	10	mW
Common-Mode Rejection Ratio	CMRR		110	dB
Common-Mode Input— Voltage Range	V_{CMR}	$V^+ = 30$ V High	28.8	V
		$V^+ = 30$ V Low	0.5	V
		$V^+ = 15$ V	+13.8	V
		$V^- = 15$ V	−14.5	V
Unity Gain-Bandwidth		$I_C = 7.5$ mA, $V_{CE} = 15$ V, $I_{ABC} = 500\ \mu A$	30	MHz
Open-Loop Bandwidth At −3 dB Point	BW_{OL}	$I_C = 7.5$ mA, $V_{CE} = 15$ V, $I_{ABC} = 500\ \mu A$	4	kHz
Total Harmonic Distortion (Class A Operation)	THD	$P_D = 220$ mW	0.4	%
		$P_D = 600$ mW	1.4	%
Amplifier Bias Voltage (Terminal (No.5 to Terminal No.4)	V_{ABC}		0.68	V
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$		4	$\mu V/^oC$
Power-Supply Rejection	$\Delta V_{IO}/\Delta V$		15	$\mu V/V$
1/F Noise Voltage	E_N	f = 10 Hz, $I_{ABC} = 50\ \mu A$	18	$nV/\sqrt{Hz}$
1/F Noise Current	I_N	f = 10 Hz, $I_{ABC} = 50\ \mu A$	1.8	$pA/\sqrt{Hz}$
Differential Input Resistance	R_I	$I_{ABC} = 20\ \mu A$	1	MΩ
Differential Input Capacitance	C_I	f = 1 MHz, $V^+ = 30$ V	2.6	pF

ELECTRICAL CHARACTERISTICS T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: Single Supply V^+ = 30 V, Dual Supply V^+ = 15 V, V^- = 15 V, I_{ABC} = 100 μA Unless Otherwise Specified	LIMITS Typ.	UNITS
OUTPUT PARAMETERS (Differential Input Voltage = 1 V)				
Peak Output Voltage: (Terminal No. 6) With Q13 "ON"	$+V_{OM}$	V^+ = 30 V, R_L = 2 kΩ to ground	27	V
With Q13 "OFF"	$-V_{OM}$		0.01	V
Peak Output Voltage: (Terminal No. 6) Positive	$+V_{OM}$	V^+ = +15 V, V^- = -15 V, R_L = 2 kΩ to −15 V	+12	V
Negative	$-V_{OM}$		−14.99	V
Peak Output Voltage: (Terminal No. 8) With Q13 "ON"	$+V_{OM}$	V^+ = 30 V, R_L = 2 kΩ to 30 V	29.99	V
With Q13 "OFF"	$-V_{OM}$		0.040	V
Peak Output Voltage: (Terminal No. 8) Positive	$+V_{OM}$	V^+ = 15 V, V^- = − 15 V, R_L = 2 kΩ to + 15 V	+14.99	V
Negative	$-V_{OM}$		14.96	V
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$	V^+ = 30 V, I_C = 50 mA, Terminal No.6 grounded	0.17	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)		V^+ = 30 V	2	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13})	h_{fe}	V^+ = 30 V, V_{CE} = 5 V, I_C = 50 mA	100,000	
Output Capacitance: Terminal No. 6	C_O	f = 1 MHz, All Remaining Terminals Tied to Terminal No. 4	5.5	pF
Terminal No. 8			17	pF
TRANSFER PARAMETERS				
Voltage Gain	A	V^+ = 30 V, I_{ABC} = 100 μA, ΔV_{out} = 20 V, R_L = 2 kΩ	100,000	V/V
			100	dB
Forward Transconductance To Terminal No. 1	g_m		2200	μmhos
Slew Rate: Open Loop: Positive Slope	SR	I_{ABC} = 500 μA, R_L = 2 kΩ	500	V/μs
Negative Slope			50	V/μs
Unity Gain (Non-Inverting, Compensated)		I_{ABC} = 500 μA, R_L = 2 kΩ	0.7	V/μs

Table I — Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits*

Characteristic	Symbol	Test Conditions $V^+ = 30$ V, $I_{ABC} = 100\ \mu A$, $T_A = 25^oC$	Limits Min.	Limits Max.	Limits Max.	Units
Input Offset Voltage	V_{IO}		–	5	±1	mV
Input Offset Current	I_{IO}		–	0.2	±0.02	μA
Input Bias Current	I_I		0.04	0.5	±0.1	μA
Forward Transconductance To Terminal No.1	g_m		1650	2750	±660	μmho
Collector-to-Emitter Saturation Voltage (Terminal No.8)	$V_{CE}(sat)$	$I_C = 50$ mA Terminal No.6 grounded	–	0.8	±0.02	V

* Levels /IN, /IR, /1, and /2 require pre and post burn-in electrical tests and delta limits.
Level /3 requires pre-burn in electrical test only. The burn-in circuit is shown in Fig. 13.

Table II — Final Electrical Tests

Characteristic	Symbol	Test Conditions $V^+ = 30$ V, $I_{ABC} = 100\ \mu A$ Unless Otherwise Specified	Limits For Indicated Temperatures (°C) Minimum −55	Minimum +25	Minimum +125	Maximum −55	Maximum +25	Maximum +125	Units
Input Offset Voltage	V_{IO}		–	–	–	7	5	7	mV
Input Offset Current	I_{IO}		–	–	–	0.85	0.2	0.22	μA
Input Bias Current	I_I		–	–	–	3.2	0.5	1.1	μA
Forward Transconductance To Terminal No. 1	g_m		910	1650	1850	2100	2750	4000	μmho
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	Change in V_{IO} between $I_{ABC} = 100\ \mu A$ and $I_{ABC} = 5\ \mu A$	–	–	–	–	8	–	mV
		Change in V_{IO} between $I_{ABC} = 100\ \mu A$ and $I_{ABC} = 15\ \mu A$	–	–	–	3.2	–	3.2	mV
Peak Output Voltage (Terminal No.6) with Q_{13} "ON"	V^+_{OM}	$R_L = 2\ k\Omega$ to ground	26	26	26	–	–	–	V
Common Mode Rejection Ratio	CMRR		70	70	70	–	–	–	dB
Supply Current	I^+_{Supply}		–	–	–	400	400	400	μA
Power Supply Rejection	$\Delta V_{IO}/\Delta V$		–	–	–	150	150	150	μV/V
Power Dissipation	P_D	$I_{OM} = 0$	–	8	–	–	12	–	mW
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE}(sat)$	$I_C = 50$ mA Terminal No.6 Grounded	–	–	–	0.8	0.8	1.0	V

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No. 8) and the "Drive" Output (terminal No. 6) of the CA3094T are not inherently current (or power) limited. Therefore, if a load is connected between terminal No. 6 and terminal No. 4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No. 7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No. 8 and terminal No. 7, the current-limiting resistor should be connected between terminal 6 and terminal No. 4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No. 7 and the V^+ supply.

Table III – Group A Electrical Sampling Inspection

Characteristic	Symbol	Test Conditions $V^+ = 30$ V, $I_{ABC} = 100\ \mu A$ Unless Otherwise Specified	Limits For Indicated Temperatures (°C) Minimum –55	Minimum +25	Minimum +125	Maximum –55	Maximum +25	Maximum +125	Units
Input Offset Voltage	V_{IO}		–	–	–	7	5	7	mV
Input Offset Current	I_{IO}		–	–	–	0.85	0.2	0.22	μA
Input Bias Current	I_I		–	–	–	3.2	0.5	1.1	μA
Forward Transconductance To Terminal No. 1	g_m		910	1650	1850	2100	2750	4000	μmho
Input Offset Voltage Change	$\|\Delta V_{IO}\|$	Change in V_{IO} between $I_{ABC} = 100\ \mu A$ and $I_{ABC} = 5\ \mu A$	–	–	–	–	8	–	mV
		Change in V_{IO} between $I_{ABC} = 100\ \mu A$ and $I_{ABC} = 15\ \mu A$	–	–	–	3.2	–	3.2	mV
Peak Output Voltage (Terminal No.6) with Q_{13} "ON"	V^+_{OM}	$R_L = 2\ k\Omega$ to ground	26	26	26	–	–	–	V
Common Mode Rejection Ratio	CMRR		70	70	70	–	–	–	dB
Supply Current	I^+_{Supply}		–	–	–	400	400	400	μA
Power Supply Rejection	$\Delta V_{IO}/\Delta V$		–	–	–	150	150	150	μV/V
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$	$I_C = 50$ mA Terminal No.6 Grounded	–	–	–	0.8	0.8	1.0	V
Output Leakage Current Q_{13} "OFF"	$-I_{OL}$	$V^+ = 25$ V	–10	–10	–10	0.1	0.1	0.1	μA
Max. Output Current Q_{13} "ON"	$-I_{OM}$	$I_{ABC} = 15\ \mu A$	–140	–140	–140	–98	–98	–98	mA

Table IV – Group C Electrical Characteristics Sampling Tests ($T_A = 25°C$)

Characteristic	Symbol	TEST CONDITIONS $V^+ = 30$ V, $I_{ABC} = 100\ \mu A$ Unless Otherwise Specified	LIMITS Min.	LIMITS Max.	Units
Input Offset Voltage	V_{IO}		–	5	mV
Input Offset Current	I_{IO}		–	0.25	μA
Forward Transconductance to Terminal No. 1	g_m		1420	3350	μmho
Peak Output Voltage (Terminal No.6) with Q_{13} "ON"	$+V_{OM}$	$R_L = 2\ k\Omega$ to ground	25	–	V
Supply Current	I^+_{Supply}		–	400	μA
Output Leakage Current Q_{13} "OFF"	$-I_{OL}$	$V^+ = 25$ V	–15	–	μA
Max. Output Current Q_{13} "ON"	$-I_{OM}$	$I_{ABC} = 3\ \mu A$	–	–45	mA

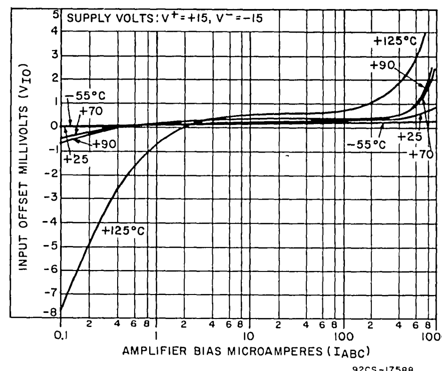


Fig.2 – Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

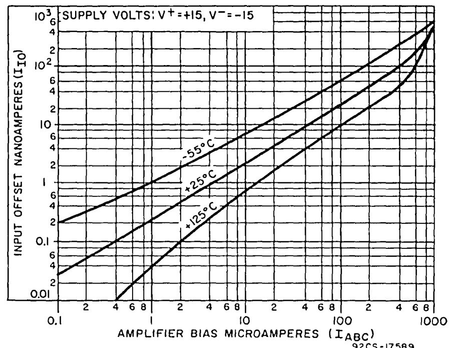


Fig.3 – Input offset current vs. amplifier bias current (I_{ABC}, terminal No.5).

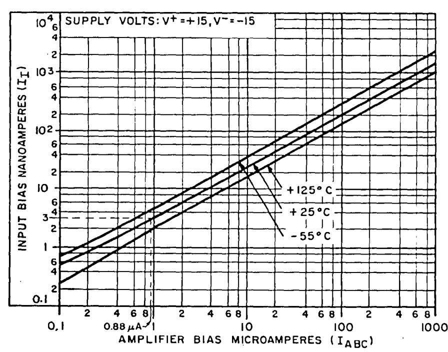


Fig.4 – Input bias current vs. amplifier bias current (I_{ABC}, terminal No.5).

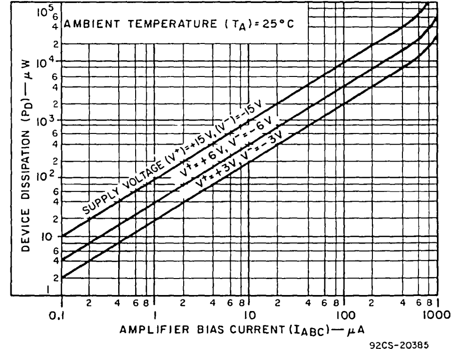


Fig.5 – Device dissipation vs. amplifier bias current (I_{ABC}, terminal No.5).

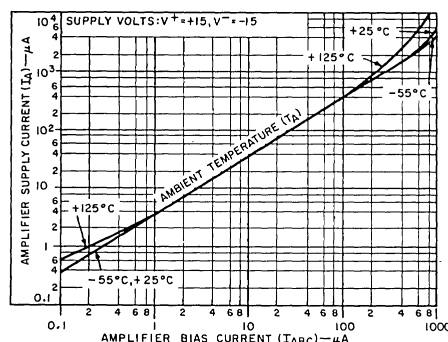


Fig.6 – Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No.5).

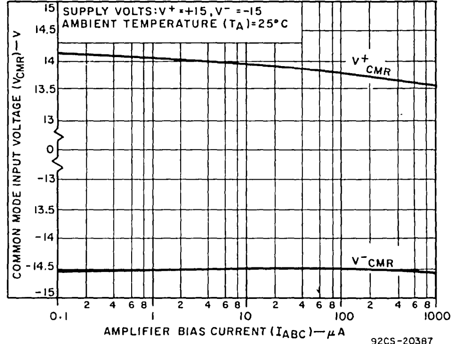


Fig.7 – Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

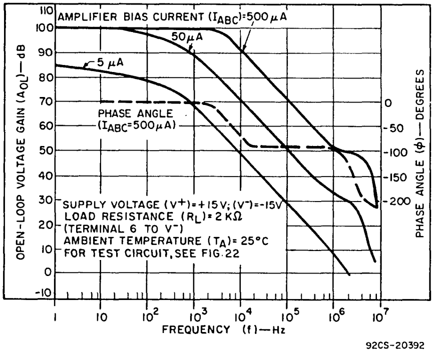


Fig. 8 — Open-loop voltage gain vs. frequency.

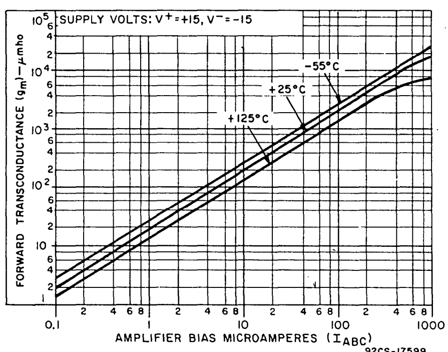


Fig. 9 — Forward transconductance vs. amplifier bias current.

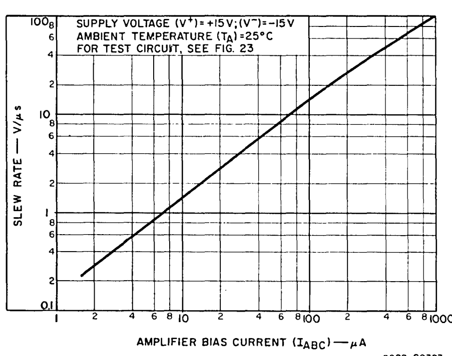


Fig. 10 — Slew rate vs. amplifier bias current.

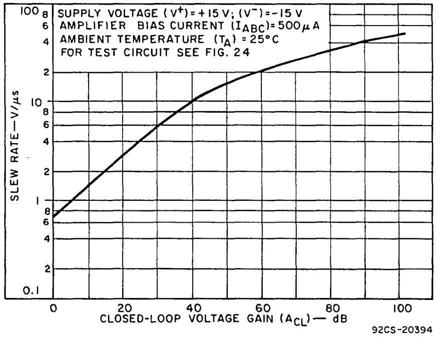


Fig. 11 — Slew rate vs. closed-loop voltage gain.

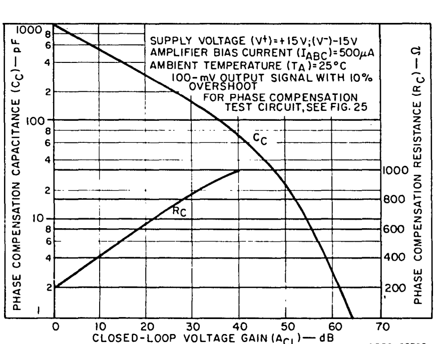


Fig. 12 — Phase compensation capacitance and resistance vs. closed-loop voltage gain.

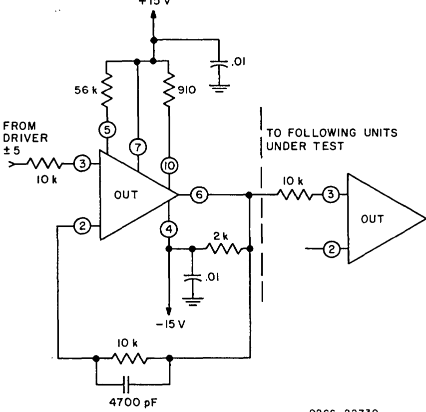


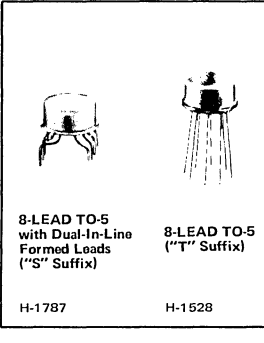
Fig. 13 — Burn-in and life-test circuit.

Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series CA3100/ . . .



High-Reliability Wideband Operational Amplifiers

For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **High unity-gain crossover frequency (f_T) – 38 MHz typ.**
- **Wide power Bandwidth – V_O = 18 V p-p typ. at 1.2 MHz**
- **High slew rate – 70 V/μs (typ.) in 20 dB amplifier**
  25 V/μs (typ.) in unity-gain amplifier
- **Fast settling time – 0.6 μs typ.**
- **High open-loop gain at video frequencies – 42 dB typ. at 1 MHz**
- **High output current – ±15 mA min.**
- **Single capacitor compensation**
- **LM118, 748/LM101 pin compatibility**
- **Offset null terminals**

The RCA-CA3100S, CA3100T Slash (/) Series types are high-reliability large-signal wideband, high-speed operational amplifiers intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard type CA3100 described in Data Bulletin File No. 625 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged type can be supplied to six screening levels – 1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /M, /N, and /R. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

The CA3100S and CA3100T have a unity gain crossover frequency (f_T) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. They can operate at a total supply voltage of from 14 to 36 volts (±7 to ±18 volts when using split supplies) and can provide at least 18 V p-p and 30 mA p-p at the output when operating from ±15 volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null.

The CA3100 circuit contains both bipolar and P-MOS transistors on a single monolithic chip.

The CA3100 is supplied in either the standard 8-lead TO-5 package (T suffix), in the 8-lead TO-5 dual-in-line formed-lead "DIL-CAN" package (S suffix), or in chip form (H suffix).

Applications:

- **Video amplifiers**
- **Fast peak detectors**
- **Meter-driver amplifiers**
- **Video pre-drivers**
- **Oscillators**
- **Multivibrators**
- **High-frequency feedback amplifiers**

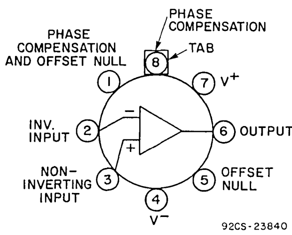


Fig. 1–Functional diagram of CA3100S, CA3100T.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage (between V^+ and V^- terminals)	36	V
Differential Input Voltage	±12	V
Input Voltage to Ground*	±15	V
Offset Terminal to V^- Terminal Voltage	±0.5	V
Output Current	50	mA●
Device Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C Derate Linearly at	6.67	mW/°C

Ambient Temperature Range:
Operating . . . . . −55 to +125°C
Storage . . . . . −65 to +150°C
Lead Temperature (During Soldering):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max. . . . . . 300 °C

* If supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage

● CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C: For Design Guidance*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15V UNLESS OTHERWISE SPECIFIED	TYP.	UNITS
STATIC				
Input Offset Voltage	V_{IO}	V_O = 0 ±0.1 V	±1	mV
Input Bias Current	I_{IB}	V_O = 0 ±1 V	0.7	μA
Input Offset Current	I_{IO}		±0.05	μA
Low-Frequency Open-Loop Voltage Gain●	A_{OL}	V_O = ± 1 V Peak, f = 1 kHz	61	dB
Common-Mode Input Voltage Range	V_{ICR}	CMRR ⩾ 76 dB	+14 −13	V
Common-Mode Rejection Ratio	CMRR	V_I Common Mode = ±12 V	90	dB
Maximum Output Voltage Positive	V_{OM}^+	Differential Input Voltage = 0 ±0.1 V	+11	V
Negative	V_{OM}^-	R_L = 2 KΩ	−11	
Maximum Output Current Positive	I_{OM}^+	Differential Input Voltage = 0 ±0.1 V	+30	mA
Negative	I_{OM}^-	R_L = 250 Ω	−30	
Supply Current	I^+	V_O = 0 ±0.1 V, R_L ⩾ 10 KΩ	8.5	mA
Power-Supply Rejection Ratio	PSRR	ΔV^+ = ± 1 V, ΔV^- = ± 1 V	70	dB
DYNAMIC				
Unit-Gain Crossover Frequency	f_T	C_C = 0, V_O = 0.3 V (P-P)	38	MHz
1-MHz Open-Loop Voltage Gain	A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	42	dB
Slew Rate: 20-dB Amplifier	SR	A_V = 10, C_C = 0, V_I = 1 V (Pulse)	70	V/μs
Follower Mode		A_V = 1, C_C = 10 pF, V_I = 10 V (Pulse)	25	
Power Bandwidth▲: 20-dB Amplifier	PBW	A_V = 10, C_C = 0, V_O = 18 V (P-P)	1.2	MHz
Follower Mode		A_V = 1, C_C = 10 pF, V_O = 18 V (P-P)	0.4	
Open-Loop Differential Input Impedance	Z_I	f = 1 MHz	30	KΩ
Open-Loop Output Impedance	Z_O	f = 1 MHz	110	Ω
Wideband Noise Voltage Referred to Input	e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	8	μV_{RMS}
Settling Time [To Within ±50 mV of 9 V Output Swing]	t_s	R_L = 2 KΩ, C_L = 20 pF	0.6	μs

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$

● Low-frequency dynamic characteristic

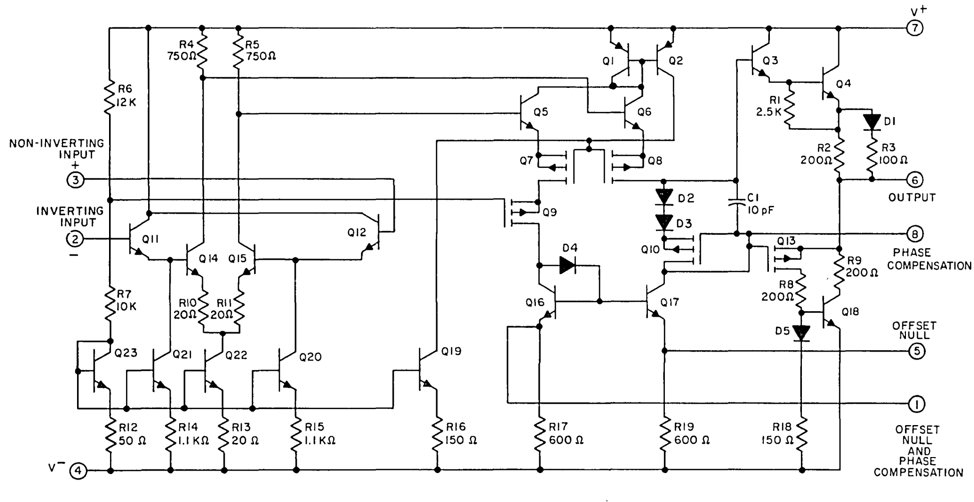


Fig. 2—Schematic diagram for CA3100.

Table I. Pre Burn-in Electrical and Post Burn-in Electrical Tests, and Delta Limits. ●

ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$, $V^+ = 15V$, $V^- = -15V$*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX.Δ	
Input Offset Voltage	V_{IO}	$V_O = 0 \pm 0.1$ V	–	5	±1	mV
Input Offset Current	I_{IO}	$V_O = 0 \pm 1V$	–	400	±40	nA
Input Bias Current	I_{IB}	$V_O = 0 \pm 1V$	–	2	±0.5	μA
Supply Current	I^+	$V_O = 0 \pm 1V$	–	10.5	±1.5	mA

● Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 9

Table II. Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15V UNLESS OTHERWISE SPECIFIED	LIMITS						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}	$V_O = 0 \pm 0.1$ V	–	–	–	6	5	6	mV
Input Bias Current	I_{IB}	$V_O = 0 \pm 1$ V	–	–	–	4	2	2	μA
Input Offset Current	I_{IO}		–	–	–	1000	400	600	nA
Low-Frequency Open-Loop Voltage Gain●	A_{OL}	$V_O = \pm 1$ V Peak	50	56	50	–	–	–	dB
Common-Mode Input Voltage Range	V_{ICR}	CMRR ≥ 76 dB	–	±12	–	–	–	–	V
Common-Mode Rejection Radio	CMRR	V_I Common Mode = ±12 V	–	76	–	–	–	–	dB
Maximum Output Voltage Positive	V_{OM}^+	Differential Input Voltage = 0 ± 0.1V	+9	+9	+9	–	–	–	V
Negative	V_{OM}^-	R_L = 2 KΩ	−9	−9	−9	–	–	–	
Maximum Output Current Positive	I_{OM}^+	Differential Input Voltage = 0 ±0.1V	+15	+15	+12	–	–	–	mA
Negative	I_{OM}^-	R_L = 250 Ω	−15	−15	−12	–	–	–	
Supply Current	I^+	$V_O = 0 \pm 0.1$ V, $R_L \geq 10$ KΩ	–	–	–	10.5	10.5	10.5	mA
Power Supply Rejection Ratio	PSRR	$\Delta V^+ = \pm 1$ V, $\Delta V^- = \pm 1$ V	60	60	60	–	–	–	dB
DYNAMIC									
1-MHz Open-Loop Voltage Gain	A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	–	36	–	–	–	–	dB
Slew Rate: 20-dB Amplifier	SR	A_V = 10, C_C=0, V_I = 1 V (Pulse)	–	50	–	–	–	–	V/μs
Power Bandwidth ▲: 20-dB Amplifier	PBW	A_V = 10, C_C = 0, V_O = 18 V (P-P)	–	0.8	–	–	–	–	MHz

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_{O\,(P\text{-}P)}}$ ● Low-frequency dynamic characteristic

Table III. Group C Electrical Characteristics Sampling Tests

T_A = +25°C V^+ = +15 V V^- = −15 V

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	V_{IO}	$V_O = 0 \pm 0.1$ V	–	5	mV
Input Offset Current	I_{IO}	$V_O = 0 \pm 0.1$ V	–	400	nA
Input Bias Current	I_I	$V_O = 0 \pm 0.1$ V	–	2	μA
Large-Signal Voltage Gain	A_{OL}	$V_O = \pm 1$V Peak	56	–	dB
Supply Current	I^+	$V_O = 0 \pm 0.1$ V	–	10.5	mA

TYPICAL CHARACTERISTICS CURVES

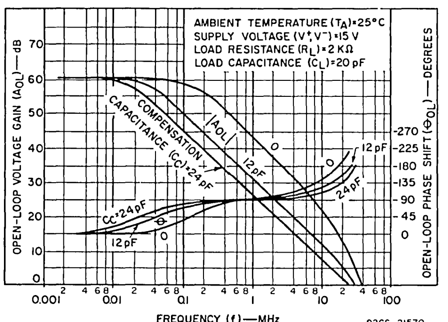


Fig. 3—Open-loop gain, open-loop phase shift vs. frequency.

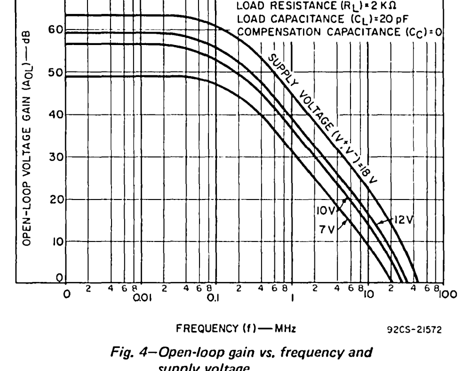


Fig. 4—Open-loop gain vs. frequency and supply voltage.

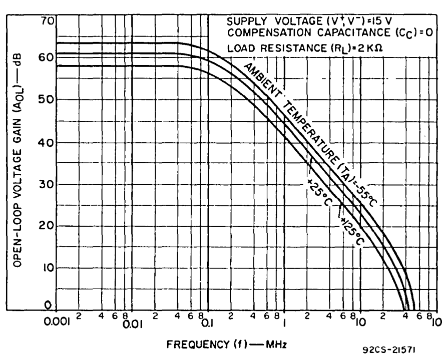


Fig. 5—Open-loop gain vs. frequency and temperature.

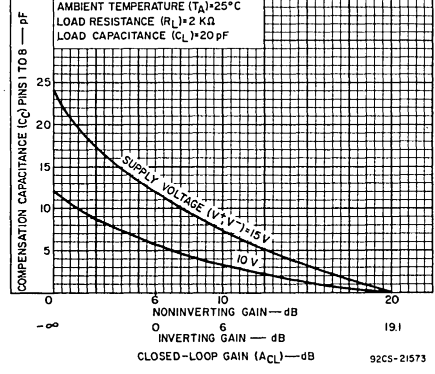


Fig. 6—Required compensation capacitance vs. closed-loop gain.

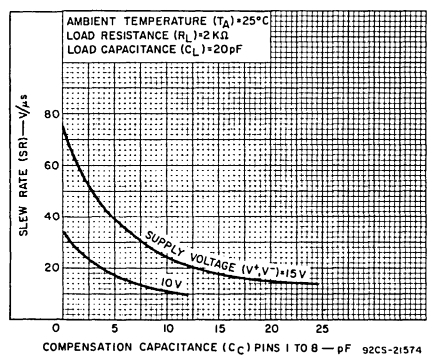


Fig. 7—Slew rate vs. compensation capacitance.

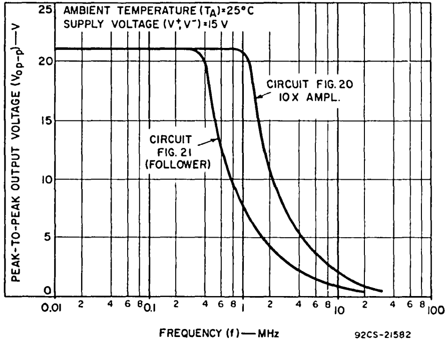


Fig. 8—Maximum output voltage swing vs. frequency.

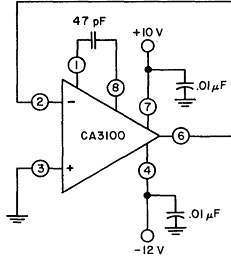


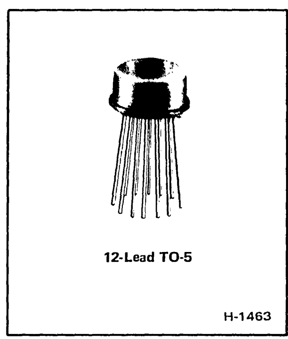
Fig. 9—Life test and burn-in circuit.

Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series CA3118/ . . ., CA3118A/ . . .



High-Reliability High-Voltage Transistor Arrays

For Applications in Aerospace, Military, and Critical Industrial Equipment

Applications:

- **General use in signal processing systems in DC through VHF range**
- **Custom designed differential amplifiers**
- **Temperature compensated amplifiers**

Features:

- **Matched general-purpose transistors**
- **V_{BE} matched ±5 mV max.**
- **Operation from DC to 120 MHz (CA3118AT, T).**
- **Low-noise figure: 3.2 dB typ. at 1 kHz (CA3118AT, T).**

The CA3118T and CA3118AT Slash (/) Series types are high-reliability, general-purpose silicon n-p-n transistor arrays on a common monolithic substrate. They are intended for applications in aerospace, military and industrial equipment. They are electrically and mechanically identical with the standard type CA3118 described in Data Bulletin File No. 532 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged type can be supplied to six screening levels — /1N, /1R, /1, /2, /3, and /4 — which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels — /M, /N, and /R. These screening levels and detailed information on test methods, procedures and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

Types CA3118AT and CA3118T consist of four transistors with two of the transistors connected in a Darlington configuration. These types are well suited for a wide variety of applications in low-power systems in the DC through VHF range. Both types are supplied in a hermetically sealed 12-lead TO-5 type package, ("T" suffix), and in chip form ("H" suffix), and operate over the full military temperature range. (CA3118AT and CA3118T are high-voltage versions of the popular predecessor type CA3018.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated Circuit Transistor Array."

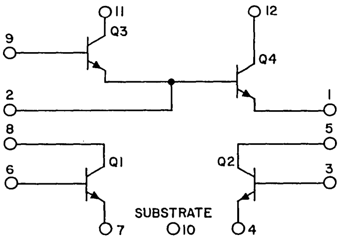


Fig. 1—Schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

POWER DISSIPATION:		
Any one transistor –		
CA3118AT, CA3118T	300	mW
Total package –		
Up to 85°C (CA3118AT, CA3118T)	450	mW
Above 85°C (CA3118AT, CA3118T)	derate linearly 5	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating –		
CA3118AT, CA3118T	–55 to +125	°C
Storage (all types)	–65 to +150	°C
THE FOLLOWING RATINGS APPLY FOR EACH TRANSISTOR IN THE DEVICE:		
Collector-to-Emitter Voltage (V_{CEO}):		
CA3118AT	40	V
CA3118T	30	V
Collector-to-Base Voltage (V_{CBO}):		
CA3118AT	50	V
CA3118T	40	V
Collector-to-Substrate Voltage (V_{CIO}):■		
CA3118AT	50	V
CA3118T	40	V
EMITTER-TO-BASE VOLTAGE (V_{EBO}) all types	5	V
Collector Current –		
CA3118AT, CA3118T	50	mA

■The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC ELECTRICAL CHARACTERISTICS For Design Guidance Only

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $T_A = 25°C$		Typ. Char. Curve Fig. No.	Typ. Values	UNITS
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10 \mu A, I_E = 0$		–	72	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA, I_B = 0$		–	56	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 10 \mu A, I_B = 0$, $I_E = 0$		–	72	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10 \mu A, I_C = 0$		–	7	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10 V, I_B = 0$		2	see curve	μA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10 V, I_E = 0$		3	0.002	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 5V$	$I_C = 10 mA$	4	85	
			$I_C = 1 mA$	4	100	
			$I_C = 10 \mu A$	4	90	
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V, I_C = 1 mA$		–	0.73	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	$I_C = 10mA, I_B = 1mA$		5	0.33	V
For transistors Q3 and Q4 (Darlington Configuration):						
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10 V, I_B = 0$		–	–	μA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 5V, I_C = 1 mA$		6	9000	
Base-to-Emitter (Q3 to Q4)	V_{BE}	$V_{CE} = 5V$	$I_E = 10 mA$	7	1.46	V
			$I_E = 1 mA$	7	1.32	
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	$V_{CE} = 5V, I_E = 1 mA$		–	4.4	mV/°C
For transistors Q1 and Q2 (As a Differential Amplifier):						
Magnitude of Input Offset Voltage $\lvert V_{BE1} - V_{BE2}\rvert$	$\lvert V_{IO}\rvert$	$V_{CE} = 5V, I_E = 1 mA$		–	0.48	mV
Magnitude of h_{FE}		$V_{CE} = 5V$, $I_{C1} = I_{C2} = 1mA$		–	1	
Magnitude of Base-to-Emitter Temprature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	$V_{CE} = 5V$, $I_E = 1mA$		–	1.9	mV/°C
Magnitude of V_{IO} ($V_{BE1} - V_{BE2}$) Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$	$V_{CE} = 5V$, $I_{C1} = I_{C2} = 1mA$		–	1.1	μV/°C

DYNAMIC ELECTRICAL CHARACTERISTICS For Design Guidance Only

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $T_A = 25^oC$	TEST CONDITIONS Typ. Char. Curve Fig. No.	CA3118T Typ.	CA3118AT Typ.	UNITS
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100 μA, Source resistance = kΩ		3.25	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: Forward-Current Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	8	100	100	
Short-Circuit Input Impedance	h_{ie}		8	3.5	2.7	kΩ
Open-circuit Output Impedance	h_{oe}		8	15.6	15.6	μmho
Open-Circuit Reverse Voltage Transfer Ratio	h_{re}		8	1.8 x 10^{-4}	1.8 x 10^{-4}	
Admittance Characteristics: Forward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	9	31-j1.5	31-j1.5	mmho
Input Admittance	Y_{ie}		10	0.3 + j0.04	0.35 + j0.04	mmho
Output Admittance	Y_{oe}		11	0.001 + j0.03	0.001 + j0.03	mmho
Reverse Transfer Admittance	Y_{re}		12	See curve	See curve	mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	13	500	500	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	14	0.70	0.70	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	14	0.37	0.37	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	14	2.2	2.2	pF

Table I. Pre Burn-In Electrical and Post Burn-In Electrical Tests and Delta Limits*

ELECTRICAL CHARACTERISTICS, *at $T_A = 25^oC$*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	LIMITS MAX△	UNITS
Emitter-to-Base Breakdown Volts Q1, Q2	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	–	±0.5	V
Collector Cutoff Current Q1, Q2	I_{CEO}	V_{CE} = 10 V, I_B = O	–	5	±1	μA
Collector Cutoff Current Q3, Q4	$I_{CEO(D)}$	V_{CE} = 10 V, I_B = O	–	5	±1	μA
Input Current Q1, Q2	I_I	I_C = 1 mA, V_{CE} = 5 V	–	33	±3	μA
Input Current Q3, Q4	$I_{I(D)}$	I_C = 1 mA, V_{CE} = 5 V	–	0.66	±0.1	μA
Base to Emitter Voltage Q1, Q2	V_{BE}	I_E = 1 mA, V_{CE} = 3 V	0.63	0.83	±0.1	V

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 15.

Table II Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS NOTE – Unless otherwise specified, limits apply to both CA3118 and CA3118A		LIMITS						UNITS
				MINIMUM			MAXIMUM			
				-55	+25	+125	-55	+25	+125	
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$	CA3118	–	40	–	–	–	–	V
			CA3118A	–	50	–	–	–	–	
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\ mA$, $I_B = 0$	CA3118	–	30	–	–	–	–	V
			CA3118A	–	40	–	–	–	–	
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 10\ \mu A$, $I_B = 0$, $I_E = 0$	CA3118	–	40	–	–	–	–	V
			CA3118A	–	50	–	–	–	–	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$		–	5	–	–	–	–	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10\ V$, $I_B = 0$		–	–	–	–	5	100	μA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10\ V$, $I_E = 0$		–	–	–	–	100	–	mA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 5\ V$, $I_C = 1\ mA$		15	30	40	–	–	–	·
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3\ V$, $I_C = 1\ mA$		.7	0.63	0.43	1.3	0.83	0.73	V
For transistors Q3 and Q4 (Darlington Configuration):										
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10\ V$, $I_B = 0$		–	–	–	–	5	2000	μA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 5\ V$, $I_C = 1\ mA$		750	1500	2000	–	–	–	
For transistors Q1 and Q2 (As a Differential Amplifier):										
Magnitude of Input Offset Voltage $\lvert V_{BE1} - V_{BE2} \rvert$	$\lvert V_{IO} \rvert$	$V_{CE} = 5\ V$, $I_E = 1\ mA$		–	–	–	–	5	–	mV
Magnitude of h_{FE}		$V_{CE} = 5\ V$, $I_{C1} = I_{C2} = 1\ mA$		–	0.9	–		1.1	–	
Dynamic Characteristics:										
Gain Bandwidth Product	f_T	$V_{CE} = 5\ V$, $I_C = 3\ mA$		–	300	–	–	–	–	MHz

Table III. Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Emitter-to-Base Breakdown Volts, Q_1, Q_2, Q_3, Q_4	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	4	–	V
Collector-to-Emitter Breakdown Volts, Q_1, Q_2, Q_3, Q_4	$V_{(BR)CEO}$	I_C = 1 mA, $I_B = 0$	28	–	V
Input Current, Q_1, Q_2	I_{IN}	I_C = 1 mA, V_{CE} = 5V	–	50	μA
Input Current, Darlington Pair, Q_3, Q_4	$I_{IN(D)}$	I_C = 1 mA, V_{CE} = 5V	–	1	μA
Base-to-Emitter Voltage, Q_1, Q_2	V_{BE}	I_E = 1 mA, V_{CE} = 3V	0.63	0.83	V

STATIC CHARACTERISTICS CURVES

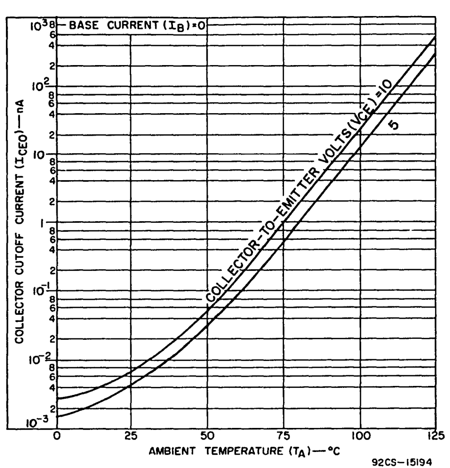


Fig. 2—I_{CEO} vs. T_A for any transistor.

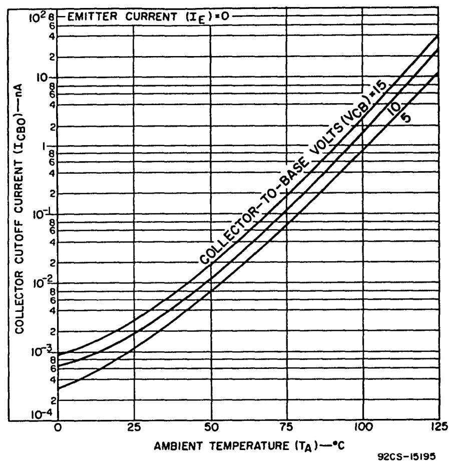


Fig. 3—I_{CBO} vs. T_A for any transistor.

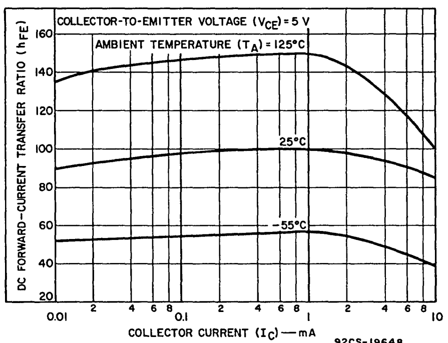


Fig. 4—h_{FE} vs. I_C for any transistor.

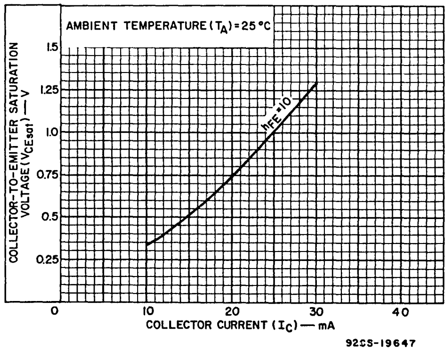


Fig. 5—V_{CE} sat vs. I_C for any transistor.

STATIC CHARACTERISTICS CURVES (Cont'd)

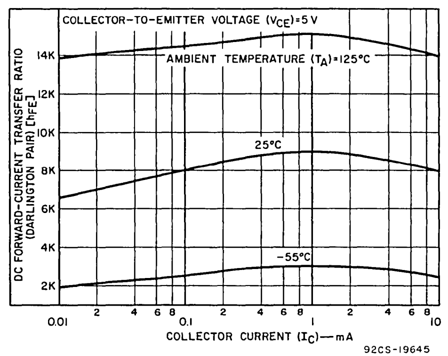


Fig. 6–h_{FE} vs. I_C for Darlington pair (Q3 and Q4) for types CA3118AT and CA3118T.

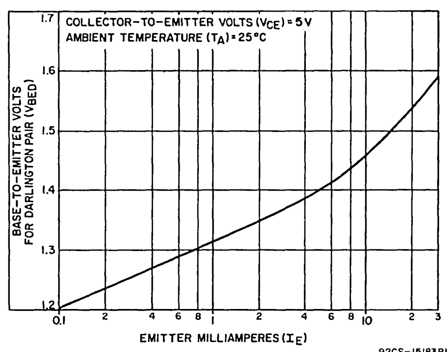


Fig. 7–V_{BE} vs. I_E for Darlington pair (Q3 and Q4).

TYPICAL DYNAMIC CHARACTERISTICS CURVES (For Any Transistor)

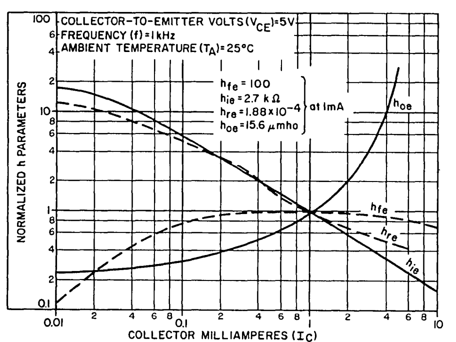


Fig. 8–h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

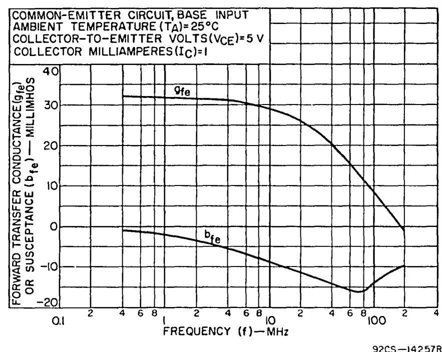


Fig. 9– y_{fe} vs. f.

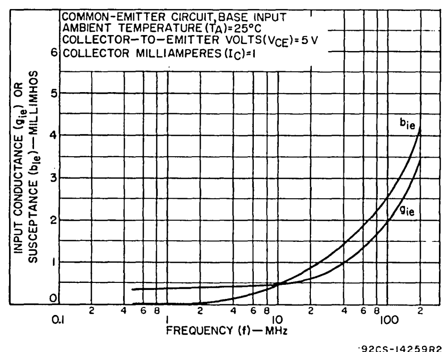


Fig. 10–y_{ie} vs. f.

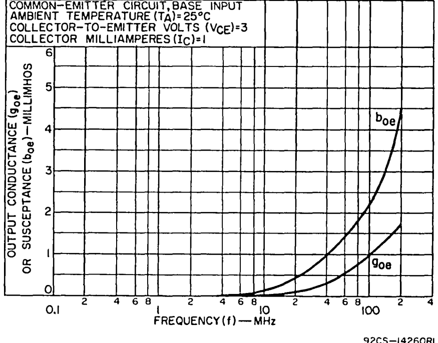


Fig. 11–y_{oe} vs. f.

TYPICAL DYNAMIC CHARACTERISTICS CURVES (Cont'd)

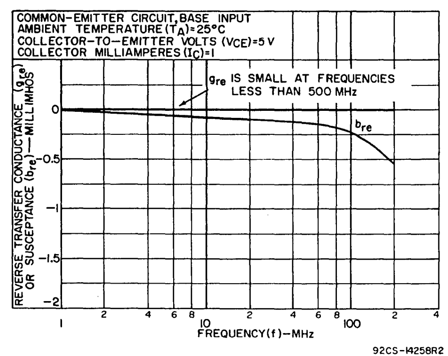


Fig. 12—y_{re} vs. f.

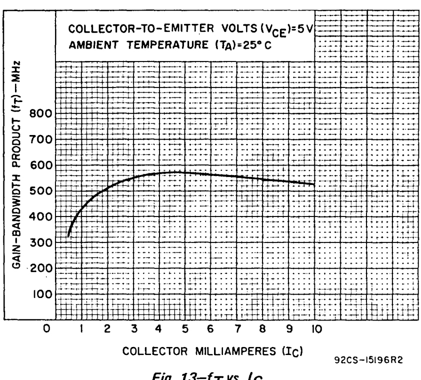


Fig. 13—f_T vs. I_C.

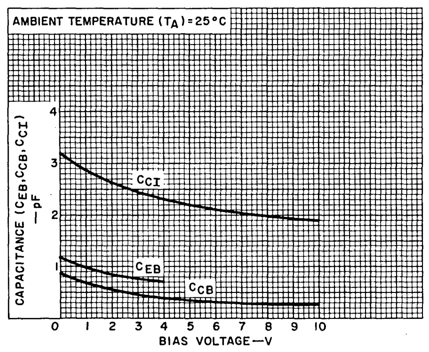


Fig. 14—C_{EB}, C_{CB}, C_{CI} vs. bias voltage.

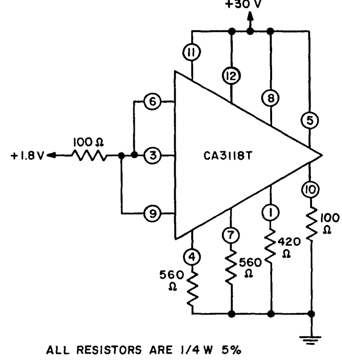


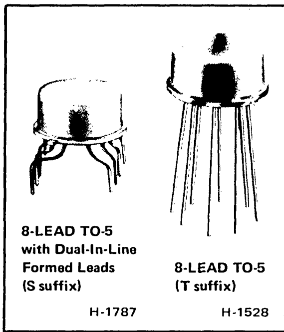
Fig. 15—Burn-in and operating life test circuit.

Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series CA3130A/ . . ., CA3130B/ . . .



High-Reliability COS/MOS Operational Amplifiers

With MOS/FET Input

For Aerospace, Military, and Critical Industrial Applications

Features:

- MOS/FET input stage provides:
  very high Z_I = 1.5 TΩ (1.5×10^{12} Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  2 pA typ. at 5 V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails

} Ideal for single-supply applications

- Low V_{IO}: 2 mV max. (CA3130B)
- Wide BW: 15 MHz typ. (unity-gain crossover)
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor

The RCA-CA3130A and CA3130B "Slash" (/) Series types are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip. Intended for applications in aerospace, military, and critical industrial equipment, they are electrically and mechanically identical with the standard types CA3130A and CA3130B described in Data Bulletin File No. 817 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/M, /N, and /R. These screening levels and detailed information on test methods, procedures, and test sequence are given in Reliability Report RIC-202A "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883."

The CA3130A and CA3130B Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators
  (ideal interface with digital COS/MOS)
- High-input-impedance wideband amplifiers
- Voltage followers
  (e.g., follower for single-supply D/A converter)
- Voltage regulators
  (permits control of output voltage down to zero volts)
- Peak detectors
- Single-supply full-wave precision rectifiers
- Photo-diode sensor amplifiers

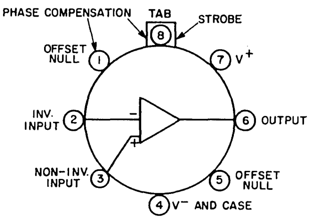


Fig. 1—Functional diagram of the CA3130 Series.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(BETWEEN V+ AND V− TERMINALS) .... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE .... ±8 V
COMMON-MODE DC INPUT VOLTAGE .... V+ to (V− -0.5 V)
INPUT-TERMINAL CURRENT .... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK–
UP TO 55°C .... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK–
AT 125°C .... 418 mW
BELOW 125°C .... Increase linearly at 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING .... −55 to +125°C
STORAGE .... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* .... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 SECONDS MAX. .... +265°C

*Short circuit may be applied to ground or to either supply.

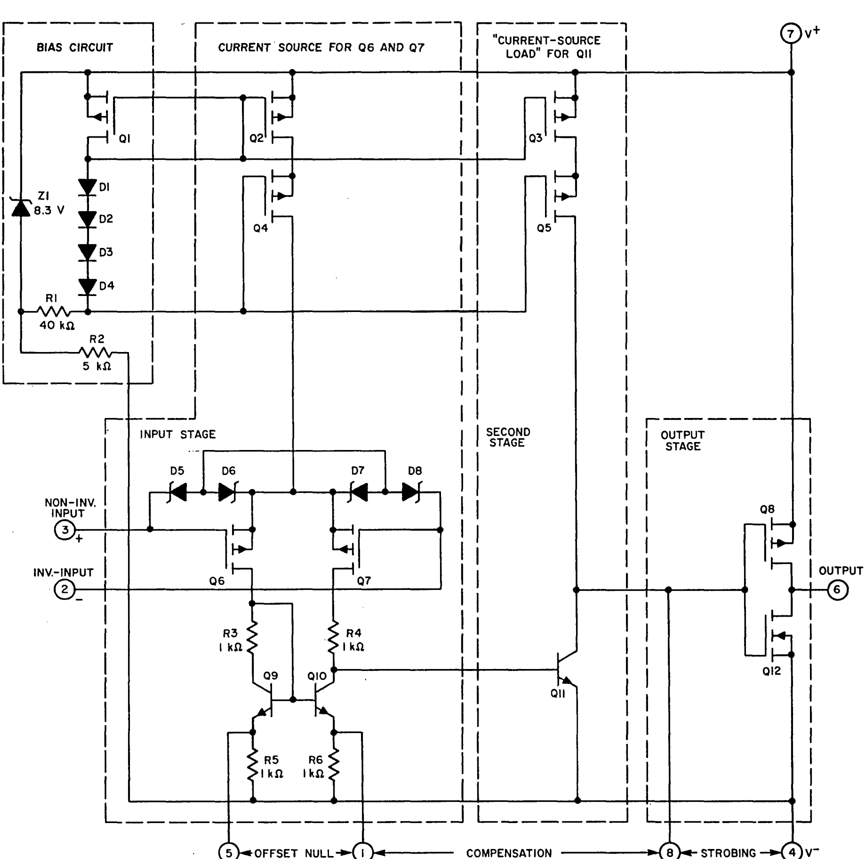


Fig. 2–Schematic diagram of the CA3130 Series.

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=15 V V^-=0 V T_A=25°C (Unless Specified Otherwise)	CA3130A	CA3130B	UNITS
Input Offset Voltage	$\lvert V_{IO} \rvert$	$V^{\pm}$=±7.5 V	2	0.8	mV
Input Offset Current	$\lvert I_{IO} \rvert$	$V^{\pm}$=±7.5 V	0.5	0.5	pA
Input Current	I_I	$V^{\pm}$=±7.5 V	5	5	pA
Large-Signal Voltage Gain	A_{OL}	V_O=10 $V_{p\text{-}p}$ R_L=2 kΩ	320 k	320 k	V/V
			110	110	dB
Common-Mode Rejection Ratio	CMRR		90	100	dB
Common-Mode Input-Voltage Range	V_{ICR}		−0.5 to 12	−0.5 to 12	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	$V^{\pm}$=±7.5 V	32	32	μV/V
	$\Delta V_{IO}/\Delta V^-$		32	32	
Maximum Output Voltage	V_{OM}^+	R_L=2 kΩ	13.3	13.3	V
	V_{OM}^-		0.002	0.002	
	$\lvert V_{OM}^+ \rvert$	R_L=∞	15	15	
	$\lvert V_{OM}^- \rvert$		0	0	
Maximum Output Current: Source	I_{OM}^+	V_O=0 V	22	22	mA
Sink	I_{OM}^-	V_O=15 V	20	20	
Supply Current	I^+	V_O=7.5 V R_L=∞	10	10	mA
		V_O=0 V R_L=∞	2	2	
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	T_A=−55 to 125°C $V^{\pm}$=±7.5 V ▲	10	5	μV/°C
Large-Signal Voltage Gain	A_{OL}	V_O=10 $V_{p\text{-}p}$ * R_L=2 kΩ *	320 k	320 k	V/V
			110	110	dB

* Applies only to A_{OL}.

▲ Applies only to $\Delta V_{IO}/\Delta T$.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=+7.5 V V^-=−7.5 V T_A=25°C (Unless Specified Otherwise)	CA3130A	CA3130B	UNITS
Input Offset Voltage Adjustment Range		10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	mV
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1 MHz	4.3	4.3	pF
Equivalent Input Noise	e_n	BW=0.2 MHz R_S=1 MΩ*	23	23	μV
Unity Gain Crossover Frequency	f_T	C_C = 0	15	15	MHz
		C_C = 47 pF	4	4	
Slew Rate: Open Loop	SR	C_C = 0	30	30	V/μs
Closed Loop		C_C = 56 pF	10	10	
Transient Response: Rise Time	t_r	C_C = 56 pF C_L = 25 pF R_L = 2 kΩ (Voltage Follower)	0.09	0.09	μs
Overshoot			10	10	%
Settling Time (4 Vp-p Input to <0.1%)			1.2	1.2	μs

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for sources of R_S up to 10 MΩ.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = 5 V V^- = 0 V T_A = 25°C (Unless Specified Otherwise)	CA3130A	CA3130B	UNITS
Input Offset Voltage	V_{IO}		2	1	mV
Input Offset Current	I_{IO}		0.1	0.1	pA
Input Current	I_I		2	2	pA
Common-Mode Rejection Ratio	CMRR		90	100	dB
Large-Signal Voltage Gain	A_{OL}	V_O = 4 Vp-p R_L = 5 kΩ	100 k	100 k	V/V
			100	100	dB
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current	I^+	V_O = 5 V, R_L = ∞	300	300	μA
		V_O=2.5 V, R_L = ∞	500	500	
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$		200	200	μV/V

Table I. Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*
ELECTRICAL CHARACTERISTICS At T_A = 25°C, V^+ = +7.5 V, V^- = −7.5 V

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	LIMITS		UNITS
				MAX.	MAX.Δ	
Input Offset Voltage	CA3130A	V_{IO}		5	±1	mV
	CA3130B			2	±0.5	
Input Offset Current	CA3130A	I_{IO}		20	±2	nA
	CA3130B			10	±1	
Input Bias Current	CA3130A	I_I		30	±3	nA
	CA3130B			20	±2	

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 6.

Table II. Final Electrical Tests and Group A Sampling Inspection

CHARACTERISTIC		SYMBOL	TEST CONDITIONS V^+ = +15 V, V^- = 0 V Unless Otherwise Specified	LIMITS						UNITS
				MINIMUM			MAXIMUM			
				−55	+25	+125	−55	+25	+125	
Input Offset Voltage	CA3130A	V_{IO}	$V^{\pm}$ = ±7.5 V	–	–	–	7	5	7	mV
	CA3130B			–	–	–	3.5	2	3.5	
Input Offset Current	CA3130A	I_{IO}	$V^{\pm}$ = ±7.5 V	–	–	–	30	20	30	pA
	CA3130B			–	–	–	20	10	20	
Input Current	CA3130A	I_I	$V^{\pm}$ = ±7.5 V	–	–	–	15	0.03	15	nA
	CA3130B			–	–	–	15	0.03	15	
Large Signal Voltage Gain	CA3130A	A_{OL}	V_O = 10 V_{p-p}	88	94	88	–	–	–	dB
	CA3130B		R_L = 2 kΩ	94	100	94	–	–	–	
Common-Mode Rejection Ratio	CA3130A	CMRR		80	80	80	–	–	–	dB
	CA3130B			86	86	86	–	–	–	
Common-Mode Input Voltage Range		V_{ICR}		0	0	0	10	10	10	V
Power Supply Rejection Ratio	CA3130A	PSRR	$V^{\pm}$ = ±7.5 V	150	150	150	–	–	–	μV/V
	CA3130B			100	100	100	–	–	–	
Maximum Output Voltage		V_{OM}^+	R_L = 2 kΩ	10	12	10	–	–	–	V
		V_{OM}^-		–	–	–	0.05	0.01	0.05	
Maximum Output Voltage		V_{OM}^+	R_L = ∞	14.95	14.99	14.95	–	–	–	V
		V_{OM}^-		–	–	–	0.05	0.01	0.05	
Maximum Output Current		I_{OM}^+	V_O = 0 V	–	12	–	–	45	–	mA
		I_{OM}^-	V_O = 15 V	–	12	–	–	45	–	
Supply Current		I^+	V_O = 25 V, R_L = ∞	–	–	–	–	15	–	mA
			V_O = 0 V, R_L = ∞	–	–	–	–	3	–	
Input Offset Voltage Temperature Coefficient		$\Delta V_{IO}/\Delta T$	CA3130B Only	–	–	–	15	15	15	μV/°C

Table III. Group C Electrical Characteristics Sampling Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25°C V^+ = +15 V, V^- = −15 V	LIMITS MIN.	LIMITS MAX.	UNITS
Input Offset Voltage	V_{IO}	CA3130A	–	5	mV
		CA3130B	–	2	
Input Offset Current	I_{IO}	CA3130A	–	20	pA
		CA3130B	–	10	
Input Bias Current	I_I	CA3130A	–	30	pA
		CA3130B	–	20	
Large Signal Voltage Gain	A_{OL}	CA3130A	91	–	dB
		CA3130B	97	–	

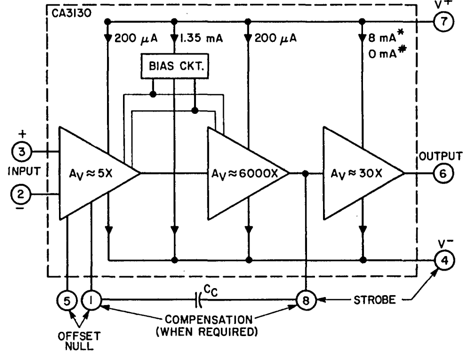


Fig. 3—Block diagram of the CA3130 Series.

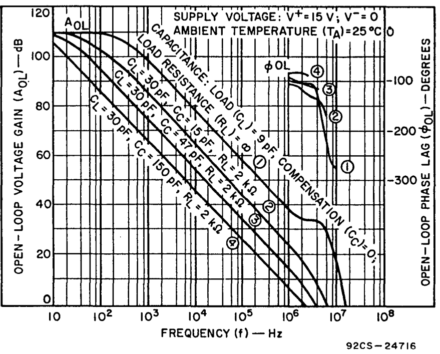


Fig. 4—Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

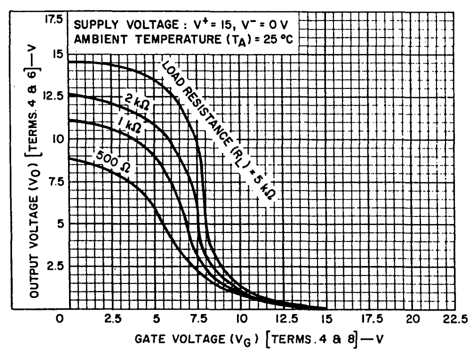


Fig. 5—Voltage transfer characteristics of COS/MOS output stage.

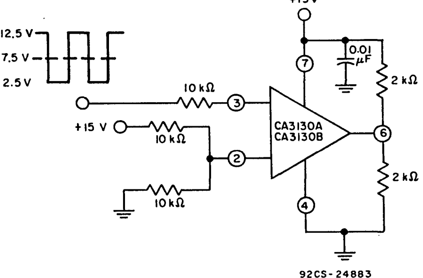


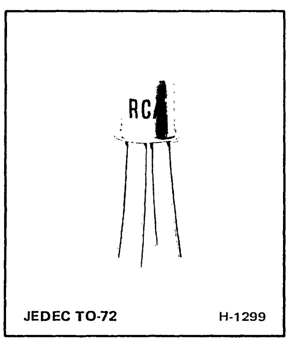
Fig. 6—Burn-in and life test circuit.

Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Types

High-Reliability Type
HR3N187



High-Reliability Silicon Dual Insulated-Gate Field-Effect Transistor

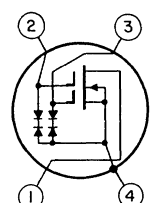
With Integrated Gate-Protection Circuits
For Applications in Aerospace, Military, and Critical Industrial Equipment up to 300 MHz

Device Features:

- **Back-to-back diodes to protect each gate against handling and in-circuit transients**
- **High forward transconductance – g_{FS} = 12,000 µmho (typ.)**
- **High unneutralized RF power gain – G_{ps} = 18 dB(typ.) at 200 MHz**
- **Low VHF noise figure – 3.5 dB(typ.) at 200 MHz**

The RCA-HR3N187 is a high-reliability n-channel silicon, depletion type, dual insulated-gate field-effect transistor. It is intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type 3N187 described in Data Bulletin File No. 436 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The excellent over-all performance characteristics of HR3N187 make it useful for a wide variety of rf-amplifier applications at frequencies up to 300 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element. The HR3N187 is hermetically sealed in the metal JEDEC TO-72 package.



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

Fig. 1—Terminal diagram.

Applications

- **RF amplifier amplifier, mixer, and IF amplifier in military, and industrial communications equipment**
- **Aircraft and marine vehicular receivers**
- **CATV and MATV equipment**
- **Telemetry and multiplex equipment**

Performance Features

- **Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's**
- **Wide dynamic range permits large-signal handling before overload**
- **Virtually no agc power required**
- **Greatly reduces spurious responses in FM receivers**

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} ...	–0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	–6 to +3	V
Peak ac	–6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	–6 to 30% of V_{DS}	V
Peak ac	–6 to +6	V
*DRAIN-TO-GATE VOLTAGE,		
V_{DG1} OR V_{DG2}	+20	V
*DRAIN CURRENT, I_D	50	mA
*TRANSISTOR DISSIPATION P_T:		
At ambient temperatures } up to 25°C	330	mW
At ambient temperatures } above 25°C	derate linearly at 2.2 mW/°C	
*AMBIENT TEMPERATURE RANGE:		
Storage and Operating	–65 to +175	°C
*LEAD TEMPERATURE (During Soldering):		
At distances ≥1/32 inch from seating surface for 10 seconds max.	265	°C

*In accordance with JEDEC Registration Data Format JS-9 RDF-19A

Electrical Characteristics, *at T_A = 25°C Unless Otherwise Specified*

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN.	TYP.	MAX.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		−0.5	−2	−4	V
*	Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		−0.5	−2	−4	V
*	Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V V_{G2S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
*	Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = −6 V V_{G2S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
*	Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V V_{G1S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
*	Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = −6 V V_{G1S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
*	Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V V_{G2S} = +4 V V_{G1S} = 0		5	15	30	mA
	Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz		7000	12,000	18,000	μmho
*	Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz		4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)♣	C_{rss}			0.005	0.02	0.08	pF
*	Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2.0	–	pF
	Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 200 MHz		15	18	22	dB
	Maximum Available Power Gain	MAG			–	20	–	dB
	Maximum Usable Power Gain (unneutralized)	MUG			–	20▲	–	dB
	Noise Figure (see Fig. 1)	NF			–	3.5	4.5	dB
*	Magnitude of Forward Transadmittance	$\|Y_{fs}\|$			–	12,000	–	μmho
*	Phase Angle of Forward Transadmittance				–	−35	–	Degrees
	Magnitude of Reverse Transadmittance	$\|Y_{rs}\|$			–	25	–	μmho
	Angle of Reverse Transadmittance	θ_{rs}			–	−25	–	Degrees
*	Input Resistance	r_{iss}			–	1.0	–	kΩ
*	Output Resistance	r_{oss}			–	2.8	–	kΩ
*	Gate-to-Source Forward Breakdown Voltage: Gate No. 1 / Gate No. 2	$V_{(BR)G1SSF}$ / $V_{(BR)G2SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA		6.5	10	–	V
*	Gate-to-Source Reverse Breakdown Voltage: Gate No. 1 / Gate No. 2	$V_{(BR)G1SSR}$ / $V_{(BR)G2SSR}$	I_{G1SSR} = I_{G2SSR} = −100 μA		−6.5	−10	–	V

▲ Limited only by practical design considerations.
† Capacitance between Gate No. 1 and all other terminals.
♣ Three-terminal measurement with Gate No. 2 and Source return to ground terminal.
* In accordance with JEDEC Registration Data Format JS-9 RDF-19A.

Table I—Pre Burn-In and Post Burn-In Electrical Go/No-Go Tests, at $T_A = 25^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Gate No. 1-Terminal Forward Current	I_{G1SSF}	$V_{G1S} = +6$ V, $V_{G2S} = V_{DS} = 0$	–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	$V_{G1S} = -6$ V, $V_{G2S} = V_{DS} = 0$	–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	$V_{G2S} = +6$ V, $V_{G1S} = V_{DS} = 0$	–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	$V_{G2S} = -6$ V, $V_{G1S} = V_{DS} = 0$	–	50	nA
Zero-Bias Drain Current	I_{DS}	$V_{DS} = +15$ V, $V_{G2S} = +4$ V $V_{G1S} = 0$	5	30	mA
Gate-to-Source Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	$I_{G1SSF} = I_{G2SSF} = 100\ \mu A$	6.5	–	V
Gate No. 2	$V_{(BR)G2SSF}$				
Gate-to-Source Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	$I_{G1SSR} = I_{G2SSR} = 100\ \mu A$	-6.5	–	V
Gate No. 2	$V_{(BR)G2SSR}$				

Table II—Final Electrical Tests, *at $T_A = 25°C$*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	$V_{DS} = +15$ V, $I_D = 50\ \mu A$ $V_{G2S} = +4$ V	-0.5	-4	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	$V_{DS} = +15$ V, $I_D = 50\ \mu A$ $V_{G1S} = 0$	-0.5	-4	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	$V_{G1S} = +6$ V, $V_{G2S} = V_{DS} = 0$	–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	$V_{G1S} = -6$ V, $V_{G2S} = V_{DS} = 0$	–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	$V_{G2S} = +6$ V, $V_{G1S} = V_{DS} = 0$	–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	$V_{G2S} = -6$ V, $V_{G1S} = V_{DS} = 0$	–	50	nA
Zero-Bias Drain Current	I_{DS}	$V_{DS} = +15$ V, $V_{G2S} = +4$ V $V_{G1S} = 0$	5	30	mA
Gate-to-Source Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	$I_{G1SSF} = I_{G2SSF} = 100\ \mu A$	6.5	–	V
Gate No. 2	$V_{(BR)G2SSF}$				
Gate-to-Source Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	$I_{G1SSR} = I_{G2SSR} = 100\ \mu A$	-6.5	–	V
Gate No. 2	$V_{(BR)G2SSR}$				

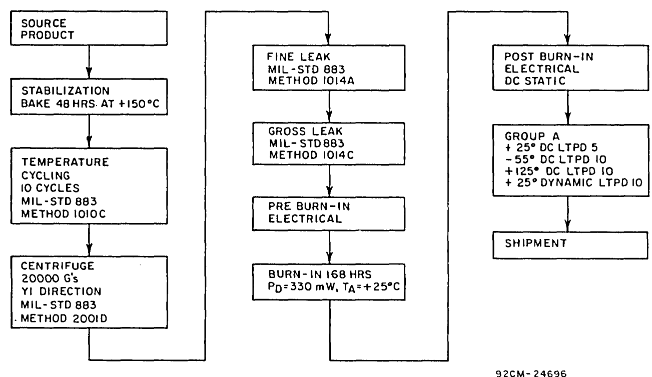
Table III – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			MINIMUM			MAXIMUM			
			-55	+25	+125	-55	+25	+125	°C
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G2S} = +4 V	-0.5	-0.5	–	-4	-4	–	V
		V_{DS} = +15 V, I_D = 100 μA, V_{G2S} = +4 V	–	–	0.5	–	–	-4	
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G1S} = +4 V	-0.5	-0.5	–	-4	-4	–	V
		V_{DS} = +15 V, I_D = 100 μA, V_{G1S} = +4 V	–	–	-0.5	–	–	-4	
Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +6 V, V_{G2S} = V_{DS} = 0	–	–	–	–	50	–	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V, V_{G2S} = V_{DS} = 0	–	–	–	–	50	–	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V, V_{G1S} = V_{DS} = 0	–	–	–	–	50	–	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V, V_{G1S} = V_{DS} = 0	–	–	–	–	50	–	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G2S} = +4 V, V_{G1S} = 0	5	5	3.5	30	30	21	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 kHz	–	7000	–	–	18,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance	C_{iss}		–	4.0	–	–	8.5	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)	C_{rss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 MHz	–	0.05	–	–	0.03	–	pF
Gate-to-Source Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	6.5	6.5	4.5	–	–	–	V
Gate No. 2	$V_{(BR)G2SSF}$								
Gate-to-Source Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	-6.5	-6.5	-4.5	–	–	–	V
Gate No. 2	$V_{(BR)G2SSR}$								

TYPICAL CHARACTERISTICS

For Y Parameters, see 3N187 Data Bulletin File No. 436

High-Reliability Processing Flow Chart



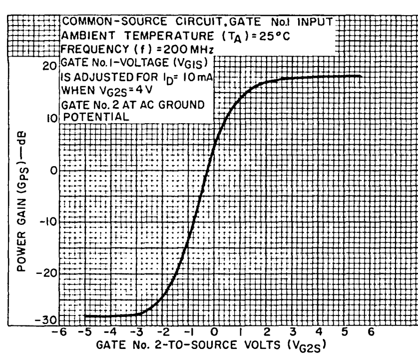


Fig. 2– G_{PS} vs. V_{G2S}.

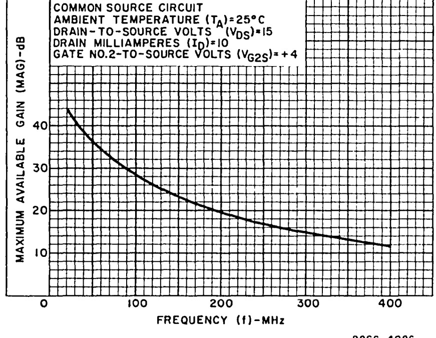


Fig. 3– MAG vs. f.

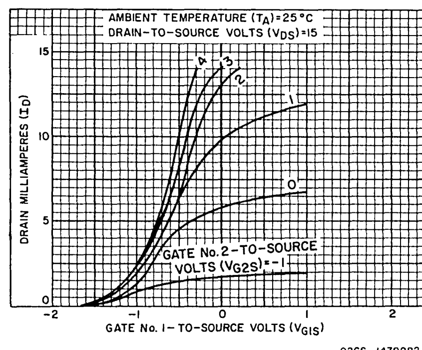


Fig. 4– I_D vs. V_{G1S}.

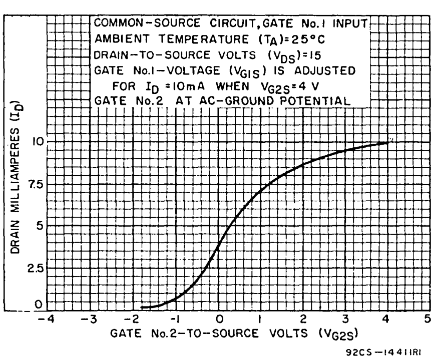


Fig. 5– I_D vs. V_{G2S}.

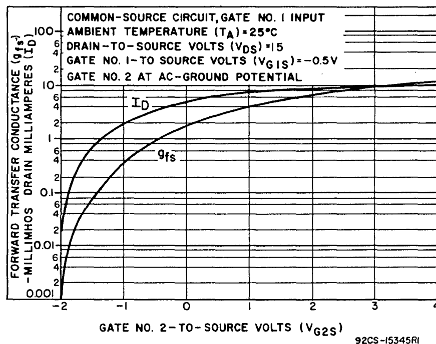


Fig. 6—g_{fs} and I_D vs. V_{G2S}.

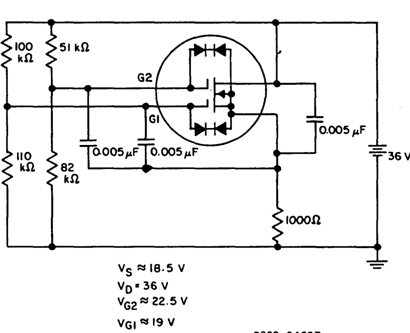


Fig. 9—Burn-In and operating life-test circuit.

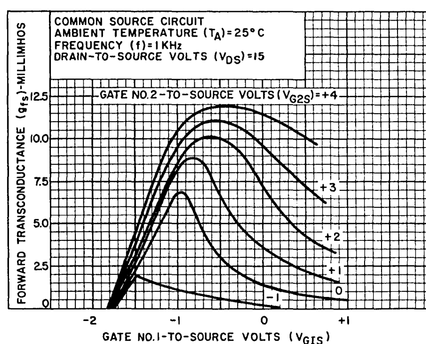


Fig. 7—g_{fs} vs. V_{G1S}.

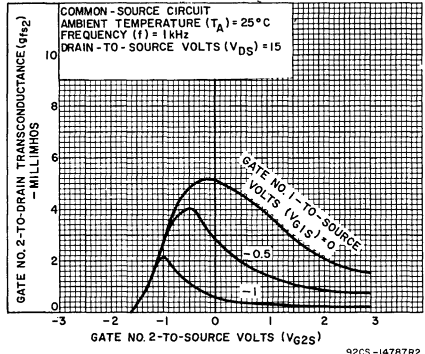
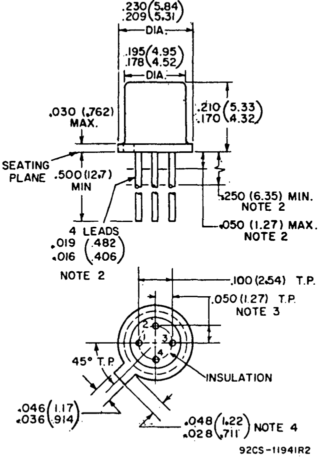


Fig. 8—g_{fs2} vs. V_{G2S}.

DIMENSIONAL OUTLINE JEDEC TO-72



Dimensions in Inches and Millimeters

Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0.250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a guaging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) −0.000" (0.000 mm) below seating plane shall be within 0.007" (0.177 mm) at their true position (location) relative to a maximum width of tab.

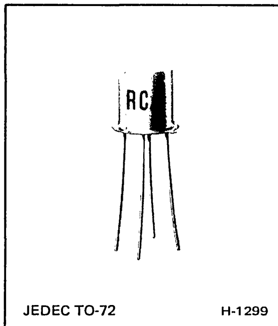
Note 4: Measured from actual maximum diameter.

Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Types

High-Reliability Type
HR3N200



JEDEC TO-72 H-1299

High-Reliability Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits
For Applications in Aerospace, Military, and Critical Industrial Equipment Up to 500 MHz.

Applications:

- **RF amplifier, mixer, and IF amplifier in military and industrial communications equipment**
- **Aircraft and marine vehicular receivers**
- **CATV and MATV equipment**
- **Telemetry and multiplex equipment**

RCA HR3N200 is a high-reliability n-channel silicon, depletion type, dual insulated-gate field-effect transistor. It is intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type 3N200 described in Data Bulletin File No. 437 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The excellent over-all performance characteristics of the HR3N200 make it useful for a wide variety of rf-amplifier applications at frequencies up to 500 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The HR3N200 is hermetically sealed in the metal JEDEC TO-72 package.

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} ...	−0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	−6 to +3	V
Peak ac	−6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	−6 to 30% of V_{DS}	V
Peak ac	−6 to +6	V
*DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
*DRAIN CURRENT, I_D	50	mA
*TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
*AMBIENT TEMPERATURE RANGE:		
Storage and Operating	−65 to +175	°C
*LEAD TEMPERATURE (During soldering): At distances ≥1/32 inch from seating surface for 10 seconds max. ...	265	°C

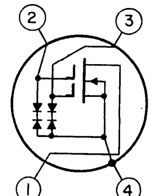
*In accordance with JEDEC registration data format (JS-9 RDF-19A)

Performance Features:

- **Superior cross-modulation performance and greater dynamic range than bipolar and single-gate FET's**
- **Wide dynamic range permits large-signal handling before overload**
- **Dual gate permits simplified agc circuitry**
- **Virtually no agc power required**
- **Greatly reduces spurious responses in FM receivers**

Device Features:

- **Back-to-back diodes protect each gate against handling and in-circuit transients**
- **High forward transconductance — g_{fs} = 15,000 μmho (typ.)**
- **High unneutralized RF power gain — G_{ps} = 12.5 dB (typ.) at 400 MHz = 19 dB (typ.) at 200 MHz**
- **Low VHF noise figure — 4.5 dB (typ.) at 400 MHz 3.0 dB (typ.) at 200 MHz**



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

Fig. 1—Terminal diagram.

Electrical Characteristics for Design Guidance Only

	ELECTRICAL CHARACTERISTICS at T_A = 25°C *unless otherwise specified*	SYMBOL	TEST CONDITIONS		LIMITS Min.	Typ.	Max.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G2S} = +4 V		-0.1	-1	-3	V
*	Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G1S} = 0		-0.1	-1	-3	V
*	Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V, V_{G2S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
*	Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V, V_{G2S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
*	Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V, V_{G1S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
*	Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V, V_{G1S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
*	Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		0.5	5.0	12	mA
*	Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V	f = 1 kHz	10,000	15,000	20,000	μmho
	Small-Signal, Short-Circuit Input Capacitance†	C_{iss}		f = 1 MHz	4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♠	C_{rss}			0.005	0.02	0.03	pF
	Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2.0	–	pF
*	Power Gain (see Fig. 1)	G_{PS}		f = 400 MHz	10	12.5	–	dB
	Noise Figure (see Fig. 1)	NF			–	4.5	6.0	dB
*	Bandwidth	BW			28	–	38	MHz
*	Gate-to-Source Forward Breakdown Voltage, Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	V_{G2S} = V_{DS} = 0	6.5	–	13	V
	Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} = V_{DS} = 0				
*	Gate-to-Source Reverse Breakdown Voltage, Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	V_{G2S} = V_{DS} = 0	-6.5	–	-13	V
	Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} = V_{DS} = 0				

†Capacitance between Gate No. 1 and all other terminals.
♠Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.
*In accordance with JEDEC registration data format (JS-9 RDF-19A).

OPERATING CONSIDERATIONS

The flexible leads of the 3N200 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

Table I— Pre Burn-In and Post Burn-In Electrical Go/No-Go Tests

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ *unless otherwise specified*	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
				Min.	Max.	
Gate No. 1-Terminal Forward Current	I_{G1SSF}	$V_{G1S} = +6$ V, $V_{G2S} = V_{DS} = 0$		—	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	$V_{G1S} = -6$V, $V_{G2S} = V_{DS} = 0$		—	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	$V_{G2S} = +6$ V, $V_{G1S} = V_{DS} = 0$		—	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	$V_{G2S} = -6$ V, $V_{G1S} = V_{DS} = 0$		—	50	nA
Zero-Bias Drain Current	I_{DS}	$V_{DS} = +15$ V, $V_{G1S} = 0$, $V_{G2S} = +4$ V		0.5	12	mA
Gate-to-Source Forward Breakdown Voltage, Gate No. 1	$V_{(BR)G1SSF}$	$I_{G1SSF} = I_{G2SSF} = 100\ \mu A$	$V_{G2S} = V_{DS} = 0$	6.5	13	V
Gate No. 2	$V_{(BR)G2SSF}$		$V_{G1S} = V_{DS} = 0$			
Gate-to-Source Reverse Breakdown Voltage, Gate No. 1	$V_{(BR)G1SSR}$	$I_{G1SSR} = I_{G2SSR} = 100\ \mu A$	$V_{G2S} = V_{DS} = 0$	-6.5	-13	V
Gate No. 2	$V_{(BR)G2SSR}$		$V_{G1S} = V_{DS} = 0$			

Table II—Final Electrical Tests

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ *unless otherwise specified*	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
				Min.	Max.	
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	$V_{DS} = +15$ V, $I_D = 50\ \mu A$, $V_{G2S} = +4$ V		-0.1	-3	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	$V_{DS} = +15$ V, $I_D = 50\ \mu A$, $V_{G1S} = 0$		-0.1	-3	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	$V_{G1S} = +1$ V, $V_{G2S} = V_{DS} = 0$		—	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	$V_{G1S} = -6$ V, $V_{G2S} = V_{DS} = 0$		—	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	$V_{G2S} = +6$ V, $V_{G1S} = V_{DS} = 0$		—	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	$V_{G2S} = -6$ V, $V_{G1S} = V_{DS} = 0$		—	50	nA
Zero-Bias Drain Current	I_{DS}	$V_{DS} = +15$ V, $V_{G1S} = 0$, $V_{G2S} = +4$ V		0.5	12	mA
Gate-to-Source Forward Breakdown Voltage, Gate No. 1	$V_{(BR)G1SSF}$	$I_{G1SSF} = I_{G2SSF} = 100\ \mu A$	$V_{G2S} = V_{DS} = 0$	6.5	13	V
Gate No. 2	$V_{(BR)G2SSF}$		$V_{G1S} = V_{DS} = 0$			
Gate-to-Source Reverse Breakdown Voltage, Gate No. 1	$V_{(BR)G1SSR}$	$I_{G1SSR} = I_{G2SSR} = 100\ \mu A$	$V_{G2S} = V_{DS} = 0$	-6.5	-13	V
Gate No. 2	$V_{(BR)G2SSR}$		$V_{G1S} = V_{DS} = 0$			

Table III—
Group A Electrical Sampling Inspection

ELECTRICAL CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			MINIMUM			MAXIMUM			
			-55	+25	+125	-55	+25	+125	°C
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G2S} = +4 V	-0.1	-0.1	–	-3	-3	–	V
		V_{DS} = +15 V, I_D = 100 μA, V_{G2S} = +4 V	–	–	-0.1	–	–	-3	
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G1S} = +4 V	-0.1	-0.1	–	-3	-3	–	V
		V_{DS} = +15 V, I_D = 100 μA, V_{G1S} = +4 V	–	–	-0.1	–		-3	
Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +6 V, V_{G2S} = V_{DS} = 0	–	–	–	–	50	–	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V, V_{G2S} = V_{DS} = 0	–	–	–	–	50	–	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V, V_{G1S} = V_{DS} = 0	–	–	–	–	50	–	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V, V_{G1S} = V_{DS} = 0	–	–	–	–	50	–	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V	0.5	0.5	0.3	12	12	8.5	mA
Forward Transconductance Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 1 MHz	–	10,000	–	–	20,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 1 MHz	–	4.0	–	–	8.5	–	pF
Small-Signal, Short-Circuit Reverse Transfer Capacitance (Drain-to-Gate-No. 1)	C_{rss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 1 MHz	–	0.005	–	–	0.03	–	pF
Power Gain	G_{PS}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 400 MHz	–	10	–	–	–	–	dB
Noise Figure	NF	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 400 MHz	–	–	–	–	6.0	–	dB
Bandwidth	BW	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 400 MHz	–	28	–	–	38	–	MHz
Gate-to-Source Forward Breakdown Voltage Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA; V_{G2S} = V_{DS} = 0	6.5	6.5	4.5	13	13	14.5	V
Gate No. 2	$V_{(BR)G2SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA; V_{G1S} = V_{DS} = 0							
Gate-to-Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA; V_{G2S} = V_{DS} = 0	-6.5	-6.5	-4.5	-13	-13	-14.5	V
Gate No. 2	$V_{(BR)G2SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA; V_{G1S} = V_{DS} = 0							

TYPICAL CHARACTERISTICS

For Y Parameters, see 3N200 Data Bulletin File No. 437

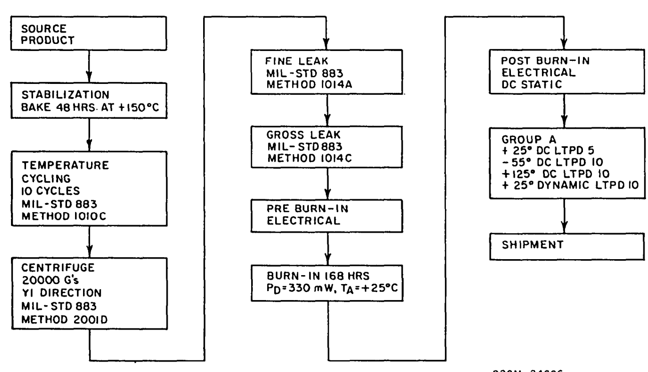
Fig. 2—I_D vs. V_{G1S}.

Fig. 3—I_D vs. V_{G2S}.

Fig. 4—I_D vs. V_{DS}.

Fig. 5—V_{AGC} vs. V_{G1S}.

High-Reliability Processing Flow Chart



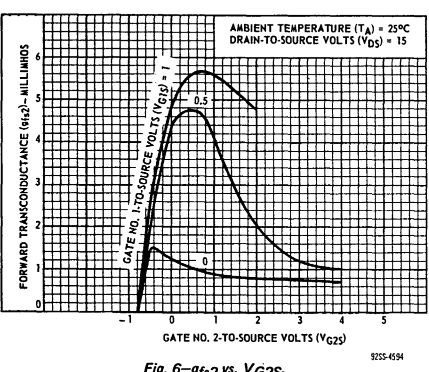


Fig. 6—g_{fs2} vs. V_{G2S}.

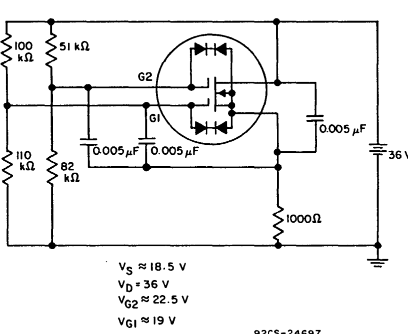


Fig. 9—Burn-In and operating life-test circuit.

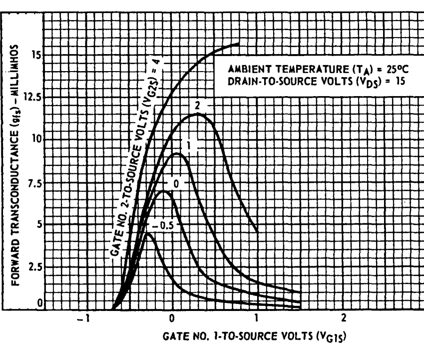
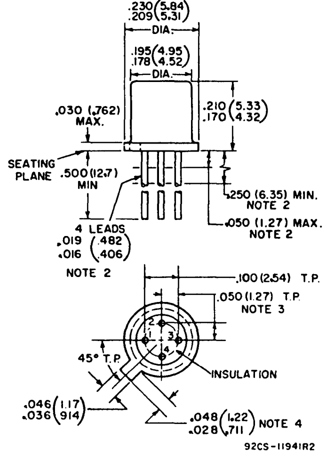


Fig. 7—g_{fs} vs. V_{G1S}.

DIMENSIONAL OUTLINE JEDEC TO-72



Dimensions in Inches and Millimeters

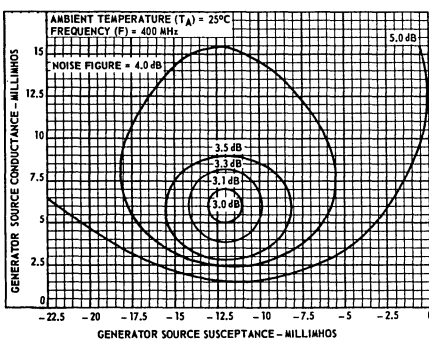


Fig. 8—Noise figure vs. generator source admittance.

Lead Finish:
In accordance with MIL-M-38510, Paragraph 3.6.2.5, Lead Finish "A".

Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0.250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a guaging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) −0.000" (0.000 mm) below seating plane shall be within 0.007" (0.177 mm) at their true position (location) relative to a maximum width of tab.

Note 4: Measured from actual maximum diameter.

Solid State
Division

Linear Integrated Circuits

High-Reliability CA3000 Slash (/) Series Types

Screened to MIL-STD-883

RCA linear high-reliability slash (/) series integrated circuits are available for applications in aerospace, military, and industrial equipment. These circuits are supplied to six screening levels (/1N, /1R, /1, /2, /3, /4) which meet the electrical, mechanical, and environmental test methods and procedures established for micro-electronic devices in MIL-STD-883. These six screening levels are equivalent to MIL-STD-883 Classes A, B, C and are summarized in Table 1.

RCA also offers standard commercial product with a 168-hour burn-in, designated level /5.

This bulletin defines the test procedures employed with linear IC devices to meet the reliability standards required by MIL-STD-883. The level /1N part includes SEM (Scanning Electron Microscope) Inspection to NASA-Goddard Specification GSFC-S-311-P-12 of MIL-M-38510, and Precap Visual Inspection, Condition A, Method 2010-1, MIL-STD-883. The level /R part includes the SEM inspection in addition to the requirements of level /1 part.

The Product Flow Diagram shown in Fig. 1 lists a summary of processing, screening tests, and sampling procedures followed in the manufacture of high-reliability linear integrated circuits.

Table 2 gives detailed information for the screening tests included in the Product Flow Diagram. Tables 3 and 4 give test criteria for Final Electrical and Group A Electrical Tests. Tables 5 and 6 describe Group B and C Environmental Sampling Inspection Tests.

MIL-STD-883
2010.1A OR
2010.2B
PRECAP VISUAL
SEM INSPECTION AS REQUIRED
PRESEAL BAKE
SEAL AND LOT IDENTIFICATION
CONDITIONING SCREENS
STABILIZATION BAKE
THERMAL SHOCK
TEMPERATURE CYCLING
MECHANICAL SHOCK
CENTRIFUGE
FINE LEAK
GROSS LEAK
SERIALIZE
PRE BURN-IN ELEC.
BURN-IN
POST BURN-IN ELECTRICAL
FINAL ELECTRICAL
GROUP A
RADIOGRAPHIC INSPECTION
EXTERNAL VISUAL
LEVEL /IN
LEVEL /IR
LEVEL /I
LEVEL /2
B GROUP
C GROUP
CONDITIONING SCREENS
STABILIZATION BAKE
TEMPERATURE CYCLING
CENTRIFUGE
FINE LEAK
GROSS LEAK
ELECTRICAL TESTS
BURN-IN
FINAL ELECTRICAL
GROUP A
EXTERNAL VISUAL
LEVEL /3
FINAL ELECTRICAL
GROUP A
EXTERNAL VISUAL
LEVEL /4
STANDARD COMMERCIAL PRODUCT
168-HOUR BURN-IN
LEVEL /5
92CL-24949

Fig. 1 – Product flow diagram. See Tables 2, 3, 4, 5, and 6 for details.

Table 1 – Description of RCA Integrated-Circuit Screening Levels

<table>
<tr><th colspan="2">Screening Levels▲</th><th rowspan="2">Application</th><th rowspan="2">Description</th></tr>
<tr><th>RCA Levels</th><th>Equivalent to MIL-STD-883, Method 5004.1</th></tr>
<tr><td colspan="4">For Packaged Devices</td></tr>
<tr><td>/1N</td><td>Class A with SEM* Inspection and Condition A Precap Visual Inspection</td><td rowspan="3">Aerospace and Missiles</td><td rowspan="3">For devices intended for use where maintenance and replacement are impossible and reliability is imperative</td></tr>
<tr><td>/1R</td><td>Class A with SEM* Inspection and Condition B Precap Visual Inspection</td></tr>
<tr><td>/1</td><td>Class A with Condition B Precap Visual Inspection</td></tr>
<tr><td>/2</td><td>Class A with Condition B Precap Visual Inspection. Radiographic Inspection Omitted</td><td>Aerospace and Missiles</td><td>For devices intended for use where maintenance and replacement are extremely difficult or impossible and reliability is imperative</td></tr>
<tr><td>/3</td><td>Class B</td><td>Military and Industrial For example, in Airborne Electronics</td><td>For devices intended for use where maintenance and replacement can be performed but are difficult and expensive</td></tr>
<tr><td>/4</td><td>Class C</td><td>Military and Industrial For example, in Ground-Based Electronics</td><td>For devices intended for use where replacement can readily be accomplished</td></tr>
<tr><td>/5 Standard commercial plus burn-in</td><td>–</td><td>Commercial and Industrial</td><td>For devices intended for use where a higher level of reliability is required than can be provided by product without a burn-in</td></tr>
<tr><td colspan="4">For Chips■</td></tr>
<tr><td>/N</td><td>SEM* Inspection and Condition A Precap Visual Inspection</td><td rowspan="2">Aerospace and Missiles</td><td rowspan="2">For hybrid applications where maintenance and replacement are extremely difficult and reliability is imperative</td></tr>
<tr><td>/R</td><td>SEM* Inspection and Condition B Precap Visual Inspection</td></tr>
<tr><td>/M</td><td>Condition B Precap Visual Inspection</td><td>Military and Industrial</td><td>For general applications</td></tr>
</table>

*SEM – Scanning Electron Microscope Inspection per NASA Specification GSFC-S-311-P-12

▲For details on Condition A and Condition B Precap Visual Inspection, refer to MIL-STD-883 Method 2010.1

■ Lot acceptance testing for chips is available on a custom basis

Ordering Information

1. Packaged Device and Chip Type Number Identification

When ordering a packaged device or a chip, it is important that the desired Screening Level and Package Designation for the Packaged Device, and the desired Screening Level for the Chip Version indicated by the appropriate suffix letters be added to the Part Number as shown below. For example, a CA3094A in an 8-lead TO-5 package and processed to meet MIL-STD-883 Class A requirements with SEM Inspection plus Condition A Precap Visual would be identified as the CA3094AT/1N. In similar manner, a CA3094 Chip having SEM inspection plus Condition A Precap Visual would be identified as the CA3094H/N.

2. Data Supplied With Order for Packaged Devices

	For the Following RCA Screening Levels
a) Product Screening Data	
Certificate of Compliance Signed by RCA Representative – Provides lot identity, customer order identity, lists and certifies tests, methods and conditions of required processing per MIL-STD-883	All except /5
Group A Subgroup – Test Summary Attributes Data	All except /5
Variables Data, Pre Burn-In and Post Burn-In	/1N, /1R, /1, /2
Radiographic Inspection Film and Film Inspection Record	/1N, /1R, /1
SEM Inspection Certificate of Compliance to NASA Specification GSFC-S-311-P-12 Includes lot identification and one worst-case photograph	/1N, /1R

b) Lot Quality Conformance Data –
Group B and Group C Subgroups

Attributes Data Summary of the Latest Group B and/or Group C Subgroup can be ordered at a nominal charge.

Special Group B and/or Group C quality conformance tests on samples from the specific lot of parts ordered will be considered on a custom basis only.

Description of RCA Linear IC High-Reliability Part Numbers

Packaged Device CA3094AT/1N

CA3094A	T	/1N
	Package Suffix Letter	**Screening Level**
Type Designation	T = TO-5 Style Package D = Dual-in-Line Weld-Seal Ceramic F = Dual-in-Line Frit-Seal Ceramic	/1N /2 /1R /3 /1 /4 /5 For Description, See Table 1

Chip Version, CA3094H/N

CA3094	H	/N
	Package Suffix Letter	**Screening Level**
Type Designation	H = Chip Version	/N /R /M For Description, See Table 1

Table 2 – Description of Total Lot Screening (X = 100% Testing)

Test	Conditions	MIL-STD-883		RCA Screening Levels*					
		Method	Conditions	/1N	/1R	/1	/2	/3	/4
SEM Inspection	NASA Per GSFC-S-311-P-12	–	–	X	X	–	–	–	–
Precap Visual	–	2010.1	A	X	–	–	–	–	–
Precap Visual	–	2010.1	B	–	X	X	X	X	X
Preseal Bake	16 to 32 hrs at 200°C	–	–	X	X	X	X	X	X
Seal & Lot Identification	–	–	–	X	X	X	X	X	X
Stabilization Bake	48 hrs. at 150°C	1008	C	X	X	X	X	X	X
Thermal Shock	15 cycles	1011	C	X	X	X	X	–	–
Temperature Cycling	10 cycles	1010	C	X	X	X	X	X	X
Mechanical Shock	5 pulses, Y_1 direction	2002	B	X	X	X	X	–	–
Centrifuge	Y_2, Y_1 direction	2001	E	X	X	X	X	–	–
	Y_1 direction only	2001	E	–	–	–	–	X	X
Fine Leak	–	1014	A	X	X	X	X	X	X
Gross Leak	–	1014	C	X	X	X	X	X	X
Electrical Tests	See Note 1	–	–	X	X	X	X	X	–
Serialize	–	–	–	X	X	X	X	–	–
Pre Burn-in Electrical	See Note 2	–	–	X	X	X	X	–	–
Burn-in	240 hours	1015	B, D or E	X	X	X	X	–	–
	168 hours	1015	B, D or E	–	–	–	–	X	–
Post Burn-in Electrical	Delta Requirements (See Note 2)	–	–	X	X	X	X	–	–
Final Electrical	–	–	–	–	–	–	–	–	–
a) 25°C	see Table 4	–	–	X	X	X	X	X	X
b) -55 and +125°C	see Table 4	–	–	X	X	X	X	X	S
Radiographic Inspection	1 view	2012	–	X	X	X	–	–	–
External Visual	–	2009	–	X	X	X	X	X	X

Note 1: See specific type Slash (/) Series type data bulletin for test conditions and limits

Note 2: For requirements, see specific Slash (/) Series type data bulletin

* RCA screening level /5 consists of a 168-hour burn-in screen performed on standard commercial product. The ambient test temperature is the maximum possible without exceeding device thermal ratings. After burn-in, /5 devices meet all of the electrical requirements specified in the appropriate commercial data bulletin, Reference: RCA DATABOOK SSD-201.

Table 3 — Final Electrical Tests

TEMPERATURE (T_A)	TEST	TEST CRITERIA LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
+25°C	Selected Static Parameters	100%	100%	100%
+125°C	Selected Static Parameters	100%	100%	–
-55°C	Selected Static Parameters	100%	100%	–
+25°C	Selected Dynamic Parameters	100%	100%	–

Table 4 — Group A Electrical Sampling Inspection

SUBGROUP	TEST	CONDITION	LTPD LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Selected Static Parameters	T_A = +25°C	5	5	5
2	Selected Static Parameters	T_A = +125°C	5	7	10
3	Selected Static Parameters	T_A = -55°C	5	7	10
4	Selected Dynamic Parameters	T_A = +25°C	5	5	5

Table 5 — Group B Environmental Sampling Inspection (Note 1)

SUBGROUP	TEST	MIL-STD-883 REFERENCE	CONDITIONS	LTPD LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Physical Dimensions	2003	Test Cond. A per applicable data sheet	10	15	20
2	Marking Permanency	2008	Test Cond. B per Par. 3.2.1	4 devices (no failures)		
	Visual and Mechanical	2008	Test Cond. B 10 X mag.	1 device (no failure)		
	Bond Strength	2011	Test Cond. D 10 Devices minimum	5	15	20
3	Solderability	2003		10	15	15
4	Lead Fatigue	2004	Test Cond. B2 any 5 leads	10	15	15
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			

Note 1: Group B tests are performed on each inspection lot per requirements of MIL-M-38510
Note 2: Operating life circuits are included in specific type high-reliability data bulletins

Table 6 — Group C Environmental Sampling Inspection (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Thermal Shock	1011	Test Cond. C	10	15	15
	Temperature Cycling	1010	Test Cond. C			
	Moisture Resistance	1004	No Voltage Applied			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests — Note 3					
2	Mechanical Shock	2002	Test Cond. B, 0.5 ms	10	15	15
	Vibration, Var. Freq.	2007	Test Cond. A			
	Constant Acceleration	2001	Test Cond. E			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests — Note 3					
3	Salt Atmosphere	1009	Test Cond. A Omit Initial Conditioning	10	15	15
4	High Temp. Storage Critical Post Tests — Note 3	1008	Test Cond. C 1000 hours	7	7	7
5	Operating Life Critical Post Tests — Note 3	1005	T_A - 125°C, 1000 hrs. Test Circuit (Note 2)	5	5	5
6	Steady State Bias Critical Post Tests — Note 3	1015	Test Cond. A, 72 hrs. At T_A = 150°C (Note 3)	7	—	—

Note 1: Group C tests are performed at 3-month intervals for reliability history.
Note 2: Operating life circuits are included in specific type high-reliability data bulletins.
Note 3: Static parameters and limits are shown in High-Reliability Devices DATABOOK SSD-207, and in specific type high-reliability data bulletins.

Solid State
Division

Linear Integrated Circuits

High-Reliability MIL-M-38510 CA3000-Series Types

RCA high-reliability linear integrated circuits are available for applications in aerospace, military, and industrial equipment where screening requirements of MIL-M-38510 are specified. Linear circuits are supplied to two screening classes of MIL-M-38510 as specified in MIL-STD-883 Method 5004 Classes B and C. Table 1 describes the screening levels.

This bulletin defines the procedures employed to manufacture linear devices to meet the reliability requirements of MIL-M-38510. These linear devices are available in TO-5 packages.

MIL-M-38510 is the general specification for integrated circuits and is more comprehensive than MIL-STD-883. This general specification was introduced a year after MIL-STD-883. It adds a number of quality constraints not included in MIL-STD-883, which is a specification of test methods, procedures, and screening tests. Linear parts are provided to MIL-M-38510 under a series of /100 numbers, of which six are in existence. Parts meet requirements similar to those of Classes B and C of MIL-STD-883 Method 5004 screening, except that additional requirements, including more test conditions and tightened limits, are imposed. The Product Flow Diagram shown in Fig. 1 summarizes the processing, screening tests, and sampling procedures followed in the manufacture of high-reliability linear integrated circuits. The additional criteria for each class of product are indicated by an X in Table 2. Also provided in the MIL-M-38510 test is a PDA (Per-Cent Defective Allowed) of 10 per cent for the one burn-in of Class B product. Tables 3 and 4 give test criteria for Final Electrical and Group A Electrical Tests. Tables 5 and 6 describe Group B and C Environmental Sampling Inspection tests. Table 7 describes the product assurance program that RCA implements in the performance of MIL-M-38510. Table 8 provides a classification guide for linear integrated circuits.

The basic processing operations for high-reliability linear integrated circuits are shown in Fig. 2; details of the high-reliability processing are shown in Fig. 3. The wafer processing and metallization steps, the wafer finishing operations, and the wafer testing are the same as for standard-product linear integrated circuits. After these three basic operations are completed, the tested wafer is subjected to the special high-reliability processing. As shown in Fig. 3, twenty-eight additional processing and screening operations are required for Class B linear parts.

Ordering Information

Order linear MIL-M-38510 Series types by giving the appropriate reliability screen as shown in Fig. 4. For example, the CA741 processed to Class B requirements should be marked MIL-M-38510/10101BGA.

Table 1 — Description of MIL-M-38510 Screening Levels for RCA Integrated Circuits

MIL-M-38510	Application	Description
Class B	Military & Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement are difficult and expensive.
Class C	Military & Industrial For example, in Ground-Based Electronics	For devices intended for use where replacement can readily be accomplished.

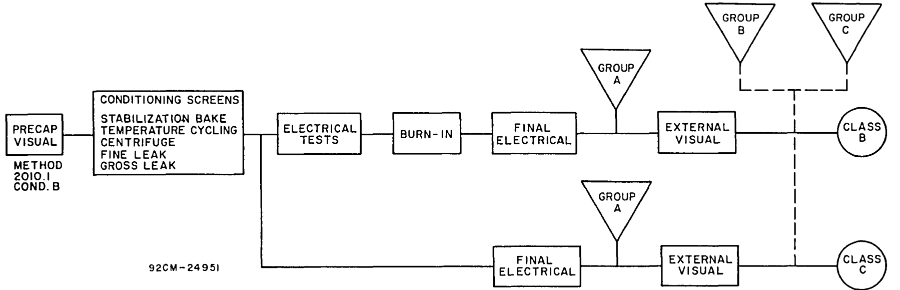


Fig. 1 — Product flow diagram for RCA high-reliability linear integrated circuits processed in accordance with MIL-M-38510.

Table 2 – MIL-M-38510 Processing and Screening Requirements for RCA High-Reliability Linear Integrated Circuits

MIL-M-38510 Processing	MIL-STD-883 METHOD	Condition	MIL-M-38510 CLASS	
			B	C
• Assembly				
Precap Visual	2010.1	B	X	X
• Preconditioning				
Stabilization Bake	1008	C, 48 hours at 150°C	X	X
Temperature Cycle	1010	C, 10 cycles, –65°C to +150°C	X	X
Centrifuge Y1	2001	E, 30000 G's	X	X
Fine Leak	1014	A	X	X
Gross Leak	1014	C	X	X
• Test and Burn-In				
Initial Test	–	MIL-M-38510/100 Series	X	–
Operating Burn-In 168 Hrs.	1015	B	X	–
Final Electrical DC +25°C		MIL-M-38510/100 Series	X	X
Final Electrical AC +25°C		MIL-M-38510/100 Series	X	S
Final Electrical DC –55°C		MIL-M-38510/100 Series	X	S
Final Electrical AC –55°C		MIL-M-38510/100 Series	S	S
Final Electrical DC +125°C		MIL-M-38510/100 Series	X	S
Final Electrical AC +125°C		MIL-M-38510/100 Series	S	S

Table 3 – Final Electrical Tests

TEMPERATURE (T_A)	TESTS TO MIL-M-38510 SPECIFICATIONS	TEST CRITERIA	
		Class B	Class C
+25°C	DC & Functional Parameters	100%	100%
+125°C	DC & Functional Parameters	100%	–
–55°C	DC & Functional Parameters	100%	–
+25°C	AC Parameters	100%	–

Table 4 – Group A Electrical Sampling Inspection

SUBGROUP OF MIL-STD-883 5005.1	TESTS TO MIL-M-38510 SPECIFICATIONS	CONDITION	LTPD	
			Class B	Class C
1, 7	DC & Functional Parameters	T_A = +25°C	5	5
2, 8	DC & Functional Parameters	T_A = +125°C	7	10
3, 8	DC & Functional Parameters	T_A = –55°C	7	10
4, 9	AC Parameters	T_A = +25°C	5	5
10	AC Parameters	T_A = +125°C	5	–
11	AC Parameters	T_A = –55°C	7	–

Details of static, functional, and dynamic tests, conditions, and limits appear in the specific MIL-M-38510/ specifications.

Table 5 — Group B Environmental Sampling Inspection to MIL-M-38510 (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD	
		REFERENCE	CONDITIONS	Class B	Class C
1	Physical Dimensions	2008	Test Cond. A per applicable data sheet	15	20
2	Marking Permanency	2008	Test Cond. B per Par. 3.2.1	← 4 devices (no failures) →	
	Visual and Mechanical	2008	Test Cond. B, 10 X mag.	← 1 device (no failures) →	
	Bond Strength	2011	Test Cond. D, 10 devices minimum	15	20
3	Solderability	2003		15	15
4	Lead Fatigue	2004	Test Cond. B2, any 5 leads	15	15
	Fine Leak	1014	Test Cond. A		
	Gross Leak	1014	Test Cond. C		

Note 1: Group B tests are performed on each inspection lot.
Note 2: Operating life circuits are included in specific type bulletins.

Table 6 — Group C Environmental Sampling Inspection to MIL-M-38510 (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD	
		REFERENCE	CONDITIONS	Class B	Class C
1	Thermal Shock	1011	Test Cond. C	15	15
	Temperature Cycling	1010	Test Cond. C		
	Moisture Resistance	1004	No Voltage Applied		
	Fine Leak	1014	Test Cond. A		
	Gross Leak	1014	Test Cond. C		
	Critical Post Tests—Note 3				
2	Mechanical Shock	2002	Test Cond. B, 0.5 ms	15	15
	Vibration, Var. Freq.	2007	Test Cond. A		
	Constant Acceleration	2001	Test Cond. E		
	Fine Leak	1014	Test Cond. A		
	Gross Leak	1014	Test Cond. C		
	Critical Post Test—Note 3				
3	Salt Atmosphere	1009	Test Cond. A Omit Initial Conditioning	15	15
4	High Temp. Storage Critical Post Tests—Note 3	1008	Test Cond. C 1000 hours	7	7
5	Operating Life Critical Post Tests—Notes 2 and 3	1005	T_A = +125°C, 1000 hrs. Test Circuit (Note 2)	5	5

Note 1: Group C tests performed at 3-month intervals.
Note 2: Operating life circuits are included in specific type bulletins.
Note 3: Static parameters and limits are shown in High-Reliability Devices DATABOOK SSD-207, and in specific type high-reliability integrated-circuit data bulletin.

Table 7 — MIL-M-38510 Product-Assurance Program Requirements

In-House Documentation Covering These Areas

a. Conversion of customer requirements into manufacturer's internal instructions
b. Personnel training and testing
c. Inspection of incoming materials, utilities and work in process
d. Quality-control operations
e. Quality-assurance operations
f. Design, processing, tool and materials standards and instructions
g. Cleanliness and atmospheres in work areas
h. Design, material, and process change control
i. Tool and test equipment maintenance and calibration
j. Failure and defect analysis and data feedback
k. Corrective action and evaluation
l. Incoming, in process, and outgoing inventory control

In-House Records Covering These Areas

a. Personnel training and testing
b. Inspection operations
c. Failure reports and analyses
d. Changes in design, materials, or processing
e. Equipment calibrations
f. Process utility and material controls
g. Product lot identification

A Program Plan Covering These Areas

a. Functional block organization chart
b. Manufacturing flow chart
c. Proprietary-document listing
d. Examples of design, material, equipment, and processing instructions
e. Examples of records
f. Examples of design, material and process change control documents
g. Examples of failure and defect analysis and feedback documents
h. Examples of corrective action and evaluation documents

Table 8 — Product Classification Guide

Linear Types (MIL-STD-883 Slash Sheets and MIL-M-38510 Series)		
Standard Product Type No.	Descriptive Title	MIL-M-38510/100 Series Type Detailed Electrical Specification No.
CA101A	Operational Amplifier	MIL-M-38510/10103
CA108A	Operational Amplifier	MIL-M-38510/10104
CA741	Operational Amplifier	MIL-M-38510/10101
CA747	Operational Amplifier	MIL-M-38510/10102
CA723	Voltage Regulator	MIL-M-38510/10201
CA111	Voltage Comparator	MIL-M-38510/10304
CA3018A CA3045	Transistor Arrays	In Process

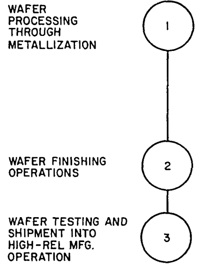


Fig. 2 — Basic processing operations for high-reliability linear integrated circuits as described in MIL-M-38510.

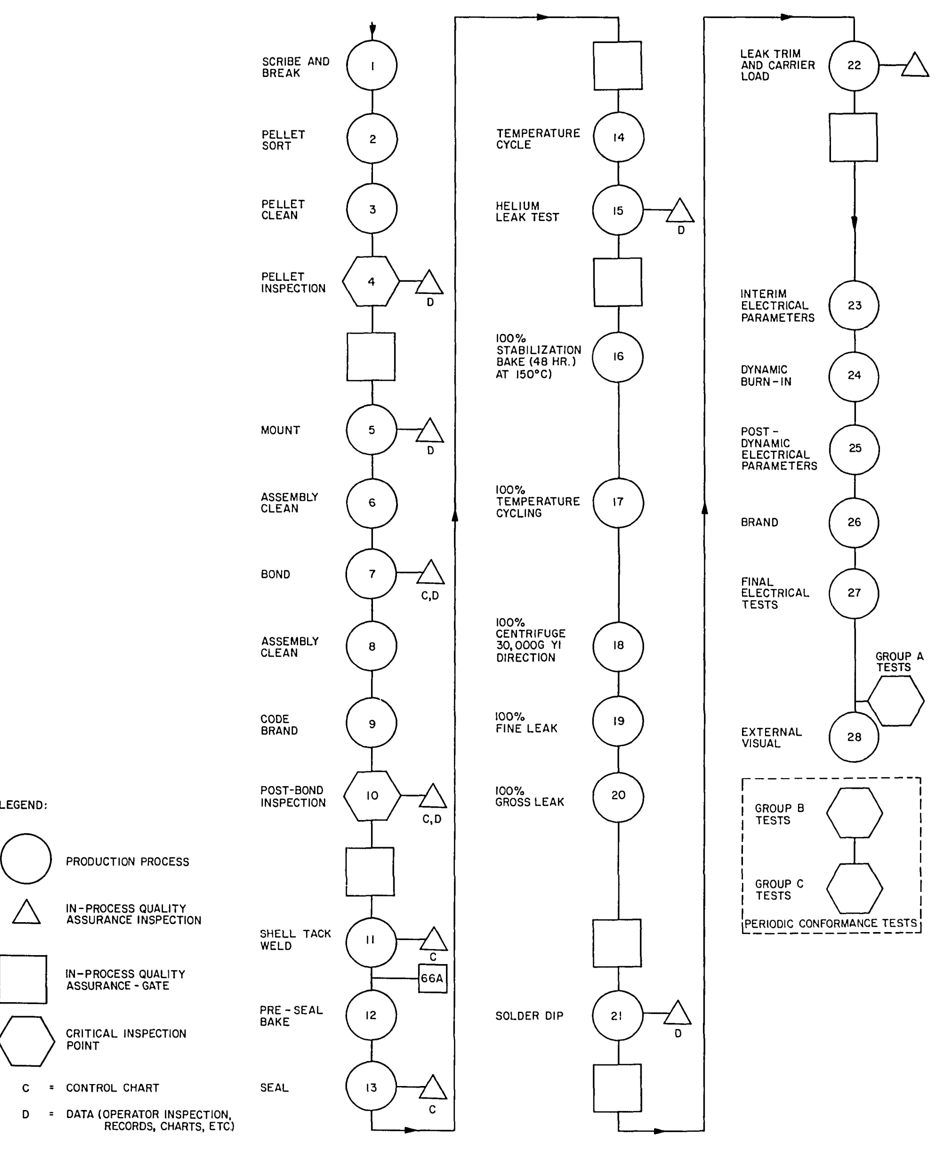


Fig. 3 – Flow Chart for Linear High-Reliability TO-5 MIL-M-38510 Class B Integrated Circuits.

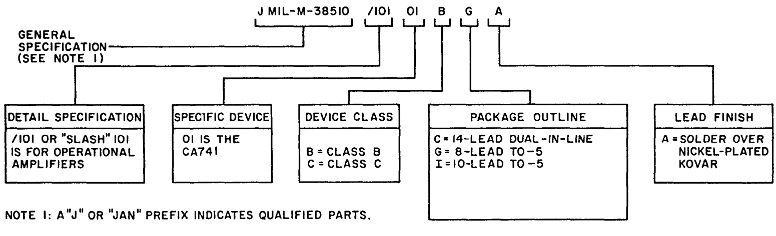


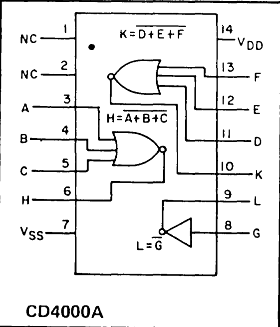
Fig. 4 — Guide to the reliability, class, package, and lead finish of RCA high-reliability linear integrated circuits processed in accordance with MIL-M-38510.

Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4000A/..., CD4001A/... CD4002A/..., CD4025A/...



CD4000A

High-Reliability COS/MOS NOR Gates

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Dual 3 Input plus Inverter --- CD4000A/···
Quad 2 Input --------- CD4001A/···
Dual 4 Input --------- CD4002A/···
Triple 3 Input --------- CD4025A/···

Special Features:

- **Medium speed operation . . . $t_{PHL} = t_{PLH}$ = 25 ns (typ.) at C_L = 15 pF**
- **Low "high"- and "low" -level output impedance . . .500 Ω and 200 Ω (typ.), respectively, at $V_{DD} - V_{SS}$ = 10 V**
- **Low power — 10 nW typ. for gates**
- **Logic compatibility T^2L and DTL interfacing (see ICAN-6602)**
- **High fanout**
- **Excellent temperature stability — ±1.5% shift in transfer characteristics over −55 to +125°C**
- **Inputs fully protected**

RCA CD4000A, CD4001A, CD4002A, and CD4025A "Slash" (/) Series are high-reliability COS/MOS integrated circuit NOR Gates (Positive Logic). They are intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The combination of these devices and the RCA NAND Positive Logic Gate Series CD4011A, CD4012A, and CD4023A can contribute to appreciable package count savings in many of these logic function configurations. These devices are electrically and mechanically identical with standard COS/MOS types CD4000A, CD4001A, CD4002A, and CD4025A described in data Bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designatior
CD4000A	MIL-M-38510/05201
CD4001A	MIL-M-38510/05202
CD4002A	MIL-M-38510/05203
CD4025A	MIL-M-38510/05204

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4000A, CD4001A, CD4002A, and CD4025A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150	°C
Operating-Temperature Range	−55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

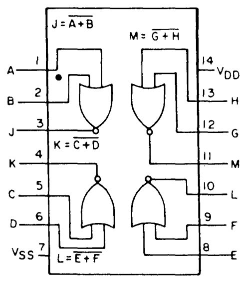
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS CD4000AD, CD4001AD, CD4002AD, CD4025AD, CD4000AK, CD4001AK, CD4002AK, CD4025AK -55°C Min.	-55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L			5	–	0.05	–	0.001	0.05	–	3	μA	1
				10	–	0.1•	–	0.001	0.1•	–	2•		
Quiescent Device Dissipation/Package	P_D			5	–	0.25	–	0.005	0.25	–	15	μW	–
				10	–	1	–	0.01	1	–	20		
Output Voltage Low-Level	V_{OL}	$V_I=V_{DD}$ $I_O=0$		5	–	0.01	–	0	0.01	–	0.05	V	1
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.6•	–	0.7•		
High-Level	V_{OH}	$V_I=V_{SS}$ $I_O=0$		5	4.99	–	4.99	5	–	4.95	–	V	
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.4•	–	–	14.3•	–		1
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D=-10$ μA			−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	$I_D=10$ μA			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity	V_{NL}	$I_O=0$	3.6	5	1.5	–	1.5•	2.25	–	1.4	–	V	2
			7.2	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}		0.95	5	1.4	–	1.5•	2.25	–	1.5	–	V	–
			2.9	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN	$V_I=V_{DD}$	0	3	0.02•	–	0.025•	–	–	–	–	mA	2
			0.4▲	5	0.5	–	0.40•	1	–	0.28	–		
			0.5	10	1.1	–	0.9•	2.5	–	0.65	–		
P-Channel	I_DP	$V_I=V_{SS}$	3	3	−0.02•	–	−0.025•	–	–	–	–	mA	2
			2.5†	5	−0.62	–	−0.5•	−2	–	−0.35	–		
			9.5	10	−0.62	–	−0.5•	−1	–	−0.35	–		
Diode Test	V_{DF}				–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

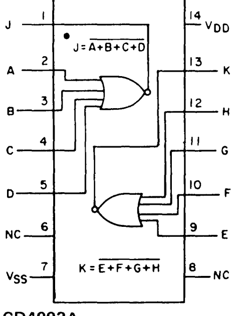
Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or a one output only.

▲Maximum noise-free saturated Bipolar output voltage. †Minimum noise-free saturated Bipolar output voltage.

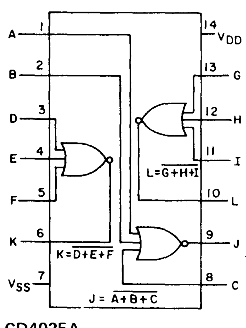
For Noise Immunity Test Circuits, Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations see Appendix.



CD4001A



CD4002A



CD4025A

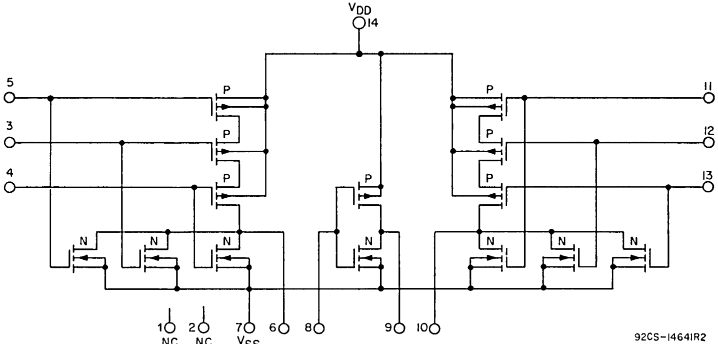


Fig. 1– Schematic diagram for type CD4000A.

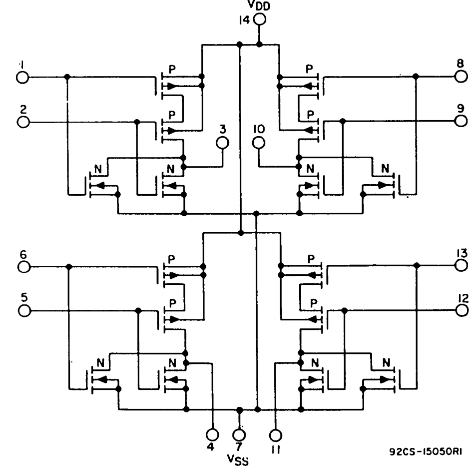


Fig. 2– Schematic diagram for type CD4001A.

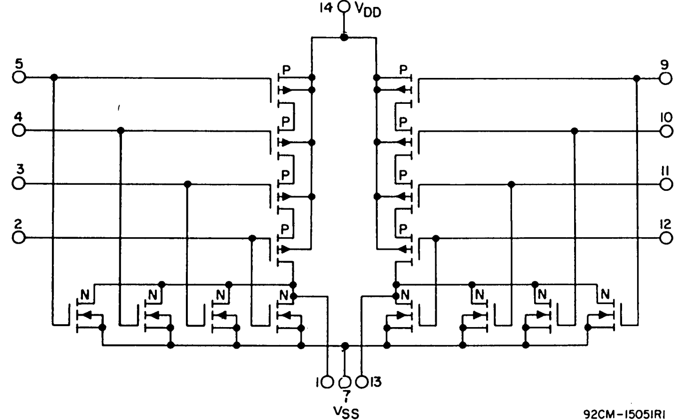


Fig. 3– Schematic diagram for type CD4002A.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4000AD,CD4000AK CD4001AD,CD4001AK CD4002AD,CD4002AK CD4025AD,CD4025AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	–	35	50	ns	–
			10	–	25	40•		
Low-to-High Level	t_{PLH}		5	–	35	95	ns	–
			10	–	25	45•		
Transition Time: High-to-Low Level	t_{THL}		5	–	65	125	ns	–
			10	–	35	70•		
Low-to-High Level	t_{TLH}		5	–	65	175	ns	–
			10	–	35	75•		
Input Capacitance	C_I	Any Input		–	5	–	pF	1

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

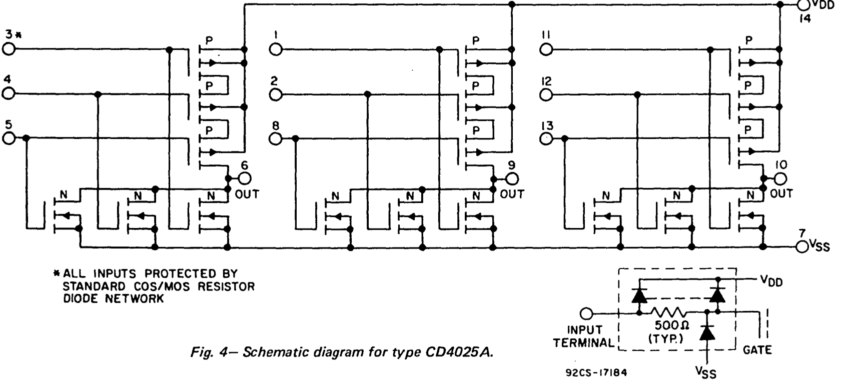


Fig. 4— Schematic diagram for type CD4025A.

Fig. 5— Min. and max. voltage transfer characteristics.

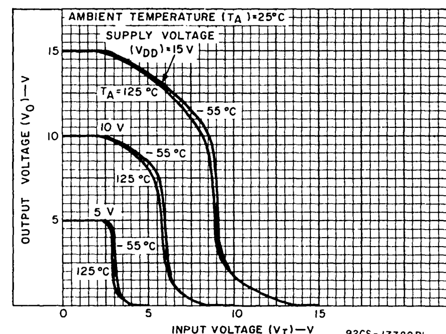


Fig. 6— Typ. voltage transfer characteristics as a function of temperature.

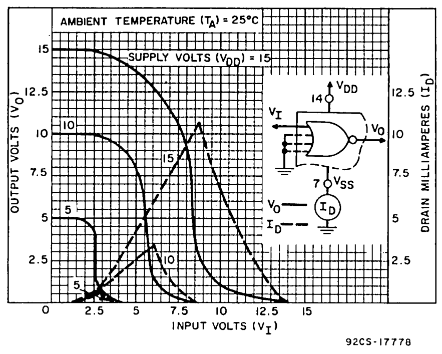


Fig. 7— Typ. current and voltage transfer characteristics.

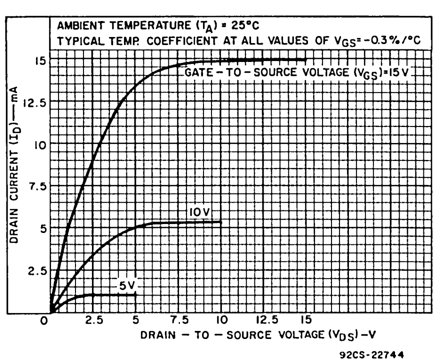


Fig. 8 — Min. n-channel drain characteristics.

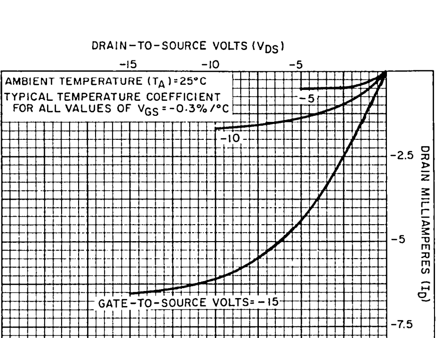


Fig. 9 — Min. p-channel drain characteristics.

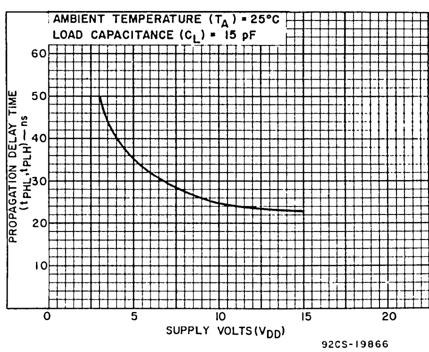


Fig. 10 — Typ. propagation delay time vs. V_{DD}.

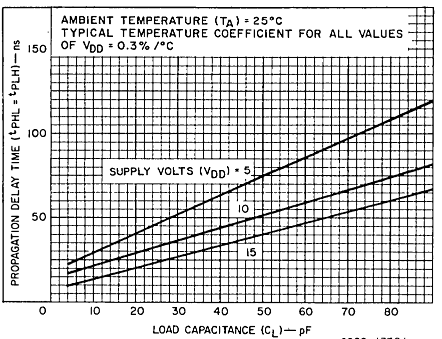


Fig. 11 —Typ. propagation delay time vs.C_L.

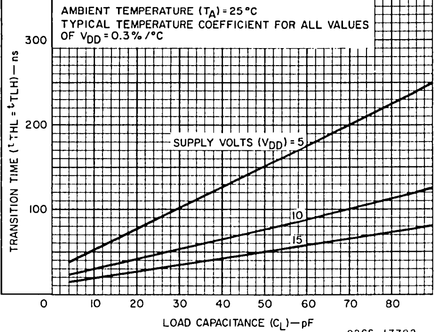


Fig. 12 — Typ. transition time vs. C_L.

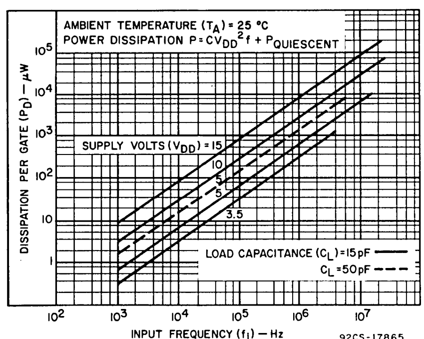


Fig. 13 — Typ. dissipation characteristics.

TEST CIRCUITS

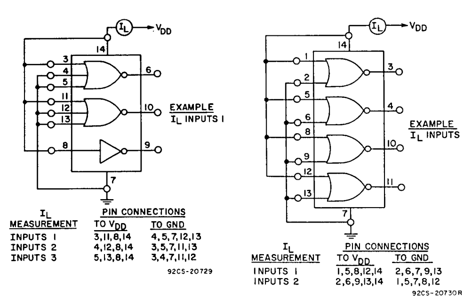


Fig. 14 — Quiescent device current test circuit for CD4000A.

Fig. 15 — Quiescent device current test circuit for CD4001A.

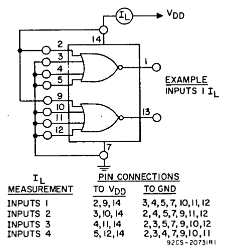


Fig. 16 — Quiescent device current test circuit for CD4002A.

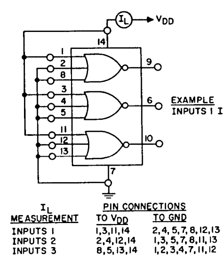


Fig. 17 — Quiescent device current test circuit for CD4025A.

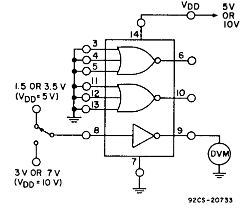


Fig. 18 — Noise immunity test circuit for CD4000A.

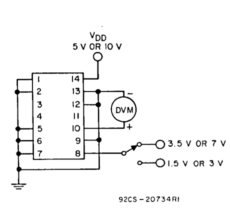


Fig. 19 — Noise immunity test circuit for CD4001A.

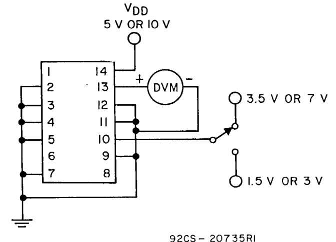


Fig. 20 — Noise immunity test circuit for CD4002A.

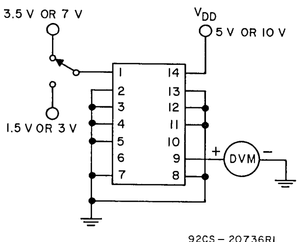


Fig. 21 — Noise immunity test circuit for CD4025A.

Solid State
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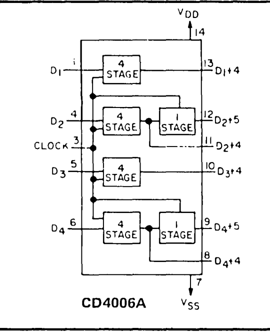
High-Reliability Slash(/) Series
CD4006A/...



High-Reliability COS/MOS 18-Stage Static Shift Register

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Fully static operation**
- **Up to 5 MHz shifting rates**
- **Permanent register storage with clock line "high" or "low" — no information recirculation required**

Applications:

- **Serial shift registers**
- **Time delay circuits**
- **Frequency division**

RCA CD4006A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. CD4006A types are comprised of 4 separate "shift register" sections; two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent "single rail" data path.

A common clock signal is used for all stages. Data is shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17, and 18 can be implemented using one CD4006A package. Longer shift register sections can be assembled by using more than one CD4006A.

These devices are electrically and mechanically identical with standard COS/MOS CD4006A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

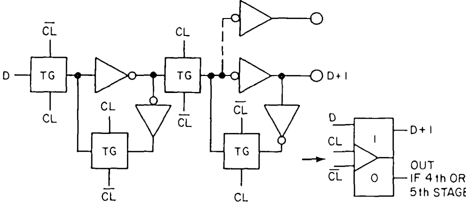
In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as shown in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4006A	MIL-M-38510/05701

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4006A "Slash" Series Types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).



TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL▲	D+1
0	⌐_	0
1	⌐_	1
X	_⌐	NC

NC = NO CHANGE
X = DON'T CARE
▲ = LEVEL CHANGE

92CS-17887

Fig. 1— Logic diagram and truth table (one register stage) for type CD4006A.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range .... −65 to +150 °C
Operating-Temperature Range .... −55 to +125 °C
DC Supply-Voltage Range:
  ($V_{DD} - V_{SS}$) .... −0.5 to +15 V
Device Dissipation (Per Package) .... 200 mW
All Inputs .... $V_{SS} \leq V_I \leq V_{DD}$

Recommended
  DC Supply-Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V
Recommended
  Input-Voltage Swing .... V_{DD} to V_{SS}
Lead Temperature (During Soldering)
  At distance 1/16″ ± 1/32″
  (1.59 ± 0.79 mm) from case
  for 10 s max. .... +265 °C

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4006AD, CD4006AK							UNITS	NOTES
		V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L		5	–	0.5	–	0.01	0.5	–	30	µA	1
			10	–	1•	–	0.01	1•	–	20•		
Quiescent Device Dissipation/Package	P_D		5	–	2.5	–	0.05	2.5	–	150	µW	–
			10	–	10	–	0.1	10	–	200		
Output Voltage Low-Level	V_{OL}		3	–	0.55•	–	–	0.5•	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	–	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = 20 µA		−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	I_D = 20 µA		0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}	0.5	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
		0.5	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}	4.5	5	1.4	--	1.5•	2.25	–	1.5	–	V	
		9.5	10	2.9•	--	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	$I_D N$	0.5	5	0.155	–	0.125•	0.25	–	0.085	–	mA	2
		0.5	10	0.31	·	0.25•	0.5	–	0.175	–		
P-Channel	$I_D P$	4.5	5	−0.125	–	−0.1•	0.15	–	−0.07	–	mA	2
		9.5	10	−0.25	–	−0.2•	−0.3	--	−0.14	–		
Diode Test, 100 µA Test Pin	V_{DF}			–	1.5•	--	–	1.5•	--	1.5•	V	3
Input Current	I_I			--	–	–	10	–	--	--	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

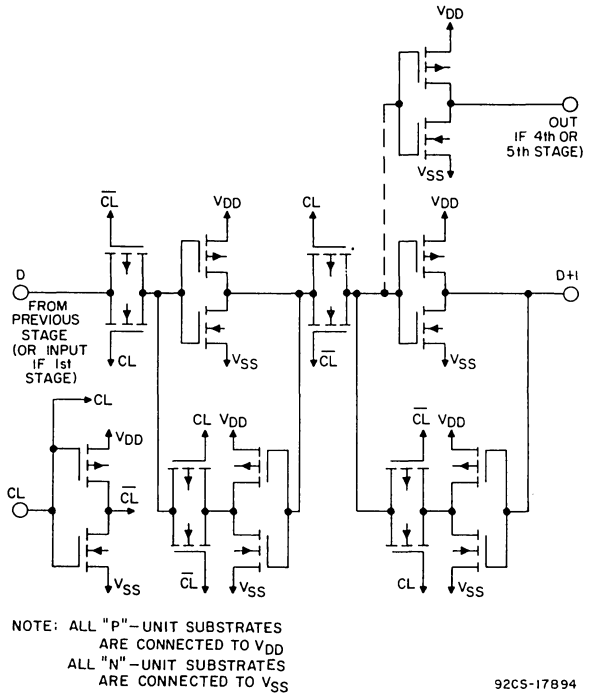


Fig. 2– Schematic diagram (one register stage) for type CD4006A.

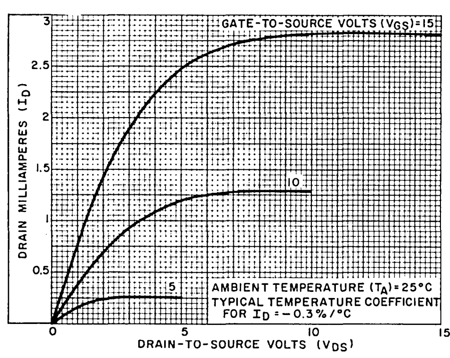


Fig. 3– Minimum n-channel drain characteristics.

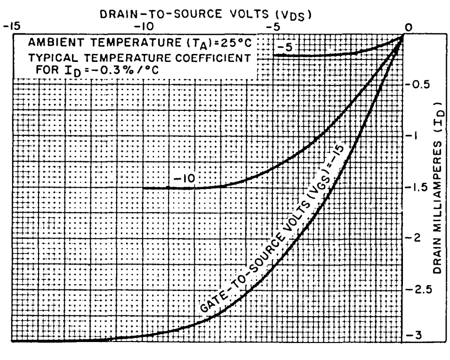


Fig. 4– Minimum p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4006AD,CD4006AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	250	400	ns	1
			10	–	125	200●		
Transition Time	t_{THL}, t_{TLH}		5	–	250	400	ns	1
			10	–	125	200●		
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	500	ns	–
			10	–	100	200		
Clock Rise & Fall Time	t_{rCL}, t_{fCL}*		5	–	–	15	μs	1
			10	–	–	5●		
Set-Up Time			5	–	50	80	ns	–
			10	–	25	40		
Maximum Clock Frequency	f_{CL}		5	1	2.5	–	MHz	1
			10	2.5●	5	–		
Input Capacitance	C_I	Data Input		–	5	–	pF	–
		Clock Input		–	30	–		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

* If more than one unit is cascaded t_fCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

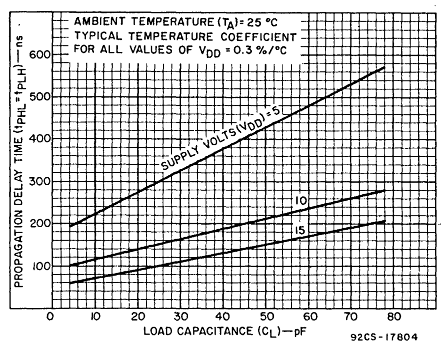


Fig. 5— Typical propagation delay time vs. C_L.

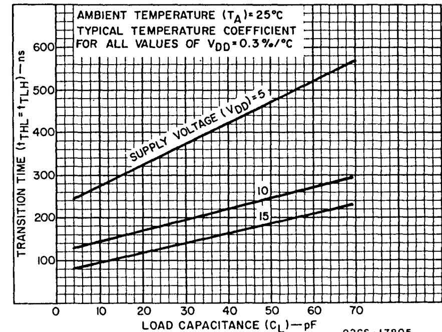


Fig. 6— Typical transition time vs. C_L.

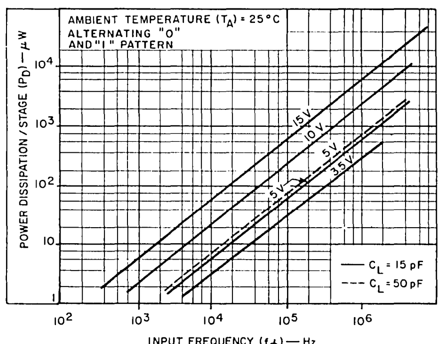


Fig. 7— Typical dissipation characteristics.

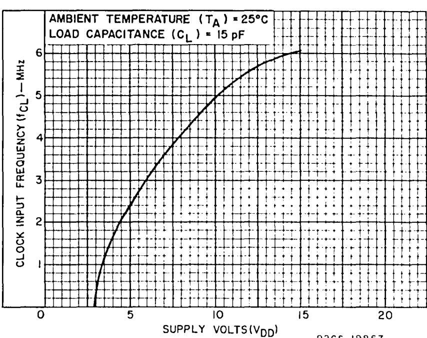
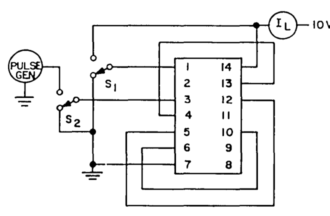


Fig. 8— Typical clock frequency vs. V_{DD}.



With S_1 at ground, clock unit 18 times by connecting S_2 to pulse generator. Return S_2 to ground and measure leakage current. Repeat with S_2 at V_{DD}.

Fig. 9— Quiescent device current test circuit.

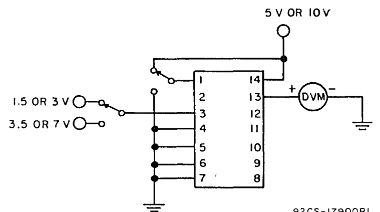


Fig. 10— Noise immunity test circuit.

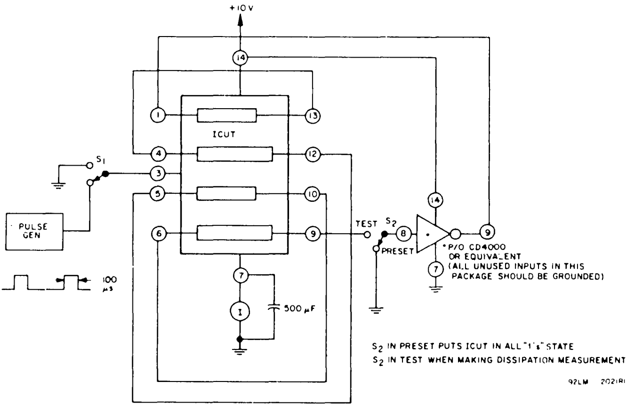


Fig. 11— Device dissipation test setup.

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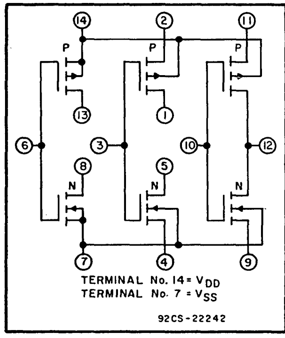
High-Reliability Slash(/) Series
CD4007A/...



High-Reliability COS/MOS
Dual Complementary Pair Plus Inverter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- Medium speed operation . . . $t_{PHL} = t_{PLH} = 20$ ns (typ.) at $C_L = 15$ pF
- Low "high"- and "low"-output impedance . . . 500 Ω (typ.) at $V_{DD} - V_{SS} = 10$ V

Applications:

- Extremely high-input impedance amplifiers, inverters, shapers, linear amplifiers, threshold detectors

RCA CD4007A "Slash" (/) Series high-reliability COS/MOS integrated circuits are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits shown in Fig. 1. More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed. For proper operation $V_{SS} \leq V_I \leq V_{DD}$ must be satisfied.

The CD4007A "Slash" (/) Series are electrically and mechanically identical to the standard COS/MOS CD4007A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as shown in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4007A	MIL-M-38510/05301

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4007A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	–65 to +150	°C
Operating-Temperature Range	–55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	–0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

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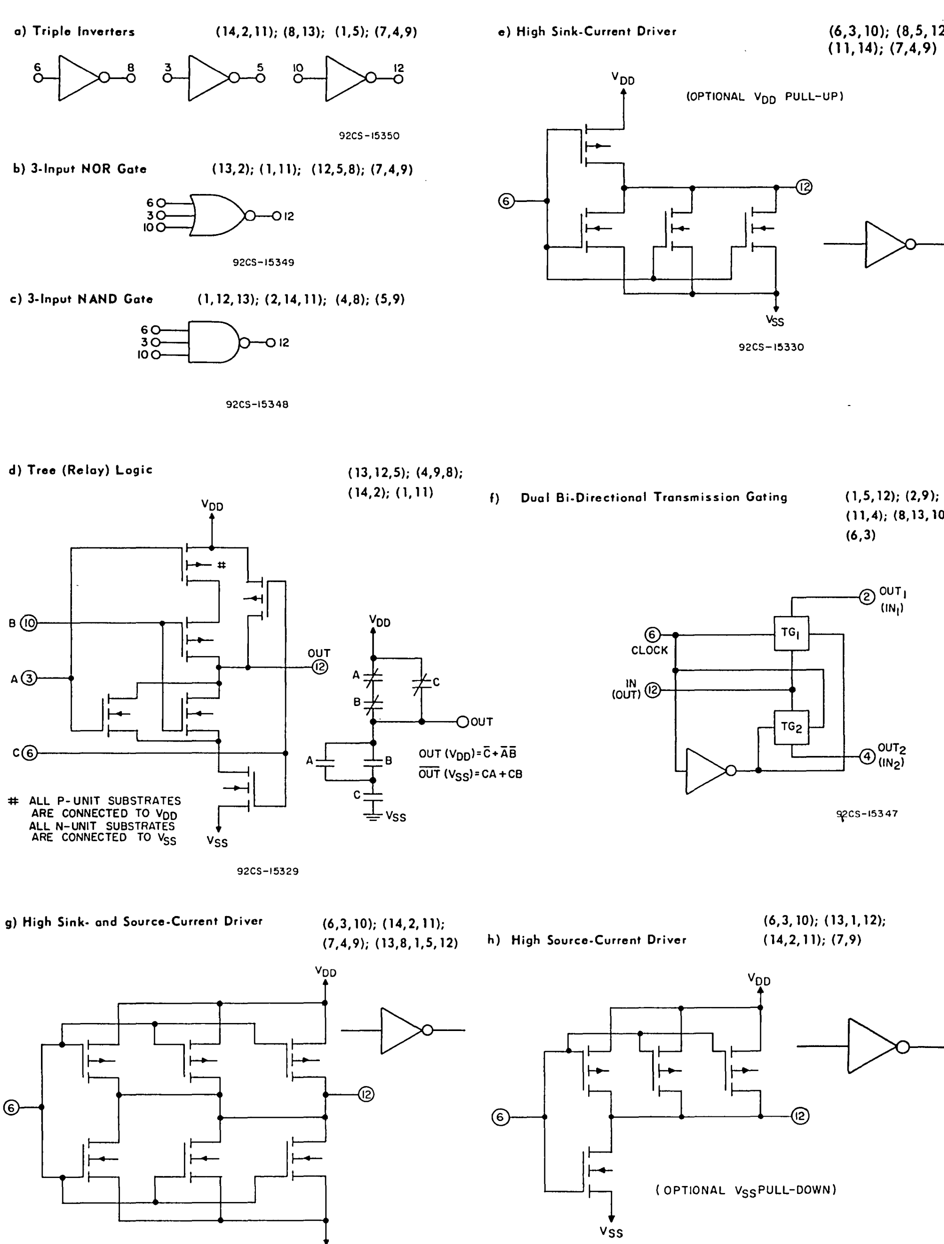

Fig. 1— Sample COS/MOS logic circuit arrangements using type CD4007A.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4007AD, CD4007AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L			5	–	0.05	–	0.001	0.05	–	3	μA	1
				10	–	0.1•	–	0.001	0.1•	–	2•		
Quiescent Device Dissipation/Package	P_D			5	–	0.25	–	0.005	0.25	–	15	μW	–
				10	–	1	–	0.01	1	–	200		
Output Voltage Low-Level	V_{OL}			5	–	0.01	–	0	0.01	–	0.05	V	1
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.6•	–	0.7•		
High-Level	V_{OH}			5	4.99	–	4.99	5	–	4.95	–	V	
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.4•	–	–	14.3•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -10$ μA			−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	$I_D = 10$ μA			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}		3.6	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
			7.2	10	3•	–	3•	4.5	–	2.9•	–		
	V_{NH}		0.95	5	1.4	–	1.5•	2.25	–	1.5	–	V	
			2.9	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN	$V_I = V_{DD}$	0	3	0.04•	–	0.05•	–	–	–	–	mA	2
			0.4▲	5	0.75	–	0.6•	1	–	0.4	–		
			0.5	10	1.6	–	1.5•	2.5	–	0.95	–		
P-Channel	I_DP	$V_I = V_{SS}$	3	3	−0.04•	–	−0.05•	–	–	–	–	mA	2
			2.5†	5	−1.75	–	−1.4•	−4	–	−1	–		
			9.5	10	−1.35	–	−1.1•	−2.5	–	−0.75	–		
Diode Test, 100 μA Test Pin	V_{DF}					1.5•			1.5•		1.5•	V	3
Input Current	I_I					–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

▲Maximum noise-free saturated Bipolar output voltage. †Minimum noise-free saturated Bipolar output voltage.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4007AD,CD4007AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	–	35	60	ns	1
			10	–	20	40●		
Low-to-High Level	t_{PLH}		5	–	35	60	ns	1
			10	–	20	40●		
Transition Time: High-to-Low Level	t_{THL}		5	–	50	75	ns	1
			10	–	30	40●		
Low-to-High Level	t_{TLH}		5	–	50	75	ns	1
			10	–	30	40●		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

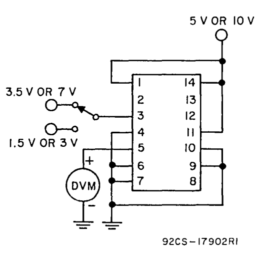

Fig. 2— Noise immunity test circuit.

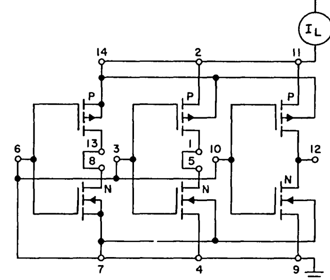

Fig. 3— Quiescent device current test circuit.

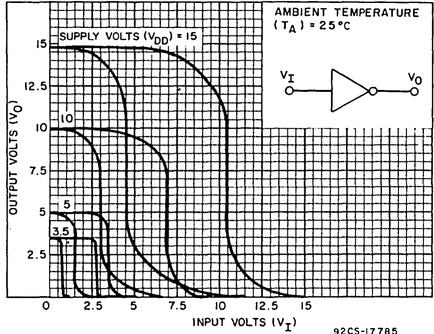

Fig. 4— Min. and max. voltage transfer characteristics for inverter.

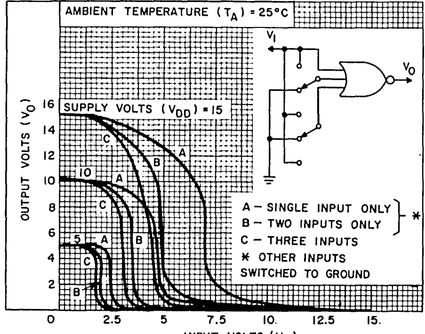

Fig. 5— Typ. voltage transfer characteristics for NOR gate.

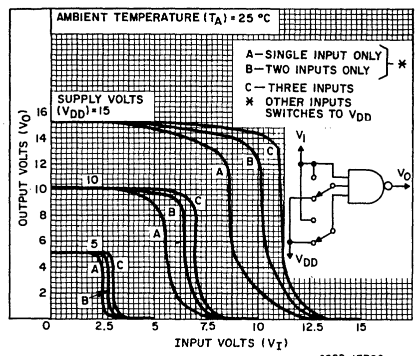

Fig. 6— Typ. voltage transfer characteristics for NAND gate.

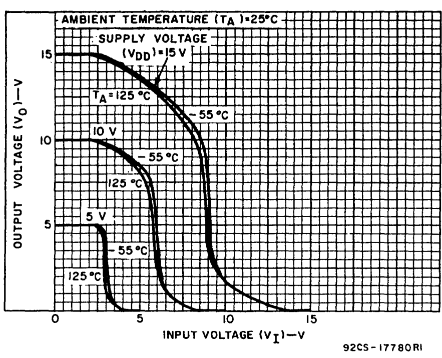

Fig. 7— Typ. voltage transfer characteristics as a function of temp.

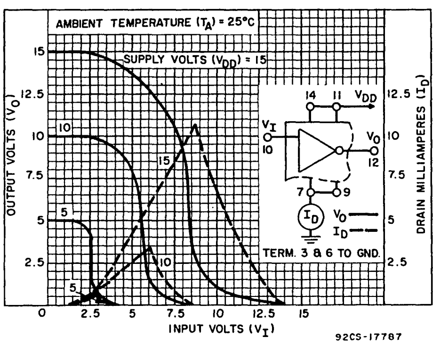

Fig. 8— Typ. current and voltage transfer characteristics for inverter.

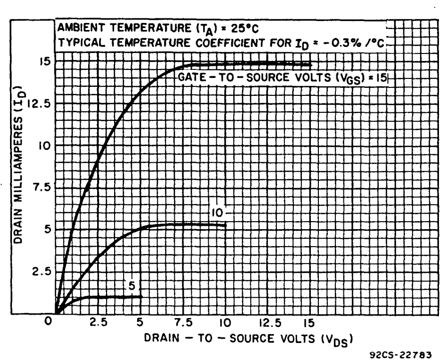

Fig. 9— Minimum n-channel drain characteristics.

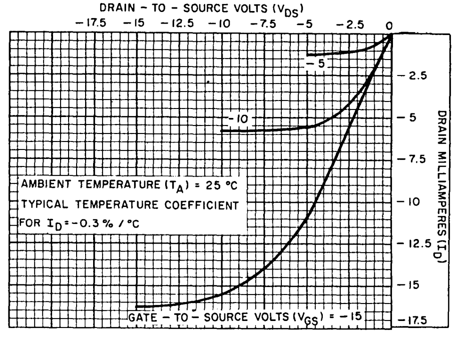

Fig. 10— Minimum p-channel drain characteristics.

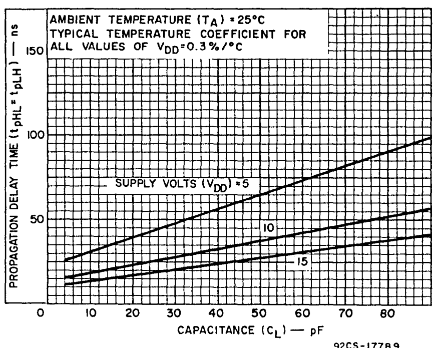

Fig. 11— Typical propagation delay time vs. C_L.

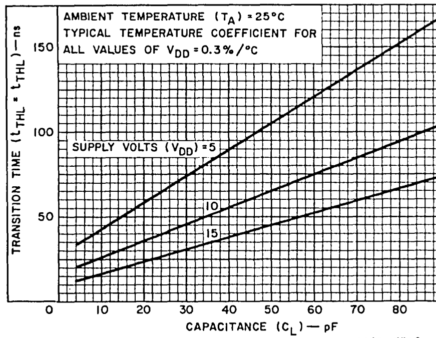

Fig. 12— Typical transition time vs. C_L.

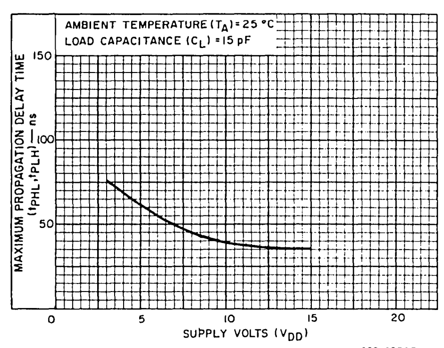

Fig. 13— Maximum propagation delay time vs. V_{DD}.

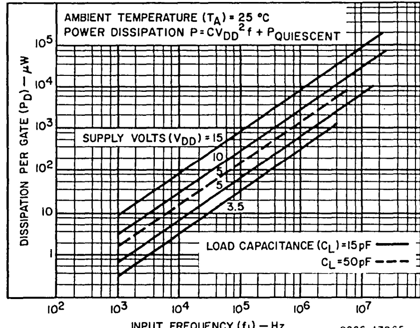

Fig. 14— Typical dissipation characteristics.

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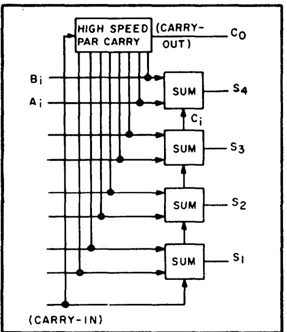
High-Reliability Slash(/) Series

CD4008A/...



High-Reliability COS/MOS Four-Bit Full Adder With Parallel Carry-Out

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **MSI complexity on a single chip . . . 4 Sum Outputs plus parallel Carry Output**
- **High speed operation . . . Carry-In to Carry-Out delay, t_{PHL}, t_{PLH} = 45 ns at C_L = 15 pF**

Applications:

- **Binary addition/arithmetic unit**

RCA CD4008A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4008A types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008A's. CD4008A inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "carry-in" bit from a previous section. CD4008A outputs include the four sum bits, S_1 to S_4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008A section.

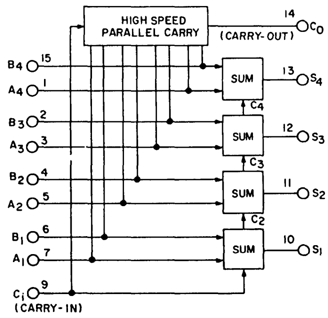


Fig. 1– Logic diagram for type CD4008A.

These devices are electrically and mechanically identical to the standard COS/MOS CD4008A described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4008A	MIL-M-38510/05401

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4008A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

TRUTH TABLE

A_i	B_i	C_i	C_O	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range .... −65 to +150 °C
Operating-Temperature Range .... −55 to +125 °C
DC Supply-Voltage Range:
 ($V_{DD} - V_{SS}$) .... −0.5 to +15 V
Device Dissipation (Per Package) .... 200 mW
All Inputs .... $V_{SS} \leq V_I \leq V_{DD}$

Recommended
 DC Supply-Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V
Recommended
 Input-Voltage Swing .... V_{DD} to V_{SS}
Lead Temperature (During Soldering)
 At distance 1/16" ± 1/32"
 (1.59 ± 0.79 mm) from case
 for 10 s max. .... +265 °C

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4008AD,CD4008AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L			5	–	5	–	0.3	5	–	300	μA	1
				10	–	10•	–	0.5	10•	–	200•		
Quiescent Device Dissipation/Package	P_D			5	–	25	–	1.5	25	–	1500	μW	–
				10	–	100	–	5	100	–	2000		
Output Voltage Low-Level	V_{OL}			3	–	0.55•	–	–	0.5•	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}			3	2.25•	–	2.3•	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = −20 μA			−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}		0.95	5	1.5	–	1.5•	2.25	–	1.4	–	V	2
			2.9	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}		3.6	5	1.4	–	1.5•	2.25	–	1.5	–	V	
			7.2	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current N-Channel	I_DN	Carry Output	0.5	5	0.31	–	0.25•	0.5	–	0.175	–	mA	2
			0.5	10	0.93		0.75•	1.5	–	0.53	–		
		Sum Output	3	5	0.12	–	0.1•	0.2	–	0.07	–		
			3	10	0.31	–	0.25•	0.5	–	0.175	–		
P-Channel	I_DP	Carry Output	4.5	5	−0.31	–	−0.25•	−0.5	–	−0.175	–	mA	
			9.5	10	−0.93	–	−0.75•	−1.5	–	−0.53	–		
		Sum Output	2	5	−0.06•	–	−0.05	−0.06	–	−0.035	–		
			7	10	−0.185	–	−0.15•	−0.3	–	−0.105	–		
Diode Test, 100 μA Test Pin	V_{DF}				–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% test.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4008AD,CD4008AK Min.	Typ.	Max.	UNITS	NOTES
Propagation Delay Time: At Sum Outputs; From Sum Input	t_{PHL}, t_{PLH}	5	–	900	1300	ns	1
		10	–	325	500●		
From Carry Input		5	–	900	1300	ns	
		10	–	325	500		
At Carry Output; From Sum Input		5	–	320	600	ns	–
		10	–	120	200		
From Carry Input		5	–	100	175	ns	1
		10	–	45	75●		
Transition Time: At Sum Outputs	t_{THL}, t_{TLH}	5	–	1250	2200	ns	–
		10	–	550	900		
At Carry Output		5	–	125	225	ns	–
		10	–	45	75		
Input Capacitance	C_I	Any Input	–	10	–	pF	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

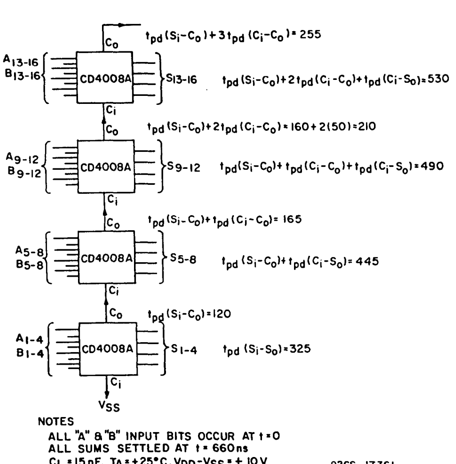


Fig. 2– Typical speed characteristics of a 16-bit adder.

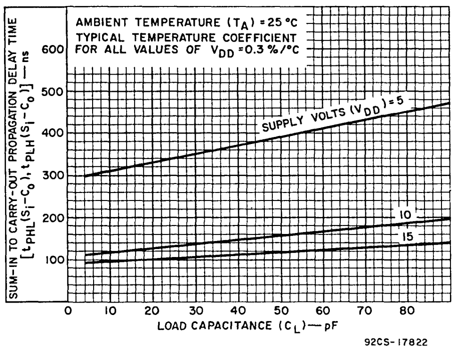


Fig. 3– Sum-in to carry-out propagation delay time vs. C_L.

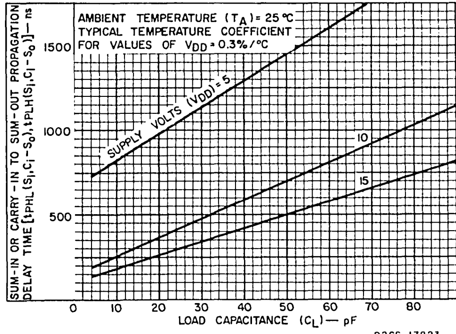


Fig. 4— Sum-in or carry-in to sum-out propagation delay time vs. C_L.

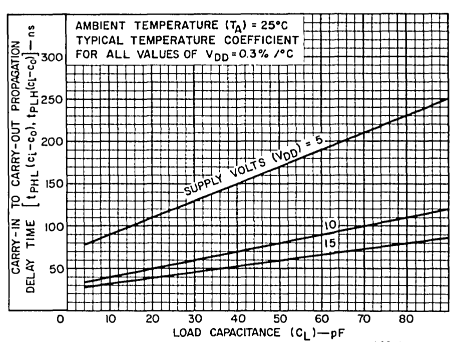


Fig. 5— Carry-in to carry-out propagation delay time vs. C_L.

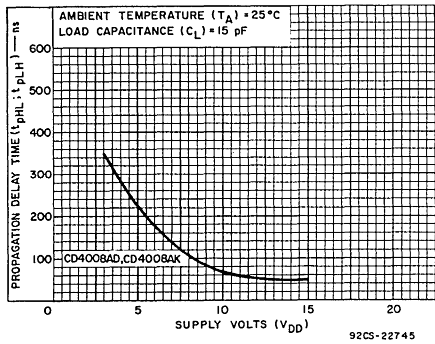


Fig. 6— Max. propagation delay time vs. V_{DD} for carry-in to carry-out.

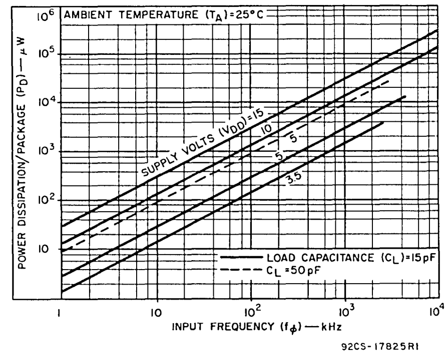


Fig. 7— Typical dissipation characteristics.

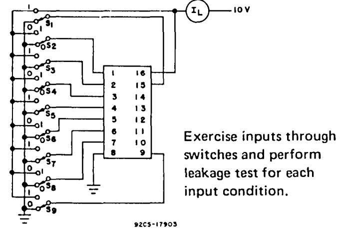


Fig. 8— Quiescent device current test circuit.

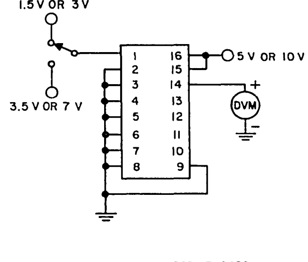


Fig. 9— Noise immunity test circuit.

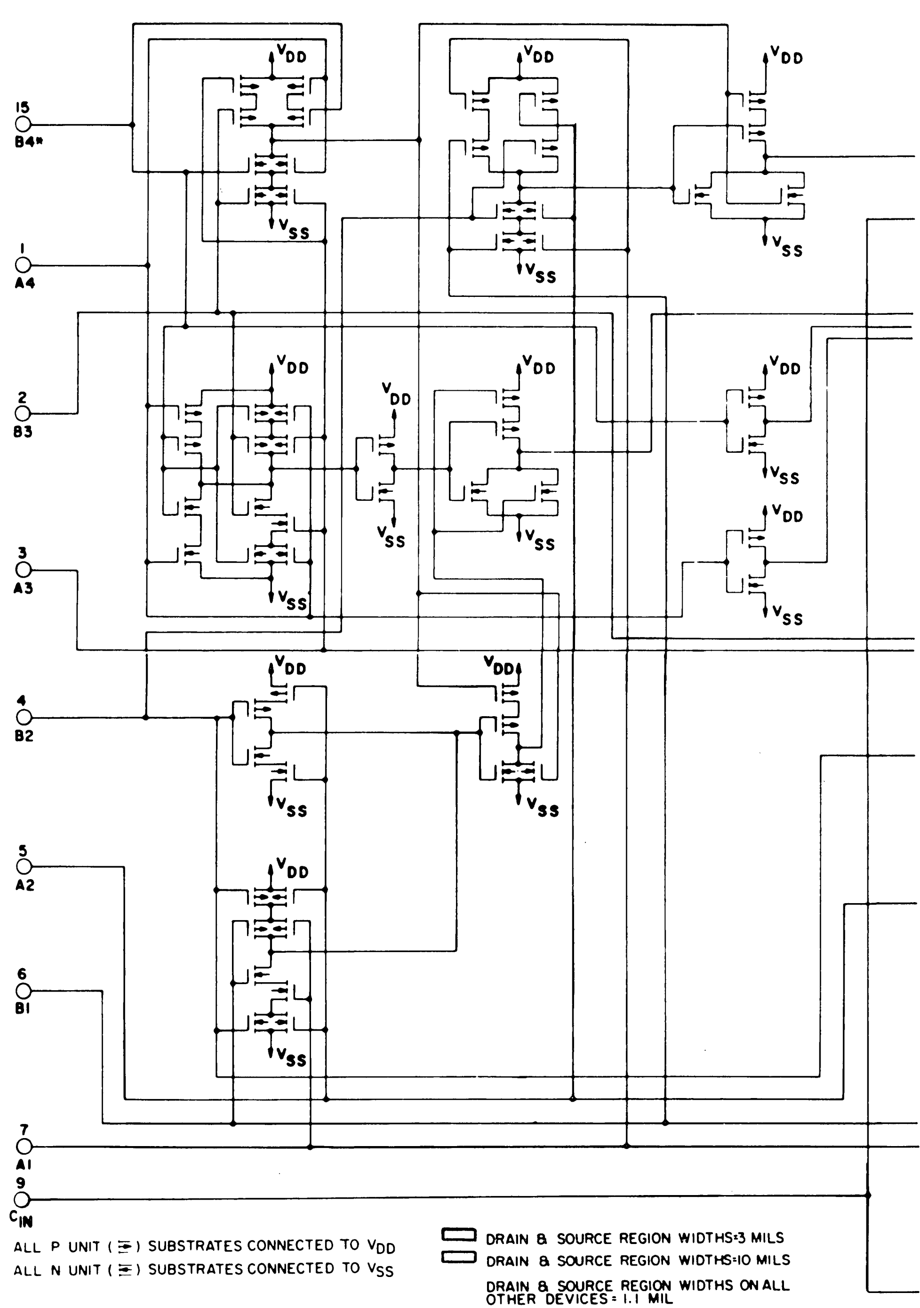
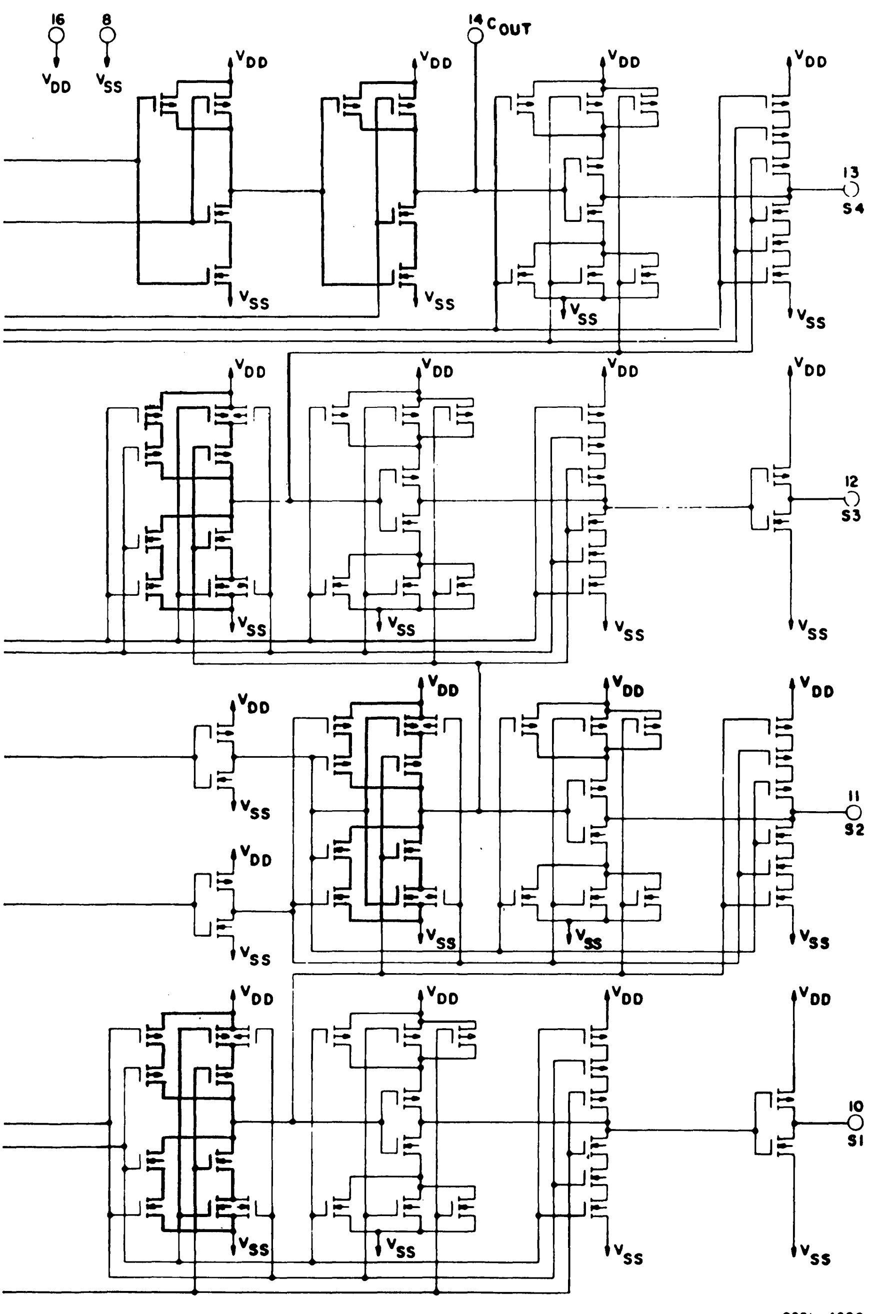


Fig. 10— Schematic Diagram.



16
8
VDD
VSS
14 COUT
VDD
VSS
13
S4
12
S3
11
S2
10
S1
92SL-4299

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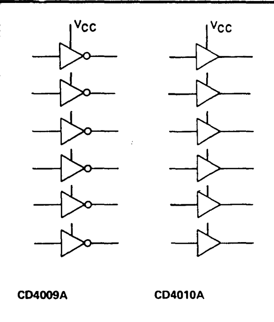
Monolithic Silicon

High-Reliability Slash(/) Series CD4009A/..., CD4010A/...



High-Reliability COS/MOS Hex Buffers/Converters

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Inverting Type: CD4009AD, CD4009AK

Non-Inverting Type: CD4010AD, CD4010AK

Special Features (Each Buffer):

- **High current sinking capability . . . 8 mA (min. at V_{OL} = 0.5 V and V_{DD} = +10 V**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS hex inverter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS logic-level converter**
- **Multiplexer – 1 to 6 or 6 to 1**

CAUTION:
V_{CC} VOLTAGE LEVEL MUST BE EQUAL TO OR LESS THAN V_{DD}. FOR 10.5- TO 15-VOLT SUPPLIES, C_{LOAD} MUST BE EQUAL TO OR LESS THAN 5000 pF.

RCA CD4009A and CD4010A "Slash" (/) Series are high-reliability integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4009A types may be used as a hex COS/MOS inverter, a COS/MOS to DTL or TTL logic-level converter, or a COS/MOS current driver. CD4010A types may be used as a COS/MOS to DTL or TTL hex converter or a COS/MOS current driver.

Conversion ranges are from COS/MOS logic operating at +3 V to +15 V supply levels to DTL or TTL logic operating at +3 V to +6 V supply levels. Conversion to logic output levels greater than +6 V is permitted providing V_{CC}(DTL/TTL) $\leq$ V_{DD}(COS/MOS).

These devices are electrically and mechanically identical with standard COS/MOS types CD4009A and CD4010A described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4009A	MIL-M-38510/05501
CD4010A	MIL-M-38510/05502

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4009A and CD4010A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	–65 to +150	°C
Operating-Temperature Range	–55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	–0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

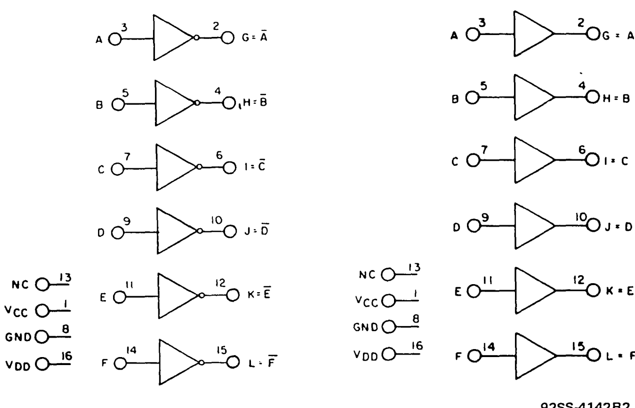


Fig. 1— Logic diagrams for types CD4009A and CD4010A.

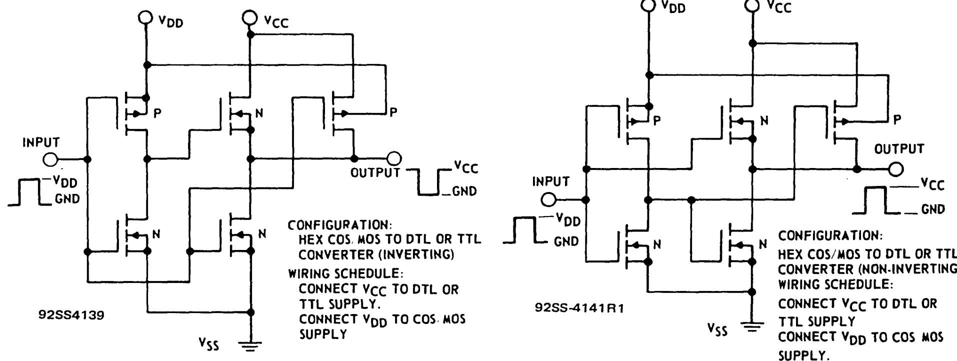


Fig. 2— Schematic diagram for types CD4009A (one of 6 identical stages).

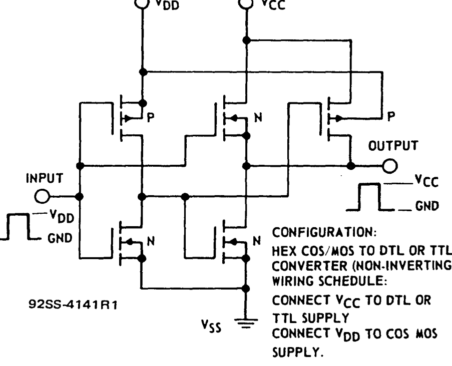


Fig. 3— Schematic diagram for types CD4010A (one of 6 identical stages).

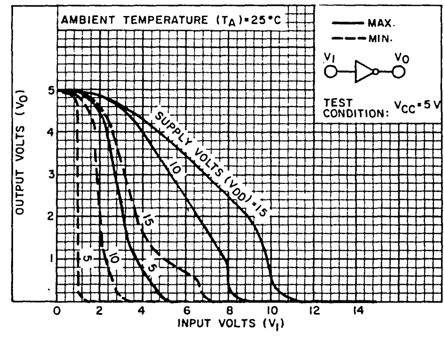


Fig. 4— Min. and max. voltage transfer characteristics — CD4009A.

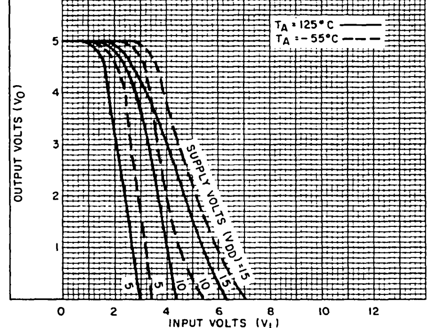


Fig. 5— Typical voltage transfer characteristics as function of temp. — CD4009A.

STATIC ELECTRICAL CHARACTERISTICS (All inputs .... $V_{SS} < V_I < V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4009AD, CD4009AK, CD4010AD, CD4010AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current:	I_L			5	–	0.3	–	0.01	0.3	–	20	μA	1
				10	–	0.5•	–	0.01	0.5•	–	10•		
Quiescent Device Dissipation/Package	P_D			5	–	1.5	–	0.05	1.5	–	100	μW	–
				10	–	5	–	0.1	5	–	100		
Output Voltage: Low-Level	V_{OL}			5	–	0.01	–	0	0.01	–	0.05	V	1
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.6•	–	0.7•		
High-Level	V_{OH}			5	4.99	–	4.99	5	–	4.95	–	V	
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.4•	–	–	14.3•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D=−10 μA			−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	I_D=10 μA			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input) CD4009A	V_{NL}	V_{OH}=3.6 V		5	1	–	1•	2.25	–	0.9	–	V	1
		V_{OH}=7.2 V		10	2•	–	2•	4.5	–	1.9•	–		
CD4010A		V_{OL}=0.95 V		5	1.5	–	1.5•	2.25	–	1.4	–		
		V_{OL}=2.9 V		10	3•	–	3•	4.5	–	2.9•	–		
CD4009A	V_{NH}	V_{OL}=0.95 V		5	1.4	–	1.5•	2.25	–	1.5	–	V	
		V_{OL}=2.0 V		10	2.9•	–	3•	4.5	–	3•	–		
CD4010A		V_{OH}=3.6 V		5	1.4	–	1.5•	2.25	–	1.5	–		
		V_{OH}=7.2 V		10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	$I_D N$	CD4009A & CD4010A	0.4	5	3.75	–	3•	4	–	2.1	–	mA	2
			0.5	10	10	–	8•	10	–	5.6	–		
		CD4009A	0	3	0.4•	–	0.5•	–	–	–	–		
		CD4010A	0	3	0.02•	–	0.025•	–	–	–	–		
P-Channel	$I_D P$	CD4009A & CD4010A	2.5	5	−1.85	–	−1.25•	−1.75	–	−0.9	–		2
			9.5	10	−0.9	–	−0.6•	−0.8	–	−0.4	–		
		CD4009A	3	3	−0.04•	–	−0.05•	–	–	–	–		
		CD4010A	3	3	−0.02•	–	−0.025•	–	–	–	–		
Diode Test	V_{DF}	100 μA Test Pin			–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4009AD,CD4009AK CD4010AD,CD4010AK Min.	Typ.	Max.	UNITS	NOTES
Propagation Delay Time: High-to-Low Level	t_{PHL}	$V_{CC} = V_{DD}$	5	–	15	55	ns	1
			10	–	10	30●		
		V_{DD} = 10 V, V_{CC} = 5 V		–	10	25		
Low-to-High Level	t_{PLH}	$V_{CC} = V_{DD}$	5	–	50	80	ns	
			10	–	25	55●		1
		V_{DD} = 10 V, V_{CC} = 5 V		–	15	30		
Transition Time: High-to-Low Level	t_{THL}	$V_{CC} = V_{DD}$	5	–	20	45	ns	1
			10	–	16	40●		
Low-to-High Level	t_{TLH}	$V_{CC} = V_{DD}$	5	–	80	125	ns	1
			10	–	50	100●		
Input Capacitance (Any Input)	C_I	CD4009A		–	15	–	pF	–
		CD4010A		–	5	–		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

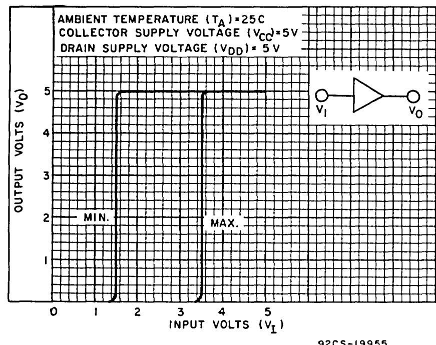


Fig. 6– Min. and max. voltage transfer characteristics (V_{DD} = 5) – CD4010A.

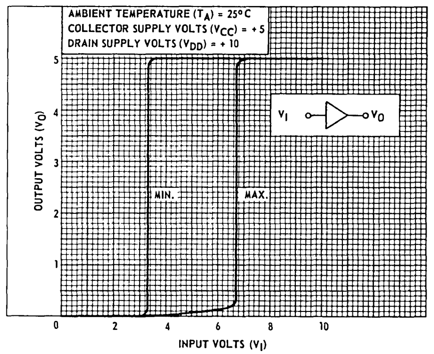


Fig. 7– Min. and max. voltage transfer characteristics (V_{DD} = 10) – CD4010A.

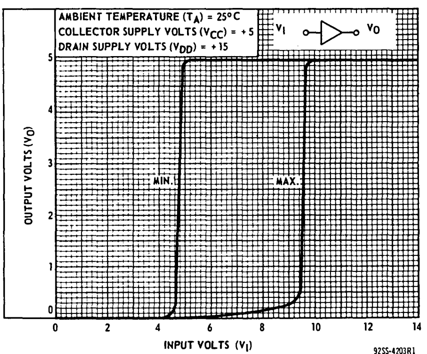


Fig. 8– Min. and max. voltage transfer characteristics (V_{DD} = 15) – CD4010A.

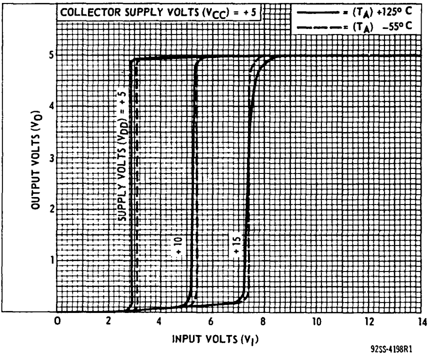


Fig. 9– Typical voltage transfer characteristics as a function of temp. – CD4010A.

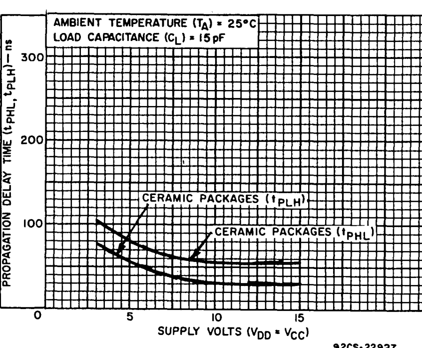


Fig. 10– Maximum propagation delay time vs. V_{DD} – CD4010A.

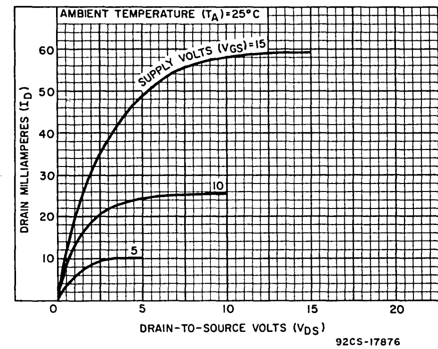


Fig. 11– Minimum n-channel drain characteristics.

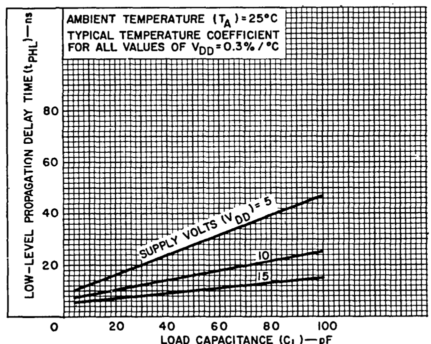


Fig. 12– Typical high-to-low level propagation delay time vs. C_L – CD4009A, CD4010A.

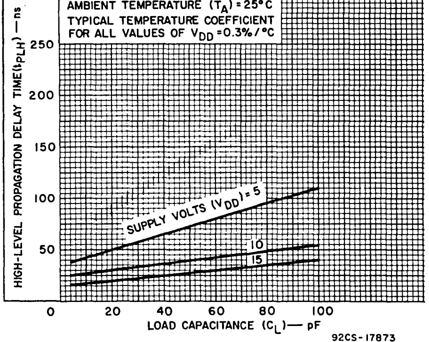


Fig. 13– Typical low-to-high level propagation delay time vs. C_L – CD4009A, CD4010A.

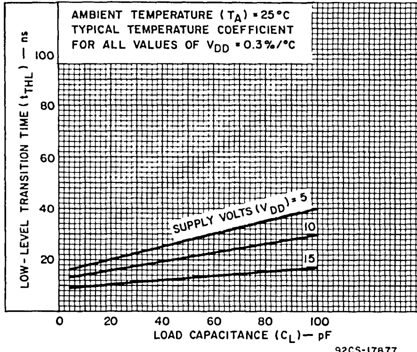


Fig. 14— Typical high-to-low level transition time vs. C_L – CD4009A, CD4010A.

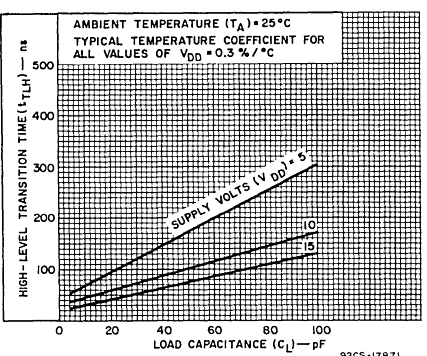


Fig. 15— Typical low-to-high level transition time vs. C_L – CD4009A, CD4010A.

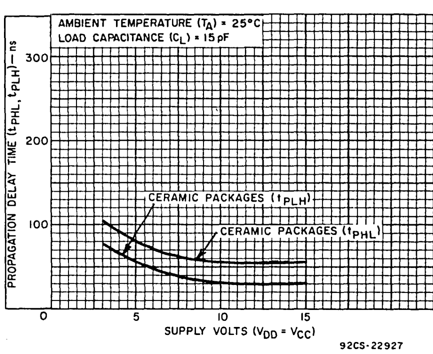


Fig. 16— Maximum propagation delay time vs. V_{DD} – CD4009A.

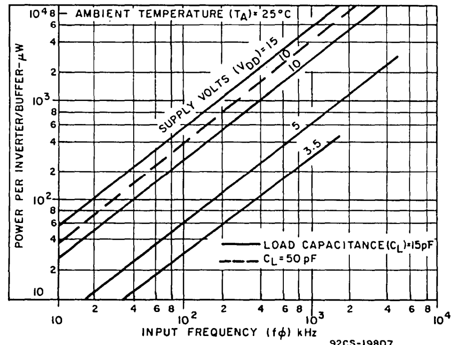


Fig. 17— Typical dissipation characteristics – CD4009A, CD4010A.

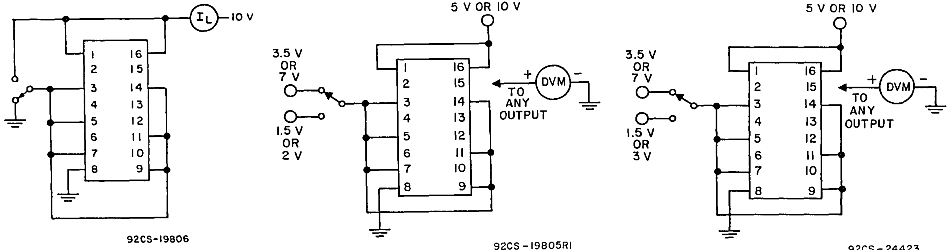


Fig. 18— Quiescent device current test circuit.

Fig. 19— Noise immunity test circuit for CD4009A.

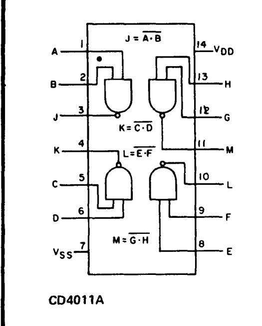
Fig. 20— Noise immunity test circuit for CD4010A.

Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4011A/..., CD4012A/..., CD4023A/...



CD4011A

High-Reliability COS/MOS NAND Gates

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Quad 2 Input --- CD4011AD, CD4011AK
Dual 4 Input --- CD4012AD, CD4012AK
Triple 3 Input --- CD4023AD, CD4023AK

Special Features:

- **Medium speed operation . . . $t_{PHL} = t_{PLH}$ = 25 ns (typ.) at C_L = 15 pF**
- **Low "high"- and "low"-level output impedance . . . 400 and 800 Ω (typ.), respectively, at $V_{DD} - V_{SS}$ = 10 V**

RCA CD4011A, CD4012A, and CD4023A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. The combination of these devices and the RCA NOR positive logic gate types CD4000A, CD4001A, CD4002A, and CD4025A can account for appreciable package count savings in various logic function configurations. These devices are electrically and mechanically identical with standard COS/MOS types CD4011A, CD4012A, and CD4023A described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

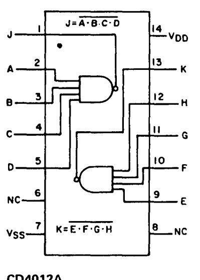
RCA Designation	MIL-M-38510 Designation
CD4011A	MIL-M-38510/05001
CD4012A	MIL-M-38510/05002
CD4023A	MIL-M-38510/05003

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

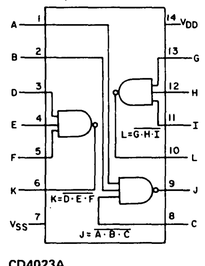
For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the following page.

The CD4011A, CD4012A, and CD4023A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).



CD4012A



CD4023A

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

92CS-15970

Fig. 1– Schematic diagram for type CD4012A.

Fig. 2– Schematic diagram for type CD4011A.

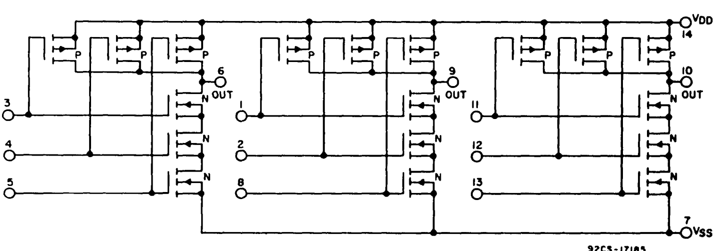


Fig. 3– Schematic diagram for type CD4023A.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS CD4011AD, CD4012AD, CD4023AD, CD4011AK, CD4012AK, CD4023AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L			5	–	0.05	–	0.001	0.05	–	3	µA	1
				10	–	0.1•	–	0.001	0.1•	–	2•		
Quiescent Device Dissipation/Package	P_D			5	–	0.25	–	0.005	0.25	–	15	µW	–
				10	–	1	–	0.01	1	–	20		
Output Voltage Low-Level	V_{OL}			5	–	0.01	–	0	0.01	–	0.05	V	1
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.6•	–	0.7•		
High-Level	V_{OH}			5	4.99	–	4.99	5	–	4.95	–	V	1
				10	9.99	–	9.99	10	–	9.95	--		
				15	–	–	14.4•	–	–	14.3•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -10\ \mu A$			−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	$I_D = 10\ \mu A$			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity Any Input	V_{NL}		3.6	5	1.5	–	1.5•	2.25	–	1.4	–	V	2
			7.2	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix	V_{NH}		0.95	5	1.4	–	1.5•	2.25	–	1.5	–	V	2
			2.9	10	2.9•	--	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN	CD4011A, CD4023A Series	0	3	0.02•	–	0.025•	–	–	–	–	mA	2
			0.5	5	0.31	–	0.25•	0.5	–	0.175	–		
			0.5	10	0.62	–	0.5•	0.6	–	0.35	–		
		CD4012A Series	0	3	0.02•	–	0.025•	–	–	–	–	mA	2
			0.5	5	0.15	–	0.12•	0.25	–	0.085	–		
			0.5	10	3.1	--	0.25•	0.6	–	0.175	–		
P-Channel	I_DP		3	3	−0.02•	–	−0.025•	–	--	–	–	mA	2
			4.5	5	−0.31	–	−0.25•	−0.5	–	−0.175	–		
			9.5	10	−0.75	–	−0.6•	−1.2	–	−0.4	–		
Diode Test	V_{DF}	100 µA Test Pin			–	1.5•	--	–	1.5•	–	1.5•	V	3
Input Current	I_I				–	–	–	10	--	–	–	pA	--

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or a one output only.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4011AD, AK CD4012AD, AK CD4023AD, AK Min.	Typ.	Max.	UNITS	NOTES
Propagation Delay Time: Low-to-High Level	t_{PLH}	5	–	50	75	ns	1
		10	–	25	40●		
High-to-Low Level CD4011A and CD4023A Series	t_{PHL}	5	–	50	75	ns	1
		10	–	25	40●		
CD4012A Series		5	–	100	150	ns	1
		10	–	50	75●		
Transition Time: Low-to-High Level	t_{TLH}	5	–	75	100	ns	1
		10	–	40	60●		
High-to-Low Level CD4011A and CD4023A Series	t_{THL}	5	–	75	125	ns	1
		10	–	50	75●		
CD4012A Series		5	–	250	375	ns	1
		10	–	125	200●		
Input Capacitance	C_I	Any Input	–	5	–	pF	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

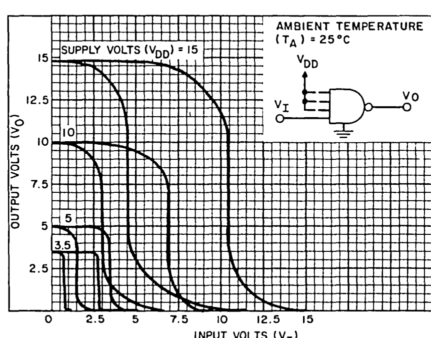


Fig. 4— Min. and max. voltage transfer characteristics.

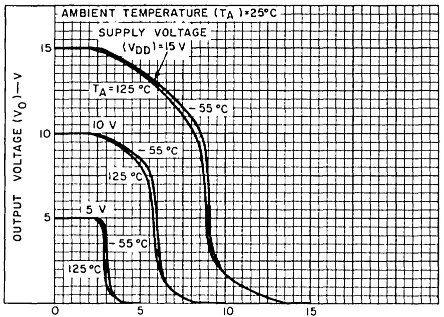


Fig. 5— Typical voltage transfer characteristics as a function of temperature.

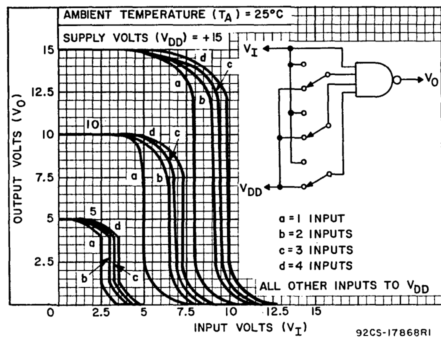


Fig. 6— Typical multiple input switching transfer characteristics for CD4012A.

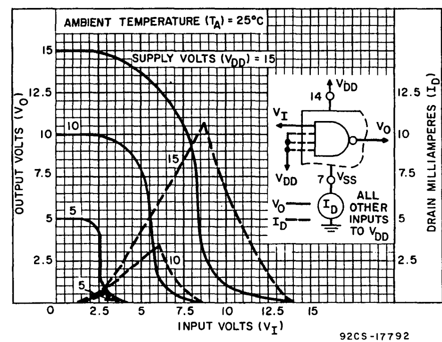


Fig. 7— Typical current and voltage transfer characteristics.

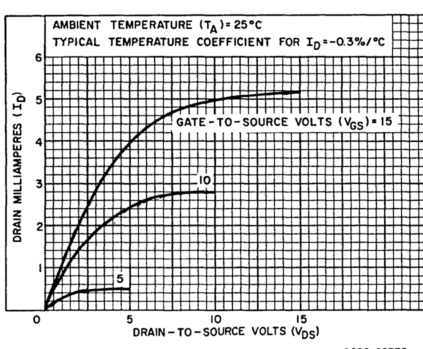


Fig. 8— Minimum n-channel drain characteristics — CD4011A and CD4023A.

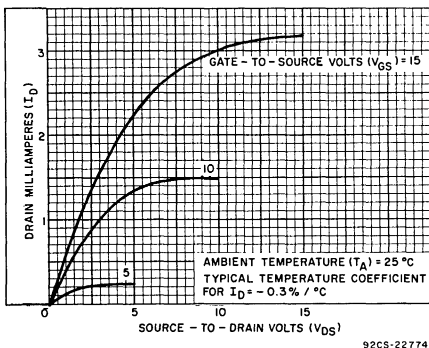


Fig. 9— Minimum n-channel drain characteristics — CD4012A.

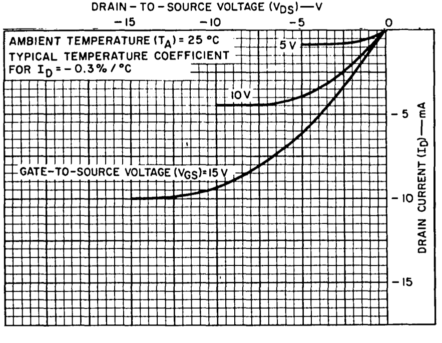


Fig. 10— Minimum p-channel drain characteristics.

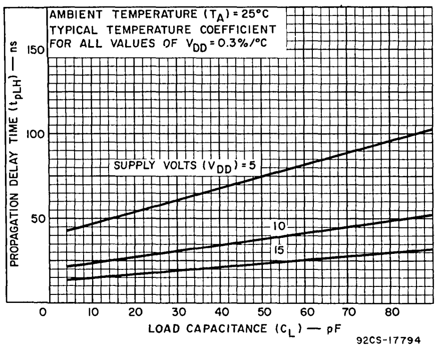


Fig. 11— Typical low-to-high level propagation delay time vs. C_L.

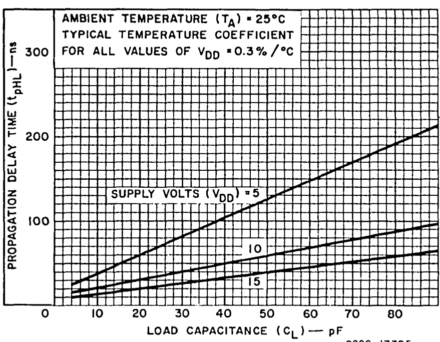


Fig. 12— Typical high-to-low level propagation delay time vs. C_L – CD4011A and CD4023A.

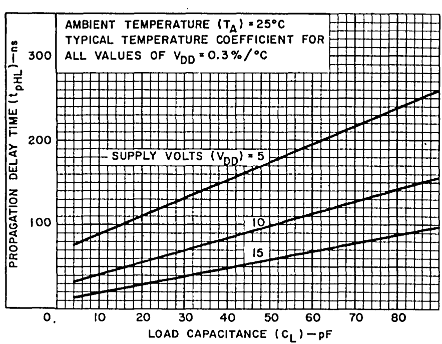


Fig. 13— Typical high-to-low level propagation delay time vs. C_L – CD4012A.

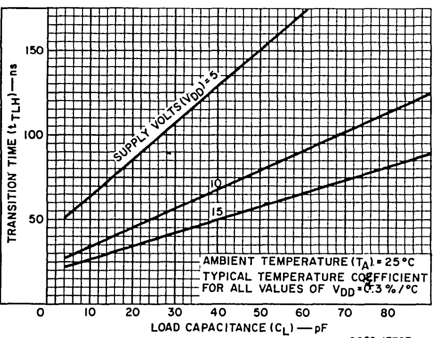


Fig. 14— Typical low-to-high transition time vs. C_L.

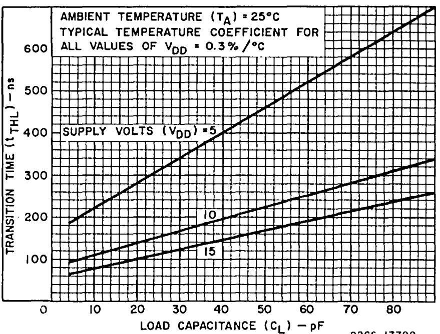


Fig. 15— Typical high-to-low level transition time vs. C_L – CD4011A and CD4023A.

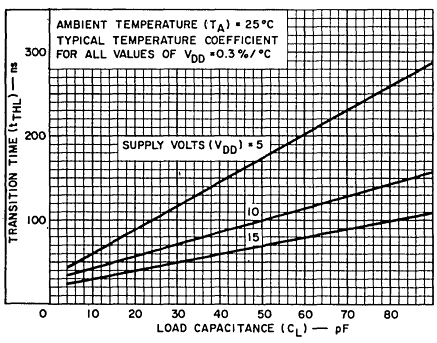


Fig. 16— Typical high-to-low level transition time vs. C_L – CD4012A.

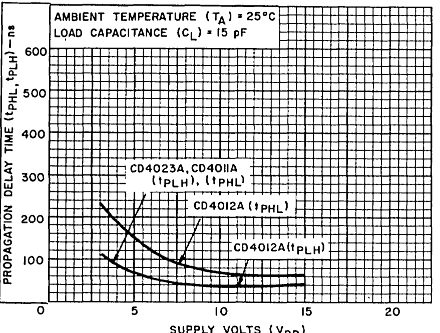


Fig. 17— Minimum propagation delay time vs. V_{DD}.

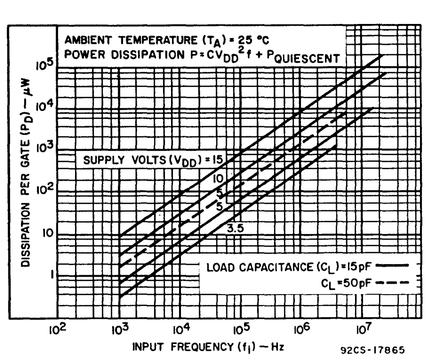
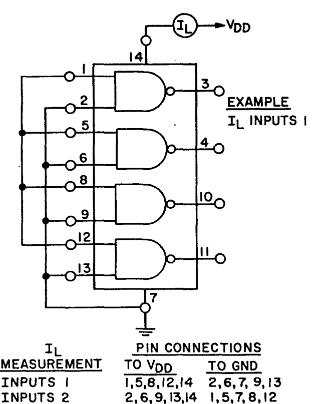
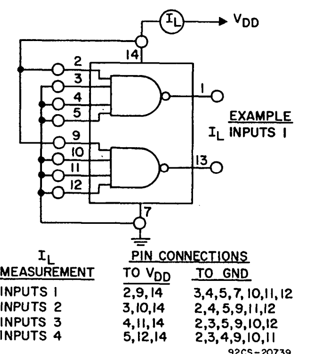


Fig. 18— Typical dissipation characteristics.



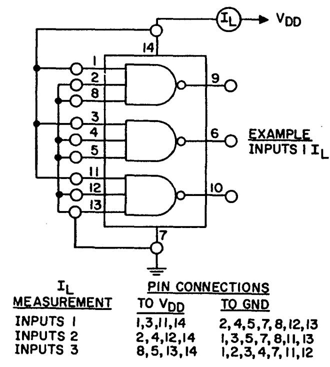
IL MEASUREMENT	PIN CONNECTIONS TO VDD	TO GND
INPUTS 1	1,5,8,12,14	2,6,7,9,13
INPUTS 2	2,6,9,13,14	1,5,7,8,12

Fig. 19— Quiescent device current test circuit for CD4011A.



IL MEASUREMENT	PIN CONNECTIONS TO VDD	TO GND
INPUTS 1	2,9,14	3,4,5,7,10,11,12
INPUTS 2	3,10,14	2,4,5,9,11,12
INPUTS 3	4,11,14	2,3,5,9,10,12
INPUTS 4	5,12,14	2,3,4,9,10,11

Fig. 20— Quiescent device current test circuit for CD4012A.



IL MEASUREMENT	PIN CONNECTIONS TO VDD	TO GND
INPUTS 1	1,3,11,14	2,4,5,7,8,12,13
INPUTS 2	2,4,12,14	1,3,5,7,8,11,13
INPUTS 3	8,5,13,14	1,2,3,4,7,11,12

Fig. 21— Quiescent device current test circuit for CD4023A.

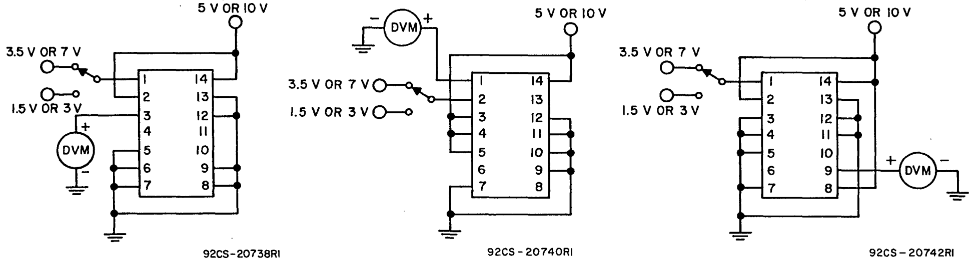


Fig. 22—Noise-immunity test circuit for CD4011A.

Fig. 23—Noise-immunity test circuit for CD4012A

Fig. 24—Noise-immunity test circuit for CD4023A.

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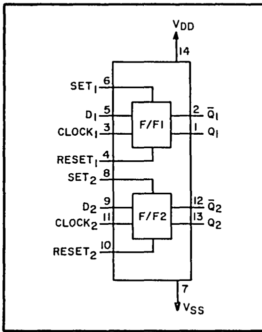
Monolithic Silicon

High-Reliability Slash(/) Series CD4013A/...



High-Reliability Dual "D"-Type Flip-Flop With Set-Reset Capability

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Static flip-flop operation . . . retains state indefinitely with clock level either "high" or "low"**
- **Medium speed operation . . . 10 MHz (typ.) clock toggle rate at $V_{DD} - V_{SS} = 10$ V**
- **Low "high"- and "low"-output impedance . . . 400 Ω and 200 Ω, respectively, at $V_{DD} - V_{SS} = 10$ V**

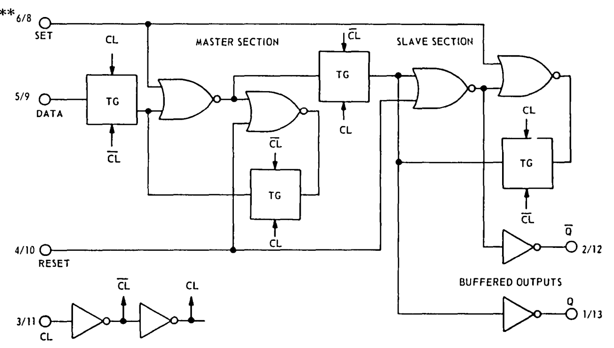
Applications:

- **Register, counters, control circuits**

RCA CD4013A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. CD4013A types consist of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\bar{Q}$" outputs. These devices can be used for shift register applications, and, by connecting "$\bar{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the "Q" output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

This device is electrically and mechanically identical with standard COS/MOS CD4013A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4013A	MIL-M-38510/05101



TRUTH TABLE

CL▲	D	R	S	Q	$\bar{Q}$	
⟋ (rising)	0	0	0	0	1	
⟋ (rising)	1	0	0	1	0	
⟍ (falling)	X	0	0	Q	$\bar{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

▲ = LEVEL CHANGE

X = DON'T CARE CASE

** = FF1/FF2 TERMINAL ASSIGNMENTS

92SS-4386

Fig. 1— Logic diagram and truth table (one of two identical flip-flops).

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4013A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	–65 to +150	°C
Operating-Temperature Range	–55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	–0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

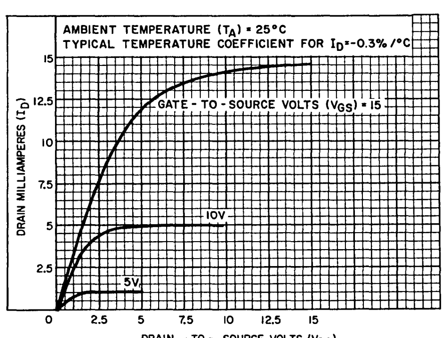


Fig. 2— Minimum n-channel drain characteristics.

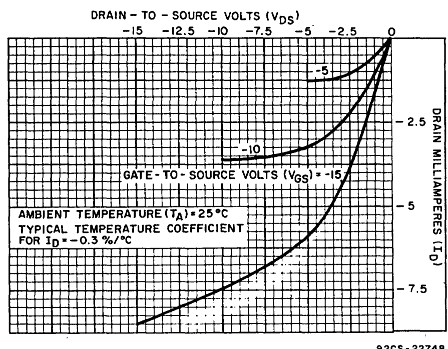


Fig. 3— Minimum p-channel drain characteristics.

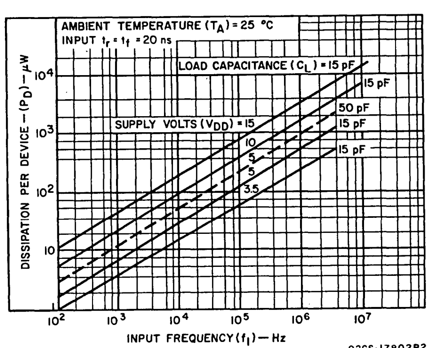


Fig. 4— Typical dissipation characteristics.

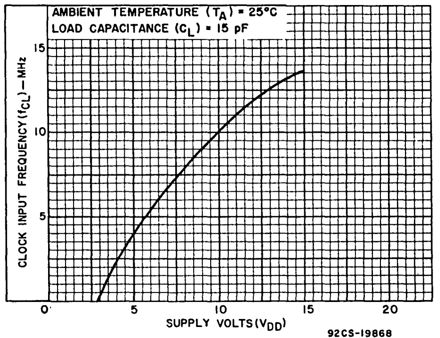


Fig. 5— Typical clock frequency vs. V_{DD}.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4013AD,CD4013AK							UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
		V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.			
Quiescent Device Current	I_L		5	–	1	–	0.005	1	–	60	μA	10	1
			10	–	2•	–	0.005	2•	–	40•			
Quiescent Device Dissipation/Package	P_D		5	–	5	–	0.025	5	–	300	μW	6	–
			10	–	20	–	0.05	20	–	400			
Output Voltage Low-Level	V_{OL}		3	–	0.55•	–	–	0.5•	–	–	V	–	1
			5	–	0.01	–	0	0.01	–	0.05			
			10	–	0.01	–	0	0.01	–	0.05			
			15	–	–	–	–	0.5•	–	0.55•			
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	–	–	V	–	1
			5	4.99	–	4.99	5	–	4.95	–			
			10	9.99	–	9.99	10	–	9.95	–			
			15	–	–	14.5•	–	–	14.45•	–			
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = 20 μA		−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	–	2
P-Channel	$V_{TH}P$	I_D = 20 μA		0.7•	3•	0.7•	1.5	3•	0.3•	3•			
Noise Immunity (All Inputs)	V_{NL}	0.8	5	1.5	–	1.5•	2.25	–	1.4	–	V	11	1
		1	10	3•	–	3•	4.5	–	2.9•	–			
For Definition, See Appendix	V_{NH}	4.2	5	1.4	–	1.5•	2.25	–	1.5	–	V		
		9	10	2.9•	–	3•	4.5	–	3•	–			
Output Drive Current: N-Channel	I_DN	0.5	5	0.65	–	0.5•	1	–	0.35	–	mA	2, 4	2
		0.5	10	1.25	–	1•	2.5	–	0.75	–			
P-Channel	I_DP	4.5	5	−0.31	–	−0.25•	−0.5	–	−0.175	–	mA	3, 5	2
		9.5	10	−0.8	–	−0.65•	−1.3	–	−0.45	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	1.5•	–	–	1.5•	–	1.5•	V	–	3
Input Current	I_I			–	–	–	10	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

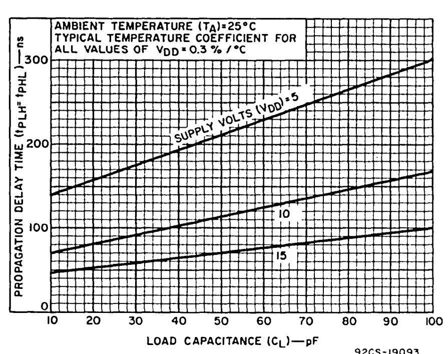


Fig. 6— Typical propagation delay time vs. C_L.

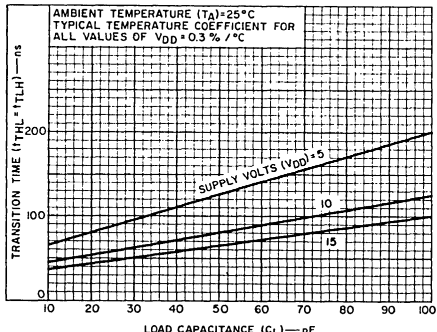


Fig. 7— Typical transition time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $C_L = 15$ pF, and input rise an times = 20 ns except t_rCL, t_fCL

Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/^oC$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4013AD, CD4013AK Min.	Typ.	Max.	UNITS	NOTES
CLOCKED OPERATION							
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	150	300	ns	1
		10	–	75	110●		
Transition Time	t_{THL}, t_{TLH}	5	–	75	125	ns	–
		10	–	50	70		
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	125	200	ns	–
		10	–	50	80		
Clock Rise & Fall Time	*t_rCL, t_fCL	5	–	–	15	μs	1
		10	–	–	5●		
Set-Up Time		5	–	20	40	ns	–
		10	–	10	20		
Maximum Clock Frequency	f_{CL}	5	2.5	4	–	MHz	1
		10	7●	10	–		
Input Capacitance	C_I	Any Input	–	5	–	pF	–
SET & RESET OPERATION							
Propagation Delay Time	$t_{PHL(R)}$, $t_{PLH(R)}$	5	–	175	300	ns	–
		10	–	75	110		
Minimum Set and Reset Pulse Widths	$t_{WH(S)}$, $t_{WH(R)}$	5	–	125	250	ns	–
		10	–	50	100		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

* If more than one unit is cascaded in a parallel clocked operation, t_fCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

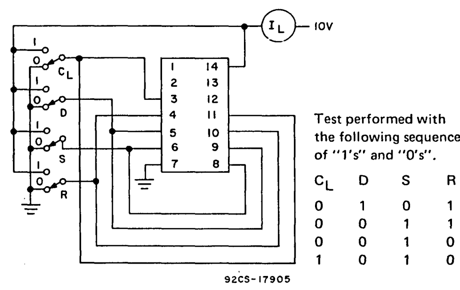


Fig. 8– Quiescent device current test circuit.

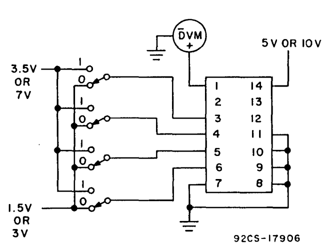


Fig. 9–Noise immunity test circuit.

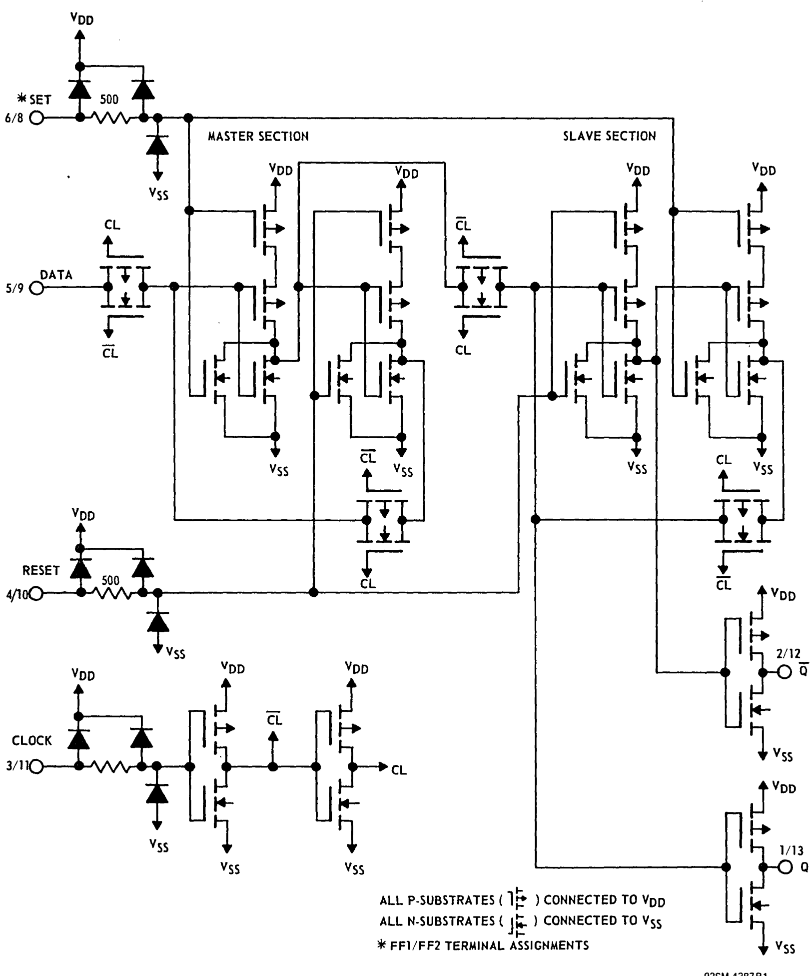


Fig. 11– Schematic diagram (one of two identical flip-flops).

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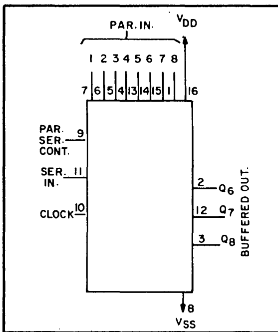
High-Reliability Slash(/) Series CD4014A/...



High-Reliability COS/MOS 8-Stage Static Shift Register

Synchronous Parallel or Serial Input/Serial Output

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation...... 5 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10 V**
- **Fully static operation**
- **MSI complexity on a single chip...... 8 master-slave flip-flops plus output buffering and control gating**

Applications:

- **Synchronous parallel input/serial output data queueing**
- **Parallel to serial data conversion**
- **General purpose register**

RCA CD4014A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4014A types are 8-stage parallel-input/serial output registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7.

Parallel as well as serial entry is made into the register synchronous with the positive clock line transition and under control of the Parallel/Serial Control input. When the Parallel/Serial Control input is "low", data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the Parallel/Serial Control input is "high", data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. Register expansion using multiple CD4014A packages is permitted.

These types are electrically and mechanically identical to standard COS/MOS CD4014A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4014A	MIL-M-38510/05702

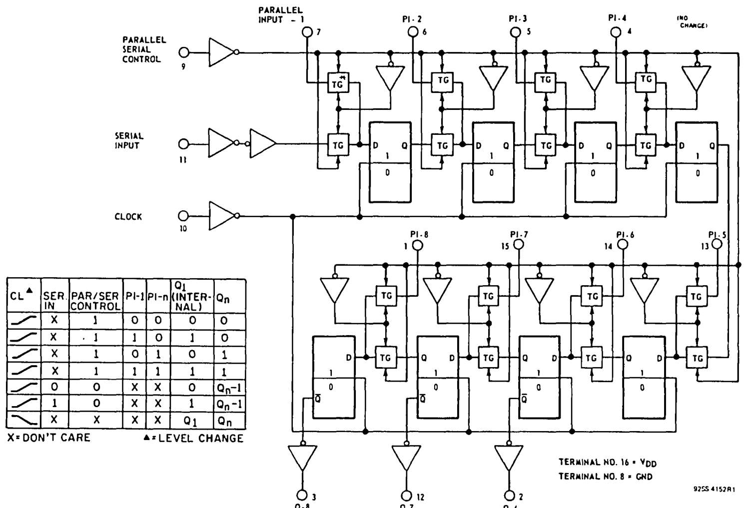
The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4014A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150	°C
Operating-Temperature Range	−55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C



CL▲	SER. IN	PAR/SER CONTROL	PI-1	PI-n	Q_1 (INTER-NAL)	Q_n
_/‾	X	1	0	0	0	0
_/‾	X	1	1	0	1	0
_/‾	X	1	0	1	0	1
_/‾	X	1	1	1	1	1
_/‾	0	0	X	X	0	Q_{n-1}
_/‾	1	0	X	X	1	Q_{n-1}
‾_	X	X	X	X	Q_1	Q_n

X = DON'T CARE ▲ = LEVEL CHANGE

Fig. 1—Logic block diagram and truth table.

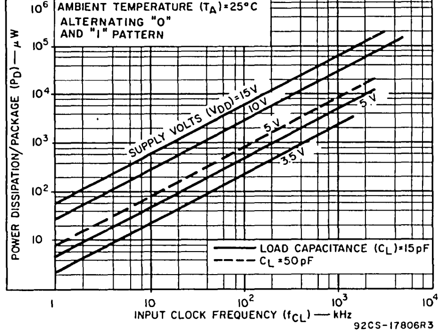


Fig. 2—Typ. dissipation characteristics.

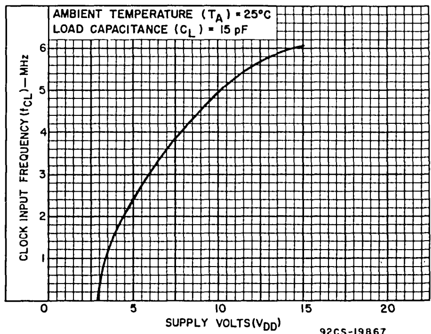


Fig. 3—Typ. clock frequency vs. V_{DD}

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS CD4014AD, CD4014AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L			5	–	5	–	0.5	5	–	300	μA	1
				10	–	10●	–	1	10●	–	300●		
Quiescent Device Dissipation/Package	P_D			5	–	25	–	2.5	25	–	1500	μW	–
				10	–	100	–	10	100	–	2000		
Output Voltage Low Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.5●	–	0.55●		
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.5●	–	–	14.45	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = −20 μA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V	2
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7●	3●	0.7●	1.5	3●	0.3●	3●		
Noise Immunity (Any Input)	V_{NL}		0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V	1
			0.5	10	3●	–	3●	4.5	–	2.9●	–		
For Definition, See Appendix SSD-207	V_{NH}		4.2	5	1.4	–	1.5●	2.25	–	1.5	–	V	
			9.5	10	2.9●	–	3●	4.5	–	3●	–		
Output Drive Current: N-Channel	I_DN		0.5	5	0.15	–	0.12●	0.3	–	0.085	–	mA	2
			0.5	10	0.31	–	0.25●	0.5	–	0.175	–		
P-Channel	I_DP		4.5	5	−0.1	–	−0.08●	−0.16	–	−0.055	–	mA	2
			9.5	10	−0.25	–	−0.2●	−0.44	–	−0.14	–		
Diode Test, 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

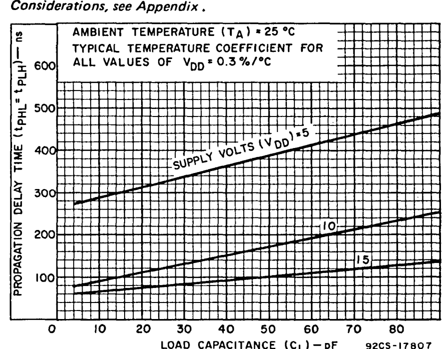


Fig. 4—Typ. propagation delay time vs. C_L.

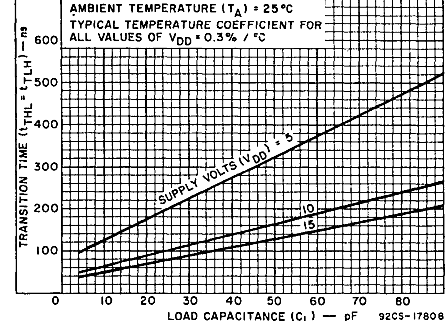


Fig. 5—Typ. transition time vs. C_L.

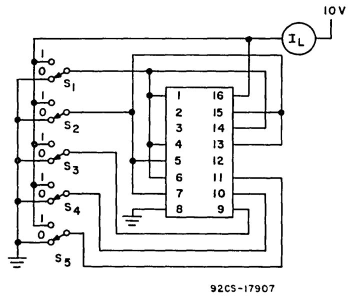
DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25^oC$, $C_L = 15$ pF, and input rise and fall times = 20 ns except t_rCL, t_fCL*
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4014AD, CD4014AK Min.	Typ.	Max.	UNITS	NOTES
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	300	750	ns	1
		10	–	100	225●		
Transition Time	t_{THL}, t_{TLH}	5	–	150	300	ns	–
		10	–	75	125		
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	200	500	ns	–
		10	–	100	175		
Clock Rise & Fall Time	t_{rCL}, t_{fCL}*	5	–	–	15	μs	1
		10	–	–	15●		
Set-Up Time		5	–	100	350	ns	–
		10	–	50	80		
Maximum Clock Frequency	f_{CL}	5	1	2.5	–	MHz	1
		10	3●	5	–		
Input Capacitance	C_I	Any Input	–	5	–	pF	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

* If more than one unit is cascaded t_fCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the output driving stage for the estimated capacitive load.



Test performed with the following sequence of "1's" and "0's"

	S_1	S_2	S_3	S_4	S_5
Don't Test	0	1	1	0	0
Test	0	1	1	1	0
Test	1	0	0	0	0
Test	1	0	1	1	1
Test	1	0	0	0	1

Fig. 6—Quiescent device current test circuit.

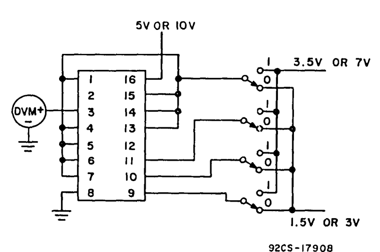


Fig. 7—Noise immunity test circuit.

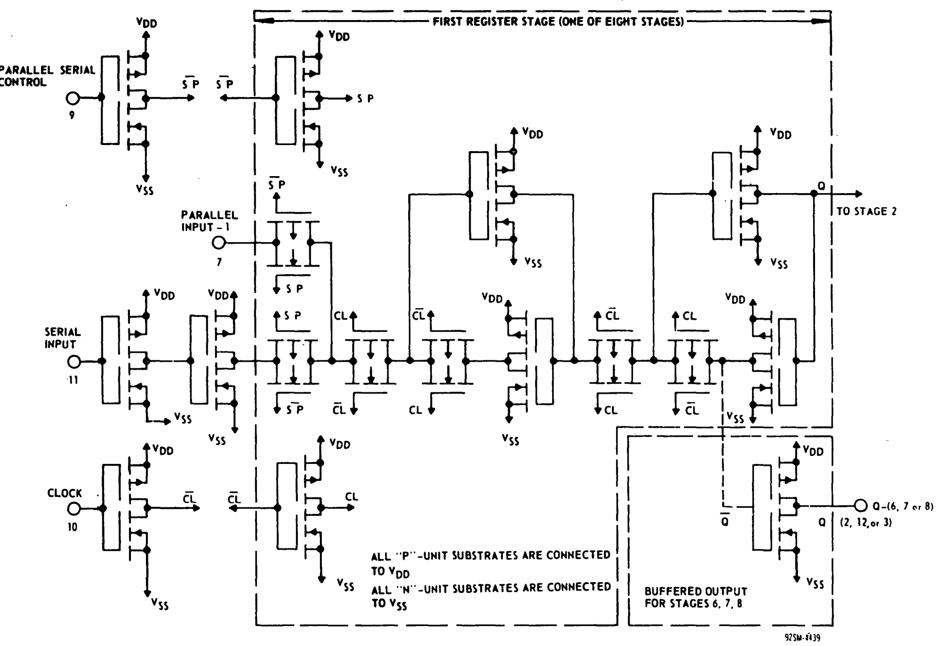


Fig. 8—Schematic diagram — CD4014A.

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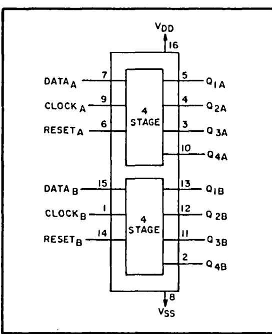
CD4015A/...



High-Reliability COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- **Medium speed operation...... 5 MHz (typ.) clock rate at $V_{DD} - V_{SS} = 10$ V**
- **Fully static operation**
- **MSI complexity on a single chip...... 8 master-slave flip-flops plus output buffering**

Applications

- **Serial-input/parallel-output data queueing**
- **Serial to parallel data conversion**
- **General purpose register**

RCA CD4015A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. CD4015A types consist of two identical, independent, 4-stage serial input/parallel-output registers. Each register has independent "Clock" and "Reset" inputs as well as a single serial "Data" input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015A package, or to more than 8 stages using additional CD4015A packages is possible.

These devices are electrically and mechanically identical with standard COS/MOS CD4015A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4015A	MIL-M-38510/05703

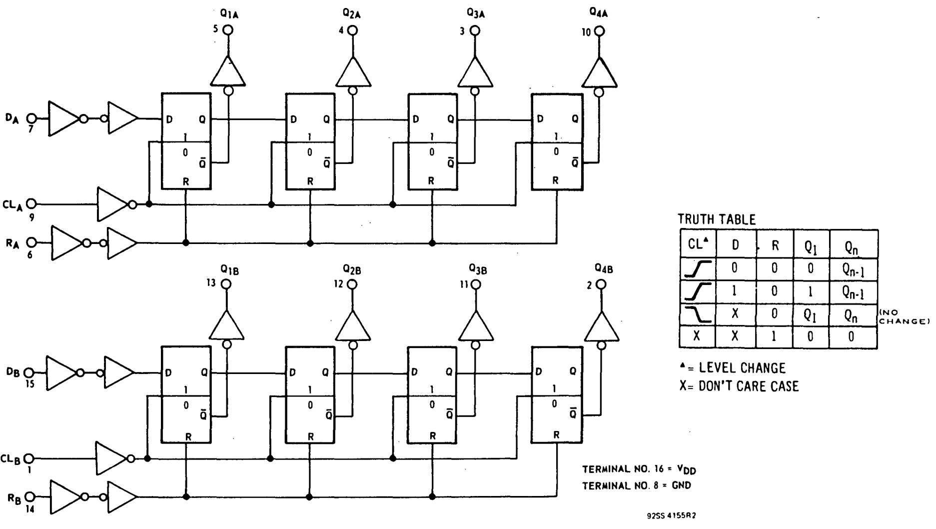
The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4015A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150	°C
Operating-Temperature Range	−55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C



CL▲	D	R	Q1	Qn
_/‾	0	0	0	Qn-1
_/‾	1	0	1	Qn-1
‾_	X	0	Q1	Qn (NO CHANGE)
X	X	1	0	0

Fig. 1—Logic diagram and truth table.

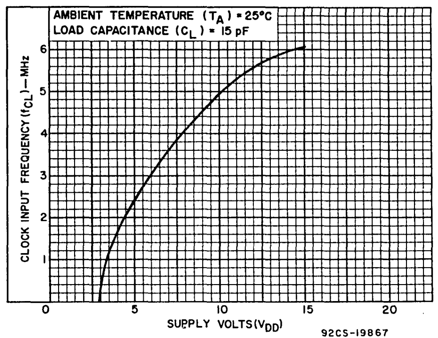


Fig. 2—Typ. clock frequency vs. V_{DD}.

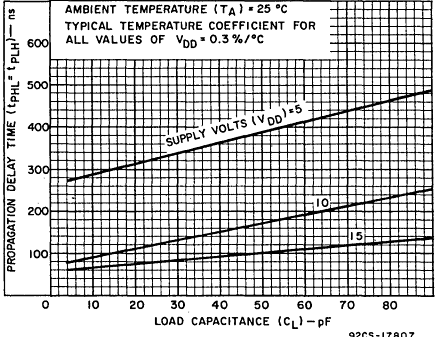


Fig. 3—Typ. propagation delay time vs. C_L.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$)*
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4015AD, CD4015AK							UNITS	NOTES
		V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L		5	–	5	–	0.5	5	–	300	μA	1
			10	–	0.5•	–	1	0.5•	–	10•		
Quiescent Device Dissipation/Package	P_D		5	–	25	–	2.5	2.5	–	1500	μW	–
			10	–	5	–	10	5	–	100		
Output Voltage Low-Level	V_{OL}		3	–	0.55•	–	–	0.5•	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	–	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$		−0.3•	−3•	−0.7•	−1.5	−3•	−0.7•	−3•	V	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$		0.3•	3•	0.7•	1.5	3•	0.7•	3•		
Noise Immunity (Any Input)	V_{NL}	0.8	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
		1	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}	4.2	5	1.4	–	1.5•	2.25	–	1.5	–	V	
		9	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN	0.5	5	0.15	–	0.125•	0.3	–	0.085	–	mA	2
		0.5	10	0.31	–	0.25•	0.5	–	0.175	–		
P-Channel	I_DP	4.5	5	−0.1	–	−0.08•	−0.16	–	−0.055	–	mA	2
		9.5	10	−0.25	–	−0.2•	−0.44	–	−0.14	–		
Diode Test, 100 μA Test Pin	V_{DF}			–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I			–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C and C_L = 15 pF*

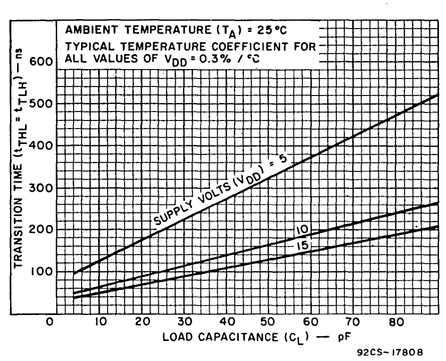
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4015AD, CD4015AK Min.	Typ.	Max.	UNITS	NOTES
CLOCKED OPERATION							
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	300	750	ns	1
		10	–	100	225●		
Transition Time	t_{THL}, t_{TLH}	5	–	150	300	ns	–
		10	–	75	125		
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	200	500	ns	–
		10	–	100	175		
Clock Rise & Fall Time	*t_{rCL}, t_{fCL}	5	–	–	15	μs	1
		10	–	–	15●		
Set-Up Time		5	–	100	350	ns	–
		10	–	50	80		
Maximum Clock Frequency	f_{CL}	5	1	2.5	–	MHz	1
		10	3●	5	–		
Input Capacitance	C_I		–	5	–	pF	–
RESET OPERATION							
Propagation Delay Time	$t_{PHL(R)}$	5	–	300	750	ns	–
		10	–	100	225		
Minimum Set and Reset Pulse Widths	$t_{WH(R)}$	5	–	200	500	ns	–
		10	–	100	175		

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1. Test is a one input one output only.



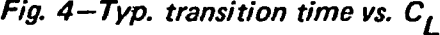


Fig. 4—Typ. transition time vs. C_L.

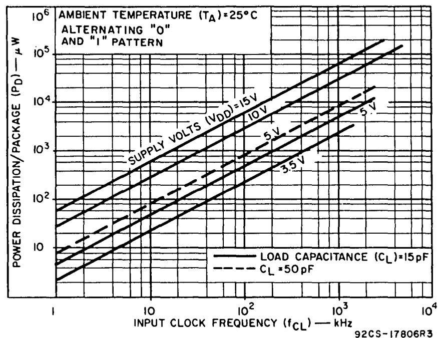
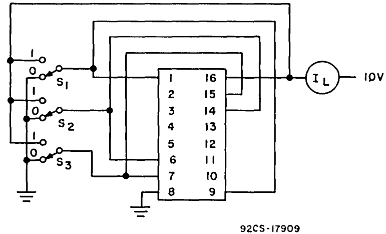


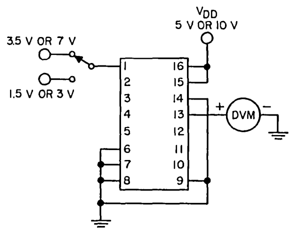
Fig. 5—Typ. dissipation characteristics.



Test performed with the following sequence of "1's" and "0's"

	S_1	S_2	S_3
Test	0	1	0
Don't Test	0	0	1
Don't Test	1	0	1
Don't Test	0	0	0
Don't Test	1	0	0
Don't Test	0	0	1
Test	1	0	1
Don't Test	0	0	0
Test	1	0	0

Fig. 6—Quiescent device current test circuit.



92CS-17910R1

Fig. 7—Noise immunity test circuit.

STAGE NO. 1 (ALL OTHER STAGES ARE IDENTICAL)

ALL P SUBSTRATES ARE CONNECTED TO V_{DD}
ALL N SUBSTRATES ARE CONNECTED TO V_{SS}

92SM-4443R1

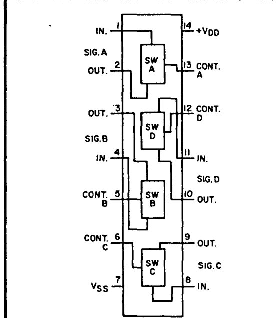
Fig. 8—Schematic diagram.

Solid State
Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series
CD4016A/...



High-Reliability COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- **Wide range of digital and analog signal levels — Digital or analog signal to 15 V peak Analog signal ± 7.5 V peak**
- **Low "ON" resistance— 300 Ω typ. over 15 V_{p-p} signal input range, for $V_{DD} - V_{SS} = 15$ V**
- **Matched switch characteristics — 40 Ω typ. difference between R_{ON} values at a fixed bias point over 15 V_{p-p} signal input range $V_{DD} - V_{SS} = 15$ V**
- **High "On/Off" output voltage ratio — 65 dB type@ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity — < 0.5% distortion typ. @ f_{is} = 1kHz, $V_{is} = 5V_{p-p}$, $V_{DD}-V_{SS} \geq 10$ V, R_L = 10 kΩ.**

RCA CD4016A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. These devices are electrically and mechanically identical with standard COS/MOS CD4016A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4016A	MIL-M-38510/05801

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

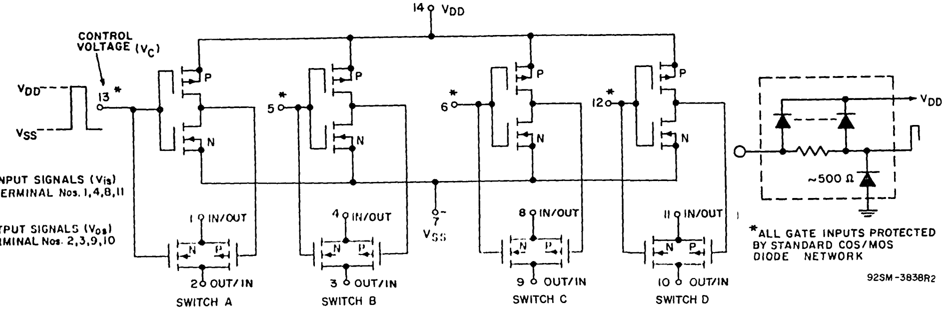
Applications

- **Analog signal switching/multiplexing**

Signal gating	**Modulator**
Squelch control	**Demodulator**
Chopper	**Commutating switch**

- **Digital signal switching/Multiplexing**
- **COS/MOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**
- **Extremely low "OFF" switch leakage resulting in very low offset current and high effective "OFF" resistance — 10 pA typ. @ $V_{DD} - V_{SS} = 10$ V, $T_A = 25°$ C**
- **Extremely high control input impedance (control circuit isolated from signal circuit) — 10^{12} Ω typ.**
- **Low crosstalk between switches — −50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitances — Reduces output signal transients**
- **Transmits frequencies up to 10 MHz**

The CD4016A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).



NOTE: All switch P-channel substrates are internally connected to terminal No. 14.
All switch N-channel substrates are internally connected to terminal No. 7.

Caution:
If V_{is} exceeds V_{DD}, input currents must not be allowed to exceed 5 mA.

NORMAL OPERATION:

Control-Line Biasing
Switch "ON": V_C "1" = V_{DD}
Switch "OFF": V_C "0" = V_{SS}

SIGNAL-LEVEL RANGE:
$V_{SS} \leq V_{is} \leq V_{DD}$

Fig. 1—Schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range .... −65 to +150 °C
Operating-Temperature Range .... −55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) .... −0.5 to +15 V
Device Dissipation (Per Package) .... 200 mW
All Inputs .... $V_{SS} \leq V_I \leq V_{DD}$

Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V
Recommended
Input-Voltage Swing .... V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32"
(1.59 ± 0.79 mm) from case
for 10 s max. .... 265 °C

ELECTRICAL CHARACTERISTICS *(All inputs .... $V_{SS} \leq V_I \leq V_{DD}$) (Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) ..... 3 to 15 V)*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS −55°C Min.	−55°C Max.	25°C Min.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Dissipation per Package, All Switches "OFF"	P_D	TERMINALS / VOLTS APPLIED: V_{DD} 14 +10; V_{SS} 7 GND	–	5•	–	5	–	300	μW	1
Quiescent Device Current	I_L	V_C 5, 6, 12, 13 GND; V_{is} 1, 4, 8, 11 ≤ +10; V_{os} 2, 3, 9, 10 ≤ +10	–	0.5•	–	0.5•	–	10•	μA	1
Quiescent Dissipation per Package, All Switches "ON"	P_D	TERMINALS / VOLTS APPLIED: V_{DD} 14 +10; V_{SS} 7 GND	–	5	–	5	–	300	μW	1
Quiescent Device Current	I_L	V_C 5, 6, 12, 13 +10; $V_{is}=V_{os}$ 1-4, 8-11 ≤ +10	–	0.5•	–	0.5•	–	10•	μA	1
Output Voltage Low-Level	V_{OL}	V_{DD} 3	–	0.55•	–	0.5•	–	–	V	1
		V_{DD} 15	–	–	–	1•	–	2•	V	1
Output Voltage High-Level	V_{OH}	V_{DD} 3	2.25•	–	2.3•	–	–	–	V	1
		V_{DD} 15	–	–	14•	–	13•	–	V	1
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = −10 μA Terminal 13 = GND; V_{DD} = 5V, 10V	−0.7•	−3•	−0.7•	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	I_{DS} = 10 μA Terminal 13 = GND; V_{DD} = 5V, 10V	0.7•	3•	0.7•	3•	0.3•	3•	V	2
Diode Test	V_{DF}	100 μA Test pin	–	1.5•	–	1.5•	–	1.5•	V	3

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or a one output only.

•±10 x 10^{-3} ▲Symmetrical about 0 volts

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS -55°C Typ.	-55°C Max.	25°C Typ.	25°C Max.	125°C Typ.	125°C Max.	UNITS	NOTES
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})													
			$V_C = V_{DD}$	V_{SS}	V_{is}								
"ON" Resistance	R_{ON}	R_L = 10k Ω	+7.5V	7.5V	+7.5V	120	360•	200	400•	300	600•	Ω	2
					7.5V	120	360•	200	400•	300	600•		
					±0.25V	130	775	280	850	470	1230		
			+5V	−5V	+5V	130	600•	250	660•	400	960•	Ω	2
					−5V	130	600•	250	660•	400	960•		
					±0.25V	325	1870	580	2000	900	2600		
			+15V	0V	+15V	120	360•	200	400•	300	600•	Ω	2
					+0.25V	120	360	200	400	300	600		
					9.3V	150	775	300	850	490	1230		
			+10V	0V	+10V	130	600•	250	660•	400	960•	Ω	2
					+0.25V	130	600	250	660	400	960		
					5.6V	300	1870	560	2000	880	2600		
▲"ON" Resistance Between Any 2 of 4 Switches	▲R_{ON}		+7.5V	−7.5V	±7.5V	–	–	10	–	–	–	Ω	–
			+5V	−5V	±5V	–	–	15	–	–	–		
Sine Wave Response (Distortion)		R_L = 10k Ω, f_{is} = 1kHz	+5V	−5V	5V (p p)▲	–	–	0.4	–	–	–	%	–
			V_{DD}	$V_C = V_{SS}$	V_{is}								
Input or Output Leakage Switch "OFF" (Effective "OFF" Resistance)			+7.5V	−7.5V	+7.5V	–	–	•100				pA	1
					−7.5V			•100		–			
			+5V	−5V	+5V			100	500	–	–	nA	
					−5V	–	–	100	500	–	–		
Frequency Response—Switch "ON" (Sine Wave Input)		R_L = 1kΩ, V_{is} = 5V (p p)	$V_C = V_{DD} = -5V$ $V_{SS} = -5V$; $20 \text{ Log}_{10} \frac{V_{os}}{V_{is}} = -3dB$			–	–	40	–	–	–	MHz	–
Feedthrough Switch "OFF"			$V_{DD} = +5V$, $V_C = V_{SS} = -5V$; $20 \text{ Log}_{10} \frac{V_{os}}{V_{is}} = -50dB$			–	–	1.25	–	–	–	MHz	–
Crosstalk Between Any 2 of the 4 Switches (Frequency at −50dB)		R_L = 1kΩ, $V_{is}(A)$ = 5V (p p)	$V_C(A)$ $V_{DD} = +5V$; $V_C(B) = V_{SS} = -5V$; $20 \text{ Log}_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50dB$			–	–	0.9	–	–	–	MHz	–
Capacitance Input	C_{IS}	$V_{DD} = +5V$, $V_C = V_{SS} = -5V$				–	–	4	–	–	–	pF	–
Output	C_{OS}					–	–	4	–	–	–		
Feedthrough	C_{IOS}					–	–	0.2	–	–	–		
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD} = +10V$, V_{SS} = GND, C_L = 15pF; V_{is} = 10V (square wave); $t_r = t_f$ = 20 ns (input signal)				–	–	10	25•	–	–	ns	2

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or a one output only.

•$\pm 10 \times 10^{-3}$ ▲Symmetrical about 0 volts

ELECTRICAL CHARACTERISTICS *(All Inputs .... $V_{SS} \leqslant V_I \leqslant V_{DD}$)*
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4016AD, CD4016AK –55°C Min.	–55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
CONTROL (V_C)												
Switch Threshold Voltage	V_{THN}	$V_{IS} \leqslant V_{DD}$	$V_{DD} - V_{SS}$ = 15V, 10V, 5V, I_{IS} = 10μA	0.7	2.9	0.5	1.5	2.7	0.2	2.4		–
Input Current	I_C	$V_{IS} \leqslant V_{DD}$	$V_{DD} - V_{SS}$ = 10V, $V_C \leqslant V_{DD} - V_{SS}$	–	–	–	±10	–	–	–	pA	–
Noise Immunity (Control Inputs)	V_{NL}	V_{DD} = 10V		0.5•	–	0.7•	–	–	0.5•	–	V	1
For Definition, See Appendix SSD-207	V_{NH}	V_{DD} = 10V		–	3•	–	–	2.7•	–	3•	V	1
Average Input Capacitance	C_C			–	–	–	5	–	–	–	pF	–
Crosstalk – Control Input to Signal Output		$V_{DD}-V_{SS}$ = 10V, V_C = 10V (square wave) $t_{rc} = t_{fc}$ = 20 ns	R_L = 10 kΩ	–	–	–	50	–	–	–	mV	–
Turn "ON" Propagation Delay	$t_{pd}C$	$V_{DD}-V_{SS}$ = 10V, V_C = 10V (square wave) $t_{rc} = t_{fc}$ = 20 ns	$V_{is} \leqslant$ 10V, C_L = 15 pF	–	–	–	20	50•	–	--	ns	2
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1kΩ, C_L = 15pF, V_C = 10V (square wave), $t_r = t_f$ = 20 ns		–	–	–	10	–	–	–	MHz	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is all inputs

TYPICAL "ON" RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS V_{DD} (V)	V_{SS} (V)	LOAD CONDITIONS R_L = 1kΩ VALUE (Ω)	V_{is} (V)	R_L = 10kΩ VALUE (Ω)	V_{is} (V)	R_L = 100kΩ VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	–7.5	200	+7.5	200	+7.5	180	+7.5
			200	–7.5	200	–7.5	180	–7.5
R_{ON}(max.)	+7.5	–7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+ 5	– 5	260	+ 5	250	+ 5	240	+ 5
			310	– 5	250	– 5	240	– 5
R_{ON}(max.)	+ 5	– 5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	–2.5	590	+2.5	450	+2.5	490	+2.5
			720	-2.5	520	-2.5	520	–2.5
R_{ON}(max.)	+2.5	–2.5	232k	±0.25	300k	±0.25	870k	±0.25

* Variation from a perfect switch; R_{ON} = 0Ω.

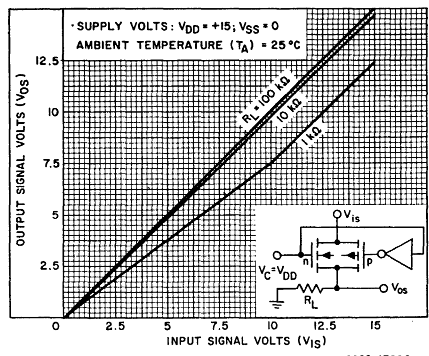


Fig. 2–Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +15V, V_{SS} = 0V.

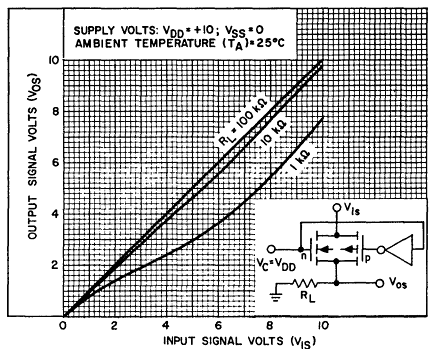


Fig. 3–Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +10V, V_{SS} = 0V.

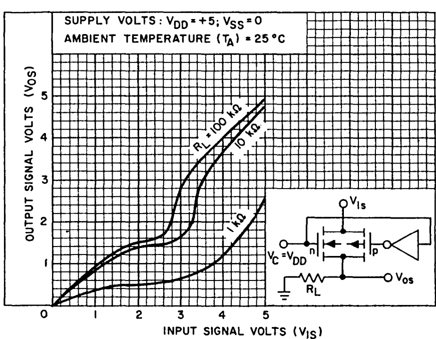


Fig. 4–Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5V, V_{SS} = 0V.

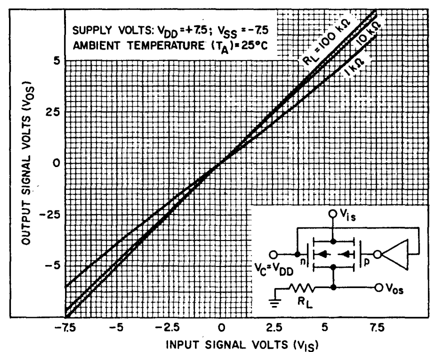


Fig. 5–Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +7.5V, V_{SS} = -7.5V.

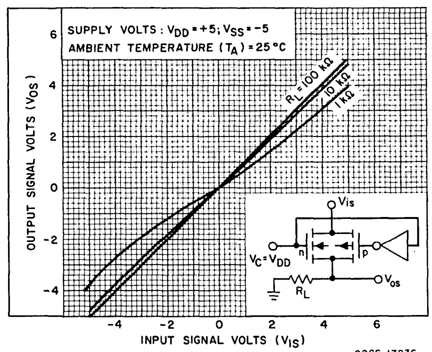


Fig. 6–Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5V, V_{SS} = -5V.

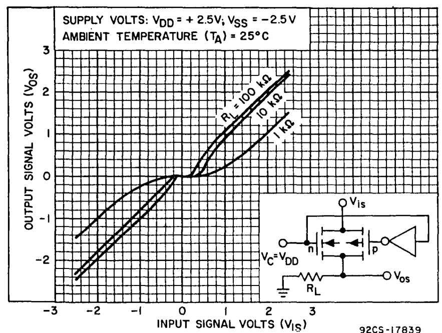


Fig. 7–Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +2.5V, V_{SS} = -2.5V.

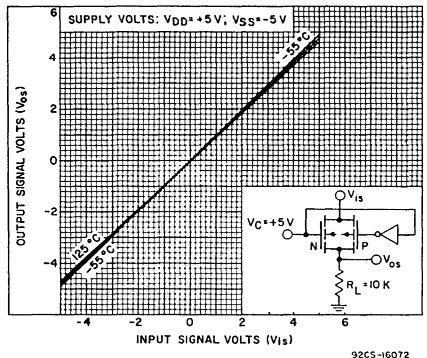


Fig. 8—Typ. "ON" characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5V, V_{SS} = -5V.

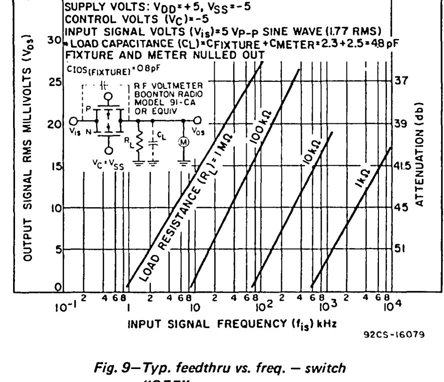


Fig. 9—Typ. feedthru vs. freq. – switch "OFF".

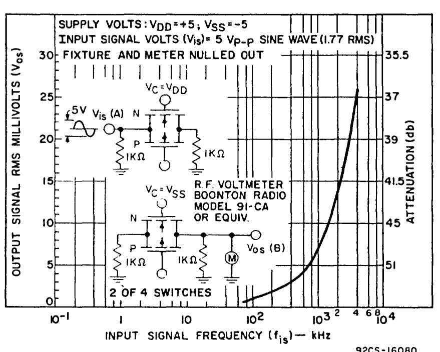


Fig. 10—Typ. crosstalk between switch circuits in the same package.

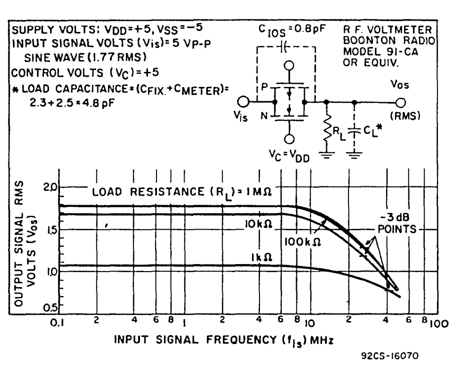


Fig. 11—Typ. switch frequency response –switch "ON".

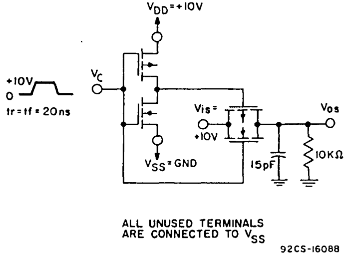


Fig. 12—Turn-on propagation delay control input.

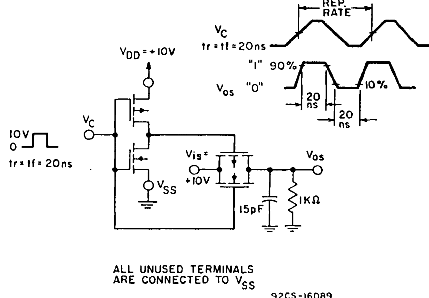


Fig. 13—Max. allowable control-input repetition rate.

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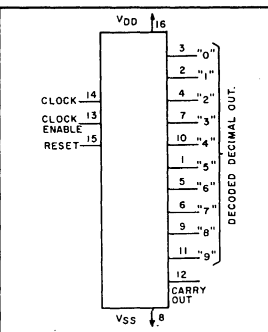

High-Reliability COS/MOS Decade Counter/Divider

Plus 10 Decoded Decimal Outputs

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation. . . . . 5 MHz (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Fully static operation**
- **MSI complexity on a single chip. . . . . decade counter plus 10 decoded outputs**

Applications:

- **Decade counter/decimal decode display applications**
- **Frequency division**
- **Counter control/timers**
- **Divide by N counting**
  N = 2 – 10 with one CD4017A and one CD4001A
  N> 10 with multiple CD4017A's
- **For further application information, see ICAN6166 "COS/MOS MSI Counter and Register Design & Applications"**

RCA CD4017A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4017A types consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a "Clock", a "Reset", and a "Clock Enable" signal.

The decade counter is advanced one count at the positive clock signal transition if the clock enable signal is "low". Counter advancement via the clock line is inhibited when the clock enable signal is "high". A "high" reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally "low" and go "high" for one full clock cycle. A carry-out (C_{OUT}) signal completes one cycle every 10

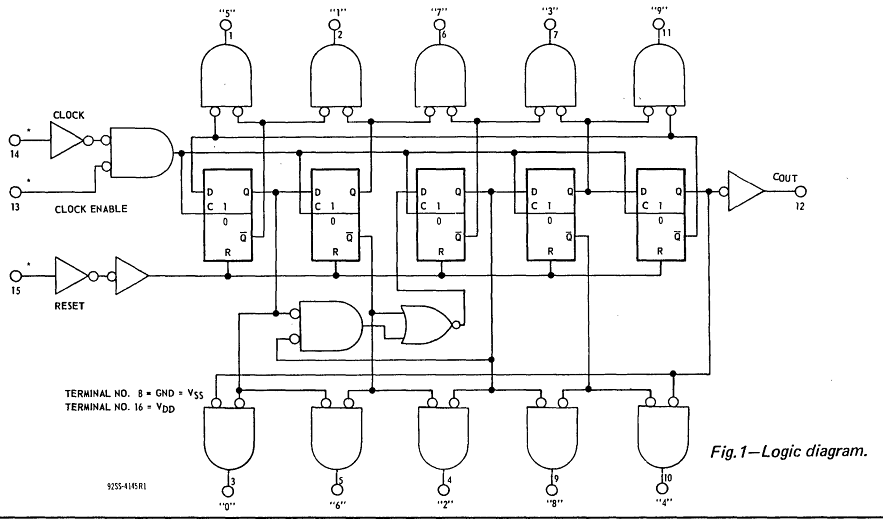

Fig.1—Logic diagram.

clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

These devices are electrically and mechanically identical with standard COS/MOS CD4017A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4017A	MIL-M-38510/05601

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4017A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

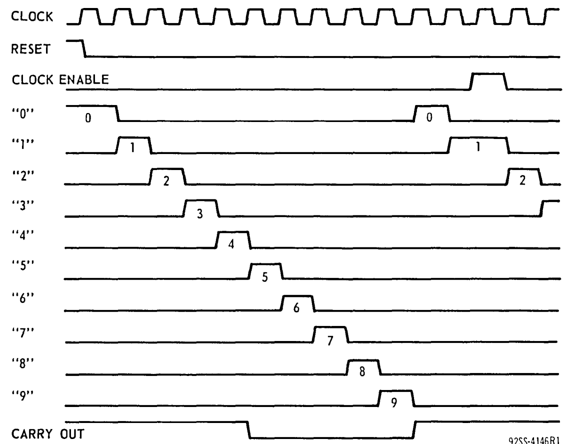

Fig. 2—Timing diagram.

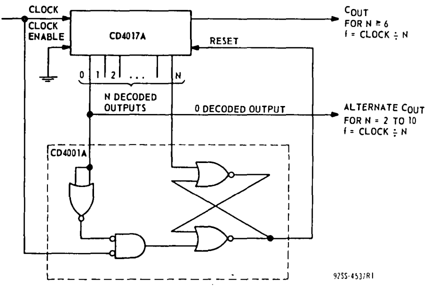

Fig. 3— Divide by N counter (N ⩽ 10) with N decoded outputs.

When the Nth decoded output is reached (N^th clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001A) generates a reset pulse which clears the CD4017A to its zero count. At this time, if the Nth decoded output is greater than or equal to 6, the C_{OUT} line goes "high" to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of the clock "low" and decoded "0" output "low" resets the S-R flip flop to enable the CD4017A. If the Nth decoded output is less than 6, the C_{OUT} line will not go "high" and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4017AD, CD4017AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L			5	–	5	–	0.3	5	–	300	μA	1
				10	–	10•	–	0.5	10•	–	200•		
Quiescent Device Dissipation/Package	P_D			5	–	25	–	1.5	25	–	1500	μW	–
				10	–	100	–	5	100	–	2000		
Output Voltage Low-Level	V_{OL}			3	–	0.55•	–	–	0.5•	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}			3	2.25•	–	2.3•	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = −20 μA			−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}		0.8	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
			1	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}		4.2	5	1.4	–	1.5•	2.25	–	1.5	–	V	
			9	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current N-Channel	I_DN	Decoded Outputs	0.5	5	0.06	–	0.05•	0.1	–	0.035	–	mA	2
			0.5	10	0.12	–	0.1•	0.4	–	0.07	–		
		Carry Output	0.5	5	0.185		0.15•	0.4		0.105			
			0.5	10	0.45		0.35•	1		0.25			
P-Channel	I_DP	Decoded Outputs	4.5	5	−0.0375	–	−0.03•	−0.075	–	−0.021	–	mA	2
			9.5	10	−0.12	–	−0.1•	−0.2	–	−0.07	–		
		Carry Output	4.5	5	−0.185		−0.15•	−0.4		−0.105			
			9.5	10	−0.45		−0.35•	−1		−0.25			
Diode Test, 100 μA Test Pin	V_{DF}				–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range . . . . −65 to +150 °C
Operating-Temperature Range . . . . −55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) . . . . −0.5 to +15 V
Device Dissipation (Per Package) . . . . 200 mW
All Inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$
Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) . . . . . 3 to 15 V

Recommended
Input-Voltage Swing . . . . V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32"
(1.59 ± 0.79 mm) from case
for 10 s max. . . . . +265 °C

DYNAMIC ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL*
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4017AD, CD4017AK Min.	Typ.	Max.	UNITS	NOTES
CLOCKED OPERATION								
Propagation Delay Time: Carry Out Line	t_{PHL}, t_{PLH}		5	–	350	1000	ns	1
			10	–	125	250●		
Decode Out Lines			5	–	500	1200	ns	1
			10	–	200	400●		
Transition Time: Carry Out Line	t_{THL}, t_{TLH}		5	–	100	300	ns	1
			10	–	50	150●		
Decode Out Lines			5	–	300	900	ns	1
			10	–	125	350●		
Minimum Clock * Pulse Width	t_{WL}, t_{WH}		5	–	200	500	ns	–
			10	–	100	170		
Clock Rise & Fall Time	t_{rCL}, t_{fCL}		5	–	–	15	µs	1
			10	–	–	15●		
Clock Enable Set-Up Time			5	–	175	500	ns	–
			10	–	75	200		
Maximum Clock Frequency	f_{CL}		5	1	2.5	–	MHz	–
			10	3●	5	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	–
RESET OPERATION								
Propagation Delay Time: To Carry Out Line	$t_{PHL(R)}$		5	–	350	1000	ns	–
			10	–	125	250		
To Decode Out Lines			5	–	450	1200	ns	–
			10	–	200	400		
Reset Pulse Width	$t_{WH(R)}$		5	–	200	500	ns	–
			10	–	100	165		
Reset Removal Time			5	–	300	750	ns	–
			10	–	100	225		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
Note 1: Test is a one input one output only. * Measured with respect to carry output line

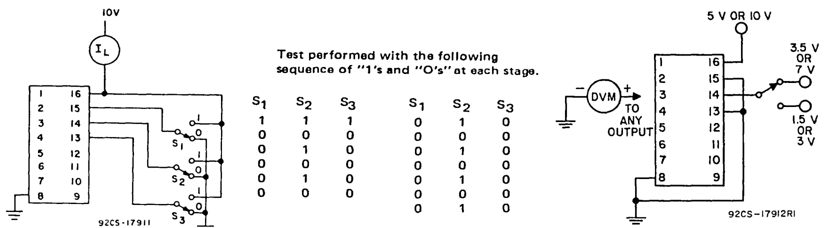

Fig. 4 – Quiescent device current test circuit.

Fig. 5 – Noise immunity test circuit.

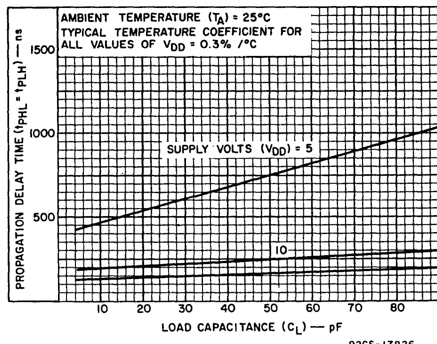

Fig. 6 — Typ. propagation delay time vs. C_L for decoded outputs.

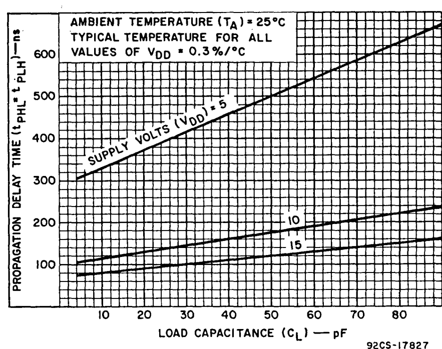

Fig. 7 — Typ. propagation delay time vs. C_L for carry output.

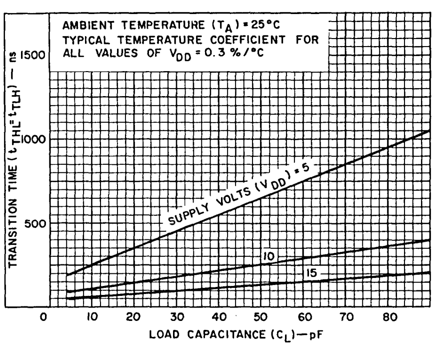

Fig. 8 — Typ. transition time vs. C_L for decoded outputs.

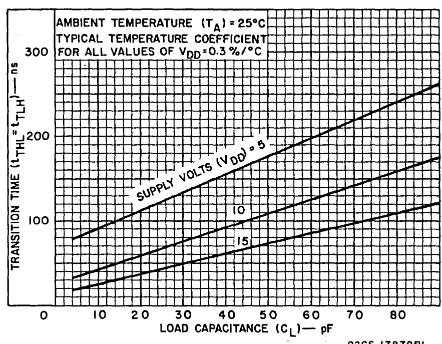

Fig. 9 — Typ. transition time vs. C_L for carry output.

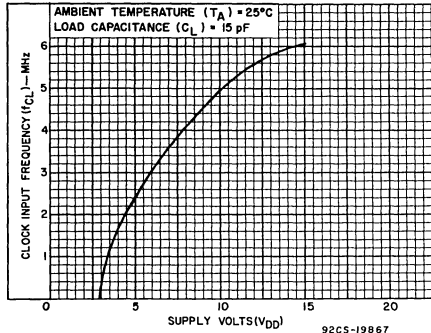

Fig. 10 — Typ. clock frequency vs. V_{DD}.

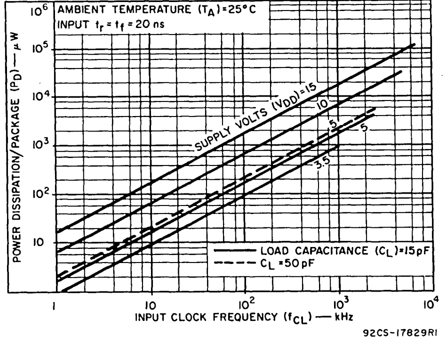

Fig. 11 — Typ. dissipation characteristics.

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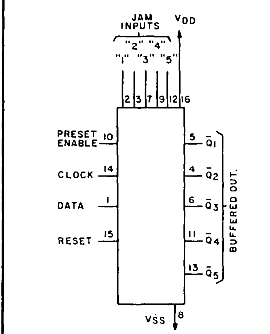


High-Reliabilty COS/MOS Presettable Divide-By-'N' Counter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- Medium speed operation. . . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- MSI complexity on a single chip

Applications

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

RCA CD4018A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. CD4018A types consist of 5 Johnson-Counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. "Clock", "Reset", "Data", "Preset Enable", and 5 individual "jam" inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package to properly gate the feedback connection to the Data input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018A units. The counter is advanced one count at the positive clock-signal transition. A "high" Reset signal clears the counter to an "all-zero" condition. A "high"

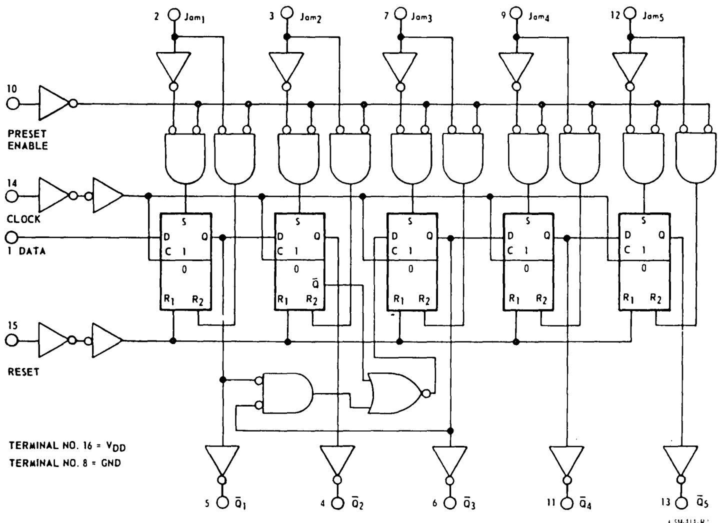


Fig. 1—Logic Diagram.

Preset-Enable signal allows information on the Jam inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

These devices are electrically and mechanically identical with standard CD4018A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

CD4018A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

RCA Designation	MIL-M-38510 Designation
CD4018A	MIL-M-38510/05602

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	–65 to +150	°C
Operating-Temperature Range	–55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	–0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

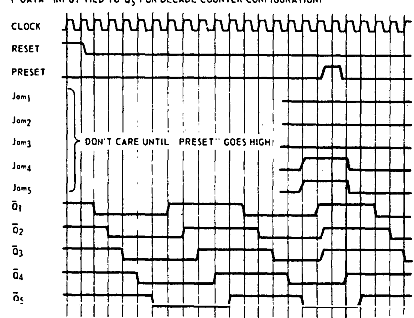


Fig. 2–Timing diagram.

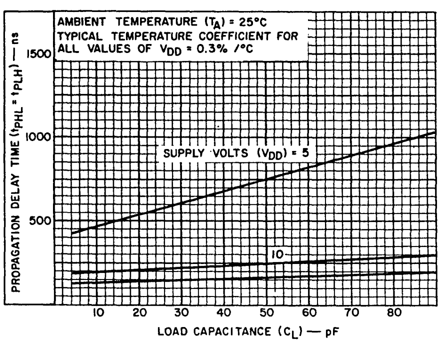


Fig. 3–Typ. propagation delay time vs. C_L for decoded outputs.

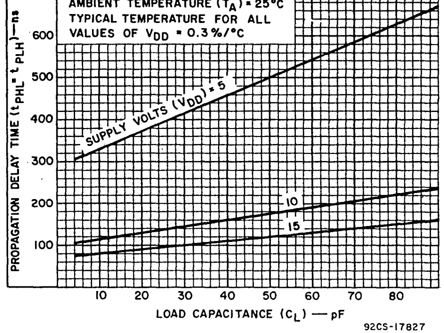


Fig. 4–Typ. propagation delay time vs. C_L for $\bar{Q}_5$ output.

DYNAMIC ELECTRICAL CHARACTERISTICS, *at T_A = 25° C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL*

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4018AD, CD4018AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
CLOCKED OPERATION								
Propagation Delay Time: To $\overline{Q}_5$ Output	t_{PHL},		5	–	350	1000	ns	1
			10	–	125	250●		
To Other Outputs	t_{PLH}		5	–	500	1200	ns	1
			10	–	200	400●		
Transition Time: To $\overline{Q}_5$ Output	t_{THL},		5	–	100	300	ns	1
			10	–	50	150●		
To Other Outputs	t_{TLH}		5	–	300	900	ns	1
			10	–	125	350●		
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	500	ns	–
			10	–	100	170		
Clock Rise & Fall Time	t_{rCL}, t_{fCL}		5	–	–	15	μs	1
			10	–	–	15●		
Data Input Set-Up Time			5	–	175	500	ns	–
			10	–	75	200		
Maximum Clock Frequency	f_{CL}		5	1	2.5	–	MHz	1
			10	3●	5	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	–
PRESET* OR RESET OPERATION								
Propagation Delay Time: To $\overline{Q}_5$ Output	$t_{PLH(R)}$,		5	–	350	1000	ns	–
			10	–	125	250		
To Other Outputs	$t_{PHL(PR)}$, $t_{PLH(PR)}$		5	–	500	1200	ns	–
			10	–	200	400		
Preset or Reset Pulse Width	$t_{WH(R)}$, $t_{WH(PR)}$		5	–	200	500	ns	–
			10	–	100	165		
Preset or Reset Removal Time			5	–	300	750	ns	–
			10	–	100	225		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only

*At Preset Enable or Jam Inputs.

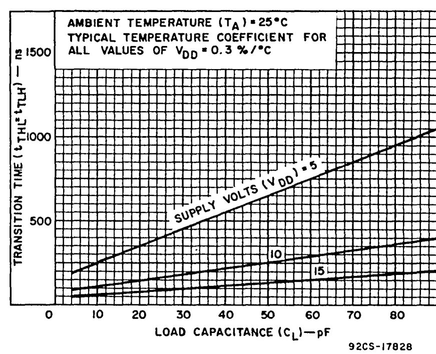


Fig. 5—Typ. transition time vs. C_L for decoded outputs.

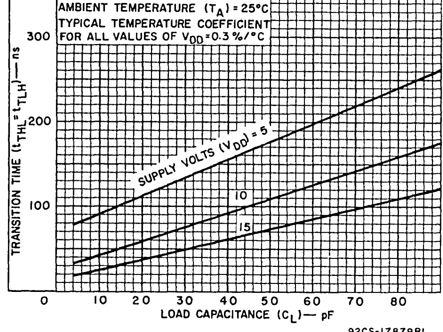


Fig. 6—Typ. transition time vs. C_L for $\overline{Q}_5$ output.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4018AD, CD4018AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L			5	–	5	–	0.3	5	–	300	µA	1
				10	–	10•	–	0.5	10•	–	200•		
Quiescent Device Dissipation/Package	P_D			5	–	25	–	1.5	25	–	1500	µW	–
				10	–	100	–	5	100	–	2000		
Output Voltage Low-Level	V_{OL}			3	–	0.55•	–	–	0.5•	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}			3	2.25•	–	2.3•	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$			−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}		0.8	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
			1	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}		4.2	5	1.4	–	1.5•	2.25	–	1.5	–	V	
			9	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	$I_D N$	$\overline{Q}_5$	0.5	5	0.18	–	0.15•	0.4	–	0.105	–	mA	2
			0.5	10	0.45	–	0.4•	1	–	0.25	–		
		$\overline{Q}_1\ \overline{Q}_2$	0.5	5	0.06	–	0.12•	0.1	–	0.035	–		
		$\overline{Q}_3\ \overline{Q}_4$	0.5	10	0.25	–	0.23•	0.4	–	0.14	–		
P-Channel	$I_D P$	$\overline{Q}_5$	4.5	5	−0.185	–	−0.15•	−0.4	–	−0.105	–	mA	
			9.5	10	−0.45	–	−0.4•	−1	–	−0.25	–		
		$\overline{Q}_1\ \overline{Q}_2$	4.5	5	−0.075	–	−0.065•	−0.15	–	−0.04	–		
		$\overline{Q}_3\ \overline{Q}_4$	9.5	10	−0.25	–	−0.2•	−0.4	–	−0.14	–		
Diode Test, 1000 µA Test Pin	V_{DF}				–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

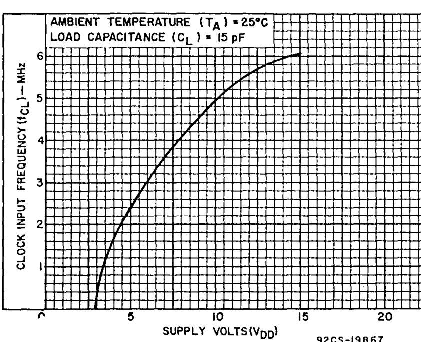


Fig. 7—Typ. clock frequency vs. V_{DD}*.*

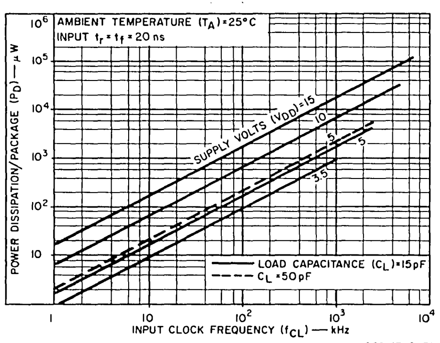
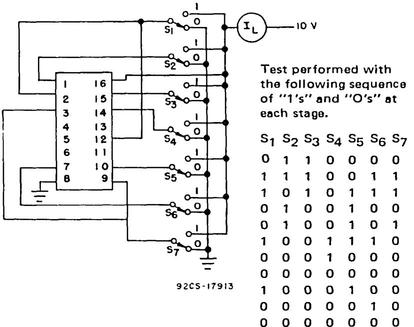


Fig. 8—Typ. dissipation characteristics.



Test performed with the following sequence of "1's" and "0's" at each stage.

S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	1	1	0	0	0	0
1	1	1	0	0	1	1
1	0	1	0	1	1	1
0	1	0	0	1	0	0
0	1	0	0	1	0	1
1	0	0	1	1	1	0
0	0	0	1	0	0	0
0	0	0	0	0	0	0
1	0	0	0	1	0	0
0	0	0	0	0	1	0
0	0	0	0	0	0	0

Fig. 9—Quiescent device current test circuit.

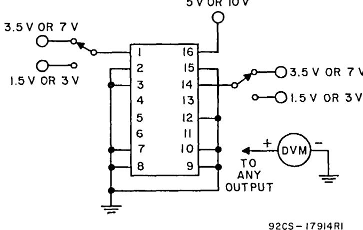


Fig. 10—Noise immunity test circuit.

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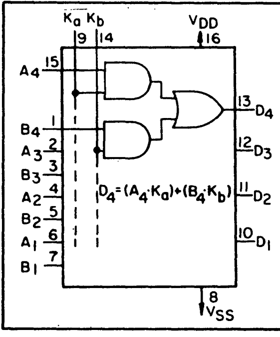
High-Reliability Slash(/) Series
CD4019A/...



High-Reliability COS/MOS Quad AND-OR Select Gate

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- Medium speed operation . . . $t_{PHL} = t_{PLH}$ = 50 ns (typ.) at C_L = 15 pF

Applications

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/Exclusive-OR selection

RCA CD4019A "Slash" (/) Series are high-reliability COS/MOS integrated circuit Quad AND-OR Select Gates intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4019A types are comprised of four AND-OR-Select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A+B function.

These devices are electrically and mechanically identical with standard COS/MOS CD4019A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4019A	MIL-M-38510/05302

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4019A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

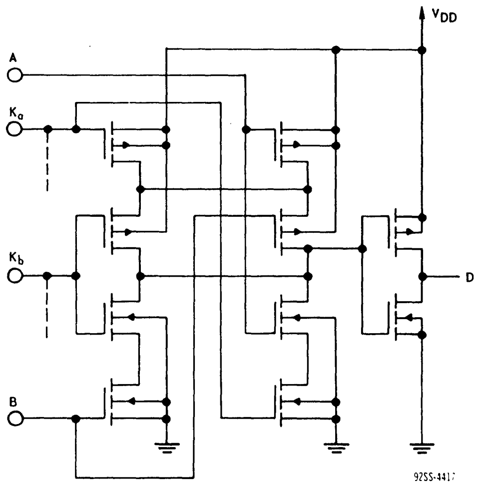


Fig. 1 — Schematic diagram for 1 of 4 identical stages.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4019AD, CD4019AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L		5	–	5	–	0.03	5	–	300	µA	1
			10	–	10•	–	0.05	10•	–	200•		
Quiescent Device Dissipation/Package	P_D		5	–	25	–	0.15	25	–	1500	µW	–
			10	–	100	–	0.5	100	–	2000		
Output Voltage Low-Level	V_{OL}		3	–	0.55•	–	–	0.5•	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	4.95	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.45•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$		−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$		0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Inputs)	V_{NL}	0.95	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
		2.9	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}	3.6	5	1.4	–	1.5•	2.25	–	1.5	–	V	
		7.2	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN	0.5	5	0.6	–	0.7•	0.9	–	0.3	–	mA	2
		0.5	10	0.9	–	1.2•	1.5	–	0.55	–		
P-Channel	I_DP	4.5	5	−0.31	–	−0.25•	−0.5	–	−0.175	–	mA	2
		9.5	10	−0.95	–	−0.7•	−1.5	–	−0.5	–		
Diode Test, 100 µA Test Pin	V_{DF}			–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I			–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range . . . . −65 to +150 °C
Operating-Temperature Range . . . . −55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) . . . . −0.5 to +15 V
Device Dissipation (Per Package) . . . . 200 mW
All Inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$
Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) . . . . . 3 to 15 V
Recommended
Input-Voltage Swing . . . . V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32"
(1.59 ± 0.79 mm) from case
for 10 s max. . . . . +265 °C

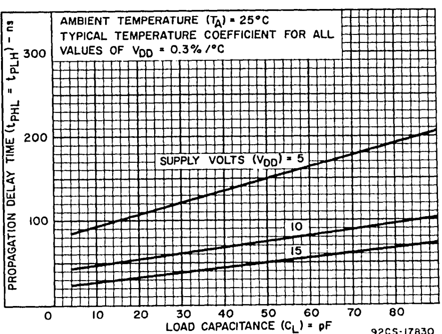


Fig.6—Typ. propagation delay time vs C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3 %/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4019AD, CD4019AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time:	t_{PHL}, t_{PLH}		5	–	100	225	ns	1
			10	–	50	100●		
Transition Time	t_{THL}, t_{TLH}		5	–	100	200	ns	1
			10	–	40	65●		
Input Capacitance	C_I	All A and B Inputs		–	5	–	pF	–
		K_A and K_B Inputs		–	12	–		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
NOTE 1: Test is a one input one output only.

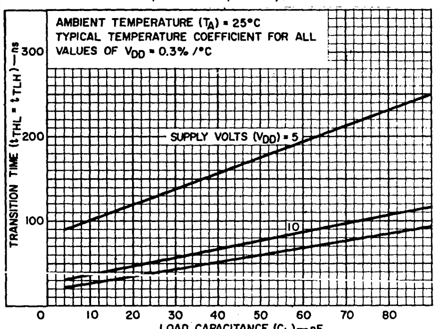


Fig. 3— Typ. transition time vs C_L.

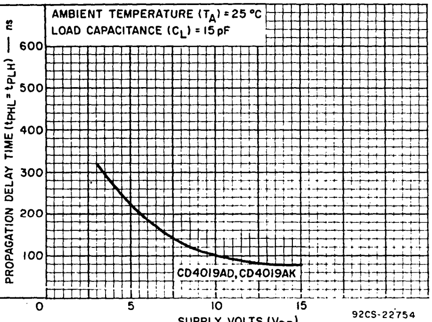


Fig. 4— Max. propagation delay time vs V_{DD}.

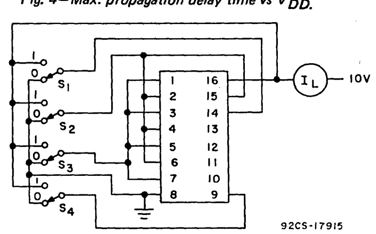


Fig. 6— Quiescent device current test circuit.

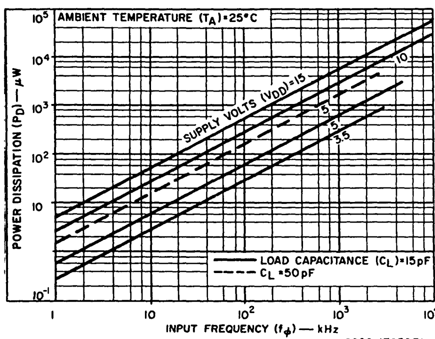


Fig. 5— Typ. dissipation characteristics (per output).

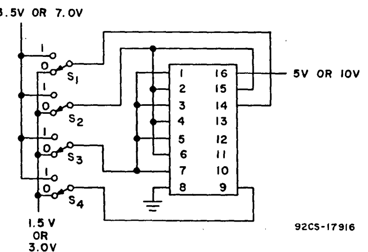


Fig. 7— Noise immunity test circuit.

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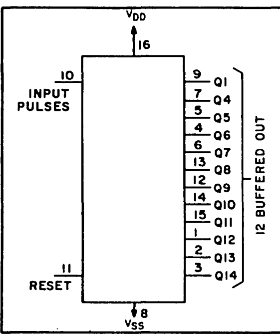
High-Reliability Slash(/) Series CD4020A/...



High-Reliability COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- Medium speed operation..... 7 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
- Low "high" - and "low" -level output impedance...... 1000Ω (typ.) at $V_{DD} - V_{SS} = 10$ V
- MSI complexity on a single chip...... 14 fully static, master-slave stages
- COS/MOS gate-input loading at both Reset and Input-pulse lines

Applications

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- Counting functions

RCA Designation	MIL-M-38510 Designation
CD4020A	MIL-M-38510/05603

RCA CD4020A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4020A types consist of a pulse input shaping circuit, reset line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its "all zeroes" state by a high level on the reset inverter input line. Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each input pulse. These devices are electrically and mechanically identical with standard COS/MOS types CD4020A described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

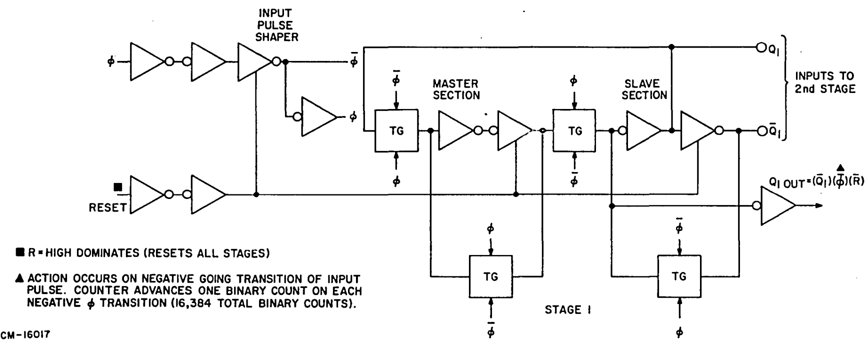


Fig. 1—Logic diagram for 1 to 4 binary stages.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4020A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	–65 to +150	°C
Operating-Temperature Range	–55 to +125	°C
DC Supply-Voltage Range: (V_{DD} – V_{SS})	–0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage (V_{DD} – V_{SS})	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

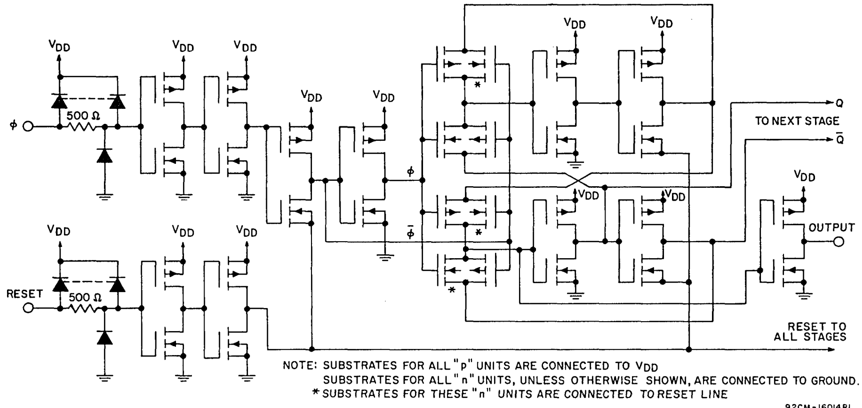


Fig. 2–Schematic diagram of pulse shapers and 1 of 14 binary stages.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} < V_I < V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4020AD, CD4020AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L		5	–	15	–	0.5	15	–	900	μA	1
			10	–	25●	–	1	25●	–	500●		
Quiescent Device Dissipation/Package	P_D		5	–	75	–	2.5	75	–	4500	μW	–
			10	–	250	–	10	250	–	5000		
Output Voltage Low-Level	V_{OL}		3	–	0.55●	–	–	0.5●	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5●	–	0.55●		
High-Level	V_{OH}		3	2.25●	–	2.3●	–	–	–	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.5●	–	–	14.45●	–		
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$		−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$		0.7●	3●	0.7●	1.5	3●	0.3●	3●		
Noise Immunity (Any Input)	V_{NL}	0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V	1
		1	10	3●	–	3●	4.5	–	2.9●	–		
For Definition, See Appendix SSD-207	V_{NH}	4.2	5	1.4	–	1.5●	2.25	–	1.5	–	V	
		9	10	2.9●	–	3●	4.5	–	3●	–		
Output Drive Current: N-Channel	I_DN	0.5	5	0.9	–	0.15●	0.2	–	0.05	–	mA	2
		0.5	10	0.185	–	0.3●	0.4	–	0.105	–		
P-Channel	I_DP	4.5	5	−0.11	–	−0.09●	−0.25	–	−0.065	–	mA	2
		9.5	10	−0.25	–	−0.2●	−0.5	–	−0.14	–		
Diode Test, 100 μA Test Pin	V_{DF}			–	1.5●	–	–	1.5●	–	1.5●	V	3
Input Current	I_I			–	–	–	10	–	–	–	pA	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL*
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4020AD, CD4020AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
CLOCKED OPERATION								
Propagation Delay Time	t_{PHL}, t_{PLH}	*	5	–	450	600	ns	1
			10	–	150	225●		
Transition Time	t_{THL}, t_{TLH}		5	–	450	600	ns	1
			10	–	200	300●		
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	335	ns	–
			10	–	70	125		
Clock Rise & Fall Time	t_{rCL}, t_{fCL}		5	–	–	15	μs	1
			10	–	–	15●		
Maximum Clock Frequency	f_{CL}		5	1.5	2.5	–	MHz	1
			10	4●	7	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	–
RESET OPERATION								
Propagation Delay Time:	$t_{PHL(R)}$		5	–	2000	3000	ns	–
			10	–	500	775		
Minimum Reset Pulse Width	$t_{WH(R)}$		5	–	1800	2500	ns	–
			10	–	300	475		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

*Propagation Delay is from clock input to Q_1 output.

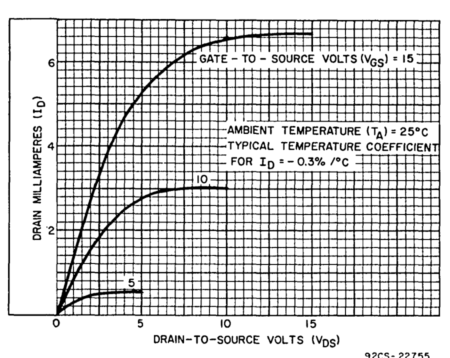


Fig. 3—Min. n-channel drain characteristics.

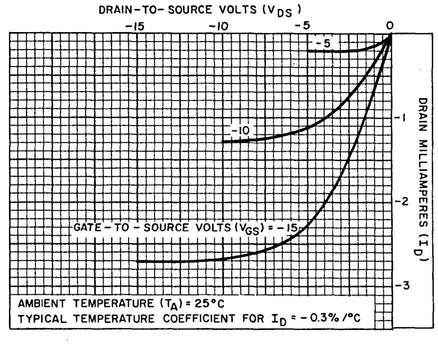


Fig. 4—Min. p-channel drain characteristics.

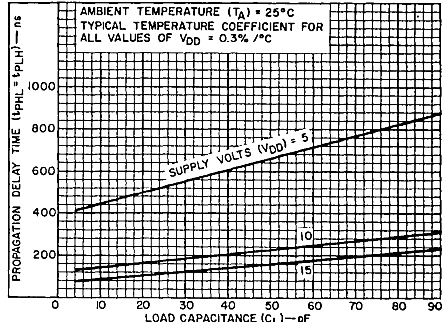


Fig. 5—Typ. propagation delay time vs. C_L.

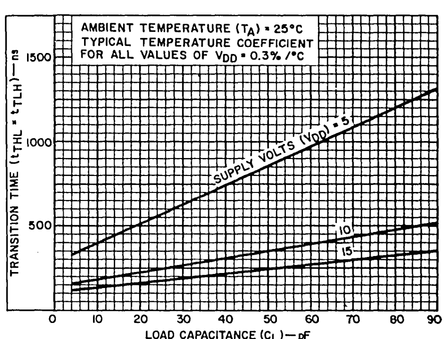


Fig. 6—Typ. transition time vs. C_L.

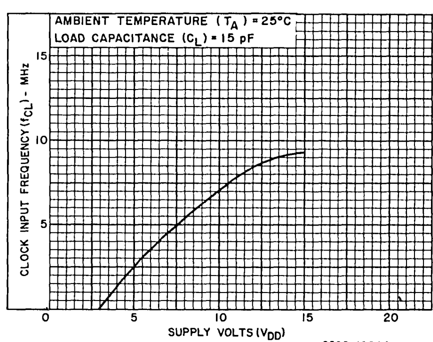


Fig. 7—Typ. clock frequency vs. V_{DD}.

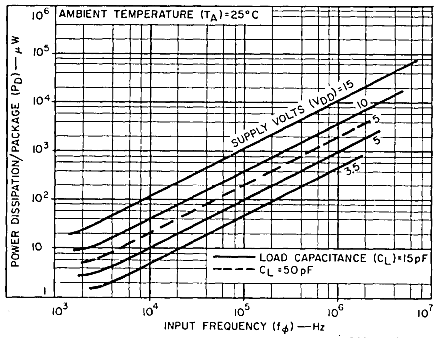


Fig. 8—Typ. dissipation characteristics.

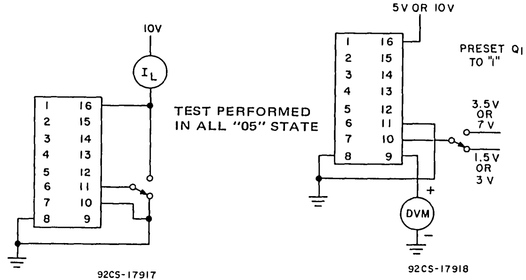


Fig. 9—Quiescent device dissipation test circuit.

Fig. 10—Noise immunity test circuit.

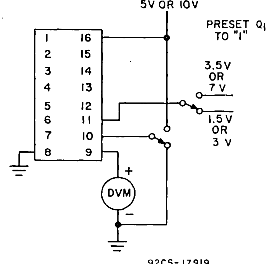


Fig. 11—Reset noise immunity test circuit.

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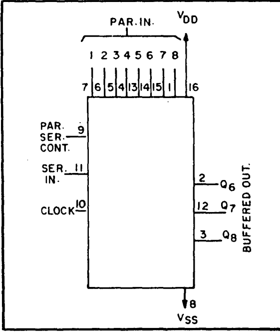
CD4021A/...



High-Reliability COS/MOS 8-Stage Static Shift Register

Asynchronous Parallel Input/Serial Output,
Synchronous Serial Input/Serial Output
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Asynchronous parallel or synchronous serial operation under control of parallel/serial control-input**
- **Individual "jam" inputs to each register stage**
- **Master-slave flip-flop register stages**
- **Fully static operation. . . . . .DC to 5 MHz**

Applications:

- **Asynchronous parallel input/serial output data queueing**
- **Parallel to serial data conversion**
- **General purpose register**

RCA CD4021A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4021A types are 8-stage parallel or serial-input/serial-output shift registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. "Q" outputs are available from the sixth, seventh, and eighth stages.

When the parallel/Serial Control input is "low", data is serially shifted into the 8-stage register synchronously with the positive-going transition of the Clock pulse. When the Parallel/Serial Control input is "high", data is Jammed into the 8-stage register via the parallel input lines asychronously with the clock line. Register expansion is possible using additional CD4021A packages.

These devices are electrically and mechanically identical with standard COS/MOS CD4021A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as shown in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series types."

RCA Designation	MIL-M-38510 Designation
CD4021A	MIL-M-38510/05704

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4021A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150	°C
Operating-Temperature Range	−55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16″ ± 1/32″ (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

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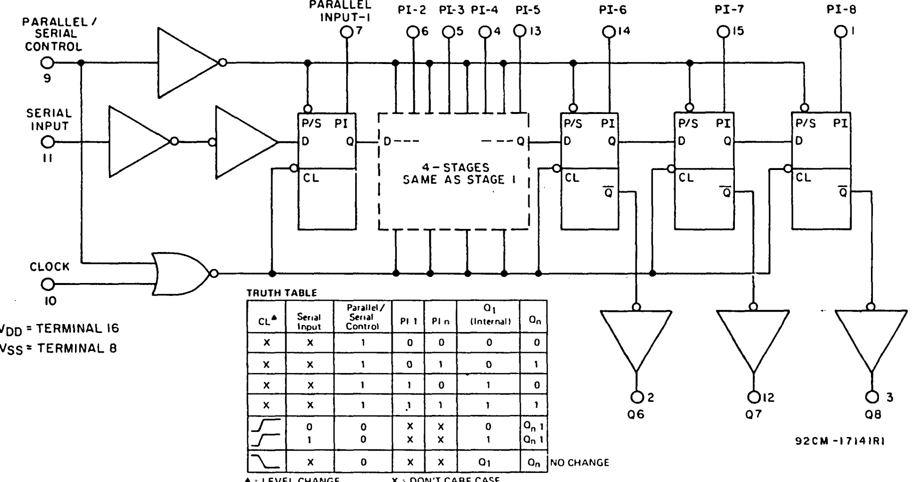

TRUTH TABLE

CL▲	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q_1 (Internal)	Q_n
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
↑	0	0	X	X	0	Q_n 1
↑	1	0	X	X	1	Q_n 1
↓	X	0	X	X	Q_1	Q_n NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

Fig. 1—Logic diagram and truth table.

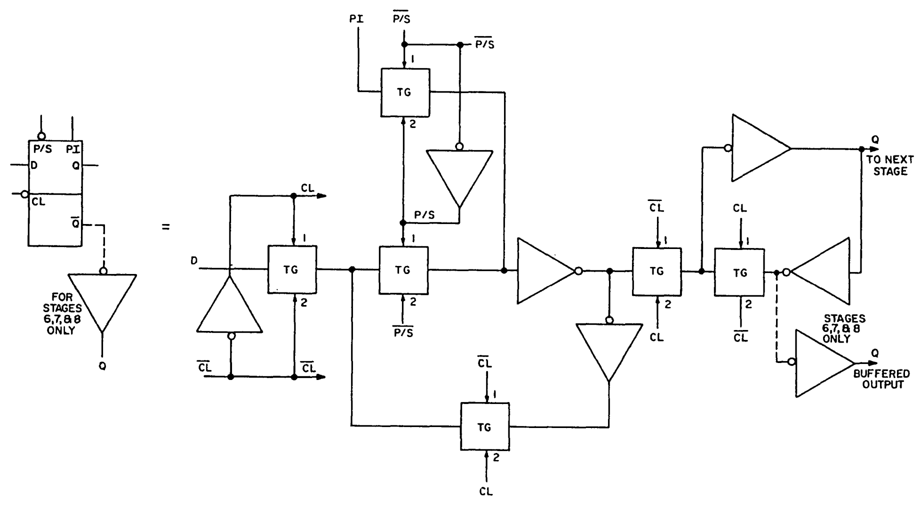

Fig. 2—One typical stage and its equivalent detailed circuit.

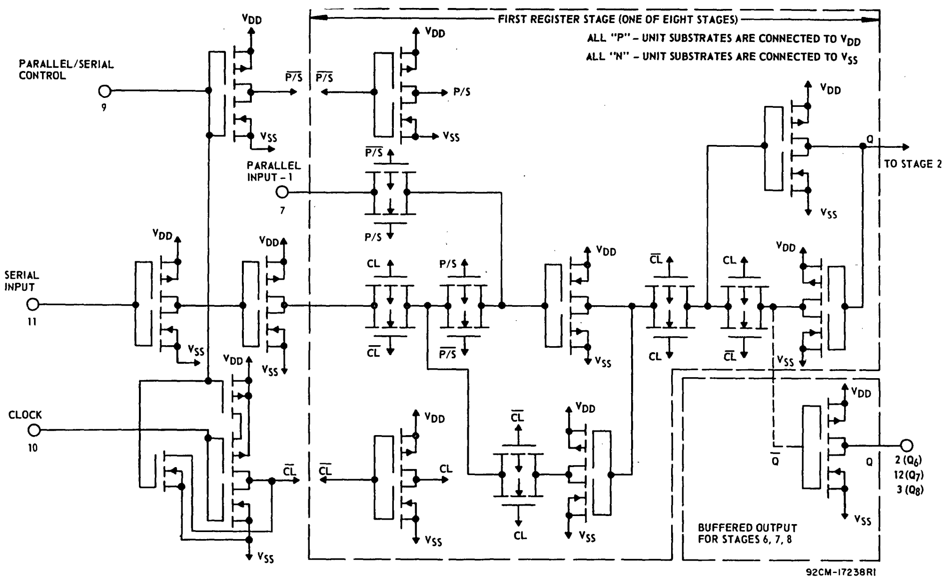

Fig. 3–Schematic diagram–CD4021A.

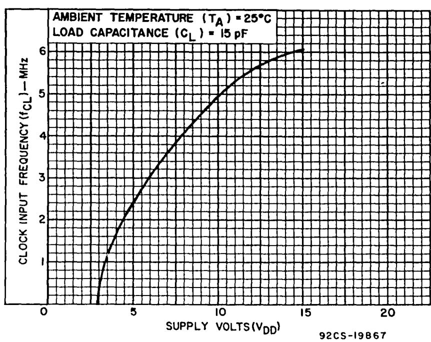

Fig. 4–Typ. clock frequency vs. V_{DD}.

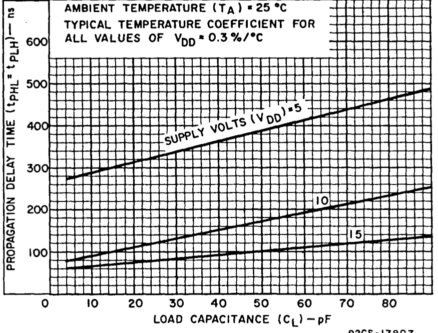

Fig. 5–Typ. propagation delay time vs. C_L.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4021AD, CD4021AK									UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.		
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	µA	1
				10	–	–	10•	–	1	10•	–	–	200.		
Quiescent Deivce Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	µW	–
				10	–	–	100	–	10	100	–	–	2000		
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55•	–	–	0.5•	–	–	–	V	1
				5	–	–	0.01	–	0	0.01	–	–	0.05		
				10	–	–	0.01	–	0	0.01	–	–	0.05		
				15	–	–	–	–	–	0.5•	–	–	0.55•		
High-Level	V_{OH}			3	2.25•	–	–	2.3•	–	–	–	–	–	V	1
				5	4.99	–	–	4.99	5	–	4.95	–	–		
				10	9.99	–	–	9.99	10	–	9.95	–	–		
				15	–	–	–	14.5•	–	–	14.45•	–	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = -20 µA			-0.7•	-1.7	-3•	-0.7•	-1.5	-3•	-0.3•	-1.3	-3•	V	2
P-Channel	$V_{TH}P$	I_D = 20 µA			0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•	V	
Noise Immunity (All Inputs)	V_{NL}		0.8	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	1
			1.0	10	3•	–	–	3•	4.5	–	2.9•	–	–		
For Definition, See Appendix in SSD-207	V_{NH}		4.2	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V	
			9.0	10	2.9•	–	–	3•	4.5	–	3•	–	–		
Output Drive Current: N-Channel	I_DN		0.5	5	0.15	–	–	0.15•	0.3	–	0.085	–	–	mA	2
			0.5	10	0.31	–	–	0.25•	0.5	–	0.175	–	–		
P-Channel	I_DP		4.5	5	-0.1	–	–	-0.08•	-0.16	–	-0.055	–	–	mA	
			9.5	10	-0.25	–	–	-0.20•	-0.44	–	-0.14	–	–		
Diode Test 100 µA Test Pin	V_{DF}			–	–	–	1.5•	–	–	1.5•	–	–	1.5•	V	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

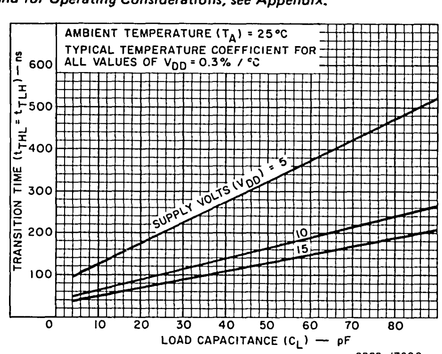

Fig. 6—Typ. transition time vs. C_L.

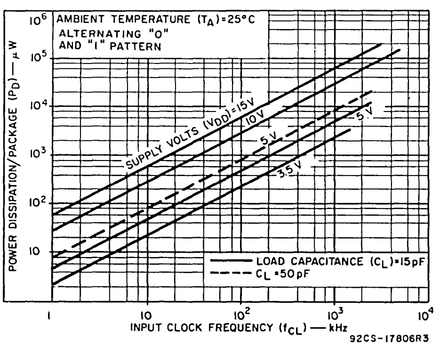

Fig. 7—Typ. dissipation characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF and input rise and fall times = 20 ns except t_rCL, t_fCL Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4021AD, CD4021AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time**	t_{PHL}, t_{PLH}		5	–	300	750	ns	1
			10	–	100	225•		
Transition Time	t_{THL}, t_{TLH}		5	–	150	300	ns	–
			10	–	75	125•		
Minimum Clock Pulse Width	t_{WL} = t_{WH}		5	–	200	500	ns	–
			10	–	100	175		
Minimum High-Level Parallel/Serial Control Pulse Width	$t_{WH(P/S)}$		5	–	200	500	ns	–
			10	–	100	175		
Clock Rise & Fall Time	*t_rCL = t_fCL		5	–	–	15	μs	1
			10	–	–	15•		
Set-Up Time			5	–	100	350	ns	–
			10	–	50	80		
Maximum Clock Frequency	f_{CL}		5	1	2.5	–	MHz	1
			10	3•	5	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

**From Clock or Parallel/Serial Control Input

NOTE 1: Test is a one input one output only

* If more than one unit is cascaded in a parallel clocked operation t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

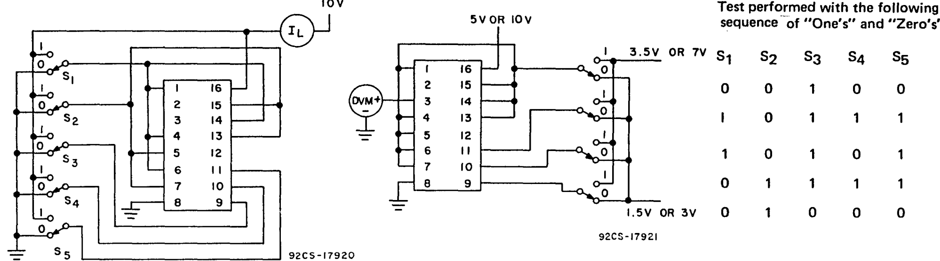

Fig. 8—Quiescent device current test circuit.

Fig. 9—Noise immunity test circuit.

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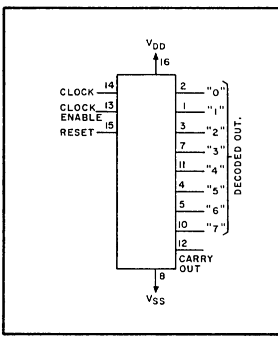
CD4022A/...



High Reliability COS/MOS Divide-By-8 Counter/Divider with 8 Decoded Outputs

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- Medium speed operation. . . . . .5 MHz (typ.) at $V_{DD}-V_{SS}$ = 10 V
- MSI complexity on a single chip
- Divide by N counting; N = 2 to 8 with one CD4022A plus one CD4001A, package

Applications:

- Binary counting/decoding
- Binary frequency division
- Binary counter control/timers

RCA CD4022A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4022A types consist of a 4-stage divide-by-8 Johnson counter, associated decode output gating, and a carry-out bit. The counter is cleared to its zero count by a "high" reset signal. The counter is advanced on the positive clock-signal transition provided the clock enable signal is "low".

Use of the Johnson divide-by-8 counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoder outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decode gating outputs are normally "low" and go "high" only at their respective decoded time slot. Each decode gate output remains "high" for one full clock cycle. The carry-out signal completes one cycle every 8 clock-input cycles and is used as a ripple-carry signal to directly clock a succeeding counter package in a multi-package counting system. These devices are electrically and mechanically identical to standard COS/MOS CD4022A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

RCA Designation	MIL-M-38510 Designation
CD4022A	MIL-M-38510/05604

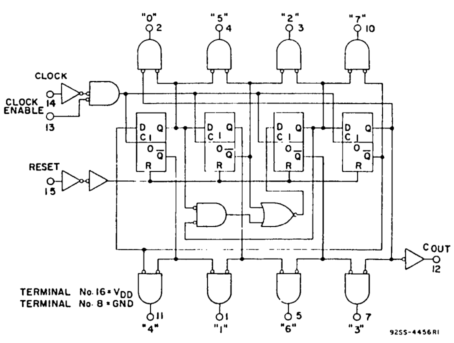


Fig. 1—Logic diagram.

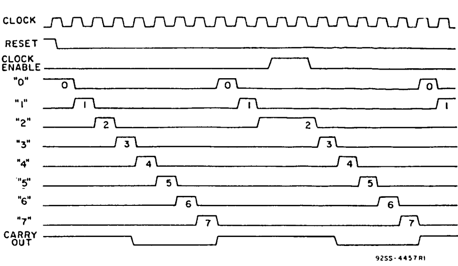


Fig. 2—Timing diagram.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4022A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

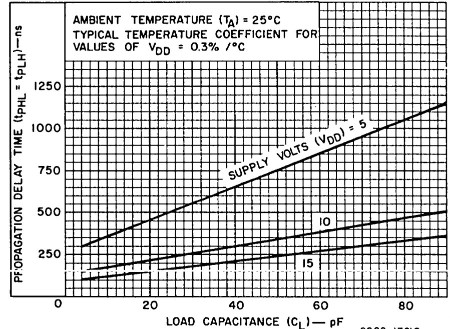


Fig. 3—Typ. propagation delay time vs. C_L for decoded outputs.

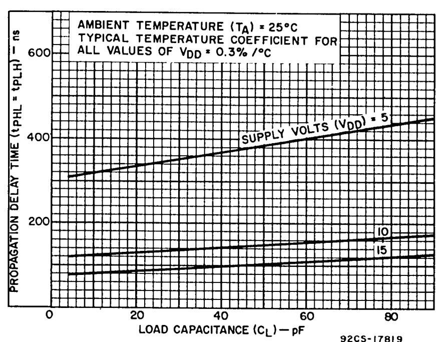


Fig. 4—Typ. propagation delay time vs. C_L for carry output.

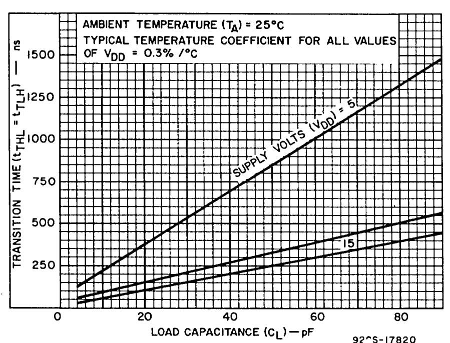


Fig. 5—Typ. transition time vs. C_L for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS (All inputs .... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4022AD, CD4022AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L			5	–	5	–	0.5	5	–	300	μA	2
				10	–	10.	–	1	10.	–	200.		
Quiescent Device Dissipation/Package	P_D			5	–	25	–	2.5	25	–	1500	μW	
				10	–	100	–	10	100	–	2000		
Output Voltage: Low-Level	V_{OL}			3	–	0.55.	–	–	0.5.	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.5	–	0.55.		
High-Level	V_{OH}			3	2.25.	–	2.3.	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.5.	–	–	14.45.	–		
Threshold Voltage: N-Channel	V_{THN}	I_D = -20 μA			-0.7.	-3.	-0.7.	-1.5	-3.	-0.3.	-3.	V	2
P-Channel	V_{THP}	I_D = 20 μA			0.7.	3.	0.7.	1.5	3.	0.3.	3.		
Noise Immunity (All Inputs)	V_{NL}		0.8	5	1.5	–	1.5.	2.25	–	1.4	–	V	1
			1.0	10	3.	–	3	4.5	–	2.9	–		
	V_{NH}		4.2	5	1.4	–	1.5.	2.25	–	1.5	–	V	
			9.0	10	2.9.	–	3.	4.5	–	3.	–		
Output Drive Current N-Channel	I_{DN}	Decoded Outputs	0.5	5	0.062	–	0.05.	0.15	–	0.035	–	mA	2
			0.5	10	0.12	–	0.1.	0.3	–	0.07	–		
		Carry Outputs	0.5	5	0.185	–	0.15.	0.5	–	0.105	–		
			0.5	10	0.375	–	0.3.	1	–	0.21	–		
P-Channel	I_{DP}	Decoded Outputs	4.5	5	-0.038	–	-0.03	-0.075	–	-0.021	–	mA	
			9.5	10	-0.12	–	-0.1.	-0.15	–	-0.035	–		
		Carry Outputs	4.5	5	-0.185	–	-0.15.	-0.4	–	-0.105	–		
			9.5	10	-0.375	–	-0.3.	-0.8	–	-0.21	–		
Diode Test 100 μA Test Pin	–			–	–	1.5.	–	–	1.5.	–	1.5.	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD400CA Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times 20 ns except t_rCL, t_fCL

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C.

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4022AD, CD4022AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
CLOCKED OPERATION								
Propagation Delay Time: Carry-Out Line	t_{PHL} = t_{PLH}		5	–	325	1000	ns	1
			10	–	125	250•		
Decode Out Lines			5	–	400	1200	ns	
			10	–	200	400		
Transition Time: Carry-Out Line	t_{THL} = t_{TLH}		5	–	85	300	ns	
			10	–	50	100		
Decode-Out Lines			5	–	300	900	ns	
			10	–	125	250		
Minimum Clock Pulse Width	t_{WL} = t_{WH}		5	–	250	500	ns	
			10	–	85	170		
Clock Rise & Fall Time	t_rCL = t_fCL		5	–	–	15	μs	1
			10	–	–	15•		
Clock Enable Set-Up Time			5	350	175	–	ns	
			10	150	75	–		
Maximum Clock Frequency	f_{CL}		5	1	2.5	–	MHz	1
			10	3•	5	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	
RESET OPERATION								
Propagation Delay Time: Carry-Out Line	t_{PHL} = t_{PLH}		5	–	300	900	ns	
			10	–	125	250		
Decade-Out Line			5	–	500	1250	ns	
			10	–	200	400		
Minimum Reset Pulse Width	t_{WL} = t_{WH}		5	–	150	300	ns	
			10	–	75	150		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is a one-input, one-output only.

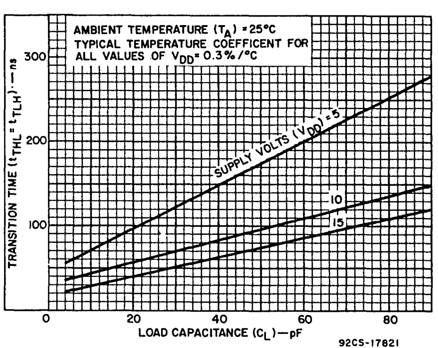


Fig. 6—Typ. transition time vs. C_L for carry output.

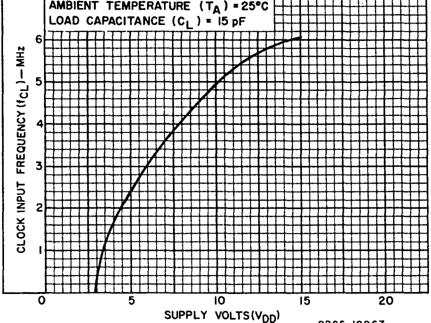


Fig. 7—Typical clock frequency vs. V_{DD}.

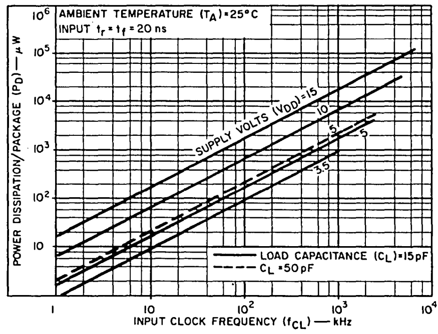


Fig. 8—Typical dissipation characteristics.

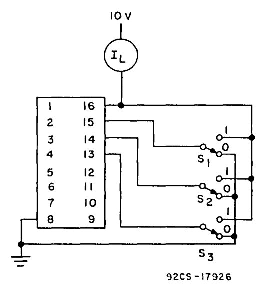


Fig. 9—Quiescent device current test circuit.

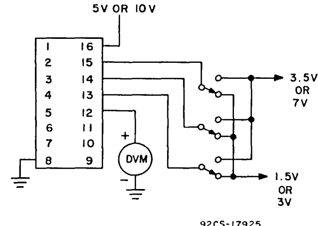


Fig. 10—Noise immunity test circuit.

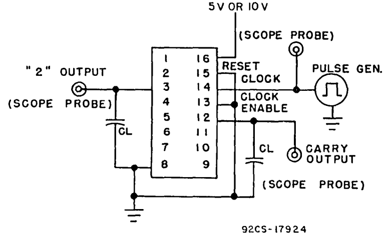


Fig. 11—Clock line test set-up.

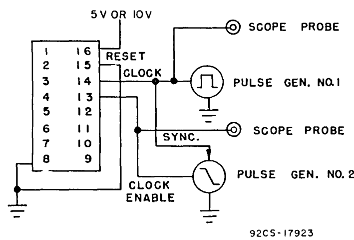


Fig. 12—Clock enable and set-up time test circuit.

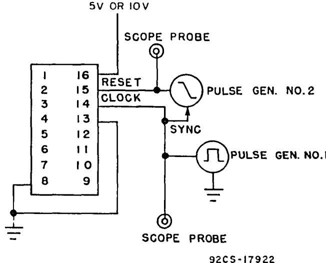


Fig. 13—Reset propagation delay time and minimum reset pulse duration.

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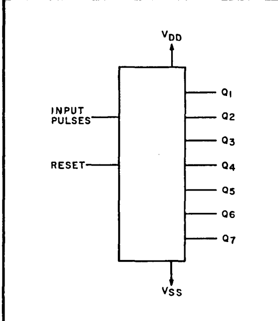
High-Reliability Slash(/) Series

CD4024A/...



High-Reliability COS/MOS 7-Stage Binary Counter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation......7MHz (typ.) input pulse rate at $V_{DD}-V_{SS}$ = 10 V**
- **Low "high" and "low" level output impedance......700Ω and 500Ω (typ.), respectively at $V_{DD}-V_{SS}$ = 10 V**
- **Logic block complexity on a single chip......each output accessible and resettable**
- **Static counter operation—counter retains state indefinitely with input pulse level "low" or "high"**
- **COS/MOS gate input loading on both reset and input-pulse lines**

RCA CD4024A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4024A types consist of an input-pulse-shaping circuit, reset-line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse. These devices are electrically and mechanically identical to standard COS/MOS CD4024A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

RCA Designation	MIL-M-38510 Designation
CD4024A	MIL-M-38510/05605

Applications:

- **Frequency-dividing circuits.**
- **Time-delay circuits**
- **Counter control**
- **D/A counter and switch on one chip**

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4024A "Slash (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

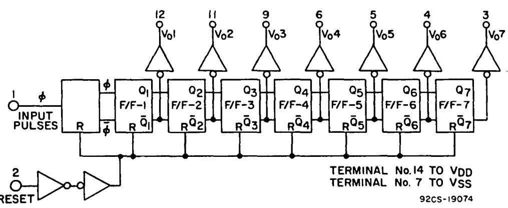


Fig. 1—Functional diagram for CD4024AD, AK.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

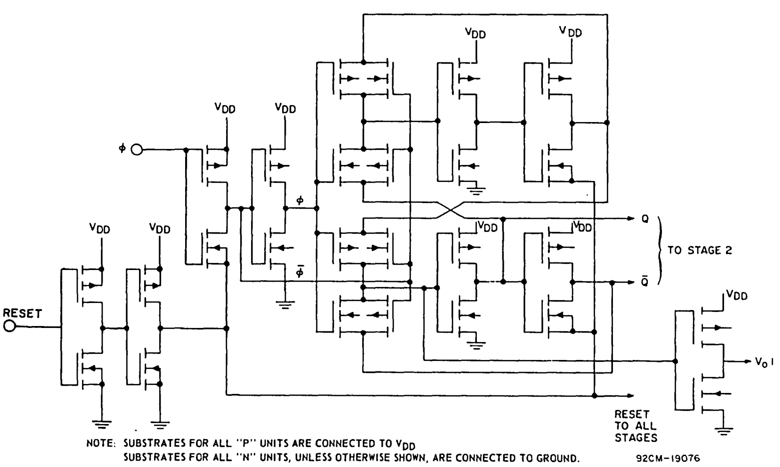


Fig. 2—Schematic diagram (pulse shaper and 1 binary stage).

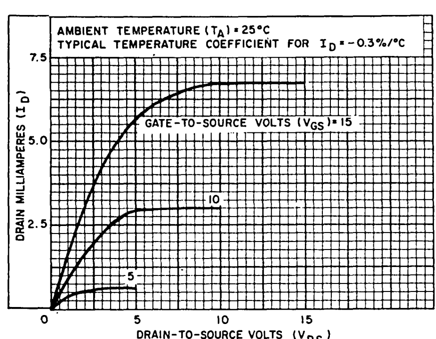


Fig. 3—Min. N-channel drain characteristics.

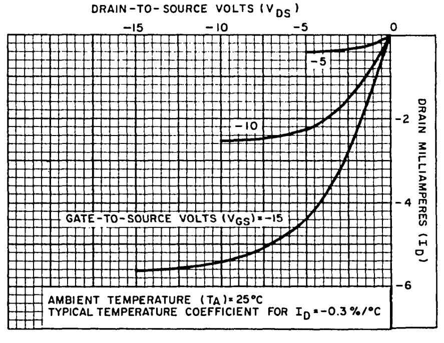


Fig. 4—Min. P-channel drain characteristics.

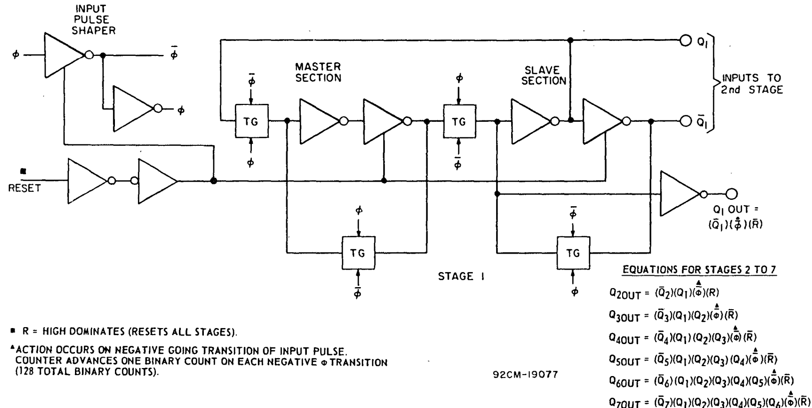


Fig.5— Logic block diagram (pulse shaper and 1 binary stage).

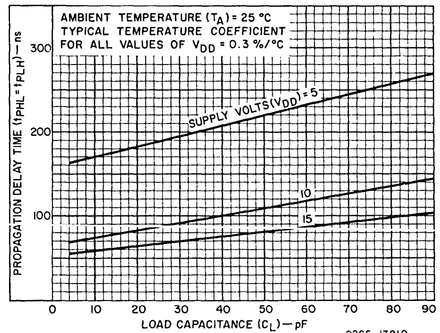


Fig. 6— propagation delay time vs. C_L.

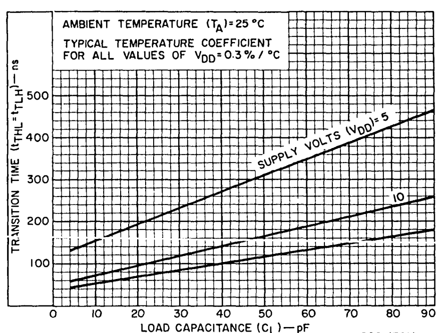


Fig. 7— Typ. transition time vs. C_L.

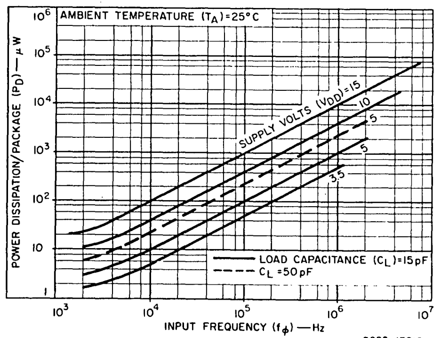


Fig. 8— Typ. dissipation characteristics.

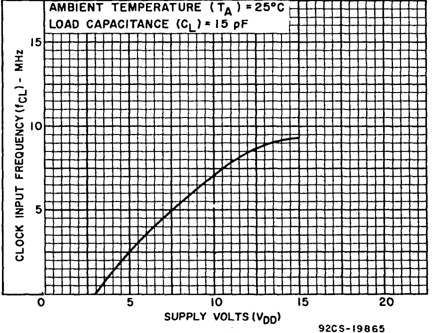


Fig. 9— Typ. input pulse frequency vs. V_{DD}.

STATIC ELECTRICAL CHARACTERISTICS (All inputs .... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4024AD, CD4024AK									UNITS	NOTES
			V_O	V_{DD}	−55°C			25°C			125°C				
			Volts	Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	I_L			5	—	—	5	—	0.5	5	—	—	300	μA	2
				10	—	—	10.	—	1	10.	—	—	200.		
Quiescent Device Dissipation/Package	P_D			5	—	—	25	—	2.5	25	—	—	1500	μW	
				10	—	—	100	—	10	100	—	—	2000		
Output Voltage: Low-Level	V_{OL}		0	3	—	—	0.55.	—	—	0.5.	—	—	—	V	1
				5	—	—	0.01	—	0	0.01	—	—	0.05		
				10	—	—	0.01	—	0	0.01	—	—	0.05		
			0	15	—	—	—	—	—	—	—	—	0.55.		
High-Level	V_{OH}		3	3	2.25.	—	—	2.3.	—	—	—	—	—	V	1
				5	4.99	—	—	4.99	5	—	4.95	—	—		
				10	9.99	—	—	9.99	10	—	9.95	—	—		
			15	15	—	—	—	14.5.	—	—	14.45.	—	—		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = -20 μA			-0.7 •	-1.7	-3 •	-0.7 •	-1.5	-3 •	-0.3 •	-1.3	-3 •	V	2
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7 •	1.7	3 •	0.7 •	1.5	3 •	0.3 •	1.3	3 •	V	
Noise Immunity (All Inputs)	V_{NL}		0.8	5	1.5	—	—	1.5.	2.25	—	1.4.	—	—	V	1
			1.0	10	3.	—	—	3.	4.5	—	2.9.	—	—		
	V_{NH}		4.2	5	1.4	—	—	1.5.	2.25	—	1.5.	—	—	V	
			9.0	10	2.9.	—	—	3.	4.5	—	3.	—	—		
Output Drive Current: N-Channel	I_DN		0.5	5	0.31	—	—	0.25.	0.5	—	0.175	—	—	mA	2
			0.5	10	0.62	—	—	0.5.	1	—	0.35	—	—		
P-Channel	I_DP		4.5	5	-0.19	—	—	-0.15.	0.3	—	-0.105	—	—	mA	
			9.5	10	-0.45	—	—	-0.35.	-0.7	—	-0.25	—	—		
Diode Test 100 μA Test Pin	—				—	—	1.5.	—	—	1.5.	—	—	1.5.	V	3
Input Current	I_I				—	—	—	—	10	—	—	—	—	pA	

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

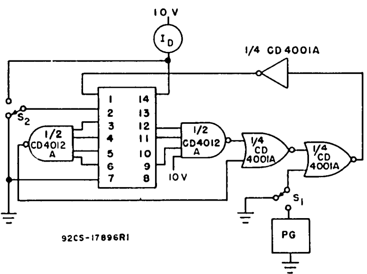


Fig. 10—Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = 0V, C_L = 15pF, and input rise and fall times = 20ns, except $t_r\phi$ and $t_f\phi$. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4024AD, CD4024AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
ϕ INPUT OPERATION								
Propagation Delay Time*	t_{PHL}, t_{PLH}		5	–	175	350	ns	1
			10	–	80	150●		
Transition Time	t_{THL}, t_{TLH}		5	–	175	225	ns	1
			10	–	80	150●		
Minimum Input-Pulse Width	t_{WL}, t_{WH}		5	–	200	330	ns	
			10	–	140	125		
Input Pulse Rise & Fall Time	$t_r\phi$, $t_f\phi$		5	–	–	15	µs	1
			10	–	–	10●		
Maximum Input Pulse Frequency	$f\phi$		5	1.5	2.5	–	MHz	1
			10	4●	7	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	
RESET OPERATION								
Propagation Delay Time	$t_{PHL(R)}$		5	–	500	700	ns	
			10	–	250	350		
Minimum Reset Pulse Width	$t_{WH(R)}$		5	–	375	500	ns	
			10	–	200	300		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is a one-input, one-output only. * Propagation delay time is from clock input to Q_1 output.

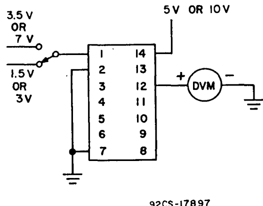


Fig. 11— Noise Immunity test circuit.

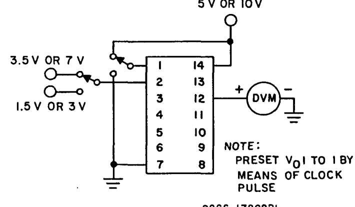


Fig. 12— Reset noise immunity test circuit.

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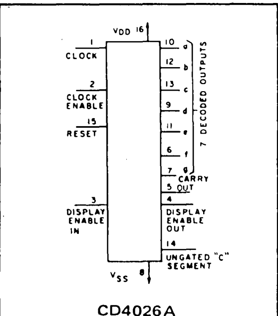
High-Reliability 'Slash' (/) Series
CD4026A/... CD4033A/...



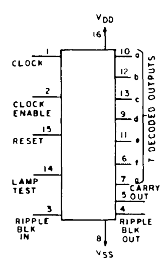
CD4026A

High-Reliability COS/MOS Decade Counters/Dividers

With Decoded 7-Segment Display Outputs and:

Display Enable – CD4026A
Ripple Blanking – CD4033A

Special Features:
- **Counter and 7-segment decoding in one package**
- **Ideal for low-power displays**
- **Easily interfaced with 7-segment display types**
- **Fully static counter operation: DC to 2.5 MHz (typ.)**
- **Display Enable Output (CD4026A)**
- **"Ripple Blanking" and Lamp Test (CD4033A)**



CD4033A

RCA CD4026A and CD4033A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4026A and CD4033A each consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package counter are important.

Inputs common to both types are Clock, Reset, and Clock Enable; common outputs are carry out and seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026A include Display Enable input and Display Enable and Ungated "C-segment" outputs. Signals peculiar to the CD4033A are Ripple-Blanking and Lamp Test inputs and a Ripple-Blanking output.

A "high" Reset signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the Clock Enable signal is "low". Counter advancement via the clock line is inhibited when the Clock Enable signal is "high". Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (C_{out}) Signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multidecade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for

Applications:
- **Decade counting/7-segment decimal display**
- **Frequency division/7-segment decimal displays**
- **Clock/watches/timers (e.g. ÷ 60, ÷ 60, ÷ 12 counter/display)**
- **Counter/display driver for meter applications**

representing the decimal number 0 to 9. The 7-segment outputs go "high" on selection in the CD4033A; in the CD4026A these outputs go "high" only when the Display Enable IN is "high".

CD4026A

When the Display Enable IN is "low" the seven decoded outputs are forced "low" regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of cettain divider functions such as divide-by-60 and divide-by-12.

CD4033A

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display, consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero

suppression on the integer side is obtained by connecting the RB1 terminal of the CD4033A associated with the most significant digit in the display to a "low-level" voltage and connecting the RBO terminal of that stage to the RB1 of the CD4033A in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

On the fraction side of the display the RB1 of the CD4033A associated with the least significant bit is connected to a "low level" voltage and the RBO of the CD4033A is connected to the RB1 terminal of the CD4033A in the next more-significant-bit position. Again, this procedure is continued for all CD4033A's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RB1 of that stage to a "high level" voltage (instead of the RBO of the next more-significant-stage). For Example: optional zero → 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RB1 of the CD4033A associated with it to a "high level" voltage.

Ripple blanking of non-significant zeroes provides an appreciable savings in display power.

The CD4033A has a "Lamp Test" input which, when connected to a "high level" voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the "high" state.

These devices are electrically and mechanically identical with standard COS/MOS CD4026A and CD4033A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4026A and CD4033A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

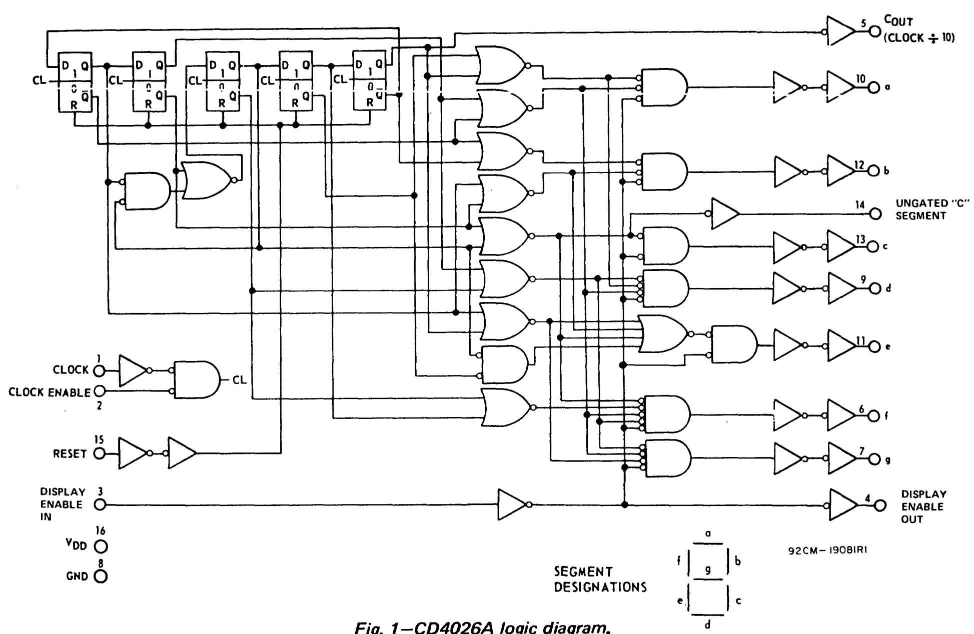


Fig. 1—CD4026A logic diagram.

Fig. 2 – CD4033A logic diagram.

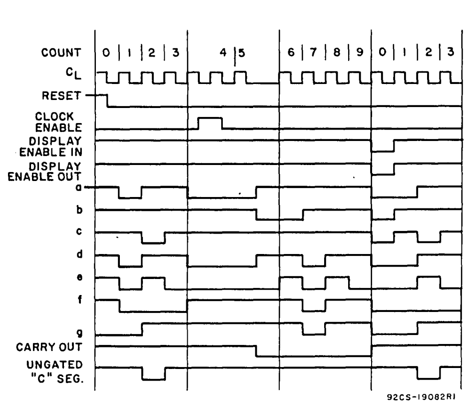


Fig. 3 – CD4026A timing diagram.

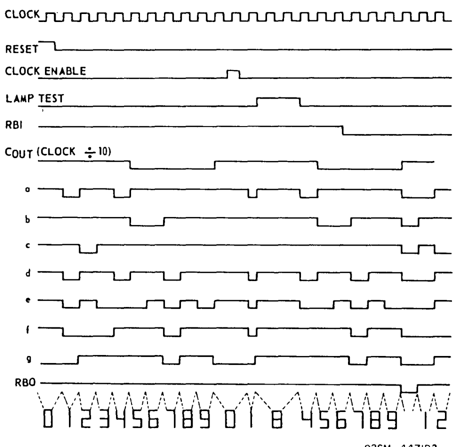


Fig. 4 – CD4033A timing diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: (V_{DD} − V_{SS})	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage (V_{DD} − V_{SS})	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16″ ± 1/32″ (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

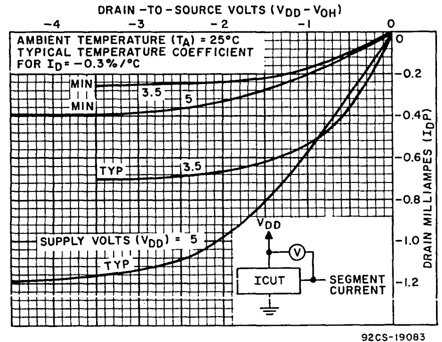


Fig. 5— Min. & typ. P-channel segment drain characteristics @ V_{DD} = 3.5 & 5 V.

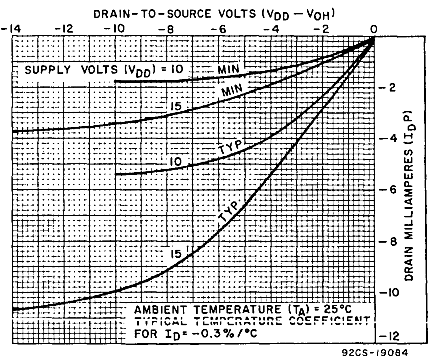


Fig. 6— Min. & typ. P-channel segment drain characteristics @ V_{DD} = 10 & 15 V.

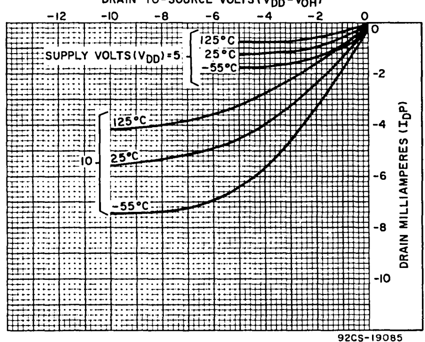


Fig. 7—Typ. P-channel drain characteristics at a function of temp.

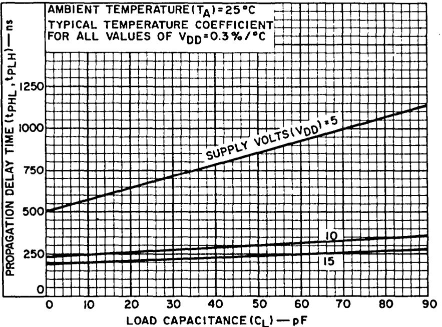


Fig. 8—Typ. propagation delay time vs. C_L for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS (All inputs .... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4026AD, CD4026AK CD4033AD, CD4033AK									UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.		
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	μA	1
				10	–	–	10.	–	1	10.	–	–	200.		
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	μW	
				10	–	–	100	–	10	100	–	–	2000		
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55.	–	–	0.5.	–	–	–	V	1
				5	–	–	0.01	–	0	0.01	–	–	0.05		
				10	–	–	0.01	–	0	0.01	–	–	0.05		
				15	–	–	–	–	–	0.5.	–	–	0.55.		
High-Level	V_{OH}			3	2.25.	–	–	2.3.	–	–	–	–	–	V	1
				5	4.99	–	–	4.99	5	–	4.95	–	–		
				10	9.99	–	–	9.99	10	–	9.95	–	–		
				15	–	–	–	14.5.	–	–	14.45.	–	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = -10 μA			-0.7.	-1.7	-3.	-0.7.	-1.5	-3.	-0.3.	-1.3	-3.	V	2
P-Channel	$V_{TH}P$	I_D = 10 μA			0.7.	1.7	3.	0.7.	1.5	3.	0.3.	1.3	3.	V	
Noise Immunity (All Inputs)	V_{NL}		0.8	5	1.5	–	–	1.5.	2.25	–	1.4	–	–	V	1
			1.0	10	3.	–	–	3.	4.5	–	2.9.	–	–		
For Definition, See Appendix in SSD-207	V_{NH}		4.2	5	1.4	–	–	1.5.	2.25	–	1.5	–	–	V	
			9.0	10	2.9.	–	–	3.	4.5	–	3.	–	–		
Output Drive Current: N-Channel	I_DN	Decoded Outputs	0.5	5	0.15	–	–	0.12.	0.24	–	0.09	–	–	mA	2
			0.5	10	0.32	–	–	0.25.	0.5	–	0.18	–	–		
		Carry Output	0.5	5	0.12	–	–	0.15	0.4	–	0.1	–	–		
			0.5	10	0.45	–	–	0.35	1	–	0.25	–	–		
P-Channel	I_DP	Decoded Outputs	4.5	5	-0.21	–	–	-0.14.	0.28	–	-0.1	–	–	mA	2
			9.5	10	-0.45	–	–	-0.3.	-0.6	–	-0.22	–	–		
		Carry Output	4.5	5	-0.12	–	–	-0.15	-0.4	–	-0.1	–	–		
			9.5	10	-0.45	–	–	-0.35	-1	–	-0.25	–	–		
Diode Test 100 μA	–			–	–	–	1.5.	–	–	1.5.	–	–	1.5.	V	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

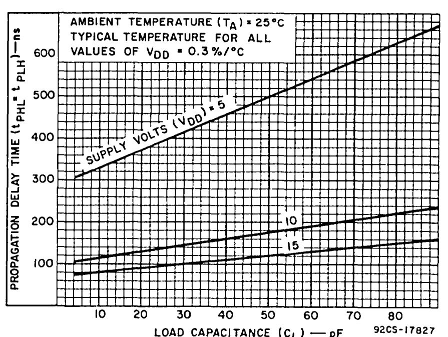


Fig. 9—Typ. propagation delay time vs. C_L for carry outputs.

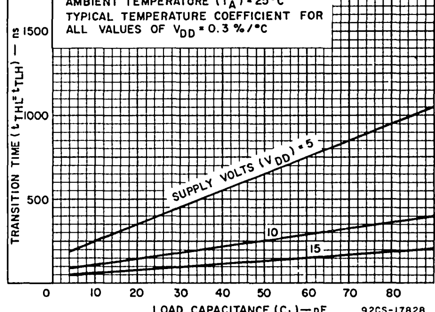


Fig. 10—Typ. transition time vs. C_L for decoded outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V_{SS} = OV, C_L = 15pF, and input rise and fall times - 20 ns, except t_rCL and t_fCL. Typical Temperatuer Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS	NOTES
				CD4026AD, CD4025AK CD4033AD, CE4033AK				
			V_{DD} (Volts)	Min.	Typ.	Max.		
CLOCKED OPERATION								
Propagation Delay Time: Carry Out Line	t_{PHL}		5	–	350	1000	ns	1
			10	–	125	250•		
Decode Out Lines	t_{PLH}		5	–	600	1700	ns	
			10	–	250	500		
Transition Time: Carry Out Line	t_{THL}		5	–	100	300	ns	
			10	–	50	150		
Decode Out Lines	t_{TLH}		5	–	300	900	ns	
			10	–	125	350		
Minimum Clock Pulse Width	t_{WL} t_{WH}		5	–	200	300	ns	
			10	–	100	170		
Clock Rise & Fall Time	t_rCL t_fCL		5	–	–	15	μs	1
			10	–	–	15.		
Clock Enable Set-Up Time			5	–	175	500	ns	
			10	–	75	200		
Maximum Clock Frequency	f_{CL}	Measured with Respect to Carry Out Line	5	1.5	2.5	–	MHz	1
			10	3.	5	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	
RESET OPERATION								
Propagation Delay Time: To Carry Out Line	$t_{PHL(R)}$		5	–	350	1000	ns	1
			10	–	125	125		
To Decode Out Lines			5	–	550	1400	ns	
			10	–	240	500		
Reset Pulse Width	$t_{WH(R)}$		5	–	200	330	ns	
			10	–	100	165		
Reset Removal Time			5	–	300	750	ns	
			10	–	100	225		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input, one output only.

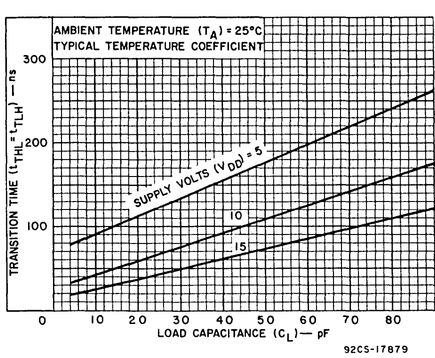


Fig. 11—Typ. transition time vs. C_L for carry output

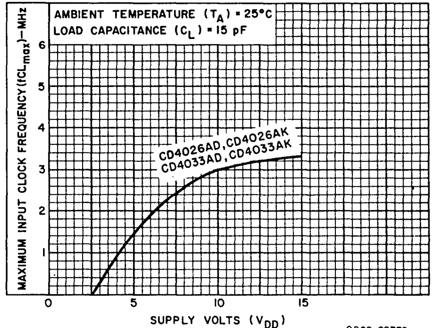


Fig. 12—Max. input clock frequency vs. V_{DD}.

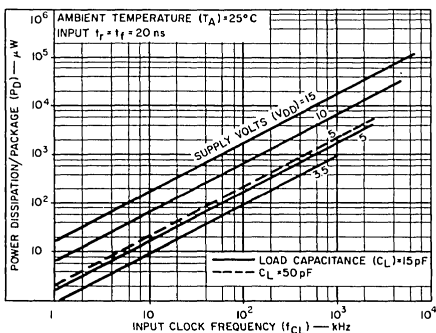


Fig. 13—Typ. dissipation characteristics.

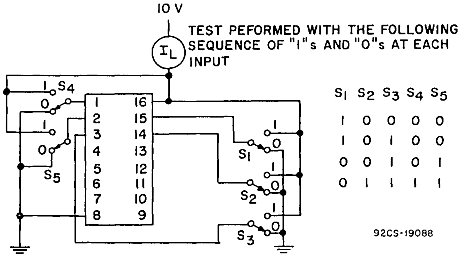


Fig. 14—Quiescent device current test circuit.

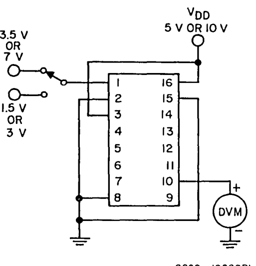


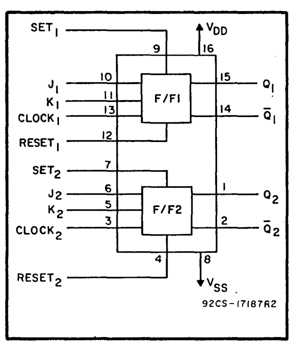
Fig. 15—Noise immunity test circuit.

Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4027A/...



High-Reliability COS/MOS Dual J-K Master-Slave Flip Flop

With Set/Reset Capability
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

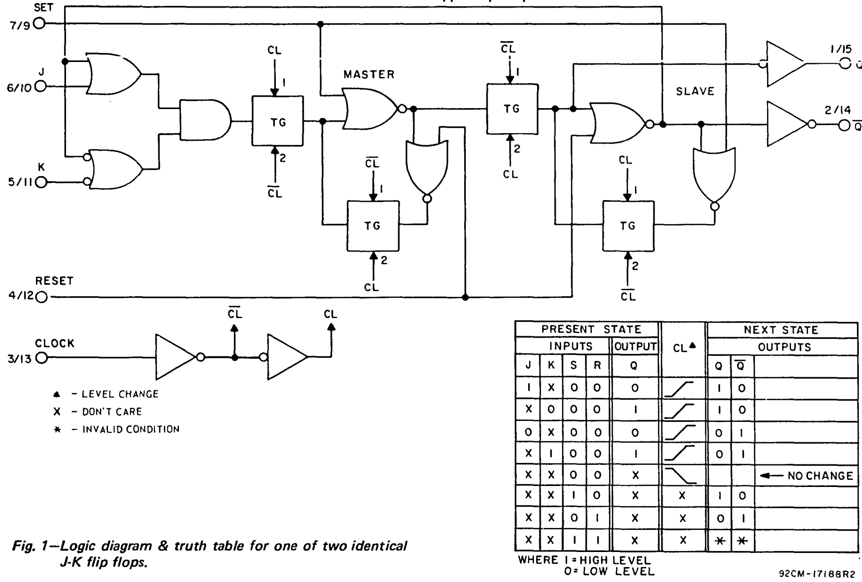
Special Features:

- **Static flip-flop operation......retains state indefinitely with clock level either "high" or low"**
- **Medium speed operation......8 MHz (typ.) clock toggle rate at $V_{DD}-V_{SS} = 10$ V**
- **Low "high"-and "low" output impedance......700Ω and 300Ω, respectively, at $V_{DD}-V_{SS} = 10$ V**

Applications:

- **Registers, counters, control circuits**

RCA CD4027A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4027A is a single monolithic chip integrated circuit containing two identical complementary-symmetry "J-K" master-slave flip-flops. Each flip-flop has provisions for individual "J" "K", "Set", "Reset", and "Clock" input signals. Buffered "Q" and "Q" signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA CD4013A dual "D" type flip-flop.



PRESENT STATE						NEXT STATE		
INPUTS				OUTPUT	CL▲	OUTPUTS		
J	K	S	R	Q		Q	Q̄	
1	X	0	0	0	⟋	1	0	
X	0	0	0	1	⟋	1	0	
0	X	0	0	0	⟋	0	1	
X	1	0	0	1	⟋	0	1	
X	X	0	0	X	⟍			← NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	*	*	

Fig. 1—Logic diagram & truth table for one of two identical J-K flip flops.

The CD4027A is useful in performing control, register, and toggle functions. Logic levels present at the "J" and "K" inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the "clock" pulse. Set and reset functions are independent of the clock and are initiated when a "high"-level signal is present at either the "Set" or "Reset" input.

These devices are electrically and mechanically identical to standard COS/MOS CD4027A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA High-Reliability "Slash" (/) series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series types."

RCA Designation	MIL-M-38510 Designation
CD4027A	MIL-M-38510/05102

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4027A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

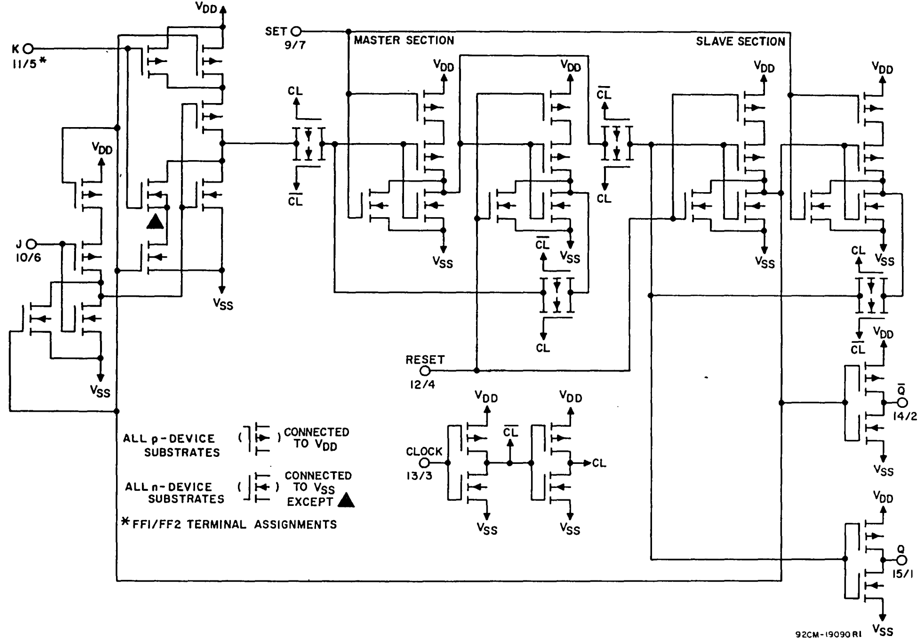


Fig. 2—Schematic diagram for one of two identical J-K flip flops.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4027AD, CD4027AK							UNITS	NOTES
		V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L		5	–	1	–	0.005	1	–	60	µA	1
			10	–	2•	–	0.005	2•	–	40•		
Quiescent Device Dissipation/Package	P_D		5	–	5	–	0.025	5	–	300	µW	–
			10	–	20	–	0.05	20	–	400		
Output Voltage Low-Level	V_{OL}		3	–	0.55•	–	–	0.5•	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	–	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.5•	–	–	1445•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = -10 µA		-0.7•	-3•	-0.7•	-1.5	-3•	-0.3•	-3•	V	2
P-Channel	$V_{TH}P$	I_D = 10 µA		0.7•	3•	0.7•	1.5	3•	0.3	3•	V	
Noise Immunity (All Inputs)	V_{NL}	0.8	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
		1.0	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix	V_{NH}	4.2	5	1.4	–	1.5•	2.25	–	1.5	–	V	
		9.0	10	2.9•	–	3•	–	–	3•	–		
Output Drive Current: N-Channel	I_DN	0.5	5	0.63	–	0.5•	1	–	0.33	–	mA	2
		0.5	10	1.25	–	1.0•	2.5	–	0.7	–		
P-Channel	I_DP	4.5	5	-0.31	–	-0.25•	-0.5	–	-0.175	–	mA	
		9.5	10	-0.8	–	-0.65•	-1.3	–	-0.45	–		
Diode Test 100 µA Test Pin	–			–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I			–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

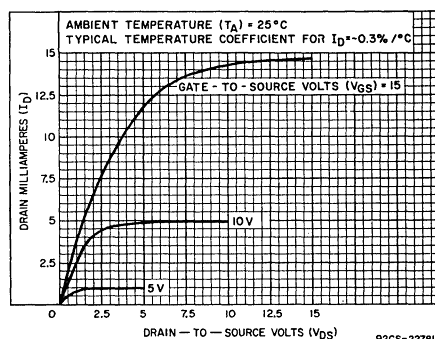


Fig. 3—Min. N-channel drain characteristics.

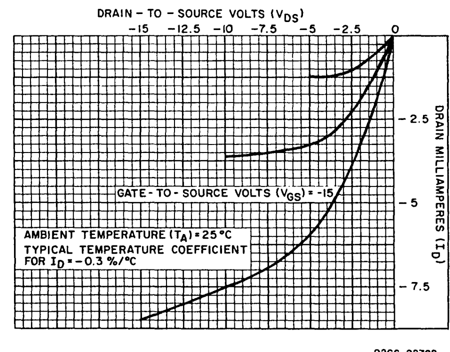


Fig. 4—Min. P-channel drain characteristics.

Dynamic Electrical Characteristics at T_A = 25°C, V_{SS} = 0V, C_L = 15pF, and input rise and fall times = 20 ns, except t_rCL and t_fCL. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4027AD, CD4027AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	150	300	ns	1
			10	–	75	110•		
Transition Time	t_{THL}, t_{TLH}		5	–	75	125	ns	–
			10	–	50	70		
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	165	330	ns	
			10	–	65	110		
Clock Rise & Fall Time	*t_{rCL}, t_{fCL}		5	–	–	15	μs	1
			10	–	–	5•		
Set-Up Time			5	–	70	150	ns	–
			10	–	25	50		
Maximum Clock Frequency (toggle mode)	f_{CL}		5	1.5	3	–	MHz	1
			10	4.5•	8	–		
Input Capacitance	C_I		–	–	5	–	pF	–
SET & RESET OPERATION								
Propagation Delay Time	$t_{PHL(R)}$, $t_{PLH(S)}$		5	–	175	225	ns	–
			10	–	75	110		
Minimum Set and Reset Pulse Widths	$t_{WH(S)}$, $t_{WL(R)}$		5	–	125	200	ns	
			10	–	50	80		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
NOTE 1: Test is a one input one output only.

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

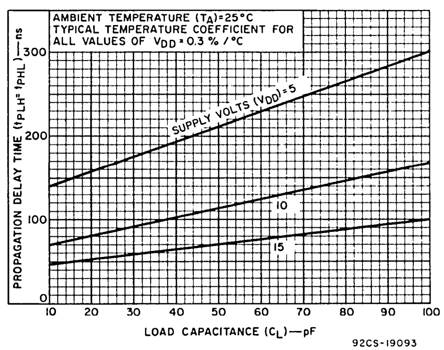


Fig. 5– Typ. propagation delay time vs. C_L.

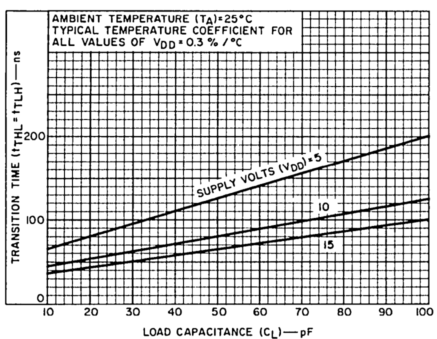


Fig. 6– Typ. transition time vs. C_L.

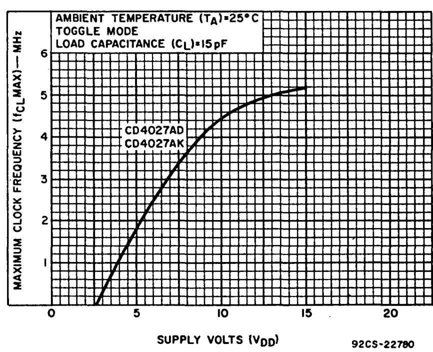


Fig. 7—Max. clock frequency vs. supply voltage.

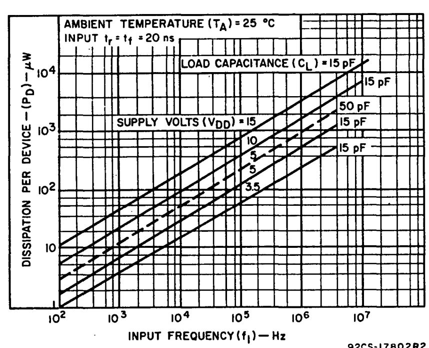


Fig. 8— Typ. dissipation characteristics.

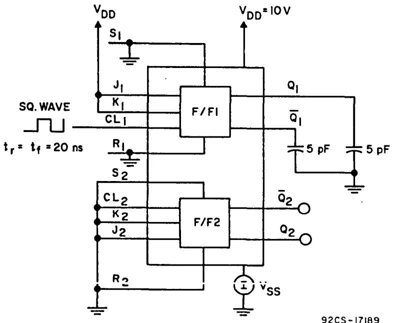


Fig. 9— Dissipation test circuit.

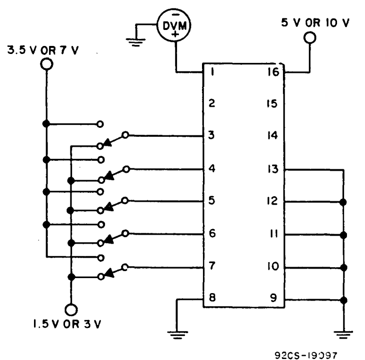
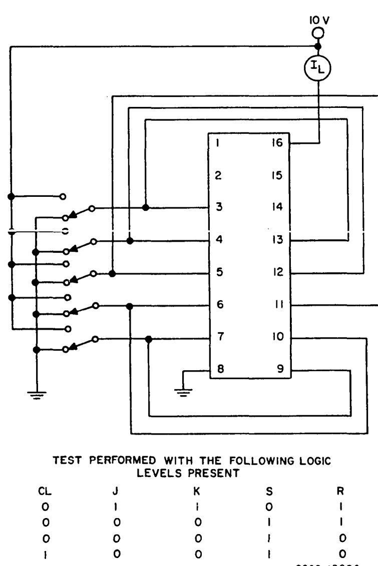


Fig. 11— Noise-immunity test circuit.



TEST PERFORMED WITH THE FOLLOWING LOGIC LEVELS PRESENT

CL	J	K	S	R
0	1	1	0	1
0	0	0	1	1
0	0	0	1	0
1	0	0	1	0

Fig. 10—Quiescent device current test circuit.

File No. 735

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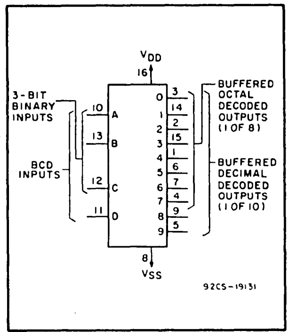
Monolithic Silicon

High-Reliability Slash(/) Series

CD4028A/...



High-Reliability COS/MOS BCD-to-Decimal Decoder

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **BCD to decimal decoding or binary to octal decoding**
- **High decoded output drive capability. . . . . 8 mA (typ.) sink or source**
- **"Positive Logic" inputs and outputs. . . . . decoded outputs go "high" on selection**
- **Medium speed operation. . . . . t_{THL}, t_{TLH} = 30 ns (typ.) @ V_{DD} = 10 V**

Applications:

- **Code conversion**
- **Indicator-tube decoder**
- **Address decoding—memory selection control**

RCA CD4028A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a "high" level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A "high"-level signal at the D input inhibits octal decoding and causes inputs 0 through 7 to go "low". If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications. All inputs and outputs are protected against electrostatic effects.

These devices are electrically and mechanically identical with standard COS/MOS CD4028A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical,

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

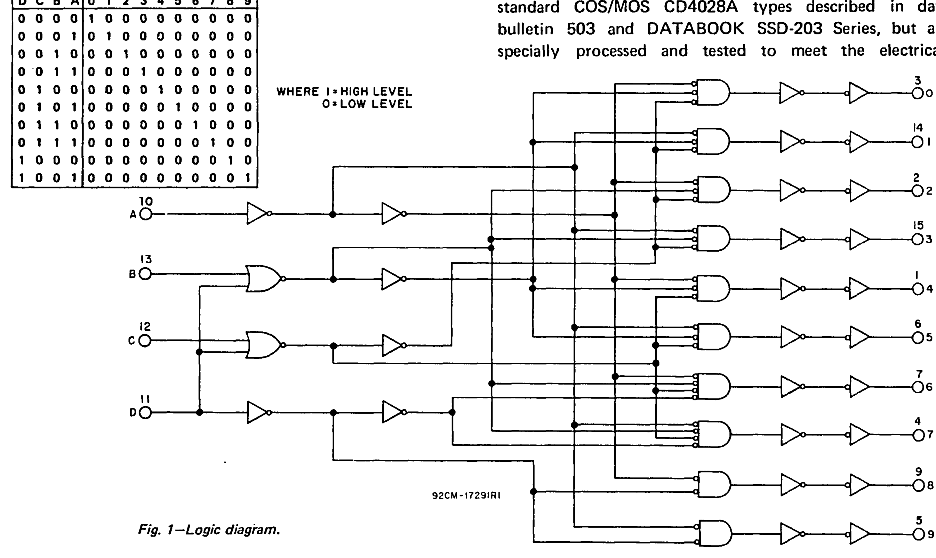


Fig. 1—Logic diagram.

mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4028A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

STATIC ELECTRICAL CHARACTERISTICS (All inputs .... $V_{SS} \leqslant V_I \leqslant V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS CD4028AD, CD4028AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	μA	1
				10	–	–	10•	–	1	10•	–	–	200•		
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	μW	
				10	–	–	100	–	10	100	–	–	2000		
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55•	–	–	0.5•	–	–	–	V	1
				5	–	–	0.01	–	0	0.01	–	–	0.05		
				10	–	–	0.01	–	0	0.01	–	–	0.05		
				15	–	–	–	–	–	0.5•	–	–	0.55•		
High-Level	V_{OH}			3	2.25•	–	–	2.3•	–	–	–	–	–	V	1
				5	4.99	–	–	4.99	5	–	4.95	–	–		
				10	9.99	–	–	9.99	10	–	9.95	–	–		
				15	–	–	–	14.5•	–	–	14.45•	–	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = -20 μA			-0.7•	-1.7	-3•	-0.7•	-1.5	-3•	-0.3•	-1.3	-3•	V	2
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7•	1.7	3•	0.7•	1.5	3•	0.3•	-1.3	3•	V	
Noise Immunity (All Inputs)	V_{NL}		0.8	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	1
			1.0	10	3•	–	–	3•	4.5	–	2.9•	–	–		
	V_{NH}		4.2	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V	
			9.0	10	2.9•	–	–	3•	4.5	–	3•	–	–		
Output Drive Current N-Channel	$I_D N$		0.5	5	0.75	–	–	0.6•	1.2	–	0.45	–	–	mA	2
			0.5	10	1.5	–	–	1.2•	2.4	–	0.9	–	–		
P-Channel	$I_D P$		4.5	5	-0.7	–	–	-0.37•	-0.9	–	-0.32	–	–	mA	
			9.5	10	-1.4	–	–	-0.9•	-1.9	–	-0.65	–	–		
Diode Test 100 μA Test Pin	–			–	–	–	1.5•	–	–	1.5•	–	–	1.5•	V	3
Input Current	I_I			–	–	–	–	–	10	–	–	–	–	pA	

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = 0V, C_l = 15pF, and all input rise and fall times = 20 ns Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS	NOTES
				CD4028AD, CD4028AK				
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	250	480	ns	1
			10	–	100	180.		
Transition Time	t_{THL}, t_{TLH}		5	–	60	150	ns	1
			10	–	30	75.		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is a one-input, one output only.

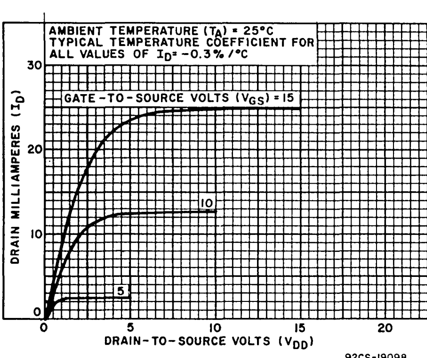


Fig. 2—Typ. N-channel drain characteristics.

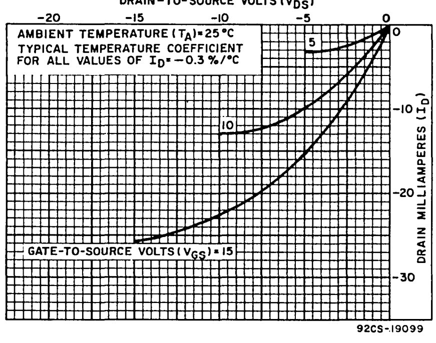


Fig. 3—Typ. P-channel drain characteristics.

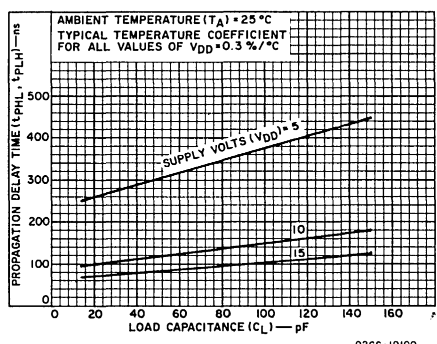


Fig.4—Typ. propagation delay time vs. C_L.

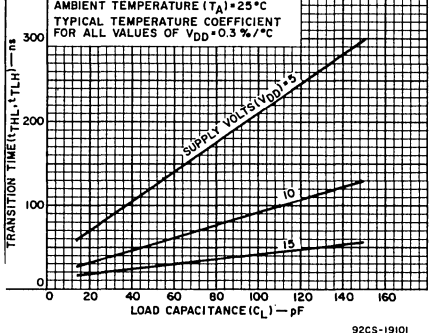


Fig. 5—Typ. transition time vs. C_L.

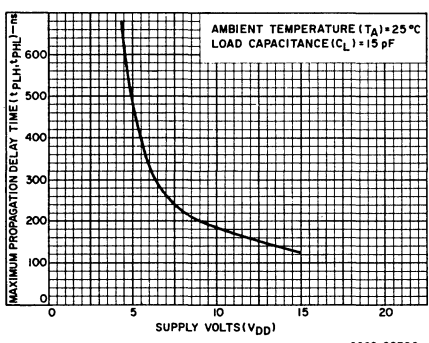


Fig. 6—Max. propagation delay time vs. V_{DD}.

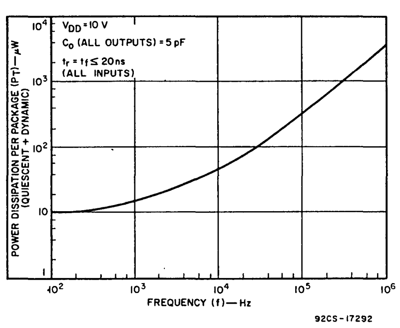


Fig. 7—Dissipation vs. input frequency.

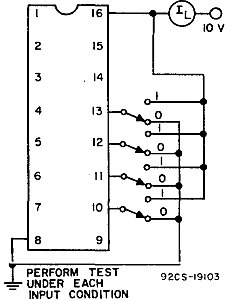


Fig. 8—Quiescent device current test circuit.

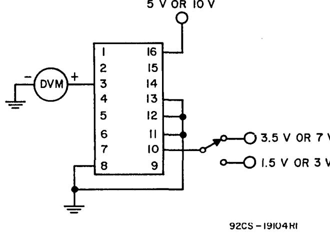


Fig.9 — Noise-immunity test circuit.

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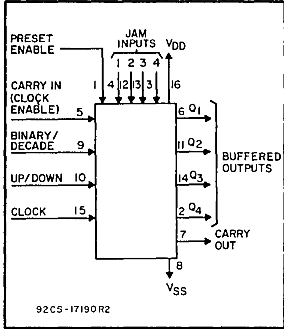

High-Reliability COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation. . . . 5 MHz (typ.) @ C_L = 15 pF and $V_{DD}-V_{SS}$ = 10 V**
- **Multi-package parallel clocking for synchronous high speed output response of ripple clocking for slow clock input rise and fall times**
- **"Preset Enable" and individual "Jam" inputs provided**
- **Binary or decade up/down counting**
- **BCD outputs in decade mode**

Applications:

- **Programmable binary and decade counting/frequency synthesizers-BCD output**
- **Analog to digital and digital to analog conversion**
- **Up/Down binary counting**
- **Up/Down decade counting**
- **Magnitude and sign generation**
- **Difference counting**

RCA CD4029A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4029A types consist of a four-stage binary or BCD decade up/down counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Binary/Decade, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-Out signal are provided as outputs.

A "high" Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the clock. A "low" on each Jam line, when the Preset-Enable signal is "high", resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the Carry-In and Preset-Enable signals are "low". Advancement is inhibited when the Carry-In or Preset-Enable signals are "high". The Carry-Out signal is normally "high" and goes "low" when the counter reaches its maximum count in the "Up" mode or the minimum count in the "Down" mode provided the Carry-In signal is "low". The Carry-In signal in the "low" state can thus be considered a Clock Enable. The Carry-In terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the Binary/Decade input is "high"; the counter counts in the Decade mode when the Binary/Decade input is "low". The counter counts "Up" when the Up/Down input is "high", and "Down" when the Up/Down input is "low". Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 10. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

These devices are electrically and mechanically identical with standard COS/MOS CD4029A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical,

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4029A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Parameter	Value
Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

BINARY/DECADE 9; PRESET ENABLE 1; CARRY IN 5 (CLOCK ENABLE); UP/DOWN 10; CLOCK 15; 4 J_1; 12 J_2; 13 J_3; 3 J_4; V_{SS}=8; V_{DD}=16; CARRY OUT 7; 6 Q_1; 11 Q_2; 14 Q_3; 2 Q_4

* TRUTH TABLE FOR F-F No.1

CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
↓	1	1	X	$\bar{Q}$	Q
X	X	0	1	1	Q
↓	0	1	X	Q	$\bar{Q}$ NC
↑	X	1	X	Q	$\bar{Q}$ NC

** TRUTH TABLE FOR F-F'S 2,3,4

CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
↓	0	1	X	$\bar{Q}$	Q
X	X	0	1	1	0
↓	1	1	X	Q	$\bar{Q}$ NC
↑	X	1	X	Q	$\bar{Q}$ NC

NC-NO CHANGE TE-TOGGLE ENABLE X-DON'T CARE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	1 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	1 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	1 0	JAM IN NO JAM
CARRY IN (CI) (CLOCK ENABLE)	1 0	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION ADVANCE COUNTER AT POS. CLOCK TRANSITION

92CL-17191R1

Fig. 1—Logic diagram.

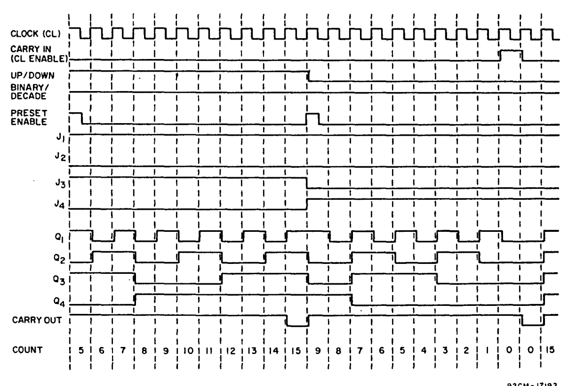

Fig. 2—Timing diagram-binary mode.

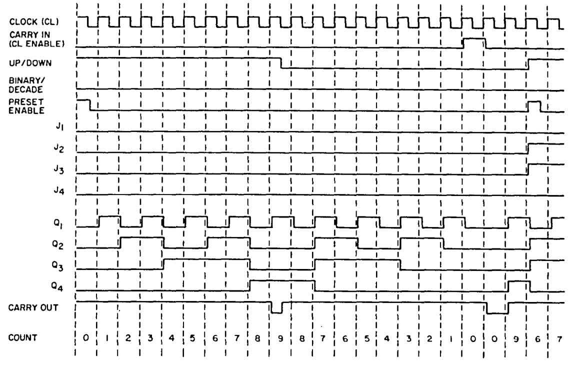

Fig. 3—Timing diagram-decade mode.

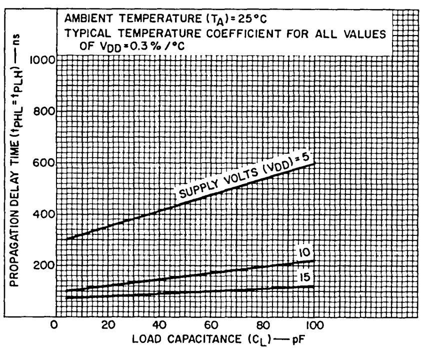

Fig. 4—Typ. propagation delay time vs. C_L for Q outputs.

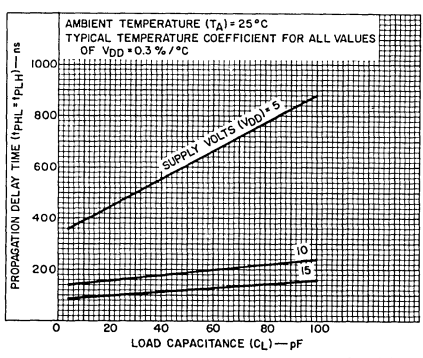

Fig. 5—Typ. propagation delay time vs. C_L for carry output.

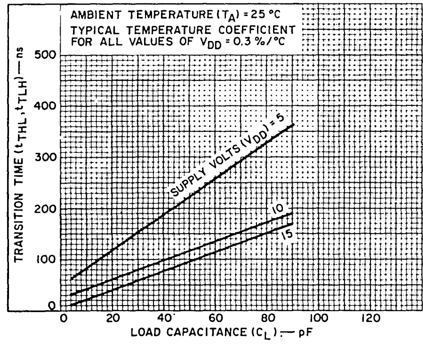

Fig. 6—Typ. transition time vs. C_L for Q outputs.

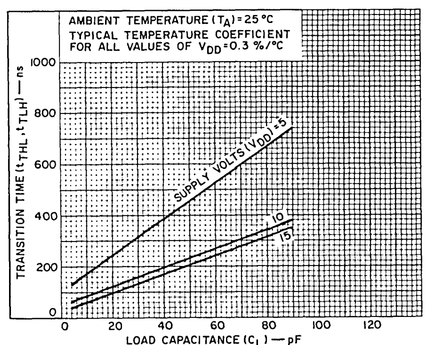

Fig. 7—Typ. transition time vs. C_L for carry output.

STATIC ELECTRICAL CHARACTERISTICS (All inputs .... $V_{SS} \leqslant V_I \leqslant V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4029AD, CD4029AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	-55°C Min.	-55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L			5	–	5	–	0.5	5	–	300	μA	1
				10	–	10.	–	1	10.	–	200.		
Quiescent Device Dissipation/Package	P_D			5	–	25	–	2.5	25	–	1500	μW	
				10	–	100	–	10	100	–	2000		
Output Voltage: Low-Level	V_{OL}			3	–	0.55.	–	–	0.5.	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.5.	–	0.55.		
High-Level	V_{OH}			3	2.25.	–	2.3.	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10.	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.5.	–	–	14.45.	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = -20 μA			-0.7.	-3.	-0.7.	-1.5	-3.	-0.3.	-3.	V	2
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7.	3.	0.7.	1.5	3.	0.3.	3.	V	
Noise Immunity (All Inputs) *For Definition, See Appendix*	V_{NL}		0.8	5	1.5	–	1.5.	2.25	–	1.4	–	V	1
			1.0	10	3.	–	3.	4.5	–	2.9.	–		
	V_{NH}		4.2	5	1.4	–	1.5.	2.25	–	1.5	–	V	
			9.0	10	2.9.	–	3.	4.5	–	3.	–		
Output Drive Current N-Channel	I_DN	Q Outputs	0.5	5	0.5	–	0.4.	0.15	–	0.28	–	mA	1
			0.5	10	0.74	–	0.6.	0.3	–	0.42	–		
		Carry Outputs	0.5	5	0.1	–	0.08.	0.5	–	0.06	–		
			0.5	10	0.4	–	0.32.	1	–	0.22	–		
P-Channel	I_DP	Q Output	4.5	5	-0.18	–	-0.12.	-0.075	–	-0.08	–	mA	
			9.5	10	-0.3	–	-0.2.	-0.15	–	-0.14	–		
		Carry Output	4.5	5	-0.09	–	-0.06.	-0.4	–	-0.04	–		
			9.5	10	-0.15	–	-0.1.	-0.8	–	-0.01	–		
Diode Test 100 μA Test Pin	–				–	1.5.	–	–	1.5.	–	1.5.	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or a one output only.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = 0V, C_L = 15 pF, and input rise and fall times = 20 ns, except t_rCL and t_fCL Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4029AD, CD4029AK Min.	Typ.	Max.	UNITS	NOTES
CLOCKED OPERATION								
Propagation Delay Time: Q Outputs	t_{PHL}, t_{PLH}		5	–	325	650	ns	1
			10	–	115	230•		
Carry Output			5	–	425	850	ns	1
			10	–	150	300•		
Transition Time: Q Outputs	t_{THL}, t_{TLH}		5	–	100	200	ns	–
			10	–	50	100		
Carry Output			5	–	200	400	ns	–
			10	–	100	200		
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	340	ns	–
			10	–	100	170		
Clock Rise & Fall Time	t_rCL, ▲ t_fCL		5	–	–	15	μs	–
			10	–	–	15•		
Set-Up Times *	t_{SHL}, t_{SLH}		5	–	325	650	ns	–
			10	–	115	230		
Maximum Clock Frequency	f_{CL}		5	1.5	2.5	–	MHz	–
			10	3•	5	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	–
PRESET ENABLE								
Propagation Delay Time: Q Outputs	t_{PHL}, t_{PLH}		5	–	325	650	ns	–
			10	–	115	230		
Carry Output			5	–	425	850	ns	–
			10	–	150	300		
Reset Enable Pulse Width	t_{WH}		5	–	115	330	ns	–
			10	–	80	160		
Preset Enable Removal Time	t_{rem}		5	–	325	650	ns	–
			10	–	115	230		
CARRY INPUT								
Propagation Delay Time: Carry Output	t_{PHL}, t_{PLH}		5	–	175	350	ns	–
			10	–	50	100		

* From Up/Down, Binary/Decade or Carry Input Control Inputs to Clock Input.

▲ If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimate capacitive load.

NOTE 1: Test is a one-input, one-output only.

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

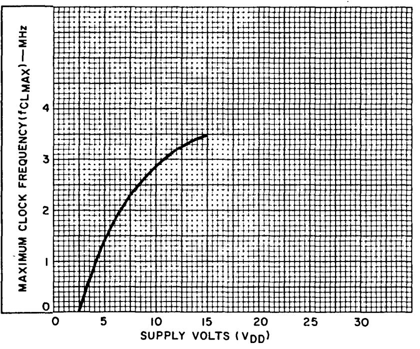

Fig. 8—Max. clock frequency vs. V_{DD}.

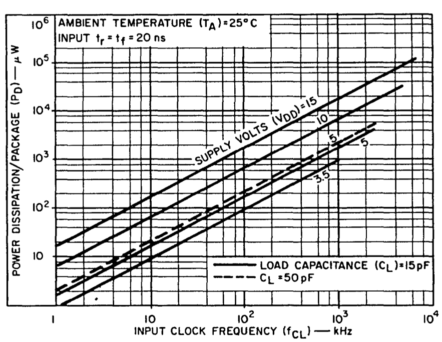

Fig. 9—Typ. dissipation characteristics.

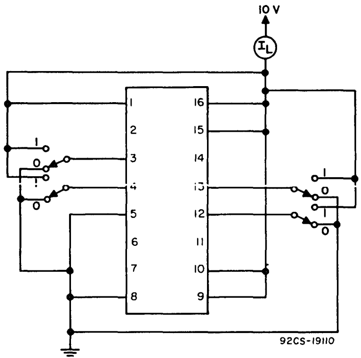

Fig. 10—Quiescent device current test circuit.

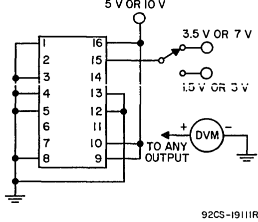

Fig. 11— Noise-immunity test circuit.

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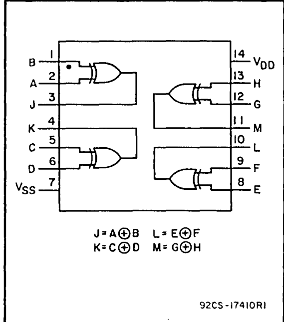
High-Reliability Slash(/) Series CD4030A/...



High-Reliability COS/MOS Quad Exclusive-OR Gate

(Positive Logic)

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation** .... $t_{PHL} = t_{PLH}$ = 40 ns (typ.) @ C_L = 15 pF and $V_{DD}-V_{SS}$ = 10 V
- **Low output impedance** .... 500Ω (typ.) @ $V_{DD}-V_{SS}$ = 10 V

Applications:

- **Even and odd-parity generators and checkers**
- **Logical comparators**
- **Adders/subtractors**
- **General logic functions**

RCA CD4030A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4030A types each contain four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four N-channel and four P-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

These devices are electrically and mechanically identical with standard COS/MOS CD4030A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4030A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14 lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

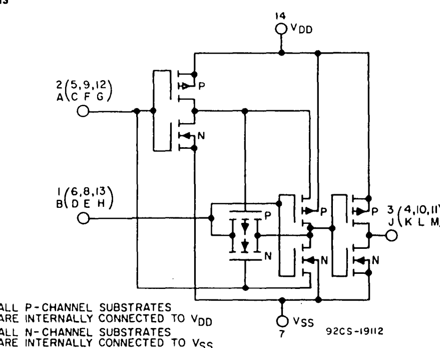


Fig. 1—Schematic diagram for 1 of 4 identical exclusive-OR gates.

TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

WHERE "1" = HIGH LEVEL
"0" = LOW LEVEL

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . $V_{SS} \leqslant V_I \geqslant V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4030AD, CD4030AK									UNITS	NOTES
		V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.		
Quiescent Device Current	I_L		5	–	–	0.5	–	0.005	0.5	–	–	30	µA	1
			10	–	–	0.5•	–	0.01	0.5•	–	–	10•		
Quiescent Device Dissipation/Package	P_D		5	–	–	2.5	–	0.025	1.5	–	–	150	µW	
			10	–	–	10	–	0.1	10	–	–	100		
Output Voltage: Low-Level	V_{OL}		3	–	–	0.55•	–	–	0.5•	–	–	–	V	1
			5	–	–	0.01	–	0	0.01	–	–	0.05		
			10	–	–	0.01	–	0	0.01	–	–	0.05		
			15	–	–	–	–	–	0.5•	–	–	0.55•		
High-Level	V_{OH}		3	2.25•	–	–	2.3•	–	–	–	–	–	V	1
			5	4.99	–	–	4.99	5	–	4.95	–	–		
			10	9.99	–	–	9.99	10	–	9.95	–	–		
			15	–	–	–	14.5•	–	–	14.45•	–	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = -10µA		-0.7•	-1.7	-3•	-0.7•	-1.5	-3•	-0.3•	-1.3	-3•	V	2
P-Channel	$V_{TH}P$	I_D = 10µA		0.7•	1.7	3•	-0.7•	1.5	3•	0.3•	1.3	3•	V	
Noise Immunity (All inputs)	V_{NL}	0.95	5	1.5	–	–	1.5•	2.25	–	1.4•	–	–	V	1
For Definition,		2.9	10	3•	–	–	3•	4.5	–	2.9	–	–		
See Appendix in	V_{NH}	3.6	5	1.4	–	–	1.5•	2.25	–	1.5•	–	–	V	
SSD-207		7.2	10	2.9•	–	–	3•	4.5	–	3	–	–		
Output Drive Current: N-Channel	$I_D N$	0.5	5	0.75	–	–	0.6•	1.2	–	0.45	–	–	mA	2
		0.5	10	1.5	–	–	1.2•	2.4	–	0.9	–	–		
P-Channel	$I_D P$	4.5	5	-0.45	–	–	-0.25•	-0.6	–	-0.21	–	–	mA	
		9.5	10	-0.95	–	–	-0.6•	-1.3	–	-0.45	–	–		
Diode Test 100µA Test Pin	–			–	–	1.5•	–	–	1.5•	–	–	1.5•	V	3
Input Current	I_I	V_I = O or V_{DD}		–	–	–	–	10	–	–	–	–	pA	

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range . . . . −65 to +150 °C
Operating-Temperature Range . . . . −55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) . . . . −0.5 to +15 V
Device Dissipation (Per Package) . . . . 200 mW
All Inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$
Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) . . . . . 3 to 15 V
Recommended
Input-Voltage Swing . . . . V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32"
(1.59 ± 0.79 mm) from case
for 10 s max. . . . . +265 °C

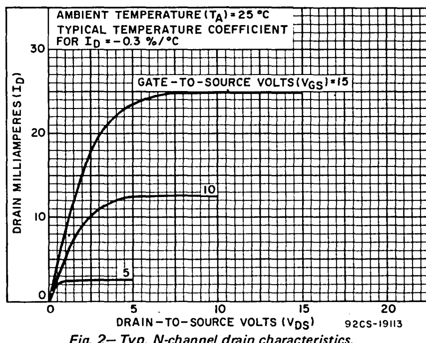


Fig. 2— Typ. N-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = 0V, C_L = 15pF, and all input rise and fall times = 20ns Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4030AD, CD4030AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	100	200	ns	1
			10	–	40	100.		
Transition Time: High-to-Low Level	t_{THL}		5	–	70	150	ns	1
			10	–	25	75.		
Low-to-High Level	t_{TLH}		5	–	80	150	ns	
			10	–	30	75.		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
NOTE 1: Test is a one input one output only.

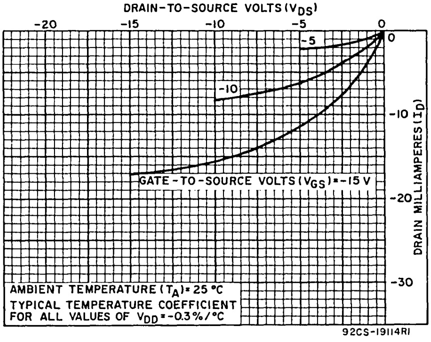


Fig. 3– Typ. P-channel drain chacteristics.

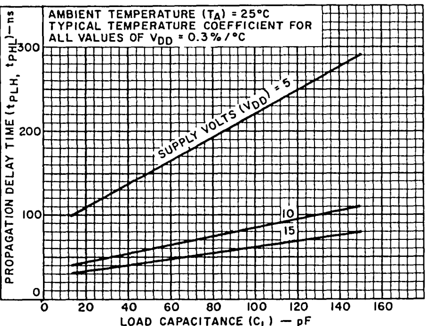


Fig. 4–Typ. propagation delay time vs. C_L.

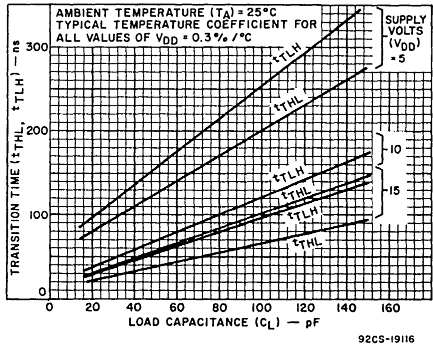


Fig. 5– Typ. transition time vs. C_L.

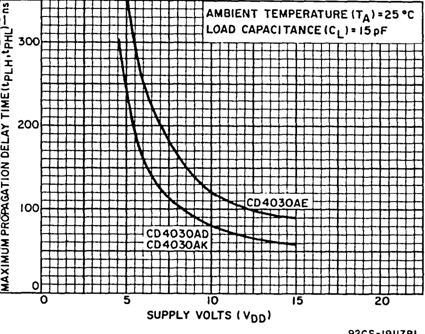


Fig. 6–Max. propagation delay time vs. V_{DD}.

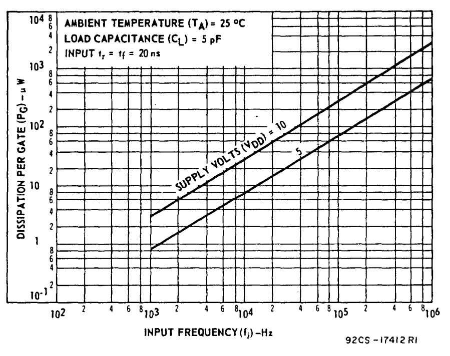


Fig. 7– Dissipation vs. input frequency.

Fig. 8–Quiescent device current test circuit.

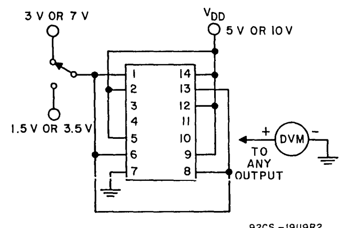


Fig. 9– Noise-immunity test circuit.

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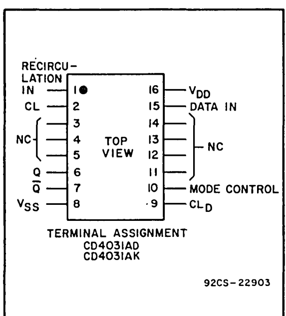
Monolithic Silicon

High-Reliability Slash(/) Series

CD4031A/...



High-Reliability COS/MOS 64-stage Static Shift Register

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Applications:

For use in digital equipment where low-power dissipation, low package count, and/or high noise immunity are primary design requirements.

- **Serial shift registers**
- **Time delay circuits**

RCA CD4031A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4031A is a 64-stage static shift register in which each stage is a D-type, master-slave flip-flop.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 2 Megahertz can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the "low" or "high" state. the CD4031A has a mode control input that, when in the "high" state, allows operation in the recirculating mode. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements.

Data (Q) and $\overline{\text{Data}}$ ($\overline{Q}$) outputs are provided from the 64th register stage. The Data (Q) output is capable of driving one TTL or DTL load. These devices are electrically and mechanically identical with standard COS/MOS CD4031A types described in data bulletin 569 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA High-Reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

Features:

- **Fully static operation: DC to 4 MHz @ $V_{DD}-V_{SS}$ = 10V**
- **Operation from a single 3 to 15 V positive or negative power supply**
- **High noise immunity**
- **Microwatt quiescent power dissipation: 10 μW (typ.)**
- **Full military operating temperature range: −55°C to +125°C**
- **Single-phase clocking requirements**
- **Protection against electrostatic effects on all inputs**
- **Data compatible with TTL-DTL**
- **Recirculation capability**
- **Two cascading modes:**
  Direct clocking for high-speed operation
  Delayed clocking for reduced clock drive requirements

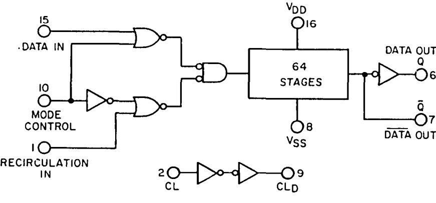


Fig. 1—Functional diagram.

RCA Designation	MIL-M-38510 Designation
CD4031A	MIL-M-38510/05705

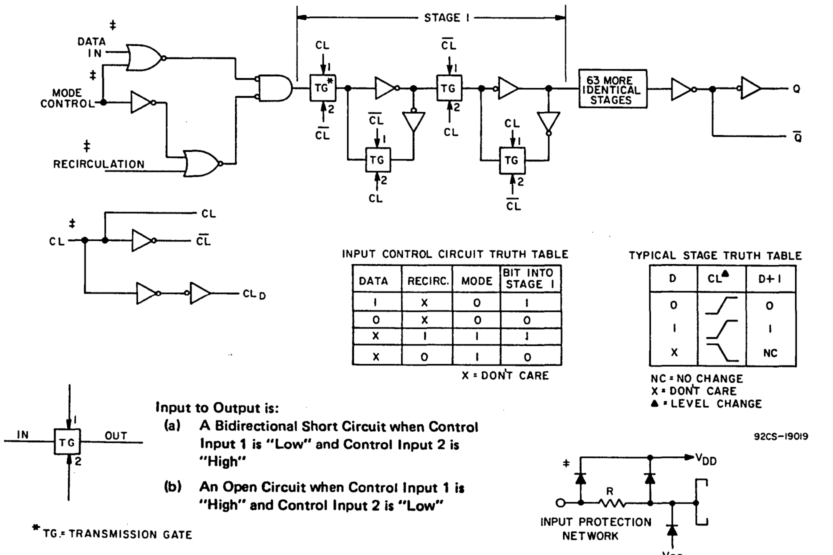
The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4031A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C



INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

X = DON'T CARE

TYPICAL STAGE TRUTH TABLE

D	CL▲	D+1
0	⟋	0
1	⟋	1
X	⟍	NC

NC = NO CHANGE
X = DON'T CARE
▲ = LEVEL CHANGE

Fig. 2—CD4031A logic diagram and truth tables.

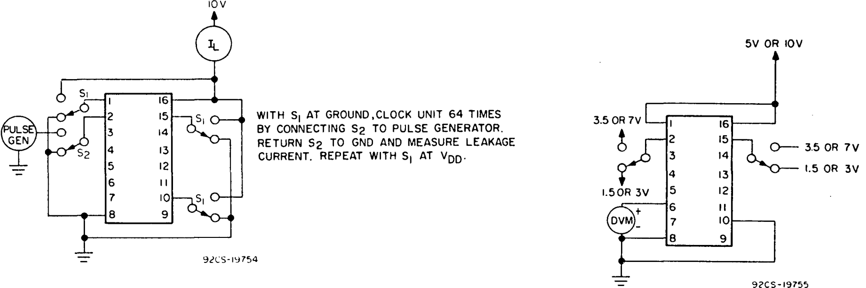


Fig. 3—Quiescent device current.

Fig. 4—Noise immunity.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4031AD, CD4031AK									UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.		
Quiescent Device Current	I_L			5	–	–	10	–	0.5	10	–	–	600	μA	1
				10	–	–	25•	–	1	25•	–	–	500•		
Quiescent Device Dissipation/Package	P_D			5	–	–	50	–	2.5	50	–	–	3000	μW	–
				10	–	–	250	–	10	250	–	–	5000		
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55•	–	–	0.5•	–	–	–	V	1
				5	–	–	0.01	–	0	0.01	–	–	0.05		
				10	–	–	0.01	–	0	0.01	–	–	0.05		
				15	–	–	–	–	–	0.5•	–	–	0.55•		
High-Level	V_{OH}			3	2.25•	–	–	2.3•	–	–	–	–	–	V	1
				5	4.99	–	–	4.99	5	–	4.95	–	–		
				10	9.99	–	–	9.99	10	–	9.95	–	–		
				15	–	–	–	14.5•	–	–	14.45•	–	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = -20 μA			-0.7•	-1.7	-3•	-0.7•	-1.5	-3•	-0.3•	-1.3	-3•	V	2
P-Channel	$V_{TH}P$	I_D = 20μA			0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•	V	
Noise Immunity (All Inputs)	V_{NL}		0.8	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	1
			1.0	10	3•	–	–	3•	4.5	–	2.9•	–	–		
For Definition, See Appendix in SSD-207	V_{NH}		4.2	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V	
			9.0	10	2.9•	–	–	3•	4.5	–	3•	–	–		
Output Drive Current: N-Channel	I_DN	Q	0.4	4.5	1.6	–	–	1.3•	2.6	–	0.91	–	–	mA	2
		Q	0.5	10	–	9.6	–	–	8	–	–	5.6	–		
		$\bar{Q}$	0.5	5	0.11	–	–	0.09•	0.18	–	0.06	–	–		
		$\bar{Q}$	0.5	10	0.24	–	–	0.2•	0.4	–	0.14	–	–		
		CL_D	0.5	5	0.48	–	–	0.4•	0.8	–	0.28	–	–		
		CL_D	0.5	10	1.5	–	–	1.2•	2.4	–	0.84	–	–		
P-Channel	I_DP	Q	4.5	5	-0.4	–	–	-0.32•	-0.64	–	-0.22	–	–	mA	2
		Q	9.5	10	-0.85•	–	–	-0.70•	-1.4	–	-0.49	–	–		
		$\bar{Q}$	4.5	5	-0.11	–	–	-0.09•	-0.18	–	-0.06	–	–		
		$\bar{Q}$	9.5	10	-0.24	–	–	-0.20•	-0.4	–	-0.14	–	–		
		CL_D	4.5	5	-0.48	–	–	-0.40•	-0.8	–	-0.28	–	–		
		CL_D	9.5	10	-1.0	–	–	-0.80•	-1.6	–	-0.56	–	–		
Diode Test 100 μA Test Pin	–				–	–	1.5•	–	–	1.5•	–	–	1.5•	V	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.

Note 2: Test is either a one input or one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = OV, C_L = 15pF (unless otherwise specified), and input rise and fall times = 20 ns, except t_rCL and t_fCL.

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4031AD, CD4031AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Clock to Data Output Q & $\bar{Q}$*	t_{PHL}		5	–	400	800	ns	1
			10	–	200	400		
Clock to CL_D	t_{PLH}	C_L = 60pF	5	–	400	800		
			10	–	200	400		
Transition Time: Q Output	t_{THL}, t_{TLH}		5	–	75	150	ns	—
			10	–	30	60		
$\bar{Q}$ Output			5	–	300	600		
			10	–	150	300		
CL_D Output		C_L = 60pF	5	–	200	400		
			10	–	100	200		
Clock Rise & Fall Time**	t_rCL, t_fCL		5	–	–	2	μs	1
			10	–	–	1		
Set-Up Time	t_{SHL}, t_{SLH}		5	–	200	400	ns	—
			10	–	50	100		
Data Overhang Time	t_{DO}		5	–	0		ns	—
			10	–	20	50		
Maximum Clock*** Frequency	f_{CL}		5	0.8	2	–	MHz	1
			10	2•	4	–		
Input Capacitance Clock	C_I			–	60	—	pF	—
All Others				–	5	—		

*Capacitive loading on $\bar{Q}$ output affects propagation delay of Q output. These limits apply for $\bar{Q}$ load C_L ≤ 15pF.

**If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15pF and the transition time of the output driving stage.

***Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature – $f_{max} = \frac{1}{(n\text{-}1)\ CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$ where n = number of packages

b) Not Using Delayed Clock – $f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

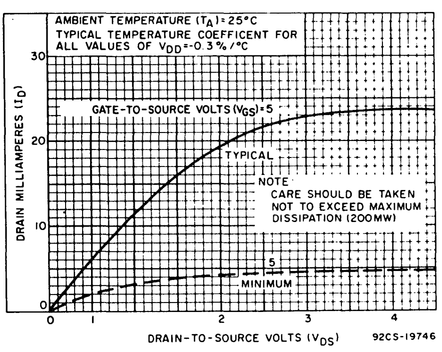


Fig. 5—Typical & minimum N-channel drain characteristics for Q output.

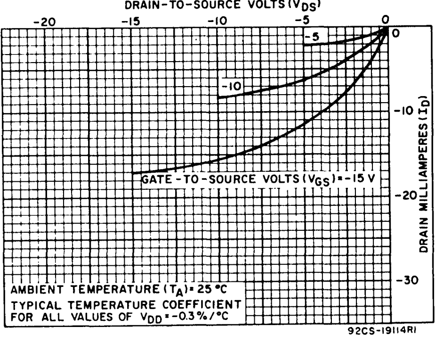


Fig. 6—Typical P-channel drain characteristics for Q output.

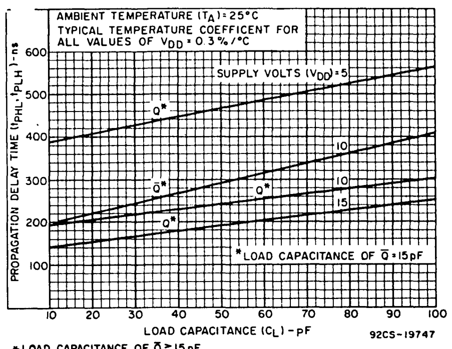


Fig. 7—Typical propagation delay time vs. C_L for data outputs.

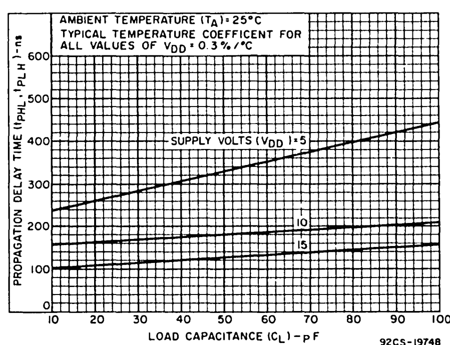


Fig. 8—Typical propagation delay vs. C_L for delayed clock output.

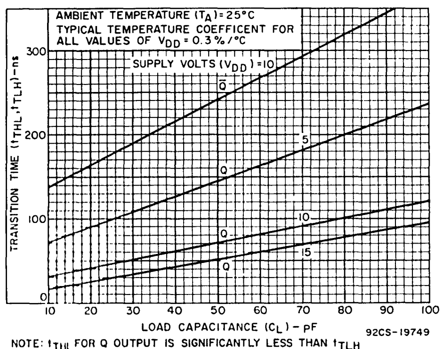


Fig. 9—Typical transition time vs. C_L for data outputs.

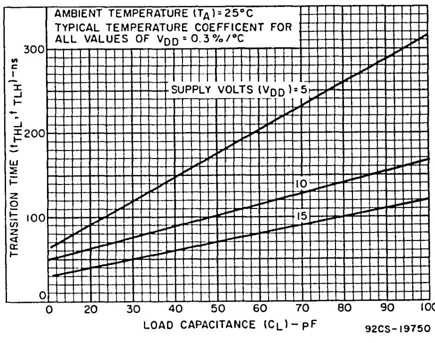


Fig. 10—Typical transition time vs. C_L for delayed clock output.

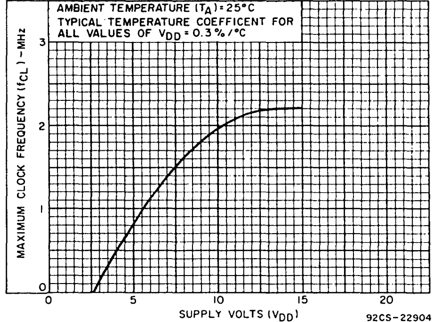


Fig. 11—Maximum clock frequency vs. V_{DD}.

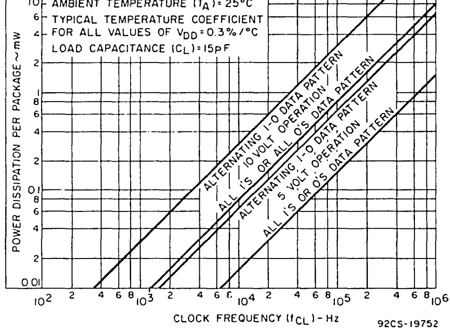


Fig. 12—Typical power dissipation vs. frequency.

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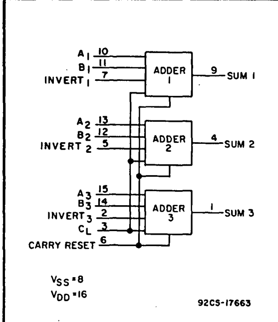
High-Reliability Slash(/) Series CD4032A/... CD4038A/...



High-Reliability COS/MOS Triple Serial Adder

Positive Logic Adder – CD4032A
Negative Logic Adder – CD4038A
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Invert inputs on all adders for sum complementing applications**
- **Fully static operation. . . . .dc to 5 MHz (typ.)**
- **Buffered outputs**
- **Single-phase clocking**
- **Microwatt quiescent power dissipation. . . . . 5 μW (typ.)**

RCA CD4032A and CD4038A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4032A and CD4038A types consist of three serial-adder circuits with common clock and carry-reset inputs. Each adder has provisions for two serial-data input signals and an invert command signal which (when a logical "1") complements the sum. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032A or at the negative-going clock for the CD4038A. For spike-free operation the input data transitions should occur as soon as possible after the triggering edge.

The carry is reset to a logical "0" at the end of each word by applying a logical "1" signal to a carry-reset input one bit-position before the application of the first bit of the next word. Figs.2 and 4 show definitive waveforms for all input and output signals.

Applications:

- **Serial arithmetic units**
- **Digital correlators**
- **Digital datalink computers**
- **Flight control computers**
- **Digital servo control systems**

These devices are electrically and mechanically identical with standard COS/MOS CD4032A and CD4038A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

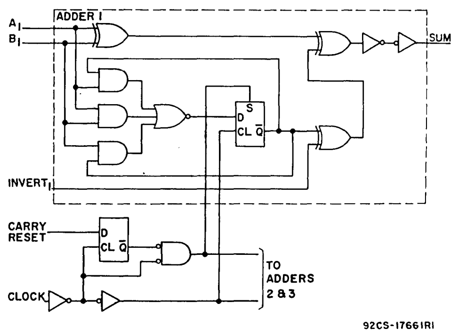


Fig.1 – CD4032A logic diagram of one of three serial adders.

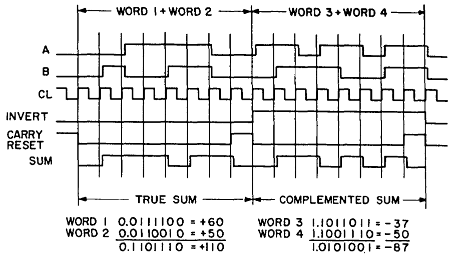


Fig.2 – CD4032A timing diagram.

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The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4032A and CD4038A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Parameter	Value	Unit
Storage-Temperature Range	−65 to +150	°C
Operating-Temperature Range	−55 to +125	°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

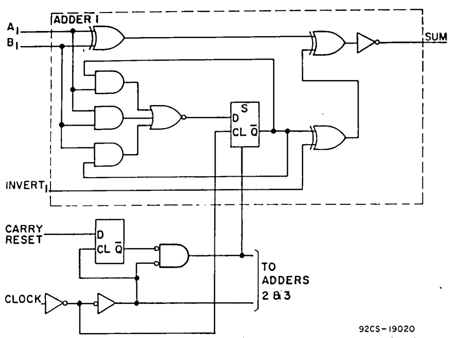

Fig.3 — CD4038A logic diagram of one of three serial adders.

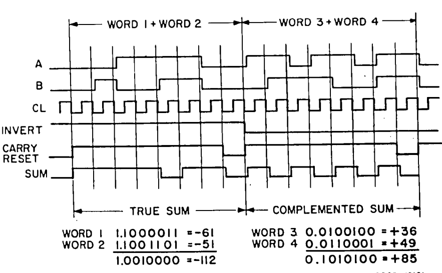

Fig.4 — CD4038A timing diagram.

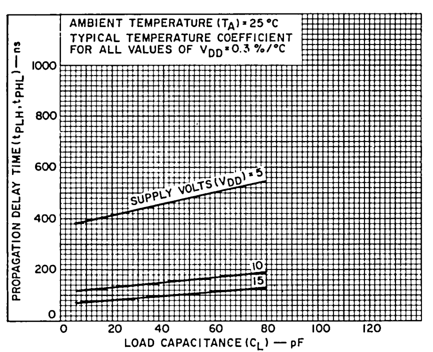

Fig.5 — Typ. propagation delay time vs. C_L for A, B, or invert inputs to sum outputs.

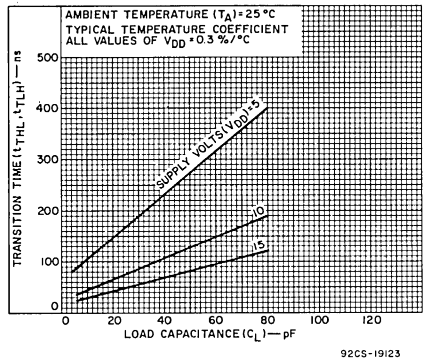

Fig.6 — Typ. transition time vs. C_L for sum outputs.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4032AD, CD4032AK CD4038AD, CD4038AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L		5	–	5	–	0.5	5	–	300	µA	1
			10	–	10●	–	1	10●	–	200●		
Quiescent Device Dissipation/Package	P_D		5	–	25	–	2.5	25	–	1500	µW	
			10	–	100	–	10	100	–	2000		
Output Voltage: Low Level	V_{OL}		3	–	0.55●	–	–	0.5●	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5●	–	0.55●		
High-Level	V_{OH}		3	2.25●	–	2.3●	–	–	–	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.5●	–	–	14.45●	–		
Threshold Voltage: N-Channel	V_{THP}	I_D = −20 µA		−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V	2
P-Channel	V_{THP}	I_D = 20 µA		0.7●	3●	0.7●	1.5	3●	0.3●	3●	V	
Noise Immunity (All Inputs) *For Definition, See Appendix in SSD-207*	V_{NL}	0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V	1
		1.0	10	3●	–	3●	4.5	–	2.9●	–		
	V_{NH}	4.2	5	1.4	–	1.5●	2.25	–	1.5	–	V	
		9.0	10	2.9●	–	3●	4.5	–	3●	–		
Output Drive Current: N-Channel	I_{DN}	0.5	5	0.6	–	0.5●	0.9	–	0.3	–	mA	2
		0.5	10	0.75	–	0.7●	2.4	–	0.6	–		
P-Channel	I_{DP}	4.5	5	−0.21	–	−0.23●	−0.4	–	−0.075	–	mA	
		9.5	10	−0.7	–	−0.55●	−1.2	–	−0.35	–		
Diode Test 100 µA test pin	V_{DF}				1.5●			1.5●		1.5●	V	3
Input Current	I_I			–	–	–	10	–	–	–	pA	

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

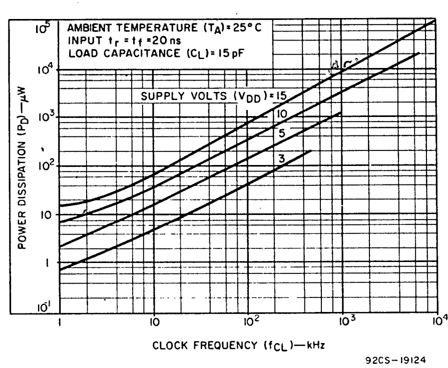

Fig.7 – Typ. dissipation characteristics.

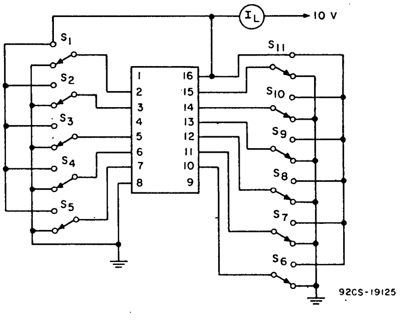

Fig.8 – Quiescent device current test circuit CD4032A.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = 0V, C_L = 15pF, and input rise and fall times = 20ns, except t_rCL and t_fCL. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4032AD, CD4032AK CD4038AD, CD4038AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time: A, B, or Invert Inputs to Sum Outputs	t_{PHL}, t_{PLH}		5	–	400	1100	ns	1
			10	–	125	250 •		
Clock Input to Sum Outputs			5	–	800	2200	ns	1
			10	–	250	500 •		
Transition Time (Sum Outputs)	t_{THL}, t_{TLH}		5	–	125	375	ns	1
			10	–	50	150 •		
Clock Rise & Fall Time	** t_rCL, t_fCL		5	–	–	15	μs	1
			10	–	–	15 •		
Input Set-Up Times *			5	t_rCL	–	–	–	
			10					
Maximum Clock Frequency	f_{CL}		5	1.5	2.5	–	MHz	1
			10	3 •	5	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	

* This characteristic refers to the minimum time required for the A, B, or Reset Inputs to change state following a positive clock transition (CD4032A) or negative transition (CD4038A).

** If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one-input, one-output only.

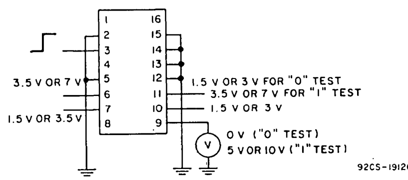

Fig.9 – Noise-immunity test circuit CD4032A.

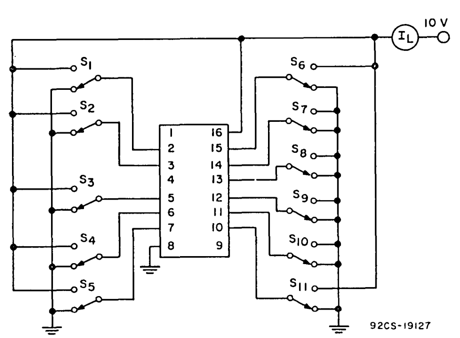

Fig.10 – Quiescent device current test circuit CD4038A.

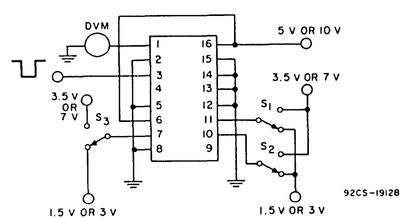

Fig.11 – Noise-immunity test circuit CD4038A.

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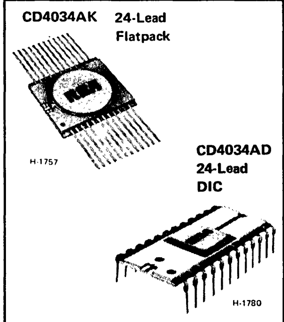
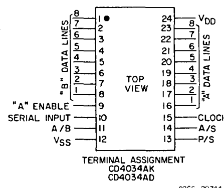


High-Reliability COS/MOS MSI 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Bidirectional parallel data input**
- **Parallel or serial inputs/parallel outputs**
- **Asynchronous or synchronous parallel data loading**
- **Parallel data-input enable on "A" data lines**
- **Data recirculation for register storage**
- **Multipackage register expansion**
- **Fully static operation DC-to-5 MHz (typ.) at $V_{DD}-V_{SS}$ = 10 V**



Applications:

- **Parallel Input/Parallel Output, Parallel Input/Serial Output, Serial Input/Parallel Output, Serial Input/Serial Output Register**
- **Shift right/shift left register**
- **Shift right/shift left with parallel loading**
- **Address register**
- **Buffer register**
- **Bus system register with enable parallel lines at bus side**
- **Double bus register system**
- **Up-Down Johnson or ring counter**
- **Pseudo-random code generators**
- **Sample and hold register (storage, counting, display)**
- **Frequency and phase comparator**

RCA CD4034A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4034A is a static eight-stage parallel- or serial-input parallel-output register. It can be used to: 1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single phase clock (CL), "A"-data enable (AE), Asynchronous/synchronous (A/S), "A" bus to "B" bus/"B" bus to "A" bus (A/B), and parallel/serial (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight "A" data lines are inputs (outputs) and the "B" data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for serial data is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A "high" P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is "low". If the A/S input is "high" this transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is "high" the A data lines are inputs (and B data lines are outputs); a "low" A/B signal reverses the direction of data flow.

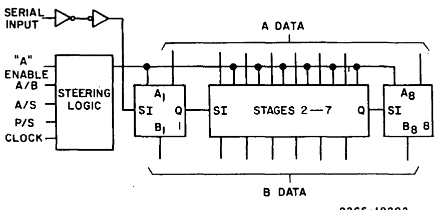


Fig. 1—Functional diagram.

These devices are electrically and mechanically identical with standard COS/MOS CD4034A types described in data bulletin 575 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4034A "Slash" (/) Series types are supplied in 24-lead dual-in-line ceramic packages ("D" suffix), in 24-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4034AD, CD4034AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L			5	–	5	–	0.3	5	–	300	μA	1
				10	–	10•	–	0.5	10•	–	200•		
Quiescent Device Dissipation/Package	P_D			5	–	25	–	2.5	25	–	1500	μW	–
				10	–	100	–	10	100	–	2000		
Output Voltage Low-Level	V_{OL}			3	–	0.55•	–	–	0.5•	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}			3	2.25•	–	2.3•	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -10\ \mu A$			0.7•	-3•	-0.7•	-1.5	-3•	-0.3•	-3•	V	2
P-Channel	$V_{TH}P$	$I_D = 10\ \mu A$			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}		0.8	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
			1.0	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}		4.2	5	1.4	–	1.5•	2.25	–	1.5	–	V	
			9.0	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN		0.5	5	0.124	–	0.1•	0.2	–	0.07	–	mA	2
			0.5	10	0.31		0.25•	0.5	–	0.175	–		
P-Channel	I_DP		4.5	5	−0.075	–	−0.05•	0.1	–	−0.035	–	mA	2
			9.5	10	−0.188		−0.125•	−0.25	–	−0.088	–		
Diode Test, 100 μA Test Pin	V_{DF}				–	1.5•		–	1.5•	–	1.5•	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.

Note 2: Test is either a one input or one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		CD4034AD,CD4034AK			UNITS	NOTES
			V_{DD} Volts	Min.	Typ.	Max.		
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	600	1200	ns	1
			10	–	240	480●		
Transition Time	t_{THL}, t_{TLH}		5	–	250	750	ns	–
			10	–	100	300		
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	400	ns	–
			10	–	100	175		
Minimum High-Level AE, P/S, A/S Pulse Width	t_{WH}		5	–	240	480	ns	–
			10	–	85	195		
Clock Rise and Fall Time	$^*t_rCL$, t_fCL		5	–	–	15	μs	1
			10	–	–	15●		
Set-Up Time	–		5	–	250	500	ns	–
			10	–	100	200		
Maximum Clock Frequency	f_{CL}		5	1.5	2.5	–	MHz	1
			10	3.0●	5	–		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

* If more than one unit is cascaded, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF (see chart above) and the transition time of the output driving stage for the estimated capacitvie load.

Note 1: Test is a one input one output only.

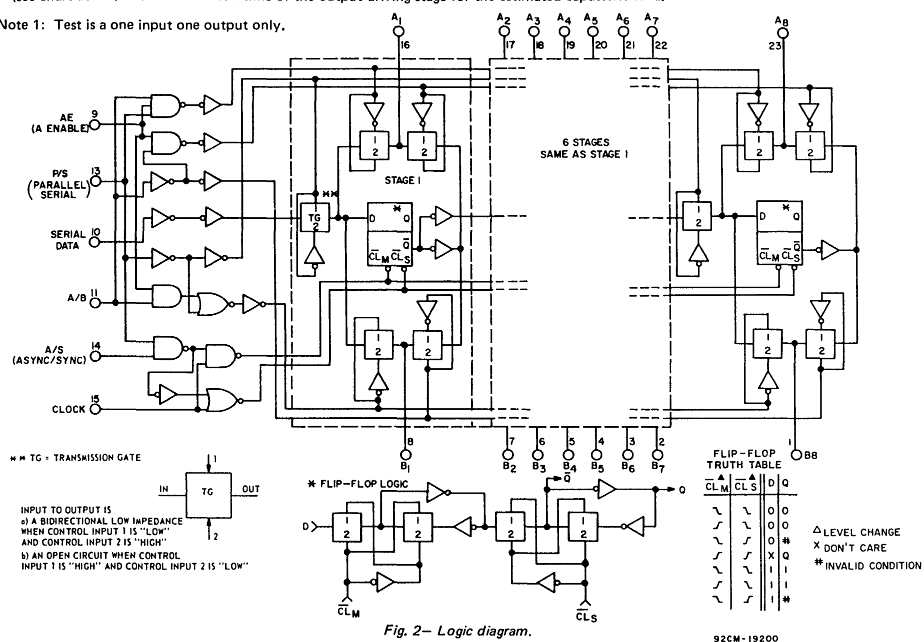


Fig. 2– Logic diagram.

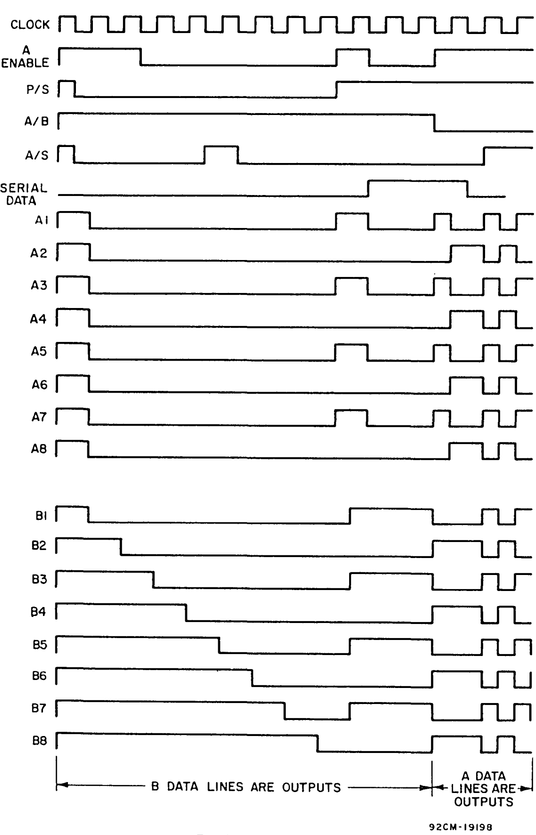


Fig. 3—Timing diagram.

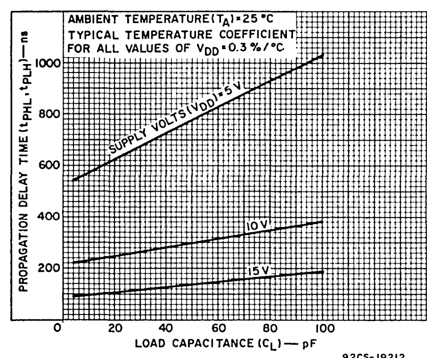


Fig. 4—Typical propagation delay time vs. C_L.

AMBIENT TEMPERATURE (T_A) = 25 °C
TYPICAL TEMPERATURE COEFFICIENT FOR ALL VALUES OF V_{DD} = 0.3 %/°C
SUPPLY VOLTS (V_{DD}) = 5 V
10 V
15 V
TRANSITION TIME (T_{THL}, T_{TLH}) — ns
0 200 400 600 800 1000
20 40 60 80 100
LOAD CAPACITANCE (C_L) — pF
92CS-19213

Fig. 5—Typical transition time vs. C_L.

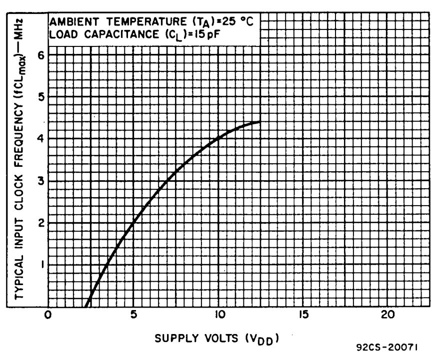


Fig. 6— Typical input frequency vs. V_{DD}.

AMBIENT TEMPERATURE (T_A)=25°C
ALTERNATING "0" AND "1" PATTERN
SUPPLY VOLTS (V_{DD})=15 V, 10 V, 5 V, 5 V, 3.5 V
POWER DISSIPATION/PACKAGE (P_D) — μW
INPUT CLOCK FREQUENCY (f_{CL}) — kHz
——— LOAD CAPACITANCE (C_L)=15 pF
– – – – C_L = 50 pF
92CS-17806R3

Fig. 7— Typical dissipation characteristics.

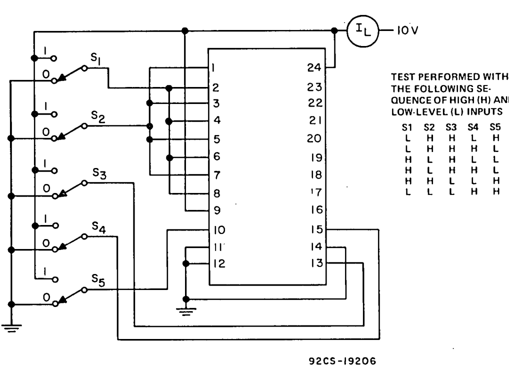


Fig. 8— Quiescent device current test circuit.

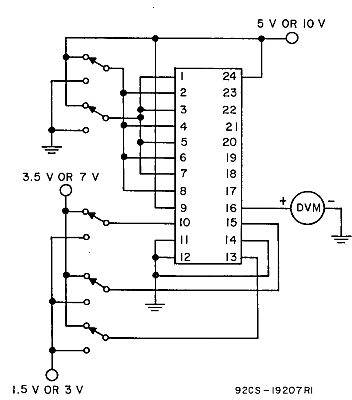
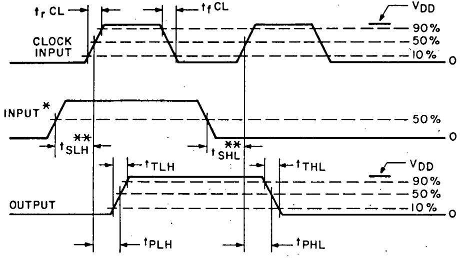


Fig. 9— Noise immunity test circuit.



* INPUT REFERS TO ANY OF THE "A" OR "B" DATA INPUTS, "A" ENABLE, SERIAL INPUT, A/B, P/S, OR A/S INPUTS

** t_{SLH} AND t_{SHL} ARE SET-UP TIMES

92CS-20078

Fig. 10— Synchronous operation propagation delay times, transition times, and set-up times.

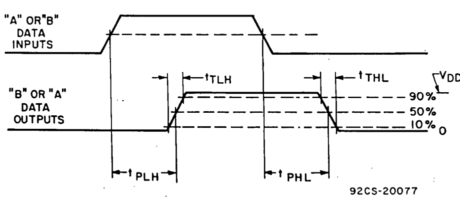


Fig. 11—Asynchronous operation propagation delay time.

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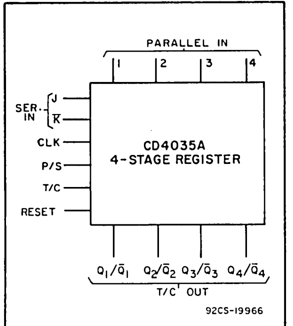
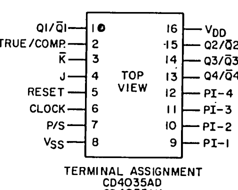
High-Reliability Slash(/) Series CD4035A/...



High-Reliability COS/MOS 4-Stage Parallel In/Parallel Out Shift Register



with J-K Serial Inputs and True/ Complement Outputs

For Logic Systems Applications on Aerospace, Military, and Critical Industrial Equipment

RCA CD4035A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4035A is a four-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via JK logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is "high". In the parallel or serial mode information is transferred on positive clock transitions.

When the True/Complement control is "high", the True contents of the register are available at the output terminals. When the True/Complement control is "low", the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the clock signal.

$J\bar{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With JK inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

These devices are electrically and mechanically identical with standard COS/MOS CD4035A types described in data bulletin 568 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

Applications:

- **Sequence generation, control circuits, code conversion**
- **Counters, Registers, Arithmetic-Unit Registers, Shift Left – Shift Right Registers, Serial-to-Parallel/Parallel-to-Serial conversions.**

Features:

- **4-Stage clocked shift operation**
- **Synchronous parallel entry on all 4 stages**
- **$J\bar{K}$ inputs on first stage**
- **Asynchronous True/Complement control on all outputs**
- **Reset control**
- **Static flip-flop operation; Master-slave configuration**
- **Buffered outputs**
- **Low-Power Dissipation - 5 μW typ. (ceramic)**
- **High speed – to 5 MHz**

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4035A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range . . . . −65 to +150 °C
Operating-Temperature Range . . . . −55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) . . . . −0.5 to +15 V
Device Dissipation (Per Package) . . . . 200 mW
All Inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$

Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) . . . . . 3 to 15 V
Recommended
Input-Voltage Swing . . . . V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16″ ± 1/32″
(1.59 ± 0.79 mm) from case
for 10 s max. +265 °C

STATIC ELECTRICAL CHARACTERISTICS ***(All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V***

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4035AD, CD4035AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L		5	–	5	–	0.3	5	–	300	µA	1
			10	–	10•	–	0.5	10•	–	200•		
Quiescent Device Dissipation/Package	P_D		5	–	25	–	1.5	25	–	1500	µW	–
			10	–	100	–	5	100	–	2000		
Output Voltage Low-Level	V_{OL}		3	–	0.55•	–	–	0.5•	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	–	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = −20 µA		−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	I_D = 20 µA		0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}	0.8	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
		1	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix	V_{NH}	4.2	5	1.4	–	1.5•	2.25	–	1.5	–	V	
		9	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	$I_D N$	0.5	5	0.62	–	0.5•	1	–	0.35	–	mA	2
		0.5	10	1.55	–	1.25•	2.5	–	0.87	–		
P-Channel	$I_D P$	4.5	5	−0.31	–	−0.25•	−0.5	–	−0.17	–	mA	2
		9.5	10	−0.81	–	−0.65•	−1.3	–	−0.45	–		
Diode Test, 100 µA Test Pin	V_{DF}			–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I			–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

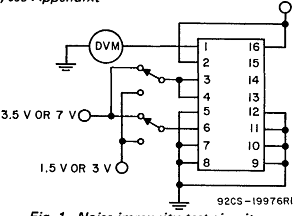
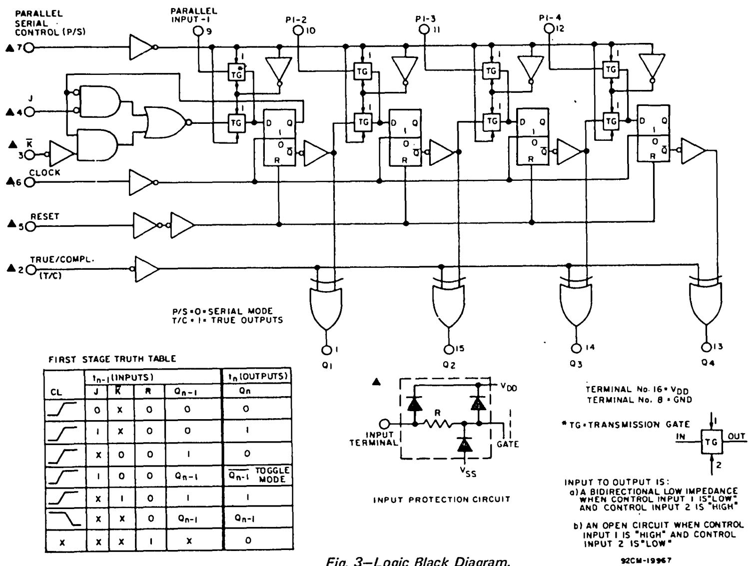


Fig. 1—Noise immunity test circuit.

I_L — 5 V OR 10 V

92CS-19975

Fig. 2—Quiescent device current test circuit.



FIRST STAGE TRUTH TABLE

CL	t_{n-1} (INPUTS) J	$\bar{K}$	R	Q_{n-1}	t_n (OUTPUTS) Q_n
↑	0	X	0	0	0
↑	1	X	0	0	1
↑	X	0	0	1	0
↑	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
↑	X	1	0	1	1
↓	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Fig. 3—Logic Black Diagram.

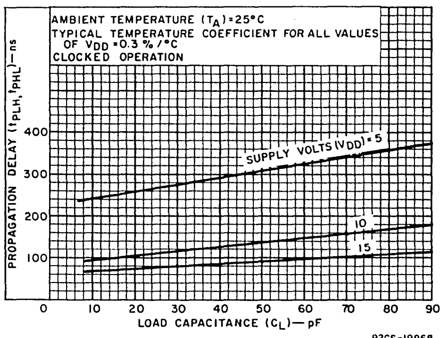


Fig. 4— Typical Propagation Delay Time vs. Load Capacitance.

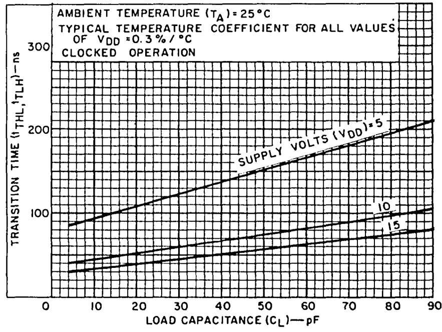


Fig. 5— Typical Transition Time vs. Load Capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C and C_L = 15 pF*

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4035AD, CD4035AK Min.	Typ.	Max.	UNITS	NOTES
CLOCKED OPERATION							
Propagation Delay Time:	t_{PLH}, t_{PHL}	5	–	250	500	ns	1
		10	–	100	200●		
Transition Time:	t_{THL}, t_{TLH}	5	–	100	200	ns	1
		10	–	50	100●		
Minimum Clock Pulse Duration	t_{WL}, t_{WH}	5	–	200	335	ns	–
		10	–	100	165		
Clock Rise & Fall Time	t_{fCL}*, t_{fCL}	5		–	15	μs	1
		10		–	5		
Setup Time: $\overline{J}$/K Lines		5	–	250	500	ns	–
		10	–	100	200		
Parallel-In Lines		5	–	100	350		
		10	–	50	80		
Maximum Clock Frequency	f_{CL}	5	1.5	2.5	–	MHz	1
		10	3 ●	5	–		
Input Capacitance	C_I	Any Input	–	5	–	pF	–
RESET OPERATION							
Propagation Delay Time:	t_{PHL}, t_{PLH}	5	–	250	500	ns	–
		10	–	100	200		
Minimum Reset Pulse Duration	t_{WL}, t_{WH}	5	–	200	400	ns	–
		10	–	100	175		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is either a one input or a one output only.

*If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

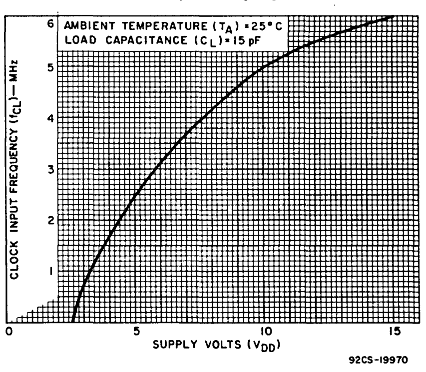


Fig. 6—Typical clock input frequency vs. V_{DD}

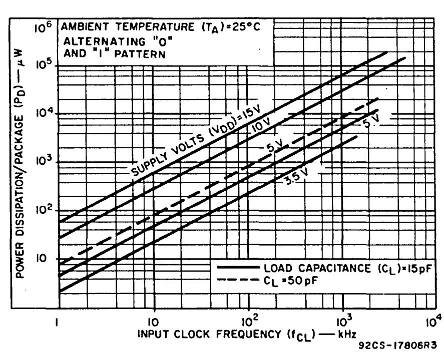


Fig. 7— Typical dissipation characteristics.

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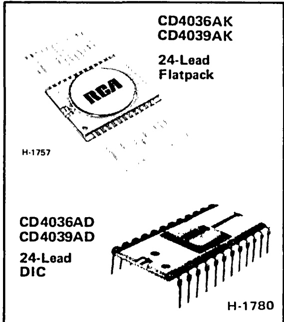


High-Reliability COS/MOS 4-Word by 8-Bit Random-Access NDRO Memory

For Logic Systems Applications on Aerospace, Military, and Critical Industrial Equipment

Binary Addressing — CD4036AD, CD4036AK
Direct Word-Line Addressing — CD4039AD, CD4039AK

Special Features:

- **COS/MOS logic compatibility at all input and output terminals**
- **Memory bit expansion**
- **Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines**
- **Memory bypass capability for all bits**
- **Buffering on all outputs**
- **CD4036A- on-chip binary address decoding, separate READ INHIBIT and WRITE controls**
- **CD4039A-Direct word-line addressing**
- **Access Time—200 ns(Typ) at V_{DD}=10 V**

Applications

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements.

- **Channel Preset Memory in digital frequency-synthesizer circuits**
- **General-purpose and scratch-pad memory in COS/MOS and other low-power systems.**

RCA CD4036A and CD4039A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4036A is a single monolithic integrated circuit containing a 4-word x 8-bit Random Access NDRO Memory. Inputs include 8 INPUT-BIT lines, CHIP INHIBIT, WRITE, READ INHIBIT, MEMORY BYPASS, and 2 ADDRESS inputs. 8 OUTPUT-BIT lines are provided.

All input and output lines utilize standard COS/MOS inverter configurations and hence can be directly interfaced with COS/MOS logic devices.

CHIP INHIBIT allows memory word expansion by WIRE-ORing of multiple CD4036A packages at either the 8-bit input and/or output lines (See Fig. 1). With CHIP INHIBIT "high", both READ and WRITE operations are inhibited on the CD4036A. With CHIP INHIBIT "low", information can be written into and/or read continuously from one of the

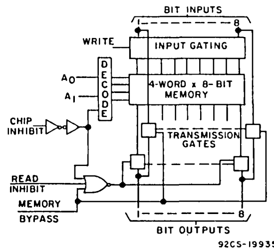


Fig. 1 – CD4036A – Logic block diagram.

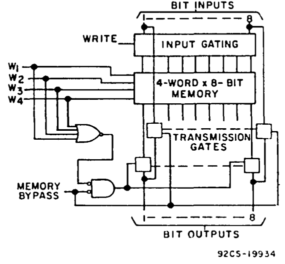


Fig. 2–CD4039A -- Logic block diagram.

four words selected by the binary code on the two address lines. With CHIP INHIBIT "low", a "high" WRITE signal and a "low" READ INHIBIT signal activate WRITE and READ operations, respectively, at the addressed word location (See Fig. 9).

The MEMORY BYPASS signal, when "high", allows shunting of information from the 8 INPUT-BIT lines directly to the 8 OUTPUT-BIT lines without disturbing the state of the 4 words. During the bypass operation input information may also be written into a selected word location, provided the CHIP INHIBIT is "low" and the WRITE is "high". The READ operation is deactivated during the BYPASS operation because information is fed directly from the 8 INPUT-BIT lines to the 8 OUTPUT-BIT lines.

RCA type CD4039A is identical to the CD4036A with the exception that individual address-line inputs have been provided for each memory word in place of the binary ADDRESS, CHIP INHIBIT, and READ INHIBIT inputs. When Wire-Oring multiple CD4039A packages for memory word expansion, an individual CD4039A is selected by addressing one of its word locations. The READ operation is activated whenever a word location is addressed (via a "high" signal—see Fig. 10).

These devices are electrically and mechanically identical with standard COS/MOS CD4036A and CD4039A types described in data bulletin 613 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4036A and CD4039A "Slash" (/) Series types are supplied in 24-lead dual-in-line ceramic packages ("D" suffix), in 24-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Parameter	Value	Unit
Storage-Temperature Range	−65 to +150	°C
Operating-Temperature Range	−55 to +125	°C
DC Supply-Voltage Range: ($V_{DD}-V_{SS}$)	−0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} < V_I < V_{DD}$	
Recommended DC Supply-Voltage ($V_{DD}-V_{SS}$)	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

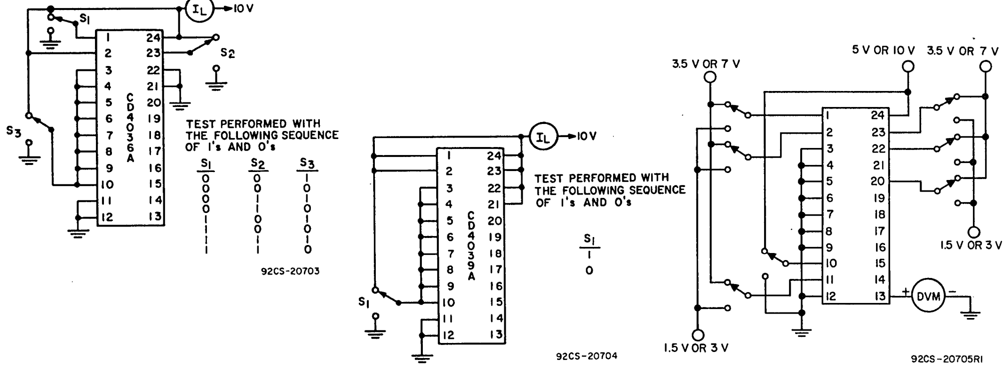


Fig. 3— Quiescent current (CD4036A).

Fig. 4— Quiescent current (CD4039A).

Fig. 5— Noise immunity.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4036AD, CD4036AK CD4039AD, CD4039AK							NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	
Quiescent Device Current	I_L			5	–	5	–	0.5	5	–	300	1
				10	–	10●	–	1	10●	–	200●	
Quiescent Device Dissipation/Package	P_D			5	–	25	–	2.5	25	–	1500	–
				10	–	100	–	10	100	–	2000	
Output Voltage: Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	1
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	–	0.5●	–	0.5●	
High-Level	V_{OH}			3	1.45●	–	1.5●	–	–	–	–	1
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	–	–	14.45●	–	
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = −20 μA			−0.7●	−3●	−0.7●	−1.5●	−3●	−0.3●	−3●	2
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	2
Noise Immunity (All inputs except bit inputs when in memory by-pass mode.)	V_{NL}		0.8	5	1.5	–	1.5●	2.25	–	1.4	–	1
			1	10	3●	–	3●	4.5	–	2.9●	–	
	V_{NH}		4.2	5	1.4	–	1.5●	2.25	–	1.5	–	
			9	10	2.9●	–	3●	4.5	–	3●	–	
Output Drive Current: N-Channel	$I_D N$	Normal Read Modes	0.5	5	0.12	–	0.10●	0.2	–	0.07	–	2
			0.5	10	0.3	–	0.25●	0.5	–	0.17	–	
P-Channel	$I_D P$		4.5	5	−0.12	–	−0.10●	−0.2	–	−0.07	–	2
			9.5	10	−0.3	–	−0.25●	−0.5	–	−0.17	–	
Output Drive Current N-Channel	$I_D N$	Memory By-pass Mode +	0.5	5	0.04	–	0.03●	0.06	–	0.02	–	2
			0.5	10	0.09	–	0.075●	0.15	–	0.05	–	
P-Channel	$I_D P$		4.5	5	−0.04	–	−0.03●	−0.06	–	−0.02	–	2
			9.5	10	−0.09	–	−0.075●	−0.15	–	−0.05	–	
Diode Test	V_{DF}	100 μA Test Pin			–	1.5●	–	–	1.5●	–	1.5●	3
Input Current	I_I		–	–	–	–	–	10	–	–	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or a one output only.

+Bit inputs driven from low-impedance driver.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

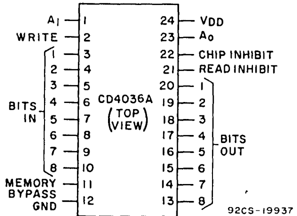
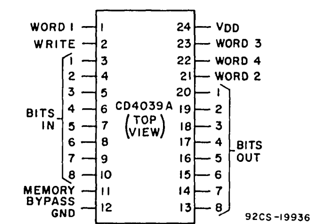


Fig. 6a)–CD4036AD and CD4036AK terminal assignments.



b)–CD4039AD and CD4039AK terminal assignments.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C and C_L = 15 pF*
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	V_{DD} Volts	CD4036AD, CD4036AK CD4039AD, CD4039AK Min.	Typ.	Max.	UNITS	NOTES
Read Delay Time: (Access time) Read Inhibit (RI)	t_{rd}	OUTPUT TIED THROUGH 100 kΩ TO V_{SS} FOR DATA OUTPUT "HIGH" AND TO V_{DD} FOR DATA OUTPUT "LOW"	5	–	375	750	ns	4
			10	–	150	300●		
Chip Inhibit (CI)			5	–	500	1000	ns	4, 7
			10	–	200	400●		
Memory Bypass (MB)			5	–	375	750	ns	7
			10	–	150	300●		
Address (ADD)			5	–	500	1000	ns	1, 7
			10	–	200	400●		
Write Set-up Time	t_{WS}		5	250	125	–	µs	2, 7
			10	100●	50	–		
Write Removal Time	t_{WR}		5	0	0	–	ns	3, 7
			10	30●	0	–		
Write Pulse Duration	t_W		5	150	75	–	ns	7
			10	60●	30	–		
Data Set-up Time	t_{DS}		5	–	0	0*	ns	5
			10	–	0	0*		
Data Overlap Time	t_{DO}		5	100▲	50	–	ns	6
			10	40▲	20	–		
Output Transition Time	t_{THL}, t_{TLH}		5	–	200	400	ns	–
			10	–	100	200		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

1. For CD4036A only, remove 100-kΩ test condition and write all 1's in word one, and all 0's in word two, or vice-versa.
2. Delay from change of ADDRESS or CHIP-INHIBIT signals to application of WRITE pulse.
3. Delay from removal of WRITE pulse to change of ADDRESS or CHIP-INHIBIT signals.
4. Values for CD4036AD & 4036AK only.
5. The time that DATA signal must be present before the WRITE pulse removal.
6. The time that DATA signal must remain present after the WRITE pulse removal.
7. Test is a one input one output only.

▲ Min. indicates satisfactory operation if t_{DO} equals or exceeds this value.

* Max. indicates satisfactory operation if t_{DS} equals or exceeds this value.

● For footnote, see Page 563.

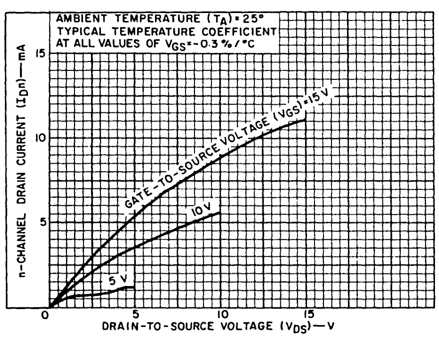


Fig. 7—Typical n-channel drain characteristics.

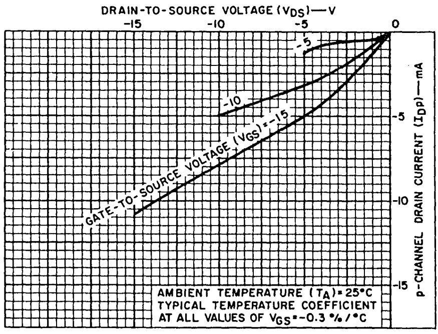


Fig. 8—Typical p-channel drain characteristics.

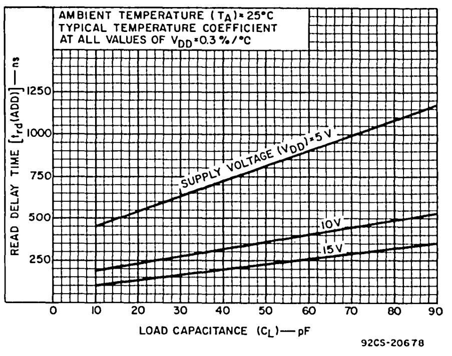


Fig. 9—Typical read delay time vs C_L.

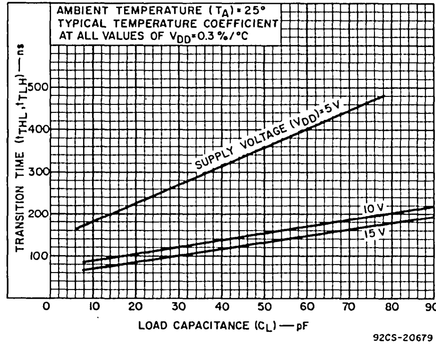


Fig. 10—Typical transition time vs. C_L.

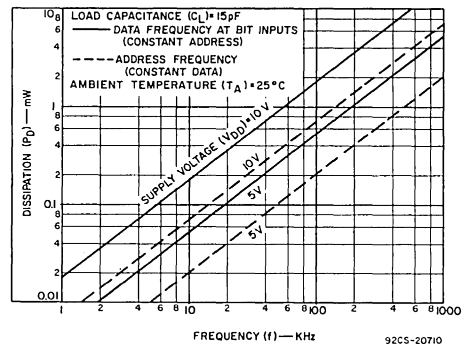


Fig. 11— Typical power dissipation vs. frequency.

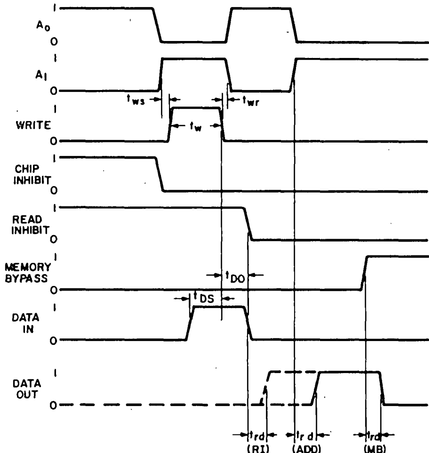


Fig. 12—CD4036A Timing Diagram.

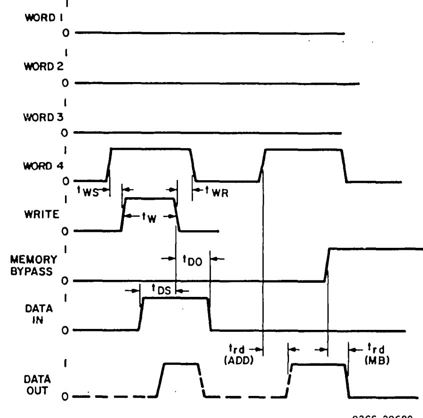


Fig. 13—CD4039A Timing Diagram.

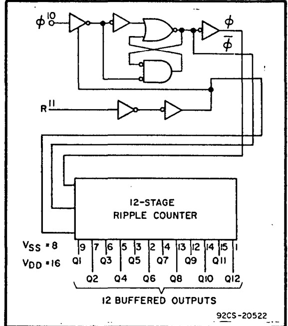
Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4040A/...



High-Reliability COS/MOS 12-Stage Ripple-Carry Binary Counter/Divider

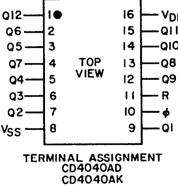
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Medium-speed operation . . . . 5-MHz (typ.) input pulse rate at $V_{DD}-V_{SS}$ = 10V**
- **Low "high"- and "low"-level output impedance . . . . . . 750 Ω (typ.) at $V_{DD}-V_{SS}$ = 10 V and V_{DS} = 0.5 V**
- **Common reset**
- **Fully static operation**
- **All 12 buffered outputs available**
- **Low-power TTL compatible**

Applications:

- **Frequency-dividing circuits**
- **Time-delay circuits**
- **Control counters**



TERMINAL ASSIGNMENT CD4040AD CD4040AK

92CS-22901

RCA CD4040A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

These devices are electrically and mechanically identical with standard COS/MOS CD4040A types described in data bulletin 624 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the CD4040A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic packages ("K" suffix), or in chip form ("H" suffix).

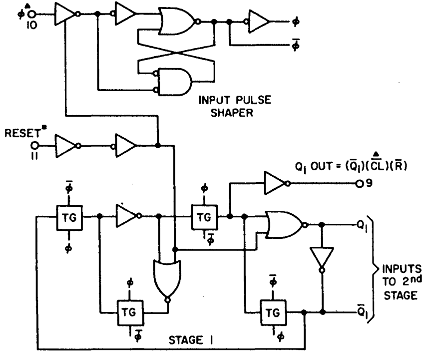


Fig. 1—Logic diagram of CD4040A input pulse shaper and 1 of 12 stages.

INPUT PULSE SHAPER

RESET BUFFERS

ON COUNTER STAGE

NOTE: SUBSTRATES FOR ALL "p" UNITS ARE CONNECTED TO V_{DD}
SUBSTRATES FOR ALL "n" UNITS, UNLESS OTHERWISES SHOWN, ARE CONNECTED TO GROUND

92CM-21509

Fig. 2—Schematic diagram of input shaping, reset buffers, and one counter stage of CD4040A.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150	°C
Operating-Temperature Range	−55 to +125	°C
DC Supply-Voltage Range:		
(V_{DD} − V_{SS})	−0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} < V_I < V_{DD}$	
Recommended DC Supply-Voltage (V_{DD} − V_{SS})	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

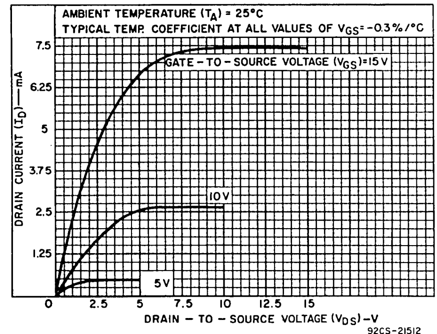


Fig. 3—Minimum n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4040AD, CD4040AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device Current	I_L			5	–	15	–	0.5	15	–	900	µA	1
				10	–	25•	–	1	25•	–	500•		
Quiescent Device Dissipation/Package	P_D			5	–	75	–	2.5	75	–	4500	µW	–
				10	–	250	–	10	250	–	5000		
Output Voltage Low-Level	V_{OL}	Fanout of 50 COS/MOS Inputs		3	–	0.55•	–	–	0.5•	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}			3	2.25•	–	2.3•	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10	9.99	–	9.99	10	–	9.95	–		
				15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$			−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$			0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}		0.8	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
			1	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}		4.2	5	1.4	–	1.5•	2.25	–	1.5	–	V	
			9	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN		0.5	5	0.22	–	0.145•	0.36	–	0.125	–	mA	2
			0.5	10	0.44	–	0.4•	0.75	–	0.25	–		
P-Channel	I_DP		4.5	5	−0.15	–	0.1•	−0.25	–	−0.085	–	mA	2
			9.5	10	−0.3	–	−0.25•	−0.5	–	−0.175	–		
Diode Test, 100 µA Test Pin	V_{DF}				–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I				–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS, *At T_A = 25°C, V_{SS} = 0V, C_L = 15 pF (unless otherwise specified), and input rise and fall times = 20 ns, except t_rCL and t_fCL. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4040AK, AD			UNITS	NOTE
			V_{DD}	Min.	Typ.	Max.		
Input-Pulse Operation								
Propagation Delay Time	t_{PHL}, t_{PLH}		5 10	– –	300 150	400 200●	ns	1, 4
Transition Time	t_{THL}, t_{TLH}		5 10	– –	150 75	300 150●	ns	4
Min. Input-Pulse Width	t_{WL}, t_{WH}	f = 100KHz	5 10	– –	200 75	400 110	ns	–
Input-Pulse Rise & Fall Time	$t_{r\phi}$, $t_{f\phi}$		5 10	– –	– –	15 7.5●	μs	2, 4
Max. Input-Pulse Frequency	f_ϕ		5 10	1.5 5●	1.75 6	– –	MHz	4
Input Capacitance	C_I	Any input		–	5	–	pF	
Reset Operation								
Propagation Delay Time	t_{PHL}		5 10	– –	500 250	1000 500	ns	3
Minimum Reset Pulse Width	t_{WH}		5 10	– –	500 250	1000 500	ns	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTES:

1. Measured from the 50% level of the negative clock edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.
2. Maximum input rise or fall time for functional operation.
3. Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).
4. Test is a one input one output only.

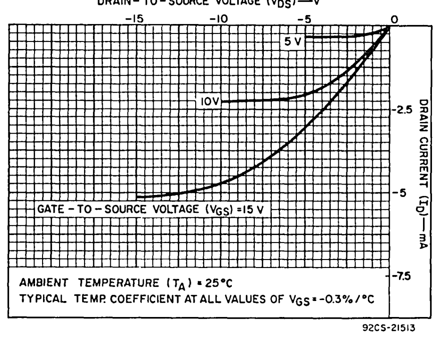


Fig. 4—Minimum p-channel drain characteristics.

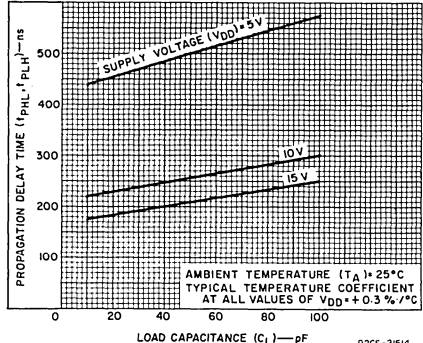


Fig. 5—Typical propagation delay time vs. load capacitance (per stage).

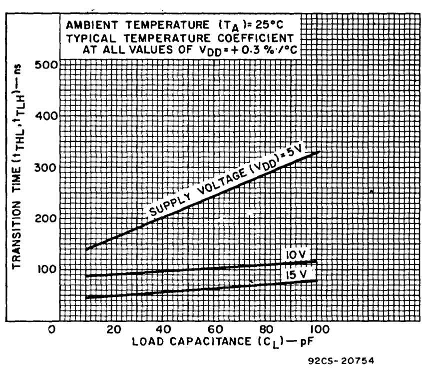


Fig. 6— Typical transition time vs. load capacitance.

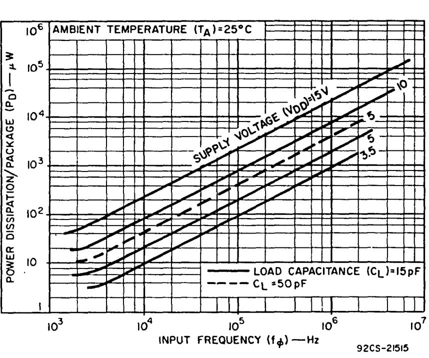


Fig. 7— Typical dissipation characteristics.

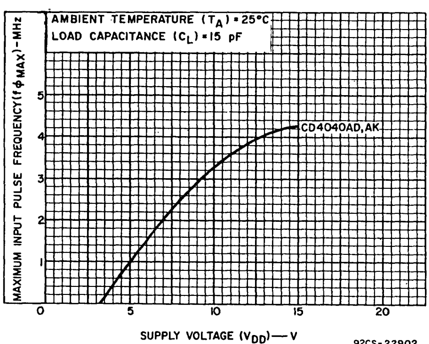


Fig. 8— Maximum input-pulse frequency vs. supply voltage.

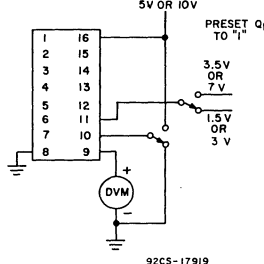


Fig. 9— Reset-noise-immunity test circuit.

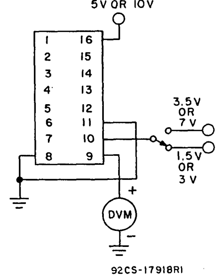


Fig. 10— Input-pulse noise-immunity test circuit.

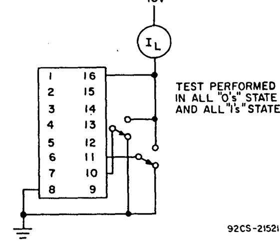


Fig. 11— Quiescent-device-current test circuit.

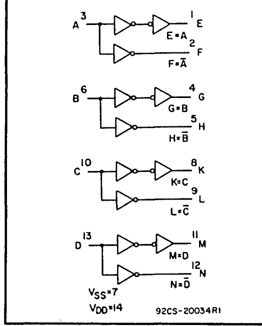
Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4041A/...



High-Reliability COS/MOS Quad True/Complement Buffer

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

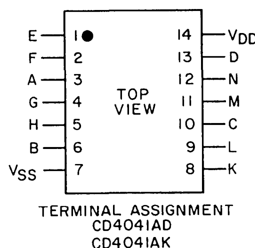
Features:

True Output

- **High current source and sink capability**
  8 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  3.2 mA (typ.) @ V_{DS} = 0.4 V, V_{DD} = 5 V (two TTL loads)

Complement Output

- **Medium current source and sink capability**
  3.6 mA (typ) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  1.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 5 V



TERMINAL ASSIGNMENT
CD4041AD
CD4041AK
92CS-20755

RCA CD4041A "Slash" (/) Series types are high-reliability COS/MOS integrated circuit Quad True/Complement Buffers designed for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4041A consists of n-and p-channel units having low channel resistance and high current (source and sink) capability. It is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can also be used as an ultra-low power resistor-network driver, and in other applications where high noise immunity and low power dissipation are primary design requirements.

These devices are electrically and mechanically identical with standard COS/MOS CD4041A types described in data bulletin 572 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4041A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in the 14-lead ceramic flat package ("K" suffix), or in chip form ("H" suffix).

Applications:

- **High current source/sink driver**
- **COS/MOS-to-DTL/TTL converter**
- **Display driver**
- **MOS clock driver**
- **Resistor network driver (Ladder or weighted R)**
- **Buffer**
- **Transmission line driver**

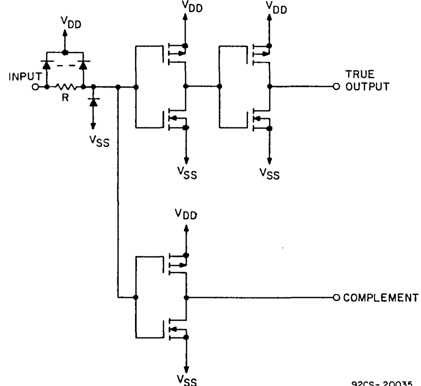


Fig.1 — CD4041A schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range	−65°C to +150	°C
Operating Temperature Range	−55°C to +125	°C
DC Supply Voltage Range ($V_{DD} - V_{SS}$)	−0.5 V to +15	V
Device Dissipation (Per Pkg.)	200	mW
Average Dissipation Per Output	100	mW
Allowable Input Rise and Fall Time vs Supply and Frequency	See Fig. 17	
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS CD4041AD, CD4041AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	Notes
Quiescent Device Current	I_L	Inputs to Ground or V_{DD}		5	–	1	–	0.005	1	–	60	μA	1
				10	–	2•	–	0.005	2•	–	40•		
Quiescent Device Dissipation/Package	P_D			5	–	5	–	0.025	5	–	300	μW	
				10	–	20	–	0.05	20	–	400		
Output Voltage: Low-Level	V_{OL}	Fan-out of 50 COS/MOS Inputs		3		0.55•			0.50•			V	1
				5	–	0.01	–	0	0.01		0.05		
				10	–	0.01	–	0	0.01	–	0.05		
				15					0.50•		0.55•		1
High-Level	V_{OH}			3	2.25•		2.3•					V	1
				5	4.99	–	4.99	5	–	4.95	–		
				10	9.99	–	9.99	10	–	9.95	–		
				15			14.40•			14.45•			1
Threshold Voltage: N-Channel	V_{THN}	I_D = −10 μA			−0.7•	−3.0•	−0.7•	−1.5	−3.0•	−0.3•	−3.0•	V	2
P-Channel	V_{THP}	I_D = 10 μA			0.7•	3.0•	0.7•	1.5	3.0•	0.3•	3.0•	V	
Noise Immunity▲ (All Inputs)	V_{NL}	True Output	0.95	5	1.5	–	1.5•	2.25	–	1.4	–	V	
			2.9	10	3•	–	3•	4.5	–	2.9•	–		
	V_{NH}		3.6	5	1.4	–	1.5•	2.25	–	1.5	–	V	
			7.2	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_{DN}	True Output	0.4	5	2.1	–	1.6•	3.2	–	1.2	–	mA	2
			0.5	10	6.25•	–	5•	10	–	3.5•	–		
		Complement Output	0.5	5	1	–	0.8•	1.6	–	0.55	–		
			0.5	10	2.5•	–	2•	4	–	1.4	–		
P-Channel	I_{DP}	True Output	4.5	5	−1.75	–	−1.4•	−2.8	–	−1	–	mA	
			9.5	10	−5•	–	−4•	−8	–	−2.8•	–		
		Complement Output	4.5	5	−0.75	–	−0.6•	−1.2	–	−0.4	–		
			9.5	10	−2.25•	–	−1.8•	−3.6	–	−1.25•	–		
Diode Test		10 μA at any input or output				1.5•			1.5•		1.5•	V	3
Input Current	I_I	Any Input			–	–	–	10	–	–	–	pA	

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.
▲ Values shown are for True Output.

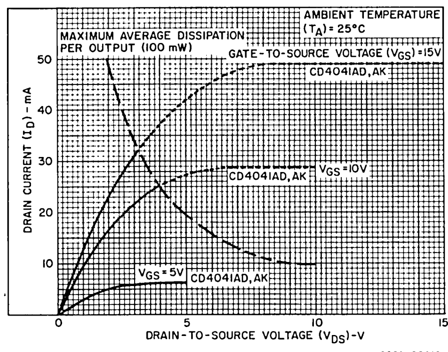


Fig. 2— Minimum n-channel drain characteristics-true output.

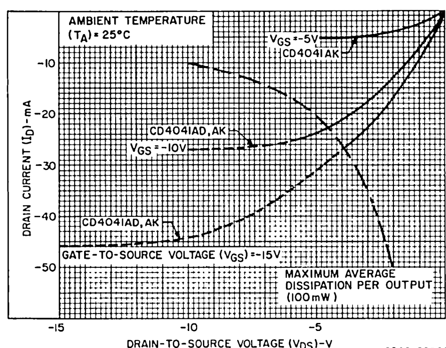


Fig. 3— Minimum p-channel drain characteristics-true output.

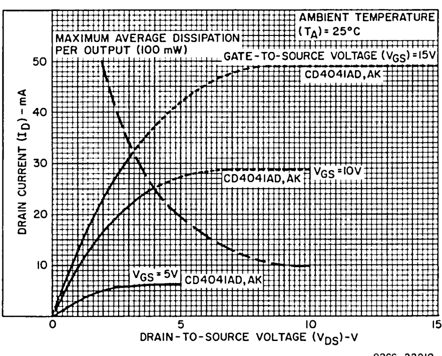


Fig. 4—Minimum n-channel drain characteristics-complement output.

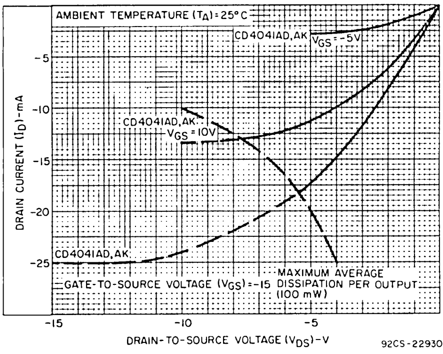


Fig. 5— Minimum p-channel drain characteristics-complement output.

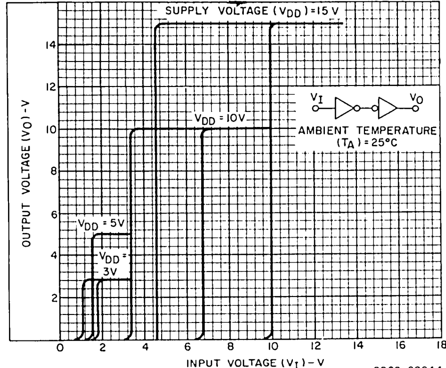


Fig. 6— Minimum and maximum transfer characteristics-true output.

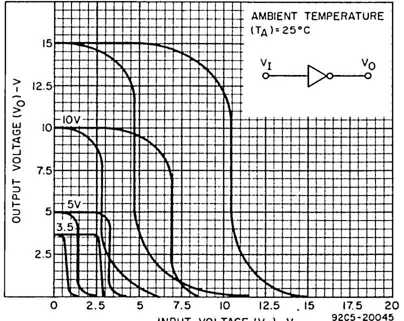


Fig. 7— Minimum and maximum transfer characteristics-complement output.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C and C_L = 15pF
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4041AD, CD4041AK MIN.	TYP.	MAX.	UNITS
Propagation Delay Time: High-to-Low Level	t_{PHL}	True Output	5	–	65	115	ns
			10	–	40	75 •	
		Complement Output	5		55	100	ns
			10		30	45 •	
Low-to-High Level	t_{PLH}	True Output	5	–	75	125	ns
			10	–	45	75 •	
		Complement Output	5	–	45	100	ns
			10	–	25	40 •	
Transition Time: High-to-Low Level	t_{THL}	True Output	5	–	20	40	ns
			10	–	13	25 •	
		Complement Output	5	–	40	60	ns
			10	–	25	40 •	
Low-to-High Level	t_{TLH}	True Output	5	–	20	40	ns
			10	–	13	25 •	
		Complement Output	5	–	35	55	ns
			10	–	25	40 •	
Input Capacitance	C_I	Any Input		–	5	–	pF

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

DYNAMIC ELECTRICAL CHARACTERISTICS (Driving TTL,DTL) AT T_A = 25°C, V_{DD}–V_{SS} = 5V, C_L = 15pF (True Output)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Driving TTL,DTL	LIMITS CD4041AD CD4041AK MIN.	TYP.	MAX.	UNITS
Propagation Delay Time: High-To-Low Level	t_{PHL}	R_L = 2kΩ	Med. Power	–	75	150	ns
		R_L = 20kΩ	Low Power	–	75	150	
Low-To-High Level	t_{PLH}	R_L = 2kΩ	Med. Power	–	85	175	ns
		R_L = 20kΩ	Low Power	–	85	175	
Transition Time	t_{THL} = t_{TLH}	R_L = 2kΩ	Med. Power	–	20	50	ns
		R_L = 20kΩ	Low Power	–	20	50	

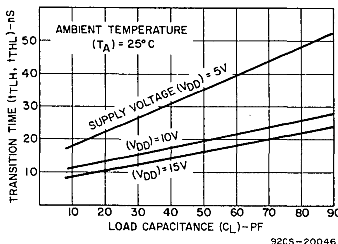


Fig. 8— Typical transition time vs. C_L-true output.

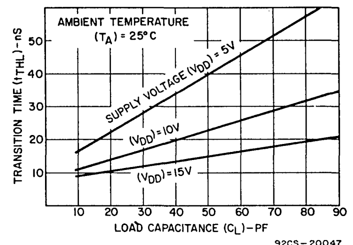


Fig. 9— Typical high-to-low level transition time vs. C_L-complement output.

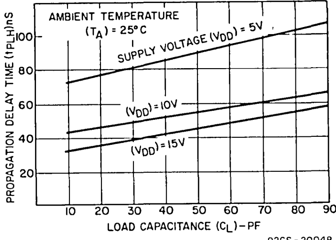


Fig. 10— Typical low-to-high level propagation delay time vs. C_L-true output.

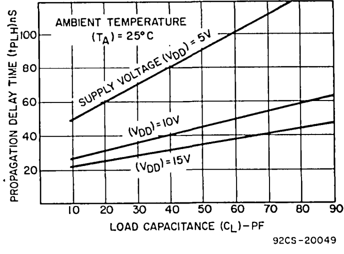


Fig. 11— Typical low-to-high level propagation delay time vs. C_L-complement output.

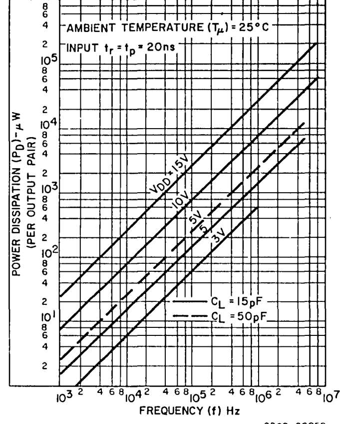


Fig. 12— Typical power dissipation vs. frequency per output pair

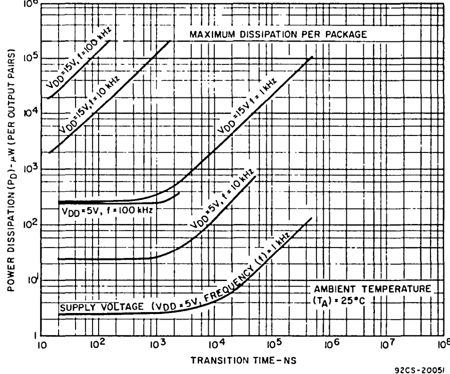


Fig. 13— Typical power dissipation vs. input rise & fall time per output pair.

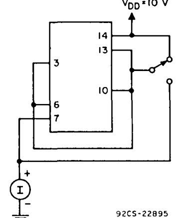


Fig. 14— Quiescent device current test circuit.

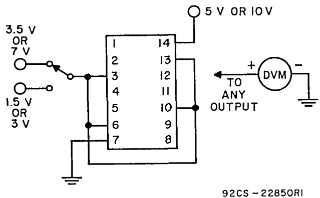


Fig. 15— Noise immunity test circuit.

Solid State
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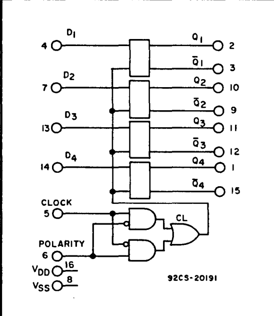
Monolithic Silicon

High-Reliability Slash(/) Series
CD4042A/...



High-Reliability COS/MOS Quad Clocked "D" Latch

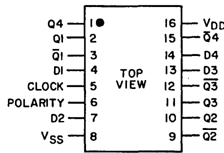
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Medium Speed Operation . . . $t_{PHL} = t_{PLH}$ = 50 ns (typ) at V_{DD} = 10 V and C_L = 15 pF**
- **Clock Polarity Control**
- **Q and Q̄ Outputs**
- **Common Clock**
- **Low Power TTL Compatible**

Applications:

- **Buffer Storage**
- **Holding Register**
- **General Digital Logic**



TERMINAL ASSIGNMENT
CD4042AD
CD4042AK

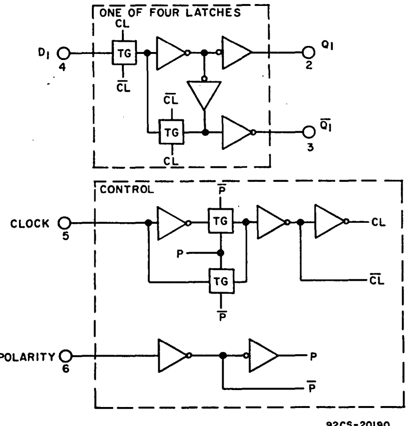
92CS-20756

RCA CD4042A "Slash" (/) Series are high-reliability COS/MOS integrated circuit Quad Clocked "D" Latches intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4042A types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and Q̄ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

These devices are electrically and mechanically identical with standard COS/MOS CD4042A types described in data bulletin 589 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types



CLOCK	POLARITY	Q
0	0	D
⌐ (positive transition)	0	LATCH
1	1	D
⌐ (negative transition)	1	LATCH

Fig.1 — Logic block diagram and truth table.

can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4042A "Slash" (/) Series types are supplied in 16-lead welded-seal dual-in-line ceramic packages ("D" suffix), in the 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4042AD, CD4042AK −55°C		25°C			125°C		UNITS	Notes
			V_O Volts	V_{DD} Volts	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Quiescent Device Current	I_L	Inputs to Ground or V_{DD}		5	–	1	–	0.005	1	–	60	µA	1
				10	–	2•	–	0.005	2•	–	40•		
Quiescent Device Dissipation/Package	P_D			5	–	5	–	0.025	5	–	300	µW	–
				10	–	20	–	0.05	20	–	400		
Output Voltage: Low-Level	V_{OL}	Fan-out of 50 COS/MOS Inputs		3		0.55•			0.50•			V	1
				5	–	0.01	–	0	0.01		0.05		–
				10	–	0.01	–	0	0.01	–	0.05		–
				15					0.50•		0.55•		1
High-Level	V_{OH}			3	2.25•		2.3•						1
				5	4.99	–	4.99	5	–	4.95	–		–
				10	9.99	–	9.99	10	–	9.95	–		–
				15			14.5•			14.45•			1
Threshold Voltage: N-Channel	V_{THN}	I_D = −10 µA			−0.7•	−3.0•	−0.7•	−1.5	−3.0•	−0.3•	−3.0•	V	2
P-Channel	V_{THP}	I_D = 10 µA			0.7•	3.0•	0.7•	1.5	3.0•	0.3•	3.0•	V	
Noise Immunity (All Inputs)	V_{NL}		0.95	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
			2.9	10	3•	–	3•	4.5	–	2.9•	–		
	V_{NH}		3.6	5	1.4	–	1.5•	2.25	–	1.5	–	V	
			7.2	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN		0.5	5	0.5	–	0.4•	1	–	0.27	–	mA	2
			0.5	10	1.25	–	1•	2	–	0.7	–	mA	
P-Channel	I_DP		4.5	5	−0.45	–	−0.35•	−1	–	−0.25	–		2
			9.5	10	−1.15	–	−0.9•	−2	–	−0.6	–		
Diode Test	V_{DF}	10 µA at any input or output			–	1.5•	–	–	1.5•	–	1.5•	–	3
Input Current	I_I	Any Input			–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or a one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = 0V, C_L = 15pF, and input rise and fall times = 20 ns, except t_rCL and t_fCL.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS			UNITS	NOTES
				CD4042AD, CD4042AK				
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	150	300	ns	1
			10	–	75	125 ●		
Transition Time	t_{THL}, t_{TLH}		5	–	100	200	ns	1
			10	–	50	100 ●		
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	175	250	ns	–
			10	–	50	75		
Clock Rise & Fall Time	t_rCL, t_fCL		5		–	15	μs	1
			10		–	5 ●		
Set-Up Time			5	–	50	100	ns	–
			10	–	25	50		
Input Capacitance	C_I		–	–	5	–	pF	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input, one output only.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range .... –65 to +150 °C
Operating-Temperature Range .... –55 to +125 °C
DC Supply-Voltage Range:
(V_{DD} – V_{SS}) .... –0.5 to +15 V
Device Dissipation (Per Package) .... 200 mW
All Inputs .... $V_{SS} \leq V_I \leq V_{DD}$
Recommended
DC Supply-Voltage (V_{DD} – V_{SS}) ..... 3 to 15 V
Recommended
Input-Voltage Swing .... V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32"
(1.59 ± 0.79 mm) from case
for 10 s max. .... +265 °C

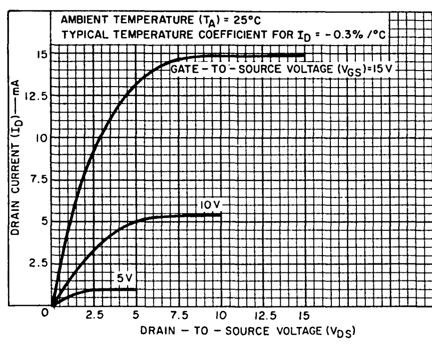


Fig. 2– Min. n-channel drain characteristics.

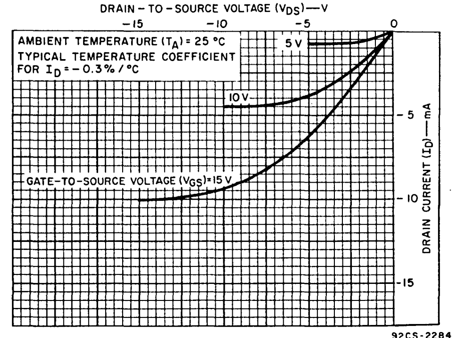


Fig. 3– Min. p-channel drain characteristics.

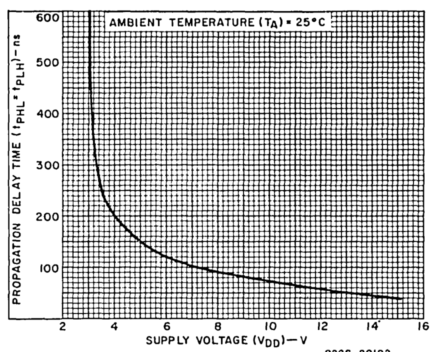


Fig. 4— Typical propagation delay time vs. V_{DD}.

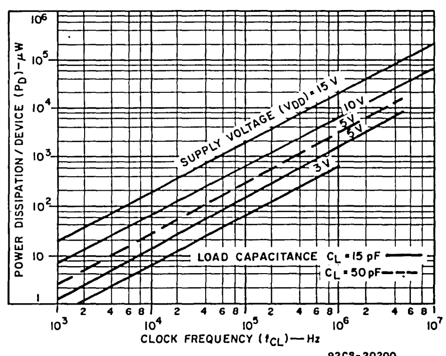


Fig. 5— Typical dissipation characteristics.

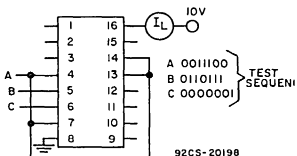


Fig. 6— Quiescent device current.

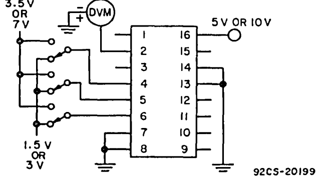


Fig. 7— Noise immunity.

Solid State Division

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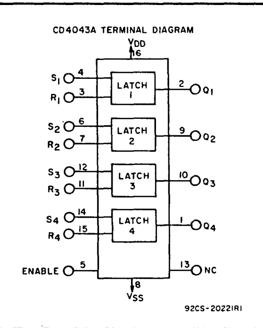
High-Reliability Slash(/) Series CD4043A/..., CD4044A/...



High-Reliability COS/MOS Quad 3-State R/S Latches

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Quad NOR R/S Latch – CD4043A

Quad NAND R/S Latch - CD4044A

Special Features:

- Medium Speed Operation
- 3-Level Outputs with Common Output Enable
- Separate Set and Reset Inputs for Each Latch
- Low Power TTL Compatible
- NOR and NAND Configurations

Applications:

- Holding Register in Multi-Register System
- Four Bits of Independent Storage with Output Enable
- Strobed Register
- General Digital Logic

RCA-CD4043A and CD4044A "Slash" (/) Series are high-reliability COS/MOS integrated circuit Quad 3-State R/S Latches intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4043A types are quad cross-coupled 3-State NOR latches; the CD4044A types, quad cross-coupled 3-State NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are gated through transmission gates controlled by a common ENABLE input. A logic "1" or "high" on the ENABLE input connects the latch states to the Q outputs. A logic "0" or "low" on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs. The logic operation of the latches is summarized in the truth table on the following page.

These devices are electrically and mechanically identical with standard COS/MOS CD4043A and CD4044A types described in data bulletin 590 and DATABOOK SSD-203B Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4043A and CD4044A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	–65 to +150	°C
Operating-Temperature Range	–55 to +125	°C
DC Supply-Voltage Range: (V_{DD} – V_{SS})	–0.5 to +15	V
Device Dissipation (Per Package)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply-Voltage (V_{DD} – V_{SS})	3 to 15	V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} Volts	LIMITS CD4043AD, CD4043AK, CD4044AD, CD4044AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	Notes
Quiescent Device Current	I_L	Inputs to Ground or V_{DD}	5	–	1	–	0.005	1	–	60	µA	1
			10	–	2•	–	0.005	2•	–	40•		
Quiescent Device Dissipation/Package	P_D		5	–	5	–	0.025	5	–	300	µW	–
			10	–	20	–	0.05	20	–	400		
Output Voltage: Low-Level	V_{OL}	Fan-out of 50 COS/MOS Inputs	3	–	0.55•	–	–	0.5•	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	–	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = −10 µA		−0.7•	−3.0•	−0.7•	−1.5	−3.0•	−0.3•	−3.0•	V	2
P-Channel	$V_{TH}P$	I_D = 10 µA		0.7•	3.0•	0.7•	1.5	3.0•	0.3•	3.0•	V	
Noise Immunity (All Inputs)	V_{NL}	V_O = 0.95 V	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
		V_O = 2.9 V	10	3•	–	3•	4.5	–	2.9•	–		
	V_{NH}	V_O = 3.6 V	5	1.4	–	1.5•	2.25	–	1.5	–	V	
		V_O = 7.2 V	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	I_DN	V_O = 0.5 V	5	0.25	–	0.2•	0.5	–	0.14	–	mA	2
			10	0.61	–	0.5•	1	–	0.35	–		
P-Channel	I_DP	V_O = 4.5 V	5	−0.22	–	−0.175•	−0.5	–	−0.12	–	mA	2
		V_O = 9.5 V	10	−0.5	–	−0.4•	−1	–	−0.28	–		
Diode Test	V_{DF}	100 µA at any input or output		–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I	Any Input		–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

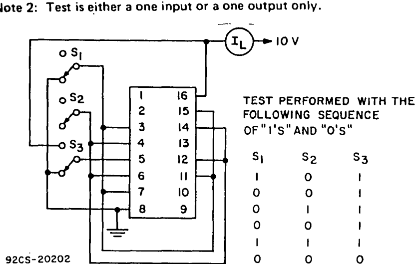


Fig. 1— Quiescent current.

VDD
5 V OR 10 V
3.5 V OR 7 V
1.5 V OR 3 V
DVM
92CS-20203RI

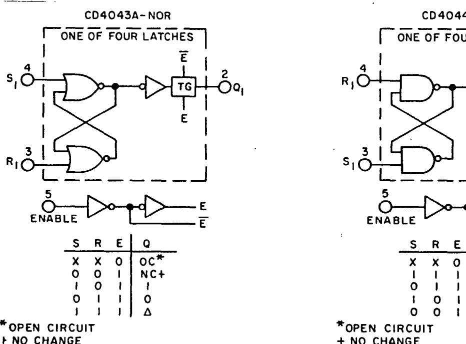
Fig. 2— Noise immunity.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = 0V, C_L = 15pF, and input rise and fall times = 20 ns, except t_rCL and t_fCL.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4043AD, CD4043AK CD4044AD, CD4044AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	175	350	ns	1
			10	–	75	175●		
Transition Time	t_{THL}, t_{TLH}		5	–	100	200	ns	1
			10	–	50	100●		
Minimum Set and Reset Pulse Width	$t_{WH(S)}$, $t_{WH(R)}$		5	–	80	200	ns	1
			10	–	40	100●		
Input Capacitance	C_I		–	–	5	–	pF	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is one input or a one output only.



CD4044A Terminal Diagram

Fig. 3—Logic diagrams & truth tables.

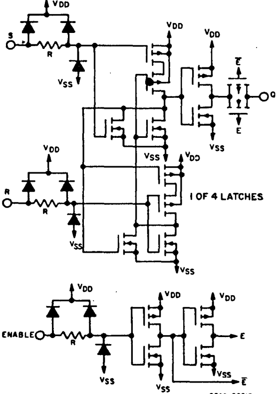


Fig. 4—Schematic diagram—CD4043A.

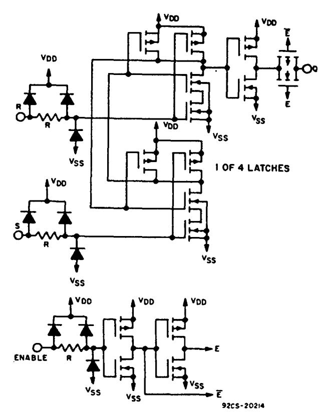


Fig. 5—Schematic diagram-CD4044A.

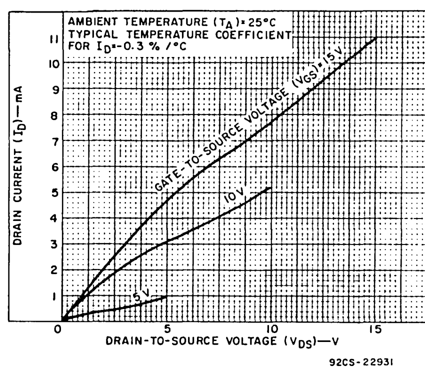


Fig.6—Min. n-channel drain characteristics.

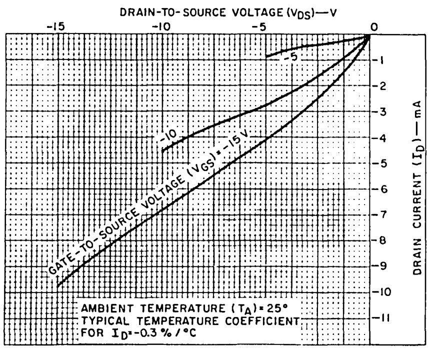


Fig.7—Min. p-channel drain characteristics.

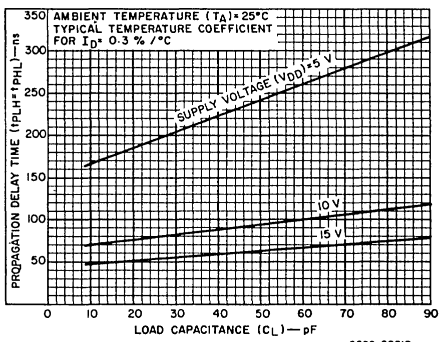


Fig.8—Typ. propagation delay time vs. C_L.

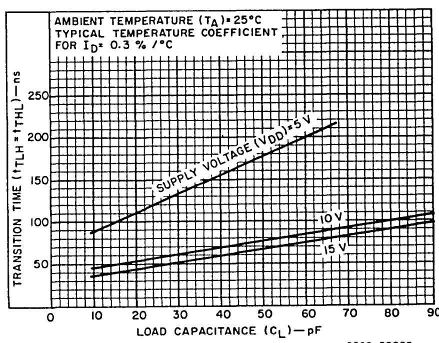


Fig.9—Typ. transistion time vs. C_L.

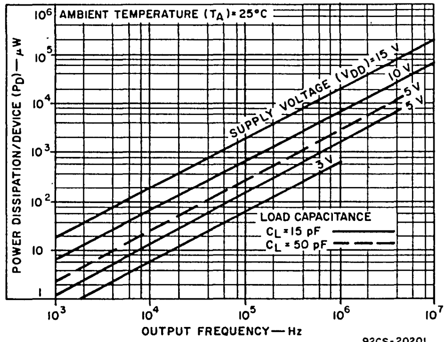


Fig.10—Typ. dissipation characteristics.

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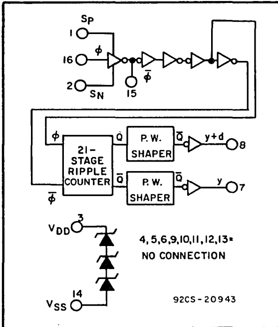
High-Reliability Slash(/) Series

CD4045A/...



High-Reliability COS/MOS 21-Stage Counter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**

RCA CD4045A "Slash" (/) Series types are high-reliability COS/MOS integrated circuit 21-Stage Counters intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4045A is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, three 5.5 V zener diodes (providing transient protection at 16.5 V), and input inverters for use in a crystal oscillator. This device may be operated over a 3-to-15 V supply voltage range. The CD4045A configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/ amplifier. However, it may be used as a normal logic inverter if desired.

A crystal oscillator circuit can be made less sensitive to voltage supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_P to V_{DD}, S_N to V_{SS}). See Fig. 1.

These devices are electrically and mechanically identical with standard COS/MOS CD4045A types described in data bulletin 614 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

Features:

- **Operation from 3 to 15 volts**
- **Microwatt quiescent dissipation . . .**
  2.5 μW (typ.) @ V_{DD} = 5 V; 10 μW (typ.) @ V_{DD} = 10 V
- **Very-low operating dissipation . . .**
  1 mW (typ.); @ V_{DD} = 5 V, fϕ = 1 MHz
- **Output drivers with sink or source capability . . .**
  7 mA (typ.) @ V_O = 0.5 V, V_{DD} = 5 V (sink)
  5 mA (typ.) @ V_O = 4.5 V, V_{DD} = 5 V (source)
- **Medium speed (typ.) . . . fϕ = 5 MHz @ V_{DD} = 5 V**
  fϕ = 10 MHz @ V_{DD} = 10 V
- **16.5 V zener diode transient protection on chip for automotive use**

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/ MOS CD4000A "Slash" (/) Series Types".

The CD4045A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

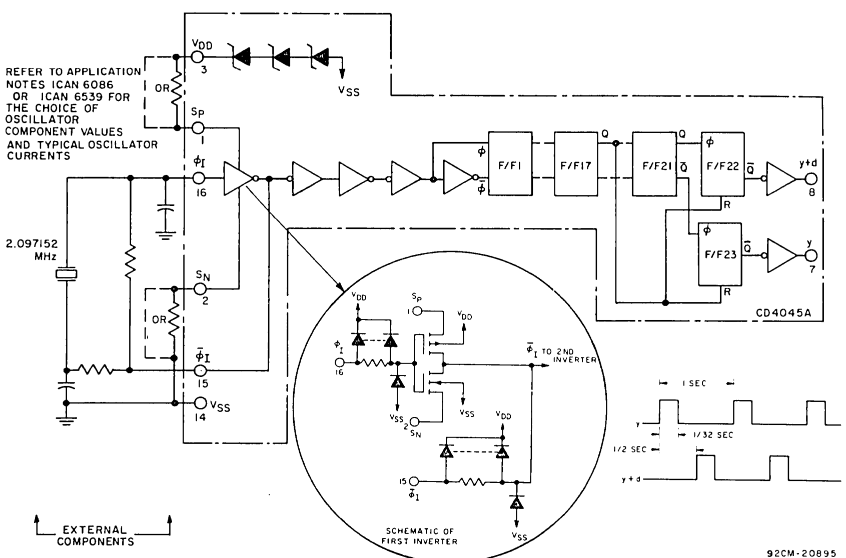


Fig. 1 – CD4045A and outboard components in a typical 21-stage counter application.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range:	
Ceramic packages	−55°C to +125°C
Plastic package	−40°C to +85°C
DC Supply-Voltage Range:	
$(V_{DD} - V_{SS})$	−0.5 to +15 V
Device Dissipation:	
(Per package, including zener diodes)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage $(V_{DD} - V_{SS})$	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Peak Zener Diode Current	
(Decay τ = 80 ms)	150 mA

Note 1: To minimize power dissipation in the zener diodes, and to ensure device dissipation less than 200 mW, a 150 Ω current-limiting resistor must be placed in series with the power supply for $V_{DD} > 13$ V.

Note 2: Observe power supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in all other CD4000A Series 16-lead devices).

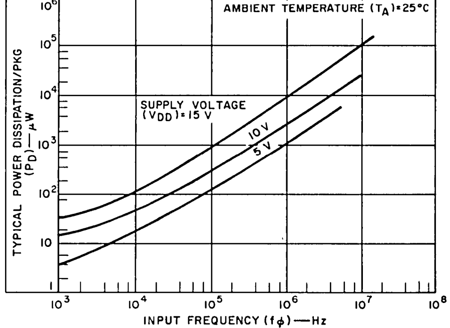


Fig. 2– Typical dissipation vs. input frequency (21 counting stages).

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \le V_I \le V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4045AD,CD4045AK							UNITS	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.		
Quiescent Device▲ Current	I_L			5	–	15	–	0.5	15	–	900	μA	1
				10	–	25•	–	1	25•	–	500•		
Quiescent Device▲ Dissipation/Package	P_D			5	–	0.075	–	0.0025	0.075	–	4.5	mW	–
				10	–	0.25	–	0.01	0.25	–	5		
Output Voltage Low-Level	V_{OL}	Driving COS/MOS		3	–	0.55•	–	–	0.5•	–	–	V	1
				5	–	0.01	–	0	0.01	–	0.05		–
				10	–	0.01	–	0	0.01	–	0.05		–
				15	–	–	–	–	0.50•	–	0.55•		1
High-Level	V_{OH}			3	2.25•	–	2.3•	–	–	–	–	V	1
				5	4.99	–	4.99	5	–	4.95	–		–
				10	9.99	–	9.99	10	–	9.95	–		–
				15	–	–	14.5•	–	–	14.45•	–		1
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -10\ \mu A$			−0.3•	−3•	−0.3•	−1.5	−2.8•	−0.3•	−2.8•	V	2
P-Channel	$V_{TH}P$	$I_D = 10\ \mu A$			0.3•	3•	0.3•	1.5	2.8•	0.3•	2.8•		
Sum	$V_{TH}S$				–	3.7	–	–	3.6	–	3.7		2
Noise Immunity (Any Input)	V_{NL}			5	1.5	–	1.5•	2.25	–	1.4	–	V	1
				10	3•	–	3•	4.5	–	2.9•	–		
	V_{NH}			5	1.4	–	1.5•	2.25	–	1.5	–		
				10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current N-Channel	I_DN		0.5	5	4.4	–	3.5•	7	–	2.5	–	mA	2
			0.5	10	6.9	–	5.5•	11	–	3.9	–		
P-Channel	I_DP		4.5	5	−3.1	–	−2.5•	−5	–	−1.8	–	mA	
			9.5	10	−5.6	–	−4.5•	−9	–	−3.2	–		
Input Current	I_I				–	–	–	10	–	–	–	pA	3
Diode Test	V_{DF}	100 μA at each input or output			–	1.5•	–	–	1.5•	–	1.5•	V	–
Zener Breakdown Voltage	$V_{(BR)Z}$	I = 100 μA			13.3	17.8	13.5	16.5	18	13.7	18.2	V	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A/Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

▲Maximum noise-free saturated Bipolar output voltage.

†Minimum noise-free saturated Bipolar output voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns, except $t_r\phi$ and $t_f\phi$. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4045AD,CD4045AK Min.	Typ.	Max.	UNITS	NOTES
Propagation Delay Time ϕ_1 to y or y+d out	t_{PHL},	5	–	2.2	4.4	µs	–
	t_{PLH}	10	–	1.2	2.4		
Transition Time	t_{THL},	5	–	450	800	ns	–
	t_{TLH}	10	–	375	650		
Minimum Input-Pulse Width	t_{WL},	5	–	100	115	ns	–
	t_{WH}	10	–	50	60		
Input Pulse Rise & Fall Time	$t_r\phi$,	5	–	–	15	µs	–
	$t_f\phi$	10	–	–	10		
Maximum Input-Pulse Frequency	$f\phi$	3	50●	–	–	kHz	1
	$f_m\phi$	5	4.4	5	–	MHz	–
	$f_m\phi$	10	8.5	10	–		
	$f\phi$	15	2●	–	–	MHz	1
Input Capacitance	C_I	Any Input	–	5	–	pF	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional tests, all inputs/outputs to truth table.

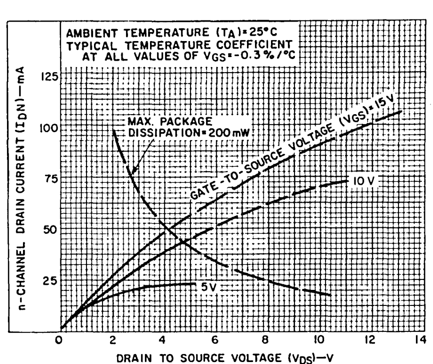


Fig. 3—Minimum n-channel drain characteristics.

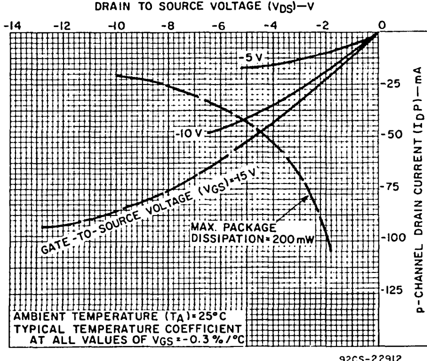


Fig. 4—Minimum p-channel drain characteristics.

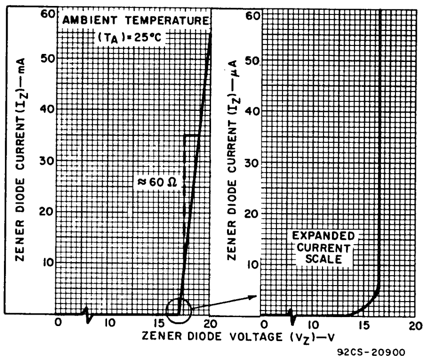
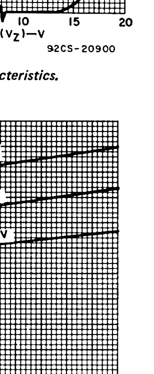



Fig. 5 – Typical zener diode characteristics.

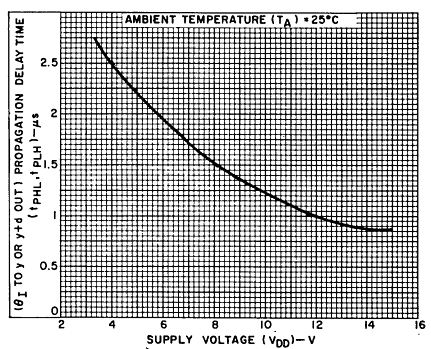


Fig. 6 – Typical propagation delay (ϕ_1 to y or y+d out) vs. V_{DD}.

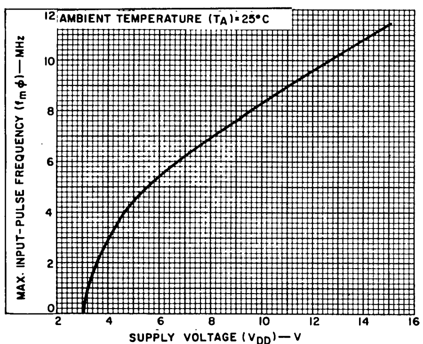


Fig. 7 – Typical transition time vs. C_L.

Fig. 8 – Minimum $f_m\phi$ vs. V_{DD}

TEST CIRCUITS

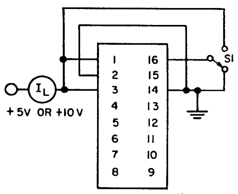


Fig. 9 – Quiescent current.

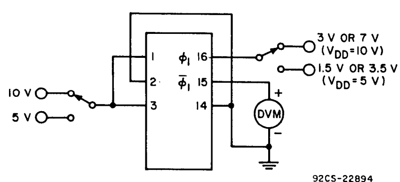


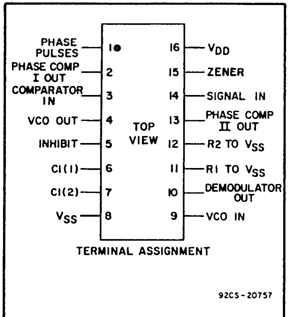
Fig. 10 – Noise immunity.

Solid State Division

Digital Integrated Circuits

Monolithic Silicon

CD4046A/...



High-Reliability COS/MOS Micropower Phase-Locked Loop

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- Very low power consumption ...... 70 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V
- Operating frequency range .... up to 1.2 MHz (typ.) at V_{DD} = 10 V
- Wide supply-voltage range .... $V_{DD} - V_{SS}$ = 5 to 15 V
- Low frequency drift .... 0.06%/°C (typ.) at V_{DD} = 10 V
- Choice of two phase comparators .... 1. Exclusive-OR network 2. Edge-controlled memory network with phase-pulse output for lock indication
- High VCO linearity .... 1% (typ.)
- VCO inhibit control for ON-OFF keying and ultra-low standby power consumption
- Zener diode to assist supply regulation
- Source-follower output of VCO control input (Demod. output)

Applications:

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discriminator
- Data synchronization
- Voltage-to-frequency conversion
- Tone decoding
- FSK – Modems
- Signal conditioning
- (See companion application note ICAN-6101 for application information and circuit details)

RCA-CD4046A "Slash" (/) Series are high-reliability COS/MOS integrated circuit Phase-Locked Loops intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment.

These devices are electrically and mechanically identical with standard COS/MOS CD4046A types described in data bulletin 637 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4046A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

The RCA-CD4046A COS/MOS Micropower Phase-Locked Loop (PPL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a

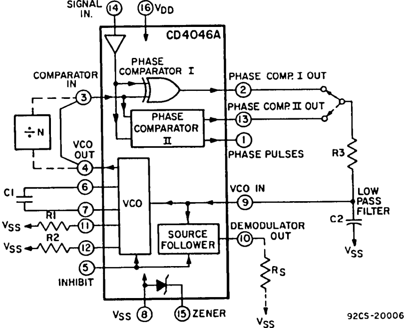


Fig. 1 – COS/MOS phase-locked loop block diagram.

common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary. The CD4046A is supplied in a 16-lead dual-in-line ceramic package (CD4046AD), It is also available in chip form (CD4046AH).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD4024A,CD4018A,CD4020A,CD4022A, or CD4029A. One or more CD4018A (Presettable Divide-by-N Counter) or CD4029A (Presettable Up/Down Counter), together with the CD4046A (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ⩽ 30% ($V_{DD}-V_{SS}$), logic "1" ⩾ 70% ($V_{DD}-V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_c$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ⩽ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response charac-

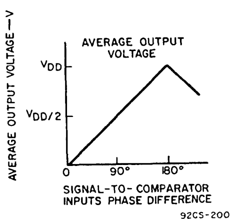


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

teristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The

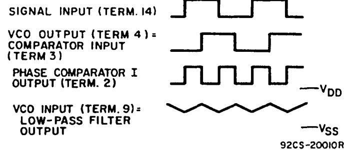


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON continuously. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs

are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

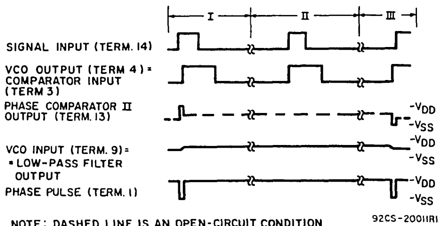
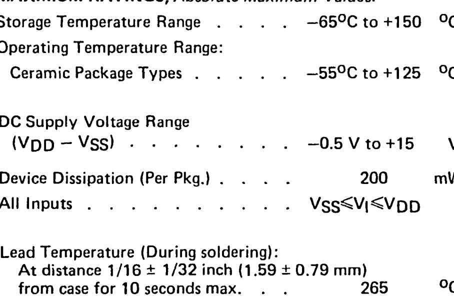


Fig.4 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.



MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range	−65°C to +150	°C
Operating Temperature Range:		
Ceramic Package Types	−55°C to +125	°C
DC Supply Voltage Range ($V_{DD} - V_{SS}$)	−0.5 V to +15	V
Device Dissipation (Per Pkg.)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Lead Temperature (During soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . .	265	°C

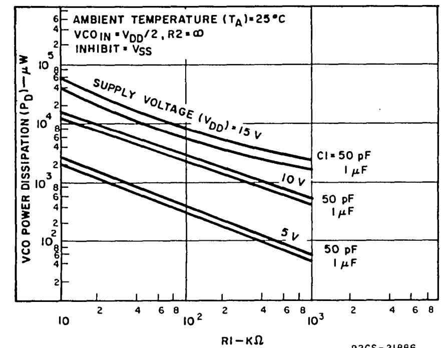


Fig.5 (a) – Typical VCO power dissipation at center frequency vs R1.

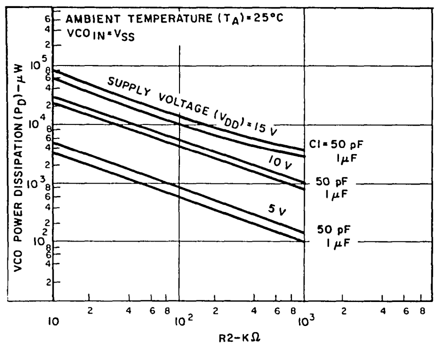


Fig.5 (b) – Typical VCO power dissipation at f_{min} vs R2.

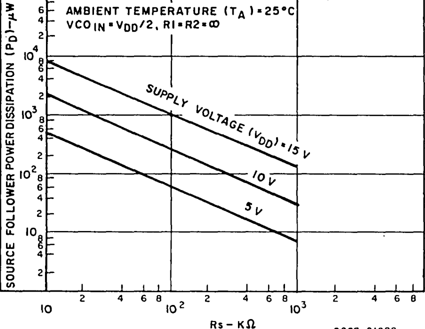


Fig. 5(c) Typical source follower power dissipation vs. R_S.

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S) – Phase Comparator I

P_D (Total) = P_D (f_{MIN}) – Phase Comparator II

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$10\ k\Omega \leq R1, R2, R_S \leq 1\ M\Omega$
$C1 \geq 100\ pF$ at $V_{DD} \geq 5\ V$;
$C1 \geq 50\ pF$ at $V_{DD} \geq 10\ V$

In addition to the given design information refer to Fig. 5 for R1, R2, and C1 component selections.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency	f_{MAX}, f_O, $2f_L$, f_{MIN}, $V_{DD}/2$, V_{DD} — VCO INPUT VOLTAGE	f_O, f_{MAX}, $2f_L$, f_{MIN}, $V_{DD}/2$, V_{DD} — VCO INPUT VOLTAGE	f_{MAX}, f_O, $2f_L$, f_{MIN}, $V_{DD}/2$, V_{DD} — VCO INPUT VOLTAGE	f_O, f_{MAX}, $2f_L$, f_{MIN}, $V_{DD}/2$, V_{DD} — VCO INPUT VOLTAGE 92CS-20012R1
For No Signal Input	VCO in PLL system will adjust to center frequency, f_O		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	IN R3 OUT, C2; $\tau 1 = R3C2$	(1),(2) $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$	$f_C = f_L$	
Loop Filter Component Selection	IN R3 OUT, R4, C2 92CS-21901	For $2f_C$, see Ref. (2)		
Phase Angle between Signal and Comparator	90° at center frequency (f_O), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	– Given: f_O – Use f_O with Fig.5a to determine R1 and C1	– Given: f_O and f_L – Calculate f_{min} from the equation $f_{min} = f_O - f_L$ – Use f_{min} with Fig. 5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_O + f_L}{f_O - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1	– Given: f_{max} – Calculate f_O from the equation $f_O = \frac{f_{max}}{2}$ – Use f_O with Fig.5a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1

For further information, see

(1) F. Gardner, "Phase-Lock Techniques", John Wiley and Sons, New York, 1966
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O VOLTS	V_{DD} VOLTS	LIMITS CD4046AD, CD4046AK MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
VCO Section									
Operating Supply Voltage	$V_{DD}-V_{SS}$	As fixed oscillator only			3	–	15	V	–
		Phase-lock-loop operation			5	–	15		
Operating Power Dissipation	P_D	f_o = 10 kHz, R_1 = 1 MΩ, R2 = ∞, $VCO_{IN} = \frac{V_{DD}}{2}$		5	–	70	–	µW	6a
				10	–	600	–		
				15	–	2400	–		
Maximum Operating Frequency	f_{MAX}	R1 = 10 kΩ, R2 = ∞, $VCO_{IN} = V_{DD}$; C1 = 100 pF		5	0.25	0.5	–	MHz	–
		C1 = 50 pF		10	0.6	1.2	–		
				15	–	1.5	–		
Center Frequency and	f_o	Programmable with external components R1, R2, and C1							See Design Info.
Frequency Range	$f_{MAX}-f_{MIN}$								
Linearity	–	VCO_{IN} = 2.5 V ±0.3 V, R1 > 10 kΩ		5	–	1	–	%	–
		= 5 V ± 2.5 V, R1 > 400 kΩ		10	–	1	–		7a,b
		= 7.5 V ± 5 V, R1 = 1 MΩ		15	–	1	–		
Temperature-Frequency Stability: No Frequency Offset f_{MIN} = 0	–	R2 = ∞, $\%/°C \propto \frac{1}{f \cdot V_{DD}}$		5	–	0.12–0.24	–	%/°C	–
				10	–	0.04–0.08	–		
				15	–	0.015–0.03	–		
Frequency Offset $f_{MIN} \neq 0$	–	$\%/°C \propto \frac{1}{f \cdot V_{DD}}$		5	–	0.06–0.12	–		–
				10	–	0.05–0.1	–		
				15	–	0.03–0.06	–		
Input Resistance of VCO_{IN} (Term 9)	R_I			5,10,15	–	10^{12}	–	Ω	–
VCO Output Voltage (Term 4) Low Level	V_{OL}	Driving COS/MOS-Type Load (e.g. Term 3 Phase Comparator Input)		5,10,15	–	–	0.01	V	–
High Level	V_{OH}			5	4.99	–	–		–
				10	9.99	–	–		
				15	14.99	–	–		
VCO Output Duty Cycle				5,10,15	–	50	–	%	–
VCO Output Transition Times	t_{THL}, t_{TLH}			5	–	75	150	ns	–
				10	–	50	100		
				15	–	40	–		
VCO Output Drive Current: n-Channel (Sink)	I_DN		0.5	5	0.43	0.86	–	mA	–
			0.5	10	1.3	2.6	–		
p-Channel (Source)	I_DP		4.5	5	–0.3	–0.6	–		–
			9.5	10	–0.9	–1.8	–		
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	–	R_S > 10 kΩ		5,10	–	1.5	2.2	V	–
				15	–	1.5	–		
Linearity	–	R_S > 50 kΩ, VCO_{IN} = 2.5 ±0.3 V		5	–	0.1	–	%	–
		= 5 ± 2.5 V		10	–	0.6	–		
		= 7.5 ± 5 V		15	–	0.8	–		
Zener Diode Voltage CD4046AD, CD4046AK	V_Z	I_Z = 50 µA			4.7	5.2	5.7	V	–
Zener Dynamic Resistance	R_Z	I_Z = 1 mA			–	100	–	Ω	–

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O VOLTS	V_{DD} VOLTS	LIMITS CD4046AD, CD4046AK MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
PHASE COMPARATOR Section									
Operating Supply Voltage	$V_{DD}-V_{SS}$	Amplifier Operation		–	5	–	15	V	–
		Comparators only		–	3	–	15	V	–
Total Quiescent Device Current: Term. 14 Open	I_L	Term. 15 open, Term. 5 at V_{DD}, Terms. 3 & 9 at V_{SS}		5	–	25	55	μA	–
				10	–	200	410		
Term. 14 at V_{SS} or V_{DD}				5	–	5	15		
				10	–	25	60		
Term. 14 (SIGNAL IN) Input Impedance	Z_{14}			5	1	2	–	MΩ	–
				10	0.2	0.4	–		
				15	–	0.2	–		
AC-Coupled Signal Input Voltage Sensitivity				5	–	200	400	mV	8
				10	–	400	800		
				15	–	700	–		
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity: Low Level				5	1.5	2.25	–	V	–
				10	3	4.5	–		
				15	4.5	6.75	–		
High Level				5	–	2.75	3.5	V	–
				10	–	5.5	7		
				15	–	8.25	–		
Output Drive Current: n-Channel (Sink)	I_DN	Phase Comparator I & II Term. 2 & 13	0.5	5	0.43	0.86	–	mA	–
			0.5	10	1.3	2.5	–		–
		Phase Pulses	0.5	5	0.23	0.47	–		–
			0.5	10	0.7	1.4	–		–
p-Channel (Source)	I_DP	Phase Comparator I & II Term. 2 & 13	4.5	5	–0.3	–0.6	–	mA	–
			9.5	10	–0.9	–1.8	–		–
		Phase Pulses	4.5	5	–0.08	–0.16	–		–
			9.5	10	–0.25	–0.5	–		–

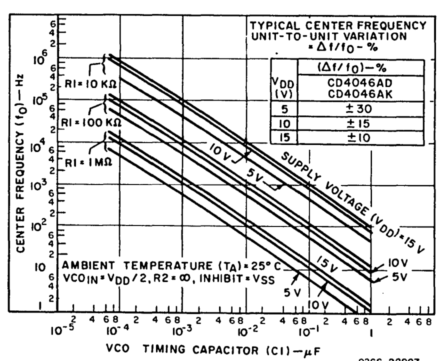


Fig. 6(a) – Typical center frequency vs. C1 for R1 = 10 kΩ, 100 kΩ, and 1 MΩ. Lower frequency values are obtainable if larger values of C1 are used.

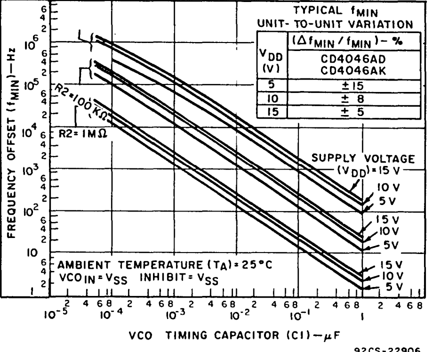


Fig. 6(b) – Typical frequency offset vs. C1 for R2 = 10 kΩ, 100 kΩ, and 1 MΩ. Lower frequency values are obtainable if larger values of C1 are used.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS AT INDICATED TEMPERATURES CD4046AD, CD4046AK −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	NOTES
Static												
Total Quiescent Device Current (Term 16 at V_{DD})	I_L			10	–	10•	–	10•	–	200•	μA	1
Quiescent Device Dissipation Per Package (Term 16 at V_{DD})	P_D			10	–	100	–	100	–	2000	μW	–
VCO Oscillator Current	I_{VCO}	Adjust R_2 on Term 12 For: −10 μA		10	-21	−31	−20•	−30•	−19	−29	μA	2
		Adjust R_2 on Term 12 For: −100 μA		10	−210	−270	−200•	−260•	−190	−250	μA	2
Output Voltage: Low Level	V_{OL}			4.5	–	0.55•	–	0.5•	–	–	V	1
				15	–	–	–	0.5•	–	0.25•		
High-Level	V_{OH}			4.5	3.96•	–	4.0•	–	–	–	V	1
				15	–	–	14.5•	–	14.7•	–		
Threshold Voltage: n-Channel	$V_{TH}N$	I_D = −10 μA		10	−7.5•	–	−7.8•	–	−7.8•		V	2
p-Channel	$V_{TH}P$	I_D = 10 μA		10	7.5•	–	7.8•	–	7.8•			
Output Drive Current: n-Channel:												
VCO Out (Term 4)					–	–	1.3•	–	–	–		
VCO C1 (Term 6)					–	–	1.9•	–	–	–		
VCO C1 (Term 7)					–	–	1.9•	–	–	–		
VCO R_2 to V_{SS} Term 12	I_{DN}		0.5	10	–	–	5.0•	–	–	–	mA	2
Phase Comp. I Out (Term 2)					–	–	1.3•	–	–	–		
Phase Comp. II Out (Term 13)					1.6•	–	1.3•	–	1.1•	–		
Phase Comp. II Phase Pulses (Term 1)					–	–	0.7•	–	–	–		
p-Channel:												
VCO Out (Term 4)					–	–	−0.9•	–	–	–		
Phase Comp. I Out (Term 2)	I_DP				–	–	−0.9•	–	–	–	mA	2
Phase Comp. II Out (Term 13)			9.5	10	−1.1•	–	−0.9•	–	0.7•	–		
Phase Comp. II Phase Pulses (Term 1)					–	–	−0.65•	–	–	–		
Zener Diode Voltage	V_Z	V_{SS} = Ground, 50 μA into Term 15	–	–	–	–	4.7•	5.7•	–	–	V	2
Diode Test	V_F	100 μA at each input or output	–	–	–	1.5•	–	1.5•	–	1.5•	V	
Dynamic												
Phase Comp. No. 1 Output Voltage		Input Signal Voltage (Term 14) = 400 mV f = 10 kHz, See Fig. 7	–	5	–	–	2.4•	2.6•	–	–	V	2
Phase Comp. No. 1 Output Voltage		Input Signal Voltage (Term 14) = 800 mV f = 10 kHz, See Fig. 7	–	10	–	–	4.8•	5.2•	–	–	V	2

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.

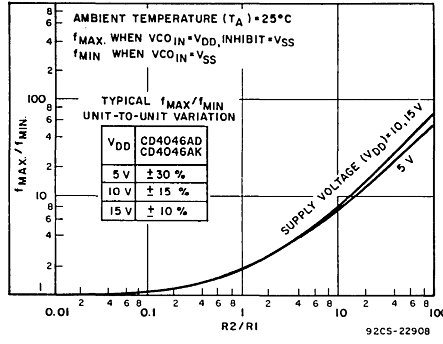


Fig. 6(c) – Typical $f_{max.}/f_{min.}$ vs. R2/R1.

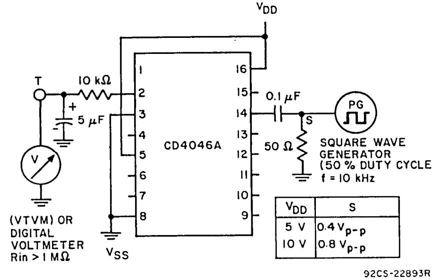


Fig. 7 – Test circuit for Phase Comparator I Output voltage.

Solid State Division

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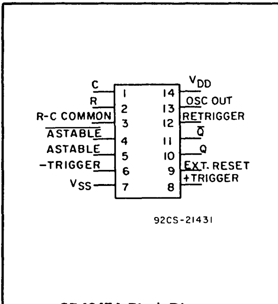
Monolithic Silicon

High-Reliability Slash(/) Series

CD4047A/...



CD4047A Block Diagram

High-Reliability COS/MOS Low-Power Monostable/Astable Multivibrator

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Low power consumption: special COS/MOS oscillator configuration**
- **Monostable (one-shot) or astable (free-running) operation**
- **True and complemented buffered outputs**
- **Only one external R and C required**

Monostable Multivibrator Features:

- **Positive- or negative-edge trigger**
- **Output pulse width independent of trigger pulse duration**
- **Retriggerable option for pulse width expansion**
- **Long pulse widths possible using small RC components by means of external counter provision**
- **Fast recovery time essentially independent of pulse width**
- **Pulse-width accuracy maintained at duty cycles approaching 100%**

Astable Multivibrator Features:

- **Free-running or gatable operating modes**
- **50% duty cycle**
- **Oscillator output available**
- **Good astable frequency stability:**
  frequency deviation = ±2% + 0.03%/°C @ 100 kHz*
  = ±0.5% + 0.015%/°C @ 10 kHz*

COS/MOS Features:

- **Microwatt quiescent power dissipation: 0.5 μW (typ.)**
- **High noise immunity: 45% of supply voltage (typ.)**
- **Wide operating-temperature range: −55°C to +125°C**

Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- **Frequency discriminators**
- **Timing circuits**
- **Time-delay applications**
- **Envelope detection**
- **Frequency multiplication**
- **Frequency division**

* Circuits "trimmed" to frequency; V_{DD} = 10 V ± 10%.

RCA CD4047A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment.

RCA CD4047A consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action having retriggering and external counting options.

Inputs include +Trigger, −Trigger, Astable, $\overline{\text{Astable}}$, Retrigger, and External Reset. Buffered outputs are Q, $\overline{\text{Q}}$, and Oscillator. In all modes of operation an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the Astable input. The period of the square wave at the Q and $\overline{\text{Q}}$ outputs in this mode of operation is a function of the external components employed. "True" input pulses on the Astable input or "Complement" pulses on the $\overline{\text{Astable}}$ input allow the circuit to be used as a gatable multivibrator. An output whose period is half of that which appears at the Q terminal is available at the Oscillator Output terminal. However, a 50% duty cycle is not guaranteed at this output. A high level should be applied to the external reset whenever V_{DD} power is applied or removed.

In the monostable mode positive-edge triggering is accomplished by application of a leading-edge pulse to the "+Trigger" input and a low level to the "−Trigger" input. For negative-edge triggering a trailing-edge pulse is applied to the "−Trigger" and a high level is applied to the "+Trigger". Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the "Retrigger" and "+Trigger" inputs. In this mode the output pulse remains "high" as long as the input pulse period is shorter than the period determined by the RC components.

An external countdown option can be implemented by coupling "Q" to an external "N" counter (e.g. CD4017A) and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{Astable}}$ input and has a duration equal to N times the period of the multivibrator.

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A high level on the External Reset input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time.

These devices are electrically and mechanically identical with standard COS/MOS CD4047A types described in data bulletin 623 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4047A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs†	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}

† Special input protection circuit permits terminal 3 voltage to exceed V_{DD} or V_{SS} by as much as 15 volts.

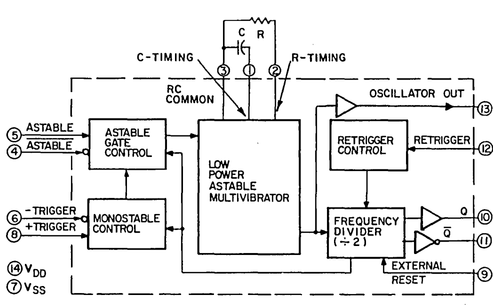


Fig.1 – CD4047A logic block diagram.

CD4047A FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	t_A(10,11)=4.40 RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A(13)=2.20 RC
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator:					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M(10,11)=2.48 RC
External Countdown*	14	5, 6, 7, 8, 9, 12	–	10, 11	

* Input Pulse to Reset of External Counting Chip
External Counting Chip Output To Terminal 4

▲ See Text.

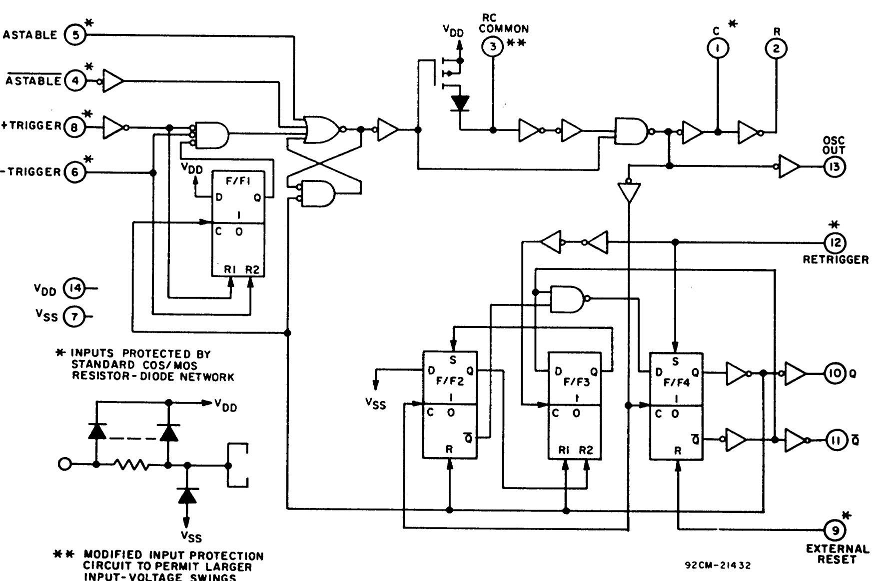


Fig.2 – CD4047A logic diagram.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4047AD,CD4047AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.5	5	–	–	300	µA	20	1
			10	–	–	10•	–	1	10•	–	–	200•			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	2.5	25	–	–	1500	µW	–	–
			10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}		3	–	–	0.55•	–	–	0.5•	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5•	–	–	0.55•			
High-Level	V_{OH}		3	2.25•	–	–	2.3•	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5•	–	–	14.45•	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = −10 µA		−0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	–	2
P-Channel	$V_{TH}P$	I_D = 10 µA		0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity (Any input)	V_{NL}	0.8	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	21	1
		1.0	10	3•	–	–	3•	4.5	–	2.9•	–	–			
For Definition, see Appendix in SSD-207	V_{NH}	4.2	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V		
		9.0	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: (Q and $\bar{Q}$) N-Channel	$I_D N$	0.5	5	0.5	–	–	0.4•	0.8	–	0.28	–	–	mA	3,4	2
		0.5	10	1.25	–	–	1•	2	–	0.7	–	–			
P-Channel	$I_D P$	4.5	5	−0.5	–	–	−0.4•	−0.8	–	−0.28	–	–	mA	5,6	
		9.5	10	−1.25	–	–	−1•	−2	–	−0.7	–	–			
(OSCILLATOR) N-Channel	$I_D N$	0.5	5	–	–	–	0.8	–	–	–	–	–	–	–	–
		0.5	10	–	–	–	2	–	–	–	–	–			
P-Channel	$I_D P$	4.5	5	–	–	–	−0.8	–	–	–	–	–	–	–	
		9.5	10	–	–	–	−2	–	–	–	–	–			
Diode Test 100 µA Test Pin	V_{DF}			–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $C_L = 15$ pF
Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4047AK CD4047AD			UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time: Astable, $\overline{Astable}$ to Osc. Out	t_{PHL} t_{PLH}		5	–	200	400	ns	–	–
			10	–	100	200			
Astable, $\overline{Astable}$ to Q, $\overline{Q}$			5	–	550	900		–	1
			10	–	250	500●			
+Trigger, −Trigger to Q, $\overline{Q}$			5	–	700	1200		7	1
			10	–	300	600●			
+Trigger, Retrigger to Q, $\overline{Q}$			5	–	300	600		–	–
			10	–	175	300			
External Reset to Q, $\overline{Q}$			5	–	300	600		–	–
			10	–	125	250			
Transition Time: Q, $\overline{Q}$	t_{THL}, t_{TLH}		5	–	75	125	ns	8	–
			10	–	45	75			
Osc. Out			5	–	75	150		–	–
			10	–	45	100			
Minimum Input Pulse Duration (Any input)	t_{WL}, t_{WH}		5	–	500	1000	ns	–	–
			10	–	200	400			
+Trigger, Retrigger Rise & Fall Time	t_r, t_f		5	–	–	15	μs	–	–
			10	–	–	5			
Average Input Capacitance	C_I	Any input	–	–	5	–	pF	–	–

Note 1: Test is a one input, one output only.
Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

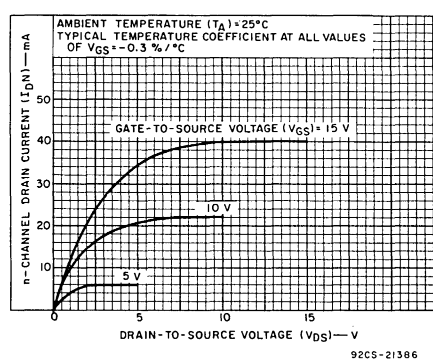


Fig.3 – Typical n-channel drain characteristics for Q and $\overline{Q}$ buffers.

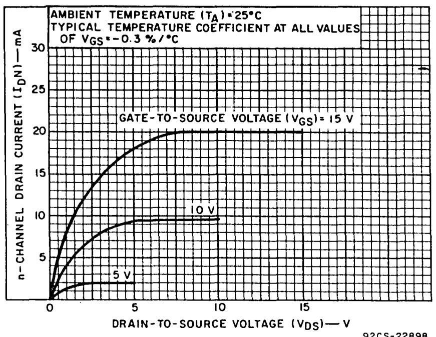


Fig.4 – Minimum n-channel drain characteristics for Q and $\overline{Q}$ buffers.

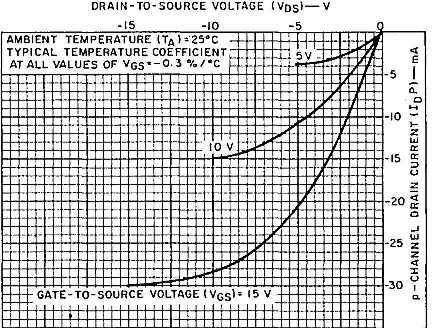


Fig.5 — Typical p-channel drain characteristics for Q and $\overline{Q}$ buffers.

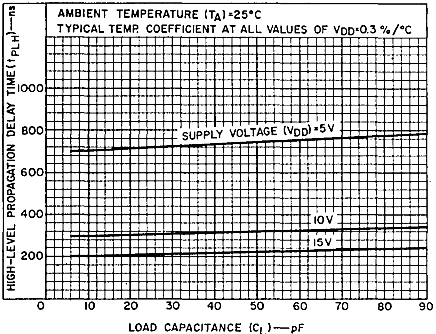


Fig.7 — Typical low-to-high level propagation delay time vs. load capacitance for Q and $\overline{Q}$ buffers.

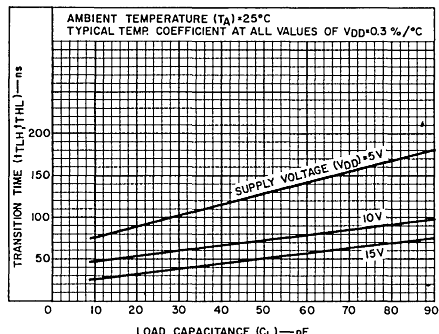


Fig.8 — Typical transition time vs. load capacitance for Q and $\overline{Q}$ buffers.

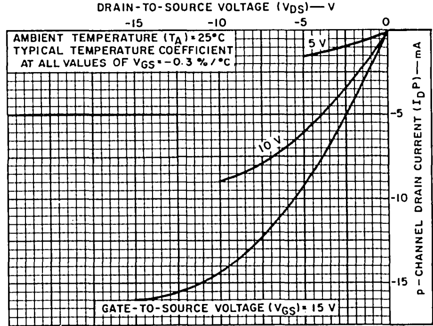


Fig.6 — Minimum p-channel drain characteristics for Q and $\overline{Q}$ buffers.

I. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33%–67% V_{DD}) for free-running (astable) operation.

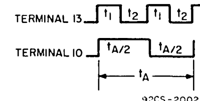


Fig.9 — Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2\,(t_1 + t_2)$$

$$= -2\,RC \ln \frac{(V_{TR})\,(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})\,(2V_{DD} - V_{TR})}$$

Typ:	$V_{TR} = 0.5\,V_{DD}$	$t_A = 4.40\,RC$
Min:	$V_{TR} = 0.33\,V_{DD}$	$t_A = 4.62\,RC$
Max:	$V_{TR} = 0.67\,V_{DD}$	$t_A = 4.62\,RC$

thus if $\boxed{t_A = 4.40\,RC}$ is used, the maximum variation will be (+5.0%, –0.0%).

B. Variations Due to V_{DD} and Temperature Changes

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 10 to 20 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

II. Monostable Mode Design Information

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% – 67% V_{DD}) for one-shot (monostable) operation.

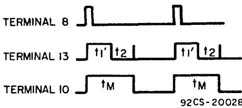


Fig.21 – Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ:	$V_{TR} = 0.5\ V_{DD}$	$t_M = 2.48\ RC$
Min:	$V_{TR} = 0.33\ V_{DD}$	$t_M = 2.71\ RC$
Max.	$V_{TR} = 0.67\ V_{DD}$	$t_M = 2.48\ RC$

Thus if $t_M = 2.48\ RC$ is used, the maximum variation will be (+9.3%, –0.0%).

Note:

In the astable mode, the first positive half cycle has a duration of T_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature. These variations are presented in graphical form in Figs.10 to 14 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

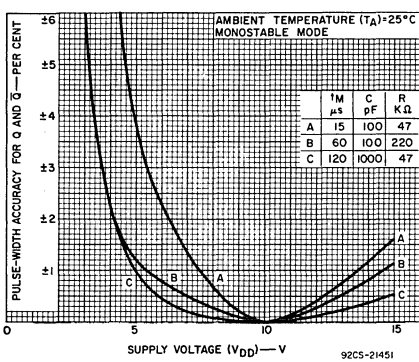


Fig.11 – Typical Q-and-Q̄-pulse-width accuracy vs. supply voltage (t_M = 15, 60, 120 µs).

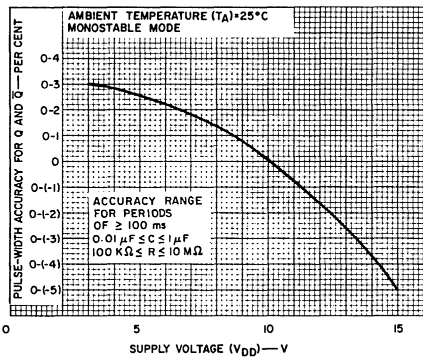


Fig.12 – Typical Q-and-Q̄-pulse-width accuracy vs. supply voltage (t_M ≥ 100 ms).

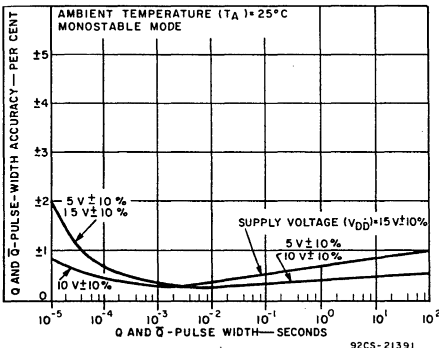


Fig.10 – Typical Q-and-Q̄-pulse-width accuracy vs. Q and Q̄ pulse width for a variation of ± 10% from value indicated.

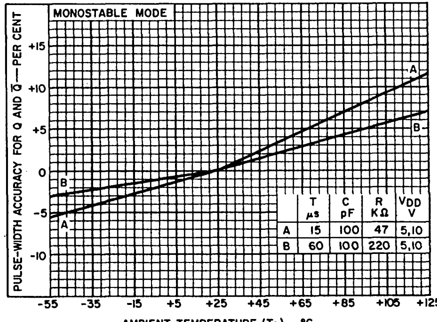


Fig.13 – Typical Q-and-Q̄-pulse-width accuracy vs. temperature (high frequency).

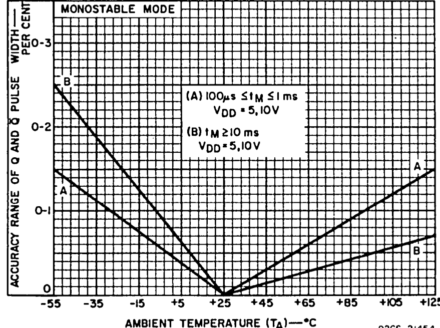


Fig.14 — Typical Q-and-$\overline{Q}$-pulse-width accuracy range vs. temperature.

III. Retrigger Mode Operation

The CD4047A can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig.15, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT) terminates at some variable time t_D

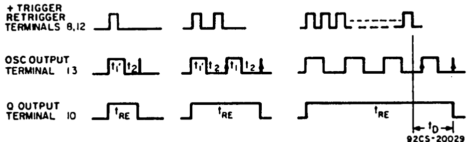


Fig.15 — Retrigger-mode waveforms.

after the termination of the last retrigger pulse. t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig.2).

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig.29. The pulse duration at the output is

$$t_{ext} = (N - 1)(t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

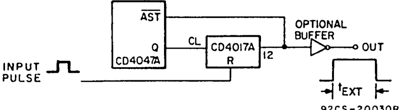


Fig.16 — Implementation of external counter option.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i. e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geq 100$ pF, up to any practical value, for astable modes;

$C \geq 1000$ pF, up to any practical value for monostable modes.

$10\ K\Omega \leq R \leq 1\ M\Omega$.

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode: $P = 2CV^2f$. (Output at terminal No. 13)

$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

Monostable Mode: $$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 30–32 for typical power consumption in astable mode.

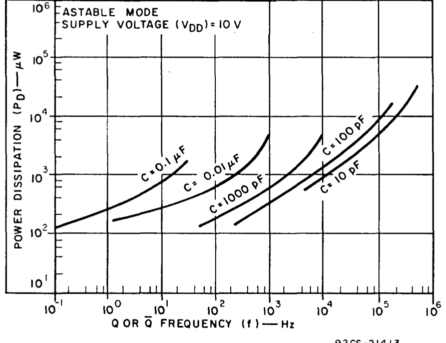
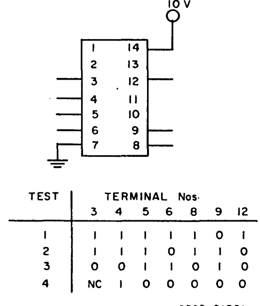


Fig.18 – Power dissipation vs. output frequency (V_{DD} = 10 V).



TEST	TERMINAL Nos. 3	4	5	6	8	9	12
1	1	1	1	1	1	0	1
2	1	1	1	0	1	1	0
3	0	0	1	1	0	1	0
4	NC	1	0	0	0	0	0

Fig.20 – Quiescent device current.

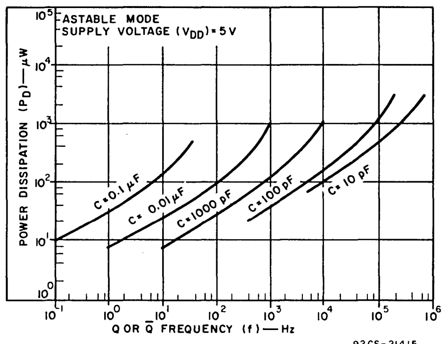


Fig.17 – Power dissipation vs. output frequency (V_{DD} = 5 V).

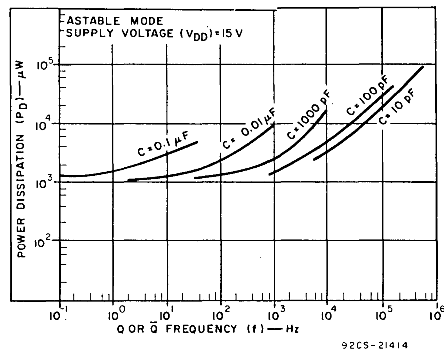


Fig.19 – Power dissipation vs. output frequency (V_{DD} = 15 V).

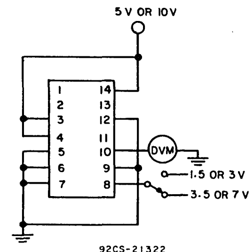


Fig.21 – Noise immunity.

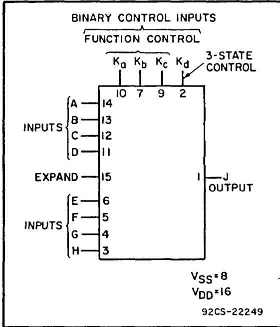
Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4048A/...



High-Reliability COS/MOS Multi-Function Expandable 8-Input Gate

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- **Medium-power TTL drive capability**
- **Three-state output**
- **High-current source and sink capability 9 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V**
- **Many logic functions available in one package**

Applications:

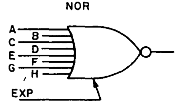
- **Selection of up to 8 logic functions**
- **Digital control of logic**
- **General-purpose gating logic**
  - **—Decoding**
  - **—Encoding**

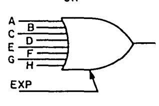
RCA CD4048A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4048A is an 8-input gate having four control inputs. Three binary control inputs — Ka, Kb, and Kc — provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR.

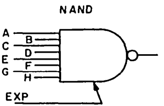
A fourth control input — Kd — provides the user with 3-state outputs. When control input Kd is "high" the output is either a logic 1 or a logic 0 depending on the input states. When control input Kd is "low", the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048A, (see Fig. 2). For example, two CD4048A's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

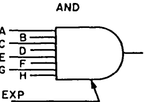
These devices are electrically and mechanically identical with standard COS/MOS CD4048A types described in data bulletin 636 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

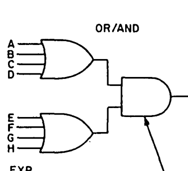
The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

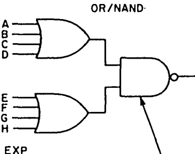


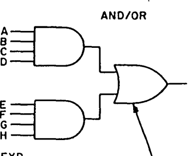


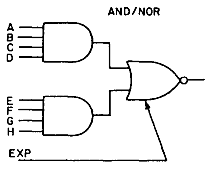












92CM-22250

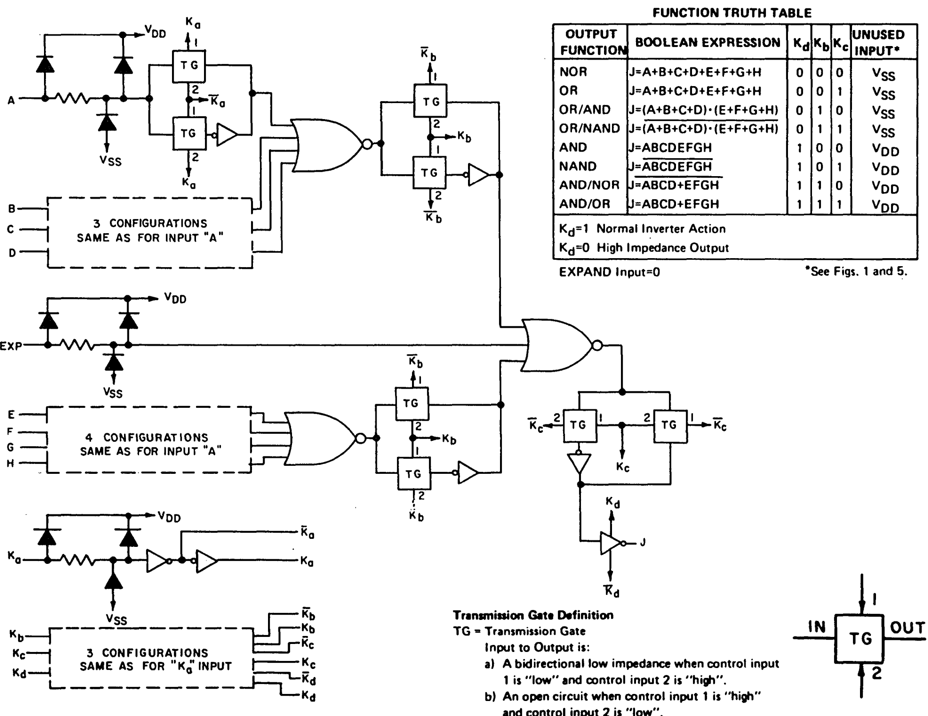
Fig. 1—Basic logic configurations.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4048A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range . . . . −65 to +150 °C
Operating-Temperature Range . . . . −55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) . . . . −0.5 to +15 V
Device Dissipation (Per Package) . . . . 200 mW
All Inputs . . . . $V_{SS} < V_I < V_{DD}$
Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) . . . . . 3 to 15 V
Recommended
Input-Voltage Swing . . . . V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32"
(1.59 ± 0.79 mm) from case
for 10 s max. . . . . +265 °C



FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_d	K_b	K_c	UNUSED INPUT*
NOR	J=A+B+C+D+E+F+G+H	0	0	0	V_{SS}
OR	J=A+B+C+D+E+F+G+H	0	0	1	V_{SS}
OR/AND	J=(A+B+C+D)·(E+F+G+H)	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	J=ABCDEFGH	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	J=ABCD+EFGH	1	1	1	V_{DD}

K_d=1 Normal Inverter Action
K_d=0 High Impedance Output

EXPAND Input=0

*See Figs. 1 and 5.

Transmission Gate Definition
TG = Transmission Gate
Input to Output is:
a) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high".
b) An open circuit when control input 1 is "high" and control input 2 is "low".

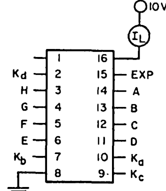
Fig. 2—Logic diagram and truth table.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4048AD, CD4048AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	NOTES
Quiescent Device Current	I_L		5	–	1	–	0.005	1	–	60	µA	1
			10	–	2•	–	0.01	2•	–	40•		
Quiescent Device Dissipation/Package	P_D		5	–	5	–	0.025	5	–	300	µW	–
			10	–	20	–	0.05	20	–	400		
Output Voltage Low-Level	V_{OL}		3	–	0.55•	–	–	0.5•	–	–	V	1
			5	–	0.01	–	0	0.01	–	0.05		
			10	–	0.01	–	0	0.01	–	0.05		
			15	–	–	–	–	0.5•	–	0.55•		
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	–	–	V	1
			5	4.99	–	4.99	5	–	4.95	–		
			10	9.99	–	9.99	10	–	9.95	–		
			15	–	–	14.5•	–	–	14.45•	–		
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = −20 µA		−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V	2
P-Channel	$V_{TH}P$	I_D = 20 µA		0.7•	3•	0.7•	1.5	3•	0.3•	3•		
Noise Immunity (Any Input)	V_{NL}	4.2	5	1.5	–	1.5•	2.25	–	1.4	–	V	1
		9	10	3•	–	3•	4.5	–	2.9•	–		
For Definition, See Appendix SSD-207	V_{NH}	0.8	5	1.4	–	1.5•	2.25	–	1.5	–	V	
		1	10	2.9•	–	3•	4.5	–	3•	–		
Output Drive Current: N-Channel	$I_D N$	0.4	4.5	2	–	1.6•	3.2	–	1.1	–	mA	2
		0.5	10	5.6	–	4.5•	9	–	3.1	–		
P-Channel	$I_D P$	4.6	5	−2	–	−1.6•	−3.2	–	−1.1	–	mA	2
		9.5	10	−5.6	–	−4.5•	−9	–	−3.1	–		
High and Low Voltage Current Test	$I_D N$, $I_D P$	0	3	–	–	0.28•	–	–	–	–	µA	2
		0	15	–	–	1.7•	–	–	–	–		
Diode Test, 100 µA Test Pin	V_{DF}			–	1.5•	–	–	1.5•	–	1.5•	V	3
Input Current	I_I			–	–	–	10	–	–	–	pA	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.



Input Conditions For Leakage Measurements:

	K_d	H	G	F	E	K_b	K_c	K_a	D	C	B	A	EXP
(1)	0	0	0	0	0	0	0	0	0	0	0	0	0
(2)	1	0	0	0	0	1	1	1	0	0	0	0	0
(3)	0	1	1	1	1	0	0	0	1	1	1	1	1
(4)	1	1	1	1	1	1	1	1	1	1	1	1	1

92CS-22259

Fig. 3— Quiescent device current.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C and C_L = 15 pF and 50 pF*

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

C_L = 15 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4048AD CD4048AK			UNITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.*		
Propagation Delay Time	t_{PLH}, t_{PHL}		5	–	750	1300	ns	1
			10	–	225	400●		
Transition Time: High-to-Low Level	t_{THL}		5	–	90	140	ns	1
			10	–	30	50●		
Low-to-High Level	t_{TLH}		5	–	130	250	ns	1
			10	–	40	60●		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (Volts)	Min.	Typ.	Max.*	UNITS	NOTES
Propagation Delay Time	t_{PLH}, t_{PHL}		5	–	775	1350	ns	–
			10	–	240	430		
Transition Time: High-to-Low Level	t_{THL}		5	–	105	170	ns	–
			10	–	40	70		
Low-to-High Level	t_{TLH}		5	–	145	280	ns	–
			10	–	50	80		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

*Max. Limits represent worst-case limits for worst-case modes of operation shown in test circuits in Appendix.

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is a one input one output only.

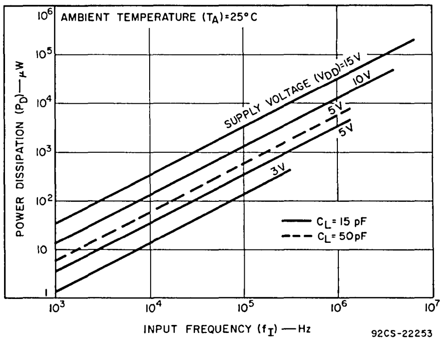


Fig. 4—Typical power dissipation as a function of input frequency.

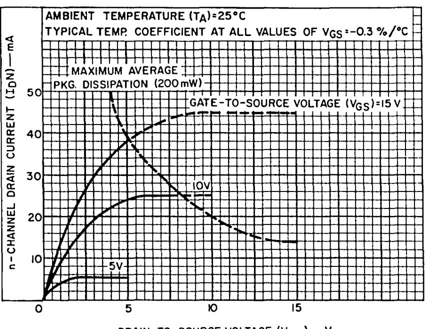


Fig. 5— Minimum n-channel drain characteristics.

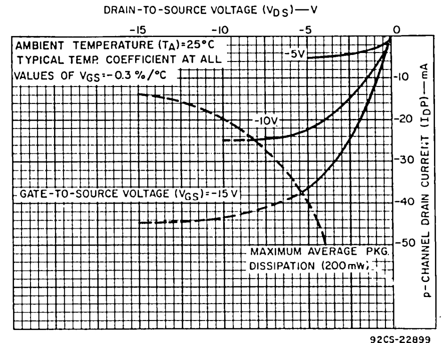


Fig. 6—Minimum p-channel drain characteristics.

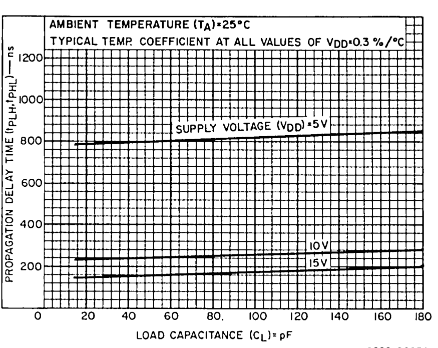


Fig. 7— Typical propagation delay time as a function of load capacitance.

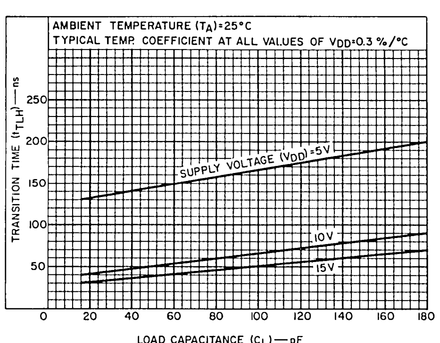


Fig. 8— Typical low-to-high level transition time as a function of load capacitance.

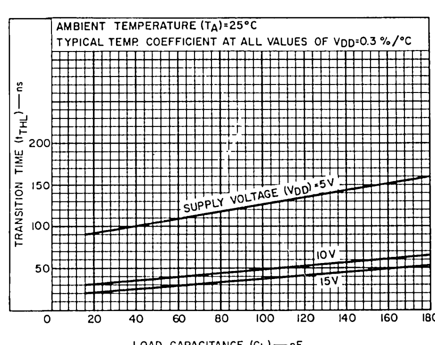


Fig. 9—Typical high-to-low level transition time as a function of load capacitance.

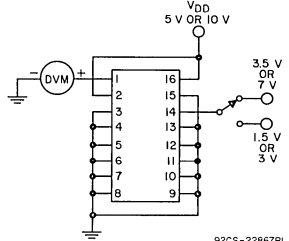


Fig. 10—Noise immunity test circuit.

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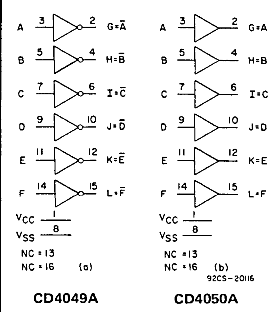


High-Reliability COS/MOS Hex Buffer/Converters

CD4049A–INVERTING TYPE   CD4050A–NON-INVERTING TYPE

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Direct Drive to 2 TTL Loads at 5 V, V_{CC} = 5 V, $V_{OL} \leq 0.4$ V, $I_DN \geq 3$ mA**
- **High Source and Sink Current Capability**
- **General COS/MOS Characteristics**

Applications:

- **COS/MOS to DTL/TTL Hex Converter**
- **COS/MOS Current "Sink" or "Source" Driver**
- **COS/MOS High-to-Low Logic-Level Converter**

RCA CD4049A and CD4050A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment.

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC} = 5 V, $V_{OL} \leq$ 0.4 V, and $I_DN \geq 3$ mA.)

Table 1 shows the range of voltage-supply levels that can be utilized for such logic level conversions. Conversion to logic-levels greater than +6 V is permitted provided that $V_{CC} \leq V_{IH}$. At 15 V the maximum allowable load capacitance is 5000 pF.

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation.

For simple logic-inversion applications it is more economical to use the CD4069B Hex Inverter scheduled for announcement in early 1974.

These devices are electrically and mechanically identical with standard COS/MOS CD4049A and CD4050A types described in data bulletin 599 and DATABOOK SSD-203 Series, but

TABLE I

FUNCTION	COS/MOS VOLTAGE RANGE (INPUT)	DTL/TTL VOLTAGE RANGE (OUTPUT)	POWER SUPPLY RANGE (V_{CC})
HEX LEVEL SHIFTER	3–15 V	3–6 V	3–6 V
HEX INVERTER HEX BUFFER	3–15 V	3–15 V	3–15 V

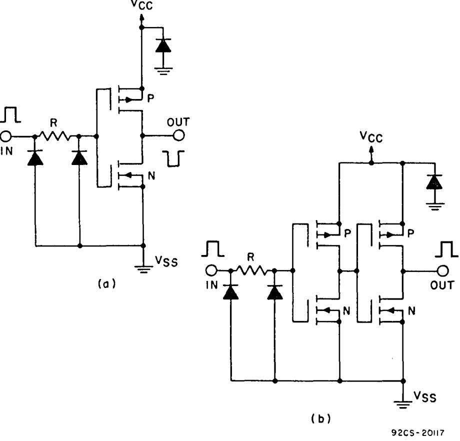


Fig. 1—a) Schematic diagram of CD4049A, 1 of 6 identical units; b) Schematic diagram of CD4050A, 1 of 6 identical units.

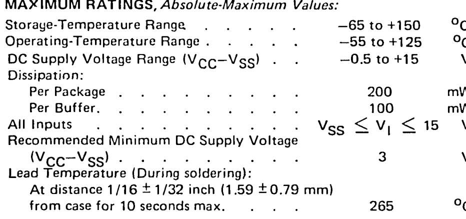
are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

RCA Designation	MIL-M-38510 Designation
CD4049A	MIL-M-38510/05503
CD4050A	MIL-M-38510/05504

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4049A and CD4050A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).



MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	–65 to +150	°C
Operating-Temperature Range	–55 to +125	°C
DC Supply Voltage Range (V_{CC}–V_{SS})	–0.5 to +15	V
Dissipation:		
Per Package	200	mW
Per Buffer	100	mW
All Inputs	$V_{SS} \leq V_I \leq 15$	V
Recommended Minimum DC Supply Voltage (V_{CC}–V_{SS})	3	V
Lead Temperature (During soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

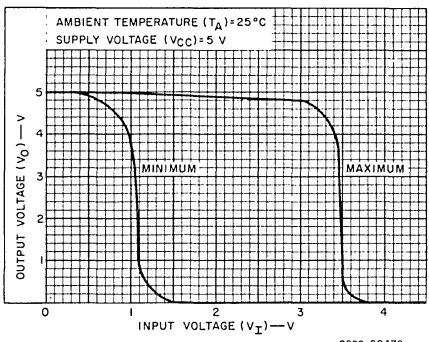


Fig. 2—Min. & max. voltage transfer characteristics of CD4049A.

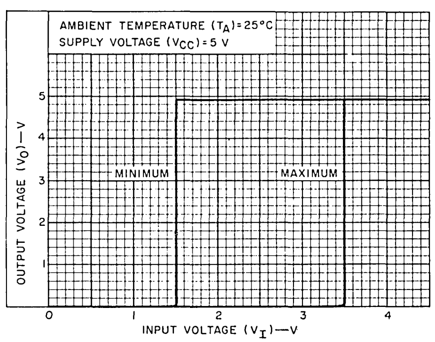


Fig. 3—Min. & max. voltage transfer characteristics of CD4050A.

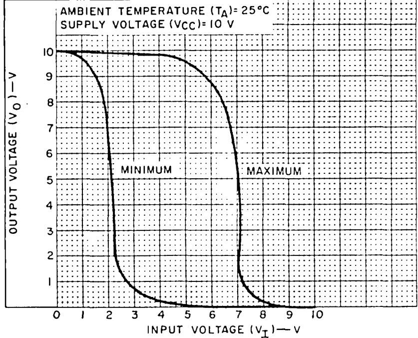


Fig. 4—Min. & max. voltage transfer characteristics for CD4049A.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{CC} Volts	LIMITS CD4049AD, CD4049AK CD4050AD, CD4050AK −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L	$V_{IH} = V_{CC}$		5	–	0.3	–	0.01	0.3	–	20	μA	17	1
				15	–	0.5•	–	0.01	0.5•	–	10•			
Quiescent Device Dissipation Package	P_D	$V_{IH} = V_{CC}$		5	–	1.5	–	0.05	1.5	–	100	μW		
				15	–	5	–	0.1	5	–	100			
Output Voltage Low-Level	V_{OL}			3	–	0.2•	–	–	0.6•	–	–	V	2–7	
				5	–	0.01	–	0	0.01	–	0.05			
				10	–	0.01	–	0	0.01	–	0.05			
				15	–	–	–	–	0.6•	–	0.7•			
High-Level	V_{OH}			3	2.8•	–	2.2•	–	–	–	–	V		
				5	4.99	–	4.99	5	–	4.95	–			
				10	9.99	–	9.99	10	–	9.95	–			
				15	–	–	14.4•	–	–	14.3•	–			
Threshold Voltage N-Channel	$V_{TH}N$	I_D = -10μA			-0.7•	-3•	-0.7•	-1.5	-3•	-0.3•	-3•	V		2
P-Channel	$V_{TH}P$	I_D = 10μA			0.7•	3•	0.7•	1.5	3•	0.3•	3•			
Noise Immunity (All Inputs) CD4049A	V_{NL}	V_{OH} = 3.6 V		5	1	–	1•	2.25	–	0.9	–	V	18	1
		V_{OH} = 7.2 V		10	2•	–	2•	4.5	–	1.9•	–			
CD4050A		V_{OL} = 0.95 V		5	1.5	–	1.5•	2.25	–	1.4	–			
		V_{OL} = 2.9 V		10	3•	–	3•	4.5	–	2.9•	–			
CD4050A	V_{NH}	V_{OH} = 7.2 V		10	2.9•	–	3•	4.5	–	3•	–			
		V_{OH} = 3.6 V		5	1.4	–	1.5•	2.25	–	1.5	–			
CD4049A		V_{OH} = 2.9 V		10	2.9•	–	3•	4.5	–	3•	–			
For Definition, See Appendix SSD-207		V_{OL} = 0.95 V		5	1.4	–	1.5•	2.25	–	1.5	–			
Output Drive Current N-Channel	$I_D N$		0.4	4.5	3.3	–	2.6•	5.2	–	1.8	–	mA	8,9	2
			0.4	5	3.75	–	3.0•	6	–	2.1	–			
			0.5	10	10	–	8•	16	–	5.6	–			
P-Channel	$I_D P$		4.5	5	-0.62	–	-0.5•	-1	–	-0.35	–			
			2.5	5	-1.85	–	-1.25•	-2.5	–	-0.9	–			
			9.5	10	-1.85	–	-1.25•	-2.5	–	-0.9	–			
Diode Test 100 μA Test Pin	V_{DF}				–	1.5•	–	–	1.5•	–	1.5•			
Input Current	I_I	$V_{IH} = V_{CC}$			–	–	–	10	–	–	–	pA		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{CC} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
				CD4049AD CD4049AK			CD4050AD CD4050AK					
			V_{CC} (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.			
Propagation Delay Time: High-to-Low Level	t_{PHL}	$V_{IH} = V_{CC}$	5	–	15	55	–	55	110	ns	10,11	1
			10	–	10	30•	–	25	55•			
Low-to-High Level	t_{PLH}	$V_{IH} = V_{CC}$	5	–	50	80	–	90	140	ns	12,13	
			10	–	25	55•	–	40	85•			
Transition Time: High-to-Low Level	t_{THL}	$V_{IH} = V_{CC}$	5	–	20	45	–	20	45	ns	14	1
			10	–	16	40•	–	16	40•			
Low-to-High Level	t_{TLH}	$V_{IH} = V_{CC}$	5	–	50	100	–	50	100	ns	15	
			10	–	30	60•	–	30	60•			
Input Capacitance	C_I	Any Input		–	5	–	–	5	–	pF	—	—

NOTE 1: Test is a one-input, one-output only.
Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

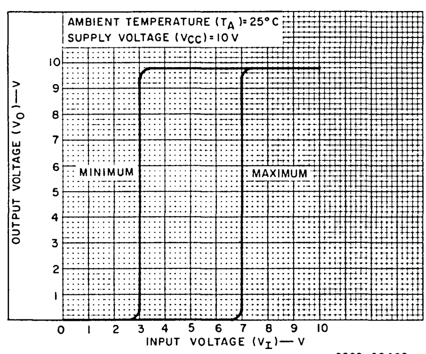


Fig. 5—Min. & max. voltage transfer characteristics for CD4050A.

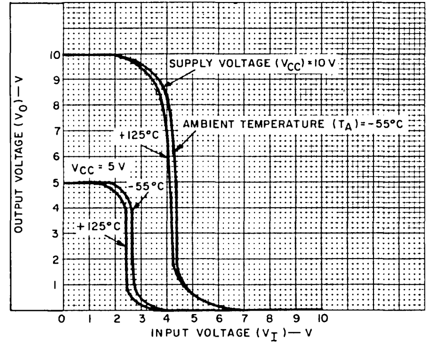


Fig. 6—Typ. voltage transfer characteristics as a function of temperature for CD4049A.

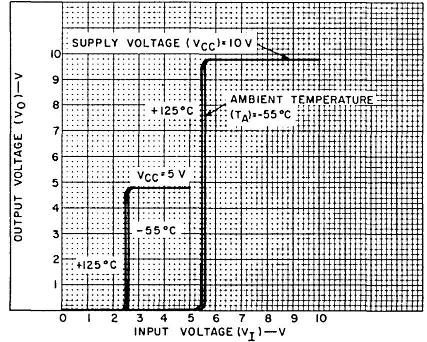


Fig. 7—Typ. voltage transfer characteristics as a function of temperature for CD4050A.

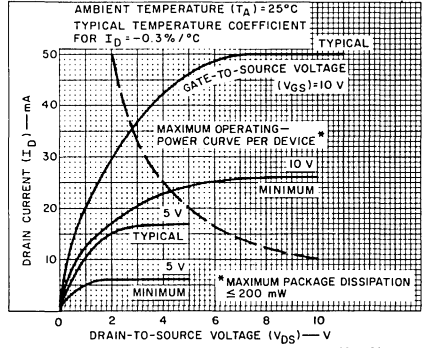


Fig. 8—Typ. & min. n-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

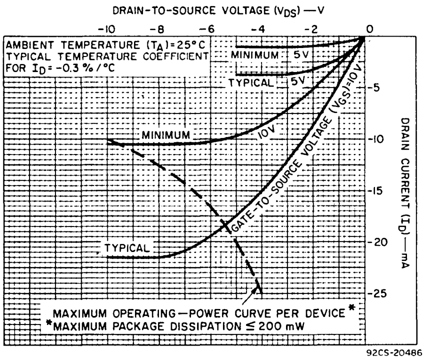


Fig. 9—Typ. & min. P-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

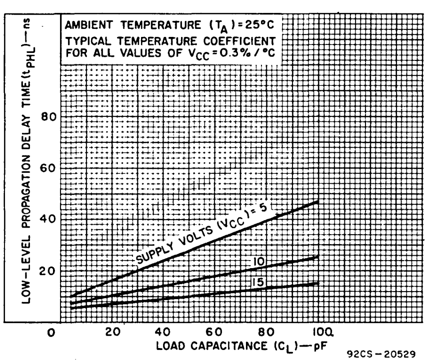


Fig. 10—Typ. high-to-low level propagation delay time vs. C_L for CD4049A.

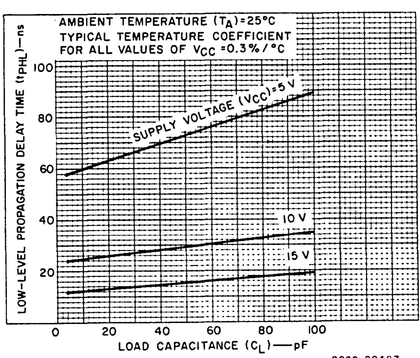


Fig. 11—Typ. high-to-low level propagation delay time vs. C_L for CD4050A.

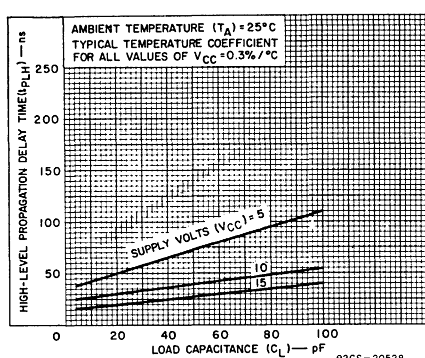


Fig. 12—Typ. low-to-high level propagation delay time vs. C_L for CD4049A.

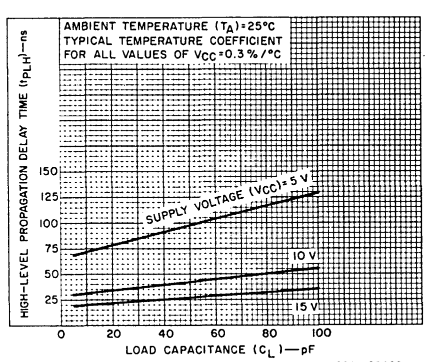


Fig. 13—Typ. low-to-high level propagation delay time vs. C_L for CD4050A.

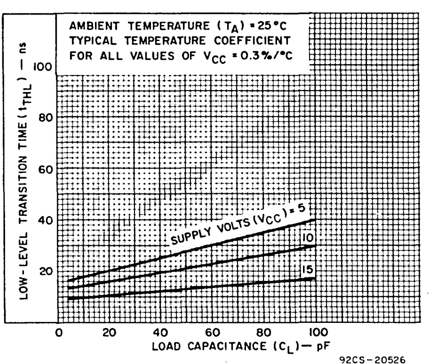


Fig. 14—Typ. high-to-low level transition time vs. C_L for CD4049A, CD4050A.

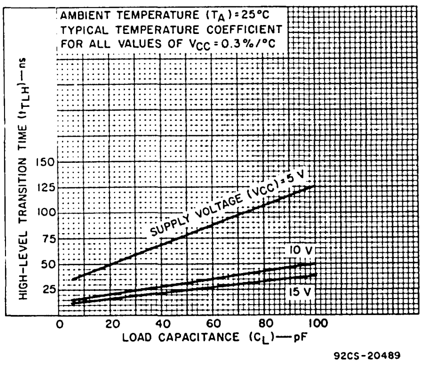


Fig. 15—Typ. low-to-high level transistion time vs C_L for CD4049A, CD4050A.

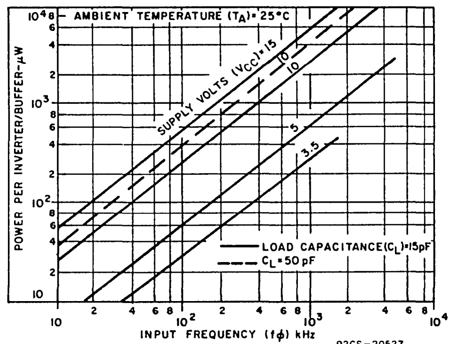


Fig. 16—Typ. dissipation characteristics for CD4049A, CD4050A.

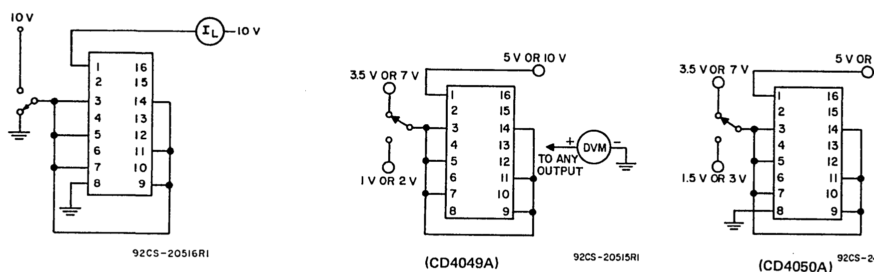


Fig. 17—Quiescent device current test circuit.

Fig. 18—Noise immunity test circuits.

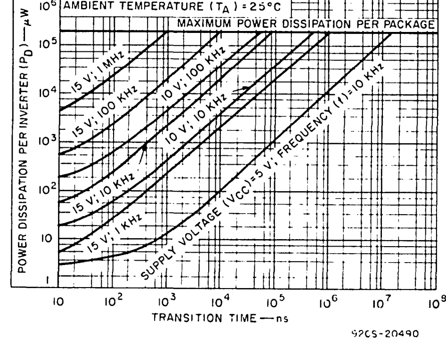


Fig. 19—Typ. power dissipation vs. transition time per inverter CD4049A.

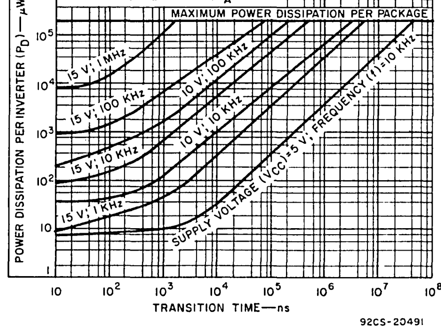


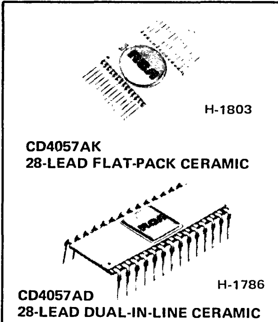
Fig. 20—Typ. power dissipation vs. transition time per inverter CD4050A.

Solid State
Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series
CD4057A/. . .



High-Reliability COS/MOS LSI 4-Bit Arithmetic Logic Unit

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **LSI Complexity on a Single Chip**
- **16-Instruction Capability**
  - **-Add, Subtract, Count**
  - **-AND, OR, Exclusive-OR**
  - **-Right, Left, or Cyclic Shifts**
- **Bidirectional Data Busses**
- **Instruction Decoding on Chip**
- **Fully Static Operation**
- **Single-Phase Clocking**
- **Easily Expandable to 8, 12, 16, . . . Bit Operation**
- **Conditional-Operation Controls on Chip**
- **Low Quiescent Device Dissipation . . . 10 μW (typ) at V_{DD} = 10 V**
- **Add Time (Data In-To Sum Out) = 375 ns (typ) at 10 V**
- **All Terminals Protected Against Static Discharge**
- **High Noise Immunity . . . 45% of V_{DD} (typ) Over Full Temperature Range**
- **Operation from Single Positive or Negative Power Supply . . . 3 V to 15 V**
- **Full Military Temperature Range . . . –55°C to +125°C**

RCA-CD4057A Slash (/) Series is a low-power arithmetic logic unit (ALU) designed for use in LSI computers. An arithmetic system of virtually any size can be constructed by wiring together a number of CD4057A ALU's. The CD4057A provides 4-bit arithmetic operations, time sharing of data terminals, and full functional decoding for all control lines. The distributed control system of this device provides great flexibility in system designs by allowing hard-wired connection of N units in 4^N unique combinations. Four control lines provide 16 instructions which include Addition, Subtraction, Bidirectional and Cycle Shifts, Up-Down Counting, AND, OR, and Exclusive-OR logic operations.

Two mode control lines allow the CD4057A to function as any 4-bit section of a larger arithmetic unit by controlling the bidirectional serial transfer of data to adjacent arithmetic arrays. By means of three "Conditional Control" lines Overflow, All Zeros, and Negative State conditions may be detected and used to establish a conditional operation. Predetermined operation of the CD4057A on a conditional basis allows greater ALU flexibility. Although especially applicable as a parallel arithmetic unit, the CD4057A also finds use in virtually any application requiring one or more of its 16 basic instructions. The CD4057A is supplied in a hermetically sealed 28-lead dual-in-line ceramic package (CD4057AD), in a flat-pack (CD4057AK), and in chip form (CD4057AH).

These devices are electrically and mechanically identical with standard COS/MOS CD4057A types described in data bulletin 635 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

Applications:

- **Parallel Arithmetic Units**
- **Process Controllers**
- **Remote Data Sets**
- **Graphic Display Terminals**

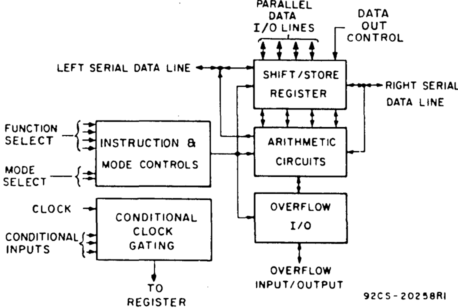


Fig. 1 – Block diagram – CD4057A.

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The packaged types in the CD4057A "Slash" (/) Series can be supplied to five screening levels – 1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

MAXIMUM RATINGS, *Absolute Maximum Values:*

STORAGE-TEMPERATURE RANGE .... −65 to +150 °C
OPERATING-TEMPERATURE RANGE .... −55 to +125 °C
DISSIPATION PER PACKAGE .... 200 mW
DC SUPPLY-VOLTAGE RANGE ($V_{DD}-V_{SS}$) ...... −0.5 to +15 V
ALL INPUTS .... $V_{SS} \leq V_I \leq V_{DD}$
Lead Temperature (During soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 seconds max. .... 265 °C
MINIMUM RECOMMENDED
DC SUPPLY VOLTAGE ($V_{DD}-V_{SS}$) .... 3 V

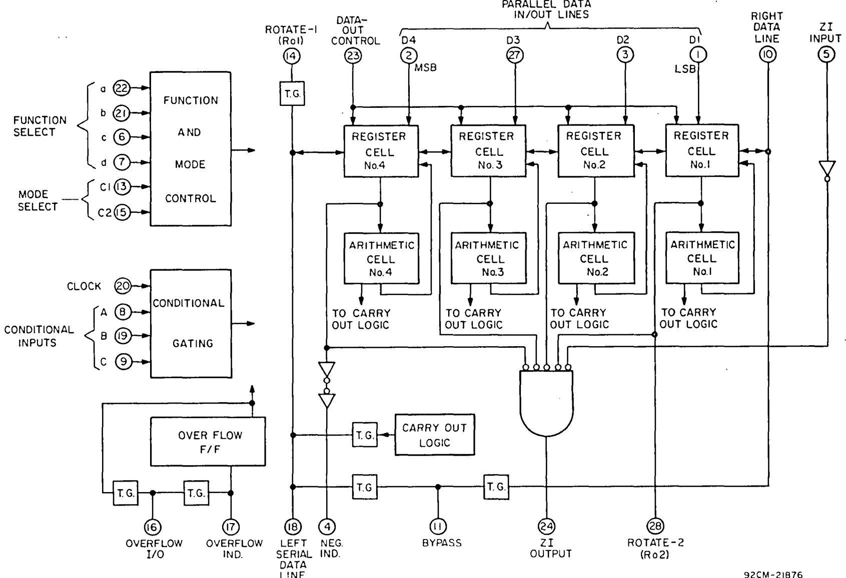


Fig.2 – Simplified logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS							UNITS
		V_O	V_{DD}	−55°C		25°C			125°C		
		Volts	Volts	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device Current	I_L		5	–	3.7	–	0.5	5	–	150	µA
			10	–	7.5●	–	1	10●	–	200●	
Quiescent Device Dissipation/Package	P_D		5	–	–	–	2.5	2.5	–	750	µW
			10	–	–	–	10	100	–	2000	
Output Voltage:[1] Low-Level	V_{OL}		3	–	0.55	–	–	0.5	–	–	V
			5	–	0.01	–	–	0.01	–	0.05	
			10	–	0.01	–	–	0.01	–	0.05	
			15	–	–	–	–	0.5	–	0.55	
High-Level	V_{OH}		3	2.25	–	2.3	–	–	–	–	
			5	4.99	–	4.99	5	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	
			15	–	–	14.5	–	–	14.95	–	
Threshold Voltage[2] N-Channel	V_{THN}	I_D = −20 µA		−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	V_{THP}	I_D = 20 µA		0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1] (All Inputs)	V_{NIL}	0.8	5	1.5●	–	1.5●	2.25	–	1.4●	–	V
		1	10	3●	–	3●	4.5	–	2.9●	–	
	V_{NIH}	4.2	5	1.4●	–	1.5●	2.25	–	1.5●	–	
		9	10	2.9●	–	3●	4.5	–	3●	–	
Output Drive Current[2] Zero Indicator N-Channel	I_DN	0.5	5	0.11	–	0.09●	0.16	–	0.06	–	mA
		0.5	10	0.12	–	0.10●	0.16	–	0.07	–	
P-Channel	I_DP	3	5	−0.04	–	−0.03	−0.06	–	−0.02	–	
		7	10	−0.08	–	−0.07●	−0.13	–	−0.05	–	
Negative Indicator N-Channel	I_DN	0.5	5	0.11	–	0.09	0.30	–	0.06	–	
		0.5	10	0.12	–	0.10●	0.40	–	0.07	–	
P-Channel	I_DP	4.5	5	−0.07	–	−0.06	−0.19	–	−0.04	–	
		9.5	10	−0.12	–	−0.10●	−0.30	–	−0.07	–	
Overflow Indicator N-Channel	I_DN	0.5	5	0.25	–	0.20	0.50	–	0.14	–	
		0.5	10	0.37	–	0.30●	0.90	–	0.21	–	
P-Channel	I_DP	4.5	5	−0.08	–	−0.07	−0.21	–	−0.05	–	
		9.5	10	−0.12	–	−0.10●	−0.38	–	−0.07	–	
All Other Outputs N-Channel	I_DN	0.5	5	0.11	–	0.09	0.10	–	0.06	–	
		0.5	10	0.06	–	0.05●	0.12	–	0.03	–	
P-Channel	I_DP	4.5	5	−0.02	–	−0.02	−0.05	–	−0.01	–	
		9.5	10	−0.06	–	−0.05●	−0.08	–	−0.03	–	
Diode Test[3] 100 µA Test Pin	V_{DF}			–	1.5●	–	–	1.5●	–	1.5●	V

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test,all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS, *at T_A = 25°C and C_L = 15 pF*
Typical Temperature Coefficient at all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS *	V_{DD} Volts	LIMITS CD4057AD, CD4057AK Min.	Typ.	Max.	UNITS
Propagation Delay Time: DATA IN-to-SUM OUT	t_{PLH}, t_{PHL}		5	–	1430	3900	ns
			10	–	375	720	
CARRY IN-to-SUM OUT			5	–	915	2550	
			10	–	310	840	
DATA IN-to-CARRY OUT			5	–	950	2580	
			10	–	265	720	
CARRY IN-to-CARRY OUT			5	–	485	1320	
			10	–	175	480	
ZI Input -to- ZI Output	t_{PLH}		5	–	1980	5400	
			10	–	750	2040	
	t_{PHL}		5	–	265	720	
			10	–	110	300	
Transition Time: ZI Output	t_{TLH}		5	–	3700	10350	ns
			10	–	1650	4500	
	t_{THL}		5	–	420	1140	
			10	–	220	600	
Negative Indicator and Overflow Indicator	t_{TLH}, t_{THL}		5	–	300	825	
			10	–	165	450	
All Other Outputs			5	–	1000	2775	
			10	–	475	1275	
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	400	1200	ns
			10	–	125	375	
Clock Rise and Fall Time	t_rCL, t_fCL		5	–	–	15	μs
			10	–	–	15	
Set Up Time: DATA	t_{SLH}, t_{SHL}		5	–	20	40	ns
			10	–	10	20	
OP CODE			5	–	1675	4590	ns
			10	–	485	1320	
Data Hold Time	t_{Dh}		5	–	20	40	ns
			10	–	10	20	
Maximum Clock Frequency: Count Mode	f_{CL}		5	0.13	0.36	–	MHz
			10	0.46●	1.35	–	
Shift Mode	f_{CL}		5	0.33	0.90	–	
			10	1.4	3.8	–	
Input Capacitance	C_I	ANY INPUT		–	5	–	pF

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

LOGIC DESCRIPTION

OPERATIONAL MODES

The CD4057A arithmetic logic unit operates in one of four possible modes. These modes control the transfer of information, either serial data or arithmetic operation carries, to and from the serial-data lines. Fig. 3 shows the manner in which the four modes control the data on the serial-data lines.

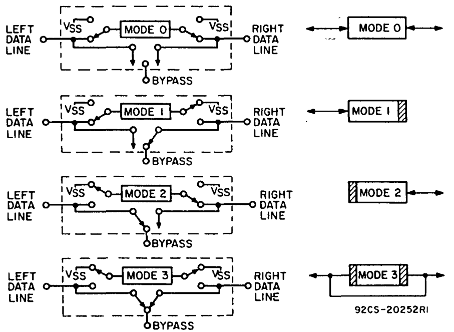


Fig.3 – Schematic of "Mode" concept.

In MODE 0, data can enter or leave from either the left or the right serial-data line.

In MODE 1, data can enter or leave only on the left serial-data line;

In MODE 2, data can enter or leave only on the right serial data line.

In MODE 3, serial data can neither enter nor leave the register, regardless of the nature of the operation. Furthermore, the register is by-passed electrically, i.e., there is an electrical bidirectional path between the right and left serial data terminals.

The two input lines labeled C1 and C2 in the terminal assignment diagram define one of four possible modes shown in Table I.

Through the use of mode control, individual arithmetic arrays can be cascaded to form one large processor or many processors of various lengths.

TABLE I – MODE DEFINITION

C2	C1	MODE
0	0	0
0	1	1
1	0	2
1	1	3

Examples of how one "hard-wired" combination of three ALU's can form (a) a 12-bit parallel processor, (b) one 8-bit and one 4-bit parallel processor, or (c) three 4-bit parallel processors, merely by changes in the modes of each ALU are shown in Fig. 4.

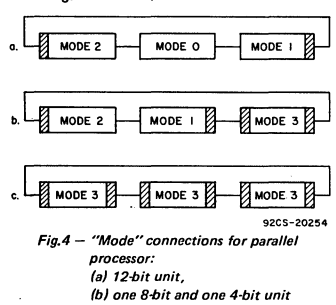


Fig.4 – "Mode" connections for parallel processor:
(a) 12-bit unit,
(b) one 8-bit and one 4-bit unit
(c) three 4-bit units.

Data-flow interruptions are shown by shaded areas. With these three ALU's and the four available modes, 61 more system combinations can be formed. If 4 ALU's are used, 4^4 combinations (256) are possible.

NOTE: The BYPASS terminal of the "most significant" CD4057A is connected to the bypass terminal of the "least significant" CD4057A. The bypass terminals on all other CD4057A's are left floating. This interconnection is performed whenever more than one CD4057A are used to form a processor.

INSTRUCTION REPERTOIRE

Four encoded lines are used to represent 16 instructions. Encoded instructions are as follows:

a b c d	
0 0 0 0	NO-OP (Operational Inhibit)
0 0 0 1	AND
0 0 1 0	Count down
0 0 1 1	Count up
0 1 0 0	Subtract Stored number from zero (SMZ)
0 1 0 1	Subtract from parallel data lines (SM) (stored number from parallel data lines)
0 1 1 0	Add (AD)
0 1 1 1	Subtract (SUB) (Parallel data lines from stored number)
1 0 0 0	Set to all ones (SET)
1 0 0 1	Clear to all zeroes (CLEAR)
1 0 1 0	Exclusive-OR
1 0 1 1	OR
1 1 0 0	Input Data (From parallel data lines)
1 1 0 1	Left shift
1 1 1 0	Right shift
1 1 1 1	Rotate (cycle) right

All instructions ar executed on the positive edge of the clock.

CONDITIONAL OPERATION

Inhibition of the clock pulse can be accomplished with a programmed NO-OP instruction or through conditional input terminals A, B, and C. In a system of many CD4057A's, each CD4057A can be made to automatically control its own operation or the operation of any other CD4057A in the system in conjunction with the Overflow, Zero, or Negative (Number) indicators. Table II, the conditional-inputs truth table, defines the interactions among A, B, and C.

TABLE II – CONDITIONAL-INPUTS TRUTH TABLE

A	B	C	OPERATION PERMITTED
0	X	X	Yes
1	0	0	Yes
1	0	1	No
1	1	0	No
1	1	1	Yes

X = don't care

Two examples of how the conditional operation can be used are as follows:

1) For the Multiplication Algorithm
   - A = 1, for step 7 (1)
   - A = 0, for step 7 (2)
   - B = 1
   - C = negative Indicator
2) For the Division Algorithm
   - A = 1, for step 7 (1)
   - A = 0, for step 7 (2)
   - B = 1
   - C = C_O (left data line)

OVERFLOW DETECTION

The CD4057A is capable of detecting and indicating the presence or absence of an arithmetic two's-complement overflow. A two's-complement overflow is defined as having occurred if the signs of the two initial words are the same and the sign of the result is different while performing a carry-generating instruction.

$$\begin{array}{r} 0.011 \\ \text{For example:} \quad (+)\ \underline{0.110} \\ 1.001 \end{array}$$

Overflows can be detected and indicated only during operation in Mode 2 or Mode 3 and can occur for only four instructions (AD, SMZ, SM, and SUB). If an overflow is detected and stored in the overflow flip-flop, any one of the five instructions AD, SMZ, SM, SUB, or IN can change the overflow indicator.

When any of the three subtraction instructions is used, the sign bit of the data being subtracted is complemented and this value is used as one of the two initial signs to detect overflows. If an overflow has occurred, the final sign of the sum or difference is one's complemented and stored in the most-significant-bit position of the register.

The overflow flip-flop is updated at the same time the new result is stored in the CD4057A. Whenever data on the parallel-data lines are loaded into the CD4057A, whatever is on the Overflow I/0 line is loaded into the overflow flip-flop. Also, whenever data are dumped on the parallel data lines from the CD4057A, the contents of the overflow flip-flop are dumped on the Overflow I/0 line. Thus overflows may be stored elsewhere and then fed into the CD4057A at another time.

OPERATIONAL SEQUENCE AND WAVEFORMS FOR PROPAGATION-DELAY MEASUREMENTS

1. DATA IN-to-CARRY OUT and DATA IN-to-SUM OUT
   - A. Apply Word A and IN instruction
   - B. Apply Clock to load word A into register
   - C. Apply AD instruction
   - D. Apply Word B (data in)
   - E. Apply Clock to load result (sum out)
   - F. Apply DATA OUT CONTROL to look at result

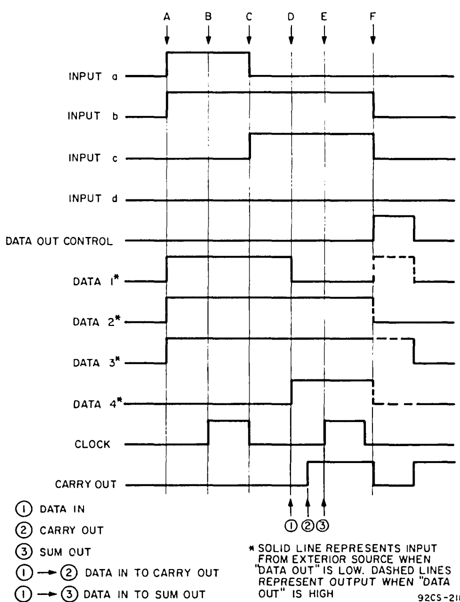


Fig. 5 – DATA IN-to-CARRY OUT and DATA IN-to-SUM OUT.

2. CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT
   A. Apply Word A and IN instruction
   B. Apply Clock to load word A into register
   C. Apply AD instruction
   D. Apply Word B
   E. Apply CARRY IN (carry in)
   F. Apply Clock to load result (sum out)
   G. Apply DATA OUT CONTROL to look at result

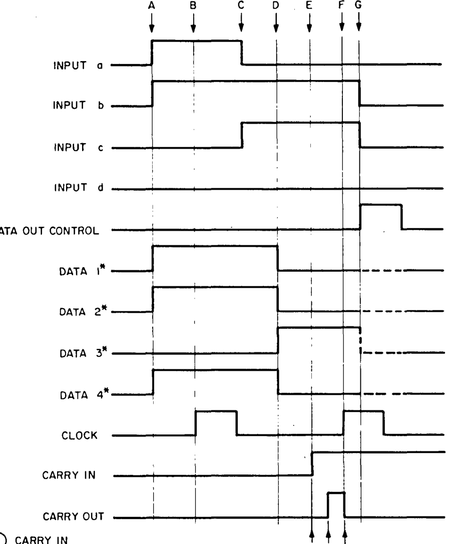


Fig. 6 – CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT.

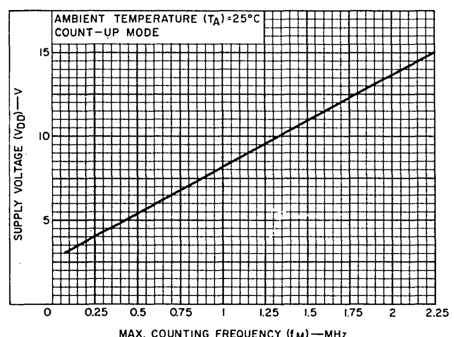


Fig.7 – Max. counting frequency vs. supply voltage for a typical CD4057A.

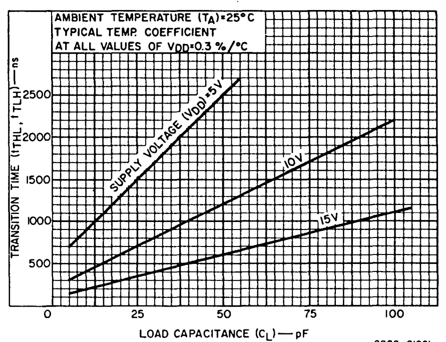


Fig. 8 – Transition time vs. load capacitance for Data Outputs (D1-D4).

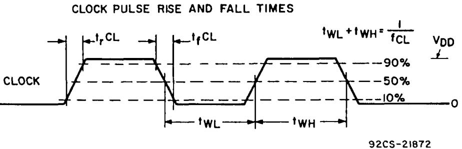


Fig. 9—Clock Pulse Rise and Fall Times.

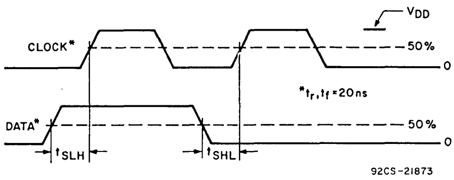


Fig.10 – Data setup time.

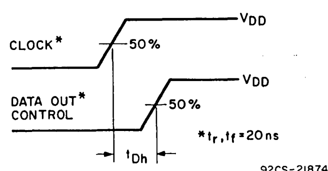


Fig. 11 – Data hold time.

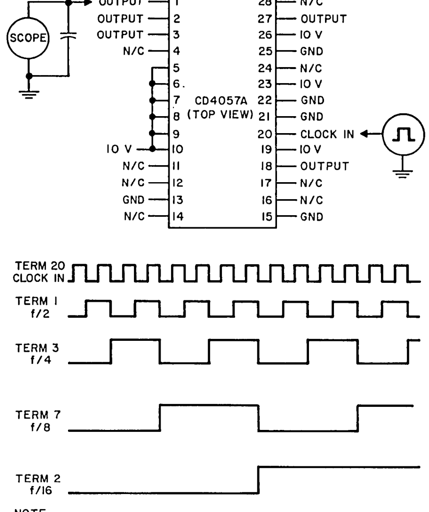


Fig.12 — Dynamic test circuit and waveforms (maximum frequency).

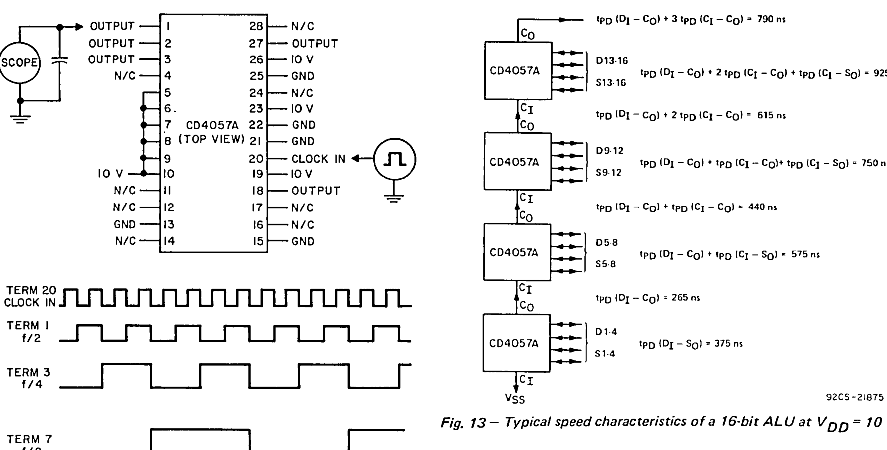


Fig. 13 — Typical speed characteristics of a 16-bit ALU at V_{DD} = 10 V.

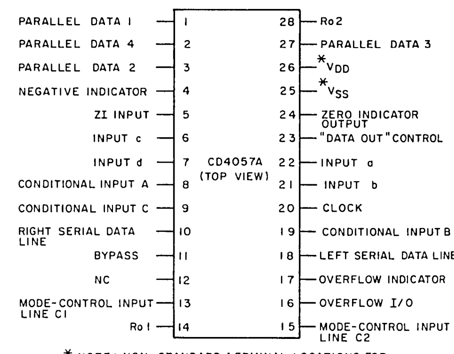


Fig. 14 — Terminal assignments.

TYPICAL APPLICATION

The CD4057A has been designed for use as a parallel processor in flexible, programmable, easily expandable, special or general purpose computers, where minimization of external connections and data busing are primary design goals. The block diagram of Fig. 15 is an example of a computer that processes 8 bits in parallel.

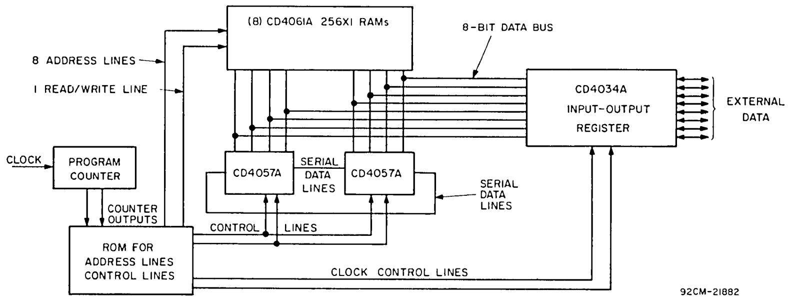


Fig. 15 — Example of Computer Organization Using CD4057A.

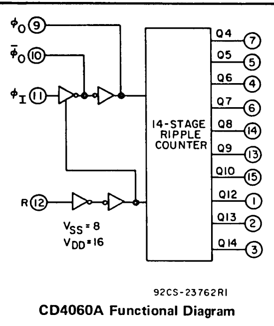
Solid State
Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series

CD4060A/. . .



CD4060A Functional Diagram

High-Reliability COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **4-MHz operating frequency (typ.) at $V_{DD}-V_{SS}$ = 10 V**
- **Common reset**
- **Fully static operation**
- **10 buffered outputs available**

The RCA-CD4060A Slash (/) Series consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\phi_I(\phi_O)$. All inputs and outputs are fully buffered.

These devices are electrically and mechanically identical with standard COS/MOS CD4060A types described in data bulletin 813 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4060A "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4060A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Oscillator Features:

- **All active components on chip**
- **RC or crystal oscillator configuration**

Applications:

- **Timers**
- **Frequency dividers**

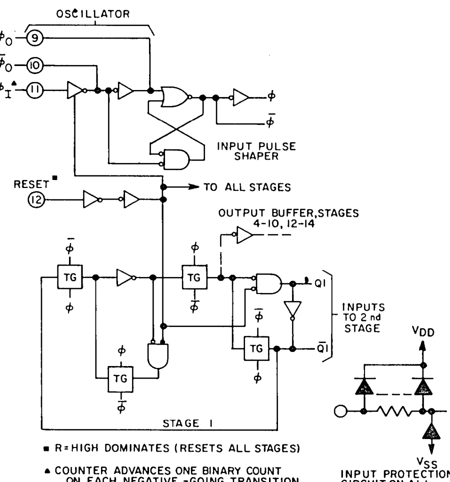


Fig. 1–Logic diagram of CD4060A oscillator, pulse shaper, and 1 of 14 counter stages.

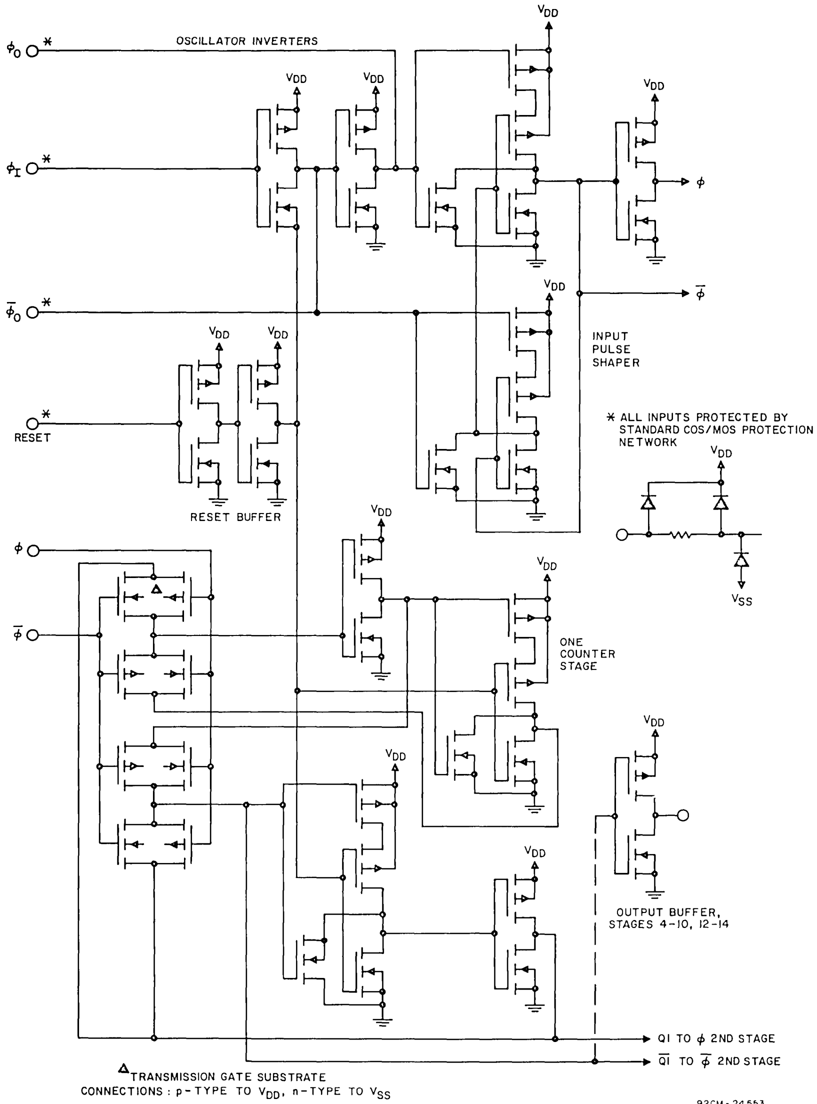


Fig. 2–Schematic diagram of input pulse shapers, reset buffers, and 1 of 14 binary counter stages of the CD4060A.

STATIC ELECTRICAL CHARACTERISTICS (All inputs .... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O V	V_{DD} V	LIMITS −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS
Quiescent Device[1] Current	I_L			5	–	15	–	0.5	15	–	900	μA
				10	–	25●	–	1●	25	–	500●	
Quiescent Device Dissipation/Package	P_D			5	–	75	–	2.5	75	–	4500	μW
				10	–	250	–	10	250	–	15000	
Output Voltage:[1] Low-Level	V_{OL}	Fan Out = 50		3	–	0.55●	–	–	0.5●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	–	0.5●	–	0.55●	
High-Level	V_{OH}	Fan Out = 50		3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4,99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	–	–	14.45●	–	
Threshold Voltage:[2] N-Channel	V_{THN}	I_D = −20 μA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	V_{THP}	I_D = 20 μA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1] (Any Input)	V_{NL}		0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V
			1	10	3●	–	3●	4.5	–	2.9●	–	
	V_{NH}		4.2	5	1.4	–	1.5●	2.25	–	1.5	–	
			9	10	2.9●	–	3●	4.5	–	3●	–	
Output Drive Current[2]:▲ N-Channel (Sink)	I_{DN}		0.5	5	0.22	–	0.18●	0.36	–	0.125	–	mA
			0.5	10	0.44	–	0.36●	0.75	–	0.25	–	
P-Channel (Source)	I_{DP}		4.5	5	−0.15	–	−0.125●	−0.25	–	−0.085	–	mA
			9.5	10	−0.3	–	−0.25●	−0.5	–	−0.175	–	
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I	Any Input			–	–	–	±10−5	±1	–	–	μA

▲ Data does not apply to terminals 9 or 10.

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test,all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, C_L = 15 pF (unless otherwise specified), Input t_r,t_f = 20 ns

CHARACTERISTIC	SYMBOL	TEST CONDITIONS*		LIMITS			UNITS
			V_{DD}	MIN.	TYP.	MAX.	
Input-Pulse Operation							
Propagation Delay Time ϕ_I to Q4 Out	t_{PHL}, t_{PLH}		5	–	900	1800●	ns
			10	–	450	900●	
Propagation Delay Time, Q_n to Q_{n+1}	t_{PHL}, t_{PLH}		5	–	450	900●	ns
			10	–	225	450●	
Transition Time	t_{THL}, t_{TLH}		5	–	150	300●	ns
			10	–	75	150●	
Min. Input-Pulse Width	t_{WL}, t_{WH}	f = 100 kHz	5	–	200	400	ns
			10	–	75	110	
Input-Pulse Rise & Fall Time	$t_{r\phi}$, $t_{f\phi}$		5	–	–	15	μs
			10	–	–	7.5	
Max. Input-Pulse Frequency	f_ϕ		5	1●	1.75	–	MHz
			10	3●	4	–	
Input Capacitance	I_I			–	5	–	pF
Reset Operation							
Propagation Delay Time	t_{PHL}		5	–	500	1000●	ns
			10	–	250	500●	
Minimum Reset Pulse Width	t_{WH}		5	–	500	1000●	ns
			10	–	250	500●	

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE .... –65 to +150°C
OPERATING-TEMPERATURE RANGE .... –55 to +125°C
DC SUPPLY-VOLTAGE RANGE:
(V_{DD}–V_{SS}) .... –0.5 to +15 V
DEVICE DISSIPATION (PER PACKAGE) .... 200 mW
ALL INPUTS .... $V_{SS} \leq V_I \leq V_{DD}$

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. .... 265°C
RECOMMENDED OPERATING CONDITIONS:
DC Supply-Voltage Range
(V_{DD}–V_{SS}) .... 3 to 15 V
Input Voltage Swing .... V_{SS} to V_{DD}

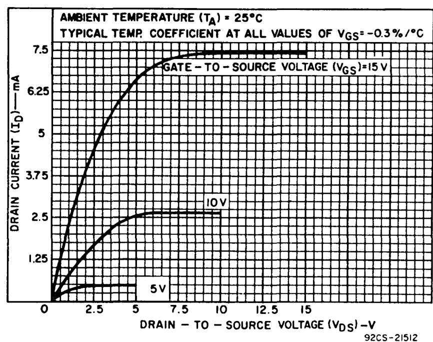


Fig. 3—Minimum n-channel drain characteristics.

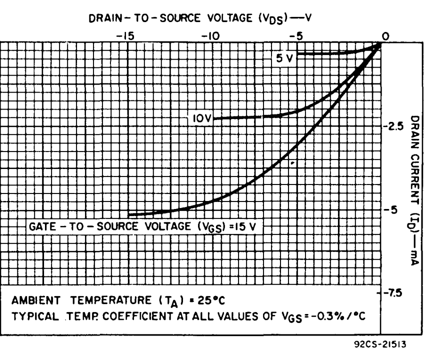


Fig.4—Minimum p-channel drain characteristics.

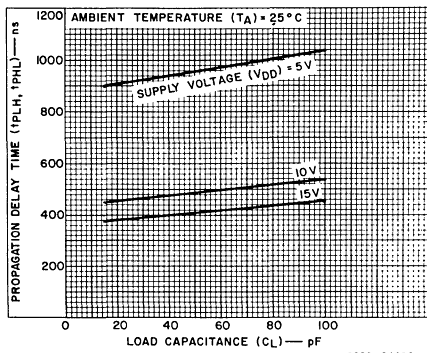


Fig. 5—Typical propagation delay time vs. load capacitance (ϕ_I to Q4 output).

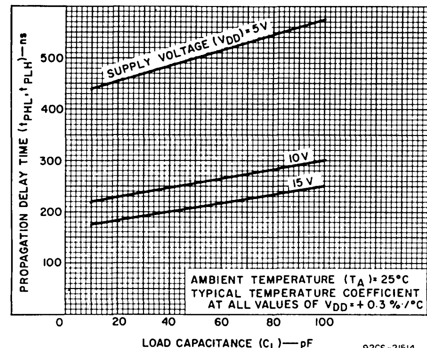


Fig. 6—Typical propagation delay time vs. load capacitance (Q_n to Q_{n+1}).

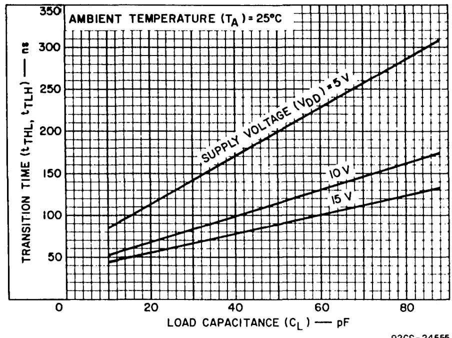


Fig. 7—Typical output transition time vs. load capacitance.

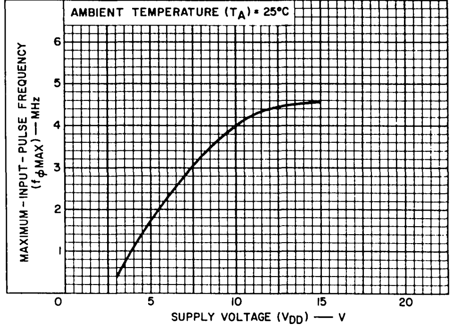


Fig. 8—Typical maximum-input-pulse frequency vs. supply voltage.

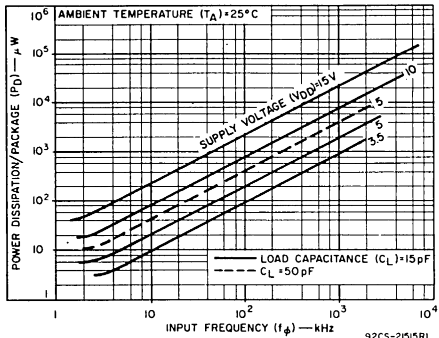


Fig. 9 — Typical dynamic power dissipation characteristics.

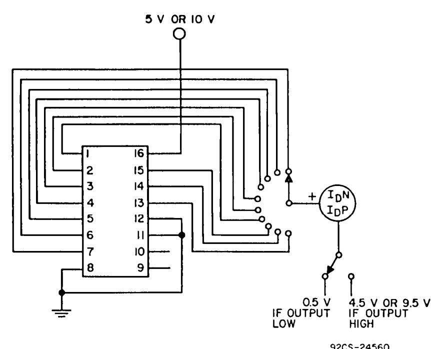


Fig. 10 — Output drive current test circuit.

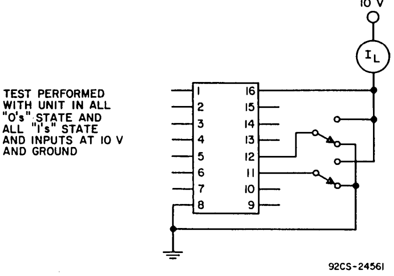


Fig. 11 — Quiescent device current test circuit.

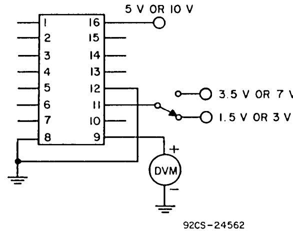


Fig. 12 — Input-pulse noise immunity test circuit.

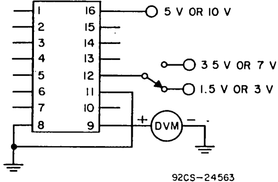
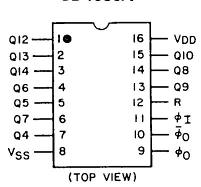


Fig. 13 — Reset-pulse noise immunity test circuit.

TERMINAL ASSIGNMENT CD4060A



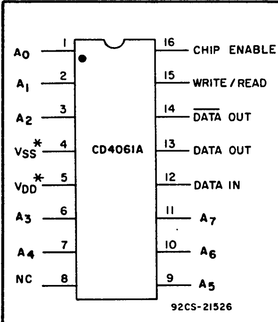
Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series

CD4061A/. . .



High-Reliability COS/MOS 256-Word by 1-Bit Static Random-Access Memory

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- Low standby power: 10 Nanowatts/bit (typ.) @ V_{DD} = 10 V
- Access time: 380 ns (max.) @ V_{DD} = 10 V
- Noise immunity: 45% of V_{DD} (typ.)
- Single 3-to-15 V power supply
- Fully decoded addressing
- COS/MOS input/output logic compatibility
- Single write/read control line
- TTL output drive capability
- Three-state data outputs for bus-oriented systems
- 1101-type pin designations*
- Separate data output and data input lines

The RCA-CD4061A "Slash" (/) Series are single monolithic integrated circuits containing a 256-word by 1-bit fully static, random-access, NDRO memory. The memory is fully decoded and requires 8 address input lines (A_0 – A_7) to select one of 256 storage locations. Additional connections are provided for a WRITE/READ command CHIP ENABLE, DATA IN, and DATA OUT and $\overline{\text{DATA}}$ OUT lines.

To perform READ and WRITE operations the CHIP-ENABLE signal must be low. When the CHIP-ENABLE signal is high, read and write operations are inhibited and the output is a high impedance. To change addresses, the CHIP-ENABLE signal must be returned to a high level, regardless of the logic level of the WRITE/READ input. In a multiple package application, the CHIP-ENABLE signal may be used to permit the selection of individual packages.

Output-voltage levels appear on the outputs only when the CHIP-ENABLE and WRITE/READ signals are both low. Separate data inputs and outputs are provided; they may be tied together; or, to eliminate interaction between READ and WRITE functions, may be used separately. The circuit arrangement permits the outputs from many arrays to be tied to a common bus.

All input and output lines are buffered. The CD4061A output buffers are capable of direct interfacing with TTL devices.

These devices are electrically and mechanically identical with standard COS/MOS CD4061A types described in data bulletin 768 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to five screening levels /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to two screening levels – /M and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4061A "Slash" (/) Series types are supplied in 16-lead dual-in-line side-brazed ceramic packages ("D" suffix) or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE	–65 to +150 °C
OPERATING-TEMPERATURE RANGE	–55 to +125 °C
DC SUPPLY-VOLTAGE RANGE ($V_{DD} - V_{SS}$)	–0.5 to +15 V
DEVICE DISSIPATION (PER PKG.)	200 mW
ALL INPUTS	$V_{SS} \leq V_I \leq V_{DD}$
RECOMMENDED DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$)	3 to 15 V
LEAD TEMPERATURE (DURING SOLDERING) At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	265 °C

* The pin designations are compatible with other static 256-Bit memories and are, therefore, not compatible with standard COS/MOS CD4000A-series devices; i.e. V_{DD} is pin 5 and V_{SS} is pin 4.

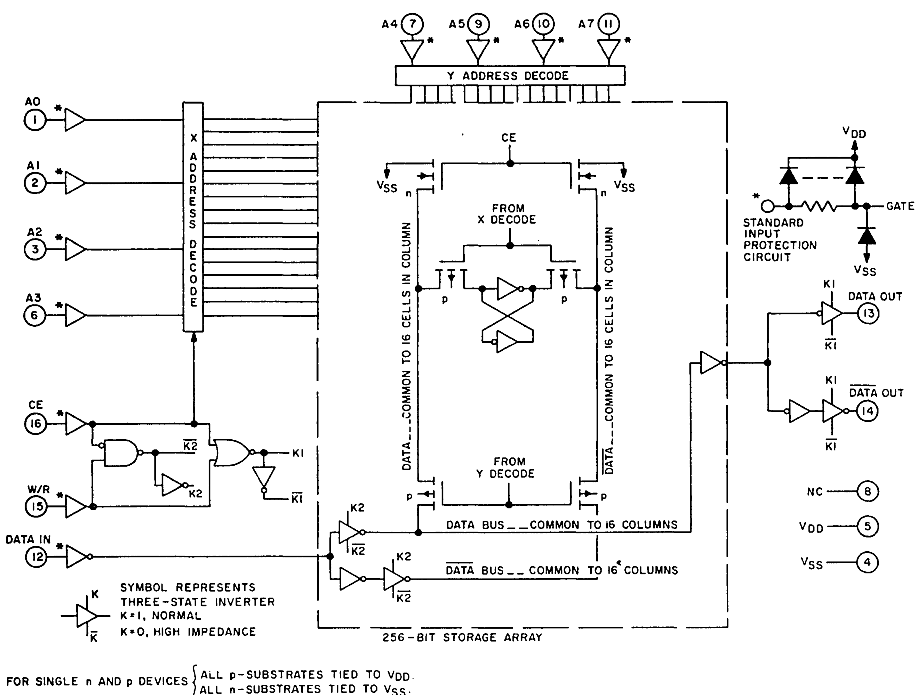


Fig. 1 — CD4061A logic diagram.

CD4061A OPERATIONAL MODES

OPERATION	ADDRESS LINES	CHIP-ENABLE	WRITE/READ	DATA IN	DATA OUTPUTS
Write "0"	Stable	0	1	0	High-Impedance
Write "1"	Stable	0	1	1	High-Impedance
Read	Stable	0	0	X	Valid 1 or 0
*Read/Write	Stable	0	0/1	X	Valid 1 or 0/High-Impedance
Address Change	Changing	1	X	X	High-Impedance

X = Don't Care

* For a READ/WRITE operation on the same address, chip-enable may be held to a logic 0 for both successive operations.

STATIC ELECTRICAL CHARACTERISTICS (All inputs .... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS							UNITS
		V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	
Quiescent Device Current[1]	I_L		5	–	5	–	0.12	5	–	150	µA
			10	–	10●	–	0.25	10●	–	200●	
Quiescent Device Dissipation/Package	P_D		5	–	–	–	0.6	25	–	750	µW
			10	–	–	–	2.5	100	–	2000	
Output Voltage[5,6] Low-Level	V_{OL}		3	–	0.55●	–	–	0.5●	–	–	V
			5	–	0.01	–	0	0.01	–	0.05	
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}		3	2.25●	–	2.3●	–	–	–	–	
			5	4.99	–	4.99	5	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	
			15	–	–	14.5●	–	–	14.45●	–	
Threshold Voltage[2] N-Channel	$V_{TH}N$	I_D = −20 µA		−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	$V_{TH}P$	I_D = 20 µA		0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[3] (All Inputs)	V_{NL}	0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V
		1	10	3●	–	3●	4.5	–	2.9●	–	
	V_{NH}	4.2	5	1.4	–	1.5●	2.25	–	1.5	–	
		9	10	2.9●	–	3●	4.5	–	3●	–	
Output Drive Current:[4] (Data Out, $\overline{\text{Data}}$ Out) N-Channel (Sink)	I_DN	0.4	4.5	2	–	1.6●	2.5	–	1.1	–	mA
		0.5	10	4.3	–	3.5●	5	–	2.4	–	
P-Channel (Source)	I_DP	2.5	5	−1.1	–	−0.9●	−1.8	–	−0.65	–	mA
		4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
		9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
Output Off Resistance[4] (High-Impedance State)	R_o(Off)		5	10	–	10●	–	–	10	–	MΩ
			10	10	–	10●	–	–	10	–	
Diode Test[3] 100 µA Test Pin	V_{DF}			–	1.5●	–	–	1.5●	–	1.5●	V

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Functional test, all inputs and outputs.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

Note 4: Tests on all outputs.

Note 5: Functional GAL PAT test for 5 volts at 800 kHz and 10 volts at 2 MHz.

Note 6: Functional MARCH test for 3 volts at 250 kHz and 15 volts at 2 MHz.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $V_{SS} = 0$ V, $C_L = 50$ pF, and t_r, $t_f = 20$ ns

	CHARACTERISTICS	SYMBOLS	TEST CONDITIONS▲ V_{DD} (Volts)	LIMITS Min.*	Typ.	Max.*	UNITS
READ CYCLE	Read Cycle Time	t_{RC}	5	1200 ●	1000	–	ns
			10	550 ●	450	–	
	Chip-Enable Hold Time	t_{CEH}	5	40 ●	0	–	ns
			10	0 ●	–	–	
	Chip-Enable Pulse Width	t_{CE}	5	700 ●	500	–	ns
			10	350 ●	250	–	
	Chip-Enable Setup Time	t_{CES}	5	460 ●	–	–	ns
			10	200 ●	–	–	
	Read Access Time	t_{RA}	5	–	450	750 ●	ns
			10	–	250	380 ●	
WRITE CYCLE	Write Cycle Time	t_{WC}	5	1200 ●	1000	–	ns
			10	550 ●	450	–	
	Chip-Enable Hold Time	t_{CEH}	5	40 ●	0	–	
			10	0 ●	–	–	
	Chip-Enable Pulse Width	t_{CE}	5	700 ●	500	–	
			10	350 ●	250	–	
	Chip-Enable Setup Time	t_{CES}	5	460 ●	–	–	
			10	200 ●	–	–	
	Write Hold Time	t_{WH}	5	150 ●	100	–	
			10	100 ●	70	–	
	Write Pulse Width	t_W	5	150 ●	100	–	
			10	100 ●	70	–	
	Data Setup Time	t_{DS}	5	140 ●	80	–	
			10	80 ●	35	–	
	Data Hold Time	t_{DH}	5	25 ●	10	–	
			10	20 ●	10	–	
	Output Transition Time	t_{TLH}	5	–	60	100	ns
			10	–	50	75	
		t_{THL}	5	–	35	60	
			10	–	25	40	
	Chip-Enable Input Rise and Fall Time	t_{rCE}, t_{fCE}	5	–	–	15	μs
			10	–	–	5	
			15	–	–	1	

* See "Symbol Definitions"

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

▲ Tests are on all inputs and outputs.

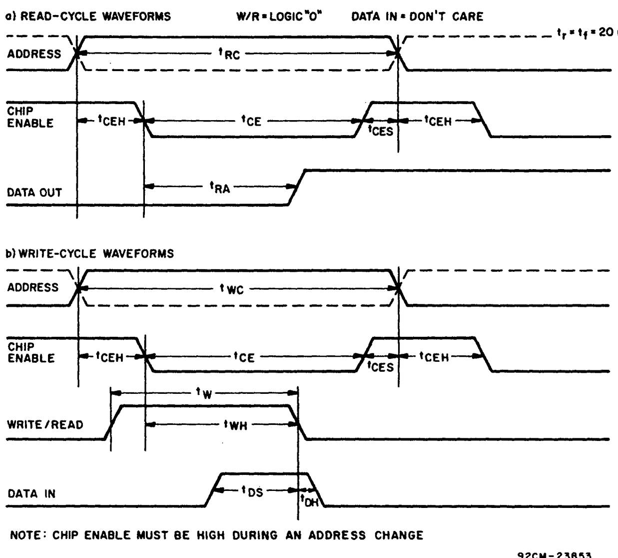


Fig. 2 – Typical write-read waveforms.

SYMBOL DEFINITIONS

READ CYCLE

t_{RC} – READ CYCLE TIME – Time required between address changes during a read cycle. Minimum read cycle time is equal to t_{CEH} (min.) + t_{CE} (min.) + t_{CES} (min.). (See Definitions below).

t_{CEH} – CHIP-ENABLE HOLD TIME – Time required before chip-enable level can be lowered after an address transition.

t_{CE} – CHIP-ENABLE PULSE WIDTH – Time required for the chip to be active for valid reading of output data.

t_{CES} – CHIP-ENABLE SETUP TIME – Time required before ar address transition can take place after chip-enable level has been increased. t_{CES}(min.) + t_{CEH}(min.) is the minimum time required to discharge internal nodes and allow settling of address decoders during an address transition. Chip-enable level must be raised during each address change, even if read cycles only or write cycles only are successively performed. However, if address is not changed, chip enable may remain in its active (low) state during successive read and write cycles.

t_{RA} – READ ACCESS TIME – Measured from chip-enable transition; time before output data is valid.

WRITE CYCLE

t_{WC} – WRITE CYCLE TIME – Time required between address changes during a write cycle. This time sets the maximum operating frequency for the memory, with minimum write cycle time equal to t_{CEH} (min.) + t_{CE} (min.) + t_{CES} (min.).

t_{CEH} – CHIP-ENABLE HOLD TIME – See Definition under read cycle.

t_{CE} – CHIP-ENABLE PULSE WIDTH – See Definition under read cycle.

t_{CES} – CHIP-ENABLE SETUP TIME – See Definition under read read cycle.

t_{WH} – WRITE HOLD TIME – Measured from chip-enable transition; time required before negative transition of write pulse can occur for successful write operation.

t_W – WRITE PULSE WIDTH – Time required for W/R pulse to be high. Note that no specification for positive transition of this pulse is made – it may occur before or after the chip-enable transition. In many applications, the W/R control is normally low and is strobed high during a write cycle.

t_{DS} – DATA SETUP TIME – Measured from write-pulse negative transition; time required for data input to be valid.

t_{DH} – DATA HOLD TIME – Measured from write-pulse negative transition; time required for data input to be valid after W/R is returned to a low level. The minimum data pulse width is equal to t_{DS} (min.) + t_{DH} (min.).

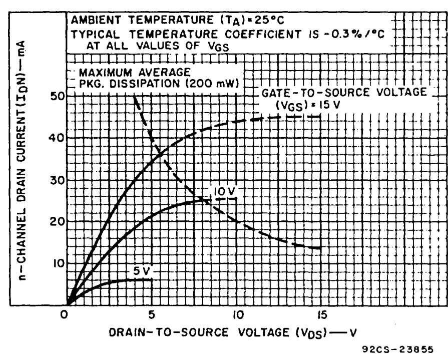
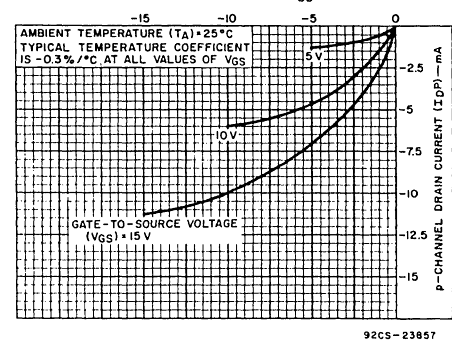


Fig. 3 — Minimum n-channel drain characteristics.



Figl 4 — Minimum p-channel drain characteristics.

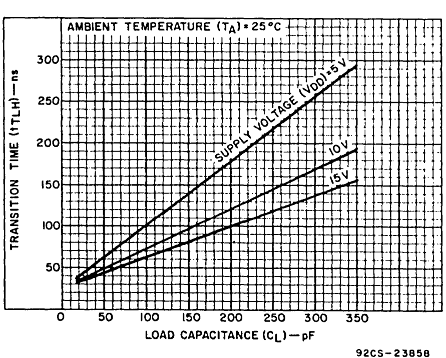


Fig. 5 — Typical low-to-high transition time (t_{TLH}) vs C_L.

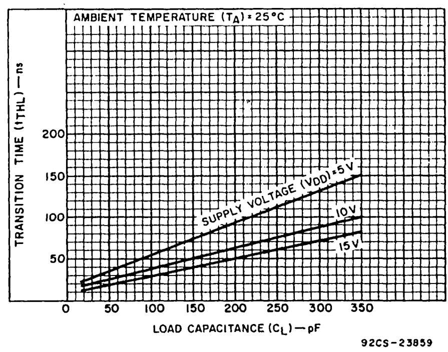


Fig. 6 — Typical high-to-low transition time (t_{THL}) vs C_L.

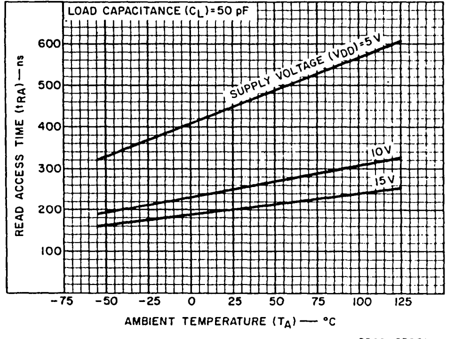


Fig. 7 — Typical read access time (t_{RA}) vs temperature.

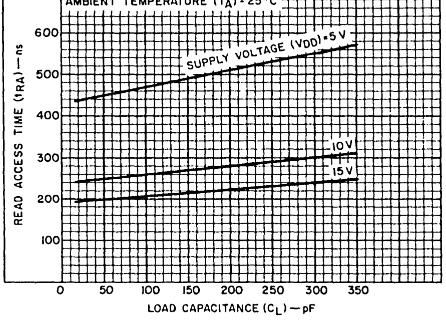


Fig. 8 — Typical read access time (t_{RA}) vs C_L.

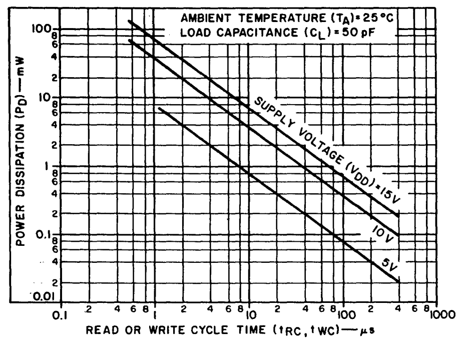


Fig. 9 — Typical power dissipation vs cycle time.

Note:

Power dissipation measured using random data pattern. Input pulse delays and widths set to minimum values specified on data sheet with the exception of cycle time, 15 V setups identical to 10 V data sheet values, with the exception of t_{CE} = 400 ns.

TEST CIRCUITS

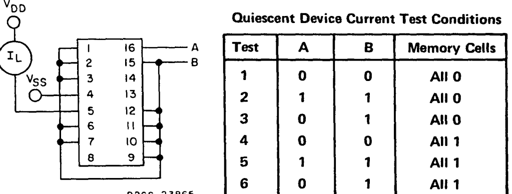
A0 — 1, A1 — 2, A2 — 3, A3 — 4, V_{DD} — 5, V_{SS} — 6, A4 — 7, 8
16 — CE, 15 — W/R, 14 — $\overline{DO}$, 13 — DO, 12 — DI, 11 — A7, 10 — A6, 9 — A5

92CS-23868

Description of Test:

Functional test run with random data input. All inputs toggle betweem 30% and 70% of V_{DD}.

Fig. 10 — Noise immunity.



Quiescent Device Current Test Conditions

Test	A	B	Memory Cells
1	0	0	All 0
2	1	1	All 0
3	0	1	All 0
4	0	0	All 1
5	1	1	All 1
6	0	1	All 1

Fig. 11 — Quiescent device current.

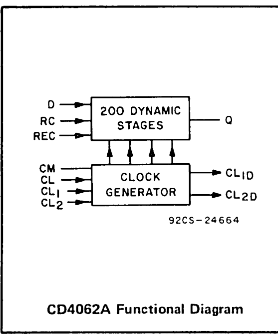
Solid State
Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4062A/ . . .



CD4062A Functional Diagram

High-Reliability COS/MOS 200-Stage Dynamic Shift Register

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Applications:

- **Serial shift registers** ▪ **CRT refresh memory** ▪ **Time-delay circuits** ▪ **Long serial memory**

Special Features:

- **Operation from a single 3-V to 15-V positive or negative power supply**
- **Minimum shift rates over full temperature range —**
  Single phase clock: $3\ V \leq V_{DD} \leq 10\ V$; $f_{min} = 10$ kHz; $-55°C \leq T_A \leq +125°C$ ($f_{min} = 1$ kHz up to $T_A \leq 75°C$)
  Two-phase clock: $3\ V \leq V_{DD} \leq 15\ V$; $f_{min} = 10$ kHz; $-55°C \leq T_A$ $+125°C$ ($f_{min} = 1$ kHz up to $T_A \leq 75°C$)
- **Low power dissipation**
  0.3 mW/bit at 1 MHz and 10 V
  0.04 mW/bit at 0.5 MHz and 5 V
  (alternating 1-0 data pattern)
- **Data output TTL-DTL compatible**
- **Recirculating capability**
- **Delayed two-phase clock outputs available for cascading registers**
- **Asynchronous ripple-type presettable to all 1's or 0's**
- **Ultra-low-power-dissipation standby operation**

The RCA-CD4062A Slash (/) Series is a 200-stage dynamic shift register with provision for either single- or two-phase clock input signals. Single-phase-clocked operation is intended for low-power low clock-line capacitance requirements. Single-phase clocking is specified for medium-speed operation (< 1 MHz) at supply voltages up to 10 volts. Clock input capacitance is extremely low (< 5 pF), and clock rise and fall times are non-critical. The clock-mode signal (CM) must be low for single-phase operation.

Two-phase clock-input signals may be used for high-speed operation (up to 5 MHz) or to further reduce clock rise and fall time requirements at low speeds. Two-phase operation is specified for supply voltages up to 15 volts. Clock input capacitance is only 50 pF/phase. The clock-mode signal (CM) must be high for two-phase operation. The single-phase-clock input has an internal pull-down device which is activated when CM is high and may be left unconnected in two-phase operation.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition for single-phase operation, and at the positive-going transition of CL_1 for two-phase operation.

These devices are electrically and mechanically identical with standard COS/MOS CD4062A types described in data bulletin 816 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4062A "Slash" (/) Series can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4062A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE .... −65 to +150°C
OPERATING-TEMPERATURE RANGE .... −55 to +125°C
DC SUPPLY-VOLTAGE RANGE ($V_{DD}-V_{SS}$) ...... −0.5 to +15 V
DEVICE DISSIPATION (PER PACKAGE) .... 200 mW
ALL INPUTS .... $V_{SS} \leq V_I \leq V_{DD}$
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 MM) FROM CASE FOR 10 S MAX. .... 265°C

RECOMMENDED OPERATING CONDITIONS

DC SUPPLY VOLTAGE ($V_{DD}-V_{SS}$): SINGLE-PHASE CLOCK 3 to 10 V
TWO-PHASE CLOCK 3 to 15 V
INPUT VOLTAGE SWING .... V_{DD} to V_{SS}

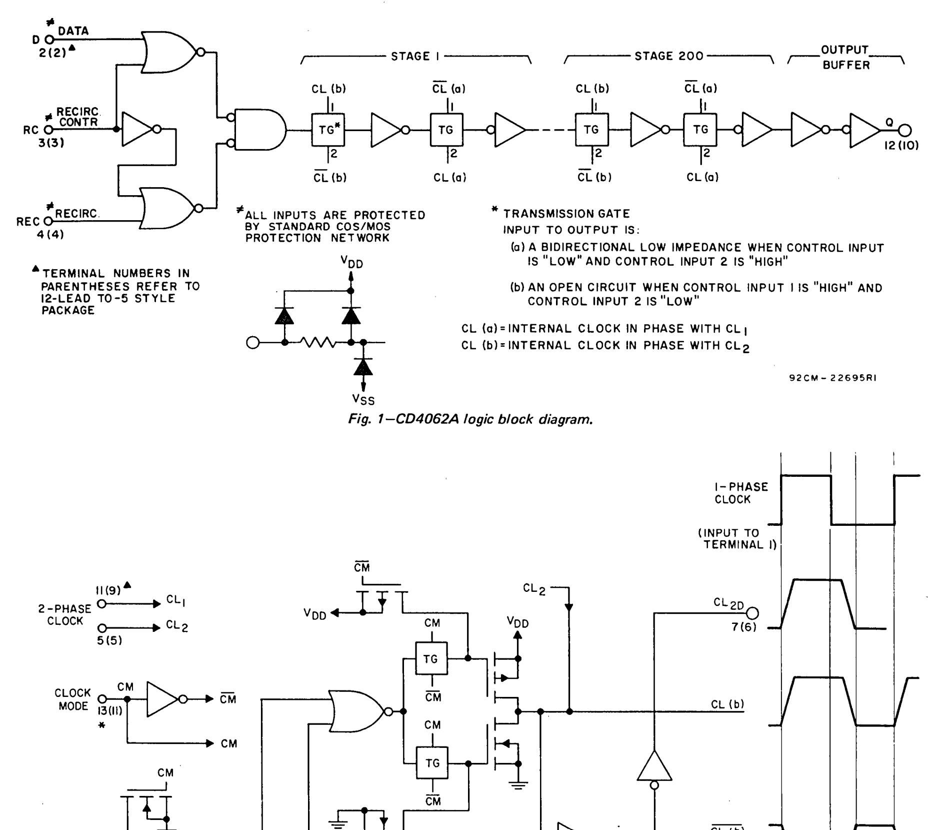


Fig. 1—CD4062A logic block diagram.

Fig. 2—Clock circuit logic diagram.

STATIC ELECTRICAL CHARACTERISTICS, All Inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . . . . 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS							UNITS
			V_O	V_{DD}	−55°C		25°C			125°C		
			V	V	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device[1] Current	I_L	CM=High, CL_1=High, CL_2=Low		5	–	12	–	0.5	12	–	720	µA
				10	–	25●	–	1	25●	–	500●	
Quiescent Device Dissipation/Package	P_D	CM=High, CL_1=High, CL_2=Low		5	–	60	–	2.5	60	–	3600	µW
				10	–	250	–	10	250	–	5000	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●			V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				12	–	–	–	–	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				12	–	–	11.5●	–	–	11.55●	–	
Threshold Voltage[2] N-Channel	$V_{TH}N$	I_D = −20 µA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	$V_{TH}P$	I_D = 20 µA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1] (Any Input)	V_{NL}		0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V
			1.0	10	3●	–	3●	4.5	–	2.9●	–	
	V_{NH}		4.2	5	1.4	–	1.5	2.25	–	1.5	–	
			9.0	10	2.9●	–	3●	4.5	–	3●	–	
Output Drive Current:[2] N-Channel (Sink)	I_DN	Q Output	0.4	4.5	1.6	–	1.3●	2.6	–	0.91	–	mA
			0.5	10	5	–	4	8*	–	3.2	–	
		CL_{1D}, CL_{2D}	0.5	5	0.87	–	0.7●	1.4	–	0.49	–	
			0.5	10	2.2	–	1.8●	3.6	–	1.26	–	
P-Channel (Source)	I_DP	Q Output	4.5	5	−0.31	–	−0.25●	−0.5	–	−0.17	–	mA
			2.5	5	−0.93	–	−0.75	−1.5	–	−0.52	–	
			9.5	10	−0.87	–	−0.7●	−1.4	–	−0.49	–	
		CL_{1D}, CL_{2D}	4.5	5	−0.43	–	−0.35●	−0.7	–	−0.24	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.63	–	
Diode Test[3] 100 µA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I	Any Input	–	–	–	–	–	10	–	–	–	pA

* Maximum power dissipation rating ≤200 mW.

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test,all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC CHARACTERISTICS AT T_A = 25°C, V_{SS} = 0 V, C_L = 50 pF, Input t_r, t_f = 20 ns, except t_rCL and t_fCL

Single-Phase-Clock Operation; Clock Mode (CM) = Low; 3 V ≤ V_{DD} ≤ 10 V (See Figure 3)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS			UNITS	FIG. NO.
			V_{DD} V	MIN.	TYP.	MAX.		
Maximum Clock Frequency [1] (50% Duty Cycle)	f_{CL}	t_r, t_f=20 ns	5	0.5	1●	–	MHz	–
			10	1	2	–		
Minimum Clock Frequency [1] (50% Duty Cycle)	f_{CL}		5	150	10	–	Hz	18
			10	1000●	10	–		
Clock Rise and Fall Times** [1]	t_rCL, t_fCL		5	–	–	10	μs	–
			10	–	–	1●		
Average Input Capacitance All Inputs Except CL_1 and CL_2	C_I			–	5	–	pF	–
Propagation Delays: [1] CL to Q	t_{PLH}, t_{PHL}		5	–	1000	2000	ns	–
			10	–	400	800●		
CL to CL_{1D} (Positive Going)	t_{PLH}	(50% Points)	5	–	750	1500	ns	–
			10	–	300	600		
CL to CL_{2D} (Positive Going)		(50% Points)	5	–	500	1000		
			10	–	200	400		
CL to CL_{1D} (Negative Going)	t_{PHL}	(50% Points)	5	–	450	900		
			10	–	175	350		
CL to CL_{2D} (Negative Going)		(50% Points)	5	–	750	1500		
			10	–	300	600		
Transition Time: [1] Q Output	t_{TLH}, t_{THL}		5	–	100	200	ns	–
			10	–	50	100●		
CL_{1D}, CL_{2D}			5	–	200	400		
			10	–	100	200●		
Data Set-Up Time	t_{SU}		5	0	–	–	ns	–
			10	0	–	–		
▲Data Hold Time	t_{HOLD}		5	150	–	–	ns	–
			10	50	–	–		

** If more than one unit is cascaded in single-phase parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF, and the transition time of the output driving stage. (See Figs. 5 and 7 for cascading options.)

▲ Use of delayed clock permits high-speed logic to precede CD4062A register (see cascade register operation).

NOTE: Test is either several inputs or several outputs.

Two-Phase Clock Operation (CL_1, CL_2); Clock Mode (CM) = High; 3 V ⩽ V_{DD} ⩽ 15 V. See Figure 4.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{DD} V	LIMITS MIN.	TYP.	MAX.	UNITS	FIG. NO.
Maximum Clock Frequency	f_{CL}	5	1.25	2.5	–	MHz	–
		10	2.5	5	–		
Minimum Clock Frequency	f_{CL}	5	150	10	–	Hz	–
		10	150	10	–		
Clock Overlap Time (CL2: 90%, –90%; CL1: 10%, 10%; td1, td2)			40	–	–	ns	–
Average Input Capacitance CL_1, CL_2	C_I		–	50	–	pF	–
Propagation Delays CL_1 to Q	t_{PHL}, t_{PLH}	5	–	250	500	ns	–
		10	–	100	200		
CL_1 to CL_{1D}, CL_2 to CL_{2D}		5	–	250	500		
		10	–	100	200		
Data Set-Up Time (CL2, D)	t_{SU}	5	300	150	–	ns	–
		10	100	50			
Data Hold Time (CL2)	t_{HOLD}	5	0	–	–	ns	–
		10	0	–	–		
Clock Rise and Fall Times	t_rCL_1, CL_2; t_fCL_1, CL_2		No Restrictions If Clock Overlap Requirement Is Met				

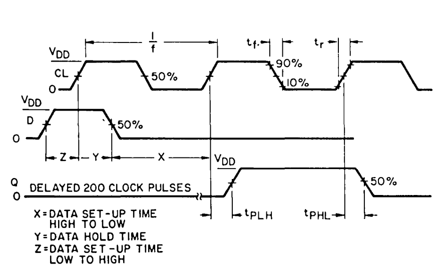


Fig. 3—Timing diagram—single-phase clock.

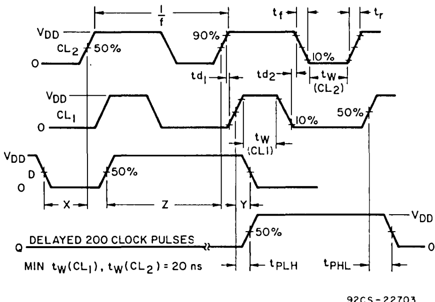


Fig. 4—Timing diagram—two-phase clock.

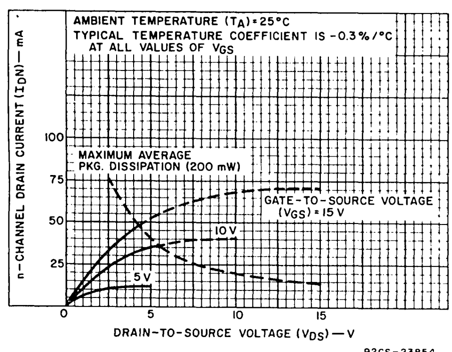


Fig. 5 — Typical n-channel drain characteristics for Q output.

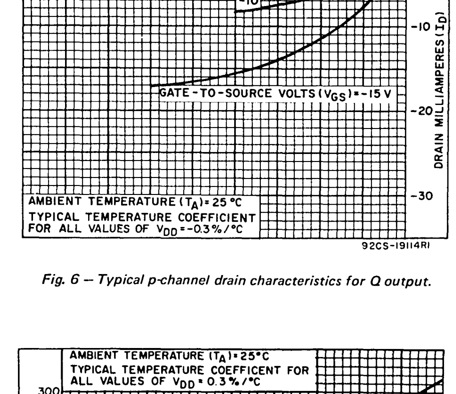


Fig. 6 — Typical p-channel drain characteristics for Q output.

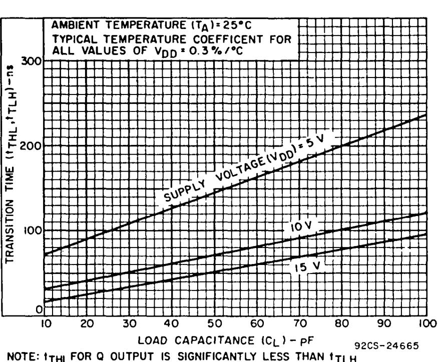


Fig. 7 — Typical transition time vs. C_L for data outputs.

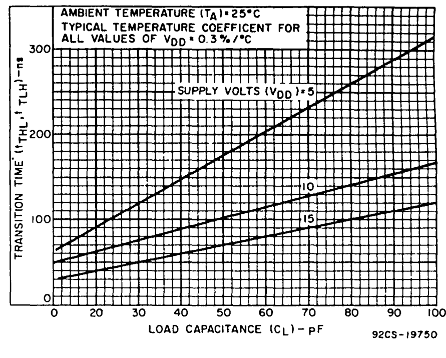


Fig. 8 — Typical transition time vs. C_L for delayed clock output.

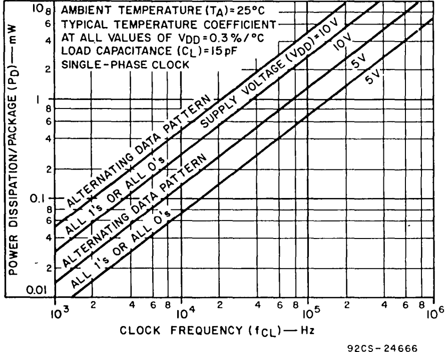


Fig. 9 — Typical power dissipation vs. frequency.

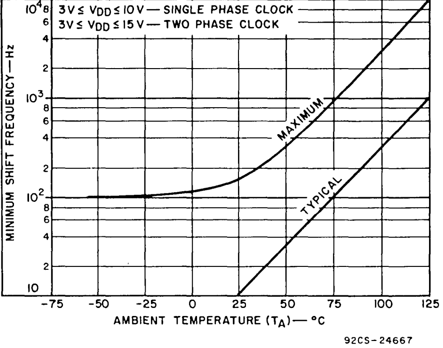


Fig. 10 — Minimum shift frequency vs. ambient temperature.

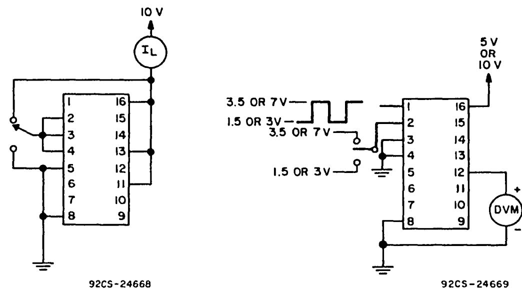


Fig. 11 – Quiescent device current.

Fig. 12 – Noise immunity.

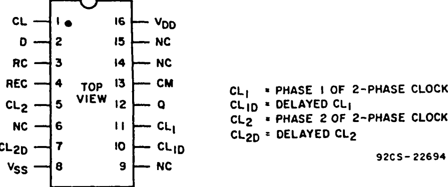
CD4062AT TERMINAL DIAGRAM

V_{DD}, CL, CM, D, Q, RC, CL_1, REC, CL_{1D}, CL_2, V_{SS}, CL_{2D}

TOP VIEW

92CS-22693

CD4062AK TERMINAL DIAGRAM



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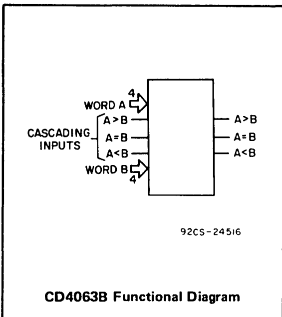
High-Reliability Slash (/) Series

CD4063B/. . .



CD4063B Functional Diagram

High-Reliability COS/MOS 4-Bit Magnitude Comparator

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Standard B-series output drive**
- **Expansion to 8, 16 . . . 4N bits by cascading units**
- **Medium-speed operation: compares two 4-bit words in 250 ns (typ.) at 10 V**

Applications:

- **Servo motor controls**
- **Process controllers**

The RCA-CD4063B Slash (/) Series types are low-power 4-bit magnitude comparators designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 . . .4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

All outputs have equal source- and sink-current capabilities and conform to standard B-series output drive (see Static Electrical Characteristics).

These devices are electrically and mechanically identical with standard COS/MOS CD4063B types described in data bulletin 805 and DATABOOK SSD-203 Series, but are specially pro-

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3 > B3	X	X	X	X	X	X	0	0	1
A3 = B3	A2 > B2	X	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care   1 ≡ High State   0 ≡ Low State

cessed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4063B "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS							UNITS
			V_O	V_{DD}	−55°C		25°C			125°C		
			V	V	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device[1] Current	I_L			5	–	5	–	0.02	5	–	300●	μA
				10	–	10●	–	0.02	10●	–	200●	
				15	–	–	–	0.02	–	–	–	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.45●	–	
Threshold Voltage[2] N-Channel	$V_{TH}N$	I_D = −20 μA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1]	V_{NL}		0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V
			1	10	3●	–	3●	4.5	–	2.9●	–	
			1.5	15	–	–	–	6.75	–	–	–	
	V_{NH}		4.2	5	1.4	–	1.5●	2.25	–	1.5	–	
			9	10	2.9●	–	3●	4.5	–	3●	–	
			13.5	15	–	–	–	6.75	–	–	–	
Output Drive Current:[2] N-Channel (Sink)	I_DN		0.4	5	0.5	–	0.4●	0.8	–	0.3	–	mA
			0.5	10	1.1	–	0.9●	1.8	–	0.65	–	
			1.5	15	–	-	3	6	–	–	–	
P-Channel (Source)	I_DP		2.5	5	−1.8	–	−1.6●	−3.2	–	−1.3	–	mA
			4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
			13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I		–	15	–	–	–	$\pm10^{-5}$	±1	–	–	μA

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS*	V_{DD} Volts	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: Comparing Inputs to Outputs	t_{PHL}, t_{PLH}		5	625	1250●	ns
			10	250	500●	
			15	175	–	
Cascading Inputs to Outputs	t_{PHL}, t_{PLH}		5	500	1000●	
			10	200	400●	
			15	140	–	
Transition Time	t_{THL}, t_{TLH}		5	100	200●	ns
			10	50	100●	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	–	pF

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

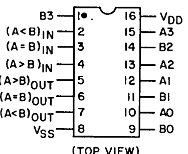
STORAGE-TEMPERATURE RANGE .... −65 to +150°C
OPERATING-TEMPERATURE RANGE .... −55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} • .... −0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) .... 200 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. .... 265°C

• All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	−0.5 V to V_{DD} + 0.5 V	V	–



TERMINAL ASSIGNMENT CD4063B

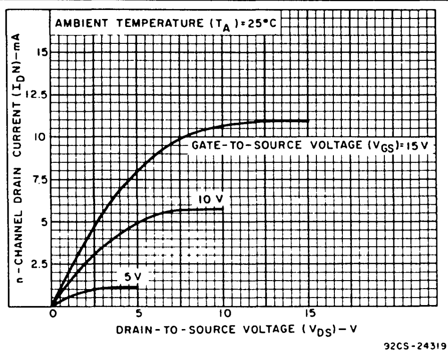


Fig. 1— Minimum output-N-channel drain characteristics.

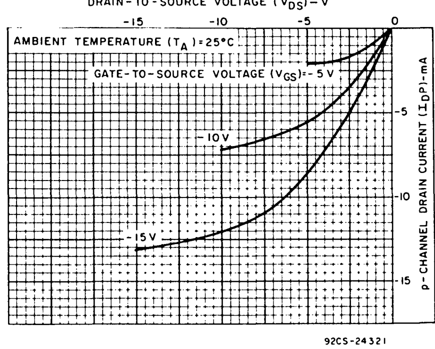
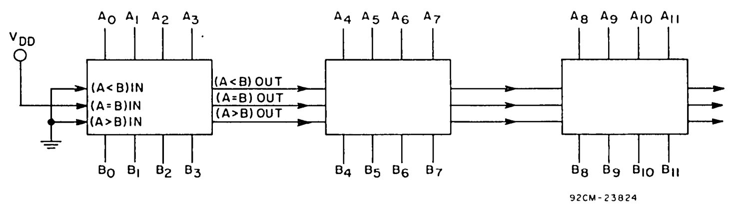


Fig. 2— Minimum output-P-channel drain characteristics.

$\ast$ ALL INPUTS PROTECTED BY THE STANDARD COS/MOS PROTECTION NETWORK

92CM-23823

Fig. 3– Logic diagram CD4063B.



$t_{P\ TOTAL} = t_P \begin{pmatrix}\text{COMPARE}\\ \text{INPUTS}\end{pmatrix} + 2 \times t_P \begin{pmatrix}\text{CASCADE}\\ \text{INPUTS}\end{pmatrix}$, AT C_L = 15 pF (each output), V_{DD} = 10V

(3 STAGES)

= 250 + 2 x (200) = 650 ns (TYP.)

Fig. 4– Typical speed characteristics of a 12-bit comparator.

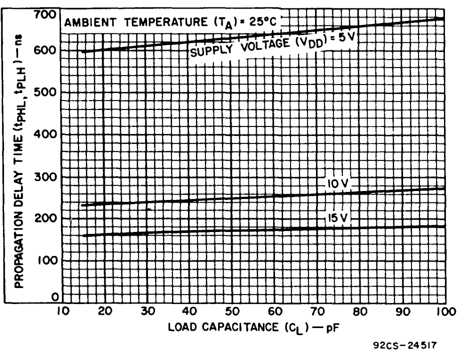


Fig. 5—Typical propagation delay time vs. load capacitance.

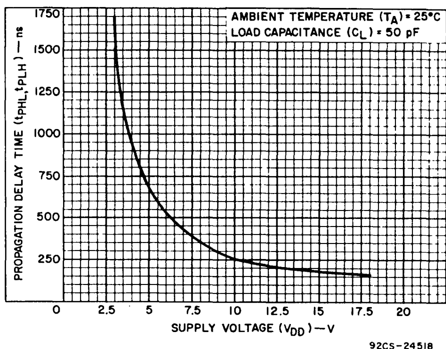


Fig. 6—Typical propagation delay time vs. supply voltage ("comparing inputs" to outputs).

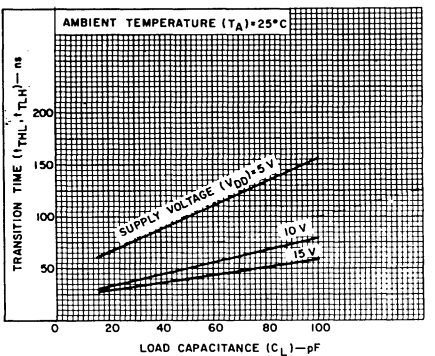


Fig. 7—Typical transition time vs. load capacitance.

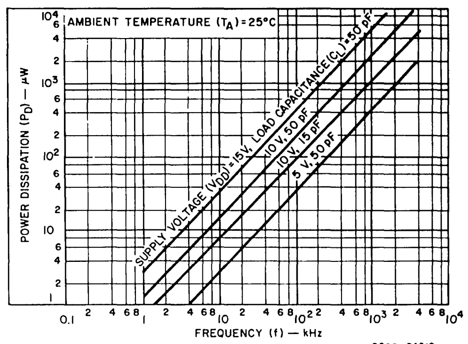


Fig. 8—Typical dynamic power dissipation characteristics.

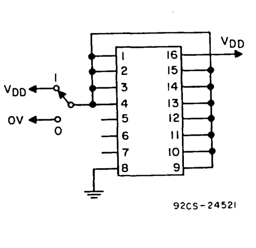


Fig. 9—Quiescent device current test circuit.

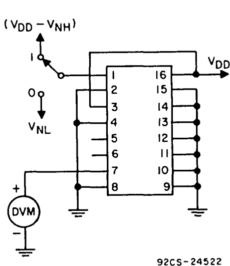


Fig. 10—Noise immunity test circuit.

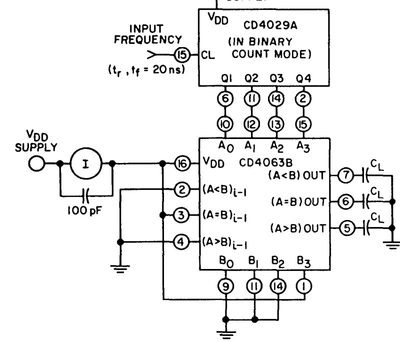


Fig. 11—Dynamic power dissipation test circuit.

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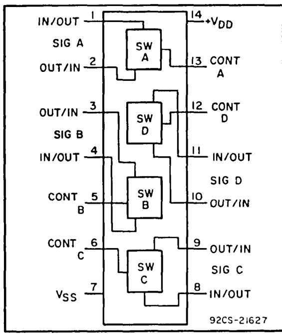


High-Reliability COS/MOS Quad Bilateral Switch

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- 15-V digital or ± 7.5-V peak-to-peak switching
- 80-Ω typical ON resistance for 15-V operation
- Switch ON resistance matched to within 5 Ω over 15-V signal-input range
- ON resistance flat over full peak-to-peak signal range
- High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity: < 0.5% distortion typ. @f_{is}=1 kHz V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ
- Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: –50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch ON = 40 MHz (typ.)

The RCA-CD4066A Slash (/) Series is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016A, but exhibits much lower ON resistance. In addition, ON resistance is relatively constant over the full input-signal range.

The CD4066A consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration minimizes the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016A is recommended.

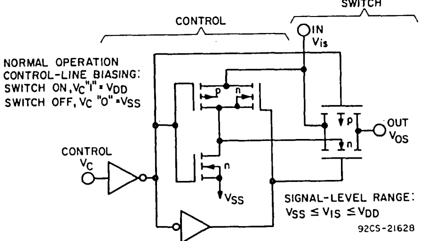


Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

Applications:

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

These devices are electrically and mechanically identical with standard COS/MOS CD4066A types described in data bulletin 769 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4066A "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to "High-Reliability Report RIC-102C "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4066A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

STATIC ELECTRICAL CHARACTERISTICS, All Inputs . . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . . . . **3 to 15 V**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS							UNITS
			V_O	V_{DD}	–55°C		25°C			125°C		
			V	V	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device Current All Switches OFF*	I_L			10	–	0.5●	–	–	0.5●	–	10●	μA
				15	–	1●	–	–	1●	–	100●	
All Switches ON▲				10	–	0.5●	–	–	0.5●	–	10●	μA
Output Voltage[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V
				15	–	–	–	–	1.1●	–	1.1●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				15	–	–	13.9●	–	–	13.9●	–	
Threshold Voltage[2] N-Channel	V_{THN}	$I_D = -20\ \mu A$			–0.7●	–3●	–0.7●	–1.5	–3●	–0.3●	–3●	V
P-Channel	V_{THP}	$I_D = 20\ \mu A$			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1] (Any Input)	V_{NL}	TERMINALS 5,6,12,13	0.5	5	1	–	1●	–	–	9	–	V
			1	10	2	–	2●	–	–	1.8	–	
	V_{NH}		4.5	5	4	–	4●	–	–	3.8	–	
			9	10	8	–	8●	–	–	7.8		
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V

*	TERMINALS	VOLTS APPLIED
V_{SS}	7	GND
V_C	5,6,12,13	GND
V_{IS}	1,4,8,11	≤ + 10
V_{OS}	2,3,9,10	≤ + 10

▲	TERMINALS	VOLTS APPLIED
V_{SS}	7	GND
V_C	5,6,12,13	+ 10
$V_{IS} = V_{OS}$	1,4,8,11	≤ + 10 (Thru 100 Ω)

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE . . . . . −65°C to +150°C

OPERATING TEMPERATURE RANGE . . . −55°C to +125°C

DISSIPATION PER PACKAGE . . . . 200 mW

DC SUPPLY VOLTAGES:

$V_{DD}-V_{SS}$; $V_{DD}-V_{EE}$ . . . . −0.5 to +15 V

ALL SIGNAL AND DIGITAL CONTROL INPUTS . $V_{SS} \leq V_I \leq V_{DD}$

MINIMUM RECOMMENDED POWER SUPPLY VOLTAGES

$V_{DD}-V_{SS}$; $V_{DD}-V_{EE}$ . . . . 3 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.. . . . . 265°C

SPECIAL CONSIDERATIONS – CD4066A

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066A bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066A.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10. Failure to observe this condition may result in distortion of the signal.

ELECTRICAL CHARACTERISTICS, All Inputs. . . . . $V_{SS} \leq V_I \leq V_{DD}$

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . . . . 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS -55°C Typ.	-55°C Max.	25°C Typ.	25°C Max.	125°C Typ.	125°C Max.	UNITS
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
			$V_C=V_{DD}$	V_{SS}	V_{is}							
ON Resistance	R_{ON}	R_L = 10 kΩ	+7.5 V	−7.5 V	−7.5 V to +7.5 V	60	220●	80	280●	145	320●	Ω
			+15 V	0 V	0 to +15 V							
			+5 V	−5 V	−5 V to +5 V	85	400●	120	500●	190	550●	
			+10 V	0 V	0 to +10 V							
			+2.5 V	−2.5 V	−2.5 V to +2.5 V	160	3000●	270	5000●	360	5500●	
			+5 V	0 V	0 to +5 V							
Δ ON Resistance Between Any 2 of 4 Switches	ΔR_{ON}	R_L = 10 kΩ	+7.5 V or +15 V	−7.5 V or 0 V	+7.5 to −7.5 / +15 to 0 V	–	–	5	–	–	–	Ω
			+5 V or +10 V	−5 V or 0 V	+5V to −5V / +10 V to 0 V	–	–	10	–	–	–	
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz	+5 V	−5 V	5 V(p-p)▲	–	–	0.4	–	–	–	%
Input or Output Leakage–Switch OFF (Effective OFF Resistance)			V_{DD}: +7.5 V	$V_C = V_{SS}$: −7.5 V	V_{is}: ±7.5 V	–	* ±100	±0.1	* ±100	–	* ±200	nA
			+5 V	−5 V	±5 V	–	±100*	±0.01	±100*	–	±200*	

* Limit determined by minimum feasible leakage measurement for automatic testing.

▲ Symmetrical about 0 volts.

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

ELECTRICAL CHARACTERISTICS (All inputs . . . . $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS −55°C Min.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	UNITS
Frequency Response-Switch ON (Sine Wave Input)		R_L = 1 kΩ, V_{is}=5 V (p-p)	$V_C = V_{DD}$ = +5 V V_{SS} = −5 V; $20 \text{ Log}_{10} \frac{V_{os}}{V_{is}}$ = −3 dB	–	–	40	–	–	MHz
Feedthrough Switch OFF		R_L = 1 kΩ, V_{is}=5 V (p-p)	V_{DD} = +5 V, $V_C = V_{SS}$ = −5 V; $20 \text{ Log}_{10} \frac{V_{os}}{V_{is}}$ = −50 dB	–	–	1.25	–	–	MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB		R_L = 1 KΩ, V_{is} (A) = 5 V (p-p)	$V_C(A) = V_{DD}$ = +5 V; $V_C(B) = V_{SS}$ = −5 V; $20 \text{ Log}_{10} \frac{V_{os}(B)}{V_{is}(A)}$ = −50 dB	–	–	0.9	–	–	MHz
Capacitance Input	C_{IS}	V_{DD} = +5 V, $V_C = V_{SS}$ = −5 V		–	–	8	–	–	pF
Capacitance Output	C_{OS}			–	–	8	–	–	pF
Capacitance Feedthrough	C_{IOS}			–	–	0.5	–	–	pF
Propagation Delay* Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10 V, V_{SS} = GND, C_L = 15 pF; V_{is} = 10 V (square wave); $t_r = t_f$ = 20 ns (input signal)		–	–	10	20●	–	ns
Control (V_C)									
Noise Immunity	V_{NL}	$V_{is} \leq V_{DD}$	$V_{DD}-V_{SS}$ = 10 V; I_{is} = 10 μA	2	2	4.5	–	2	V
Input Current	I_C	$V_{is} \leq V_{DD}$	$V_{DD}-V_{SS}$ = 10 V; $V_C \leq V_{DD}-V_{SS}$	–	–	±10	–	–	pA
Average Input Capacitance	C_C			–	–	5	–	–	pF
Crosstalk Control Input to Signal Output		$V_{DD}-V_{SS}$=10V, V_C = 10V, (square wave), $t_{rc} = t_{fc}$ = 20 ns	R_L = 10 kΩ	–	–	50	–	–	mV
Propagation Delays*	$t_{pd}C$	$V_{DD}-V_{SS}$=10V, V_C = 10V, (square wave), $t_{rc} = t_{fc}$ = 20 ns	R_L = 300 Ω; $V_{is} \leq$ 10 V, C_L = 15 pF	–	–	35	90●	–	ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10 V, V_{SS} = GND, R_L = 1 kΩ; C_L = 15 pf; V_C = 10 V (square wave); $t_r = t_f$ = 20 ns		–	–	10	–	–	MHz

* Test is a one input or one output only.

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

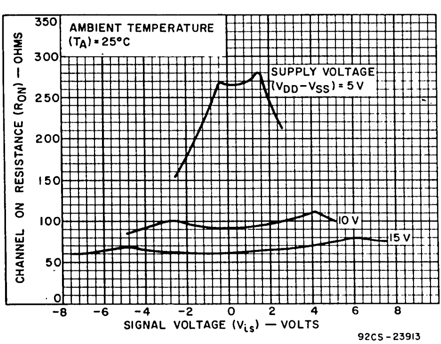


Fig.2 (a) — Typical channel ON resistance vs. signal voltage for three values of supply voltage ($V_{DD}-V_{SS}$).

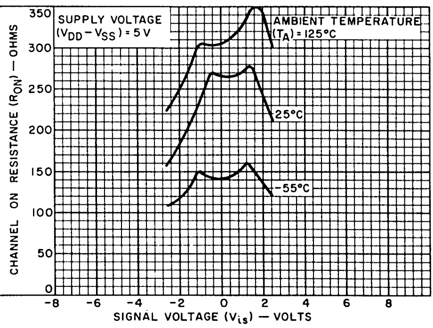


Fig.2 (b) — Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 5 V.

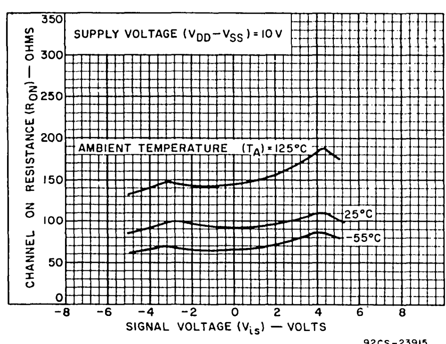


Fig.2 (c) — Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 10 V.

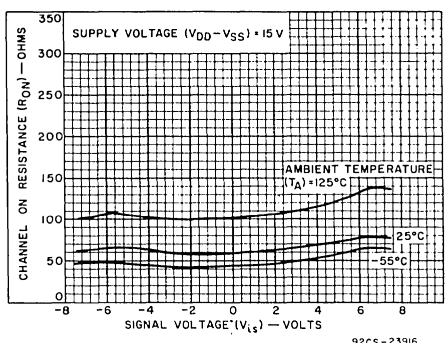


Fig.2 (d) — Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 15 V.

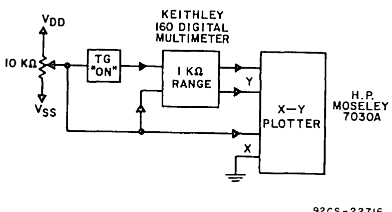


Fig.3 — Channel ON resistance measurement circuit.

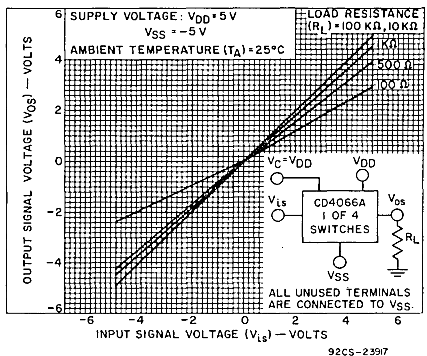


Fig.4 — Typical ON characteristics for 1 of 4 channels.

TEST CIRCUITS

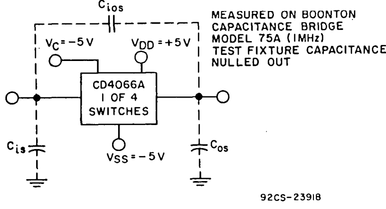


Fig.5 — Capacitance.

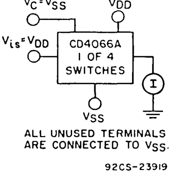


Fig.6 — OFF switch input or output leakage

TEST CIRCUITS (Cont'd)

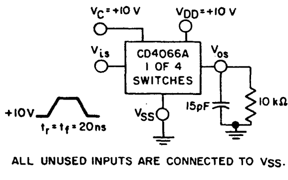


Fig.7 – Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

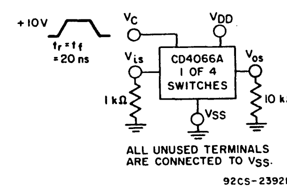


Fig.8 – Crosstalk-control input to signal output.

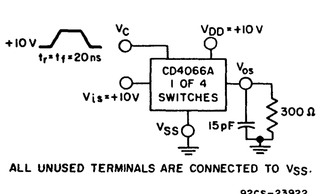


Fig.9 – Propagation delay t_{PLH}, t_{PHL} control-signal output.

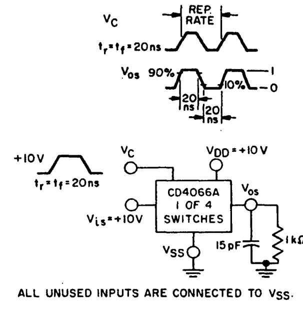


Fig.10 – Maximum allowable control input repetition rate.

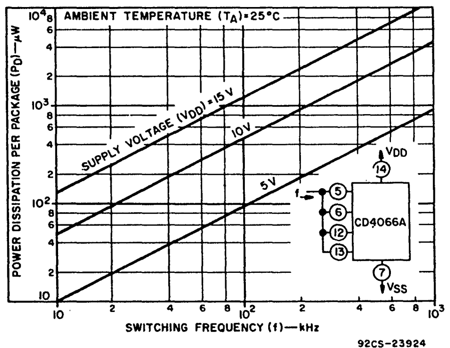


Fig.11 – Power dissipation per package vs switching frequency.

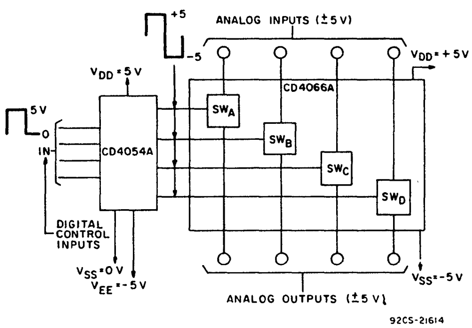


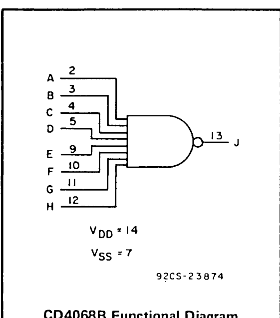
Fig.12 – Bidirectional signal transmission via digital control logic.

Solid State
Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series
CD4068B/. . .



CD4068B Functional Diagram

High-Reliability
COS/MOS 8-Input NAND Gate

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- Medium-Speed Operation – t_{PHL} = 130 ns, t_{PLH} = 100 ns (typ.) at 10 V
- Standard B-Series Output Drive

The RCA-CD4068B "Slash" (/) Series NAND gates provide the system designer with direct implementation of the positive-logic 8-input NAND function and supplement the existing family of COS/MOS gates. These devices have equal source- and sink-current capabilities and conform to standard B-series output drive (see Static Electrical Characteristics).

These devices are electrically and mechanically identical with standard COS/MOS CD4068B types described in data bulletin 809 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4068B "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE . . . . –55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} * . . . . –0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) . . . . 200 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 seconds max. 265°C

* All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	–0.5 V to V_{DD} + 0.5 V	V	–

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS							UNITS
			V_O	V_{DD}	−55°C		25°C			125°C		
			V	V	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device[1] Current	I_L			5	–	0.5	–	0.01	0.5	–	30	μA
				10	–	1●	–	0.01	1●	–	20●	
				15	–	–	–	0.01	–	–	–	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.45●	–	
Threshold Voltage[2] N-Channel	V_{THN}	I_D = −20 μA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	V_{THP}	I_D = 20 μA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1]	V_{NL}		4.2	5	1.5	–	1.5●	2.25	–	1.4	–	V
			9	10	3●	–	3●	4.5	–	2.9●	–	
			13.5	15	–	–	–	6.75	–	–	–	
	V_{NH}		0.8	5	1.4	–	1.5●	2.25	–	1.5	–	
			1	10	2.9●	–	3●	4.5	–	3●	–	
			1.5	15	–	–	–	6.75	–	–	–	
Output Drive Current:[2] N-Channel (Sink)	I_{DN}		0.4	4.5	0.5	–	0.4●	0.8	–	0.3	–	mA
			0.5	10	1.1	–	0.9●	1.8	–	0.65	–	
			1.5	15	–	–	3	6	–	–	–	
P-Channel (Source)	I_{DP}		2.5	5	−2	–	−1.6●	−3.2	–	−1.15	–	mA
			4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
			13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I		–	15	–	–	–	$\pm10^{-5}$	±1	–	–	μA

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS*		LIMITS		UNITS
			V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	325	650●	ns
			10	130	260●	
			15	100	–	
Low-to-High Level	t_{PLH}		5	250	500●	ns
			10	100	200	
			15	75	–	
Transition Time	t_{THL}, t_{TLH}		5	100	200●	ns
			10	50	100●	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	–	pF

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

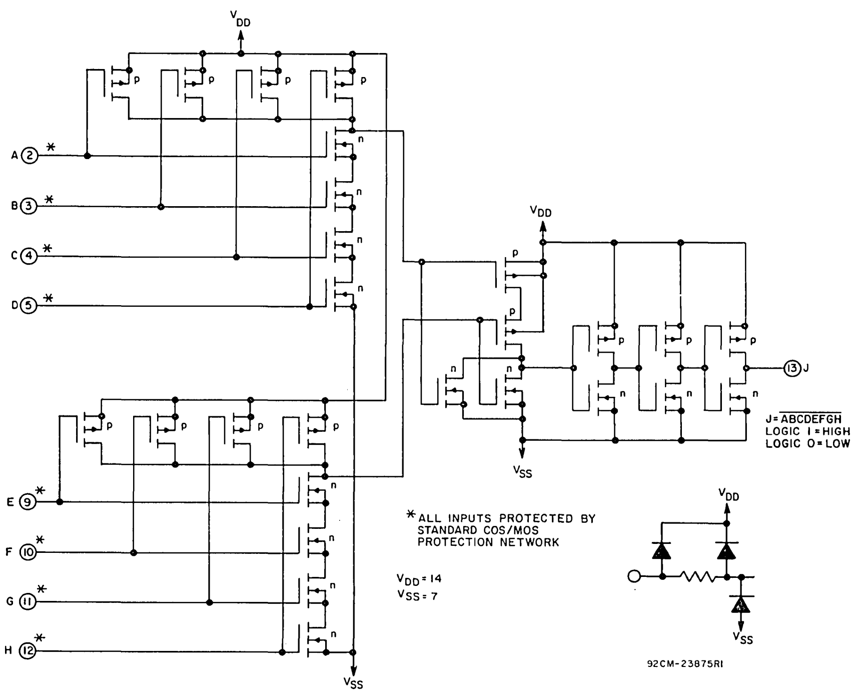


Fig. 1—CD4068B schematic diagram.

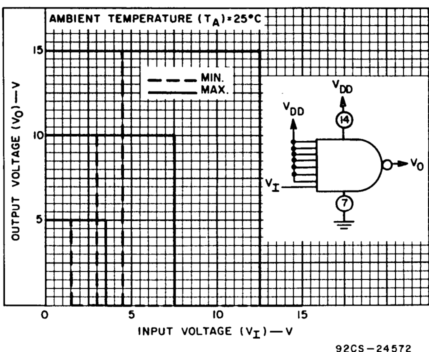


Fig.2—Min. and max. voltage transfer characteristics.

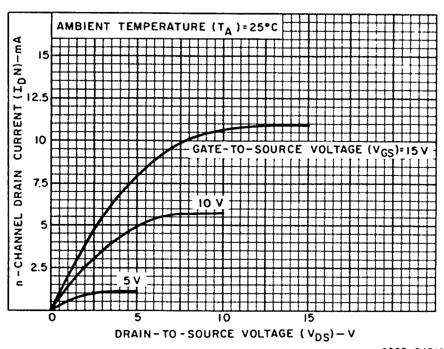


Fig.3—Minimum output-N-channel drain characteristics.

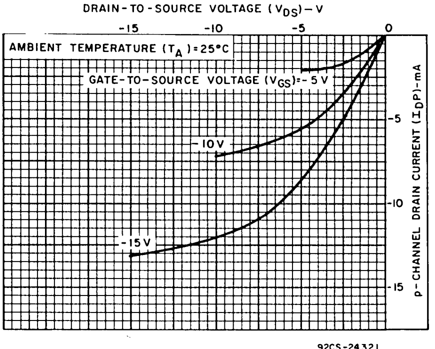


Fig.4—Minimum output-P-channel drain characteristics.

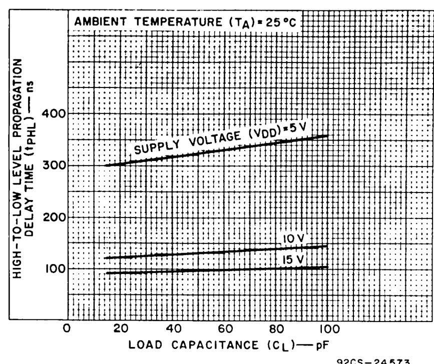


Fig.5—Typical high-to-low level propagation delay time vs. load capacitance.

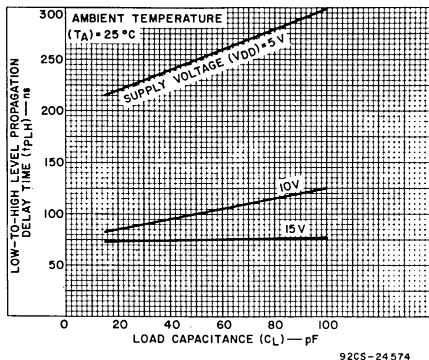


Fig.6—Typical low-to-high level propagation delay time vs. load capacitance.

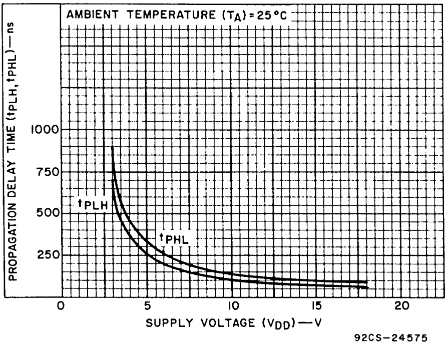


Fig.7—Typical propagation delay time vs. supply voltage.

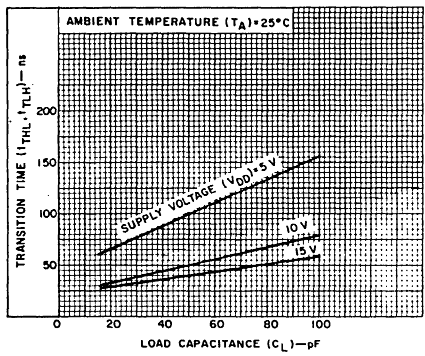


Fig.8—Typical transition time vs. load capacitance.

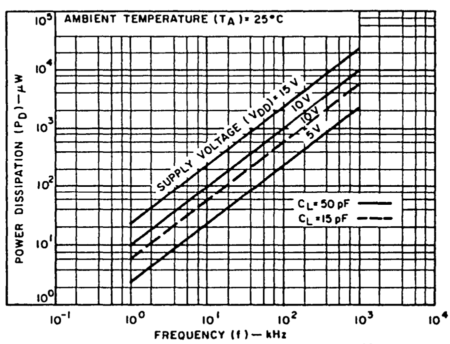


Fig.9—Typical power dissipation vs. frequency.

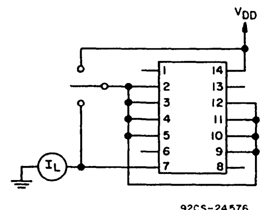


Fig.10—Quiescent device current test circuit.

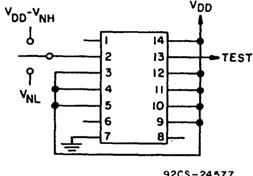
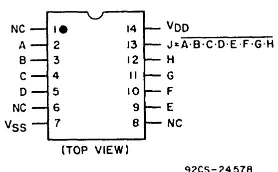


Fig.11—Noise immunity test circuit.

TERMINAL ASSIGNMENT
CD4068B



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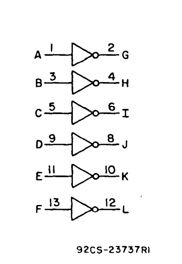
High-Reliability Slash(/) Series CD4069B/ . . .



CD4069B FUNCTIONAL DIAGRAM

High-Reliability COS/MOS Hex Inverter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Medium Speed Operation — t_{PHL}, t_{PLH} = 40 ns (typ.) at 10 V**
- **Standard B-Series Output Drive**

Applications:

- **Logic inversion**
- **Pulse shaping**
- **Oscillators**
- **High-input-impedance amplifiers**

The RCA-CD4069B Slash(/) Series consists of six COS/MOS inverter circuits. All outputs have equal source and sink current capabilities and conform to the standard B-series output drive (see Static Electrical Characteristics).

This device is intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009A and CD4049A Hex Inverter/Buffers are not required.

These devices are electrically and mechanically identical with standard COS/MOS CD4069B types described in data bulletin 804 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4069B "Slash"(/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels—/M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash"(/) Series Types".

The CD4069B "Slash"(/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE . . . . −55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} * . . . . −0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) . . . . 200 mW
ALL INPUTS . . . . $V_{SS} \leq V_I \leq V_{DD}$
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. 265°C

* All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	−0.5 V to V_{DD} + 0.5 V	V	–

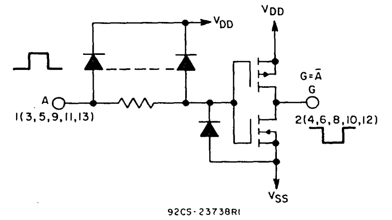


Fig. 1—Schematic diagram of one of six identical inverters.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS							UNITS
		V_O V	V_{DD} V	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	
Quiescent Device[1] Current	I_L		5	–	0.5	–	0.01	0.5	–	30	μA
			10	–	1•	–	0.01	1•	–	20•	
			15	–	–	–	0.01	–	–	–	
Output Voltage[1] Low-Level	V_{OL}		3	–	0.55•	–	–	0.5•	–	–	V
			5	–	0.01	–	0	0.01	–	0.05	
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	0.5•	–	0.55•	
High-Level	V_{OH}		3	2.25•	–	2.3•	–	–	–	–	
			5	4.99	–	4.99	5	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	
			15	–	–	14.5•	15	–	14.45•	–	
Threshold Voltage N-Channel	$V_{TH}N$	I_D = −20 μA		−0.7•	−3•	−0.7•	−1.5	−3•	−0.3•	−3•	V
P-Channel	$V_{TH}P$	I_D = 20 μA		0.7•	3•	0.7•	1.5	3•	0.3•	3•	
Noise Immunity[1]	V_{NL}	3.6	5	1.5	–	1.5•	2.25	–	1.4	–	V
		7.2	10	3•	–	3•	4.5	–	2.9•	–	
		10.8	15	–	–	–	6.75	–	–	–	
	V_{NH}	1.4	5	1.4	–	1.5•	2.25	–	1.5	–	
		2.8	10	2.9•	–	3•	4.5	–	3•	–	
		4.2	15	–	–	–	6.75	–	–	–	
Output Drive[2] Current: N-Channel (Sink)	I_DN	0.4	5	0.5	–	0.4•	0.8	–	0.3	–	mA
		0.5	10	1.1	–	0.9•	1.8	–	0.65	–	
		1.5	15	–	–	3	6	–	–	–	
P-Channel (Source)	I_DP	2.5	5	−2	–	−1.6•	−3.2	–	−1.15	–	
		4.6	5	−0.5	–	−0.4•	−0.8	–	−0.3	–	
		9.5	10	−1.1	–	−0.9•	−1.8	–	−0.65	–	
		13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 μA Test Pin	V_DF			–	1.5•	–	–	1.5•	–	1.5•	V
Input Current	I_I		15	–	–	–	$\pm 10^{-5}$	±1	–	–	μA

Limits with black dot (•) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash(/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS*		LIMITS		UNITS
			V_{DD} Volts	Typ.	Max.	
Propagation Delay Time:	t_{PHL}, t_{PLH}		5 10 15	65 40 30	125 • 80 • –	ns
Transition Time	t_{THL}, t_{TLH}		5 10 15	100 50 40	200 • 100 • 80	ns
Average Input Capacitance	C_I	Any Input		5	–	pF

Limits with black dot (•) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash(/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

*Note: Test is a one input, one output only.

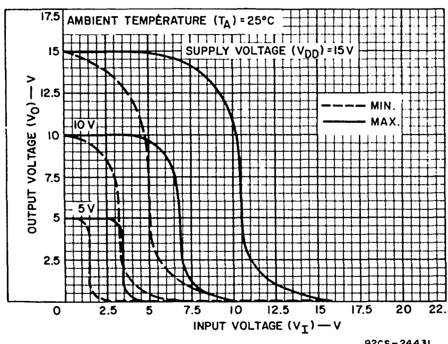


Fig. 2—Min. and max. voltage transfer characteristics.

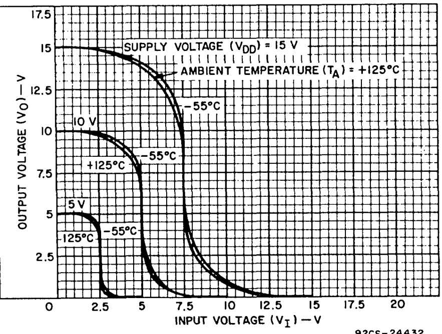


Fig. 3—Typical voltage transfer characteristics as a function of temperature.

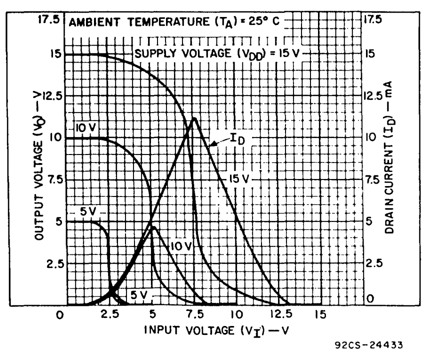


Fig. 4—Typical current and voltage transfer characteristics.

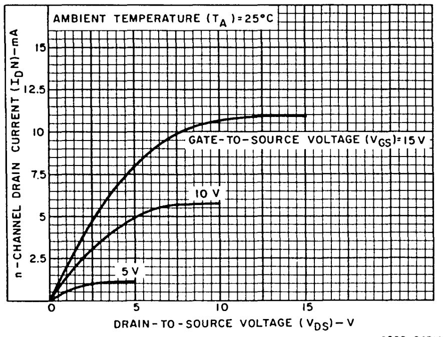


Fig. 5—Minimum output-N-channel drain characteristics.

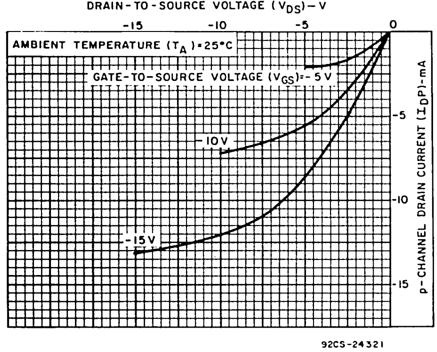


Fig. 6—Minimum output-P-channel drain characteristics.

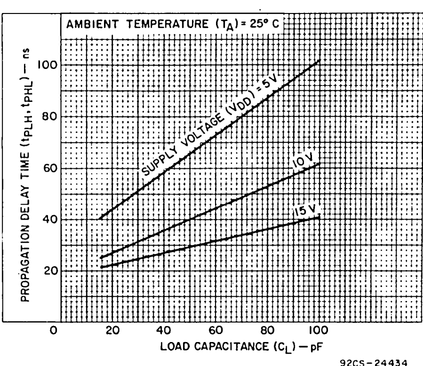


Fig. 7—Typical propagation delay time vs. load capacitance.

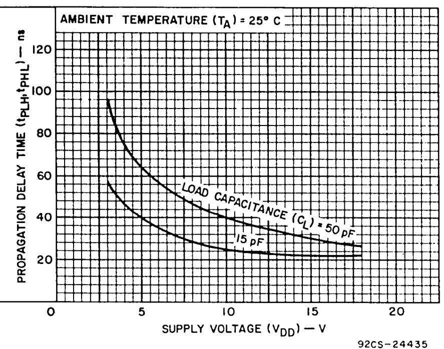


Fig. 8—Typical propagation delay time vs. supply voltage.

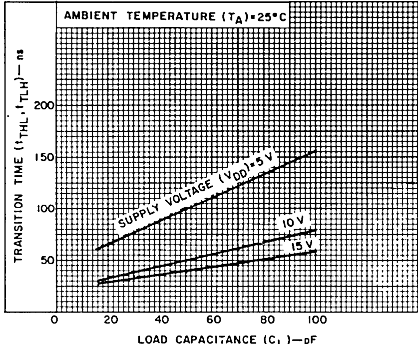


Fig. 9—Typical transition time vs. load capacitance.

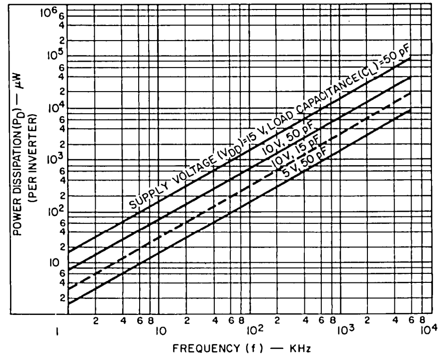


Fig. 10—Typical dynamic power dissipation.

TEST CIRCUITS

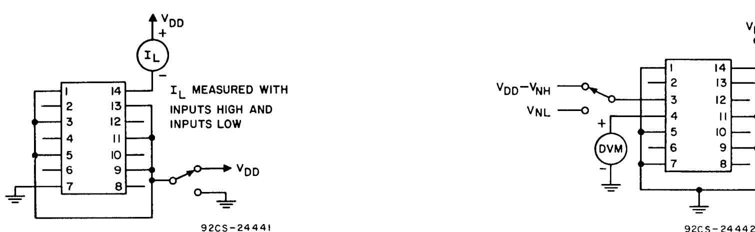


Fig. 11—Quiescent device current.

Fig. 12—Noise immunity.

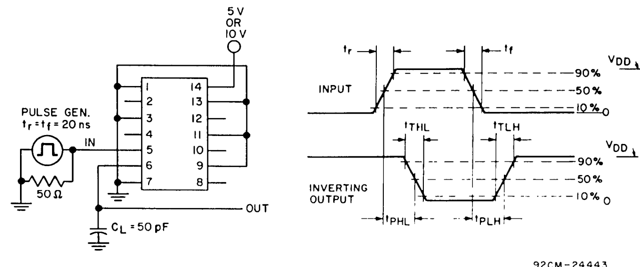
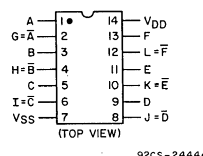


Fig. 13—Dynamic electrical characteristics test circuit and waveforms.

CD4069B
TERMINAL ASSIGNMENT



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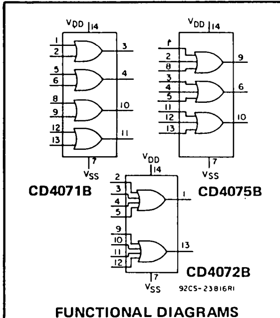
High-Reliability Slash (/) Series

CD4071B/. . ., CD4072B/. . ., CD4075B/. . .



FUNCTIONAL DIAGRAMS

High-Reliability COS/MOS OR Gates

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

CD4071B Quad 2-Input OR Gate
CD4072B Dual 4-Input OR Gate
CD4075B Triple 3-Input OR Gate

Features:

- **Medium-Speed Operation t_{PLH} = 70 ns (typ.); t_{PHL} = 100 ns (typ.) at 10 V**
- **Standard B-Series Output Drive**

The RCA-CD4071B, CD4072B, and CD4075B "Slash" (/) Series OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of COS/MOS gates. These devices have equal source- and sink-current capabilities and conform to standard B-Series output drive (see Static Electrical Characteristics).

These devices are electrically and mechanically identical with standard COS/MOS CD4071B, CD4072B, CD4075B types described in data bulletin 807 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4071B, CD4072B, CD4075B "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE . . . . −55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} * . . . . −0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) . . . . 200 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. 265°C

* All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	−0.5 V to V_{DD} + 0.5 V	V	–

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O	V_{DD}	LIMITS −55°C		25°C			125°C		UNITS
			V	V	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device[1] Current	I_L			5	–	0.5	–	0.01	0.5	–	30	μA
				10	–	1●	–	0.01	1●	–	20●	
				15	–	–	–	0.01	–	–	–	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.05●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.45●	–	
Threshold Voltage[2] N-Channel	V_{THN}	I_D = −20 μA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	V_{THP}	I_D = 20 μA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1]	V_{NL}		0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V
			1	10	3●	–	3●	4.5	–	2.9●	–	
			1.5	15	–	–	–	6.75	–	–	–	
	V_{NH}		4.2	5	1.4	–	1.5●	2.25	–	1.5●	–	
			9	10	2.9●	–	3●	4.5	–	3	–	
			13.5	15	–	–	–	6.75	–	–	–	
Output Drive Current:[2] N-Channel (Sink)	I_{DN}		0.4	4.5	0.5	–	0.4●	0.8	–	0.3	–	mA
			0.5	10	1.1	–	0.9●	1.8	–	0.65	–	
			1.5	15	–	-	3	6	–	–	–	
P-Channel (Source)	I_{DP}		2.5	5	−2	–	−1.6●	−3.2	–	−1.15	–	mA
			4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
			13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I		–	15	–	–	–	$\pm10^{-5}$	±1	–	–	μA

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS*		LIMITS		UNITS
			V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	250	500●	ns
			10	100	200●	
			15	75	–	
Low-to-High Level	t_{PLH}		5	175	350●	ns
			10	70	140●	
			15	55	–	
Transition Time	t_{THL}, t_{TLH}		5	100	200●	ns
			10	50	100●	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	–	pF

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

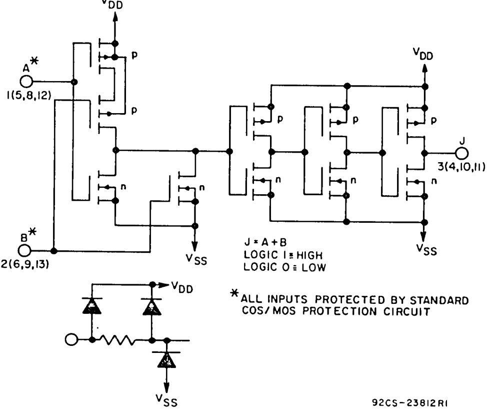


Fig. 1—CD4071B schematic diagram (1 of 4 identical OR gates).

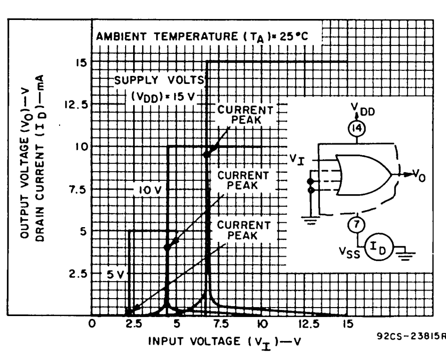


Fig. 2— Typical voltage and current transfer characteristics.

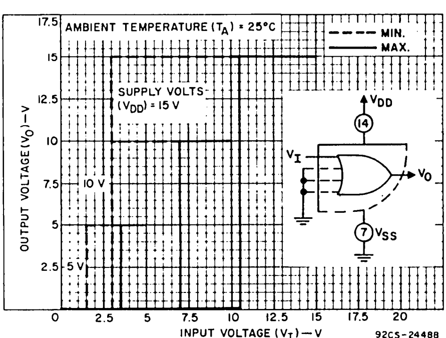


Fig.3—Min. and max. voltage transfer characteristics.

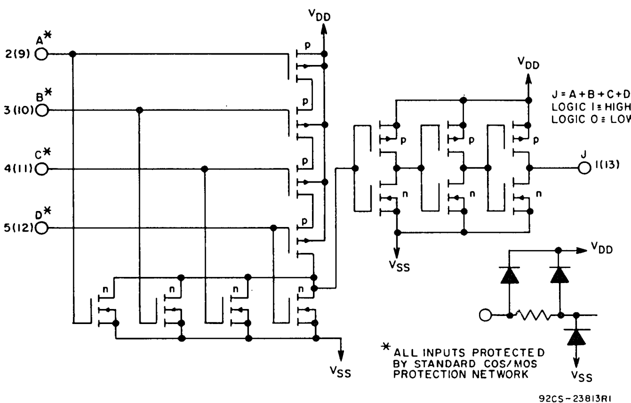


Fig. 4 – CD4072B schematic diagram (1 of 2 identical OR gates).

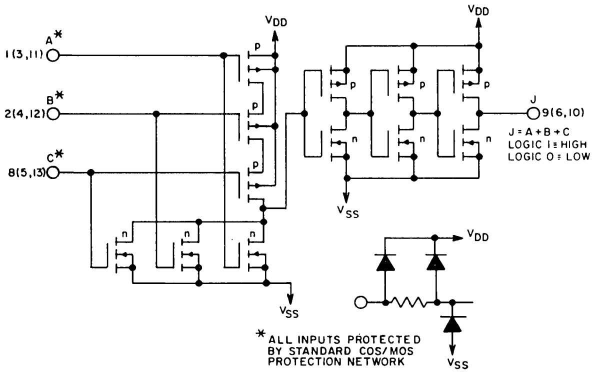


Fig. 5– CD4075B schematic diagram (1 of 3 identical OR gates).

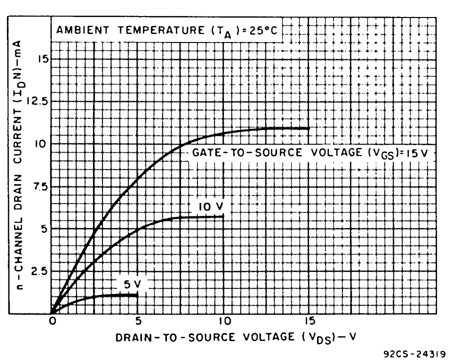


Fig. 6– Minimum output-N-channel drain characteristics.

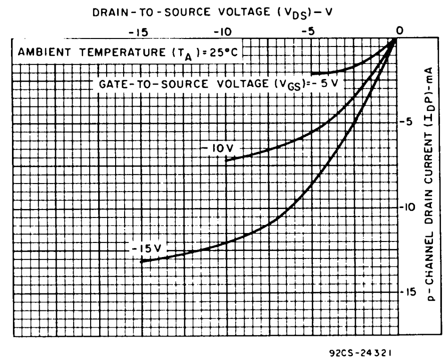


Fig. 7– Minimum output-P-channel drain characteristics.

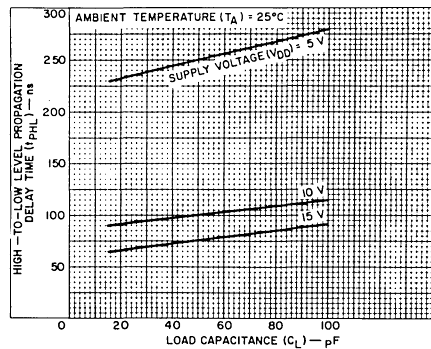


Fig. 8 — Typical high-to-low level propagation delay time vs. load capacitance.

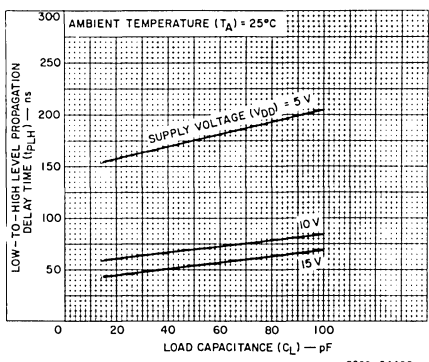


Fig. 9 — Typical low-to-high level propagation delay time vs. load capacitance.

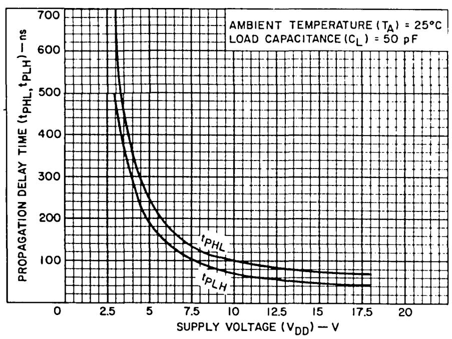


Fig. 10 — Typical propagation delays vs. supply voltage.

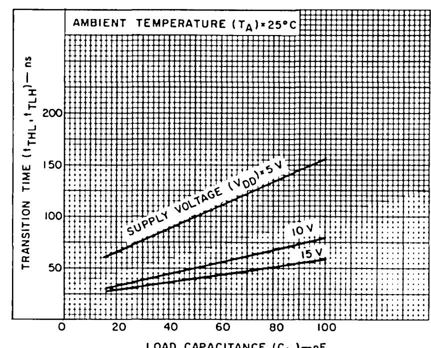


Fig. 11 — Typical transition time vs. load capacitance.

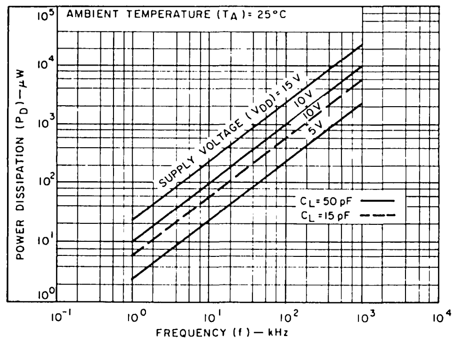


Fig. 12 — Typical dynamic power dissipation vs. frequency.

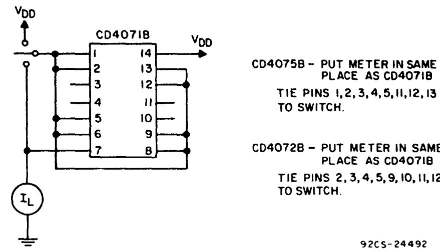


Fig. 13 – Quiescent current test circuits.

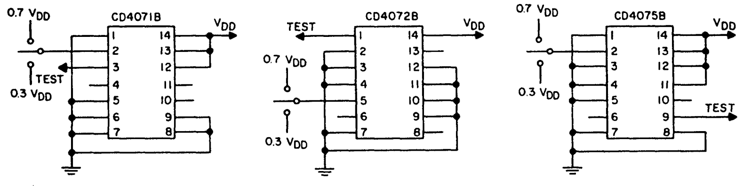
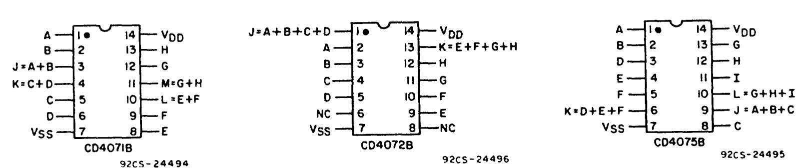


Fig. 14 – Noise immunity test circuits.

TERMINAL ASSIGNMENTS
(Top Views)



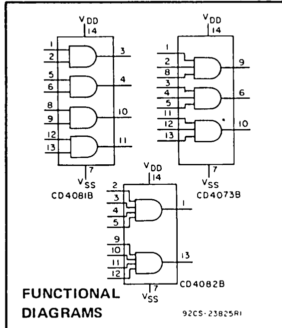
Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series

CD4081B/. . ., CD4082B/. . ., CD4073B/. . .



FUNCTIONAL DIAGRAMS

High-Reliability COS/MOS AND Gates

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate
CD4073B Triple 3-Input AND Gate

Features:

- Medium-Speed Operation — t_{PLH} = 85 ns (typ.); t_{PHL} = 65 ns (typ.) at 10 V
- Standard B-Series Output Drive

The RCA-CD4081B, CD4082B, and CD4073B "Slash" (/) Series AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates. These devices have equal source- and sink-current capabilities and conform to standard B-series output drive (see Electrical Characteristics).

These devices are electrically and mechanically identical with standard COS/MOS CD4081B, CD4082B, CD4073B types described in data bulletin 806 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4081B, CD4082B, CD4073B "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE . . . . −55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} * . . . . −0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) . . . . 200 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 seconds max. 265°C

* All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	−0.5 V to V_{DD} + 0.5 V	V	–

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS							UNITS
			V_O	V_{DD}	−55°C		25°C			125°C		
			V	V	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device[1] Current	I_L			5	–	0.5	–	0.01	0.5	–	30	μA
				10	–	1●	–	0.01	1●	–	20●	
				15	–	–	–	0.01	–	–	–	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.05●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.45●	–	
Threshold Voltage[2] N-Channel	$V_{TH}N$	I_D = −20 μA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1]	V_{NL}		0.8	5	1.5	–	1.5●	2.25	–	1.4	–	V
			1	10	3●	–	3●	4.5	–	2.9●	–	
			1.5	15	–	–	–	6.75	–	–	–	
	V_{NH}		4.2	5	1.4	–	1.5●	2.25	–	1.5	–	
			9	10	2.9●	–	3●	4.5	–	3	–	
			13.5	15	–	–	–	6.75	–	–	–	
Output Drive Current:[2] N-Channel (Sink)	$I_D N$		0.4	5	0.5	–	0.4●	0.8	–	0.3	–	mA
			0.5	10	1.1	–	0.9●	1.8	–	0.65	–	
			1.5	15	–	–	3	6	–	–	–	
P-Channel (Source)	$I_D P$		2.5	5	−2	–	−1.6●	−3.2	–	−1.15	–	mA
			4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
			13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I		–	15	–	–	–	$\pm 10^{-5}$	±1	–	–	μA

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS *		LIMITS		UNITS
			V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	160	320 ●	ns
			10	65	130 ●	
			15	50	—	
Low-to-High Level	t_{PLH}		5	210	420 ●	ns
			10	85	170 ●	
			15	65	—	
Transition Time	t_{THL}, t_{TLH}		5	100	200 ●	ns
			10	50	100 ●	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	—	pF

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

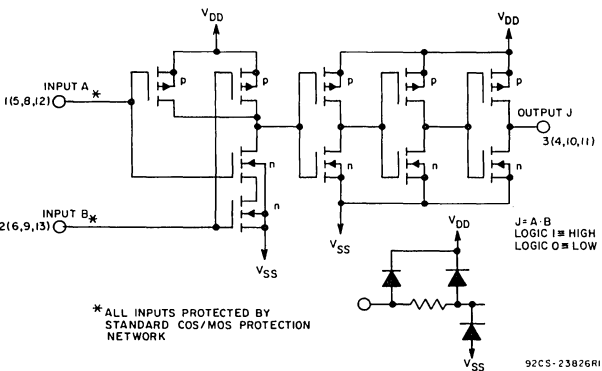


Fig. 1—CD4081B schematic diagram (1 of 4 identical AND gates).

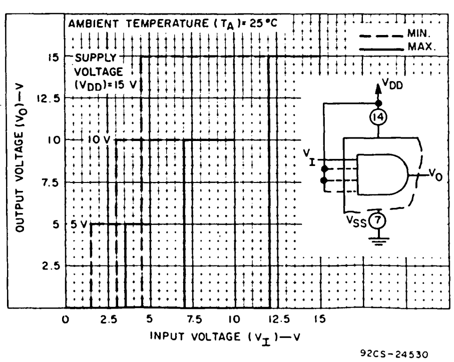


Fig. 2— —Min. and max. voltage transfer characteristics.

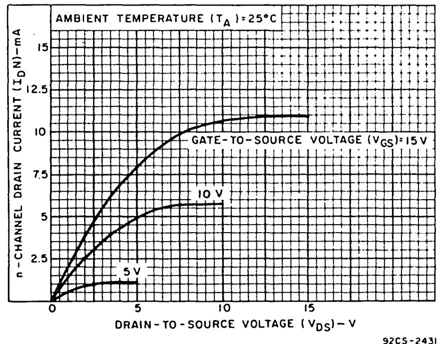


Fig. 3—Minimum output-N-channel drain characteristics.

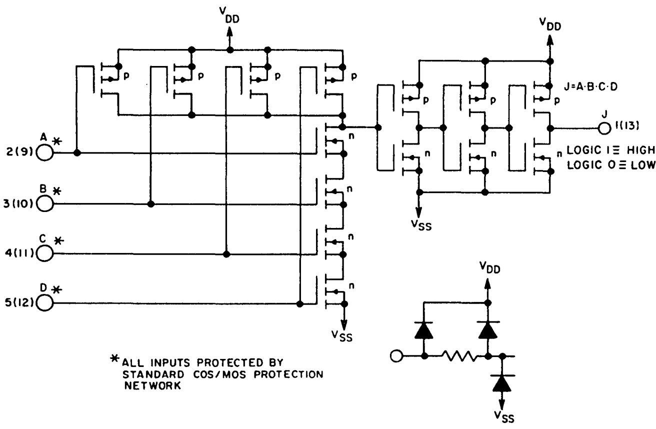


Fig. 4—CD4082B Schematic diagram (1 of 2 identical AND gates).

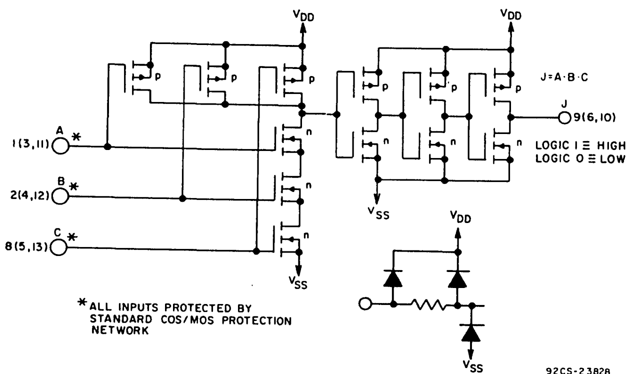


Fig. 5—CD4073B schematic diagram (1 of 3 identical AND gates).

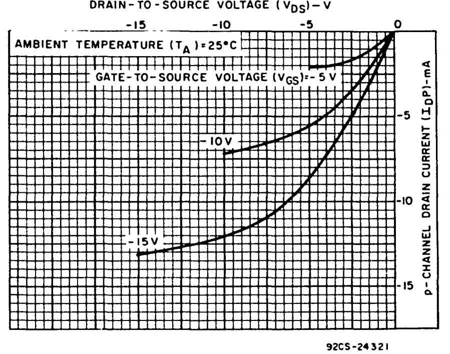


Fig. 6— Minimum output-P-channel drain characteristics.

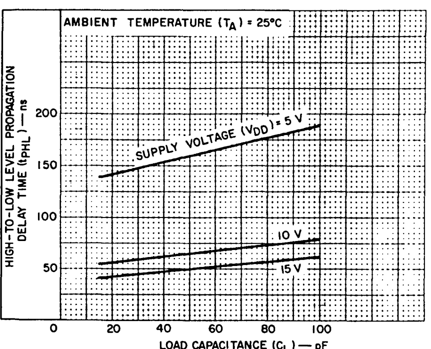


Fig. 7— Typical high-to-low level propagation delay vs. load capacitance.

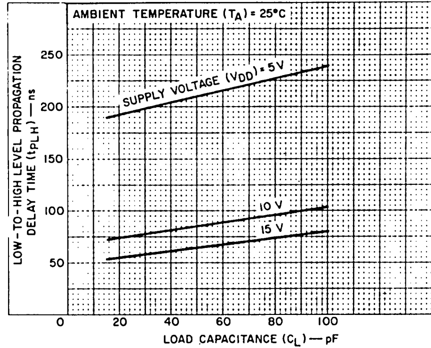


Fig. 8— Typical low-to-high level propagation delay vs. load capacitance.

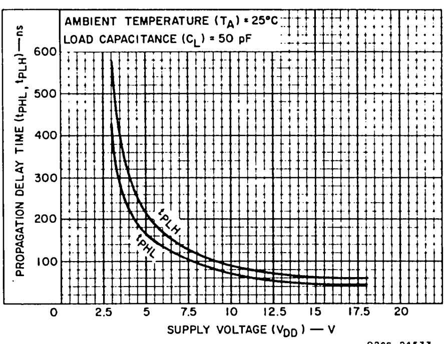


Fig. 9 —Typical propagation delays vs. supply voltage.

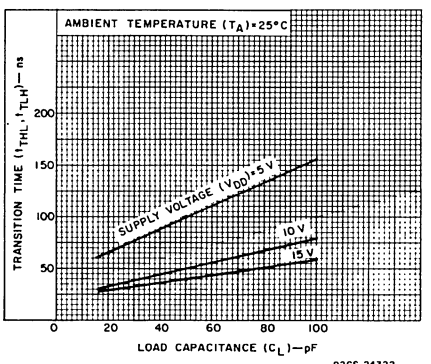


Fig. 10— Typical transition time vs. load capacitance.

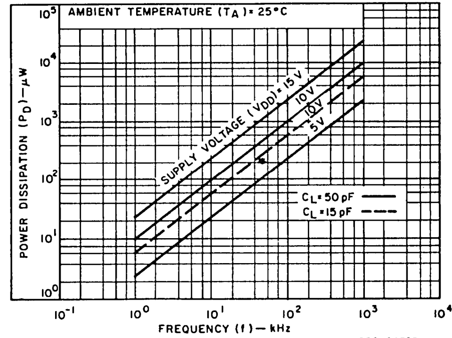


Fig. 11— Typical dynamic power dissipation vs. frequency.

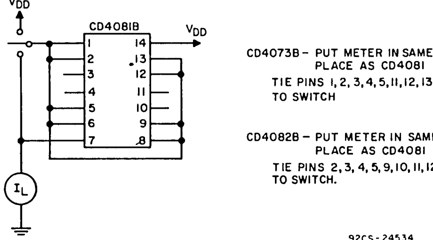


Fig. 12—Quiescent current test circuits.

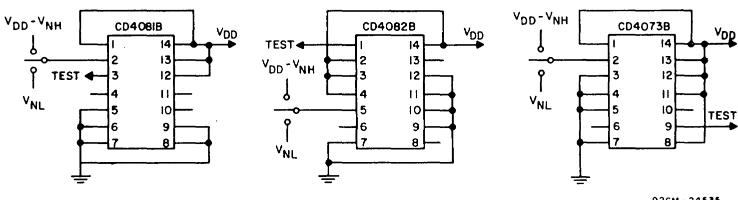
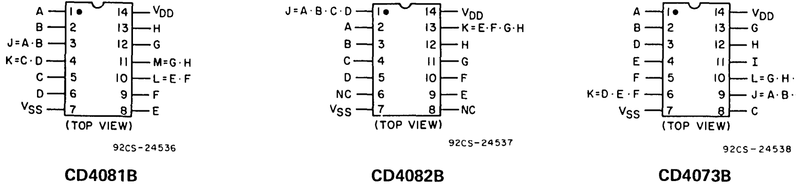


Fig. 13– Noise immunity test circuits.

TERMINAL ASSIGNMENTS



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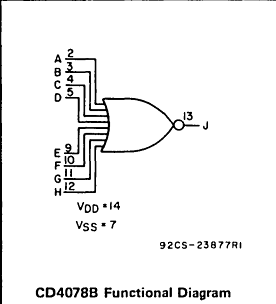


CD4078B Functional Diagram

High-Reliability COS/MOS 8-Input NOR Gate

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Medium-speed operation – t_{PHL} = 80 ns, t_{PLH} = 170 ns (typ.) at 10 V**
- **Standard B-series output drive**

The RCA-CD4078B Slash (/) Series NOR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR function and supplements the existing family of COS/MOS gates.

This device has equal source- and sink-current capability and conforms to standard B-series output drive (see Static Electrical Characteristics).

These devices are electrically and mechanically identical with standard COS/MOS CD4078B types described in data bulletin 810 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4078B "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE . . . . –55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} * . . . . –0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) . . . . 200 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . 265°C

* All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	–0.5 V to V_{DD} + 0.5 V	V	–

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O	V_{DD}	LIMITS −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS
			V	V								
Quiescent Device[1] Current	I_L			5	–	0.5	–	0.01	0.5	–	30	μA
				10	–	1●	–	0.01	1●	–	20●	
				15	–	–	–	0.01	–	–	–	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.45●	–	
Threshold Voltage[2] N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1]	V_{NL}		4.2	5	1.5	–	1.5●	2.25	–	1.4	–	V
			9	10	3●	–	3●	4.5	–	2.9●	–	
			13.5	15	–	–	–	6.75	–	–	–	
	V_{NH}		0.8	5	1.4	–	1.5●	2.25	–	1.5	–	
			1	10	2.9●	–	3●	4.5	–	3●	–	
			1.5	15	–	–	–	6.75	–	–	–	
Output Drive Current:[2] N-Channel (Sink)	$I_D N$		0.4	5	0.5	–	0.4●	0.8	–	0.3	–	mA
			0.5	10	1.1	–	0.9●	1.8	–	0.65	–	
			1.5	15	–	–	3	6	–	–	–	
P-Channel (Source)	$I_D P$		2.5	5	−2	–	−1.6●	−3.2	–	−1.15	–	mA
			4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
			13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I		–	15	–	–	–	$\pm 10^{-5}$	±1	–	–	μA

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS*		LIMITS		UNITS
			V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	200	400●	ns
			10	80	160●	
			15	60	–	
Low-to-High Level	t_{PLH}		5	425	850●	ns
			10	170	340●	
			15	120	–	
Transition Time	t_{THL}, t_{TLH}		5	100	200●	ns
			10	50	100●	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	–	pF

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

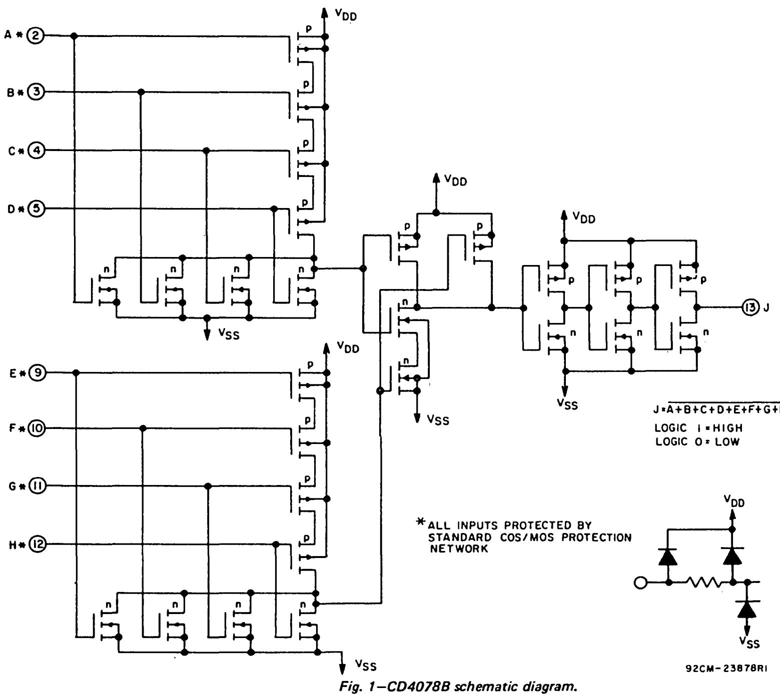


Fig. 1–CD4078B schematic diagram.

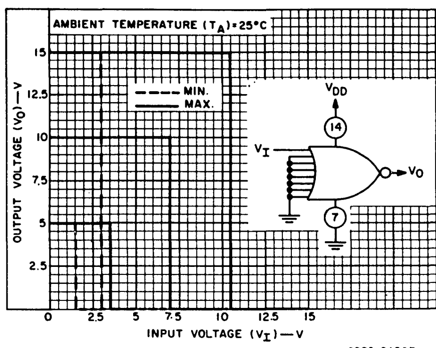


Fig. 2—Min. and max. voltage transfer characteristics.

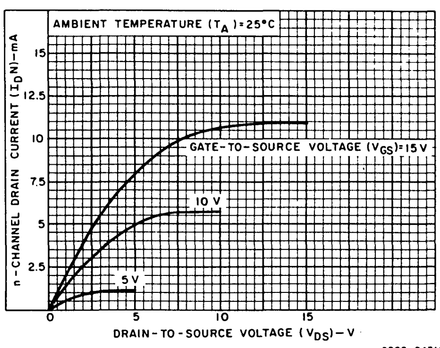


Fig. 3—Minimum output n-channel drain characteristics.

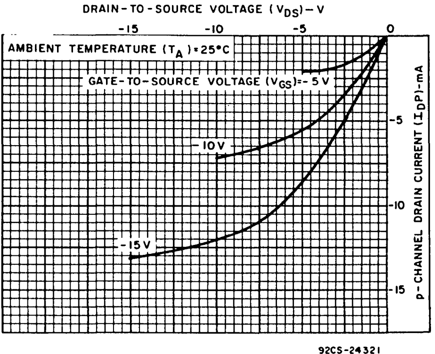


Fig. 4—Minimum output p-channel drain characteristics.

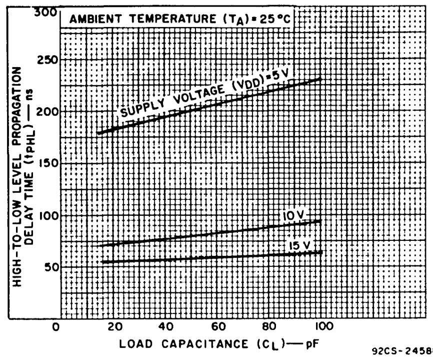


Fig. 5—Typical high-to-low level propagation delay time vs. load capacitance.

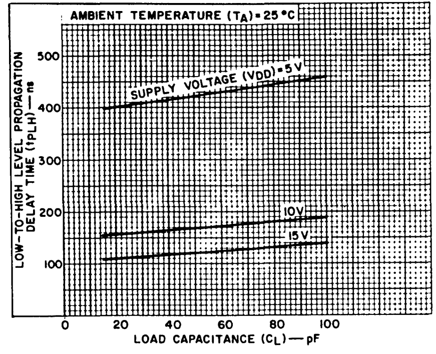


Fig. 6—Typical low-to-high level propagation delay time vs. load capacitance.

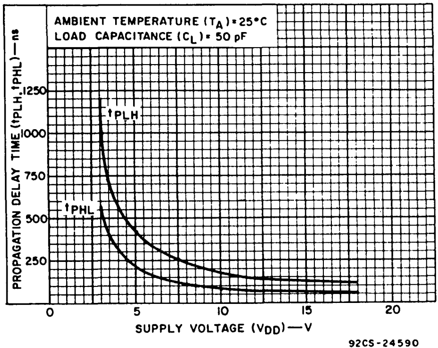


Fig. 7—Typical propagation delay time vs. supply voltage.

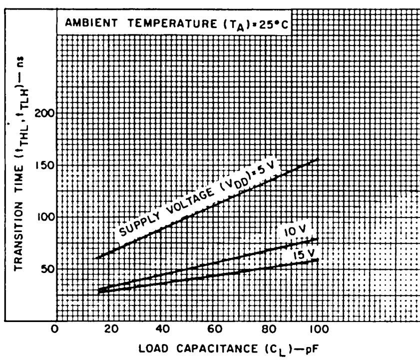


Fig. 8— Typical transition time vs. load capacitance.

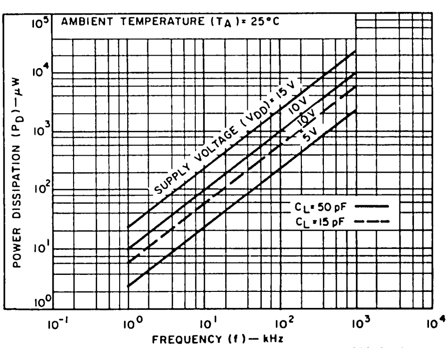


Fig. 9— Typical power dissipation vs. frequency.

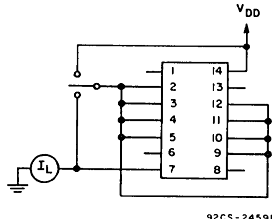


Fig. 10— Quiescent device current test circuit.

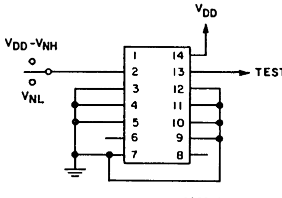
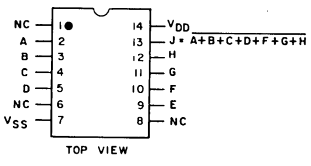


Fig. 11— Noise immunity test circuit.

TERMINAL ASSIGNMENT
CD4078B



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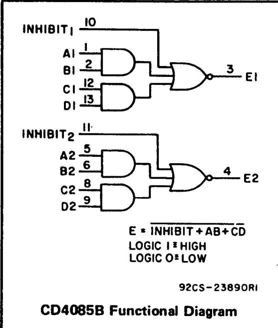
Monolithic Silicon

High-Reliability Slash (/) Series

CD4085B/. . .



CD4085B Functional Diagram

High-Reliability COS/MOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Medium-speed operation — t_{PHL} = 90 ns; t_{PLH} = 125 ns (typ.) at 10 V**
- **Individual inhibit controls**
- **Standard B-series output drive**

The RCA-CD4085B Slash (/) Series contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input OR gate followed by an inverter. Individual inhibit controls are provided for both A-O-I gates. This device has equal source- and sink-current capabilities and conforms to standard B-Series output drive (see Static Electrical Characteristics).

These devices are electrically and mechanically identical with standard COS/MOS CD4085B types described in data bulletin 811 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4085B "Slash" (/) Series can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4085B "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE . . . . −55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} * . . . . −0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) . . . . 200 mW
ALL INPUTS . . . . $V_{SS} \leq V_I \leq V_{DD}$
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 seconds max. . . . . 265°C

* All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	−0.5 V to V_{DD} + 0.5 V	V	–

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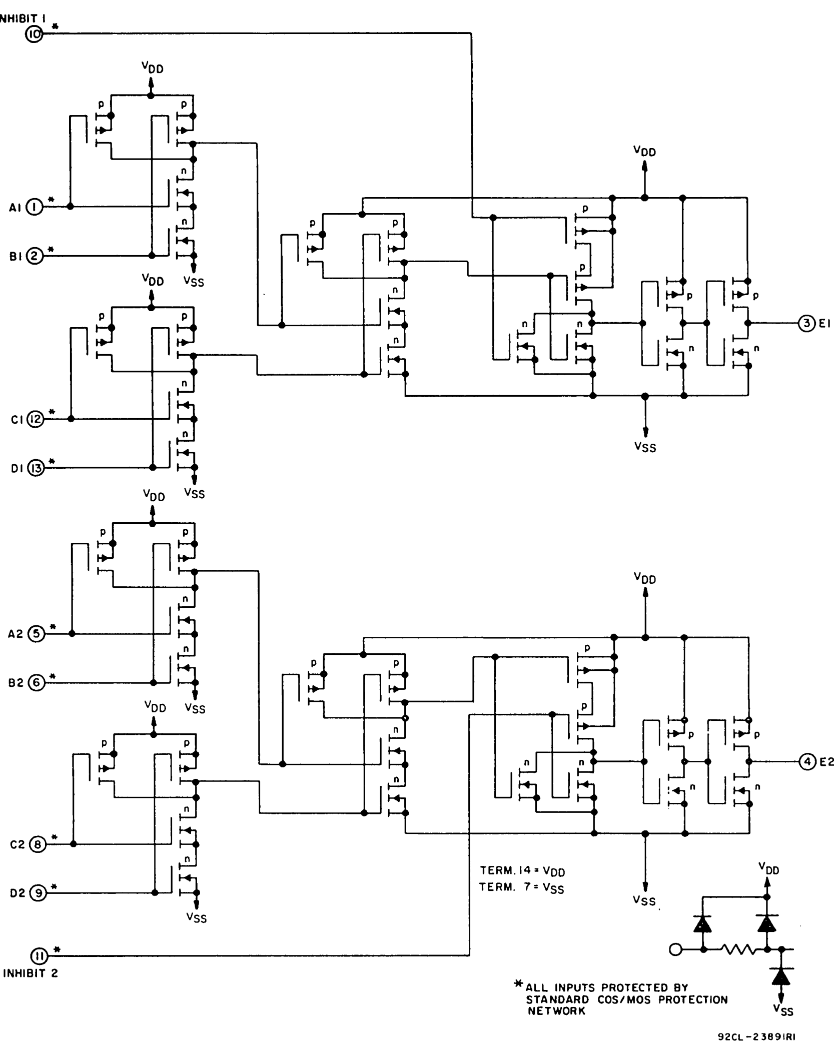


Fig. 1—CD4085B schematic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O (V)	V_{DD} (V)	−55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS
Quiescent Device[1] Current	I_L			5	–	0.5	–	0.01	0.5	–	30	μA
				10	–	1●	–	0.01	1●	–	20●	
				15	–	–	–	0.01	–	–	–	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.45●	–	
Threshold Voltage[2] N-Channel	$V_{TH}N$	I_D = −20 μA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	$V_{TH}P$	I_D = 20 μA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1]	V_{NL}		4.2	5	1.5	–	1.5●	2.25	–	1.4	–	V
			9	10	3●	–	3●	4.5	–	2.9●	–	
			13.5	15	–	–	–	6.75	–	–	–	
	V_{NH}		0.8	5	1.4	–	1.5●	2.25	–	1.5	–	
			1	10	2.9●	–	3●	4.5	–	3●	–	
			1.5	15	–	–	–	6.75	–	–	–	
Output Drive Current:[2] N-Channel (Sink)	I_DN		0.4	5	0.5	–	0.4●	0.8	–	0.3	–	mA
			0.5	10	1.1	–	0.9●	1.8	–	0.65	–	
			1.5	15	–	-	3	6	–	–	–	
P-Channel (Source)	I_DP		2.5	5	−2	–	−1.6●	−3.2	–	−1.15	–	mA
			4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
			13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I		–	15	–	–	–	$\pm10^{-5}$	±1	–	–	μA

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns

CHARACTERISTIC	SYMBOL	TEST CONDITIONS *		LIMITS		UNITS
			V_{DD} V	Typ.	Max.	
Propagation Delay Time (Data): High-to-Low Level	t_{PHL}		5	225	450 ●	ns
			10	90	180 ●	
			15	65	–	
Low-to-High Level	t_{PLH}		5	310	620 ●	ns
			10	125	250 ●	
			15	90	–	
Propagation Delay Time (Inhibit): High-to-Low Level	$t_{PHL(INH)}$		5	150	300 ●	ns
			10	60	120 ●	
			15	40	–	
Low-to-High Level	$t_{PLH(INH)}$		5	250	500 ●	ns
			10	100	200 ●	
			15	70	–	
Transition Time	t_{THL}, t_{TLH}		5	100	200 ●	ns
			10	50	100 ●	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	–	pF

Limits with black dot (●) designate 100% testing. Refer to HIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

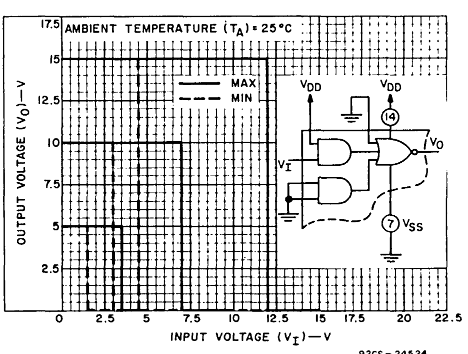


Fig. 2– Min. and max. voltage transfer characteristics.

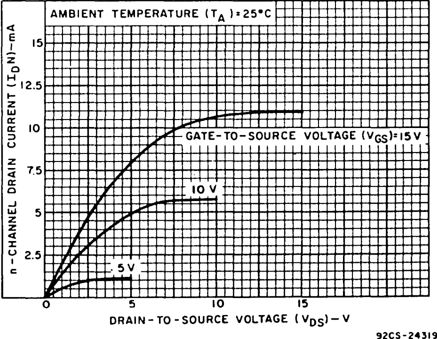


Fig. 3—Minimum output n-channel drain characteristics.

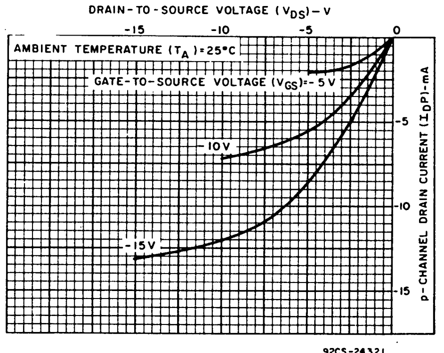


Fig. 4— Minimum output p-channel drain characteristics.

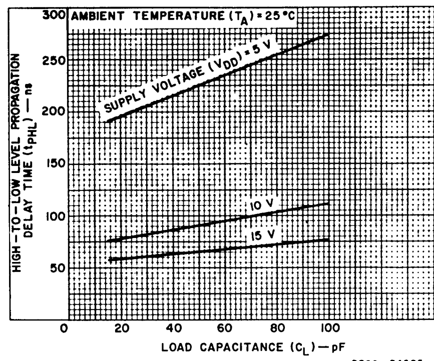


Fig. 5— Typical data high-to-low level propagation delay time vs. load capacitance.

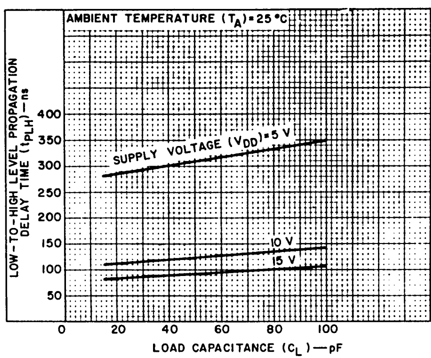


Fig. 6— Typical data low-to-high level propagation delay time vs. load capacitance.

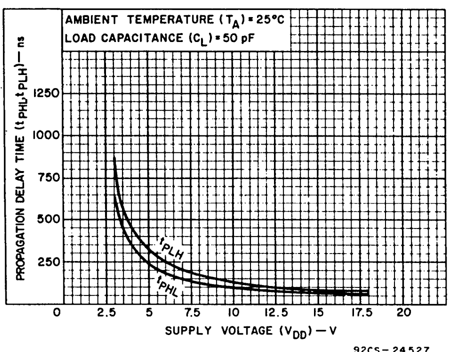


Fig. 7— Typical data propagation delay time vs. supply voltage.

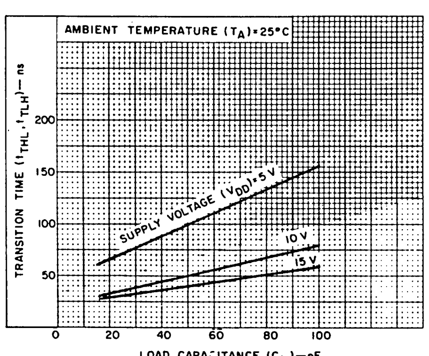


Fig. 8— Typical transition time vs. load capacitance.

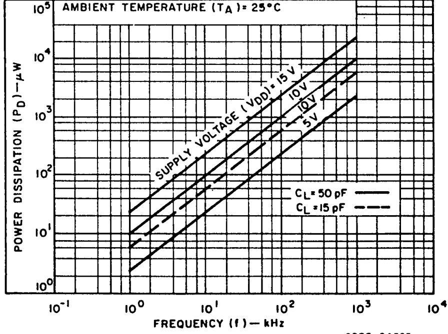


Fig. 9— Typical power dissipation vs. frequency.

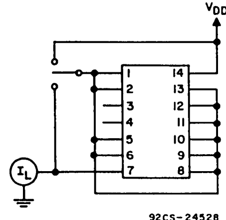


Fig. 10—Quiescent device current test circuit.

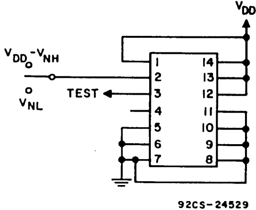
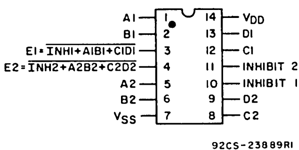


Fig. 11—Noise immunity test circuit.

TERMINAL ASSIGNMENT
(TOP VIEW)
CD4085B



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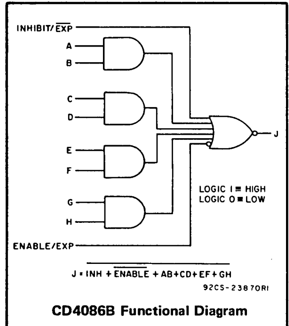

CD4086B Functional Diagram

High-Reliability COS/MOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Medium-speed operation – t_{PHL} = 90 ns; t_{PLH} = 140 ns (typ.) at 10 V**
- **INHIBIT and ENABLE inputs**
- **Standard B-series output drive**

The RCA-CD4086B "Slash" (/) Series contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/$\overline{EXP}$ is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig. 2 and its associated explanation for applications where a capability greater than 4-wide is required. This device has equal source- and sink-current capabilities and conforms to standard B-series output drive (see Static Electrical Characteristics).

These devices are electrically and mechanically identical with standard COS/MOS CD4086B types described in data bulletin 812 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4086B "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE . . . . –55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} * . . . . –0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) . . . . 200 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. 265°C

* All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	–0.5 V to V_{DD} + 0.5 V	V	–

TERM. 14 = V_{DD}
TERM 7 = V_{SS}

*ALL INPUTS PROTECTED BY STANDARD COS/MOS PROTECTION NETWORK.

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Fig. 1–CD4086B schematic diagram.

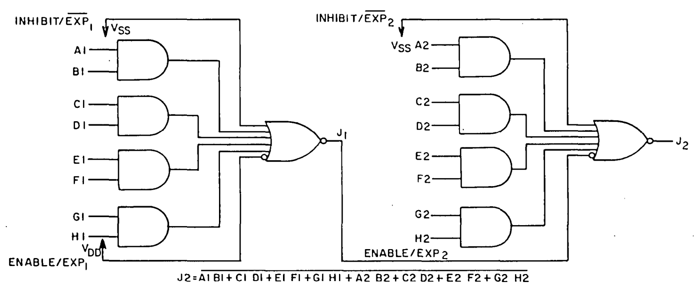


Fig. 2–Two CD4086B's connected as an 8-wide 2-input A-O-I gate.

Fig. 2 above shows two CD4086B's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086B is fed directly to the ENABLE/EXP2 line of the second CD4086B. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/$\overline{EXP}$ input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/EXP input with the same result.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O	V_{DD}	LIMITS −55°C		25°C			125°C		UNITS
			V	V	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device[1] Current	I_L			5	–	0.5	–	0.01	0.5	–	30	μA
				10	–	1●	–	0.01	1●	–	20●	
				15	–	–	–	0.01	–	–	–	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.45●	–	
Threshold Voltage[2] N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1]	V_{NL}		4.2	5	1.5	–	1.5●	2.25	–	1.4	–	V
			9	10	3●	–	3●	4.5	–	2.9●	–	
			13.5	15	–	–	–	6.75	–	–	–	
	V_{NH}		0.8	5	1.4	–	1.5●	2.25	–	1.5	–	
			1	10	2.9●	–	3●	4.5	–	3●	–	
			1.5	15	–	–	–	6.75	–	–	–	
Output Drive Current:[2] N-Channel (Sink)	I_DN		0.4	4.5	0.5	–	0.4●	0.8	–	0.3	–	mA
			0.5	10	1.1	–	0.9●	1.8	–	0.65	–	
			1.5	15	–	–	3	6	–	–	–	
P-Channel (Source)	I_DP		2.5	5	−2	–	−1.6●	−3.2	–	−1.15	–	mA
			4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
			13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 μA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I		–	15	–	–	–	$\pm 10^{-5}$	±1	–	–	μA

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, C_L = 50 pF, Input t_r,t_f = 20 ns

CHARACTERISTIC	SYMBOL	TEST CONDITIONS*	V_{DD} Volts	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time (Data): High-to-Low Level	t_{PHL}		5	225	450●	ns
			10	90	180●	
			15	60	–	
Low-to-High Level	t_{PLH}		5	350	700●	ns
			10	140	280●	
			15	100	–	
Propagation Delay Time (Inhibit): High-to-Low Level	$t_{PHL(INH)}$		5	150	300●	ns
			10	60	120●	
			15	40	–	
Low-to-High Level	$t_{PLH(INH)}$		5	250	500●	ns
			10	100	200●	
			15	70	–	
Transition Time	t_{THL}, t_{TLH}		5	100	200●	ns
			10	50	100●	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	–	pF

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash(/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

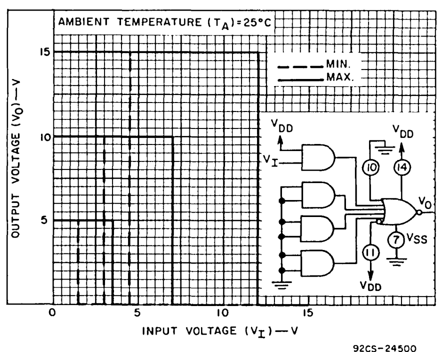


Fig.3— Min. and max. voltage transfer characteristics.

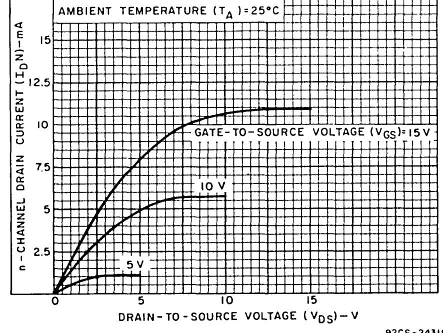


Fig.4—Minimum output n-channel drain characteristics.

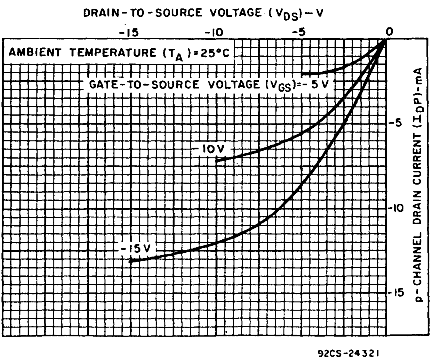


Fig.5—Minimum output p-channel drain characteristics.

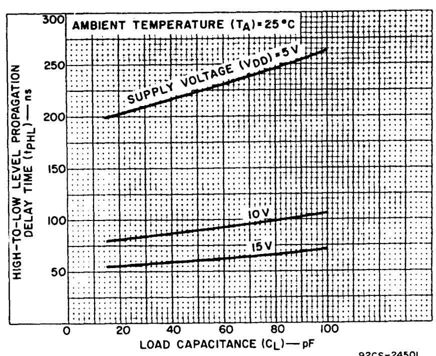


Fig.6—Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

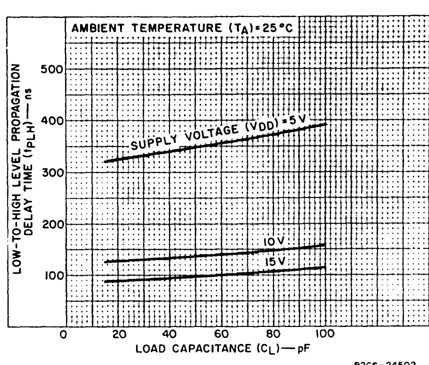


Fig.7—Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

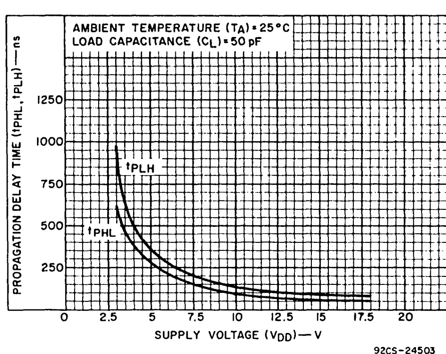


Fig.8—Typical DATA or ENABLE propagation delay time vs. supply voltage.

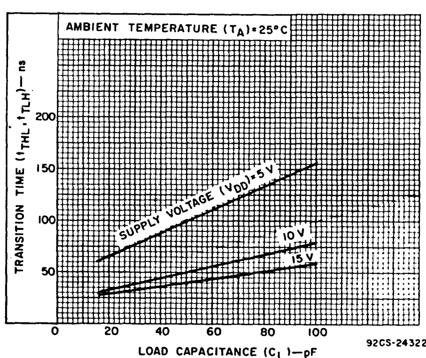


Fig.9—Typical transition time vs. load capacitance.

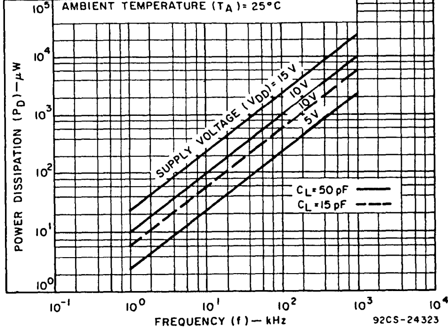


Fig.10—Typical power dissipation vs. frequency.

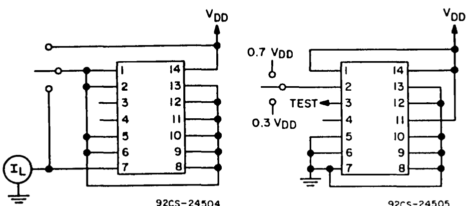
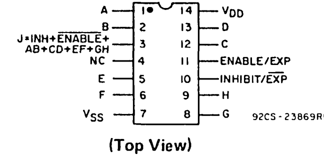


Fig. 11 – Quiescent device current test circuit.

Fig. 12 – Noise immunity test circuit.



(Top View)

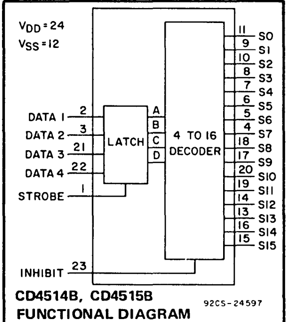
TERMINAL ASSIGNMENT CD4086B

Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/)Series
CD4514B/. . . CD4515B/. . .



CD4514B, CD4515B FUNCTIONAL DIAGRAM 92CS-24597

High-Reliability COS/MOS 4-Bit Latch/4-to-16 Line Decoder

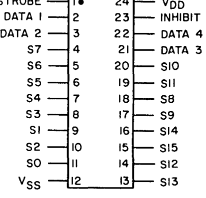
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

CD4514B Output "High" on Select
CD4515B Output "Low" on Select

Features:

- **Strobed input latch**
- **Inhibit control**

TERMINAL ASSIGNMENT
CD4514B
CD4515B



92CS-24554

The RCA-CD4514B▲ and CD4515B▲ "Slash" (/) Series are monolithic integrated circuits consisting of a 4-bit strobed latch and a 4-to-16 line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0 (CD4514B) or 1 (CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are electrically and mechanically identical with standard COS/MOS CD4514B and CD4515B types described in data bulletin 814 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4514B and CD4515B "Slash" (/) Series types are supplied in 24-lead dual-in-line ceramic packages ("D" suffix), in 24-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

▲ Formerly CD4064A and CD4065A, respectively.

Applications:

- **Digital multiplexing**
- **Address decoding**
- **Hexadecimal/BCD decoding**
- **Program-counter decoding**
- **Control decoder**

DECODE TRUTH TABLE (Strobe = 1)

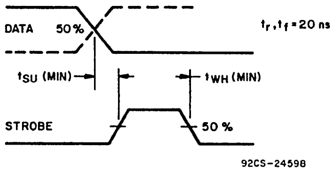
INHIBIT	DATA INPUTS				SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE .... −65 to +150°C
OPERATING-TEMPERATURE RANGE .... −55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} * .... −0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) .... 200 mW
ALL INPUTS .... $V_{SS} \leqslant V_I \leqslant V_{DD}$
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 seconds max. .... 265°C

* All voltage values are referenced to V_{SS} terminal.



Waveforms for setup time and strobe pulse width.

OPERATING CONDITIONS AT $T_A = 25°C$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	−0.5 V to V_{DD} + 0.5 V	V	–
Setup Time	5 10	250 100	None	ns	A
Strobe Pulse Width	5 10	350 100	None	ns	A

DATA 1 2
DATA 2 3
DATA 3 21
DATA 4 22
STROBE 1
INHIBIT 23
S Q A R $\bar{Q}$
S Q B R $\bar{Q}$
S Q C R $\bar{Q}$
S Q D R $\bar{Q}$
$\bar{A}\bar{B}\bar{C}\bar{D}$ 11 S0
$A\bar{B}\bar{C}\bar{D}$ 9 S1
$\bar{A}B\bar{C}\bar{D}$ 10 S2
$AB\bar{C}\bar{D}$ 8 S3
$\bar{A}\bar{B}C\bar{D}$ 7 S4
$A\bar{B}C\bar{D}$ 6 S5
$\bar{A}BC\bar{D}$ 5 S6
$ABC\bar{D}$ 4 S7
$\bar{A}\bar{B}\bar{C}D$ 18 S8
$A\bar{B}\bar{C}D$ 17 S9
$\bar{A}B\bar{C}D$ 20 S10
$AB\bar{C}D$ 19 S11
$\bar{A}\bar{B}CD$ 14 S12
$A\bar{B}CD$ 13 S13
$\bar{A}BCD$ 16 S14
$ABCD$ 15 S15
THESE INVERTERS USED ONLY ON CD4515B
V_{DD}
V_{SS}
* ALL INPUTS PROTECTED BY STANDARD COS/MOS PROTECTION NETWORK
92CL-23770R1

Fig. 1—Logic diagram for CD4514B and CD4515B.

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	SYMBOL	TEST CONDITIONS V_O (V) ▲	V_O (V) ★	V_{DD} V	LIMITS −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°V Min.	125°V Max.	UNITS
Quiescent Device[1] Current	I_L			5	–	5	–	0.02	5	–	300	µA
				10	–	10●	–	0.02	10●	–	200●	
				15	–	–	–	0.02	–	–	–	
Output Voltage[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.45●	–	
Threshold Voltage N-Channel	V_{THN}	I_D = −20 µA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	V_{THP}	I_D = 20 µA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1] Any Input	V_{NL}	0.8	4.2	5	1.5	–	1.5●	2.25	–	1.4	–	V
		1	9	10	3●	–	3●	4.5	–	2.9●	–	
		1.5	13.5	15	–	–	–	6.75	–	–	–	
	V_{NH}	4.2	0.8	5	1.4	–	1.5●	2.25	–	1.5	–	
		9	1	10	2.9●	–	3●	4.5	–	3●	–	
		13.5	1.5	15	–	–	–	6.75	–	–	–	
Output Drive[2] Current: N-Channel (Sink)	I_{DN}	0.4		5*	0.5	–	0.4●	0.8	–	0.3	–	mA
		0.5		10†	1.1	–	0.9●	2	–	0.65	–	
		1.5		15	–	–	–	7.8	–	–	–	
P-Channel (Source)	I_{DP}	4.6		5*	−0.25	–	−0.2●	−0.4	–	−0.15	–	mA
		2.5		5†	−1	–	−0.8●	−1.6	–	−0.60	–	
		9.5		10†	−0.62	–	−0.5●	−0.9	–	−0.35	–	
		13.5		15	–	–	–	−3.5	–	–	–	
Diode Test[3] 100 µA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I	Any Input		15	–	–	–	$\pm 10^{-5}$	±1	–	–	µA

▲ For CD4514B * See Note 1

★ For CD4515B † See Note 2

Limits with black dot (●) designate 100% testing. Refer to RIC 102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS*		LIMITS		UNITS
			V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time: Strobe or Data	t_{PHL}, t_{PLH}		5	550	1100●	ns
			10	225	450●	
			15	150	–	
Inhibit			5	400	800●	
			10	150	300●	
			15	100	–	
Transition Time: High-to-Low	t_{THL}		5	100	200●	ns
			10	50	100●	
			15	40	80	
Low-to-High	t_{TLH}		5	200	400●	
			10	100	200●	
			15	60	–	
Average Input Capacitance	C_I	Any Input		5	–	pF

Limits with black dot (●) designate 100% testing. Refer to RIC–102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

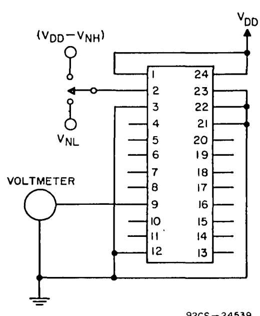


Fig. 2—Noise immunity test circuit.

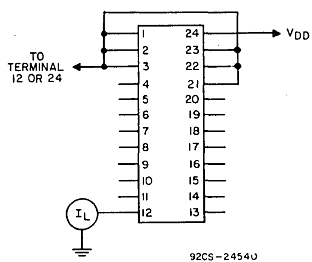


Fig. 3—Quiescent device current test circuit.

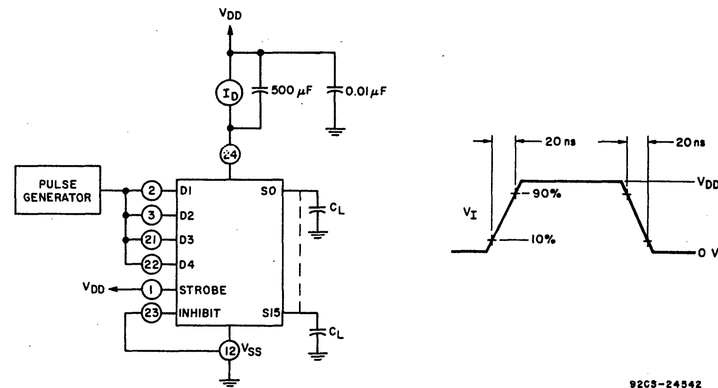


Fig. 4 —Dynamic power dissipation test circuit and waveform.

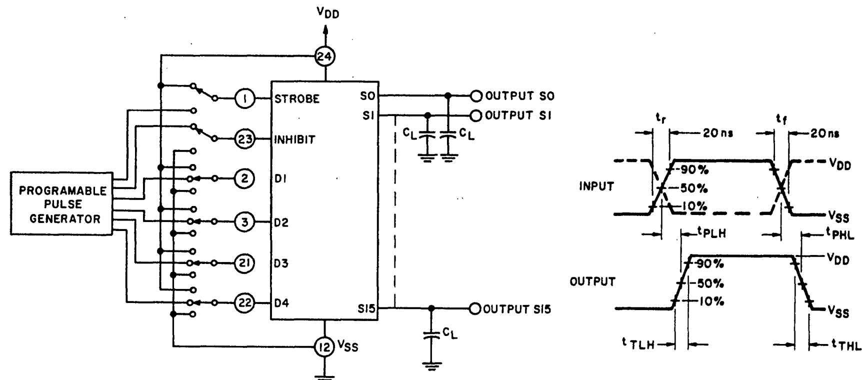
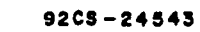


Fig.5 —Switching time test circuit and waveforms.



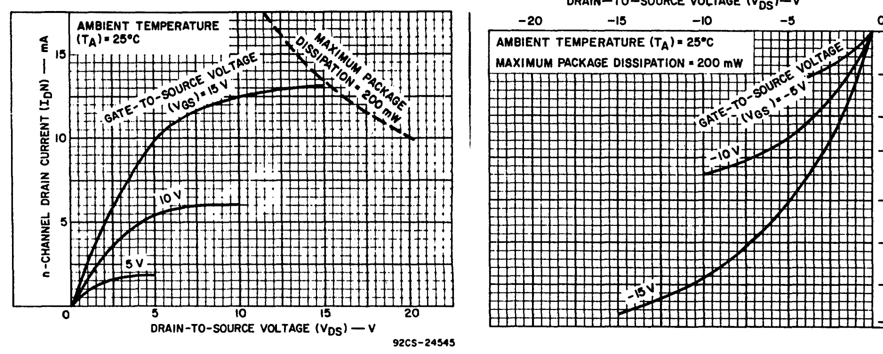


Fig. 6 —Minimum output-N-channel drain characteristics.

Fig. 7 — Minimum output-P-channel drain characteristics.

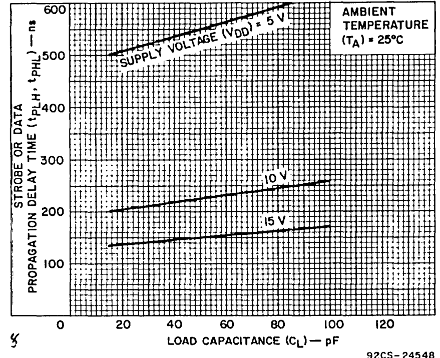


Fig.8 — Typical strobe or data propagation delay time vs. load capacitance.

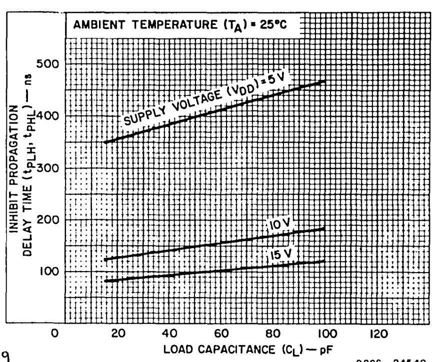


Fig.9 — Typical inhibit propagation delay time vs. load capacitance.

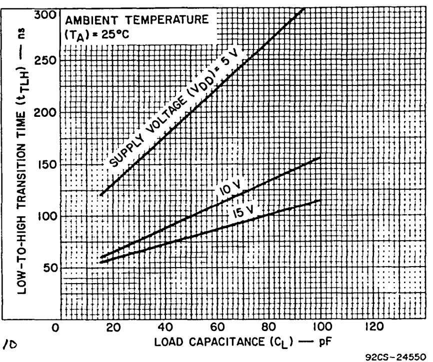


Fig.10 — Typical low-to-high transition time vs. load capacitance.

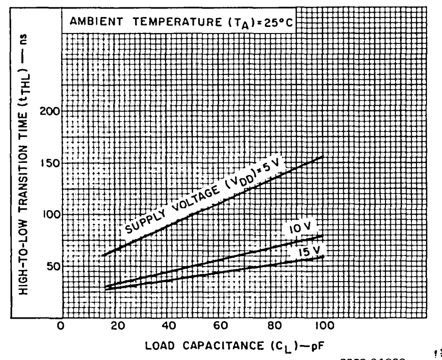


Fig.11 — Typical high-to-low transition time vs. load capacitance.

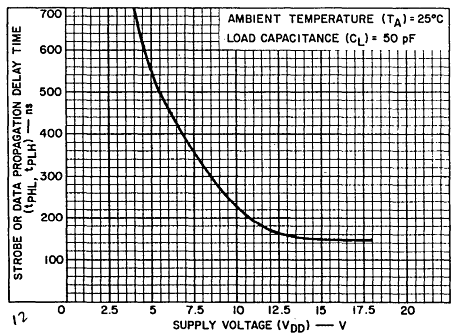


Fig.12 — Typical strobe or data propagation delay time vs. supply voltage.

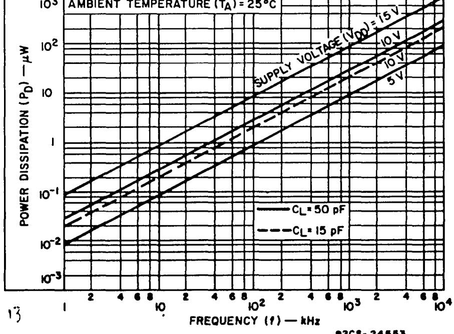


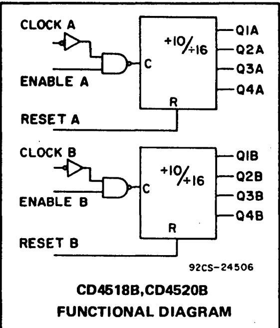
Fig.13 — Typical power dissipation vs. frequency.

Solid State
Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series CD4518B/. . ., CD4520B/. . .



CD4518B,CD4520B
FUNCTIONAL DIAGRAM

High-Reliability COS/MOS Dual Up Counters

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

CD4518B Dual BCD Up Counter
CD4520B Dual Binary Up Counter

Features:

- **Medium-speed operation — 6-MHz typical clock frequency at 10 V**
- **Positive- or negative-edge triggering**
- **Standard B-series output drive**
- **Synchronous internal carry propagation**

The RCA-CD4518B Slash (/) Series Dual BCD Up Counter and CD4520B Slash (/) Series Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the Enable input is maintained "high" and the counter advances on each positive-going transition of the Clock. The counters are cleared by high levels on their Reset lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held low.

All outputs have equal source- and sink-current capabilities and conform to standard B-Series output drive (see Static Electrical Characteristics).

These devices are electrically and mechanically identical with standard COS/MOS CD4518B, CD4520B types described in data bulletin 808 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /M, /N, and /R.

Applications:

- **Multistage synchronous counting**
- **Multistage ripple counting**
- **Synchronous frequency dividers**

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102C, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4518B, CD4520B "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care   1 ≡ High State   0 ≡ Low State

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS *		ALL TYPES LIMITS		UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
			V_{DD} Volts	Typ.	Max.		
Propagation Delay Time: Clock or Enable to Output	t_{PHL}, t_{PLH}		5 10 15	280 115 80	560● 230● –	ns	8
Reset to Output			5 10 15	330 130 90	660● 260● –	ns	8
Transition Time	t_{THL}, t_{TLH}		5 10 15	100 50 40	200● 100● 80	ns	9
Average Input Capacitance	C_I	Any Input		5	–	pF	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

* Tests are either several inputs or several outputs.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE .... –65 to +150°C
OPERATING-TEMPERATURE RANGE .... –55 to +125°C
DC SUPPLY-VOLTAGE RANGE
V_{DD} ▲ .... –0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) .... 200 mW
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. .... 265°C

▲ All voltage values are referenced to V_{SS} terminal.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units	Fig.
Supply Voltage Range	–	3	18	V	–
Input Voltage Swing (Recommended V_{SS} to V_{DD})	–	0.2 V_{DD} to 0.8 V_{DD} (Any one input)	–0.5 V to V_{DD} + 0.5 V	V	–
Enable Pulse Width	5 10 15	440 200 140	None	ns	–
Clock Pulse Width	5 10 15	200 100 70	None	ns	–
Clock Input Frequency	5 10 15	DC	1.5 3 4	MHz	–
Clock or Enable Input Rise or Fall Time	4 - 15	None	15	µs	–
Reset Pulse Width	5 10 15	250 110 80	None	ns	–

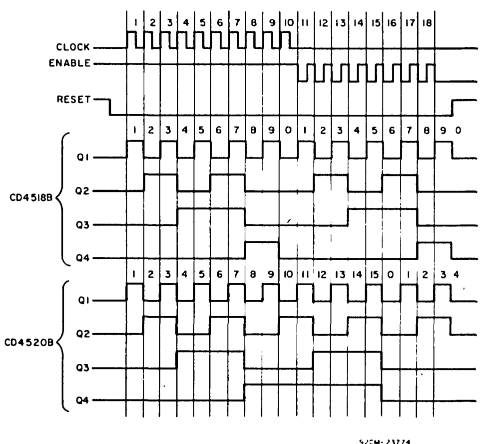


Fig. 1— Timing diagrams for CD4518B and CD4520B.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS							UNITS
			V_o	V_{DD}	−55°C		25°C			125°C		
			V	V	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device Current[1]	I_L			5	–	5	–	0.02	5	–	300	µA
				10	–	10●	–	0.02	10●	–	200●	
				15	–	–	–	0.02	–	–	–	
Output Voltage:[1] Low-Level	V_{OL}			3	–	0.55●	–	–	0.5●	–	–	V
				5	–	0.01	–	0	0.01	–	0.05	
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	0.5●	–	0.55●	
High-Level	V_{OH}			3	2.25●	–	2.3●	–	–	–	–	
				5	4.99	–	4.99	5	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	
				15	–	–	14.5●	15	–	14.55●	–	
Threshold Voltage[2] N-Channel	$V_{TH}N$	I_D = −20 µA			−0.7●	−3●	−0.7●	−1.5	−3●	−0.3●	−3●	V
P-Channel	$V_{TH}P$	I_D = 20 µA			0.7●	3●	0.7●	1.5	3●	0.3●	3●	
Noise Immunity[1]	V_{NL}		0.8, 4.2	5	1.5	–	1.5●	2.25	–	1.4	–	V
			1, 9	10	3●	–	3●	4.5	–	2.9●	–	
			1.5, 13.5	15	–	–	–	6.75	–	–	–	
	V_{NH}		0.8, 4.2	5	1.4	–	1.5●	2.25	–	1.5	–	
			1, 9	10	2.9●	–	3●	4.5	–	3●	–	
			1.5, 13.5	15	–	–	–	6.75	–	–	–	
Output Drive Current:[2] N-Channel (Sink)	I_DN		0.4	5	0.5	–	0.4●	0.8	–	0.3	–	mA
			0.5	10	1.1	–	0.9●	1.8	–	0.65	–	
			1.5	15	–	-	3	6	–	–	–	
P-Channel (Source)	I_DP		2.5	5	−2	–	−1.6●	−3.2	–	−1.2	–	mA
			4.6	5	−0.5	–	−0.4●	−0.8	–	−0.3	–	
			9.5	10	−1.1	–	−0.9●	−1.8	–	−0.65	–	
			13.5	15	–	–	−3	−6	–	–	–	
Diode Test[3] 100 µA Test Pin	V_{DF}				–	1.5●	–	–	1.5●	–	1.5●	V
Input Current	I_I		–	15	–	–	–	$\pm10^{-5}$	±1	–	–	µA

Limits with black dot (●) designate 100% testing. Refer to RIC-102C "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

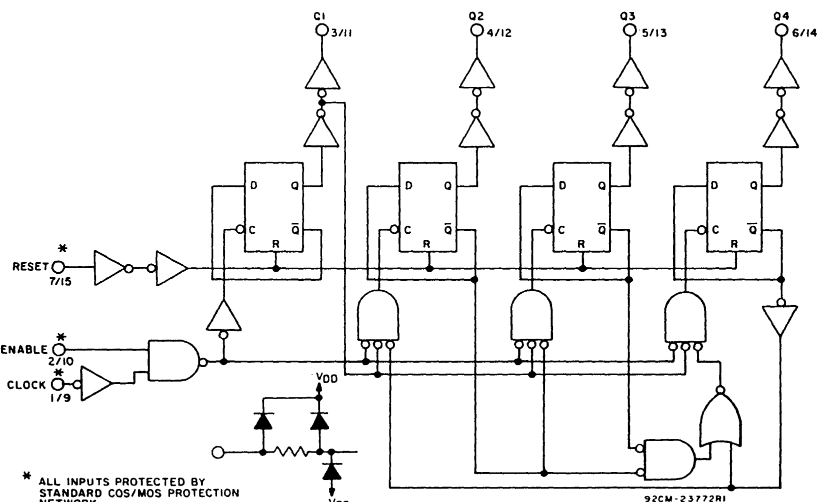


Fig. 2— Decade counter (CD4518B) logic diagram for one of two identical counters.

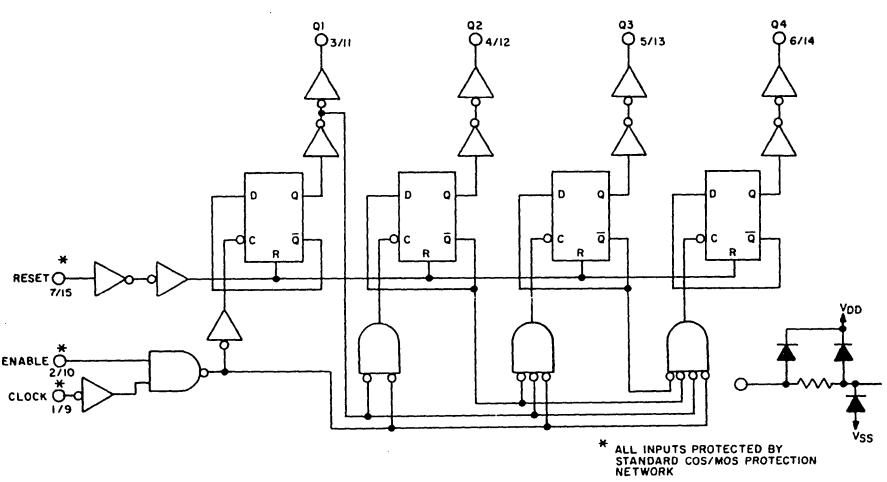


Fig. 3— Binary counter (CD4520B) logic diagram for one of two identical counters.

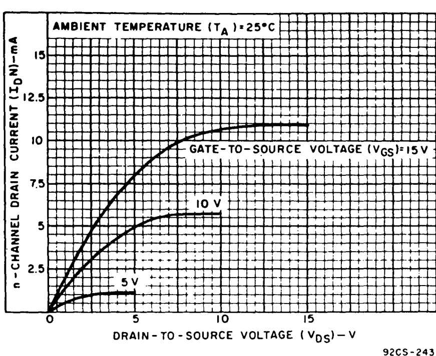


Fig. 4— Minimum output-N-channel drain characteristics.

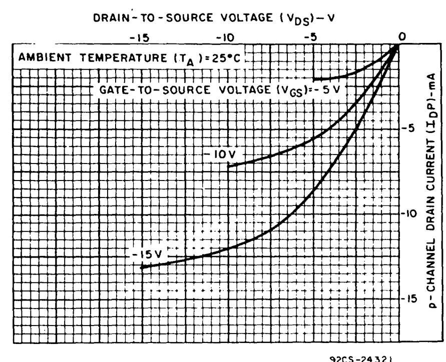


Fig. 5— Minimum output-P-channel drain characteristics.

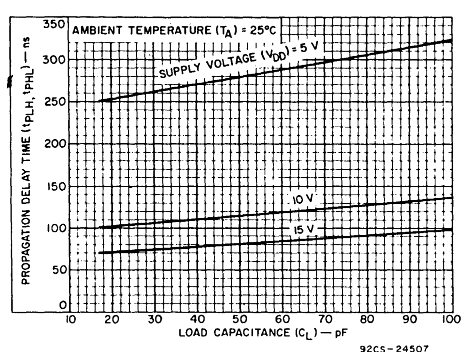


Fig. 6— Typical propagation delay vs. load capacitance (clock or enable to output).

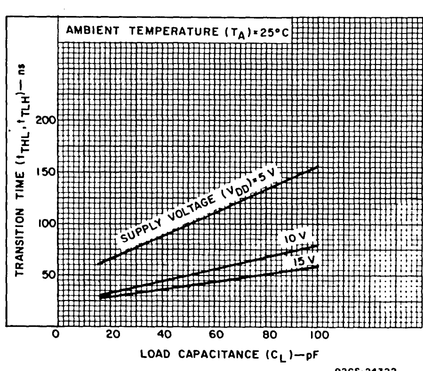


Fig. 7— Typical transition time vs. load capacitance.

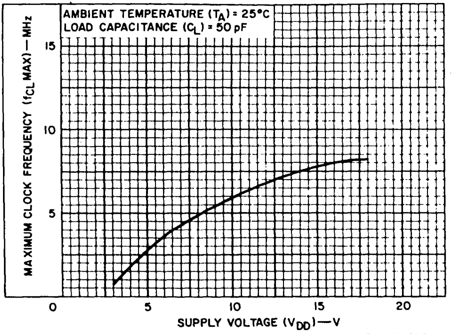


Fig. 8— Typical maximum-clock-frequency vs. supply voltage.

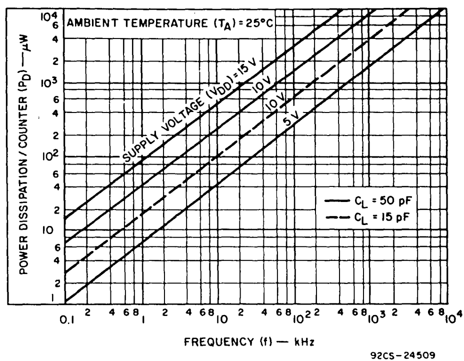


Fig. 9— Typical power dissipation characteristics.

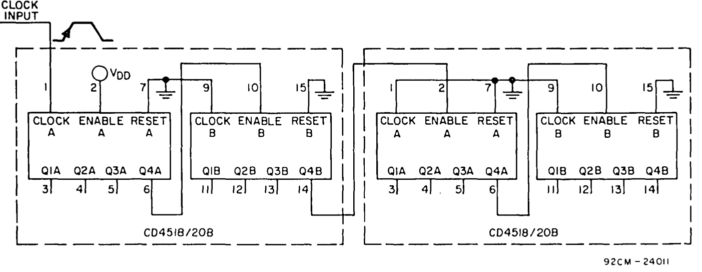


Fig. 10— Ripple cascading of four counters with positive-edge triggering.

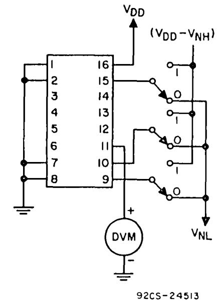


Fig. 11— Noise immunity test circuit.

Fig. 12—Synchronous cascading of four binary counters with negative-edge triggering.

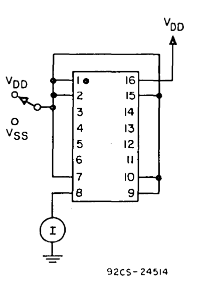


Fig. 13— Quiescent device current test circuit.

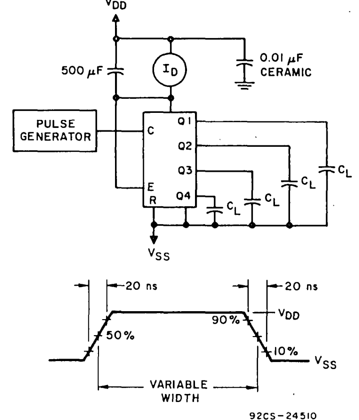
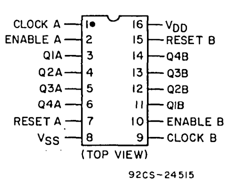


Fig. 14—Power dissipation test circuit and waveform.

TERMINAL ASSIGNMENT
CD4518B and CD4520B



Solid State Division

Digital Integrated Circuits

Application Note ICAN-6000

Handling and Operating Considerations for MOS Integrated Circuits

by S. Dansky
R. E. Funk

This Note describes practices for handling and operating MOS integrated circuits that will guard against device damage and assure optimum performance.

Handling Considerations

The input protection networks incorporated in all RCA COS/MOS devices are effective in a wide variety of device handling situations. To be totally safe, however, it is desirable to restate the general conditions for eliminating all possibilities of device damage.

Because MOS devices have extremely high input resistance, they are susceptible to damage when exposed to extremely high static electrical charges. To avoid possible damage to the devices during handling, testing, or actual operation, therefore, the following procedures should be followed:

1. The leads of devices should be in contact with a conductive material, except when being tested or in actual operation, to avoid build-up of static charge.
2. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
3. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
4. Signals should not be applied to the inputs while the device power supply is off.
5. All unused input leads must be connected to either V_{SS} (ground) or V_{DD} (device supply), whichever is appropriate for the logic circuit involved.

Table I indicates general handling procedures recommended to prevent damage from static electrical charges.

Table I – General Handling Considerations

	Should be conductive	Should be grounded to common point
Handling Equipment	X	
Metal Parts of Fixtures and Tools		X
Handling Trays	X	X
Soldering Irons		X
Table Tops	X	X
Transport Carts		(Static Discharge Straps)
Manufacturing Operating Personnel		● (Utilize grounded metal wrist straps)
General Handling of Devices		● (Utilize grounded metal wrist straps)

Total protection results when personnel and materials are all at the same or ground potential.

Dry weather (relative humidity less than 30%) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed above take on added importance and should be adhered to without exceptions.

● 1-megohm series resistor.

Handling of Unmounted Chips

In handling of unmounted chips, care should be taken to avoid differences in voltage potential. A conductive carrier, or a carrier having a conductive overlay, should be used.

Another important consideration is the sequence in which bonds are made; the V_{DD} (device supply) connection should always be made before the V_{SS} (ground) bond.

Handling of Subassembly Boards

After COS/MOS units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system in which the proper voltages are applied, the board is no more than an extension of the leads of the device mounted on the board.

It is good practice to put conductive clips or conductive tape[1] on the circuit-board terminals. This precaution prevents static charges from being transmitted through the board wiring to the devices mounted on the board.

Automatic Handling Equipment

When automatic handling equipment is used, static electricity may not always be eliminated through grounding

[1] See Table II for sources of anti-static materials.

techniques alone. Automatic feed mechanisms must be insulated from the devices under test at the point where the devices are connected to the test set. The device-insulated part of the automatic handling mechanism (anvil transport) can generate very high levels of static electricity which are developed by the continuous flow of devices sliding over and then separating from the anvil. Total control of these static voltages is critical because of the high throughputs associated with automatic handling.

Fortunately, the resolution of this problem is simple, practical, and inexpensive. Ionized-air blowers, which supply large volumes of ionized air to objects that are to be charge neutralized, are commercially available from many supply sources. Field experience with ionized-air techniques reveals this method to be extremely effective in eliminating static electricity when grounding techniques cannot be used.

Lead Bending and Forming Considerations

Other problems that can occur in handling COS/MOS devices relate to the proper handling of leads during mounting of devices. In any method of mounting integrated circuits that involves bending or forming of the device leads, it is extremely important that the leads be supported and clamped between the bend and the package seal, and that bends be made with extreme care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead flat-packaged integrated circuits, less than the lead thickness. It is also extremely important that the ends of the bent leads be perfectly straight and parallel to assure easy insertion through the holes in the printed-circuit board.

Bending, forming, and clinching of integrated-circuit leads produce stresses in the leads and can cause stresses in the seals if the above precautions are not taken. In addition, wide variations in temperature during normal use result in stresses in the device leads. Tests of 14-lead flat-pack integrated circuits, conducted under worst-case conditions in which the packages were rigidly attached to posts extending from the printed-circuit board, showed that over a temperature swing of 180°C (from −55°C to +125°C) the stress developed in the leads, the tensile pull on the leads, the shear stress introduced on the seal, and the tensile stress developed in the seal were all well within the limits for these materials. The use of thermal-stress-relief bends is, therefore, not necessary.

Soldering Time and Temperature

All device leads can withstand exposure to temperatures as high as 265°C for as long as ten seconds, and as close as 1/16 ± 1/32 inch from the body of the device.

Storing of COS/MOS Chips

COS/MOS chips, unlike most packaged devices, are non-hermetic devices, fragile and small in physical size, and therefore require the following special handling considerations:

1. Chips must be stored under proper conditions to assure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the storage temperature should not exceed 40°C and the environment should be clean, dust-free, and less than 50% relative humidity.
2. After mounting and bonding, these non-hermetic chips should not be subjected to moist or contaminated atmospheres that might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

For further information on COS/MOS chip handling, refer to File No. 517, "CD4000AH Series COS/MOS Chips".

Storing of Printed-Circuit Boards

Excessive humidity (greater than 60%) should be avoided during circuit-board check-out to prevent the false impression of excessive device internal leakage. High relative humidity may cause leakage paths between closely spaced elements of the circuit boards, such as the terminals and insulated metallized connection strips. Normally this added leakage is not significant in non-COS/MOS devices. However, when the nanoampere-leakage advantages of COS/MOS devices are desired, leakage currents on circuit boards or non-hermetic modules which are affected by high humidity become of major concern and must be controlled by coating, cleaning, or better environmental controls.

Effects of Humidity on Static Electricity

Dry weather (relative humidity less than 30%) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed in Table I take on added importance and should be adhered to without exceptions.

Electrical Failure Modes Due To Improper Handling

When the possibilities exist for appreciable static-energy discharge, and proper handling techniques are not used, electrical damage can result as follows:

(a) shorted input protection diodes,
(b) shorted or open gates,
(c) opening in metal paths from the device input.

The presence of this type of device damage can be detected by curve-tracer checks of the input protection diodes of the gate-oxide protection circuits described on page 3, and also by a check of the device characteristics, especially mutual transconductance (gm).

Operating Considerations

Maximum Ratings	CD4000A Series
Storage-Temperature Range	-65 to +150°C
Operating-Temperature Range:	
Ceramic-Package Types	-55 to +125°C
Plastic-Package Types	-40 to + 85°C
DC Supply-Voltage Range:	
$V_{DD} - V_{SS}$	-0.5 to +15 V
$V_{DD} - V_{EE}$	-0.5 to + 15 V
$V_{CC} - V_{SS}$	-0.5 to +15 V
DC Input-Voltage Range	$V_{SS} \leqslant V_I \leqslant V_{DD}$
for CD4009A, CD4010A	$V_{SS} \leqslant V_I \leqslant V_{DD} \geqslant V_{CC}$
for CD4049A, CD4050A	$V_{SS} \leqslant V_I \leqslant 15$ V
for CD4051A, CD4052A, CD4053A:	
Controls	$V_{SS} \leqslant V_I \leqslant V_{DD}$
Signals	$V_{EE} \leqslant V_I \leqslant V_{DD}$
Device Dissipation (per package)	200 mW
Lead Temperature (during soldering) at a distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds maximum	+ 265°C

Operating Voltage

When operating near the maximum supply-voltage range of 15 volts, care should be taken to avoid or suppress power-supply turn-on or turn-off transients, power-supply ripple or regulation, and ground noise; any of the above conditions must not cause $(V_{DD} - V_{SS})$ to exceed the absolute maximum rating.

Power supplies should have a current compliance compatible with actual COS/MOS current drain.

Another good power-supply practice is to use a zener protection diode in parallel with the power bus. The zener value should be above the expected maximum regulation excursion, but should not exceed 15 volts. Fig. 1 illustrates a practical zener shunt circuit. A current-limiting resistor is included if the supply-current compliance is higher than the zener power-dissipation rating for a given zener voltage. The shunt capacitance value is chosen to supply required peak current switching transients.

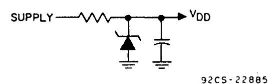


Fig. 1 – Zener-diode shunt circuit.

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type (such as the CD4009A, CD4010A, CD4041A, CD4049A, CD4050A) not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Another consideration with these high-current types is that a pull-up resistor from their inputs to V_{SS} or V_{DD} should be used if there is any possibility that the device may become temporarily unterminated (e.g., if the printed circuit board driving the high-current types is removed from the chassis). A useful range of values for such resistors is from 0.2 to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of typically less than 10 milliamperes. Input signal interfaces having the allowable 0.5 volt above V_{DD} or below V_{SS}, respectively, should be current-limited to typically 10 milliamperes or less.

Whenever the possibility of exceeding 10 milliamperes of input current exists, a resistor in series with the input is recommended. The value of this resistor can be as high as 10 kilohms without affecting static electrical characteristics. Speed, however, will be reduced due to the added RC delay. Particular attention should be given to long input-signal lines where high inductance can increase the likelihood of large signal pickup in noisy environments. In these cases, series resistance with shunt capacitance at the IC input terminals is

recommended. The shunt capacitance should be made as large as possible consistent with the system speed requirements.

Interfacing with T^2L Devices

The COS/MOS hex buffers (CD4009A, CD4010A, CD4049A, and CD4050A) are designed to drive two normal-power T^2L loads. Other device types (such as the CD4041A, CD4048A, and CD4031A) can also directly drive at least one T^2L load. Always consult the published data on the particular COS/MOS type for this capability. Most gates and inverters and some MSI types can drive one or more low-power T^2L loads. To provide a good noise margin in the logic "1" state, T^2L devices that drive COS/MOS devices require a pull-up resistor at the COS/MOS input. The COS/MOS hex buffers can also convert COS/MOS logic levels (5 to 15 volts) to T^2L logic levels (5 volts), i.e., down-level conversion.

Rules for safe system design when COS/MOS interfaces with T^2L and both logic systems have independent power supplies of the same voltage level but possibly on at different times are as follows:

a) T^2L driving COS/MOS – use 1 kilohm in series with COS/MOS input

b) COS/MOS driving T^2L – connect directly

Interfacing with p-MOS Devices

COS/MOS devices can operate at $V_{DD} = 0$ and $V_{SS} = -3$ to -15 volts to interface directly with p-MOS devices with no degradation in noise immunity or other characteristics.

Interfacing with n-MOS Devices

COS/MOS devices can be interfaced directly with n-MOS devices over the +3 to +15 volt range of power supplies.

Fan-Out – COS/MOS to COS/MOS

All RCA COS/MOS devices have a dc fan-out capability of 50. The reduction in COS/MOS switching speed caused by added capacitive loading should, however, be consistent with high-speed system design. The input capacitance is typically 5 pF for most types; the CD4009A and CD4049A buffers have an input capacitance of typically 15 pF.

Maximum Clock Rise and Fall Time

All COS/MOS clocked devices show maximum clock rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly.

Parallel Clocking

When two or more different COS/MOS devices use a common clock, the clock rise time must be kept at a value less than the sum of the propagation delay time, the output transition time, and the setup time. Most flip-flop and shift-register types are included in this rule and are so noted in the individual data sheets.

Noise Immunity

COS/MOS inputs normally switch at 30 to 70 per cent of the power-supply voltage. For example, for a 10-volt supply, a logic "0" is 0 to 3 volts, and a logic "1" is 7 to 10 volts. For 5-volt operation, a logic "0" is 0 to 1.5 volts, and a logic "1" is 3.5 to 5 volts. COS/MOS noise immunity is 30 per cent of the supply voltage for the range from +3 to +15 volts.

The inherent 30-per-cent noise immunity of COS/MOS also permits a 1-volt noise margin when interfaced with T^2L or DTL. For example, standard T^2L and DTL interfacing with COS/MOS at a nominal $V_{DD} = V_{CC} = 5$ volts provides at least 1-volt noise margin; i.e., $V_{OL}max(T^2L) = 0.4$ volt and $V_{OL}min(DTL) = 0.45$ volt; 30% of 5 volts = 1.5 volts.

This example applies typically to the 5400/7400 series, the 9000 series, and the 8000 series. HI NIL (300 series) can interface with COS/MOS at a nominal $V_{DD} = V_{CC} = 12$ volts with a worst-case noise margin of 2.1 volts.

Because COS/MOS voltage-transfer switching characteristics vary from 30 to 70 per cent of the supply voltage, system designers employing COS/MOS multivibrators, level detectors, and RC networks must consider this variation. Application Note ICAN-6267 illustrates an accurate multivibrator design technique which minimizes the switching-point variation.

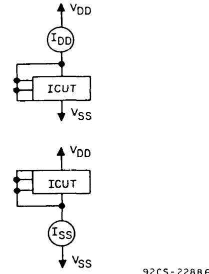
Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can cause the device power dissipation to exceed the safe value of 200 milliwatts for high-output-current types such as the CD4007A, CD4009A, CD4010A, CD4041A, CD4049A, and CD4050A. In general, outputs of these types can all be safely shorted when operated with $V_{DD} - V_{SS} \leq 5$ volts, but may exceed the 200-milliwatt dissipation rating at higher power-supply voltages. For cases in which a short-circuited load, such as the base of a p-n-p or n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for safe operation below 200 milliwatts.

COS/MOS Characteristics

Quiescent Device Leakage Current (I_L):

Quiescent device leakage is measured for inputs tied high (I_{DD}) and also for all inputs tied low (I_{SS}), as illustrated below:



Quiescent Device Dissipation (P_D):

Quiescent device dissipation is given by

$$P_D = (V_{DD} - V_{SS})\, I_L$$

where $I_L = I_{DD}$ or I_{SS}

Output Voltage Levels (COS/MOS driving COS/MOS):

V_{OL} = Low-Level("0")Output = 10 mV* at 25°C
V_{OH} = High-Level("1")Output = V_{DD} - 10 mV* at +25°C

Noise Immunity:
V_{NL} = the maximum noise voltage that can be applied to a logic "0" input (added to V_{SS}) before the output changes state.
V_{NH} = the maximum noise voltage that can be applied to a logic "1" input (subtracted from V_{DD}) before the output changes state.

Output Drive Current:
Sink Current (I_DN) = the output sink current provided by the n-channel transistor without exceeding a given output voltage (V_o) as shown on each data sheet.
Source Current (I_DP) = the output source current provided by the p-channel transistor without dropping below a given output voltage (V_o) as shown on each data sheet.

Input Current (I_I):
Input current is typically 10 picoamperes (3 to 15 volts) at T_A = 25°C. Maximum input currents for COS/MOS devices are normally below 10 nanoamperes at 15 volts, and below 50 nanoamperes at T_A = +125°C.

AC (Dynamic) Characteristics:
Test parameters shown in the published data are measured at T_A = 25°C with a 15-pF load and an input-signal rise or fall time of 20 nanoseconds. Actual system delays and transition times may be increased due to longer input rise and fall times. Graphs are included in the individual data sheets to illustrate typical variation of delays and transition times with capacitive loading. The designer should use a typical temperature coefficient of 0.3%/°C for estimating speeds at temperatures other than +25°C. Propagation delays and transition times increase with rising temperature; maximum clock input frequencies decrease with rising temperatures.

Dynamic power dissipation for each device type is shown graphically in the published data as a function of device operating frequency.

* This voltage may be difficult to measure depending on accuracy, resolution, and offset voltage of test equipment used. Although device output "1" or "0" limits to which RCA tests in manufacture are 10 millivolts, a value of 50 millivolts may be used for customer measurements without compromise of device quality or system performance.

Gate-Oxide Protection Circuits

Most COS/MOS gate inputs have the protection shown in Fig. 2. An exception to this statement is the input network for the CD4049A and CD4050A shown in Fig. 3. Figs. 4 and 5 illustrate the protection diodes inherently present at all transmission-gate input/output terminals and all inverter outputs. ICAN-6218 gives further information on protection circuits.

The protection networks can typically protect against 1-2 kilovolts of energy discharge from a 250-pF source.

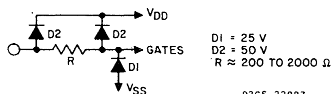


Fig. 2 – Normal gate-input-protection circuit.

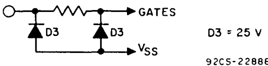


Fig. 3 – CD4049A/CD4050A gate-input-protection circuit.

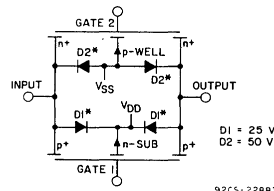


Fig. 4 – Transmission gate-input-output protection.

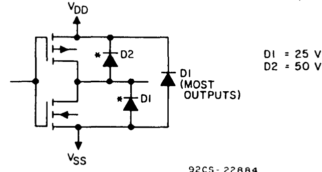


Fig. 5 – Active (inverter) output protection.

* THESE DIODES ARE INHERENTLY PART OF THE MANUFACTURING PROCESS

Table II – Partial List of Materials and Equipment Available for the Control of Static Charge

Company	Conductive Foam	Conductive Envelopes	Static Neutralizing Air Blowers	Anti-Static Sprays	Conductive Tape
Custom Material Inc. Chelmsford, Mass.	Velofoam #7672	Velobags #1798M	TEC Dynastat DS120		P. C. Contab Shunt
3M Company St. Paul, Minn.			Ionized Air Blower #905	See Technical Bulletins	Scotch Shielding Tapes
Scientific Enterprises, Inc. Bloomfield, Colo.			Micro Stat 575 Portable Ionizer		
Emerson & Cuming, Inc. Canton, Mass.	ECCOSORB LD26			See Technical Bulletins	

Solid State Division

Digital Integrated Circuits

Application Note ICAN-6224

Radiation Resistance of the COS/MOS CD4000A Series

by M. N. Vincoff

Complementary MOS (COS/MOS) integrated circuits possess many advantages which recommend their use in radiation-susceptible space and military environments. Several of the most significant of these advantages are: ultra-low standby-power consumption, high noise immunity,[1] extremely high packaging density, and inherently high reliability.[2] These advantages, along with the improved radiation resistance of the RCA CD4000A series over the CD4000 series described in earlier radiation studies,[3] exhibit the maturity reached by the MOS technology since 1971.

A number of studies of the radiation resistance of complementary MOS devices by NASA, the Navy and various companies in the space industry have revealed two areas of prime concern.[4-15] The first, *permanent* radiation exposure, as experienced in a space environment, causes a shift in threshold or switching voltage and a possible increase in leakage current, I_L. The second, *transient* radiation exposure, as experienced in an atomic environment, causes the output-voltage levels to respond to a pulse of ionizing radiation; this effect could change the state of the logic circuitry and require resetting of that circuitry for proper equipment or system operation.

Permanent-Radiation Resistance

The CD4000 series was resistant to permanent radiation levels of 2×10^4 rads (approximately 10^{12} e/cm^2). Now, however, RCA CD4000A-series devices without special shielding have been found to be resistant to radiation levels up to 2×10^5 rads (approximately 10^{13} e/cm^2), as shown in Fig. 1.[3] In this figure the change in switching voltage ΔV_S is plotted as a function of dose. The value of ΔV_S was calculated from the average value of ΔV_{TN} and ΔV_{TP} for the devices mentioned. The new radiation level of the CD4000A series represents a significant improvement over the CD4000 series. In addition, with minimal shielding (for example, 1/16-inch of aluminum) the CD4000A series can be used in application with levels of radiation up to 3×10^6 rads (approximately 10^{14} e/cm^2).

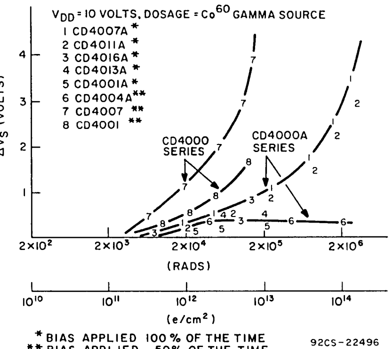


Fig. 1 – Permanent radiation resistance of CD4000A- and CD4000-series devices.

Transient-Radiation Resistance

The resistance of the CD4000A series to transient radiation is expected to be ten times better than that of the CD4000 series, which can withstand pulses of radiation of approximately 10^{10} rads/s.[5]

Design Considerations

The resistance of the CD4000A-series devices to either permanent- or transient-radiation exposure can be increased by providing either minimal shielding through the design of the equipment enclosure containing the devices or by locating the devices deep within the equipment in which they are used. In any case, the action taken will depend on the constraints dictated by the radiation environment imposed by the system or program. Each application must be tested and the results analyzed with the data in this Note as criteria. Test items to be considered are radiation environment, which

will vary greatly depending on dosage rate; time of exposure; amount of normal shielding; distance of the device from the radiation source; shielding afforded by the atmosphere; power-supply voltage selection; and switching cycles used during exposure. For example, consider the effects of permanent radiation on two spacecraft in 90-degree orbits at 600 and 1500 nautical miles from the earth, respectively. The dose-depth is determined as shown in the curves of Fig. 2. In these curves the dose in rads(Al)/day is plotted as a function of the thickness of spacecraft aluminum required to shield the devices from trapped electrons and protons.[4]

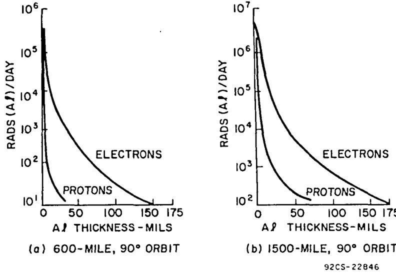


Fig. 2 – Dose-depth curves for trapped electrons and protons in spacecraft in orbit.

Conclusion

The RCA COS/MOS CD4000A series exhibits improved radiation resistance over the CD4000 series, and is well suited for use in many applications in which permanent and transient radiation effects are factors. When stringent radiation requirements are imposed, additional shielding can be employed to increase the radiation life of COS/MOS CD4000A-series devices to any desired level, i.e., to make their radiation resistance equivalent to that of bipolar devices.

Custom COS/MOS devices that can resist a radiation level of 10^6 rads are now being developed by means of an aluminum implantation process which requires one additional masking step in the production line.[11-14]

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Solid State Division

Digital Integrated Circuits

High-Reliability COS/MOS CD4000A Slash (/) Series Types

Screened to MIL-STD-883

RCA COS/MOS high-reliability slash (/) series digital integrated circuits are available for applications in aerospace, military, and industrial equipment. These COS/MOS circuits are supplied to six screening levels (/1N, /1R, /1, /2, /3, /4) which meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. These six screening levels are equivalent to MIL-STD-883 Classes A, B, and C and are summarized in Table 1.

RCA also offers standard commercial product with a 168-hour burn-in, designated level /5.

This bulletin defines the test procedures employed with COS/MOS devices to meet the reliability standards required by MIL-STD-883. The level /1N part includes SEM (Scanning Electron Microscope) Inspection to NASA-Goddard Specification GSFC-S-311-P-12A of MIL-M-38510, and Precap Visual Inspection, Condition A, Method 2010-1, MIL-STD-883. The level /R part includes the SEM inspection in addition to the requirements of level /1 part. RCA also offers the CD4000A slash (/) series screened to MIL-M-38510 (Slash (/) 050-Series Types). For COS/MOS devices in this series, refer to RIC-104A, "High-Reliability COS/MOS MIL-M-38510 CD4000A-Series Types".

The Product Flow Diagram shown in Fig. 1 lists a summary of processing, screening tests, and sampling procedures followed in the manufacture of high-reliability COS/MOS devices.

Table 2 gives detailed information for the screening tests included in the Product Flow Diagram. Table 3 gives pre burn-in and post burn-in electrical tests and delta limits for critical test parameters. Tables 4 and 5 give test criteria for Final Electrical and Group A Electrical Tests. Tables 6 and 7 describe Group B and C Environmental Sampling Inspection tests.

MIL-STD-883 2010.1A OR 2010.2B
PRECAP VISUAL
SEM INSPECTION AS REQUIRED
PRESEAL BAKE
SEAL AND LOT IDENTIFICATION
CONDITIONING SCREENS: STABILIZATION BAKE, THERMAL SHOCK, TEMPERATURE CYCLING, MECHANICAL SHOCK, CENTRIFUGE, FINE LEAK, GROSS LEAK
SERIALIZE
PRE BURN-IN ELEC.
BURN-IN
POST BURN-IN ELECTRICAL
FINAL ELECTRICAL
GROUP A
RADIOGRAPHIC INSPECTION
EXTERNAL VISUAL
LEVEL /1N
LEVEL /1R
LEVEL /1
LEVEL /2
CONDITIONING SCREENS: STABILIZATION BAKE, TEMPERATURE CYCLING, CENTRIFUGE, FINE LEAK, GROSS LEAK
ELECTRICAL TESTS
B GROUP
C GROUP
LEVEL /3
LEVEL /4
STANDARD COMMERCIAL PRODUCT
168-HOUR BURN-IN
LEVEL /5
92CL-24949

Fig. 1 – Product flow diagram. See Tables 2, 4, 5, 6, and 7 for details.

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Table 1 — Description of RCA Integrated-Circuit Screening Levels

Screening Levels▲		Application	Description
RCA Levels	Equivalent to MIL-STD-883, Method 5004.1		
For Packaged Devices			
/1N	Class A with SEM* Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **impossible and reliability is imperative**
/1R	Class A with SEM* Inspection and Condition B Precap Visual Inspection		
/1	Class A with Condition B Precap Visual Inspection		
/2	Class A with Condition B Precap Visual Inspection. Radiographic Inspection Omitted	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **extremely difficult or impossible and reliability is imperative**
/3	Class B	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement **can be performed but are difficult and expensive**
/4	Class C	Military and Industrial For example, in Ground-Based Electronics	For devices intended for use where replacement **can readily be accomplished**
/5 Standard commercial plus burn-in	—	Commercial and Industrial	For devices intended for use where a higher level of reliability is required than can be provided by product without a burn-in
For Chips■			
/N	SEM* Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For hybrid applications where maintenance and replacement **are extremely difficult and reliability is imperative**
/R	SEM* Inspection and Condition B Precap Visual Inspection		
/M	Condition B Precap Visual Inspection	Military and Industrial	For general applications

*SEM — Scanning Electron Microscope Inspection per NASA Specification GSFC-S-311-P-12
▲For details on Condition A and Condition B Precap Visual Inspection, refer to MIL-STD-883 Method 2010.1
■ Lot acceptance testing for chips is available on a custom basis

Ordering Information

1. Packaged Device and Chip Type Number Identification

When ordering a packaged device or a chip, it is important that the desired Screening Level and Package Designation for the Packaged Device, and the desired Screening Level for the Chip Version indicated by the appropriate suffix letters be added to the Part Number as shown below. For example, a CD4024A in a 14-lead dual-in-line ceramic package and processed to meet MIL-STD-883 Class A requirements with SEM Inspection plus Condition A Precap Visual would be identified as the CD4024AD/1N. In similar manner, a CD4024A Chip having SEM inspection plus Condition A Precap Visual would be identified as the CD4024AH/N.

2. Data Supplied With Order for Packaged Devices

	For the Following RCA Screening Levels
a) Product Screening Data	
Certificate of Compliance Signed by RCA Representative – Provides lot identity, customer order identity, lists and certifies tests, methods and conditions of required processing per MIL-STD-883	All except /5
Group A Subgroup – Test Summary Attributes Data	All except /5
Variables Data, Pre Burn-In and Post Burn-In	/1N, /1R, /1, /2
Radiographic Inspection Film and Film Inspection Record	/1N, /1R, /1
SEM Inspection Certificate of Compliance to NASA Specification GSFC-S-311-P-12 Includes lot identification and one worst-case photograph	/1N, /1R

b) Lot Quality Conformance Data –

Group B and Group C Subgroups

Attributes Data Summary of the Latest Group B and/or Group C Subgroup can be ordered at a nominal charge.

Special Group B and/or Group C quality conformance tests on samples from the specific lot of parts ordered will be considered on a custom basis only.

Description of RCA COS/MOS IC High-Reliability Part Numbers

Packaged Device CD4000AD/1N

CD4000A	D	/1N
Type Designation	Package Suffix Letter: D = Dual-in-Line Ceramic Weld-Seal K = Ceramic Flat Pack F = Dual-in-Line Ceramic Frit-Seal	Screening Level: /1N /2 /1R /3 /1 /4 /5 For Description, See Table 1

Chip Version, CD4000AH/N

CD4000A	H	/N
Type Designation	Package Suffix Letter: H = Chip Version	Screening Level: /N /R /M For Description, See Table 1

Table 2 – Description of Total Lot Screening (X = 100% Testing)

Test	Conditions	MIL-STD-883		RCA Screening Levels*					
		Method	Conditions	/1N	/1R	/1	/2	/3	/4
SEM Inspection	NASA Per GSFC-S-311-P-12	–	–	X	X	–	–	–	–
Precap Visual	–	2010.1	A	X	–	–	–	–	–
Precap Visual	–	2010.1	B	–	X	X	X	X	X
Preseal Bake	16 to 32 hrs at 200°C	–	–	X	X	X	X	X	X
Seal & Lot Identification	–	–	–	X	X	X	X	X	X
Stabilization Bake	48 hrs. at 150°C	1008	C	X	X	X	X	X	X
Thermal Shock	15 cycles	1011	C	X	X	X	X	–	–
Temperature Cycling	10 cycles	1010	C	X	X	X	X	X	X
Mechanical Shock	5 pulses, Y_1 direction	2002	B	X	X	X	X	–	–
Centrifuge	Y_2, Y_1 direction	2001	E	X	X	X	X	–	–
	Y_1 direction only	2001	E	–	–	–	–	X	X
Fine Leak	–	1014	A	X	X	X	X	X	X
Gross Leak	–	1014	C	X	X	X	X	X	X
Electrical Tests	See Note 1	–	–	X	X	X	X	X	–
Serialize	–	–	–	X	X	X	X	–	–
Pre Burn-in Electrical	see Table 3	–	–	X	X	X	X	–	–
Burn-in	240 hours	1015	D or E	X	X	X	X	–	–
	168 hours	1015	D or E	–	–	–	–	X	–
Post Burn-in Electrical	Delta Requirements (See Table 3)	–	–	X	X	X	X	–	–
Final Electrical	–	–	–	–	–	–	–	–	–
a) 25°C	see Table 4	–	–	X	X	X	X	X	X
b) −55 and +125°C	see Table 4	–	–	X	X	X	X	X	S
Radiographic Inspection	1 view	2012	–	X	X	X	–	–	–
External Visual	–	2009	–	X	X	X	X	X	X

Note 1: See specific type data bulletin for test conditions and limits

* RCA screening level /5 consists of a 168-hour burn-in screen performed on standard commercial product. The ambient test temperature is the maximum possible without exceeding device thermal ratings. After burn-in, /5 devices meet all of the electrical requirements specified in the appropriate commercial data bulletin. Reference: RCA DATABOOK SSD-203.

Table 3 – Pre and Post Burn-In Electrical Tests and Delta Limits (T_A = 25°C)

CRITICAL PARAMETERS (at V_{DD} = 10 V)	SYMBOLS	LIMIT VALUES: For specific CD4000A Series Types and corresponding Δ limits for High-Reliability Versions *									
QUIESCENT DEVICE CURRENT	Total I_L(max)	0.1	0.5	1	2	5	10	15	25	50	Unit µA
	ΔI_L	0.05	0.2	0.3	0.5	1.0	1.3	1.5	2.5	5.0	µA
THRESHOLD VOLTAGE: "N" Channel	ΔV_{TH}"N"	←±0.3→									V
"P" Channel	ΔV_{TH}"P"	←±0.3→									V
DEVICE DRAIN CURRENT: Total	Total I_{DS}(min)	-0.1 - 0.5		0.5 - 2	2 - 5	5 - 10	10 - 25		25 - 50		mA
"N" Channel	ΔI_{DS}"N"	±0.1		±0.5	±0.75	±1	±2		±5		mA
"P" Channel	ΔI_{DS}"P"	±0.1		±0.5	±0.75	±1	±2		±5		mA

* For example, if a specific CD4000A Series type has a maximum quiescent device current of 0.5 µA at T_A = 25°C, RCA will test to a Δ limit of 0.2 µA for the high-reliability version of that type. In a similar manner, if a type has a quiescent device current rating of 5 µA, RCA will test to a Δ limit of 1.0 µA.

Table 4 — Final Electrical Tests

TEMPERATURE (T_A)	TEST	TEST CRITERIA		
		LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
+25°C	Selected Static Parameters	100%	100%	100%
+125°C	Selected Static Parameters	100%	100%	–
-55°C	Selected Static Parameters	100%	100%	–
+25°C	Selected Dynamic Parameters	100%	100%	–

Table 5 — Group A Electrical Sampling Inspection

SUBGROUP	TEST	CONDITION	LTPD		
			LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Selected Static Parameters	T_A = +25°C	5	5	5
2	Selected Static Parameters	T_A = +125°C	5	7	10
3	Selected Static Parameters	T_A = -55°C	5	7	10
4	Selected Dynamic Parameters	T_A = +25°C	5	5	5

Details of static and dynamic tests, conditions, and limits appear in the High-Reliability Devices DATABOOK SSD-207. Tested static and dynamic characteristics are identified for each Slash (/) Series type by a dot (•)

Table 6 — Group B Environmental Sampling Inspection (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Physical Dimensions	2008	Test Cond. A per applicable data sheet	10	15	20
2	Marking Permanency	2008	Test Cond. B per Par. 3.2.1	4 devices (no failures)		
	Visual and Mechanical	2008	Test Cond. B 10 X mag.	1 device (no failure)		
	Bond Strength	2011	Test Cond. D 10 Devices minimum	5	15	20
3	Solderability	2003		10	15	15
4	Lead Fatigue	2004	Test Cond. B2 any 5 leads	10	15	15
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			

Note 1: Group B tests are performed on each inspection lot per requirements of MIL-M-38510.
Note 2: Operating life circuits are included in specific type high-reliability data bulletins.

Table 7 – Group C Environmental Sampling Inspection (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Thermal Shock	1011	Test Cond. C	10	15	15
	Temperature Cycling	1010	Test Cond. C			
	Moisture Resistance	1004	No Voltage Applied			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests – Note 3					
2	Mechanical Shock	2002	Test Cond. B, 0.5 ms	10	15	15
	Vibration, Var. Freq.	2007	Test Cond. A			
	Constant Acceleration	2001	Test Cond. E			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Test – Note 3					
3	Salt Atmosphere	1009	Test Cond. A Omit Initial Conditioning	10	15	15
4	High Temp. Storage Critical Post Tests – Note 3	1008	Test Cond. C 1000 hours	7	7	7
5	Operating Life Critical Post Tests – Notes 2 and 3	1005	T_A = 125°C, 1000 hrs. Test Circuit (Note 2)	5	5	5
6	Steady State Bias Critical Post Tests – Note 3	1015	Test Cond. A, 72 hrs. At T_A = 150°C (Note 3)	7	–	–

Note 1: Group C tests are performed at 3-month intervals for reliability history.
Note 2: Operating life circuits are included in specific type high-reliability data bulletins.
Note 3: Static parameters and limits are shown in High-Reliability Devices DATABOOK SSD-207, and in specific type high-reliability data bulletins.

Solid State Division

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High-Reliability COS/MOS MIL-M-38510 CD4000A Series Types

RCA COS/MOS high-reliability digital integrated circuits are available for applications in aerospace, military, and industrial equipment where screening requirements of MIL-M-38510 are specified. COS/MOS circuits are supplied to the three screening classes of MIL-M-38510 as specified in MIL-STD-883 Method 5004 Classes A, B, and C. Table 1 describes the screening levels.

This bulletin defines the procedures employed to manufacture COS/MOS CD4000A Series devices to meet the reliability requirements of MIL-M-38510. These COS/MOS devices are available in flat pack and dual-in-line ceramic packages.

Since 1970, RCA has been working closely with various aerospace and military agencies to qualify and provide COS/MOS devices to MIL-M-38510 specifications. Among these agencies are the NASA Goddard Space Flight Center, NASA Marshall Space Flight Center, NASA Headquarters Center in Washington, Rome Air Development Center, and the Defense Electronic Supply Center (DESC) at Dayton, a branch of the Defense Supply Agency.

MIL-M-38510 is the general specification for integrated circuits and is more comprehensive than MIL-STD-883. This general specification, introduced a year after MIL-STD-883 was in existence, adds a number of quality constraints not included in MIL-STD-883, which is a specification of test methods, procedures, and screening tests. COS/MOS parts are provided to MIL-M-38510 under a series of /050 numbers of which nine are in existence. These nine numbers cover twenty-seven COS/MOS types. Parts meet requirements similar to those of Classes A, B, and C of MIL-STD-883, Method 5004 screening, except that additional requirements, including more test conditions and tightened limits, are imposed. The Product Flow Diagram shown in Fig. 1 lists a summary of processing, screening tests, and sampling procedures followed in the manufacture of high-reliability COS/MOS devices. The additional criteria for each class of product are indicated by an X in Table 2. Also provided in MIL-M-38510 tests are PDA's (Per-Cent Defective Allowable) of 10 per cent for the three burn-in operations performed on Class A product, and 10 percent for the one burn-in of Class B product. Table 3 provides a list of the COS/MOS devices for which MIL-M-38510 /050-number specification sheets have been written. The /054(CD4008A) and /058(CD4016A) types are still in preliminary status and are available for custom screening. Table 4 compares the screening requirements for COS/MOS integrated circuits to Class A Parts of MIL-M-38510. Tables 5 and 6 give test criteria for Final Electrical and Group A Electrical Tests. Tables 7 and 8 describe Group B and C Environmental Sampling Inspection tests. Table 9 describes the product-assurance program RCA implements in the performance of MIL-M-38510. Table 10 provides a classification guide for COS/MOS circuits.

The processing of high-reliability COS/MOS integrated circuits is shown in Fig. 3. The wafer processing and metallization steps, the wafer finishing operations, and the wafer testing are the same as for standard-product COS/MOS devices. For Class A parts, an SEM inspection step is inserted after the wafer processing and metallization, as shown in Fig. 2. After these four basic operations are completed, the tested wafer is subjected to the special high-reliability processing. As shown in Fig. 3, thirty-five additional processing and screening operations are required for Class A COS/MOS parts.

Ordering Information

Order COS/MOS MIL-M-38510 Series types by giving the appropriate reliability screen as shown in Fig. 4. For example, the CD4013AD processed to Class A requirements should be marked MIL-M-38510/05101ACA.

Table 1: Description of MIL-M-38510 Screening Levels for RCA Integrated Circuits

MIL-M-38510	Application	Description
Class A (See Note 1)	Aerospace & Missiles	For devices intended for use where maintenance and replacement are extremely difficult or impossible and Reliability is imperative
Class B	Military & Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive
Class C	Military & Industrial For example, in Ground-Based Electronics	For devices intended for use where replacement can readily be accomplished

Note 1: In the Condition A Visual Inspection of COS/MOS devices, the specification for metallization alignment in section 3.1.1.7(a) of the general specification will be changed, to read as follows: alignment:
1. Contact window that has less than 50 per cent of its area covered by the metallization.
2. Contact which has less than 75 per cent of the length of two adjacent sides covered by the metallization.
3. A metallization path not intended to cover a contact window which is separated from the window by less than 0.25 mil.
4. Any exposure of the gate oxide.

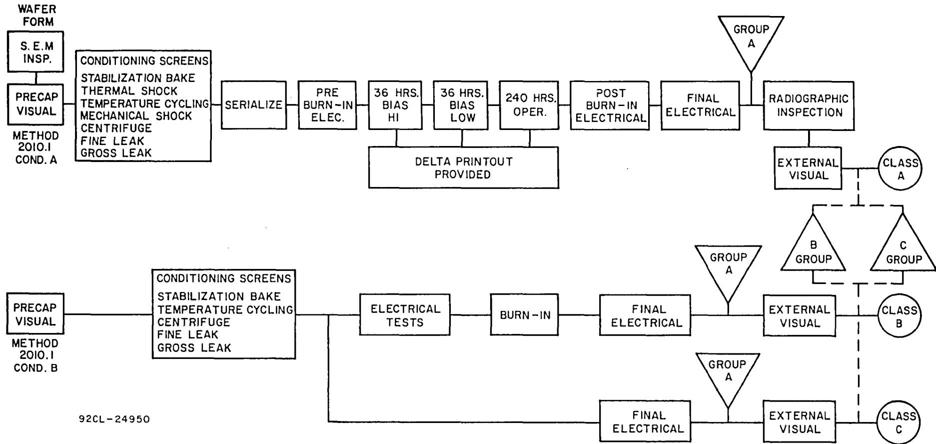


Fig. 1 — Product flow diagram for RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-M-38510.

Table 2 — MIL-M-38510 Processing and Screening Requirements for RCA High-Reliability COS/MOS Integrated Circuits

MIL-M-38510 Processing	MIL-STD-883 METHOD	Condition	MIL-M-38510 CLASS		
			A	B	C
• Wafer					
SEM Inspection	GSFC-S-311-P-12	Photographs Available	X	–	–
• Assembly					
Precap Visual	2010.1	A	X	–	–
Precap Visual	2010.1	B	–	X	X
• Preconditioning					
Stabilization Bake	1008	C, 48 hours at 150°C	X	X	X
Thermal Shock	1011	C, 15 cycles, -65°C to +150°C	X	–	–
Temperature Cycle	1010	C, 10 cycles, -65°C to +150°C	X	X	X
Mechanical Shock	2002	B, 5 pulses	X	–	–
Centrifuge Y1	2001	E, 30000 G's	–	X	X
Centrifuge Y1 & Y2	2001	E, 30000 G's	X	–	–
Fine Leak	1014	A	X	X	X
Gross Leak	1014	C	X	X	X
• Test and Burn-In					
Initial Test	–	MIL-M-38510/50 Series	X	X	–
Serialize			X	–	–
Bias Burn-In, Two 36-Hr. Deltas	1015	A, Bias at 150°C	X	–	–
Operating Burn-In, 240-Hr. Deltas	1015	A, Bias at 150°C	X	–	–
Operating Burn-In 168 Hrs.	1015	D, Dynamic at +125°C	–	X	–
Final Electrical DC +25°C		MIL-M-38510/50 Series	X	X	X
Final Electrical AC +25°C		MIL-M-38510/50 Series	X	X	S
Final Electrical DC -55°C		MIL-M-38510/50 Series	X	X	S
Final Electrical AC -55°C		MIL-M-38510/50 Series	S	S	S
Final Electrical DC +125°C		MIL-M-38510/50 Series	X	X	S
Final Electrical AC +125°C		MIL-M-38510/50 Series	S	S	S
• X-ray Inspection	NH853004(3E)	Two views	X	–	–

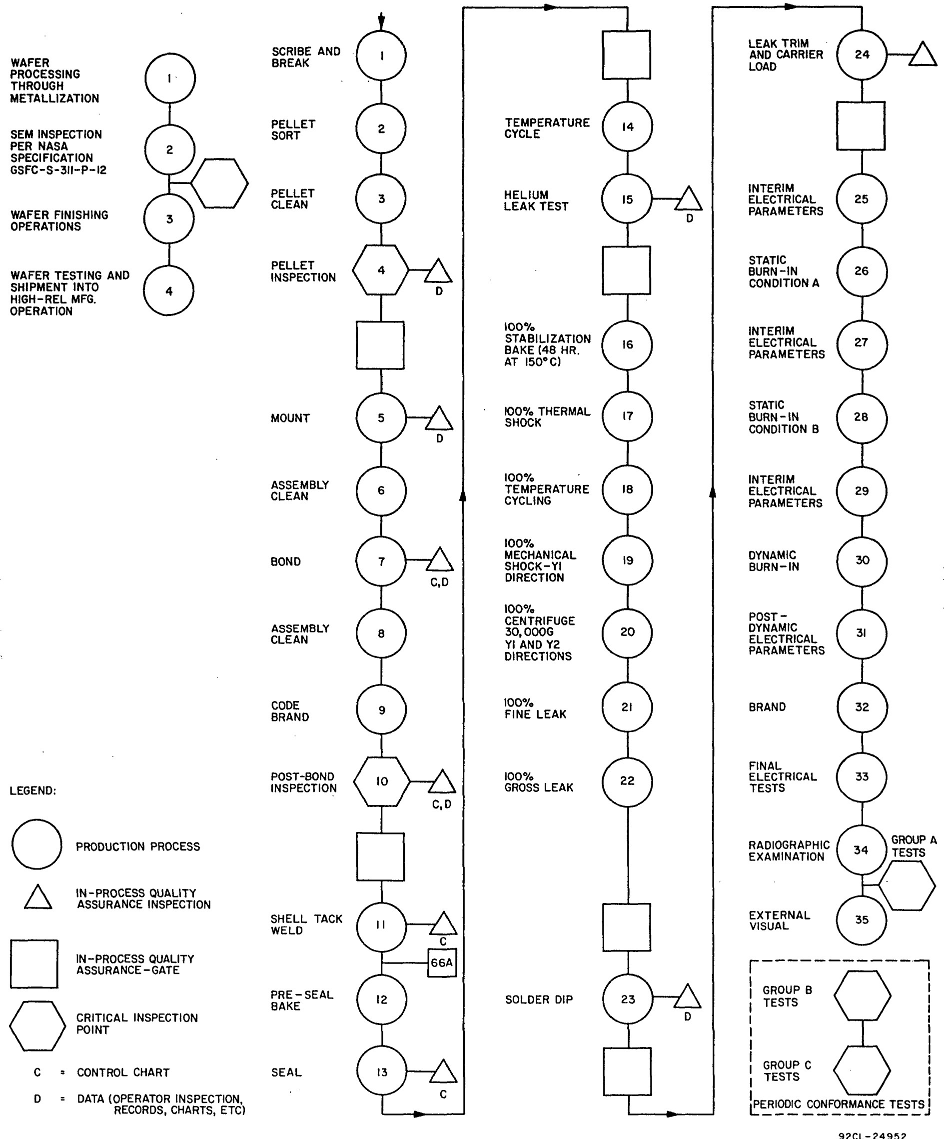


Fig. 3 — Flow Chart for COS/MOS High-Reliability Flat-Pack MIL-M-38510 Class A Device.

Table 3 – COS/MOS Devices For Which MIL-M-38510/50 Specifications Have Been Written

Detailed Electrical Specification, MIL-M-38510	Device Covered	Detailed Electrical Specification, MIL-M-38510	Device Covered
MIL-M-38510/050		MIL-M-38510/055	
01	CD4011A	01	CD4009A
02	CD4012A	02	CD4010A
03	CD4023A	03	CD4049A
MIL-M-38510/051		04	CD4050A
01	CD4013A	MIL-M-38510/056	
02	CD4027A	01	CD4017A
MIL-M-38510/052		02	CD4018A
01	CD4000A	03	CD4020A
02	CD4001A	04	CD4022A
03	CD4002A	05	CD4024A
04	CD4025A	MIL-M-38510/057	
MIL-M-38510/053		01	CD4006A
01	CD4007A	02	CD4014A
02	CD4019A	03	CD4015A
MIL-M-38510/054		04	CD4021A
01	CD4008A	05	CD4031A
		MIL-M-38510/058	
		01	CD4016A

Table 4 – Comparison of Screening Requirements for RCA Level /1N COS/MOS Devices and MIL-M-38510 Class A COS/MOS Devices

SCREENING PROCEDURES	RCA LEVEL /1N (PER MIL-STD-883)	CLASS A MIL-M-38510
1. SEM Inspection	Yes	Yes
2. Visual, Precap	2010.1 Cond. A	2010.1 Cond. A
3. Pre-conditioning	MIL-STD-883	MIL-STD-883
4. Bias Burn-in High	None	36 hrs @ 150°C, Δ[2] PDA[1]
5. Bias Burn-in Low	None	36 hrs @ 150°C, Δ[2] 5%
6. Operating Burn-in 240 hrs @ 125°C	Cirteria 10% Lot Reject Max; If Exceeded, Repeat Allowed	PDA 5% Max; if over 5% Reject Entire Lot Δ[2]
7. DC Elect. Tests	Measurements on Selected Inputs and Outputs	Measurements on all Inputs and Outputs
8. DC Test-Limit Resolution	50 nA Minimum; 10 mV Minimum	1 nA Minimum; 1 mV Minimum
9. AC Dynamic Tests	Measurements on Selected Inputs and Outputs	Measurements on all Inputs and Outputs
10. AC Test Limits	At 15-pF Load	AT 50-pF Load
11. Radiographic	View in One Dimension	View in Two Dimensions
12. Parts Qualification Requirement		9 Detailed Electrical Specifications
13. Group B and C Qualification Conformance	10 Generic Families for 50 COS/MOS Types	9 Generic Families for 27 COS/MOS Types

[1] PDA = Per-Cent Defective Allowable

[2] Δ = Delta Variables, Data Required

Table 5 — Final Electrical Tests

TEMPERATURE (T_A)	TESTS TO MIL-M-38510 SPECIFICATIONS	TEST CRITERIA		
		Class A	Class B	Class C
+25°C	DC & Functional Parameters	100%	100%	100%
+125°C	DC & Functional Parameters	100%	100%	–
-55°C	DC & Functional Parameters	100%	100%	–
+25°C	AC Parameters	100%	100%	–

Table 6 — Group A Electrical Sampling Inspection

SUBGROUP OF MIL-STD-883 5005.1	TESTS TO MIL-M-38510 SPECIFICATIONS	CONDITION	LTPD		
			Class A	Class B	Class C
1, 7	DC & Functional Parameters	T_A = +25°C	5	5	5
2, 8	DC & Functional Parameters	T_A = +125°C	5	7	10
3, 8	DC & Functional Parameters	T_A = -55°C	5	7	10
4, 9	AC Parameters	T_A = +25°C	5	5	5
10	AC Parameters	T_A = +125°C	5	5	–
11	AC Parameters	T_A = -55°C	7	7	–

Details of static, functional, and dynamic tests, conditions, and limits appear in the specific MIL-M-38510/050 series specifications.

Table 7 — Group B Environmental Sampling Inspection to MIL-M-38510 (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	CLASS A	CLASS B	CLASS C
1	Physical Dimensions	2008	Test Cond. A per applicable data sheet	10	15	20
2	Marking Permanency	2008	Test Cond. B per Par. 3.2.1	← 4 devices (no failures) →		
	Visual and Mechanical	2008	Test Cond. B 10 X mag.	← 1 device (no failure) →		
	Bond Strength	2011	Test Cond. D 10 Devices minimum	5	15	20
3	Solderability	2003		10	15	15
4	Lead Fatigue	2004	Test Cond. B2 any 5 leads	10	15	15
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			

Note 1: Group B tests are performed on each inspection lot per requirements of MIL-M-38510.
Note 2: Operating life circuits are included in MIL-M-38510 detailed specifications (/ sheets).

Table 8 – Group C Environmental Sampling Inspection to MIL-M-38510 (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	CLASS A	CLASS B	CLASS C
1	Thermal Shock	1011	Test Cond. C	10	15	15
	Temperature Cycling	1010	Test Cond. C			
	Moisture Resistance	1004	No Voltage Applied			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests – Note 3					
2	Mechanical Shock	2002	Test Cond. B, 0.5 ms	10	15	15
	Vibration, Var. Freq.	2007	Test Cond. A			
	Constant Acceleration	2001	Test Cond. E			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Test – Note 3					
3	Salt Atmosphere	1009	Test Cond. A Omit Initial Conditioning	10	15	15
4	High Temp. Storage	1008	Test Cond. C	7	7	7
	Critical Post Tests – Note 3		1000 hours			
5	Operating Life	1005	T_A = 125°C, 1000 hrs.	5	5	5
	Critical Post Tests – Notes 2 and 3		Test Circuit (Note 2)			
6	Steady State Bias	1015	Test Cond. A, 72 hrs.	7	–	–
	Critical Post Tests – Note 3		At T_A = 150°C (Note 3)			

Note 1: Group C tests are performed at 3-month intervals.
Note 2: Operating life circuits are included in MIL-M-38510 detailed specifications (/ sheets).
Note 3: Static parameters and limits are shown in MIL-M-38510 detailed specifications (/ sheets).

Table 9 – MIL-M-38510 Product-Assurance Program Requirements

In-House Documentation Covering These Areas

a. Conversion of customer requirements into manufacturer's internal instructions
b. Personnel training and testing
c. Inspection of incoming materials, utilities and work in process
d. Quality-control operations
e. Quality-assurance operations
f. Design, processing, tool and materials standards and instructions
g. Cleanliness and atmospheres in work areas
h. Design, material, and process change control
i. Tool and test equipment maintenance and calibration
j. Failure and defect analysis and data feedback
k. Corrective action and evaluation
l. Incoming, in process, and outgoing inventory control

In-House Records Covering These Areas

a. Personnel training and testing
b. Inspection operations
c. Failure reports and analyses
d. Changes in design, materials, or processing
e. Equipment calibrations
f. Process utility and material controls
g. Product lot identification

A Program Plan Covering These Areas

a. Functional block organization chart
b. Manufacturing flow chart
c. Proprietary-document listing
d. Examples of design, material, equipment, and processing instructions
e. Examples of records
f. Examples of design, material and process change control documents
g. Examples of failure and defect analysis and feedback documents
h. Examples of corrective action and evaluation documents

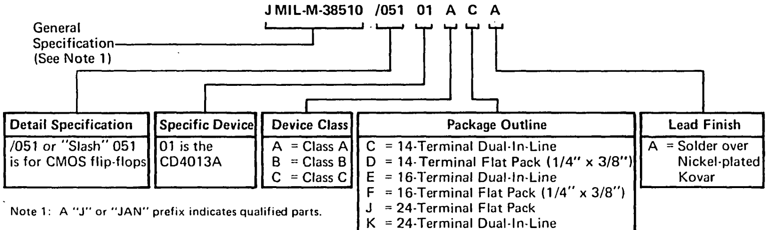
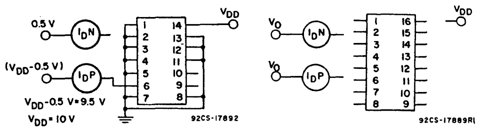


Fig. 4 – Guide to the reliability, class, package, and lead finish of RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-M-38510.

DRIVE CURRENT TEST CIRCUIT CONNECTIONS To be used as an example of test method.

Example: CD4000A I_{DP}

Example: **16-Lead Types**



Type	M♦	Ground	V_{DD}	V_O
CD4000A	I_{DN}	1-4,7,8,11,13	5,14	6
	I_{DP}	1-5,7,8,11-13	14	
CD4001A	I_{DN}	2,5-9,12,13	1,14	3
	I_{DP}	1,2,5-9,12,13	14	
CD4002A	I_{DN}	3-5,7,9-12	2,14	1
	I_{DP}	2-5,7,9-12	14	
CD4006A*	I_{DN}	1,4-7	14	13
	I_{DP}	4-7	1,14	
CD4007A	I_{DN}	3,7,10	6,14	8
	I_{DP}	3,6,7,10	14	13
CD4008A	I_{DN}	1-9,15	16	14
	I_{DP}	8	1-7,9,15,16	
CD4009A	I_{DN}	5,7-9,11,14	1,3,16	2
	I_{DP}	3,5,7-9,11,14	1,16	
CD4010A	I_{DN}	3,5,7-9,11,14	1,16	2
	I_{DP}	5,7-9,11,14	1,3,16	
CD4011A	I_{DN}	5-9,12,13	1,2,14	3
	I_{DP}	1,5-9,12,13	2,14	
CD4012A	I_{DN}	7,9-12	2-5,14	1
	I_{DP}	2,7,9-12	3-5,14	
CD4013A	I_{DN}	3,5-11	4,14	1
	I_{DP}	3-5,7-11	6,14	
CD4014A*	I_{DN}	1,4-8,11,13–15	9,16	3
	I_{DP}	4-8,11,13-15	1,9,16	
CD4015A*	I_{DN}	1,6-8,14,15	16	5
	I_{DP}	1,6,8,14,15	7,16	
CD4017A	I_{DN}	8	13-16	3
	I_{DP}	8	13-16	2
CD4018A	I_{DN}	1-3,7-10,12	14-16	11
	I_{DP}	1-3,7,8,10	9,12,14-16	
CD4019A	I_{DN}	1-9	14-16	13
	I_{DP}	1-8	9,14-16	
CD4020A*	I_{DN}	8,11	16	9
	I_{DP}	8,11	16	
CD4021A	I_{DN}	1,4-8,10,11, 13-15	9,16	3
	I_{DP}	4-8,10,11,13-15	1,9,16	
CD4022A*	I_{DN}	8,13,15	16	2
	I_{DP}	8,13,15	16	
CD4023A	I_{DN}	1,2,7,8,11-13	3-5,14	6
	I_{DP}	1-3,7,8,11-13	4,5,14	
CD4024A* (K,D)	I_{DN}	1,7	2,14	12
	I_{DP}	2,7	14	
CD4024A* (T)	I_{DN}	1,12	2,3	11
	I_{DP}	3.12	2	
CD4025A	I_{DN}	1-4,7,8,11-13	5,14	6
	I_{DP}	1-5,7,8,11-13	14	
CD4026A	I_{DN}	1-3,8,15	16	10
	I_{DP}	1,2,8	3,15,16	
CD4027A	I_{DN}	3,5-13	4,16	1
	I_{DP}	3-6,8-13	7,16	
CD4028A	I_{DN}	8,10-13	16	2
	I_{DP}	8,10-13	16	3
CD4029A	I_{DN}	3,4,8,10,12, 13,15	1,5,9,16	6
	I_{DP}	5,8,15	1,3,4,9,10,12, 13,16	
CD4030A	I_{DN}	1,2,5-9,12,13	14	3
	I_{DP}	2,5-9,12,13	1,14	
CD4031A	I_{DN}	1,2,8,10,15	7,16	6
	I_{DP}	1,2,7,8,10,15	16	
CD4032A	I_{DN}	2,3,5-8,10-15	16	9
	I_{DP}	2,3,5,6,8,10-15	7,16	
CD4033A	I_{DN}	1-3,8,14	15,16	10
	I_{DP}	1-3,8,15	14,16	
CD4034A	I_{DN}	1-8,10-12,15	9,13,14,24	16
	I_{DP}	10-12,15	1-9,13,14,24	
CD4035A	I_{DN}	2-4,6-12	2,5,16	1
	I_{DP}	2-4,6-12	5,16	
CD4036A	I_{DN}	3-12,21-23	1,2,24	13
	I_{DP}	11,12,21-23	1-10,24	
CD4037A	I_{DN}	7	1-5,14	10
	I_{DP}	2-7	14	
CD4038A	I_{DN}	2,3,5-8,10-15	10,11,16	9
	I_{DP}	2,3,5,6,8,12-15	7,10,11,16	
CD4039A	I_{DN}	3-12,21-23	1,2,24	13
	I_{DP}	11,12,21-23	1-10,24	
CD4040A*	I_{DN}	8,10	11,16	9
	I_{DN}	8,11	16	
CD4041A (TRUE)	I_{DN}	3,6,7,10,13	14	1
	I_{DP}	6,7,10,13	3,14	
CD4041A (COMP)	I_{DN}	6,7,10,13	3,14	2
	I_{DP}	3,6,7,10,13	14	

Refer to applicable data sheet for V_O values.
Voltage outputs shall be supplied by an external power supply.

♦ M = Measurement

* These types must be clocked into the proper state.

DRIVE-CURRENT TEST-CIRCUIT CONNECTIONS (Cont'd)

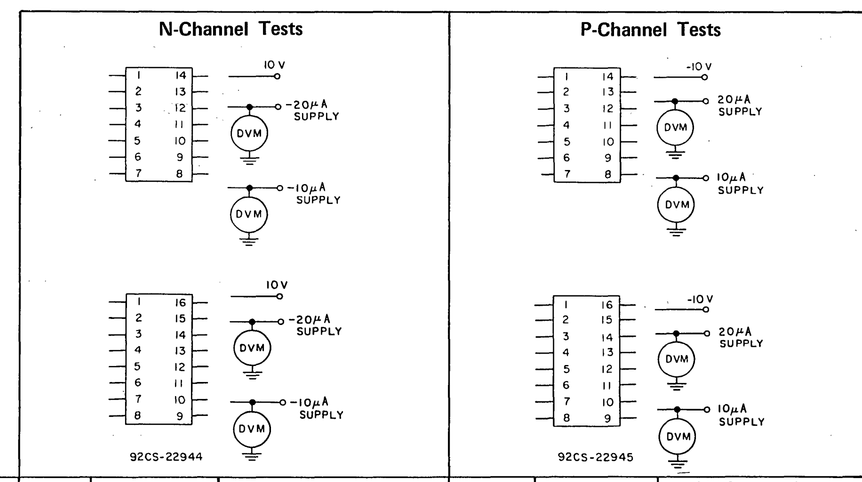
Type	M♦	Ground	V_{DD}	V_O
CD4042A	I_{DN}	4,7,8,13,14	5,6,16	2
	I_{DP}	7,8,13,14	4-6,16	
CD4043A	I_{DN}	4,6-8,11,12 14,15	3,5,16	2
	I_{DP}	3,6-8,11,12 14,15	4,5,16	
CD4044A	I_{DN}	4,8	3,5-7,11,12, 14-16	13
	I_{DP}	3,8	4-7,11,12, 14-16	
CD4045A (ϕ to 16)	I_{DN}	2,14	1,3	8
	I_{DP}	2,14	1,3	
CD4046A	I_{DN}	5,8,9	3,14,16	2
COMP 1	I_{DP}	5,8,9,14	3,16	
	I_{DN}	5,8,9,14	3,16	13
COMP 2	I_{DP}	5,8,9	3,14,16	
CD4047A	I_{DN}	5,7,12	4,6,8,9,14	10
	I_{DP}	7,9	3-6,8,12,14	
CD4048A	I_{DN}	3-14	2,15,16	1
	I_{DP}	2-14	15,16	
CD4049A	I_{DN}	5,7-9,11,14	1,3	2
	I_{DP}	5,7-9,11,14	1	
CD4050A	I_{DN}	3,5,7-9,11,14	1	2
	I_{DP}	5,7-9,11,14	1,3	
CD4054A	I_{DN}	2,7-15	1,16	3
	I_{DP}	2,7-14	1,15,16	
CD4055A	I_{DN}	2-4,6-8	5,16	9
	I_{DP}	2-8	16	
CD4056A	I_{DN}	2-4,6-8	1,5,16	9
	I_{DP}	2-8	1,16	
CD4057A	I_{DN}	1-3,6,7,14,21 23,25,27,28	8,9,13,15,19, 22,26	24
ZERO IND	I_{DP}	6,14,21,23 25,28	1-3,7-9,13,15, 19,20,22,26,27	
	I_{DN}	1-3,6,14,21,23, 25,27,28	7-9,13,15,19 20,22,26	4
NEG IND	I_{DP}	1-3,6,7,14,21, 23,25,27,28	8,9,13,15,19, 20,22,26	
	I_{DN}	1-3,5,7-9,14,19 22,23,25,27,28	6,13,15,20, 21,26	17
OVERFLOW IND	I_{DP}	5,7-9,14,19,22, 23,25,28	1-3,6,13,15,20, 21,26,27	
OTHER OUTPUTS	I_{DN}	6,7,21,25	8,9,13,15,19,20, 22,23,26	1
DATA OUT 1 & 3	I_{DP}	6,7,21,22,25	8,9,13,15,19,20, 23,26	27
CD4060A*	I_{DN}	8,11	12,16	7
	I_{DP}	8,12	16	
CD4061A*	I_{DN}	1-4,6,7,9-12, 15,16	5	13
	I_{DP}	1-4,6,7,9-11, 15,16	5,12	

Type	M♦	Ground	V_{DD}	V_O
CD4062AK*	I_{DN}	2-5,8	11,13,16	7
CLD	I_{DP}	3-5,8	2,11,13,16	
	I_{DN}	2-5,8	11,13,16	12
Q	I_{DP}	3-5,8	2,11,13,16	
CD4062AT*	I_{DN}	2-5,7	9,11,12	6
CLD	I_{DP}	3-5,7	2,9,11,12	
	I_{DN}	2-5,7	9,11,12	10
Q	I_{DP}	3-5,7	2,9,11,12	
CD4063B	I_{DN}	1,3,4,8-15	3,16	5
	I_{DP}	1-3,8-15	4,16	
CD4066A	I_{DN}	NO I_{DN}, I_{DP}		
	I_{DP}			
CD4068B	I_{DN}	7	2-5,9-12,14	13
	I_{DP}	2-5,7,9-12	14	
CD4069B	I_{DN}	7	1,3,5,9,11,13,14	2
	I_{DP}	1,3,5,7,9,11,13	14	
CD4071B	I_{DN}	1,2,5-9,12,13	14	10
	I_{DP}	7	1,2,5-9,12,13,14	
CD4072B	I_{DN}	2-5,7,9-12	14	1
	I_{DP}	7	2-5,9-12,14	
CD4073B	I_{DN}	1-5,7,8,11-13	14	6
	I_{DP}	7	1-5,8,11-14	
CD4075B	I_{DN}	1-5,7,8,11-13	14	6
	I_{DP}	7	1-5,8,11-14	
CD4078B	I_{DN}	7	2-5,9-12,14	13
	I_{DP}	2-5,7,9-12	14	
CD4081B	I_{DN}	1,2,5-9,12,13	14	3
	I_{DP}	7	1,2,5,6,8,9, 12-14	
CD4082A	I_{DN}	2-5,7,9-12	14	1
	I_{DP}	7	2-5,9-12,14	
CD4085B	I_{DN}	1,2,5-9,11-13	10-14	3
	I_{DP}	1,2,5-13	14	
CD4086B	I_{DN}	1,2,5-9,11,13	11,14	3
	I_{DP}	1,2,5-10,12,13	11,14	
CD4514B	I_{DN}	2,3,12,21,22	1,2,3,24	11
	I_{DP}	2,3,12,21-23	1,24	
CD4515B	I_{DN}	2,3,12,21-23	1,24	11
	I_{DP}*	2,3,12,21,22	1,23,24	
CD4518B*	I_{DN}	1,2,7-10	15,16	14
	I_{DP}	1,2,7,8,10,15	16	
CD4520B	I_{DN}	1,2,7-10	15,16	14
	I_{DP}	1,2,7,8,10,15	16	

♦ M = Measurement

* These types must be clocked into the proper state.

THRESHOLD-VOLTAGE TEST-CIRCUIT CONNECTIONS



Type	Ground	10V	V_{THN} measured at −20 µA Supply	V_{THN} measured at −10 µA Supply	Ground	−10V	V_{THP} measured at 20 µA Supply	V_{THP} measured at 10 µA Supply
CD4000A	3	14		1,2,4,5,7,8, 11-13	3	1,2,4,5,7,8, 11-13		14
CD4001A	1	14		2,5-9,12,13	1	2,5-9,12,13		14
CD4002A	2	14		3-5,7,9-12	2	3-5,7,9-12		14
CD4006A	3	14	1,4-7		3	1,4-7	14	
CD4007A	6	14,8		7	6	7,13		14
CD4008A	9	2,4,6,15,16	1,3,5,7,8		9	1,3,5,7,8	2,4,6,15,16	
CD4009A	3	1,16		5,7-9,11,14	3	5,7-9,11,14		1,16
CD4010A	3	1,16		5,7-9,11,14	3	5,7-9,11,14		1,16
CD4011A	2	1,14		5-9,12,13	2	5-9,12,13		1,14
CD4012A	2	3-5,14		7,9-12	2	7,9-12		3-5,14
CD4013A	3	14		4-11	3	4-11		14
CD4014A	10	16	1,4-9,11,13-15		10	1,4-9,11,13-15	16	
CD4015A	1	16	6-9,14,15		1	6-9,14,15	16	
CD4016A	13	5,6,12,14		7	13	5-7,12		14
CD4017A	15	16	8,13,14		15	8	13,14,16	
CD4018A	15	16	1-3,7-10,12,14		15	1-3,7-10,12,14	16	
CD4019A	9	14-16	1-8		9	1-8	14-16	
CD4020A	10,11	16	8		10	8,11	16	
CD4021A	10	16	1,4-9,11,13-15		10	1,4-9,11,13-15	16	
CD4022A	14	13,15,16	8		14	8,13,15	16	
CD4023A	3	4,5,14		1,2,7,8,11-13	3	1,2,7,8,11-13		4,5,14
CD4024A (K,D)	1,2	14	7		1	2,7	14	
CD4024A (T)	1,3	2	12		1	3,12	2	
CD4025A	3	14		1,2,4,5,7,8, 11-13	3	1,2,4,5,7,8, 11-13		14
CD4026A	1	2,3,15,16		8	1	2,3,8,15		16
CD4027A	13	3-7,9-12,16		8	13	3-12		16
CD4028A	10	16	8,11-13		10	8,11-13	16	
CD4029A	10	1,3-5,9,12,13, 15,16	8		10	1,3-5,8,9,12, 13,15	16	
CD4030A	8	14		1,2,5-7,12,13	8	1,2,5-7,9,12,13		14
CD4031A	2	1,10,15,16*	8		2	1,8,10,15*	16	
CD4032A	3	2,5-7,10-16		8	3	2,5-8,10-15		16
CD4033A	1	2,3,14-16	8		1	2,3,8,14,15	16	

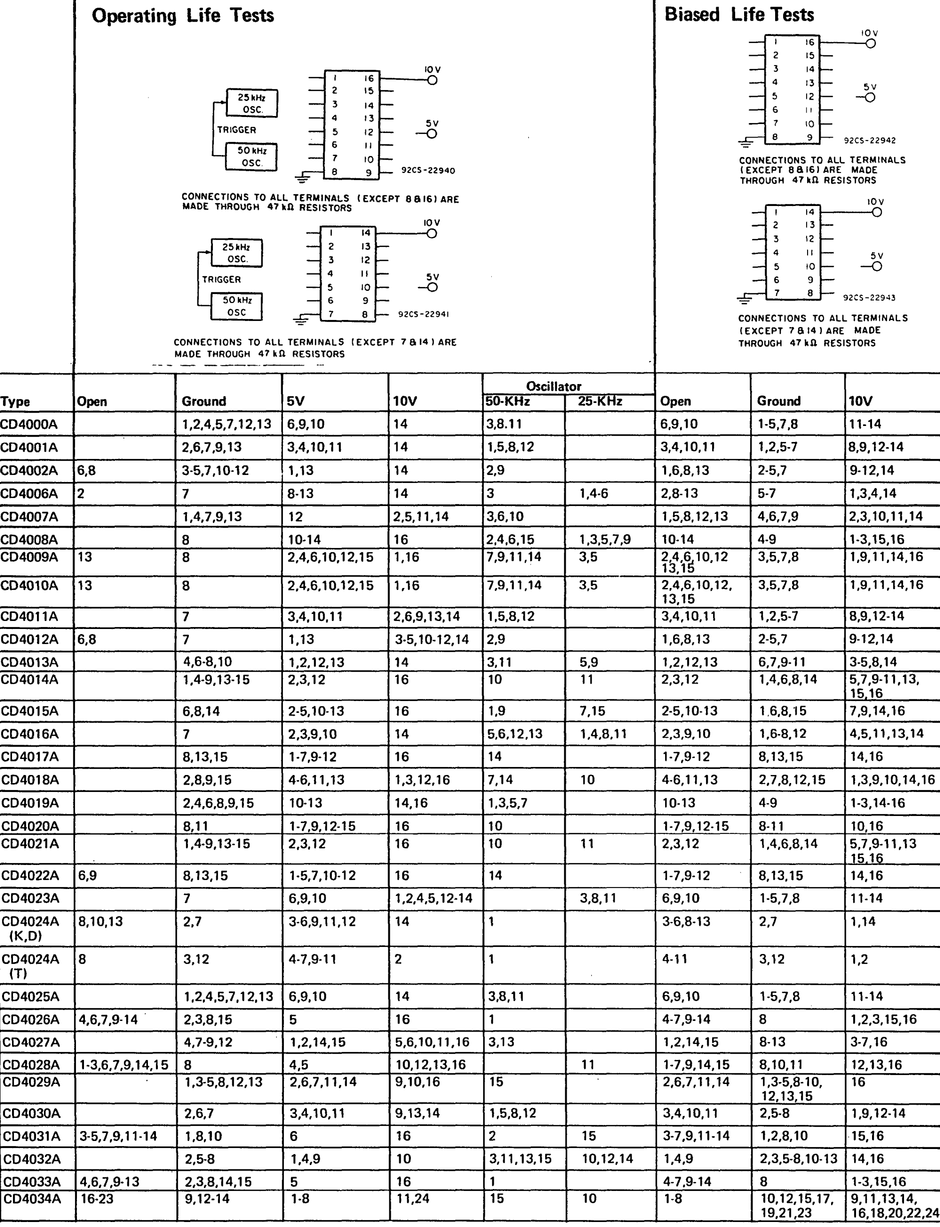
THRESHOLD-VOLTAGE TEST-CIRCUIT CONNECTIONS (CONT'D)

	N-Channel Tests				P-Channel Tests			
			$V_{TH}N$ measured at				$V_{TH}P$ measured at	
Type	Ground	10V	−20 µA Supply	−10 µA Supply	Ground	−10V	20 µA Supply	10 µA Supply
CD4034A	10	9,11,13-24		12	10	1-9,11-15		24
CD4035A	6	16	2-5,7-12		6	2-5,7-12	16	
CD4036A	23	1-11,21,22,14	12		23	1-12,21,22	24	
CD4038A	3	2,5,6,10-16		8	3	2,5-8,10-15		16
CD4039A	23	1-11,21,22,24	12		23	1-12,21,22	24	
CD4040A	10,11	16	8		10	8,11	16	
CD4041A	3	14		6,7,10,13	3	6,7,10,13		14
CD4042A	6	16		4,5,7,8,13,14	6	4,5,7,8,13,14		16
CD4043A	5	16		3,4,6-8,11,12, 14,15	5	3,4,6-8,11,12, 14,15		16
CD4044A	5	16		3,4,6-8,11,12, 14,15	5	3,4,6-8,11,12, 14,15		16
CD4045A	16	1,3•		2,14,15	16	2,14,15•		1,3
CD4046A	3,5-8,14	9,11,12,16		10	3,5-9,11,14	16		12
CD4047A	4,8,12	3,5,6,14		7	4,8,12	3,5-7,9		14
CD4048A	10	16	2-9,11-15		10	2-9,11-15	16	
CD4049A	3	1		5,7-9,11,14	3	5,7-9,11,14		1
CD4050A	3	1		5,7-9,11,14	3	5,7-9,11,14		1
CD4057A	A special detailed test set-up is reuired							
CD4060A	12	16		9-11	12	9,10,11		16
CD4061A	1	2,3,5,6,7,9,10 11,15,16	4		1	2-4,6,7,9-12, 15,16	5	
CD4062AK	5	10,13,16	2-4,8		10	2-5,8	13,16	
CD4062AT	5	8,11,12	2-4,7		8	2-5,7	11,12	
CD4063B	1	16	2-4,8-15		1	2-4,8-15	16	
CD4066A	13	5,6,12,14		7	13	5-7,12		14
CD4068B	2	3-5,14		7,9-12	2	7,9-12		3-5,14
CD4069B	1	14		3,5,7,9,11,13	1	3,5,7,9,11,13		14
CD4071B	1	14		2,5-9,12,13	1	2,5-9,12,13		14
CD4072B	2	14		3-5,7,9-12	2	3-5,7,9-12		14
CD4073B	3	4,5,14		1,2,7,8,11-13	3	1,2,7,8,11-13		4,5,14
CD4075B	3	14		1,2,4,5,7,8, 11,12,13	3	1,2,4,5,7,8, 11-13		14
CD4078B	2	14		3-5,7,9-12	2	3-5,7,9-12		14
CD4081B	2	1,14		5-9,12,13	2	5-9,12,13		1,14
CD4082B	2	3-5,14		7,9-12	2	7,9-12		3-5,14
CD4085B	1	2,14		5-13	1	5-13		2,14
CD4086B	1	2,14		5-13	1	5-13		2,14
CD4514B	1	24		2,3,12,21-23	1	2,3,12,21-23		24
CD4515B	1	24		2,3,12,21-23	1	2,3,12,21-23		24
CD4518B	15	16	1,2,7-10		15	1,2,7-10	16	
CD4520B	15	16	1,2,7-10		15	1,2,7-10	16	

* Use 5V for n-channel test, −5V for p-channel test.

• Use 4V for n-channel test, −4 V for p-channel test.

LIFE-TEST CIRCUIT CONNECTIONS



Type	Open	Ground	5V	10V	Oscillator 50-KHz	Oscillator 25-KHz	Open	Ground	10V
CD4000A		1,2,4,5,7,12,13	6,9,10	14	3,8.11		6,9,10	1-5,7,8	11-14
CD4001A		2,6,7,9,13	3,4,10,11	14	1,5,8,12		3,4,10,11	1,2,5-7	8,9,12-14
CD4002A	6,8	3-5,7,10-12	1,13	14	2,9		1,6,8,13	2-5,7	9-12,14
CD4006A	2	7	8-13	14	3	1,4-6	2,8-13	5-7	1,3,4,14
CD4007A		1,4,7,9,13	12	2,5,11,14	3,6,10		1,5,8,12,13	4,6,7,9	2,3,10,11,14
CD4008A		8	10-14	16	2,4,6,15	1,3,5,7,9	10-14	4-9	1-3,15,16
CD4009A	13	8	2,4,6,10,12,15	1,16	7,9,11,14	3,5	2,4,6,10,12 13,15	3,5,7,8	1,9,11,14,16
CD4010A	13	8	2,4,6,10,12,15	1,16	7,9,11,14	3,5	2,4,6,10,12, 13,15	3,5,7,8	1,9,11,14,16
CD4011A		7	3,4,10,11	2,6,9,13,14	1,5,8,12		3,4,10,11	1,2,5-7	8,9,12-14
CD4012A	6,8	7	1,13	3-5,10-12,14	2,9		1,6,8,13	2-5,7	9-12,14
CD4013A		4,6-8,10	1,2,12,13	14	3,11	5,9	1,2,12,13	6,7,9-11	3-5,8,14
CD4014A		1,4-9,13-15	2,3,12	16	10	11	2,3,12	1,4,6,8,14	5,7,9-11,13, 15,16
CD4015A		6,8,14	2-5,10-13	16	1,9	7,15	2-5,10-13	1,6,8,15	7,9,14,16
CD4016A		7	2,3,9,10	14	5,6,12,13	1,4,8,11	2,3,9,10	1,6-8,12	4,5,11,13,14
CD4017A		8,13,15	1-7,9-12	16	14		1-7,9-12	8,13,15	14,16
CD4018A		2,8,9,15	4-6,11,13	1,3,12,16	7,14	10	4-6,11,13	2,7,8,12,15	1,3,9,10,14,16
CD4019A		2,4,6,8,9,15	10-13	14,16	1,3,5,7		10-13	4-9	1-3,14-16
CD4020A		8,11	1-7,9,12-15	16	10		1-7,9,12-15	8-11	10,16
CD4021A		1,4-9,13-15	2,3,12	16	10	11	2,3,12	1,4,6,8,14	5,7,9-11,13 15,16
CD4022A	6,9	8,13,15	1-5,7,10-12	16	14		1-7,9-12	8,13,15	14,16
CD4023A		7	6,9,10	1,2,4,5,12-14		3,8,11	6,9,10	1-5,7,8	11-14
CD4024A (K,D)	8,10,13	2,7	3-6,9,11,12	14	1		3-6,8-13	2,7	1,14
CD4024A (T)	8	3,12	4-7,9-11	2	1		4-11	3,12	1,2
CD4025A		1,2,4,5,7,12,13	6,9,10	14	3,8,11		6,9,10	1-5,7,8	11-14
CD4026A	4,6,7,9-14	2,3,8,15	5	16	1		4-7,9-14	8	1,2,3,15,16
CD4027A		4,7-9,12	1,2,14,15	5,6,10,11,16	3,13		1,2,14,15	8-13	3-7,16
CD4028A	1-3,6,7,9,14,15	8	4,5	10,12,13,16		11	1-7,9,14,15	8,10,11	12,13,16
CD4029A		1,3-5,8,12,13	2,6,7,11,14	9,10,16	15		2,6,7,11,14	1,3-5,8-10, 12,13,15	16
CD4030A		2,6,7	3,4,10,11	9,13,14	1,5,8,12		3,4,10,11	2,5-8	1,9,12-14
CD4031A	3-5,7,9,11-14	1,8,10	6	16	2	15	3-7,9,11-14	1,2,8,10	15,16
CD4032A		2,5-8	1,4,9	10	3,11,13,15	10,12,14	1,4,9	2,3,5-8,10-13	14,16
CD4033A	4,6,7,9-13	2,3,8,14,15	5	16	1		4-7,9-14	8	1-3,15,16
CD4034A	16-23	9,12-14	1-8	11,24	15	10	1-8	10,12,15,17, 19,21,23	9,11,13,14, 16,18,20,22,24

LIFE-TEST CIRCUIT CONNECTIONS (CONT'D)

	Operating Life Tests						Biased Life Tests		
					Oscillator				
Type	Open	Ground	5V	10V	50-KHz	25-KHz	Open	Ground	10V
CD4035A	Jumpered 1,3,4	2,5,7-12,14,15	13	16	6		1,13-15	4-10	2,3,11,12,16
CD4036A		11,12,21,22	13-20	2,24	1,23	3-10	1,13-20	3-12,21,22	2,23,24
CD4038A		2,5-8	1,4,9	16	3,11,13,15	10,12,14	1,4,9	2,3,5-8,10-13	14-16
CD4039A		11,12	13-20	24	1,2,21-23	3-10	1,13-20	3-12,21,22	2,23,24
CD4040A		8,11	1-7,9,12-15	16	10		1-7,9,13-15	8,11	10,16
CD4041A		7	1,2,4,5,8, 9,11,12	14	3,6,10,13		1,2,4,5, 8,9,11,12	3,6,7	10,13,14
CD4042A		8	1,2,3,9-12,15	6,16	5	4,7,13,14	1-3,9-12,15	6,8,13,14	4,5,7,16
CD4043A	13	8	1,2,9,10	5,16	4,6,12,14	3,7,11,15	1,2,9,10,13	3,7,8,12,14	4,5,6,11,15,16
CD4044A	2	8	1,9,10,13	5,16	4,6,12,14	3,7,11,15	1,2,9,10,13	4,6,8,11,15	3,5,7,12,14,16
CD4045A	4-6,9-13,15	2,14•		1,3•,7,8	16		4-6,9-13,15	2,14•	1,3•, 7, 8, 16
CD4046A	1,4,6,7 10,11,13,15	8,9	2	3,5,12,16	14		1,2,4,6,7, 10,11,13,15	3,8,9,14	5,12,16
CD4047A		7,9,12	1,2,10,11,13	4,5,14	6,8	3	1,2,10,11,13	4,7,12	3,5,6,8,9,14
CD4048A		8,15	1	2,16	9-14	3-7	1	3-6,8,15	2,7,9-14,16
CD4049A	13	8	2,4,6,10, 12,15	1,16	7,9 11,14	3,5	2,4,6,10 12,13,15	3,5,7,8	1,9,11,14,16
CD4050A	13	8	2,4,6,10, 12,15	1,16	3,5,7,9 11,14		2,4,6,10, 12,13,15	3,5,7,8	1,9,11,14,16
CD4057A		1,8-10,18,19, 21-23,25	4,16,17,24	2,3,5,6,26	2	29		1-3,8-10 13,21,22,25	6,7,15,18, 20,23,26,27
CD4060A		8,12	1-7,9,10,13-15	16	11		1-7,9,10,13-15	8,11	12,16
CD4061A	8	4,15	13,14	5,12	16	1-3,6,7,9-11	8,13,14	4,15,16	1-3,5-7,9-12
CD4062AK	5-7,9-11,14,15	3,4,8,13	12	16	1	2	1,6,7,9,10, 12,14,15	2-5, 8	11,13,16
CD4062AT	5,6,8,9	3,4,7,11	10	12	1	2	1,6,8,10	2-5,7	9,11,12
CD4063B		1,2,4,8,10, 11,13	5-7	3,16	12.15	9,14		1,2,4,8-12	3,13-16
CD4066A		7	2,3,9,10	14	5,6,12,13	1,4,8,11	2,3,9,10	1,6-8,12	4,5,11,13,14
CD4068B	1,6,8	7	13	14	2-5,10-12		1,6,8,13	2-5,7	9-12,14
CD4069B		7	2,4,6,8,10,12	14	1,3,5,9,11,13	2,4,6,8,10,12	1,3,5,7	9,11,13,14	
CD4071B		2,6,7,9,13	3,4,10,11	14	1,5,8,12		3,4,10,11	1,2,5,7	8,9,12,14
CD4072B	6,8	3,5,7,10,12	1,13	14	2,9		1,6,8,13	2,5,7	9,12,14
CD4073B		7	6,9,10	1,2,4,5,12-14		3,8,11	6,9,10	1,5,7,8	11-14
CD4075B		1,2,4,5,7,12,13	6,9,10	14	3,8,11		3,4,10,11	1,5,7,8	11,14
CD4078B	1,6,8	7	13	14	3,5,9,11	2,4,10,12	1,6,8,13	2-5,7	9-12,14
CD4081B		7	3,4,10,11	2,6,9,13,14	1,5,8,12		3,4,10,11	1,2,5-7	8,9,12-14
CD4082B	6,8	7	1,13	3-5,10-12,14	2,9		1,6,8,14	2-5,7	9-12,14
CD4085B		7,10,11	3,4	2,6,9,13,14	1,5,8,12		3,4	2,6,9-11,13	1,5,8,12,14
CD4086B		7,10	3	1,5,8,11,12,14	2,6,9,13		3	1,5,7,8,10,12	2,6,9,11,14
CD4514B		2,3,12	4-11,13-20	21,22,24	1	23	4-11,13-20	12,21-23	1-3,24
CD4515B		2,3,12	4-11,13-20	21,22,24	1	23	4-11,13-20	12,21-23	1-3,24
CD4518B		7,8,15	3-6,11-14	16	1,9	2,10		1,2,7,8	9,10,15,16
CD4520B		7,8,15	3-6,11-14	16	1,9	2,10		1,2,7,8	9,10,15,16

• No 47-KΩ resistor.

DIMENSIONAL OUTLINES FOR INTEGRATED CIRCUITS

Ceramic Flat Packs

14-LEAD CERAMIC FLAT PACKAGE MIL-M-38510 CASE OUTLINE F-2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.045	0.085		1.14	2.16
b	0.010	0.019	5	0.25	0.48
c	0.003	0.006	5	0.08	0.15
D		0.390	3		9.91
E	0.235	0.280	3	5.97	7.11
E_1	0.125			3.18	
E_2	0.030			0.76	
e	0.050 BSC		4, 6	1.27 BSC	
L	0.250	0.370		6.35	9.40
L_1	0.735			18.67	
Q	0.010	0.040	2	0.25	1.02
S	0.005		7, 8	0.13	
S_1		0.045	7		1.14

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is 0.050 in. (1.25 mm) between centerlines. Each pin centerline shall be located within ±0.005 in. (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
5. All leads.
6. Twelve spaces.
7. Applies to all four corners (lead numbers 1, 7, 8, and 14).
8. Dimension S may be 0.000 in. (0.00 mm) if lead numbers 1, 7, 8, and 14 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body or if the leads are brazed to the metallized ceramic body.

92CS-24772

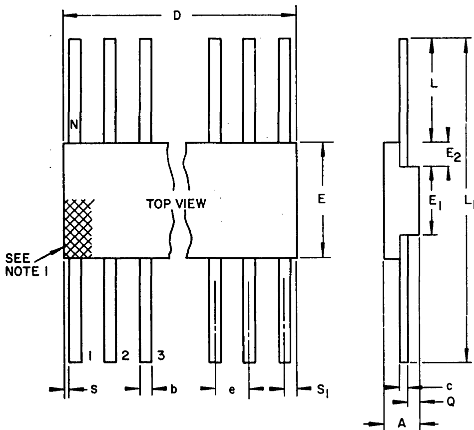
16-LEAD CERAMIC FLAT PACKAGE MIL-M-38510 CASE OUTLINE F-5

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.045	0.085		1.14	2.16
b	0.015	0.019	5	0.38	0.48
c	0.003	0.006	5	0.08	0.15
D		0.440	3		11.18
E	0.245	0.305	3	6.22	7.75
E_1	0.130			3.30	
E_2	0.030			0.76	
e	0.050 BSC		4, 6	1.27 BSC	
L	0.250	0.370		6.35	9.40
L_1	0.745			18.92	
Q	0.010	0.040	2	0.25	1.02
S	0.005		7, 8	0.13	
S_1		0.045	7		1.14

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is 0.050 in. (1.25 mm) between centerlines. Each pin centerline shall be located within ±0.005 in. (0.13 mm) of its exact longitudinal position relative to pins 1 and 16.
5. All leads.
6. Fourteen spaces.
7. Applies to all four corners (lead numbers 1, 8, 9, and 16).
8. Dimension S may be 0.000 in. (0.00 mm) if lead numbers 1, 8, 9, and 16 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body or if the leads are brazed to the metallized ceramic body.

92CS-24786



The lead finish for the packaged types is in accordance with MIL-M-38510, Paragraph 3.6.2.5, Lead Finish "A". When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

Ceramic Flat Packs (Cont'd)

24-LEAD CERAMIC FLAT PACK

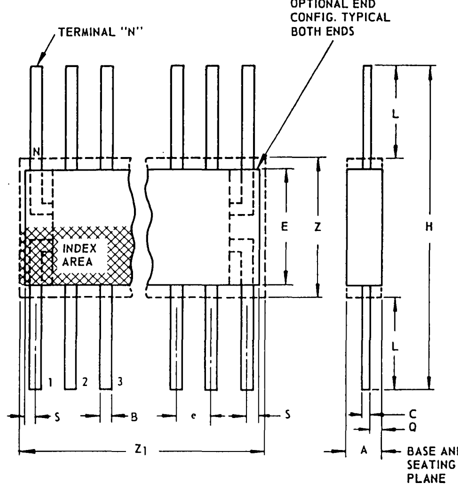
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-19949

28-LEAD CERAMIC FLAT PACK

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	28		3	28	
Q	0.035	0.070		0.89	1.77
S	0	0.060	1	0	1.53
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-20972



NOTES:

1. Refer to JEDEC Publication No. 13 for Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

The lead finish for the packaged types is in accordance with MIL- M-38510, Paragraph 3.6.2.5, Lead Finish "A". When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

Ceramic Dual-in-Line Packages

14-LEAD DUAL-IN-LINE CERAMIC PACKAGE MIL-M-38510 CASE OUTLINE D-1

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A		0.200			5.08
b	0.014	0.023	8	0.36	0.58
b_1	0.030	0.070	2, 8	1.02	1.78
c	0.008	0.015	8	0.20	0.38
D		0.796	4		20.22
E	0.220	0.310	4	5.59	7.87
E_1	0.290	0.320	7	7.37	8.13
E_2	0.100			2.54	
E_3	0.045			1.14	
e	0.100 BSC		5, 9	2.54 BSC	
L	0.125	0.200		3.18	5.08
L_1	0.150			3.81	
Q	0.015	0.060	3	0.38	1.52
Q_1	0.020			0.51	
S	0.005		6	0.13	
S_1		0.098	6		2.49
α	0°	15°		0°	15°

NOTES:
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be 0.020 in. (0.51 mm) for lead numbers 1, 7, 8, and 14 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic pin spacing is 0.100 in. (2.54 mm) between centerlines. Each pin centerline shall be located within ±0.010 in. (0.25 mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (lead numbers 1, 7, 8, and 14).
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
8. All leads.
9. Twelve spaces.

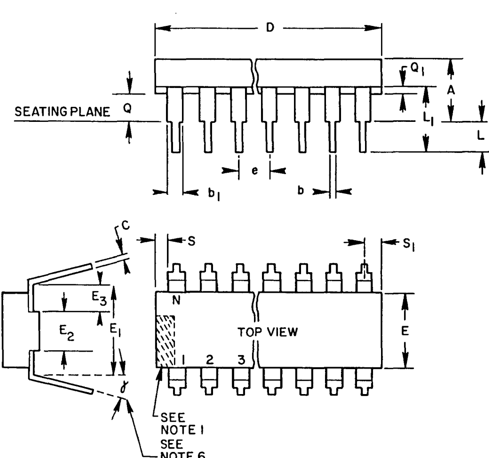
92CS-24773

16-LEAD DUAL-IN-LINE CERAMIC PACKAGE MIL-M-38510 CASE OUTLINE D-2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A		0.200			5.08
b	0.014	0.023	8	0.36	0.58
b_1	0.030	0.070	2, 8	1.02	1.78
c	0.008	0.015	8	0.20	0.38
D		0.896	4		22.76
E	0.220	0.310	4	5.59	7.87
E_1	0.290	0.320	7	7.37	8.13
E_2	0.100			2.54	
E_3	0.045			1.14	
e	0.100 BSC		5, 9	2.54 BSC	
L	0.125	0.200		3.18	5.08
L_1	0.150			3.81	
Q	0.015	0.060	3	0.38	1.52
Q_1	0.020			0.51	
S	0.005		6	0.13	
S_1		0.098	6		2.49
α	0°	15°		0°	15°

NOTES:
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be 0.020 in. (0.51 mm) for lead numbers 1, 8, 9, and 16 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic pin spacing is 0.100 in. (2.54 mm) between centerlines. Each pin centerline shall be located within ±0.010 in. (0.25 mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (lead numbers 1, 8, 9, and 16).
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
8. All leads.
9. Fourteen spaces.

92CS-24787



The lead finish for the packaged types is in accordance with MIL- M-38510, Paragraph 3.6.2.5, Lead Finish "A". When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

Ceramic Dual-in-Line Packages (Cont'd)

14-LEAD DUAL-IN-LINE CERAMIC (FRIT-SEAL) PACKAGE JEDEC MO-001-AB

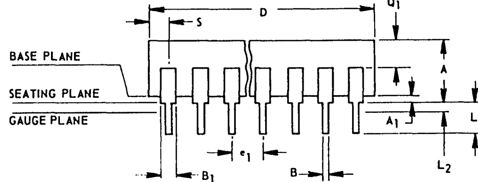
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012		0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

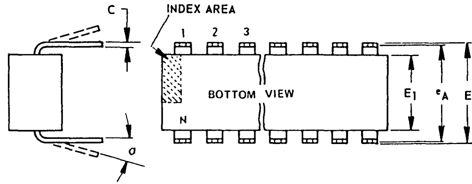
92SS-4296R2

16-LEAD DUAL-IN-LINE CERAMIC (FRIT-SEAL) PACKAGE JEDEC MO-001-AC

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012		0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R2



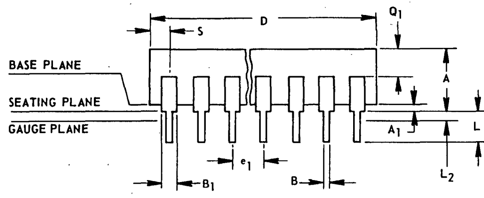


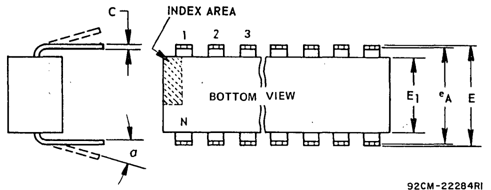
NOTES:

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

The lead finish for the packaged types is in accordance with MIL-M- 38510, Paragraph 3.6.2.5, Lead Finish "A". When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

Ceramic Dual-in-Line Packages (Cont'd)





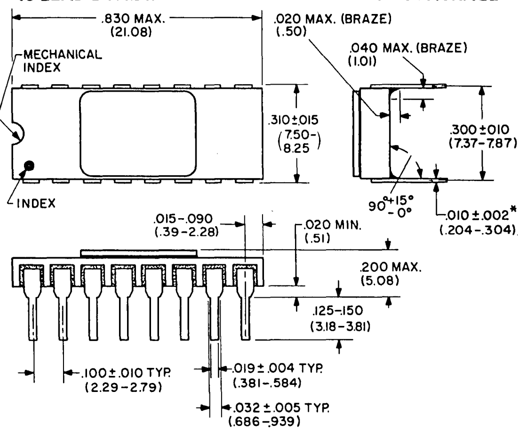
16-LEAD DUAL-IN-LINE CERAMIC (FRIT-SEAL) PACKAGE JEDEC MO-001-AG (CD4026AF, CD4029AF, CD4031AF, CD4033AF ONLY)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.165	0.210		4.20	5.33
A_1	0.015	0.045		0.381	1.14
B	0.015	0.020		0.381	0.508
B_1	0.045	0.070	7	1.15	1.77
C	0.009	0.011		0.229	0.279
D	0.750	0.795		19.05	20.19
E	0.295	0.325		7.50	8.25
E_1	0.245	0.300		6.23	7.62
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.120	0.160		3.05	4.06
L_2	0.000	0.030		0.000	0.76
a	2°	15°	4	2°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.080		1.27	2.03
S	0.010	0.060		0.254	1.52

NOTES

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. a applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.
7. B_1 applies to all leads except the four end leads which have one-half the normal width (B_1 min. = 0.025 in.)

16-LEAD DUAL-IN-LINE SIDE-BRAZED CERAMIC PACKAGE



*WHEN THIS DEVICE IS SUPPLIED SOLDER-DIPPED, THE MAX. LEAD THICKNESS (NARROW PORTION) WILL NOT EXCEED 0.013 (0.33mm)

NOTE: DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS AND ARE DERIVED FROM THE BASIC INCH DIMENSIONS

92CS-21219

The lead finish for the packaged types is in accordance with MIL-M-38510, Paragraph 3.6.2.5, Lead Finish "A". When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

Ceramic Dual-in-Line Packages (Cont'd)

24-LEAD CERAMIC DUAL-IN-LINE PACKAGE

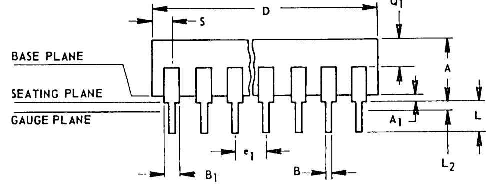
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A_1	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012		0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

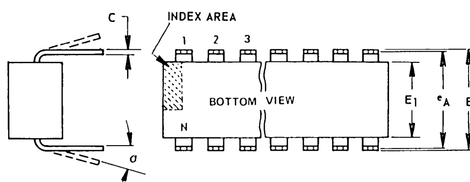
92CS-19948

28-LEAD CERAMIC DUAL-IN-LINE PACKAGE JEDEC MO-015-AH

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.100	.200	2.6	5.0	2
A_1	.000	.070	0	1.77	
B	.015	.020	.381	.508	
B_1	.015	.055	.39	1.39	
C	.008	.012	.204	.304	
D	1.380	1.420	35.06	36.06	
E	.600	.625	15.24	15.87	
E_1	.485	.515	12.32	13.08	
e_1	.100 TP		2.54 TP		3
e_A	.600 TP		15.24 TP		3
L	.100	.200	2.6	5.0	
L_2	.000	.030	0	.76	
α	0	15	0°	15°	4
N	28		28		5
N_1	0		0		6
Q_1	.020	.070	.51	1.77	
S	.040	.070	1.02	1.77	
See Note	1				

92CM-20250





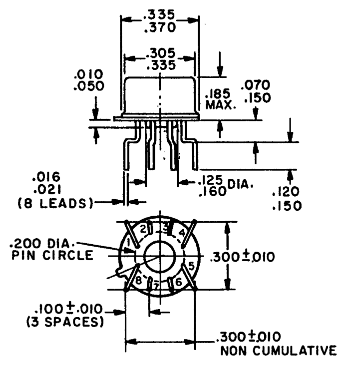
NOTES:

1. REFER TO RULES FOR DIMENSIONING (JEDEC PUBLICATION No. 13) AXIAL LEAD PRODUCT OUTLINES.
2. WHEN BASE OF BODY IS TO BE ATTACHED TO HEAT SINK, TERMINAL LEAD STAND-OFFS ARE NOT REQUIRED AND A_1 = 0. WHEN A_1 = 0, THE LEADS EMERGE FROM THE BODY WITH THE B_1 DIMENSION AND REDUCE TO THE B DIMENSION ABOVE THE SEATING PLANE.
3. e_1 AND e_A APPLY IN ZONE L_2 WHEN UNIT INSTALLED. LEADS WITHIN .005" RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION.
4. APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
5. N IS THE MAXIMUM QUANTITY OF LEAD POSITIONS.
6. N_1 IS THE QUANTITY OF ALLOWABLE MISSING LEADS.

The lead finish for the packaged types is in accordance with MIL-M-38510, Paragraph 3.6.2.5, Lead Finish "A". When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

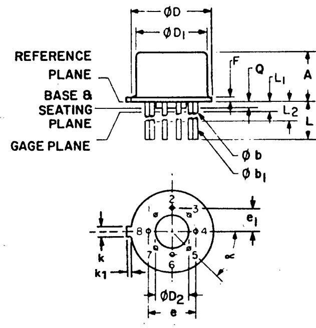
TO-5 Style Packages

8-LEAD TO-5 WITH DUAL-IN-LINE FORMED LEADS



92CS-20296R1

8-LEAD TO-5 STYLE PACKAGE MIL-M-38510 CASE OUTLINE A-1



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.165	0.185		4.19	4.70
ϕb	0.016	0.019	1	0.41	0.48
ϕb_1	0.016	0.021	1	0.41	0.53
ϕD	0.335	0.370		8.51	9.40
ϕD_1	0.305	0.335		7.75	8.51
ϕD_2	0.120	0.160		3.05	4.06
e	0.200 BSC		3	5.08 BSC	
e_1	0.100 BSC		3	2.54 BSC	
F		0.040			1.02
k	0.027	0.034		0.69	0.86
k_1	0.027	0.045	2	0.69	1.14
L	0.500	0.750	1	12.70	19.05
L_1	0.000	0.050	1	0.00	1.27
L_2	0.250		1	6.35	
Q	0.010	0.045		0.25	1.14
α	45° BSC		3	45° BSC	

NOTES:
1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500 in. (12.70 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500 in. (12.70 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019 in. (0.48 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.03 mm) −0.000 in. (0.00 mm) below the base plane of the product shall be within 0.007 in. (0.18 mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gage.

92CS-24774

The lead finish for the packaged types is in accordance with MIL-M-38510, Paragraph 3.6.2.5, Lead Finish "A".

TO-5 Style Packages (Cont'd)

10-LEAD TO-5 STYLE PACKAGE JEDEC MO-006-AF

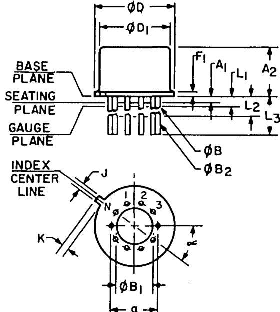
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230 TP		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0	0		0	0
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	36° TP			36° TP	
N	10		6	10	
N_1	1		5	1	

92CS-15835

12-LEAD TO-5 PACKAGE JEDEC MO-006-AG

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0	0		0	0
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	30° TP			30° TP	
N	12		6	12	
N_1	1		5	1	

92CS-19774



NOTES:

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

The lead finish for the packaged types is in accordance with MIL-M-38510, Paragraph 3.6.2.5, Lead Finish "A".

Operating Considerations for RCA Solid State Devices

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

TRANSISTORS AND THYRISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operatings to provide some slack or an expansion elbow in each lead to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

TRANSISTORS AND THYRISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange of a transistor be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device. Soldering is the preferred method for mounting thyristors; see "Rectifiers and Thyristors," below. Devices which cannot be soldered can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between device and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance not less than 1/8 inch from the plastic case. When

wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic high-power packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

Mounting

Recommended mounting arrangements and suggested hardward for the VERSAWATT package are given in the data bulletins for specific devices and in RCA Application Note AN-4142. When the package is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the package. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphtalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The package should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the device to become excessively high.

The TO-220AA plastic package can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the package to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term device life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with

respect to their component parts as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohol is an acceptable solvent. Examples of specific, acceptable alchols are isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44.

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing the "modified TO-5" package is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. This package can be mounted to the heat sink mechanically with glue or an expoxy adhesive, or by soldering, the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

RF POWER TRANSISTORS

Mounting and Handling

Stripline rf devices should be mounted so that the leads are not bent or pulled away from the stud (heat sink) side of the device. When leads are formed, they should be supported to avoid transmitting the bending or cutting stress to the ceramic portion of the device. Excessive stresses may destroy the hermeticity of the package without displaying visible damage.

Devices employing silver leads are susceptible to tarnishing; these parts should not be removed from the original tarnish-preventive containers and wrappings until ready for use. Lead solderability is retarded by the presence of silver tarnish; the tarnish can be removed with a silver cleaning solution, such as thiourea.

The ceramic bodies of many rf devices contain beryllium oxide as a major ingredient. These portions of the transistors should not be crushed, ground, or abraded in any way because the dust created could be hazardous if inhaled.

Operating

Forward-Biased Operation. For Class A or AB operation, the allowable quiescent bias point is determined by reference to the infrared safe-area curve in the appropriate data bulletin. This curve depicts the safe current/voltage combinations for extended continuous operation.

Load VSWR. Excessive collector load or tuning mismatch can cause device destruction by over-dissipation or secondary breakdown. Mismatch capability is generally included on the data bulletins for the more recent rf transistors.

See RCA RF Power Transitor Manual, Technical Series RMF-430, pp 39-41, for additional information concerning the handling and mounting of rf power transistors.

*Trade Mark: Emerson and Cumming, Inc.

INTEGRATED CIRCUITS

Handing

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect COS/MOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6000, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 10 kilohms to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current COS/MOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC operating and handling considerations, refer to Application Note ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

*Mil-M-38510A, paragraph 3.5.6.1 (a), lead material.

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