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NRMEC MOS/LSI

STANDARD BUILDING - BLOCK

CIRCUITS FOR CALCULATORS

Approved By

R.L. Doty
Vice President, Engineering
Microelectronics Company

NRMEC

APPLICATION NOTES

TYPICAL MOS/LSI STANDARD BUILDING-BLOCK CIRCUITS FOR CALCULATORS AND OTHER REAL-TIME DATA REDUCTION SYSTEMS

1. Scope

1.1 NRMEC has available for immediate application families of "standard" MOS/LSI (metal-oxide-semiconductor/large-scale-integrated) circuit chips, designed to provide logic and memory functions for calculators and other real-time data reduction equipment.

1.2 Within NRMEC's families of MOS/LSI circuit chips, the "standards" have been organized as "building blocks" for repetitive use in a number of equipment models meeting widely varying specifications.

1.3 These application notes cover a typical family of standards -- those for implementing a variety of calculator configurations. The notes are intended to give equipment designers an insight into the design potentials of NRMEC's building-block approach.

2. Reference: Pub. No. P71-10/701 Introduction to MOS/LSI Technology (NRMEC, 1971).

3. Circuit Terminology

3.1 General

The particular group of circuit chips described in these notes as being a typical NRMEC family of MOS/LSI standards form a set of modular building blocks for mechanizing calculator systems. The combination of chips selected to implement a system can be varied in type, quantity, and organization to construct calculators both conventional and programmable, and of any operational complexity required.

3.2 The Four Calculator Standards

3.2.1 Four MOS/LSI circuit chips comprise the set of NRMEC calculator standards.

3.2.1.1 "C" Chip: master control over other circuit chips in the set.

3.2.1.2 "A" Chip: performs decimal calculations.

3.2.1.3 "T" Chip: contains arithmetic and memory registers.

3.2.1.4 "S" Chip: contains (1) logic for an auxiliary Z register, exponents, and binary logic; and (2) an exponent register and a master time-base generator.

3.2.2 Circuit chips in a given standard set are completely interchangeable with those in other sets or with corresponding spare circuit chips. Handpicking of parts is not required. Equipment containing replacement devices will function precisely according to original specifications.

3.2.3 A variety of mounting methods are available: PCB, multilayer board, ceramic substrate, etc.

3.3 To complete a calculator configuration mechanized with C, A, T, and S chips, a NRMEC standard MOS ROM (read-only memory), custom-coded to implement unique customer requirements, is included in the configuration. Interfacing logic chips -- one, two, or three, depending upon the complexity of the input/output interfaces -- are either added from NRMEC's standard MOS/LSI product line or are custom-designed to customer specifications. Only power supplies and peripheral input/output equipment (displays, keyboards, typewriters, tape recorders and playback units, etc.) then are required to round out the system.

4. Basic Features

4.1 Word Length

In calculators formed from NRMEC standard calculator chips, all memory and operand registers are 20 digits long. Two discretes (inputs) set the timing to cause the machine to manipulate operands of length 10, 12, 14, or 16 decimal digits.

4.2 Decimal Point Modes

4.2.1 A machine made up of the standard chips may operate in either a fixed decimal point mode and/or a floating decimal point mode. In the floating-point mode, the machine operates on any number within the specified range of the calculator. It normalizes the result to allow the highest number of significant digits to be displayed and/or printed. Leading and trailing zeroes can be handled in various ways, depending on how the machine is programmed.

4.2.2 When the machine is operating in the fixed-point mode, the decimal point can be set manually over the range of values indicated in Table 1. All results may be displayed or printed as specified by the selected decimal setting. Other manners of outputting the results can be microprogrammed into the ROM.

Table 1. Range of Decimal Point Settings

Operand Length (Decimal Digits)	Point Setting Range
10	From 0 to 10
12	From 0 to 12
14	From 0 to 14
16	From 0 to 15

4.3 Rounding or Truncation

With the machine operating in either fixed-point or floating-point mode, the ROM can be programmed to:

4.3.1 Allow either manual or automatic roundoff of results

4.3.2 Allow either manual or automatic truncation of a result

4.4 Automatic Clear With Power Turn-On

The necessary logic is provided by the standard chips for initializing the calculator after power turn-on. In effect the power-on condition clears certain registers and can be used to set necessary conditions so that the machine is initialized to a specified state.

4.5 Multiple Memories

4.5.1 Multiple independent memories (as many as four) can be included in the calculator configuration to store cumulative totals or data constants while calculations are performed. The functions in which a particular memory register takes part are under ROM control and may vary from configuration to configuration -- i.e., a particular memory may be selected for use in chaining operations to hold a constant "divisor" or a multiplier, etc.

4.5.2 The term "chaining" refers to a sequence of similar (of equal precedence) operations, where "similar" is used to pair (1) multiply and divide operations or (2) add or subtract operations. In chaining, the result of the preceding operation may be used as input for the next operation, without the necessity for re-entering the result. Three types of chaining sequences are shown in Figure 1, where A, B, C, and D represent decimal numbers.

4.6 Constant Calculations

4.6.1 In certain calculations it may be convenient to:

4.6.1.1 Multiply many numbers by the same multiplier

4.6.1.2 Divide many numbers by the same divisor

4.6.1.3 Divide the same number by many divisors

4.6.2 The ROM can be programmed to permit such operations to be performed conveniently. The operations may make use of one or more of the memories that are included in the calculator configuration. Examples of the operations are shown in Figure 2.

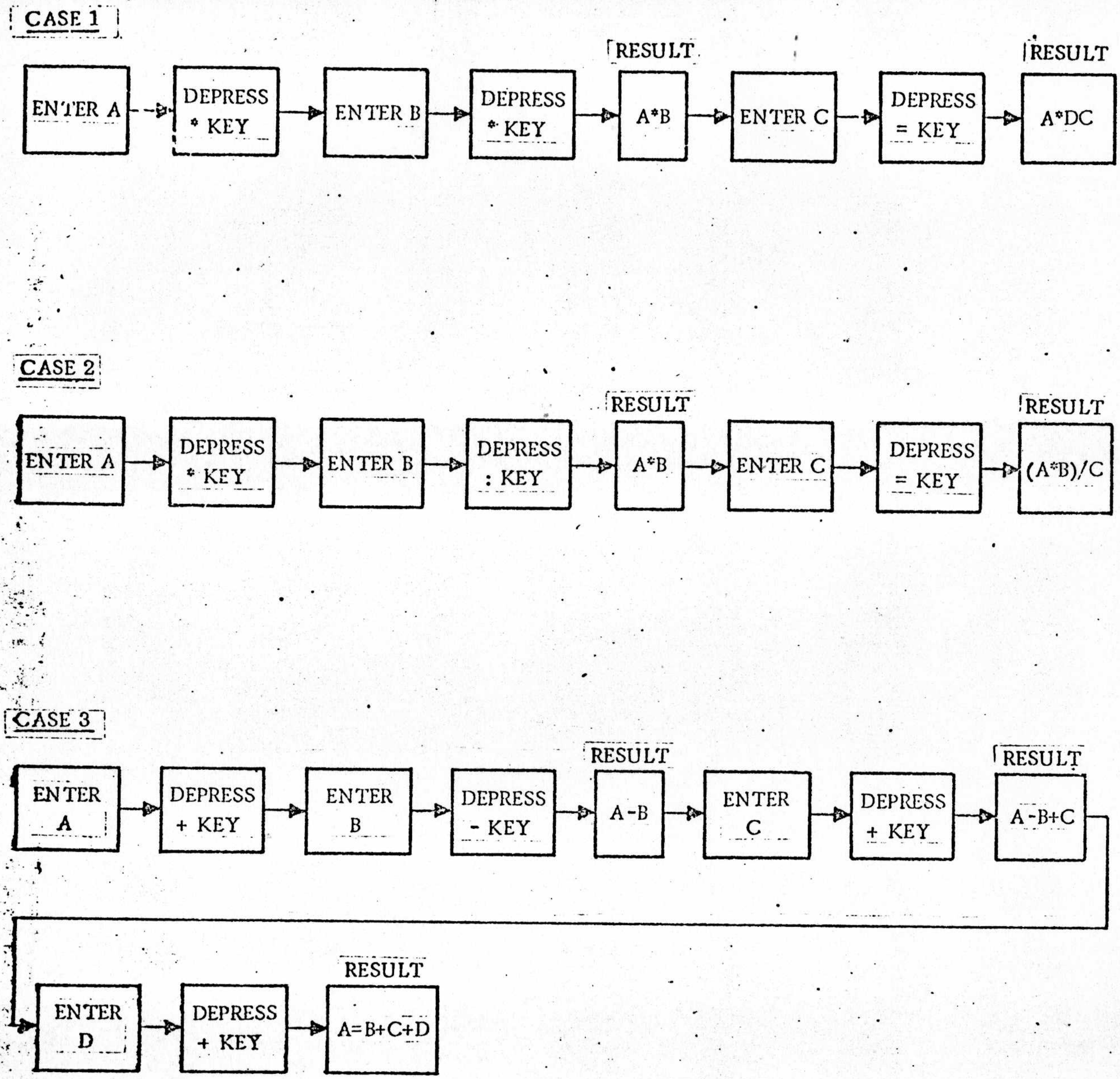

Figure 1. Chaining Operations

CASE 1. CONSTANT DIVISOR

ENTER A → DEPRESS : KEY → DEPRESS = KEY → RESULT A/B → ENTER C → DEPRESS = KEY → RESULT C/B

CASE 2. CONSTANT MULTIPLIER

ENTER A → DEPRESS * KEY → ENTER B → DEPRESS = KEY → RESULT A*B → ENTER C → DEPRESS = KEY → RESULT A*C

CASE 3. CONSTANT DIVIDEND

ENTER A → DEPRESS : KEY → ENTER B → DEPRESS = KEY → RESULT A/B → ENTER C → DEPRESS = KEY → RESULT A/C

Figure 2. Constant Calculation Operations

4.7 Internal Clock Generation

Because the S chip contains an internal clock, the calculator formed from the standard chips requires no external clocking. If it is desired, however, the standard-chip calculator can operate on external clock signals of the appropriate duration and timing. Synchronization of input/output to the keyboard, displays, and/or other peripheral input/output equipment is accomplished in the custom interface.

5. Arithmetic Capabilities

5.1 Calculators formed from NRMEC standard calculator chips are capable of performing all operations on operands and yield results which have the algebraically correct sign and magnitude.

5.2 The basic set of operations includes:

5.2.1 Addition

5.2.2 Subtraction

5.2.3 Multiplication

5.2.4 Division

5.2.5 Square root calculation

5.2.6 Percentage calculation

5.2.7 Various combinations of operations 5.2.1 through 5.2.6.

5.3 The routines to perform operations 5.2.1 through 5.2.7, and to handle normal input/output are microprogrammed into a ROM.

5.4 If expanded capabilities (additional functions) are required, a second ROM can be used to mechanize them. Such functions might include, for example:

5.4.1 Trigonometric functions

5.4.2 Exponentiation

5.4.3 Averaging

5.4.4 Standard deviation calculation

6. Programmable Calculator

6.1 With the addition of only two more chips -- a program-control chip and a program ROM chip -- programmability can be included as a feature of the standard-chip calculator. This feature:

6.1.1 Allows a stored program of 200 steps to be entered into the machine. (The length can be increased in blocks of 200 steps, up to a maximum of 1,000 steps, by adding one shift register chip for each 200-step increment.

6.1.2 Provides for either single-step or automatic sequencing of program steps.

6.1.3 Allows normal keyboard mode operation.

6.1.4 Provides subroutine generation with two levels of program returns.

7. The Four Calculator Chips -- C, A, T, S

7.1 The C Chip

7.1.1 The C chip serves as a master control over other chips in the standard calculator chip set. Although only 150 by 150 mils in size, the C chip implements 240 logical equations.

7.1.2 The C chip contains status registers which are used to indicate such conditions as those in which the calculator is in an "add" state, has overflowed, or has an error.

7.1.3 The C chip senses the status of selected registers, the status of flip-flops or discretes as selected by a ROM address, and the status of keyboard inputs such as the decimal pointing. Using this information, the C chip generates output commands to coordinate the activities of the other standard calculator chips.

7.2 The A Chip

7.2.1 The 160-mil-square A chip performs decimal calculations. Included on the A chip is circuitry for input/output logic control of the data entered into the various registers. The chip implements 250 logical equations.

7.2.2 Specifically, the A chip contains: a serial decimal adder, a ROM address register, a two-level stack for return address storage, register status-determining logic, X and Y register storage and shift logic, and operand inter-register transfer logic.

7.3 The T Chip

7.3.1 The T chip contains the arithmetic registers and the memory registers. It implements 200 equations and measures approximately 150 by 160 mils in size.

7.3.2 The T chip provides:

7.3.2.1 Storage for four numbers (of length 10, 12, 14, or 16 decimal digits, depending upon the model) in four memory registers.

7.3.2.2 Storage for values (exponents) which indicate the decimal point setting of the four memory registers.

7.3.2.3 Three 73-bit registers for operands X, Y, and Z.

7.3.2.4 Interfacing logic to a keyboard.

7.3.2.5 An output signal to indicate the maximum decimal point setting permissible on the model.

7.4 The S Chip

7.4.1 The S chip contains logic for the auxiliary register Z, exponents, and binary logic. It also contains the exponent register and the master time-base generator. Two hard-wired inputs to the S chip cause the time-base to generate clocking for word lengths of 10, 12, 14, or 16 digits. The chip implements 250 equations and is approximately 140 by 160 mils overall.

7.4.2 Specifically, the S chip:

7.4.2.1 Generates timing signals.

7.4.2.2 Contains a binary adder.

7.4.2.3 Contains seven bits of the Z register and logic for either left-shifting or right-shifting the contents of Z.

7.4.2.4 Contains the eight-bit exponent registers associated with the operand registers X, Y, and Z.

7.4.2.5 Contains logic for decoding ROM and C chip commands.

7.4.2.6 Contains logic for determining the condition of the Z register and outputting the status.

7.4.2.7 Generates the algebraic sign to be used by the decimal adder.

7.4.2.8 Generates a "power on" signal.

8. <u>ROM Circuit(s)</u>

8.1 The ROM circuitry implements the microprogram for the set of standard calculator chips. In addition, the ROM contains the 4-phase clock for the calculator.

8.2 The ROM is available with three different capacities -- 256, 384, or 512 words of 17 bits each. There may be as many as four micro instructions per word.

8.3 In a two-ROM configuration, ROM No. 1 would contain the 4-phase clock and the more "conventional" instructions. ROM No. 2 would be used to perform additional functions such as sin, cos, or exponential operators.

9. <u>Input/Output Chip(s)</u>

Depending upon requirements of the particular calculator system, from one to four input/output interfacing chips are necessary.

10. <u>Programmability</u>

Additional dynamic storage is required to configure for a programmable calculator. From one to three additional chips are needed for this storage, depending upon the length of the program (number of instructions) and the type of instructions which are to be implemented.

11. Register Expandability

11.1 A "TT" chip may be substituted for the T chip, and with the addition of one or two "M" chips either eight or 16 independent full registers may be obtained.

11.2 The TT chip performs functions 5.2.3, 5.2.4, and 5.2.5, listed earlier in these notes. The TT chip also performs register selection for 1-of-16.

11.3 Each M chip contains eight memory registers, including decimal point and sign of each word.

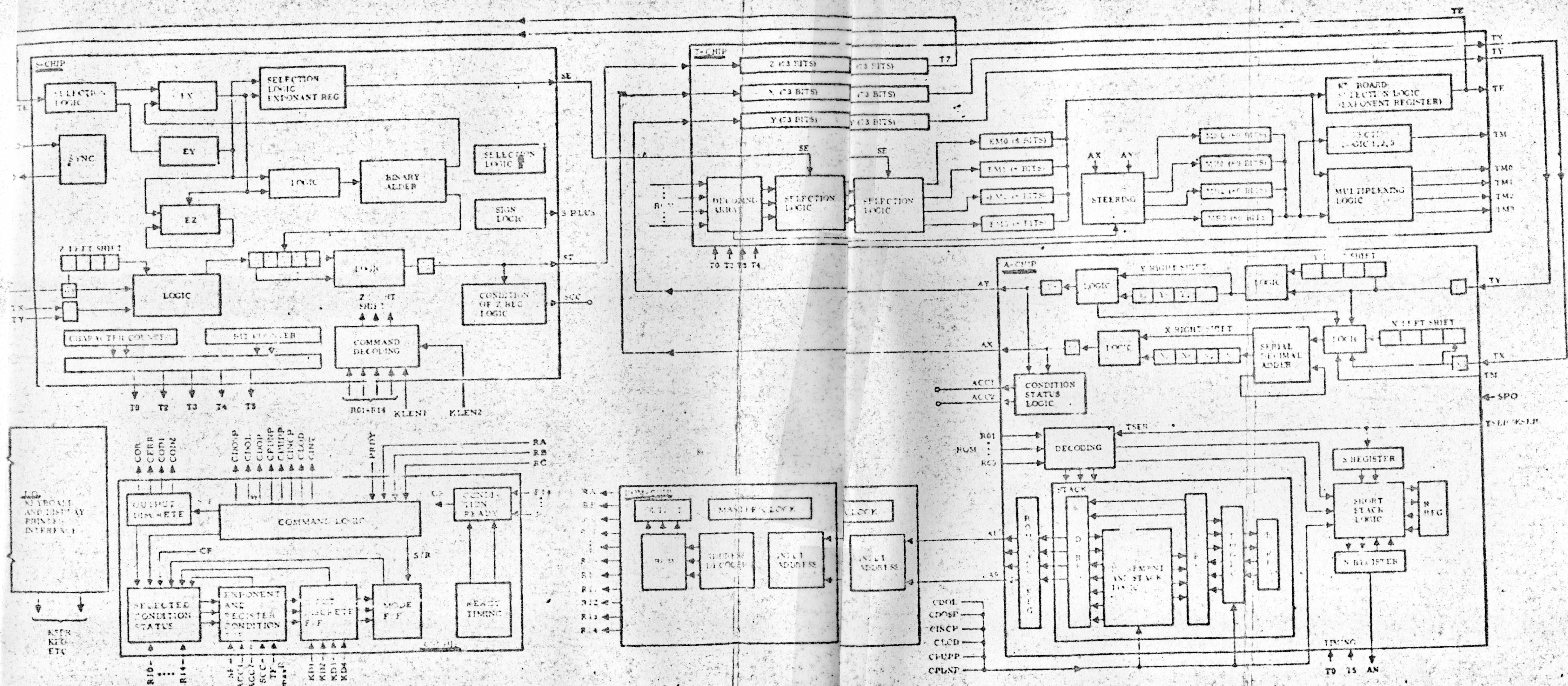

Figure 3. Example of a C-A-T-S Calculator -- Implemented with One Set of NRMEC Standard C, A, T, and S Calculator Chips; One ROM Chip; and Input/Output Interfacing Chip(s)

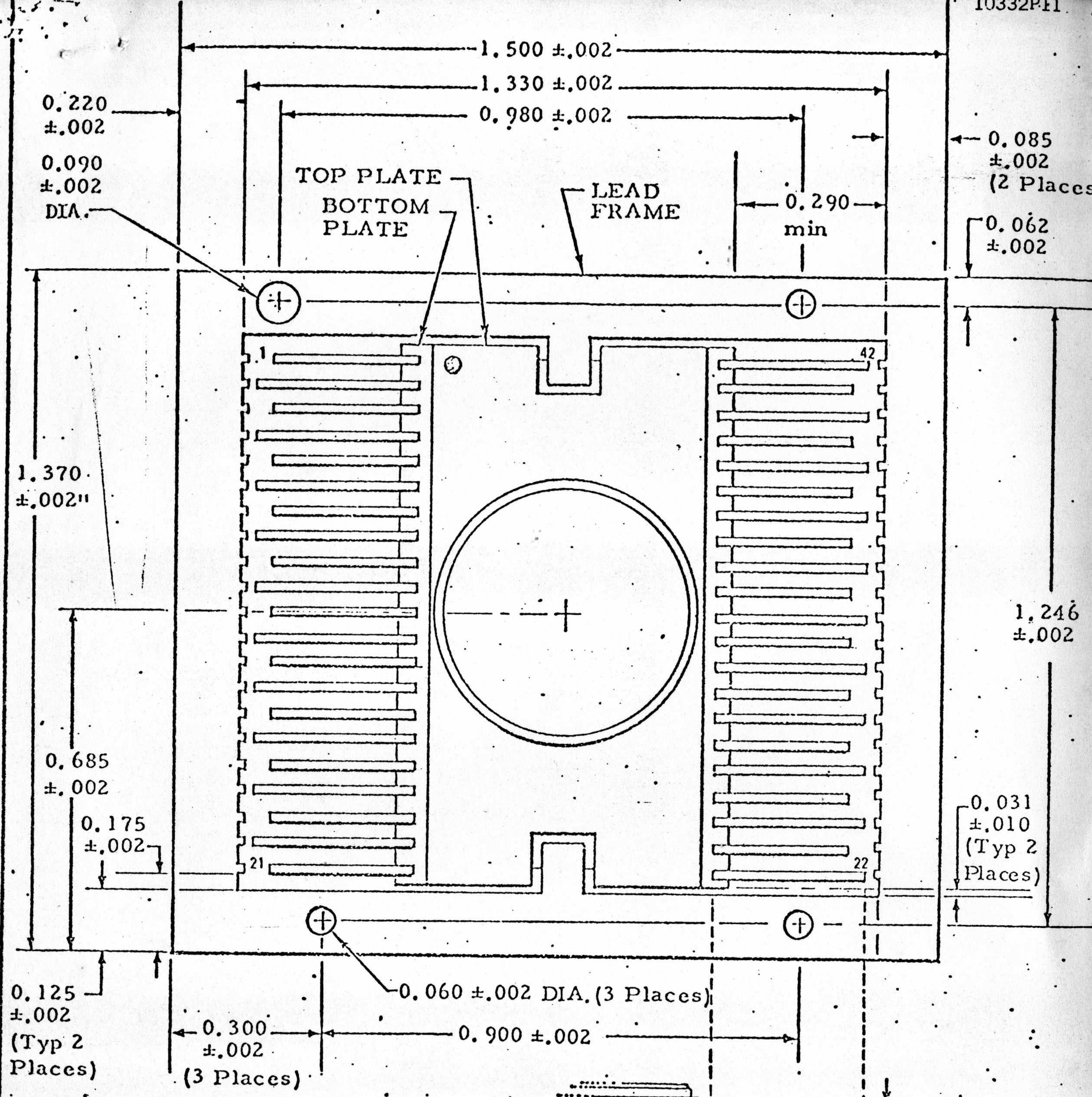

Figure 1. NRMEC 42 LEAD FLAT PACKAGE IN LEAD FRAME AFTER STAGGER CUTTING OF LEADS