COMMUNICATION PRODUCTS

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Rockwell International

Semiconductor Products Division

Order No. 4

1989
COMMUNICATION PRODUCTS
DATA BOOK

Rockwell International
Semiconductor Products Division

Order No. 4
January 1989

Rockwell Semiconductor Products Division is headquartered in Newport Beach, California with Field Sales Offices located throughout the United States, Canada, Europe and the Far East. Their listings, plus those of domestic and international representatives and distributors, appear in Appendix A.

Definition of Document Types

Document Type	Product Status	Definition
Product Preview	Formative or Development	The document type contains the general features and/or specifications for a product in definition or development. The features and/or specifications may change in any manner without notice.
Product Summary	Development or Production	This document type contains the general features and/or specifications of a product in development or in production. Additional information is usually available in a separate document, not contained in this book, such as a Designer's Guide.
Data Sheet (Preliminary)	Sampling or Pre-Production	This document type contains preliminary or design-to-characteristic data for a product in pre-production. Additional and/or refined characteristic data will be released in subsequent revisions to the document.
Data Sheet	Production	This document type contains final specification information resulting from measured characteristics. This document type is subject to revision if characteristics are further refined during production.
Product Description	Production	This document type contains final specification information resulting from measured characteristics along with additional application aid information. This document type is subject to revision if characteristics are further defined during production.
Application Note	Development or Production	This document type contains application aids in the use of the subject product. Schematics included in an application note are intended to convey system design concept only.

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DIAL-UP DATA MODEMS

EXPERIENCE MAKES A DIFFERENCE

Rockwell offers a complete line of 1200 to 9600 bits per second (bps) OEM modem products that can easily be incorporated into your communications systems requiring high performance, quality and reliability while maintaining a competitive cost advantage. Whether the modem application is for personal computer communications or for installation into remote monitoring equipment, Rockwell has the product with the features, form factor and cost advantage to meet your business objectives.

With the dial-up (PSTN) market advancing so quickly, time to market is critical. Rockwell offers a complete family of products that address every segment of the dial-up market. For the low power applications such as laptops (battery powered), Rockwell offers the RC224AT, a complete single device modem, and the RC2324DP, Rockwell's true quad function (V.21, V.22A/B, V.22 bis, and V.23) modem. Rockwell also provides products that easily assist you in migrating to higher speeds. The R96QT is a value added V.22 bis modem that communicates at 9600 bps, and the RC9696DP is a "turbo charged" R9696DP with fall-forward capability to 12000 bps full duplex operation. With throughput increasingly more critical over dial-up lines, data compression and error correction protocols are crucial features. For integrated applications, Rockwell offers the RC224AT, which provides the "AT" command set, error correction and data compression protocols in addition to standard modem features.

System designers now have a product line that completely meets their needs including a smooth migration path from all of Rockwell's current products to any future requirements.

Model	Data Speed (bps)	Compliance
R212AT	1200, 0-300	Bell 212A, 103; "AT" Command Set
R212DP	1200, 0-300	Bell 212A, 103
R1212	1200, 600, 0-300	CCITT V.22 A/B; Bell 212A, 103
R2424	2400, 1200, 600, 0-300	CCITT V.22 bis, V.22 A/B; Bell 212A, 103
RC224AT	2400, 1200, 600, 0-300	CCITT V.22 bis, V.22 A/B, V.21; Bell 212A, 103; "AT" Command Set
RC2324SME	2400, 1200, 600, 0-300	CCITT V.22 bis, V.22 A/B, V.23, V.21, Bell 212A, 103; V.25 bis Commands, "AT" Commands, MNP 3, 4, 5
RC2324DP	2400, 1200, 600, 0-300	CCITT V.22 bis, V.22 A/B V.21, V.23; Bell 212A, 103
R96QT	9600, 7200, 4800, 2400, 1200 600, 300	V.29 (HDX), V.22 bis, V.22 A/B; Bell 212A, 103
R9696DP	1200, 9600, 4800, 7200	V.32, V.22 bis, V.22, V.21 V.23; Bell 212A, 103

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R212DP
Modem Device Set
Bell 212A Compatible

1

INTRODUCTION

The R212DP/DS Data Pump device set is a high performance 1200/300 bps modem. Using state-of-the-art VLSI technology, the R212DP provides the entire modulation/demodulation process, high and low band filtering, and complete auto dialing function in only two devices.

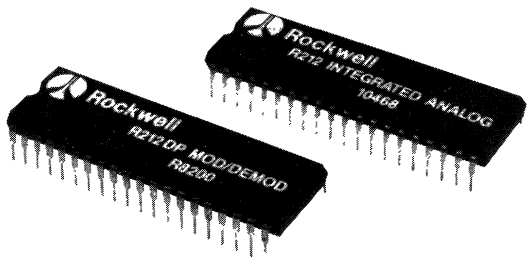
The R212DP is ideal for data transmission over the 2-wire dial-up network. Bell 212A and 103 compatible, the R212DP can handle virtually all applications for full-duplex 1200 bps and 0 to 300 bps asynchronous data transmission over the public switched telephone network (PSTN).

The RS-232-C compatible interface integrates easily into a personal computer, box modem, terminal or any other communications product. The added feature of an integral asynchronous serial auto dialer capable of dialing with DTMF tones or pulses from its 40-byte character buffer offers the user added flexibility in creating a 1200 bps modem customized for specific packaging and functional requirements.

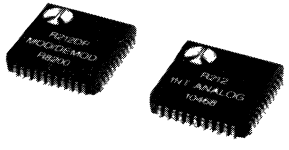
An R212DP/EB Evaluation Board is also available to aid modem system design and evaluation. Included on the printed circuit board are the R212DP/DS modem device set, RS-232-C connector, power connector, an RJ-11 phone jack, six LED indicators, and four configuration switches. The evaluation board comes with an in-depth R212DP Device Set Designer's Guide (Order No. 678) and a wall-mount power supply. All that is required to use the R212DP/EB is an RS-232-C cable connected to a terminal or computer, and a phone cord.

FEATURES

- 2 Device Implementation
  - — R8200 Modulator/Demodulator
  - — 10468 Integrated Analog
- Bell 212A and 103 Compatible (2-Wire Full-Duplex)
  - — Asynchronous
    - 1200 bps DPSK (+1%, −2.5%)
    - 0–300 bps FSK
    - Auto Fallback, Answer Mode
- DTE Interface
  - — Functionally: RS-232-C Compatible
  - — Electrically: TTL
- Auto/Manual Answer
- Auto/Manual Dial
  - — DTMF or Pulses
  - — 0–9 # *, T P CR (ASCII)
  - — 40-Byte Character Buffer
- 10-Bit Character Length
- Break Generation/Detection
- Send/Receive Space Disconnect
- Automatic Adaptive Equalizer
- Analog Loopback
  - — 0 to 300 bps, 1200 bps
- Packaging Options
  - — 40-pin Plastic DIP
  - — 44-pin PLCC

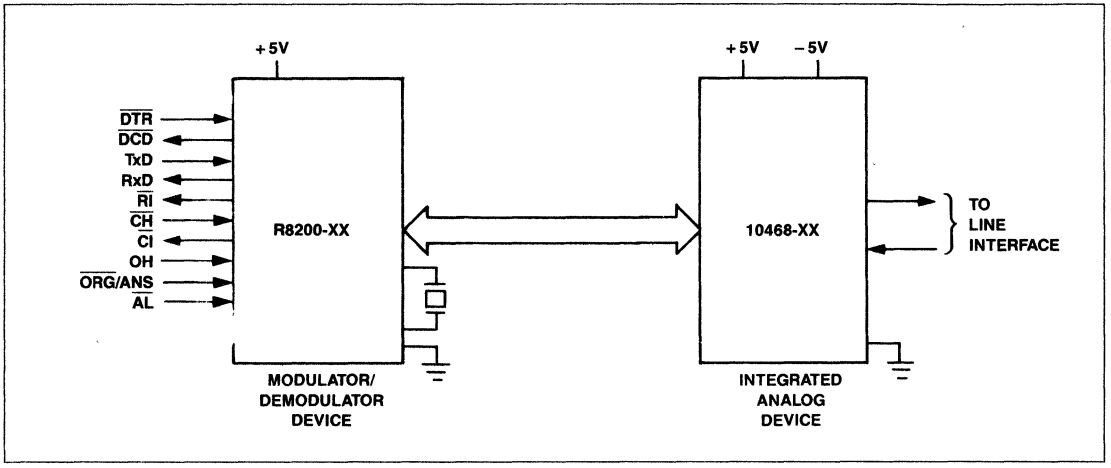


40-PIN DIP



44-PIN PLCC

R212DP/DS Modem Device Set



R212DP/DS Modem Device Set Interface Diagram

SPECIFICATIONS

Power Consumption

+5 Vdc ±5% <300 mA
−5 Vdc ±5% <40 mA
600 mW (typical)

Environmental

Temperature: Operating 0°C to 70°C
Storage −55°C to +150°C
Relative Humidity: Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

R212AT Modem Device Set
"AT" Command Set
Bell 212A Compatible

INTRODUCTION

The R212AT/DS ("AT" Command Set Compatible) device set is a high performance 1200/300 bps modem. Using state-of-the-art VLSI technology, the R212AT provides the entire modulation/demodulation process, high and low band filtering, and an enhanced "AT" Command Set in only two devices.

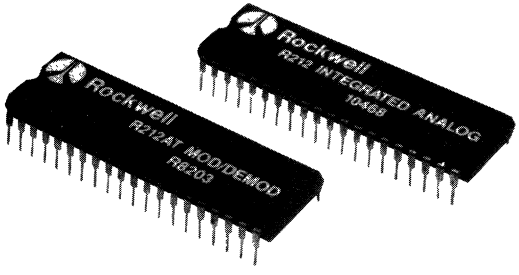
The R212AT is ideal for data transmission over the 2-wire dial-up network. Bell 212A and 103 compatible, the R212AT can handle virtually all applications for full-duplex 1200 bps and 0 to 300 bps asynchronous data transmission over the public switched telephone network (PSTN).

The RS-232-C compatible interface integrates easily into a personal computer, box modem, terminal or any other communications product. The added features of the enhanced "AT" Command Set offer the user added flexibility in creating a 1200 bps modem customized for specific packaging and functional requirements. The R212AT can be readily used with industry standard communication software packages.

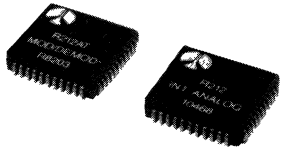
An R212AT/EB Evaluation Board is also available to aid modem system design and evaluation. Included on the printed circuit board are the R212AT/DS modem device set, RS-232-C connector, power connector, two RJ-11 phone jacks, 11 LED indicators, four configuration switches, and a speaker with volume control. The evaluation board comes with a detailed R212AT Device Set Designer's Guide (Order No. 686), and a wall-mount power supply. All that is required to use the R212AT/EB is an RS-232-C cable connected to a terminal or computer, and a phone cord.

FEATURES

- 2 Device Implementation
  - — R8203 Modulator/Demodulator
  - — 10468 Integrated Analog
- Bell 212A and 103 Compatible (2-Wire Full-Duplex)
  - — 1200 bps DPSK (+1%, −2.5%) asynchronous
  - — 0–300 bps FSK asynchronous
  - — Auto Fallback, Answer Mode
- Auto/Manual Answer
- Auto/Manual Dial
- "AT" Command Set (see reverse side)
- DTE Interface
  - — Functionally: RS-232-C Compatible
  - — Electrically: TTL
- Data Format
  - — 7 Data Bits; 1 or 2 Stop Bits; Even, Odd, or Fixed Parity
  - — 8 Data Bits; 1 or 2 Stop Bits; No Parity
- Automatic Adaptive Equalizer
- Packaging Options
  - — 40-pin Plastic DIP
  - — 44-pin PLCC



40-PIN DIP

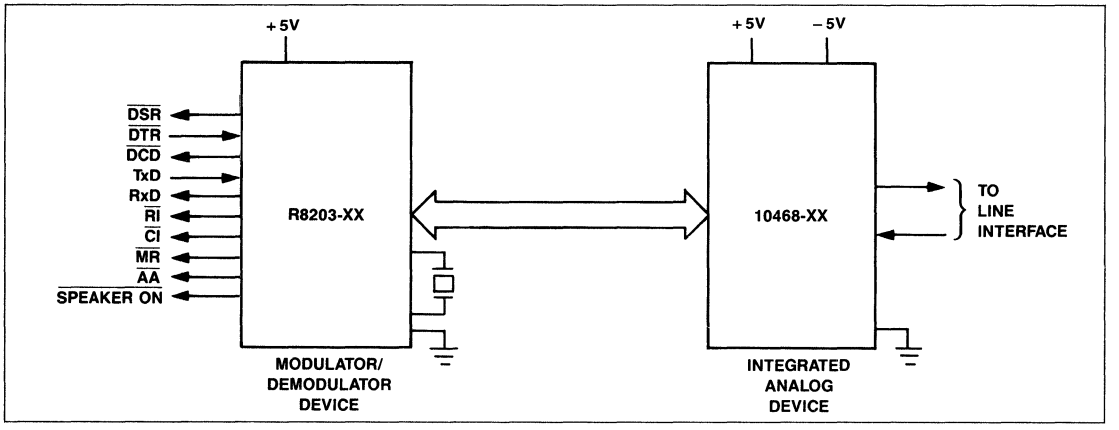


44-PIN PLCC

R212AT/DS Modem Device Set

R212AT "AT" Command Set

Command	Function	Command	Function	Command	Function
AT	Attention Code	Sr=n	Set Register	H	On/Off Hook
A/	Repeat Last Command	V	Verbal/Numeric	I	Returns Product Code
A	Answer		Result Code	M	Speaker On/Off
D	Dial	,	Pause	O	On Line
R	Reverse Dial	;	Return to Command	Q	Quiet On/Off
T	Tone Dial		State After Dialing	Z	Reset
P	Pulse Dial	E	Echo On/Off	+++	Escape Code
Sr?	Read Register				



R212AT/DS Modem Device Set Interface Diagram

SPECIFICATIONS

Power Consumption

+5 Vdc ±5% <300 mA
−5 Vdc ±5% <40 mA
600 mW (typical)

Environmental

Temperature: Operating 0°C to 70°C
Storage −55°C to +150°C
Relative Humidity: Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

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RC224AT 2400 bps Single Device Modem with "AT" Commands

INTRODUCTION

The RC224AT is an integrated 2400 bps full-duplex modem supplied in either one or two CMOS VLSI packages. The RC224AT complies with CCITT V.22 bis and V.22 A/B recommendations, and meets Bell 212A and 103 standards. The RC224AT also implements a 2400 "AT" command set.

Two versions of the RC224AT are available. The RC224AT/1 integrates digital signal processing (DSP) and integrated analog (IA) functions into a single VLSI package.

The RC224AT/2 2-device set performs the same functions as the RC224AT/1 single device with the addition of a memory expansion bus. The RC224AT/2 supplies DSP and IA functions in separate packages.

The RC224AT may operate over a parallel or serial interface to the host. A hardware input selects either parallel or serial host interface upon power turn-on or reset. The parallel host interface emulates a 16C450 UART and is compatible with IBM PC, PC/XT, PC/AT, or PS/2 systems. The serial host interface is CCITT V.24 (EIA-232-D) logic compatible with TTL levels.

RC224AT based modem designs reduce the bill of material due to the elimination of an external microprocessor and parallel/serial (UART) devices. This results in significant cost savings for OEM customers.

Implemented in low power CMOS, the RC224AT is also designed especially for portable and/or battery powered applications. Power requirements are further reduced when sleep (power down) mode is enabled.

The RC224AT is based on a new generation CMOS microcontroller, the MicroDSP. The MicroDSP combines the best features of an 8-bit microcomputer with a digital signal processor. The MicroDSP enables the RC224AT to handle traditional microprocessor functions, such as the AT command interpretation, without degrading performance in core modulation and demodulation of digital signal processing functions.

FEATURES

- No external microcomputer and PROM required
- Built-in DTE interfaces supported:
  - Parallel 16C450
  - Serial CCITT V.24 (EIA-232-D)
- Implements new Hayes commands
  - &V, &Wn, &Yn, &Zn=x, and S=n as a dial modifier
- NVRAM interface allows storage of two user configurations and four 36-digit dial strings
- 40-character command line
- Automatic sleep mode and wake-up
- Expansion PROM interface permitting user-modification of AT commands
- Compatibilities
  - CCITT V.22 bis, V.22 A/B
  - Bell 212A and 103
  - Hayes "AT" 2400B and 2400 command set
- Low power requirements:
  - 305 mW (typical) operating
  - 37 mW (typical) sleep (power down) mode
- Call progress and dialing features:
  - Detect: busy, ringback and dial tone
  - Wait for quiet answer
  - Programmable speaker volume control
  - DTMF and pulse dial
  - Programmable pause interval
  - Flash PBX support
  - Wait for dial tone before dialing
  - Originate call from answer-mode modem
- Automatic adaptive and fixed compromise equalization
- A/A1 feature for multi-line key telephones
- RC224AT/1 (1 device) packaging
  - 64-pin plastic QUIP
  - 68-pin PLCC
- RC224AT/2 (2-device set) packaging
  - DSP: 64-pin plastic QUIP or 68-pin PLCC
  - IA: 40-pin plastic DIP or 44-pin PLCC

GENERAL DESCRIPTION

The major hardware signal interfaces of the single-device RC224AT/1are illustrated in Figure 1-a. The major hardware interface signals of the RC224AT/2 are shown in Figure 1-b.

Additional design information is described in the RC224AT Designer's Guide (Order No. 845).

DEVICES

MicroDSP

The MicroDSP is a medium speed modem engine offering high speed central processing at a 6 MHz (internal clock) instruction execution rate. The MicroDSP performs the modem digital signal processing, command set interpreting, line control, and modem control processing. Two pulse rate multipliers optimize performance by generating precision timing for the analog filters.

Integrated Analog

The integrated analog function is divided into three sections: transmitter, receiver, and telephone line interface. The transmitter section contains a digital-to-analog (D/A) converter, bandsplit and lowpass filters, a guard tone generator, and a transmit level attenuator. The receiver section implements variable gain control, bandsplit filters, and an analog-to-digital (A/D) converter. The telephone interface circuitry provides relay drivers for off-hook, talk/data, and A/A1 relays.

SUPPORTED INTERFACES

"AT" Command Line

A 40-character command line is provided. The command line starts with AT and may contain several commands. A separator is not required between the commands. The AT prefix and the terminating CR prefix are not counted in the character total. Spaces are counted; as are left and right parenthesis.

Parallel Host Interface

When the parallel PC bus interface is selected by a hardware input signal (use of $\overline{HWT}$), a 16C450 compatible parallel interface is provided.

Indicator Interface (Serial Interface only)

When the serial interface is selected, four signals are output by the DSP to the indicator interface ($\overline{DCDL}$, $\overline{MR/TEST}$, $\overline{AAE}$, and $\overline{OHRELAY}$). The 2-device RC224AT/2 also outputs the $\overline{DTRL}$ indicator signal.

Serial Host Interface

When the serial interface is selected by a hardware input signal ($\overline{SEREN}$ = GND), a V.24 (EIA-232-D) compatible interface is provided.

NVRAM Interface

A serial interface to an optional user-supplied 1024-bit non-volatile RAM (NVRAM) is provided. The NVRAM can store up to two user-selectable configurations which can take precedence over the factory default setting, and can store up to four 36-digit dial strings.

Speaker Interface

An interface to an externally supplied speaker circuit is provided. The speaker can be used to monitor call progress. The AT Ln command can be used to adjust the volume in suitable steps.

Expansion ROM Interface (RC224AT/2 Only)

An expansion bus is provided to interface with an optional user-supplied 8k-byte PROM, as a user option. This PROM can be used to alter the AT command set.

SLEEP (POWER DOWN) MODE

To minimize the modem power consumption, the RC224AT includes a sleep (power down) mode which may be enabled or disabled. If enabled, the RC224AT enters sleep mode whenever the modem has been inactive from 30 seconds to one minute. (Note that the modem never enters power down mode while in data mode.) The modem returns to full operation whenever a ring signal occurs, or the host writes to the DSP (parallel interface) or the DTR input is asserted (serial interface). In the serial interface, the V.24 and indicator outputs are forced high in the sleep mode to save power.

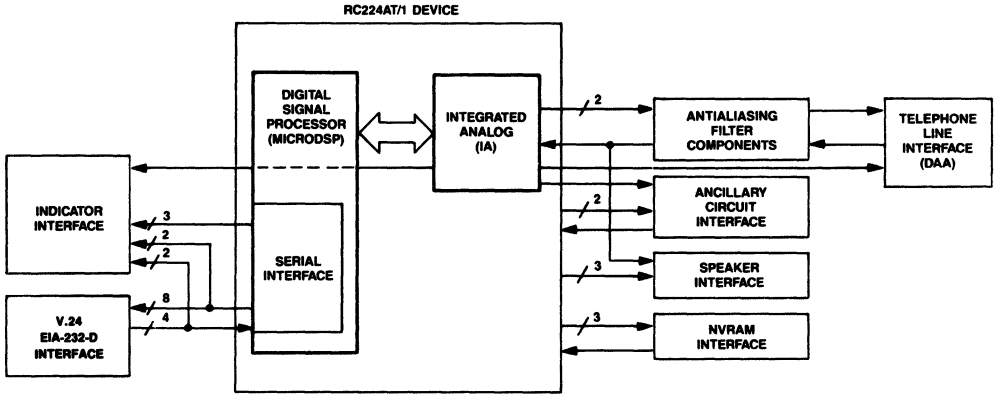
TECHNICAL SPECIFICATIONS

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

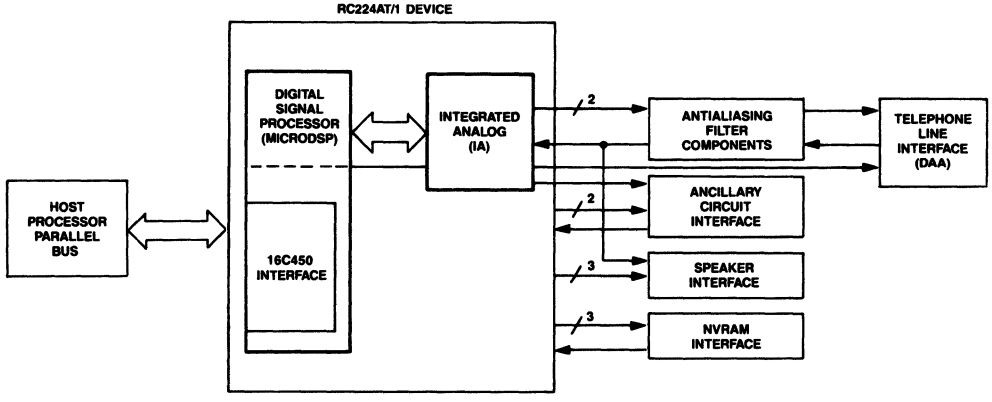
TONE GENERATION

DTMF Tone: A DTMF tone pair can be generated with an frequency accuracy of ±1.5%. The dial digit tone pairs are:

Dial Digit	Tone 1	Tone 2
0	941	1336
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
*	941	1209
#	941	1477
A	697	1633
B	770	1633
C	852	1633
D	941	1633

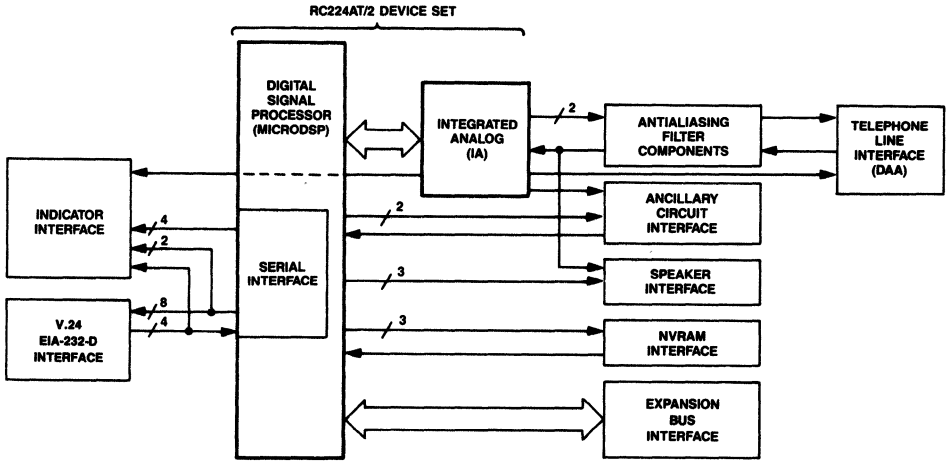


a. Serial Host Interface

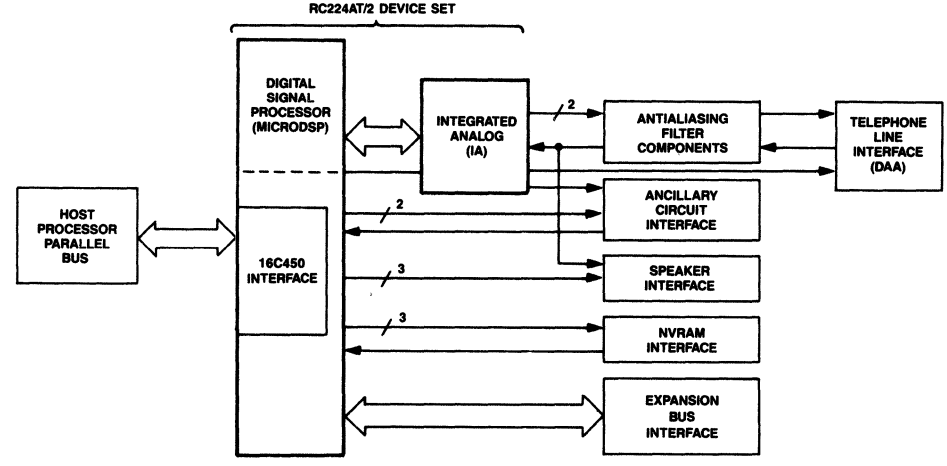


b. Parallel Host Interface

Figure 1-a. RC224AT/1 General Interface



a. Serial Host Interface



b. Parallel Host Interface

Figure 1-b. RC224AT/2 General Interface

Guard Tone: A guard tone of 550 ± 20 Hz or 1800 ± 20 Hz can be generated at 3 ±1 dB or 6 ±1 db below the transmit level, respectively.

Answer Tone: A CCITT (2100 ±15 Hz) or Bell (2225 ±10 Hz) answer tone is generated depending on the selected configuration.

DATA ENCODING

The data encoding conforms to CCITT Recommendations V.22 bis or V.22, or to Bell 212A or 103, depending on the selected configuration.

LINE EQUALIZATION

Transmitter and receiver digital filters compensate for delay and amplitude distortion during operation on nominal phone lines. In addition, automatic adaptive equalization in the receiver minimizes the effects of intersymbol interference.

TRANSMITTED DATA SPECTRUM

The transmitted spectrum is shaped by the square root of a 75% raised cosine filter function.

TRANSMIT LEVEL

The transmitter level is –10 dBm ±1 dB.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with the applicable CCITT recommendation.

RECEIVE LEVEL

The receiver satisfies performance requirements for a received line signal from –9 dBm to –43 dBm. The carrier detect is ON at –43 dBm and OFF at –48 dBm with a minimum of 2 dB hysterisis.

RECEIVER TIMING

The modem can track a frequency error up to ±0.01% in the associated transmit timing source.

CARRIER RECOVERY

The modem can track a frequency offset up to ±7 Hz in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

TRANSMISSION SPEED

With the parallel interface, the transmission rate of the host computer must be 110, 300, 1200, or 2400 bps. The modem will connect at the selected speed or will fallback to the speed set by the remote modem with the serial interface, the DTE transmission speed is speed sensed.

When the modem answers a call, it determines the transmission speed from the carrier signal of the originating modem. V.22 bis ORG can also adapt so that the setting of the modem is matched to the remote system.

AT COMMAND SET

The AT command set is Hayes 2400B compliant. The commands are divided into three types; basic commands, dial modifiers, and ampersand commands as listed in Table 2. The supporting S registers are listed in Table 3.

AT COMMAND DATA RATE

With the parallel interface, AT commands to the modem in the local command state must be asynchronous, ASCII coded, and transmitted at rates of 110, 300, 1200, or 2400 bps. With the serial interface, the rate is speed sensed for parity and format.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Transmitter Carrier Frequency (Hz) ±0.01%		Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits Per Symbol	Constellation Points
		Answer	Originate				
V.22 bis	QAM	2400	1200	2400	600	4	16
V.22A/B	DPSK	2400	1200	1200	600	2	4
Bell 212A	DPSK	2400	1200	1200	600	2	4
Bell 103	FSK	2225 M 2025 S	1270 M 1070 S	300	300	1	1

Notes: 1. Modulation legend: QAM Quadrature Amplitude Modulation
DPSK Differential Phase Shift Keying
FSK Frequency Shift Keying

2. M indicates a mark condition, S indicates a space condition.

Table 2. RC224AT "AT" Command Set Summary

Basic Commands	Function
AT	Attention Code
A	Answer Command
A/	Repeat Last Command
Bn	Communications Standard Option
C1	Carrier Control Option
D	Dial Command
En	Off-line Character Echo Option
F1	On-line Character Echo Option
Hn	Switch Hook Control Option
In	Identification/Checksum Option
Ln	Speaker Volume Option
Mn	Speaker Control Option
On	On-line Command
P	Pulse Dial
Qn	Result Code Display Option
Sn	Select an S Register
Sn=	Write to an S Register
Sn?	Read an S Register
T	Touch Tone Dial
Vn	Result Code Form Option
Xn	Result Code Set/Call Progress Option
Yn	Long Space Disconnect Option
Zn	Recall Stored Profile Command
+++	Escape Code Sequence
,	Pause

Dial Modifiers	Function
P	Pulse Dial
R	Originate Call in Answer Mode
S=n	**Dial Stored Number (n=0:3)***
T	Touch Tone Dial
W	Wait for Dial Tone
;	Return to Idle State
@	Wait for Quiet Answer Command
!	Flash Hook
,	Pause
0–9	Dial Digits/Characters
A,B,C,D	
#,*	

Ampersand Commands	Function
&Cn	Data Carrier Detect Option
&Dn	Data Terminal Ready Option
&F	Load Factory Defaults
&Gn	Guard Tone Option
&Jn	Auxiliary Relay Control
&Mn	Communications Mode Option
&Pn	Make to Break Ratio Selection
&Qn	Communications Mode Option
&Sn	Data Set Ready Option
&Tn	Test Command Selection
&V	**View Active Configuration and User Profiles***
&Wn	**Store Active Profile***
&Xn	Synchronous Transmit Clock Source Option
&Yn	**Select Stored Profile on Powerup Option***
&Zn=x	**Store Telephone Number (n=0:3)***

* = New Commands

Table 3. RC224AT S Register Summary

Register	Function
S0*	Ring to Answer On
S1	Ring Count
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait For Dial Tone
S7	Wait Time for Data Carrier
S8	Pause Time for Comma
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang-up Delay
S11	DTMF Dialing Speed
S12	Escape Code Guard Time
S14*	Bit Mapped Options Register
S16	Modem Test Options
S18*	Test Timer
S21*	Bit Mapped Options Register
S22*	Bit Mapped Options Register
S23*	Bit Mapped Options Register
S25*	Delay to DTR
S26*	RTS to CTS Delay Interval
S27*	Bit Mapped Options Register

Notes:
*This S-Register is stored in the modem NVRAM upon receipt of the &W command so that the contents are preserved when modem power is removed.

HARDWARE INTERFACE SIGNALS

The RC224AT/1 pin assignments are shown in Figure 2 and listed in Table 4. The RC224AT/1 hardware interface signals are shown in Figure 3.

The RC224AT/2 pin assignments are shown in Figure 4 and listed in Table 5. The RC224AT/2 interface signals are shown in Figure 5.

The RC224AT/1 and RC224AT/2 digital and analog characteristics are described in Tables 6 and 7, respectively.

The RC224AT hardware interface signals are described in Table 8. The signal definitions apply to both RC224AT/1 and RC224AT/2 except as noted.

APPLICATION

Recommended modem circuits based on the RC224AT/1 are shown in Figures 6-a and 6-b for serial and parallel interfaces, respectively.

Recommended modem circuits based on the RC224AT/2 are shown in Figures 7-a and 7-b for serial and parallel interfaces, respectively.

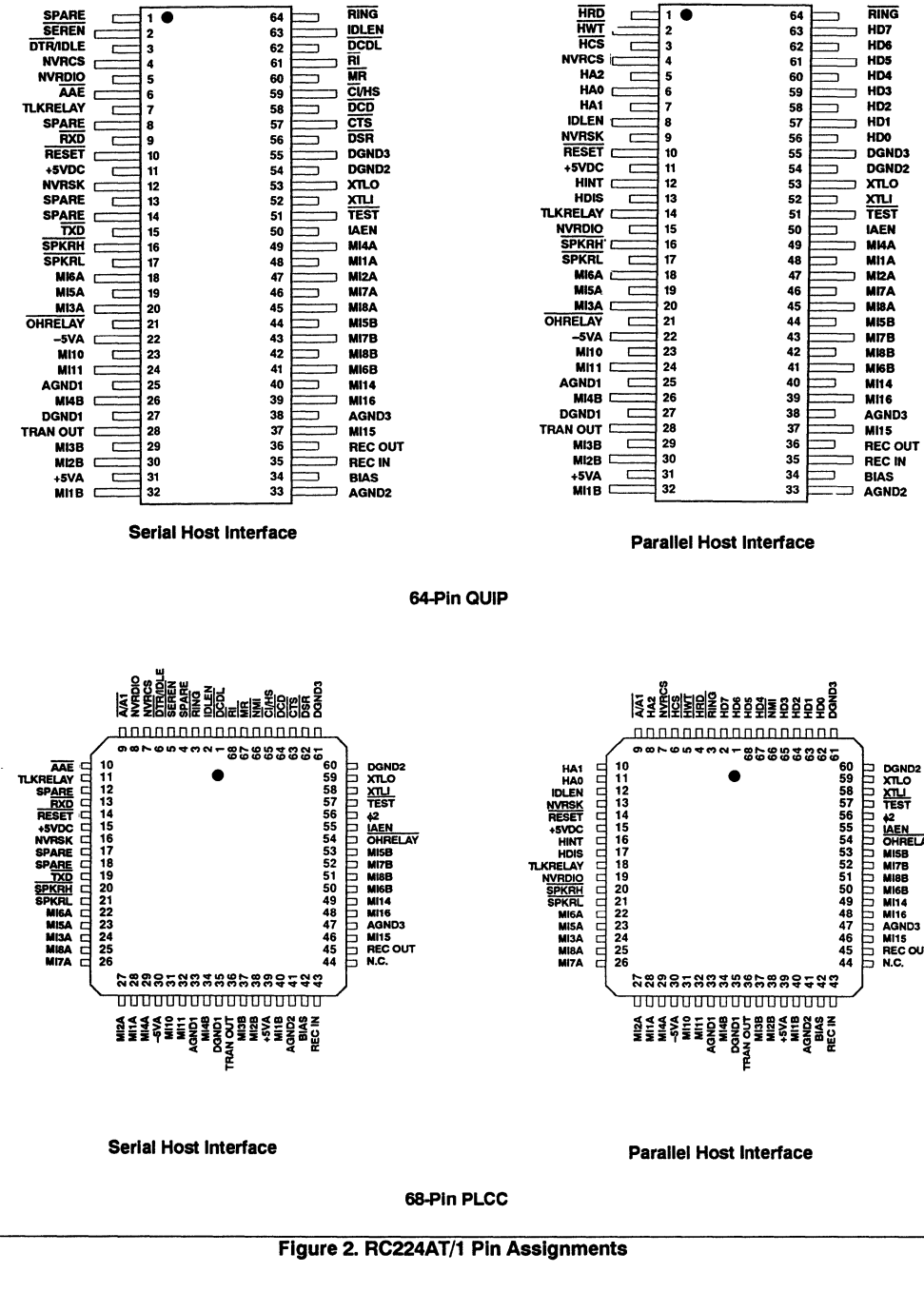


Figure 2. RC224AT/1 Pin Assignments

Table 4-a. RC224AT/1 Pin Assignments-Serial

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Label	I/O Type
4	1	RTS	IA
5	2	SEREN	IA
6	3	DTR/IDLE	IA
7	4	NVRCS	OA
8	5	NVRDIO	IA/OA
9	–	A/A1	OA
10	6	AAE	OA
11	7	TLKRELAY	OA
12	8	RDCLK	OA
13	9	RXD	OA
14	10	RESET	IB
15	11	+5VDC	
16	12	NVRSK	OA
17	13	XTCLK	IA
18	14	TDCLK	OA
19	15	TXD	IA
20	16	SPKRH	OA
21	17	SPKRL	OA
22	18	MI6A	TO MI6B
23	19	MI5A	TO MI5B
24	20	MI3A	TO MI3B
54	21	OHRELAY	OD
30	22	–5VA	
31	23	MI10	
32	24	MI11	
33	25	AGND1	
34	26	MI4B	TO MI4A
35	27	DGND1	
36	28	TRAN OUT	O (DD)
37	29	MI3B	TO MI3A
38	30	MI2B	TO MI2A
39	31	+5VA	
40	32	MI1B	TO MI1A
41	33	AGND2	
42	34	BIAS	
43	35	REC IN	I (DB)
44	–	N.C.	
45	36	REC OUT	O (DA)
46	37	MI15	
47	38	AGND3	
48	39	MI16	
49	40	MI14	
50	41	MI6B	TO MI6A
51	42	MI8B	TO MI8A
52	43	MI7B	TO MI7A
53	44	MI5B	TO MI5A
25	45	MI8A	TO MI8B
26	46	MI7A	TO MI7B
27	47	MI2A	TO MI2B
28	48	MI1A	TO MI1B
29	49	MI4A	TO MI4B
55	50	IAEN	OA
56	–	φ2	OA
57	51	TEST	IA
58	52	XTLI	IE
59	53	XTLO	OB
60	54	DGND2	
61	55	DGND3	
62	56	DSR	OA
63	57	CTS	OA
64	58	DCD	OA
65	59	CI/HS	OA
66	–	NMI	IA
67	60	MR	OA
68	61	RI	OA
1	62	DCDL	OA
2	63	IDLEN	IA
3	64	RING	IA

Notes:
1. MI = Modem Interconnection (e.g., MI7), see Figure 3.
2. N.C. = No Connection, leave pin disconnected (open).
3. I/O types are described in Table 6 (digital signals) and in Table 7 (analog signals).

Table 4-b. RC224AT/1 Pin Assignments-Parallel

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Label	I/O Type
4	1	HRD	IA
5	2	HWT	IA
6	3	HCS	IA
7	4	NVRCS	OA
8	5	HA2	IA
9	–	A/A1	OA
10	6	HA1	IA
11	7	HA0	IA
12	8	IDLEN	I
13	9	NVRSK	OA
14	10	RESET	IA
15	11	+5VDC	IA
16	12	HINT	OA
17	13	HDIS	OA
18	14	TLKRELAY	OA
19	15	NVRDIO	IA/OA
20	16	SPKRH	OA
21	17	SPKRL	OA
22	18	MI6A	TO MI6B
23	19	MI5A	TO MI5B
24	20	MI3A	TO MI3B
54	21	OHRELAY	OD
30	22	–5VA	
31	23	MI10	
32	24	MI11	
33	25	AGND1	
34	26	MI4B	TO MI4A
35	27	DGND1	
36	28	TRAN OUT	O (DD)
37	29	MI3B	TO MI3A
38	30	MI2B	TO MI2A
39	31	+5VA	
40	32	MI1B	TO MI1A
41	33	AGND2	
42	34	BIAS	
43	35	REC IN	I (DB)
44	–	N.C.	
45	36	REC OUT	O (DA)
46	37	MI15	
47	38	AGND3	
48	39	MI16	
49	40	MI14	
50	41	MI6B	TO MI6A
51	42	MI8B	TO MI8A
52	43	MI7B	TO MI7A
53	44	MI5B	TO MI5A
25	45	MI8A	TO MI8B
26	46	MI7A	TO MI7B
27	47	MI2A	TO MI2B
28	48	MI1A	TO MI1B
29	49	MI4A	TO MI4B
55	50	IAEN	OA
56	–	φ2	OA
57	51	TEST	IA
58	52	XTLI	IE
59	53	XTLO	OB
60	54	DGND2	
61	55	DGND3	
62	56	HD0	IA/OA
63	57	HD1	IA/OA
64	58	HD2	IA/OA
65	59	HD3	IA/OA
66	–	NMI	IA
67	60	HD4	IA/OA
68	61	HD5	IA/OA
1	62	HD6	IA/OA
2	63	HD7	IA/OA
3	64	RING	IA

Notes:
1. MI = Modem Interconnection (e.g., MI7), see Figure 3.
2. N.C. = No Connection, leave pin disconnected (open).
3. I/O types are described in Table 6 (digital signals) and in Table 7 (analog signals).

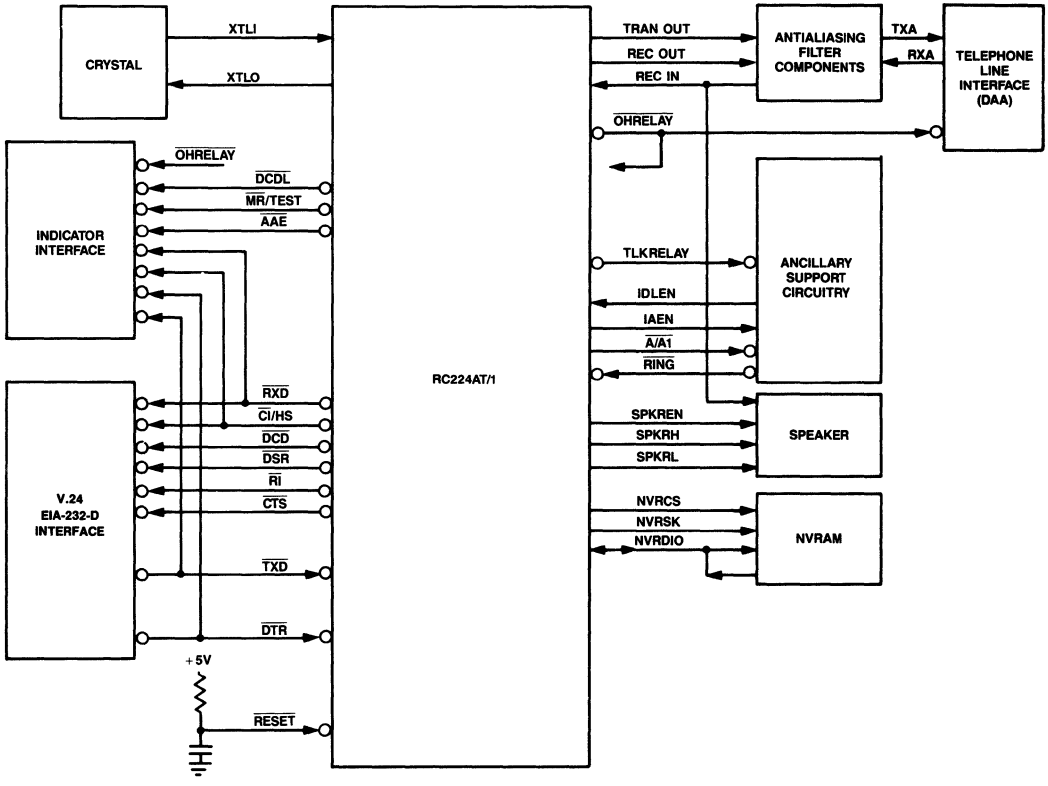


Figure 3-a. RC224AT/1 Interface Signals-Serial Interface

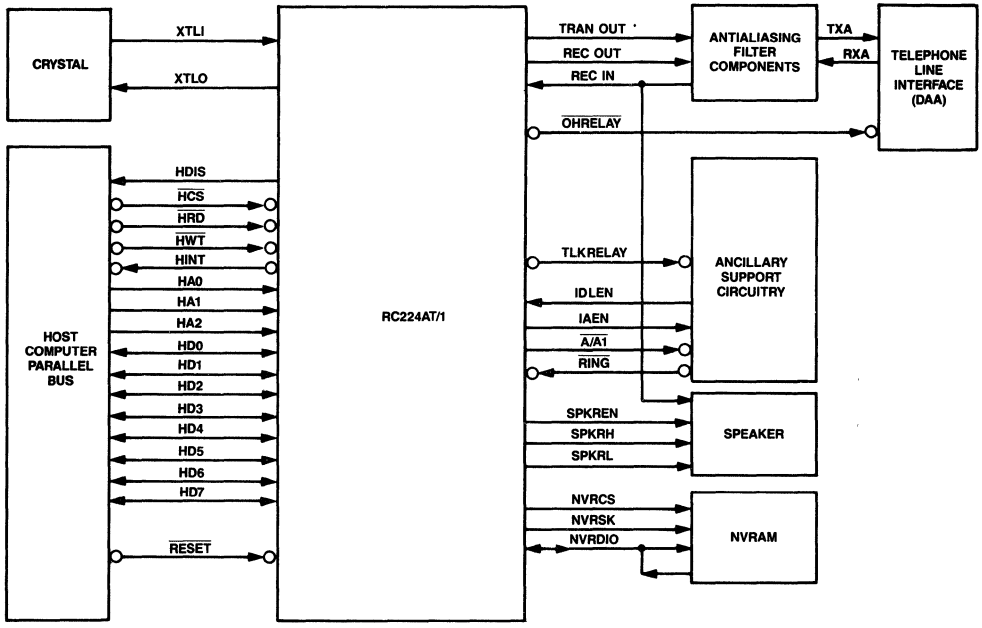
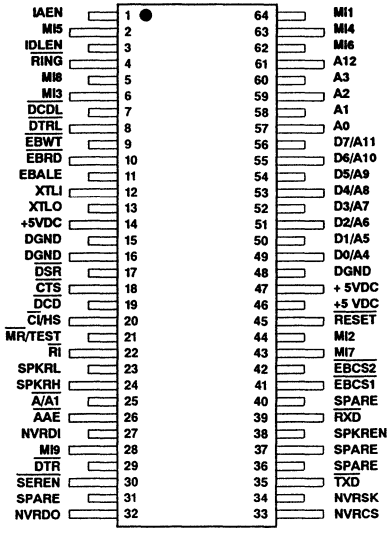
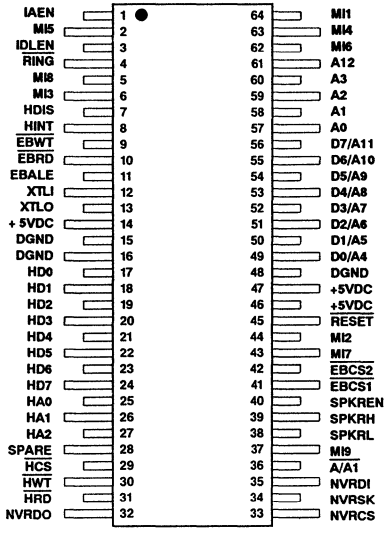


Figure 3-b. RC224AT/1 Interface Signals-Parallel Interface

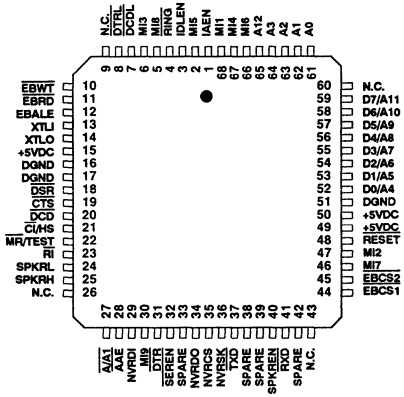


Serial Host Interface

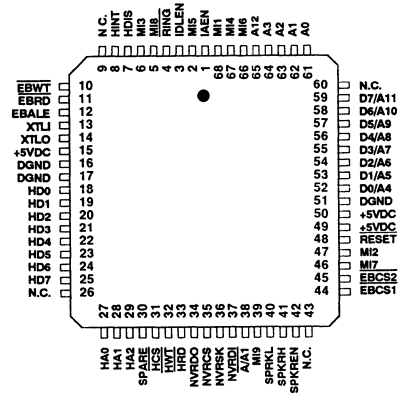


Parallel Host Interface

64-Pin QUIP



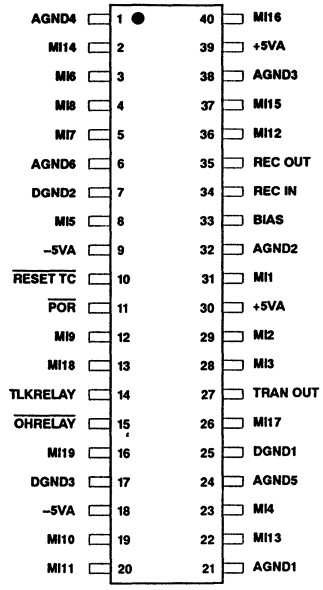
Serial Host Interface



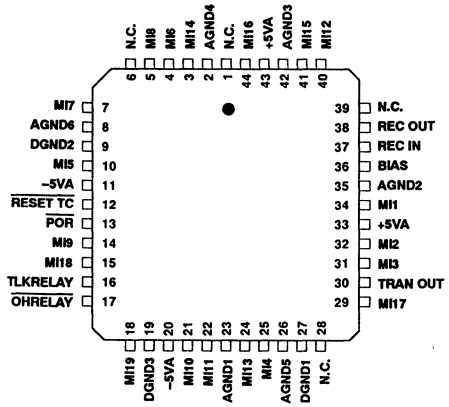
Parallel Host Interface

68-Pin PLCC

Figure 4-a. RC224AT/2 Pin Assignments-DSP Device



40-PIN DIP (IA)



44-PIN PLCC

Figure 4-b. RC224AT/2 Pin Assignments-IA Device

Table 5-a. RC224AT/2 DSP Pin Assignments-Serial

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Label	I/O Type
1	1	IAEN	OA
2	2	MI5	
3	3	IDLEN	IA
4	4	RING	IA
5	5	MI8	
6	6	MI3	
7	7	DCDL	OA
8	8	DTRL	OA
9	–	N.C.	
10	9	EBWT	OA
11	10	EBRD	OA
12	11	EBALE	OA
13	12	XTLI	IE
14	13	XTLO	OB
15	14	+5VDC	
16	15	DGND	
17	16	DGND	
18	17	DSR	OA
19	18	CTS	OA
20	19	DCD	OA
21	20	CI/HS	OA
22	21	MR/TEST	OA
23	22	RI	OA
24	23	SPKRL	OA
25	24	SPKRH	OA
26	–	N.C.	
27	25	A/A1	OA
28	26	AAE	OA
29	27	NVRDI	OA
30	28	MI9	
31	29	DTR	IA
32	30	SEREN	IA
33	31	SPARE	IA
34	32	NVRD0	IA
35	33	NVRCS	OA
36	34	NVRSK	OA
37	35	TXD	IA
38	36	SPARE	OA
39	37	SPARE	IA
40	38	SPKREN	OA
41	39	RXD	OA
42	40	SPARE	OA
43	–	N.C.	
44	41	EBCS1	OA
45	42	EBCS2	OA
46	43	MI7	
47	44	MI2	
48	45	RESET	IB
49	46	+5VDC	
50	47	+5VDC	
51	48	DGND	
52	49	D0/A4	IA/OA
53	50	D1/A5	IA/OA
54	51	D2/A6	IA/OA
55	52	D3/A7	IA/OA
56	53	D4/A8	IA/OA
57	54	D5/A9	IA/OA
58	55	D6/A10	IA/OA
59	56	D7/A11	IA/OA
60	–	N.C.	
61	57	A0	OA
62	58	A1	OA
63	59	A2	OA
64	60	A3	OA
65	61	A12	OA
66	62	MI6	
67	63	MI4	
68	64	MI1	

NOTES:
1. MI = Modem Interconnection (e.g., MI7), see Figure 3.
2. N.C. = No Connection, leave pin disconnected (open).
3. I/O types are described in Table 6 (digital signals) and in Table 7 (analog signals), respectively.

Table 5-b. RC224AT/2 DSP Pin Assignments-Parallel

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Label	I/O Type
1	1	IAEN	OA
2	2	MI5	
3	3	IDLEN	IA
4	4	RING	IA
5	5	MI8	
6	6	MI3	
7	7	HDIS	OA
8	8	HINT	OA
9	–	N.C.	
10	9	EBWT	OA
11	10	EBRD	OA
12	11	EBALE	OA
13	12	XTLI	IE
14	13	XTLO	OB
15	14	+5VDC	
16	15	DGND	
17	16	DGND	
18	17	HD0	IA/OA
19	18	HD1	IA/OA
20	19	HD2	IA/OA
21	20	HD3	IA/OA
22	21	HD4	IA/OA
23	22	HD5	IA/OA
24	23	HD6	IA/OA
25	24	HD7	IA/OA
26	–	N.C.	
27	25	HA0	IA
28	26	HA1	IA
29	27	HA2	IA
30	28	SPARE	
31	29	HCS	IA
32	30	HWT	IA
33	31	HRD	IA
34	32	NVRD0	IA
35	33	NVRCS	OA
36	34	NVRSK	OA
37	35	NVRDI	OA
38	36	A/A1	OA
39	37	MI9	
40	38	SPKRL	OA
41	39	SPKRH	OA
42	40	SPKREN	OA
43	–	N.C.	
44	41	EBCS1	OA
45	42	EBCS2	OA
46	43	MI7	
47	44	MI2	
48	45	RESET	IB
49	46	+5VDC	
50	47	+5VDC	
51	48	DGND	
52	49	D0/A4	IA/OA
53	50	D1/A5	IA/OA
54	51	D2/A6	IA/OA
55	52	D3/A7	IA/OA
56	53	D4/A8	IA/OA
57	54	D5/A9	IA/OA
58	55	D6/A10	IA/OA
59	56	D7/A11	IA/OA
60	–	N.C.	
61	57	A0	OA
62	58	A1	OA
63	59	A2	OA
64	60	A3	OA
65	61	A12	OA
66	62	MI6	
67	63	MI4	
68	64	MI1	

NOTES:
1. MI = Modem Interconnection (e.g., MI7), see Figure 3.
2. N.C. = No Connection, leave pin disconnected (open).
3. I/O types are described in Table 6 (digital signals) and in Table 7 (analog signals), respectively.

Table 5-c. RC224AT/2 IA Pin Assignments

44-Pin PLCC Pin Number	40-Pin DIP Pin Number	Signal Label	I/O Type
1	–	N.C.	
2	1	AGND4	
3	2	MI14	
4	3	MI6	
5	4	MI8	
6	–	N.C.	
7	5	MI7	
8	6	AGND6	
9	7	DGND2	
10	8	MI5	
11	9	–5VA	
12	10	RESET TC	IA
13	11	POR	IA/OA
14	12	MI9	
15	13	MI18	
16	14	TLKRELAY	OD
17	15	OHRELAY	OD
18	16	MI19	
19	17	DGND3	
20	18	–5VA	
21	19	MI10	
22	20	MI11	
23	21	AGND1	
24	22	MI13	
25	23	MI4	
26	24	AGND5	
27	25	DGND1	
28	–	N.C.	
29	26	MI17	
30	27	TRAN OUT	O (DD)
31	28	MI3	
32	29	MI2	
33	30	+5VA	
34	31	MI1	
35	32	AGND2	
36	33	BIAS	
37	34	REC IN	I (DB)
38	35	REC OUT	O (DA)
39	–	N.C.	
40	36	MI12	
41	37	MI15	
42	38	AGND3	
43	39	+5VA	
44	40	MI16	

LEGEND:
1. MI = Modem Interconnection (e.g., MI7), see Figure 3.
2. N.C. = No Connection, leave pin disconnected (open).

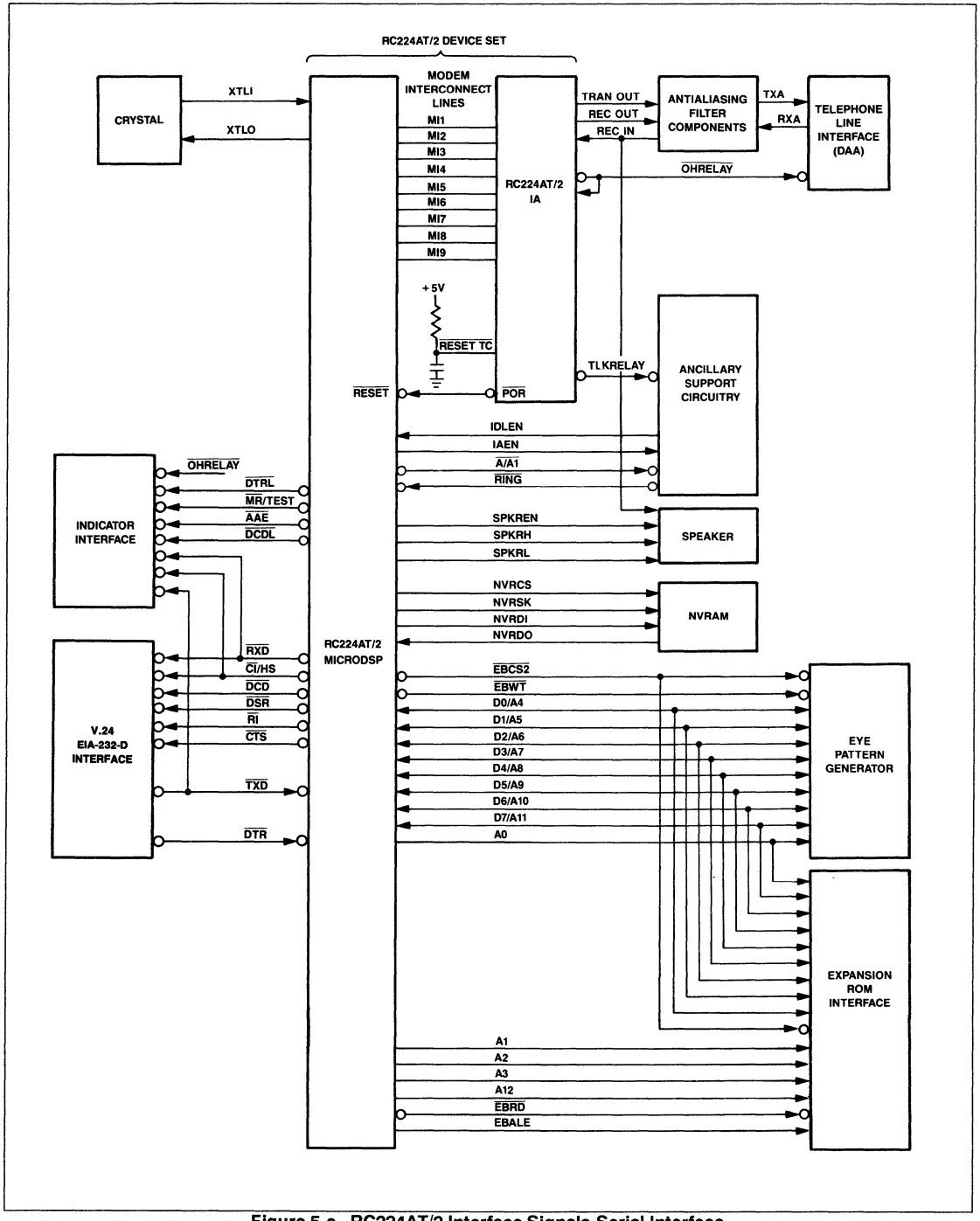


Figure 5-a. RC224AT/2 Interface Signals-Serial Interface

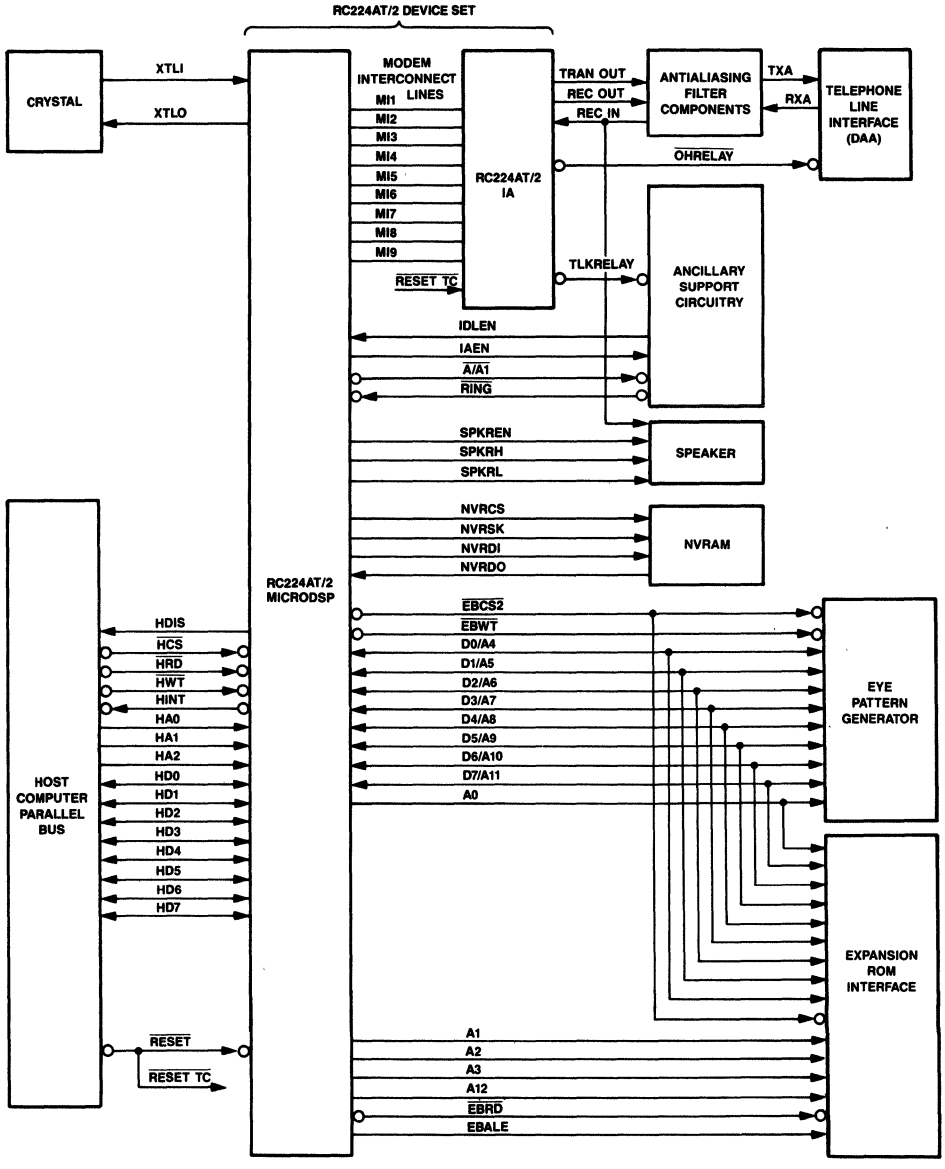


Figure 5-b. RC224AT/2 Interface Signals-Parallel Interface

Table 6. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				Vdc	
Type A		2.0	–	V_{CC}		
Type B		2.4	–	V_{CC}		
Input Low Voltage	V_{IL}				Vdc	
Types A & B		–0.3	–	0.8		
Input Leakage Current	I_{IN}				µAdc	
Type A (Non-multiplexed)		–	–	±10		V_{IN} = 0 to V_{CC}
Output High Voltage	V_{OH}				Vdc	
Type A		2.4	–	–		I_{LOAD} = – 100 µA
Type D		–	–	V_{CC}		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				Vdc	
Type A		–	–	0.4		I_{LOAD} = 1.6 mA
Type D		–	0.75	–		I_{LOAD} = 15 mA
Three-State (Off)	I_{TS}				µAl	
Type A Output		–	–	±25		V_{IN} = 0.8 V to 4.5 V
Power Dissipation	P_D					
DSP Operating		–	125	180	mW	
DSP Power Down		–	22	30	mW	
IA Operating		–	180	350	mW	
IA Power Down		–	15	20	mW	

Note:
1. Test Conditions: T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, (unless otherwise stated).

Table 7. Analog Interface Characteristics

Name	Type	Characteristic
REC OUT	DA	1458 type op amp output
REC IN	DB	1458 type op amp input
TRAN OUT	DD	1458 type op amp output
RXA	DE	Input impedance: 68.1 KΩ ± 1%
TXA	DF	1458 type op amp output

Table 8. RC224AT Hardware Signal Definitions

Label	I/O Type	Signal Name/Description
		OVERHEAD SIGNALS
XTLI	IE	**Crystal/Clock In.** The RC224AT DSP must be connected to an external crystal circuit consisting of a 12.000393 MHz crystal and a suitable capacitance network. Alternatively, XTLI may be driven with a buffered clock.
XTLO	OB	**Crystal Out.** Crystal return (crystal input on XTLI) or not connected (clock input on XTLI).
$\overline{\text{RESET}}$	IB	**Reset.** The active low $\overline{\text{RESET}}$ input resets the internal DSP and IA logic (RC224AT/1) or the DSP logic (RC224AT/2). Upon a transition of $\overline{\text{RESET}}$ from high to low, the AT command set returns to the original factory default values and "stored values" in NVRAM. During DSP power turn-on, $\overline{\text{RESET}}$ must be held low for at least 2 milliseconds after V_{CC} operating voltage is attained for the internal DSP clock oscillator to stabilize.
		Serial Interface (RC224AT/1). The $\overline{\text{RESET}}$ input can be connected to an external RC network to cause the DSP to reset upon power turn on.
		Serial Interface (RC224AT/2). The DSP $\overline{\text{RESET}}$ input may be connected to the IA $\overline{\text{POR}}$ output whereby DSP power-on reset is initiated by the IA via a $\overline{\text{POR}}$ output pulse. With this connection, the IA $\overline{\text{POR}}$ output will also initiate a DSP reset if the IA detects a low power condition.
		Alternatively, DSP $\overline{\text{RESET}}$ may be connected to an external RC circuit to provide power turn-on reset.
		Parallel Interface. The $\overline{\text{RESET}}$ input should be connected to the host bus reset line.
$\overline{\text{POR}}$	IA	**IA Power-On-Reset (RC224AT/2 only).** The IA $\overline{\text{POR}}$ output can be used to initiate an external reset of the DSP when a low power condition is detected within the IA device. The IA device power-on reset circuit monitors the IA +5V supply and outputs a 100 ms to 300 ms low pulse on $\overline{\text{POR}}$ upon IA +5V turn-on. This pulse is generated regardless of the IA –5V supply level. A 10 ms minimum low pulse on $\overline{\text{POR}}$ is also generated when the IA +5V supply drops below 3.5V.
		When DSP $\overline{\text{RESET}}$ and IA $\overline{\text{POR}}$ are tied together, the IA devices pulses $\overline{\text{POR}}$ low upon IA power turn-on to begin the $\overline{\text{POR}}$ sequence. The modem is ready to use 350 ms after the low-to-high transition of $\overline{\text{POR}}$. The $\overline{\text{POR}}$ sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms. $\overline{\text{POR}}$ may also be "wired-or" to an external open collector/drain output.
		NOTE: If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a $\overline{\text{POR}}$ sequence (i.e., <+3.5V), the host system should initiate a reset signal upon supply voltage recovery to ensure proper modem initialization and operation.
		Serial Interface. The $\overline{\text{POR}}$ pin may be connected to the DSP $\overline{\text{RESET}}$ input to provide an output to reset the DSP device.
		Parallel Interface. The $\overline{\text{POR}}$ pin should be left open.
$\overline{\text{RESET TC}}$	IA	**IA Reset Time Constant (RC224AT/2 only).**
		Serial Interface. The $\overline{\text{RESET TC}}$ input must be connected to an external RC circuit with a long time constant if the $\overline{\text{POR}}$ pin is used to reset the DSP device. If $\overline{\text{POR}}$ is unconnected, $\overline{\text{RESET TC}}$ may be connected to DSP $\overline{\text{RESET}}$ or pulled high with a resistor to +5V.
		Parallel Interface. The $\overline{\text{RESET TC}}$ input should be connected to the host bus reset line.
+ 5V		**+ 5V Supply.** +5V ±5% is required by both the DSP and the IA functions.
–5V		**–5V Supply.** –5V ±5% is required by the IA function.
DGND		**Digital Ground.**
AGND		**Analog Ground.**

Table 8. RC224AT Hardware Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		DSP DEVICE/ANCILLIARY SUPPORT
IDLEN	IA	**Idle Enable.** When IDLEN input is high, the modem enters the sleep (power down) mode after 30 to 60 seconds of inactivity. IDLEN low disables entry into the sleep mode.
IAEN	OA	**IA Enable.** IAEN output high indicates the DSP is operating in its normal mode. IAEN low indicates that the DSP is in the sleep (power down) mode. This signal can be used to turn off the 72 μA bias current to the IA in order to reduce analog power consumption during the sleep mode. IAEN can also be used to control power to other devices (e.g., as a speaker enable when used with the RC224AT/1).
$\overline{\text{RING}}$	IA	**Ring Frequency.** A low going edge on the $\overline{\text{RING}}$ input alerts the modem and removes it from the sleep mode. Either a half-wave or a full-wave ring detector can be used with this input.
$\overline{\text{A/A1}}$	OA	**Key Telephone Hold Indicator.** $\overline{\text{A/A1}}$ output low indicates that the telephone line is in use when used on multi-line key telephones. Although TTL compatible, this output can be used to sink up to 5 mA with $V_{OL} \leq 0.65$ V, making it suitable for opto relay control without the need to provide buffering.
		IA/LINE INTERFACE/ANCILLIARY SUPPORT
TLKRELAY	OD	**Talk/Data Relay Driver. RC224AT/1:** TLKRELAY is a TTL compatible output (I_{OL} = 1.6 mA, V_{OL} = 0.4V). This output can, however, sink up to 5 mA with $V_{OL} \leq 0.65$ V, making it suitable for opto relay control without the need to provide buffering. **RC224AT/2:** TLKRELAY is an open drain type output that can control a normally closed relay with a resistance of greater than 360 ohms. This output is suitable for both mechanical and optical/solid state relays. Quenching diodes are built-in to the output, hence there is no need to apply them externally when driving a mechanical relay. This output may be used to disconnect the handset from the telephone line during a data connection.
$\overline{\text{OHRELAY}}$	OD	**Off-Hook Relay Driver.** $\overline{\text{OHRELAY}}$ is an open drain type output that can control a normally open relay with greater than 360 ohms resistance. This output also has built-in quenching diode protection making it suitable for both mechanical and optical/solid state relays. This output is used to connect the modem to the telephone line.
		IA/EXTERNAL FILTER COMPONENTS
REC IN	I (DB)	**IA Receiver OP Amp Input.** REC IN is the IA input from the RXA input filter circuit (see Figures 6 and 7).
REC OUT	O(DA)	**IA Receiver OP Amp Output.** REC OUT is the IA output to the RXA input filter circuit (see Figures 6 and 7).
TRAN OUT	O (DD)	**IA Transmitter OP Amp Output.** TRAN OUT is the IA output to the TXA output filter circuit.
		EXTERNAL FILTER COMPONENTS/LINE INTERFACE
RXA	I (DE)	**Receive Analog.** RXA is an input to the external filter components from a data access arrangement (see Figures 6 and 7). The input impedance at RXA is determined by R6. R6 is selected such that the power at REC OUT is 0 dBm when the maximum signal is applied to RXA.
TXA	O (DF)	**Transmit Analog.** The TXA output can drive a data access arrangement (see Figures 6 and 7) for connection to the public switched telephone network (PSTN). The transmitter output impedance is that of a 1458 type operational amplifier output. The output level is determined by R8.
		NVRAM INTERFACE
NVRCS	OA	**NVRAM Chip Select.** NVRCS output HIGH enables the NVRAM.
NVRSK	OA	**NVRAM Shift Clock.** The NVRSK output is used to shift data to or from the NVRAM.
NVRDIO	IA/OA	**NVRAM Data In/NVRAM Data Out (RC224AT/1 only).** NVRDIO carries both the serial input data from the NVRAM and the serial output to the NVRAM. Depending on the specific NVRAM used, a

Table 8. RC224AT Hardware Signal Definition (Cont'd)

Label	I/O Type	Signal Name/Description
NVRDI	OA	**NVRAM Data In (RC224AT/2 only).** The NVRDI output supplies serial data to the NVRAM DI serial data input pin.
NVRDO	IA	**NVRAM Data Out (RC224AT/2 only).** The NVRDO input accepts serial data from the NVRAM DO serial data output pin.
		SPEAKER INTERFACE
SPKREN	OA	**Speaker Enable (RC224AT/2 Only).** SPKREN output can be used to control power to a speaker driver. SPKREN high turns the speaker on.
$\overline{\text{SPKRH}}$/SPKRH	OA	**Speaker High.** Active low (RC224AT/1) or active high (RC224AT/2) output signal that can be used with $\overline{\text{SPKRL}}$/SPKRL to control the speaker volume.
$\overline{\text{SPKRL}}$/SPKRL	OA	**Speaker Low.** Active low (RC224AT/1) or active high (RC224AT/2) output signal that can be used with $\overline{\text{SPKRH}}$/SPKRH to control the speaker volume. When the AT command set is used for volume control, $\overline{\text{SPKRH}}$/SPKRH and $\overline{\text{SPKRL}}$/SPKRL react as follows:

		RC224AT/1		RC224AT/2	
Volume	AT Command	$\overline{\text{SPKRH}}$	$\overline{\text{SPKRL}}$	$\overline{\text{SPKRH}}$	$\overline{\text{SPKRL}}$
Off	M0	H	H	L	L
Low	L0, L1	H	L	L	H
Medium	L2	L	H	H	L
High	L3	L	L	H	H

		ASYNCHRONOUS SERIAL HOST INTERFACE (SERIAL INTERFACE ONLY)
$\overline{\text{SEREN}}$	IA	**Serial Interface Enable.** When the $\overline{\text{SEREN}}$ input is connected to ground, the serial interface is selected upon power turn-on. The serial interface signals can be connected to the V.24/RS-232-C and indicator interfaces as shown in Figures 3-a and 5-a.
$\overline{\text{RXD}}$	OA	**Received Data.** The modem presents received serial data to the host on the $\overline{\text{RXD}}$ output.
$\overline{\text{TXD}}$	IA	**Transmitted Data.** The modem obtains serial data to be transmitted from the host on the $\overline{\text{TXD}}$ input.
DCD	OA	**Data Carrier Detected.** $\overline{\text{DCD}}$ is controlled by the AT&C command. The data detect threshold is –43 dBm. The turn-off level is ≤ –48 dBm.
$\overline{\text{DSR}}$	OA	**Data Set Ready.** $\overline{\text{DSR}}$ output is controlled by the AT&Sn command. DSR OFF (high) indicates that the host is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{\text{RI}}$).
$\overline{\text{RI}}$	OA	**Ring Indicator.** $\overline{\text{RI}}$ output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The OFF (high) condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received. $\overline{\text{RI}}$ will respond to a $\overline{\text{RING}}$ input signal with frequencies greater than 15.3 Hz, making the modem device compatible with both have-wave and full-wave detectors.
$\overline{\text{CTS}}$	OA	**Clear To Send.** In asynchronous mode, $\overline{\text{CTS}}$ output is controlled by the AT&Q0 command (always ON). In synchronous mode, $\overline{\text{CTS}}$ ON indicates that the modem will transmit any data present on TXD.
$\overline{\text{DTR}}$	OA	**Data Terminal Ready.** DTR input on (low) indicates that the DTE is ready to operate. DTR input OFF (high) indicates that the DTE is not ready to operate.
$\overline{\text{DTRL}}$	OA	**DTR Indicator.** $\overline{\text{DTRL}}$ output is controlled by the AT&Dn command.
$\overline{\text{CI}}$/HS	OA	**Calling Indicator/High Speed Indicator.** $\overline{\text{CI}}$/HS output low indicates modem connection at 2400 bps.

Table 8. RC224AT Hardware Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
DCDL	OA	**DCD Indicator.** DCDL output is controlled by the AT&Cn command.
MR/TEST	OA	**Modem Ready/Test.** MR/TEST output low indicates that the modem is ready, i.e., modem power is on and a test mode is not selected. In a test mode, the MR/TEST output pulses to flash the Modem Ready/Test indicator.
		PARALLEL HOST INTERFACE (PARALLEL INTERFACE ONLY) When the HWT input signal is connected to the host bus write line, the parallel interface is selected upon power turn-on. The parallel interface emulates a 16C450 UART interface. The parallel interface is compatible with communications software designed to operate with a 16C450 interface on an IBM PC. Table 9 identifies the parallel interface registers. Parallel interface operation is equivalent to 16C450 operation with CS0 and CS1 inputs high and DISTR, DOSTR, and ADS inputs low. The corresponding RC224AT and 16C450 signals are shown below. 16C450 signals not required for RC224AT host computer operation are not shown. **16C450 Signal** — **RC224AT Signal** A0 - A2 — HA0 - HA2 D0 - D7 — HD0 - HD7 MR — RESET (Active low) CS2 — HCS DISTR — HWT DOSTR — HRD INTRPT — HINT DDIS — HDIS OUT1 — None (Implemented internally in RC224AT) OUT2 — None (Implemented internally in RC224AT)
HA0-HA2	IA	**Host Bus Address Lines 0-2.** During a host read or write operation, HA0-HA2 select an internal DSP 16C450-compatible register. The state of the divisor latch access bit (DLAB) affects the selection of certain DSP registers. DLAB must be set high to access the baud generator divisor latches.
HD0-HD7	IA/OA	**Host Bus Data Lines 0-7.** HD0-HD7 are comprised of eight tri-state input/output lines providing bidirectional communication between the host and the DSP. Data, control words, and status information are transferred through HD0-HD7.
HCS	IA	**Host Bus Chip Select.** HCS input low selects the host bus.
HRD	IA	**Host Bus Read.** HRD is an active low, 8086-compatible read control input. When the DSP is selected, HRD low allows the host to read status information or data from a selected DSP register.
HWT	IA	**Host Bus Write.** HWT is an active low, 8086-compatible write control input. When the DSP is selected, HWT low allows the host to write data or control words into a selected DSP register.
HDIS	OA	**Host Bus Driver.** HDIS output is low when the host is reading data from the DSP over the host data bus (both HRD and HCS are low). HDIS is also used to disable the external transceiver drivers whenever the host is not reading data from the DSP.
HINT	OA	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt has an active high condition. HINT is reset low upon the appropriate interrupt service or master reset operation.

Table 8. RC224AT Hardware Signal Definition (Cont'd)

Label	I/O Type	Signal Name/Description
		EXPANSION BUS INTERFACE (RC224AT/2 only)
$\overline{AAE}$	OA	**Auto Answer Enable.** $\overline{AAE}$ output low indicates that modem auto answer mode has been enabled with the S0 = command. AAE high indicates auto answer has been disabled.
A0-A3, A12	OA	**Address Lines 0-3 and 12.** A0-A3 and A12 are the expansion bus dedicated address lines.
D0-D7/A4-A11	IA/OA	**Data Lines 0-7/Address Lines 4-11.** D0-D7/A4-A11 are the expansion bus multiplexed data/address lines.
EBALE	OA	**Expansion Bus Address Latch Enable.** A negative transition on EBALE output latches the address on the multiplexed address/data bus.
$\overline{EBCS1}$	OA	**Expansion Bus Chip Select 1.** When $\overline{EBCS1}$ is low, an address in the $4000-$BFFF address range (32k bytes) is selected.
$\overline{EBCS2}$	OA	**Expansion Bus Chip Select 2.** When $\overline{EBCS2}$ is low, an address in the $2000-$3FFF address range (8k bytes) is selected.
$\overline{EBRD}$	OA	**Expansion Bus Read Enable.** When $\overline{EBRD}$ is low, data is transferred to the DSP from data lines D0-D7.
$\overline{EBWT}$	OA	**Expansion Bus Write Enable.** When $\overline{EBWT}$ is low, data is output from the DSP to data lines D0-D7.

Table 9. RC224AT Parallel Interface Registers

Register Number	Register Name	Bit 7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	0	Transmitter Empty (TEMT)	Transmitter Holding Register (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Loop	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	Interrupt Identify Register (IIR) (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" if Interrupt Pending
1 DLAB = 0	Interrupt Enable Register (IER)	0	0	0	0	Enable MODEM Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 DLAB = 0	Transmitter Holding Register (THR)	Transmitter Holding Register (Write Only)							
0 DLAB = 0	Receiver Buffer Register (RBR)	Receiver Buffer Register (Ready Only)							
1 DLAB = 1	Divisor Latch (MSB) Register (DLM)	Divisor Latch (MS)							
0 DLAB = 1	Divisor Latch (LSB) Register (DLL)	Divisor Latch (LS)							

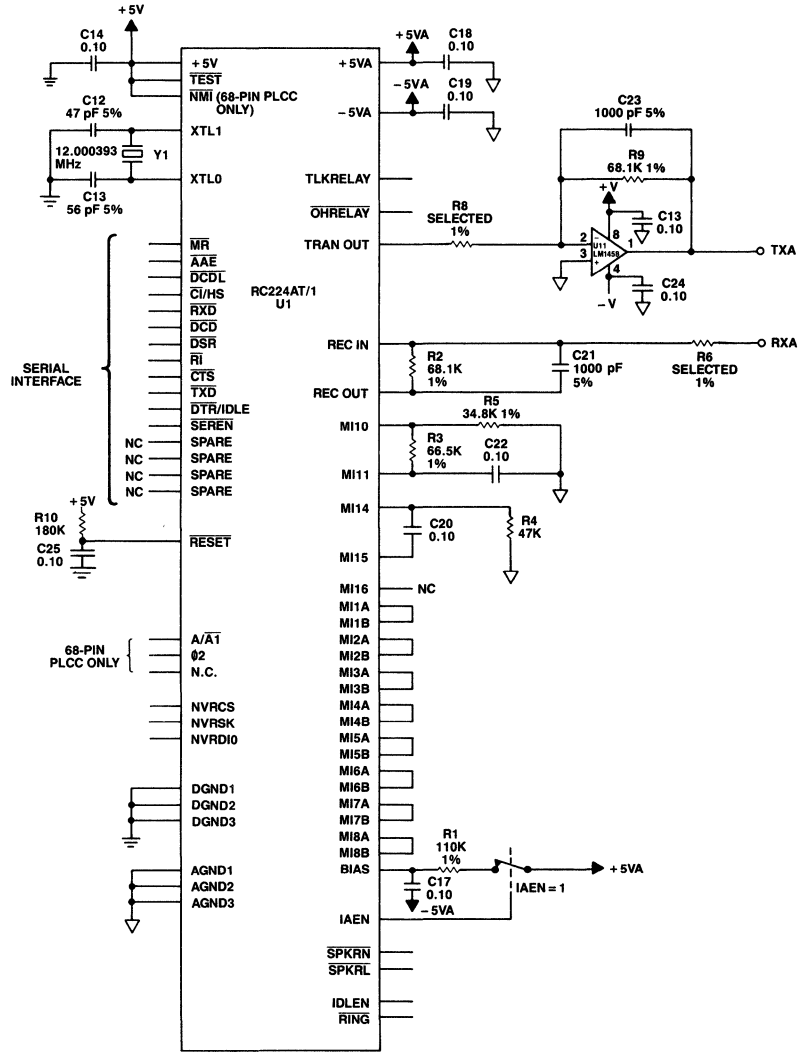


Figure 6-a. Recommended RC224AT/1 Circuit - Serial

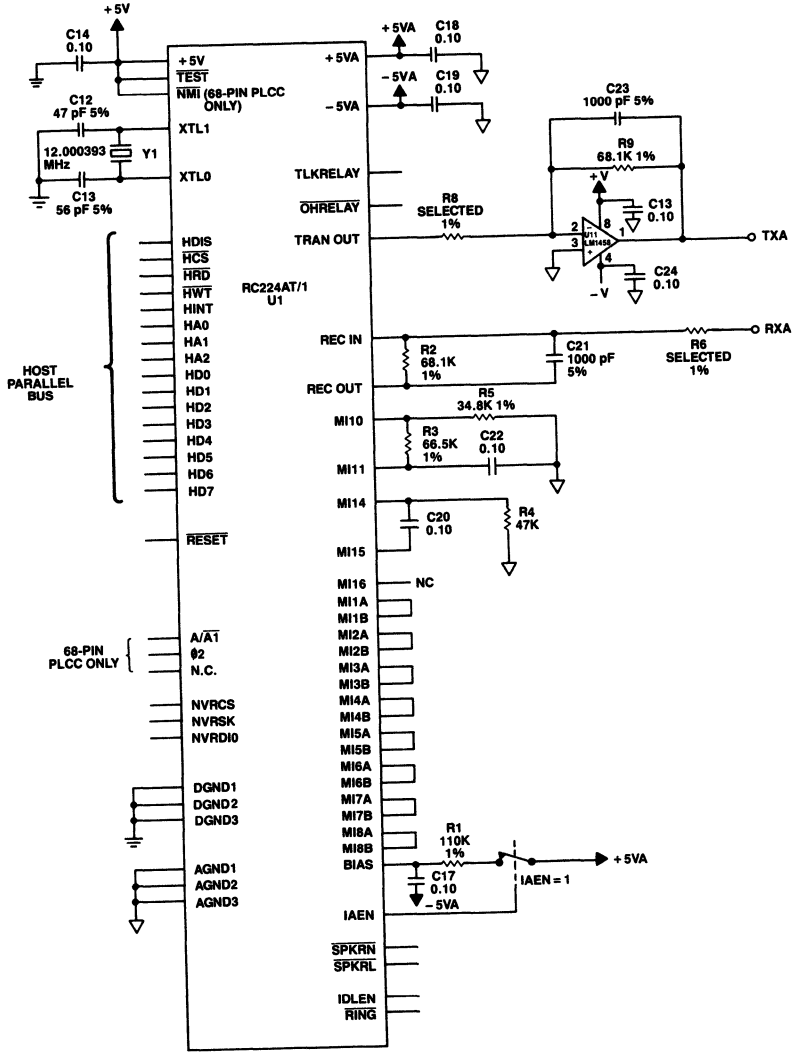


Figure 6-b. Recommended RC224AT/1 Circuit - Parallel

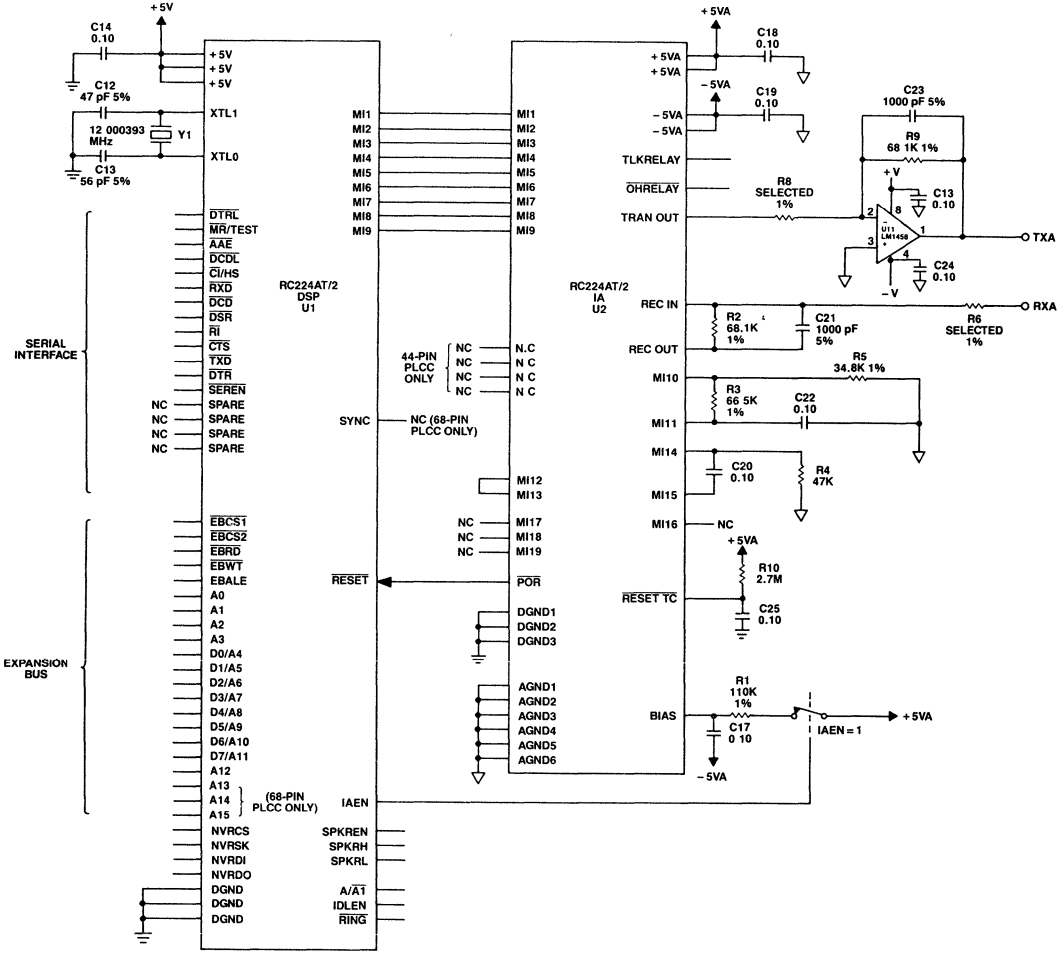


Figure 7-a. Recommended RC224AT/2 Circuit - Serial

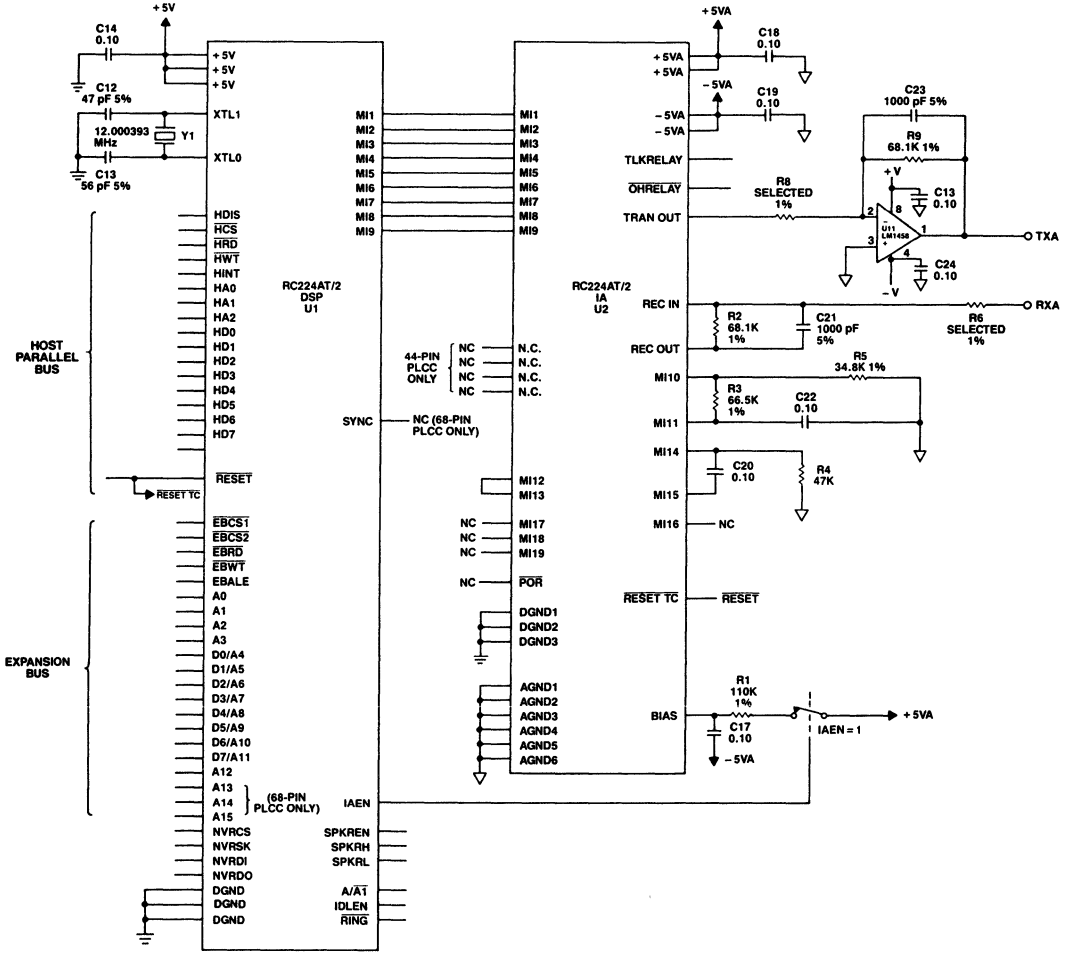


Figure 7-b. Recommended RC224AT/2 Circuit - Parallel

GENERAL SPECIFICATIONS

Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Maximum) @ 0°C
Operating			
+ 5 VDC	±5%	44 mA	71 mA
–5 VDC	±5%	17 mA	35 mA
Sleep (Power Down)			
+5VDC	±5%	5.9 mA	8.0 mA
–5 VDC	±5%	1.5 mA	2.0 mA

Note: Input voltage ripple ≤ 0.1 volts peak-to-peak.

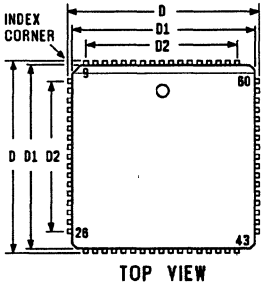
Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0° C to + 60° C (32° F to 140° F)
Storage	– 40° C to + 80° C (–40° F to 176° F) (Stored in heat sealed antistatic bag and shipping container).
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35° C, whichever is less.
Altitude	– 200 feet to + 10,000 feet

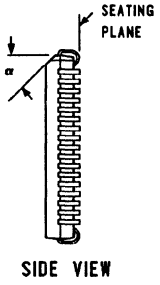
Typical Crystal Specifications

Parameter	Value
Operating Temperature	0°C to 50°C
Storage Temperature	–55°C to 85°C
Nominal Frequency @ 25°C	12.000393 MHz
Frequency Tolerance @ 25°C	±0.0020% (±20 PPM)
Temperature Stability @ T_A = 0°C to 50°C	±0.0030% (±10 PPM)
Calibration Mode	Parallel resonant
Shunt Capacitance	7 pF max.
Load Capacitance	32 ±0.3 pF
Drive Level	2.5 mW max.
Aging, per Year Max.	0.0005% (± 5 PPM)
Oscillation Mode	Fundamental
Series Resistance	60 ohms max., tested at 20 nW
Max. Frequency Variation with 28.8 or 35.2 pF Load Capacitance	±0.0020% (±20 PPM)
Third Lead and Sleeving	Required

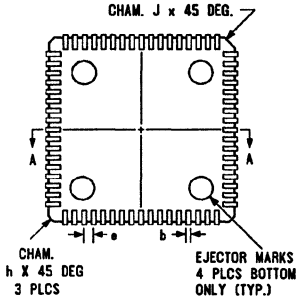
PACKAGE DIMENSIONS



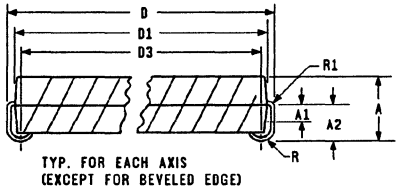
TOP VIEW



SIDE VIEW



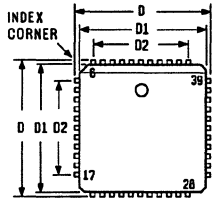
BOTTOM VIEW



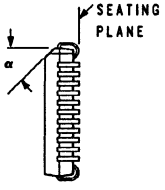
SECTION A-A

DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23.50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	

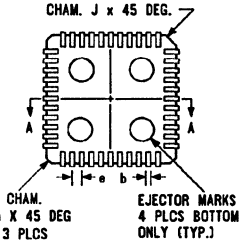
68-Pin PLCC



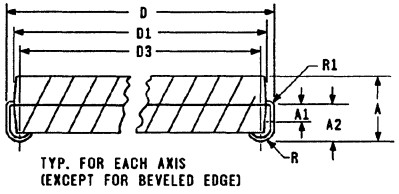
TOP VIEW



SIDE VIEW



BOTTOM VIEW

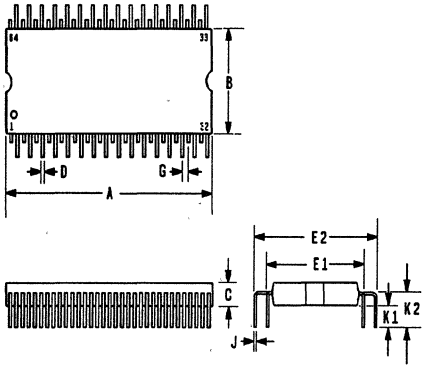


SECTION A-A

DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	

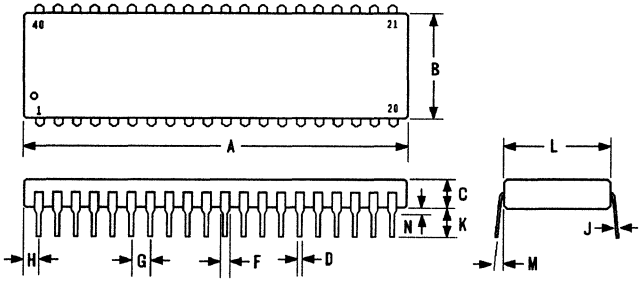
44-Pin PLCC

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	41.10	41.61	1.618	1.638
B	17.02	17.23	0.670	0.690
C	3.56	4.58	0.140	0.180
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	2.92	3.18	0.115	0.125
K2	4.83	5.34	0.190	0.210

64-Pin Plastic QUIP



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

40-Pin Plastic DIP

RC224EB 2400 bps Modem Device Set Evaluation Board

INTRODUCTION

The RC224EB Evaluation Module is a 2400 bps full-duplex modem on a PC half-card. The RC224EB is compatible with IBM PC, PC/XT, and PC/AT personal computers.

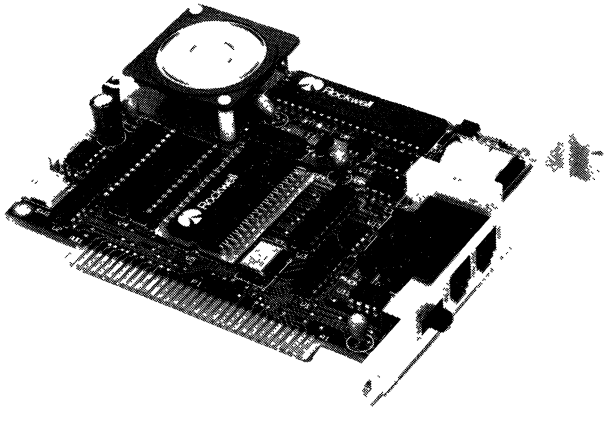
Incorporating the Rockwell RC224AT 2400 bps full-duplex modem device set, the RC224EB complies with CCITT V.22 bis and V.22 A/B, and meets Bell 212A and 103 interfaces. The RC224EB also implements a Hayes-2400B-compatible "AT" command set.

The RC224EB contains circuitry that demonstrates the complete performance and interface capability of the RC224AT device set. In addition to the 2-device modem set, the evaluation board contains a digital access arrangement (DAA), speaker circuitry and attached speaker, eye pattern generation circuitry, an 8k-byte PROM socket, and a 1024-bit non-volatile RAM (NVRAM).

The full capabilities of the RC224AT device set are described in the RC224AT Data Sheet (Order No. MD54).

FEATURES

- Modem Compatibilities
  - CCITT V.22 bis and V.22 A/B
  - Bell 212A and 103
- Modem Components
  - 2-device RC224AT device set
  - On-board DAA
  - Speaker circuit and speaker
  - 8k-byte PROM Socket
  - 1024-bit NVRAM
  - Eye Pattern Generator circuit
- PC Hardware Interface
  - PC half-card size
  - IBM PC bus interface
  - 16C450 compatible
- Line/Telephone/Diagnostic Interface
  - 6-pin line interface modular jack
  - 6-pin telephone interface modular jack
  - Eye pattern oscilloscope test points
- Switches
  - COM1/COM2 switch (SW1)
  - Sleep Enable/Disable switch (SW2)
- Software Interface
  - IBM PC Async
  - Hayes Smartcom II, Version 2.1
  - Hayes 2400B and 2400 AT command set



RC224EB Modem Evaluation Board

GENERAL DESCRIPTION

The RC224AT modem device set consists of the major building blocks shown in Figure 1. A board layout of the RC224EB module is shown in Figure 2. Tables 1 through 7 show the interface signals and switch positions.

The Data Access Arrangement (DAA) contained on this evaluation board is considered suitable for use on U.S. public switch telephone lines, although it has not yet been certified by FCC.

SUPPORTED INTERFACES

Speaker Interface

Speaker driver circuitry and a speaker mounted on the board is provided. The speaker can be used to monitor call progress. The AT command set can be used to adjust the speaker volume.

NVRAM Interface

A 1024-bit NVRAM is provided. The NVRAM can accommodate a user-selectible AT command set configuration which can take precedence over the factory default setting.

Expansion ROM Interface

A socket for an 8k-byte PROM is included. The PROM can be used to expand the AT command set. (Refer to Application Note Order No. 830 for detail usage instructions.)

Eye Pattern Generator Interface

Eye pattern generation circuitry is provided. The eye pattern generator (EPG) circuit can be used for diagnostic purposes.

Sleep (Power Down) Mode Circuit

The RC224EB includes power down circuitry which may be used to enable or disable sleep mode. If enabled, the RC224AT enters sleep mode whenever the modem has been inactive for more than one minute. (Note that the modem never enters sleep mode while it is in data mode. During sleep mode, power is turned off to the Integrated analog device, speaker and the MicroDsp™ (except the crystal circuit). The modem returns to full operation whenever a ring signal occurs or the host writes to the modem.

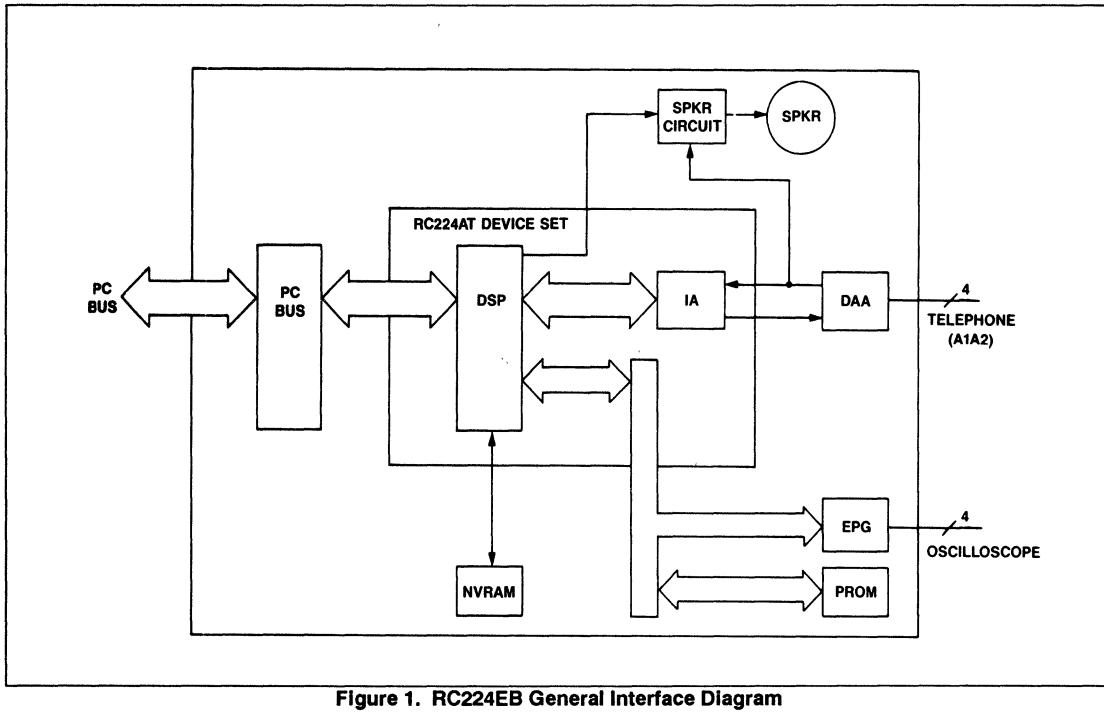


Figure 1. RC224EB General Interface Diagram

Table 1. PC Connector P1 Pin Signals

Pin	Signal	Pin	Signal
A2	HD7	A22	A9
A3	HD6	A23	A8
A4	HD5	A24	A7
A5	HD4	A25	A6
A6	HD3	A26	A5
A7	HD2	A27	A4
A8	HD1	A28	A3
A9	HD0	A29	HA2
A11	AEN	A30	HA1
		A31	HA0

Table 2. PC Connector P2 Signals

Pin	Signal	Pin	Signal
B1	GND	B13	HWTP
B2	RESET	B14	HRDP
B3	+5 V	B24	IRQ4
B5	-5 V	B25	IRQ3
B9	+12 V	B29	+5 V
B10	GND	B31	GND

Table 3. Telephone Line Connector J1 Signals

Pin	Signal
3	Ring (R)
4	Tip (T)

Table 4. Line Interface Connector J2 Signals

Pin	Signal
1	N.C.
2	A1
3	Tip (T)
4	Ring (R)
5	A
6	N. C .

Table 5. Eye Pattern Test Point Signals

Point	Signal
TP1	EYEY
TP2	EYEY Return (GND)
TP3	EYEX
TP4	EYEX Return (GND)

Table 6. Switch 1 (SW1) - COM1/COM2

Point	Signal
ON (Up)	COM1
OFF (Down)	COM2

Table 7. Switch 2 (SW2) - Sleep Enable/Disable

Position	Selection
ON (Toward Switch 1)	Sleep Enable
OFF (From Switch 1)	Sleep Disable

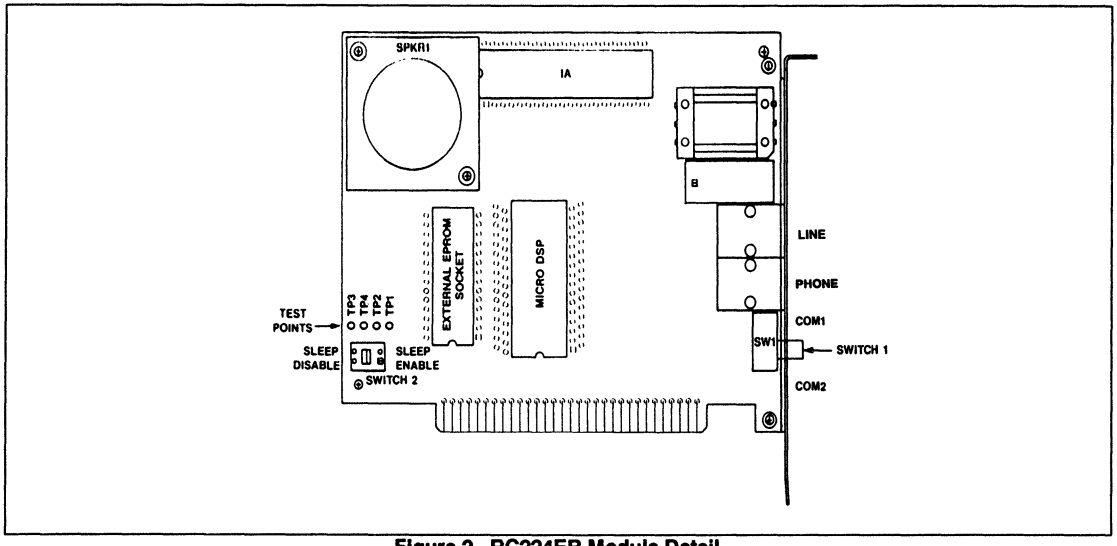


Figure 2. RC224EB Module Detail

HARDWARE INSTALLATION PROCEDURE

1. Turn-off the computer system.
2. Remove the computer cover in accordance with your computer's expansion card installation procedures.
3. Select either COM1 or COM2 using SW1 (Table 6).
4. Select either Sleep Enable or Sleep Disable using SW2 (Table 7).
5. Select an available full- or half-card expansion slot to install the modem module. Some computers assign specific slots to specific functions. (Refer to the your computer's expansion card installation guidelines.)
6. Remove the blank card panel corresponding to the selected expansion slot. Save the screw for attaching the modem module.
7. Install the modem module into the selected expansion slot and secure it with the screw.
8. Connect the cable from the wall telephone jack to the LINE plug (upper connector) on the modem module rear panel.
9. Connect the cable from the telephone to the PHONE plug (lower connector) on the modem module rear panel.
10. Replace the computer cover.
11. Restore power to the computer system.

SOFTWARE INSTALLATION PROCEDURE

Install the communications software (e. g., CROSSTALK XVI or Smartcom II) in accordance with the communication software's installation procedure.

OPERATION

AT COMMAND SET

The AT command set is Hayes 2400B compatible. The commands are divided into three types; basic commands, dial modifiers, and ampersand commands. These commands are summarized in Table 8.

AUTOMATIC OPERATION

Operate the modem automatically using the communication software's high level instructions in accordance with the communication software's operating procedure.

(Note: To use communication software that doesn't have a 2400 bps setup configuration type the following commands in manual terminal mode: ATZ, AT&F [Optional], AT&C1, AT&D2, ATS25 = 0, ATV0, and AT&W).

Table 8. RC224AP "AT" Command Set Summary

Basic Commands	Function
AT	Attention Code
A	Answer Command
A/	Repeat Last Command
Bn	Communications Standard Option
C1	Carrier Control Option
D	Dial Command
En	Off-line Character Echo Option
F1	On-line Character Echo Option
Hn	Switch Hook Control Option
In	Identification/Checksum Option
Ln	Speaker Volume Option
Mn	Speaker Control Option
On	On-line Command
P	Pulse Dial
Qn	Result Code Display Option
Sn	Select an S Register
Sn=	Write to an S Register
Sn?	Read an S Register
T	Touch Tone Dial
Vn	Result Code Form Option
Xn	Result Code Set/Call Progress Option
Yn	Long Space Disconnect Option
Zn	Recall Stored Profile Command
+++	Escape Code Sequence
	Pause
Dial Modifiers	**Function**
P	Pulse Dial
R	Originate Call in Answer Mode
S=n	Dial Stored Number
T	Touch Tone Dial
W	Wait for Dial Tone
;	Return to Idle State
@	Wait for Quiet Answer Command
!	Flash Hook
,	Pause
0-9 A,B,C,D #,*	Dial Digits/Characters
Ampersand Commands	**Function**
&Cn	Data Carrier Detect Option
&Dn	Data Terminal Ready Option
&F	Load Factory Defaults
&Gn	Guard Tone Option
&Jn	Auxiliary Relay Control
&Mn	Communications Mode Option
&Pn	Make to Break Ratio Selection
&Qn	Communications Mode Option
&Sn	Data Set Ready Option
&Tn	Test Command Selection
&V	View Active Configuration and User Profiles
&Wn	Store Active Profile
&Xn	Synchronous Transmit Clock Source Option
&Yn	Select Stored Profile on Powerup Option
&Zn=x	Store Telephone Number

MANUAL OPERATION

Operate the modem manually by issuing "AT" commands from the communication software direct access mode.

Enter an "AT" command by typing the command characters. Use the backspace key to correct a typing mistake.

Execute the command by pressing the ENTER (or RETURN) key. Two commands, A/ and +++ , execute immediately upon character entry, thus, do not require pressing of the ENTER key.

Refer to the OPERATION section of the RC224AT Data Sheet (Order No. MD54) for a detail description of the "AT" commands.

NVRAM COMMANDS

The following "AT" commands can be used to store and to recall a telephone number and a subset of the S registers from the NVRAM:

Command	Function
DS=n	Dials a stored telephone number.
Zn	Resets the modem and recalls a user profile from the NVRAM.
&F	Loads the factory default configuration.
&V	Displays the active configuration and user profiles.
&Wn	Saves storage parameters of active configuration as a user profile into the NVRAM.
&Zn	Stores a telephone number into the NVRAM.

Example

AT&Z0=767-2676 <CR> Stores 767-2676 into the NVRAM.

ATDS=1 Dials the telephone number stored in the NVRAM.

SPEAKER COMMANDS

The following "AT" commands can be used to control the speaker:

Command	Function
Mn	Controls the speaker operation.
Ln	Adjusts the speaker volume.

EYE PATTERN

DEFINITION

The eye pattern is an oscilloscope display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

In quadrature amplitude modulation (QAM), two multilevel amplitude modulated (AM) carriers are transmitted simultaneously. Interference between these two modulated carriers is minimized by using carriers of identical frequency with a constant 90° relative phase angle. After demodulation, the multilevel baseband signals can be displayed on an oscilloscope with the set of levels received on one carrier displayed on the X axis and the set of levels received on the other carrier displayed on the Y axis. Since these signals consist of discrete levels sent at high data rates, the resulting oscilloscope pattern appears to be a fixed set of points.

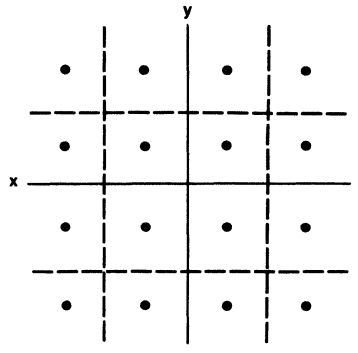
Figure 3 illustrates the RC224AT ideal eye patterns for 2400 bps and 1200 bps.

EXAMPLES

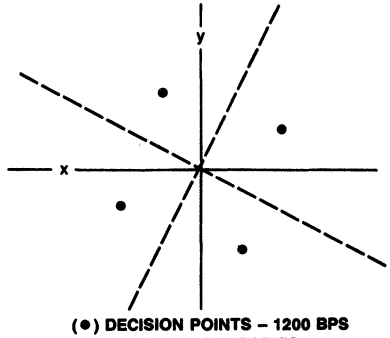
Figures 4a through 4d illustrate four examples of an eye pattern for V.22A/B with and without impairments. Figure 4a shows the location of four ideal points. The X and Y axes represent decision boundaries used by the receiver in deciding which ideal point corresponds to the actual received point. Although the transmitter sends ideal points, line impairments cause the received points to be misaligned.

Figure 4b shows the effect of random noise. The received points cluster around the ideal location, but are randomly offset from the ideal point by the noise causing undesired signal modulation. The random offsets are a result of the random nature of the noise. If the line impairment is not random but periodic or is a function of the received signal itself (e.g., harmonic distortion) then the distribution of points around the ideal location is not random.

Figure 4c illustrates the tangential smearing resulting from phase jitter and Figure 4d shows the effect of amplitude distortion (either gain jitter or harmonic distortion). The magnitude of the spreading is directly proportional to the severity of the impairment, and represents the quality of the signal or the likelihood of errors in the received data.



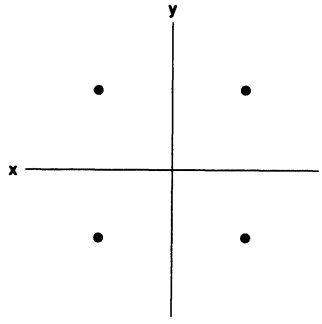
(●) DECISION POINTS – 2400 BPS
(—) DECISION BOUNDARIES (includes x & y axis)



(●) DECISION POINTS – 1200 BPS
(---) DECISION BOUNDARIES

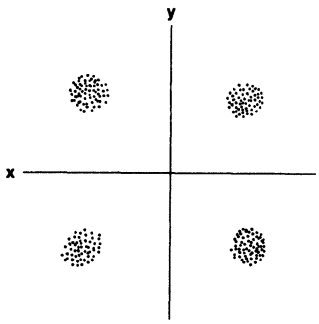
Figure 3. Ideal Eye Patterns

a) IDEAL EYE PATTERN



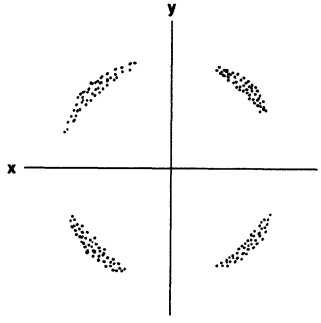
- X AND Y AXIS REPRESENT DECISION BOUNDARIES

b) WHITE NOISE



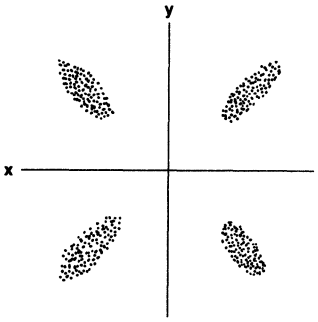
- SMEARING AROUND EACH IDEAL LOCATION

c) PHASE JITTER



- CONTINUOUSLY PERIODIC PHASE SMEARING
- LITTLE OR NO AMPLITUDE SMEARING

d) HARMONIC DISTORTION



- NON-PERIODIC AMPLITUDE SMEARING
- LITTLE PHASE EFFECT
- GAIN-JITTER (AM) EFFECT IS SIMILAR AND IS PERIODIC

*DEGREE OF THE SPREADING OF THE EYE PATTERN IS PROPORTIONAL TO THE SEVERITY OF THE LINE DISTURBANCE

Figure 4. Typical Eye Patterns Showing Noise

GENERAL SPECFICATIONS

Voltage[1]	Current (Normal) @ 25°C	Current (Sleep mode) @ 25°C
+ 5 VDC ±5%	70 mA	9.1 mA
+ 12 VDC ±5%	100 mA[2]	0 A
–5 VDC ±5%	20 mA	1.8 mA

Note:
1. Input voltage ripple ≤0.1 volts peak-to-peak.
2. Only used to power speaker; 0 mA when speaker turned off.

Parameter	Specification
Temperature	
Operating	10°C to + 40°C
Storage	0°C to + 70°C (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	– 200 feet to + 10,000 feet

Parameter	Specification
Board Structure	Single PC board Half Card IBM PC/XT and PC/AT compatible edge connector.
Dimensions	
Width	4.20 in. (106.7)
Length	5.23 in. (132.7 mm)

Rockwell

R1212
1200 bps Full-Duplex Modem

INTRODUCTION

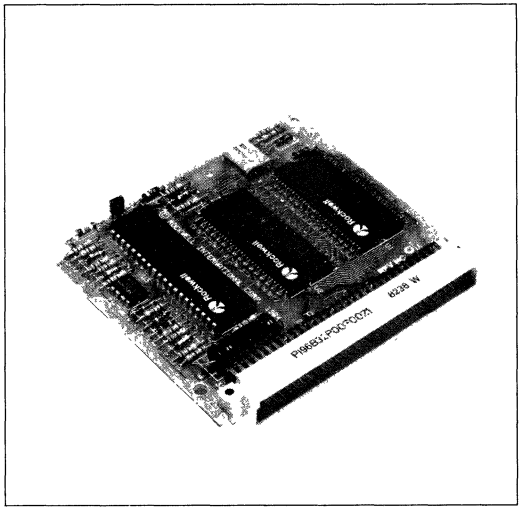
The Rockwell R1212 is a high performance full-duplex 1200 bps modem. Using state-of-the-art VLSI and signal processing technology, the R1212 provides enhanced performance and reliability. The modem is assembled as a small module with a DIN connector (R1212M amd R1212DC).

Being CCITT V.22 A, B compatible, as well as Bell 212A and 103 compatible, the R1212 fits most applications for full-duplex 1200 bps (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network, and over point-to-point leased lines.

The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product that demands the utmost in reliability and performance.

FEATURES

- CCITT V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 1200 bps, 600 bps ±0.01%
- Asynchronous: 1200 bps, 600 bps +1%, −2.5%, 0–300 bps
  - — Character Length 8, 9, 10, or 11 bits
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL Compatible
- 2-wire Full-Duplex Operation
- Adaptive and Fixed Compromise Equalization
- Test Configurations:
  - — Local Analog Loopback
  - — Remote Digital Loopback
  - — Self Test
- Auto/Manual Answer
- Auto/Manual Dial—DTMF Tone or Pulse Dial
- Power Consumption: 2.3 Watts Typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Two Functional Configurations:
  - — R1212DC (Direct Connect): DIN connector module with FCC approved DAA Part 68 Interface
  - — R1212M: DIN connector module without DAA



R1212M Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

The transmitter and signaling frequencies supported in the R1212 are listed in Table 1.

Table 1. Transmitter Carrier and Signaling Frequencies Specifications

Mode	Frequency (Hz ±0.01%)
V.22 low channel, Originate Mode	1200
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

TONE GENERATION

The specifications for tone generation are as follows:

1. **Answer Tones:** The R1212 generates echo disabling tones for both the CCITT and Bell configurations, as follows:
   a. CCITT: 2100 Hz ± 15 Hz.
   b. Bell: 2225 Hz ± 10 Hz.
2. **Guard Tones:** If GTS (see Interface Memory Definitions) is low, an 1800 Hz guard tone frequency is selected; if GTS is high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone is 6 ± 1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power is 3 ± 1 dB below the level of the main channel power, and again the overall power transmitted to the line will remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.
3. **DTMF Tones:** The R1212 generates dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits (see Interface Memory Definitions)must be set to a 1. When in this mode, the specific DTMF tones generated are decided by loading the dial digit register with the appropriate digit as shown in Table 2.

Table 2. Dial Digits/Tone Pairs

Hex	Dial Digits	Tone Pairs	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	★	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

TONE DETECTION

The R1212 detects tones in the 340 ±5 Hz to 640 ±5 Hz band.
Detection Level: −10 dBm to −43 dBm
Response Time: 17 ±2 ms

SIGNALING AND DATA RATES

The signaling and data rates for the R1212 are defined in Table 3.

Table 3. Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22:		
(Alternative A)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
(Alternative B)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
Mode ii		1200 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character
Mode iv		600 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character
Bell 212A;	600	1200 bps ±0.01%, Synchronous/Asynchronous
	0 to 300	0 to 300 bps Asynchronous

DATA ENCODING

The specifications for data encoding are as follows:

1. *1200 bps (V.22 and Bell 212A).* The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
2. *600 bps (V.22).* Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R1212 provides equalization functions that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—A fixed compromise equalizer is provided in the transmitter.

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ±150 microseconds over the frequency range 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R1212 incorporates a self-synchronizing scrambler-/descrambler. In accordance with the CCITT V.22 and the Bell 212A recommendations.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R1212 can adapt to received frequency errors of up to ±7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R1212 satisfies all specified performance requirements for the received line signals from −10 dBm to −48 dBm. The received line signal is measured at the receiver analog input RXA.

TRANSMIT LEVEL

The R1212M output control circuitry contains a variable gain buffer which reduces the modem output level. The R1212M can be strapped via the host interface memory to accomplish this.

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R1212M transmit level is +6 dBm to allow a Data Access Arrangement (DAA) to be used. The DAA then determines the permissive or programmable configuration.

The R1212DC transmit level is strapped in the permissive mode so that the maximum output level is −10 dBm ±1.0 dBm.

AUTOMATIC RECONFIGURATION

The R1212 is capable of automatically configuring itself to the compatibility of a remote modem. The R1212 can be in either the answer or originate mode for this to occur. The R1212 adaptation compatibilities are limited to V.22 A/B (1200 bps), Bell 212, and Bell 103. If the R1212 is to originate in a specific configuration, the MODE bits (see Interface Memory Definitions) must be set.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, DAA signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The column titled "Type" refers to designations found in the Hardware Circuits Interface Characteristics (Tables 5 and 6). The six groups of hardware circuits are described in the following paragraphs.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset (POR) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 μs. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The R1212 POR sequence leaves the modem configured as follows:

- 1200 bps
- Asynchronous
- 10-bit Character Length
- Constant Carrier
- Serial Mode
- Answer Mode
- Auto Answer Disabled
- RAM Access Code = 00

This configuration is suitable for performing high speed data transfer over the public switched telephone network using the serial data port. Individual features are discussed in subsequent paragraphs.

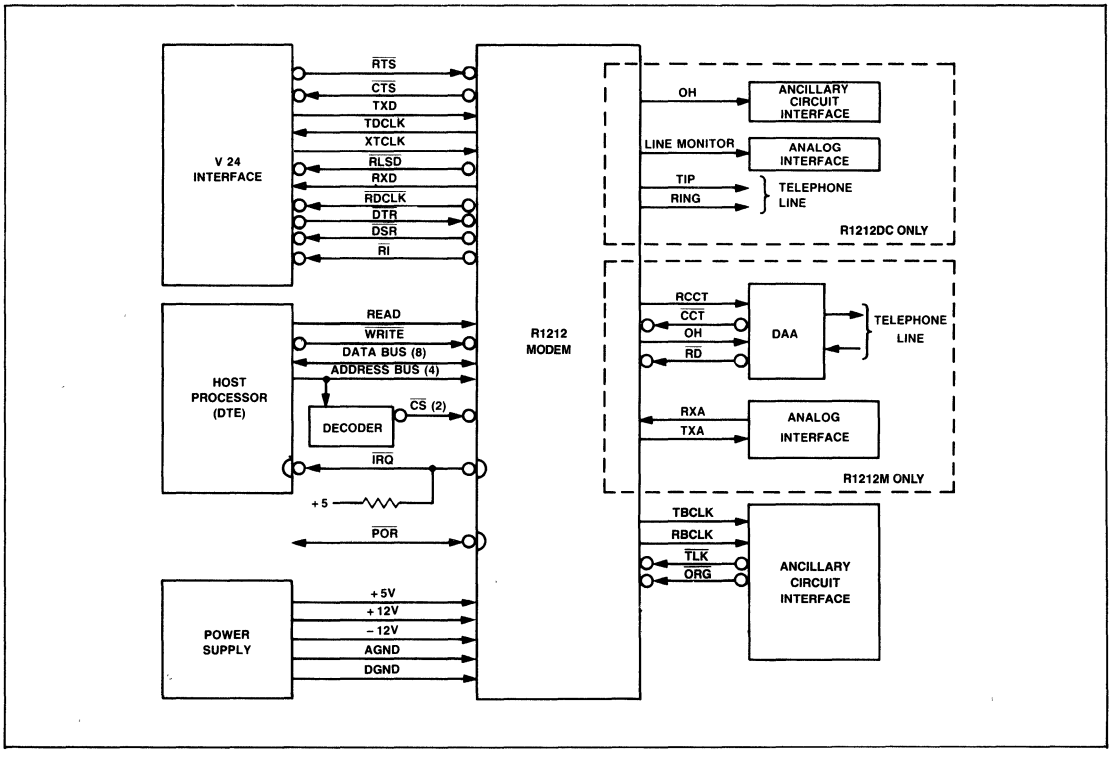


Figure 1. R1212 Modem Functional Interconnect Diagram

Table 4. Hardware Circuits

Name	Type	DIN Pin No.	Description
A. OVERHEAD SIGNALS			
Ground (A)	AGND	31C, 32C	Analog Ground Return
Ground (D)	DGND	3C, 8C, 5A, 10A	Digital Ground Return
+5 volts	PWR	19C, 23C, 26C, 30C	+5 volt supply
+12 volts	PWR	15A	+12 volt supply
−12 volts	PWR	12A	−12 volt supply
$\overline{POR}$	I/OB	13C	Power-on-Reset
B. MICROPROCESSOR INTERFACE SIGNALS			
D7	I/OA	1C	↕ Data Bus (8-Lines)
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	Register Select (4-Lines)
RS2	IA	6A	
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select Receiver (Baud Rate Device)
$\overline{CS1}$	IA	9C	Chip Select Transmitter (Sample Rate Device)
$\overline{READ}$	IA	12C	Read Enable
$\overline{WRITE}$	IA	11A	Write Enable
$\overline{IRQ}$	OB	11C	Interrupt Request

Name	Type	DIN Pin No.	Description
C. V.24 INTERFACE SIGNALS			
XTCLK	IB	22A	External Transmit Clock
$\overline{TDCLK}$	OC	23A	Transmit Data Clock
$\overline{RDCLK}$	OC	21A	Receive Data Clock
$\overline{RTS}$	IB	25A	Request-to-Send
$\overline{CTS}$	OC	25C	Clear-to-Send
TXD	IB	24C	Transmit Data
$\overline{RXD}$	OC	22C	Receive Data
$\overline{RLSD}$	OC	24A	Received Line Signal Detector
$\overline{DTR}$	IB	21C	Data Terminal Ready
$\overline{DSR}$	OC	20A	Data Set Ready
$\overline{RI}$	OC	18A	Ring Indicator
D. ANALOG SIGNALS			
RXA (M)	IB	32A	Receive Analog Input
TXA (M)	OC	31A	Transmit Analog Output
TIP/RING (DC) LINE	AE	RJ11 Jacks	Phone Line Interface
MONITOR (DC)	AD	30A	Analog Line Monitor
E. DAA INTERFACE SIGNALS			
$\overline{RD}$ (M)	IB	27A	Ring Detect
RCCT (M)	OC	28A	Request Coupler Cut Through
$\overline{CCT}$ (M)	IB	29C	Coupler Cut Through
OH	OC	29A	Off-Hook Relay Status
F. ANCILLARY INTERFACE SIGNALS			
TBCLK	OC	27C —	Transmit Baud Clock
RBCLK	OC	26A —	Receive Baud Clock
$\overline{TLK}$	IC	28C —	Talk (TLK = Data)
$\overline{ORG}$	IB	16C —	Originate (ORG = Answer)

(M) R1212M Only, (DC) R1212DC Only, — = not applicable
Unused inputs tied to +5V or ground require individual 10K Ω series resistors

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Ouput Type IA	IB	IC	OA	OB	OC	I/O A	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min [2]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0 4 max [2]	0.4 max.[2]	0 4 max.[2]	0.4 max [2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±2.5 max [4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive Circuit Type	pF	TTL	TTL w/Pull-up	TTL w/Pull-up	100 TTL	100 Open-Drain	100 Open-Drain w/Pull-up	100 3 State Transceiver	100 Open-Drain w/Pull-up

Notes: 1. I load = −100 μA 2. I load = 1.6 mA 3. I load = −40 μA 4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc 5. I load = 0.36 mA

Table 6. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604Ω ±1% with an output level of +6 dBm. To obtain a 0 dBm output, a 600Ω load to ground is needed.
RXA	AB	The receiver input impedance is 23.7 KΩ ±1%. The receive level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).
LINE MONITOR	AD	The line monitor output impedance is 15 KΩ ±5%.
TIP/RING	AE	The impedance of TIP with respect to RING is 600 Ω.

V.24 INTERFACE

Eleven hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, +5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Data Terminal Ready ($\overline{DTR}$)

$\overline{DTR}$ prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. $\overline{DTR}$ OFF places the modem in the disconnect state.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) ON indicates that the modem is in the data transfer state. $\overline{DSR}$ OFF is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except $\overline{RI}$. $\overline{DSR}$ will switch to the OFF state when in test state. The ON condition of $\overline{DSR}$ indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.
4. After ring indicate ($\overline{RI}$) goes ON, $\overline{DSR}$ waits at least two seconds before turning ON to allow the telephone company equipment to be engaged.

$\overline{DSR}$ will go OFF 50 ms after $\overline{DTR}$ goes OFF, or 50 ms plus a maximum of 4 seconds when the SSD bit is enabled.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. In constant carrier mode, $\overline{RTS}$ can be wired to $\overline{DTR}$. In controlled carrier operation, independent operation of $\overline{RTS}$ turns the carrier ON and OFF. The responses to $\overline{RTS}$ are shown in Table 7 (assume the modem is in data mode).

Table 7. $\overline{RTS}$ Responses

Leased or Dial Line[1]	$\overline{RTS}$ OFF	$\overline{RTS}$ ON
Controlled Carrier	$\overline{CTS}$ OFF Carrier OFF	Carrier ON 210 to 275 ms Scrambled 1 s Transmitted $\overline{CTS}$ ON
Constant Carrier	$\overline{CTS}$ OFF Carrier ON Scrambled 1 s Transmitted	$\overline{CTS}$ ON Carrier ON Data Transmitted

Note:
1. After handshake is complete.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON or OFF condition of $\overline{RTS}$ are shown in Table 8.

Table 8. $\overline{CTS}$ Response Times

$\overline{CTS}$ Transition	Constant Carrier	Controlled Carrier
OFF to ON	<2 ms	210 to 275 ms
ON to OFF	<20 ms*	<20 ms*

Note: *Programmable

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 1200 Hz or 600 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

TDCLK is provided to the user in both asynchronous and synchronous communications. TDCLK is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing (TDCLK is not valid in FSK). TDCLK is necessary for synchronous communication. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{\text{RDCLK}}$)

The modem provides a Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±.035% (relative) frequency error in the associated transmit timing source.

$\overline{\text{RDCLK}}$ is provided to the user in both asynchronous and synchronous communications. $\overline{\text{RDCLK}}$ is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing ($\overline{\text{RDCLK}}$ is not valid in FSK). $\overline{\text{RDCLK}}$ is necessary for synchronous communication.

Received Line Signal Detector ($\overline{\text{RLSD}}$)

The $\overline{\text{RLSD}}$ thresholds for both high and low channels are:

$\overline{\text{RLSD}}$ ON $\geq$ −43 dBm
$\overline{\text{RLSD}}$ OFF $\leq$ −48 dBm

$\overline{\text{RLSD}}$ will not respond to guard tones or answer tones.

When $\overline{\text{RLSD}}$ is active, it indicates to the terminal equipment that valid data is available on RXD.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Ring Indicator ($\overline{\text{RI}}$)

The modem provides a Ring Indicator ($\overline{\text{RI}}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the ON segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The high condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received. The operation of $\overline{\text{RI}}$ is not disabled by an OFF condition on $\overline{\text{DTR}}$.

$\overline{\text{RI}}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across TIP and RING), with the response times given in Table 13.

This OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent ON (OFF) transition of $\overline{\text{RI}}$.

Table 9. $\overline{\text{RI}}$ Response Time

$\overline{\text{RI}}$ Transition	Response Time
OFF-to-ON*	110 ±50 ms (50% duty cycle)
ON-to-OFF	450 ±50 ms
Note: *The OFF-to-ON time is duty cycle dependent: 890 ms (15%) ≥ time ≥ 50 ms (100%)	

MICROPROCESSOR INTERFACE

Seventeen hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$ and $\overline{CS1}$) and Register Selects (RS0-RS1)

The signal processor to be accessed is selected by grounding one of two unique chip select lines, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

DAA INTERFACE

The R1212M provides a Data Access Arrangement (DAA) interface that is directly hardware and software compatible with the RDAA. Manual/automatic originate and answer are then controlled via the appropriate R1212M hardware ancillary circuits or software control bits. The modem provides the only interface with the microprocessor (MPU) bus, i.e., no RDAA interface signals must be directly controlled from the MPU bus.

Ring Detect ($\overline{RD}$)

$\overline{RD}$ indicates to the modem by an ON (low) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the $\overline{RD}$ input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on $\overline{RI}$.

Request Coupler Cut Through (RCCT)

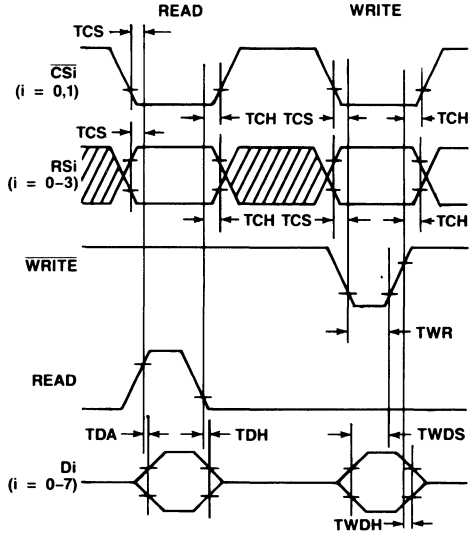
RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes OFF (low), the cut-through buffers are disabled and $\overline{CCT}$ should go OFF (high). RCCT should be OFF during dialing but ON for tone address signaling.

Coupler Cut Through ($\overline{CCT}$)

An ON (low) signal to the $\overline{CCT}$ lead indicates to the modem that the data transmission path through the DAA is connected. This input can always be grounded if the two second billing delay squelch is desired. If $\overline{CCT}$ is user controlled, the billing delay squelch can only be 2 seconds or greater.

Off-Hook Relay Status (OH)

The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.



Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
$\overline{CSi}$, RSi hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

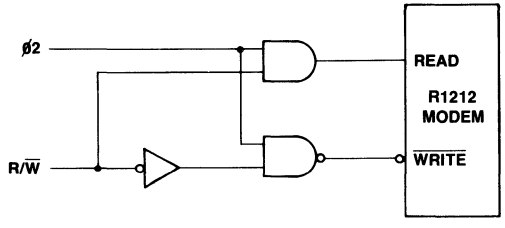


Figure 3. R/$\overline{W}$ to READ $\overline{WRITE}$ Conversion Logic

ANALOG SIGNALS (R1212M)

Two connections are devoted to analog audio signals: TXA and RXA.

Transmit Analog (TXA)

The TXA output is suitable for driving a data access arrangement for connection to either leased lines or the public switched telephone network. The transmitter output impedance is 604 ohms ±1% with an output level of +6 dBm ±1 dBm. To obtain a 0 dBm output, a 600 ohm load to ground is needed.

Receive Analog (RXA)

RXA is an input to the receiver from a data access arrangement. The input impedance is 23.7K ohms ±1%. The received level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).

ANALOG SIGNALS (R1212DC)

Three analog signals are output by the R1212DC: LINE MONITOR, TIP and RING.

Analog Line Monitor (LINE MONITOR)

The LINE MONITOR output is suitable for a speaker interface. It provides an output for all dialing signals, call progress signals, and the carrier signals. The output impedance is 15K ohms ±1%. The signals which appear on LINE MONITOR are approximately the same level as the signals would appear on the network (assuming a 1 dB loss attributed to the audio transformer).

Phone Line Interface (TIP and RING)

TIP and RING are the DAA analog outputs to the public switched telephone network. These outputs use two RJ11 jacks in parallel as the interface to the network (see Table 10 and Figure 4). The R1212DC, which contains the DAA TIP and RING interface, has been FCC Part 68 approved. The user need not apply for further Part 68 approval. The impedance of TIP with respect to RING is 600 ohms.

Table 10. R1212DC Network Interface

Connector Type	Pin Number	Name	Function
RJ11 Jack	3	RING	One Side of TELCO Line
	4	TIP	One Side of TELCO Line

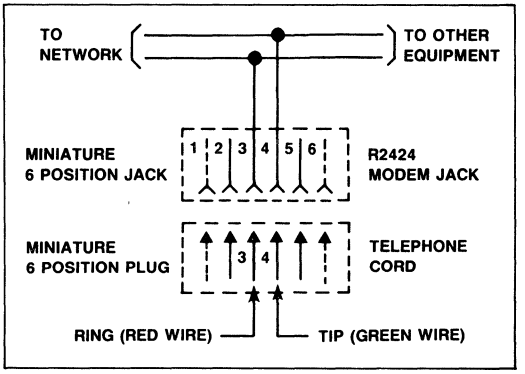


Figure 4. RJ11 Telephone Jack

ANCILLARY CIRCUITS

Transmit Baud Clock (TBCLK) and Received Baud Clock (RBCLK)

TBCLK and RBCLK are provided to the user at the baud rate (600 Hz).

Talk ($\overline{TLK}$)

$\overline{TLK}$ is an input which manually places the modem on-hook (relay open, $\overline{TLK}$ = 0) or off-hook (relay closed, $\overline{TLK}$ = 1). The on-hook condition is referred to as TALK mode and the off-hook condition is referred to as DATA mode. $\overline{TLK}$ is used with $\overline{ORG}$ to manually originate or answer a call. $\overline{TLK}$ should be 0 at power-on or reset to prevent the modem from inadvertently entering the data mode.

Originate ($\overline{ORG}$)

$\overline{ORG}$ is an input which manually places the modem in the originate mode ($\overline{ORG}$ = 0) or the answer mode ($\overline{ORG}$ = 1). To manually originate a call, $\overline{ORG}$ = 0 and $\overline{TLK}$ = 0. Dial the number using the telephone. When the other modem answers and sends answer tone switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

To manually answer a call $\overline{ORG}$ = 1 and $\overline{TLK}$ = 0. When the phone rings switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

Off-Hook Relay Status (OH)

The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load-/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on two special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into two areas. These areas are partitioned into receiver and transmitter devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 32 addressable registers in the modem receiver (CS0) and transmitter (CS1) interface memory are shown in Figures 5 and 6, respectively. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Figures 7 and 8 show the registers according to the overall function they perform in the receiver and transmitter, respectively. Figures 9 and 10 show the power-on configuration for the R1212 modem receiver and transmitter devices, respectively.

Table 11 defines the individual bits in the interface memory. In the Table 11 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R							
E	IRQ	ENSI	NEWS	—	NEWC	—	—	—
D	BUS	CRQ	—	—	—	LCD	RSD	—
C	—	—	—	CHAR		—	—	—
B	—	—	—	—	—	—	—	AL
A	ERDL	RDL	DL	ST	MODE			
9	—	—	SPEED		—	—	—	—
8	TONE	ATD	—	—	—	—	TM	RLSD
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (YRAMRM)							
4	RAM Data YRL (YRAMRL)							
3	RAM Data XRM (XRAMRM)							
2	RAM Data XRL (XRAMRL)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—

Note
(—) Indicates reserved for modem use only.

Figure 5. Receiver ($\overline{CS0}$) Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T							
E	IRQ	ENSI	NEWS	—	NEWC	DDEI	—	DDRE
D	BUS	CRQ	DATA	AAE	DTR	—	—	SSD
C	DSRA	TXCLK		CHAR		—	—	DLSF[1]
B	TX LEVEL			GTE	GTS	3DB	DTMF	AL
A	ERDL	RDL	DL	ST	MODE			
9	NAT[1]	—	ORG	LL	RTS	CC	EF	NTS
8	DLO	CTS	DSR	RI	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (YRAMTM)							
4	RAM Data YTL (YRAMTL)							
3	RAM Data XTM (XRAMTM)							
2	RAM Data XTL (XRAMTL)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register							

Notes
1. Not valid before R5312-16
(—) Indicates reserved for modem use only.

Figure 6. Transmitter ($\overline{CS1}$) Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	DIAGNOSTIC CONTROL							
E	HANDSHAKE							
D	CONFIGURATION							
C	CONFIGURATION							
B	CONFIGURATION							
A	CONFIGURATION							
9	STATUS							
8	STATUS							
7	RESERVED							
6	RESERVED							
5	DIAGNOSTIC							
4	DIAGNOSTIC							
3	DIAGNOSTIC							
2	DIAGNOSTIC							
1	RESERVED							
0	RESERVED							
Register / Bit	7	6	5	4	3	2	1	0

Figure 7. Receiver ($\overline{CS0}$) Interface Memory Functions

Register \ Bit	7	6	5	4	3	2	1	0
F	DIAGNOSTIC CONTROL							
E	HANDSHAKE							
D	CONFIGURATION							
C	CONFIGURATION							
B	CONFIGURATION							
A	CONFIGURATION							
9	CONFIGURATION							
8	STATUS							
7	RESERVED							
6	RESERVED							
5	DIAGNOSTIC							
4	DIAGNOSTIC							
3	DIAGNOSTIC							
2	DIAGNOSTIC							
1	RESERVED							
0	DIAL DIGIT REGISTER							
Register / Bit	7	6	5	4	3	2	1	0

Figure 8. Transmitter ($\overline{CS1}$) Interface Memory Functions

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	—	—	—
D	BUS 0	CRQ 0	—	—	—	LCD 1	RSD 0	—
C	—	—	—	CHAR 1	0	—	—	—
B	—	—	—	—	—	—	—	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	0	MODE 0	1	1
9	—	—	SPEED 0	0	—	—	—	—
8	TONE 0	ATD 0	—	—	—	—	TM 0	RLSD 0
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (Random)							
4	RAM Data YRL (Random)							
3	RAM Data XRM (Random)							
2	RAM Data XRL (Random)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—
Register \ Bit	7	6	5	4	3	2	1	0
(—) Indicates reserved for modem use only.								

Figure 9. R1212 Receiver ($\overline{CS0}$) Interface Memory Power On Configuration

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	DDEI 0	—	DDRE 0
D	BUS 0	CRQ 0	DATA 0	AAE 0	DTR 0	—	—	SSD 0
C	DSRA 0	TX CLK 0	0	CHAR 1	0	—	—	DLSF 0
B	TX LEVEL 0	0	0	GTE 0	GTS 0	3DB 0	DTMF 0	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	0	MODE 0	1	1
9	NAT 0	—	ORG 0	LL 0	RTS 0	CC 0	EF 0	NTS 0
8	DLO 0	CTS 0	DSR 0	RI 0	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (Random)							
4	RAM Data YTL (Random)							
3	RAM Data XTM (Random)							
2	RAM Data XTL (Random)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register (Write-Only Register)							
Register \ Bit	7	6	5	4	3	2	1	0
(—) Indicates reserved for modem use only.								

Figure 10. R1212 Transmitter ($\overline{CS1}$) Interface Memory Power On Configuration

Table 11. Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When configuration bit AAE is a 1, the modem will automatically answer when a ringing signal is present on the line. When AAE is set to a 1, the modem will answer after one ring and go into data mode. The modem goes off-hook 1 second after the on-to-off transition of the ring. The $\overline{ORG}$ pin or ORG bit need not to be set to the answer polarity. If it is desired to answer after more than one ring, then the user must use the alternative answer method described under the DATA bit. The $\overline{DTR}$ pin or the DTR bit must also be set before the modem will auto answer. Writing a 0 into the AAE bit will cause the modem to go on-hook. This will occur only when the modem auto answers using the AAE bit.
AL	Analog Loopback	(0,1):B:0	When configuration bits AL are a 1, the modem is in local analog loopback (V.54 Loop 3). In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14 ±1 dBm. The modem may be placed into analog loopback in either the idle mode or the data mode. However, in the data mode, setting the AL bits to a 1 will terminate the connection. Analog loopback will only function in the high speed modes (1200, or 600 bps). The DTE may be tested when the modem is in analog loopback. Also, all parts of the modem except the line interface are checked. If no DTE is connected, the modem integrity may be verified by use of the self test function. When entering analog loopback, set AL in the receiver to a 1 before setting AL in the transmitter to a 1. When exiting analog loopback, reset AL in the transmitter to a 0 before resetting AL in the receiver to a 0.
ATD	Answer Tone Detected	0:8:6	When status bit ATD is a 1, it signifies that the modem receiver detected the answer tone. The bit is 1 set 75 ms after the answer tone is first detected, and is cleared to a 0 when the modem goes on-hook. The user may clear ATD manually after CTS is active.
BUS	Bus Select	(0,1):D:7	When configuration bits BUS are a 1, the modem is in the parallel control mode; and when 0, the modem is in the serial control mode. BUS can be in either state to configure the modem. *Serial Control Mode* The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. The control signals used in serial control mode are $\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, and $\overline{ORG}$. Outputs such as $\overline{RLSD}$ and $\overline{DSR}$ are reflected both in the interface memory and the V.24 interface. Once the bus bits have been set to a 0, the state of the DTR, RTS, DATA, and ORG bits are ignored. *Parallel Control Mode* The modem has the capability of modem control via the microprocessor bus. Data transfer is maintained over the serial V.24 channel. The control bits used in parallel control are DTR, RTS, ORG, and DATA. The modem automatically defaults to the serial mode at power-on. If the parallel control mode is to be used, it is recommended that the $\overline{TLK}$ pin be tied to ground. A floating $\overline{TLK}$ pin will assume a logic 1 which will immediately put the modem into the data mode before the BUS bits are set. In either mode, the modem is configured by the host processor via the microprocessor bus.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
CC	Controlled Carrier	1:9:2	When configuration bit CC is a 1, the modem operates in controlled carrier; when 0, the modem operates in constant carrier. Controlled carrier allows the modem transmitter to be controlled by the $\overline{RTS}$ pin or the RTS bit. Its effect may be seen in the RTS and CTS descriptions.
CHAR	Character Length Select	(0,1):C:(3,4)	These character length bits select either 8, 9, 10, or 11 bit characters (includes data, stop, and start bits) as shown below: **Configuration Word** (4 3) — **Configuration** 0 0 — 8 bits 0 1 — 9 bits 1 0 — 10 bits 1 1 — 11 bits It is possible to change character length during the data mode. Errors in the data will be expected between the changeover and the resynchronization (which occurs on the next start bit after the change is implemented).
CRQ	Call Request	(0,1):D:6	When configuration bit CRQ in chip 1 (the transmitter) is a 1, it places the transmitter in auto dial mode. The data then placed in the Dial Digit Register is treated as digits to be dialed. The format for the data should be a hex representation of the number to be dialed (if a 9 is to be dialed then an 09_{16} should be loaded in DDR). CRQ in chip 1 should be a 1 for the duration of the data mode. If CRQ in chip 1 is changed to a 0, the modem will go on-hook. Also, see DDRE bit. When configuration bit CRQ in chip 0 (the receiver) is a 1, the receiver goes into tone detect mode. Any energy above threshold and in the 345 to 635 Hz bandwidth is reflected by the TONE bit. CRQ in chip 0 must be reset to a 0 (after the last digit was dialed and tone detection completed) before the answer tone is sent by the answering modem (after ringback is detected). CRQ in chip 0 need not be used during auto dialing, but may be used to provide call progress information as part of an intelligent auto dialing routine. An example flowchart is given in Figure 11. FF (hex) should be loaded into the Dial Digit Register after the last digit is dialed and tone detection is completed. This action also puts the modem in data mode and starts a 30 second abort timer. If the handshake has not been completed in 30 seconds the modem will go on-hook.
CTS	Clear-to-Send	1:8:6	When status bit CTS is a 1, it indicates to the terminal equipment that the modem will transmit any data which are present at TXD. CTS response times from an ON or OFF condition of RTS are shown below: **CTS Transition** — **Constant Carrier** — **Controlled Carrier** OFF to ON — ≤2 ms — 210 to 275 ms ON to OFF — ≤20 ms* — ≤20 ms* *Programmable
DATA	Talk/Data	1:D:5	When control bit DATA is a 1, the modem is in the data state (off-hook); and when 0, the modem is in the talk state (on-hook). This bit allows the modem to go off-hook after a programmable number of rings by counting the required number of RI bit transitions and then setting the DATA bit (assuming ORG = 0).
DDEI	Dial Digit Empty Interrupt	1:E:2	When handshake bit DDEI is a 1, an interrupt will occur when the Dial Digit Register (1:0) is empty (DDRE = 1). This is independent of the state of the ENSI bit. The interrupt will set the IRQ bit and also assert the $\overline{IRQ}$ signal. Loading the Dial Digit Register with a new digit will clear the interrupt condition.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DDR	Dial Digit Register	1:0:(0–7)	DDR is used to load the digits to be dialed. Example: If a 4 is to be dialed, an 04 (hex) should be loaded. This action also causes the interrupt to be cleared. The modem automatically accounts for the interdigit delay. Note: DDR is a write-only register.
DDRE	Dial Digit Register Empty	1:E:0	When handshake bit DDRE is a 1, it indicates that the dial digit register is empty and can be loaded with a new digit to be dialed. If the DDEI bit is set, the IRQ bit will be set when the DDRE bit is set. Also, the $\overline{IRQ}$ signal will be generated. After the DDR is loaded, DDRE goes to a 0 and the interrupts are automatically cleared.
DL	Digital Loopback (Manual)	(0,1):A:5	When configuration bits DL are set to a 1, the modem is manually placed in digital loopback. DL should only be set during the data mode. The DSR and CTS bits will be reset to a 0. The local modem can then be tested from the remote modem end by looping a remotely generated test pattern. At the remote modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be reset to a 0. The local modem will then return to the normal data mode with control reverting to the DTEs, DTR. DL does not function in 300 bps.
DLO	Dial Line Occupied	1:8:7	When status bit DLO is a 1, it indicates that the modem is in the auto dial state, i.e., CRQ in the transmitter is a 1 and the modem is off-hook and ready to dial.
DLSF	Disable Low Speed Fallback	1:C:0	When configuration bit DLSF is a 1, the modem will not automatically fallback to the 300 bps operating mode if it is configured for another data rate. This bit is valid in originate mode only.
DSR	Data Set Ready	1:8:5	The ON condition of the status bit DSR indicates that the modem is in the data transfer state. The OFF condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits — except RI. DSR will switch to the OFF state when in test state. The ON condition of DSR indicates the following: The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing. The modem has generated an answer tone or detected answer tone. After ring indicate goes ON, DSR waits at least two seconds before turning ON to allow the telephone company equipment to be engaged. DSR will go OFF 50 msec after DTR goes OFF, or 50 msec plus a maximum of 4 sec when the SSD bit is enabled.
DSRA	Data Set Ready in Analog Loopback	1:C:7	When configuration bit DSRA is a 1, it causes DSR to be ON during analog loopback.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DTMF	Touch Tones/Pulse Dialing	1:B:1	When configuration bit DTMF is a 1, it tells the modem to auto dial using tones; and when 0, the modem will dial using pulses. The timing for the pulses and tones are as follows (power-on timing): Pulses — Relay open 64 ms Relay closed 36 ms Interdigit delay 750 ms Tones — Tone duration 95 ms Interdigit delay 70 ms The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. The output power level of the DTMF tones is as follows: ±15 dBm ±1 measured at TXA for the R1212M −1 dBm ±1 measured at TIP/RING for the R1212DC
DTR	Data Terminal Ready	1:D:3	Control bit DTR must be a 1 for the modem to enter the data state, either manually or automatically. DTR must also be a 1 in order for the modem to automatically answer an incoming call. During the data mode, DTR must remain at a 1, otherwise the connection will be terminated if DTR resets to a 0 for greater than 50 ms.
EF	Enable Filters	1:9:1	Setting CRQ in the transmitter to a 1 disables the high and low band filters used in data mode so that call progress tone detection can be done. Setting CRQ in the receiver to a 1 inserts a passband filter in the receive path which passes energy in the 345 Hz to 635 Hz bandwidth. The high and low band filters must be enabled and the passband filter disabled for the answer tone and carrier to be detected. This occurs automatically during the auto dial process when EF is set to a 0. In this case, the high and low band filters are disabled when CRQ in the transmitter is set to a 1. If tone detection is required, CRQ in the receiver should be set to a 1. After dialing and call progress tone detection, CRQ in the receiver is set to a 0 and FF is loaded into the dial digit register. (Loading FF enables the high and low band filters). At this time, the answer tone can be detected. To re-enable the high and low band filters disabled by setting CRQ in the transmitter, set EF to a 1. After CRQ in the transmitter and receiver is set to a 1 and tone detection is completed, it may be necessary to detect the answer tone before loading FF into the dial digit register (see the section on sending 1300 Hz calling tone). At that point, EF can be set to a 1 and CRQ in the receiver set to a 0 so the answer tone can be detected (using the ATD bit) and the 1300 Hz calling tone can still be sent. Once the answer tone is detected, FF should be loaded into the dial digit register and the EF bit set to a 0.
ENSI	Enable New Status Interrupt	(0,1):E:6	When handshake bit ENSI is a 1, it causes an interrupt to occur when the status bits in registers (0:[8,9]) and (1:8) are changed by the modem. (NEWS = 1). The IRQ bit will be set to a 1 and the $\overline{IRQ}$ signal will be generated. The interrupt is cleared by writing a 0 into the NEWS bit.
ERDL	Enable Response to Remote Digital Loopback	(0,1):A:7	When configuration bits ERDL are a 1, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS, DSR and RLSD bits to a 0 and turns the $\overline{CTS}$, $\overline{DSR}$ and $\overline{RLSD}$ signals to a logic 1. The TM bit is set to inform the user of the test status. When the ERDL bits are a 0, no response will be generated.
GTE	Guard Tone Enable	1:B:4	When configuration bit GTE is a 1, it causes the specified guard tone to be transmitted (CCITT configurations only), according the state of the GTS bit. Note: The guard tone will only be transmitted by the answering modem.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
GTS	Guard Tone Select	1:B:3	When configuration bit GTS is a 0, it selects the 1800 Hz tone; when GTE is a 1 it selects the 550 Hz tone. The selected guard tone will be transmitted only when GTE is enabled.
IRQ	Interrupt	(0,1):E:7	When status bit IRQ is a 1, it indicates that an interrupt has been generated. The $\overline{IRQ}$ hardware signal is generated following the setting of the IRQ bit. $\overline{IRQ}$ is cleared when either the NEWS bit is reset to a 0 or the DDR is loaded with a number.
LCD	Loss of Carrier Disconnect	0:D:2	When configuration bit LCD is a 1, the modem terminates a call when a loss of received carrier energy is detected after 400 ms. After the first 40 ms of loss of carrier, RLSD goes off. 360 ms later, if no carrier is detected, CTS goes off, and the modem goes on-hook. If energy above threshold is detected during the 360 ms period, RLSD will be set to a 1 again. If further loss of energy occurs, the 400 ms time frame is restarted. If LCD is set to a 0, RLSD will be set to a 1 when energy is above threshold, but will not force the modem on-hook when energy falls below threshold. In this case, it is necessary to re-enable LCD in order to put the modem on-hook. LCD is not automatically disabled in leased line operation. The user must write a 0 into LCD bits for this to occur.
LL	Leased Line	1:9:4	When configuration bit LL is a 1, the modem is in leased line operation; when 0, the modem is in switched line operation. When LL is set to a 1, the modem immediately goes off-hook and into data mode.
MODE	Mode Select	(0,1):A:(0,3)	These bits select the compatibility at which the modem is to operate, as shown below: **Configuration Word** / **Configuration** 3 2 1 0 0 0 1 0 — Bell 212A 1200 Sync. 0 0 1 1 — Bell 212A 1200 Async. 0 1 0 0 — Bell 212A 0 to 300 Async. 1 0 0 0 — V.22A 1200 Sync. 1 0 0 1 — V.22B 1200 Async. 1 0 1 0 — V.22A 600 Sync. 1 0 1 1 — V.22B 600 Async. NOTE: The Mode bits in both chips should be set exclusively of all other bits, followed immediately by the setting of the NEWC bits. This will ensure proper modem configuration. *Automatic Reconfiguration* The modem is capable of automatically falling back during the handshake to the compatibility of a remote modem. The modem can be in either the answer or originate mode for this to occur. The compatibilities that the modem are limited to adapt to are V.22 A/B (1200 bps), Bell 212 and Bell 103. If the R1212 is to originate in a specific configuration, the MODE bits must be set. When the answer modem is configured for Bell 300 asynchronous and is called by a 1200 bps modem, the handshake will be completed at 1200 bps.
NAT	No Answer Tone	1:9:7	When configuration bit NAT is a 1, the modem will not transmit the 2100 Hz CCITT answer tone. This bit is only valid for CCITT configurations. With this bit enabled in answer mode, when the modem goes off-hook it will remain silent for 75 ms and then transmit unscrambled ones.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
NEWC	New Configuration	(0,1):E:3	When the NEWC bit is a 1, it tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC to a 0. NEWC must be set to a 1 after a new configuration has been written into the following registers: (0:[A–D]) and (1:[9–D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.
NEWS	New Status	(0,1):E:5	When handshake bit NEWS is a 1, it tells the user that there has been a change of status in the status registers. The user must write a 0 into NEWS to reset it. This action also causes the interrupt to be cleared.
NTS	No Transmitter Scrambler	1:9:0	When configuration bit NTS is a 1, when the modem is off-hook it will transmit all data in an unscrambled form. This bit should be disabled if the normal modem handshake is desired.
ORG	Originate/Answer	1:9:5	When configuration bit ORG is a 1, the modem is in originate mode; and when a 0 the modem is in answer mode. (This is only valid in manual originate/answer and analog loopback). If ORG is a 1 in analog loopback, the modem will transmit in the high band and receive in the low band. If ORG is a 0 in analog loopback, the modem will transmit in the low band and receive in the high band.
(None)	RAM Access R	0:F:0–7	Contains the RAM access code used in reading RAM locations in chip 0 (receiver device).
(None)	RAM Access T	1:F:0–7	Contains the RAM access code used in reading RAM locations in chip 1 (transmitter device).
XRAMRL	RAM Data XRL	0:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 0.
XRAMRM	RAM Data XRM	0:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 0.
XRAMTL	RAM Data XTL	1.2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
XRAMTM	RAM Data XTM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.
YRAMRL	RAM Data YRL	0:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 0.
YRAMRM	RAM Data YRM	0:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 0.
YRAMTL	RAM Data YTL	1:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1.
YRAMTM	RAM Data YTM	1:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RDL	Remote Digital Loopback	(0,1):A:6	When configuration bits RDL are a 1, it causes the modem to initiate a request for the remote modem to go into digital loopback. RXD is clamped to a mark and the CTS bit and $\overline{CTS}$ signal will be reset until the loop is established. The TM bit is not set in this case, since the local modem initiated the request. RDL does not function in 300 bps.
RI	Ring Indicator	1:8:4	When status bit RI is a 1, it indicates that a ringing signal is being detected. The RI bit follows the ringing signal with a 1 during the on time and a zero during the off time coincident with the $\overline{RI}$ signal. The following are the RI bit response times: **RI Bit Transition** — **Response** OFF-to-ON* — 110 ±50 ms (50% duty cycle) ON-to-OFF — 450 ±50 ms *The OFF-to-ON time is duty cycle dependent: 890 ms (15%) ≥ time ≥ 50 ms (100%) This OFF-to-ON (or ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent transition of the RI bit.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RLSD	Received Line Signal Detector	0:8:0	When status bit RLSD is a 1, it indicates that the carrier has successfully been received. RLSD will not respond to the guard tones or answer tones. RLSD response times are given below: **RLSD**[1] — **Constant Carrier** — **Controlled Carrier** OFF-to-ON — 105 to 205 ms — 105 to 205 ms ON-to-OFF — 10 to 24 ms — 10 to 24 ms **Note:** 1. After handshake has occurred.
RSD	Receive Space Disconnect	0:D:1	When configuration bit RSD is a 1, the modem goes on-hook after receiving approximately 1.6 seconds of continuous spaces.
RTS	Request-to-Send	1:9:3	When control bit RTS is a 1, the modem transmits any data on TXD when CTS becomes active. In constant carrier mode, RTS should be set the same time as DTR and then left ON. In controlled carrier operation, independent operation of RTS turns the carrier ON and OFF. The responses to RTS are shown (assume the modem is in data mode). **Leased or Dial Line**[1] — **RTS Off** — **RTS On** Controlled Carrier — CTS OFF Carrier OFF — Carrier ON 210 to 275 ms Scrambled 1's Transmitted CTS ON Constant Carrier — CTS OFF Carrier ON Scrambled 1's Transmitted — CTS ON Carrier ON Data Transmitted **Note:** 1. After handshake is complete. For ease of use in constant carrier mode, RTS should be turned ON the same time as DTR.
SPEED	Speed Indication	0:9:(4,5)	The SPEED status bits reflect the speed at which the modem is operating. The SPEED bit representations are shown. **4** **5** — **Speed** 0 0 — 0–300 0 1 — 600 1 0 — 1200 **Note:** The SPEED bits are not active in analog loopback and leased line mode.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
SSD	Send Space Disconnect	1:D:0	When configuration bit SSD is a 1, it causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR goes from active to inactive state.
ST	Self Test	(0,1):A:4	When configuration bit ST is a 1, self test is activated. ST must be a 0 to end the test. It is possible to perform self test in analog loopback with or without a DTE connected. During any self test, TXD and RTS are ignored. Self test does not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver. Error detection is accomplished by monitoring the self test error counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic register when the RAM access code 00 is loaded in the diagnostic control register (0:F). *Self Test End-to-End (Data Mode)* Upon activation of self test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. *Self Test with Loop 3* Loop 3 is applied to the modem as defined in Recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test, In this test DTR is ignored. *Self Test with Loop 2 (Data Mode)* The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test. ST does not function in 300 bps.
3DB	3 dB Loss to Receive Signal	1:B:2	When configuration bit 3DB is a 1, it attenuates the received signal 3 dB. This is only used if the modem will see 0 dBm or greater line signal at the receiver input. Insertion of the 3 dB loss will then prevent saturation.
TM	Test Mode	0:8:1	When status bit TM is a 1, it indicates that the modem has completed the handshake and is in one of the following test modes: AL or RDL.
TONE	Tone Detect	0:8:7	TONE follows the energy detected in the 340 to 640 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when CRQ in chip 0 is a 1. Detection Range: −10 to −43 dBm Response Time: 17 ±2 ms
TXCLK	Transmit Clock Select	1:C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock, as shown below: **Configuration Word** **Transmit Clock** **6** **5** Internal 0 0 External 1 0 Slave 1 1 If external clock is chosen the user clock must be input at XTCLK. The clock characteristics must be the same as TDCLK. The external clock will be reflected by TDCLK. If slave clock is chosen the transmitter is slaved to the receive clock. This is also reflected by TDCLK.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TX LEVEL	Transmit Level	1:B:(5–7)	TX LEVEL allows the user to change the transmit level at TIP and RING (assuming the DAA has 10 dBm attenuation in the transmit path).

Configuration Word 7	6	5	Transmit Level (± 1.0 dBm) (at TIP and RING)
0	0	0	–10 dBm
0	0	1	–12 dBm
0	1	0	–14 dBm
0	1	1	–16 dBm
1	0	0	–18 dBm
1	0	1	–20 dBm
1	1	0	–22 dBm
1	1	1	–24 dBm

Internal Modem Timing

In a microprocessor environment it is necessary to know how long various functions last or what the response times of certain functions are. Since the modem is a part of the microprocessor environment its timing and response times are necessary. Table 12 provides the timing relationships between interface memory bits and modem functions.

Table 12. Internal Modem Timing

Parameter	Time Interval
NEWC bit checked	
Transmitter	Once per sample[1]
Receiver	Once per baud[2]
NEWC bit set by host until modem action	
Transmitter	≤ One baud time
Receiver	One baud time
Control, Configuration bits read	
Transmitter	Only after NEWC is set
Receiver	ST, RSD—every sample, all others after NEWC set
Status bits updated	
Transmitter	Once per sample
Receiver	Once per baud
Status change reflected by NEWS, IRQ	
Transmitter	MIN < one sample time MAX one sample time
Receiver	MIN one sample time MAX one baud time
Memory status reflected to modem pin	
Transmitter	33.33 μs
Receiver	33.33 μs

1. Sample Time = 7200 Hz 2. Baud Time = 600 Hz

AUTO DIAL SEQUENCE

The following flow chart defines the auto dial sequence via the microprocessor interface memory.

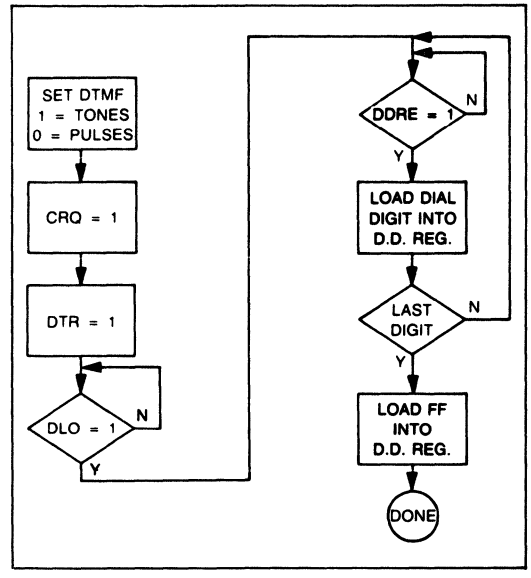


Figure 11. Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

SIGNAL PROCESSOR RAM ACCESS

RAM AND DATA ORGANIZATION

Each signal processor contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16-bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

Interface Memory Locations

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit normally transfers a word from RAM to interface memory once each clock cycle of the SP device. In the transmitter, a word is transferred from SP RAM to the interface memory every sample time. In the receiver, a word is transferred from RAM to the interface memory every sample time as well. Each RAM word transferred to the interface memory is 32-bits long. These bits are written by the SP logic unit into interface memory registers 5, 4, 3, and 2. Registers 3 and 2 contain the most significant byte and least significant byte, respectively, of the XRAM data. Registers 5 and 4 contain the most and least significant bytes of YRAM data, respectively.

RAM Access Codes

The SP logic unit determines the SP RAM address to read from, or write to, by the code stored in the RAM Access bits of interface memory register F (RAM Access R in the receiver 0:F and RAM Access T in the transmitter 1:F).

Only the transmitter (chip 1) allows data to be transferred from interface memory to SP RAM. When set to a 1, bit 1:F:7 signals the SP logic unit to disable transfer of SP RAM data to the interface memory, and instead, to transfer data from interface memory to SP RAM. When writing into SP RAM, 32 bits of data in the XRAM and YRAM registers will be written into the appropriate SP RAM location as specified by the RAM access code (82-86) in register 1:F (Table 13). Once the data is written into the RAM access register 1:F, the XRAM registers 1:2 and 1:3 or the YRAM registers 1:4 and 1:5, set the NEWC bit 1:E:3 to a 1. This action causes the information to be transferred from interface memory into SP RAM. Bit 7 of register 1:F is cleared to a 0 by the modem after the RAM is read. New data can be written into the SP RAM after the NEWC bit is reset to a 0 by the SP.

Note:

Any transmitter RAM Write operation must always be preceded by a RAM read from the desired location. This is to guarantee that the correct information is written into the 16 unchanged bits, since all transmitter RAM operations are 32 bit transfers with typically only 16 of the bits used.

Both the transmitter and receiver (chips 1 and 0, respectively) allow data to be transferred from SP RAM into the interface memory. A 0 in transmitter bit 1:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the RAM access code in register 1:F. A 0 in receiver bit 0:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the access code in register 0:F. To read the SP RAM in chip 1 (transmitter), load into 1:F the RAM access code which identifies the 32 bits of data to transfer to the XRAM and YRAM registers. Next, set the NEWC bit 1:E:3 to a 1. After transferring the data from RAM to the XRAM or YRAM registers, the NEWC bit is reset to a 0 by the SP. Chip 0 (receiver), on the other hand, will provide the XRAM and YRAM data one sample time following the loading of the RAM access code into register 0:F, and will continue to provide the same data at one sample time intervals until a new RAM access code is loaded.

When reading from or writing into RAM, no bits are provided for handshaking or interrupt functions. The NEWC bit can be used as a mechanism to provide sample and baud intervals. Since the NEWC bit is checked, once per baud in chip 0 and once per sample in chip 1, the user can set the NEWC bit and wait for it to be cleared. Depending on which chip the NEWC bit was set, the time interval from the setting to the clearing of the NEWC bit will be either one sample or one baud time. This, however, will not guarantee that the action of reading and writing the XRAM and YRAM will occur in the middle of an actual sample or baud time.

Table 13. RAM Access Codes

Node	Function	RAM Access Code		Chip	Reg. No.
		RAM Read	RAM Write		
1	Demodulator Output	56	–	0	2, 3, 4, 5
2	Low Pass Filter Output	40	–	0	2, 3, 4, 5
3	Input Signal to Equalizer Taps	41–4D	–	0	2, 3, 4, 5
4	AGC Gain Word	14	–	0	2, 3
5	Equalizer Tap Coefficients	01–0D	–	0	2, 3, 4, 5
6	Equalizer Output	53	–	0	2, 3, 4, 5
7	Rotated Equalizer Output (Received Point Eye Pattern)	11	–	0	2, 3, 4, 5
8	Decision Points (Ideal Eye Pattern)	51	–	0	2, 3, 4, 5
9	Rotated Error	52	–	0	2, 3, 4, 5
10	Rotation Angle	12	–	0	4, 5
11	Phase Error	10	–	0	2, 3
12	Self Test Error Counter	00	–	0	2, 3
	DTMF Tone Duration	02	82	1	4, 5
	DTMF Interdigit Delay	03	83	1	2, 3
	Pulse Interdigit Delay	03	83	1	4, 5
	Pulse Relay Make Time	04	84	1	2, 3
	Pulse Relay Break Time	04	84	1	4, 5
	Handshake Abort Counter	05	85	1	4, 5
	Handshake Abort Timer	06	86	1	2, 3
	CTS Off-Time	07	87	1	2, 3

NOTE: 1. All the chip 1 access codes are not valid before R5312-13.
2. Access codes are hexadecimal.
3. Only chip 1 RAM can be written.
4. CTS Off-Time is not valid before R5312-16.

ERROR RATES

Bit error rate (BER) is a measure of the throughput of data on the communication channel. It is the ratio of the number of received bits in error to the number of transmitted bits. This number increases with decreasing signal-to-noise ratio (SNR). The type of line disturbance and the modem configuration affect the BER.

Tables 14 through 16 summarize the BERs for various conditions. Figure 12 shows the BER measurement setup.

Table 14. BER Summary

R1212		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
1200 bps	1×10^{-5}	8.2 dB	7.9 dB
600 bps	1×10^{-5}	5.0 dB	5.0 dB
300 bps	1×10^{-5}	9.2 dB	7.0 dB

Test Condition: Signal Level = −30 dBm,
Sync for 1200 bps, 600 bps,
Async for 300 bps,
With 3002 Unconditioned Line.

Table 15. BER Summary

R1212		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
1200 bps	1×10^{-5}	8.3 dB	8.1 dB
600 bps	1×10^{-5}	5.0 dB	5.0 dB
300 bps	1×10^{-5}	10.4 dB	7.2 dB

Test Condition: Signal Level = −43 dBm,
Sync for 1200 bps, 600 bps,
Async for 300 bps,
With 3002 Unconditioned Line.

Table 16. BER Summary

R1212		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
1200 bps	1×10^{-5}	7.7 dB	7.9 dB
600 bps	1×10^{-5}	4.6 dB	4.5 dB
300 bps	1×10^{-5}	9.3 dB	6.2 dB

Test Condition: Signal Level = −40 dBm,
Sync for 1200 bps, 600 bps,
Async for 300 bps,
Back-To-Back.

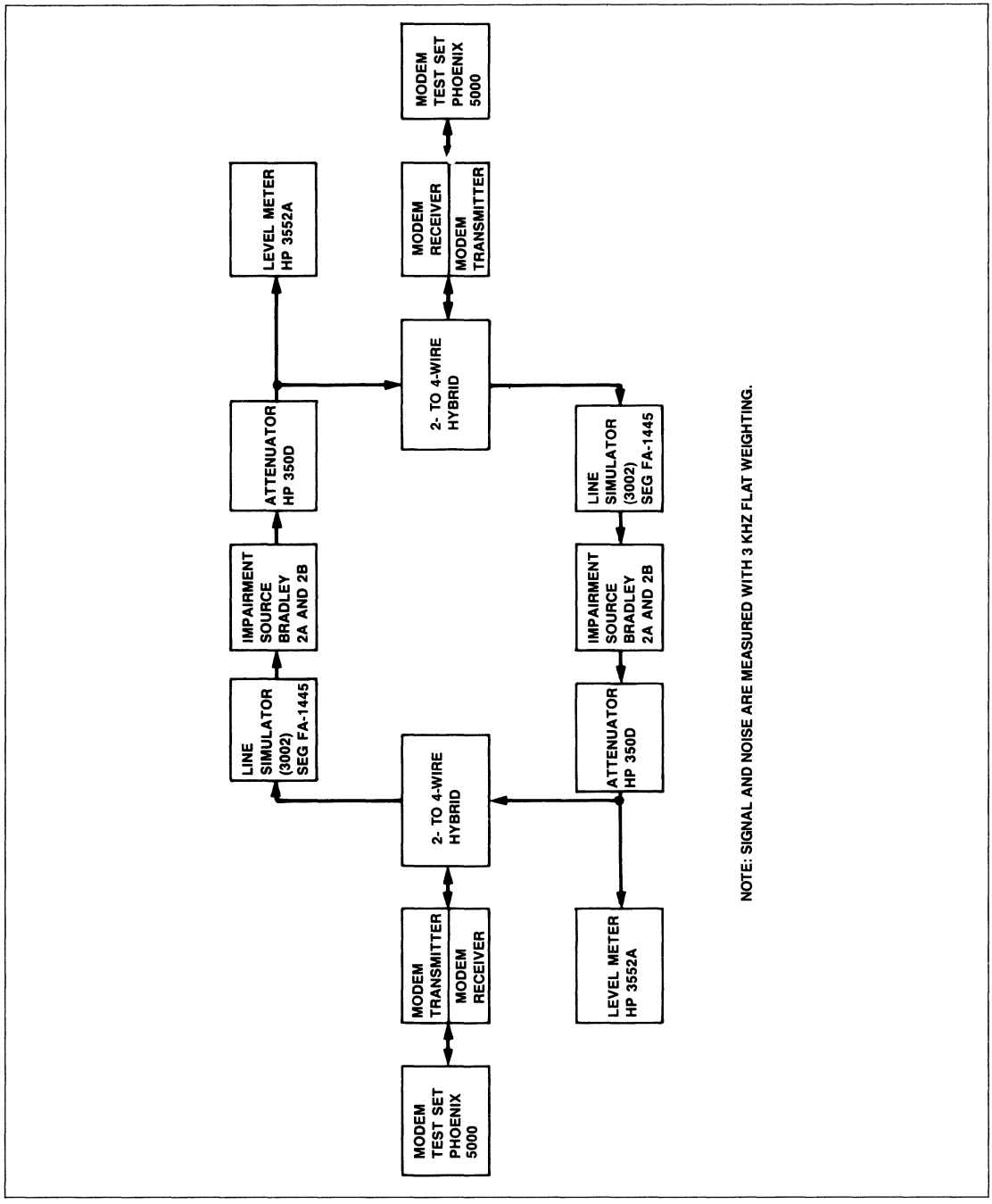


Figure 12. 2-Wire Full-Duplex Bit Error Rate Performance Test Setup (Bidirectional)

Table 17. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	390 mA	<455 mA
+12 Vdc	±5%	25 mA	< 30 mA
−12 Vdc	±5%	4 mA	< 5 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Table 18. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 19. Modem Mechanical Considerations

Parameter	Specification
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
PCB Dimensions:	
DC Version	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Height	0.75 in. (19 mm)
M Version	
Width	3.937 in. (100 mm)
Length	3.328 in. (82 mm)
Height	0.40 in. (10.2 mm)
Weight (max):	0.45 lbs. (0.20 kg.)
Lead Extrusion (max.):	0.100 in. (2.54 mm)

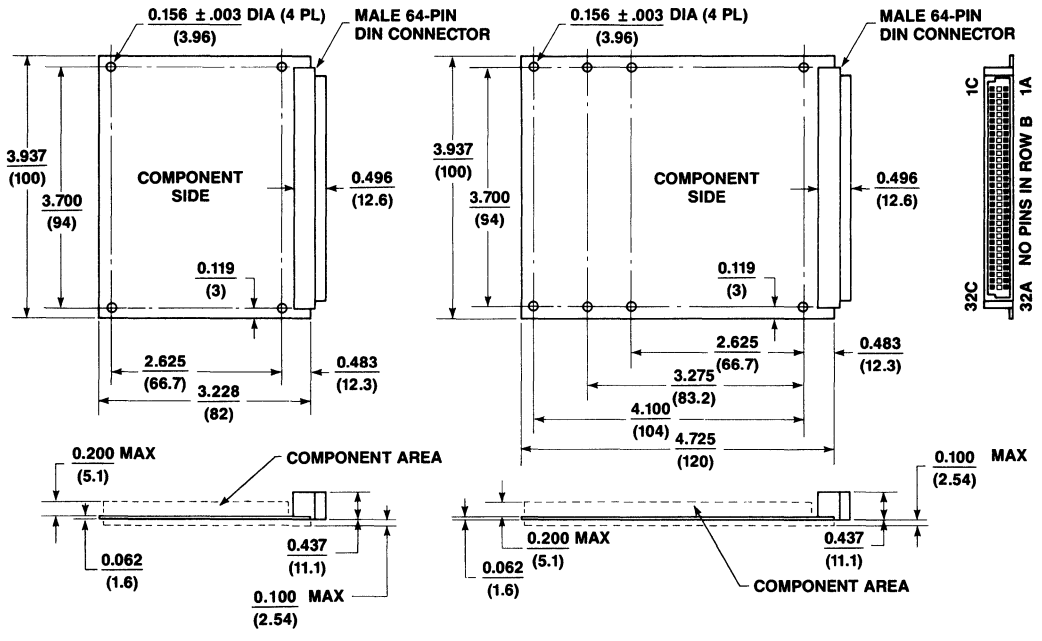


Figure 13. Modem Printed Circuit Board Dimensions

R1212 MODEM INSTALLATION AND MAINTENANCE

This section contains installation instructions and maintenance procedures for the Rockwell R1212DC Modem. It also contains a special notice from the Canadian Department of Communications (DOC) for Canadian operation and from the Federal Communications Commission (FCC) for United States operation.

GENERAL DESCRIPTION

The Rockwell R1212DC modem is designed to be used with the United States or Canadian Telephone Switched Networks in 2-wire full-duplex dial-up operation. The modem requires protective circuitry registered with the Federal Communications Commission (FCC) Part 68 which allows direct connection to the U.S. switched telephone network. This circuitry also complies with the Canadian Department of Communications (DOC) Terminal Attachment Program (TAP) which similarly defines their switched telephone network requirements.

The R1212DC features automatic dial and answer capabilities along with surge suppression and hazardous voltage and longitudinal balance protection. Its maximum output signal level at the telephone interface is set at -10 dBm ± 1 dBm (permissive mode of operation).

Two standard telephone jack connectors (RJ11s) are mounted side by side on one edge of the board and are wired in parallel. One is for connection to the telephone line network and the other for the telephone headset connection.

INSTALLATION AND SIGNAL ROUTING INSTRUCTIONS

PHYSICAL MOUNTING

The modem module may be physically incorporated into the customer's end product by utilizing the four corner 0.156" diameter mounting holes (for the self-hooking plastic type standoffs or for bolting it down to some rigid structure) or by installing the module into card guides.

ELECTRICAL INTERFACING INSTRUCTIONS

The electrical interfacing is accomplished via the DIN (Euro) connector (for external power inputs and digital logic signals) and the telco connectors (for the telephone network connection). Note that the telephone interface connectors are physically separated from the modem interface control connector and extreme care must be taken in routing the telephone interface leads from the modem to the telephone network (line connector jack in the wall).

FCC RULES PART 68 REQUIREMENTS

The FCC Rules Part 68 requires that the telephone interface leads shall:

1. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use the same connector as leads or metallic paths connecting to power connections.

   Note

   Power connections are defined as the connections between commercial power and any transformer, power supply rectifier, converter or other circuitry associated with the modem. The connections of the interface pins (including the $+12$ Vdc, -12 Vdc and $+5$ Vdc) are not considered power connections.

2. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use adjacent pins on the same connector as metallic paths that lead to unregistered equipment, when specification details provided to the FCC do not show that the interface voltages are less than nonhazardous voltage source limits in Part 68.

   Note

   All the DIN connector interface voltages to the modem have been established as non-hazardous.

ROUTING OF TELEPHONE INTERFACE LINES

In routing the telephone interface leads from the modem telephone connector jacks to the telephone line network connection, the following precautions should be strongly considered for safety.

1. The telephone interface routing path should be as direct and as short as possible.
2. Any cable used in establishing this path should contain no signal leads other than the modem telephone interface leads.
3. Any connector used in establishing this path shall contain not commercial power source signal leads, and adjacent pins to the TIP and RING (T and R) pins in any such connector shall not be utilized by any signals other than those shown in this document.

MAINTENANCE PROCEDURE

Under the FCC Rules, no customer is authorized to repair modems. In the event of a Rockwell modem malfunctioning, return it for repair to an authorized ROCKWELL INTERNATIONAL distributor (if in Canada) or send it directly to the Semiconductor Products Division, Rockwell International Corporation, El Paso, Texas 79906.

SPECIAL INSTRUCTION TO USERS

If the Rockwell modem has been registered with the Federal Communications Commission (FCC), you must observe the following to comply with the FCC regulations:

A. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.

B. It is prohibited to connect the modem to pay telephones or party lines.

C. You are required to notify the local telephone company of the connection or disconnection of the modem, the FCC registration number, the ringer equivalence number, the particular line to which the connection is made and the telephone number to be associated with the jack.

Note

If the proper jacks are not available, you must order the proper type of jacks to be installed by the telephone company (VSOC RJ11 for permissive mode of operation).

D. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only if it can be determined that the telephone line and not the modem is the source of trouble. If the Rockwell modem needs repair, return it to the ROCKWELL INTERNATIONAL CORPORATION. This applies to the modem whether it is in or out of warranty. Do not attempt to repair the unit as this is a violation of the FCC rules and may cause danger to persons or to the telephone network.

TELEPHONE COMPANY RIGHTS AND RESPONSIBILITIES

A. The Rockwell modem contains protective circuitry to prevent harmful voltages to be transmitted to the telephone network. If such harmful voltages do occur, then the telephone company may temporarily discontinue service to you. In this case, the telephone company should:

1. Promptly notify you of the discontinuance.
2. Afford you the opportunity to correct the situation which caused the discontinuance.
3. Inform you of your right to bring a complaint to the FCC concerning the discontinuance.

B. The telephone company may make changes in its facilities and services which may affect the operation of your equipment. It is, however, the telephone company's responsibility to give you adequate notice in writing to allow you to maintain uninterrupted service.

LABELING REQUIREMENTS

A. The FCC requires that the following label be prominently displayed on the outside surface of the customer's end product and that the size of the label should be such that all the required information is legible without magnification.

Sample label below:

Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.

FCC Registration Number: AMQ9SQ-14211-DM-E

Ringer Equivalence: 0.9B

Note

The Rockwell modem module has the FCC registration number and ringer equivalence number permanently affixed to the solder side of the PCB and any unit containing this modem shall use this information for the label requirements.

SPECIAL NOTICE FROM THE CANADIAN DEPARTMENT OF COMMUNICATIONS

The Canadian Department of Communications label identifies certified equipment. This certification means that the equipment meets certain telecommunications network protective, operational and safety requirements. The Department does not guarantee the equipment will operate to the user's satisfaction.

Before installing this equipment, users should insure that it is permissible to be connected to the facilities of the local telecommunications company. The equipment must also be installed using an approved method of connection. In some cases, the company's inside wiring associated with a single line individual service may be extended by means of a certified jack-plug-cord ensemble (telephone extension cord). The customer should be aware that the compliance with the above conditions may not prevent degradation of service in some situations. Existing telecommunications company requirements do not permit their equipment to be connected to customer-provided jacks except where specified by individual telecommunications company tariffs.

The Department of Communications requires the Certificate Holders to identify the method of network connection in the user literature provided with the certified terminal equipment.

Repairs to certified equipment should be made by an authorized Canadian maintenance facility designated by the supplier. Any repairs or alterations made by the user to this equipment, or equipment malfunctions may give the telecommunications company cause to request the user to disconnect the equipment.

Users should ensure for their own protection that the electrical ground connections of the power utility, telephone lines and internal metallic water pipe system, if present, are connected together. This precaution may be particularly important in rural areas.

CAUTION

Users should not attempt to make such connections themselves, but should contact the appropriate electric inspection authority, or electrician, as appropriate.

Rockwell

R2424
2400 bps Full-Duplex Modem

INTRODUCTION

The Rockwell R2424 is a high performance full-duplex 2400 bps modem. Using state-of-the-art VLSI and signal processing technology, the R2424 provides enhanced performance and reliability. The modem is assembled as a small module with a DIN connector (R2424M and R2424DC) or a new, smaller module (seven square inches) with a dual-in-line pin (DIP) interface.

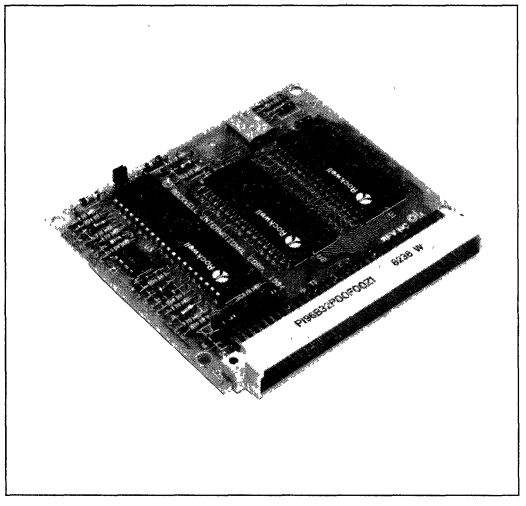
Being CCITT V.22 bis, V.22 A, B compatible, as well as Bell 212A and 103 compatible, the R2424 fits most applications for full-duplex 2400 and 1200 bps fallback (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network, and over point-to-point leased lines.

The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other microprocessor-based communications product.

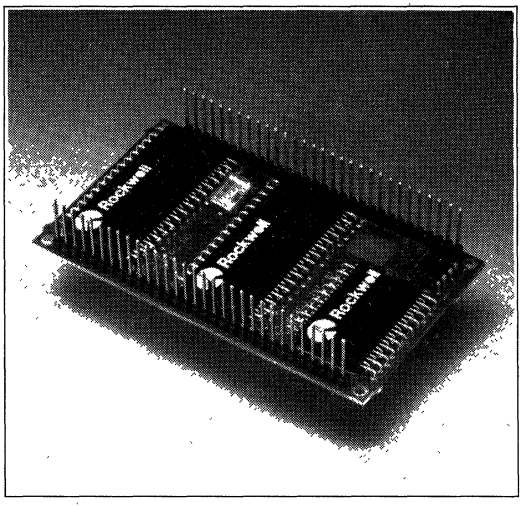
The R2424DM, with its small form factor and DIP connection, can be automatically installed and soldered onto a host module. Its small size is ideal for internal "1/2-card" PC modem applications.

FEATURES

- CCITT V.22 bis, V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 2400 bps, 1200 bps, 600 bps ±0.01%
- Asynchronous: 2400 bps, 1200 bps, 600 bps +1%, −2.5%, 0–300 bps
  - — Character Length 8, 9, 10, or 11 bits
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL Compatible
- 2-wire Full-Duplex Operation
- Adaptive and Fixed Compromize Equalization
- Test Configurations:
  - — Local Analog Loopback
  - — Remote Digital Loopback
  - — Self Test
- Auto/Manual Answer
- Auto/Manual Dial—DTMF Tone or Pulse Dial
- Power Consumption: 2.3 Watts Typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Three Module Configurations:
  - — R2424DC (Direct Connect): DIN connector module with FCC approved DAA Part 68 Interface
  - — R2424M: DIN connector module without DAA
  - — R2424DM: DIP connection module without DAA
- Two Functional Versions
  - — R2424/US All data rates specified except 600 bps
  - — R2424/INT All data rates specified except 0–300 bps



R2424M Modem



R2424DM Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

The transmitter and signaling frequencies supported in the R2424 are listed in Table 1.

Table 1. Transmitter Carrier and Signaling Frequencies Specifications

Mode	Frequency (Hz ±0.01%)
V.22 bis low channel, Originate Mode	1200
V.22 low channel, Originate Mode	1200
V.22 bis high channel, Answer Mode	2400
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

TONE GENERATION

The specifications for tone generation are as follows:

1. **Answer Tones:** The R2424 generates echo disabling tones for both the CCITT and Bell configurations, as follows:
   a. CCITT: 2100 Hz ±15 Hz.
   b. Bell: 2225 Hz ±10 Hz.
2. **Guard Tones:** If GTS (see Interface Memory Definitions) is low, an 1800 Hz guard tone frequency is selected; if GTS is high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone is 6 ±1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power is 3 ±1 dB below the level of the main channel power, and again the overall power transmitted to the line will remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.
3. **DTMF Tones:** The R2424 generates dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits (see Interface Memory Definitions)must be set to a 1. When in this mode, the specific DTMF tones generated are decided by loading the dial digit register with the appropriate digit as shown in Table 2.

Table 2. Dial Digits/Tone Pairs

Hex	Dial Digits	Tone Pairs	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	★	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

TONE DETECTION

The R2424 detects tones in the 340 ±5 Hz to 640 ±5 Hz band.
Detection Level: −10 dBm to −43 dBm
Response Time: 17 ±2 ms

SIGNALING AND DATA RATES

The signaling and data rates for the R2424 are defined in Table 3.

Table 3. Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22 bis:	600	Synchronous/Asynchronous, 2400 bps ±0.01%
V.22 bis:	600	Synchronous/Asynchronous, 1200 bps ±0.01%
V.22:		
(Alternative A)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
(Alternative B)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
Mode ii		1200 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character
Mode iv		600 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character
Bell 212A;	600 0 to 300	1200 bps ±0.01%, Synchronous/Asynchronous 0 to 300 bps Asynchronous

DATA ENCODING

The specifications for data encoding are as follows:

1. *2400 bps (V.22 bis).* The transmitted data is divided into groups of four consecutive bits (quad bits) forming a 16-point signal structure.
2. *1200 bps (V.22 and Bell 212A).* The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
3. *600 bps (V.22).* Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R2424 provides equalization functions that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—A fixed compromise equalizer is provided in the transmitter.

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ±150 microseconds over the frequency range 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R2424 incorporates a self-synchronizing scrambler-/descrambler. In accordance with the CCITT V.22 bis, V.22 and the Bell 212A recommendations.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R2424 can adapt to received frequency errors of up to ±7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R2424 satisfies all specified performance requirements for the received line signals from −10 dBm to −48 dBm. The received line signal is measured at the receiver analog input RXA.

TRANSMIT LEVEL

The R2424M, R2424DM and R2424DC output control circuitry contains a variable gain buffer which reduces the modem output level. All three R2424 modems can be strapped via the host interface memory to accomplish this.

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R2424M transmit level is +6 dBm to allow a Data Access Arrangement (DAA) to be used. The R2424DM transmit level is 0 dBm ±1.0 dBm. The DAA then determines the permissive or programmable configuration.

The R2424DC transmit level is strapped in the permissive mode so that the maximum output level is −10 dBm ±1.0 dBm.

AUTOMATIC SPEED RECOGNITION

The R2424 is capable of automatically configuring itself to the compatibility of a remote modem. The R2424 can be in either the answer or originate mode for this to occur. The compatibilities that the R2424 are limited to adapt to are V.22 bis, V.22 A/B (1200 bps), Bell 212, and Bell 103. If the R2424 is to originate in a specific configuration, the MODE bits (see Interface Memory Definitions)must be set.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, DAA signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The column titled "Type" refers to designations found in the Hardware Circuits Interface Characteristics (Tables 5 and 6). The six groups of hardware circuits are described in the following paragraphs.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 350 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 μs. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 350 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 350 ms to complete. The R2424 POR sequence leaves the modem configured as follows:

- 2400 bps
- Asynchronous
- 10-bit Character Length
- Constant Carrier
- Serial Control Mode
- Answer Mode
- Auto Answer Disabled
- RAM Access Code = 00

This configuration is suitable for performing high speed data transfer over the public switched telephone network using the serial data port. Individual features are discussed in subsequent paragraphs.

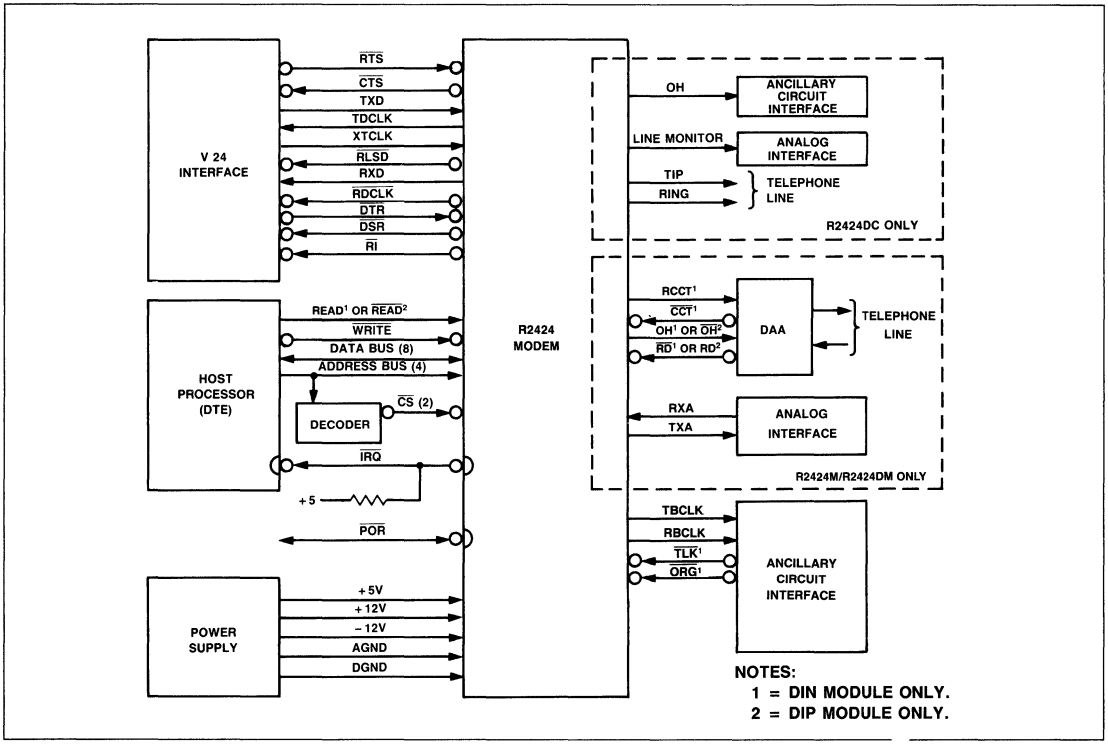


Figure 1. R2424 Modem Functional Interconnect Diagram

Table 4. Hardware Circuits

Name	Type	DIN Pin No.	DIP* Pin No.	Description
A. OVERHEAD SIGNALS				
Ground (A)	AGND	31C, 32C	23, 39	Analog Ground Return
Ground (D)	DGND	3C, 8C, 5A, 10A	22, 40, 51, 60	Digital Ground Return
+5 volts	PWR	19C, 23C, 26C, 30C	1, 21, 61	+5 volt supply
+12 volts	PWR	15A	24	+12 volt supply
−12 volts	PWR	12A	27	−12 volt supply
$\overline{POR}$	I/OB	13C	15	Power-on-Reset
B. MICROPROCESSOR INTERFACE SIGNALS				
D7	I/OA	1C	52	Data Bus (8-Lines)*
D6	I/OA	1A	53	
D5	I/OA	2C	54	
D4	I/OA	2A	55	
D3	I/OA	3A	56	
D2	I/OA	4C	57	
D1	I/OA	4A	58	
D0	I/OA	5C	59	
RS3	IA	6C	45	Register Select (4-Lines)
RS2	IA	6A	44	
RS1	IA	7C	43	
RS0	IA	7A	42	
$\overline{CS0}$	IA	10C	48	Chip Select Receiver (Baud Rate Device)
$\overline{CS1}$	IA	9C	41	Chip Select Transmitter (Sample Rate Device)
READ	IA	12C	—	Read Enable
$\overline{READ}$	IA	—	47	Read Enable
$\overline{WRITE}$	IA	11A	49	Write Enable
$\overline{IRQ}$	OB	11C	50	Interrupt Request

***Note:** The R2424DM is only used in parallel control mode. Thus, the Bus Select bits must be set to a 1 when using the R2424DM.

Name	Type	DIN Pin No.	DIP Pin No.	Description
C. V.24 INTERFACE SIGNALS				
XTCLK	IB	22A	2	External Transmit Clock
TDCLK	OC	23A	7	Transmit Data Clock
$\overline{RDCLK}$	OC	21A	8	Receive Data Clock
$\overline{RTS}$	IB	25A	—	Request-to-Send
$\overline{CTS}$	OC	25C	4	Clear-to-Send
TXD	IB	24C	5	Transmit Data
RXD	OC	22C	10	Receive Data
$\overline{RLSD}$	OC	24A	11	Received Line Signal Detector
$\overline{DTR}$	IB	21C	—	Data Terminal Ready
$\overline{DSR}$	OC	20A	13	Data Set Ready
$\overline{RI}$	OC	18A	14	Ring Indicator
D ANALOG SIGNALS				
RXA (M/DM)	IB	32A	25	Receive Analog Input
TXA (M/DM)	OC	31A	26	Transmit Analog Output
TIP/RING (DC) LINE	AE	RJ11 Jacks	—	Phone Line Interface
MONITOR (DC)	AD	30A	—	Analog Line Monitor
E. DAA INTERFACE SIGNALS				
$\overline{RD}$ (M)	IB	27A	—	Ring Detect
RD (DM)	IB	—	35	Ring Detect
RCCT (M)	OC	28A	—	Request Coupler Cut Through
$\overline{CCT}$ (M)	IB	29C	—	Coupler Cut Through
OH	OC	29A	—	Off-Hook Relay Status
$\overline{OH}$	OC	—	36	Off-Hook Relay Status
F. ANCILLARY INTERFACE SIGNALS				
TBCLK	OC	27C	6	Transmit Baud Clock
RBCLK	OC	26A	9	Receive Baud Clock
$\overline{TLK}$	IC	28C	—	Talk (TLK = Data)
$\overline{ORG}$	IB	16C	—	Originate (ORG = Answer)

(M) R2424M only. (DC) R2424DC only. — = not applicable
(DM) R2424DM only.
Unused inputs tied to +5V or ground require individual 10K Ω series resistors

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Ouput Type IA	IB	IC	OA	OB	OC	I/O A	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min.				2.0 min.	5.25 max.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	2.0 min. 0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[2]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2 5 max.						±2.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes: 1. I load = −100 μA 2. I load = 1.6 mA 3 I load = −40 μA 4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5 25 Vdc 5. I load = 0.36 mA

Table 6. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604Ω ±1% with an output level of +6 dBm. To obtain a 0 dBm output, a 600Ω load to ground is needed.
RXA	AB	The receiver input impedance is 23.7 KΩ ±1%. The receive level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).
LINE MONITOR	AD	The line monitor output impedance is 15 KΩ ±5%.
TIP/RING	AE	The impedance of TIP with respect to RING is 600 Ω.

V.24 INTERFACE

Eleven hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, +5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Data Terminal Ready ($\overline{DTR}$)

$\overline{DTR}$ prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. $\overline{DTR}$ OFF places the modem in the disconnect state.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) ON indicates that the modem is in the data transfer state. $\overline{DSR}$ OFF is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except $\overline{RI}$. $\overline{DSR}$ will switch to the OFF state when in test state. The ON condition of $\overline{DSR}$ indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.
4. After ring indicate ($\overline{RI}$) goes ON, $\overline{DSR}$ waits at least two seconds before turning ON to allow the telephone company equipment to be engaged.

$\overline{DSR}$ will go OFF 50 ms after $\overline{DTR}$ goes OFF, or 50 ms plus a maximum of 4 seconds when the SSD bit is enabled.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. In constant carrier mode, $\overline{RTS}$ can be wired to $\overline{DTR}$. In controlled carrier operation, independent operation of $\overline{RTS}$ turns the carrier ON and OFF. The responses to $\overline{RTS}$ are shown in Table 7 (assume the modem is in data mode).

Table 7. $\overline{RTS}$ Responses

Leased or Dial Line[1]	$\overline{RTS}$ OFF	$\overline{RTS}$ ON
Controlled Carrier	$\overline{CTS}$ OFF Carrier OFF	Carrier ON 210 to 275 ms Scrambled 1s Transmitted $\overline{CTS}$ ON
Constant Carrier	$\overline{CTS}$ OFF Carrier ON Scrambled 1s Transmitted	$\overline{CTS}$ ON Carrier ON Data Transmitted

Note:
1. After handshake is complete.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which is present on TXD. $\overline{CTS}$ response times from an ON or OFF condition of $\overline{RTS}$ are shown in Table 8.

Table 8. $\overline{CTS}$ Response Times

$\overline{CTS}$ Transition	Constant Carrier	Controlled Carrier
OFF to ON	<2 ms	210 to 275 ms
ON to OFF	<20 ms*	<20 ms*

Note: *Programmable

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency*. Selected data rate of 2400 Hz, 1200 Hz or 600 Hz (±0.01%).
2. *Duty Cycle*. 50 ±1%.

TDCLK is provided to the user in both asynchronous and synchronous communications. TDCLK is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing (TDCLK is not valid in FSK). TDCLK is necessary for synchronous communication. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{\text{RDCLK}}$)

The modem provides a Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±.035% (relative) frequency error in the associated transmit timing source.

$\overline{\text{RDCLK}}$ is provided to the user in both asynchronous and synchronous communications. $\overline{\text{RDCLK}}$ is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing ($\overline{\text{RDCLK}}$ is not valid in FSK). $\overline{\text{RDCLK}}$ is necessary for synchronous communication.

Received Line Signal Detector ($\overline{\text{RLSD}}$)

The $\overline{\text{RLSD}}$ thresholds for both high and low channels are:

$\overline{\text{RLSD}}$ ON ≥ -43 dBm
$\overline{\text{RLSD}}$ OFF ≤ -48 dBm

$\overline{\text{RLSD}}$ will not respond to guard tones or answer tones.

When $\overline{\text{RLSD}}$ is active, it indicates to the terminal equipment that valid data is available on RXD.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Ring Indicator ($\overline{\text{RI}}$)

The modem provides a Ring Indicator ($\overline{\text{RI}}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the ON segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The high condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received. The operation of $\overline{\text{RI}}$ is not disabled by an OFF condition on $\overline{\text{DTR}}$.

$\overline{\text{RI}}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across TIP and RING), with the response times given in Table 13.

This OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent ON (OFF) transition of $\overline{\text{RI}}$.

Table 9. $\overline{\text{RI}}$ Response Time

$\overline{\text{RI}}$ Transition	Response Time
OFF-to-ON*	110 ±50 ms (50% duty cycle)
ON-to-OFF	450 ±50 ms
Note: *The OFF-to-ON time is duty cycle dependent: 890 ms (15%) ≥ time ≥ 50 ms (100%)	

MICROPROCESSOR INTERFACE

Seventeen hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$ and $\overline{CS1}$) and Register Selects (RS0-RS1)

The signal processor to be accessed is selected by grounding one of two unique chip select lines, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ input high (R2424M) or $\overline{READ}$ input low (R2424DM), or the $\overline{WRITE}$ input low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ/$\overline{READ}$ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to + 5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

DAA INTERFACE (R2424M)

The R2424M provides a Data Access Arrangement (DAA) interace that is directly hardware and software compatible with the RDAA. Manual/automatic originate and answer are then controlled via the appropriate R2424M hardware ancillary circuits or software control bits. The modem provides the only interface with the microprocessor (MPU) bus, i.e., no RDAA interface signals must be directly controlled from the MPU bus.

Ring Detect ($\overline{RD}$)

$\overline{RD}$ low indicates to the modem by an ON condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the $\overline{RD}$ input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on $\overline{RI}$.

Request Coupler Cut Through (RCCT)

RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes OFF (low), the cut-through buffers are disabled and $\overline{CCT}$ should go OFF (high). RCCT should be OFF during dialing but ON for tone address signaling.

Coupler Cut Through ($\overline{CCT}$)

An ON (low) signal to the $\overline{CCT}$ lead indicates to the modem that the data transmission path through the DAA is connected. This input can always be grounded if the two second billing delay squelch is desired. If $\overline{CCT}$ is user controlled, the billing delay squelch can only be 2 seconds or greater.

Off-Hook Relay Status (OH)

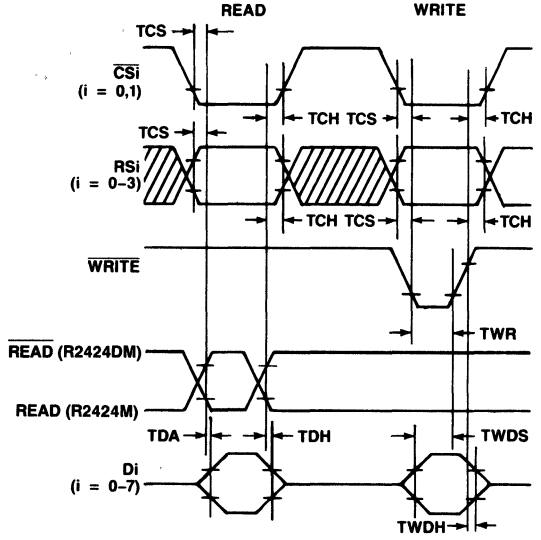
The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

DAA INTERFACE (R2424DM)

The R2424DM provides the following DAA interface signals: RD, $\overline{OH}$, TXA and RXA. Manual/automatic originate and answer are controlled via appropriate software control bits.

Ring Detect (RD)

RD indicates to the modem by an ON (high) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the RD input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than



Characteristic	Symbol	Min	Max	Units
CSi, RSi setup time prior to Read or Write	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
CSi, RSi hold time after Read/Read or Write	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

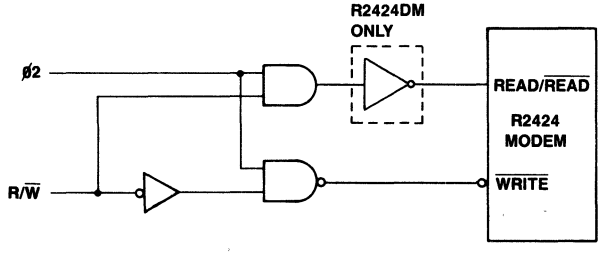


Figure 3. R/W to READ WRITE Conversion Logic

40 Vrms, 15 to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on RI.

Off-Hook Relay Status ($\overline{OH}$)

The modem provides an $\overline{OH}$ output which indicates the state of the Off-Hook relay. A low condition on $\overline{OH}$ implies the Off-Hook relay is closed and the modem is connected to the telephone line (off-hook). A high condition on $\overline{OH}$ implies the Off-Hook relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of $\overline{OH}$ and the subsequent close-to-open or open-to-close transition of the Off-Hook relay is 8 ms maximum.

ANALOG SIGNALS (R2424M/R2424DM)

Two connections are devoted to analog audio signals: TXA and RXA.

Transmit Analog (TXA)

The R2424M TXA output is suitable for driving a data access arrangement for connection to either leased lines or the public switched telephone network. The transmitter output impedance is 604 ohms ±1% with an output level of +6 dBm ±1 dBm. To obtain a 0 dBm output, a 600 ohm load to ground is needed.

The R2424DM TXA output is an op amp output at 0 dBm ±1 dBm.

Receive Analog (RXA)

RXA is an input to the receiver from a data access arrangement. The input impedance is 23.7K ohms ±1%. The received level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).

ANALOG SIGNALS (R2424DC)

Three analog signals are output by the R2424DC: LINE MONITOR, TIP and RING.

Analog Line Monitor (LINE MONITOR)

The LINE MONITOR output is suitable for a speaker interface. It provides an output for all dialing signals, call progress signals, and the carrier signals. The output impedance is 15K ohms ±1%. The signals which appear on LINE MONITOR are approximately the same level as the signals would appear on the network (assuming a 1 dB loss attributed to the audio transformer).

Phone Line Interface (TIP and RING)

TIP and RING are the DAA analog outputs to the public switched telephone network. These outputs use two RJ11 jacks in parallel as the interface to the network (see Table 10 and Figure 4). The R2424DC, which contains the DAA TIP and RING interface, has been FCC Part 68 approved. The user need not apply for further Part 68 approval. The impedance of TIP with respect to RING is 600 ohms.

Table 10. R2424DC Network Interface

Connector Type	Pin Number	Name	Function
RJ11 Jack	3	RING	One Side of TELCO Line
	4	TIP	One Side of TELCO Line

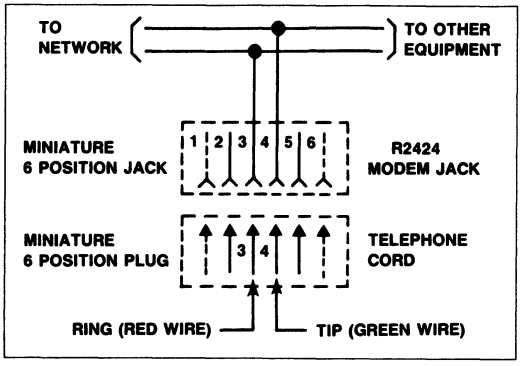


Figure 4. RJ11 Telephone Jack

ANCILLARY CIRCUITS

Transmit Baud Clock (TBCLK) and Received Baud Clock (RBCLK)

TBCLK and RBCLK are provided to the user at the baud rate (600 Hz).

Talk ($\overline{TLK}$) (DIN Module Only)

$\overline{TLK}$ is an input which manually places the modem on-hook (relay open, $\overline{TLK}$ = 0) or off-hook (relay closed, $\overline{TLK}$ = 1). The on-hook condition is referred to as TALK mode and the off-hook condition is referred to as DATA mode. $\overline{TLK}$ is used with $\overline{ORG}$ to manually originate or answer a call. $\overline{TLK}$ should be 0 at power-on or reset to prevent the modem from inadvertently entering the data mode. $\overline{TLK}$ is not provided on the R2424DM.

Originate ($\overline{ORG}$) (DIN Module Only)

$\overline{ORG}$ is an input which manually places the modem in the originate mode ($\overline{ORG}$ = 0) or the answer mode ($\overline{ORG}$ = 1). To manually originate a call, $\overline{ORG}$ = 0 and $\overline{TLK}$ = 0. Dial the number using the telephone. When the other modem answers and sends answer tone switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

To manually answer a call $\overline{ORG}$ = 1 and $\overline{TLK}$ = 0. When the phone rings switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook. $\overline{ORG}$ is not provided on the R2424DM.

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load-/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on two special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into two areas. These areas are partitioned into receiver and transmitter devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 32 addressable registers in the modem receiver ($\overline{CS0}$) and transmitter ($\overline{CS1}$) interface memory are shown in Figures 5 and 6, respectively. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Figures 7 and 8 show the registers according to the overall function they perform in the receiver and transmitter, respectively. Figures 9 through 12 show the power on configurations of the interface memory bits for the R2424/US and the R2424/INT versions.

Table 11 defines the individual bits in the interface memory. In the Table 11 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R							
E	IRQ	ENSI	NEWS	—	NEWC	—	—	—
D	BUS	CRQ	—	—	—	LCD	RSD	—
C	—	—	—	CHAR		—	—	—
B	—	—	—	—	—	—	—	AL
A	ERDL	RDL	DL	ST	MODE			
9	—	—	SPEED		—	—	—	—
8	TONE	ATD	—	—	—	—	TM	RLSD
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (YRAMRM)							
4	RAM Data YRL (YRAMRL)							
3	RAM Data XRM (XRAMRM)							
2	RAM Data XRL (XRAMRL)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—

Note
(—) Indicates reserved for modem use only.

Figure 5. Receiver ($\overline{CS0}$) Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T							
E	IRQ	ENSI	NEWS	—	NEWC	DDEI	—	DDRE
D	BUS	CRQ	DATA	AAE	DTR	—	—	SSD
C	DSRA	TXCLK		CHAR		—	—	DLSF[1]
B	TX LEVEL			GTE	GTS	3DB	DTMF	AL
A	ERDL	RDL	DL	ST	MODE			
9	NAT[1]	RTRN	ORG	LL	RTS	CC	EF	NTS
8	DLO	CTS	DSR	RI	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (YRAMTM)							
4	RAM Data YTL (YRAMTL)							
3	RAM Data XTM (XRAMTM)							
2	RAM Data XTL (XRAMTL)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register							

Notes
1. Not valid before R5310-22
(—) Indicates reserved for modem use only.

Figure 6. Transmitter ($\overline{CS1}$) Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	DIAGNOSTIC CONTROL							
E	HANDSHAKE							
D	CONFIGURATION							
C	CONFIGURATION							
B	CONFIGURATION							
A	CONFIGURATION							
9	STATUS							
8	STATUS							
7	RESERVED							
6	RESERVED							
5	DIAGNOSTIC							
4	DIAGNOSTIC							
3	DIAGNOSTIC							
2	DIAGNOSTIC							
1	RESERVED							
0	RESERVED							
Register \ Bit	7	6	5	4	3	2	1	0

Figure 7. Receiver ($\overline{CS0}$) Interface Memory Functions

Register \ Bit	7	6	5	4	3	2	1	0
F	DIAGNOSTIC CONTROL							
E	HANDSHAKE							
D	CONFIGURATION							
C	CONFIGURATION							
B	CONFIGURATION							
A	CONFIGURATION							
9	CONFIGURATION							
8	STATUS							
7	RESERVED							
6	RESERVED							
5	DIAGNOSTIC							
4	DIAGNOSTIC							
3	DIAGNOSTIC							
2	DIAGNOSTIC							
1	RESERVED							
0	DIAL DIGIT REGISTER							
Register \ Bit	7	6	5	4	3	2	1	0

Figure 8. Transmitter ($\overline{CS1}$) Interface Memory Functions

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	—	—	—
D	BUS 0	CRQ 0	—	—	—	LCD 1	RSD 0	—
C	—	—	—	CHAR 1	0	—	—	—
B	—	—	—	—	—	—	—	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	0	MODE 0	0	1
9	—	—	SPEED 0	0	—	—	—	—
8	TONE 0	ATD 0	—	—	—	—	TM 0	RLSD 0
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (Random)							
4	RAM Data YRL (Random)							
3	RAM Data XRM (Random)							
2	RAM Data XRL (Random)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 9. R2424/US Receiver ($\overline{CS0}$) Interface Memory Power On Configuration

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	DDEI 0	—	DDRE 0
D	BUS 0	CRQ 0	DATA 0	AAE 0	DTR 0	—	—	SSD 0
C	DSRA 0	TX CLK 0	0	CHAR 1	0	—	—	DLSF 0
B	TX LEVEL 0	0	0	GTE 0	GTS 0	3DB 0	DTMF 0	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	MODE 1	1	0	1
9	NAT 0	RTRN 0	ORG 0	LL 0	RTS 0	CC 0	EF 0	NTS 0
8	DLO 0	CTS 0	DSR 0	RI 0	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (Random)							
4	RAM Data YTL (Random)							
3	RAM Data XTM (Random)							
2	RAM Data XTL (Random)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register (Write-Only Register)							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 10. R2424/US Transmitter ($\overline{CS1}$) Interface Memory Power On Configuration

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	—	—	—
D	BUS 0	CRQ 0	—	—	—	LCD 1	RSD 0	—
C	—	—	—	CHAR 1	0	—	—	—
B	—	—	—	—	—	—	—	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	1	MODE 1	0	1
9	—	—	SPEED 0	0	—	—	—	—
8	TONE 0	ATD 0	—	—	—	—	TM 0	RLSD 0
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (Random)							
4	RAM Data YRL (Random)							
3	RAM Data XRM (Random)							
2	RAM Data XRL (Random)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 11. R2424/INT Receiver ($\overline{CS0}$) Interface Memory Power On Configuration

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	DDEI 0	—	DDRE 0
D	BUS 0	CRQ 0	DATA 0	AAE 0	DTR 0	—	—	SSD 0
C	DSRA 0	TX CLK 0	0	CHAR 1	0	—	—	DLSF 0
B	TX LEVEL 0	0	0	GTE 0	GTS 0	3DB 0	DTMF 0	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	MODE 1	1	0	1
9	NAT 0	RTRN 0	ORG 0	LL 0	RTS 0	CC 0	EF 0	NTS 0
8	DLO 0	CTS 0	DSR 0	RI 0	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (Random)							
4	RAM Data YTL (Random)							
3	RAM Data XTM (Random)							
2	RAM Data XTL (Random)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register (Write-Only Register)							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 12. R2424/INT Transmitter ($\overline{CS1}$) Interface Memory Power On Configuration

Table 11. Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When configuration bit AAE is a 1, the modem will automatically answer when a ringing signal is present on the line. When AAE is set to a 1, the modem will answer after one ring and go into data mode. The modem goes off-hook 1 second after the on-to-off transition of the ring. The $\overline{ORG}$ pin or ORG bit need not to be set to the answer polarity. If it is desired to answer after more than one ring, then the user must use the alternative answer method described under the DATA bit. The $\overline{DTR}$ pin or the DTR bit must also be set before the modem will auto answer. Writing a 0 into the AAE bit will cause the modem to go on-hook. This will occur only when the modem auto answers using the AAE bit.
AL	Analog Loopback	(0,1):B:0	When configuration bits AL are a 1, the modem is in local analog loopback (V.54 Loop 3). In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14 ±1 dBm. The modem may be placed into analog loopback in either the idle mode or the data mode. However, in the data mode, setting the AL bits to a 1 will terminate the connection. Analog loopback will only function in the high speed modes (2400, 1200, or 600 bps). The DTE may be tested when the modem is in analog loopback. Also, all parts of the modem except the line interface are checked. If no DTE is connected, the modem integrity may be verified by use of the self test function. When entering analog loopback, set AL in the receiver to a 1 before setting AL in the transmitter to a 1. When exiting analog loopback, reset AL in the transmitter to a 0 before resetting AL in the receiver to a 0.
ATD	Answer Tone Detected	0:8:6	When status bit ATD is a 1, it signifies that the modem receiver detected the answer tone. The bit is 1 set 75 ms after the answer tone is first detected, and is cleared to a 0 when the modem goes on-hook. The user may clear ATD manually after CTS is active.
BUS	Bus Select	(0,1):D:7	When configuration bits BUS are a 1, the modem is in the parallel control mode; and when 0, the modem is in the serial control mode. BUS can be in either state to configure the modem. *Serial Control Mode* The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. The control signals used in serial control mode are $\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, and $\overline{ORG}$. Outputs such as $\overline{RLSD}$ and $\overline{DSR}$ are reflected both in the interface memory and the V.24 interface. Once the bus bits have been set to a 0, the state of the DTR, RTS, DATA, and ORG bits are ignored. *Parallel Control Mode** The modem has the capability of modem control via the microprocessor bus. Data transfer is maintained over the serial V.24 channel. The control bits used in parallel control are DTR, RTS, ORG, and DATA. The modem automatically defaults to the serial mode at power-on. If the parallel control mode is to be used, it is recommended that the $\overline{TLK}$ pin be tied to ground. A floating $\overline{TLK}$ pin will assume a logic 1 which will immediately put the modem into the data mode before the BUS bits are set. In either mode, the modem is configured by the host processor via the microprocessor bus. *The R2424DM is only used in the parallel control mode.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
CC	Controlled Carrier	1·9:2	When configuration bit CC is a 1, the modem operates in controlled carrier; when 0, the modem operates in constant carrier. Controlled carrier allows the modem transmitter to be controlled by the $\overline{RTS}$ pin or the RTS bit. Its effect may be seen in the RTS and CTS descriptions.
CHAR	Character Length Select	(0,1):C:(3,4)	These character length bits select either 8, 9, 10, or 11 bit characters (includes data, stop, and start bits) as shown below: **Configuration Word** (4 3) — **Configuration** 0 0 — 8 bits 0 1 — 9 bits 1 0 — 10 bits 1 1 — 11 bits It is possible to change character length during the data mode. Errors in the data will be expected between the changeover and the resynchronization (which occurs on the next start bit after the change is implemented).
CRQ	Call Request	(0,1):D:6	When configuration bit CRQ in chip 1 (the transmitter) is a 1, it places the transmitter in auto dial mode The data then placed in the Dial Digit Register is treated as digits to be dialed. The format for the data should be a hex representation of the number to be dialed (if a 9 is to be dialed then an 09_{16} should be loaded in DDR). CRQ in chip 1 should be a 1 for the duration of the data mode If CRQ in chip 1 is changed to a 0, the modem will go on-hook. Also, see DDRE bit. When configuration bit CRQ in chip 0 (the receiver) is a 1, the receiver goes into tone detect mode. Any energy above threshold and in the 345 to 635 Hz bandwidth is reflected by the TONE bit. CRQ in chip 0 must be reset to a 0 (after the last digit was dialed and tone detection completed) before the answer tone is sent by the answering modem (after ringback is detected). CRQ in chip 0 need not be used during auto dialing, but may be used to provide call progress information as part of an intelligent auto dialing routine. An example flowchart is given in Figure 13. FF (hex) should be loaded into the Dial Digit Register after the last digit is dialed and tone detection is completed. This action also puts the modem in data mode and starts a 30 second abort timer. If the handshake has not been completed in 30 seconds the modem will go on-hook.
CTS	Clear-to-Send	1:8:6	When status bit CTS is a 1, it indicates to the terminal equipment that the modem will transmit any data which are present at TXD. CTS response times from an ON or OFF condition of RTS are shown below: **CTS Transition** — **Constant Carrier** — **Controlled Carrier** OFF to ON — ≤2 ms — 210 to 275 ms ON to OFF — ≤20 ms* — ≤20 ms* *Programmable
DATA	Talk/Data	1:D:5	When control bit DATA is a 1, the modem is in the data state (off-hook); and when 0, the modem is in the talk state (on-hook). This bit allows the modem to go off-hook after a programmable number of rings by counting the required number of RI bit transitions and then setting the DATA bit (assuming ORG = 0).
DDEI	Dial Digit Empty Interrupt	1:E:2	When handshake bit DDEI is a 1, an interrupt will occur when the Dial Digit Register (1·0) is empty (DDRE = 1). This is independent of the state of the ENSI bit. The interrupt will set the IRQ bit and also assert the $\overline{IRQ}$ signal. Loading the Dial Digit Register with a new digit will clear the interrupt condition.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DDR	Dial Digit Register	1.0:(0–7)	DDR is used to load the digits to be dialed. Example: If a 4 is to be dialed, an 04 (hex) should be loaded. This action also causes the interrupt to be cleared The modem automatically accounts for the interdigit delay. Note: DDR is a write-only register.
DDRE	Dial Digit Register Empty	1:E:0	When handshake bit DDRE is a 1, it indicates that the dial digit register is empty and can be loaded with a new digit to be dialed. If the DDEI bit is set, the IRQ bit will be set when the DDRE bit is set. Also, the $\overline{IRQ}$ signal will be generated. After the DDR is loaded, DDRE goes to a 0 and the interrupts are automatically cleared.
DL	Digital Loopback (Manual)	(0,1).A:5	When configuration bits DL are set to a 1, the modem is manually placed in digital loopback. DL should only be set during the data mode. The DSR and CTS bits will be reset to a 0. The local modem can then be tested from the remote modem end by looping a remotely generated test pattern. At the remote modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be reset to a 0. The local modem will then return to the normal data mode with control reverting to the DTEs, DTR. DL does not function in 300 bps.
DLO	Dial Line Occupied	1·8:7	When status bit DLO is a 1, it indicates that the modem is in the auto dial state, i e., CRQ in the transmitter is a 1 and the modem is off-hook and ready to dial.
DLSF	Disable Low Speed Fallback	1:C·0	When configuration bit DLSF is a 1, the modem will not automatically fallback to the 300 bps operating mode if it is configured for another data rate. This bit is valid in originate mode only.
DSR	Data Set Ready	1:8:5	The ON condition of the status bit DSR indicates that the modem is in the data transfer state The OFF condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits — except RI. DSR will switch to the OFF state when in test state. The ON condition of DSR indicates the following: The modem is not in the talk state, i e., an associated telephone handset is not in control of the line The modem is not in the process of automatically establishing a call via pulse or DTMF dialing. The modem has generated an answer tone or detected answer tone. After ring indicate goes ON, DSR waits at least two seconds before turning ON to allow the telephone company equipment to be engaged. DSR will go OFF 50 msec after DTR goes OFF, or 50 msec plus a maximum of 4 sec when the SSD bit is enabled
DSRA	Data Set Ready in Analog Loopback	1:C:7	When configuration bit DSRA is a 1, it causes DSR to be ON during analog loopback.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DTMF	Touch Tones/Pulse Dialing	1:B:1	When configuration bit DTMF is a 1, it tells the modem to auto dial using tones; and when 0, the modem will dial using pulses. The timing for the pulses and tones are as follows (power-on timing): Pulses — Relay open 64 ms Relay closed 36 ms Interdigit delay 750 ms Tones — Tone duration 95 ms Interdigit delay 70 ms The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. The output power level of the DTMF tones is as follows: ±15 dBm ±1 measured at TXA for the R2424M −1 dBm ±1 measured at TIP/RING for the R2424DC
DTR	Data Terminal Ready	1:D:3	Control bit DTR must be a 1 for the modem to enter the data state, either manually or automatically. DTR must also be a 1 in order for the modem to automatically answer an incoming call. During the data mode, DTR must remain at a 1, otherwise the connection will be terminated if DTR resets to a 0 for greater than 50 ms.
EF	Enable Filters	1:9:1	Setting CRQ in the transmitter to a 1 disables the high and low band filters used in data mode so that call progress tone detection can be done. Setting CRQ in the receiver to a 1 inserts a passband filter in the receive path which passes energy in the 345 Hz to 635 Hz bandwidth. The high and low band filters must be enabled and the passband filter disabled for the answer tone and carrier to be detected. This occurs automatically during the auto dial process when EF is set to a 0. In this case, the high and low band filters are disabled when CRQ in the transmitter is set to a 1. If tone detection is required, CRQ in the receiver should be set to a 1. After dialing and call progress tone detection, CRQ in the receiver is set to a 0 and FF is loaded into the dial digit register. (Loading FF enables the high and low band filters). At this time, the answer tone can be detected. To re-enable the high and low band filters disabled by setting CRQ in the transmitter, set EF to a 1. After CRQ in the transmitter and receiver is set to a 1 and tone detection is completed, it may be necessary to detect the answer tone before loading FF into the dial digit register (see the section on sending 1300 Hz calling tone). At that point, EF can be set to a 1 and CRQ in the receiver set to a 0 so the answer tone can be detected (using the ATD bit) and the 1300 Hz calling tone can still be sent. Once the answer tone is detected, FF should be loaded into the dial digit register and the EF bit set to a 0.
ENSI	Enable New Status Interrupt	(0,1):E:6	When handshake bit ENSI is a 1, it causes an interrupt to occur when the status bits in registers (0:[8,9]) and (1:8) are changed by the modem. (NEWS = 1). The IRQ bit will be set to a 1 and the $\overline{IRQ}$ signal will be generated. The interrupt is cleared by writing a 0 into the NEWS bit.
ERDL	Enable Response to Remote Digital Loopback	(0,1):A:7	When configuration bits ERDL are a 1, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS, DSR and RLSD bits to a 0 and turns the $\overline{CTS}$, $\overline{DSR}$ and $\overline{RLSD}$ signals to a logic 1. The TM bit is set to inform the user of the test status. When the ERDL bits are a 0, no response will be generated.
GTE	Guard Tone Enable	1:B:4	When configuration bit GTE is a 1, it causes the specified guard tone to be transmitted (CCITT configurations only), according the state of the GTS bit. Note: The guard tone will only be transmitted by the answering modem.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
GTS	Guard Tone Select	1:B:3	When configuration bit GTS is a 0, it selects the 1800 Hz tone, when GTE is a 1 it selects the 550 Hz tone. The selected guard tone will be transmitted only when GTE is enabled.
IRQ	Interrupt	(0,1):E:7	When status bit IRQ is a 1, it indicates that an interrupt has been generated The $\overline{IRQ}$ hardware signal is generated following the setting of the IRQ bit $\overline{IRQ}$ is cleared when either the NEWS bit is reset to a 0 or the DDR is loaded with a number.
LCD	Loss of Carrier Disconnect	0:D:2	When configuration bit LCD is a 1, the modem terminates a call when a loss of received carrier energy is detected after 400 ms After the first 40 ms of loss of carrier, RLSD goes off. 360 ms later, if no carrier is detected, CTS goes off, and the modem goes on-hook. If energy above threshold is detected during the 360 ms period, RLSD will be set to a 1 again. If further loss of energy occurs, the 400 ms time frame is restarted If LCD is set to a 0, RLSD will be set to a 1 when energy is above threshold, but will not force the modem on-hook when energy falls below threshold In this case, it is necessary to re-enable LCD in order to put the modem on-hook LCD is not automatically disabled in leased line operation The user must write a 0 into LCD bits for this to occur.
LL	Leased Line	1:9:4	When configuration bit LL is a 1, the modem is in leased line operation, when 0, the modem is in switched line operation. When LL is set to a 1, the modem immediately goes off-hook and into data mode.
MODE	Mode Select	(0,1):A:(0,3)	These bits select the compatibility at which the modem is to operate, as shown below: **Configuration Word** **3 2 1 0** — **Configuration** 0 0 0 0 — Bell 2400 — 2400 Sync 0 0 0 1 — Bell 2400 — 2400 Async 0 0 1 0 — Bell 212A — 1200 Sync. 0 0 1 1 — Bell 212A — 1200 Async 0 1 0 0 — Bell 212A — 0 to 300 Async 1 0 0 0 — V.22A — 1200 Sync 1 0 0 1 — V.22B — 1200 Async 1 0 1 0 — V.22A — 600 Sync. 1 0 1 1 — V.22B — 600 Async 1 1 0 0 — V.22 bis — 2400 Sync. 1 1 0 1 — V.22 bis — 2400 Async 1 1 1 0 — V 22 bis — 1200 Sync 1 1 1 1 — V.22 bis — 1200 Async NOTE: The Mode bits in both chips should be set exclusively of all other bits, followed immediately by the setting of the NEWC bits. This will ensure proper modem configuration. *Automatic Reconfiguration* The modem is capable of automatically falling back during the handshake to the compatibility of a remote modem. The modem can be in either the answer or originate mode for this to occur. The compatibilities that the modem are limited to adapt to are V.22 bis, V.22 A/B (1200 bps), Bell 212 and Bell 103. If the R2424 is to originate in a specific configuration, the MODE bits must be set. When the answer modem is configured for Bell 300 asynchronous and is called by a 1200 bps modem, the handshake will be completed at 1200 bps.
NAT	No Answer Tone	1:9:7	When configuration bit NAT is a 1, the modem will not transmit the 2100 Hz CCITT answer tone. This bit is only valid for CCITT configurations. With this bit enabled in answer mode, when the modem goes off-hook it will remain silent for 75 ms and then transmit unscrambled ones.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
NEWC	New Configuration	(0,1):E:3	When the NEWC bit is a 1, it tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC to a 0. NEWC must be set to a 1 after a new configuration has been written into the following registers: (0:[A–D]) and (1:[9–D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.
NEWS	New Status	(0,1):E:5	When handshake bit NEWS is a 1, it tells the user that there has been a change of status in the status registers. The user must write a 0 into NEWS to reset it. This action also causes the interrupt to be cleared.
NTS	No Transmitter Scrambler	1:9:0	When configuration bit NTS is a 1, when the modem is off-hook it will transmit all data in an unscrambled form. This bit should be disabled if the normal modem handshake is desired.
ORG	Originate/Answer	1:9:5	When configuration bit ORG is a 1, the modem is in originate mode; and when a 0 the modem is in answer mode. (This is only valid in manual originate/answer and analog loopback). If ORG is a 1 in analog loopback, the modem will transmit in the high band and receive in the low band. If ORG is a 0 in analog loopback, the modem will transmit in the low band and receive in the high band.
(None)	RAM Access R	0:F:0–7	Contains the RAM access code used in reading RAM locations in chip 0 (receiver device).
(None)	RAM Access T	1:F:0–7	Contains the RAM access code used in reading RAM locations in chip 1 (transmitter device).
XRAMRL	RAM Data XRL	0:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 0.
XRAMRM	RAM Data XRM	0:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 0.
XRAMTL	RAM Data XTL	1:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
XRAMTM	RAM Data XTM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.
YRAMRL	RAM Data YRL	0:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 0.
YRAMRM	RAM Data YRM	0:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 0.
YRAMTL	RAM Data YTL	1:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1.
YRAMTM	RAM Data YTM	1:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RDL	Remote Digital Loopback	(0,1):A:6	When configuration bits RDL are a 1, it causes the modem to initiate a request for the remote modem to go into digital loopback. RXD is clamped to a mark and the CTS bit and $\overline{CTS}$ signal will be reset until the loop is established. The TM bit is not set in this case, since the local modem initiated the request. RDL does not function in 300 bps.
RI	Ring Indicator	1:8:4	When status bit RI is a 1, it indicates that a ringing signal is being detected. The RI bit follows the ringing signal with a 1 during the on time and a zero during the off time coincident with the $\overline{RI}$ signal. The following are the RI bit response times: **RI Bit Transition** — **Response** OFF-to-ON* — 110 ±50 ms (50% duty cycle) ON-to-OFF — 450 ±50 ms *The OFF-to-ON time is duty cycle dependent. 890 ms (15%) ≥ time ≥ 50 ms (100%) This OFF-to-ON (or ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent transition of the RI bit.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RLSD	Received Line Signal Detector	0·8·0	When status bit RLSD is a 1, it indicates that the carrier has successfully been received RLSD will not respond to the guard tones or answer tones RLSD response times are given below **Constant Carrier** / **Controlled Carrier** $\overline{\text{RLSD}}$[1] OFF-to-ON: 40 to 65 ms / 40 to 65 ms ON-to-OFF: 40 to 65 ms / 40 to 65 ms **Note:** 1 After handshake has occurred
RSD	Receive Space Disconnect	0·D·1	When configuration bit RSD is a 1, the modem goes on-hook after receiving approximately 1 6 seconds of continuous spaces
RTRN	Retrain (2400 bps only)	1.9·6	When configuration bit RTRN is a 1, the modem sends the training sequence It resets when the training sequence from the remote modem has successfully been received If the sequence has not been successfully received from the remote modem, CTS will remain OFF In order to put the modem back in the data mode, it is necessary to write a 0 into the RTRN bit, then repeat the retrain sequence
RTS	Request-to-Send	1·9·3	When control bit RTS is a 1, the modem transmits any data on TXD when CTS becomes active In constant carrier mode, RTS should be set the same time as DTR and then left ON In controlled carrier operation, independent operation of RTS turns the carrier ON and OFF. The responses to RTS are shown (assume the modem is in data mode). **Leased or Dial Line[1]** / **RTS Off** / **RTS On** Controlled Carrier: CTS OFF, Carrier OFF / Carrier ON, 210 to 275 ms Scrambled 1's Transmitted, CTS ON Constant Carrier: CTS OFF, Carrier ON, Scrambled 1's Transmitted / CTS ON, Carrier ON, Data Transmitted **Note:** 1 After handshake is complete For ease of use in constant carrier mode, RTS should be turned ON the same time as DTR.
SPEED	Speed Indication	0 9·(4,5)	The SPEED status bits reflect the speed at which the modem is operating. The SPEED bit representations are shown. **4** **5** **Speed** 0 0 0–300 0 1 600 1 0 1200 1 1 2400 **Note:** The SPEED bits are not active in analog loopback and leased line mode

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
SSD	Send Space Disconnect	1:D:0	When configuration bit SSD is a 1, it causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR goes from active to inactive state.
ST	Self Test	(0,1)·A:4	When configuration bit ST is a 1, self test is activated. ST must be a 0 to end the test. It is possible to perform self test in analog loopback with or without a DTE connected. During any self test, TXD and RTS are ignored. Self test does not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver. Error detection is accomplished by monitoring the self test error counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic register when the RAM access code 00 is loaded in the diagnostic control register (0:F). *Self Test End-to-End (Data Mode)* Upon activation of self test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. *Self Test with Loop 3* Loop 3 is applied to the modem as defined in Recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test, In this test DTR is ignored. *Self Test with Loop 2 (Data Mode)* The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test. ST does not function in 300 bps.
3DB	3 dB Loss to Receive Signal	1:B:2	When configuration bit 3DB is a 1, it attenuates the received signal 3 dB. This is only used if the modem will see 0 dBm or greater line signal at the receiver input. Insertion of the 3 dB loss will then prevent saturation.
TM	Test Mode	0:8:1	When status bit TM is a 1, it indicates that the modem has completed the handshake and is in one of the following test modes: AL or RDL.
TONE	Tone Detect	0:8:7	TONE follows the energy detected in the 340 to 640 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when CRQ in chip 0 is a 1. Detection Range: –10 to –43 dBm Response Time: 17 ±2 ms
TXCLK	Transmit Clock Select	1·C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock, as shown below: **Configuration Word** **Transmit Clock** — **6** **5** Internal — 0 0 External — 1 0 Slave — 1 1 If external clock is chosen the user clock must be input at XTCLK. The clock characteristics must be the same as TDCLK. The external clock will be reflected by TDCLK. If slave clock is chosen the transmitter is slaved to the receive clock. This is also reflected by TDCLK.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TX LEVEL	Transmit Level	1 B·(5–7)	TX LEVEL allows the user to change the transmit level at TIP and RING (assuming the DAA has 10 dBm attenuation in the transmit path). Configuration Word 7 6 5 — Transmit Level (±1.0 dBm) (at TIP and RING) 0 0 0 — –10 dBm 0 0 1 — –12 dBm 0 1 0 — –14 dBm 0 1 1 — –16 dBm 1 0 0 — –18 dBm 1 0 1 — –20 dBm 1 1 0 — –22 dBm 1 1 1 — –24 dBm

Internal Modem Timing

In a microprocessor environment it is necessary to know how long various functions last or what the response times of certain functions are. Since the modem is a part of the microprocessor environment its timing and response times are necessary. Table 12 provides the timing relationships between interface memory bits and modem functions.

Table 12. Internal Modem Timing

Parameter	Time Interval
NEWC bit checked	
Transmitter	Once per sample[1]
Receiver	Once per baud[2]
NEWC bit set by host until modem action	
Transmitter	≤ One baud time
Receiver	One baud time
Control, Configuration bits read	
Transmitter	Only after NEWC is set
Receiver	ST, RSD—every sample, all others after NEWC set
Status bits updated	
Transmitter	Once per sample
Receiver	Once per baud
Status change reflected by NEWS, IRQ	
Transmitter	MIN < one sample time MAX one sample time
Receiver	MIN one sample time MAX one baud time
Memory status reflected to modem pin	
Transmitter	33 33 μs
Receiver	33.33 μs

1. Sample Time = 7200 Hz 2 Baud Time = 600 Hz

AUTO DIAL SEQUENCE

The following flow chart defines the auto dial sequence via the microprocessor interface memory.

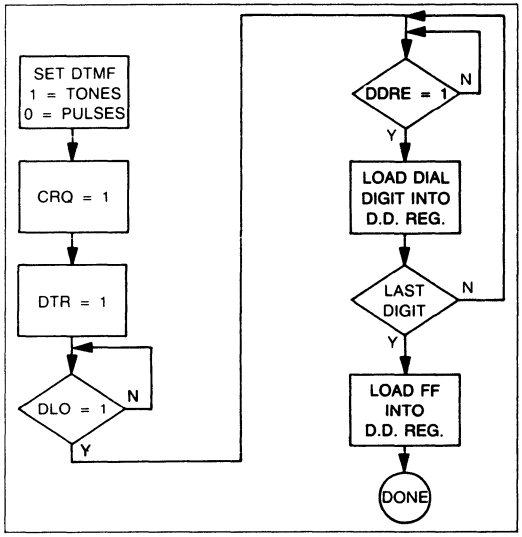


Figure 13. Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

SIGNAL PROCESSOR RAM ACCESS

RAM AND DATA ORGANIZATION

Each signal processor contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16-bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

Interface Memory Locations

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit normally transfers a word from RAM to interface memory once each clock cycle of the SP device. In the transmitter, a word is transferred from SP RAM to the interface memory every sample time. In the receiver, a word is transferred from RAM to the interface memory every sample time as well. Each RAM word transferred to the interface memory is 32-bits long. These bits are written by the SP logic unit into interface memory registers 5, 4, 3, and 2. Registers 3 and 2 contain the most significant byte and least significant byte, respectively, of the XRAM data. Registers 5 and 4 contain the most and least significant bytes of YRAM data, respectively.

RAM Access Codes

The SP logic unit determines the SP RAM address to read from, or write to, by the code stored in the RAM Access bits of interface memory register F (RAM Access R in the receiver 0:F and RAM Access T in the transmitter 1:F).

Only the transmitter (chip 1) allows data to be transferred from interface memory to SP RAM. When set to a 1, bit 1:F:7 signals the SP logic unit to disable transfer of SP RAM data to the interface memory, and instead, to transfer data from interface memory to SP RAM. When writing into SP RAM, 32 bits of data in the XRAM and YRAM registers will be written into the appropriate SP RAM location as specified by the RAM access code (82-86) in register 1:F (Table 13). Once the data is written into the RAM access register 1:F, the XRAM registers 1:2 and 1:3 or the YRAM registers 1:4 and 1:5, set the NEWC bit 1:E:3 to a 1. This action causes the information to be transferred from interface memory into SP RAM. Bit 7 of register 1:F is cleared to a 0 by the modem after the RAM is read. New data can be written into the SP RAM after the NEWC bit is reset to a 0 by the SP.

Note:

Any transmitter RAM Write operation must always be preceded by a RAM read from the desired location. This is to guarantee that the correct information is written into the 16 unchanged bits, since all transmitter RAM operations are 32 bit transfers with typically only 16 of the bits used.

Both the transmitter and receiver (chips 1 and 0, respectively) allow data to be transferred from SP RAM into the interface memory. A 0 in transmitter bit 1:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the RAM access code in register 1:F. A 0 in receiver bit 0:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the access code in register 0:F. To read the SP RAM in chip 1 (transmitter), load into 1:F the RAM access code which identifies the 32 bits of data to transfer to the XRAM and YRAM registers. Next, set the NEWC bit 1:E:3 to a 1. After transferring the data from RAM to the XRAM or YRAM registers, the NEWC bit is reset to a 0 by the SP. Chip 0 (receiver), on the other hand, will provide the XRAM and YRAM data one sample time following the loading of the RAM access code into register 0:F, and will continue to provide the same data at one sample time intervals until a new RAM access code is loaded.

When reading from or writing into RAM, no bits are provided for handshaking or interrupt functions. The NEWC bit can be used as a mechanism to provide sample and baud intervals. Since the NEWC bit is checked, once per baud in chip 0 and once per sample in chip 1, the user can set the NEWC bit and wait for it to be cleared. Depending on which chip the NEWC bit was set, the time interval from the setting to the clearing of the NEWC bit will be either one sample or one baud time. This, however, will not guarantee that the action of reading and writing the XRAM and YRAM will occur in the middle of an actual sample or baud time.

Table 13. RAM Access Codes

Node	Function	RAM Access Code		Chip	Reg. No.
		RAM Read	RAM Write		
1	Demodulator Output	56	–	0	2, 3, 4, 5
2	Low Pass Filter Output	40	–	0	2, 3, 4, 5
3	Input Signal to Equalizer Taps	41–4D	–	0	2, 3, 4, 5
4	AGC Gain Word	14	–	0	2, 3
5	Equalizer Tap Coefficients	01–0D	–	0	2, 3, 4, 5
6	Equalizer Output	53	–	0	2, 3, 4, 5
7	Rotated Equalizer Output (Received Point Eye Pattern)	11	–	0	2, 3, 4, 5
8	Decision Points (Ideal Eye Pattern)	51	–	0	2, 3, 4, 5
9	Rotated Error	52	–	0	2, 3, 4, 5
10	Rotation Angle	12	–	0	4, 5
11	Phase Error	10	–	0	2, 3
12	Self Test Error Counter	00	–	0	2, 3
	DTMF Tone Duration	02	82	1	4, 5
	DTMF Interdigit Delay	03	83	1	2, 3
	Pulse Interdigit Delay	03	83	1	4, 5
	Pulse Relay Make Time	04	84	1	2, 3
	Pulse Relay Break Time	04	84	1	4, 5
	Handshake Abort Counter	05	85	1	4, 5
	Handshake Abort Timer	06	86	1	2, 3
	CTS Off-Time	07	87	1	2, 3

NOTE: 1. All the chip 1 access codes are not valid before R5310-18.
2. Access codes are hexadecimal.
3. Only chip 1 RAM can be written.
4. CTS Off-Time is not valid before R5310-22

ERROR RATES

Bit error rate (BER) is a measure of the throughput of data on the communication channel. It is the ratio of the number of received bits in error to the number of transmitted bits. This number increases with decreasing signal-to-noise ratio (SNR). The type of line disturbance and the modem configuration affect the BER.

Tables 14 through 16 summarize the BERs for various conditions. Figure 14 shows the BER measurement setup.

Table 14. BER Summary

R2424		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
2400 bps	1×10^{-5}	16.6 dB	16.2 dB
1200 bps	1×10^{-5}	8.2 dB	7.9 dB
600 bps	1×10^{-5}	5.0 dB	5.0 dB
300 bps	1×10^{-5}	9.2 dB	7.0 dB

Test Condition: Signal Level = –30 dBm,
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
With 3002 Unconditioned Line.

Table 15. BER Summary

R2424		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
2400 bps	1×10^{-5}	19.0 dB	17.3 dB
1200 bps	1×10^{-5}	8.3 dB	8.1 dB
600 bps	1×10^{-5}	5.0 dB	5.0 dB
300 bps	1×10^{-5}	10.4 dB	7.2 dB

Test Condition: Signal Level = – 43 dBm,
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
With 3002 Unconditioned Line.

Table 16. BER Summary

R2424		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
2400 bps	1×10^{-5}	17.0 dB	16.6 dB
1200 bps	1×10^{-5}	7.7 dB	7.9 dB
600 bps	1×10^{-5}	4.6 dB	4.5 dB
300 bps	1×10^{-5}	9.3 dB	6.2 dB

Test Condition: Signal Level = –40 dBm,
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
Back-To-Back.

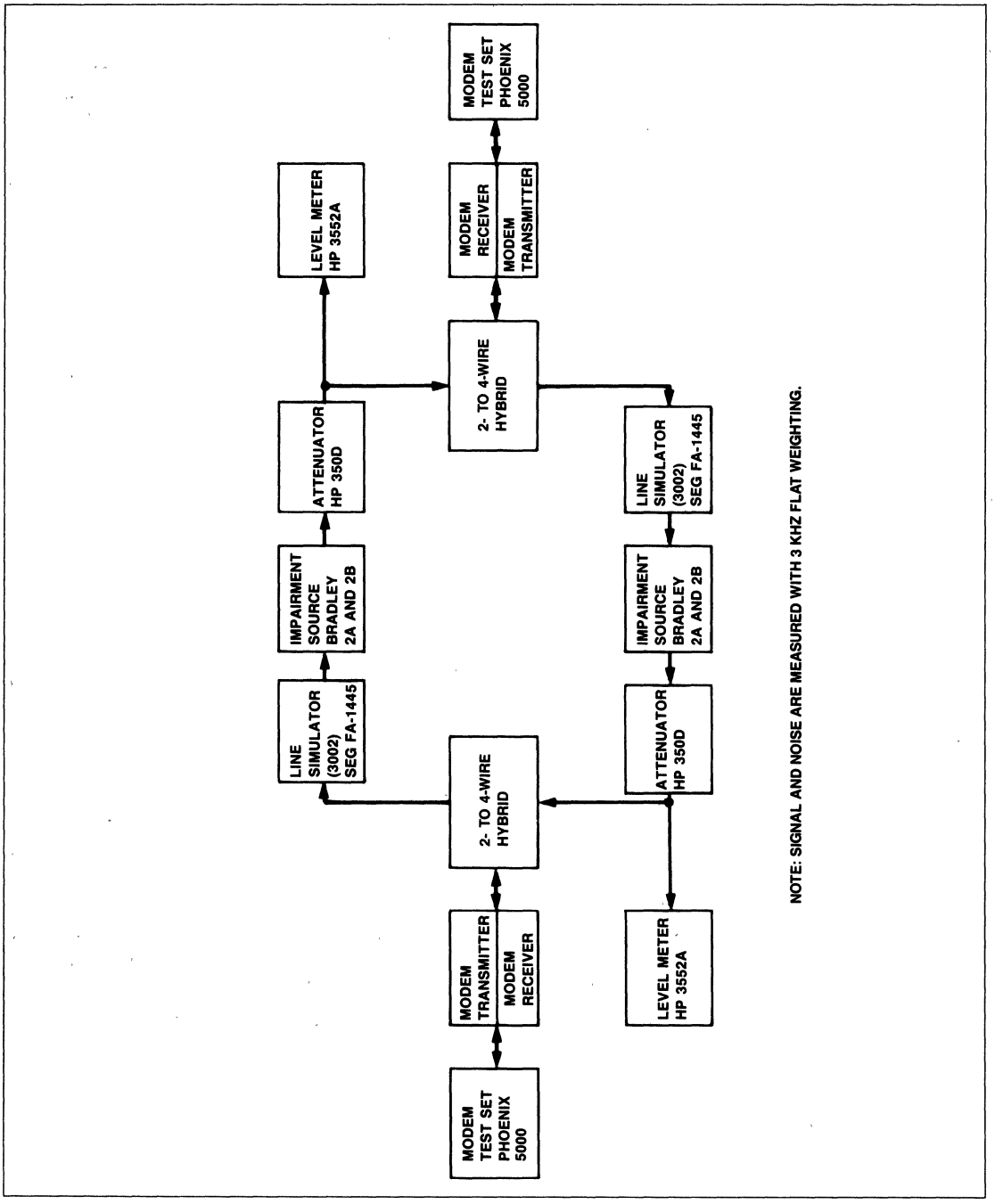


Figure 14. 2-Wire Full-Duplex Bit Error Rate Performance Test Setup (Bidirectional)

Table 17. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	390 mA	<455 mA
+12 Vdc	±5%	25 mA	< 30 mA
−12 Vdc	±5%	4 mA	< 5 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Table 18. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 19. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated.
Board Structure:	The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
PCB Dimensions:	
DC Version	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Height	0.75 in. (19 mm)
M Version	
Width	3.937 in. (100 mm)
Length	3.328 in. (82 mm)
Height	0.40 in. (10.2 mm)
Weight (max):	0.45 lbs. (0.20 kg.)
Lead Extrusion (max.):	0.100 in. (2.54 mm)
DIP Connector Version	
Board Structure	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions	
Width	2.0 in. (50.8 mm)
Length	3.5 in. (88.9 mm)
Height	0.2 in. (5.08 mm) above, 0.13 in. (3.30 mm) below
Weight (max.)	2.6 oz. (73g)
Pin Length (max.)	0.53 in. (13.5 mm) above

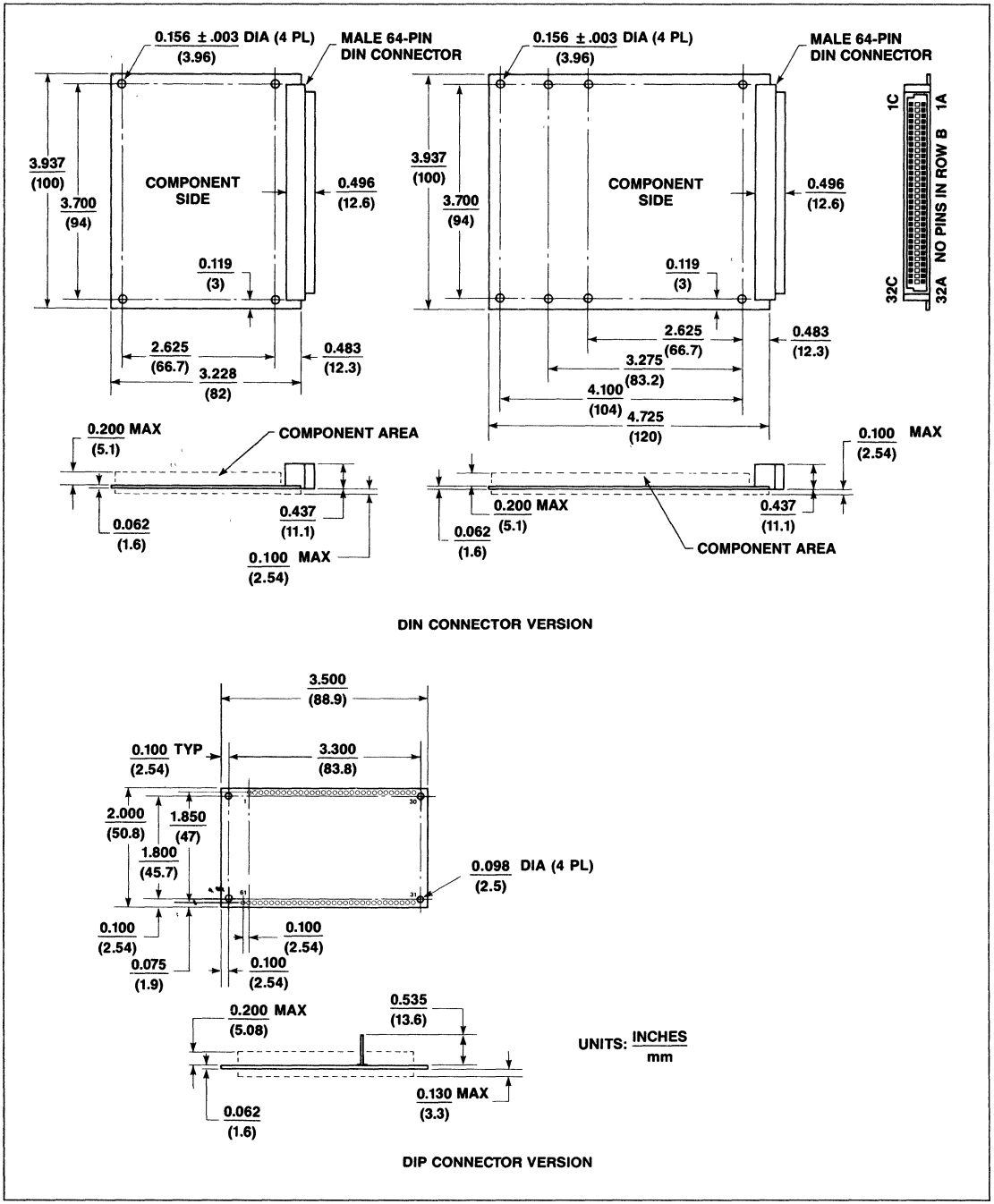


Figure 15. R2424 Modem Dimensions and Pin Locations

R2424 MODEM INSTALLATION AND MAINTENANCE

This section contains installation instructions and maintenance procedures for the Rockwell R2424DC Modem. It also contains a special notice from the Canadian Department of Communications (DOC) for Canadian operation and from the Federal Communications Commission (FCC) for United States operation.

GENERAL DESCRIPTION

The Rockwell R2424DC modem is designed to be used with the United States or Canadian Telephone Switched Networks in 2-wire full-duplex dial-up operation. The modem requires protective circuitry registered with the Federal Communications Commission (FCC) Part 68 which allows direct connection to the U.S. switched telephone network. This circuitry also complies with the Canadian Department of Communications (DOC) Terminal Attachment Program (TAP) which similarly defines their switched telephone network requirements.

The R2424DC features automatic dial and answer capabilities along with surge suppression and hazardous voltage and longitudinal balance protection. Its maximum output signal level at the telephone interface is set at -10 dBm ± 1 dBm (permissive mode of operation).

Two standard telephone jack connectors (RJ11s) are mounted side by side on one edge of the board and are wired in parallel. One is for connection to the telephone line network and the other for the telephone headset connection.

INSTALLATION AND SIGNAL ROUTING INSTRUCTIONS

PHYSICAL MOUNTING

The modem module may be physically incorporated into the customer's end product by utilizing the four corner 0.156" diameter mounting holes (for the self-hooking plastic type standoffs or for bolting it down to some rigid structure) or by installing the module into card guides.

ELECTRICAL INTERFACING INSTRUCTIONS

The electrical interfacing is accomplished via the DIN (Euro) connector (for external power inputs and digital logic signals) and the telco connectors (for the telephone network connection). Note that the telephone interface connectors are physically separated from the modem interface control connector and extreme care must be taken in routing the telephone interface leads from the modem to the telephone network (line connector jack in the wall).

FCC RULES PART 68 REQUIREMENTS

The FCC Rules Part 68 requires that the telephone interface leads shall:

1. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use the same connector as leads or metallic paths connecting to power connections.

   Note

   Power connections are defined as the connections between commercial power and any transformer, power supply rectifier, converter or other circuitry associated with the modem. The connections of the interface pins (including the + 12 Vdc, – 12 Vdc and + 5 Vdc) are not considered power connections.

2. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use adjacent pins on the same connector as metallic paths that lead to unregistered equipment, when specification details provided to the FCC do not show that the interface voltages are less than nonhazardous voltage source limits in Part 68.

   Note

   All the DIN connector interface voltages to the modem have been established as non-hazardous.

ROUTING OF TELEPHONE INTERFACE LINES

In routing the telephone interface leads from the modem telephone connector jacks to the telephone line network connection, the following precautions should be strongly considered for safety.

1. The telephone interface routing path should be as direct and as short as possible.

2. Any cable used in establishing this path should contain no signal leads other than the modem telephone interface leads.

3. Any connector used in establishing this path shall contain not commercial power source signal leads, and adjacent pins to the TIP and RING (T and R) pins in any such connector shall not be utilized by any signals other than those shown in this document.

MAINTENANCE PROCEDURE

Under the FCC Rules, no customer is authorized to repair modems. In the event of a Rockwell modem malfunctioning, return it for repair to an authorized ROCKWELL INTERNATIONAL distributor (if in Canada) or send it directly to the Semiconductor Products Division, Rockwell International Corporation, El Paso, Texas 79906.

SPECIAL INSTRUCTION TO USERS

If the Rockwell modem has been registered with the Federal Communications Commission (FCC), you must observe the following to comply with the FCC regulations:

A. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.

B. It is prohibited to connect the modem to pay telephones or party lines.

C. You are required to notify the local telephone company of the connection or disconnection of the modem, the FCC registration number, the ringer equivalence number, the particular line to which the connection is made and the telephone number to be associated with the jack.

Note

If the proper jacks are not available, you must order the proper type of jacks to be installed by the telephone company (VSOC RJ11 for permissive mode of operation).

D. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only if it can be determined that the telephone line and not the modem is the source of trouble. If the Rockwell modem needs repair, return it to the ROCKWELL INTERNATIONAL CORPORATION. This applies to the modem whether it is in or out of warranty. Do not attempt to repair the unit as this is a violation of the FCC rules and may cause danger to persons or to the telephone network.

TELEPHONE COMPANY RIGHTS AND RESPONSIBILITIES

A. The Rockwell modem contains protective circuitry to prevent harmful voltages to be transmitted to the telephone network. If such harmful voltages do occur, then the telephone company may temporarily discontinue service to you. In this case, the telephone company should:

1. Promptly notify you of the discontinuance.
2. Afford you the opportunity to correct the situation which caused the discontinuance.
3. Inform you of your right to bring a complaint to the FCC concerning the discontinuance.

B. The telephone company may make changes in its facilities and services which may affect the operation of your equipment. It is, however, the telephone company's responsibility to give you adequate notice in writing to allow you to maintain uninterrupted service.

LABELING REQUIREMENTS

A. The FCC requires that the following label be prominently displayed on the outside surface of the customer's end product and that the size of the label should be such that all the required information is legible without magnification.

Sample label below:

Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.

FCC Registration Number: AMQ9SQ-14211-DM-E

Ringer Equivalence: 0.9B

Note

The Rockwell modem module has the FCC registration number and ringer equivalence number permanently affixed to the solder side of the PCB and any unit containing this modem shall use this information for the label requirements.

SPECIAL NOTICE FROM THE CANADIAN DEPARTMENT OF COMMUNICATIONS

The Canadian Department of Communications label identifies certified equipment. This certification means that the equipment meets certain telecommunications network protective, operational and safety requirements. The Department does not guarantee the equipment will operate to the user's satisfaction.

Before installing this equipment, users should insure that it is permissible to be connected to the facilities of the local telecommunications company. The equipment must also be installed using an approved method of connection. In some cases, the company's inside wiring associated with a single line individual service may be extended by means of a certified jack-plug-cord ensemble (telephone extension cord). The customer should be aware that the compliance with the above conditions may not prevent degradation of service in some situations. Existing telecommunications company requirements do not permit their equipment to be connected to customer-provided jacks except where specified by individual telecommunications company tariffs.

The Department of Communications requires the Certificate Holders to identify the method of network connection in the user literature provided with the certified terminal equipment.

Repairs to certified equipment should be made by an authorized Canadian maintenance facility designated by the supplier. Any repairs or alterations made by the user to this equipment, or equipment malfunctions may give the telecommunications company cause to request the user to disconnect the equipment.

Users should ensure for their own protection that the electrical ground connections of the power utility, telephone lines and internal metallic water pipe system, if present, are connected together. This precaution may be particularly important in rural areas.

CAUTION

Users should not attempt to make such connections themselves, but should contact the appropriate electric inspection authority, or electrician, as appropriate.

Rockwell

RC2424DP/DS 2400 bps Full-Duplex Modem Data Pump Device Set

INTRODUCTION

The Rockwell RC2424DP/DS is a 2400 bps, full-duplex, OEM, data pump modem device set. The RC2424DP/DS operates over the public switched telephone network (PSTN), as well as on point-to-point leased lines.

The set consists of two CMOS VLSI components—a digital signal processor (DSP) device and an integrated analog (IA) device. The DSP is available in a 64-pin quad in-line package (QUIP) or a 68-pin plastic leaded chip carrier (PLCC) package. The IA device is available in a 40-pin dual in-line package (DIP) or a 44-pin PLCC package.

The RC2424DP/DS modem meets the requirements specified in CCITT V.22 bis, V.22 A/B, and V.21, as well as Bell 212A and Bell 103.

Full compatibility with V.23 is realized with the addition of an external FSK demodulator. The V.23 capability allows asynchronous operation at 1200 bps with backward channel operation to 75 bps. RC2424DP/DS DSP firmware, in conjunction with a fully compatible hardware interface, directly configures and controls the V.23 FSK demodulator device. Moreover, the centralized transmitter function in the RC2424DP/DS allows "clean" soft turn-offs in V.23 mode.

In addition, the SDLC/HDLC support eliminates the cost of an external serial input/output (SIO) device in products incorporating error correction protocols.

FEATURES

- CMOS DSP and IA devices
- 2-wire full-duplex operation
- Compatible configurations:
  - –CCITT V.22 bis, V.22A/B
  - –CCITT V.21 and V.23
  - –Bell 212A and 103
- Receive dynamic range: –9 dBm to –43 dBm
- Maximum transmit level: 0.0 dBm ±1.0 dB, programmable in 1 dB steps
- Multi-modem detection support
  - –Programmable tone detect bandpass filters
  - –Zero-crossing detector
- V.22 bis fallback/fall-forward – 2400/1200 bps
- Synchronous serial data
  - –2400, 1200, 600 bps ± 0.01% (PSK modulation) Internal/external/slave clock selection
- Parallel data both synchronous and asynchronous
  - –Synchronous: Normal sync: 8-bit data for transmit and receive
  - –SDLC/HDLC support: Transmitter: Flag generation, 0 bit stuffing, CCITT CRC generation Receiver: Flag detection, 0 bit un-stuffing, CCITT CRC checking
  - –Asynchronous: 5, 6, 7, or 8 data bits per character Odd/even parity generation/checking (or 9^{th} data bit) 2400, 1200, 600 bps +1% or (2.3%), –2.5% (PSK modulation) 75, 300, 600, 1200 bps (FSK modulation)
- Programmable ring detect
  - –Min and max frequency range
- Programmable dialer
  - –Make/break times for pulse dialling
  - –DTMF on time for touch-tone dialling
  - –Interdigit times for both pulse and tone dialling
  - –DTMF Level: 0.0 dBm ± 1.0 dB (high tone level is 2.0 dB ± 0.5 dB above low tone level)

- Diagnostics
  - —Read/write RAM
  - —Serial eye pattern output
  - —EQM value in RAM
- Host bus interface memory for configuration, control, and parallel data; compatible with either 8086 or 6502 microprocessor bus
- RS-232C (TTL compatible) interface for RTS control and serial data
- Adaptive and fixed compromise equalization
- Test Configurations:
  - —Local analog loopback
  - —Local digital loopback
  - —Remote digital loopback
- Answer and originate handshake
- Leased line operation
- Power requirements:
  - —± 5 Vdc ± 5%
  - —500 mW typical

R2424 COMPATIBILITY

A high performance modem engine, the RC2424DP/DS is the functional and performance equivalent of Rockwell's R2424DS modem with the following enhancements:

- —2-device implementation in CMOS
- —V.21 and V.23 interface
- —Asynchronous/synchronous parallel data transfer over the microprocessor bus interface
- —Extended 2.3% overspeed in asynchronous, DPSK/QAM modes
- —SDLC/HDLC framing in parallel data mode
- —Additional configuration and control capabilities

These options and enhancements, combined with a user accessible, dual port interface memory (RAM) in the DSP, offer maximum flexibility in customizing the RC2424DP/DS to meet a wide variety of functional requirements.

The RC2424DP/DS device set, with the addition of a few external filter components, interfaces easily to a data access arrangement (DAA). The RC2424DP/DS general interface is illustrated in Figure 1.

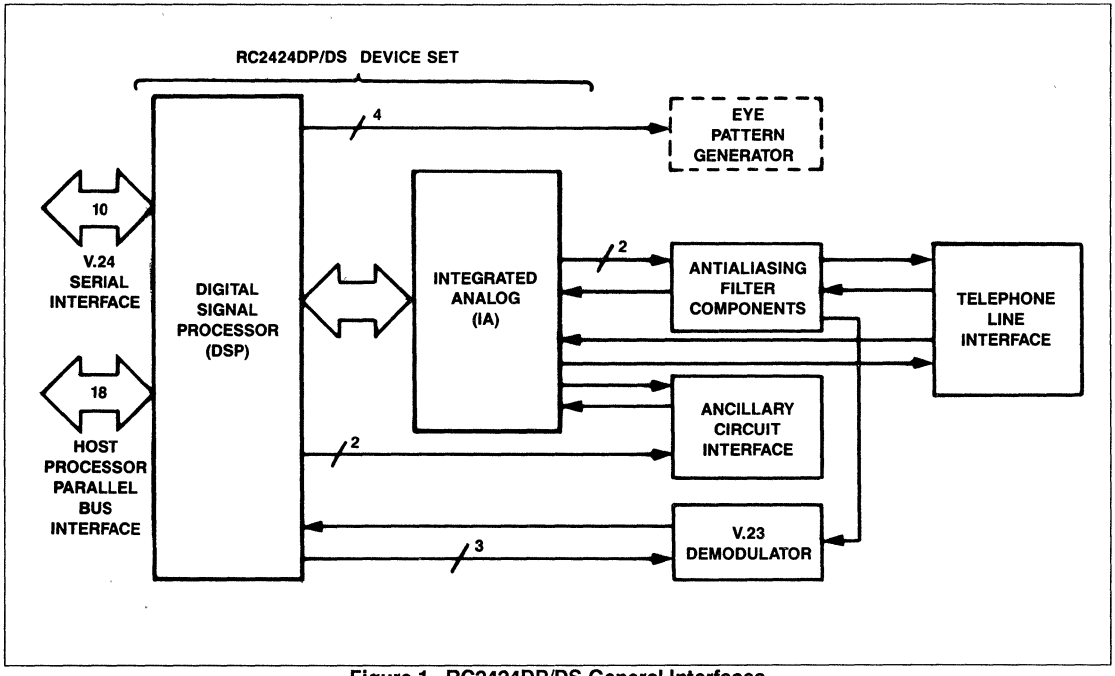


Figure 1. RC2424DP/DS General Interfaces

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES, AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1. The modem configuration is established by the CONF bits.

Note: Bit names refer to control bits in DSP Interface Memory which are set or reset by the host processor (see Software Interface Section, Figure 7 and Table 11).

TONE GENERATION

Answer Tone: A CCITT (2100 ± 15 Hz) or Bell (2225 ± 10 Hz) answer tone is generated depending on the selected configuration.

Guard Tone: A guard tone of 1800 ± 20 Hz (GTS bit = 0) or 550 ± 20 Hz (GTS bit = 1) can be generated (enabled by the GTE bit). The level of transmitted power is 6 ± 1 dB or 3 ± 1 dB below the level of the data power in the main channel for the 1800 Hz or 550 Hz guard tone, respectively. The total power transmitted to the line is the same whether or not a guard tone is enabled. When a guard tone is generated, the main channel transmit path gain is reduced by 0.97 dB or 1.76 dB for the 1800 Hz or 550 Hz guard tone, respectively.

Guard tone on/off must be controlled by the host depending on the state of the handshake sequence, i.e., the host should enable guard tone when DSR is turned on.

DTMF Tones: When Dial/Call Progress configuration is selected (CONF bits = 81) and the DTMF bit is set to a 1, dual tone multi-frequency (DTMF) tones can be generated. The specific DTMF tone generated is specified by the host loading the Transmitter Data Buffer (TBUFFER) with the appropriate digit code shown in Table 2.

User Defined Tones: When Tone Generator/Tone Detector configuration is selected (CONF bits = 80), a user-defined single or dual tone can be generated. In this mode, the transmitter immediately begins sending the frequencies specified in DSP RAM. The tones will remain on as long as Tone Generator/Tone Detector configuration is selected and the tone amplitudes are greater than zero. Setting one of the two amplitudes to zero selects single tone frequency.

Note: Frequencies from 0 to 1675 Hz can be sent when the ORG bit is set, or frequencies from 1925 Hz to 2875 Hz can be sent when the ORG bit is cleared. 1800 Hz frequency can be sent by setting the GTE bit with GTS = 0 and ORG = 0.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Transmitter Carrier Frequency (Hz) ±0.01%		Data Rate (bps)	Baud	Bits Per	Constellation
		Answer[2]	Originate[2]	± 0.01%	(Symbols/Sec.)	Symbol	Points
V.22 bis	QAM	2400	1200	2400[3]	600	4	16
V.22A/B	DPSK	2400	1200	1200[3]	600	2	4
		2400	1200	600[3]	600	1	2
Bell 212A	DPSK	2400	1200	1200[3]	600	2	4
Bell 103	FSK	2225 M 2025 S	1270 M 1070 S	300[4]	300[4]	1	1
V.21	FSK	1650 M 1850 S	980 M 1180 S	300[4]	300[4]	1	1
V.23 Forward Channel	FSK	1300 M 2100 S	1300 M 2100 S	1200[4]	1200[4]	1	1
V.23 Forward Channel	FSK	1700 M 2100 S	1700 M 2100 S	600[4]	600[4]	1	1
V.23 Backward Channel	FSK	390 M 450 S	390 M 450 S	75[4]	75[4]	1	1

Notes:
1. Modulation legend: QAM Quadrature Amplitude Modulation; DPSK Differential Phase Shift Keying; FSK Frequency Shift Keying
2. M indicates a mark condition; S indicates a space condition.
3. Synchronous accuracy = ±0.01%; asynchronous accuracy = –2.5% to +1.0% (+2.3% if extended overspeed is selected).
4. Value is upper limit for serial (e.g., 0-300).

TONE DETECTION

Answer Tone and Call Progress Tones: When Dial/Call Progress configuration is selected (CONF bits = 81), tones can be detected as follows:

Call progress frequency range: 340 ± 5 Hz to 640 ± 5 Hz

Status Bit: TONEA

Answer tones (2100 ± 15 Hz or 2225 ± 10 Hz) or Bell FSK originate tone (1270 ± 10 Hz)

Detection level:0 dBm to –43 dBm

Default detection level: –43 dBm

Response time: 25 ± 2 ms

Status Bits: ATV25, ATBELL (ORG=1), BEL103 (ORG=0)

Tones are detected as energy above a certain threshold within a digital bandpass filter. The pass band of the dual bi-quad infinite impulse response (IIR) filter (Call Progress) or the single bi-quad IIR filter (answer tone or Bell FSK originate) can be changed by writing new coefficients to DSP RAM. The tone detect threshold can also be changed in DSP RAM.

V.23 and V.21 Tones: When Tone Generator/Tone Detector configuration is selected (CONF bits = 80), tones can be detected as follows:

V.23 forward channel mark: 1300 ± 10 Hz

Status Bit: TONEA

V.23 backward channel mark: 390 ± 10 Hz

Status Bit: TONEB

V.21 high band mark (1650 ± 10 Hz) or low band mark (980 ± 10 Hz)

Table 2. Dial Digits/Tone Pairs

Hex Code	Dial Digit	Tone Pair (Hz)	(Hz)
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

Status Bit: TONEC

Detection level: 0 dBm to –43 dBm

Default detection level: –43 dBm

Response time: 25 ± 2 ms

Tones are detected as energy above the threshold within a digital bandpass filter. These filters are single bi-quad IIR filters*. The pass bands can be changed by writing new coefficients to DSP RAM. The tone detect threshold can also be changed in the DSP RAM.

*Except the filter represented by TONEA in Dial/Call Progress configuration, which is a dual biquad IIR filter.

Zero Crossing Detector: A zero crossing detector is always available. The detector can measure tone frequencies between 100 Hz and 3000 Hz. The zero crossing counter increments for both positive and negative zero crossings.

DATA ENCODING

The data encoding conforms to CCITT Recommendations V.22 bis, V.22A/B, V.23, or V.21, or to Bell 212A or 103, depending on the selected configuration.

EQUALIZERS

Equalization functions are incorporated that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer. A 13-tap automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations. Updating of the taps can be enabled or disabled (EQFZ). The equalizer taps can also be reset (EQRES).

Fixed Compromise Equalizer. A fixed compromise equalizer is provided in the transmitter. The equalizer can be enabled or disabled (CEQ bit).

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by a square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ± 150 microseconds over

Table 3. RTS - CTS Response Time

CTS Transition	Configuration	Constant Carrier	Controlled Carrier
OFF to ON	V.22 bis	≤2 ms	270 ms
	V.22	≤2 ms	270 ms
	Bell 212A	≤2 ms	270 ms
	V.21	2-5 ms	2-5 ms
	Bell 103	2-5 ms	2-5 ms
	V.23	5-20 ms	5-20 ms
ON to OFF	All	≤2 ms	≤2 ms

Note: The CTS OFF to ON response time is host programmable in DSP RAM for some configurations.

the frequency range 900 Hz to 1500 Hz (low channel) and 2100 Hz to 2700 Hz (high channel).

TRANSMIT LEVEL

The default transmitter output level is –6.0 dBm ±1.0 dB. The output level can be selected from 0 dBm to –15 dBm in 1 dB steps (TLVL bits).

TRANSMIT TIMING

Transmitter timing is selectable between internal (±0.01%), external , or loopback (TXCLK bits). When external clock is selected, the external clock rate must equal the desired data rate ±0.01% with a duty cycle of 50 ± 20%.

SCRAMBLER/DESCRAMBLER

A self-synchronizing scrambler/descrambler satisfying the applicable CCITT recommendation or Bell specification is incorporated. The scrambler and descrambler can be enabled or disabled (SDIS and DDIS bits, respectively)

RECEIVE LEVEL

The receiver satisfies performance requirements for received line signals from –9 dBm to –43 dBm. The received line signal is measured at the Receiver Analog (RXA) input.

RECEIVER TIMING

A ± 0.01% frequency error in the associated transmit timing source can be tracked.

CARRIER RECOVERY

A ± 7 Hz frequency offset in the received carrier can be tracked with less than a 0.2 dB degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector ($\overline{\text{RLSD}}$) output is off.

RTS - CTS RESPONSE TIME

The response times of CTS relative to a corresponding transition of RTS are listed in Table 3. The response time depends on the receiver operating in either constant carrier or controlled carrier mode (CC bit).

ASYNC/SYNC, SYNC/ASYNC CONVERSION

For parallel asynchronous data transfer, an asynchronous-to-synchronous converter is provided in the transmitter, and a synchronous-to-asynchronous converter is provided in the receiver. Asynchronous or synchronous mode is selected by the ASYNC bit. The asynchronous character format is 1 start bit, 5 to 8 data bits (WDSZ bits), an optional parity bit (PARSL and PEN bits), and 1 or 2 stop bits (STB bit). Valid character sizes, including all bits, are 7, 8, 9, 10 or 11 bits per character.

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters.

Two ranges of signaling rates are provided (selectable by the EXOS bit):

Basic range: +1% to –2.5%

Extended overspeed range: +2.3% to –2.5%

Break is handled in the transmitter and receiver as described in V.22 bis. If the RC2424DP/DS transmitter detects M to 2M + 3 bits of "start" polarity from the DTE, where M is the number of bits per character, the RC2424DP/DS will transmit 2M + 3 bits of start polarity. If the modem detects more then 2M +3 bits of start polarity, it will transmit all these bits as start polarity.

The RC2424DP/DS receiver will output the 2M + 3 or more bits of start polarity on RXD and will set the BRKD bit.

PIN ASSIGNMENTS

The RC2424DP/DS pin assignments are shown in Figure 2. The pin assigments are listed by pin number in Tables 4 and 5 for the DSP and IA devices, respectively.

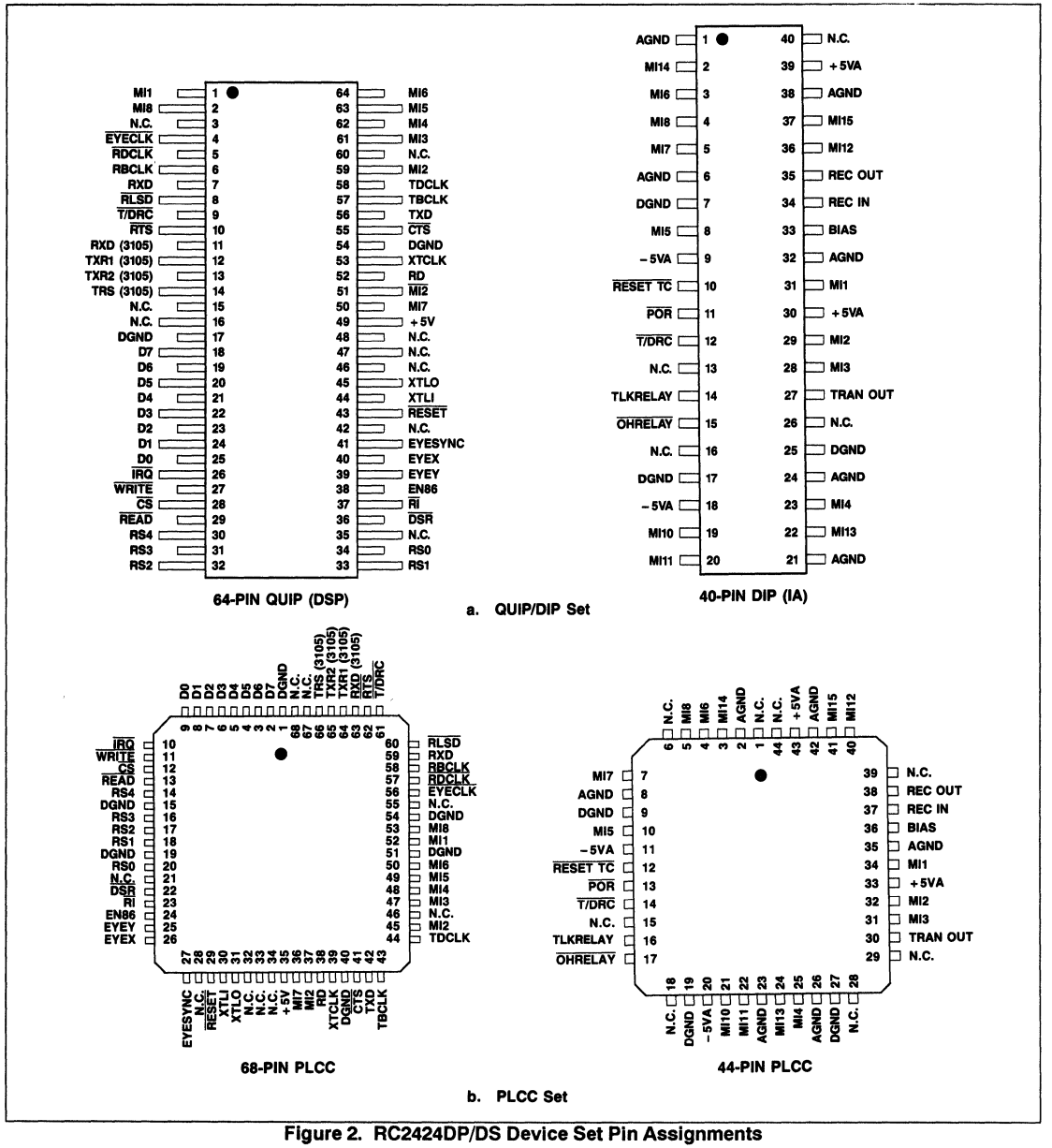


Figure 2. RC2424DP/DS Device Set Pin Assignments

Table 4. RC2424DP/DS DSP Pin Assignments

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Name	I/O Type
52	1	MI1	
53	2	MI8	
54	–	DGND	
55	3	N.C.	
56	4	EYECLK	OA
57	5	RDCLK	OA
58	6	RBCLK	OA
59	7	RXD	OA
60	8	RLSD	OA
61	9	T/DRC	IA
62	10	RTS	IA
63	11	RXD (3105)	IA
64	12	TXR1 (3105)	OB
65	13	TXR2 (3105)	OB
66	14	TRS (3105)	OB
67	15	N.C.	
68	16	N.C.	
1	17	DGND	
2	18	D7	IA/OB
3	19	D6	IA/OB
4	20	D5	IA/OB
5	21	D4	IA/OB
6	22	D3	IA/OB
7	23	D2	IA/OB
8	24	D1	IA/OB
9	25	D0	IA/OB
10	26	IRQ	OC
11	27	WRITE	IA
12	28	CS	IA
13	29	READ	IA
14	30	RS4	IA
15	–	DGND	
16	31	RS3	IA
17	32	RS2	IA
18	33	RS1	IA
19	–	DGND	
20	34	RS0	IA
21	35	N.C.	
22	36	DSR	OB
23	37	RI	OB
24	38	EN86	IA
25	39	EYEY	OB
26	40	EYEX	OB
27	41	EYESYNC	OB
28	42	N.C.	
29	43	RESET	IA
30	44	XTLI	I
31	45	XTLO	O
32	46	N.C.	
33	47	N.C.	
34	48	N.C.	
35	49	+5V	
36	50	MI7	
37	51	MI2	
38	52	RD	IA
39	53	XTCLK	IA
40	54	DGND	
41	55	CTS	OA
42	56	TXD	IA
43	57	TBCLK	OA
44	58	TDCLK	OA
45	59	MI2	
46	60	N.C.	
47	61	MI3	
48	62	MI4	
49	63	MI5	
50	64	MI6	
51	–	DGND	

Notes:
MI = Modem Interconnection (e.g., MI7), see Figure 3.
N.C. = No Connection, leave pin disconnected (open).
I/O Type: See Table 7.

Table 5. RC2424DP/DS IA Pin Assignments

44-Pin PLCC Pin Number	40-Pin DIP Pin Number	Signal Name	I/O Type
1	–	N.C.	
2	1	AGND	
3	2	MI14	
4	3	MI6	
5	4	MI8	
6	–	N.C.	
7	5	MI7	
8	6	AGND	
9	7	DGND	
10	8	MI5	
11	9	-5VA	
12	10	RESET TC	IA
13	11	POR	IA/OA
14	12	T/DRC	IA
15	13	N.C.	
16	14	TLKRELAY	OD
17	15	OHRELAY	OD
18	16	N.C.	
19	17	DGND	
20	18	-5VA	
21	19	MI10	
22	20	MI11	
23	21	AGND	
24	22	MI13	
25	23	MI4	
26	24	AGND	
27	25	DGND	
28	–	N.C.	
29	26	N.C.	
30	27	TRAN OUT	O (DD)
31	28	MI3	
32	29	MI2	
33	30	+5VA	
34	31	MI1	
35	32	AGND	
36	33	BIAS	I
37	34	REC IN	I (DB)
38	35	REC OUT	O (DA)
39	–	N.C.	
40	36	MI12	
41	37	MI15	
42	38	AGND	
43	39	+5VA	
44	40	N.C.	

Notes:
MI = Modem Interconnection (e.g., MI7), see Figure 3.
N.C. = No Connection, leave pin disconnected (open).
I/O Type: See Tables 7 and 8.

HARDWARE INTERFACE SIGNALS

The RC2424DP/DS hardware functional interface signals are shown in Figure 3. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{IRQ}$). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals are organized into functional groups. These signals, along with their interface circuit type codes, are listed in Table 6. The digital and analog interface characteristics are defined in Tables 7 and 8, respectively.

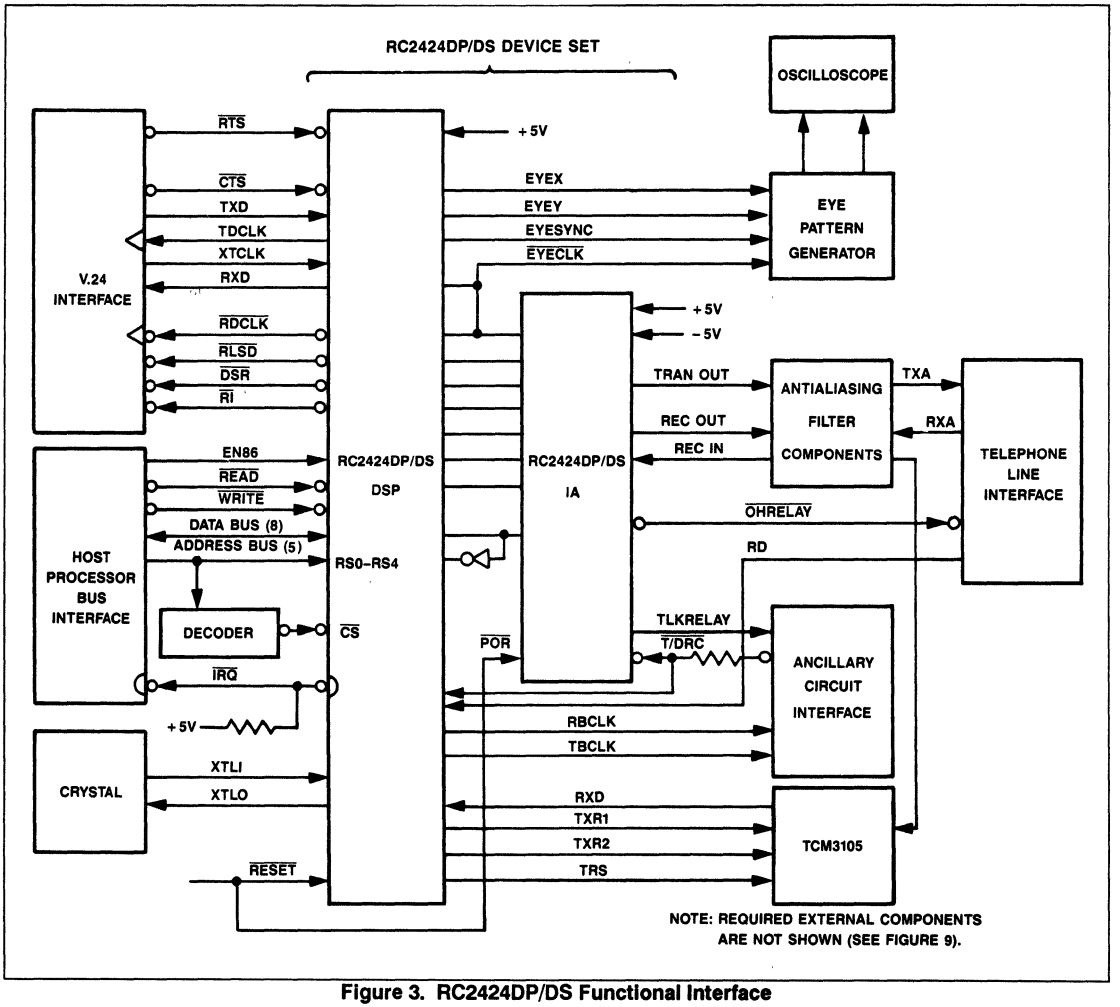


Figure 3. RC2424DP/DS Functional Interface

Table 6. RC2424DP/DS Hardware Interface Signals

Name	I/O Type	Description
DSP and IA Overhead		
AGND	GND	Analog Ground Return
DGND	GND	Digital Ground Return
+5V	PWR	+5 Volt Supply (DSP & IA)
–5V	PWR	–5 Volt Supply (IA)
RESET	IA	Reset (DSP)
POR	IA/OA	Power-On-Reset (IA)
RESET TC	IA	Reset Time Constant (IA)
XTLI	I	Crystal In
XTLO	O	Crystal Out
DSP/Host Processor Pararallel Bus Interface		
D7	IA/OB	↑
D6	IA/OB	|
D5	IA/OB	|
D4	IA/OB	Data Bus (8-Bits)
D3	IA/OB	|
D2	IA/OB	|
D1	IA/OB	|
D0	IA/OB	↓
RS4	IA	↑
RS3	IA	|
RS2	IA	Register Select (5-Bits)
RS1	IA	|
RS0	IA	↓
CS	IA	Chip Select
READ (φ2)	IA	Read Enable or φ2 Clock
WRITE (R/W)	IA	Write Enable or Read/Write
IRQ	OC	Interrupt Request
EN86	IA	Enable 8086 Bus
DSP/TCM3105 Interface		
RXD (3105)	IA	V.23 Receive Data
TXR1 (3105)	OB	V.23 TCM 3105 Control
TXR2 (3105)	OB	V.23 TCM 3105 Control
TRS (3105)	OB	V.23 TCM 3105 Control
DSP/Line Interface		
RD	IA	Ring Detect

Table 6. RC2424DP/DS Hardware Interface Signals (Cont'd)

Name	I/O Type	Description
DSP/V.24 Interface		
XTCLK	IA	External Transmit Clock
TDCLK	OA	Transmitter Data Clock
RDCLK	OA	Receiver Data Clock
RTS	IA	Request-To-Send
CTS	OA	Clear-To-Send
DSR	OB	Data Set Ready
TXD	IA	Serial Transmit Data
RXD	OA	Serial Receive Data
RLSD	OA	Received Line Signal Detector
RI	OB	Ring Indicator
IA/External Filter Components		
REC IN	DB	IA Receiver Op Amp Input
REC OUT	DA	IA Receiver Op Amp Output
TRAN OUT	DD	IA Transmitter Analog Output
External Filter Components/Line Interface		
RXA	DE	Receive Analog Input
TXA	DF	Transmit Analog Output
IA/Line Interface		
OHRELAY	OD	Off-Hook Relay Driver
DSP/Ancillary Circuits		
TBCLK	OA	Transmit Baud Clock
RBCLK	OA	Receive Baud Clock
IA/Ancillary Circuits		
T/DRC	IA	Uncommitted Relay Control
TLKRELAY	OD	Uncommitted Relay Driver
DSP/Eye Pattern Generator (Diagnostic Circuit)		
EYEX	OB	Eye Pattern Data X-Axis
EYEY	OB	Eye Pattern Data Y-Axis
EYECLK	OA	Eye Pattern Clock
EYESYNC	OB	Eye Pattern Sync

NOTES: 1. I/O types are described in Table 7 (digital signals) and Table 8 (analog signals).
2. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Table 7. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage (Types A & B)	V_{IH}	2.0	–	V_{CC}	Vdc	
Input High Current	I_{IL}	–	–	40	μA	V_{CC} = 5.25V, V_{IN} = 5.25V
Input Low Voltage (Types A & B)	V_{IL}	–0.3	–	0.8	Vdc	
Input Low Current	I_{IH}	–	–	–400	μA	V_{CC} = 5.25V
Input Leakage Current	I_{IN}	–	–	±2.5	μA	V_{IN} = 0 to +5V, V_{CC} = 5.25V
Output High Voltage	V_{OH}				Vdc	
Type A and B		3.5	–	–		I_{LOAD} = – 100 μA
Type D		–	–	V_{CC}		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				Vdc	
Type A and C		–	–	0.4		I_{LOAD} = 1.6 mA
Type B		–	–	0.4		I_{LOAD} = 0.8 mA
Type D		–	0.75	–		I_{LOAD} = 15 mA
Three–State Input Current (Off)	I_{TSI}	–	–	±10	μA	V_{IN} = 0.4 to V_{CC} –1
Power Dissipation	P_D	–	530	850	mW	

Table 8. Analog Interface Characteristics

Name	Type	Characteristic
REC OUT	DA	1458 type op amp output Dynamic range: –9 dBm to –43 dBm
REC IN	DB	1458 type op amp input
TRAN OUT	DD	1458 type op amp output Po (High Band) = –0.5 dBm Po (Low Band) = –2.5 dBm
RXA	DE	Input impedance: 68.1 KΩ ± 1% Receive level: –9 dBm
TXA	DF	1458 type op amp output Output level: 0 dBm ±1 dB

OVERHEAD SIGNALS

Overhead signals include power, ground, reset, and crystal signals.

+ 5V Supply

+5V ± 5% is required by both the DSP and the IA devices.

–5V Supply

–5V ± 5% is required by the IA device.

DSP Reset ($\overline{\text{RESET}}$)

The active low $\overline{\text{RESET}}$ input resets the internal DSP logic. Upon transition of $\overline{\text{RESET}}$ from low-to-high, the DSP interface memory bits are set to the default values shown in Table 11.

During DSP power turn-on, $\overline{\text{RESET}}$ must be held low for at least 0.5 microseconds after V_{CC} operating voltage is attained for the internal clock oscillator to stabilize. The DSP $\overline{\text{RESET}}$ input is usually tied to the IA $\overline{\text{POR}}$ line to have the IA $\overline{\text{POR}}$ output initiate a reset upon RC2424DP/DS power turn-on or if the IA detects a low power condition.

Power-On-Reset ($\overline{\text{POR}}$)

The IA Power-On Reset ($\overline{\text{POR}}$) signal is a bidirectional signal that is used as an active low input to reset the IA device and as an active low output to initiate an external reset of the DSP when a low power condition is detected within the IA device.

The IA device power-on reset circuit monitors the IA +5V supply and outputs a 100 ms to 300 ms low pulse on $\overline{\text{POR}}$ upon IA +5V turn-on. This pulse is generated regardless of the IA –5V supply level. A 10 ms minimum low pulse on $\overline{\text{POR}}$ is also generated when the IA +5V supply drops below 3.5V.

When DSP $\overline{\text{RESET}}$ and IA $\overline{\text{POR}}$ are tied together, the IA devices pulses $\overline{\text{POR}}$ low upon IA power turn-on to begin the $\overline{\text{POR}}$ sequence. The modem is ready 350 ms after the low-to-high transition of $\overline{\text{POR}}$. The $\overline{\text{POR}}$ sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{\text{POR}}$ low for at least 3 µs. $\overline{\text{POR}}$ is not pulsed low by the IA device when the $\overline{\text{POR}}$ sequence is initiated externally.

NOTE: If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a $\overline{\text{POR}}$ sequence (i.e., <+3.5V), the host system should assert the reset signals to the DSP and IA devices upon supply voltage recovery to ensure proper modem initialization and operation.

IA Reset Time Constant ($\overline{\text{RESET TC}}$)

When IA $\overline{\text{POR}}$ is used as described above, an external discrete RC network must be connected to the $\overline{\text{RESET TC}}$ pin to generate the $\overline{\text{POR}}$ long time constant (see Figure 9).

In modem circuits not requiring the bidirectional $\overline{\text{POR}}$ signal, the $\overline{\text{RESET TC}}$ input can be used as the active low reset input to the IA device rather than $\overline{\text{POR}}$. In this case, the $\overline{\text{RESET TC}}$ should be connected to the DSP $\overline{\text{RESET}}$ input instead of the RC network, and the IA $\overline{\text{POR}}$ input should be left open.

Crystal In (XTLI) and Crystal Out (XTLO)

The DSP must be connected to an external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors (see Figure 9 and Table 19).

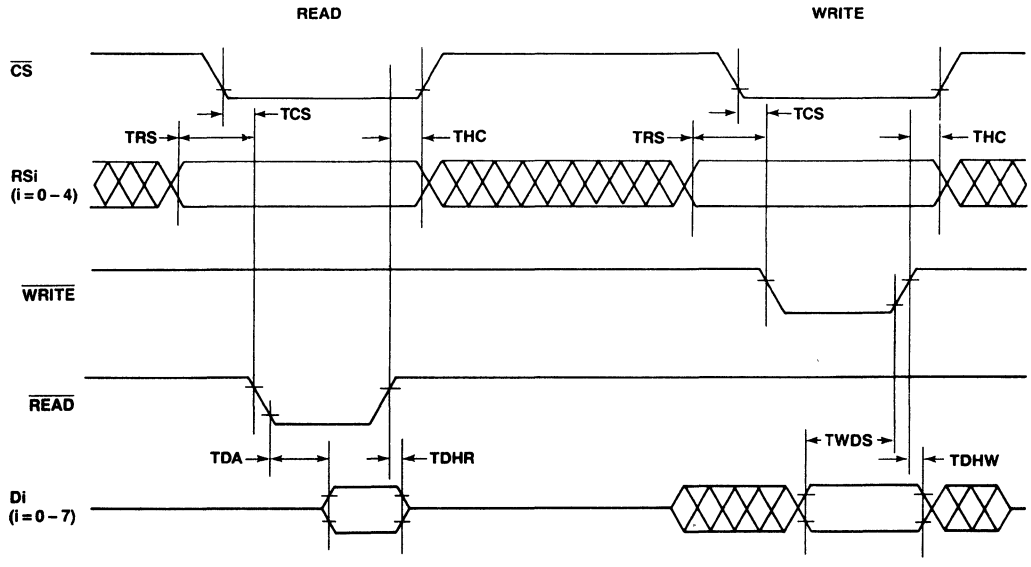
MICROPROCESSOR INTERFACE

Eighteen address, data, control and interrupt hardware interface signals implement an 8086/6502 compatible parallel microprocessor interface to a host processor. The read/write cycle timing requirements are listed in Table 9 and the timing waveforms are illustrated in Figure 4.

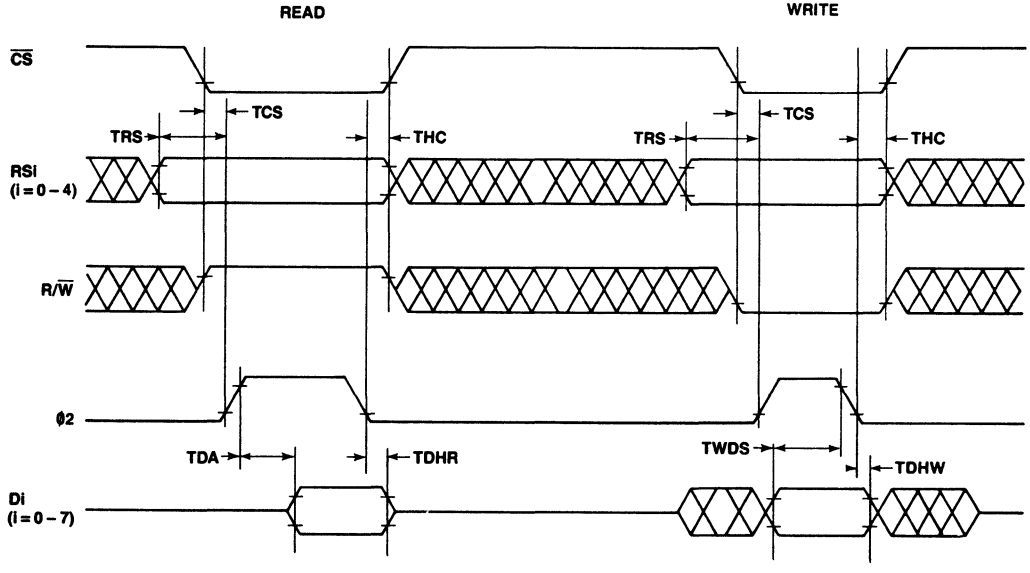
This parallel interface allows the host to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The definitions of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

Table 9. Microprocessor Bus Interface Timing

Parameter	Symbol	Min.	Max.	Units
$\overline{\text{CS}}$ Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	–	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns



a. 8086 Bus Compatible (EN86 = High)



b. 6502 Bus Compatible (EN86 = Low)

Figure 4. Microprocessor Bus Interface Waveforms

Data Lines (D0–D7)

Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable (READ) and Write Enable (WRITE) signals.

Chip Select ($\overline{CS}$)

The active low Chip Select ($\overline{CS}$) input selects the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus.

Register Select Lines (RS0 - RS4)

The five active high Register Select inputs (RS0 - RS4) address interface memory registers within the DSP when $\overline{CS}$ is low. These lines are typically connected to address lines A0-A4.

When selected by $\overline{CS}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0-D7).

Read Enable ($\overline{READ}$) and Write Enable($\overline{WRITE}$)

The microprocessor bus operates with either 8086 or 6502 compatible timing as selected by the EN86 input.

When EN86 is high, 8086 timing is selected, and the read/write control signals are Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$). Reading or writing is controlled by the host pulsing either $\overline{READ}$ or $\overline{WRITE}$ input low, respectively, during the microprocessor bus access cycle (Figure 4a).

During a read cycle, data from the addressed DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the addressed DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

When EN86 is low, 6502 timing is selected, and the read/write control signals are Phase 2 Clock ($\phi 2$) and Read/Write (R/$\overline{W}$). ($\phi 2$ replaces $\overline{READ}$ and R/$\overline{W}$ replaces $\overline{WRITE}$.) Reading or writing is controlled by pulsing R/$\overline{W}$ low or leaving R/$\overline{W}$ high, respectively, during the microprocessor bus access cycle (Figure 4b).

Interrupt Request ($\overline{IRQ}$)

The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in the DSP interface memory to indicate immediate change of conditions in the modem DSP device. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.

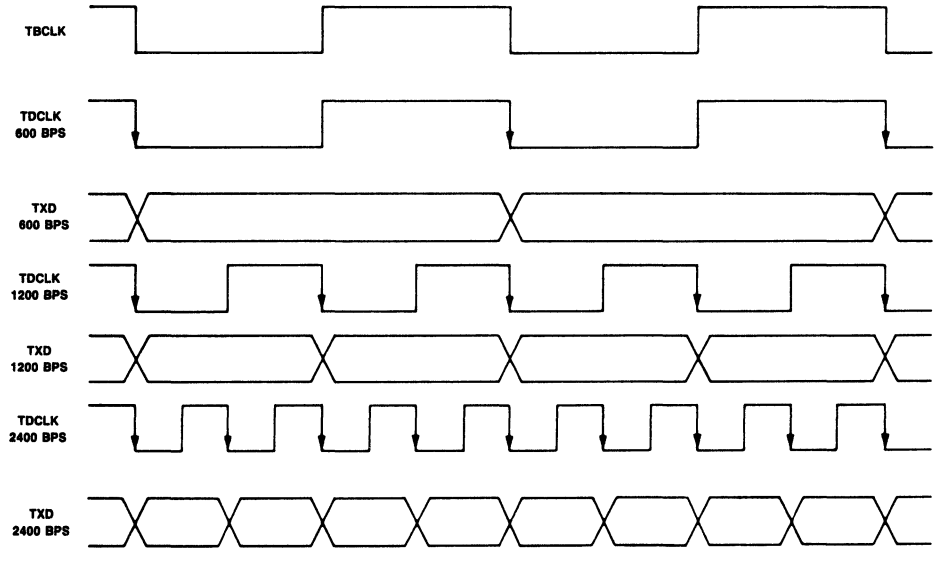
The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{IRQ}$ output can be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt request input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25W, is sufficient.

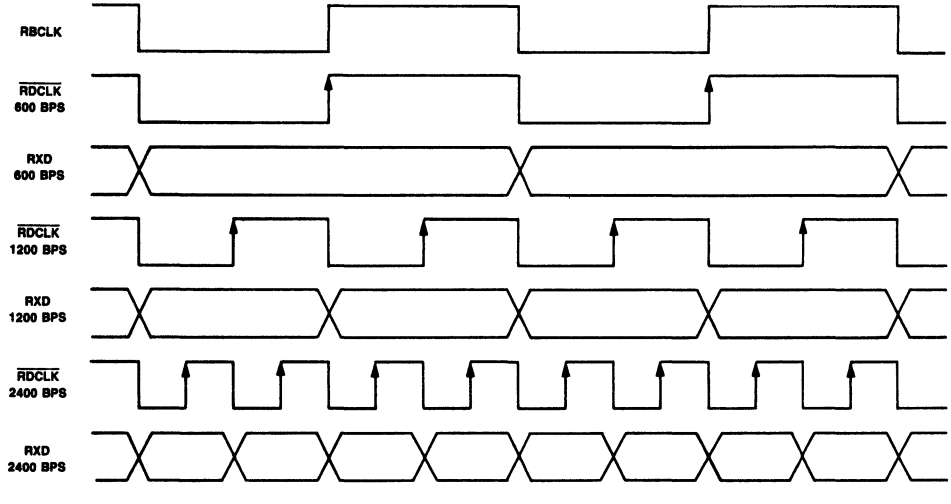
V.24 INTERFACE

Ten hardware circuits provide timing, data and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. The serial interface signals are TTL compatible and can drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels using 1489 receivers and 1488 drivers, or their equivalents. The serial interface timing is illustrated in Figure 5.

The $\overline{RTS}$ hardware control input is logically ORed with its corresponding interface memory bit by the modem to form the resultant control signal. The state of each hardware status output signal ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) is also reflected in its corresponding interface memory bit. Note that the hardware interface signals are complemented with respect to their corresponding interface memory bits (e.g., $\overline{RTS}$ signal low = RTS bit set to a 1).



a. Transmit



b. Receive

Figure 5. Serial Interface Waveforms

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the host on the Transmitted Data (TXD) input in serial mode, or from the interface memory Transmit Data Register (TBUFFER) in parallel mode. (The TPDM bit in selects the serial or parallel mode.)

Received Data (RXD)

The modem presents received serial data to the host on the Received Data (RXD) output and to the interface memory Receive Data Register (RBUFFER) in both serial and parallel modes. RXD is clamped to mark in SDLC mode.

Request To Send ($\overline{RTS}$)

Request to Send ($\overline{RTS}$) input ON (low) causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active.

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) output ON (low) indicates that the modem will transmit any data present on TXD. $\overline{CTS}$ response times relative to $\overline{RTS}$ are shown in Table 3.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) output ON (low) indicates that the modem is in the data transfer state, i.e.:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.

$\overline{DSR}$ OFF (high) indicates that the host is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{RI}$).

Received Line Signal Detector ($\overline{RLSD}$)

$\overline{RLSD}$ ON (low) indicates that valid data is available on RXD. The $\overline{RLSD}$ thresholds are programmable in DSP RAM. The $\overline{RLSD}$ default threshold values for both high and low channels are:

$\overline{RLSD}$ ON ≥ –43 dBm
$\overline{RLSD}$ OFF ≤ –48 dBm

Ring Indicator ($\overline{RI}$)

Ring Indicator ($\overline{RI}$) output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The OFF (high) condition of the $\overline{RI}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received.

The $\overline{RI}$ frequency range is programmable in DSP RAM. $\overline{RI}$ will respond to RD input signals in the frequency range of 15.3 Hz to 68 Hz (default values).

The $\overline{RI}$ OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal on the RD input and the subsequent ON (OFF) transition of RI. The RI response times are shown in Table 10.

Table 10. RI Response Time

$\overline{RI}$ Transition	Response Time
OFF to ON	One Period *
ON to OFF	One Period
* Period of the ring frequency.	

Transmit Data Clock (TDCLK)

The modem outputs a Transmit Data Clock (TDCLK) in synchronous communications. The TDCLK clock frequency is data rate ±0.01% with a duty cycle of 50 ± 1%. Transmit Data (TXD) must be stable during the one microsecond period immediately preceding and following the rising edge of TDCLK.

In asynchronous modes, TDCLK is clamped to mark.

External Transmit Clock (XTCLK)

In synchronous communication, the host may supply the external transmit data clock input (XTCLK). The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is reflected at TDCLK if the modem is set for external clock (TXCLK = 10).

Receive Data Clock ($\overline{RDCLK}$)

The modem outputs a Receive Data Clock ($\overline{RDCLK}$) in the form of 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit can track a ±0.01% frequency error in the remote transmit timing source.

$\overline{RDCLK}$ is output in synchronous communications only. In asynchronous modes, $\overline{RDCLK}$ is clamped to mark.

DAA INTERFACE

Receive Analog (RXA)

RXA is an input to the external filter components from a data access arrangement (see Figure 9). The input impedance at RXA is determined by R13 (see Design Considerations Section). R13 is selected such that power at REC OUT is –9 dBm when the maximum signal is applied to RXA.

Transmit Analog (TXA)

The TXA output from the external filter components (see Figure 9) can drive a data access arrangement for connection to either the PSTN or a leased line. The transmitter output impedance is a 1458 type operational amplifier output. The output level is determined by R15 (see Design Considerations Section).

ANCILLARY SIGNALS

Talk/Data Relay Driver (TLKRELAY)

TLKRELAY is an open drain output which can drive a normally closed relay with greater than 360 Ω coil resistance. The TLKRELAY output is controlled by the T/DRC input. The TLKRELAY output is clamped off during power-on reset. An external discrete diode is not required across the relay coil.

In a typical application, TLKRELAY OFF opens the Talk/Data relay and disconnects the handset from the telephone line (i.e., the modem has control of the line.)

Off-Hook Relay Driver (OHRELAY)

OHRELAY is an open drain output which can drive a normally open relay with greater than 360 Ω coil resistance. OHRELAY ON closes the Off-Hook relay and connects the modem to the telephone line (off-hook). The OHRELAY output is controlled by the state of the RA bit, except in pulse dial mode. OHRELAY output is clamped off during power-on reset. An external discrete diode is not required across the relay coil.

Talk/Data Relay Control (T/DRC)

Talk/Data Relay Control (T/DRC) is an uncommitted input that controls the state of the TLKRELAY output. T/DRC low turns the TLKRELAY output ON; T/DRC high turns the TLKRELAY output OFF.

Ring Detect (RD)

RD indicates to the modem by an ON (high) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the RD input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 Hz to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on RI.

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK) outputs are provided in synchronous communication modes. TBCLK and RBCLK have no counterpart in the V.24 or RS-232-C recommendations since they mark the baud interval rather than the data rate for the transmitter and receiver, respectively. Both signals are active high. The high-to-low transition of each baud clock coincides with a high-to-low transition of the respective data clock.

DIAGNOSTIC SIGNALS

Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line distrubances can usually be identified. Timing of these signals is illustrated in Figure 6.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope horizontal (X) axis and vertical (Y) axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

EYEX and EYEY outputs are 8-bit words, shifted out most significant bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.

EYECLK

EYECLK is a clock for use by the serial-to-parallel converters. The EYECLK output is a 7200 Hz clock.

EYESYNC

EYESYNC is a strobe for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

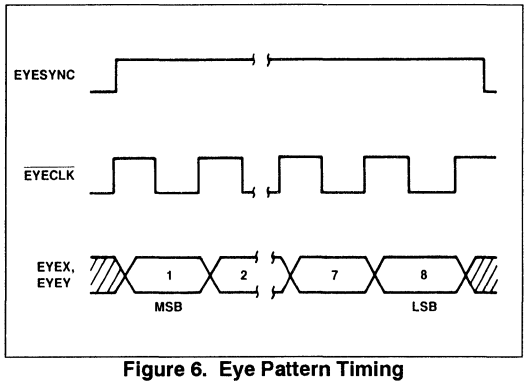


Figure 6. Eye Pattern Timing

SOFTWARE INTERFACE

Modem functions are implemented in DSP firmware.

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAP

A memory map of DSP interface memory identifying the contents of the 32 addressable registers is shown in Figure 7. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, the host must read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory register.

INTERFACE MEMORY BIT DEFINITIONS

Table 11 defines the individual bits in the interface memory. Bits in the interface memory are referred to using the format Z:Q. The register number is denoted by Z (00 through 1 F) and the bit number is located by Q (0 through 7, where 0 = LSB).

INITIALIZATION

The POR default value for each configuration/control bit is shown in Table 11. POR leaves the modem configured as follows:

- 2400 bps
- Synchronous
- Constant carrier
- Serial data mode
- Answer mode

Register	Bit 7	6	5	4	3	2	1	0
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	XACC	—	—	—	—	—	XWT	XCR
1C	X RAM ADDRESS (XADD)							
1B	YACC	—	—	—	—	—	YWT	YCR
1A	Y RAM ADDRESS (YADD)							
19	X RAM DATA MSB (XDAM)							
18	X RAM DATA LSB (XDAL)							
17	Y RAM DATA MSB (YDAM)							
16	Y RAM DATA LSB (YDAL)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	TLVL				—	—	TXCLK	
12	CONFIGURATION (CONF)							
11	—	—	—	—	—	—	—	TXP
10	TRANSMIT DATA BUFFER (TBUFFER)							
0F	RLSD	—	CTS	DSR	RI	TM	SYNCD	FLAGS
0E	RTDET	BRKD	PE	FE	OE	SPEED		
0D	—	—	S1DET	SCR1	U1DET	SADET	—	—
0C	—	—	—	—	—	—	—	—
0B	TONEA	TONEB	TONEC	ATV25	ATBELL	—	—	BEL103
0A	—	—	—	—	—	—	—	CRCS
09	NV25	CC	DTMF	ORG	LL	DATA	—	—
08	ASYNC	TPDM	—	DDIS	TRFZ	—	RTRN	RTS
07	RDLE	RDL	L2ACT	—	L3ACT	—	RA	MHLD
06	BRKS	EXOS	PARSL		PEN	STB	WDSZ	
05	—	—	—	—	CEQ	—	—	—
04	EQRES	—	—	—	EQFZ	IFIX	—	CRFZ
03	SYNCMD		SPLIT	—	ARC	SDIS	GTE	GTS
02	—	—	—	—	—	—	—	—
01	—	—	—	—	—	—	—	RXP
00	RECEIVER DATA BUFFER (RBUFFER)							

(—) Indicates reserved for modem use only

Figure 7. RC2424DP/DS Interface Memory Map

Table 11. Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
ARC	03:3	0	**Automatic Rate Change Enable.** When control bit ARC is a 1, an automatic on-line rate change sequence is enabled. This allows on-line fallback from 2400 bps to 1200 bps per V.22 bis Section 6.6.
ASYNC	08:7	0	**Asynchronous/Synchronous.** When control bit ASYNC is a 1, asynchronous data mode is selected. When ASYNC changes from a 0 to a 1, the receiver's synchronous to asynchronous converter and the transmitter's asynchronous to synchronous converter are configured according to the EXOS, PARSL, PEN, STB and WDSZ bits at that time. ASYNC may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. Asynchronous communication is available only in parallel data mode (TPDM = 1). All clocks are clamped to mark in asynchronous mode. When ASYNC is a 0, synchronous data mode is selected. The SYNCMD bits further select one of two synchronous modes.
ATBELL	0B:3	0	**Bell Answer Tone Detected.** When set to a 1, status bit ATBELL indicates that the modem is detecting a 2225 Hz answer tone. When reset to a 0, the 2225 Hz answer tone is not being detected. ATBELL is active only in the Dial/Call Progress and originate handshake configurations.
ATV25	0B:4	0	**V25 Answer Tone Detected.** When set to a 1, status bit ATV25 signifies that the modem is detecting a 2100 Hz answer tone. When reset to a 0, the 2100 Hz answer tone is not being detected. ATV25 is only active in the Dial/Call Progress and originate handshake modes (ORG = 1).
BEL103	0B:0	0	**Bell 103 Mark Frequency Detected.** When set to a 1, status bit BEL103 indicates that the modem is detecting a Bell 103 mark frequency (1270 Hz). When reset to a 0, the mark frequency is not being detected. BEL103 is available only in Dial/Call Progress and answer handshake modes (ORG = 0).
BRKD	0E:6	0	**Break Detected.** When set to a 1, status bit BRKD indicates the modem is receiving continuous space. When reset to a 0, continuous space is not being received.
BRKS	06:7	0	**Break Sequence.** When control bit BRKS is a 1 and TPDM is a 1, the modem will send continuous space. When BRKS is a 0 and TPDM is a 1, the modem will transmit parallel data from the TBUFFER. (This bit is valid only when TPDM = 1.)
CC	09:6	0	**Controlled Carrier.** When control bit CC is a 1, the modem operates in controlled carrier (i.e., the carrier is controlled by $\overline{\text{RTS}}$); when 0, the modem operates in constant carrier (i.e., the carrier stays on when $\overline{\text{RTS}}$ is off). Controlled Carrier is available only in leased line (LL = 1). Controlled carrier allows the modem transmitter to be controlled by the $\overline{\text{RTS}}$ pin or the RTS bit (see Table 3). When the $\overline{\text{RTS}}$ pin goes low, or the RTS bit set to a 1, the transmitter immediately sends scrambled ones for 270 ms and then turns on the $\overline{\text{CTS}}$ signal and the CTS bit. At 2400 bps, it is recommended that a retrain be sent once in the data mode to ensure that synchronization occurs. (V.22 bis)
CEQ	05:3	0	**Compromise Equalizer Enable.** When control bit CEQ is a 1, the transmitter's passband digital compromise equalizer is inserted into the transmit path. When CEQ is a 0, the equalizer is not inserted into the transmit path.

Table 11. Interface Memory Bit Definitions (Cont'd)

<table>
<tr><th>Mnemonic</th><th>Memory Location</th><th>Default Value</th><th>Name/Description</th></tr>
<tr><td>CONF</td><td>12:0-7</td><td>84</td><td>Modem Configuration Select. The CONF control bits select the modem operating mode from one of the following configuration codes:

<table>
<tr><th rowspan="2">Mode</th><th colspan="2">Data Rate (bps)</th><th rowspan="2">CONF (Hex)</th></tr>
<tr><th>Transmit</th><th>Receive</th></tr>
<tr><td>V.22 bis</td><td>2400</td><td>2400</td><td>84</td></tr>
<tr><td>V.22</td><td>1200</td><td>1200</td><td>52</td></tr>
<tr><td>V.22</td><td>600</td><td>600</td><td>51</td></tr>
<tr><td>Bell 212A</td><td>1200</td><td>1200</td><td>62</td></tr>
<tr><td>Bell 103</td><td>0-300</td><td>0-300</td><td>60</td></tr>
<tr><td>V.21</td><td>300</td><td>300</td><td>A0</td></tr>
<tr><td>V.23</td><td>75</td><td>1200</td><td>46</td></tr>
<tr><td>V.23</td><td>1200</td><td>75</td><td>47</td></tr>
<tr><td>V.23</td><td>75</td><td>600</td><td>44</td></tr>
<tr><td>V.23</td><td>600</td><td>75</td><td>45</td></tr>
<tr><td>V.23</td><td>1200</td><td>1200</td><td>42</td></tr>
<tr><td>V.23</td><td>600</td><td>600</td><td>41</td></tr>
<tr><td>V.23</td><td>75</td><td>75</td><td>40</td></tr>
<tr><td>Tone Generator/Detector</td><td></td><td></td><td>80</td></tr>
<tr><td>Dial/Call Progress Monitor</td><td></td><td></td><td>81</td></tr>
</table>

Note: NEWC must be set to a 1 after CONF is changed.</td></tr>
<tr><td>CRCS</td><td>0A:0</td><td>0</td><td>CRC Sending. When set to a 1, status bit CRCS indicates that the transmitter is sending the CRC (2 bytes) in SDLC mode. A 0 indicates that the CRC is not being sent.</td></tr>
<tr><td>CRFZ</td><td>04:0</td><td>0</td><td>Carrier Recovery Freeze. When control bit CRFZ is a 1, updating of the receiver's carrier recovery phase lock loop (PLL) is inhibited. When reset to a 0, normal updating is enabled.</td></tr>
<tr><td>CTS</td><td>0F:5</td><td>0</td><td>Clear to Send. When set to a 1, status bit CTS indicates that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 3. When reset to a 0, data is not being transmitted.</td></tr>
<tr><td>DATA</td><td>09:2</td><td>0</td><td>Data Mode. When control bit DATA is a 0, the modem is in the idle mode and data is not being transmitted. The modem is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering.

When control bit DATA is a 1, the modem is in the data mode in either leased line mode (LL = 1) or handshake mode (LL = 0).</td></tr>
<tr><td>DDIS</td><td>08:4</td><td>0</td><td>Descrambler Disable. When control bit DDIS is a 1, the receiver's descrambler circuit is disabled; when a 0, the descrambler circuit is enabled.</td></tr>
<tr><td>DSR</td><td>0F:4</td><td>0</td><td>Data Set Ready. When set to a 1 (ON), status bit DSR indicates that the modem is in the data transfer state. When reset to a 0 (OFF), DSR indicates that the DTE is to disregard all signals appearing on the interchange circuits–except RI.</td></tr>
</table>

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
DTMF	09:5	0	**DTMF Select.** When the modem is configured for dialing mode (CONF = 81), the modem will dial using DTMF tones or pulses. When control bit DTMF is a 1, the modem will dial using DTMF tones. When DTMF is a 0, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. Dialing mode is selected by configuration code 81 in the Configuration Register (CONF). When in dialing mode, the data placed in the Transmitter Data Buffer (TBUFFER) is treated as the digit to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the TBUFFER). Also, see TDBE bit. Dialing timing is host programmable in DSP RAM.
EQFZ	04:3	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited. When a 0, updating is enabled.
EQRES	04:7	0	**Equalizer Reset.** When control bit EQRES is a 1, the receiver adaptive equalizer taps are reset to zero. When a 0, the equalizer taps are updated normally.
EXOS	06:6	0	**Extended Overspeed.** When control bit EXOS is a 1, Extended Overspeed mode is selected in the transmitter async-to-sync converter and in the receiver sync-to-async converter. When a 0, normal overspeed mode is selected. (See SPLIT)
FE	0E:4	0	**Framing Error.** When set to a 1, status bit FE indicates that more than 1 in 8 (or 1 in 4 for extended overspeed) characters were received without a Stop bit in asynchronous mode or an ABORT sequence was detected in SDLC/HDLC synchronous mode. When reset to a 0, no framing error is detected.
FLAGS	0F:0	0	**Flag Sequence.** When set to a 1, status bit FLAGS indicates that the transmitter is sending the Flag sequence in SDLC/HDLC mode, or a constant mark in parallel asynchronous mode. When reset to a 0, FLAGS indicates that the transmitter is sending data.
GTE	03:1	0	**Guard Tone Enable.** When control bit GTE is a 1, the specified guard tone to be transmitted is enabled (CCITT configurations only), according to the state of the GTS bit. The guard tone will be transmitted only by the answering modem. When set to a 0, guard tone transmission is disabled. (V.22 bis)
GTS	03:0	0	**Guard Tone Select.** When control bit GTS is set to a 1, the 550 Hz tone is selected; when a 0, the 1800 Hz tone is selected. The selected guard tone will be transmitted only when GTE is enabled. (V.22 bis)
IFIX	04:2	1	**Eye Fix.** When control bit IFIX is a 1, the serial diagnostic data output on the EYEX and EYEY pins reflects the Rotated Equalizer Output. When IFIX is a 0, the data on EYEX and EYEY is selected by the addresses in X RAM Address and Y RAM Address registers, respectively.
LL	09:3	0	**Leased Line.** When control bit LL is set to a 1, the modem will enter the Leased Line Data Mode (selected by the ORG bit) when the DATA bit is a 1. When a 0, the modem will enter the Handshake Mode (selected by the ORG bit) when the DATA bit is a 1.
L2ACT	07:5	0	**Loop 2 (Local Digital Loopback) Activate.** When control bit L2ACT is a 1, the receiver's digital output is internally connected to the transmitter's digital input (locally activated digital loopback) in accordance with CCITT Recommendation V.54.
L3ACT	07:3	0	**Loop 3 (Local Analog Loopback) Activate.** When control bit L3ACT is a 1, the transmitter's analog output is internally coupled to the receiver's analog input (local analog loopback) in accordance with CCITT Recommendation V.54. The modem may only be placed into loop 3 mode when in idle mode (DATA bit is a 0). After setting the L3ACT bit to a 1, the NEWC bit must also be set. The loopback is then completed when the modem sets DSR, CTS, and DCD (RLSD) bits to a 1. To terminate the loopback, reset L3ACT to a 0 and then set NEWC to a 1.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
MHLD	07:0	0	**Mark Hold.** When control bit MHLD is a 1, the transmitter sends continuous mark. When MHLD is a 0, the transmitter sends continuous flag or data from TBUFFER. This bit is valid only in SDLC/HDLC mode.
NCIA	1F:6	0	**NEWC Interrupt Active.** When the new configuration interrupt is enabled (NCIE is a 1) and a new configuration is implemented (NEWC is reset to a 0 by the DSP), IRQ is asserted and status bit NCIA is set to a 1 to indicate that NEWC being a 0 caused the interrupt. NCIA and the interrupt request due to NEWC are cleared by the host writing a 0 into NCIE. (See NEWC and NCIE.)
NCIE	1F:2	0	**NEWC Interrupt Enable.** When control bit NCIE is a 1 (interrupt enabled), the modem will assert IRQ and set NCIA to a 1 when the NEWC bit is reset to a 0 by the DSP. When NCIE is a 0 (interrupt disabled), NEWC has no effect on IRQ or NCIA. (See NEWC and NCIA.)
NEWC	1F:0	0	**New Configuration.** When control bit NEWC is set to a 1, the modem will implement the new configuration. The DSP resets the NEWC bit to a 0 when the configuration change is acknowledged. A configuration change can also cause IRQ to be asserted. (See NCIE and NCIA.) **Note:** Control bit NEWC must be set to a 1 by the host after the host changes the contents of any of the following control bits: CONF Configuration SYNCMD Synchronous Mode Select GTE Guard Tone Enable GTS Guard Tone Select RDLE Remote Digital Loopback Enable RDL Remote Digital Loopback Request L2ACT Loop 2 Activate L3ACT Loop 3 Activate RA Relay Activate PARSL Parity Select PEN Parity Enable STB Stop Bit Number WDSZ Word Size ORG Originate Mode LL Leased Line Mode DATA Data ASYNC Asynchronous Mode RTRN Retrain TLVL Transmit Level EQRES Equalizer Reset
NEWS	1F:3	–	**New Status.** When set to a 1, status bit NEWS indicates that one or more status bits located in registers 0A, 0B, 0E, or 0F have changed state, or a DSP RAM read or write has been completed. This bit can be reset to a 0 only by the host. When set to a 1, this bit can cause IRQ to be asserted. (See NSIE and NSIA.)
NSIA	1F:7	0	**NEWS Interrupt Active.** When the new status interrupt is enabled (NSIE is a 1) and a change of status occurs (NEWS is set to a 1), IRQ is asserted and status bit NSIA is set to a 1 to indicate that NEWS being a 1 caused the interrupt. NSIA and the interrupt request due to NEWS are cleared when the host writes a 0 to NEWS. (See NEWS and NSIE.)
NSIE	1F:4	0	**NEWS Interrupt Enable.** When control bit NSIE is a 1 (interrupt enabled), IRQ will be asserted and NSIA will be set to a 1 when NEWS is set to a 1 by the DSP. When NSIE is a 0 (interrupt disabled), NEWS has no effect on IRQ or NSIA. (See NEWS and NSIA.)

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
NV25	09:7	0	**No. V.25 Answer Tone.** When control bit NV25 is a 1, the transmitter will not transmit the 2100 Hz CCITT answer tone when a handshake sequence is initiated and the modem is in answer mode. In originate mode, the receiver will not look for the 2100 Hz tone. When reset to a 0, the modem will transmit the answer tone in answer mode and will look for the answer tone in originate mode.
OE	0E:3	0	**Overrun Error.** When set to a 1, status bit OE indicates that the Receiver Data Buffer (RBUFFER) was loaded from the RXA input before the host read the old data from RBUFFER. When reset to a 0, RBUFFER was read before new receive data was loaded into RBUFFER. This is valid for both ASYNC mode and SDLC/HDLC mode.
ORG	09:4	0	**Originate.** When control bit ORG is a 1, the modem is in originate mode; when a 0, the modem is in answer mode. **Note:** The NEWC bit must be set after the ORG bit is changed.
PARSL	06:4, 5		**Parity Select.** Control bits PARSL select the method by which parity is generated and checked during the asynchronous parallel data mode (ASYNC = 1). The options are: 5 4 — **Parity Selected** 0 0 — Stuff Parity ("9th Data Bit") (see TXP, RXP) 0 1 — Space Parity 1 0 — Even Parity 1 1 — Odd Parity
PE	0E:5	0	**Parity Error.** When set to a 1, status bit PE indicates that a character with bad parity was received in the asynchronous mode, or bad CRC was detected in the SDLC/HDLC synchronous mode. When a 0, a character with good parity was received.
PEN	06:3	0	**Parity Enable.** When set to a 1, control bit PEN enables parity generation and checking during asynchronous parallel data mode. When reset to a 0, parity generation and checking is disabled.
RA	07:1	0	**Off-Hook Relay Activate.** When control bit RA is set to a 1, the $\overline{\text{OHRELAY}}$ output is activated causing the relay to close (off-hook); when RA is reset to 0, the $\overline{\text{OHRELAY}}$ is turned off causing the relay to open (on-hook). **Note:** The host has exclusive control of the $\overline{\text{OHRELAY}}$ output through the RA bit except in pulse dial mode.
RBUFFER	00:0-7	0	**Receive Data Buffer.** The host obtains data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER.
RDBF	1E:0	–	**Receiver Data Buffer Full.** When set to a 1, status bit RDBF signifies that the modem wrote valid received data into register 00 (RBUFFER). This condition can also cause $\overline{\text{IRQ}}$ to be asserted. The host reading or writing register 00 resets the RDBF bit to 0. (See RDBIE and RDBIA.)
RDBIA	1E:6	0	**Receiver Data Buffer Interrupt Active.** When the receiver data buffer full interrupt is enabled (RDBIE is a 1) and register 00 is written to by the DSP (RDBF is set to a 1), the modem asserts $\overline{\text{IRQ}}$ and sets RDBIA to a 1 to indicate that RDBF being a 1 caused the interrupt. The host reading or writing register 00 resets the RDBF bit to a 0 and clears the interrupt request due to RDBF. (See RDBF and RDBIE.)
RDBIE	1E:2	0	**Receiver Data Buffer Interrupt Enable.** When control bit RDBIE is a 1 (interrupt enabled), the modem will assert $\overline{\text{IRQ}}$ and set the RDBIA bit to a 1 when RDBF is set to a 1 by the DSP. When RDBIE is a 0 (interrupt disabled), RDBF has no effect on $\overline{\text{IRQ}}$ or RDBIA. (See RDBF and RDBIA.)
RDL	07:6	0	**Remote Digital Loopback Request.** When control bit RDL is a 1, the modem initiates a request for the remote modem to go into digital loopback, RXD is clamped to a mark, and the RLSD bit and $\overline{\text{RLSD}}$ signal will be reset until the loop is established. When the host resets the RDL bit the modem sends the RDL terminating sequence.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RDLE	07:7	0	**Remote Digital Loopback Response Enable.** When set to a 1, control bit RDLE enables the modem to respond to the remote modem's digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS and RLSD bits to a 0, and turns the $\overline{CTS}$ and $\overline{DCD}$ signals OFF. The TM bit is set to a 1 to inform the host of the test status.
RI	0F:3	0	**Ring Indicator.** When set to a 1, status bit RI indicates that a valid ringing signal is being detected. Ringing is detected if pulses are present on the $\overline{RD}$ input in the 15 Hz - 68 Hz frequency range (default frequency range). The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with $\overline{RI}$ output signal. The minimum and maximum valid ring frequencies are host programmable in DSP RAM. If the maximum value is set to zero, the RI bit will go on and off with each half of the ring frequency sine wave.
RLSD	0F:7	0	**Received Line Signal Detector.** When status bit RLSD is set to a 1, the carrier is being detected and receive data is valid. When a 0, the carrier is not being detected and RXD output is clamped to mark. **Note:** RXD is also clamped to mark during retrain while the RLSD bit remains on.
RTDET	0E:7	0	**Retrain Detected.** When set to a 1, status bit RTDET indicates that a retrain request sequence has been detected.
RTRN	08:1	0	**Retrain.** When control bit RTRN set to a 1 and the modem is in data mode, the modem requests retrain (or automatic rate change - see ARC) from the remote modem. RTRN is set to 0 when the previous retrain is completed. **Note:** If retrain is not completed successfully, the host must clear the RTRN bit. Fallback from 2400 bps to 1200 bps per CCITT V.22 bis may be accomplished as follows: 1. Set the ARC bit to a 1 in both modems. 2. Set the RTRN bit to a 1 in either modem. 3. Set the NEWC bit to a 1. Fall forward from 1200 bps to 2400 may be accomplished as follows: 1. Reset the ARC bit (with the remote modem having the ARC bit set). 2. Set the RTRN bit. 3. Set the NEWC bit. If the remote modem can operate at the requested rate, the SPEED bits will be changed by the modem to reflect the new rate after the retrain is completed. If the remote modem cannot operate at the new rate, then no rate change will take place during the retrain. In this case, the host must clear the RTRN bit.
RTS	08:0	0	**Request to Send.** When control bit RTS is a 1 or the $\overline{RTS}$ input is ON, the CTS bit is set to a 1 and the $\overline{CTS}$ output is turned ON. When the RTS bit is reset to 0 and the RTS input is OFF, the CTS bit is reset to a 0 and the $\overline{CTS}$ output is turned OFF.
RXP	01:0	0	**Received Parity bit.** This bit is only valid when parity is enabled (PEN = 1), and word size is set for 8 bits per character (WDSZ = 11). In this case, the parity bit received (or ninth data bit) will be available at this location. The host must read this bit before reading the received data buffer (RBUFFER).
S1DET	0D:5	0	**S1 Sequence Detected**. Status bit S1DET is set to a 1 when the S1 sequence is being detected. This bit is reset to a 0 when the S1 sequence is not being detected.
SADET	0D:2	0	**Scrambled Alternating Ones Sequence Detected.** Status bit SADET is set to a 1 when the Scrambled Alternating Ones sequence is being detected. This bit is reset to a 0 when the Scrambled Alternating Ones sequence is not being detected. **Note:** SADET is used to indicate the response of the remote modem to a V.22 bis rate change request or a remote digital loopback request.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
SCR1	0D:4	0	**Scrambled Ones Sequence Detected.** Status bit SCR1 is set to a 1 when Scrambled Ones is being detected during handshake. This bit is reset to 0 when Scrambled Ones is not being detected.
SDIS	03:2	0	**Scrambler Disable.** When control bit SDIS is a 1, the transmitter scrambler is disabled; when SDIS is a 0, the scrambler is enabled.
SPEED	0E:0-2	0	**Speed Indication.** The SPEED status bits indicate the data rate at the completion of a handshake: **2 1 0 — Data Rate (bps)** 0 0 0 — 300 0 0 1 — 600 0 1 0 — 1200 0 1 1 — 2400
SPLIT	03:5	0	**Parallel Async Extended Overspeed TX/RX Split.** When SPLIT is set to a 1 and EXOS is set, the transmitter will transmit at the basic overspeed while the receiver receives at the extended overspeed rate.
STB	06:2	0	**Stop Bit Number.** When control bit STB is a 0, one stop bit is selected in asynchronous mode; when a 1, two stop bits are selected.
SYNCD	0F:1	0	**Sync Pattern Detected.** When set to a 1, status bit SYNCD indicates that SDLC/HDLC flags (7E pattern) are being detected. When reset to a 0, the 7E pattern is not being detected.
SYNCMD	03:6,7	0	**Synchronous Mode.** Configuration bits SYNCMD select the synchronous mode (ASYNC = 0) from the following: **7 6 — Synchronous Mode** 0 0 — Normal Sync 0 1 — SDLC/HDLC Sync
TBUFFER	10:0-7	00	**Transmitter Data Buffer.** The host conveys output data to the transmitter in the parallel mode (TPDM = 1) by writing a data byte to the TBUFFER when the TDBE bit is a 1. The data is transmitted bit 0 first.
TDBE	1E:3	–	**Transmitter Data Buffer Empty.** When set to a 1, status bit TDBE signifies that the modem has read transmit data from register 10 (TBUFFER) and the host can write new data into register 10. This condition can also cause IRQ to be asserted. The host reading or writing register 10 resets the TDBE bit to 0. (See TDBIE and TDBIA.)
TDBIA	1E:7	0	**Transmitter Data Buffer Interrupt Active.** When the transmitter data buffer empty interrupt is enabled (TDBIE is a 1) and register 10 is empty (TDBE is set to a 1), the modem asserts IRQ and sets status bit TDBIA to a 1 to indicate that TDBE being a 1 caused the interrupt. The host reading or writing register 10 resets the TDBIA bit to a 0 and clears the interrupt request due to TDBE. (See TDBIE and TDBE.)
TDBIE	1E:5	0	**Transmitter Data Buffer Interrupt Enable.** When control bit TDBIE is a 1 (interrupt enabled), the modem will assert IRQ and set the TDBIA bit to a 1 when TDBE is set to 1 by the DSP. When TDBIE is a 0 (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.)

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TLVL	13:4-7	6	**Transmit Level Attenuation Select.** The TLVL control code selects the transmitter analog output level attenuation at the TXA pin as follows: **7 6 5 4 — Transmit Level Attenuation (dB ±0.5 dB)** 0 0 0 0 — 0 dB 0 0 0 1 — 1 dB 0 0 1 0 — 2 dB 0 0 1 1 — 3 dB 0 1 0 0 — 4 dB 0 1 0 1 — 5 dB 0 1 1 0 — 6 dB 0 1 1 1 — 7 dB 1 0 0 0 — 8 dB 1 0 0 1 — 9 dB 1 0 1 0 — 10 dB 1 0 1 1 — 11 dB 1 1 0 0 — 12 dB 1 1 0 1 — 13 dB 1 1 1 0 — 14 dB 1 1 1 1 — 15 dB The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.
TM	0F:2	0	**Test Mode.** When set to a 1, status bit TM indicates that the selected test mode is active. When TM is reset to a 0, no test mode is active.
TONEA	0B:7	0	**Tone Filter A Energy Detected.** When set to a 1, status bit TONEA indicates that energy above the threshold is being detected by the Call Progress Monitor filter in the Dial Configuration (CONF = 81) or that 1300 Hz FSK tone energy is being detected by the Tone A bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	0B:6	0	**Tone Filter B Energy Detected.** When set to a 1, status bit TONEB indicates that 390 Hz FSK tone energy is being detected by the Tone B bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	0B:5	0	**Tone Filter C Energy Detected.** When set to a 1, status bit TONEC indicates that either 1650 Hz (ORG = 1) or 980 Hz (ORG = 0) FSK tone energy is being detected by the Tone C bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TPDM	08:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is a 1, the transmitter accepts parallel data from the host microprocessor interface via the TBUFFER register for transmission rather than serial data from the TXD input pin. When TPDM is a 0, serial data from the TXD input pin is accepted for transmission rather than parallel data from TBUFFER.
TRFZ	08:3	0	**Timing Recovery Freeze.** When control bit TRFZ is a 1, the updating of the receiver's timing recovery algorithm is inhibited. When TRFZ is a 0, normal updating occurs.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TXCLK	13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock: **1 0 — Transmit Clock** 0 0 — Internal 0 1 — Not Used (Internal) 1 0 — External (XTCLK input) 1 1 — Slave (RDCLK output) When the external clock is chosen, the host supplied clock must be connected to the XTCLK input pin. The external clock will then be reflected at the TDCLK output pin. When the slave clock is chosen, the transmitter clock output (TDCLK) is phase locked to the receiver clock output (RDCLK).
TXP	11:0	0	**Transmit Parity bit.** This bit is only active when parity is enabled (PEN = 1), stuff parity is selected (PARSL = 00) and word size is set for 8 bits per character. The host must load the stuffed parity bit (or ninth data bit) in this location before loading the other 8 bits of data in TBUFFER.
U1DET	0D:3	0	**Unscrambled Ones Detected.** When set to a 1, status bit U1DET indicates that V.22 bis Unscrambled Ones sequence has been detected. This bit is reset to a 0 by the modem at the end of the Unscrambled Ones sequence. (V.22 bis)
WDSZ	06:0,1	0	**Data Word Size.** The WDSZ control field sets the number of data bits per character in asynchronous mode as follows: **1 0 — Data Bits/Character** 0 0 — 5 0 1 — 6 1 0 — 7 1 1 — 8
XACC	1D:7	0	**X RAM Access Enable.** When control bit XACC is a 1, the DSP accesses the X RAM associated with the address in XADD and the XCR bit. XWT determines if a read or write is performed. The DSP resets XACC to a 0 upon RAM access completion.
XADD	1C:0-7	00	**X RAM Address.** XADD contains the X RAM address used to access the DSP's X Data RAM (XCR = 0) or X Coefficient RAM (XCR = 1) via the X RAM Data LSB and MSB registers (addresses 18 and 19, respectively). (See Table 12.)
XCR	1D:0	0	**X Coefficient RAM Select.** When control bit XCR is a 1, XADD applies to the X Coefficient RAM. When XCR is a 0, XADD applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 12).
XDAL	18:0-7	00	**X RAM Data LSB.** XDAL is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XDAM	19:0-7	00	**X RAM Data MSB.** XDAM is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XWT	1D:1	0	**X RAM Write.** When XWT is a 1 and XACC is set to a 1, the DSP copies data from the X RAM Data registers (18 and 19) into the X RAM location addressed by XADD and XCR. When control bit XWT is a 0 and XACC is set to a 1, DSP reads X RAM at the location addressed by XADD and XCR and stores the data into the X RAM Data registers (18 and 19)
YACC	1B:7	0	**Y RAM Access Enable.** When control bit YACC is a 1, the DSP accesses the Y RAM associated with the address in YADD and the YCR bit. YWT determines if a read or write is performed. The DSP resets YACC to a 0 upon RAM access completion.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description (Cont'd)
YADD	1A:0-7	00	**Y RAM Address.** YADD contains the Y RAM address used to access the DSP's Y Data RAM (YCR = 0) or Y Coefficient RAM (YCR = 1) via the Y RAM Data LSB and MSB registers (adresses 16 and 17, respectively). (See Table 12.)
YCR	1B:0	0	**Y Coefficient RAM Select.** When control bit YCR is a 1, YADD applies to the DSP's Y Coefficient RAM. When YCR is a 0, YADD applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 12).
YDAL	16:0-7	00	**Y RAM Data LSB.** YDAL is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YDAM	17:0-7	00	**Y RAM Data MSB.** YDAM is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YWT	1B:1	0	**Y RAM Write.** When YWT is a 1 and YACC is set to a 1, the DSP copies data from the Y RAM Data registers (16 and 17) into the Y RAM location addressed by YADD and YCR. When control bit YWT is a 0 and YACC is set to a 1, the DSP reads Y RAM at the location addressed by YADD and YCR and stores the data into the Y RAM Data registers (16 and 17).

DSP RAM ACCESS

The DSP contains four sections of 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) sections, as well as data and coefficient sections. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously in either the data or coefficient section.

INTERFACE MEMORY ACCESS TO DSP RAM

The DSP interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The addresses stored in DSP interface memory RAM Address registers (i. e., XADD and YADD) by the host, in conjunction with the data or coefficient RAM bits (i. e., XCR and YCR) determine the DSP RAM addresses for data access.

One or two 16-bit words are transferred between DSP RAM and DSP interface memory once each internal DSP cycle. The transmitter and the receiver sample rate functions operate at the 7200 Hz sample rate. The receiver baud rate function operates at the 600 Hz.

Two RAM access bits (XACC and YACC) in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The DSP tests these bits each sample period.

HOST PROGRAMMABLE DATA

The parameters available in DSP RAM are listed in Table 12 along with the X RAM or Y RAM address and corresponding XCR or YCR bit value.

HOST DSP READ AND WRITE PROCEDURES

DSP RAM Write Procedure

1. Before writing to DSP interface memory, verify that XACC and YACC are reset to 0.
2. Load the RAM address into XRAM address (XADD) and/or YRAM address (YADD).
3. Write the desired data to the RAM data registers (XDAM, XDAL, YDAM, or YDAL).
4. Set the coressponding coefficient RAM select bits (XCR, YCR) as necessary.

Table 12. DSP RAM Parameters

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
1	1	0	–	1st Equalizer Tap, Real
1	1	11	–	Last Equalizer Tap, Real
2	1	–	0	1st Equalizer Tap, Imaginary
2	1	–	11	Last Equalizer Tap, Imaginary
3	0	16	–	Rotated Error, Real
4	0	–	16	Rotated Error, Imaginary
5	0	3F	–	Max AGC Gain Word
6	0	71	–	Pulse Dial Interdigit Time
7	0	7C	–	Tone Dial Interdigit Time
8	0	72	–	Pulse Dial Relay Make Time
9	0	7D	–	Pulse Dial Relay Break Time
10	0	7E	–	DTMF Duration
11	0	6D	–	Tone 1 Angle Increment Per Sample
12	0	–	6D	Tone 2 Angle Increment Per Sample
13	0	6F	–	Tone 1 Amplitude
14	0	–	6F	Tone 2 Amplitude
15	0	73	–	Max Samples Per Ring Frequency Period
16	0	74	–	Min Samples Per Ring Frequency Period
17	1	12	–	Real Part of Error
18	1	–	12	Imaginary Part of Error
19	1	–	14	Rotation Angle for Carrier Recovery
20	1	15	–	Rotated Equalizer Output, Real
21	1	–	15	Rotated Equalizer Output, Imaginary
22	1	16	–	Lower Part of Phase Error
23	1	–	16	Upper Part of Phase Error
24	1	3F	–	Upper Part of AGC Gain Word
25	1	–	3F	Lower Part of AGC Gain Word
26	1	1F	–	Average Power
27	1	2D	–	Phase Error
28	1	2F	–	Tone Power (ATBELL, BEL103 or TONEA
29	1	–	2F	Tone Detect Threshold (Call Progress Energy)
30	1	30	–	Tone Power (ATV25 or TONEB)

Table 12. DSP RAM Parameters (Cont'd)

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
31	1	31	–	Tone Power (TONEC)
32	1	36	–	Tone Detect Threshold (ATBELL, BEL103, or TONEA)
33	1	37	–	Tone Detect Threshold (ATV25 or TONEB)
34	1	38	–	Tone Detect Threshold (TONEC)
35	1	3B	–	Zero Crossing Counter
36	1	52	–	Eye Quality Monitor (EQM)
37	1	–	31	Filter 1 Coefficient $\alpha 0$
38	1	–	32	Filter 1 Coefficient $\alpha 1$
39	1	–	33	Filter 1 Coefficient $\alpha 2$
40	1	–	34	Filter 1 Coefficient $\beta 1$
41	1	–	35	Filter 1 Coefficient $\beta 2$
42	1	–	37	Filter 2 Coefficient $\alpha 0$
43	1	–	38	Filter 2 Coefficient $\alpha 1$
44	1	–	39	Filter 2 Coefficient $\alpha 2$
45	1	–	3A	Filter 2 Coefficient $\beta 1$
46	1	–	3B	Filter 2 Coefficient $\beta 2$
47	1	–	76	Filter 3 Coefficient $\alpha 0$
48	1	–	77	Filter 3 Coefficient $\alpha 1$
49	1	–	78	Filter 3 Coefficient $\alpha 2$
50	1	–	79	Filter 3 Coefficient $\beta 1$
51	1	–	7A	Filter 3 Coefficient $\beta 2$
52	1	–	45	Filter 4 Coefficient $\alpha 0$
53	1	–	46	Filter 4 Coefficient $\alpha 1$
54	1	–	47	Filter 4 Coefficient $\alpha 2$
55	1	–	48	Filter 4 Coefficient $\beta 1$
56	1	–	49	Filter 4 Coefficient $\beta 2$
57	1	1C	–	Turn-on Threshold (PSK)
58	1	32	–	Turn-off Threshold (PSK)
59	1	–	21	RLSD Turn-off Time (PSK)
60	0	–	1C	Turn-on Threshold (FSK)
61	0	–	1D	Turn-off Threshold (FSK)

*XCR if an XRAM address is listed; YCR if a YRAM address is listed.

5. Set the appropriate RAM write bits (XWT, YWT).
6. Set the appropriate RAM access bits (XACC, YACC).
7. After the DSP has transferred the contents of the interface memory RAM data registers into DSP RAM, the DSP resets the XACC and/or the YACC bit to a 0, then sets the NEWS bit to a 1 indicate DSP RAM write completion.
8. If the NSIE bit is a 1, $\overline{IRQ}$ is also asserted and NSIA is set to a 1 when NEWS is set to a 1. NSIA is cleared by writing a 0 into the NEWS bit, which also causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

Note: Steps 4 and 5 can be accomplished simultaneously.

DSP RAM Read Procedure

1. Before reading from DSP interface memory, verify that XACC and YACC are reset to a 0.
2. Load the RAM address into X RAM Address (XADD) and/or Y RAM Address (YADD) register(s).
3. Set the corresponding XCR and/or YCR bit(s) appropriately.
4. Reset XWT and/or YWT to a 0, inform the DSP that a RAM read will occur when XACC and/or YACC is set to a 1.
5. Set XACC and/or YACC to a 1 to signal the DSP to perform the RAM read.
6. After the DSP has transferred the contents of RAM into the interface memory RAM data registers, the DSP resets the XACC and/or the YACC bit to a 0, then sets the NEWS bit to a 1 to indicate DSP RAM read completion.
7. If the NSIE bit is a 1, IRQ is also asserted and NSIA is set to a 1 when NEWS is set to a 1. NSIA is cleared by writing a 0 into the NEWS bit, which also causes IRQ to return high if no other interrupt requests are pending.

Note: Steps 3 and 4 can be accomplished simultaneously.

SOFTWARE INTERFACE CONSIDERATIONS

INTERRUPT REQUEST HANDLING

DSP interface memory registers 00, 10, 1E, and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER) and register 10 is the Transmit Buffer (TBUFFER). Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits.

When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using $\overline{IRQ}$) or by being interrupted by $\overline{IRQ}$. When an interrupt enable bit and the corresponding interrupt flag are both set to a 1, $\overline{IRQ}$ is asserted and the corresponding interrupt active bit set to a 1.

The interrupt flag setting conditions are status changed detected, configuration changed acknowledged, receive buffer full and transmit buffer empty. Table 13 identifies the interrupt conditions and bits, and describes the interrupt clearing procedures.

Table 13. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
NSIA	NSIE	NEWS	New status detected (NEWS transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A, 0B, 0E, or 0F	Host writes a 0 into NEWS (Clears NSIA to a 0)
NCIA	NCIE	NEWC	New configuration acknowledged by DSP (NEWC transitioned from a 1 to a 0)	Host writes a 0 into NCIE (Clears NCIA to a 0)
TDBIA	TDBIE	TDBE	Transmitter Data Buffer is empty and can be written (TDBE transitioned from a 0 to a 1)	Host reads from or writes to register 10 (TBUFFER) (Clears TDBE and TDBIA to 0)
RDBIA	RDBIE	RDBF	Receiver Data Buffer is full and can be read (RDBF transitioned from a 0 to a 1)	Host reads from or register 00 (RBUFFER) (Clears RDBF and RDBIA to 0)

DIAL PROCEDURE

The host dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 8). The modem timing accounts for the DTMF tone duration and amplitude, pulse make/break ratio, and interdigit delay. These dialing parameters are host programmable in DSP RAM.

The level of the high DTMF tone is 2 dB greater than the level of the low DTMF tone.

The dialer default parameters are given in Table 14.

Table 14. Dial Default Parameters

Parameter	Default Value
DTMF Tone Duration	70 ms
DTMF Interdigit Delay	70 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	– 4 dBm
DTMF High Band Power Level	– 2 dBm
Pulse Relay Make Time	40 ms
Pulse Relay Break Time	60 ms
Pulse Interdigit Delay	750 ms

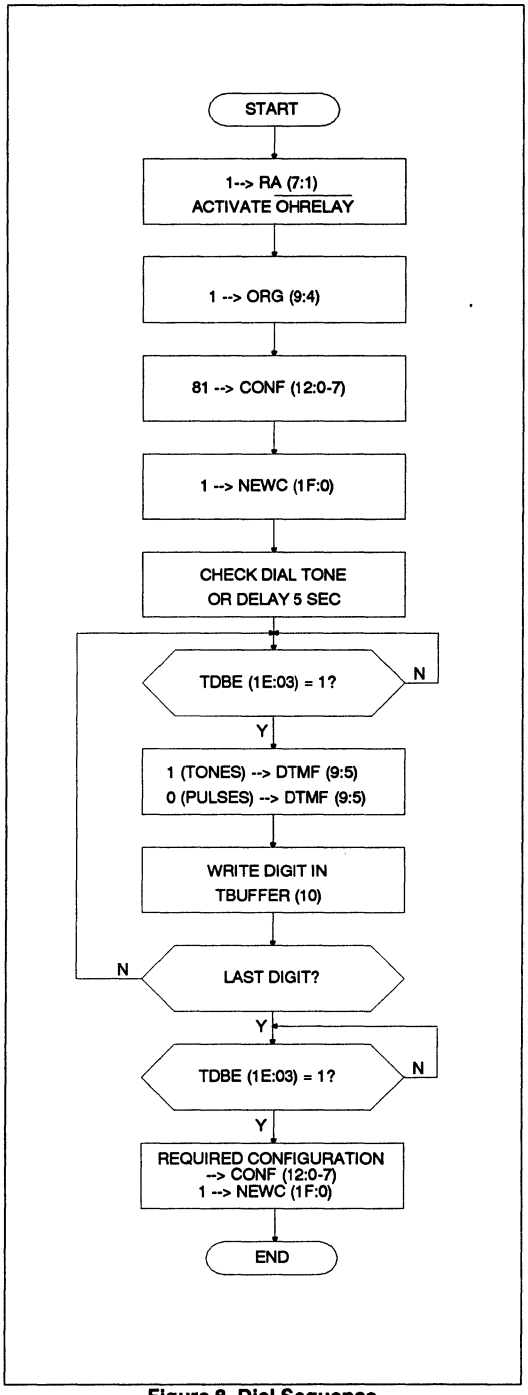


Figure 8. Dial Sequence

DESIGN CONSIDERATIONS

REQUIRED MODEM INTERFACE CIRCUIT

The RC2424DP/DS is supplied as two VLSI devices to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit (Figure 9) and parts list (Table 15) illustrate the connections and components required to connect the modem to the OEM electronics.

DAA INTERFACE

The following discussion of the interface to the integrated analog device is presented to enable designers to modify the design of the recommended line interface circuit. Also, the designer may wish to incorporate an existing line interface design with the modem device set.

Receive Input

Receive In (REC IN) and Receive Out (REC OUT) are pins associated with an integrated uncommitted operational amplifier inside the IA device. In conjunction with the three discrete components shown (R13, R14 and C11), the amplifier forms a first order lowpass antialiasing filter. This filter's function is to attenuate high frequency noise near and above the effective sampling rate of the integrated bandsplit filters (230.4 KHz).

The design of the modem requires that the pole of the anti-aliasing filter be fixed at 2337 Hz. This is calculated using the formula

$$\text{Filter Pole (Hz)} = 1/(2\pi \cdot R14 \cdot C11)$$

The recommended values of 68.1 KΩ for R14 and 1000 pF for C11 give the correct value for the filter pole. Some flexibility in choosing the component values for R14 and C11 is permissible provided that the pole of the filter is maintained within approximately ±5% of the correct value. When calculating the pole of the filter, component tolerances should be carefully considered.

Transmit Output

An external discrete smoothing filter must be added to the Transmit Output (TRAN OUT) signal to attenuate the high frequency aliases generated by the integrated switched capacitor filters. This is necessary to meet FCC requirements on transmitted high frequency energy. The pole of this filter may be calculated using the same formula as for the receiver filter, i.e.,

$$\text{Filter Pole (Hz)} = 1/(2\pi \cdot R16 \cdot C12)$$

The components values of R16 = 68.1 KΩ and C12 = 1000 pF place the pole at 2337 Hz. This may seem unusual as the response of a smoothing filter is generally designed to be flat in the band of interest, and then rolling off before the sampling rate. The bandsplit filter inside the IA is pre-distorted so that when cascaded with an external continuous first order smoothing filter, the response across the band is flat.

Some flexibility in choosing the values for R16 and C12 is permissible, provided some guidelines are followed. The choice of R16 and C12 must position the filter pole within ±5% of 2337 Hz.

The TRAN OUT integrated driver can drive a resistive load as low as 10 KΩ . This drive capability is desirable for the FCC Part 68 defined "programmable" mode.

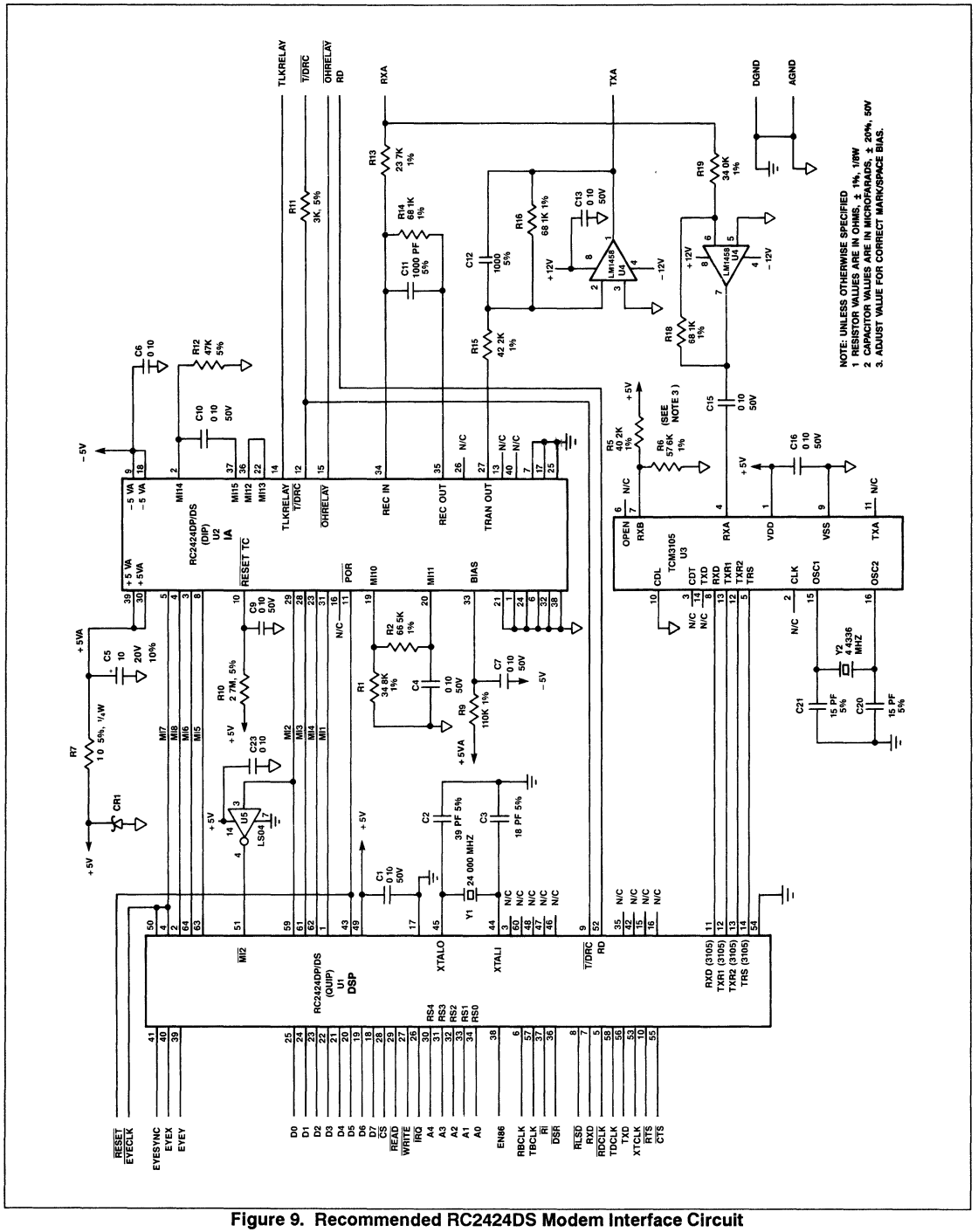


Figure 9. Recommended RC2424DS Modem Interface Circuit

Table 15. Recommended Modem Interface Circuit

Qty	Part Number	Description
1	U1	Rockwell RC2424DP/DS DSP
1	U2	Rockwell RC2424DP/DS IA
1	U3	TCM3105 FSK Modulator/ Demodulator
1	U4	1458 Dual Op
1	U5	SN74LS04 Hex Inverter
1	Y1	24.00014 MHz Crystal
1	Y2	4.4336 MHz Crystal
10	C1, C4, C6, C7, C9, C10,C13, C15, C16, C23	0.10 µF, 20%, 50V
1	C2	39 pF, 5%, 50V
1	C3	18 pF, 5%, 50V
1	C5	10 µF, 5%, 50V
2	C11, C12	1000 pF, 5%, 50V
2	C20, C21	15 pF, 5%, 50V
1	R1	34.8K Ω, 1%, 1/8 W
1	R2	66.5K Ω, 1%, 1/8 W
1	R5	40.2K Ω, 1%, 1/8 W
1	R6	57.6K Ω, 1%, 1/8 W
1	R7	1 Ω, 5%, 1/4 W
1	R9	110K Ω, 1%, 1/8W
1	R10	2.7M Ω, 5%, 1/8 W
1	R11	3K Ω, 5%, 1/8 W
1	R12	47K Ω, 5%, 1/8 W
1	R13	23.7 K Ω, 1%, 1/8 W
3	R14, R16, R18	68.1K Ω, 1%, 1/8 W
1	R15	42.2K Ω, 1%, 1/8 W
1	R19	34.0K Ω, 1%, 1/8 W
1	CR1	Schottky Diode, LL103B

PC BOARD LAYOUT GUIDELINES

The following guidelines should be adhered to when laying out a printed circuit board for the RC2424DP/DS devices. The pin numbers reflect the DSP 64-pin QUIP and the IA 40-pin DIP packages.

1. The DSP, IA and all supporting analog circuitry, including the data access arrangement should be located on the same area of printed circuit board.
2. The DSP device grounds should be routed separately from the IA device.
3. The DSP should be located on the pin 1 side of the IA device.
4. IA digital signals (pins 3, 4, 5, 8, 10, 12, 23, 28, 29, and 31) should be routed directly to the DSP, avoiding all analog components.
5. Routing of the RC2424DP/DS signals should provide maximum isolation between noise sources and noise senitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The DSP and IA noise source, neutral, and noise sensitive pins are listed in Table 16.
6. A 1.0Ω/10 µF RC network is needed to decouple the +5V supply. This must be done at the IA device to isolate it from the DSP device.
7. As a general rule, digital signals should be routed on the component side of the PCB while the analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
8. All power traces should be at least a 0.1 inch width.
9. The analog components should be located on the pin 40 side of the 40-pin IA device.
10. The IA AGND pins (1, 6, 21, 24, 32, and 38) and the DGND pins (7 and 25) should be tied together as ground directly under the device.
11. A 0.1 µF ceramic capacitor is used to decouple the –5V supply. This should be done in the immediate proximity of the IA device.
12. All circuitry connected to crystal pins 44 and 45 on the DSP device should be kept short to prevent stray capacitance from affecting the oscillator.

Table 16. RC2424DP/DS Pin Noise Characteristics

Device	Function	Noise Source	Neutral	Noise Sensitive
DSP 64-Pin QUIP	+5V DGND Crystal Control Eye Pattern V.23 Interface Host Bus Interface Serial Interface IA Interface No Connection	 4, 41 11-13 5-7, 53, 56-58 1-2, 50-51, 59, 61-64 	49, 17, 54 9, 38, 43, 52 39-40 14 18-34 8,10,36-37,55 3, 15-16, 35, 42, 46-48, 60	 44, 45
DSP 68-Pin PLCC	+5V DGND Crystal Control Eye Pattern V.23 Interface Host Bus Interface Serial Interface IA Interface No Connection	 27, 56 63, 65 39, 42-44, 57-59 36-37, 45, 47-50, 52-53 	35 1, 15, 19, 40, 51, 54 24, 29, 38, 61 25-26 66 2-14, 16-18, 20, 22-23, 41, 60, 62 21, 28, 32-34, 46, 55, 67-68	 30-31
IA 40-Pin DIP	+5VA –5VA DGND AGND Control Analog DSP Interface No Connection	 3-5, 8, 23, 28-29, 31 	30, 39 9, 18 7, 17, 25 1, 6, 21, 24, 32, 38 10, 14-15 12 11, 13, 16, 40	 2, 19-20, 22, 26-27, 33-37
IA 44-Pin PLCC	+5VA –5VA DGND AGND Control Analog DSP Interface No Connection	 4-5, 7, 10, 25, 31-32, 34 	33, 43 11, 20 9, 19, 27 2, 8, 23, 26, 35, 42 12, 16-17 14 1, 6, 13, 15, 18, 28, 39, 44	 3, 21-22, 24, 29-30, 36-38, 40-41

GENERAL SPECIFICATIONS

Table 17. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Maximum) @ 0°C
+ 5 VDC	±5%	85 mA	130 mA
–5 VDC	±5%	20 mA	40 mA
Note: Input voltage ripple ≤1 volts peak-to-peak.			

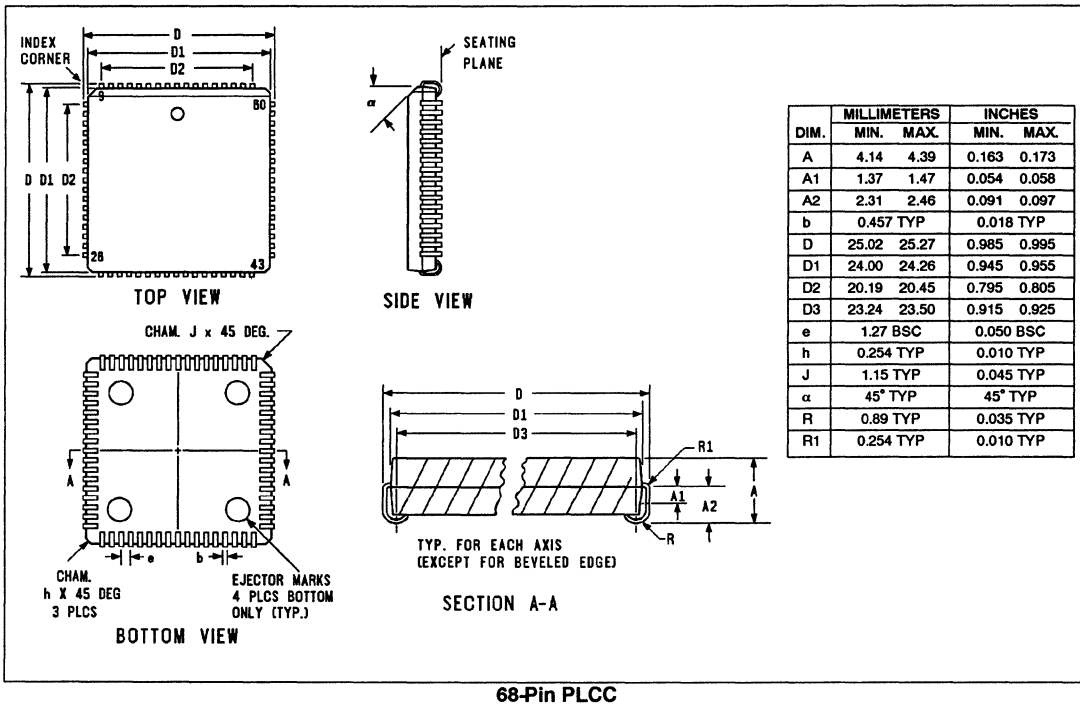
Table 18. Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to + 60°C (32°F to 140° F)
Storage	– 40°C to + 80°C (–40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	– 200 feet to + 10,000 feet

Table 19. Crystal Specifications

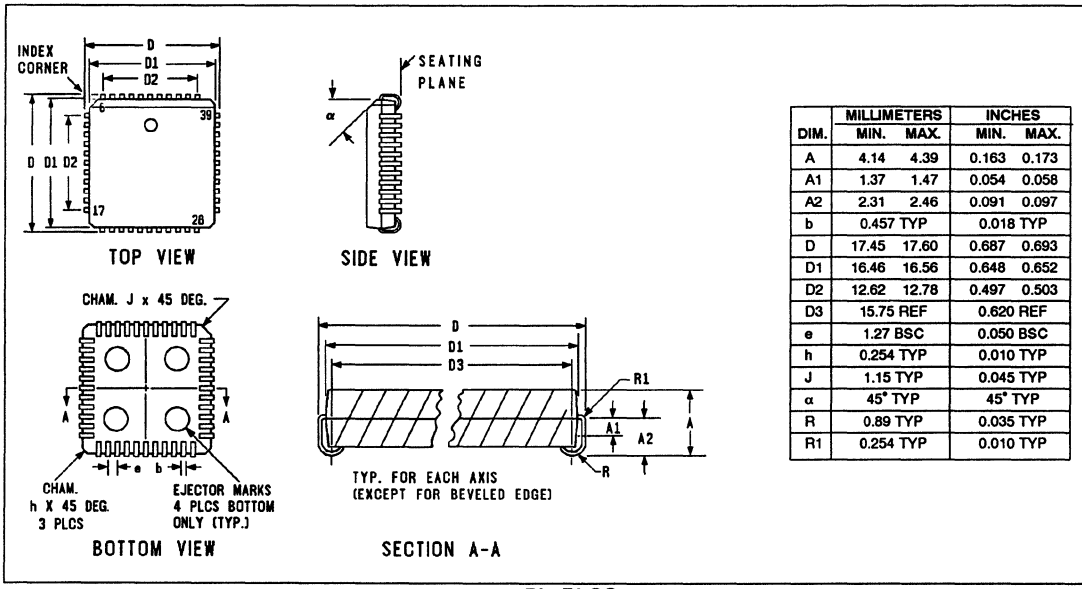
Parameter	Value
Operating Temperature	0°C to 60°C
Storage Temperature	–55°C to 85°C
Nominal Frequency @ 25°C	24.00014 MHz
Frequency Tolerance @ 25°C	±0.0015% (±15 PPM)
Temperature Stability @ T_A = 0°C to 60°C	±0.003% (±15 PPM)
Calibration Mode	Parallel resonant
Shunt Capacitance	7 pF max.
Load Capacitance	18 ±0.2 pF
Drive Level	2.5 mW max., Test at 20 nanowatts
Aging, per Year Max.	0.0005% (5PPM)
Oscillation Mode	Fundamental
Series Resistance	25 ohms max.
Max. Frequency Variation with 16.5 or 19.5 pF Load Capacitance	+0.0035% (+35 PPM)
Third Lead	Required
Sleeving	Required

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23.50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	

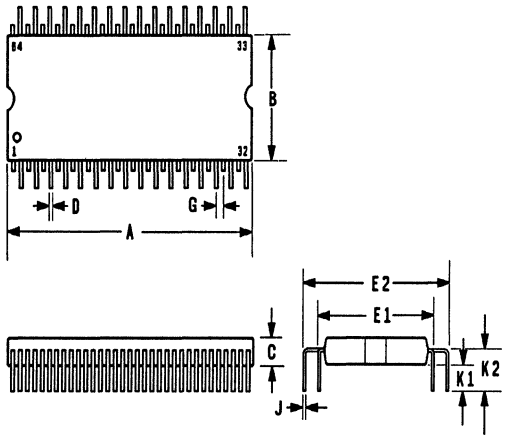
68-Pin PLCC



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	

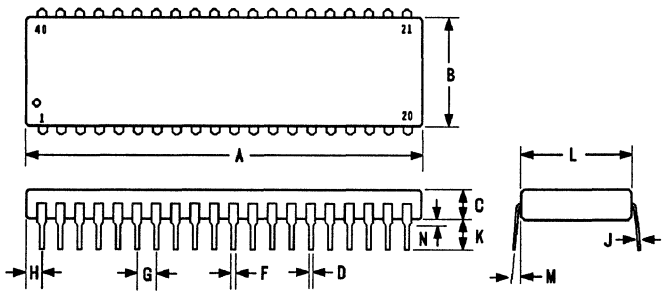
44-Pin PLCC

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	41.10	41.61	1.618	1.638
B	17.02	17.23	0.670	0.690
C	3.56	4.58	0.140	0.180
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	2.92	3.18	0.115	0.125
K2	4.83	5.34	0.190	0.210

64-Pin Plastic QUIP



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

40-Pin Plastic DIP

Rockwell

RC2324DP/DS 2400 bps Full-Duplex Modem Data Pump Device Set

INTRODUCTION

The Rockwell RC2324DP/DS is a 2400 bps, full-duplex, OEM, data pump modem device set. The RC2324DP/DS operates over the public switched telephone network (PSTN), as well as on point-to-point leased lines.

The set consists of two CMOS VLSI components—a digital signal processor (DSP) device and an integrated analog (IA) device. The DSP is available in a 64-pin quad in-line package (QUIP) or a 68-pin plastic leaded chip carrier (PLCC) package. The IA device is available in a 40-pin dual in-line package (DIP) or a 44-pin PLCC package.

The RC2324DP/DS modem meets the requirements specified in CCITT V.22 bis, V.22 A/B, and V.21, as well as Bell 212A and Bell 103.

In addition, the SDLC/HDLC support eliminates the cost of an external serial input/output (SIO) device in products incorporating error correction protocols.

FEATURES

- CMOS DSP and IA devices
- 2-wire full-duplex operation
- Compatible configurations:
  - –CCITT V.22 bis, V.22A/B
  - –CCITT V.21 and V.23
  - –Bell 212A and 103
- Receive dynamic range: –9 dBm to –43 dBm
- Maximum transmit level: 0.0 dBm ±1.0 dB, programmable in 1 dB steps
- Multi-modem detection support
  - –Programmable tone detect bandpass filters
  - –Zero-crossing detector
- V.22 bis fallback/fall-forward – 2400/1200 bps
- Serial data both synchronous and asynchronous
  - –Synchronous:
    2400, 1200, 600 bps ±0.01% (PSK modulation)
    Internal/external/slave clock selection
  - –Asynchronous:
    7, 8, 9, 10, or 11 bits per character
    2400, 1200, 600 bps +1% (or 2.3%), –2.5% (PSK modulation)
    0-75, 0-300, 0-1200 bps (FSK modulation)
- Parallel data both synchronous and asynchronous
  - –Synchronous:
    Normal sync: 8-bit data for transmit and receive
  - –SDLC/HDLC support:
    Transmitter: Flag generation, 0 bit stuffing, CCITT CRC generation
    Receiver: Flag detection, 0 bit un-stuffing, CCITT CRC checking
  - –Asynchronous:
    5, 6, 7, or 8 data bits per character
    Odd/even parity generation/checking (or 9^{th} data bit)
    2400, 1200, 600 bps +1% or (2.3%), –2.5% (PSK modulation)
    75, 300, 1200 bps (FSK modulation)

- Programmable ring detect
  - –Min and max frequency range
- Programmable dialer
  - –Make/break times for pulse dialling
  - –DTMF on time for touch-tone dialling
  - –Interdigit times for both pulse and tone dialling
  - –DTMF Level: 0.0 dBm ± 1.0 dB (high tone level is 2.0 dB ± 0.5 dB above low tone level)
- Diagnostics
  - –Read/write RAM
  - –Serial eye pattern output
  - –EQM value in RAM
- Host bus interface memory for configuration, control, and parallel data; compatible with either 8086 or 6502 microprocessor bus
- RS-232C (TTL compatible) interface for RTS control and serial data
- Adaptive and fixed compromise equalization
- Test Configurations:
  - –Local analog loopback
  - –Local digital loopback
  - –Remote digital loopback
- Answer and originate handshake
- Leased line operation
- Power requirements:
  - –± 5 Vdc ± 5%
  - –500 mW typical

R2424/RC2424 COMPATIBILITY

A high performance modem engine, the RC2324DP/DS is the functional and performance equivalent of Rockwell's R2424DS modem with the following enhancements:

- –2-device implementation in CMOS
- –V.21 and V.23 interface
- –Asynchronous/synchronous parallel data transfer over the microprocessor bus interface
- –Extended 2.3% overspeed in asynchronous, DPSK/QAM modes
- –SDLC/HDLC framing in parallel data mode
- –Additional configuration and control capabilities

These options and enhancements, combined with a user accessible, dual port interface memory (RAM) in the DSP, offer maximum flexibility in customizing the RC2324DP/DS to meet a wide variety of functional requirements.

The RC2324DP/DS is a plug-compatible replacement for the RC2424DP/DS.

The RC2324DP/DS device set, with the addition of a few external filter components, interfaces easily to a data access arrangement (DAA). The RC2324DP/DS general interface is illustrated in Figure 1.

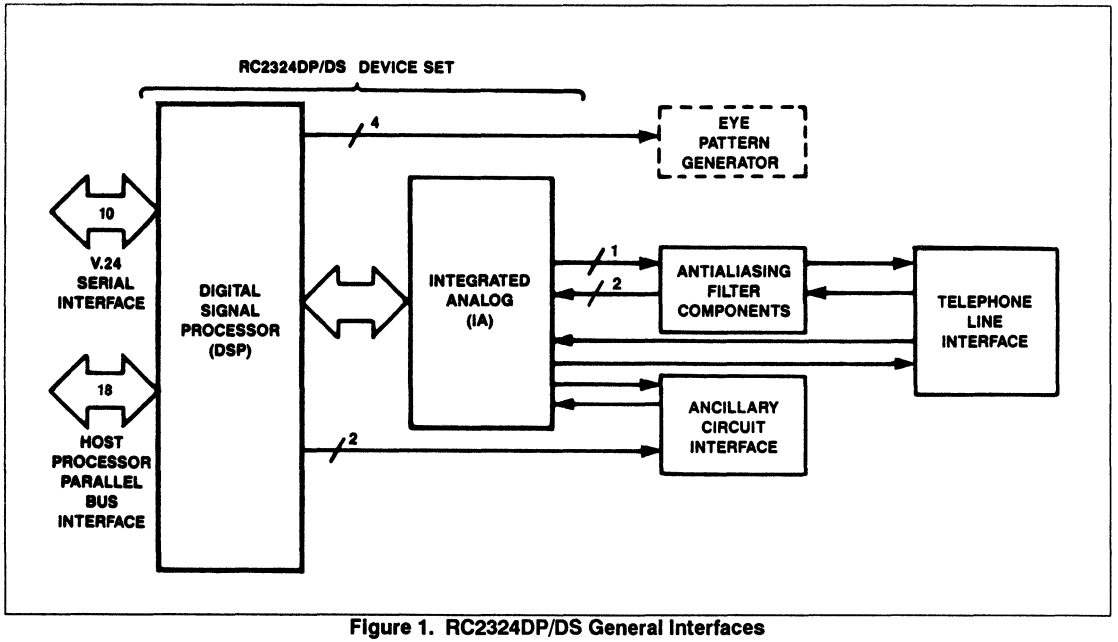


Figure 1. RC2324DP/DS General Interfaces

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES, AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1. The modem configuration is established by the CONF bits.

Note: Bit names refer to control bits in DSP Interface Memory which are set or reset by the host processor (see Software Interface Section, Figure 7 and Table 11).

TONE GENERATION

Answer Tone: A CCITT (2100 ± 15 Hz) or Bell (2225 ± 10 Hz) answer tone is generated depending on the selected configuration.

Guard Tone: A guard tone of 1800 ± 20 Hz (GTS bit = 0) or 550 ± 20 Hz (GTS bit = 1) can be generated (enabled by the GTE bit). The level of transmitted power is 6 ± 1 dB or 3 ± 1 dB below the level of the data power in the main channel for the 1800 Hz or 550 Hz guard tone, respectively. The total power transmitted to the line is the same whether or not a guard tone is enabled. When a guard tone is generated, the main channel transmit path gain is reduced by 0.97 dB or 1.76 dB for the 1800 Hz or 550 Hz guard tone, respectively.

Guard tone on/off must be controlled by the host depending on the state of the handshake sequence, i.e., the host should enable guard tone when DSR is turned on.

DTMF Tones: When Dial/Call Progress configuration is selected (CONF bits = 81) and the DTMF bit is set to a 1, dual tone multi-frequency (DTMF) tones can be generated. The specific DTMF tone generated is specified by the host loading the Transmitter Data Buffer (TBUFFER) with the appropriate digit code shown in Table 2.

User Defined Tones: When Tone Generator/Tone Detector configuration is selected (CONF bits = 80), a user-defined single or dual tone can be generated. In this mode, the transmitter immediately begins sending the frequencies specified in DSP RAM. The tones will remain on as long as Tone Generator/Tone Detector configuration is selected and the tone amplitudes are greater than zero. Setting one of the two amplitudes to zero selects single tone frequency.

Note: Frequencies from 0 to 1675 Hz can be sent when the ORG bit is set, or frequencies from 1925 Hz to 2875 Hz can be sent when the ORG bit is cleared. 1800 Hz frequency can be sent by setting the GTE bit with GTS = 0 and ORG = 0.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Transmitter Carrier Frequency (Hz) ±0.01%		Data Rate (bps)	Baud	Bits Per	Constellation
		Answer[2]	Originate[2]	± 0.01%	(Symbols/Sec.)	Symbol	Points
V.22 bis	QAM	2400	1200	2400[3]	600	4	16
V.22A/B	DPSK	2400	1200	1200[3]	600	2	4
		2400	1200	600[3]	600	1	2
Bell 212A	DPSK	2400	1200	1200[3]	600	2	4
Bell 103	FSK	2225 M 2025 S	1270 M 1070 S	300[4]	300[4]	1	1
V.21	FSK	1650 M 1850 S	980 M 1180 S	300[4]	300[4]	1	1
V.23 Forward Channel	FSK	1300 M 2100 S	1300 M 2100 S	1200[4]	1200[4]	1	1
V.23 Backward Channel	FSK	390 M 450 S	390 M 450 S	75[4]	75[4]	1	1

Notes:
1. Modulation legend: QAM Quadrature Amplitude Modulation; DPSK Differential Phase Shift Keying; FSK Frequency Shift Keying
2. M indicates a mark condition; S indicates a space condition.
3. Synchronous accuracy = ±0.01%; asynchronous accuracy = –2.5% to +1.0% (+2.3% if extended overspeed is selected).
4. Value is upper limit for serial (e.g., 0-300).

TONE DETECTION

Answer Tone and Call Progress Tones: When Dial/Call Progress configuration is selected (CONF bits = 81), tones can be detected as follows:

Call progress frequency range: 340 ± 5 Hz to 640 ± 5 Hz

Status Bit: TONEA

Answer tones (2100 ± 15 Hz or 2225 ± 10 Hz) or Bell FSK originate tone (1270 ± 10 Hz)

Detection level:0 dBm to –43 dBm

Default detection level: –43 dBm

Response time: 25 ± 2 ms

Status Bits: ATV25, ATBELL (ORG=1), BEL103 (ORG=0)

Tones are detected as energy above a certain threshold within a digital bandpass filter. The pass band of the dual bi-quad infinite impulse response (IIR) filter (Call Progress) or the single bi-quad IIR filter (answer tone or Bell FSK originate) can be changed by writing new coefficients to DSP RAM. The tone detect threshold can also be changed in DSP RAM.

V.23 and V.21 Tones: When Tone Generator/Tone Detector configuration is selected (CONF bits = 80), tones can be detected as follows:

V.23 forward channel mark: 1300 ± 10 Hz

Status Bit: TONEA

V.23 backward channel mark: 390 ± 10 Hz

Status Bit: TONEB

V.21 high band mark (1650 ± 10 Hz) or low band mark (980 ± 10 Hz)

Table 2. Dial Digits/Tone Pairs

Hex Code	Dial Digit	Tone Pair (Hz)	(Hz)
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

Status Bit: TONEC

Detection level: 0 dBm to –43 dBm

Default detection level: –43 dBm

Response time: 25 ± 2 ms

Tones are detected as energy above the threshold within a digital bandpass filter. These filters are single bi-quad IIR filters*. The pass bands can be changed by writing new coefficients to DSP RAM. The tone detect threshold can also be changed in the DSP RAM.

*Except the filter represented by TONEA in Dial/Call Progress configuration, which is a dual biquad IIR filter.

Zero Crossing Detector: A zero crossing detector is always available. The detector can measure tone frequencies between 100 Hz and 3000 Hz. The zero crossing counter increments for both positive and negative zero crossings.

DATA ENCODING

The data encoding conforms to CCITT Recommendations V.22 bis, V.22A/B, V.23, or V.21, or to Bell 212A or 103, depending on the selected configuration.

EQUALIZERS

Equalization functions are incorporated that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer. A 17-tap automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations. Updating of the taps can be enabled or disabled (EQFZ). The equalizer taps can also be reset (EQRES).

Fixed Compromise Equalizer. A fixed compromise equalizer is provided in the transmitter. The equalizer can be enabled or disabled (CEQ bit).

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by a square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ± 150 microseconds over

Table 3. RTS - CTS Response Time

CTS Transition	Configuration	Constant Carrier	Controlled Carrier
OFF to ON	V.22 bis	≤2 ms	270 ms
	V.22	≤2 ms	270 ms
	Bell 212A	≤2 ms	270 ms
	V.21	2-5 ms	2-5 ms
	Bell 103	2-5 ms	2-5 ms
	V.23	5-20 ms	5-20 ms
ON to OFF	All	≤2 ms	≤2 ms

Note: The CTS OFF to ON response time is host programmable in DSP RAM for some configurations.

the frequency range 900 Hz to 1500 Hz (low channel) and 2100 Hz to 2700 Hz (high channel).

TRANSMIT LEVEL

The default transmitter output level is –6.0 dBm ±1.0 dB. The output level can be selected from 0 dBm to –15 dBm in 1 dB steps (TLVL bits).

TRANSMIT TIMING

Transmitter timing is selectable between internal (±0.01%), external , or loopback (TXCLK bits). When external clock is selected, the external clock rate must equal the desired data rate ±0.01% with a duty cycle of 50 ± 20%.

SCRAMBLER/DESCRAMBLER

A self-synchronizing scrambler/descrambler satisfying the applicable CCITT recommendation or Bell specification is incorporated. The scrambler and descrambler can be enabled or disabled (SDIS and DDIS bits, respectively)

RECEIVE LEVEL

The receiver satisfies performance requirements for received line signals from –9 dBm to –43 dBm. The received line signal is measured at the Receiver Analog (RXA) input.

RECEIVER TIMING

A ± 0.01% frequency error in the associated transmit timing source can be tracked.

CARRIER RECOVERY

A ± 7 Hz frequency offset in the received carrier can be tracked with less than a 0.2 dB degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (RLSD) output is off.

RTS - CTS RESPONSE TIME

The response times of CTS relative to a corresponding transition of RTS are listed in Table 3. The response time depends on the receiver operating in either constant carrier or controlled carrier mode (CC bit).

ASYNC/SYNC, SYNC/ASYNC CONVERSION

An asynchronous-to-synchronous converter is provided in the transmitter, and a synchronous-to-asynchronous converter is provided in the receiver. Asynchronous or synchronous mode is selected by the ASYNC bit. The asynchronous character format is 1 start bit, 5 to 8 data bits (WDSZ bits), an optional parity bit (PARSL and PEN bits), and 1 or 2 stop bits (STB bit). Valid character sizes, including all bits, are 7, 8, 9, 10 or 11 bits per character.

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters.

Two ranges of signaling rates are provided (selectable by the EXOS bit):

Basic range: +1% to –2.5%

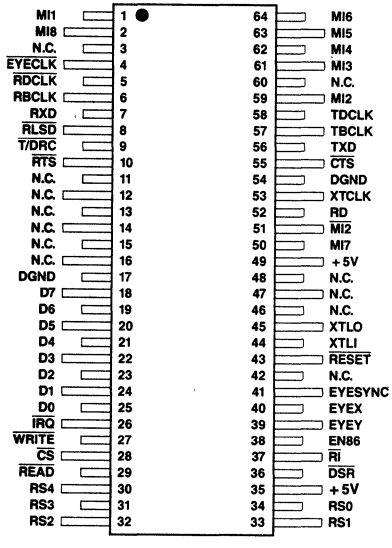
Extended overspeed range: +2.3% to –2.5%

Break is handled in the transmitter and receiver as described in V.22 bis. If the RC2324DP/DS transmitter detects M to 2M + 3 bits of "start" polarity from the DTE, where M is the number of bits per character, the RC2324DP/DS will transmit 2M + 3 bits of start polarity. If the modem detects more then 2M +3 bits of start polarity, it will transmit all these bits as start polarity.

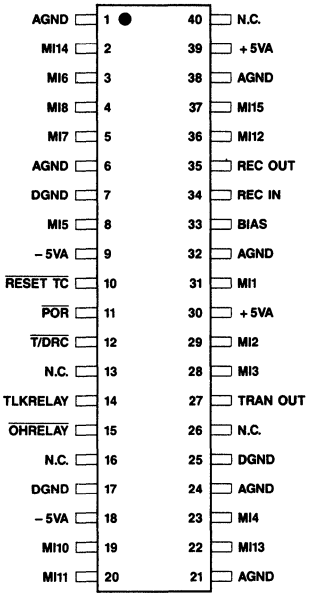
The RC2324DP/DS receiver will output the 2M + 3 or more bits of start polarity on RXD and will set the BRKD bit.

PIN ASSIGNMENTS

The RC2324DP/DS pin assignments are shown in Figure 2. The pin assigments are listed by pin number in Tables 4 and 5 for the DSP and IA devices, respectively.

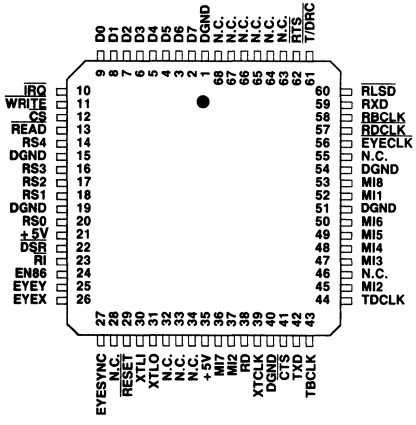


64-PIN QUIP (DSP)

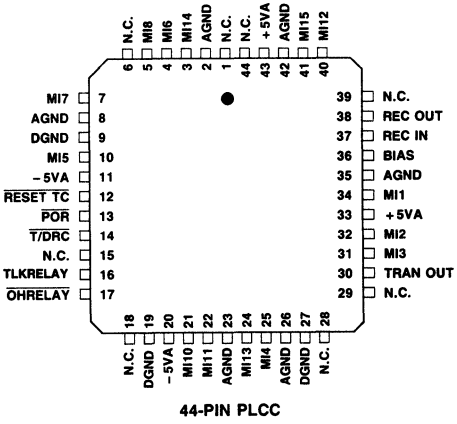


40-PIN DIP (IA)

a. QUIP/DIP Set



68-PIN PLCC



44-PIN PLCC

b. PLCC Set

Figure 2. RC2324DP/DS Device Set Pin Assignments

Table 4. RC2324DP/DS DSP Pin Assignments

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Name	I/O Type
52	1	MI1	
53	2	MI8	
54	–	DGND	
55	3	N.C.	
56	4	EYECLK	OA
57	5	RDCLK	OA
58	6	RBCLK	OA
59	7	RXD	OA
60	8	RLSD	OA
61	9	T/DRC	IA
62	10	RTS	IA
63	11	N.C.	
64	12	N.C.	
65	13	N.C.	
66	14	N.C.	
67	15	N.C.	
68	16	N.C.	
1	17	DGND	
2	18	D7	IA/OB
3	19	D6	IA/OB
4	20	D5	IA/OB
5	21	D4	IA/OB
6	22	D3	IA/OB
7	23	D2	IA/OB
8	24	D1	IA/OB
9	25	D0	IA/OB
10	26	IRQ	OC
11	27	WRITE	IA
12	28	CS	IA
13	29	READ	IA
14	30	RS4	IA
15	–	DGND	
16	31	RS3	IA
17	32	RS2	IA
18	33	RS1	IA
19	–	DGND	
20	34	RS0	IA
21	35	+5V	
22	36	DSR	OB
23	37	RI	OB
24	38	EN86	IA
25	39	EYEY	OB
26	40	EYEX	OB
27	41	EYESYNC	OB
28	42	N.C.	
29	43	RESET	IA
30	44	XTLI	I
31	45	XTLO	O
32	46	N.C.	
33	47	N.C.	
34	48	N.C.	
35	49	+5V	
36	50	MI7	
37	51	MI2	
38	52	RD	IA
39	53	XTCLK	IA
40	54	DGND	
41	55	CTS	OA
42	56	TXD	IA
43	57	TBCLK	OA
44	58	TDCLK	OA
45	59	MI2	
46	60	N.C.	
47	61	MI3	
48	62	MI4	
49	63	MI5	
50	64	MI6	
51	–	DGND	

Notes:
MI = Modem Interconnection (e.g., MI7), see Figure 3.
N.C. = No Connection, leave pin disconnected (open).
I/O Type: See Table 7.

Table 5. RC2324DP/DS IA Pin Assignments

44-Pin PLCC Pin Number	40-Pin DIP Pin Number	Signal Name	I/O Type
1	–	N.C.	
2	1	AGND	
3	2	MI14	
4	3	MI6	
5	4	MI8	
6	–	N.C.	
7	5	MI7	
8	6	AGND	
9	7	DGND	
10	8	MI5	
11	9	–5VA	
12	10	RESET TC	IA
13	11	POR	IA/OA
14	12	T/DRC	IA
15	13	N.C.	
16	14	TLKRELAY	OD
17	15	OHRELAY	OD
18	16	N.C.	
19	17	DGND	
20	18	–5VA	
21	19	MI10	
22	20	MI11	
23	21	AGND	
24	22	MI13	
25	23	MI4	
26	24	AGND	
27	25	DGND	
28	–	N.C.	
29	26	N.C.	
30	27	TRAN OUT	O (DD)
31	28	MI3	
32	29	MI2	
33	30	+5VA	
34	31	MI1	
35	32	AGND	
36	33	BIAS	I
37	34	REC IN	I (DB)
38	35	REC OUT	O (DA)
39	–	N.C.	
40	36	MI12	
41	37	MI15	
42	38	AGND	
43	39	+5VA	
44	40	N.C.	

Notes:
MI = Modem Interconnection (e.g., MI7), see Figure 3.
N.C. = No Connection, leave pin disconnected (open).
I/O Type: See Tables 7 and 8.

HARDWARE INTERFACE SIGNALS

The RC2324DP/DS hardware functional interface signals are shown in Figure 3. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{IRQ}$). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals are organized into functional groups. These signals, along with their interface circuit type codes, are listed in Table 6. The digital and analog interface characteristics are defined in Tables 7 and 8, respectively.

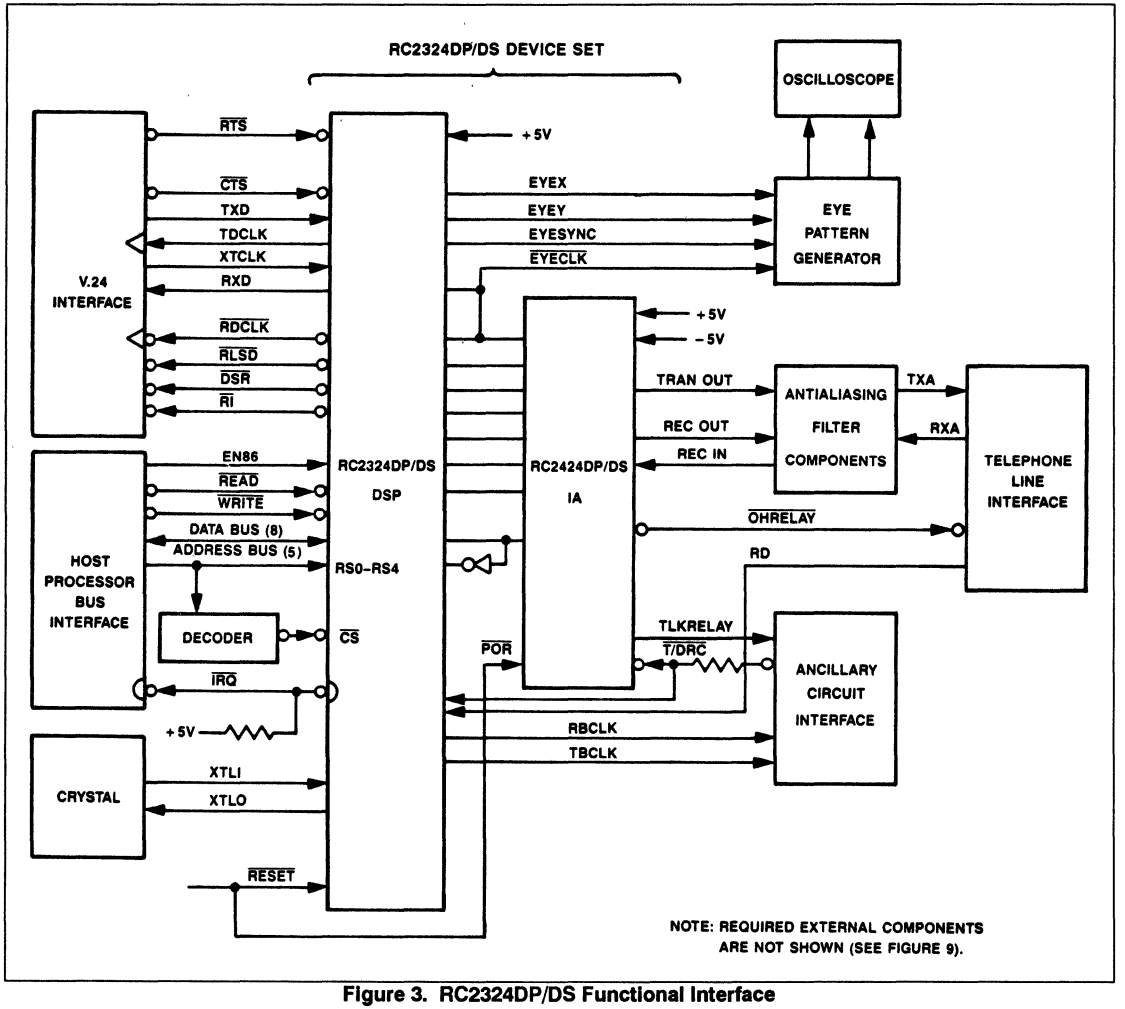


Figure 3. RC2324DP/DS Functional Interface

Table 6. RC2324DP/DS Hardware Interface Signals

Name	I/O Type	Description
DSP and IA Overhead		
AGND	GND	Analog Ground Return
DGND	GND	Digital Ground Return
+5V	PWR	+5 Volt Supply (DSP & IA)
–5V	PWR	–5 Volt Supply (IA)
RESET	IA	Reset (DSP)
POR	IA/OA	Power-On-Reset (IA)
RESET TC	IA	Reset Time Constant (IA)
XTLI	I	Crystal In
XTLO	O	Crystal Out
DSP/Host Processor Pararallel Bus Interface		
D7	IA/OB	Data Bus (8-Bits)
D6	IA/OB	
D5	IA/OB	
D4	IA/OB	
D3	IA/OB	
D2	IA/OB	
D1	IA/OB	
D0	IA/OB	
RS4	IA	Register Select (5-Bits)
RS3	IA	
RS2	IA	
RS1	IA	
RS0	IA	
CS	IA	Chip Select
READ (φ2)	IA	Read Enable or φ2 Clock
WRITE (R/W)	IA	Write Enable or Read/Write
IRQ	OC	Interrupt Request
EN86	IA	Enable 8086 Bus
DSP/Line Interface		
RD	IA	Ring Detect

Table 6. RC2324DP/DS Hardware Interface Signals (Cont'd)

Name	I/O Type	Description
DSP/V.24 Interface		
XTCLK	IA	External Transmit Clock
TDCLK	OA	Transmitter Data Clock
RDCLK	OA	Receiver Data Clock
RTS	IA	Request-To-Send
CTS	OA	Clear-To-Send
DSR	OB	Data Set Ready
TXD	IA	Serial Transmit Data
RXD	OA	Serial Receive Data
RLSD	OA	Received Line Signal Detector
RI	OB	Ring Indicator
IA/External Filter Components		
REC IN	DB	IA Receiver Op Amp Input
REC OUT	DA	IA Receiver Op Amp Output
TRAN OUT	DD	IA Transmitter Analog Output
External Filter Components/Line Interface		
RXA	DE	Receive Analog Input
TXA	DF	Transmit Analog Output
IA/Line Interface		
OHRELAY	OD	Off-Hook Relay Driver
DSP/Ancillary Circuits		
TBCLK	OA	Transmit Baud Clock
RBCLK	OA	Receive Baud Clock
IA/Ancillary Circuits		
T/DRC	IA	Uncommitted Relay Control
TLKRELAY	OD	Uncommitted Relay Driver
DSP/Eye Pattern Generator (Diagnostic Circuit)		
EYEX	OB	Eye Pattern Data X-Axis
EYEY	OB	Eye Pattern Data Y-Axis
EYECLK	OA	Eye Pattern Clock
EYESYNC	OB	Eye Pattern Sync

NOTES: 1. I/O types are described in Table 7 (digital signals) and Table 8 (analog signals).
2. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Table 7. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage (Types A & B)	V_{IH}	2.0	–	V_{CC}	Vdc	
Input High Current	I_{IL}	–	–	40	μA	V_{CC} = 5.25V, V_{IN} = 5.25V
Input Low Voltage (Types A & B)	V_{IL}	–0.3	–	0.8	Vdc	
Input Low Current	I_{IH}	–	–	–400	μA	V_{CC} = 5.25V
Input Leakage Current	I_{IN}	–	–	±2.5	μA	V_{IN} = 0 to +5V, V_{CC} = 5.25V
Output High Voltage	V_{OH}				Vdc	
Type A and B		3.5	–	–		I_{LOAD} = – 100 μA
Type D		–	–	V_{CC}		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				Vdc	
Type A and C		–	–	0.4		I_{LOAD} = 1.6 mA
Type B		–	–	0.4		I_{LOAD} = 0.8 mA
Type D		–	0.75	–		I_{LOAD} = 15 mA
Three–State Input Current (Off)	I_{TSI}	–	–	±10	μA	V_{IN} = 0.4 to V_{CC} –1
Power Dissipation	P_D	–	530	850	mW	

Table 8. Analog Interface Characteristics

Name	Type	Characteristic
REC OUT	DA	1458 type op amp output Dynamic range: –9 dBm to –43 dBm
REC IN	DB	1458 type op amp input
TRAN OUT	DD	1458 type op amp output P_O (High Band) = –0.5 dBm P_O (Low Band) = –2.5 dBm
RXA	DE	Input impedance: 68.1 KΩ ± 1% Receive level: –9 dBm
TXA	DF	1458 type op amp output Output level: 0 dBm ±1 dB

OVERHEAD SIGNALS

Overhead signals include power, ground, reset, and crystal signals.

+ 5V Supply

+5V ± 5% is required by both the DSP and the IA devices.

–5V Supply

–5V ± 5% is required by the IA device.

DSP Reset ($\overline{\text{RESET}}$)

The active low $\overline{\text{RESET}}$ input resets the internal DSP logic. Upon transition of $\overline{\text{RESET}}$ from low-to-high, the DSP interface memory bits are set to the default values shown in Table 11.

During DSP power turn-on, $\overline{\text{RESET}}$ must be held low for at least 0.5 microseconds after V_{CC} operating voltage is attained for the internal clock oscillator to stabilize. The DSP $\overline{\text{RESET}}$ input is usually tied to the IA $\overline{\text{POR}}$ line to have the IA $\overline{\text{POR}}$ output initiate a reset upon RC2324DP/DS power turn-on or if the IA detects a low power condition.

Power-On-Reset ($\overline{\text{POR}}$)

The IA Power-On Reset ($\overline{\text{POR}}$) signal is a bidirectional signal that is used as an active low input to reset the IA device and as an active low output to initiate an external reset of the DSP when a low power condition is detected within the IA device.

The IA device power-on reset circuit monitors the IA +5V supply and outputs a 100 ms to 300 ms low pulse on $\overline{\text{POR}}$ upon IA +5V turn-on. This pulse is generated regardless of the IA –5V supply level. A 10 ms minimum low pulse on $\overline{\text{POR}}$ is also generated when the IA +5V supply drops below 3.5V.

When DSP $\overline{\text{RESET}}$ and IA $\overline{\text{POR}}$ are tied together, the IA devices pulses $\overline{\text{POR}}$ low upon IA power turn-on to begin the $\overline{\text{POR}}$ sequence. The modem is ready 350 ms after the low-to-high transition of $\overline{\text{POR}}$. The $\overline{\text{POR}}$ sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{\text{POR}}$ low for at least 3 µs. $\overline{\text{POR}}$ is not pulsed low by the IA device when the $\overline{\text{POR}}$ sequence is initiated externally.

NOTE: If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a $\overline{\text{POR}}$ sequence (i.e., <+3.5V), the host system should assert the reset signals to the DSP and IA devices upon supply voltage recovery to ensure proper modem initialization and operation.

IA Reset Time Constant ($\overline{\text{RESET}}$ TC)

When IA $\overline{\text{POR}}$ is used as described above, an external discrete RC network must be connected to the $\overline{\text{RESET}}$ TC pin to generate the $\overline{\text{POR}}$ long time constant (see Figure 9).

In modem circuits not requiring the bidirectional $\overline{\text{POR}}$ signal, the $\overline{\text{RESET}}$ TC input can be used as the active low reset input to the IA device rather than $\overline{\text{POR}}$. In this case, the $\overline{\text{RESET}}$ TC should be connected to the DSP $\overline{\text{RESET}}$ input instead of the RC network, and the IA $\overline{\text{POR}}$ input should be left open.

Crystal In (XTLI) and Crystal Out (XTLO)

The DSP must be connected to an external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors (see Figure 9 and Table 19).

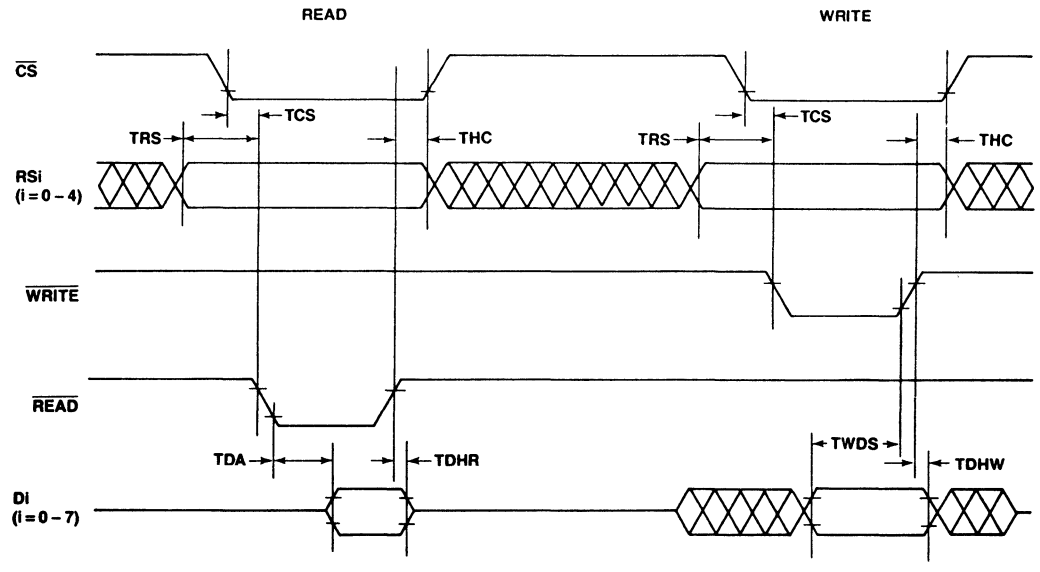
MICROPROCESSOR INTERFACE

Eighteen address, data, control and interrupt hardware interface signals implement an 8086/6502 compatible parallel microprocessor interface to a host processor. The read/write cycle timing requirements are listed in Table 9 and the timing waveforms are illustrated in Figure 4.

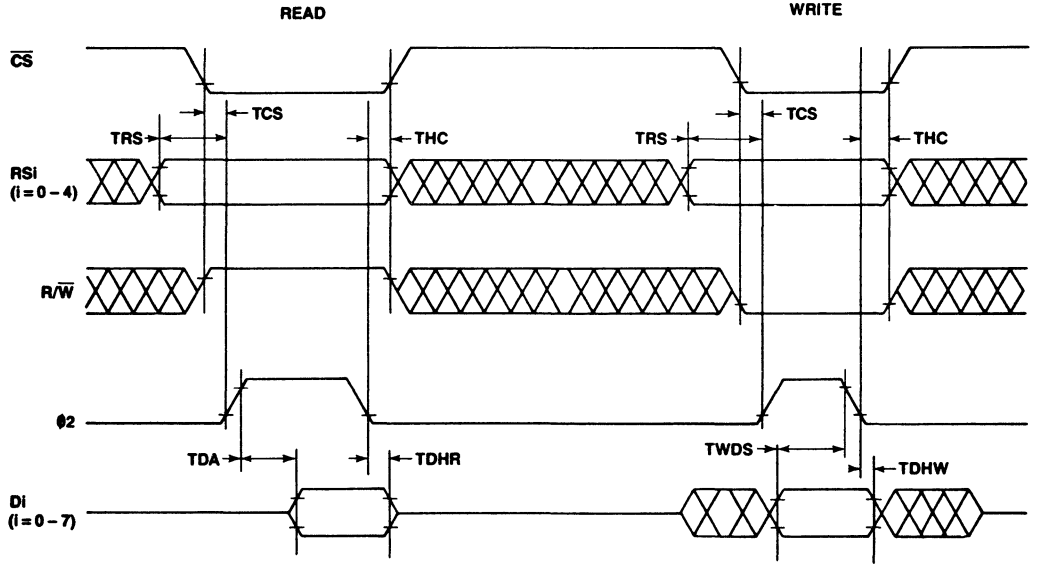
This parallel interface allows the host to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The definitions of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

Table 9. Microprocessor Bus Interface Timing

Parameter	Symbol	Min.	Max.	Units
$\overline{\text{CS}}$ Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	–	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns



a. 8086 Bus Compatible (EN86 = High)



b. 6502 Bus Compatible (EN86 = Low)

Figure 4. Microprocessor Bus Interface Waveforms

Data Lines (D0–D7)

Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable (READ) and Write Enable (WRITE) signals.

Chip Select ($\overline{CS}$)

The active low Chip Select ($\overline{CS}$) input selects the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus.

Register Select Lines (RS0 - RS4)

The five active high Register Select inputs (RS0 - RS4) address interface memory registers within the DSP when $\overline{CS}$ is low. These lines are typically connected to address lines A0-A4.

When selected by $\overline{CS}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0-D7).

Read Enable ($\overline{READ}$) and Write Enable($\overline{WRITE}$)

The microprocessor bus operates with either 8086 or 6502 compatible timing as selected by the EN86 input.

When EN86 is high, 8086 timing is selected, and the read/write control signals are Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$). Reading or writing is controlled by the host pulsing either $\overline{READ}$ or $\overline{WRITE}$ input low, respectively, during the microprocessor bus access cycle (Figure 4a).

During a read cycle, data from the addressed DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the addressed DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

When EN86 is low, 6502 timing is selected, and the read/write control signals are Phase 2 Clock ($\phi 2$) and Read/$\overline{Write}$ (R/$\overline{W}$). ($\phi 2$ replaces $\overline{READ}$ and R/$\overline{W}$ replaces $\overline{WRITE}$.) Reading or writing is controlled by pulsing R/$\overline{W}$ low or leaving R/$\overline{W}$ high, respectively, during the microprocessor bus access cycle (Figure 4b).

Interrupt Request ($\overline{IRQ}$)

The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in the DSP interface memory to indicate immediate change of conditions in the modem DSP device. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.

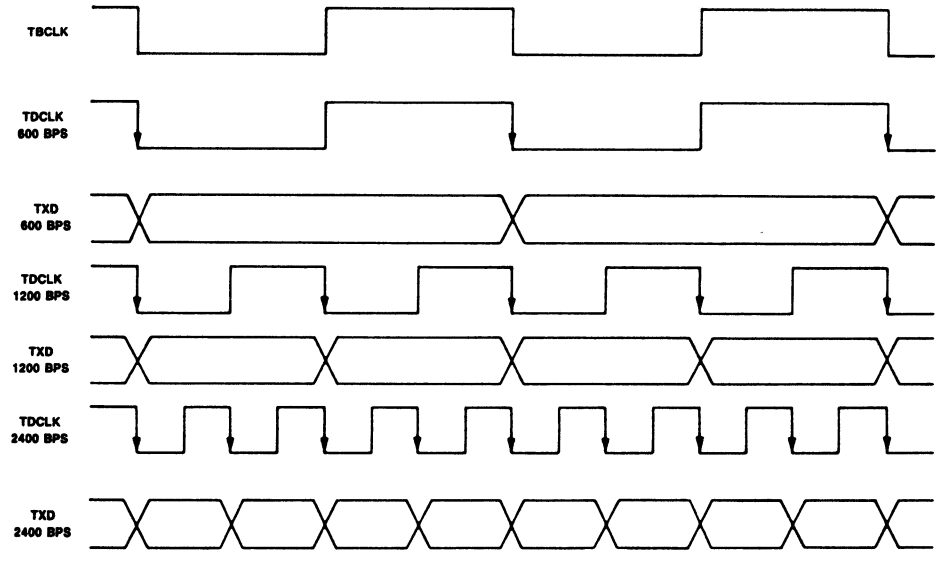
The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{IRQ}$ output can be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt request input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25W, is sufficient.

V.24 INTERFACE

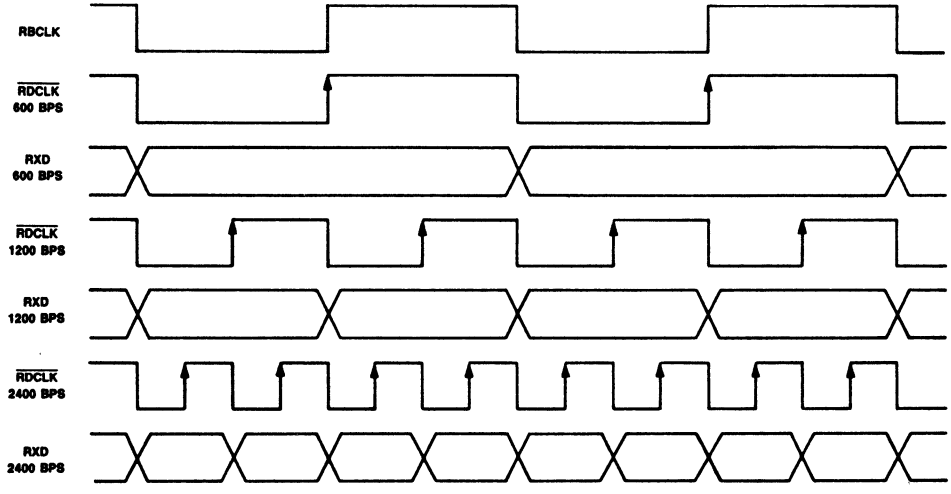
Ten hardware circuits provide timing, data and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. The serial interface signals are TTL compatible and can drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels using 1489 receivers and 1488 drivers, or their equivalents. The serial interface timing is illustrated in Figure 5.

The $\overline{RTS}$ hardware control input is logically ORed with its corresponding interface memory bit by the modem to form the resultant control signal. The state of each hardware status output signal ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) is also reflected in its corresponding interface memory bit. Note that the hardware interface signals are complemented with respect to their corresponding interface memory bits (e.g., $\overline{RTS}$ signal low = RTS bit set to a 1).



NOTE: THIS FIGURE IS VALID FOR SYNCHRONOUS MODE ONLY. THERE IS NO RELATIONSHIP BETWEEN TXD AND TDCLK IN ASYNCHRONOUS MODE

a. Transmit



NOTE: THIS FIGURE IS VALID FOR SYNCHRONOUS MODE ONLY. THERE IS NO RELATIONSHIP BETWEEN RXD AND RDCLK IN ASYNCHRONOUS MODE

b. Receive

Figure 5. Serial Interface Waveforms

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the host on the Transmitted Data (TXD) input in serial mode, or from the interface memory Transmit Data Register (TBUFFER) in parallel mode. (The TPDM bit in selects the serial or parallel mode.)

Received Data (RXD)

The modem presents received serial data to the host on the Received Data (RXD) output and to the interface memory Receive Data Register (RBUFFER) in both serial and parallel modes. RXD is clamped to mark in SDLC mode.

Request To Send ($\overline{RTS}$)

Request to Send ($\overline{RTS}$) input ON (low) causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active.

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) output ON (low) indicates that the modem will transmit any data present on TXD. $\overline{CTS}$ response times relative to $\overline{RTS}$ are shown in Table 3.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) output ON (low) indicates that the modem is in the data transfer state, i.e.:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.

$\overline{DSR}$ OFF (high) indicates that the host is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{RI}$).

Received Line Signal Detector ($\overline{RLSD}$)

$\overline{RLSD}$ ON (low) indicates that valid data is available on RXD. The $\overline{RLSD}$ thresholds are programmable in DSP RAM. The $\overline{RLSD}$ default threshold values for both high and low channels are:

$\overline{RLSD}$ ON ≥ -43 dBm
$\overline{RLSD}$ OFF ≤ -48 dBm

Ring Indicator ($\overline{RI}$)

Ring Indicator ($\overline{RI}$) output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The OFF (high) condition of the $\overline{RI}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received.

The $\overline{RI}$ frequency range is programmable in DSP RAM. $\overline{RI}$ will respond to RD input signals in the frequency range of 15.3 Hz to 68 Hz (default values).

The $\overline{RI}$ OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal on the RD input and the subsequent ON (OFF) transition of RI. The RI response times are shown in Table 10.

Table 10. RI Response Time

$\overline{RI}$ Transition	Response Time
OFF to ON	One Period *
ON to OFF	One Period
* Period of the ring frequency.	

Transmit Data Clock (TDCLK)

The modem outputs a Transmit Data Clock (TDCLK) in synchronous communications. The TDCLK clock frequency is data rate ±0.01% with a duty cycle of 50 ± 1%. Transmit Data (TXD) must be stable during the one microsecond period immediately preceding and following the rising edge of TDCLK.

In asynchronous modes, TDCLK is clamped to mark.

External Transmit Clock (XTCLK)

In synchronous communication, the host may supply the external transmit data clock input (XTCLK). The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is reflected at TDCLK if the modem is set for external clock (TXCLK = 10).

Receive Data Clock ($\overline{RDCLK}$)

The modem outputs a Receive Data Clock ($\overline{RDCLK}$) in the form of 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit can track a ±0.01% frequency error in the remote transmit timing source.

$\overline{RDCLK}$ is output in synchronous communications only. In asynchronous modes, $\overline{RDCLK}$ is clamped to mark.

DAA INTERFACE

Receive Analog (RXA)

RXA is an input to the external filter components from a data access arrangement (see Figure 9). The input impedance at RXA is determined by R13 (see Design Considerations Section). R13 is selected such that power at REC OUT is –9 dBm when the maximum signal is applied to RXA.

Transmit Analog (TXA)

The TXA output from the external filter components (see Figure 9) can drive a data access arrangement for connection to either the PSTN or a leased line. The transmitter output impedance is a 1458 type operational amplifier output. The output level is determined by R15 (see Design Considerations Section).

ANCILLARY SIGNALS

Talk/Data Relay Driver (TLKRELAY)

TLKRELAY is an open drain output which can drive a normally closed relay with greater than 360 Ω coil resistance. The TLKRELAY output is controlled by the T/DRC input. The TLKRELAY output is clamped off during power-on reset. An external discrete diode is not required across the relay coil.

In a typical application, TLKRELAY OFF opens the Talk/Data relay and disconnects the handset from the telephone line (i.e., the modem has control of the line.)

Off-Hook Relay Driver (OHRELAY)

OHRELAY is an open drain output which can drive a normally open relay with greater than 360 Ω coil resistance. OHRELAY ON closes the Off-Hook relay and connects the modem to the telephone line (off-hook). The OHRELAY output is controlled by the state of the RA bit, except in pulse dial mode. OHRELAY output is clamped off during power-on reset. An external discrete diode is not required across the relay coil.

Talk/Data Relay Control (T/DRC)

Talk/Data Relay Control (T/DRC) is an uncommitted input that controls the state of the TLKRELAY output. T/DRC low turns the TLKRELAY output ON; T/DRC high turns the TLKRELAY output OFF.

Ring Detect (RD)

RD indicates to the modem by an ON (high) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the RD input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 Hz to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on RI.

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK) outputs are provided in synchronous communication modes. TBCLK and RBCLK have no counterpart in the V.24 or RS-232-C recommendations since they mark the baud interval rather than the data rate for the transmitter and receiver, respectively. Both signals are active high. The high-to-low transition of each baud clock coincides with a high-to-low transition of the respective data clock.

DIAGNOSTIC SIGNALS

Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line distrubances can usually be identified. Timing of these signals is illustrated in Figure 6.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope horizontal (X) axis and vertical (Y) axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

EYEX and EYEY outputs are 8-bit words, shifted out most significant bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.

EYECLK

EYECLK is a clock for use by the serial-to-parallel converters. The EYECLK output is a 7200 Hz clock.

EYESYNC

EYESYNC is a strobe for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

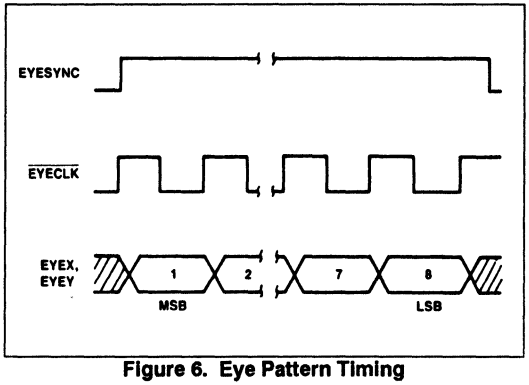


Figure 6. Eye Pattern Timing

SOFTWARE INTERFACE

Modem functions are implemented in DSP firmware.

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAP

A memory map of DSP interface memory identifying the contents of the 32 addressable registers is shown in Figure 7. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, the host must read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory register.

INTERFACE MEMORY BIT DEFINITIONS

Table 11 defines the individual bits in the interface memory. Bits in the interface memory are referred to using the format Z:Q. The register number is denoted by Z (00 through 1 F) and the bit number is located by Q (0 through 7, where 0 = LSB).

INITIALIZATION

The POR default value for each configuration/control bit is shown in Table 11. POR leaves the modem configured as follows:

- 2400 bps
- Synchronous
- Constant carrier
- Serial data mode
- Answer mode

Register	Bit 7	6	5	4	3	2	1	0
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	XACC	—	—	—	—	—	XWT	XCR
1C	X RAM ADDRESS (XADD)							
1B	YACC	—	—	—	—	—	YWT	YCR
1A	Y RAM ADDRESS (YADD)							
19	X RAM DATA MSB (XDAM)							
18	X RAM DATA LSB (XDAL)							
17	Y RAM DATA MSB (YDAM)							
16	Y RAM DATA LSB (YDAL)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	TLVL				—	—	TXCLK	
12	CONFIGURATION (CONF)							
11	—	—	—	—	—	—	—	TXP
10	TRANSMIT DATA BUFFER (TBUFFER)							
0F	RLSD	—	CTS	DSR	RI	TM	SYNCD	FLAGS
0E	RTDET	BRKD	PE	FE	OE	SPEED		
0D	—	—	S1DET	SCR1	U1DET	SADET	—	—
0C	—	—	—	—	—	—	—	—
0B	TONEA	TONEB	TONEC	ATV25	ATBELL	—	—	BEL103
0A	—	—	—	—	—	—	—	CRCS
09	NV25	CC	DTMF	ORG	LL	DATA	—	—
08	ASYNC	TPDM	—	DDIS	TRFZ	—	RTRN	RTS
07	RDLE	RDL	L2ACT	—	L3ACT	—	RA	MHLD
06	BRKS	EXOS	PARSL		PEN	STB	WDSZ	
05	—	—	—	—	CEQ	—	—	—
04	EQRES	—	—	—	EQFZ	IFIX	—	CRFZ
03	SYNCMD		SPLIT	—	ARC	SDIS	GTE	GTS
02	—	—	—	—	—	—	—	—
01	—	—	—	—	—	—	—	RXP
00	RECEIVER DATA BUFFER (RBUFFER)							

(—) Indicates reserved for modem use only

Figure 7. RC2324DP/DS Interface Memory Map

Table 11. Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
ARC	03:3	0	**Automatic Rate Change Enable.** When control bit ARC is a 1, an automatic on-line rate change sequence is enabled. This allows on-line fallback from 2400 bps to 1200 bps per V.22 bis Section 6.6.
ASYNC	08:7	0	**Asynchronous/Synchronous.** When control bit ASYNC is a 1, asynchronous data mode is selected. When ASYNC changes from a 0 to a 1, the receiver's synchronous to asynchronous converter and the transmitter's asynchronous to synchronous converter are configured according to the EXOS, PARSL, PEN, STB and WDSZ bits at that time. ASYNC may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. All clocks are clamped to mark in asynchronous mode. When ASYNC is a 0, synchronous data mode is selected. The SYNCMD bits further select one of two synchronous modes.
ATBELL	0B:3	0	**Bell Answer Tone Detected.** When set to a 1, status bit ATBELL indicates that the modem is detecting a 2225 Hz answer tone. When reset to a 0, the 2225 Hz answer tone is not being detected. ATBELL is active only in the Dial/Call Progress and originate handshake configurations.
ATV25	0B:4	0	**V25 Answer Tone Detected.** When set to a 1, status bit ATV25 signifies that the modem is detecting a 2100 Hz answer tone. When reset to a 0, the 2100 Hz answer tone is not being detected. ATV25 is only active in the Dial/Call Progress and originate handshake modes (ORG = 1).
BEL103	0B:0	0	**Bell 103 Mark Frequency Detected.** When set to a 1, status bit BEL103 indicates that the modem is detecting a Bell 103 mark frequency (1270 Hz). When reset to a 0, the mark frequency is not being detected. BEL103 is available only in Dial/Call Progress and answer handshake modes (ORG = 0).
BRKD	0E:6	0	**Break Detected.** When set to a 1, status bit BRKD indicates the modem is receiving continuous space. When reset to a 0, continuous space is not being received.
BRKS	06:7	0	**Break Sequence.** When control bit BRKS is a 1 and TPDM is a 1, the modem will send continuous space. When BRKS is a 0 and TPDM is a 1, the modem will transmit parallel data from the TBUFFER. (This bit is valid only when TPDM = 1.)
CC	09:6	0	**Controlled Carrier.** When control bit CC is a 1, the modem operates in controlled carrier (i.e., the carrier is controlled by $\overline{\text{RTS}}$); when 0, the modem operates in constant carrier (i.e., the carrier stays on when $\overline{\text{RTS}}$ is off). Controlled Carrier is available only in leased line (LL = 1). Controlled carrier allows the modem transmitter to be controlled by the $\overline{\text{RTS}}$ pin or the RTS bit (see Table 3). When the $\overline{\text{RTS}}$ pin goes low, or the RTS bit set to a 1, the transmitter immediately sends scrambled ones for 270 ms and then turns on the $\overline{\text{CTS}}$ signal and the CTS bit. At 2400 bps, it is recommended that a retrain be sent once in the data mode to ensure that synchronization occurs. (V.22 bis)
CEQ	05:3	1	**Compromise Equalizer Enable.** When control bit CEQ is a 1, the transmitter's passband digital compromise equalizer is inserted into the transmit path. When CEQ is a 0, the equalizer is not inserted into the transmit path.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CONF	12:0-7	84	**Modem Configuration Select.** The CONF control bits select the modem operating mode from one of the following configuration codes:

Mode	Data Rate (bps) Transmit	Receive	CONF (Hex)
V.22 bis	2400	2400	84
V.22	1200	1200	52
V.22	600	600	51
Bell 212A	1200	1200	62
Bell 103	0-300	0-300	60
V.21	300	300	A0
V.23	75	1200	46
V.23	1200	75	47
V.23	1200	1200	42
V.23	75	75	40
Tone Generator/Detector			80
Dial/Call Progress Monitor			81

Note: NEWC must be set to a 1 after CONF is changed.

CRCS	0A:0	0	**CRC Sending.** When set to a 1, status bit CRCS indicates that the transmitter is sending the CRC (2 bytes) in SDLC mode. A 0 indicates that the CRC is not being sent.
CRFZ	04:0	0	**Carrier Recovery Freeze.** When control bit CRFZ is a 1, updating of the receiver's carrier recovery phase lock loop (PLL) is inhibited. When reset to a 0, normal updating is enabled.
CTS	0F:5	0	**Clear to Send.** When set to a 1, status bit CTS indicates that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an $\overline{\text{RTS}}$ ON or OFF transition after the modem has completed a handshake are shown in Table 3. When reset to a 0, data is not being transmitted.
DATA	09:2	0	**Data Mode.** When control bit DATA is a 0, the modem is in the idle mode and data is not being transmitted. The modem is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering. When control bit DATA is a 1, the modem is in the data mode in either leased line mode (LL = 1) or handshake mode (LL = 0).
DDIS	08:4	0	**Descrambler Disable.** When control bit DDIS is a 1, the receiver's descrambler circuit is disabled; when a 0, the descrambler circuit is enabled.
DSR	0F:4	0	**Data Set Ready.** When set to a 1 (ON), status bit DSR indicates that the modem is in the data transfer state. When reset to a 0 (OFF), DSR indicates that the DTE is to disregard all signals appearing on the interchange circuits–except RI.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
DTMF	09:5	0	**DTMF Select.** When the modem is configured for dialing mode (CONF = 81), the modem will dial using DTMF tones or pulses. When control bit DTMF is a 1, the modem will dial using DTMF tones. When DTMF is a 0, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. Dialing mode is selected by configuration code 81 in the Configuration Register (CONF). When in dialing mode, the data placed in the Transmitter Data Buffer (TBUFFER) is treated as the digit to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the TBUFFER). Also, see TDBE bit. Dialing timing is host programmable in DSP RAM.
EQFZ	04:3	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited. When a 0, updating is enabled.
EQRES	04:7	0	**Equalizer Reset.** When control bit EQRES is a 1, the receiver adaptive equalizer taps are reset to zero. When a 0, the equalizer taps are updated normally.
EXOS	06:6	0	**Extended Overspeed.** When control bit EXOS is a 1, Extended Overspeed mode is selected in the transmitter async-to-sync converter and in the receiver sync-to-async converter. When a 0, normal overspeed mode is selected. (See SPLIT)
FE	0E:4	0	**Framing Error.** When set to a 1, status bit FE indicates that more than 1 in 8 (or 1 in 4 for extended overspeed) characters were received without a Stop bit in asynchronous mode or an ABORT sequence was detected in SDLC/HDLC synchronous mode. When reset to a 0, no framing error is detected.
FLAGS	0F:0	0	**Flag Sequence.** When set to a 1, status bit FLAGS indicates that the transmitter is sending the Flag sequence in SDLC/HDLC mode, or a constant mark in parallel asynchronous mode. When reset to a 0, FLAGS indicates that the transmitter is sending data.
GTE	03:1	0	**Guard Tone Enable.** When control bit GTE is a 1, the specified guard tone to be transmitted is enabled (CCITT configurations only), according to the state of the GTS bit. The guard tone will be transmitted only by the answering modem. When set to a 0, guard tone transmission is disabled. (V.22 bis)
GTS	03:0	0	**Guard Tone Select.** When control bit GTS is set to a 1, the 550 Hz tone is selected; when a 0, the 1800 Hz tone is selected. The selected guard tone will be transmitted only when GTE is enabled. (V.22 bis)
IFIX	04:2	1	**Eye Fix.** When control bit IFIX is a 1, the serial diagnostic data output on the EYEX and EYEY pins reflects the Rotated Equalizer Output. When IFIX is a 0, the data on EYEX and EYEY is selected by the addresses in X RAM Address and Y RAM Address registers, respectively.
LL	09:3	0	**Leased Line.** When control bit LL is set to a 1, the modem will enter the Leased Line Data Mode (selected by the ORG bit) when the DATA bit is a 1. When a 0, the modem will enter the Handshake Mode (selected by the ORG bit) when the DATA bit is a 1.
L2ACT	07:5	0	**Loop 2 (Local Digital Loopback) Activate.** When control bit L2ACT is a 1, the receiver's digital output is internally connected to the transmitter's digital input (locally activated digital loopback) in accordance with CCITT Recommendation V.54.
L3ACT	07:3	0	**Loop 3 (Local Analog Loopback) Activate.** When control bit L3ACT is a 1, the transmitter's analog output is internally coupled to the receiver's analog input (local analog loopback) in accordance with CCITT Recommendation V.54. The modem may only be placed into loop 3 mode when in idle mode (DATA bit is a 0). After setting the L3ACT bit to a 1, the NEWC bit must also be set. The loopback is then completed when the modem sets DSR, CTS, and DCD (RLSD) bits to a 1. To terminate the loopback, reset L3ACT to a 0 and then set NEWC to a 1.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
MHLD	07:0	0	**Mark Hold.** When control bit MHLD is a 1, the transmitter sends continuous mark. When MHLD is a 0, the transmitter sends continuous flag or data from TBUFFER. This bit is valid only in SDLC/HDLC mode.
NCIA	1F:6	0	**NEWC Interrupt Active.** When the new configuration interrupt is enabled (NCIE is a 1) and a new configuration is implemented (NEWC is reset to a 0 by the DSP), $\overline{IRQ}$ is asserted and status bit NCIA is set to a 1 to indicate that NEWC being a 0 caused the interrupt. NCIA and the interrupt request due to NEWC are cleared by the host writing a 0 into NCIE. (See NEWC and NCIE.)
NCIE	1F:2	0	**NEWC Interrupt Enable.** When control bit NCIE is a 1 (interrupt enabled), the modem will assert $\overline{IRQ}$ and set NCIA to a 1 when the NEWC bit is reset to a 0 by the DSP. When NCIE is a 0 (interrupt disabled), NEWC has no effect on $\overline{IRQ}$ or NCIA. (See NEWC and NCIA.)
NEWC	1F:0	0	**New Configuration.** When control bit NEWC is set to a 1, the modem will implement the new configuration. The DSP resets the NEWC bit to a 0 when the configuration change is acknowledged. A configuration change can also cause $\overline{IRQ}$ to be asserted. (See NCIE and NCIA.) **Note:** Control bit NEWC must be set to a 1 by the host after the host changes the contents of any of the following control bits: CONF Configuration SYNCMD Synchronous Mode Select GTE Guard Tone Enable GTS Guard Tone Select RDLE Remote Digital Loopback Enable RDL Remote Digital Loopback Request L2ACT Loop 2 Activate L3ACT Loop 3 Activate RA Relay Activate PARSL Parity Select PEN Parity Enable STB Stop Bit Number WDSZ Word Size ORG Originate Mode LL Leased Line Mode DATA Data ASYNC Asynchronous Mode RTRN Retrain TLVL Transmit Level EQRES Equalizer Reset
NEWS	1F:3	–	**New Status.** When set to a 1, status bit NEWS indicates that one or more status bits located in registers 0A, 0B, 0E, or 0F have changed state, or a DSP RAM read or write has been completed. This bit can be reset to a 0 only by the host. When set to a 1, this bit can cause $\overline{IRQ}$ to be asserted. (See NSIE and NSIA.)
NSIA	1F:7	0	**NEWS Interrupt Active.** When the new status interrupt is enabled (NSIE is a 1) and a change of status occurs (NEWS is set to a 1), $\overline{IRQ}$ is asserted and status bit NSIA is set to a 1 to indicate that NEWS being a 1 caused the interrupt. NSIA and the interrupt request due to NEWS are cleared when the host writes a 0 to NEWS. (See NEWS and NSIE.)
NSIE	1F:4	0	**NEWS Interrupt Enable.** When control bit NSIE is a 1 (interrupt enabled), $\overline{IRQ}$ will be asserted and NSIA will be set to a 1 when NEWS is set to a 1 by the DSP. When NSIE is a 0 (interrupt disabled), NEWS has no effect on $\overline{IRQ}$ or NSIA. (See NEWS and NSIA.)

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
NV25	09:7	0	**No. V.25 Answer Tone.** When control bit NV25 is a 1, the transmitter will not transmit the 2100 Hz CCITT answer tone when a handshake sequence is initiated and the modem is in answer mode. In originate mode, the receiver will not look for the 2100 Hz tone. When reset to a 0, the modem will transmit the answer tone in answer mode and will look for the answer tone in originate mode.
OE	0E:3	0	**Overrun Error.** When set to a 1, status bit OE indicates that the Receiver Data Buffer (RBUFFER) was loaded from the RXA input before the host read the old data from RBUFFER. When reset to a 0, RBUFFER was read before new receive data was loaded into RBUFFER. This is valid for both ASYNC mode and SDLC/HDLC mode.
ORG	09:4	0	**Originate.** When control bit ORG is a 1, the modem is in originate mode; when a 0, the modem is in answer mode. **Note:** The NEWC bit must be set after the ORG bit is changed.
PARSL	06:4, 5		**Parity Select.** Control bits PARSL select the method by which parity is generated and checked during the asynchronous parallel data mode (ASYNC = 1). The options are: **5 4 — Parity Selected** 0 0 — Stuff Parity ("9th Data Bit") (see TXP, RXP) 0 1 — Space Parity 1 0 — Even Parity 1 1 — Odd Parity
PE	0E:5	0	**Parity Error.** When set to a 1, status bit PE indicates that a character with bad parity was received in the asynchronous mode, or bad CRC was detected in the SDLC/HDLC synchronous mode. When a 0, a character with good parity was received.
PEN	06:3	0	**Parity Enable.** When set to a 1, control bit PEN enables parity generation and checking during asynchronous parallel data mode. When reset to a 0, parity generation and checking is disabled.
RA	07:1	0	**Off-Hook Relay Activate.** When control bit RA is set to a 1, the $\overline{\text{OHRELAY}}$ output is activated causing the relay to close (off-hook); when RA is reset to 0, the $\overline{\text{OHRELAY}}$ is turned off causing the relay to open (on-hook). **Note:** The host has exclusive control of the $\overline{\text{OHRELAY}}$ output through the RA bit except in pulse dial mode.
RBUFFER	00:0-7	0	**Receive Data Buffer.** The host obtains data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER.
RDBF	1E:0	–	**Receiver Data Buffer Full.** When set to a 1, status bit RDBF signifies that the modem wrote valid received data into register 00 (RBUFFER). This condition can also cause $\overline{\text{IRQ}}$ to be asserted. The host reading or writing register 00 resets the RDBF bit to 0. (See RDBIE and RDBIA.)
RDBIA	1E:6	0	**Receiver Data Buffer Interrupt Active.** When the receiver data buffer full interrupt is enabled (RDBIE is a 1) and register 00 is written to by the DSP (RDBF is set to a 1), the modem asserts $\overline{\text{IRQ}}$ and sets RDBIA to a 1 to indicate that RDBF being a 1 caused the interrupt. The host reading or writing register 00 resets the RDBF bit to a 0 and clears the interrupt request due to RDBF. (See RDBF and RDBIE.)
RDBIE	1E:2	0	**Receiver Data Buffer Interrupt Enable.** When control bit RDBIE is a 1 (interrupt enabled), the modem will assert $\overline{\text{IRQ}}$ and set the RDBIA bit to a 1 when RDBF is set to a 1 by the DSP. When RDBIE is a 0 (interrupt disabled), RDBF has no effect on $\overline{\text{IRQ}}$ or RDBIA. (See RDBF and RDBIA.)
	07:6	0	**Remote Digital Loopback Request.** When control bit RDL is a 1, the modem initiates a request for the remote modem to go into digital loopback, RXD is clamped to a mark, and the RLSD bit and $\overline{\text{RLSD}}$ signal will be reset until the loop is established. When the host resets the RDL bit the modem sends the RDL terminating sequence.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RDLE	07:7	0	**Remote Digital Loopback Response Enable.** When set to a 1, control bit RDLE enables the modem to respond to the remote modem's digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS and RLSD bits to a 0, and turns the CTS and DCD signals OFF. The TM bit is set to a 1 to inform the host of the test status.
RI	0F:3	0	**Ring Indicator.** When set to a 1, status bit RI indicates that a valid ringing signal is being detected. Ringing is detected if pulses are present on the RD input in the 15 Hz - 68 Hz frequency range (default frequency range). The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with RI output signal. The minimum and maximum valid ring frequencies are host programmable in DSP RAM. If the maximum value is set to zero, the RI bit will go on and off with each half of the ring frequency sine wave.
RLSD	0F:7	0	**Received Line Signal Detector.** When status bit RLSD is set to a 1, the carrier is being detected and receive data is valid. When a 0, the carrier is not being detected and RXD output is clamped to mark. **Note:** RXD is also clamped to mark during retrain while the RLSD bit remains on.
RTDET	0E:7	0	**Retrain Detected.** When set to a 1, status bit RTDET indicates that a retrain request sequence has been detected.
RTRN	08:1	0	**Retrain.** When control bit RTRN set to a 1 and the modem is in data mode, the modem requests retrain (or automatic rate change - see ARC) from the remote modem. RTRN is set to 0 when the previous retrain is completed. **Note:** If retrain is not completed successfully, the host must clear the RTRN bit. Fallback from 2400 bps to 1200 bps per CCITT V.22 bis may be accomplished as follows: 1. Set the ARC bit to a 1 in both modems. 2. Set the RTRN bit to a 1 in either modem. 3. Set the NEWC bit to a 1. Fall forward from 1200 bps to 2400 may be accomplished as follows: 1. Reset the ARC bit (with the remote modem having the ARC bit set). 2. Set the RTRN bit. 3. Set the NEWC bit. If the remote modem can operate at the requested rate, the SPEED bits will be changed by the modem to reflect the new rate after the retrain is completed. If the remote modem cannot operate at the new rate, then no rate change will take place during the retrain. In this case, the host must clear the RTRN bit.
RTS	08:0	0	**Request to Send.** When control bit RTS is a 1 or the RTS input is ON, the CTS bit is set to a 1 and the CTS output is turned ON. When the RTS bit is reset to 0 and the RTS input is OFF, the CTS bit is reset to a 0 and the CTS output is turned OFF.
RXP	01:0	0	**Received Parity bit.** This bit is only valid when parity is enabled (PEN = 1), and word size is set for 8 bits per character (WDSZ = 11). In this case, the parity bit received (or ninth data bit) will be available at this location. The host must read this bit before reading the received data buffer (RBUFFER).
S1DET	0D:5	0	**S1 Sequence Detected.** Status bit S1DET is set to a 1 when the S1 sequence is being detected. This bit is reset to a 0 when the S1 sequence is not being detected.
SADET	0D:2	0	**Scrambled Alternating Ones Sequence Detected.** Status bit SADET is set to a 1 when the Scrambled Alternating Ones sequence is being detected. This bit is reset to a 0 when the Scrambled Alternating Ones sequence is not being detected. **Note:** SADET is used to indicate the response of the remote modem to a V.22 bis rate change request or a remote digital loopback request.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
SCR1	0D:4	0	**Scrambled Ones Sequence Detected.** Status bit SCR1 is set to a 1 when Scrambled Ones is being detected during handshake. This bit is reset to 0 when Scrambled Ones is not being detected.
SDIS	03:2	0	**Scrambler Disable.** When control bit SDIS is a 1, the transmitter scrambler is disabled; when SDIS is a 0, the scrambler is enabled.
SPEED	0E:0-2	0	**Speed Indication.** The SPEED status bits indicate the data rate at the completion of a handshake: **2 1 0 — Data Rate (bps)** 0 0 0 — 300 0 0 1 — 600 0 1 0 — 1200 0 1 1 — 2400
SPLIT	03:5	0	**Parallel Async Extended Overspeed TX/RX Split.** When SPLIT is set to a 1 and EXOS is set, the transmitter will transmit at the basic overspeed while the receiver receives at the extended overspeed rate.
STB	06:2	0	**Stop Bit Number.** When control bit STB is a 0, one stop bit is selected in asynchronous mode; when a 1, two stop bits are selected.
SYNCD	0F:1	0	**Sync Pattern Detected.** When set to a 1, status bit SYNCD indicates that SDLC/HDLC flags (7E pattern) are being detected. When reset to a 0, the 7E pattern is not being detected.
SYNCMD	03:6,7	0	**Synchronous Mode.** Configuration bits SYNCMD select the synchronous mode (ASYNC = 0) from the following: **7 6 — Synchronous Mode** 0 0 — Normal Sync 0 1 — SDLC/HDLC Sync
TBUFFER	10:0-7	00	**Transmitter Data Buffer.** The host conveys output data to the transmitter in the parallel mode (TPDM = 1) by writing a data byte to the TBUFFER when the TDBE bit is a 1. The data is transmitted bit 0 first.
TDBE	1E:3	–	**Transmitter Data Buffer Empty.** When set to a 1, status bit TDBE signifies that the modem has read transmit data from register 10 (TBUFFER) and the host can write new data into register 10. This condition can also cause IRQ to be asserted. The host reading or writing register 10 resets the TDBE bit to 0. (See TDBIE and TDBIA.)
TDBIA	1E:7	0	**Transmitter Data Buffer Interrupt Active.** When the transmitter data buffer empty interrupt is enabled (TDBIE is a 1) and register 10 is empty (TDBE is set to a 1), the modem asserts IRQ and sets status bit TDBIA to a 1 to indicate that TDBE being a 1 caused the interrupt. The host reading or writing register 10 resets the TDBIA bit to a 0 and clears the interrupt request due to TDBE. (See TDBIE and TDBE.)
TDBIE	1E:5	0	**Transmitter Data Buffer Interrupt Enable.** When control bit TDBIE is a 1 (interrupt enabled), the modem will assert IRQ and set the TDBIA bit to a 1 when TDBE is set to 1 by the DSP. When TDBIE is a 0 (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.)

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TLVL	13:4-7	6	**Transmit Level Attenuation Select.** The TLVL control code selects the transmitter analog output level attenuation at the TXA pin as follows: **7 6 5 4 — Transmit Level Attenuation (dB ±0.5 dB)** 0 0 0 0 — 0 dB 0 0 0 1 — 1 dB 0 0 1 0 — 2 dB 0 0 1 1 — 3 dB 0 1 0 0 — 4 dB 0 1 0 1 — 5 dB 0 1 1 0 — 6 dB 0 1 1 1 — 7 dB 1 0 0 0 — 8 dB 1 0 0 1 — 9 dB 1 0 1 0 — 10 dB 1 0 1 1 — 11 dB 1 1 0 0 — 12 dB 1 1 0 1 — 13 dB 1 1 1 0 — 14 dB 1 1 1 1 — 15 dB The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.
TM	0F:2	0	**Test Mode.** When set to a 1, status bit TM indicates that the selected test mode is active. When TM is reset to a 0, no test mode is active.
TONEA	0B:7	0	**Tone Filter A Energy Detected.** When set to a 1, status bit TONEA indicates that energy above the threshold is being detected by the Call Progress Monitor filter in the Dial Configuration (CONF = 81) or that 1300 Hz FSK tone energy is being detected by the Tone A bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	0B:6	0	**Tone Filter B Energy Detected.** When set to a 1, status bit TONEB indicates that 390 Hz FSK tone energy is being detected by the Tone B bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	0B:5	0	**Tone Filter C Energy Detected.** When set to a 1, status bit TONEC indicates that either 1650 Hz (ORG = 1) or 980 Hz (ORG = 0) FSK tone energy is being detected by the Tone C bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TPDM	08:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is a 1, the transmitter accepts parallel data from the host microprocessor interface via the TBUFFER register for transmission rather than serial data from the TXD input pin. When TPDM is a 0, serial data from the TXD input pin is accepted for transmission rather than parallel data from TBUFFER.
TRFZ	08:3	0	**Timing Recovery Freeze.** When control bit TRFZ is a 1, the updating of the receiver's timing recovery algorithm is inhibited. When TRFZ is a 0, normal updating occurs.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TXCLK	13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock: **1 0 — Transmit Clock** 0 0 — Internal 0 1 — Not Used (Internal) 1 0 — External (XTCLK input) 1 1 — Slave (RDCLK output) When the external clock is chosen, the host supplied clock must be connected to the XTCLK input pin. The external clock will then be reflected at the TDCLK output pin. When the slave clock is chosen, the transmitter clock output (TDCLK) is phase locked to the receiver clock output (RDCLK).
TXP	11:0	0	**Transmit Parity bit.** This bit is only active when parity is enabled (PEN = 1), stuff parity is selected (PARSL = 00) and word size is set for 8 bits per character. The host must load the stuffed parity bit (or ninth data bit) in this location before loading the other 8 bits of data in TBUFFER.
U1DET	0D:3	0	**Unscrambled Ones Detected.** When set to a 1, status bit U1DET indicates that V.22 bis Unscrambled Ones sequence has been detected. This bit is reset to a 0 by the modem at the end of the Unscrambled Ones sequence. (V.22 bis)
WDSZ	06:0,1	0	**Data Word Size.** The WDSZ control field sets the number of data bits per character in asynchronous mode as follows: **1 0 — Data Bits/Character** 0 0 — 5 0 1 — 6 1 0 — 7 1 1 — 8
XACC	1D:7	0	**X RAM Access Enable.** When control bit XACC is a 1, the DSP accesses the X RAM associated with the address in XADD and the XCR bit. XWT determines if a read or write is performed. The DSP resets XACC to a 0 upon RAM access completion.
XADD	1C:0-7	00	**X RAM Address.** XADD contains the X RAM address used to access the DSP's X Data RAM (XCR = 0) or X Coefficient RAM (XCR = 1) via the X RAM Data LSB and MSB registers (addresses 18 and 19, respectively). (See Table 12.)
XCR	1D:0	0	**X Coefficient RAM Select.** When control bit XCR is a 1, XADD applies to the X Coefficient RAM. When XCR is a 0, XADD applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 12).
XDAL	18:0-7	00	**X RAM Data LSB.** XDAL is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XDAM	19:0-7	00	**X RAM Data MSB.** XDAM is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XWT	1D:1	0	**X RAM Write.** When XWT is a 1 and XACC is set to a 1, the DSP copies data from the X RAM Data registers (18 and 19) into the X RAM location addressed by XADD and XCR. When control bit XWT is a 0 and XACC is set to a 1, DSP reads X RAM at the location addressed by XADD and XCR and stores the data into the X RAM Data registers (18 and 19).
YACC	1B:7	0	**Y RAM Access Enable.** When control bit YACC is a 1, the DSP accesses the Y RAM associated with the address in YADD and the YCR bit. YWT determines if a read or write is performed. The DSP resets YACC to a 0 upon RAM access completion.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description (Cont'd)
YADD	1A:0-7	00	**Y RAM Address.** YADD contains the Y RAM address used to access the DSP's Y Data RAM (YCR = 0) or Y Coefficient RAM (YCR = 1) via the Y RAM Data LSB and MSB registers (adresses 16 and 17, respectively). (See Table 12.)
YCR	1B:0	0	**Y Coefficient RAM Select.** When control bit YCR is a 1, YADD applies to the DSP's Y Coefficient RAM. When YCR is a 0, YADD applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 12).
YDAL	16:0-7	00	**Y RAM Data LSB.** YDAL is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YDAM	17:0-7	00	**Y RAM Data MSB.** YDAM is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YWT	1B:1	0	**Y RAM Write.** When YWT is a 1 and YACC is set to a 1, the DSP copies data from the Y RAM Data registers (16 and 17) into the Y RAM location addressed by YADD and YCR. When control bit YWT is a 0 and YACC is set to a 1, the DSP reads Y RAM at the location addressed by YADD and YCR and stores the data into the Y RAM Data registers (16 and 17).

DSP RAM ACCESS

The DSP contains four sections of 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) sections, as well as data and coefficient sections. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously in either the data or coefficient section.

INTERFACE MEMORY ACCESS TO DSP RAM

The DSP interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The addresses stored in DSP interface memory RAM Address registers (i. e., XADD and YADD) by the host, in conjunction with the data or coefficient RAM bits (i. e., XCR and YCR) determine the DSP RAM addresses for data access.

One or two 16-bit words are transferred between DSP RAM and DSP interface memory once each internal DSP cycle. The transmitter and the receiver sample rate functions operate at the 7200 Hz sample rate. The receiver baud rate function operates at the 600 Hz.

Two RAM access bits (XACC and YACC) in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The DSP tests these bits each sample period.

HOST PROGRAMMABLE DATA

The parameters available in DSP RAM are listed in Table 12 along with the X RAM or Y RAM address and corresponding XCR or YCR bit value.

HOST DSP READ AND WRITE PROCEDURES

DSP RAM Write Procedure

1. Before writing to DSP interface memory, verify that XACC and YACC are reset to 0.
2. Load the RAM address into XRAM address (XADD) and/or YRAM address (YADD).
3. Write the desired data to the RAM data registers (XDAM, XDAL, YDAM, or YDAL).
4. Set the coressponding coefficient RAM select bits (XCR, YCR) as necessary.

Table 12. DSP RAM Parameters

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
1	1	0	–	1st Equalizer Tap, Real
1	1	11	–	Last Equalizer Tap, Real
2	1	–	0	1st Equalizer Tap, Imaginary
2	1	–	11	Last Equalizer Tap, Imaginary
3	0	16	–	Rotated Error, Real
4	0	–	16	Rotated Error, Imaginary
5	0	3F	–	Max AGC Gain Word
6	0	71	–	Pulse Dial Interdigit Time
7	0	7C	–	Tone Dial Interdigit Time
8	0	72	–	Pulse Dial Relay Make Time
9	0	7D	–	Pulse Dial Relay Break Time
10	0	7E	–	DTMF Duration
11	0	6D	–	Tone 1 Angle Increment Per Sample
12	0	–	6D	Tone 2 Angle Increment Per Sample
13	0	6F	–	Tone 1 Amplitude
14	0	–	6F	Tone 2 Amplitude
15	0	73	–	Max Samples Per Ring Frequency Period
16	0	74	–	Min Samples Per Ring Frequency Period
17	1	12	–	Real Part of Error
18	1	–	12	Imaginary Part of Error
19	1	–	14	Rotation Angle for Carrier Recovery
20	1	15	–	Rotated Equalizer Output, Real
21	1	–	15	Rotated Equalizer Output, Imaginary
22	1	16	–	Lower Part of Phase Error
23	1	–	16	Upper Part of Phase Error
24	1	3F	–	Upper Part of AGC Gain Word
25	1	–	3F	Lower Part of AGC Gain Word
26	1	1F	–	Average Power
27	1	2D	–	Phase Error
28	1	2F	–	Tone Power (ATBELL, BEL103 or TONEA
29	1	–	2F	Tone Detect Threshold (Call Progress Energy)
30	1	30	–	Tone Power (ATV25 or TONEB)

Table 12. DSP RAM Parameters (Cont'd)

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
31	1	31	–	Tone Power (TONEC)
32	1	36	–	Tone Detect Threshold (ATBELL, BEL103, or TONEA)
33	1	37	–	Tone Detect Threshold (ATV25 or TONEB)
34	1	38	–	Tone Detect Threshold (TONEC)
35	1	3B	–	Zero Crossing Counter
36	1	52	–	Eye Quality Monitor (EQM)
37	1	–	31	Filter 1 Coefficient $\alpha 0$
38	1	–	32	Filter 1 Coefficient $\alpha 1$
39	1	–	33	Filter 1 Coefficient $\alpha 2$
40	1	–	34	Filter 1 Coefficient $\beta 1$
41	1	–	35	Filter 1 Coefficient $\beta 2$
42	1	–	37	Filter 2 Coefficient $\alpha 0$
43	1	–	38	Filter 2 Coefficient $\alpha 1$
44	1	–	39	Filter 2 Coefficient $\alpha 2$
45	1	–	3A	Filter 2 Coefficient $\beta 1$
46	1	–	3B	Filter 2 Coefficient $\beta 2$
47	1	–	76	Filter 3 Coefficient $\alpha 0$
48	1	–	77	Filter 3 Coefficient $\alpha 1$
49	1	–	78	Filter 3 Coefficient $\alpha 2$
50	1	–	79	Filter 3 Coefficient $\beta 1$
51	1	–	7A	Filter 3 Coefficient $\beta 2$
52	1	–	45	Filter 4 Coefficient $\alpha 0$
53	1	–	46	Filter 4 Coefficient $\alpha 1$
54	1	–	47	Filter 4 Coefficient $\alpha 2$
55	1	–	48	Filter 4 Coefficient $\beta 1$
56	1	–	49	Filter 4 Coefficient $\beta 2$
57	1	1C	–	Turn-on Threshold (PSK)
58	1	32	–	Turn-off Threshold (PSK)
59	1	–	21	RLSD Turn-off Time (PSK)
60	0	–	1C	Turn-on Threshold (FSK)
61	0	–	1D	Turn-off Threshold (FSK)

*XCR if an XRAM address is listed; YCR if a YRAM address is listed.

5. Set the appropriate RAM write bits (XWT, YWT).
6. Set the appropriate RAM access bits (XACC, YACC).
7. After the DSP has transferred the contents of the interface memory RAM data registers into DSP RAM, the DSP resets the XACC and/or the YACC bit to a 0, then sets the NEWS bit to a 1 indicate DSP RAM write completion.
8. If the NSIE bit is a 1, IRQ is also asserted and NSIA is set to a 1 when NEWS is set to a 1. NSIA is cleared by writing a 0 into the NEWS bit, which also causes IRQ to return high if no other interrupt requests are pending.

Note: Steps 4 and 5 can be accomplished simultaneously.

DSP RAM Read Procedure

1. Before reading from DSP interface memory, verify that XACC and YACC are reset to a 0.
2. Load the RAM address into X RAM Address (XADD) and/or Y RAM Address (YADD) register(s).
3. Set the corresponding XCR and/or YCR bit(s) appropriately.
4. Reset XWT and/or YWT to a 0, inform the DSP that a RAM read will occur when XACC and/or YACC is set to a 1.
5. Set XACC and/or YACC to a 1 to signal the DSP to perform the RAM read.
6. After the DSP has transferred the contents of RAM into the interface memory RAM data registers, the DSP resets the XACC and/or the YACC bit to a 0, then sets the NEWS bit to a 1 to indicate DSP RAM read completion.
7. If the NSIE bit is a 1, IRQ is also asserted and NSIA is set to a 1 when NEWS is set to a 1. NSIA is cleared by writing a 0 into the NEWS bit, which also causes IRQ to return high if no other interrupt requests are pending.

Note: Steps 3 and 4 can be accomplished simultaneously.

SOFTWARE INTERFACE CONSIDERATIONS

INTERRUPT REQUEST HANDLING

DSP interface memory registers 00, 10, 1E, and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER) and register 10 is the Transmit Buffer (TBUFFER). Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits.

When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using IRQ) or by being interrupted by IRQ. When an interrupt enable bit and the corresponding interrupt flag are both set to a 1, IRQ is asserted and the corresponding interrupt active bit set to a 1.

The interrupt flag setting conditions are status changed detected, configuration changed acknowledged, receive buffer full and transmit buffer empty. Table 13 identifies the interrupt conditions and bits, and describes the interrupt clearing procedures.

Table 13. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
NSIA	NSIE	NEWS	New status detected (NEWS transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A, 0B, 0E, or 0F	Host writes a 0 into NEWS (Clears NSIA to a 0)
NCIA	NCIE	NEWC	New configuration acknowledged by DSP (NEWC transitioned from a 1 to a 0)	Host writes a 0 into NCIE (Clears NCIA to a 0)
TDBIA	TDBIE	TDBE	Transmitter Data Buffer is empty and can be written (TDBE transitioned from a 0 to a 1)	Host reads from or writes to register 10 (TBUFFER) (Clears TDBE and TDBIA to 0)
RDBIA	RDBIE	RDBF	Receiver Data Buffer is full and can be read (RDBF transitioned from a 0 to a 1)	Host reads from or register 00 (RBUFFER) (Clears RDBF and RDBIA to 0)

DIAL PROCEDURE

The host dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 8). The modem timing accounts for the DTMF tone duration and amplitude, pulse make/break ratio, and interdigit delay. These dialing parameters are host programmable in DSP RAM.

The level of the high DTMF tone is 2 dB greater than the level of the low DTMF tone.

The dialer default parameters are given in Table 14.

Table 14. Dial Default Parameters

Parameter	Default Value
DTMF Tone Duration	70 ms
DTMF Interdigit Delay	70 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	– 4 dBm
DTMF High Band Power Level	– 2 dBm
Pulse Relay Make Time	40 ms
Pulse Relay Break Time	60 ms
Pulse Interdigit Delay	750 ms

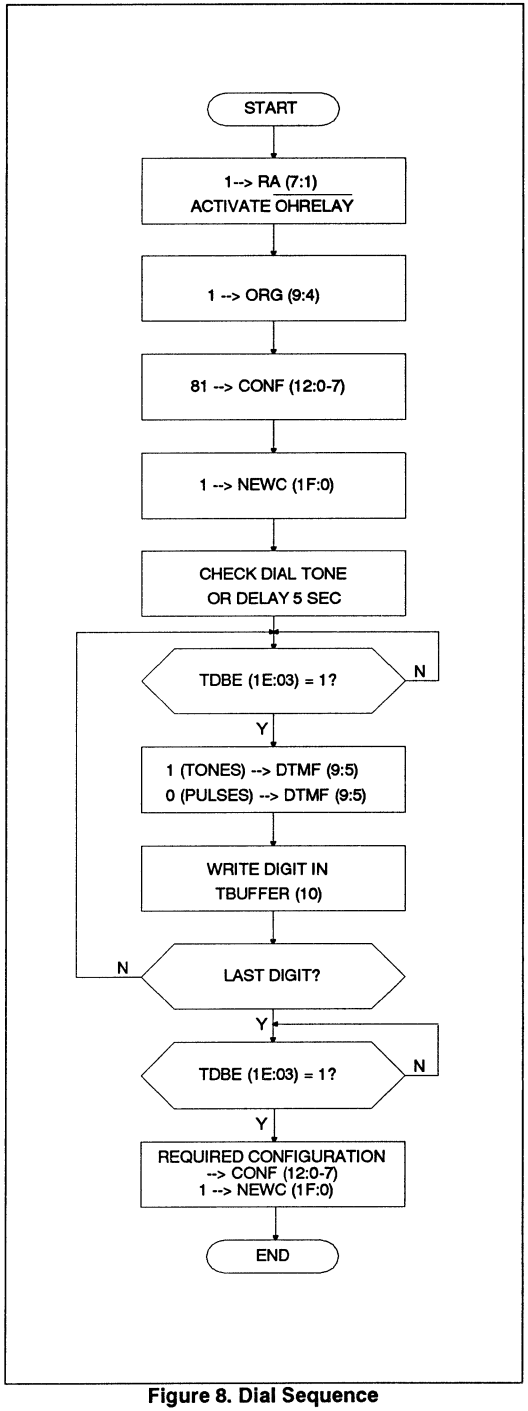


Figure 8. Dial Sequence

DESIGN CONSIDERATIONS

REQUIRED MODEM INTERFACE CIRCUIT

The RC2324DP/DS is supplied as two VLSI devices to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit (Figure 9) and parts list (Table 15) illustrate the connections and components required to connect the modem to the OEM electronics.

DAA INTERFACE

The following discussion of the interface to the integrated analog device is presented to enable designers to modify the design of the recommended line interface circuit. Also, the designer may wish to incorporate an existing line interface design with the modem device set.

Receive Input

Receive In (REC IN) and Receive Out (REC OUT) are pins associated with an integrated uncommitted operational amplifier inside the IA device. In conjunction with the three discrete components shown (R13, R14 and C11), the amplifier forms a first order lowpass antialiasing filter. This filter's function is to attenuate high frequency noise near and above the effective sampling rate of the integrated bandsplit filters (230.4 KHz).

The design of the modem requires that the pole of the anti-aliasing filter be fixed at 2337 Hz. This is calculated using the formula

$$\text{Filter Pole (Hz)} = 1/(2\pi \cdot R14 \cdot C11)$$

The recommended values of 68.1 KΩ for R14 and 1000 pF for C11 give the correct value for the filter pole. Some flexibility in choosing the component values for R14 and C11 is permissible provided that the pole of the filter is maintained within approximately ±5% of the correct value. When calculating the pole of the filter, component tolerances should be carefully considered.

Transmit Output

An external discrete smoothing filter must be added to the Transmit Output (TRAN OUT) signal to attenuate the high frequency aliases generated by the integrated switched capacitor filters. This is necessary to meet FCC requirements on transmitted high frequency energy. The pole of this filter may be calculated using the same formula as for the receiver filter, i.e.,

$$\text{Filter Pole (Hz)} = 1/(2\pi \cdot R16 \cdot C12)$$

The components values of R16 = 68.1 KΩ and C12 = 1000 pF place the pole at 2337 Hz. This may seem unusual as the response of a smoothing filter is generally designed to be flat in the band of interest, and then rolling off before the sampling rate. The bandsplit filter inside the IA is pre-distorted so that when cascaded with an external continuous first order smoothing filter, the response across the band is flat.

Some flexibility in choosing the values for R16 and C12 is permissible, provided some guidelines are followed. The choice of R16 and C12 must position the filter pole within ±5% of 2337 Hz.

The TRAN OUT integrated driver can drive a resistive load as low as 10 KΩ . This drive capability is desirable for the FCC Part 68 defined "programmable" mode.

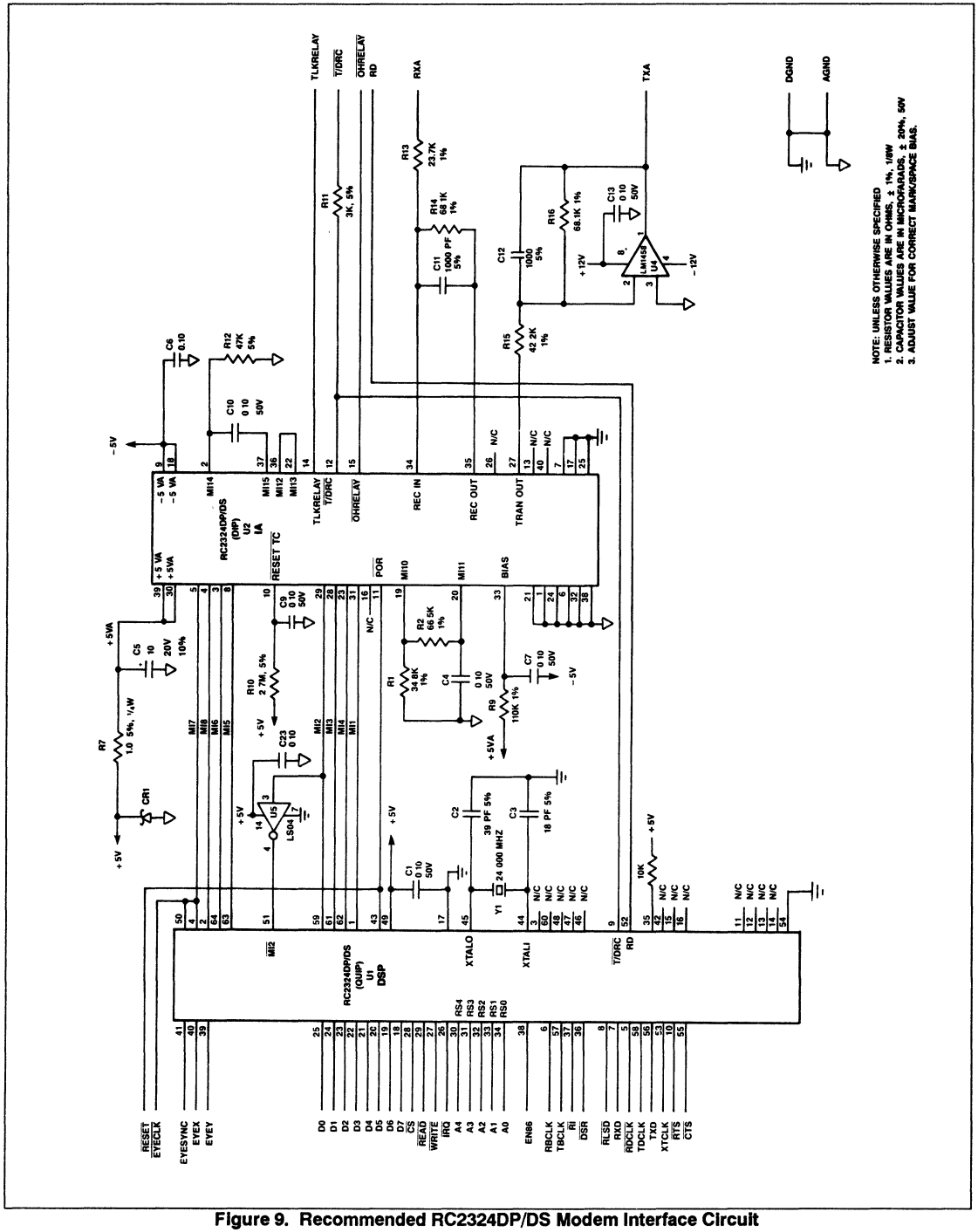


Figure 9. Recommended RC2324DP/DS Modem Interface Circuit

Table 15. Recommended Modem Interface Circuit

Qty	Part Number	Description
1	U1	Rockwell RC2424DP/DS DSP
1	U2	Rockwell RC2424DP/DS IA
1	U4	1458 Dual Op
1	U5	SN74LS04 Hex Inverter
1	Y1	24.00014 MHz Crystal
8	C1, C4, C6, C7, C9, C10,C13, C23	0.10 µF, 20%, 50V
1	C2	39 pF, 5%, 50V
1	C3	18 pF, 5%, 50V
1	C5	10 µF, 5%, 50V
2	C11, C12	1000 pF, 5%, 50V
1	R1	34.8K Ω, 1%, 1/8 W
1	R2	66.5K Ω, 1%, 1/8 W
1	R7	1 Ω, 5%, 1/4 W
1	R9	110K Ω, 1%, 1/8W
1	R10	2.7M Ω, 5%, 1/8 W
1	R11	3K Ω, 5%, 1/8 W
1	R12	47K Ω, 5%, 1/8 W
1	R13	23.7 K Ω, 1%, 1/8 W
2	R14, R16,	68.1K Ω, 1%, 1/8 W
1	R15	42.2K Ω, 1%, 1/8 W
1	CR1	Schottky Diode, LL103B

PC BOARD LAYOUT GUIDELINES

The following guidelines should be adhered to when laying out a printed circuit board for the RC2324DP/DS devices. The pin numbers reflect the DSP 64-pin QUIP and the IA 40-pin DIP packages.

1. The DSP, IA and all supporting analog circuitry, including the data access arrangement should be located on the same area of printed circuit board.
2. The DSP device grounds should be routed separately from the IA device.
3. The DSP should be located on the pin 1 side of the IA device.
4. IA digital signals (pins 3, 4, 5, 8, 10, 12, 23, 28, 29, and 31) should be routed directly to the DSP, avoiding all analog components.
5. Routing of the RC2324DP/DS signals should provide maximum isolation between noise sources and noise senitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The DSP and IA noise source, neutral, and noise sensitive pins are listed in Table 16.
6. A 1.0Ω/10 µF RC network is needed to decouple the +5V supply. This must be done at the IA device to isolate it from the DSP device.
7 As a general rule, digital signals should be routed on the component side of the PCB while the analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
8. All power traces should be at least a 0.1 inch width.
9. The analog components should be located on the pin 40 side of the 40-pin IA device.
10. The IA AGND pins (1, 6, 21, 24, 32, and 38) and the DGND pins (7 and 25) should be tied together as ground directly under the device.
11. A 0.1 µF ceramic capacitor is used to decouple the –5V supply. This should be done in the immediate proximity of the IA device.
12. All circuitry connected to crystal pins 44 and 45 on the DSP device should be kept short to prevent stray capacitance from affecting the oscillator.

Table 16. RC2324DP/DS Pin Noise Characteristics

Device	Function	Noise Source	Neutral	Noise Sensitive
DSP 64-Pin QUIP	+5V DGND Crystal Control Eye Pattern Host Bus Interface Serial Interface IA Interface No Connection	 4, 41 5-7, 53, 56-58 1-2, 50-51, 59, 61-64 	49 17, 54 9, 38, 43, 52 39-40 18-34 8,10,36-37,55 3, 11-16, 35, 42, 46-48, 60	 44, 45
DSP 68-Pin PLCC	+5V DGND Crystal Control Eye Pattern Host Bus Interface Serial Interface IA Interface No Connection	 27, 56 39, 42-44, 57-59 36-37, 45, 47-50, 52-53 	35 1, 15, 19, 40, 51, 54 24, 29, 38, 61 25-26 2-14, 16-18, 20, 22-23, 41, 60, 62 21, 28, 32-34, 46, 55, 63-68	 30-31
IA 40-Pin DIP	+5VA –5VA DGND AGND Control Analog DSP Interface No Connection	 3-5, 8, 23, 28-29, 31 	30, 39 9, 18 7, 17, 25 1, 6, 21, 24, 32, 38 10, 14-15 12 11, 13, 16, 40	 2, 19-20, 22, 26-27, 33-37
IA 44-Pin PLCC	+5VA –5VA DGND AGND Control Analog DSP Interface No Connection	 4-5, 7, 10, 25, 31-32, 34 	33, 43 11, 20 9, 19, 27 2, 8, 23, 26, 35, 42 12, 16-17 14 1, 6, 13, 15, 18, 28, 39, 44	 3, 21-22, 24, 29-30, 36-38, 40-41

Table 17. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Maximum) @ 0°C
+ 5 VDC	±5%	85 mA	130 mA
–5 VDC	±5%	20 mA	40 mA
Note: Input voltage ripple ≤1 volts peak-to-peak.			

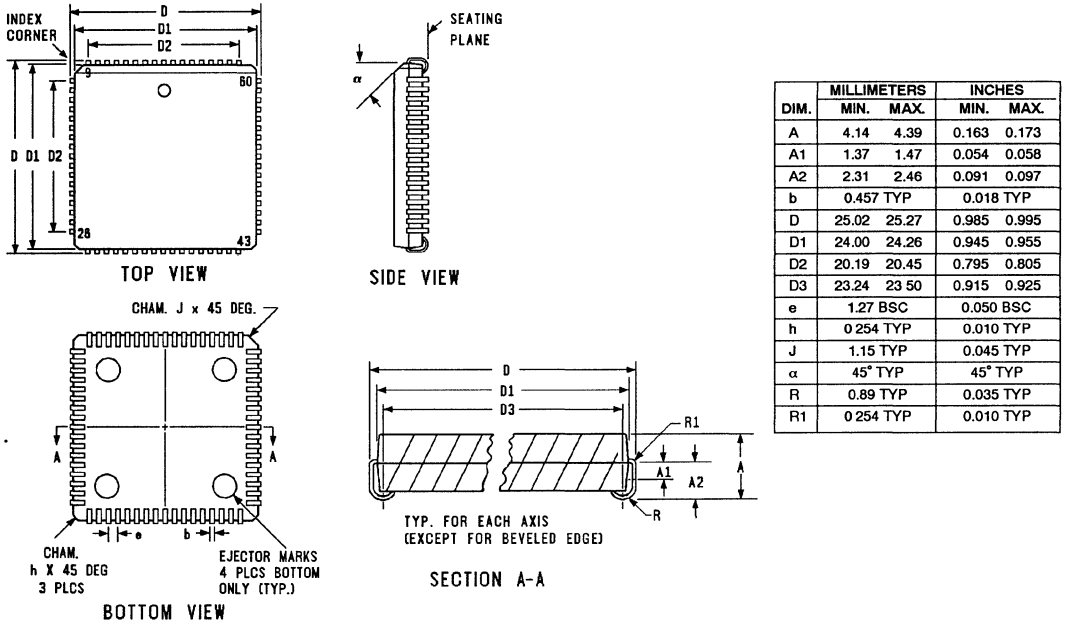
Table 18. Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to + 60°C (32°F to 140° F)
Storage	– 40°C to + 80°C (–40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	– 200 feet to + 10,000 feet

Table 19. Crystal Specifications

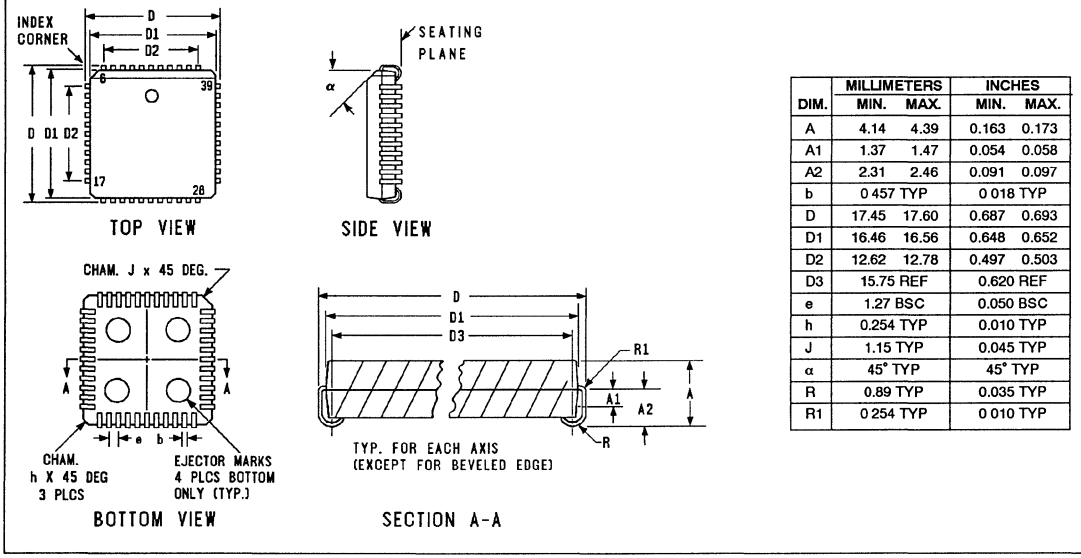
Parameter	Value
Operating Temperature	0°C to 60°C
Storage Temperature	–55°C to 85°C
Nominal Frequency @ 25°C	24.00014 MHz
Frequency Tolerance @ 25°C	±0.0015% (±15 PPM)
Temperature Stability @ T_A = 0°C to 60°C	±0.003% (±15 PPM)
Calibration Mode	Parallel resonant
Shunt Capacitance	7 pF max.
Load Capacitance	18 ±0.2 pF
Drive Level	2.5 mW max., Test at 20 nanowatts
Aging, per Year Max.	0.0005% (5PPM)
Oscillation Mode	Fundamental
Series Resistance	25 ohms max.
Max. Frequency Variation with 16.5 or 19.5 pF Load Capacitance	+0.0035% (+35 PPM)
Third Lead	Required
Sleeving	Required

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23 50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0 254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0 254 TYP		0.010 TYP	

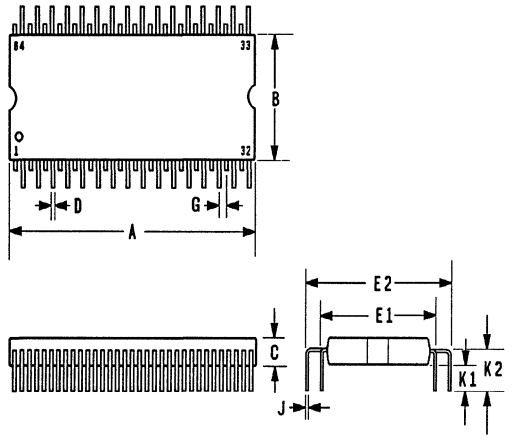
68-Pin PLCC



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0 457 TYP		0 018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0 254 TYP		0 010 TYP	

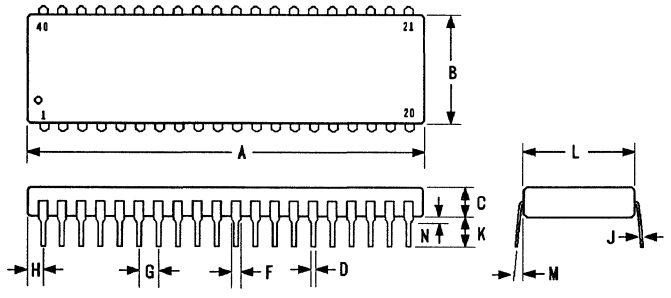
44-Pin PLCC

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	41.10	41.61	1.618	1.638
B	17.02	17.23	0.670	0.690
C	3.56	4.58	0.140	0.180
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	2.92	3.18	0.115	0.125
K2	4.83	5.34	0.190	0.210

64-Pin Plastic QUIP



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

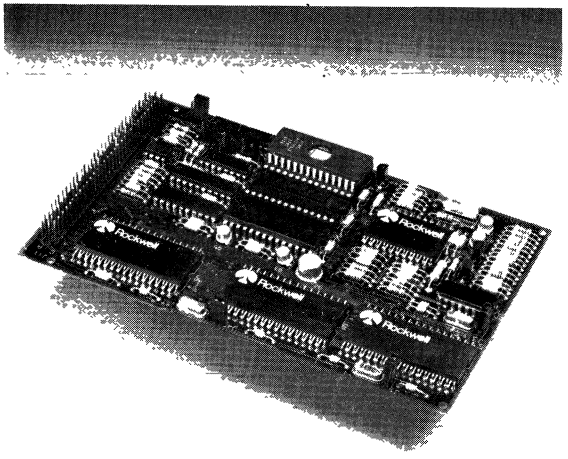
40-Pin Plastic DIP

RC2324SME System Module

INTRODUCTION

The Rockwell RC2324SME System Module is a smart multi-mode modem on a single Eurocard module. The hardware includes a 2400 bps full-duplex modem device set, a microcomputer, ROM, RAM, a socket for an OEM-supplied parameter ROM, and peripheral I/O circuits. The OEM adds a power supply, host and telephone line interfaces, indicators, switches and country dependent parameters in a ROM to complete the modem. A back-up battery and call progress audio monitor hardware can also be added.

Resident microcomputer firmware provides the basic modem control including an enhanced AT command set, V.25 bis, Call Progress, Blacklisting, and MNP protocol for both class 4 and 5. In addition, a unique open architecture with a convenient software structure allows for OEM customization of the product.



RC2324SME Module

FEATURES

- Eurocard 2400 bps modem with integrated microcontroller
- Enhanced AT command set
- Enhanced V.25 bis protocol for both synchronous and asynchronous operation
- OEM-supplied parameters in ROM for up to 16 countries
  - Call progress parameters
  - Blacklisting parameters
  - Alter AT result codes and messages
  - DAA configuration
  - Add/disable/rename AT commands
  - Alterable V.25 bis indicator messages
  - OEM configurable tone/pulse dialing parameters
- Automatic line mode/speed recognition of CCITT modes
- Compatibilities
  - CCITT V.22 bis - 2400 bps
  - CCITT V.22A/B - 1200 and 600 bps
  - CCITT V.23 - 1200 bps/75 bps
  - CCITT V.21 - 300 bps
  - Bell 212A - 1200 bps
  - Bell 103 - 300 bps
- MNP error correcting protocol class 4 and data compression class 5
- DTE autobaud/autoparity in both AT and V.25 bis
- Synchronous and asynchronous DTE interface
- Speed buffering from 75 bps to 9600 bps
- Flow control: RTS/CTS or XON/XOFF with programmable XON/XOFF threshold and repeat margin
- Receiver dynamic range: –9 dBm to –43 dBm
- Clock selection: internal, external, or slave
- Asynchronous character format
  - 7 or 8 data bits
  - 1 or 2 stop bits
  - Odd, even, mark, space, or no parity
- Tone detection: 100 Hz – 1000 Hz
- AUX DTE bus (RS-232-C/V.24)
- Voice data switching
- Auto/manual call/answer with front panel dial support
- Leased line mode
- 550 Hz and 1800 Hz guard tone
- 1300 Hz calling tone

SYSTEM OVERVIEW

HARDWARE

The RC2324SME card includes the following major components:

- R65012 Microcomputer
- 64K x 8 System ROM
- 12K x 8 OEM ROM Socket (27128 or 27256 compatible)
- 32K x 8 RAM
- RC2324DP/DS Modem Device Set
- DAA Interface

The R65012 Microcomputer provides the modem control processing and interfaces to the DTE. The RC2324DP/DS Modem provides 2400 bps modem data pump functions. The DAA interface provides signal lines for transmit and receive data, two for telephone signal sensing, and four for relay control. On-board ROM and RAM contain the resident firmware. Country specific parameters are user-selectable and discussed in the firmware interface section. Figure 1 shows the major system components of the RC2324SME module.

MODES OF OPERATION

AT Mode

The RC2324SME AT command set is Hayes compatible. Additional compatibility with the Dowty Quattro and Microcom AT command set implementations, with emphasis on the European environment, is provided. The AT command set and S-register values are listed in Table 1 and Table 2, respectively.

V.25 bis Mode

RC2324SME supports DTE/DCE communication according to CCITT Recommendation V.25 bis. Commands are received from the DTE (one command per input line) in either synchronous or asynchronous formats. Each command may contain up to 60 characters of information. The V.25 bis command set is summarized in Table 3.

Hayes is a registered trademark of Hayes Microcomputer Products, Inc.
Microcom is a trademark of Microcom.
Quattro is a trademark of Dowty Information Systems.

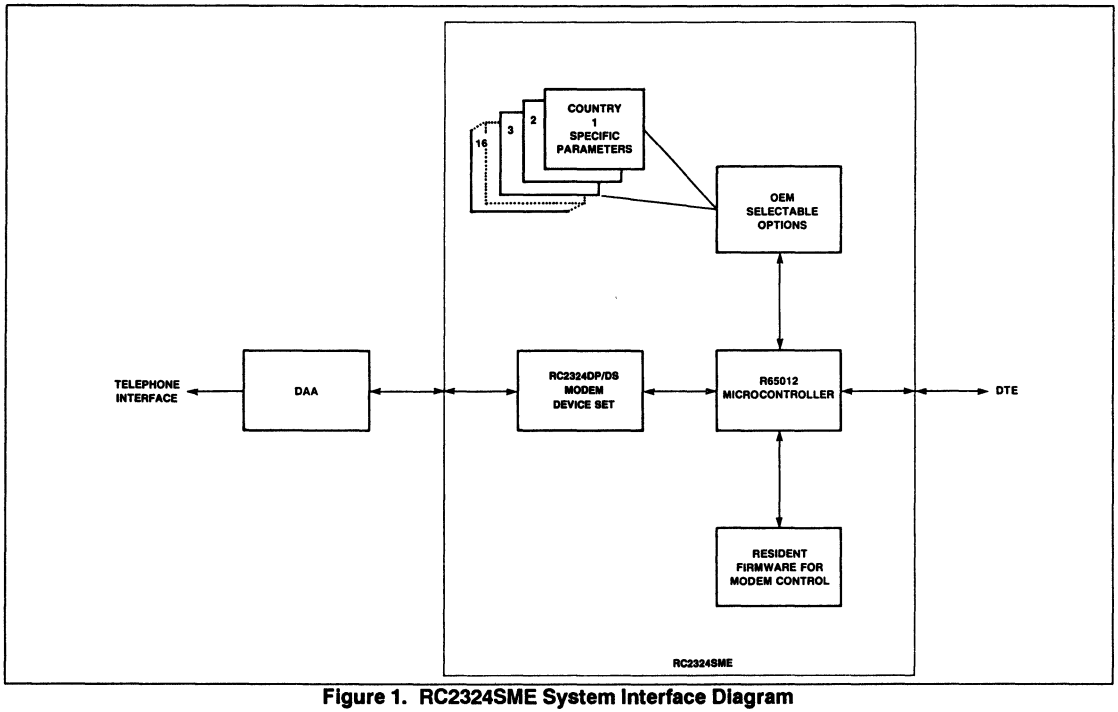


Figure 1. RC2324SME System Interface Diagram

Table 1. RC2324SME AT Command Set Summary

AT Command	Function
AT	Attention Code
A	Answer Mode
Bn	Bell/CCITT Command
D	Dial Command
En	Echo Command
Fn	Line Mode/Speed Preference Select
Hn	On-Hook Command
In	Product Code/Checksum Request
Ln	Speaker Volume Command
Mn	Speaker On/Off Command
Nn	Command Slot Entry Execute
On	On-Line Command
Pn	Pulse Dial Command
Qn	Quiet Command
Sn	S-Register Read/Write
Tn	Touch Tone Dial
Vn	Verbose Command
Xn	Extended Result Codes Enable/Disable
Yn	Control Long Space Disconnect
Zn	Configuration Reset command
%An	Set Auto-Reliable Fallback Character
%Bn	Print List of Blacklisted Numbers
%Cn	Data Compression (MNP5) Enable/Disable
%Dn	Print List of Delayed Numbers
%En	Auto-Retrain Enable/Disable
%Kn?	Auto Detect Select for MNP Link Request
%Mn	Async Commands on Auxiliary Port; Sync DTE on Primary Port
%Qn	XON/CTS ON Threshold Selection
%R	S-Register Content Display
%Sn	XOFF/CTS OFF Threshold Selection
&An	Control Line Speed Detect
&Cn	Data Carrier Detect Options
&Dn	Data Terminal Ready Options
&Fn	Fetch Factory Profile
&Gn	Guard Tone Command Set
&In	DTE Speed Adjust
&Jn	Telephone Jack Selection
&Ln	Leased Line Operation
&Mn	Synchronous Mode Selection
&On	S-Register Input/Output Format
&P	Dial Pulse Ratio
&R	RTS/CTS Option
&Sn	DSR Option
&Tn	Test Command Selection
&W	Active Configuration Write
&Xn	Clock Source Selection
&Z	Store Telephone Number
\An	Maximum MNP Block Size Selection
\Bn	Transmit Break-to-Remote
\Cn	Auto-Detect Link Request/Fallback Select
\Fn	Command Directory Display
\Gn	Modem-to-Modem Flow Control
\Kn	Break Control
\Ln	MNP Block Transfer Control
\Nn	Operation Mode
\O	Originate Reliable Link Manually
\Pn	Command Directory Store/Delete
\Qn	DTE to SM3 Flow Control
\S	Active Configuration Display
\U	Accept Reliable Link Manually
\Vn	MNP Result Message Enable/Disable
\Xn	ON/XOFF Control Pass Through
\Y	Accept Reliable Link Manually
\Z	Normal Mode Select
/	Execute Last Command Line

Table 2. RC2324SME V.25 bis Mode Command Set Summary

V.25 bis Mode Command V.25 bis Commands	Function
CIC	Connect Incoming Call
CRI	Call Request with Number and Identification
CRN	Call Request with Number
CRS	Call Request with Stored Number
DIC	Disregard Incoming Call
PRI	Store/Delete (Program) Identification Number
PRN	Store/Delete (Program) Number
RLD	Request List of Delayed Numbers
RLF	Request List of Forbidden Numbers
RLI	Request List of Identification Numbers
RLN	Request List of Stored Numbers
Additional Commands	
ARB*	Auto-Detect of Link Request/Fallback
ART	Auto-Retrain Enable/Disable
CBT*	MNP Block Transfer Control
CLP	Change Line Protocol
CNA	Change Number of Incoming Rings
CSP*	Change DTE Speed
DLN	Dial Last Number
ECH*	Echo Control
ERM*	Enable/Disable Reliable Messages
FBC*	Specify MNP Auto-Fallback Character
FLO*	Pass Through XON/XOFF Control
MBS*	Select Maximum MNP Block Size
OFT*	Select XOFF (or CTS OFF) Threshold
ONT*	Select XON (or CTS ON) Threshold
OST	Display On-Line Status
RES	Reset System
SDC*	Select Data Compression
SIT*	Set Inactivity Timer
SLF*	Select Local Flow Control
SOM*	Operation Mode Control
SPC	Speaker Control
SPD	Set Pulse Dialing
SPV	Speaker Volume
SRF*	Select Remote Flow Control
STD	Set Tone Dialing
SRF*	Modem to Modem Flow Control
STD	Set DTMF Dialing

* Asynchronous mode only

HARDWARE INTERFACE

The hardware interface consists of the external signals shown in Figure 2.

MAIN DTE BUS

The Main DTE bus provides the signal lines described in specifications RS-232C and V.24. The bus transmits data and commands from the host (DTE) to the RC2324SME module (DCE) and receives data and responses from the DCE. The signal levels are TTL compatible. The bus also provides the clock inputs and outputs for synchronous DTEs and three signals for diagnostic testing per CCITT Recommendation V.54. The Main DTE bus is selected at power-up.

AUXILIARY DTE BUS

Under program control, the Auxiliary DTE bus may duplicate the asynchronous functions of the Main DTE bus (except for clock and diagnostic signals).

SWITCH INPUTS

Fifteen switch inputs are sampled. The four front panel switch inputs are read continuously. The eleven internal switch inputs are read only at power-up or reset.

Front Panel Switch Inputs

Talk/Data (TALK/DATA). The TALK/DATA switch input selects data mode or talk mode. In addition, the SELECT switch input selects a phone number to be dialed (V.25 bis mode) or a command string (AT mode) to be performed upon subsequent transitions of TALK to DATA when SELECT is on.

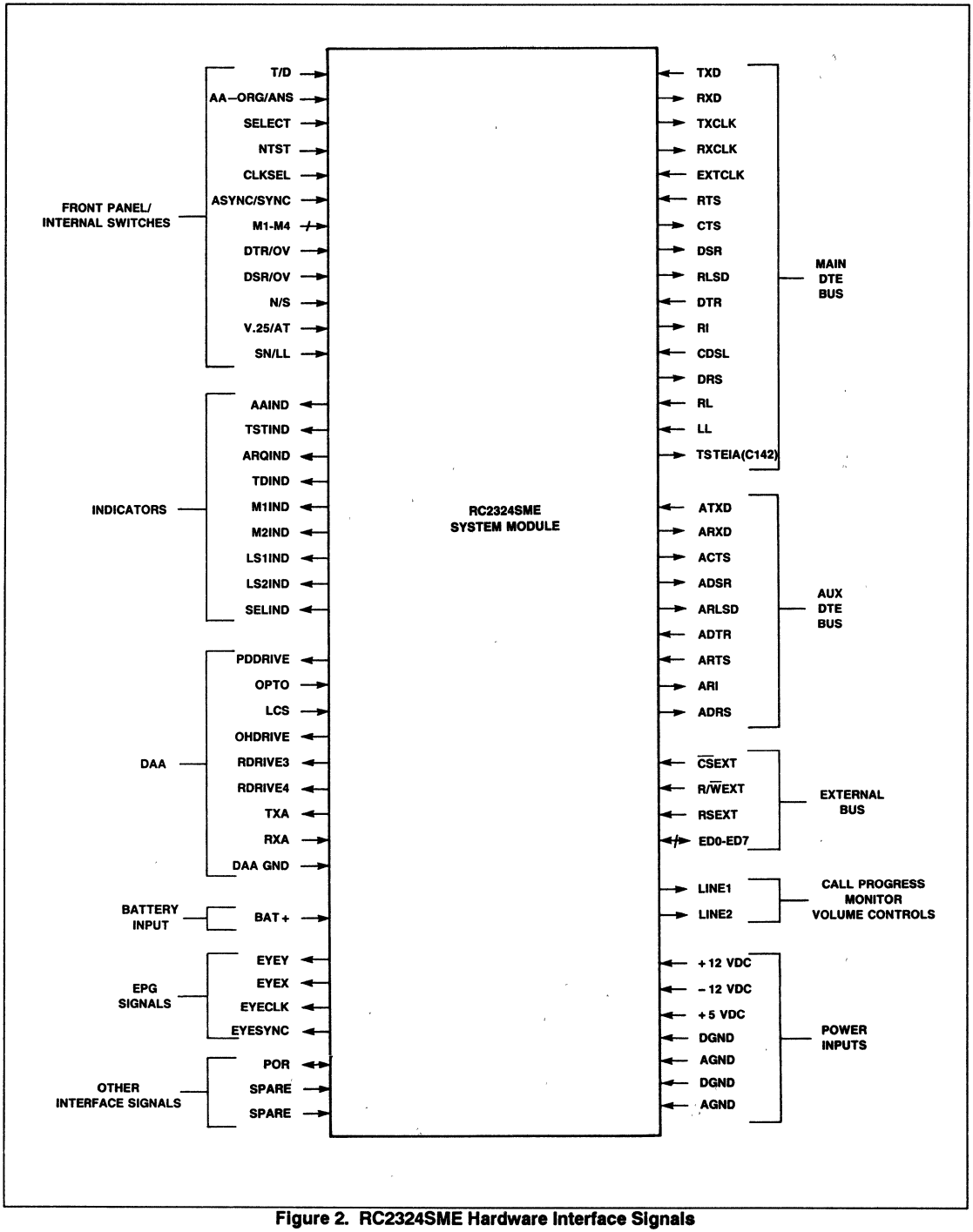


Figure 2. RC2324SME Hardware Interface Signals

Auto Answer (AA)/Originate/Answer (ORG/ANS). The AA-ORG/ANS switch input can be used to set or reset auto answer (AA) mode from the front panel. The TALK/DATA switch input can cause the firmware to pursue a handshake in originate mode or cause the firmware to handshake in answer mode.

Select (SELECT). The SELECT switch input acts like a terminal shift key by changing the meaning of the TALK/DATA and AA-ORG/ANS switches.

Normal/Test (NTST). The NTST switch input selects either normal mode of operation or test mode.

Internal Switch Inputs

Clock Select (CLKSEL). The CLKSEL switch input determines whether the transmit clock is applied to the main DTE Bus EXTCLK pin at the operating data rate for synchronous operation or whether the data is synchronized to an internal clock. In both cases, the clock is presented to the main DTE bus TXCLK pin. This switch input is used in conjunction with the Clock Normal/Slave (N/S) switch.

Async/Sync Select Switch. The Async/Sync Select switch input selects asynchronous mode or synchronous mode 3 of operation.

Mode 1, 2, 3 and 4 (M1, M2, M3, M4). The firmware reads M1, M2 M3 and M4 switch inputs during initialization and uses the values as defaults to set the RC2324SME modem to recognize one or more specific modem-to-modem connection protocols and speeds.

DTR Override (DTR/OV). The DTR/OV switch input forces DTR ON or allows the DTE to control the state of DTR. DTR/OV affects DTR operation on the Main DTE bus.

DSR Override (DSR/OV). The DSR/OV switch input forces the DSR and RLSD outputs ON for both the main and auxiliary DTE buses or it allows these signals to act in a normal manner.

Clock Normal/Slave (N/S). The N/S switch input is used in conjunction with the CLKSEL switch input.

V.25 bis/AT Mode Select (V25/AT). The V25/AT switch input selects either the AT command set or the V.25 bis mode. This input is read by the controller firmware during initialization and indicates which DTE command set to use.

Switched Network/Leased Line Select (SN/LL). The SN/LL switch input selects either switched network operation or leased line operation.

INDICATOR INTERFACE

Nine lines drive front panel indicators. Four lines are associated with momentary front panel switches to indicate their state.

Auto Answer (AA)

The AA output indicates when the auto answer mode is selected.

Test (TSTIND)

The TSTIND output indicates when a self test or Select 1 condition occurs. Select 1 shows that the user has chosen the first of the 4 pre-stored directory numbers selectable from the front panel.

ARQ (ARQ). The ARQ output indicates when the ARQ or the Select 2 condition occurs and when not in error correction mode. Select 2 shows that the user has chosen the second of the four pre-stored directory numbers selectable from the front panel.

Talk/Data Indicator (TDIND). The TDIND output indicates when the modem goes into data mode or a Select 3 condition occurs. Select 3 shows that the user has chosen the third of the 4 pre-stored directory numbers selectable from the front panel.

Mode 1 (MODE1) and Mode 2 (MODE2). The MODE1 and MODE2 outputs indicate the connection protocol. These indicator lines also show that the user has chosen the fourth of the four pre-stored directory numbers selectable from the front panel.

Line Speed 1 (LS1) and Line Speed 2 (LS2). The LS1 and LS2 outputs indicate the connected speed.

Select (SELIND) Indicator. The SELIND output indicates when the SELECT switch in on. This allows for the visual ability to determine the current (selected or unselected) meanings of multiple defined indicators.

DAA INTERFACE

The DAA interface provides the signal lines for transmit and receive data. Two lines are used for telephone signal sensing and four for relay control.

CALL PROGRESS VOLUME CONTROLS

Two output lines control the volume of a call progress audio monitor.

BATTERY CONNECTIONS

A battery connection supplies standby power to the RC2324SME module RAM in order to retain directory and configuration data during power-down and intermittent power losses. The battery must have a voltage range of +2.3 Vdc to +5.5 Vdc. The maximum current consumption is 51 μA.

COUNTRY CODE JUMPERS

Four country code jumpers select the country code. Each jumper combination selects a set of OEM-supplied country dependent parameters. The RC2324SME module can be customized for up to 16 countries with no other on-board changes.

OEM ROM SOCKET

A 28-pin IC socket is provided for installation of an OEM supplied EPROM/ROM device that occupies 12K bytes of the RC2324SME address map. The interface is compatible with a 27C128/27C256 EPROM with an access time of 150 ns or less.

MICROCOMPUTER FIRMWARE

The microcomputer firmware provides the following major functions:

- Operating system
- Modem device set control and monitoring
- DTE interface control and monitoring
- AT command set processing
- V.25 bis command set processing
- OEM parameter interface

OEM PARAMETER INTERFACE

The firmware provides a well-defined mechanism for the installation and incorporation of OEM-supplied predefined OEM configuration parameters on a country basis for up to 16 countries. The parameters are included in an OEM-supplied ROM. Jumpers on the RC2324SME card allow selection of one of 16 sets of country dependent parameters upon power-up reset.

The OEM parameters are linked to the operating system through a set of pointers — one set for each of up to 16 countries. The pointers are :

Default AT Command String for AT Command Mode. This pointer locates a string of AT style commands which the OEM can preset before modem operation in the AT command mode.

Default Command String for V.25 bis mode. This pointer locates a string of commands which the OEM can preset before modem operation in the V.25 bis mode.

Call Progress, Blacklisting and Dial Parameters. This pointer locates a block of country dependent parameters supporting dialing, call progress and blacklist operation. Table 3 identifies the parameters that can be included.

AT Mode Result Messages. This pointer locates a list of OEM-modified AT mode messages. The default result messages are listed in Table 4.

V.25 bis Mode Indications. This pointer locates a list of OEM-modified V.25 bis mode indications. Table 4 lists the default V.25 bis indications.

OEM Modified AT Commands . This pointer locates a list of OEM modified AT commands.

Table 3. Country Dependent Parameters

No. Bytes	Parameters
1	Country Code
3	International Access Dial Code
1	Blacklist Size
20	Define Tone-A Filter
20	Define Alternate Tone-A Filter
2	Progress Tone Filter Threshold
2	Connect Threshold Level
2	Leased Line Threshold Level
1	Transmit Level Attenuation Select
1	DTMF Tones Transmit Level
1	Leased Line Transmit Level
2	Receive Threshold for Dial Tone
2	Reserved
1	Maximum Time to Wait for Dial Tone
1	Minimum Time for Which Dial Tone Is Present
1	Maximum Allowable Time Dial Tone Loss
2	On Time for Primary Tone Cadence
2	Off Time for Primary Tone Cadence
12	Cadence Ring Parameters
12	Cadence Busy Parameters
12	Cadence Congestion Parameters
12	Cadence Unobtainable Parameters
12	Cadence Progress Tone Parameters
5	Cadence Repetition Counts
1	Difference Maximum Time to No Ring Wait Time
1	Maximum Time to Wait for Connect
1	Pulse Make Time
1	Pulse Break Time
1	Pulse Dial Setup Time
1	Pulse Dial Clear Time
1	Pulse Dial Interdigit Time
1	Dial Pulse Code
1	Relay Control for On-Hook/Off-Hook Action
1	Relay Control for Make/Break Action
1	Relay Control for Set/Clear Action
2	DTMF Tone On Time
2	DTMF Tone Interdigit Time
8	Blacklist Action Items
1	Reserved
2	Minimum Time to Delay Beween Calls
8	Blacklist Delay Parameters
6	Reserved
2	Blacklist Final Delay Time
1	Number of Times Blacklist Delay 1 is Used
1	Maximum Number of Tries to Fail
1	Maximum Number of Tries per Blacklist Period
1	Maximum Time Allowed Off-Hook
1	Option Flags Byte 1 Bit 0 Disable All Blacklisting Bit 1 Cause Modem To Stop Originate When Blacklist is Full Bit 2 Disable the Operator Clearing Of Blacklist Bit 3 Enable Blind Dialing On No Dial Tone Bit 4 Enable Check For Busy While Dialing Bit 5 Enable the Calling Tone Bit 6 Disable the Return to Command ";" Bit 7 Enable Alternate Dial Tone Filter

Table 3. Country Dependent Parameters (Cont'd)

No. Bytes	Parameters
1	Option Flags Byte 2 Bit 0 Enable the 1800 Hz Guard Tone Bit 1 Enable the 550 Hz Guard Tone Bit 2 Enable Line Current Sense Processing Bit 3 Enable "R" ATD modifier Bit 4 Enable Adaptive Dialing Features Bit 5 Enable Alternate Gain Relay Bit 6 Enable Pulse Grounding Relay Bit 7 Disable Monitoring for V.21 and V.23 "No Answer Tone" Modems
	Permanently Blacklisted Numbers (variable length)

Table 4. Result Codes, Messages, and Indications

AT Code	AT Command Message	V.25 bis Command Indication
00	OK	VAL
01	CONNECT	CNX 300
02	RING	INC
03	NO CARRIER	CFINC
04	ERROR	INV
05	CONNECT 1200	CNX 1200
06	NO DIAL TONE	CFIDT
07	BUSY	CFIET
08	NO ANSWER	CFIRT
09	CONNECT 600	CNX 600
10	CONNECT 2400	CNX 2400
12	RDL GRANTED	RDL GRANTED
13	RDL DENIED	RDL DENIED
14	TRYING TO CONNECT	N/A
15	ABORT	CFIAB
16	INACTIVITY TIMEOUT	ITO
17	CIRCUIT BUSY	CFINS
18	TERMINAL NOT READY	CFICB
19	REDIALING	N/A
20	RELIABLE	RELIABLE
21	NOT RELIABLE	NOT RELIABLE
22	N/A	EOL
24	DELAYED n	DLC
25	V.23 CONNECT 75TX/1200RX	CNX 75TX/1200RX
26	V.23 CONNECT 1200TX/75RX	CNX 1200TX/75RX
27	CONNECT 75	N/A
28	CONNECT 110	N/A
29	CONNECT 150	N/A
30	CONNECT 4800	N/A
31	CONNECT 9600	N/A
32	BLACKLISTED	CFIFC
33	RELIABLE COMPRESSED	RELIABLE COMPRESSED

GENERAL SPECIFICATIONS

Modem Power Requirements

Voltage*	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
+ 5 VDC + 5%, –2.5%	320 mA	535 mA
+ 12 VDC ± 5%	4 mA	5 mA
– 12 VDC ± 5%	43 mA	50 mA

* Input voltage ripple ≤ 0.1 volts peak-to-peak.

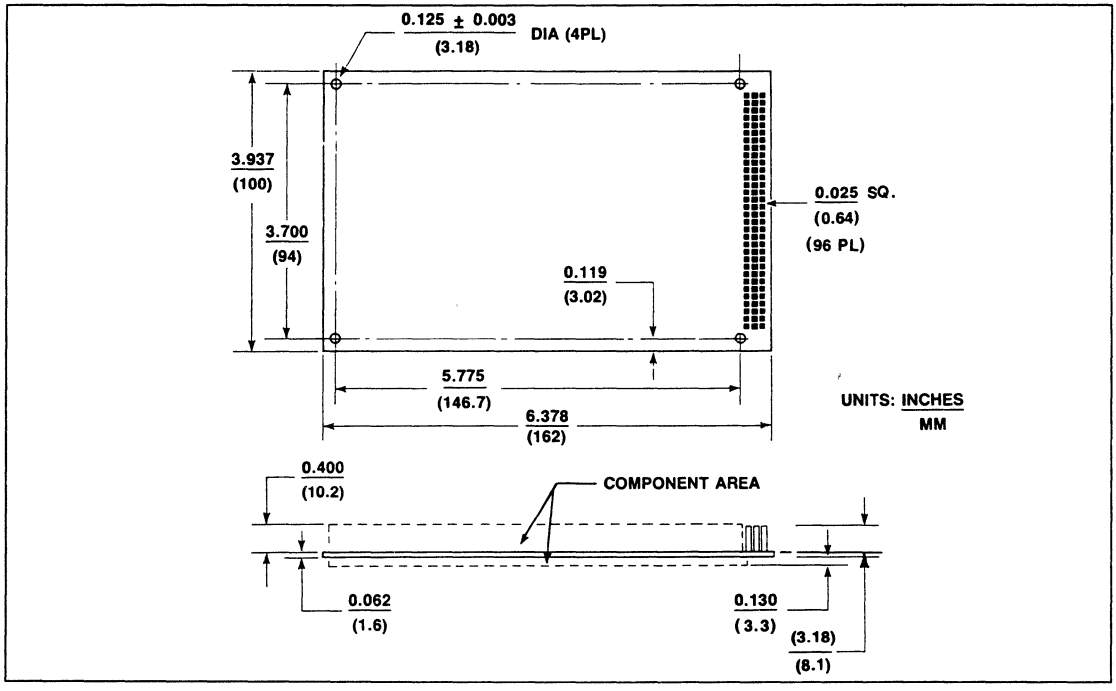
Modem Mechanical Dimensions

Parameter	Specification
Board Structure	Single PC board with three rows of 32 vertical pin positions, compatible with a 96-pin DIN receptacle. Each row has 31 pins installed, with pins 31a, 31b, and 31c removed for keying.
Dimensions	
Width	3.937 in. (100 mm)
Length	6.378 in. (162 mm)
Component Height	
Top (max.)	0.360 in. (9 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.)	5 oz. (140 g)
Pin Length (max.)	0.315 in. (8 mm)

Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0° C to + 60° C (32° F to 140° F)
Storage	– 40° C to + 80° C (–40° F to 176° F) (Stored in heat sealed antistatic bag and shipping container.)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35° C, whichever is less.
Altitude	– 200 feet to + 10,000 feet

DIMENSIONS


0.125 ± 0.003
(3.18)
DIA (4PL)
3.937
(100)
3.700
(94)
0.025 SQ.
(0.64)
(96 PL)
0.119
(3.02)
5.775
(146.7)
6.378
(162)
UNITS: INCHES
MM
0.400
(10.2)
COMPONENT AREA
0.062
(1.6)
0.130
(3.3)
(3.18)
(8.1)

Rockwell

RC2324SME/DS
Multi-Mode Modem Device Set

INTRODUCTION

The Rockwell RC2324SME/DS is a smart multi-mode modem device set. The device set consist of four components — a microcontroller, a digital signal processor (DSP) device, an integrated analog (IA) device, and a ASIC gate array. The DSP, microcontroller, and ASIC gate array are available in a 64-pin quad in-line package (QUIP) or a 68-pin plastic leaded chip carrier (PLCC) package. The IA device is available in a 40-pin dual in-line package (DIP) or a 44-pin PLCC package.

Resident microcomputer firmware provides the basic modem control including an enhanced AT command set, V.25 bis, Call Progress, Blacklisting, and MNP protocol for both class 4 and 5. In addition, a unique open architecture with a convenient software structure allows for OEM customization of the product.

FEATURES

- Enhanced AT command set
- Enhanced V.25 bis protocol for both synchronous and asynchronous operation
- OEM-supplied parameters in ROM for up to 16 countries
  - Call progress parameters
  - Blacklisting parameters
  - Alter AT result codes and messages
  - DAA configuration
  - Add/disable/rename AT commands
  - Alterable V.25 bis indicator messages
  - OEM configurable tone/pulse dialing parameters
- Automatic line mode/speed recognition of CCITT modes
- Compatibilities
  - CCITT V.22 bis - 2400 bps
  - CCITT V.22A/B - 1200 and 600 bps
  - CCITT V.23 - 1200 bps/75 bps
  - CCITT V.21 - 300 bps
  - Bell 212A - 1200 bps
  - Bell 103 - 300 bps
- MNP error correcting protocol class 4 and data compression class 5
- DTE autobaud/autoparity in both AT and V.25 bis
- Synchronous and asynchronous DTE interface
- Speed buffering from 75 bps to 9600 bps
- Flow control: RTS/CTS or XON/XOFF with programmable XON/XOFF threshold and repeat margin
- Receiver dynamic range: 0 dBm to –43 dBm
- Clock selection: internal, external, or slave
- Asynchronous character format
  - 7 or 8 data bits
  - 1 or 2 stop bits
  - Odd, even, mark, space, or no parity

Rockwell

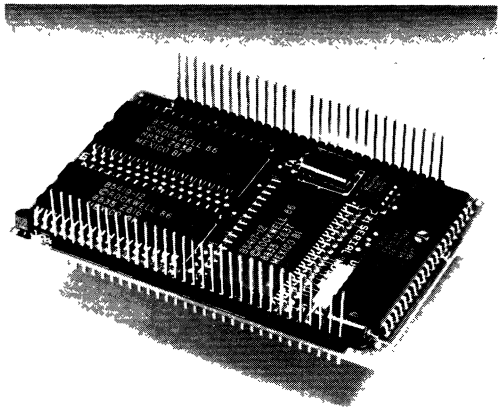
R96QT™
9600 bps QuickTurn™ Modem

INTRODUCTION

The R96QT is a high-performance 2-wire 9600 bps quick-turn modem designed for operation over the public switched (PSTN). Using state-of-the-art VLSI and signal processing technology, the R96QT combines half-duplex, fast turn around time with a low and medium speed full-duplex application in one package.

Providing proprietary fast training times of 23 ms, the R96QT is designed as an asynchronous/synchronous OEM data pump ideal for PC XT/AT and PS/2 applications.

The integrated features available in the R96QT Micromodem™ offer increased user design flexibility in a reduced package size (3.94 in. x 2.56 in.).



R96QT Modem

FEATURES

- Compatibility
  - CCITT V.29 (half-duplex), V.27 ter (half-duplex), V.22 bis, V.22A/B
  - Bell 212A, 103
- Synchronous operation
  - 9600, 7200, 4800, 2400,1200, 600, or 300 bps ±0.01%
  - Serial or parallel
- Asynchronous operation
  - 2400, 1200, 600, or 0-300 bps
  - Serial or parallel
  - Character length 8, 9, 10, or 11 bits
- 2-wire full-duplex or high speed psuedo full-duplex
- Adaptive and fixed compromise equalization
- Auto/manual dial - DTMF or pulse dial
- Programmable tone generation and detection
- Call progress tone detection
- Receiver dynamic range: – 10 dBm to – 43 dBm
- Programmable transmit level
- Proprietary fast train of 23 ms
- DTE interface
  - Microprocessor bus
  - CCITT V.24 (RS-232-C compatible)
- Built-in diagnostic capability
- Full-duplex test configurations for V.22 bis, V.22A/B, and Bell 212A
  - Local analog loopback
  - Local digital loopback
  - Remote digital loopback
- Power consumption: 3 W (typical)
- Small module with dual in-line pin (DIP) connector:
  - 100 mm x 64.7 mm (3.94 in. x 2.56 in.)

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES, AND DATA RATES

The selectable modem configurations along with the corresponding signaling (baud) rates and data rates, are listed in Table 1. Additional signaling frequencies are listed in Table 2. The receiver and transmitter configurations are established by the RCONF and TCONF bits, respectively.

NOTE: Bit names refer to control bits in DSP interface memory which are set or reset by the host processor (see Software Interface Section, Figure 4, and Table 12).

TONE GENERATION

Single Tone: Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

Answer Tone: A CCITT (2100 ±15 Hz) or Bell (2225 ±10 Hz) answer tone is generated depending on the selected configuration.

Guard Tone: An 1800 Hz ± 20 Hz guard tone can be enabled (GTE bit). The power level of the transmitted guard tone is 6 ± 1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not the guard tone is enabled.

DTMF Tones: Dual tone multi-frequency (DTMF) tones can be generated in the Call Request mode (TCONF = 80) when the DTMF bit is set to one. The DTMF tone generated is specified by the hexadecimal code loaded into the transmitter Dial Digit Register (DDR) with the appropriate digit code shown in Table 3.

Table 2. Signaling Frequencies

Mode	Frequency ±0.01% (Hz)
V.22 bis Low Channel, Originate Mode	1200
V.22 Low Channel, Originate Mode	1200
V.22 bis High Channel, Answer Mode	2400
V.22 High Channel, Answer Mode	2400
Bell 212A High Channel Answer Mode	2400
Bell 212A Low Channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

TONE DETECTION

Single Tone: In the 300 bps synchronous FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the DSP interface memory (FR1, FR2, and FR3).

Call Progress Tone: When call progress configuration is selected in the receiver, tones can be detected as follows:

Frequency Range: 340 ± 5 Hz to 640 ± 5 Hz
Detection Level: –10 dBm to –43 dBm
Response Time: 17 ± 2 ms

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ± 0.01%	Data Rate (bps) ± 0.01%	Sync/Async	Baud (Symbols/ Sec.)	Bits per Symbol	Constellation Points
V.29 FT/9600	QAM	1700, 1800[2]	9600	Sync	2400	4	16
V.29 9600	QAM	1700	9600	Sync	2400	4	16
V.29 FT/7200	QAM	1700, 1800[2]	7200	Sync	2400	3	8
V.29 7200	QAM	1700	7200	Sync	2400	3	8
V.29 FT/4800	QAM	1700, 1800[2]	4800	Sync	2400	2	4
V.29 4800	QAM	1700	4800	Sync	2400	2	
V.27 FT/4800	DPSK	1800	4800	Sync	1600	3	8
V.27 4800 Long	DPSK	1800	4800	Sync	1600	3	8
V.27 FT/2400	DPSK	1800	2400	Sync	1200	2	4
V.27 2400 Long	DPSK	1800	2400	Sync	1200	2	4
V.22 bis 2400	QAM	1200/2400	2400	Sync/Async	600	4	16
V.22 bis 1200	QAM	1200/2400	1200	Sync/Async	600	2	4
V.22 1200	DQPSK	1200/2400	1200	Sync/Async	600	2	4
V.22 600	DQPSK	1200/2400	600	Sync/Async	600	1	2
Bell 212A 1200	QAM	1200/2400	1200	Sync/Async	600	2	4
Bell 103 0-300	FSK	1170/2125	0-300	Async	300	1	–

Notes: 1. Modulation legend: QAM Quadrature Amplitude Modulation
DQPSK Differential Quadrature Phase Shift Keying
FSK Frequency Shift Keying
2. V.29 FT modes have an optional 1800 Hz carrier frequency available for use with a user-provided secondary channel.

Table 3. Dial Digits/Tone Pairs

Hex Code	Dial Digit	Tone Pairs (Hz)	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

DATA ENCODING

The data encoding conforms to CCITT recommendations V.29, V.27 ter, V.22 bis, and V.22 A/B, and to Bell interfaces 212A and 103.

EQUALIZERS

Equalization functions are incorporated to improve performance when operating over low quality lines. Delay, amplitude and cable equalizers support half-duplex operation only.

Automatic Adaptive Equalizer

An automatic adaptive equalizer is provided in the receiver circuit. The receiver is configured with a 32-tap T equalizer for half-duplex (HDX) operation. Full-duplex (FDX) modes operate with a 16-tap T/2 equalizer. Updating of the taps can be enabled or disabled (FRZEQ).

Delay Equalizer

A digital filter in the transmitter provides envelope delay equalization for half-duplex operation. The equalizer can be enabled or disabled (CDEQ).

Amplitude Equalizer

In V.29 modes, an amplitude compromise equalizer in the transmitter path can be enabled or disabled (CAEQ bit).

Link and Cable Equalizers

Selectable compromise equalizers in the receiver optimize performance over channels exhibiting severe amplitude distortion. An equalizer may be selected (CEQSEL) that meets the following standards: U.S. Survey Long, Japanese 3-Link, Cable 1, Cable 2, and Cable 3. No equalizer may also be selected. (HDX only)

TRANSMITTED DATA SPECTRUM

When the compromise equalizer is disabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

V.22 bis: Square root of 75%.
V.29: Square root of 20%.
V.27 ter 1600 baud: Square root of 50%.
V.27 ter 1200 baud: Square root of 90%.

SCRAMBLER/DESCRAMBLER

A self-synchronizing scrambler/descrambler satisfying the applicable CCITT recommendation or Bell interface is incorporated depending on the selected configuration. Both the scrambler and the descrambler can be enabled or disabled (SDIS or DDIS bits, respectively).

TRANSMIT LEVEL

The transmitter output level is programmable with a default value of –10 dBm ±1 dBm (measured at the TXA output pin). Transmit output level is selectable in 2 dBm steps from 0 dBm to –14 dBm (TLVL). The default amplitudes for DTMF tones in the auto dial mode are –4 dBm and –6 dBm for the high and low frequencies, respectively.

TRANSMIT TIMING

Transmitter timing in full-duplex modes is selectable between internal (±0.01%), external, or loopback (TXCLK). An external clock must equal the desired data rate ±0.01% with a duty cycle of 50 ± 20%.

RECEIVE LEVEL

The receiver satisfies performance requirements for the received line signals from –10 dBm to –43 dBm. The received line signal is measured at the Receive Analog (RXA) input.

RECEIVE TIMING

A frequency error up to ±0.01% in the associated transmitting source can be tracked.

CARRIER RECOVERY

A frequency offset up to ±7 Hz in the received carrier can be tracked with less than a 0.2 dB degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) when the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off.

RECEIVER CARRIER FREQUENCY

The receiver demodulator carrier frequency is shown in Table 1. In V.29FT modes, 1800 Hz or 1700 Hz may be selected (RCF and TCF bits).

TURN-ON/ TURN-OFF SEQUENCES

V.29 and V.27 Turn-On Sequence

The selectable turn-on sequences are generated as defined in the Table 4.

V.29 and V.27 Turn-Off Sequence

In V.29/FT, V.29, V.27/FT, and V.27 the turn-off sequence consists of approximately 8 ms of remaining data and scrambled ones.

V.22 and Bell 212A Turn-On/Turn-Off Sequences

RTS and CTS turn-on and turn-off sequences and times for V.22 and Bell configurations are shown in Tables 5 and 6, respectively. Controlled or constant carrier operation can be selected (CC bit).

ASYNC/SYNC, SYNC/ASYNC CONVERSION

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The asynchronous character format is 1 start bit, 5 to 8 data bits (CHAR0 and CHAR1), an optional parity bit (PARSL0 , PARSL1, PEN0, and PEN1), and 1 or 2 stop bits (STB0 and STB1). Valid character size, including all bits is 8, 9, 10, or 11 bits.

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. Break is handled in the transmitter and receiver as described in V.22 bis.

MODES OF OPERATION

The R96QT can operate synchronously or asynchronously, depending on the selected configuration.

CONTROL MODES (FDX)

The modem can operate in serial or parallel control modes (BUS bit) and in either serial or parallel data mode (RPDM and TPDM bits).

In the serial control mode, standard V.24 (RS-232 comatible) interface signals, along with the $\overline{TLK}$ and $\overline{ORG}$ signals, control the transfer of data between the modem and the host (V.22 bis only). The transmitter defaults to serial control mode upon power turn-on.

In the parallel control mode, bits in interface memory corresponding to the V.24 signals control the data transfer.

In either serial and parallel control mode, the modem is configured by the host writing configuration/control bits to the DSP interface memory via the microprocessor bus.

DATA MODES

Serial or parallel data mode can be separately selected for the transmitter and receiver (TPDM and RPDM bits, respectively). In parallel data mode, channel data is transferred 8-bits at a time between the host and the modem over the microprocessor bus.

Table 4. High Speed RTS-CTS Response Times

Configuration	$\overline{RTS}/\overline{CTS}$ Response Time (ms)
V.29 FT/9600	23
V.29 FT/7200	24
V.29 FT/4800	23
V.29 9600, 7200, or 4800	253
V.27 FT/4800	22
V.27 4800 long	708
V.27 FT/2400	30
V.27 2400 long	943

Note: V.29 $\overline{RTS}$-$\overline{CTS}$ response time is 438 ms when preceded by an echo protector.

Table 5. Medium Speed RTS Responses

RTS Transition*	Constant Carrier	Controlled Carrier
ON to OFF	CTS OFF, carrier ON, scrambled 1s transmitted	CTS OFF, carrier OFF
OFF to ON	CTS ON, carrier ON, data transmitted	carrier ON, 210 ms to 275 ms scrambled 1s transmitted, data transmitted

* After handshake is complete.

Table 6. Medium Speed CTS Response Times

CTS Transition	Constant Carrier	Controlled Carrier
OFF to ON	<2 ms	210 to 275 ms
ON to OFF	<20 ms	20 ms*

* Programmable

In the receiver serial data mode, received data is output only to the RXD pin. In the receiver parallel data mode, received data is output simultaneously to the Receive Data Register (RXDATA) in interface memory and to the RXD pin.

In the transmitter serial data mode, transmitted data is obtained from the TXD input pin. In the transmitter parallel data mode, transmitted data is obtained from the Transmit Data Register (TXDATA) in interface memory.

In parallel asynchronous data mode, the R96QT operates like a universal asynchronous receiver/transmitter (UART) except in BELL103 configuration. The length of the break signal is determined by the BRKS0 and BRKS1 bits for the transmitter and receiver, respectively.

HARDWARE INTERFACE SIGNALS

The Functional Interconnect Diagram (Figure 1) shows the typical modem connection in a system. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{IRQ}$). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The functional interconnect signals shown in Figure 1 are organized into seven functional groups: overhead, microprocessor interface, V.24 interface, analog, line interface, ancillary and diagnostic. These signals, along with their connector pin numbers and interface circuit types, are listed in Table 7. The digital and analog interface characteristics are defined in Tables 8 and 9, respectively.

POWER-ON-RESET

When power is applied to the modem, the modem pulses Power-On-Reset ($\overline{POR}$) low to begin the POR sequence. The modem is ready for use 350 ms after the low-to-high transition of $\overline{POR}$. The POR sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 µs. $\overline{POR}$ is not pulsed low by the modem when the POR sequence is initiated externally. The POR sequence initializes the modem interface memory (Table 12) to default values. This action leaves the modem configured as follows:

- V.22 bis synchronous 2400 bps
- Serial data mode
- T/2 equalizer
- –43 dBm receiver threshold
- Constant carrier
- Answer mode
- –10 dBm transmit level

NOTE: If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a POR sequence (i.e., <+3.5V), the host system should generate a $\overline{POR}$ signal upon supply voltage recovery to ensure proper modem initialization and operation.

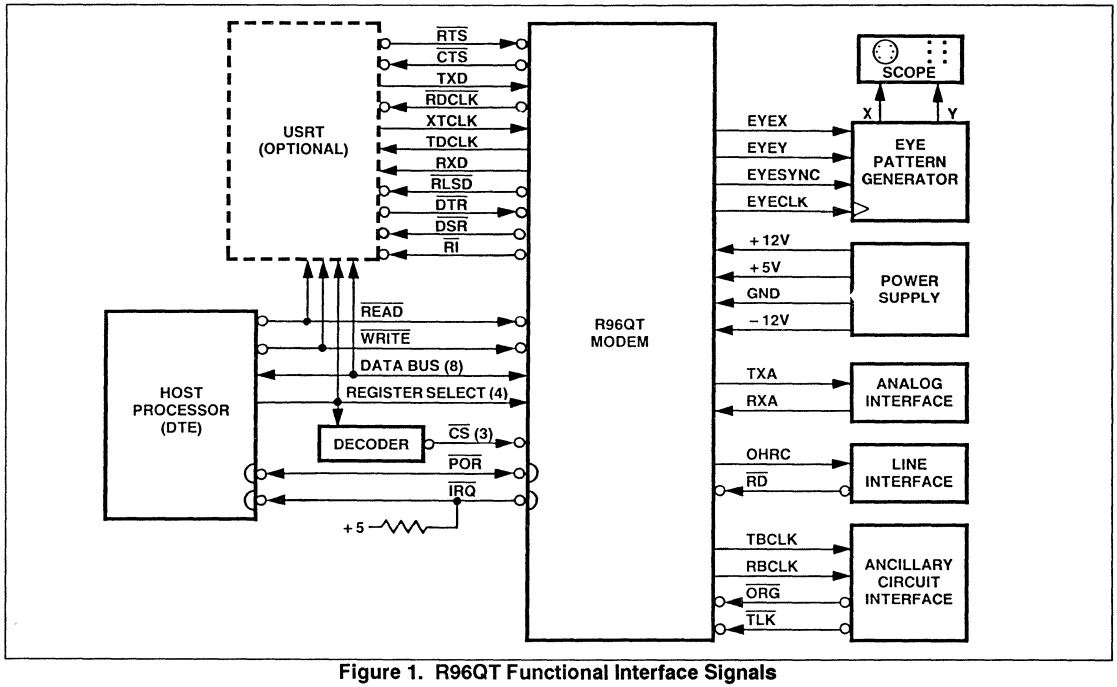


Figure 1. R96QT Functional Interface Signals

Table 7. R96QT Hardware Interface Signals

Name	I/O Type	DIP Pin No.	Description
OVERHEAD			
GND(A)	AGND	27,28	Analog Ground Return
GND(D)	DGND	32,36, 51	Digital Ground Return
+5V	PWR	9, 14, 55	+5 Volt Supply
+12V	PWR	29	+12 Volt Supply
– 12V	PWR	31	– 12 Volt supply
$\overline{POR}$	IB/OB	4	Power-On-Reset
PROCESSOR			
D7	IA/OA	50	Data Bus Bit 7
D6	IA/OA	49	Data Bus Bit 6
D5	IA/OA	48	Data Bus Bit 5
D4	IA/OA	47	Data Bus Bit 4
D3	IA/OA	46	Data Bus Bit 3
D2	IA/OA	45	Data Bus Bit 2
D1	IA/OA	44	Data Bus Bit 1
D0	IA/OA	43	Data Bus Bit 0
RS3	IA	3	Register Select 3
RS2	IA	58	Register Select 2
RS1	IA	57	Register Select 1
RS0	IA	40	Register Select 0
$\overline{CS0}$	IA	2	Chip Select Transmitter
$\overline{CS1}$	IA	42	Chip Select Receiver 1
$\overline{CS2}$	IA	60	Chip Select Receiver 2
$\overline{READ}$	IA	61	Read Enable
$\overline{WRITE}$	IA	59	Write Enable
$\overline{IRQ}$	OB	1	Interrupt Request

Table 7. R96QT Hardware Interface Signals (Cont'd)

Name	I/O Type	DIP Pin No.	Description
V.24			
XTCLK	IB	5	External Transmit Clock
$\overline{TDCLK}$	OC	6	Transmit Data Clock
$\overline{RDCLK}$	OC	38	Receive Data Clock
$\overline{RTS}$	IB	10	Request-To-Send
$\overline{CTS}$	OC	8	Clear-To-Send
TXD	IB	11	Transmit Data
$\overline{RXD}$	OC	35	Receive Data
$\overline{RLSD}$	OC	37	Receiver Line Signal Detector
$\overline{DTR}$	IB	16	Data Terminal Ready
$\overline{DSR}$	OC	13	Data Set Ready
$\overline{RI}$	OC	23	Ring Indicator
ANALOG			
TXA	AA	26	Transmit Analog Output
RXA	AB	30	Receiver Analog Input
LINE			
$\overline{RD}$	IB	22	Ring Detect
OHRC	OC	18	Off-Hook Relay Control
ANCILLARY			
TBCLK	OC	7	Transmit Baud Clock
RBCLK	OC	12	Receive Baud Clock
$\overline{ORG}$	IB	17	Originate
$\overline{TLK}$	IC	19	Talk
DIAGNOSTIC			
EYEX	OC	52	Eye Pattern Data X-Axis
EYEY	OC	56	Eye Pattern Data Y-Axis
EYECLK	OA	54	Eye Pattern Clock
EYESYNC	OA	53	Eye Pattern Synchronizing Signal

NOTES:
1. Digital and analog I/O types are described in Tables 8 and 9.
2. DIP connector pins 24, 25, 33, 34, 39 and 41 are not used. Leave these pins disconnected (i. e., open).
3. Unused inputs tied to +5V or ground require individual 10 KΩ series resistors.

Table 8. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC[4]	OA	OB	OC	OD[5]
V_{IH}	Input High Voltage	V	2.0 min.	2.0 min.	V_{CC} –0.5 max.				
V_{IL}	Input Low Voltage	V	0.8 max.	0.8 max.	0.5 max.				
I_{IN}	Input Leakage Current	µA	2.5 max.		11 max.				
V_{OH}	Output High Voltage	V				3.5 min.[1]	3.5 min.[1]		
V_{OL}	Output Low Voltage	V				0.4 max.[2]	0.4 max.[3]	0.4 max.[2]	
I_{OH}	Output High Current	mA				– 0.1 max.	– 0.1 max.		– 0.001 max.
I_{OL}	Output Low Current	mA				1.6 max.	0.8 max	1.6 max.	0.001 max.
I_L	Output Leakage Current	µA				±10 max.	±10 max.		
I_{PU}	Pull-Up Current			– 240 max.		– 240 max.			
	(Short Circuit)	µA		– 10 min.		– 10 min.			
C_L	Capacitive Load	pF	5	20	10				
C_D	Capacitive Drive	pF				100	100	100	50
	Circuit Type		TTL	TTL w/pull-up	CLK	TTL 3-state	TTL 3-state	TTL 3-state	CLK

NOTES:
1. I Load = –100 µA
2. I Load = 1.6 mA
3. I Load = 0.8 mA
4. Input waveform must be symmetric within 20%.
5. Loads on 12 MHz and 6 MHz outputs must be balanced within 20%.

Table 9. Analog Signal Characteristics

Name	Type	Characteristic
TXA	AA	The transmitter output impedance is 604 Ω ±1% with an output level of 0.488 V_{RMS}. To obtain a – 10 dBm output, an external 600 Ω load to ground is needed.
RXA	AB	The receiver input impedance is 21K Ω ±1%. The receive level at RXA must be no greater than –10 dBm.

MICROPROCESSOR INTERFACE

Eighteen address, data, control and interrupt hardware interface signals implement an 8085 compatible parallel microprocessor interface to a host processor.

This parallel interface allows a host processor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The significance of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

Data Lines (D0–D7)

Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$) signals.

Chip Select ($\overline{CS0}$–$\overline{CS2}$) and Register Selects (RS0–RS3)

Three active low chip select lines ($\overline{CS0}$-$\overline{CS2}$) select one of three modem digital signal processor (DSP) devices. The four active high register select lines (RS0-RS3) address interface memory registers within the selected DSP interface memory. All seven of these lines are typically connected to the host bus address lines; the register select lines to the four least significant lines (A0-A3) and the chip select lines to the next two significant lines (A4-A5) through a decoder.

The selected DSP decodes RS0 through RS3 to address one of 16 internal interface memory registers (0-F). The most significant address bit is RS3 while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0 - D7).

Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

During a read cycle, data from the selected DSP interface memory register is gated onto the data bus by means of three-state drivers in each DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

The read/write timing waveforms are illustrated in Figure 2 and the timing requirements are specified in Table 10.

Interrupt Request ($\overline{IRQ}$)

The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in the DSP interface memory to indicate immediate change of conditions in any of the three modem DSP devices. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.

The DSP $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). Each of the individual DSP $\overline{IRQ}$ output lines is wire-ORed to form the composite modem $\overline{IRQ}$ output signal. The modem $\overline{IRQ}$ output can also be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low. The host in-

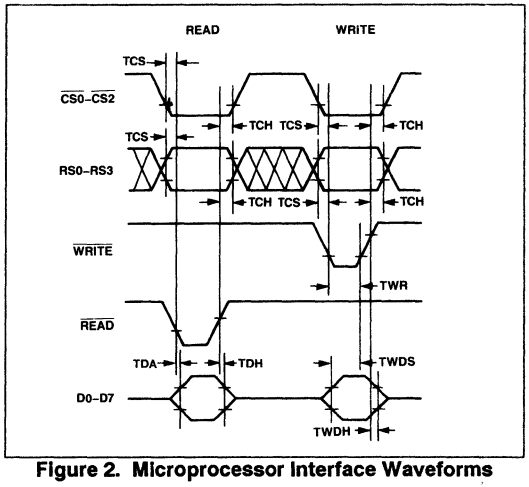


Figure 2. Microprocessor Interface Waveforms

Table 10. Microprocessor Interface Timing

Parameter	Symbol	Min.	Max.	Units
$\overline{CSi}$, RSi setup time	TCS	30	–	ns
Data access time	TDA	–	140	ns
Data hold time	TDH	10	50	ns
$\overline{CSi}$, RSi hold time	TCH	10	–	ns
Write data setup time	TWDS	75	–	ns
Write data hold time	TDHW	10	–	ns
Write strobe pulse width	TWR	75	–	ns

terrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25W, is sufficient.

V.24 INTERFACE

Eleven hardware circuits provide timing, data and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

Most V.24 hardware interface signals have a corresponding bit in DSP interface memory. In general, the hardware interface signals are complemented with respect to their corresponding interface memory bits, e.g., $\overline{RTS}$ signal low = RTS bit set to a 1.

For full-duplex operation, the hardware control input signals ($\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, and $\overline{ORG}$) are valid when the modem is in the serial control mode (BUS = 0). Their state is ignored when the modem is in the parallel control mode (BUS = 1).

For half-duplex operation, the modem logically ORs the $\overline{RTS}$ input signal with the RTS interface memory bit to form the resultant control signal regardless of the state of the BUS bit.

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the host on the Transmitted Data (TXD) input (transmitter serial data mode) or from the Transmit Data Register (TXDATA) register in interface memory (transmitter parallel data mode).

Received Data (RXD)

The modem presents received serial data to the host on the Received Data (RXD) outputs in both receiver serial and parallel data modes) and to the Receive Data Register (RXDATA) register in interface memory in receiver parallel data mode.

Request To Send ($\overline{RTS}$)

Request to Send ($\overline{RTS}$) input low causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active. In constant carrier mode, $\overline{RTS}$ can be wired to $\overline{DTR}$. In controlled carrier operation, independent operation of $\overline{RTS}$ turns the carrier ON and OFF. The responses to $\overline{RTS}$ are shown in Table 5 (when the modem is in data mode).

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) active indicates to the host that the modem will transmit any data present on TXD. $\overline{CTS}$ response times from $\overline{RTS}$ active are shown in Table 6.

Data Terminal Ready ($\overline{DTR}$) (FDX only)

Data Terminal Ready ($\overline{DTR}$) active initiates the handshake sequence when DATA = 1. In answer mode, the transmitter will immediately send answer tone. In data mode, deactivating $\overline{DTR}$ causes the transmitter to turn-off and return to the idle state.

Data Set Ready ($\overline{DSR}$) (FDX only)

Data Set Ready ($\overline{DSR}$) output low indicates that the modem is in the data transfer state. $\overline{DSR}$ OFF is an indication that the DTE is to disregard all signals appearing on the interchange circuits–except $\overline{RI}$. $\overline{DSR}$ will switch to the OFF state when in test state. The ON condition of $\overline{DSR}$ indicates the following conditions:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.
4. After Ring Indicator ($\overline{RI}$) goes ON, $\overline{DSR}$ waits at least two seconds before turning ON to allow the telephone company equipment to be engaged.

$\overline{DSR}$ will go OFF 50 ms after $\overline{DTR}$ goes OFF, or 50 ms plus a maximum of 4 seconds when the SSD bit is enabled.

Received Line Signal Detector ($\overline{RLSD}$)

$\overline{RLSD}$ Response

For Fast Train configurations, the receiver enters the training state upon detecting a significant increase in the received signal power. If the received line signal power is greater than the selected threshold level at the end of the training state, the receiver enters the data state and $\overline{RLSD}$ is activated. If the received line signal power is less than the threshold level at the end of the training state, the receiver returns to the idle state and $\overline{RLSD}$ is not activated.

Also, in Fast Train configurations, the receiver initiates the turn-off delay upon detecting a significant decrease in the received signal power. If the received signal power is less than the selected threshold at the end of the turn-off delay, the receiver enters the idle state and $\overline{RLSD}$ is deactivated. If the received signal power is greater than the selected threshold at the end of the turn-off delay, the receiver returns to the data state and $\overline{RLSD}$ is left active.

The $\overline{\text{RLSD}}$ on-to-off response times are:

Configuration	Response Time
V.29 FT	6.5 ± 1 ms
V.29	30 ± 9 ms
V.27 FT	8 ± 1 ms
V.27 ter	10 ± 5 ms

$\overline{\text{RLSD}}$ response times are measured with a signal at least 3 dB above the actual $\overline{\text{RLSD}}$ on threshold or at least 5 dB below the actual $\overline{\text{RLSD}}$ off threshold.

$\overline{\text{RLSD}}$ Threshold

The $\overline{\text{RLSD}}$ thresholds are fixed in FDX and selectable in HDX (see RTH bits):

Mode	$\overline{\text{RLSD}}$ ON	$\overline{\text{RLSD}}$ OFF
FDX	≥ –43 dBm	≤ –48 dBm
HDX1	≥ –43 dBm	≤ –48 dBm
HDX2	≥ –33 dBm	≤ –38 dBm
HDX3	≥ –26 dBm	≤ –31 dBm

$\overline{\text{RLSD}}$ will not respond to a guard tone or an answer tone.

For CCITT configurations, a minimum hysteresis action of 2 dB exists between the actual on-to-off transition levels. In half-duplex modes, the threshold level and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input . In full-duplex modes, regular data is used.

Ring Indicator ($\overline{\text{RI}}$) (FDX only)

The modem provides a Ring Indicator ($\overline{\text{RI}}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the ON segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The high condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received. The operation of $\overline{\text{RI}}$ is not disabled by an OFF condition on $\overline{\text{DTR}}$.

$\overline{\text{RI}}$ will respond to ring signals applied on $\overline{\text{RD}}$ in the frequency range of 15.3 Hz to 68 Hz.

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

Frequency. Data rate ±0.01%.

Duty Cycle. 50 ±1%.

TDCLK is provided to the user in synchronous communications. Transmit Data (TXD) must be stable during the one µs period immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication, where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{\text{RDCLK}}$)

The modem provides a Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% (relative) frequency error in the associated transmit timing source.

$\overline{\text{RDCLK}}$ is provided in both asynchronous and synchronous communications. $\overline{\text{RDCLK}}$ is not necessary in asynchronous communications but it can be used to supply a clock for UART/USART timing. $\overline{\text{RDCLK}}$ is necessary for synchronous communication.

ANALOG INTERFACE

Transient protection for TXA and RXA is recommended when interfacing directly to a transformer. This protection may take the form of back-to-back zener diodes or a varistor across the transformer. The characteristics of signals TXA and RXA are summarized in Table 9.

Transmit Analog (TXA)

The Transmit Analog (TXA) output can drive an audio transformer or data access arrangement. TXA is a low impedance amplifier output in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

Receive Analog (RXA)

The Receive Analog (RXA) input can originate from an audio transformer or data access arrangement. The input impedance is nominally 21K ohms. The RXA input must be shunted by an external 604 ohm ±1% resistor in order to match a 600 ohm source.

LINE INTERFACE

Ring Detect ($\overline{\text{RD}}$) (FDX only)

$\overline{\text{RD}}$ indicates to the modem by an ON (low) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the $\overline{\text{RD}}$ input should not respond to momentary bursts of ringing less than 125 ms in duration. The ring, if within 15 Hz to 68 Hz, is reflected on $\overline{\text{RI}}$ (if this method of ring detection has been selected, and ringing detection is active.)

Off-Hook Relay Control (OHRC) (FDX only)

The OHRC output can be used as the input to an external relay driver to drive the Off-Hook (OH) relay when control bit RA is set high. OHRC high indicates the OH relay is to be closed and the modem is to be connected to the telephone line (off-hook). OHRC low indicates the OH relay is to be opened (on-hook).

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK) outputs have no counterpart in the V.24 or RS-232-C recommendations since they mark the baud interval rather than the data rate for the transmitter and receiver, respectively. These baud clocks are useful in identifying the order of data bits in a baud (e.g., for multiplexing data). Both signals are active high. The high-to-low transition of each baud clock coincides with a high-to-low transition of the respective data clock. These clocks are held permanently high when the modem is configured for V.21 channel 2 operation.

Talk ($\overline{TLK}$) (FDX only)

$\overline{TLK}$ input low manually places the modem in idle mode. $\overline{TLK}$ high manually initiates the handshake sequence and places the modem in data mode.

Originate ($\overline{ORG}$) (FDX only)

$\overline{ORG}$ input manually places the modem in the originate mode ($\overline{ORG}$ low) or the answer mode ($\overline{ORG}$ high). To manually originate a call set $\overline{ORG}$ low and $\overline{TLK}$ high. To manually answer a call, set $\overline{ORG}$ high and $\overline{TLK}$ high.

DIAGNOSTIC SIGNALS

Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line distrubances can usually be identified. Timing of these signals is illustrated in Figure 3.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

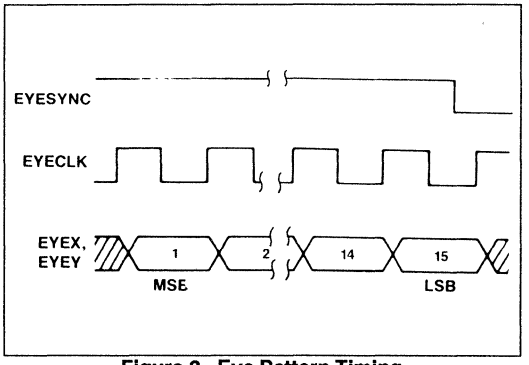


Figure 3. Eye Pattern Timing

EYEX and EYEY outputs are 15-bit words, each with 8-bits of significance. The 15-bit data words are shifted out most significant bit first with the seven most significant bits equal to zero. EYEX and EYEY are clocked by the rising edge of EYECLK.

EYECLK

EYECLK is a clock for use by the serial-to-parallel converters. The EYECLK output is a 288 kHz clock which is internally divided to create the Receiver Baud Clock (RBCLK). EYECLK is also a common multiple of all the possible receiver data clocks. The low-to-high transitions of $\overline{RDCLK}$ coincide with the low-to-high transitions of EYECLK. EYECLK, therefore, can be used as a receiver multiplexer clock.

EYESYNC

EYESYNC is a strobe for loading the D/A converters.

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in three DSP devices: a transmitter device, a receiver sample rate device, and a receiver baud rate device.

INTERFACE MEMORY

Each DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in each DSP contains sixteen 8-bit registers, labeled register 0 through F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus shared between the three DSPs.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAPS

Memory maps of the 16 addressable registers in the modem transmitter (chip 0), receiver sample rate (chip 1), and receiver baud rate (chip 2) devices are shown in Figure 4. These 8-bit registers may be read or written to during any host read or write cycle. In order to operate on a single bit or group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, the host must read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory register.

INTERFACE MEMORY BIT DEFINITIONS

Table 12 defines the individual bits in the interface memory. In the Table 12 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0, 1 or 2), the register number by Z (0 through F), and the bit number by Q (0 through 7, 0 = LSB).

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register	Bit 7	6	5	4	3	2	1	0
F	WRT0	RAM ACCESS CODE CHIP 0 (ACC0)						
E	TIA	NSIE0	NEWS0	—	NEWC0	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	TLVL			—	—	—	—	
A	—	—	—	—	—	—	CTS	DSR
9	NV25	ASCR	RTRN	—	TCF	CDEQ	DATA	DTMF
8	BUS	—	ORG	GTE	—	—	SSD	RA
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	TXCLK	
6	TRANSMITTER CONFIGURATION (TCONF)							
5	CHAR0		PEN0	PARSL0	STB0	BRKS0	DIABT	CAEQ
4	AL0	RDLE0	ST0	CC	ASYNC0	RDL0	DL0	DTR
3	X RAM DATA MSB (XDAM0)							
2	X RAM DATA LSB (XDAL0)							
1	FREQM/Y RAM DATA MSB (YDAM0)							
0	DDR/TXDATA/FREQL/Y RAM DATA LSB (YDAL0)							

Note: (—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register	Bit 7	6	5	4	3	2	1	0
F	WRT1	RAM ACCESS CODE CHIP 1 (ACC1)						
E	RIA1	NSIE1	NEWS1	—	NEWC1	RIE1	—	RBA1
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	PE	$\overline{CDET}$	TONE	—
8	—	—	—	—	$\overline{P2DET}$	—	FE	—
7	RTH		DDIS	—	—	RCF	RDIS	—
6	RECEIVER CONFIGURATION (RCONF)							
5	CHAR1		PEN1	PARSL1	STB1	RPDM	BRKS1	—
4	—	—	—	—	ASYNC1	CEQSEL		
3	X RAM DATA MSB (XDAM1)							
2	X RAM DATA LSB (XDAL1)							
1	Y RAM DATA MSB (YDAM1)							
0	RXDATA/ Y RAM DATA LSB (YDAL1)							

Note: (—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register	Bit 7	6	5	4	3	2	1	0
F	WRT2	RAM ACCESS CODE CHIP 2 (ACC2)						
E	RIA2	NSIE2	NEWS2	—	NEWC2	RIE2	—	RBA2
D	—	—	—	—	—	—	—	—
C	FR3	FR2	FR1	—	—	—	—	$\overline{PNDET}$
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	FRZEQ
6	—	—	—	—	—	—	—	—
5	—	—	TONEA	TM	RI	SPEED		
4	AL2	RDLE2	ST2	RSD	LCD	RDL2	DL2	CL
3	X RAM DATA MSB (XDAM2)							
2	X RAM DATA LSB (XDAL2)							
1	Y RAM DATA MSB (YDAM2)							
0	Y RAM DATA LSB (YDAL2)							

Note: (—) Indicates reserved for modem use only.

Figure 4. R96QT DSP Interface Memory Map

Table 12. R96QT Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
ACC0	0:F:0-7	0	**RAM Access Code Chip 0.** Register ACC0 contains the RAM access code used in reading RAM locations in the transmitter device.
ACC1	1:F:0-7	0	**RAM Access Code Chip 1.** Register ACC1 contains the RAM access code used in reading RAM locations in the receiver sample device.
ACC2	2:F:0-7	0	**RAM Access Code Chip 2.** Register ACC2 contains the RAM access code used in reading RAM locations in the receiver baud device.
AL0	0:4:7	0	**Local Analog Loopback Chip 0.**
AL2	2:4:7	0	**Local Analog Loopback Chip 2.** When both AL0 and AL2 are 1, the modem will go through an analog loopback according to recommendation V.54 loop 3. The modem may be placed in analog loopback in either idle or data mode. However, when AL0 or AL2 is a 1 in data mode, the connection is terminated. AL2 must be set first, followed by AL0. (V.22, V.22 bis, V.22 A/B, and Bell 212A) (FDX)
ASCR	0:9:6	0	**Append Scrambled Ones.** When ASCR is a 1, one baud of scrambled mark is included in the V.29 FT and V.27 FT training sequence. The RTS-CTS delay is thus extended by 1 baud period when ASCR is a 1. (HDX)
ASYNC0	0:4:3	0	**Asynchronous Mode Chip 0.** When ASYNC0 is a 1, asynchronous data mode is selected in the transmitter. When ASYNC0 is a 0, synchronous data mode is selected. (FDX)
ASYNC1	1:4:3	0	**Asynchronous Mode Chip 1.** When ASYNC1 is a 1, asynchronous data mode is selected in the receiver. When ASYNC1 is a 0, synchronous data mode is selected. (FDX)
BRKS0	0:5:1	0	**Break Sequence Chip 0.** When control bit BRKS0 is a 1, the modem will send continuous space. When BRKS0 is a 0, the modem will transmit data from TXDATA (TPDM = 1). (FDX) (Asynchronous operation only)
BRKS1	1:5:1	–	**Break Sequence Chip 1.** When status bit BRKS1 is a 1, the modem is receiving continuous space. When BRKS1 is a 0, the modem is receiving data and outputting the data to RXDATA (RPTM = 1). (FDX) (Asynchronous operation only)
BUS	0:8:7	0	**Bus Select.** When control bit BUS is a 1, the modem is in the parallel control mode; when BUS is a 0, the modem is in the serial control mode. BUS can be in either state to configure the modem. In either mode, the modem is configured by the host writing to interface memory via the microprocessor bus. Note that the modem automatically defaults to the serial mode at power-on. (FDX) ***Serial Control Mode*** In serial control mode, standard V.24 (RS-232-C compatible) signals are used to control the transfer of channel data. The control signals used are DTR, RTS, TLK, and ORG. Outputs such as RLSD and DSR are reflected both in the interface memory and the V.24 interface. Once the BUS bit has been set to a 0, the state of the DTR, RTS, DATA, and ORG bits are ignored. ***Parallel Control Mode*** In the parallel control mode, the modem is controlled by bits written to interface memory via the microprocessor bus. Data transfer is also over the microprocessor bus. The control bits are DTR, RTS, ORG, and DATA. If the parallel control mode is to be used, it is recommended that the TLK pin be tied to ground. A floating TLK pin will assume a logic 1 which will immediately put the modem into the data mode before the BUS bit is set.
CAEQ	0:5:0	0	**Cable Amplitude Equalizer.** When CAEQ = 1, an amplitude compromise equalizer is allocated in the transmitter path. The NEWC0 bit must be set after setting the CAEQ bit. (V.29 and V.29 FT modes only)

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
CC	0:4:4	0	**Controlled Carrier.** When control bit CC is a 1, the modem operates in controlled carrier; when CC is a 0, the modem operates in constant carrier. Controlled carrier allows the modem transmitter to be controlled by the $\overline{RTS}$ pin or the RTS bit. Its effect may be seen in the descriptions of the RTS and CTS bits. (FDX)
CDEQ	0:9:2	0	**Compromise Delay Equalizer Enable.** When control bit CDEQ is a 1, an Infinite Impulse Response (IIR) delay equalizer is placed in the transmitter path. (HDX)
$\overline{CDET}$	1:9:2	0	**Carrier Detector.** Status bit $\overline{CDET}$ is set to a 0 when passband energy is being detected and a training sequence is not in process.
CEQSEL	1:4:0,1,2	0	**Compromise Equalizer Select.** CEQSEL selects the type of equalizer to be placed in the receiver path. (HDX) **Curve Matched** — **2 1 0** No Equalization — 0 0 0 US - Long — 0 0 1 Japanese 3-Link — 0 1 0 Cable 1 — 0 1 1 Cable 2 — 1 0 0 Cable 3 — 1 0 1
CHAR0	0:5:6,7	2	**Character Length Select Chip 0.** CHAR0 selects either 8, 9, 10, or 11 bit characters (includes data, stop, and start bits) for the transmitter in asynchronous data mode (ASYNC0 = 1). The bit representations are: **Bits Per Character** — **7 6** 8 bits — 0 0 9 bits — 0 1 10 bits — 1 0 11 bits — 1 1
CHAR1	1:5:6,7	2	**Character Length Select Chip 1.** CHAR1 selects 8,9,10 or 11 bit character length (includes data, stop, and start bits) for the receiver in asynchronous data mode (ASYNC1 = 1). The bit representations are: **Bits Per Character** — **7 6** 8 bits — 0 0 9 bits — 0 1 10 bits — 1 0 11 bits — 1 1 It is possible to change character length during the data mode. Errors in the data will be expected between change over and the resynchronization (which occurs on the next start bit after the change is implemented).
CL	2:4:0	0	**Control Line.** When CL is set to a 1, the receiver goes to data mode upon detection of 270 ms of energy after a loss of carrier. A retrain may be required once the modem is back in data mode (see RTRN bit). Before CL is set to a 1, an initial handshake must be completed. (FDX)
CTS	0:A:1	0	**Clear-to-Send.** When status bit CTS is a 1, the modem will transmit any data present at TXD. (FDX)
DATA	0:9:1	0	**Data Mode.** When control bit DATA is a 0, the modem is in the idle mode and data is not being transmitted. The modem is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering. When control bit DATA is a 1, the modem is in the data mode. This bit allows the modem to enter the data mode after the host counts a programmable number of rings by counting the required number of RI bit transitions. (FDX)

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
DDR	0:0-7		**Dial Digit Register.** DDR is used to load the digits to be dialed when in transmitter Call Request mode (TCONF = 80). Example: If a 4 is to be dialed, a 04 (hex) should be loaded. This action also causes the interrupt to be cleared. The modem automatically accounts for the interdigit delay. Note: DDR is a write-only register. (FDX)
DDIS	1:7:5	0	**Descrambler Disable.** When control bit DDIS is a 1, the receiver descrambler is disabled; when DDIS is a 0, the descrambler is enabled. (HDX)
DIABT	0:5:1	0	**Disable Abort Timer.** When DIABT is set to a 1, the 30 second abort timer in the modem initializing a handshake is disabled. When DIABT is set to a 0, setting the DATA bit will initialize the modem for a handshake (originating modem looks for tone or answering modem sends tone and unscrambled 1s) for 30 seconds before it aborts the handshake. (FDX only)
DL0	0:4:1	0	**Digital Loop Chip 0.**
DL2	2:4:1	0	**Digital Loop Chip 2.** When DL0 and DL2 are both a 1, the modem is manually placed in digital loopback. DL0 and DL2 should be set only during the data mode. The DSR and CTS bits will be reset to 0. The local modem can then be tested from the remote modem end by looping a remotely generated test pattern. At the remote modem, all interface circuits behave normally (as in the data mode). At the conclusion of the test, DL0 and DL2 must be reset to 0. The local modem will then return to the normal data mode with control reverting to the $\overline{\text{DTR}}$ input. (DL2 must be set first followed by DL0.) (V.22, V.22 bis, V.22 A/B, and Bell 212A). (FDX)
DSR	0:A:0	0	**Data Set Ready.** The ON condition of the status bit DSR indicates that the modem is in the data transfer state. The OFF condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits - except RI. DSR will switch to the OFF state when in test state. The ON condition of DSR indicates the following: The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing. The modem has generated or detected answer tone. After ring indicate goes ON, DSR waits at least two seconds before turning ON to allow the telephone company equipment to be engaged. DSR will go OFF 50 ms after DTR goes OFF, or 50 ms plus a maximum of 4 seconds when the SSD bit is enabled. (FDX)
DTMF	0:9:0	0	**Touch Tone/Pulse Dialing.** When transmitter Call Request configuration is selected (TCONF = 80) and control bit DTMF is a 1, the modem will auto dial using tones. When DTMF is a 0, the modem will dial using pulses. The timing for the pulses and tones are as follows (power-on timing): Pulses – Relay open 64 ms Relay closed 36 ms Interdigit delay 750 ms Tones – Tone duration 95 ms Interdigit delay 71 ms The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. The tone pairs and corresponding dial digits are shown in Table 3. The output power level of the DTMF tones is: – 1 dBm ± 1 measured at TXA

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
DTR	0:4:0	0	**Data Terminal Ready.** When set to a 1, control bit DTR initiates the handshake sequence if DATA = 1. In answer mode, the transmitter will immediately send answer tone. In the data mode, setting the DTR bit to a 0 causes the transmitter to turn off and return to the idle state. (FDX)
EPT	0:7:3	0	**Echo Protector Tone.** When EPT is a 1, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the start of the transmission. (HDX)
FE	1:8:1	0	**Framing Error.** When set to a 1, status bit FE indicates that more than 1 in 8 (or 1 in 4) characters were received without a stop bit in asynchronous mode. When FE is reset to a 0, no framing error is detected. (FDX)
$\overline{\text{FED}}$	1:9:6	0	**Fast Energy Detect.** When $\overline{\text{FED}}$ is a 0, energy above the threshold is present in the passband. (HDX)
FREQL	0:1:0-7	0	**Frequency Number Least Significant Byte.**
FREQM	0:0:0-7	0	**Frequency Number Most Significant Byte.** The host conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers as shown below (HDX): FREQM Register (0:0) Bit: 7 6 5 4 3 2 1 0 Data Word: 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0 FREQL Register (0:1) Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8 The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Frequency number (FREQM and FREQL) codes in hexadecimal for generally used tones are: **Frequency (Hz) / FREQM (Hex) / FREQL (Hex)** 462 / 0C / 52 1100 / 1D / 55 1650 / 2C / 00 1850 / 31 / 55 2100 / 38 / 00
FRZEQ	2:7:0	0	**Freeze Equalizer Taps.** When control bit FRZEQ is set to a 1, updating of the equalizer tap values is inhibited. (FDX only)

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
FR1	2:C:5	0	**Frequency 1.**
FR2	2:C:6	0	**Frequency 2.**
FR3	2:C:7	0	**Frequency 3.** The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for V.21 Channel 2. The default frequencies for FR1, FR2 and FR3 are: Bit — Frequency (Hz) FR1 — 2100 FR2 — 1100 FR3 — 462
GTE	0:8:4	0	**Guard Tone Enable.** When control bit GTE is a 1, an 1800 guard tone will be transmitted (CCITT FDX configuration only). **Note:** The guard tone will only be transmitted by the answering modem.
LCD	2:4:3	1	**Loss of Carrier Disconnect.** When control bit LCD is a 1, the modem terminates a call when a loss of received carrier energy is detected after 400 ms. After 40 ms of loss of carrier, $\overline{RLSD}$ goes off. If carrier is not detected within the next 360 ms, $\overline{CTS}$ goes off, and the modem goes to idle mode. If energy above threshold is detected during the 360 ms period, $\overline{RLSD}$ will go on again. If further loss of energy occurs, the 400 ms time frame is restarted. If LCD is set to a 0, $\overline{RLSD}$ will be a 0 when energy is above threshold, but will not force the modem into idle mode when energy falls below threshold. In this case, it is necessary to re-enable LCD in order to put the modem in idle mode. (FDX)
MHLD	0:7:4	0	**Mark Hold.** When control bit MHLD is a 1, the transmitter input data stream is forced to all marks (1s). (HDX only)
NEWC0	0:E:3	0	**New Configuration Chip 0.** When the host changes the transmitter configuration (TCONF), the host must write a 1 to this bit. NEWC0 goes to 0 when the change becomes effective.
NEWC1	1:E:3	0	**New Configuration Chip 1.** When the host changes the receiver configuration (RCONF), the host must write a 1 to this bit. NEWC1 goes to 0 when changes become effective.
NEWC2	2:E:3	0	**New Configuration Chip 2.** When the host changes the receiver configuration (RCONF), the host must write a 1 to this bit. NEWC2 goes to 0 when changes become effective.
NEWS0	0:E:5	0	**New Status Chip 0.** NEWS0 is set to a 1 when any of the status bits in the transmitter status register A (0:A) change state. The host must write a 0 into NEWS0 to reset it. (FDX)
NEWS1	1:E:5	0	**New Status Chip 1.** NEWS1 is set to a 1 when any of the status bits in the receiver Chip 1 status registers 8 or 9 (1:8 or 1:9) change state. The host must write a 0 into NEWS1 to reset it. (FDX)
NEWS2	2:E:5	0	**New Status Chip 2.** NEWS2 is set to a 1 when of the status bits n the receiver chip 2 status register 5 (2:5) change state. The host must write a 0 into NEWS2 to reset it. (FDX)
NSIE0	0:E:6	0	**NEW Status Interrupt Enable Chip 0.** When NSIE0 is set to a 1, the modem sets the TIA bit and asserts $\overline{IRQ}$ if NEWS0 is a 1. The TIA bit is cleared by writing a 0 to the NEWS0 bit. (FDX)
NSIE1	1:E:6	0	**NEW Status Interrupt Enable Chip 1.** When NSIE1 is set to a 1, the modem sets the RIA1 bit and asserts $\overline{IRQ}$ if NEWS1 is a 1. The RIA1 bit is cleared by writing a 0 to the NEWS1 bit. (FDX)
NSIE2	2:E:6	0	**NEW Status Interrupt Enable Chip 2.** When NSIE2 is set to a 1, the modem sets the RIA2 bit and asserts $\overline{IRQ}$ if NEWS2 is a 1. The RIA2 bit is cleared by writing a 0 to the NEWS2 bit. (FDX)
NV25	0:9:7	0	**No V25 Answer Tone.** When NV25 is a 1, the modem will not transmit the 2100 Hz CCITT answer tone when a handshake sequence is initiated and the modem is in answer mode. (FDX)

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
ORG	0:8:5	0	**Originate/Answer.** When ORG is a 1, the modem is in originate mode. When ORG is a 0, the modem is in answer mode. (This is valid in manual originate/answer and analog loop back). If ORG is a 1 in analog loopback, the modem will transmit in low band and receive in high band. If ORG is a 0 in analog loop back, the modem will transmit in the high band and receive in low band. (FDX)
PARSL0	0:5:4		**Parity Select Chip 0.**
PARSL1	1:5:4		**Parity Select Chip 1.** Control bits PARSL0 and PARSL1 select the method by which parity is generated in the transmitter (PARSL0) and checked by the receiver (PARSL1) during the asynchronous mode (ASYNC1 and ASYNC0 = 1). The options are: **Parity Selected** **4** Even parity 0 Odd Parity 1
PE	1:9:3	0	**Parity Error.** When set to a 1, status bit PE indicates that a character with bad parity was received in the asynchronous mode (ASYNC1 and ASYNC0 = 1). When a 0, a character with good parity was received.
PEN0	0:5:5	0	**Parity Enable Chip 0.** When control bit PEN0 is a 1, parity generation is enabled in the transmitter in asynchronous mode (ASYNC0 = 1).
PEN1	0:5:5	0	**Parity Enable Chip 1.** When control bit PEN1 is a 1, parity checking is enabled in the receiver in asynchronous mode (ASYNC1 = 1).
$\overline{\text{PNDET}}$	2:C:0	1	**PN Sequence Detect.** Status bit $\overline{\text{PNDET}}$ is set to a 0 when a PN sequence has been detected. $\overline{\text{PNDET}}$ is set to a 1 at the end of the PN sequence. (HDX)
$\overline{\text{P2DET}}$	1:8:3	1	**Period 2 Sequence Detect.** Status bit $\overline{\text{P2DET}}$ is set to a 0 when a period 2 sequence has been detected. $\overline{\text{P2DET}}$ is set to a 1 at the start of the period N sequence. (HDX)
RA	0:8:0	0	**Relay Active.** When control bit RA is set to a 1, the OHRC output is activated causing the relay to close (off-hook); when RA is reset to 0, the OHRC is turned off causing the relay to open (on-hook). **Note:** The host has exclusive control of the OHRC output through the RA bit except in pulse dial mode. (FDX)
RBA1	1:E:0	1	**Receiver Buffer Available Chip 1.** Status bit RBA1 is set to a 1 when the receiver writes data to the Receiver Data Register (1:0). RBA1 resets to a 0 when the host reads data from register 1:0.
RBA2	2:E:0	0	**Receiver Buffer Available Chip 2.** Status bit RBA2 is set to a 1 when the receiver writes data to register 2:0. RBA2 resets to a 0 when the host reads from register 2:0.
RCF	1:7:2	0	**Receiver Carrier Frequency.** When set to a 1, control bit RCF selects 1800 Hz demodulator carrier frequency; when a 0, 1700 Hz is selected. (HDX V.29 FT only)

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
RCONF	1:6:0-7	84	**Receiver Configuration.** The host configures the receiver by writing one of the following control codes into RCONF:

Mode	RCONF (Hex) No TOD	RCONF (Hex) (HDX)[1]
V.29 FT/9600	1C	9C
V.29 FT/7200	1A	9A
V.29 FT/4800	19	99
V.29 9600	14	94
V.29 7200	12	92
V.29 4800	11	91
V.27 FT/4800	0A	8A
V.27 FT/2400	09	89
V.27 4800 Long	22	A2
V.27 2400 Long	21	A1
V.22 bis 2400	84	–
V.22 bis 1200	88	–
V.22 1200	52	–
V.22 600	51	–
Bell 212A 1200	62	–
Bell 103 0-300	60	–
Call Progress[2]	80	–

NOTES:

1. These configurations enable the train-on-data (TOD) algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD configurations are selected, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-date.
2. When Call Progress is selected, the receiver is placed in tone detect mode. Any energy above threshold and in the 340 to 640 Hz bandwidth is reflected by the TONE bit. The receiver configuration (RCONF) must be set to the desired receive mode (after last digit was dialed and tone detection completed) before the answer tone is sent by the answering modem (after ringback is detected). Call Progress need not be used during auto dialing, but may be used to provide call progress information as part of an intelligent auto dialing routine.
3. RDIS bit must be set to 1 prior to reconfiguration in half-duplex mode.
4. When the modem shifts between half-duplex and full-duplex modes, 10 ms initialization time is required before continued operation.

RDIS	1:7:1	0	**Receiver Disable.** When control bit RDIS is a 1, the receiver is disabled. When RDIS is a 0, the receiver is enabled. RDIS must be set to a 1 prior to changing the receiver configuration. (HDX)
RDL0	0:4:2	0	**Remote Digital Loopback Chip 0.**
RDL2	2:4:2	0	**Remote Digital Loopback Chip 2.** When RDL0 and RDL2 are 1s, the modem sends a remote digital loop request. When RDL0 and RDL2 are 0s, the modem sends a remote digital loopback termination. (V.22, V.22 bis, V.22 A/B, and Bell 212A) (FDX) (RDL2 must be set first followed by RDL0).
RDLE0	0:4:6	0	**Response to Remote Digital Loopback Enable Chip 0.** When RDLE0 is a 1, the transmitter can respond to another modem's request for digital loopback. When RDLE0 is a 0, no response will be generated. (FDX)

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
RDLE2	2:4:6	0	**Response to Remote Digital Loopback Enable Chip 2.** When RDLE2 is a 1, the receiver can respond to another modem's request for digital loopback. When RDEL2 is a 0, no response will be generated. (FDX)
RIA1	1:E:7	0	**Receiver Interrupt Active Chip 1.** Status bit RIA1 is set to a 1 when the receiver sample rate device is driving $\overline{IRQ}$ low (see NSIE1 and RIE1).
RIA2	2:E:7	0	**Receiver Interrupt Active Chip 2.** Status bit RIA2 is set to a 1 when the receiver baud rate device is driving $\overline{IRQ}$ low (see NSIE2 and RIE2).
RIE1	1:E:2	0	**Receiver Interrupt Enable Chip 1.** When the RIE1 control bit is a 1, the RIA1 bit is set to a 1 and the $\overline{IRQ}$ output is asserted when RBA1 is a 1.
RIE2	2:E:2	0	**Receiver Interrupt Enable Chip 2.** When the RIE2 control bit is a 1, the RIA2 bit is set to a 1 and the $\overline{IRQ}$ output is asserted when RBA2 is a 1.
RI	2:5:3	0	**Ring Indicator.** When set to a 1, status bit RI indicates that a ringing signal is being detected. The RI bit follows the ringing signal with a 1 during the on time and a zero during the off time coincident with the $\overline{RI}$ signal. (FDX)
RPDM	1:5:2	0	**Receiver Parallel Data Mode.** When RPDM is a 1, the receiver is in parallel data mode.In this mode, received data is output to the Receive Data Register (RXDATA) and to the RXD pin. Diagnostics are not operational in the parallel data mode (i.e., DSP RAM can not be accessed). When RPDM is a 0, the receiver is in serial data mode. In this mode, received data is output to RXD only.
RSD	2:4:4	0	**Receiver Space Disconnect.** When configuration bit RSD is a 1, the modem goes to idle mode after receiving approximately 1.6 seconds of continuous spaces. (FDX)
RTH	1:7:6, 7	0	**Receiver Threshold.** The receiver energy detector threshold is set by the RTH field as follows: (see NEWC1). (HDX only) RTH / $\overline{RLSD}$ ON / $\overline{RLSD}$ OFF 0 / ≥ –43 dBm / ≤ –48 dBm 1 / ≥ –33 dBm / ≤ –38 dBm 2 / ≥ –26 dBm / ≤ –31 dBm
RTRN	0:9:5		**Retrain.** When RTRN is a 1, the modem sends the training sequence. RTRN resets to 0 when the training sequence from the remote modem has successfully been received. If the sequence has not been successfully received from the remote modem, $\overline{CTS}$ will remain off. In order to put the modem back into data mode, it is necessary to write a 0 into the RTRN bit, then repeat the retrain sequence. (FDX)
RTS	0:7:7	0	**Request To Send.** When RTS is a 1, the modem begins a transmit sequence. The transmitter continues to transmit until RTS is a 0 and a turn off sequence has been completed.
RXDATA	1:0:0-7	0	**Receive Data Register.** The host obtains channel data from the modem receiver in the parallel data mode (RPDM = 1) by reading a data byte from RXDATA.
SDIS	0:7:5	0	**Scrambler Disable.** When control bit SDIS is a 1, the transmitter's scrambler circuit is disabled; When SDIS is a 0, the scrambler is enabled.
SPEED	2:5:0-2	0	**Speed Indicator.** The SPEED status bits indicates the received rate at the completion of a handshake (FDX). The SPEED bit representations are: Data Rate / 2 1 0 0 - 300 / 0 0 0 600 / 0 0 1 1200 / 0 1 0 2400 / 0 1 1

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
SSD	0:8:1	0	**Send Space Disconnect.** When $\overline{DTR}$ goes from an active to an inactive state and configuration bit SSD is a 1, the modem transmits approximately 3.4 seconds of spaces before disconnecting. (FDX)
ST0	0:4:5	0	**Self Test Chip 0.**
ST2	2:4:5	0	**Self Test Chip 2.** When configuration bit ST2 is a 1, receiver self test is activated. ST2 must be a 0 to end the test. It is possible to perform self test in analog loopback with or without a DTE connected. During self test, TXD and $\overline{RTS}$ are ignored. Self test does not test asynchronous-to-synchronous converter circuits in the receiver. (FDX) Error detection is accomplished by monitoring the self test error counter in DSP RAM. If the counter increments during the self test, an error occurred. The counter contents are available in the diagnostic register when the RAM access code 27 is loaded in ACC2. ***Self Test End-to-End (Data Mode)*** Upon activation of self test, an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. ***Self Test with Loop 3*** Loop 3 is applied to the modem as defined in Recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test. $\overline{DTR}$ is ignored in this test. ***Self Test with Loop 2 (Data Mode)*** The modem is conditioned to instigate a loop 2 at the remote modem as specified in Recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test. ST2 does not function in 300 bps.
STB0	0:5:3	0	**Stop Bit Number Chip 0.** When STB0 is a 0, one stop bit is selected in the transmitter in the asynchronous mode. When STB0 is a 1, two stop bits are selected in asynchronous mode. (FDX)
STB1	1:5:3	0	**Stop Bit Number Chip 1.** When STB1 is a 0, one stop bit is selected in the receiver in the asynchronous mode. When STB1 is a 1, two stop bits are selected in the asynchronous mode. (FDX)
TBA	0:E:0	1	**Transmitter Buffer Available.** Status bit TBA is set to a 1 when the transmitter empties Transmitter Data Register (0:0). TBA resets to a 0 when the host writes to the Transmitter Data Register (TXDATA).
TCF	0:9:3	0	**Transmitter Carrier Frequency.** When TCF is a 0, the transmitter carrier is 1700 Hz. When TCF is a 1, the transmitter carrier is 1800 Hz. The NEWC0 bit must be set to a 1 after changing this bit. (HDX V.29 FT only.)
TLVL	0:B:5-7	5	**Transmit Level.** The transmit level bits select the transmit level in steps of 2 dB, as follows: **Transmit Level (dBm) — 7 6 5** 0 — 0 0 0 –2 — 0 0 1 –4 — 0 1 0 –6 — 0 1 1 –8 — 1 0 0 –10 — 1 0 1 –12 — 1 1 0 –14 — 1 1 1 At the power up, the transmit level defaults to –10 dBm.

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
TXDATA	0:0:0-7	00	**Transmitter Data Register.** The host sends channel data from the modem transmitter in the parallel data mode (TPDM = 1) by reading a data byte from TXDATA when TBA is a 1.
TCONF	0:6:0-7	84	**Transmitter Configuration.** The host configures the transmitter by writing one of the following codes into TCONF: **Note:** When the modem switches between half-duplex and full-duplex modes, 10 ms initialization time is required before continued operation. **Mode** — **TCONF (Hex)** V.29 FT/9600 — 1C V.29 FT/7200 — 1A V.29 FT/4800 — 19 V.29 9600 — 14 V.29 7200 — 12 V.29 4800 — 11 V.27 FT/4800 — 0A V.27 FT/2400 — 09 V.27 4800 Long — 22 V.27 2400 Long — 21 V.22 Bis 2400 — 84 V.22 Bis 1200 — 88 V.22 1200 — 52 V.22 600 — 51 Bell 212A 1200 — 62 Bell 103 0-300 — 60 Call Request — 80 Single Tone Transmit — 04 When Call Request is selected, the transmitter is placed in auto dial mode. The data then placed in the Dial Digit Register (DDR) is treated as the digit to be dialed. The format for the data should be a hex representation of the number to be dialed (if a 9 is to be dialed then a 09_{16} should be loaded in DDR). The modem must be off-hook in this mode. (DTR must be on when in auto dial mode.)
TIA	0:E:7	0	**Transmitter Interrupt Active.** TIA status bit is a 1 whenever the transmitter is driving $\overline{IRQ}$ signal low (see NSIE0 and TIE).
TIE	0:E:2	0	**Transmitter Interrupt Enable.** When control bit TIE is a 1, the modem sets the TIA bit to a 1 and asserts the $\overline{IRQ}$ output when status bit TBA is a 1.
TM	2:5:4	0	**Test Mode.** When TM is a 1, test mode is active in the transmitter. When TM is a 0, test mode is not active. (FDX)
TONE	1:9:1	0	**Tone Detect.** Tone is set to a 1 when energy is detected in the 340 to 640 Hz frequency band. The host must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when Call Progress is selected (RCONF = 80). (FDX)
TONEA	2:5:5	0	**Answer Tone Detected.** When set to a 1, status bit TONEA signifies that the receiver detected the answer tone. This bit is set 75 ms after the answer tone is first detected, and is cleared to a 0 when the modem goes to idle mode. The host may clear the TONEA bit manually after $\overline{CTS}$ is active.

Table 12. R96QT Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value (Hex)	Name/Description
TPDM	0:7:2	0	**Transmitter Parallel Data Mode.** When TPDM is a 1, the transmitter parallel data mode is selected. In this mode, the transmitter accepts data from the Transmitter Data Register (0:0) rather than the serial TXD hardware data input. Diagnostics are not operational in this mode (i.e., DSP RAM can not be accessed). When TPDM is a 0, transmitter serial data mode is selected. The transmitter accepts data from the TXD input. DSP RAM can be accessed in the serial data mode.
TTDIS	0:7:6	0	**Transmitter Train Disable.** When TTDIS is a 1, the transmitter does not generate a training sequence at the start of transmission. With training disable, RTS/CTS delay is less than 2 baud times. (HDX)
TXCLK	0:7:0,1	0	**Transmit Clock Select.** TXCLK designates the origin of the transmitter data clock. **Clock Source** **1** **0** Internal 0 0 (HDX, FDX) External 1 0 (HDX, FDX) Slave 1 1 (FDX)
WRT0	0:F:7	0	**RAM Write Chip 0.** When WRT0 is a 1, the RAM write operation is enabled for Chip 0.
WRT1	1:F:7	0	**RAM Write Chip 1.** When WRT1 is a 1, the RAM write operation is enabled for Chip 1.
WRT2	2:F:7	0	**RAM Write Chip 2.** When WRT2 is a 1, the RAM write operation is enabled for Chip 2.
XDAL0	0:2:0-7	00	**X RAM DATA LSB Chip 0.** XDAL0 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAL1	1:2:0-7	00	**X RAM DATA LSB Chip 1.** XDAL1 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAL2	2:2:0-7	00	**X RAM DATA LSB Chip 2.** XDAL2 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2.
XDAM0	0:3:0-7	00	**X RAM DATA MSB Chip 0.** XDAM0 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAM1	1:3:0-7	00	**X RAM DATA MSB Chip 1.** XDAM1 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAM2	2:3:0-7	00	**X RAM DATA MSB Chip 2.** XDAM2 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2.
YDAL0	0:0:0-7	00	**Y RAM DATA LSB Chip 0.** YDAL0 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAL1	1:0:0-7	00	**Y RAM DATA LSB Chip 1.** YDAL1 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAL2	2:0:0-7	00	**Y RAM DATA LSB Chip 2.** YDAL2 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 2.
YDAM0	0:1:0-7	00	**Y RAM DATA MSB Chip 0.** YDAM0 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP Chip 0.
YDAM1	1:1:0-7	00	**Y RAM DATA MSB Chip 1.** YDAM1 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP Chip 1.
YDAM2	2:1:0-7	00	**Y RAM DATA MSB Chip 2.** YDAM2 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP Chip 2.

DSP RAM ACCESS

DSP RAM Organization

Each DSP contains four banks of 16-bit wide random access memory (RAM). This memory is divided into two banks of 32-bit wide words of Data RAM (DRAM) and Coefficient RAM (CRAM). Each 32-bit word is further broken down into a 16-bit real part and a 16-bit imaginary part.

RAM Access Codes

The DSP logic unit determines the DSP RAM address to read from, or write to, by the code stored in the RAM Access bits of interface memory register (0,1,2):F.

Data can be transferred from interface memory to DSP RAM. When set to a 1, bit WRT (0,1,2) signals the DSP to disable transfer of DSP RAM data to the interface memory, and instead, to transfer data from interface memory to DSP RAM. When writing into DSP RAM, 32 bits of data in the XRAM and YRAM registers will be written into the appropriate DSP RAM location as specified by the RAM access code in Table 13.

To transfer data into the DSP RAM, first load the desired access code into the appropriate RAM Access register (ACC0-2) and set the write bit (WRT0-2) to a one. Data may then be written into registers 3, 2, 1 and 0 in that order. If writing to registers 3 and 2 only, the data in registers 1 and 0 must be rewritten without modification in order for the data transfer to occur. When the host processor writes into register (0, 1, 2):0:0-7, the buffer available bit (0, 1, 2):E:0 is reset to zero. When the DSP reads data from register (0, 1, 2):0:0-7, the buffer available bit (0, 1, 2):E:0 is set to a one, indicating the RAM write has been completed. After the RAM write is complete, reset the write bit (WRT0-2) to a zero.

When reading from DSP RAM, or writing to DSP RAM, the bits in register 0, 1, 2:E can be used for handshaking or interrupt functions as in parallel data mode.

Table 13. RAM Access Codes

Function	RAM Access Code (Hex) Read	Write	Chip	Register
Half-Duplex Modem Operation				
Demodulator Output				
2400 baud	53	–	1	0,1,2,3
1600 baud	51	–	1	0,1,2,3
1200 baud	4F	–	1	0,1,2,3
Low Pass Filter Output	5F	–	1	0,1,2,3
Input Signal to Equalizer Taps	40	–	2	0,1,2,3
AGC Gain Word	30	–	1	2,3
Equalizer Tap Coefficients	01-20	–	2	0,1,2,3
Equalizer Output	61	–	2	0,1,2,3
Rotated Equalizer Output	62	–	2	0,1,2,3
Decision Points	68	–	2	0,1,2,3
Rotated Error	64	–	2	0,1,2,3
Rotation Angle	27	–	2	2,3
Phase Vector	21	–	2	0,1,2,3
Error Vecor	65	–	2	0,1,2,3
EQM	2C	–	2	2,3
Frequency Correction	25	–	2	2,3
Full-Duplex Modem Operation				
Demodulator	62	–	1	0,1,2,3
Low Pass Filter Output	63	–	1	0,1,2,3
Input Signal to Equalizer Taps	41-50	–	2	0,1,2,3
AGC Gain Word	02	–	1	2,3
Equalizer Tap Coefficients	01-10	–	2	0,1,2,3
Equalizer Output	56	–	2	0,1,2,3
Rotated Equalizer Output	14	–	2	0,1,2,3
Decision Points	54	–	2	0,1,2,3
Rotated Error	55	–	2	0,1,2,3
Rotation Angle	15	–	2	0,1
Phase Vector	13	–	2	2,3
Self-Test Error Counter	27	–	2	2,3
DTMF Tone Duration	02	82	0	0,1
DTMF Interdigit Delay	03	83	0	2,3
Pulse Interdigit Delay	03	83	0	0,1
Pulse Relay Make Time	04	84	0	2,3
Pulse Relay Break Time	04	84	0	0,1
Handshake Abort Counter	05	85	0	0,1
Handshake Abort Timer	06	86	0	2,3
CTS Off-Time	07	87	0	2,3
Checksum	3F	–	0,1,2	0,1
DSP–ID	3F	–	0,1,2	2,3

PERFORMANCE

BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56.

PHASE JITTER

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak jitter at 30 Hz.

Polling Success

In the 9600 bps fast train configuration the modem approaches a 98% success rate over unconditioned 3002 lines for a signal-to-noise ratio of 26 dB, with a received signal level of –20 dBm.

HIGH SPEED

Bit Error Rate

Typical bit error rate (BER) curves for high speed operation are shown in Figure 5. The BER curves were prepared from data obtained using a TAS1000 test system.

MEDIUM SPEED

Bit Error Rate

Typical BER curves for the medium speed operation are shown in Figure 6. The BER curves were prepared from data obtained using a TAS1000 test system.

GENERAL SPECIFICATIONS

Table 14. Modem Power Requirements

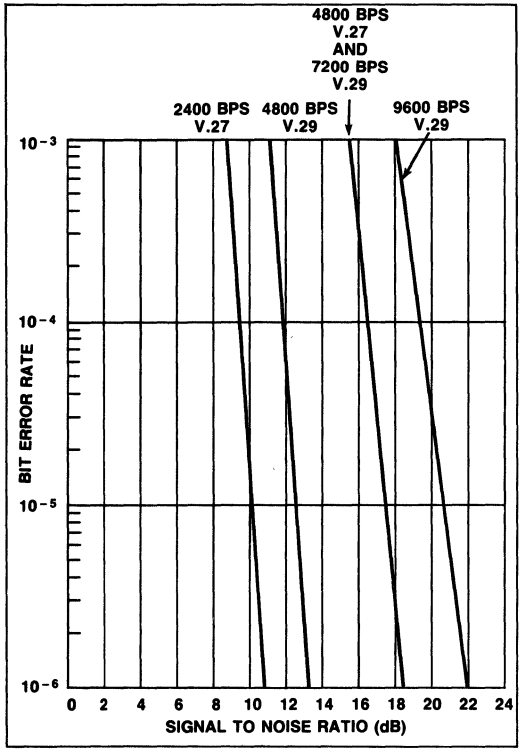
Voltage*	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
+ 5 VDC + 5%, + 12 VDC ± 5% – 12 VDC ± 5%	550 mA 5 mA 25 mA	700 mA 10 mA 50 mA
* Input voltage ripple ≤ 0.1 volts peak-to-peak.		

Table 15. Modem Environmental Specifications

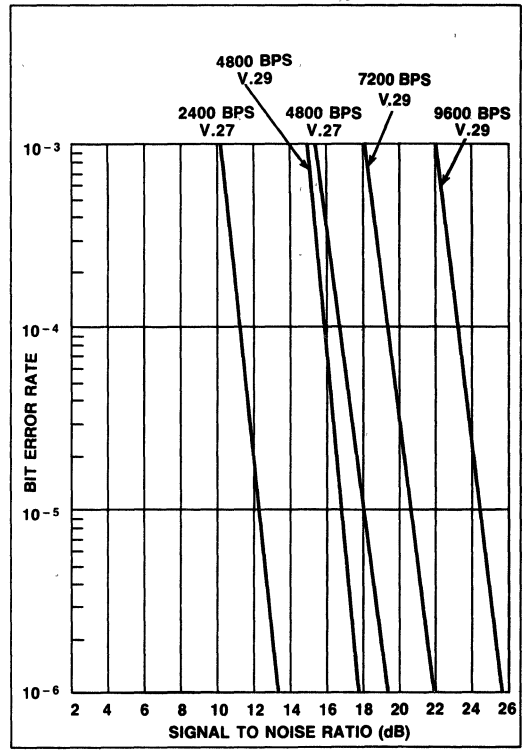
Parameter	Specification
Temperature Operating Storage	 0° C to + 60° C (32° F to 140° F) – 40° C to + 80° C (–40° F to 176° F) (Stored in heat sealed antistatic bag and shipping container.)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35° C, whichever is less.
Altitude	– 200 feet to + 10,000 feet

Table 16. Modem Mechanical Dimensions

Parameter	Specification
Board Structure:	Single PC board with 60 pins in a dual in-line pin configuration. Row 1 has 29 pins (pins 1 through 30 with pin 15 deleted for keying). Row 2 has 31 pins (pins 31 through 61 with pin 31 off-set from pin 1 for keying).
Dimensions: Width Length	 2.559 in. (65 mm) 3.937 in. (100 mm)
Component Height Top (max.) Bottom (max.)	 0.300 in. (7.62 mm) 0.100 in. (2.54 mm)
Weight (max.):	2.5 oz. (70 g)
Pin Length (max.)	0.433 ± 0.015 in. (11.0 ± 0.4 mm), gold plated

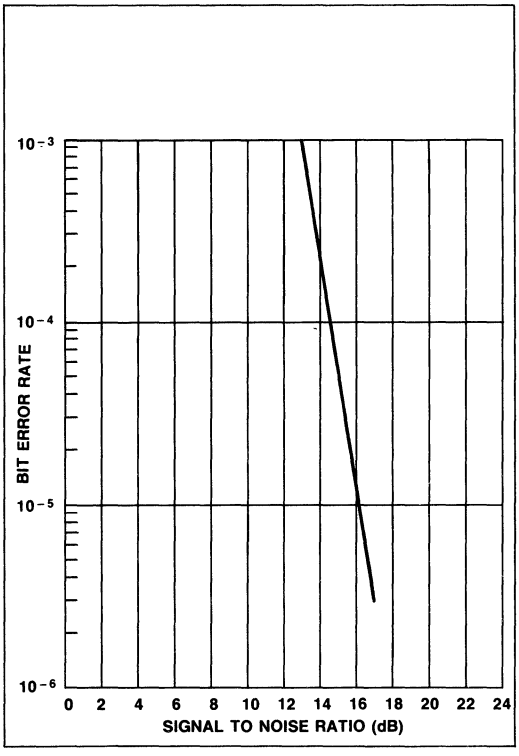


Back-to-Back, –20 dBm Receive Signal Level

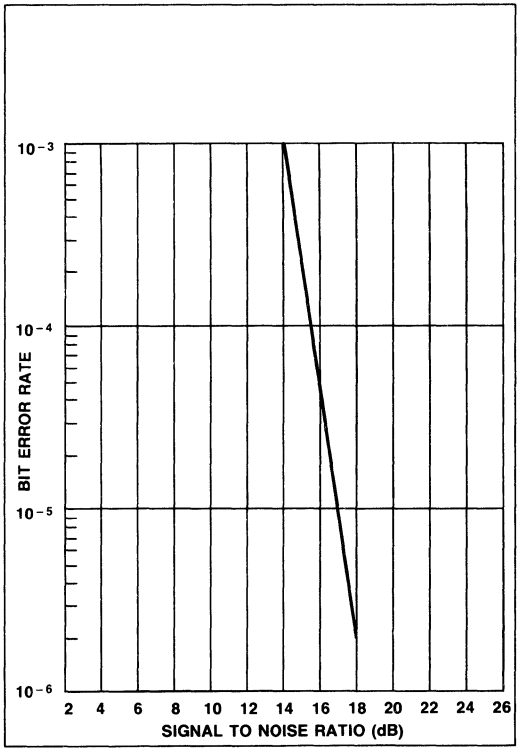


3002 Unconditioned Line, –20 dBm Receive Signal Level

Figure 5. Typical High Speed Bit Error Rate Curves



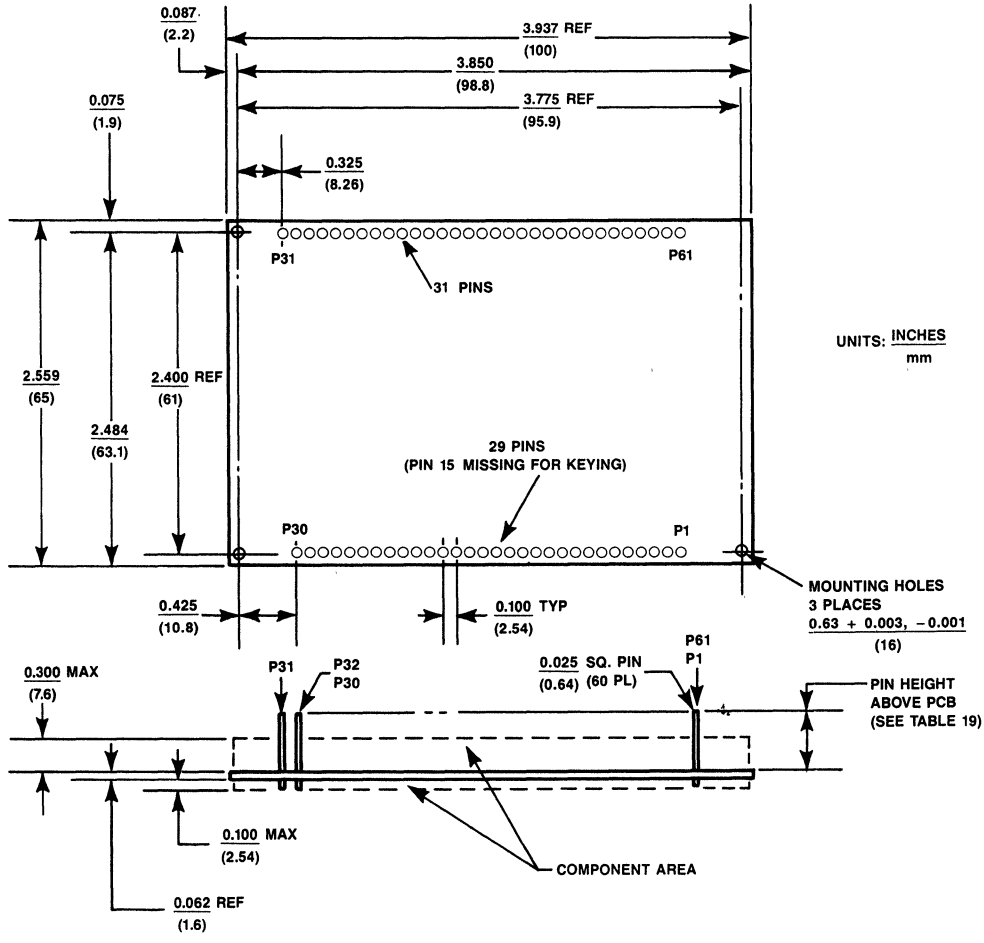
2400 BPS, Synchronous Answer
3002 Unconditioned Line, – 30 dBm Receive Signal Level



2400 BPS, Synchronous, Originate
3002 Unconditioned Line, – 32 dBm Receive Signal Level

Figure 6. Typical Medium Speed Bit Error Rate Curves

DIMENSIONS


0.087
(2.2)
3.937 REF
(100)
3.850
(98.8)
3.775 REF
(95.9)
0.075
(1.9)
0.325
(8.26)
P31
P61
31 PINS
UNITS: INCHES
mm
2.559
(65)
2.400 REF
(61)
2.484
(63.1)
29 PINS
(PIN 15 MISSING FOR KEYING)
P30
P1
MOUNTING HOLES
3 PLACES
0.63 + 0.003, −0.001
(16)
0.425
(10.8)
0.100 TYP
(2.54)
0.300 MAX
(7.6)
P31
P32
P30
P61
P1
0.025 SQ. PIN
(0.64) (60 PL)
PIN HEIGHT
ABOVE PCB
(SEE TABLE 19)
0.100 MAX
(2.54)
COMPONENT AREA
0.062 REF
(1.6)

Rockwell

R9696DP
V.32 9600 bps Full-Duplex Modem

INTRODUCTION

The Rockwell R9696DP is a 2-wire full-duplex, synchronous/asynchronous CCITT V.32 and V.22 bis modem data pump. It is designed to operate over the public switched telephone network (PSTN), as well as leased lines, through the appropriate line termination. It is packaged in a small module with dual-in-line (DIP) connection for direct installation onto a host module.

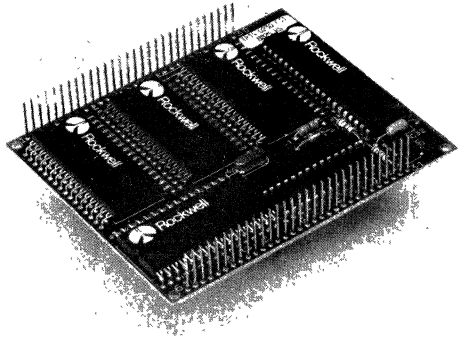
The modem satisfies the telecommunications requirements specified in CCITT recommendations V.32, V.22 bis, V.22, V.23 and V.21 and is compatible with Bell 212A and Bell 103 modems. The R9696DP can operate at speeds of 12000, 9600, 7200, 4800, 2400, 1200, 600 or 300 bps.

The R9696DP is designed for use in ultra high speed data applications. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size (less than 13 square inches), low power consumption, serial/parallel host interface, and DIP connection simplify system development and reduce system production cost.

This data sheet applies to the R9696DP with device numbers C5305-16, C5306-17, C5307-17 and subsequent.

FEATURES

- Compatibilities
  - — CCITT: V.32, V.22 bis, V.22, V.23 and V.21
  - — Bell: Bell 212A/103
- Parallel synchronous
- Serial synchronous/asynchronous
- 2-Wire Full-Duplex Operation
- Trellis-Coded Modulation (TCM) at 12000, 9600, and 7200 bps
- 12000 bps data rate in V.32 (proprietary)
- Programmable Near and Far End Echo Cancellation
- Bulk Delay for Satellite Transmission
- Auto-Dial and Auto-Answer Capability
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Dynamic Range: −43 dBm to 0 dBm
- Equalization
  - — Compromise Equalizer in Transmitter
  - — Automatic Adaptive Equalizer in Receiver
- Diagnostic Capability
- Loopback
  - — Local Analog
  - — Remote Digital
- Small Size
  - — 82 mm x 100 mm (3.23 in. x 3.94 in.) with DIP Connection
- Low Power Consumption: 1.9 W (Typical)



R9696DP Modem

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

TONE GENERATION

Under control of the host processor, the modem can generate single or dual voice-band tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

DATA ENCODING

The data encoding conforms to CCITT recommendations V.32, V.22 bis, V.22, V.23 and V.21; and to Bell 212A and 103.

EQUALIZERS

Equalization functions are provided that improve performance when operating over low quality lines.

Compromise Equalizer — A 40-tap digital finite impulse response (FIR) filter in the transmitter provides compromise equalization. The filter taps can be changed in DSP RAM for varying line conditions. The default equalizer tap coefficients compensate for half the amplitude distortion of a 3002 unconditioned line and for half the group delay distortion of a 3002 unconditioned line. The filter can be enabled or disabled using the CEQ bit in the Chip 0 interface memory.

A 40-tap digital finite impulse response (FIR) filter in the receiver provides compromise equalization for V.23 1200 and 600 configurations only. The filter is identical to the transmitter compromise equalizer and can be programmed via the DSP RAM. This feature is enabled and disabled using the CEQ23 bit in the Chip 1 interface memory.

Automatic Adaptive Equalizer — A 48-tap automatic adaptive equalizer is provided in the receiver. The equalizer can be configured as either a T or a T/2 equalizer using the EQT2 bit in the Chip 2 interface memory.

TRANSMITTED DATA SPECTRUM

When the transmitter compromise equalizer is disabled, the transmitter spectrum is shaped by raised cosine filter functions as follows:

Configuration	Raised Cosine Filter Function
V.32	Square root of 12.5%
V.22 bis, Bell 212A	Square root of 75%

RTS–CTS RESPONSE TIME

The response times of CTS relative to a corresponding transition of RTS are given in Table 2.

Table 2. RTS-CTS Response Time

CTS Transition	Configuration	Constant Carrier	Controlled Carrier
OFF to ON	V.32	≤2 ms	N/A
	V.22 bis	≤2 ms	270 ms
	V.22	≤2 ms	270 ms
	Bell 212A	≤2 ms	270 ms
	V.21	500 ms	500 ms
	Bell 103	210 ms	210 ms
	V.23	210 ms	210 ms
ON to OFF	All	≤2 ms	≤2 ms

Notes: The CTS OFF to ON response time is host programmable in DSP RAM
N/A = not applicable.

TRANSMIT LEVEL

The transmitter output level is selectable from −0.5 dBm to −15.5 dBm in 1 dB steps and is accurate to ±0.5 dB. The output level can also be fine tuned to a value within a 1 dB step by changing a gain constant in RAM.

TRANSMITTER TIMING

Transmitter timing is selectable between internal (±0.01%), external or loopback.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with the applicable CCITT recommendation or Bell interface depending on the selected configuration.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits per Symbol		Constellation Points
					Data	TCM	
V.32 12000 TCM[2]	TCM	1800	12000	2400	5	1	64
V.32 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 9600	QAM	1800	9600	2400	4	0	16
V.32 4800	QAM	1800	4800	2400	2	0	4
V.32 7200 TCM[2]	TCM	1800	7200	2400	3	1	16
V.22 bis 2400	QAM	1200/2400	2400	600	4	0	16
V.22 bis 1200	QAM	1200/2400	1200	600	2	0	4
V.22 1200	QAM	1200/2400	1200	600	2	0	4
V.22 600	QAM	1200/2400	600	600	1	0	2
Bell 212A	QAM	1200/2400	1200	600	2	0	4
Bell 103	FSK	1170/2125	0–300	300	1	0	—
V.23 1200	FSK	1700/420	1200/75	1200	1	0	—
V.23 600	FSK	1500/420	600/75	600	1	0	—
V.21	FSK	1080/1750	0–300	300	1	0	—
Tone Transmit							

Notes: 1. Modulation legend: TCM: Trellis-Coded Modulation
QAM: Quadrature Amplitude Modulation
FSK: Frequency Shift Keying
2. Proprietary

ANSWER TONE

The transmitter generates a 2100 Hz answer tone for 3.6 seconds at the beginning of the answer handshake when the NV25 bit is a zero. This is applicable to V.32, V.22 bis, V.22, V.21, and V.23. The V.32 answer tone has 180 degree phase reversals every 0.45 seconds to disable network echo cancellers.

RECEIVE LEVEL

The receiver satisfies performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the Receiver Analog (RXA) input.

RECEIVER TIMING

The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

CARRIER RECOVERY

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off. $\overline{\text{RLSD}}$ can also be clamped to a mark by a bit in the receiver sample rate device interface memory.

ECHO CANCELLER

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full duplex V.32 operation. The combined echo span of near and far cancellers is host programmable with a default value of 53.3 ms (53.3 ms is also the maximum programmable value). The proportion allotted to each end is host programmable with default values of 23.3 ms for near-end and 30 ms for far-end. The delay between near-end and far-end echoes can be up to 1.7 seconds. The canceller can compensate for ±7 Hz frequency offset in the far-end echo.

The echo canceller error signal may be monitored through the transmitter DSP interface memory.

ASYNC/SYNC, SYNC/ASYNC CONVERSION

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converter operates in serial mode only. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character sizes, including all bits, are 7, 8, 9, 10 and 11 bits per character. Two ranges of signaling rates are provided:

- Basic range: +1% to −2.5%
- Extended overspeed range: +2.3% to −2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break is handled in the transmitter and receiver as described in V.22 bis.

Asynchronous characters are accepted by the transmitter on the TXD serial input and issued by the receiver on the RXD serial output. To configure the converters, the host must set up interface memory bits EXOS0, PEN0, STB0 and WDSZ0 bits before setting ASYN0 for the transmitter and EXOS1, PEN1, STB1 and WDSZ1 bits before setting ASYN1 for the receiver. (See description of these bits in Table 8.) Asynchronous data mode is not supported in V.32 12000 bps.

1

AUTO-DIALING AND AUTO-ANSWERING CONTROL

General Description

Functions are provided to allow the host to perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection and a comprehensive supervisory tone detection scheme. The major parameters of these functions are host programmable, enabling the host to customize the modem to work on the public switched telephone network (PSTN).

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path. Therefore, the tone detect signal does not pass through the highpass section of the analog receive bandpass filter, enabling the tone detection to be largely independent of the receiver status. The tone detection bandwidth depends on the configuration:

Receiver Configuration	Tone Detection Bandwidth
V.32, V.23	0–3400 Hz
V.22 bis, V.22, Bell 212A, Bell 103 Originate	0–2800 Hz
V.22 bis, V.22, Bell 212A, Bell 103 Answer	0–1700 Hz
V.21 Originate	0–2200 Hz
V.21 Answer	0–1300 Hz

There are, however, some restrictions depending on the receiver configuration and status:

1. When DATA1 bit (see Table 8) is a 0, all three tone detectors are enabled.
2. When DATA1 bit is a 1 and the receiver is in synchronous mode (except V.32 12000), tone detectors A and B are enabled and tone detector C is disabled.
3. When DATA1 bit is a 1, the receiver is in asynchronous mode or V.32 12000, and the TDAE bit is a 1, tone detector A is enabled and tone detectors B and C are disabled.
4. All three tone detectors are disabled during a V.32 handshake.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit in interface memory causing tone detector C to be an eighth order filter.

Supervisory Tone Detectors, Default Characteristics

The default bandwidths and thresholds of the tone detectors are as follows:

Tone Detector	Bandwidth	Turn-On Threshold	Turn-Off Threshold
A	245–650 Hz	– 25 dBm	– 31 dBm
B	360–440 Hz	– 25 dBm	– 31 dBm
C Prefilter	0–500 Hz	N/A	N/A
C	50–110 Hz	*	*

*Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range – 1 dBm to – 26 dBm.

HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 1) shows the typical modem connection in a system. In this diagram, any point that is active low is represented by a small circle at the signal point. Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{IRQ}$). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high, (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals shown in Figure 1 are organized into six functional groups: overhead, microprocessor interface, V.24 interface, ancillary, analog, and diagnostic. These signals, along with their connector pin numbers and interface circuit types, are listed in Table 3. The digital interface characteristics are defined in Table 4.

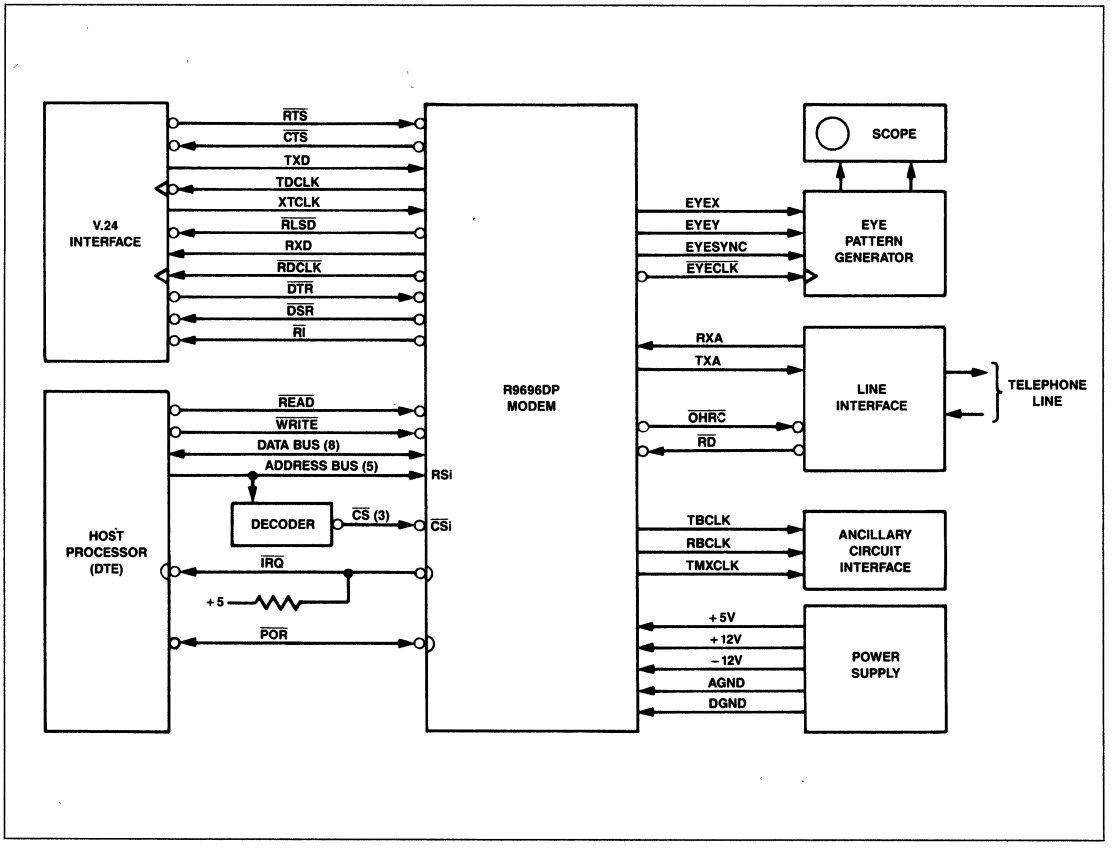


Figure 1. R9696DP Functional Interconnect Diagram

Table 3. R9696DP Hardware Interface Signals

Name	Type[1]	Pin No.[2]	Description
A. OVERHEAD:			
Ground (A)	AGND	30,31	Analog Ground Return
Ground (D)	DGND	29,37,53	Digital Ground Return
+5V	PWR	1,45,61	+5 Volt Supply
+12V	PWR	32	+12 Volt Supply
−12V	PWR	36	−12 Volt Supply
$\overline{POR}$	IA/OB	2	Power-On-Reset
B. MICROPROCESSOR INTERFACE:			
D7	IA/OB	3	Data Bus (8 Bits)
D6	IA/OB	4	
D5	IA/OB	5	
D4	IA/OB	6	
D3	IA/OB	7	
D2	IA/OB	8	
D1	IA/OB	9	
D0	IA/OB	10	
RS4	IA	15	Register Select (5 Bits)
RS3	IA	16	
RS2	IA	17	
RS1	IA	18	
RS0	IA	19	
$\overline{CS0}$	IA	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	13	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	14	Read Enable
$\overline{WRITE}$	IA	12	Write Enable
$\overline{IRQ}$	OC	11	Interrupt Request
C. V.24 INTERFACE:			
$\overline{RDCLK}$	OA	23	Receive Data Clock
TDCLK	OA	46	Transmit Data Clock
XTCLK	IA	51	External Transmit Clock
$\overline{RTS}$	IA	50	Request-to-Send
$\overline{CTS}$	OA	49	Clear-to-Send
TXD	IA	48	Transmitter Data
RXD	OA	26	Receiver Data
$\overline{RLSD}$	OA	27	Received Line Signal Detector
$\overline{DTR}$	IA	40	Data Terminal Ready
$\overline{DSR}$	OA	41	Data Set Ready
$\overline{RI}$	OA	25	Ring Indicator
D. ANCILLARY CIRCUITS:			
RBCLK	OA	22	Receiver Baud Clock
TBCLK	OA	47	Transmitter Baud Clock
TMXCLK	OA	43	Transmitter Mux Clock
E. LINE INTERFACE:			
TXA	AA	34	Transmitter Analog Output
RXA	AB	33	Receiver Analog Input
$\overline{OHRC}$	OD	35	Off-Hook Relay Control
$\overline{RD}$	IA	24	Ring Detect
F. DIAGNOSTIC:			
EYEX	OA	56	Eye Pattern Data—X Axis
EYEY	OA	55	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	57	Eye Pattern Clock
EYESYNC	OA	58	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 4 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. The following pins should be left open: 28, 39, 44, 52, 59 and 60.
3. The following pins are not used but should be connected to DGND through individual 10 KΩ series resistors: 38, 42 and 54.
4. Unused inputs tied to +5V or ground require individual 10 KΩ series resistors.

Table 4. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type				
			IA	OA	OB	OC	OD
V_{IH}	Input Voltage, High	V	2.0 Min.				
V_{IL}	Input Voltage, Low	V	0.8 Max.				
V_{OH}	Output Voltage, High	V		3.5 Min.[1]	3.5 Min.[1]		5.0 Max.
V_{OL}	Output Voltage, Low	V		0.4 Max.[2]	0.4 Max.[3]	0.4 Max.[2]	0.75 Typ.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.				
I_{OH}	Output Current, High	mA		−0.1 Max.	−0.1 Max		0[4]
I_{OL}	Output Current, Low	mA		1.6 Max.	0.8 Max.	1.6 Max.	15.0 Max.[5]
I_L	Output Current, Leakage	μA		±10 Max.	±10 Max.		
C_L	Capacitive Load	pF	5				
C_D	Capacitive Drive	pF		100	100	100	
	Circuit Type		TTL	TTL 3-state	TTL 3-state	Open-Drain	Open-Drain

Notes

1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = 0.8 mA
4. μA leakage
5. Can drive a +5V relay with coil resistance greater than 360Ω.

POWER-ON-RESET

When power is applied to the modem, the modem pulses Power-On-Reset ($\overline{POR}$) low to begin the POR sequence. The modem is ready to use 350 ms after the low-to-high transition of $\overline{POR}$. The POR sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 μs. $\overline{POR}$ is not pulsed low by the modem when the POR sequence is initiated externally. The POR sequence initializes the modem interface memory to default values (Table 8). This action leaves the modem configured as follows:

- V.32 9600 TCM
- Synchronous mode
- Originate mode
- Serial channel data
- T equalizer
- −43 dBm receiver threshold
- Transmitter compromise equalizer enabled
- Automatic rate change enabled
- Train-on-data disabled

NOTE: If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a POR sequence (i.e., < +3.5V), the host system should generate a $\overline{POR}$ signal upon supply voltage recovery to ensure proper modem initialization and operation.

MICROPROCESSOR INTERFACE

Nineteen address, data, control, and interrupt hardware interface signals allow modem connection to an 8086 compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000.

The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The significance of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

Data Lines (D0–D7)

Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.

Chip Selects ($\overline{CS0}$–$\overline{CS2}$) and Register Selects (RS0–RS4)

The three active low chip select lines ($\overline{CS0}$–$\overline{CS2}$) select one of three modem digital signal processor (DSP) devices. The five active high register select lines (RS0–RS4) address interface memory registers within the selected DSP interface memory. All eight of these lines are typically connected to the host bus address lines; the register select lines to the five least significant lines (A0–A4) and the chip select lines to the next two significant lines (A5–A6) through a decoder.

The selected DSP decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7 while the least significant data bit is D0.

Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

During a read cycle, data from the selected DSP interface memory register is gated onto the data bus by means of three-state drivers in each DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

The read/write cycle timing waveforms are illustrated in Figure 2 and the timing requirements are specified in Table 5.

Table 5. Microprocessor Interface Timing Parameters

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$i Setup Time	TCS	0	—	ns
RSi Setup Time	TRS	25	—	ns
Data Access Time	TDA	—	75	ns
Data Hold Time	TDHR	10	—	ns
Control Hold Time	THC	10	—	ns
Write Data Setup Time	TWDS	20	—	ns
Write Data Hold Time	TDHW	10	—	ns

Interrupt Request ($\overline{IRQ}$)

The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in the DSP interface memory to indicate immediate change of conditions in any of the three modem DSP devices. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.

The DSP $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). Each of the individual DSP $\overline{IRQ}$ output lines is wire-ORed to form the modem $\overline{IRQ}$ output signal. The modem $\overline{IRQ}$ output can also be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25W, is sufficient.

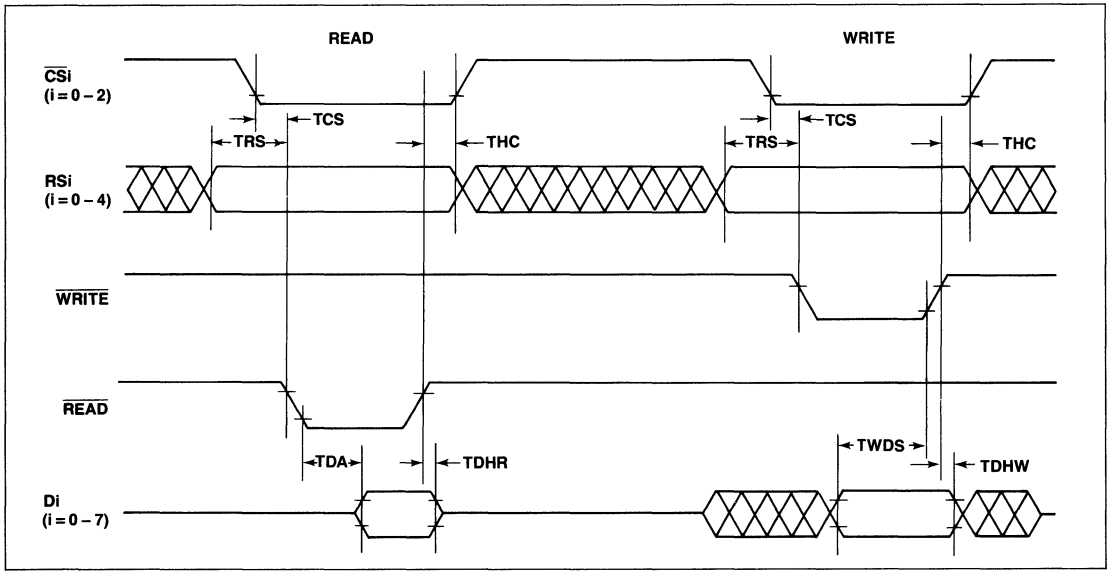


Figure 2. Microprocessor Interface Timing Waveforms

V.24 INTERFACE

Eleven pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels using 1489 receivers and 1488 drivers, or their equivalents.

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.

Received Data (RXD)

The modem presents received serial data to the local DTE on the Received Data (RXD) output.

Request To Send ($\overline{RTS}$)

Activating Request to Send ($\overline{RTS}$) causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The $\overline{RTS}$ pin is logically ORed with the RTS bit.

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) active indicates to the local DTE that the modem will transmit any data present on TXD. $\overline{CTS}$ response times from an active condition of $\overline{RTS}$ are shown in Table 2.

Received Line Signal Detector ($\overline{RLSD}$)

Received Line Signal Detector ($\overline{RLSD}$) active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence.

One of four $\overline{RLSD}$ receive level threshold options can be selected (Table 6). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than −43 dBm. The $\overline{RLSD}$ on and off thresholds are host programmable in DSP RAM.

Table 6. $\overline{RLSD}$ On and OFF Thresholds

Option	Receive Level	
	RLSD On	RLSD Off
0	> −43 dBm	< −48 dBm
1	> −33 dBm	< −38 dBm
2	> −26 dBm	< −31 dBm
3	> −16 dBm	< −21 dBm

Data Terminal Ready ($\overline{DTR}$)

In V.32, V.22 bis, V.22 and Bell 212A configurations, activating Data Terminal Ready ($\overline{DTR}$) initiates the handshake sequence, provided that the DATA0 bit is a 1. If in answer mode, the transmitter will immediately send answer tone.

In V.21, V.23 and Bell 103 configurations, activating $\overline{DTR}$ causes the modem to enter the data state provided that the DATA0 bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In these modes, if controlled carrier is enabled, carrier is controlled by Request-to-Send ($\overline{RTS}$).

During the data mode, deactivating $\overline{DTR}$ causes the transmitter to turn-off and return to the idle state.

The $\overline{DTR}$ input and the DTR control bit in chip 0 are logically ORed.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) ON indicates that the modem is in the data transfer state. The OFF condition of $\overline{DSR}$ indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{RI}$). $\overline{DSR}$ is OFF when the modem is in a test mode (i.e., local analog or remote digital loopback).

The DSR status bit in chip 0 reflects the state of the $\overline{DSR}$ output.

Ring Indicator ($\overline{RI}$)

The Ring Indicator ($\overline{RI}$) output follows the ringing signal present on the line with a low level (0V) during the ON time, and a high level (+5V) during the OFF time coincident with the ringing signal.

The RI status bit in chip 2 reflects the state of the $\overline{RI}$ output.

Transmit Data Clock (TDCLK)

The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%.

Transmit Data (TXD) must be stable during the one μs periods immediately preceding the rising edge of TDCLK and following the rising edge of TDCLK. The TDCLK source can be internal, external (input on XTCLK) or slave (to $\overline{RDCLK}$) as selected by bits in the transmitter interface memory.

External Transmit Clock (XTCLK)

In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.

Receive Data Clock ($\overline{RDCLK}$)

The modem outputs a synchronous Receive Data Clock ($\overline{RDCLK}$) for USRT timing. The $\overline{RDCLK}$ frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The $\overline{RDCLK}$ low-to-high transitions coincide with the center of the received data bits. The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK) outputs have no counterpart in the V.24 or RS-232-C recommendations since they mark the baud interval rather than the data rate for the transmitter and receiver, respectively. These baud clocks are useful in identifying the order of data bits in a baud (e.g., for multiplexing data). Both signals are active high. The first bit in each baud begins with the falling edge of the corresponding baud clock.

Transmitter Multiplexer Clock (TMXCLK)

The Transmitter Multiplexer Clock (TMXCLK) output is a 288 kHz clock which is internally divided down to create the Transmitter Baud Clock (TBCLK). TMXCLK is also a common multiple of all the possible transmitter data clocks. The high-to-low transitions of TDCLK coincide with the high-to-low transitions of TMXCLK.

LINE INTERFACE

The Transmitter Analog (TXA) output and Receiver Analog (RXA) input allow modem connection to either a leased line or the public switched telephone network (PSTN) through an audio transformer or a data access arrangement. The analog signal characteristics of TXA and RXA are described in Table 7.

Table 7. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 66.5K ohms.

Transmitter Analog (TXA)

The Transmitter Analog (TXA) output can drive an audio transformer or data access arrangement. TXA is a low impedance amplifier output in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

Receiver Analog (RXA)

The Receiver Analog (RXA) input can originate from an audio transformer or data access arrangement. The input impedance is nominally 66.5K ohms. The RXA input must be shunted by an external 604 ohm ±1% resistor in order to match a 600 ohm source.

The maximum received signal at RXA is 0 dBm. The maximum near-end echo at RXA that the modem can cancel in V.32 mode is −5 dBm.

Transient protection for TXA and RXA is recommended when interfacing directly to a transformer. This protection may take the form of back-to-back zener diodes or a varistor across the transformer.

Ring Detect ($\overline{RD}$)

The Ring Detect ($\overline{RD}$) input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving $\overline{RD}$ should be a 4N35 optoisolator or equivalent. The circuit driving $\overline{RD}$ should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING.

DATA2 bit must be set to a 0 to enable ring detection. Detected ring signals are reflected on the $\overline{RI}$ output.

Off-Hook Relay Control ($\overline{OHRC}$)

$\overline{OHRC}$ is an output designed to drive directly a +5V reed relay coil with a worst case resistance of 360 ohms having a must operate voltage of 4.0 Vdc. A clamp diode integrated in the modem eliminates the need for a diode across the relay coil. An

external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). $\overline{OHCR}$ is controlled by the host setting the RA bit in the interface memory.

Line Transformer Requirements for V.32

V.32 places high requirements upon the Data Access Arrangement (DAA) to the telephone line. V.32 uses the same bandwidth for transmission of data in both directions. Any non-linear distortion generated by the DAA in the transmit direction (known as near-end echo) cannot be canceled by the modem's echo canceller and interferes with data reception. The user must therefore ensure that the total harmonic distortion due to near-end echo at the RXA input to the R9696DP is at least 27 dB below the minimum level of received signal at the same point. Note that the major source of non-linear distortion in a DAA is the line transformer. When designing a DAA the user should take into account a worst case subscriber line, giving very poor matching to the DAA hybrid circuit and resulting in a large near-end echo (to simulate worst case conditions it is suggested that an 1800 ohm resistor in series with a 0.47 μF capacitor be used in place of the two wire telephone line).

DIAGNOSTIC SIGNALS

Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. Timing of these signals is illustrated in Figure 3.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

EYEX and EYEY outputs are 15-bit words, each with 8-bits of significance. The 15-bit data words are shifted out most significant bit first with the seven most significant bits equal to zero. EYEX and EYEY are clocked by the rising edge of $\overline{EYECLK}$.

$\overline{EYECLK}$

$\overline{EYECLK}$ is a clock for use by the serial-to-parallel converters. The $\overline{EYECLK}$ output is a 288 kHz clock which is internally divided down to create the Receiver Baud Clock (RBCLK). $\overline{EYECLK}$ is also a common multiple of all the possible receiver data clocks. The low-to-high transitions of $\overline{RDCLK}$ coincide with the low-to-high transitions of $\overline{EYECLK}$. $\overline{EYECLK}$, therefore, can be used as a receiver multiplexer clock.

EYESYNC

EYESYNC is a strobe for loading the D/A converters.

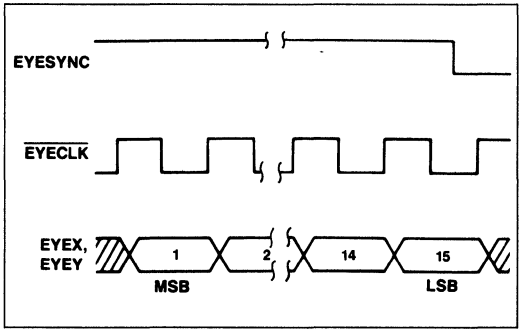


Figure 3. Eye Pattern Timing

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in three DSPs: transmitter device, receiver sample rate device, and receiver baud rate device.

INTERFACE MEMORY

Each DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in each DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus shared between the three DSPs.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAPS

Memory maps of the 96 addressable registers in the modem transmitter (chip 0), receiver sample rate (chip 1), and receiver baud rate (chip 2) devices are shown in Figure 4. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory.

INTERFACE MEMORY BIT DEFINITIONS

Table 8 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0,1 or 2), the register number by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

R9696DP DSP Interface Memory (Chip 0)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA0	NCIA0	—	NSIE0	NEWS0	NCIE0	—	NEWC0
1E	—	DBIA0	—	—	—	DBIE0	—	DBA0
1D	XACC0	—	—	—	—	XCRD0	XWT0	XCR0
1C	X RAM ADDRESS (XADD0)							
1B	YACC0	—	—	—	—	YCRD0	YWT0	YCR0
1A	Y RAM ADDRESS (YADD0)							
19	X RAM DATA MSB (XDAM0)							
18	X RAM DATA LSB (XDAL0)							
17	Y RAM DATA MSB (YDAM0)							
16	Y RAM DATA LSB (YDAL0)							
15	—	—	—	—	—	—	—	EARC0
14	—	—	—	—	—	—	—	—
13	TLVL				—	—	TXCLK	
12	TCONF							
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	—	—	CTS	DSR	—	TM	—	—
0E	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	HKAB0
0C	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	NV25	CC	DTMF	ORG	LL0	DATA0	—	DTR
08	ASYN0	TPDM	V21S0	—	—	—	RTRN	RTS
07	—	RDL	L2ACT	—	L3ACT	—	RA	MHLD
06	—	EXOS0	—	—	PEN0	STB0	WDSZ0	
05	ECFZ	ECSQ	FECSQ	TXSQ	CEQ	—	STOFF	TSPA
04	—	—	—	—	—	—	—	—
03	—	—	—	—	ARC0	SDIS	GTE	GTS
02	—	—	—	—	—	—	—	—
01	TSPY							
00	TBUFFER/TSPX							

(—) Indicates reserved for modem use only.

R9696DP DSP Interface Memory (Chip 1)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA1	NCIA1	—	NSIE1	NEWS1	NCIE1	—	NEWC1
1E	—	DBIA1	—	—	—	DBIE1	—	DBA1
1D	XACC1	—	—	—	—	XCRD1	XWT1	XCR1
1C	X RAM ADDRESS (XADD1)							
1B	YACC1	—	—	—	—	YCRD1	YWT1	YCR1
1A	Y RAM ADDRESS (YADD1)							
19	X RAM DATA MSB (XDAM1)							
18	X RAM DATA LSB (XDAL1)							
17	Y RAM DATA MSB (YDAM1)							
16	Y RAM DATA LSB (YDAL1)							
15	—	—	—	—	—	—	—	EARC1
14	ABCODE							
13	—	—	—	—	RTH		—	—
12	RCONF							
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	RLSD	FED	—	—	—	—	—	—
0E	RTDET	—	—	—	—	SPEED		
0D	—	—	S1DET	SCR1	U1DET	SADET	—	HKAB1
0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	—	RSEQ
0B	TONEA	TONEB	TONEC	ATV25	ATBEL	V21	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	—	—	LL1	DATA1	—	—
08	ASYN1	—	V21S1	—	—	—	—	—
07	RDLE	—	—	—	—	—	—	—
06	—	EXOS1	—	—	PEN1	STB1	WDSZ1	
05	—	—	—	—	CEQ23	—	—	—
04	—	—	—	—	—	—	—	—
03	—	—	—	RLSDE	ARC1	—	—	—
02	TDAE	SQDIS	—	—	—	—	—	—
01	RSEQM							
00	RBUFFER/RSEQL							

(—) Indicates reserved for modem use only.

R9696DP Interface Memory (Chip 2)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA2	—	—	NSIE2	NEWS2	—	—	—
1E		DBIA2	—	—	—	DBIE2	—	DBA2
1D	XACC2	—	—	—	—	XCRD2	XWT2	XCR2
1C	X RAM ADDRESS (XADD2)							
1B	YACC2	—	—	—	—	YCRD2	YWT2	YCR2
1A	Y RAM ADDRESS (YADD2)							
19	X RAM DATA MSB (XDAM2)							
18	X RAM DATA LSB (XDAL2)							
17	Y RAM DATA MSB (YDAM2)							
16	Y RAM DATA LSB (YDAL2)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	—	—	—	—	—	—	—	—
12	—	—	—	—	—	—	—	—
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	—	—	—	—	RI	—	—	—
0E	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	—	—	—	DATA2	—	—
08	—	—	—	DDIS	—	—	—	—
07	—	—	—	—	—	—	—	—
06	—	—	—	—	—	—	—	—
05	—	—	—	—	—	—	—	—
04	EQRES	EQT2	—	RSPA	EQFZ	IFIX	TOD	—
03	—	—	—	—	—	—	—	—
02	—	—	AMTD	—	—	—	—	—
01	RSPY							
00	RSPX							

(—) Indicates reserved for modem use only.

Figure 4. R9696DP DSP Interface Memory Map

Table 8. R9696DP Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
AADET	1:C:7	—	**AA Detector.** When set to a 1, status bit AADET indicates that a V.32 AA sequence has been detected. This bit is reset to a 0 by the modem at the start of the CC sequence. (V.32)
ABCODE	1:14:0–7	00	**Abort Code.** If the V.32 handshake fails, status bit HSKAB is set to a 1 and an abort code is written into ABCODE. This code indicates the point in the handshake where the failure occurred. The abort code is not cleared by the modem but should be cleared by the host after it has been read. The abort codes and their meanings are listed in the table below. Refer to CCITT Recommendation V.32 for meanings of the signal mnemonics used. (V.32) **Abort Code** — **Reason for Aborting** 00 — No failure. 01 — Failed to detect AC/CA transition (calling). Failed to detect AA/CC transition (answering). 02 — Failed to detect CA/AC transition (calling). 03 — Not used. 04 — Timed out waiting for signal at the start of the S sequence. 05 — Failed to detect S sequence. 06 — Not used. 07 — Failed to detect Rate sequence (R1, R2 or R3). 08 — Failed to detect S/$\overline{S}$ transition. 09 — Failed to detect E sequence. 0A — Power loss during TRN or Rate sequence.
ACDET	1:C:6	—	**AC Detector.** When set to a 1, status bit ACDET indicates that a V.32 AC sequence has been detected. This bit is reset to a 0 by the modem when a CA sequence or an energy dropout is detected. (V.32)
AMTD	2:2:5	1	**Amplitude Modulation Tracker Disable.** When control bit AMTD is a 0, an adaptive amplitude modulation tracker is enabled in the receiver; when a 1, the tracker is disabled. (V.32, V.22 bis, V.22, Bell 212A)
ARC0	0:3:3	1	**Automatic Rate Change Enable Chip 0.** When control bits ARC0 and ARC1 are a 1, the modem will automatically condition itself to transmit data at the highest common rate negotiated during the V.32 handshake. The host may specify the undefined bits in the rate sequence in DSP RAM. When ARC0 and ARC1 are a 0, the modem cannot change from the rate it is configured to before beginning the handshake. However, it is possible for the host to interact with the rate sequences during the handshake and then set the transmitter configuration as desired. (See EARC0.) (V.32) When control bit ARC0 and ARC1 are a 1, then setting the RTRN bit will cause the modem to send a rate change sequence, rather than the normal retrain sequence. (V.22 bis) (See RTRN.)
ARC1	1:3:3	1	**Automatic Rate Change Enable Chip 1.** See ARC0 and EARC0.
ASYN0	0:8:7	0	**Asynchronous/Synchronous.** When configuration bit ASYN0 is a 1, asynchronous mode is selected in the transmitter; when 0, synchronous mode is selected. When the ASYN0 bit changes from 0 to 1, the transmitter's asynchronous to synchronous converter is configured according to the EXOS0, PEN0, STB0 and WDSZ0 bits at that time. (EXOS0, PEN0, STB0 and WDSZ0 must be configured before ASYN0 changes from a 0 to a 1.) ASYN0 may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. Do not set this bit in V.21, V.23 or Bell 103 modes. Asynchronous operation is not available in V.32 12000 bps. (V.32, V.22 bis, V.22, Bell 212A)
ASYN1	1:8:7	0	**Asynchronous/Synchronous.** When configuration bit ASYN1 is a 1, asynchronous mode is selected in the receiver; when 0, synchronous mode is selected. When the ASYN1 bit changes from 0 to 1, the receiver's synchronous to asynchronous converter is configured according to the EXOS1, PEN1, STB1 and WDSZ1 bits at that time. (EXOS1, PEN1, STB1 and WDSZ1 must be configured before ASYN1 changes from a 0 to a 1.) ASYN1 may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. Do not set this bit in V.21, V.23 or Bell 103 modes. Asynchronous operation is not available in V.32 12000 bps. (V.32, V.22 bis, V.22, Bell 212A)
ATBEL	1:B:3	—	**Bell Answer Tone Detector.** When set to a 1, status bit ATBEL signifies that the modem receiver detected a 2225 Hz answer tone. The bit is set to a 1 when the answer tone is detected, and is cleared to a 0 when the tone ends. ATBEL is only active when the DATA1 bit is a 0 and the modem is in originate mode. (Bell 212A, Bell 103)
ATV25	1:B:4	—	**V25 Answer Tone Detector.** When set to a 1, status bit ATV25 signifies that the modem receiver detected a 2100 Hz answer tone. The bit is set to a 1 when the answer tone is detected, and is cleared to a 0 when the tone ends. ATV25 is only active when the DATA1 bit is a 0 and the modem is in originate mode. (V.32, V.22 bis, V.22, V.23, V.21)

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
CADET	1:C:5	—	**CA Detector.** When set to a 1, status bit CADET indicates that a V.32 CA sequence has been detected. This bit is reset to a 0 by the modem when a AC sequence is detected. (V.32)
CC	0:9:6	0	**Controlled Carrier.** When control bit CC is a 1, the modem operates in controlled carrier; when 0, the modem operates in constant carrier. Controlled carrier allows the modem transmitter to be controlled by the $\overline{RTS}$ pin or the RTS bit (see Table 2). In V.22 bis and V.22 controlled carrier, when the $\overline{RTS}$ pin goes to a 0, or the RTS bit set to a 1, the transmitter immediately sends scrambled ones for 270 ms and then turns on the $\overline{CTS}$ signal and the CTS bit. At 2400 bps, it is recommended that a retrain be sent once in the data mode to ensure that synchronization occurs. (V.22 bis, V22, V.21, V.23, Bell 103)
CCDET	1:C:4	—	**CC Detector.** When set to a 1, status bit CCDET indicates that a V.32 CC sequence has been detected. This bit is reset to a 0 by the modem when an energy dropout is detected. (V.32)
CEQ	0:5:3	1	**Compromise Equalizer Enable.** When control bit CEQ is a 1, the transmitter's digital compromise equalizer is inserted into the transmit path. This bandpass equalizer has host programmable taps in DSP RAM. CEQ should be a 0 during local analog loopback.
CEQ23	1:5:3	0	**V.23 Compromise Equalizer Enable.** When control bit CEQ23 is a 1, the receiver's digital compromise equalizer is inserted into the receive path. This equalizer can only be enabled in V.23 1200 and 600 configurations. This bandpass equalizer has host programmable taps in DSP RAM. (V.23)
CTS	0:F:5	—	**Clear To Send.** When set to a 1, status bit CTS indicates to the DTE that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 2. The CTS OFF-to-ON response time is programmable in DSP RAM.
DATA0	0:9:2	1	**Data Chip 0.** When control bit DATA0 is a 0, the transmitter is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering.
DATA1	1:9:2	1	**Data Chip 1.** When control bit DATA1 is a 0, the receiver is prevented from entering and proceeding with the handshake (start-up) sequence. If in originate mode, the answer tone detector is still active. Also, in V.32 the AC detector is active. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering. Recommended procedure for originating a call in V.32 using DATA1: Reset DATA1 and DTR to a 0 Establish a call Detect answer tone using ATV25 After receiving answer tone for 1 second, set DTR to a 1 When ATV25 equals 0 AND ACDET equals 1, set DATA1 to a 1 The handshake will now proceed
DATA2	2:9:2	1	**Data Chip 2.** When control bit DATA2 is a 0, the ringing detector is enabled, and when a 1, the ringing detector is disabled. This bit should be set to a 1 after the modem goes off-hook, otherwise the $\overline{RI}$ signal and RI bit will give spurious outputs.
DBA0	0:1E:0	—	**Data Buffer Available Chip 0.** When set to a 1, status bit DBA0 signifies that the transmitter has read register 0:0 (TBUFFER), or registers 0:1 (TSPY) and 0:0 (TSPX), and the host can write new data into register 0:0, or registers 0:1 and 0:0. This condition can also cause $\overline{IRQ}$ to be asserted. The host writing to register 0:0 resets the DBA0 and DBIA0 bits to 0. (See DBIE0 and DBIA0.)
DBA1	1:1E:0	—	**Data Buffer Available Chip 1.** When set to a 1, status bit DBA1 signifies that the receiver wrote valid data into register 1:0 (RBUFFER), or registers 1:1 (RSEQM) and 1:0 (RSEQL). This condition can also cause $\overline{IRQ}$ to be asserted. The host reading register 1:0 resets the DBA1 and DBIA1 bits to 0. (See DBIE1 and DBIA1.)
DBA2	2:1E:0	—	**Data Buffer Available Chip 2.** When set to a 1, status bit DBA2 signifies that the receiver wrote valid data into registers 2:1 (RSPY) and 2:0 (RSPX). This condition can also cause $\overline{IRQ}$ to be asserted. The host reading register 2:0 resets the DBA2 and DBIA2 bits to 0. (See DBIE2 and DBIA2.)

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
DBIA0	0:1E:6	—	**Data Buffer Interrupt Active Chip 0.** When the transmitter data buffer interrupt is enabled (DBIE0 is a 1) and register 0:0 is empty (DBA0 is set to a 1), the transmitter asserts $\overline{IRQ}$ and sets status bit DBIA0 to a 1 to indicate that DBA0 going to a 1 caused the interrupt. The host writing to register 0:0 resets the DBIA0 bit to a 0 and clears the interrupt request due to DBA0. (See DBIE0 and DBA0.)
DBIA1	1:1E:6	—	**Data Buffer Interrupt Active Chip 1.** When the receiver chip 1 data buffer interrupt is enabled (DBIE1 is a 1) and register 1:0 is written to by the DSP (DBA1 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets DBIA1 to a 1 to indicate that DBA1 going to a 1 caused the interrupt. The host reading register 1:0 resets the DBIA1 bit to a 0 and clears the interrupt request due to DBA1. (See DBA1 and DBIE1.)
DBIA2	2:1E:6	—	**Data Buffer Interrupt Active Chip 2.** When the receiver chip 2 data buffer interrupt is enabled (DBIE2 is a 1) and register 2:0 is written to by the DSP (DBA2 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets DBIA2 to a 1 to indicate that DBA2 going to a 1 caused the interrupt. The host reading register 2:0 resets the DBIA2 bit to a 0 and clears the interrupt request due to DBA2. (See DBA2 and DBIE2.)
DBIE0	0:1E:2	0	**Data Buffer Interrupt Enable Chip 0.** When control bit DBIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set the DBIA0 bit to a 1 when DBA0 is set to 1 by the DSP. When DBIE0 is a 0 (interrupt disabled), DBA0 has no effect on $\overline{IRQ}$ or DBIA0. (See DBA0 and DBIA0.)
DBIE1	1:1E:2	0	**Data Buffer Interrupt Enable Chip 1.** When control bit DBIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set the DBIA1 bit to a 1 when DBA1 is set to a 1 by the DSP. When DBIE1 is a 0 (interrupt disabled), DBA1 has no effect on $\overline{IRQ}$ or DBIA1. (See DBA1 and DBIA1.)
DBIE2	2:1E:2	0	**Data Buffer Interrupt Enable Chip 2.** When control bit DBIE2 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set the DBIA2 bit to a 1 when DBA2 is set to a 1 by the DSP. When DBIE2 is a 0 (interrupt disabled), DBA2 has no effect on $\overline{IRQ}$ or DBIA2. (See DBA2 and DBIA2.)
DDIS	2:8:4	0	**Descrambler Disable.** When control bit DDIS is a 1, the receiver's descrambler circuit is disabled; when a 0, the descrambler circuit is enabled.
DSR	0:F:4	—	**Data Set Ready.** When set to a 1 (ON), status bit DSR indicates that the modem is in the data transfer state. When reset to a 0 (OFF), DSR indicates that the DTE is to disregard all signals appearing on the interchange circuits—except $\overline{RI}$. DSR will switch to the OFF state when the modem is in a test mode.
DTMF	0:9:5	0	**DTMF Select.** When the modem is configured for dialing mode, the modem will dial using DTMF tones or pulses. When control bit DTMF is a 1, the modem will dial using DTMF tones. When DTMF is a 0, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. Dialing mode is selected by configuration code 81 in the Transmitter Configuration Register (TCONF). When in dialing mode, the data placed in the Transmitter Data Register is treated as digits to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the Transmitter Data Register). Also, see DBA0 bit. Dialing timing and power levels are host programmable in DSP RAM (Table 11).
DTR	0:9:0	0	**Data Terminal Ready.** In V.32, V.22 bis, V.22 and Bell 212A modes, setting control bit DTR to a 1 initiates a handshake sequence, providing DATA0 bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In V.21, V.23 and Bell 103 modes, control bit DTR must be a 1 for the modem to enter data state providing DATA0 bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In these configurations, if controlled carrier is selected, then carrier is controlled by the $\overline{RTS}$ pin or bit (see Table 2). During the data mode, setting DTR to a 0 will cause the transmitter to turn off. The DTR bit parallels the operation of the hardware $\overline{DTR}$ control input. These inputs are ORed by the modem.
EARC0	0:15:0	0	**Extended Automatic Rate Change Chip 0.** When control bits EARC0 and EARC1 are 1 (and also ARC0 and ARC1 are 1), then rate changes to the proprietary 12000 and 7200 TCM configurations are allowed during the V.32 handshake. The modem will condition itself to transmit data at the highest common rate negotiated during the V.32 handshake. These rates include the proprietary 12000 and 7200 TCM configurations, if both calling and answering modems support these configurations. When EARC0 and EARC1 are 0 then rate changes are only allowed to standard CCITT V.32 configurations.

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
			There are two methods for operating in the proprietary 12000 and 7200 TCM configurations. The first is to set bits ARC0, ARC1, EARC0 and EARC1 all to 0. TCONF and RCONF should then be set for the required configuration. The modem will then only be able to connect in the configuration selected. Both calling and answering modems have to be configured the same way for a successful connection. The second method is to set bits ARC0, ARC1, EARC0 and EARC1 all to 1. TCONF and RCONF should be set as desired, but in this case rate negotiation takes place during the V.32 handshake. Use of this method allows fall-back or fall-forward retrains in 2400 bps steps from 12000 bps to 4800 bps. In order to accomplish rate changes to the proprietary configurations, the modem uses two bits in the V.32 16 bit rate sequence that are undefined in CCITT Recommendation V.32. These are bits B9 and B10. (V.32)
EARC1	1:15:1	0	**Extended Automatic Rate Change Chip 1.** See EARC0. (V.32)
ECFZ	0:5:7	0	**Echo Canceller Freeze.** When control bit ECFZ is a 1, the updating of the echo canceller taps is inhibited. (V.32)
ECSQ	0:5:6	0	**Echo Canceller Squelch.** When control bit ECSQ is a 1, the echo canceller output is forced to zero. (V.32) ECSQ, along with TXSQ, can be used to determine if the line has been dropped by the remote modem. Many times due to the dropping of the line by the remote modem, a line mismatch occurs at the near end modem's line interface. This causes a large increase in near end echo. Many errors should be seen at this time. If this is the case, squelching both the echo canceller and the transmitter should cause RLSD to go inactive. The host should first freeze the echo canceller (this is done in case the line is not dropped) by setting ECFZ to a 1. Then set both ECSQ and TXSQ to a 1. If RLSD drops, then the line was dropped by the remote modem and the near end modem should then be disconnected from the line by the host. If RLSD does not drop, then the host should reset ECFZ, ECSQ, and TXSQ to a 0 and issue a retrain, if applicable.
EQFZ	2:4:3	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited. (V.32, V.22 bis, V.22, Bell 212A)
EQRES	2:4:7	0	**Equalizer Reset.** When control bit EQRES is a 1, the receiver resets all of the adaptive equalizer's taps to zero. When EQRES is a 0, the equalizer taps are updated normally by the receiver (chip 2). (V.32, V.22 bis, V.22, Bell 212A) Setting EQRES to a 1 effectively clamps the receiver. EQRES along with RLSDE can be used to clamp the receiver off and turn off the $\overline{\text{RLSD}}$ pin. An equalizer reset is automatically done for a brief period of time at the beginning of the train-on-data state (TOD = 1). Therefore, the host does not have to manually set then clear this bit to reset the equalizer for line hits, etc., when TOD is active.
EQT2	2:4:6	0	**Equalizer T/2 Spacing Select.** When control bit EQT2 is a 1, the receiver's adaptive equalizer is T/2 fractionally spaced. When EQT2 is a 0, the equalizer is T spaced (T = 1 baud time). (V.32)
EXOS0	0:6:6	0	**Extended Overspeed Chip 0.** When control bit EXOS0 is a 1, Extended Overspeed mode is selected in the transmitter async-to-sync converter. This bit must be configured appropriately before the ASYN0 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis, V.22, Bell 212A)
EXOS1	1:6:6	0	**Extended Overspeed Chip 1.** When control bit EXOS1 is a 1, Extended Overspeed mode is selected in the receiver sync-to-async converter. This bit must be configured appropriately before the ASYN1 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis, V.22, Bell 212A)
FECSQ	0:5:5	0	**Far Echo Canceller Squelch.** When control bit FECSQ is a 1, the output of the far-end echo canceller is forced to zero; the near-end echo canceller continues to operate normally. (V.32) Squelching the far end echo canceller should only be done for testing purposes to manually characterize the far end echo.
FED	1:F:6	—	**Fast Energy Detector.** When status bit FED is a 1, energy in the passband above the selected receiver threshold has been detected (see RTH).
GTE	0:3:1	0	**Guard Tone Enable.** When set to a 1, control bit GTE causes the specified guard tone to be transmitted (CCITT configurations only), according to the state of the GTS bit. Note: The guard tone will only be transmitted by the answering modem. (V.22 bis)
GTS	0:3:0	0	**Guard Tone Select.** When set to a 1, control bit GTS selects the 550 Hz tone; when reset to a 0, GTE selects the 1800 Hz tone. The selected guard tone will be transmitted only when GTE is enabled. (V.22 bis)
HKAB0	0:D:0	—	**Handshake Abort Chip 0.** When set to a 1 status bit HKAB0 indicates that the V.32 handshake has failed. The transmitter remains in an abort state for 1 second after which HKAB0 is reset to 0 and the transmitter returns to idle mode. While in the abort state the transmitter output is silent. Normally this bit is set shortly after the HKAB1 bit with one exception. When the calling modem receives rate sequence R3 (refer to CCITT Recommendation V.32) and ARC0 is set to a 1, then if no common rates are found or R3 is calling for a GSTN cleardown then HKAB0 will be set before HKAB1. (V.32)

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
HKAB1	1:D:0	—	**Handshake Abort Chip 1.** When set to a 1, status bit HKAB1 indicates that the V.32 handshake has failed. At the same time an abort code is written into ABCODE (see ABCODE). The receiver remains in an abort state for 0.5 second after which HKAB1 is reset to 0 and the receiver returns to idle mode. (V.32)
IFIX	2:4:2	1	**Eye Fix.** When control bit IFIX is a 1, the serial diagnostic data at the EYEX and EYEY pins reflects the Rotated Equalizer Output. When IFIX is a 0, the data on EYEX and EYEY is selected by the addresses in X RAM ADDRESS and Y RAM ADDRESS registers in chip 2, respectively.
LL0	0:9:3	0	**Leased Line Chip 0.** When control bit LL0 is a 1, the transmitter is in leased line operation; when 0, the transmitter is in switched line operation. When LL0 is set to a 1 and the CC bit is a 0, the modem immediately sends scrambled ones and goes into data mode. (V.22 bis, V.22) At 2400 bps it is recommended that a retrain be sent once in the data state to ensure that synchronization occurs.
LL1	1:9:3	0	**Leased Line Chip 1.** When control bit LL1 is a 1, the receiver is in leased line operation; when 0, the receiver is in switched line operation. (V.22 bis, V.22)
L2ACT	0:7:5	0	**Loop 2 Activate.** When control bit L2ACT is a 1, the receiver's digital output is connected to the transmitter's digital input (locally activated remote digital loopback) in accordance with CCITT Recommendation V.54.
L3ACT	0:7:3	0	**Loop 3 Activate.** When control bit L3ACT is a 1, the transmitter's analog output is coupled to the receiver's analog input through an attenuator (local analog loopback) in accordance with CCITT Recommendation V.54. The modem may only be placed into analog loopback mode when in idle mode ($\overline{DTR}$ signal is OFF and the DTR bit is 0). NEWC0 and NEWC1 must be set after any change in the L3ACT bit. Set NEWC0 to a 1 and wait until the modem resets it to a 0. Wait 2 ms. Set the NEWC1 bit to a 1 and wait for the modem to reset it to a 0. The loopback is then completed (terminated) by setting the $\overline{DTR}$ signal ON (OFF) or the DTR bit to a 1 (0). The transmitter's compromise equalizer should be disabled, by setting CEQ to a 0, during local analog loopback.
MHLD	0:7:0	0	**Mark Hold.** When control bit MHLD is a 1, the transmitter's digital input data is clamped to a mark. When MHLD is a 0, the transmitter's input is taken from TXD or TBUFFER (see TPDM).
NCIA0	0:1F:6	—	**NEWC0 Interrupt Active.** When the new configuration chip 0 interrupt is enabled (NCIE0 is a 1) and a new transmitter configuration is implemented (NEWC0 is reset to a 0), the DSP asserts $\overline{IRQ}$ and sets status bit NCIA0 to a 1 to indicate that NEWC0 going to a 0 caused the interrupt. NCIA0 and the interrupt request due to NEWC0 are cleared by the host writing a 0 into NCIE0. (See NEWC0 and NCIE0.)
NCIA1	1:1F:6	—	**NEWC1 Interrupt Active.** When the new configuration chip 1 interrupt is enabled (NCIE1 is a 1) and a new receiver configuration is implemented (NEWC1 is reset to a 0), the DSP asserts $\overline{IRQ}$ and sets status bit NCIA1 to a 1 to indicate that NEWC1 going to a 0 caused the interrupt. NCIA1 and the interrupt request due to NEWC1 are cleared by the host writing a 0 into NCIE1. (See NEWC1 and NCIE1.)
NCIE0	0:1F:2	0	**NEWC0 Interrupt Enable.** When control bit NCIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set NCIA0 to a 1 when the NEWC0 bit is reset to a 0 by the DSP. When NCIE0 is a 0 (interrupt disabled), NEWC0 has no effect on $\overline{IRQ}$ or NCIA0. (See NEWC0 and NCIA0.)
NCIE1	1:1F:2	0	**NEWC1 Interrupt Enable.** When control bit NCIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA1 to a 1 when the NEWC1 bit is reset to a 0 by the DSP. When NCIE1 is a 0 (interrupt disabled), NEWC1 has no effect on $\overline{IRQ}$ or NCIA1. (See NEWC1 and NCIA1.)
NEWC0	0:1F:0	0	**New Configuration Chip 0.** Control bit NEWC0 must be set to a 1 by the host after the host changes the configuration code in TCONF (0:12), the L3ACT bit (0:7:3), the ORG bit (0:9:4) or the V21S0 bit (0:8:5). This informs the transmitter to implement the new transmitter configuration. The DSP resets the NEWC0 bit to a 0 when the configuration change is implemented. A configuration change can also cause $\overline{IRQ}$ to be asserted. (See NCIE0 and NCIA0.)
NEWC1	1:1F:0	0	**New Configuration Chip 1.** Control bit NEWC1 must be set to a 1 by the host after the host changes the configuration code in RCONF (1:12), the L3ACT bit (0:7:3), RTH (1:13:2-3), the ORG bit (0:9:4) or the V21S1 bit (1:8:5). This informs the receiver to implement the new receiver configuration and/or the new receiver threshold. The DSP resets the NEWC1 bit to a 0 when the change is implemented. A configuration/receiver threshold change can also cause $\overline{IRQ}$ to be asserted. (See NCIE1 and NCIA1.)
NEWS0	0:1F:3	—	**New Status Chip 0.** When set to a 1, status bit NEWS0 indicates that one or more status bits located in registers 0E or 0F have changed state, or a DSP RAM read or write has been completed, in the transmitter. This bit can be reset to a 0 only by the host. The host may mask the effect of individual status bits upon NEWS0 by writing a mask value to DSP RAM. When set to a 1, this bit can cause $\overline{IRQ}$ to be asserted. (See NSIE0 and NSIA0.)
NEWS1	1:1F:3	—	**New Status Chip 1.** When set to a 1, status bit NEWS1 indicates that one or more status bits located in registers 0A to 0F have changed state, or a DSP RAM read or write has been completed, in receiver DSP chip 1. This bit can be reset to a 0 only by the host. The host may mask the effect of individual status bits upon NEWS1 by writing a mask value to DSP RAM. When set to a 1, this bit can cause $\overline{IRQ}$ to be asserted. (See NSIE1 and NSIA1.)

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
NEWS2	2:1F:3	—	**New Status Chip 2.** When set to a 1, status bit NEWS2 indicates that the RI status bit in register 0F has changed state, or a DSP RAM read or write has been completed, in receiver DSP chip 2 This bit can be reset to a 0 only by the host. The host may mask the effect of the RI status bit upon NEWS2 by writing a mask value to DSP RAM. When set to a 1, this bit can cause $\overline{IRQ}$ to be asserted. (See NSIE2 and NSIA2.)
NSIA0	0:1F:7	—	**NEWS0 Interrupt Active Chip 0.** When the new status interrupt chip 0 is enabled (NSIE0 is a 1) and a change of status occurs (NEWS0 is set to a 1), the transmitter asserts $\overline{IRQ}$ and sets status bit NSIA0 to a 1 to indicate that NEWS0 going to a 1 caused the interrupt. NSIA0 and the interrupt request due to NEWS0 are cleared when the host writes a 0 to NEWS0. (See NEWS0 and NSIE0.)
NSIA1	1:1F:7	—	**NEWS1 Interrupt Active Chip 1.** When the new status interrupt chip 1 is enabled (NSIE1 is a 1) and a change a status occurs (NEWS1 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets status bit NSIA1 to a 1 to indicate that NEWS1 going to a 1 caused the interrupt. NSIA1 and the interrupt request due to NEWS1 are cleared when the host writes a 0 to NEWS1. (See NEWS1 and NSIE1.)
NSIA2	2:1F:7	—	**NEWS2 Interrupt Active Chip 2.** When the new status interrupt chip 2 is enabled (NSIE2 is a 1) and a change of status occurs (NEWS2 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets status bit NSIA2 to a 1 to indicate that NEWS2 going to a 1 caused the interrupt. NSIA2 and the interrupt request due to NEWS2 are cleared when the host writes a 0 to NEWS2. (See NEWS2 and NSIE2.)
NSIE0	0:1F:4	0	**NEWS0 Interrupt Enable Chip 0.** When control bit NSIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set NSIA0 to a 1 when NEWS0 is set to a 1 by the DSP. When NSIE0 is a 0 (interrupt disabled), NEWS0 has no effect on $\overline{IRQ}$ or NSIA0. (See NEWS0 and NSIA0.)
NSIE1	1:1F:4	0	**NEWS1 Interrupt Enable Chip 1.** When control bit NSIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA1 to a 1 when NEWS1 is set to a 1 by the DSP. When NSIE1 is a 0 (interrupt disabled), NEWS1 has no effect on $\overline{IRQ}$ or NSIA1. (See NEWS1 and NSIA1.)
NSIE2	2:1F:4	0	**NEWS2 Interrupt Enable Chip 2.** When control bit NSIE2 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA2 to a 1 when NEWS2 is set to a 1 by the DSP. When NSIE2 is a 0 (interrupt disabled), NEWS2 has no effect on $\overline{IRQ}$ or NSIA2. (See NEWS2 and NSIA2.)
NV25	0:9:7	0	**No V.25 Answer Tone.** When control bit NV25 is a 1, the modem will not transmit the 2100 Hz CCITT answer tone when a handshake sequence is initiated and the modem is in answer mode. (V.32, V.22 bis, V.22, V.21, V.23)
ORG	0:9:4	1	**Originate.** When configuration bit ORG is a 1, the modem is in originate mode; when a 0, the modem is in answer mode. Since this is a configuration bit, the NEWC0 and NEWC1 bits must be set after any change in the ORG bit. Set NEWC0 to a 1 and wait until the modem resets it to a 0. Wait 2 ms. Set the NEWC1 bit to a 1 and wait for the modem to reset it to a 0.
PEN0	0:6:3	0	**Parity Enable Chip 0.** When control bit PEN0 is a 1, parity is enabled in asynchronous mode in the transmitter. This bit must be configured appropriately before the ASYN0 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis, V.22, Bell 212A)
PEN1	1:6:3	0	**Parity Enable Chip 1.** When control bit PEN1 is a 1, parity is enabled in asynchronous mode in the receiver. This bit must be configured appropriately before the ASYN1 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis, V.22, Bell 212A)
RA	0:7:1	0	**Relay Activate.** When control bit RA is a 1, the output $\overline{OHRC}$ is activated (low); when a 0, the $\overline{OHRC}$ output is off (high).
RBUFFER	1:0:0–7	—	**Receive Buffer.** The host obtains channel data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER. The data is divided on the baud boundaries shown under TBUFFER. The RBUFFER reflects the received data when the RSEQ bit is a 0.
RCONF	1:12:0–7	74	**Receiver Configuration.** The RCONF control bits select one of the following receiver configurations:

Mode	Data Rate	RCONF (Hex)
V.32 TCM	12000	72
V.32 TCM	9600	74
V.32	9600	75
V.32	4800	71
V.32 TCM	7200	78
V.22 bis	2400	84
V.22	1200	52
V.22	600	51
V.21	0–300	A0
Bell 212A	1200	62
Bell 103	0–300	60
V.23	1200	A4
V.23	600	A2
V.23	75	A1

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
RDL	0:7:6	0	**Remote Digital Loopback.** When set to a 1, control bit RDL causes the modem to initiate a request for the modem to go into digital loopback; RXD is clamped to a mark and the CTS bit and $\overline{CTS}$ signal will be reset until the loop is established. The TM bit is not set in this case, since the local modem initiated the request. (V.22 bis)
RDLE	1:7:7	1	**Remote Digital Loopback Response Enable.** When set to a 1, control bit RDLE enables the modem to respond to another modem's remote digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS, DSR and RLSD bits to a 0, and turns the $\overline{CTS}$, $\overline{DSR}$ and $\overline{RLSD}$ signals to a logic 1. The TM bit is set to a 1, to inform the host of the test status. When the RDLE bit is a 0, no response will be generated. (V.22 bis)
RI	2:F:3	—	**Ring Indicator.** When set to a 1, status bit RI indicates that a ringing signal is being detected. Ringing is detected if pulses are present on the $\overline{RD}$ input in the 15 Hz – 68 Hz frequency range. The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with $\overline{RI}$ output signal. The decision bounds are host programmable in DSP RAM. The bit is valid only when the receiver DATA2 bit (2:9:2) is a 0.
RLSD	1:F:7	—	**Received Line Signal Detector.** When status bit RLSD is a 1, the receiver has finished receiving the training sequence or has turned on due to detected energy above threshold, and is receiving data. RLSD is a 0 when the receiver is in the idle state and during the reception of a training sequence.
RLSDE	1:3:4	1	**RLSD Enable.** When control bit RLSDE is a 1, the $\overline{RLSD}$ pin reflects the RLSD bit. When RLSDE is a 0, the $\overline{RLSD}$ pin is clamped to a 1 (OFF condition) regardless of the state of the RLSD bit. (V.22 bis)
RSEQ	1:C:0	0	**Rate Sequence Received.** When status bit RSEQ is a 1, the 16-bit rate sequence included in the CCITT V.32 start-up procedure has been received and the 16-bit rate sequence word is available in RSEQM (1:1) and RSEQL (1:0). (V.32)
RSEQL	1:0:0–7	—	**Rate Sequence LSB.** When the RSEQ bit is a 1, register 1:0 holds the least significant byte of the 16-bit V.32 rate sequence word (RSEQL) received by the modem. When the RSEQ bit is a 0, register 1:0 holds the received data (see RBUFFER). (V.32)
RSEQM	1:1:0–7	—	**Rate Sequence MSB.** When the RSEQ bit is a 1, register 1:1 holds the most significant byte of the 16-bit V.32 rate sequence word (RSEQM) received by the modem. When the RSEQ bit is a 0, register 1:1 is not used. (V.32)
RSPA	2:4:4	1	**Receiver Signal Point Activate.** When control bit RSPA is a 1, the receiver writes the received signal point coordinates, after the decision processing, into registers RSPY (2:1) and RSPX (2:0). When RSPA is a 0, RSPY and RSPX do not contain the signal point coordinates. (V.32, V.22 bis, V.22, Bell 212A)
RSPX	2:0:0–7	—	**Receiver Signal Point X.** RSPX holds the X (in-phase) coordinate of the received signal point. RSPX is valid only when RSPA is a 1. (See RSPA.) (V.32, V.22 bis, V.22, Bell 212A)
RSPY	2:1:0–7	—	**Receiver Signal Point Y.** RSPY holds the Y (quadrature) coordinate of the received signal point. RSPY is valid only when RSPA is a 1. (See RSPA.) (V.32, V.22 bis, V.22, Bell 212A)
RTDET	1:E:7	—	**Retrain Detector.** When set to a 1, status bit RTDET indicates that a training sequence has been detected. (V.32 and V.22 bis) This bit parallels the operation of the following: **Mode** / **Detector Bit** V.32 Originate — ACDET V.32 Answer — AADET V.22 bis — S1DET
RTH	1:13:2,3	0	**Receiver Threshold.** The RTH control bits select the receiver energy detector threshold according to the following codes: **RTH** / **RLSD ON** / **RLSD OFF** 0 / –43 dBm / –48 dBm 1 / –33 dBm / –38 dBm 2 / –26 dBm / –31 dBm 3 / –16 dBm / –21 dBm

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
RTRN	0:8:1	0	**Retrain.** When the modem is in V.32 or V.22 bis data mode, and control bit RTRN is set to a 1, a retrain sequence is initiated. RTRN resets to a 0 as soon as the initiation is acknowledged. Fall-back or fall-forward retrains may be accomplished as follows: Change the Transmitter Configuration Register (TCONF) to the required configuration code. Note that the mode cannot be changed, only the data rate within a given mode. (In other words, it is not possible to fall-back from V.32 to V.22 bis.) **Do not** set the NEWC bits in either the transmitter (NEWC0) or receiver chip 1 (NEWC1) and do not change the receiver configuration register (RCONF) code. Ensure that ARC0 and ARC1 bits are set to a 1. If it is desired to fall-back or fall-forward to one of the proprietary V.32 configurations, then also ensure that EARC0 and EARC1 are set to a 1. Finally, set the RTRN bit to a 1. If the remote modem can operate at the requested rate, the receiver configuration will be changed by the modem to reflect the new rate **after the retrain is completed.** If the remote modem cannot operate at the new rate, then no rate change will take place during the retrain and the transmitter configuration register will automatically revert back to its original configuration. If the modem reconfigures from V.22 bis 2400 bps to V.22 1200 bps during a handshake or as a result of a retrain, the TCONF and RCONF registers will contain the hex number 82.
RTS	0:8:0	0	When control bit RTS is a 1, the modem transmits any data on TXD when CTS becomes active. In V.22 bis, V.22, V.23, V.21, and Bell 103 constant carrier and V.32 modes, RTS controls data transmission and DTR controls the carrier. For ease of use, RTS can be turned ON at the same time as DTR. In V.22 bis controlled carrier mode, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, the modem then transmits 270 ms of scrambled 1s before turning CTS ON. In V.21, V.23 and Bell 103 controlled carrier modes, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, CTS is turned ON per Table 2. The RTS bit parallels the operation of the $\overline{RTS}$ hardware control input. These inputs are ORed by the modem. (See descriptions of CTS and DTR bits)
SADET	1:D:2	—	**Scrambled Alternating Sequence Detector.** When set to a 1, status bit SADET indicates that scrambled alternating data is being received. This bit is intended to be used for the automatic rate change sequence. (See ARC0 and ARC1.) This bit is reset to 0 at the end of the alternating sequence. (V.22 bis)
SCR1	1:D:4	—	**Scrambled Ones Detector.** When set to a 1, status bit SCR1 indicates that V.22 bis scrambled 1s have been detected during handshake. This bit is reset to 0 at the end of the scrambled 1s sequence. (V.22 bis)
SDET	1:C:3	—	**S Detector.** When set to a 1, status bit SDET indicates that a V.32 S sequence has been detected. This bit is reset to a 0 by the modem at the end of the S sequence. (V.32)
SDIS	0:3:2	0	**Scrambler Disable.** When control bit SDIS is a 1, the transmitter scrambler circuit is disabled; when a 0, the scrambler circuit is enabled. (V.32,V.22 bis.)
SNDET	1:C:2	—	**S Negative Detector.** When set to a 1, status bit SNDET indicates that a V.32 $\overline{S}$ sequence has been detected. This bit is reset to a 0 at the end of the $\overline{S}$ sequence. (V.32)
SPEED	1:E:0–2	—	**Speed Indication.** The SPEED status bits indicate the receiver's data rate at the completion of a handshake. **Data Rate / SPEED (Hex) / Data Rate / SPEED (Hex)** 0–300 / 0 / 4800 / 4 600 / 1 / 9600 / 5 1200 / 2 / 12000 / 6 2400 / 3
SQDIS	1:2:6	0	**Squarer Disable (Tone Detector C).** When control bit SQDIS is a 1, the squarer in front of tone dectector C is disabled; when a 0, the squarer is enabled.
STB0	0:6:2	0	**Stop Bit Number Chip 0.** When control bit STB0 is a 0, one stop bit is selected in asynchronous mode in the transmitter; when a 1, two stop bits are selected. This bit must be configured appropriately before the ASYN0 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis, V.22, Bell 212A)
STB1	1:6:2	0	**Stop Bit Number Chip 1.** When control bit STB1 is a 1, one stop bit is selected in asynchronous mode in the receiver; when a 1, two stop bits are selected. This bit must be configured appropriately before the ASYN1 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis, V.22, Bell 212A)

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Memory Location</th><th>Default Value</th><th>Name/Description</th></tr>
<tr><td>STOFF</td><td>0:5:1</td><td>0</td><td>Soft Turn Off. When control bit STOFF is a 1, the transmitter sends a tone at the end of a transmission in V.23, V.21 and Bell 103 configurations. This tone is detected as a mark frequency at the receiver. The soft turn off tone frequencies and durations are as follows:
<table>
<tr><th>Configuration</th><th>Frequency (Hz)</th><th>Duration (mS)</th></tr>
<tr><td>V.23/1200</td><td>900</td><td>7</td></tr>
<tr><td>V21 Orig.</td><td>880</td><td>30</td></tr>
<tr><td>V21 Ans.</td><td>1550</td><td>30</td></tr>
<tr><td>Bell 103 Orig.</td><td>1370</td><td>30</td></tr>
<tr><td>Bell 103 Ans.</td><td>2325</td><td>30</td></tr>
</table></td></tr>
<tr><td>S1DET</td><td>1:D:5</td><td>—</td><td>S1 Detector. When set to a 1, status bit S1DET indicates that a V.22 bis S1 sequence has been detected. This bit is reset to a 0 by the modem at the end of the S1 sequence. (V.22 bis)</td></tr>
<tr><td>TBUFFER</td><td>0:0:0–7</td><td>00</td><td>Transmitter Buffer/Transmitter Signal Point X. The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. Parallel data mode is available only in synchronous mode. The data is transmitted bit 0 first and is divided on the following baud boundaries:
<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.32 TCM 12000</td><td>—</td><td>—</td><td>—</td><td colspan="5">Baud 0</td></tr>
<tr><td>V.32 TCM 9600</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.32 9600</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.32 4800</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.32 TCM 7200</td><td>—</td><td>—</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.22 bis 2400</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.22 1200</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.22 600</td><td colspan="8">8 bit data</td></tr>
<tr><td>Bell 212A 1200</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.21</td><td colspan="8">8 bit data</td></tr>
</table></td></tr>
<tr><td>TCONF</td><td>0:12:0–7</td><td>74</td><td>Transmitter Configuration. The TCONF control bits select one of the following transmitter configurations:
<table>
<tr><th>Mode</th><th>Data Rate</th><th>TCONF (Hex)</th></tr>
<tr><td>V.32 TCM</td><td>12000</td><td>72</td></tr>
<tr><td>V.32</td><td>9600</td><td>74</td></tr>
<tr><td>V.32</td><td>9600</td><td>75</td></tr>
<tr><td>V.32</td><td>4800</td><td>71</td></tr>
<tr><td>V.32 TCM</td><td>7200</td><td>78</td></tr>
<tr><td>V.22 bis</td><td>2400</td><td>84</td></tr>
<tr><td>V.22</td><td>1200</td><td>52</td></tr>
<tr><td>V.22</td><td>600</td><td>51</td></tr>
<tr><td>V.21</td><td>0–300</td><td>A0</td></tr>
<tr><td>Bell 212A</td><td>1200</td><td>62</td></tr>
<tr><td>Bell 103</td><td>0–300</td><td>60</td></tr>
<tr><td>V.23</td><td>1200</td><td>A4</td></tr>
<tr><td>V.23</td><td>600</td><td>A2</td></tr>
<tr><td>V.23</td><td>75</td><td>A1</td></tr>
<tr><td>Single Tone</td><td>—</td><td>80</td></tr>
<tr><td>Dual Tone</td><td>—</td><td>83</td></tr>
<tr><td>Dialing</td><td>—</td><td>81</td></tr>
<tr><td colspan="3">When single tone or dual tone mode is selected the modem transmits one or two tones respectively. The tone frequencies are host programmable in DSP RAM. Single tone transmit uses the Dual Tone 1 frequency and level.</td></tr>
</table></td></tr>
</table>

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
TDAE	1:2:7	1	**Tone Detector A Enable.** When control bit TDAE is a 1, tone detector A is enabled; when a 0, tone detector A is disabled. This bit only has an effect when DATA1 bit is a 1 and the receiver is in asynchronous mode or V.32 12000 bps.
TLVL	0:13:4–7	0	**Transmit Level.** The TLVL code selects the transmitter analog output level at the TXA pin as follows: **TLVL Code (Hex)** / **TX Output Level (dBm ±0.5 dB)** 0 / −0.5 1 / −1.5 2 / −2.5 3 / −3.5 4 / −4.5 5 / −5.5 6 / −6.5 7 / −7.5 8 / −8.5 9 / −9.5 A / −10.5 B / −11.5 C / −12.5 D / −13.5 E / −14.5 F / −15.5 The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.
TM	0:F:2	—	**Test Mode.** When set to a 1, status bit TM indicates that the modem has completed the handshake and is in the Loop 3 or RDL test mode. (V.22 bis)
TOD	2:4:1	0	**Train On Data.** When set to a 1, control bit TOD enables the train-on-data algorithm to converge the equalizer if the signal quality degrades. A BER of 10^{-3} for 0.5 seconds initiates the train-on-data. When TOD is a 1, the modem is still able to recognize an incoming training sequence. (V.32.)
TONEA	1:B:7	—	**Tone A Detected.** When set to a 1, status bit TONEA indicates that energy is present on the line within the tone detector A passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	1:B:6	—	**Tone B Detected.** When set to a 1, status bit TONEB indicates that energy is present on the line within the tone detector B passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	1:B:5	—	**Tone C Detected.** When set to a 1, status bit TONEC indicates that energy is present on the line within the tone detector C passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM. The TONEC filter is preceded by a squarer in order to facilitate detection of difference tones. This squarer may be disabled with the SQDIS bit (see SQDIS bit).
TPDM	0:8:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is a 1, the transmitter accepts data for transmission from the TBUFFER (0:0) rather than the TXD input.
TSPA	0:5:0	0	**Transmitter Signal Point Activate.** When control bit TSPA is a 1, the transmitter uses the signal points X and Y directly from registers TSPX (0:0) and TSPY (0:1). The transmitter data input, TBUFFER and TXD, are ignored. When TSPA is a 0, the transmitter accepts data for transmission from the TBUFFER or the TXD input.
TSPX	0:0:0–7	00	**Transmitter Signal Point X.** When TSPA is a 1, register 0:0 is used to transmit the in-phase (X) coordinate of the transmitted signal point (TSPX). (V.32, V.22 bis, V.22, Bell 212A.)
TSPY	0:1:0–7	00	**Transmitter Signal Point Y.** When TSPA is a 1, register 0:1 is used to transmit the quadrature (Y) coordinate of the transmitted signal point (TSPY). (V.32, V.22 bis, V.22, Bell 212A.)
TXCLK	0:13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock. **TXCLK** / **Transmit Clock** 0 / Internal 2 / External (XTCLK) 3 / Slave ($\overline{\text{RDCLK}}$) When the external clock is chosen, the host supplied clock must be connected to the XTCLK input pin. The external clock will then be reflected at the TDCLK output pin. When the slave clock is chosen, the transmitter clock (TDCLK) is phase locked to the receiver clock ($\overline{\text{RDCLK}}$).

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
TXSQ	0:5:4	0	**Transmitter Squelch.** When control bit TXSQ is a 1, the transmitter analog output is squelched. All other transmitter functions continue as normal. When TXSQ is a 0, the transmitter output functions normally. This bit is useful in 2-wire configurations where it is necessary to measure the spectrum and transmit level of a transmitter. Setting the TXSQ bit to a 1 turns off the transmitter so that only one of the two carriers is present. After TXSQ is set to a 0, a retrain should be sent to reestablish the data transfer.
U1DET	1:D:3	—	**Unscrambled 1s Detector.** When set to a 1, status bit U1DET indicates that V.22 bis unscrambled 1s sequence has been detected. This bit is reset to a 0 by the modem at the end of the unscrambled 1s sequence. U1DET is not active when DATA1 is a 0. (V.22 bis)
V21	1:B:2	—	**V.21 Mark Detector.** When set to a 1, status bit V21 indicates that a V.21 mark frequency was detected during a handshake. (V.21)
V21S1	1:8:5	0	**V21 Synchronous Chip 0.** When configuration bit V21S1 is a 1 and the Receiver Configuration (RCONF) has been set for V.21, then V21 Synchronous mode is selected in the receiver. Synchronous data is output in both serial and parallel form. A synchronous clock is provided on the RDCLK pin. When V21S1 is a 0 and the Receiver Configuration (RCONF) has been set for V.21, then V.21 Asynchronous mode is selected in the receiver. Since V21S1 is a configuration bit, then NEWC1 must be set for any changes in this bit to take effect.
V21S0	0:8:5	0	**V21 Synchronous Chip 1.** When configuration bit V21S0 is a 1 and the Transmitter Configuration (TCONF) has been set for V.21, then V21 Synchronous mode is selected in the transmitter. Synchronous data may be applied in either serial or parallel form. A synchronous clock is provided on the TDCLK pin. When V21S0 is a 0 and the Transmitter Configuration (TCONF) has been set for V.21, then V.21 Asynchronous mode is selected in the transmitter. Since V21S0 is a configuration bit, then NEWC0 must be set for any changes in this bit to take effect.
WDSZ0	0:6:0,1	0	**Data Word Size Chip 0.** The WDSZ0 field sets the number of data bits per character in asynchronous mode in the transmitter as follows (V.32, V.22 bis, V.22, Bell 212A): **Data Bits/Character** — **WDSZ0 (Hex)** 5 — 0 6 — 1 7 — 2 8 — 3 This bit must be configured appropriately before the ASYN0 bit changes from a 0 to a 1 for asynchronous mode.
WDSZ1	1:6:0,1	0	**Data Word Size Chip 1.** The WDSZ1 field sets the number of data bits per character in asynchronous mode in the receiver as follows (V.32, V.22 bis, V.22, Bell 212A): **Data Bits/Character** — **WDSZ1 (Hex)** 5 — 0 6 — 1 7 — 2 8 — 3 This bit must be configured appropriately bvefore the ASYN1 bit changes from a 0 to a 1 for asynchronous mode.
XACC0	0:1D:7	0	**X RAM Access Enable Chip 0.** When control bit XACC0 is a 1, DSP chip 0 accesses the X RAM associated with the address in XADD0 and the XCR0 bit. XWT0 determines if a read or write is performed. The DSP resets XACC0 to a 0 upon RAM access completion.
XACC1	1:1D:7	0	**X RAM Access Enable Chip 1.** When control bit XACC1 is a 1, DSP chip 1 accesses the X RAM associated with the address in XADD1 and the XCR1 bit. XWT1 determines if a read or write is performed. The DSP resets XACC1 to a 0 upon RAM access completion.
XACC2	2:1D:7	0	**X RAM Access Enable Chip 2.** When control bit XACC2 is a 1, DSP Chip 2 accesses the X RAM associated with the address in XADD2 and the XCR2 bit. XWT2 determines if a read or write is performed. The DSP resets XACC2 to a 0 upon RAM access completion.
XADD0	0:1C:0–7	00	**X RAM Address Chip 0.** XADD0 contains the X RAM address used to access DSP chip 0's X Data RAM (XCR0 = 0) or X Coefficient RAM (XCR0 = 1) via the X RAM Data LSB and MSB registers (0:18 and 0:19, respectively) (See Table 9.)
XADD1	1:1C:0–7	00	**X RAM Address Chip 1.** XADD1 contains the X RAM address used to access DSP chip 1's X Data RAM (XCR1 = 0) or X Coefficient RAM (XCR1 = 1) via the X RAM Data LSB and MSB registers (1:18 and 1:19, respectively) (See Table 9.).
XADD2	2:1C:0–7	00	**X RAM Address Chip 2.** XADD2 contains the X RAM address used to access DSP chip 2's X Data RAM (XCR2 = 0) or X Coefficient RAM (XCR2 = 1) via the X RAM Data LSB and MSB registers (2:18 and 2:19, respectively). (See Table 9.)

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
XCRD0	0:1D:2	0	**X RAM Continuous Read Chip 0.** When control bit XCRD0 is a 1, bits XACC0 and XWT0 are overridden and an X RAM read from chip 0 is performed every sample from the location addressed by XADD0 (see DSP RAM Access).
XCRD1	1:1D:2	0	**X RAM Continuous Read Chip 1.** When control bit XCRD1 is a 1, bits XACC1 and XWT1 are overridden and an X RAM read from chip 1 is performed every sample from the location addressed by XADD1 (see DSP RAM Access).
XCRD2	2:1D:2	0	**X RAM Continuous Read Chip 2.** When control bit XCRD2 is a 1, bits XACC2 and XWT2 are overridden and an X RAM read from chip 2 is performed every baud from the location addressed by XADD2 (see DSP RAM Access).
XCR0	0:1D:0	0	**X Coefficient RAM Select Chip 0.** When control bit XCR0 is a 1, XADD0 applies to DSP chip 0's X Coefficient RAM. When XCR0 is a 0, XADD0 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 9).
XCR1	1:1D:0	0	**X Coefficient RAM Select Chip 1.** When control bit XCR1 is a 1, XADD1 applies to DSP chip 1's X Coefficient RAM. When XCR1 is a 0, XADD1 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 9).
XCR2	2:1D:0	0	**X Coefficient RAM Select Chip 2.** When control bit XCR2 is a 1, XADD2 applies to DSP chip 2's X Coefficient RAM. When XCR2 is a 0, XADD2 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 10).
XDAL0	0:18:0-7	00	**X RAM Data LSB Chip 0.** XDAL0 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAL1	1:18:0-7	00	**X RAM Data LSB Chip 1.** XDAL1 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAL2	2:18:0-7	00	**X RAM Data LSB Chip 2.** XDAL2 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2.
XDAM0	0:19:0-7	00	**X RAM Data MSB Chip 0.** XDAM0 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAM1	1:19:0-7	00	**X RAM Data MSB Chip 1.** XDAM1 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAM2	2:19:0-7	00	**X RAM Data MSB Chip 2.** XDAM2 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2.
XWT0	0:1D:1	0	**X RAM Write Chip 0.** When XWT0 is a 1 and XACC0 is set to a 1, DSP chip 0 copies data from the X RAM Data registers (0:18 and 0:19) into the X RAM location addressed by XADD0 and XCR0. When control bit XWT0 is a 0 and XACC0 is set to a 1, DSP chip 0 reads X RAM at the location addressed by XADD0 and XCR0. The read data is stored into the X RAM Data registers (0:18 and 0:19).
XWT1	1:1D:1	0	**X RAM Write Chip 1.** When XWT1 is a 1 and XACC1 is set to a 1, DSP chip 1 copies data from the X RAM Data registers (1:18 and 1:19) into the X RAM location addressed by XADD1 and XCR1. When control bit XWT1 is a 0 and XACC1 is set to a 1, DSP chip 1 reads X RAM at the location addressed by XADD1 and XCR1. The read data is stored into the X RAM Data registers (1:18 and 1:19).
XWT2	2:1D:1	0	**X RAM Write Chip 2.**When XWT2 is a 1 and XACC2 is set to a 1, DSP chip 2 copies data from the X RAM Data registers (2:18 and 2:19) into the X RAM location addressed by XADD2 and XCR2. When control bit XWT2 is a 0 and XACC2 is set to a 1, the DSP chip 2 reads X RAM at the location addressed by XADD2 and XCR2. The read data is stored in the X RAM Data registers (2:18 and 2:19).
YACC0	0:1B:7	0	**Y RAM Access Enable Chip 0.** When control bit YACC0 is a 1, DSP chip 0 accesses the Y RAM associated with the address in YADD0 and the YCR0 bit. YWT0 determines if a read or write is performed. The DSP resets YACC0 to a 0 upon RAM access completion.
YACC1	1:1B:7	0	**Y RAM Access Enable Chip 1.** When control bit YACC1 is a 1, DSP chip 1 accesses the Y RAM associated with the address in YADD1 and the YCR1 bit. YWT1 determines if a read or write is performed. The DSP resets YACC1 to a 0 upon RAM access completion.
YACC2	2:1B:7	0	**Y RAM Access Enable Chip 2.** When control bit YACC2 is a 1, DSP chip 2 accesses the Y RAM associated with the address in YADD2 and the YCR2 bit. YWT2 determines if a read or write is performed. The DSP sets YACC2 to a 0 upon RAM access completion.
YADD0	0:1A:0-7	00	**Y RAM Address Chip 0.** YADD0 contains the Y RAM address used to access DSP chip 0's Y Data RAM (YCR0 = 0) or Y Coefficient RAM (YCR0 = 1) via the Y RAM Data LSB and MSB registers (0:16 and 0:17, respectively). (See Table 9.)

Table 8. R9696DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
YADD1	1:1A:0–7	00	**Y RAM Address Chip 1.** YADD1 contains the Y RAM address used to access DSP chip 1's Y Data RAM (YCR1 = 0) or Y Coefficient RAM (YCR1 = 1) via the Y RAM Data LSB and MSB registers (1:16 and 1:17, respectively). (See Table 9.)
YADD2	2:1A:0–7	00	**Y RAM Address Chip 2.** YADD2 contains the Y RAM address used to access DSP chip 2's Y Data RAM (YCR2 = 0) or Y Coefficient RAM (YCR2 = 1) via the Y RAM Data LSB and MSB registers (2:16 and 2:17, respectively). (See Table 9.)
YCRD0	0:1B:2	0	**Y RAM Continuous Read Chip 0.** When control bit YCRD0 is a 1, bits YACC0 and YWT0 are overridden and a Y RAM read from chip 0 is performed every sample from the location addressed by YADD0 (see DSP RAM Access).
YCRD1	1:1B:2	0	**Y RAM Continuous Read Chip 1.** When control bit YCRD1 is a 1, bits YACC1 and YWT1 are overridden and a Y RAM read from chip 1 is performed every sample from the location addressed by YADD1 (see DSP RAM Access).
YCRD2	2:1B:2	0	**Y RAM Continuous Read Chip 2.** When control bit YCRD2 is a 1, bits YACC2 and YWT2 are overridden and a Y RAM read from chip 2 is performed every baud from the location addressed by YADD2 (see DSP RAM Access).
YCR0	0:1B:0	0	**Y Coefficient RAM Select Chip 0.** When control bit YCR0 is a 1, YADD0 applies to DSP chip 0's Y Coefficient RAM. When YCR0 is a 0, YADD0 applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 9).
YCR1	1:1B:0	0	**Y Coefficient RAM Select Chip 1.** When control bit YCR1 is a 1, YADD1 applies to DSP chip 1's Y Coefficient RAM. When YCR1 is a 0, YADD1 applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 9).
YCR2	2:1B:0	0	**Y Coefficient RAM Select Chip 2.** When control bit YCR2 is a 1, YADD2 applies to the DSP chip 2's Y Coefficient RAM. When YCR2 is a 0, YADD2 applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 9).
YDAL0	0:16:0–7	00	**Y RAM Data LSB Chip 0.** YDAL0 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAL1	1:16:0–7	00	**Y RAM Data LSB Chip 1.** YDAL1 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAL2	2:16:0–7	00	**Y RAM Data LSB Chip 2.** YDAL2 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM location in DSP chip 2.
YDAM0	0:17:0–7	00	**Y RAM Data MSB Chip 0.** YDAM0 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAM1	1:17:0–7	00	**Y RAM Data MSB Chip 1.** YDAM1 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAM2	2:17:0–7	00	**Y RAM Data MSB Chip 2.** YDAM2 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 2.
YWT0	0:1B:1	0	**Y RAM Write Chip 0.** When YWT0 is a 1 and YACC0 is set to a 1, DSP chip 0 copies data from the Y RAM Data registers (0:16 and 0:17) into the Y RAM location addressed by YADD0 and YCR0. When control bit YWT0 is a 0 and YACC0 is set to a 1, DSP chip 0 reads Y RAM at the location addressed by YADD0 and YCR0. The read data is stored into the Y RAM Data registers (0:16 and 0:17).
YWT1	1:1B:1	0	**Y RAM Write Chip 1.** When YWT1 is a 1 and YACC1 is set to a 1, DSP chip 1 copies data from the Y RAM Data registers (1:16 and 1:17) into the Y RAM location addressed by YADD1 and YCR1. When control bit YWT1 is a 0 and YACC1 is set to a 1, DSP chip 1 reads Y RAM at the location addressed by YADD1 and YCR1. The read data is stored into the Y RAM Data registers (1:16 and 1:17).
YWT2	2:1B:1	0	**Y RAM Write Chip 2.** When YWT2 is a 1 and YACC2 is set to a 1, DSP chip 2 copies data from the Y RAM Data registers (2:16 and 2:17) into the Y RAM location addressed by YADD2 and YCR2. When control bit YWT2 is a 0 and YACC2 is set to a 1, DSP chip 2 reads Y RAM at the location addressed by YADD2 and YCR2. The read data is stored in the Y RAM Data registers (2:16 and 2:17).

DSP RAM ACCESS

GENERAL

DSP RAM Organization

Each DSP contains a 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously.

Interface Memory Access to DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in DSP interface memory RAM Access registers by the host, in conjunction with the data or coefficient RAM bit (e.g., XCR0) determines the DSP RAM address for data access.

One or two 16-bit words are transferred between DSP RAM and DSP interface memory once each device cycle. The transmitter device and the receiver sample rate device operate at the 9600 Hz sample rate. The receiver baud rate device operates at the baud rate of the selected data rate.

Two RAM access bits in each DSP interface memory tell the DSP to access the X RAM and/or Y RAM. For example, the transfer is initiated in the transmitter by the host setting the XACC0 and/or the YACC0 bit(s). The transmitter tests these bits each sample period. The receiver tests XACC1 and YACC1 each sample period and XACC2 and YACC2 each baud period.

The following procedure applies to DSP RAM access in the transmitter device. The procedure to access DSP RAM in the receiver devices is the same with the exception of the RAM access bit names.

DSP RAM Write Procedure (Transmitter)

Before writing to DSP interface memory, set XACC0 and YACC0 to a 0. Set XWT0 and/or YWT0 to a 1 to inform the DSP that a RAM write will occur when XACC0 and/or YACC0 is set to a 1. Load the RAM address into X RAM Address and/or Y RAM Address registers; then set XCR0 and/or YCR0 appropriately. Write the desired data into the interface memory RAM Data registers then set XACC0 and/or YACC0 to a 1 to signal the DSP to perform the RAM write. When the DSP has transferred the contents of the interface memory RAM Data registers into RAM, the DSP sets the XACC0 and/or the YACC0 bit to a 0 and the NEWS0 bit to a 1 to indicate DSP RAM write completion.

If the NSIE0 bit is a 1, $\overline{IRQ}$ is also asserted and NSIA0 is set to a 1 when NEWS0 is set to a 1. NSIA0 is cleared by writing a 0 into the NEWS0 bit, which also causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

DSP RAM Read Procedure (Transmitter)

Before reading from DSP interface memory, set XACC0 and YACC0 to a 0. Set XWT0 and/or YWT0 to a 0 to inform the DSP that a RAM read will occur when XACC0 and/or YACC0 is set to a 1. Load the RAM Address code into X RAM Address and/or Y RAM address register; then set XCR0 and/or YCR0 appropriately. Set XACC0 and/or YACC0 to a 1 to signal the DSP to perform the RAM read. When the DSP has transferred the contents of RAM into the interface memory RAM Data registers, the DSP sets the XACC0 and/or the YACC0 bit to a 0 and the NEWS0 bit to a 1 to indicate DSP RAM read completion.

If the NSIE0 bit is a 1, $\overline{IRQ}$ is also asserted when NEWS0 is set to a 1. When $\overline{IRQ}$ is asserted, NSIA0 goes to a 1 to inform the host that setting of the NEWS0 bit was the source of the interrupt. NSIA0 is cleared by writing a 0 into the NEWS0 bit, which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

CONTINUOUS RAM READ PROCEDURE

There are several diagnostic parameters that the host may wish to read every sample or every baud period. One example of this is the EQM (Eye Quality Monitor) value in chip 2 (receiver baud). The host may avoid having to set the XACC2/YACC2 bit every baud period by using the continuous read feature. Setting XCRD2 to a 1 overrides both XACC2 and XWT2 bits, while setting YCRD2 to a 1 overrides both YACC2 and YWT2 bits.

The RAM address registers 1A and 1C and the XCR2 and YCR2 bits must be set up as described in the general DSP RAM read procedure. Then set XCRD2 and YCRD2 to 1. The chip 2 DSP will then transfer data to the interface memory every baud. The NEWS2 bit is set as described in the general DSP RAM read procedure.

The transmitter (chip 0) and receiver (chip 1) can be similarly treated, however, data will be transferred every sample by each device.

Table 9 provides the RAM functions, address codes, and registers.

SOFTWARE INTERFACE CONSIDERATIONS

INTERRUPT REQUEST HANDLING

DSP interface memory registers registers 00, 1E and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER)/Rate Sequence Code LSB (RSEQL) in the receiver sample rate device and the Transmit Buffer (TBUFFER)/Transmit Signal Point X (TSPX) in the transmitter device. Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits. When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using $\overline{IRQ}$) or by being interrupted by $\overline{IRQ}$. When an interrupt enable bit is a 1, $\overline{IRQ}$ is asserted and the appropriate interrupt active bit set to a 1 when the corresponding interrupt condition occurs.

The basic sources for $\overline{IRQ}$ generation are status change detected, configuration change implemented, receive buffer full and transmit buffer empty. Each source is individually maskable. Table 10 identifies the interrupt sources and describes the interrupt clearing procedures.

Table 9. R9696DP RAM Addresses

No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imaginary Part (Y)	CR Bit[1]	No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imaginary Part (Y)	CR Bit[1]
1	Transmitter Compromise Equalizer Coefficients·					28	Tone Detector C Bandpass Filter Coefficients	1	32	—	1
	First Tap	0	5B	—	1	29	RLSD On-to-Off Threshold	1	07	—	1
	Last Tap	0	34	—	1	30	RLDS Off-to-On Threshold	1	01	—	0
2	V.33/V.32 Rate Sequence	0	93	—	1	31	Receiver Chip 1 New Status Bit (NEWS1)				
3	DTMF Tone Duration	0	9A	—	1		Masking Register for 1:A and 1:B	1	9B	—	1
4	DTMF Interdigit Delay	0	1A	—	1		Masking Register for 1:C and 1:D	1	9C	—	1
5	DTMF Low Band Power Level	0	19	—	1		Masking Register for 1:E and 1:F	1	9D	—	1
6	DTMF High Band Power Level	0	99	—	1	32	Received Signal Samples	1	03	—	0
7	Pulse Relay Make Time	0	9C	—	1	33	Demodulator Output	1	04	84	0
8	Pulse Relay Break Time	0	1C	—	1	34	Low Pass Filter Output	1	00	80	0
9	Pulse Interdigit Delay	0	1B	—	1	35	Average Energy	1	02	—	0
10	Transmitter Output Level Gain Constant	0	99	—	0	36	AGC Gain Word	1	01	—	1
11	Dual Tone 1 Frequency	0	87	—	0	37	Timing Recovery Update	1	25	—	0
12	Dual Tone 2 Frequency	0	90	—	1	38	V.23 Receiver Compromise Equalizer Coefficients:				
13	Dual Tone 1 Power Level	0	02	—	0		Tap 1	1	76	—	1
14	Dual Tone 2 Power Level	0	82	—	0		Tap 20	1	63	—	1
15	Transmitter New Status Bit (NEWS0) Masking Register for 0:E and 0·F	0	11	—	1		Tap 21	1	F6	—	1
							Tap 40	1	E3	—	1
16	Total Span of Echo Canceller	0	9D	—	0	39	Equalizer Input	2	18	98	0
17	Echo Canceller Dividing Point	0	A0	—	0	40	Equalizer Tap Coefficients:				
18	Far End Echo Canceller Center Tap Position	0	24	—	0		First Tap	2	18	98	1
							Last Tap	2	47	C7	1
19	Echo Canceller Update Coefficient (Training Mode)	0	24	—	1	41	Unrotated Equalizer Output	2	01	81	0
						42	Rotated Equalizer Output (Received Points)	2	02	82	1
20	Echo Canceller Update Coefficient (Data Mode)	0	A4	—	1	43	Decision Points (Ideal Points)	2	02	82	0
21	CTS OFF-to-ON Response Time (RTS–CTS Delay)	0	10	—	1	44	Equalizer Error	2	03	83	0
						45	Equalizer Rotation Angle	2	87	—	1
22	Round Trip Far Echo Delay	0	9E	—	0	46	Equalizer Frequency Correction	2	0A	—	1
23	Echo Canceller Error	0	20	—	0	47	Eye Quality Monitor (EQM)	2	07	—	1
24	Far End Echo Frequency Offset	0	20	—	1	48	Maximum Period of Valid Ring Signal	2	17	—	0
25	Far End Echo Level	0	25	—	0	49	Minimum Period of Valid Ring Signal	2	97	—	0
26	Tone Detector A Bandpass Filter Coefficients	1	26	—	1	50	Receiver Chip 2 New Status Bit (NEWS2) Masking Register for 2·E and 2:F	2	7E	—	0
27	Tone Detector B Bandpass Filter Coefficients	1	2C	—	1						

Note: 1. CR corresponds to XCR0, YCR0, XCR1, YCR1, XCR2, or YCR2 depending on the chip number and address code.

Table 10. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
Transmitter (DSP Chip 0)				
NSIA0	NSIE0	NEWS0	New status detected (NEWS0 transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A through 0F	Host writes a 0 into NEWS0 (Clears NSIA0 to a 0)
NCIA0	NCIE0	NEWC0	New transmitter configuration implemented by DSP (NEWC0 transitioned from a 1 to a 0)	Host writes a 0 into NCIE0 (Clears NCIA0 to a 0)
DBIA0	DBIE0	DBA0	Transmitter Data Buffer is empty and can be written (DBA0 transitioned from a 0 to a 1)	Host writes to register 0:0 (TBUFFER/TSPX) (Clears DBA0 and DBIA0 to 0)
Receiver (DSP Chip 1)				
NSIA1	NSIE1	NEWS1	New status detected (NEWS1 transitioned from a 0 to a 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A through 0F	Host writes a 0 into NEWS1 (Clears NSIA1 to a 0)
NCIA1	NCIE1	NEWC1	New receiver configuration or receiver threshold implemented by DSP (NEWC1 transitioned from a 1 to a 0)	Host writes a 0 into NCIE1 (Clears NCIA1 to a 0)
DBIA1	DBIE1	DBA1	Receiver Chip 1 Data Buffer is full and can be read (DBA1 transitioned from a 0 to a 1)	Host reads register 1:0 (RBUFFER/RSEQL) (Clears DBA1 and DBIA1 to 0)
Receiver (DSP Chip 2)				
NSIA2	NSIE2	NEWS2	New status detected (NEWS2 transitioned from a 0 to a 1) a RAM read or RAM write occurred b. Status bit changed in register 0F	Host writes a 0 into NEWS2 (Clears NSIA2 to a 0)
TBIA2	DBIE2	DBA2	Receiver Chip 2 Data Buffer is full and can be read (DBA2 transitioned from a 0 to a 1)	Host reads register 2:0 (RSPX) (Clears DBA2 and DBIA2 to 0)

AUTO DIAL PROCEDURE

The host auto dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 5). The modem timing accounts for the DTMF tone duration and amplitude, pulse make/break ratio, and interdigit delay. These dialing parameters are host programmable in DSP RAM.

The levels of the high band and low band DTMF tones may be modified by the host in DSP RAM. The level of the high band DTMF tone should be 2 dB greater than the level of the low band DTMF tone.

The auto dialer default parameters are given in Table 11.

Table 11. Auto Dialer Default Parameters

Parameter	Default Value
DTMF Tone Duration	95 ms
DTMF Interdigit Delay	70 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	−4 dBm
DTMF High Band Power Level	−2 dBm
Pulse Relay Make Time	36 ms
Pulse Relay Break Time	64 ms
Pulse Interdigit Delay	750 ms

Dial Digits/Tone Pairs

Hex	Dial Digits	Tone Pairs	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	#	941	1477

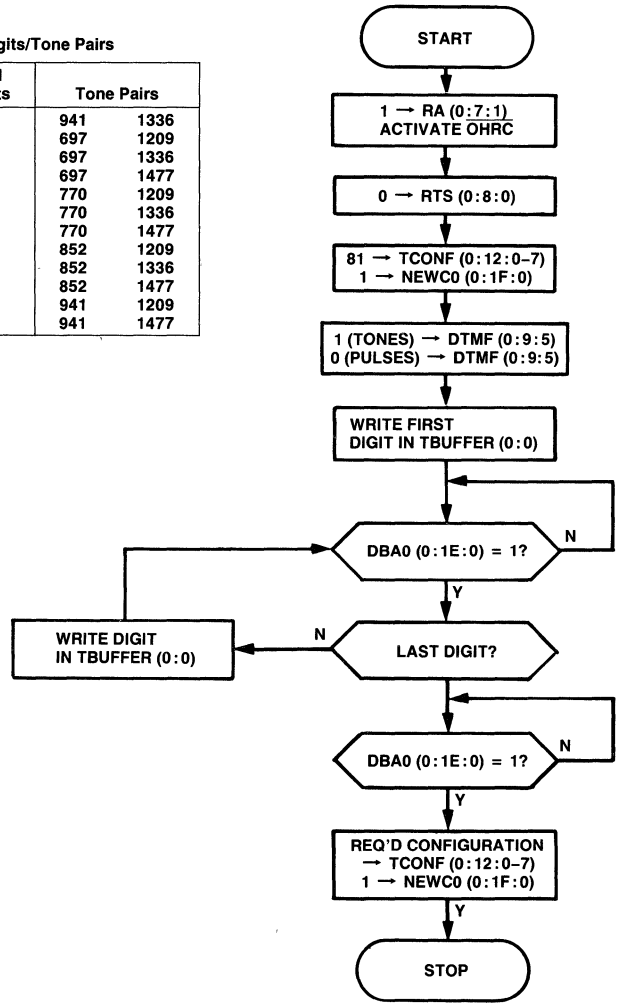


Figure 5. R9696DP Auto Dial Sequence and Dial Digits

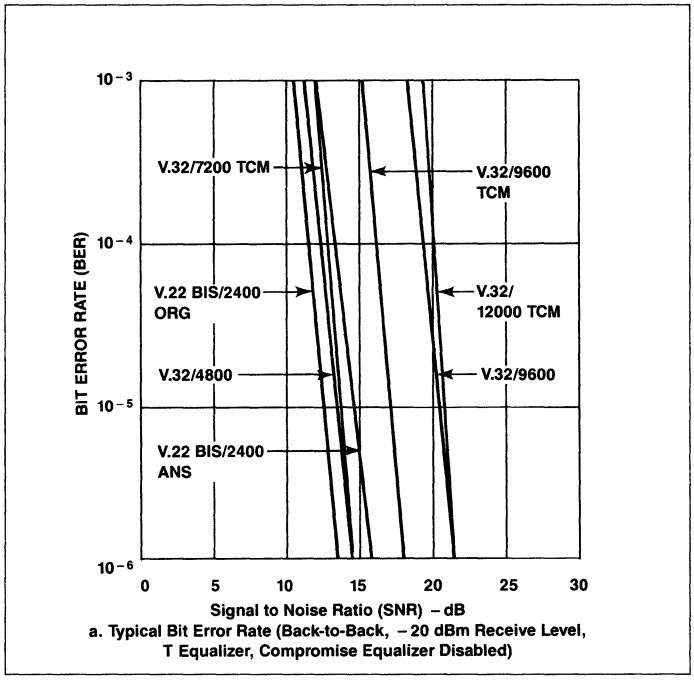
PERFORMANCE

TYPICAL BIT ERROR RATES

Typical modem bit error rate (BER) curves are shown in Figure 6 for a back-to-back connection.

TYPICAL BER TEST SETUP

The BER curves shown in Figure 6 were prepared from data obtained using a TAS 1002 test system.



a. Typical Bit Error Rate (Back-to-Back, – 20 dBm Receive Level, T Equalizer, Compromise Equalizer Disabled)

Figure 6. Bit Error Rate Curves

ELECTROMECHANICAL DESIGN CONSIDERATIONS

The area outlined by the analog ground plane in Figure 7 contains components which are sensitive to electromagnetic interference (EMI). When designing the host system, do not position radiating circuitry in the vicinity of this sensitive area. A ground plane adjacent to the modem analog circuitry is recommended.

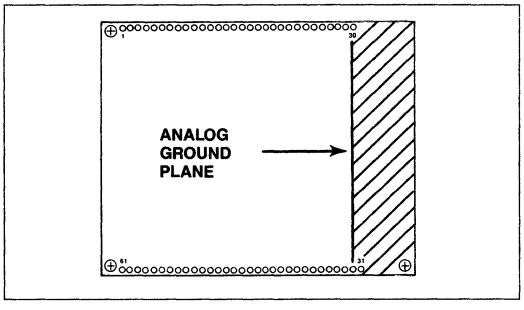


Figure 7. Analog Ground Plane Location

GENERAL SPECIFICATIONS

Table 12. R9696DP Modem Power Requirements

Voltage[1]	Tolerance	Current (Typical) @ 25°C	Current (Maximum) @ 0°C
+5 VDC	±5%	300 mA	585 mA
+12 VDC	±5%	3 mA	6 mA
−12 VDC	±5%	30 mA	36 mA

Note: 1. Input voltage ripple ≤0.1 volts peak-to-peak.

Table 13. R9696DP Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to +70°C (32°F to 158°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 14. R9696DP Modem Mechanical Dimensions

Parameter	Specification
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.228 in. (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0.300 in. (7.62 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.535 ±0.015 in. (13.6 ±0.4 mm), gold plated
	0.433 ±0.015 in. (11.0 ±0.4 mm), gold plated
	0.315 ±0.015 in. (8.0 ±0.4 mm), gold plated

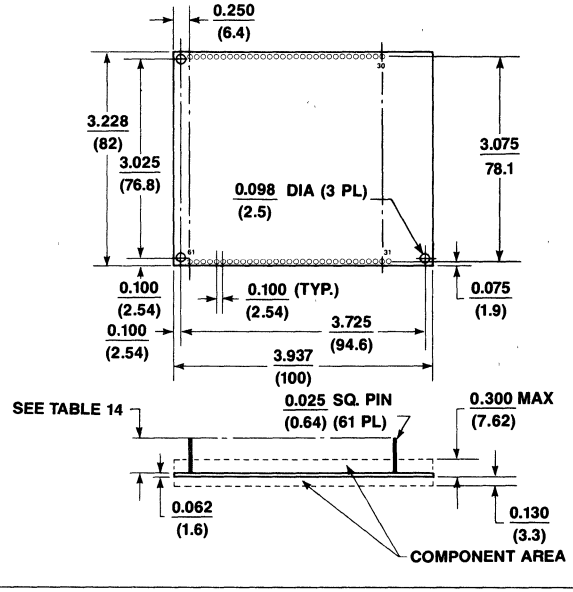


Figure 7. R9696DP Modem Dimensions and Pin Locations

SECTION 2
Leased Line Data Modems

Product Family Overview 2-2
R208/201 4800 bps Modem 2-3
R96DP 9600 bps Data Pump Modem 2-26
R96FT 9600 bps Fast Train Modem 2-47
R96FT/SC 9600 bps Fast Train Modem with Forward Secondary Channel 2-63
R144DP V.33 14.4 kbps Full-Duplex Modem 2-78
R1496DP V.33 14.4 kbps/V.32 9600 bps Full-Duplex Modem 2-103

LEASED LINE DATA MODEMS

LEADING THE INDUSTRY WITH HIGH PERFORMANCE AND QUALITY

Rockwell's extensive 4800 to 14400 bps leased-line modem product line can easily be incorporated into standalone or system level products at a minimal cost while offering your customer high performance, quality and reliability. This line of modems uses the latest technology to provide customers with the smallest, most integrated designs available on the market.

Our high and ultra-high speed modems are designed to meet the Bell standard as well as the rigid CCITT recommendations. Whether operating at 4800 bps or 14400 bps, transmitting data across the street or across the world, customers can be assured that Rockwell modems have been designed, built and tested to ensure world-wide connectivity.

Model	Data Speed (bps)	Compliance
R208/201	4800, 2400, 1200	Bell 201B/C, 208A/B CCITT V.27 bis/ter, V.26, V.26 bis
R96DP	9600, 7200, 4800, 2400	CCITT V.29, V.27 bis/ter
R96FT	9600, 7200, 4800, 2400	CCITT V.29, V.27 bis/ter, V.21 Channel 2, Proprietary Fast Train
R96FT/SC	9600, 7200, 4800, 2400, 75	CCITT V.29, V.27 bis/ter, V.21 Channel 2, Proprietary Fast Train, Secondary Channel
R144DP	14400, 12000, 9600, 7200, 4800, 2400	CCITT V.33, V.29, V.27 bis/ter
R1496DP	14400, 12000, 9600, 4800, 7200, 2400, 1200	CCITT V.33, V.32, V.29, V.22 bis

Rockwell

R208/201
Bell 208A/B and Bell 201C Modem

INTRODUCTION

The Rockwell R208/201 is a synchronous 4800, 2400 and 1200 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) as well as leased lines through the appropriate line termination. The R208/201 automatically senses the mode of the remote modem (Bell 208 A/B or Bell 201C) and configures itself to operate in a compatible mode.

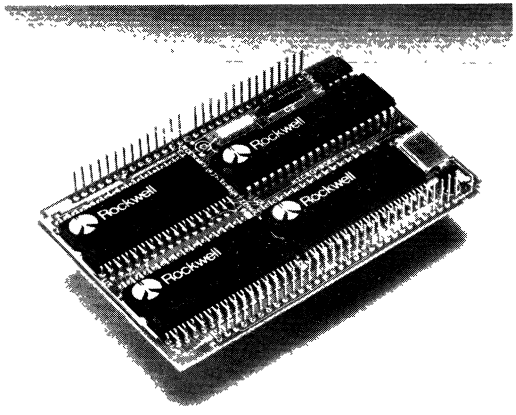
The modem satisfies the telecommunications requirements specified in Bell 208A/B, Bell 201C, CCITT V.27, and CCITT V.26A/B. The R208/201 can operate at speeds of 4800, 2400 and 1200 bps. Employing advanced signal processing techniques, the R208/201 can transmit and receive data even under extremely poor line conditions.

User programmable features allow the R208/201 to be tailored to support a wide variety of functional requirements. The modem's small size, low power consumption, and serial/parallel host interface simplify system design and allow installation in a compact enclosure. The modem module is available with a DIN connector for connection to a mating connector or with dual-in-line pins (DIP) in normal or Micromodem™ size modules for direct plug-in installation onto a host module.

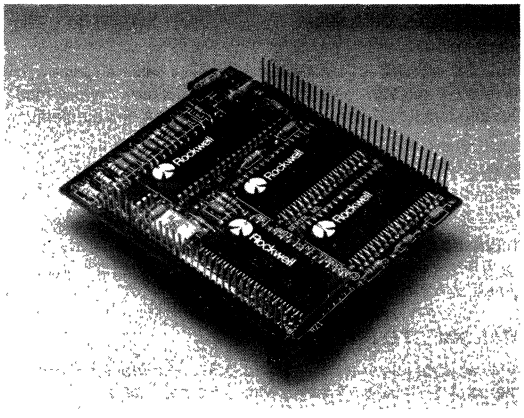
Micromodem is a trademark of Rockwell International

FEATURES

- Compatible with
  - — Bell 208A/B, Bell 201C
  - — CCITT V.27 and V.26
- Automatic Configuration during Synchronizing Sequence
- 2-Wire Half-Duplex, 4-Wire Full-Duplex
- Programmable Tone Generation
- Programmable DTMF Tone Dialer
- Call Progress Tone Detection
- Programmable RTS/CTS Delay (Bell 201C and V.26 only)
- Dynamic Range: – 43 dBm to 0 dBm
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C)(Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Diagnostic Capability
- Programmable Transmit Output Level
- Loopbacks
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — DIN Connector Version: 100 mm × 120 mm (3.94 in. × 4.73 in.)
  - — DIP Connector Version: (normal size) 82 mm × 100 mm (3.23 in. × 3.94 in.)
  - — Micromodem Version 65 mm × 100 mm (2.56 in. × 3.94 in.)
- Power Consumption: 3 W (Typical)



R208/201 Micromodem Version



R208/201 DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

The supported transmitter carrier frequencies are listed in Table 1.

Table 1. Transmitter Carrier Frequencies

Function	Frequency (Hz ±0.01%)
Bell 208A/B and Bell 201C	1800
CCITT V.27 and V.26	1800

TONE GENERATION

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. DTMF tone transmission capability is provided to allow the modem to operate as a programmable DTMF tone dialer.

SIGNALING AND DATA RATES

The supported signaling and data rates are listed in Table 2.

Table 2. Signaling/Data Rates

Specification	Baud Rate (Symbols/sec.)	Bits Per Baud	Data Rate (bps)(±0.01%)	Symbol Points
Bell 208A/B	1600	3	4800	8
CCITT V.27	1600	3	4800	8
CCITT V.27	1200	2	2400	4
V.26B/Bell 201C	1200	2	2400	4
CCITT V.26	1200	2	2400	4
CCITT V.26	1200	1	1200	4

DATA ENCODING

The modem data encoding conforms to Bell 208A/B, Bell 201C, CCITT V.27, and CCITT V.26.

EQUALIZERS

The modem provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with V.27 bis/ter.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The modem receiver circuit can adapt to received frequency error of up to ±10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The modem receiver circuit satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

TRANSMIT LEVEL

The transmitter output level is accurate to ±1.0 dB and is programmable from −1.0 dBm to −15.0 dBm in 2 dB steps.

TRAIN ON DATA

When train on data is enabled, the receiver typically trains on data in less than 3.5 seconds.

TURN-ON SEQUENCE

Selectable turn-on sequences can be generated for Bell 208A/B and V.27 as defined in Table 3. V.26A/B/Bell 201C have a programmable RTS/CTS delay with a default time of 26.6 ms (see page 18).

Table 3. Bell 208A/B and V.27 Turn-On Sequences

Specification	RTS-CTS Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled*
Bell 208A/B Long	150	355
Bell 208A/B Short	50	255
V.27 4800 Long	708	913
V.27 4800 Short	50	255
V.27 2400 Long	943	1148
V.27 2400 Short	67	272

*For short echo protector tone, subtract 155 ms from RTS-CTS turn-on time.

TURN-OFF SEQUENCE

For Bell 208A/B and CCITT V.27, the turn-off sequence consists of approximately 7 ms and 10 ms, respectively, of remaining data and scrambled ones. For V.26B/Bell 201C and CCITT V.26, the turn-off sequence consists of approximately 6 ms of remaining data and scrambled ones.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, diagnostic signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The six groups of hardware circuits are described in the following paragraphs. Table 5 lists the digital interface characteristics.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{\text{POR}}$) causes the modem to assume a valid operational state. The modem drives pin $\overline{\text{POR}}$ to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin $\overline{\text{POR}}$, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin $\overline{\text{POR}}$ low for at least 3 μs. When an external low input is applied to pin $\overline{\text{POR}}$, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin $\overline{\text{POR}}$ is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The modem POR sequence leaves the modem configured as follows:

- Bell 208 Short
- Serial channel data
- T/2 equalizer
- No echo protector tone
- −43 dBm threshold
- Cable and link equalizers disabled
- Train-On-Data enabled
- Scrambler and descrambler enabled

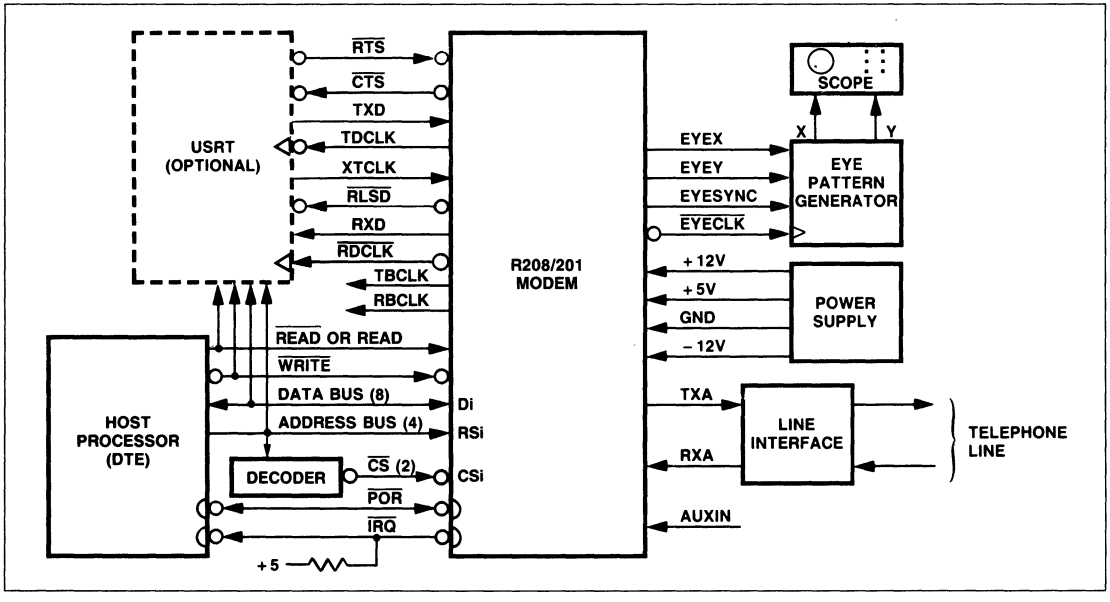


Figure 1. R208/201 Functional Interconnect Diagram

Table 4. R208/201 Hardware Circuits

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Micromodem Pin No.	Description
A. OVERHEAD:					
Ground (A)	AGND	31C,32C	30,31	27,28	Analog Ground Return
Ground (D)	DGND	3C,8C, 5A,10A	29,37,53	32,36,51	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	1,45,61	9,14,55	+5 volt supply
+12 volts	PWR	15A	32	29	+12 volt supply
−12 volts	PWR	12A	36	31	−12 volt supply
$\overline{POR}$	I/OB	13C	2	4	Power-on-reset
B. MICROPROCESSOR INTERFACE:					
D7	I/OA	1C	3	50	Data Bus (8 Bits)
D6	I/OA	1A	4	49	
D5	I/OA	2C	5	48	
D4	I/OA	2A	6	47	
D3	I/OA	3A	7	46	
D2	I/OA	4C	8	45	
D1	I/OA	4A	9	44	
D0	I/OA	5C	10	43	
RS3	IA	6C	16	3	Register Select (4 Bits)
RS2	IA	6A	17	58	
RS1	IA	7C	18	57	
RS0	IA	7A	19	40	
$\overline{CS0}$	IA	10C	20	2	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	21	42	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	13	60	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	12C	14	—	Read Enable
$\overline{READ}$	IA	—	—	61	Read Enable
$\overline{WRITE}$	IA	11A	12	59	Write Enable
$\overline{IRQ}$	OB	11C	11	1	Interrupt Request
C. V.24 INTERFACE:					
$\overline{RDCLK}$	OC	21A	23	38	Receive Data Clock
TDCLK	OC	23A	46	6	Transmit Data Clock
XTCLK	IB	22A	51	5	External Transmit Clock
$\overline{RTS}$	IB	25A	50	10	Request-to-Send
$\overline{CTS}$	OC	25C	49	8	Clear-to-Send
TXD	IB	24C	48	11	Transmitter Data
RXD	OC	22C	26	35	Receiver Data
$\overline{RLSD}$	OC	24A	27	37	Received Line Signal Detector
D. ANCILLARY CIRCUITS:					
RBCLK	OC	26A	22	12	Receiver Baud Clock
TBCLK	OC	27C	47	7	Transmitter Baud Clock
E. ANALOG SIGNALS:					
TXA	AA	31A	34	26	Transmitter Analog Output
RXA	AB	32A	33	30	Receiver Analog Input
AUXIN	AC	30A	—	—	Auxiliary Analog Input
F. DIAGNOSTIC:					
EYEX	OC	15C	56	52	Eye Pattern Data—X Axis
EYEY	OC	14A	55	56	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	57	54	Eye Pattern Clock
EYESYNC	OA	13A	58	53	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 5 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. Pins not used on the DIP Version: 15, 24, 25, 28, 35, 38, 39, 40, 41, 42, 43, 44, 52, 54, 59, and 60.
3. Pins not used on the Micromodem: 13, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 33, 34, 39, and 41.
4. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes

1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I Load = 0.36 mA

This configuration is suitable for performing high speed data transfer using the serial data port. Individual features are discussed in subsequent paragraphs.

V.24 INTERFACE

Eight hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, +5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The responses to $\overline{RTS}$ are shown in Table 3.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON condition of $\overline{RTS}$ are shown in Table 3.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in data state is a maximum of 2 baud times for all configurations.

Received Line Signal Detector ($\overline{RLSD}$)

For Bell 208A/B and CCITT V.27, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ±10 ms. For Bell 201C, RLSD turns on in 10 ±5 ms after the detection of energy above threshold. The RLSD on-to-off response time for Bell 208A/B, CCITT V.27 and Bell 201C is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on the threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

1. Greater than −43 dBm (RLSD on)
   Less than −48 dBm (RLSD off)
2. Greater than −33 dBm (RLSD on)
   Less than −38 dBm (RLSD off)
3. Greater than −26 dBm (RLSD on)
   Less than −31 dBm (RLSD off)
4. Greater than −16 dBm (RLSD on)
   Less than −21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 4800 or 2400 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

TDCLK is provided to the user in synchronous communications for USRT timing. In this case Transmit Data (TXD) must be stable during the one μs period immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{\text{RDCLK}}$)

The modem provides a Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. $\overline{\text{RDCLK}}$ is provided to the user in synchronous communications for USRT timing. The timing recovery circuit is capable of tracking a ±.01% frequency error in the associated transmit timing source.

MICROPROCESSOR INTERFACE

Eight hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{\text{CS0}}$-$\overline{\text{CS2}}$) and Register Selects (RS0-RS3)

The signal processor to be accessed is selected by grounding one of three unique chip select lines, $\overline{\text{CS2}}$, $\overline{\text{CS1}}$ or $\overline{\text{CS0}}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable (READ) and Write Enable ($\overline{\text{WRITE}}$)

Reading or writing is activated by pulsing either the READ line high (low for micromodem) or the $\overline{\text{WRITE}}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{\text{W}}$ output from a 65XX series microprocessor to the separate READ and $\overline{\text{WRITE}}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{\text{IRQ}}$)

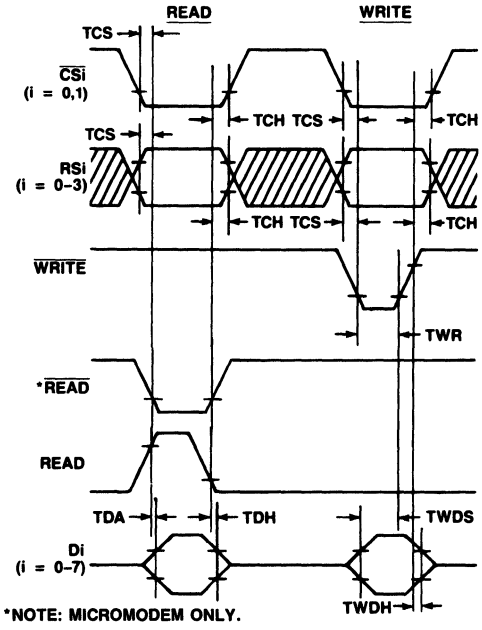
The final signal on the microprocessor interface is Interrupt Request ($\overline{\text{IRQ}}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{\text{IRQ}}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{\text{IRQ}}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{\text{IRQ}}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{\text{IRQ}}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{\text{IRQ}}$, an external pull-up resistor to +5 volts is required at some point on the $\overline{\text{IRQ}}$ line. The resistor value should be small enough to pull the $\overline{\text{IRQ}}$ line high when all $\overline{\text{IRQ}}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{\text{IRQ}}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

ANALOG SIGNALS

The analog signal characteristics are described in Table 6.

Table 6. Analog Interface Characteristics

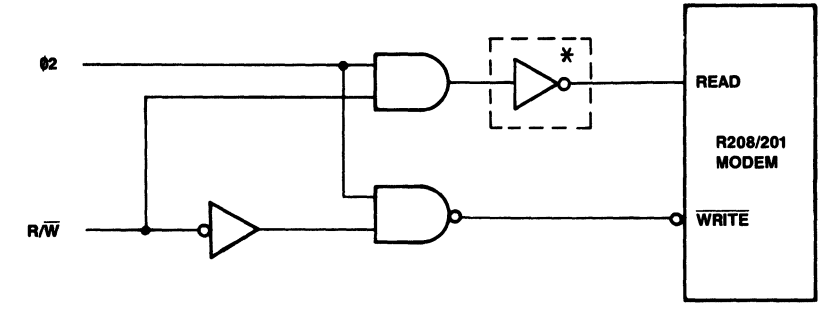
Name	Type	Characteristics
TXA	AA	The transmitter output is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is the TLVL setting +0.6 dB −1.4 dB.



*NOTE: MICROMODEM ONLY.

Characteristic	Symbol	Min	Max	Units
CSi, RSi setup time prior to Read or Write	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
CSi, RSi hold time after Read or Write	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram



*MICROMODEM ONLY.

Figure 3. R/W to READ WRITE Conversion Logic

Transmitter Analog (TXA)

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

Receiver Analog (RXA)

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may take the form of back-to-back zener diodes across the transformer or a varistor across the transformer.

Auxiliary Input (AUXIN)

AUXIN provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit at a rate of 9600 samples-per-second. Any signal above 4800 Hz on the AUXIN line will be aliased back into the passband as noise. The input impedance of AUXIN is 1K ohm. The gain from AUXIN to TXA is the same as the selected transmit level +0.6 dB −1.4 dB. AUXIN must be grounded if not used.

DIAGNOSTIC SIGNALS
EYEX, EYEY, $\overline{\text{EYECLK}}$, and EYESYNC

Four card edge connections provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

The outputs EYEX and EYEY provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. Since this data is in serial digital form it must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two D/A converters. A clock for use by the serial-to-parallel converters is furnished by signal $\overline{\text{EYECLK}}$. A strobe for loading the D/A converters is furnished by signal EYESYNC. Timing of these signals is illustrated in Figure 4. The EYEX and EYEY outputs furnish 9-bit serial words. Since most serial to parallel conversion logic is designed for 8-bit words, an extra storage flip-flop is required for 9-bit resolution. However, the ninth bit is not generally needed for eyepattern generation, and eight-bit hardware can be used if data is copied on the rising edge of $\overline{\text{EYECLK}}$ rather than the falling edge.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Two clock signals called TBCLK and RBCLK are provided at the modem connector. These signals have no counterpart in the V.24 or RS-232 recommendations since they mark the baud interval for the transmitter and receiver rather than the data rate. The baud clocks can be useful in identifying the order of data bits in a baud (e.g., for multiplexing data, etc.). Both signals are high active, meaning the baud boundaries occur on falling edges. The first bit in each baud begins with the falling edge of the corresponding baud clock.

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on three special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into areas. These areas are partitioned into transmitter, baud rate, and sample rate devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its

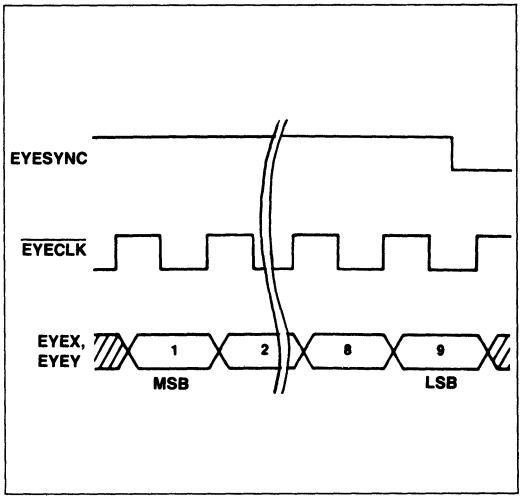


Figure 4. Eye Pattern Timing

internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 48 addressable registers in the modem are shown in Figure 5. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Table 7 defines the individual bits in the interface memory. In the Table 7 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

SIGNAL PROCESSOR RAM ACCESS

RAM and Data Organization

Each signal processor contains 128 words of random access memory (RAM). Each word is 32 bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16 bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. In the sample rate and baud rate devices the entire contents of XRAM and YRAM may be read from or written into by the host processor via the microprocessor interface. Access to the YRAM is possible only in the transmitter device.

Interface Memory

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit determines the RAM address to read from or write into by the code stored in the RAM ACCESS bits of interface memory registers. The SP logic unit normally transfers a word from RAM to interface memory once each cycle of the device code. Each RAM word transferred to the interface memory is 32 bits long (16 bits in the transmitter). These bits are written by the SP logic unit into interface memory registers 3, 2, 1, and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data, respectively. As previously described for parallel data mode, the data available bits set to a one when register 0 of the respective signal processor is written into by the device and resets to a zero when register 0 is read from by the host. Since the parallel data mode transmitter and receiver data register shares register 0 with the YRAM data, chip 0 and 1 RAM access are disabled in parallel data mode. However, chip 2 RAM access remains active in receiver parallel data mode.

The transmitter, sample rate device and the baud rate device allow data to be transferred from interface memory to RAM. When set to a one, bit SWRT (1:7:3) signals the chip 1 SP logic unit to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. Bit TWRT (0:6:3) performs the same function for chip 0 RAM and bit BWRT (1:7:2) performs the same function for chip 2 RAM. When writing into the RAM, 32 bits are transferred. The 16 bits written into XRAM come from registers 3 and 2, with register 3 being the more significant byte. The 16 bits written into YRAM come from registers 1 and 0, with register 1 being the more significant byte. When only 16 bits of data are to be written, FF (a dummy RAM location) must be stored in RAM ACCESS XS or RAM ACCESS YS to prevent writing the insignificant 16 bits of registers 1:3 through 1:0 into a valid RAM location. When the host processor writes into register 1:0 the RSDA bit (1:E:0) is reset to zero. When the SP logic unit reads data from register 1:0, the RSDA bit (1:E:0) is set to a one. In a similar manner, bit RBDA (2:E:0) resets to zero when the host processor writes into register 2:0 and sets to a one when the SP logic unit reads data from register 2:0.

When reading from RAM, or writing into RAM, the bits in registers 0:E, 1:E, 2:E can be used for handshaking or interrupt functions as in parallel data mode. When not in parallel data mode, the bits in register 1:E perform the handshake and interrupt functions for RAM access. In both serial and parallel data modes, the bits in register 2:E perform handshake and interrupt functions for RAM access. When set to one, bit RBIE (2:E:2) enables RBDA to drive the IRQ connector signal to zero volts when RBDA is a one. Bit RBIA (2:E:7) identifies chip 2, the baud rate device, as a source of IRQ interrupt. Bit RBIA is a one when both RBIE and RBDA are set to one. In the event that other system elements may cause IRQ to be driven low, the host must determine if modem chip 2 is causing an interrupt by reading RBIA.

Table 8 provides the available RAM access functions, codes, and registers.

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS T							
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION/TWRT (BIT 3)							
5	—	DCEQ	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	RAM DATA YTM							
0	RAM DATA YTL; TRANSMITTER DATA; DDR							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	SQH	—	—	—	—	—	—	—
E	RSIA	—	—	—	RSB	RSIE	—	RSDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	$\overline{TONE}$	—	—
8	—	—	—	—	—	$\overline{P2DET}$	—	—
7	RTH		DDIS	RPDM	SWRT	BWRT	T2	RTDIS
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL; RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 5. Interface Memory Map

Table 7. R208/201 Interface Memory Definitions

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>A3L</td><td>Amplitude 3-Link Select</td><td>0:5:1</td><td>A3L is used in conjunction with LAEN. When A3L is a one the Japanese 3 link equalizer is selected and when A3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
<tr><td>BWRT</td><td>Baud Write</td><td>1:7:2</td><td>When control bit BWRT is a one, the RAM write operation is enabled for Chip 2.</td></tr>
<tr><td>CEQ</td><td>Cable Equalizer Field</td><td>0:5:(4.5)</td><td>The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following tables list the possible cable equalizer selection codes and responses.

CEQ — Cable Length (0.4 mm diameter)
0 — 0.0
1 — 1.8 km
2 — 3.6 km
3 — 7.2 km

Cable Equalizer Nominal Gain

CEQ CODE 1
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>Transmitter</th><th>Receiver</th></tr><tr><td>700</td><td>−0.99</td><td>−0.94</td></tr><tr><td>1500</td><td>−0.20</td><td>−0.24</td></tr><tr><td>2000</td><td>+0.15</td><td>+0.31</td></tr><tr><td>3000</td><td>+1.43</td><td>+1.49</td></tr></table>
CEQ CODE 2
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>Transmitter</th><th>Receiver</th></tr><tr><td>700</td><td>−2.39</td><td>−2.67</td></tr><tr><td>1500</td><td>−0.65</td><td>−0.74</td></tr><tr><td>2000</td><td>+0.87</td><td>+1.02</td></tr><tr><td>3000</td><td>+3.06</td><td>+3.17</td></tr></table>
CEQ CODE 3
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>Transmitter</th><th>Receiver</th></tr><tr><td>700</td><td>−3.93</td><td>−3.98</td></tr><tr><td>1500</td><td>−1.22</td><td>−1.20</td></tr><tr><td>2000</td><td>+1.90</td><td>+1.81</td></tr><tr><td>3000</td><td>+4.58</td><td>+4.38</td></tr></table>
Unless a problem with training or high bit error rate is encountered, most applications operate successfully with no cable equalizer selected.</td></tr>
<tr><td>$\overline{\text{CDET}}$</td><td>Carrier Detector</td><td>1:B:0</td><td>When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$. If the $\overline{\text{FED}}$ bit goes to a zero and no P2 sequence is detected, the $\overline{\text{CDET}}$ bit goes to zero within 5 to 25 ms indicating that the receiver has entered the data state without a training sequence.</td></tr>
<tr><td>DCEQ</td><td>Digital Compromise Equalizer</td><td>0:5:6</td><td>When control bit DCEQ is a one, a digital compromise equalizer is inserted in the transmit path. (Bell 201C/V 26 modes only.) Applicable to B5407-18 and subsequent.</td></tr>
<tr><td>DDIS</td><td>Descramble Disable</td><td>1.7:5</td><td>When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.</td></tr>
<tr><td>DDR</td><td>Dial Digit Register</td><td>0:0:0–7</td><td>DDR is used to tell the modem which DTMF digit to transmit (see Transmitter Data).</td></tr>
<tr><td>D3L</td><td>Delay 3-Link Select</td><td>0:5:0</td><td>D3L is used in conjunction with LDEN. When D3L is a one the Japanese 3 link equalizer is selected and when D3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
</table>

Table 7. R208/201 Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>EPT</td><td>Echo Protector Tone</td><td>0:7:3</td><td>When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission.</td></tr>
<tr><td>$\overline{\text{FED}}$</td><td>Fast Energy Detector</td><td>1:9:6</td><td>When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband, and the receiver is searching for the training sequence.</td></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0–7,
0:3:0–7</td><td>The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below:

FREQM Register (0:3)
<table>
<tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr>
</table>
FREQL Register (0:2)
<table>
<tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr>
</table>
The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%

Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below:
<table>
<tr><th>FREQM</th><th>FREQL</th><th>Frequency (Hz)</th></tr>
<tr><td>0C</td><td>52</td><td>462</td></tr>
<tr><td>1D</td><td>55</td><td>1100</td></tr>
<tr><td>2C</td><td>00</td><td>1650</td></tr>
<tr><td>31</td><td>55</td><td>1850</td></tr>
<tr><td>38</td><td>00</td><td>2100</td></tr>
</table></td></tr>
<tr><td>IFIX</td><td>Eye Fix</td><td>1:6:7</td><td>When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB</td></tr>
<tr><td>LAEN</td><td>Link Amplitude Equalizer Enable</td><td>0:5:3</td><td>The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table:
<table>
<tr><th>LAEN</th><th>A3L</th><th>Curve Matched</th></tr>
<tr><td>0</td><td>X</td><td>No Equalizer</td></tr>
<tr><td>1</td><td>0</td><td>U.S. Survey Long</td></tr>
<tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr>
</table>
The link amplitude equalizer responses are given in the following table.

Link Amplitude Equalizer
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr>
<tr><td>1000</td><td>−0.27</td><td>−0.13</td></tr>
<tr><td>1400</td><td>−0.16</td><td>−0.08</td></tr>
<tr><td>2000</td><td>+0.33</td><td>+0.16</td></tr>
<tr><td>2400</td><td>+1.54</td><td>+0.73</td></tr>
<tr><td>2800</td><td>+5.98</td><td>+2.61</td></tr>
<tr><td>3000</td><td>+8.65</td><td>+3.43</td></tr>
</table></td></tr>
</table>

Table 7. R208/201 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5:2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN / D3L / Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link The link delay equalizer responses are given in the following table. **Link Delay Equalizer** **Frequency (Hz) / Delay Relative to 1700 Hz (Microseconds) / U.S. Survey Long / Japanese 3-Link** 800 / -498.1 / -653.1 1200 / -188.3 / -398.5 1600 / -15.1 / -30.0 1700 / +0.0 / +0.0 2000 / -39.8 / +11.7 2400 / -423.1 / -117.1 2800 / -672.4 / -546.3
L2ACT	Remote Digital Loopback Activate	0:4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2.
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0:4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4:5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
$\overline{\text{PNDET}}$	Period N Detector	1:B:6	When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence.
$\overline{\text{P2DET}}$	Period Two Detector	1:8:2	When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a P2 sequence has been detected. This bit sets to a one at the start of the PN sequence.
(None)	RAM Access T	0:F:0–7	Contains the RAM access code used in reading or writing chip 0 RAM locations via word Y (0:1 and 0:0).
(None)	RAM Access XB	2:5:0–7	Contains the RAM access code used in reading or writing chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access XS	1:5:0–7	Contains the RAM access code used in reading or writing chip 1 RAM locations via word X (1:3 and 1:2).
(None)	RAM Access YB	2:4:0–7	Contains the RAM access code used in reading or writing chip 2 RAM locations via word Y (2:1 and 2:0).

Table 7. R208/201 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Access YS	1:4:0–7	Contains the RAM access code used in reading or writing chip 1 RAM locations via word Y (1:1 and 1:0).
(None)	RAM Data XBL	2:2:0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 2.
(None)	RAM Data XBM	2:3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 2.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 1.
(None)	RAM Data YBL	2:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YBM	2:1:0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YSL	1:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data.'
(None)	RAM Data YSM	1:1:0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1.
(None)	RAM Data YTL	0:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 0. It is shared by parallel data mode and DTMF dialing (see Transmitter Data).
(None)	RAM Data YTM	0:1:0–7	Most significant byte of 16-byte word Y used in reading or writing locations in chip 0.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low. In idle mode the interrupts from chip 2 occur at half the baud rate. During diagnostic access in data mode, the interrupts occur at the baud rate.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
(None)	Receiver Configuration	1:6:0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are: **Configuration Code (Hex) — Receiver Configuration** 18 — Bell 208/201 Auto Configuration* 12 — Bell 208A/B 10 — V.26B/Bell 201C 22 — V.27 4800 Long 21 — V.27 2400 Long 02 — V.27 4800 Short 01 — V.27 2400 Short 15 — V.26A 2400 11 — V.26 1200 08 — Tone Detector *When this configuration is selected, the receiver will detect a Bell 208 or V.26B/Bell 201C handshake and configure itself accordingly. After writing the auto configuration code 18h in RCONF, the DSP will change the code to a 16(hex). If a Bell 208 carrier is received, the modem will auto configure itself accordingly and the configuration code will remain a 16(hex). However, if a Bell 201 carrier is received, the modem will auto configure itself to Bell 201 and change the receiver configuration code to a 14(hex).

Table 7. R208/201 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	Receiver Data	1:0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data. When using receiver parallel data mode, the registers 1:3 through 1:0 can not be used for reading the chip 1 RAM.
RPDM	Receiver Parallel Data Mode	1:7:4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1:0) as well as to the hardware serial data output. (See Receiver Data)
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective. Worst case setup time is 2 baud times.
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0. RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receiver Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one.
RTDIS	Receiver Training Disable	1:7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state.
RTH	Receiver Threshold Field	1:7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** / **RLSD On** / **RLSD Off** 0 / > –43 dBm / < –48 dBm 1 / > –33 dBm / < –38 dBm 2 / > –26 dBm / < –31 dBm 3 / > –16 dBm / < –21 dBm
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector tone is 30 ms long rather than 185 ms.
SQH	Receiver Squelch	1:F:7	When control bit SQH is set to a one, the receiver is squelched, $\overline{RLSD}$ is turned off and RXD is clamped to all marks.
SWRT	Sample Write	1:7:3	When control bit SWRT is a one, the RAM write operation is enabled for chip 1.
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one. During a RAM access in chip 0, when TBA is a one the host can perform either a RAM read or write depending on the state of bit 0:6:3 (see Transmitter Configuration).
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.

Table 7. R208/201 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL — Transmitter Analog Output* — TLVL — Transmitter Analog Output*** 0 — −1 dBm ±1 dB — 4 — −9 dBm ±1 dB 1 — −3 dBm ±1 dB — 5 — −11 dBm ±1 dB 2 — −5 dBm ±1 dB — 6 — −13 dBm ±1 dB 3 — −7 dBm ±1 dB — 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-on-Data	1:6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-data.
$\overline{\text{TONE}}$	Tone Detect	1:9:2	$\overline{\text{TONE}}$ indicates with a zero the presence of energy in the 345–650 ± 10 Hz frequency range. For call progress purposes, the user may determine which tone is present by determining the duty cycle of the $\overline{\text{TONE}}$ bit.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0). When TPDM is a zero channel data from the serial hardware input TXD is accepted and the chip 0 RAM access is enabled.
(None)	Transmitter Configuration*	0:6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB.) *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration Code (Hex)* — Configuration** 32 — Bell 208A/B Long 12 — Bell 208A/B Short 10 — V.26B/Bell 201C 22 — V.27 4800 Long 02 — V.27 4800 Short 21 — V.27 2400 Long 01 — V.27 2400 Short 15 — V.26 2400 11 — V.26 1200 80 — Tone Transmit 04 — DTMF Tone Transmit ***Note:** Bit 3 of the transmitter configuration register is used in the RAM access operation for chip 0 (see bit TWRT). **Configuration Definitions** Definitions of the eight Transmitter Configurations are: 1. *Bell 208.* When any of the Bell 208 configurations are selected, the modem operates as specified in the Bell 208A/B Standard. 2. *V.26B/Bell 201C.* When V.26B/Bell 201C is selected, the modem operates as specified in the V.26B/Bell 201C Standard. RTS/CTS time is programmable. 3. *V.27.* When any of the V.27 configurations are selected, the modem operates as specified in CCITT Recommendation V.27 ter. 4. *V.26.* When any of the V.26 configurations are selected, the modem operates as specified in CCITT Recommendation V.26. RTS/CTS time is programmable. 5. *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by two registers in the host interface memory space containing the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%. 6. *DTMF Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a Dual Tone Multi-Frequency (DTMF) tone specified by the code loaded in the Dial Digit Register (DDR, 0:0). The twelve codes, their associated dial digits and tone pairs are as follows:

Table 7. R208/201 Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Dial Digit Register (DDR) Hexadecimal Code</th><th>Dial Digit</th><th colspan="2">Tone Pair (Hz)</th></tr>
<tr><td>00</td><td>0</td><td>941</td><td>1336</td></tr>
<tr><td>01</td><td>1</td><td>697</td><td>1209</td></tr>
<tr><td>02</td><td>2</td><td>697</td><td>1336</td></tr>
<tr><td>03</td><td>3</td><td>697</td><td>1477</td></tr>
<tr><td>04</td><td>4</td><td>770</td><td>1209</td></tr>
<tr><td>05</td><td>5</td><td>770</td><td>1336</td></tr>
<tr><td>06</td><td>6</td><td>770</td><td>1477</td></tr>
<tr><td>07</td><td>7</td><td>852</td><td>1209</td></tr>
<tr><td>08</td><td>8</td><td>852</td><td>1336</td></tr>
<tr><td>09</td><td>9</td><td>852</td><td>1477</td></tr>
<tr><td>0A</td><td>★</td><td>941</td><td>1209</td></tr>
<tr><td>0B</td><td>#</td><td>941</td><td>1477</td></tr>
</table>
Figure 6 shows the utilization of the DTMF Tone Transmit configuration in an auto dialing application.
</td></tr>
<tr><td>(None)</td><td>Transmitter; DDR; RAM Data YTL</td><td>0:0:0–7</td><td>
1. The host processor transmits data in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

NOTE
Data is transmitted bit zero first

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Bell 208A/B V.27 4800</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>Bell 201C, V.26, V.27 2400</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table>
2. Register 0.0 is used to transmit DTMF digits when the transmitter is configured in the DTMF tone transmit mode.

3. Register 0·0 is a RAM data register used for reading or writing the least significant byte of the 16-bit Y word in Chip 0 when TPDM is a zero and no tone or DTMF tone transmission is occurring.
</td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>TWRT</td><td>Transmitter Write</td><td>0:6:3</td><td>When control bit TWRT is a one, the RAM write operation is enabled for chip 0.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>1:7:1</td><td>When control bit T2 is a one, an adaptive equalizer with two taps per baud is used. When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a one, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A. The clock appearing at the XTCLK input will appear at the TDCLK output.</td></tr>
</table>

Table 8. RAM Access Codes

No.	Function	Chip	X Access Code (Hex)	Y Access Code (Hex)	Register
1	DTMF Low Frequency Amplitude[1]	0	—	88	0,1
2	DTMF High Frequency Amplitude[1]	0	—	08	0,1
3	Interdigit Delay[1]	0	—	89	0,1
4	DTMF Tone Duration[1]	0	—	09	0,1
5	Received Signal Samples	1	C0	Not Used	2,3
6	Demodulator Output	1	D3	53	0,1,2,3
7	Low Pass Filter Output	1	D4	54	0,1,2,3
8	Average Energy	1	DC	Not Used	2,3
9	AGC Gain Word	1	81	Not Used	2,3
10	Equalizer Input	2	C0	40	0,1,2,3
11	Equalizer Tap Coefficients	2	81 – A0	01 – 20	0,1,2,3
12	Unrotated Equalizer Output	2	E1	61	0,1,2,3
13	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
14	Decision Points Ideal Points	2	E2	62	0,1,2,3
15	Error	2	E3	63	0,1,2,3
16	Rotation Angle	2	Not Used	00	0,1
17	Frequency Correction	2	AA	Not Used	2,3
18	EQM	2	A7	Not Used	2,3
19	Dual Point	2	AE	2E	0,1,2,3
20	Unscrambled Synchronizing Segment	0	—	93	0,1
21	Scrambled Synchronizing Segment	0	—	13	0,1

Bell 201C and V.26 Programmable Turn-On Sequence

The turn-on sequence for Bell 201C and V.26 modes is composed of two segments. The first segment consists of unscrambled mark. The second sequence consists of scrambled mark. The segments may be independently programmed for a desired length of time.

When Bell 201C or V.26 mode is chosen, the default RTS-CTS delay is 26.6 ms of unscrambled mark and no scrambled segment. If using only the unscrambled segment, DDIS and SDIS must be set to a 1.

RTS-CTS delay = (unscrambled + scrambled) baud times ± 1 baud time)

1 baud time = 1/1200 = 0.833 ms

Total minimum time recommended = 15 ms.
Total maximum time = 900 ms.

Turn-on word = (time in ms / 0.833) – 1, convert to hex and subtract from FFFF. Write this value into registers 1 & 0 of chip 0.

For example, for a RTS-CTS delay of 150 ms:

(150 / 0.833) – 1 = 179 (decimal) = B3 (hex), FFFF – B3 = FF4C

Write FF into register 1 and write 4C into register 0 using the appropriate access code listed in Table 8. (See interface memory section for RAM Write procedure.)

Note: When using both unscrambled and scrambled segments, the unscrambled segment should be limited to 10 ms or less for compatibility with existing V.26 modems.

Auto Dial Sequence

The Figure 6 flowchart defines the auto dial sequence via the microprocessor interface memory. The modem timing for the auto dialer accounts for DTMF tone duration and interdigit delay. The default tone duration is 95 ms and the default interdigit delay is 71 ms. The default amplitudes for the high and low frequencies are – 4 dBm and – 6 dBm, respectively. The above four parameters can be changed by performing a RAM write.

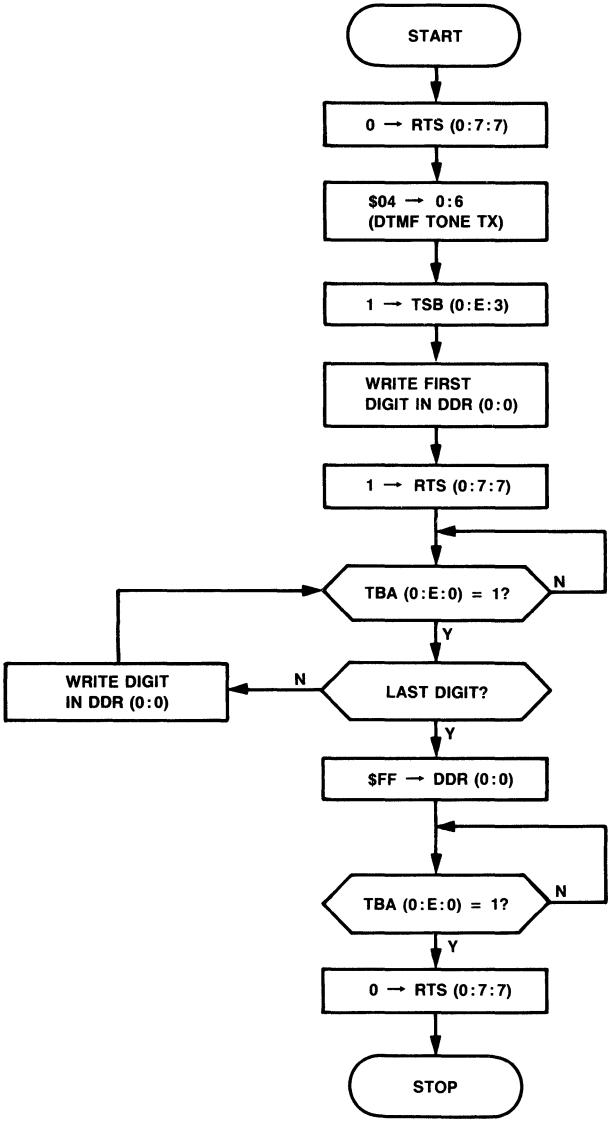


Figure 6. R208/201 Auto Dial Sequence

PERFORMANCE

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

Typical BER performance is shown in Figure 7. The BER curves shown in Figure 7 were prepared from data obtained using a TAS 1010 test system.

TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

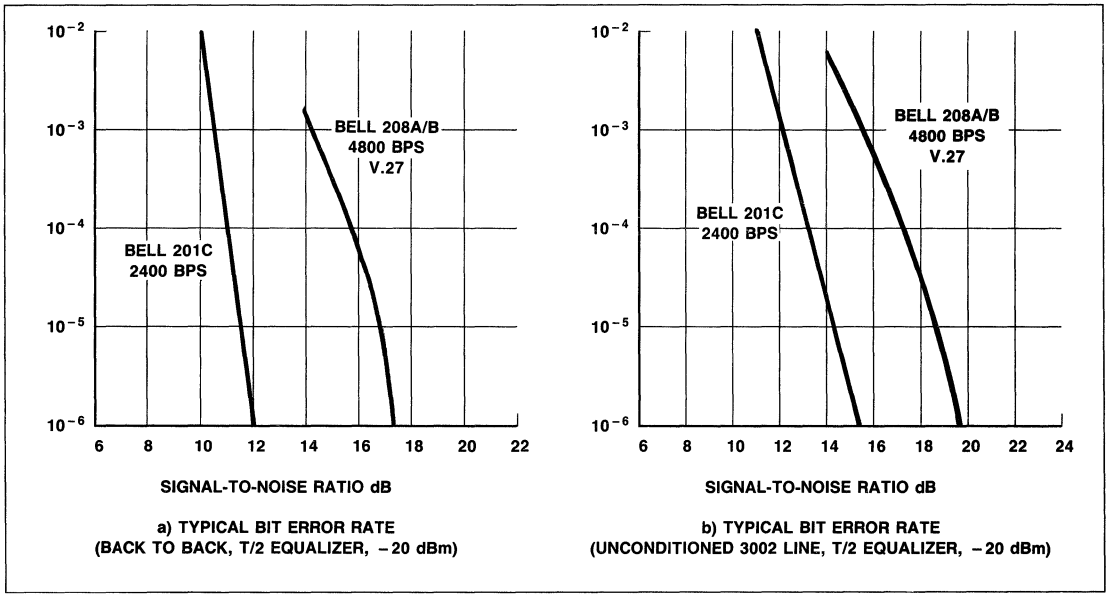


Figure 7. R208/201 BER versus SNR

GENERAL SPECIFICATIONS

Table 9. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	700 mA
+12 Vdc	±5%	5 mA	10 mA
−12 Vdc	±5%	25 mA	50 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Table 10. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 11. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.94 in. (100 mm)
Length	4.725 in. (120 mm)
Connector Height	0.437 in. (11.1 mm)
Component Height	
Top (max.)	0.300 in (7.6 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max):	3.6 oz. (100 g)
Lead Extrusion (max.):	0.100 in. (2.54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.228 in. (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0.300 in. (7.6 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.53 in. (13.5 mm)
Micromodem Version	
Board Structure:	Single PC board with 60 pins in a dual in-line pin configuration. Row 1 has 29 pins (pins 1 through 30 with pin 15 deleted for keying). Row 2 has 31 pins (pins 31 through 61 with pin 31 offset from pin 1 for keying).
Dimensions:	
Width	2.559 in. (65 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0.300 in (7.6 mm)
Bottom (max.)	0.100 in. (2.54 mm)
Weight (max.):	2.5 oz. (70 g))
Pin Length (max.)	0.433 in. ±0.015 in. (11.0 ±0.4 mm), gold plated

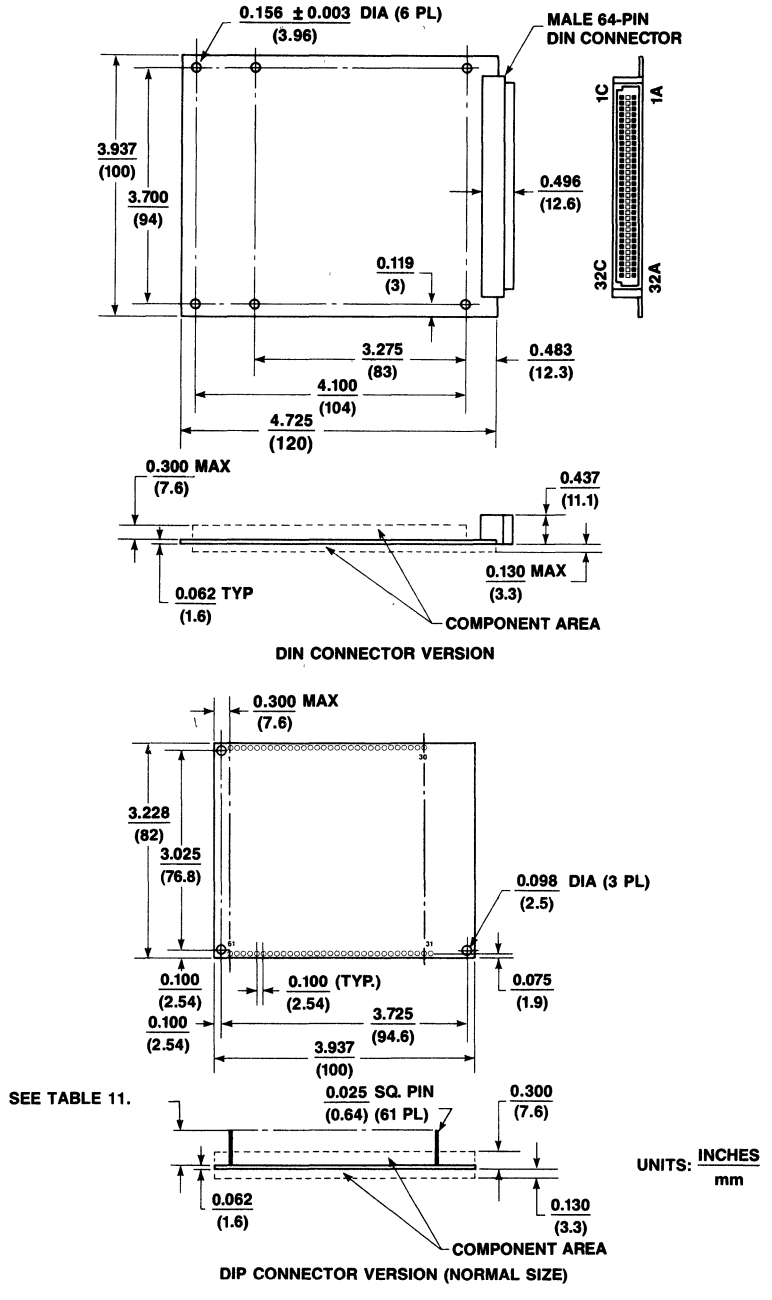


Figure 8. R208/201 Modem Dimensions and Pin Locations

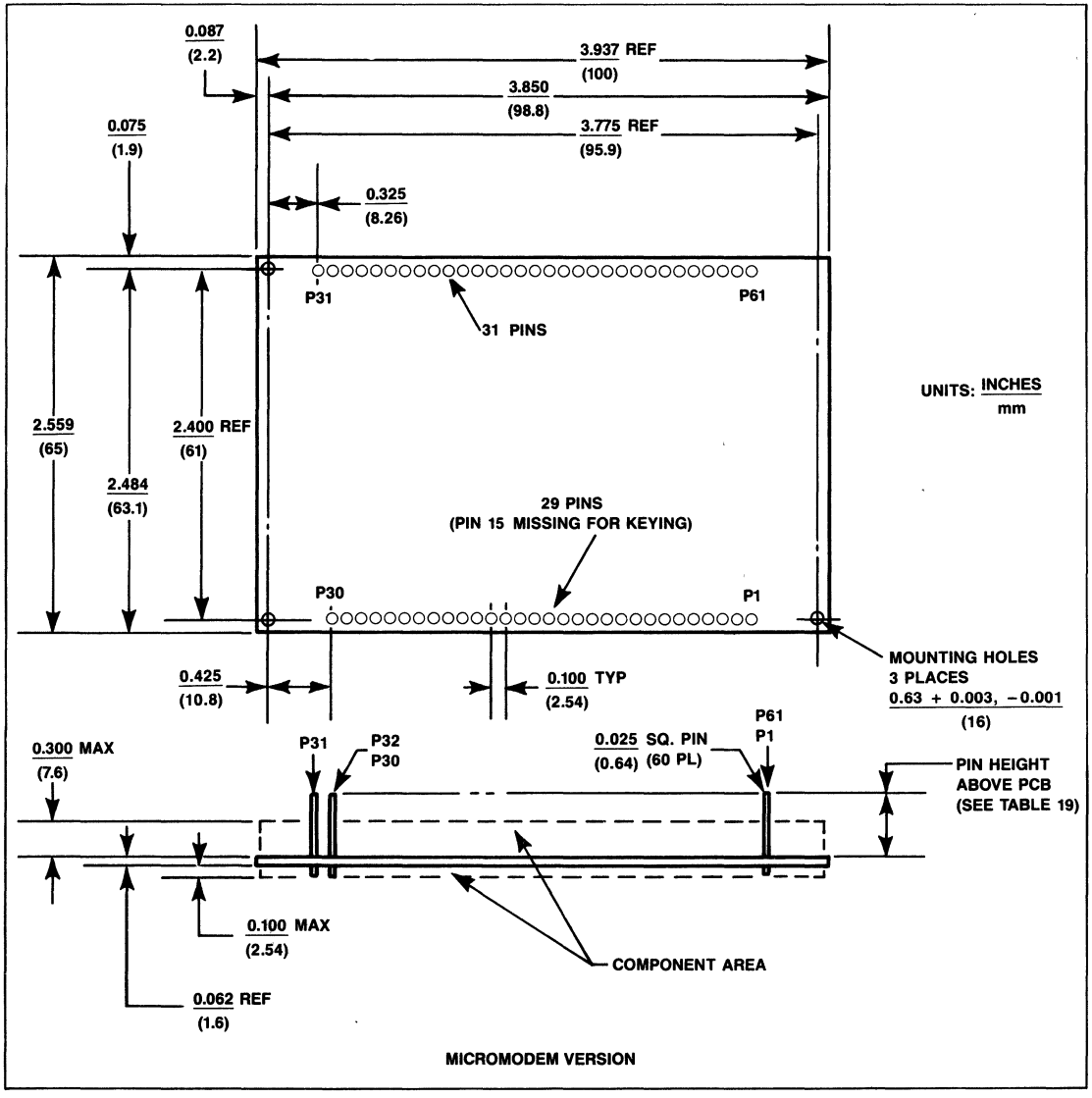


Figure 8. R208/201 Modem Dimensions and Pin Locations (Continued)

Rockwell

R96DP
9600 bps Data Pump Modem

INTRODUCTION

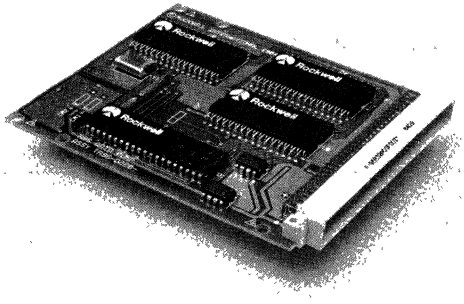
The Rockwell R96DP is a synchronous 9600 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) as well as leased lines through the appropriate line termination.

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29 and V.27 bis/ter. The R96DP can operate at speeds of 9600, 7200, 4800, and 2400 bps. Employing advanced signal processing techniques, the R96DP can transmit and receive data even under extremely poor line conditions.

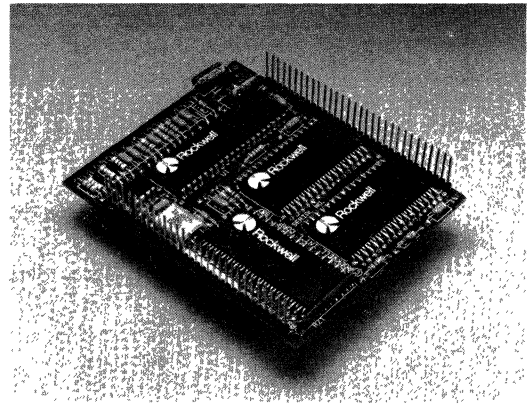
The R96DP is designed for use in point-to-point environments. User programmable features allow the modem operation to be tailored to support a wide variety of functional requirements. The modem's small size, low power consumption, and serial/parallel host interface simplify system design and allow installation in a compact enclosure. The modem module is available with a DIN connector for connection to a mating connector or with dual-in-line pins (DIP) for direct plug-in installation onto a host module.

FEATURES

- CCITT V.29, V.27 bis/ter Compatible
- Point-to-Point Applications
- 2-Wire Half-Duplex, 4-Wire Full-Duplex
- Programmable Tone Generation
- Programmable DTMF Tone Dialer
- Dynamic Range: – 43 dBm to 0 dBm
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C)(Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Diagnostic Capability
- Programmable Transmit Output Level
- Loopbacks
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — DIN Connector Version: 100 mm × 120 mm (3.94 in. × 4.73 in.)
  - — DIP Connector Version: 82 mm × 100 mm (3.23 in. × 3.94 in.)
- Power Consumption: 3 W (Typical)



R96DP DIN Connector Version



R96DP DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

The transmitter carrier frequencies supported by the R96DP are listed in Table 1.

Table 1. Transmitter Carrier Frequencies

Function	Frequency (Hz ±0.01%)
V.27 bis/ter Carrier	1800
V.29 Carrier	1700

TONE GENERATION

Under control of the host processor, the R96DP can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. DTMF tone transmission capability is provided to allow the modem to operate as a programmable DTMF tone dialer.

SIGNALING AND DATA RATES

The signaling and data rates supported by the R96DP are listed in Table 2.

Table 2. Signaling/Data Rates

Specification	Baud Rate (Symbols/sec.)	Bits Per Baud	Data Rate (bps)(±0.01%)	Symbol Points
V.29	2400	4	9600	16
V.29	2400	3	7200	8
V 29	2400	2	4800	4
V 27	1600	3	4800	8
V.27	1200	2	2400	4

DATA ENCODING

The R96DP data encoding conforms to CCITT recommendations V.29 and V.27 bis/ter.

EQUALIZERS

The R96DP provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent
3. *2400 Baud.* Square root of 20 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96DP incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96DP can adapt to received frequency error of up to ± 10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

TRANSMIT LEVEL

The transmitter output level is accurate to ± 1.0 dB and is programmable from −1.0 dBm to −15.0 dBm in 2 dB steps.

TRAIN ON DATA

When train on data is enabled, the receiver typically trains on data in less than 15 seconds for V.29 and 3.5 seconds for V.27.

TURN-ON SEQUENCE

Selectable turn-on sequences can be generated as defined in Table 3.

Table 3. Turn-On Sequences

Specification	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector* Tone Enabled
V.29 (All data rates)	253 ms	438 ms
V.27 4800 bps long	708 ms	913 ms
V 27 4800 bps short	50 ms	255 ms
V 27 2400 bps long	943 ms	1148 ms
V 27 2400 bps short	67 ms	272 ms

* For short echo protector tone, subtract 155 ms from $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ turn-on time

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, diagnostic signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The six groups of hardware circuits are described in the following paragraphs. Table 5 lists the digital interface characteristics.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{\text{POR}}$) causes the modem to assume a valid operational state. The modem drives $\overline{\text{POR}}$ to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of $\overline{\text{POR}}$, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{\text{POR}}$ low for at least 3 μs. When an external low input is applied to $\overline{\text{POR}}$, the modem is ready for normal use approximately 10 ms after the low input is removed. $\overline{\text{POR}}$ is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The R96DP POR sequence leaves the modem configured as follows:

- 9600 bps
- Serial channel data
- T/2 equalizer
- Standard echo protector tone
- −43 dBm threshold
- Cable and link equalizers disabled
- Train-On-Data disabled

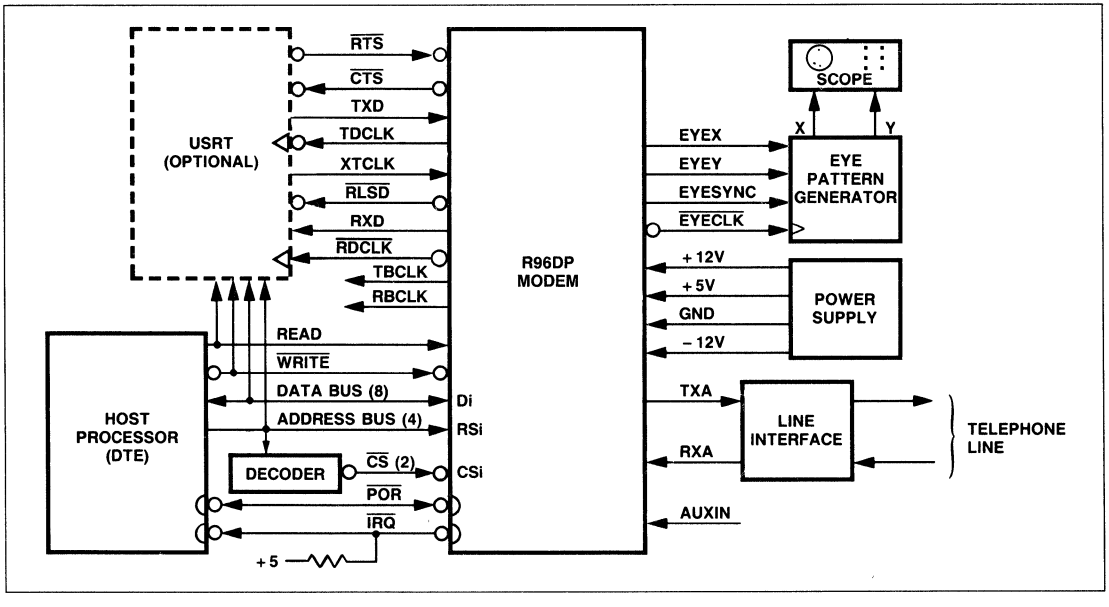


Figure 1. R96DP Functional Interconnect Diagram

Table 4. R96DP Hardware Circuits

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
A. OVERHEAD:				
Ground (A)	AGND	31C,32C	30,31	Analog Ground Return
Ground (D)	DGND	3C,8C, 5A,10A	29,37,53	Digital Ground Return
+5 volts	PWR	19C,23C, 26C,30C	1,45,61	+5 volt supply
+12 volts	PWR	15A	32	+12 volt supply
−12 volts	PWR	12A	36	−12 volt supply
$\overline{POR}$	I/OB	13C	2	Power-on-reset
B. MICROPROCESSOR INTERFACE:				
D7	I/OA	1C	3	Data Bus (8 Bits)
D6	I/OA	1A	4	
D5	I/OA	2C	5	
D4	I/OA	2A	6	
D3	I/OA	3A	7	
D2	I/OA	4C	8	
D1	I/OA	4A	9	
D0	I/OA	5C	10	
RS3	IA	6C	16	Register Select (4 Bits)
RS2	IA	6A	17	
RS1	IA	7C	18	
RS0	IA	7A	19	
$\overline{CS0}$	IA	10C	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	13	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	12C	14	Read Enable
$\overline{WRITE}$	IA	11A	12	Write Enable
$\overline{IRQ}$	OB	11C	11	Interrupt Request

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
C. V.24 INTERFACE:				
$\overline{RDCLK}$	OC	21A	23	Receive Data Clock
TDCLK	OC	23A	46	Transmit Data Clock
XTCLK	IB	22A	51	External Transmit Clock
$\overline{RTS}$	IB	25A	50	Request-to-Send
$\overline{CTS}$	OC	25C	49	Clear-to-Send
TXD	IB	24C	48	Transmitter Data
$\overline{RXD}$	OC	22C	26	Receiver Data
$\overline{RLSD}$	OC	24A	27	Received Line Signal Detector
D. ANCILLARY CIRCUITS:				
RBCLK	OC	26A	22	Receiver Baud Clock
TBCLK	OC	27C	47	Transmitter Baud Clock
E. ANALOG SIGNALS:				
TXA	AA	31A	34	Transmitter Analog Output
RXA	AB	32A	33	Receiver Analog Input
AUXIN	AC	30A	—	Auxiliary Analog Input
F. DIAGNOSTIC:				
EYEX	OC	15C	56	Eye Pattern Data—X Axis
EYEY	OC	14A	55	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	57	Eye Pattern Clock
EYESYNC	OA	13A	58	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 5 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. Pins not used on the DIP Version: 15, 24, 25, 28, 35, 38, 39, 40, 41, 42, 43, 44, 52, 54, 59, 60
3. Unusd inputs tied to +5V or ground require individual 10K Ω series resistors.

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I Load = 0.36 mA

This configuration is suitable for performing high speed data transfer using the serial data port. Individual features are discussed in subsequent paragraphs.

V.24 INTERFACE

Eight hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, + 5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The responses to $\overline{RTS}$ are shown in Table 6.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON condition of $\overline{RTS}$ are shown in Table 6.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in data state is a maximum of 2 band times for all configurations.

Table 6. $\overline{RTS}$-$\overline{CTS}$ Response Times

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector* Tone Enabled
V.29 (All data rates)	253 ms	438 ms
V.27 4800 bps long	708 ms	913 ms
V.27 4800 bps short	50 ms	255 ms
V.27 2400 bps long	943 ms	1148 ms
V.27 2400 bps short	67 ms	272 ms

* For short echo protector tone, subtract 155 ms from $\overline{RTS}$-$\overline{CTS}$ turn-on time.

Received Line Signal Detector ($\overline{RLSD}$)

For V.27 bis/ter or V.29, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ± 10 ms. The RLSD on-to-off response time for V.27 is 10 ± 5 ms and for V.29 is 30 ± 9 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on the threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

1. Greater than – 43 dBm (RLSD on)
   Less than – 49 dBm (RLSD off)
2. Greater than – 33 dBm (RLSD on)
   Less than – 38 dBm (RLSD off)
3. Greater than – 26 dBm (RLSD on)
   Less than – 31 dBm (RLSD off)
4. Greater than – 16 dBm (RLSD on)
   Less than – 21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than – 43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with an unmodulated 2400 Hz tone applied to the receiver's audio input (RXA).

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, or 2400 Hz (± 0.01%).
2. *Duty Cycle.* 50 ± 1%.

TDCLK is provided to the user in synchronous communications for USRT timing. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{RDCLK}$)

The modem provides a Receive Data Clock ($\overline{RDCLK}$) output in the form of a 50 ± 1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. $\overline{RDCLK}$ is provided to the user in synchronous communications for USRT timing. The timing recovery circuit is capable of tracking a ± .01% frequency error in the associated transmit timing source.

MICROPROCESSOR INTERFACE

Eight hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$-$\overline{CS2}$) and Register Selects (RS0-RS3)

The signal processor to be accessed is selected by grounding one of three unique chip select lines, $\overline{CS2}$, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable (READ) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

ANALOG SIGNALS

The analog signal characteristics are described in Table 7.

Table 7. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is the TLVL setting +0.6 dB −1.4 dB.

Transmitter Analog (TXA)

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

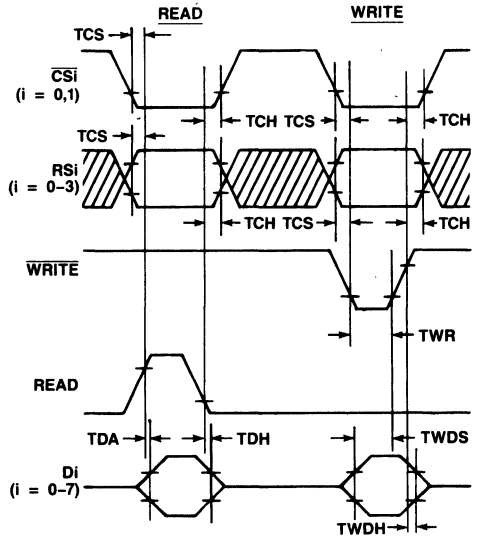
Receiver Analog (RXA)

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may take the form of back-to-back zener diodes across the transformer or a varistor across the transformer.

Auxiliary Input (AUXIN)

AUXIN provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit at a rate of 9600 samples-per-second. Any signal above 4800 Hz on the AUXIN line will be aliased back into the passband as noise. One application for AUXIN is to inject dual-tone multifrequency (DTMF) touch-tone signals for dialing, however, the source of these tones must be well filtered to eliminate components above 4800 Hz. The input impedance of AUXIN is 1K ohm. The gain from AUXIN to TXA is the same as the selected transmit level +0.6 dB −1.4 dB.



Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
$\overline{CSi}$, RSi hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

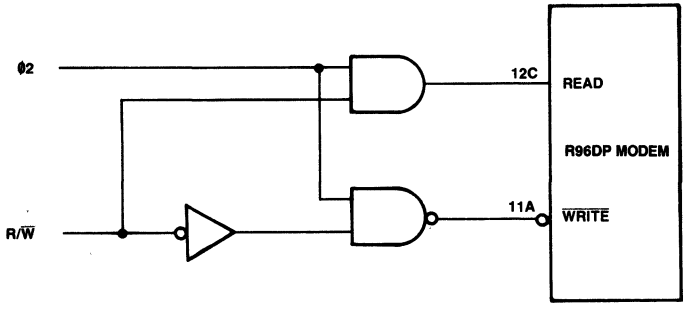


Figure 3. R/$\overline{W}$ to READ $\overline{WRITE}$ Conversion Logic

DIAGNOSTIC SIGNALS
EYEX, EYEY, EYECLK, and EYESYNC

Four card edge connections provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

The outputs EYEX and EYEY provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. Since this data is in serial digital form it must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two D/A converters. A clock for use by the serial-to-parallel converters is furnished by signal EYECLK. A strobe for loading the D/A converters is furnished by signal EYESYNC. Timing of these signals is illustrated in Figure 4. The EYEX and EYEY outputs furnish 9-bit serial words. Since most serial to parallel conversion logic is designed for 8-bit words, an extra storage flip-flop is required for 9-bit resolution. However, the ninth bit is not generally needed for eyepattern generation, and eight-bit hardware can be used if data is copied on the rising edge of EYECLK rather than the falling edge.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Two clock signals called TBCLK and RBCLK are provided at the modem connector. These signals have no counterpart in the V.24 or RS-232 recommendations since they mark the baud interval for the transmitter and receiver rather than the data rate. The baud clocks can be useful in identifying the order of data bits in a baud (e.g., for multiplexing data, etc.). Both signals are high active, meaning the baud boundaries occur on falling edges. The first bit in each baud begins with the falling edge of the corresponding baud clock.

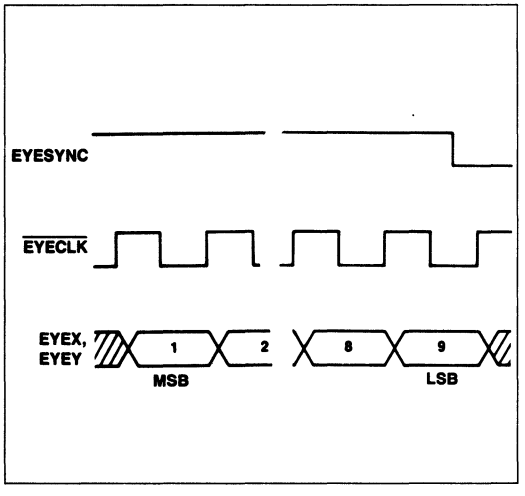


Figure 4. Eye Pattern Timing

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on three special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into areas. These areas are partitioned into transmitter, baud rate, and sample rate devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 48 addressable registers in the modem are shown in Figure 5. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Table 8 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS T							
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	RAM DATA YTM							
0	RAM DATA YTL; TRANSMITTER DATA, DDR							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RSIA	—	—	—	RSB	RSIE	—	RSDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	—	—	—
8	—	—	—	—	—	$\overline{P2DET}$	—	—
7	RTH		DDIS	RPDM	SWRT	BWRT	T2	RTDIS
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL; RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 5. Interface Memory Map

Table 8. R96DP Interface Memory Definitions

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>A3L</td><td>Amplitude 3-Link Select</td><td>0:5:1</td><td>A3L is used in conjunction with LAEN. When A3L is a one the Japanese 3 link equalizer is selected and when A3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
<tr><td>BWRT</td><td>Baud Write</td><td>1:7:2</td><td>When control bit BWRT is a one, the RAM write operation is enabled for Chip 2.</td></tr>
<tr><td>CEQ</td><td>Cable Equalizer Field</td><td>0:5:4,5</td><td>The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following tables list the possible cable equalizer selection codes and responses.
<table>
<tr><th>CEQ</th><th>Cable Length (0.4 mm diameter)</th></tr>
<tr><td>0</td><td>0.0</td></tr>
<tr><td>1</td><td>1.8 km</td></tr>
<tr><td>2</td><td>3.6 km</td></tr>
<tr><td>3</td><td>7.2 km</td></tr>
</table>
Cable Equalizer Nominal Gain
CEQ CODE 1
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−0.99</td><td>−0.94</td></tr>
<tr><td>1500</td><td>−0.20</td><td>−0.24</td></tr>
<tr><td>2000</td><td>+0.15</td><td>+0.31</td></tr>
<tr><td>3000</td><td>+1.43</td><td>+1.49</td></tr>
</table>
CEQ CODE 2
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−2.39</td><td>−2.67</td></tr>
<tr><td>1500</td><td>−0.65</td><td>−0.74</td></tr>
<tr><td>2000</td><td>+0.87</td><td>+1.02</td></tr>
<tr><td>3000</td><td>+3.06</td><td>+3.17</td></tr>
</table>
CEQ CODE 3
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−3.93</td><td>−3.98</td></tr>
<tr><td>1500</td><td>−1.22</td><td>−1.20</td></tr>
<tr><td>2000</td><td>+1.90</td><td>+1.81</td></tr>
<tr><td>3000</td><td>+4.58</td><td>+4.38</td></tr>
</table>
Unless a problem with training or high bit error rate is encountered, most applications operate successfully with no cable equalizer selected.</td></tr>
<tr><td>$\overline{\text{CDET}}$</td><td>Carrier Detector</td><td>1:B:0</td><td>When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$. If the $\overline{\text{FED}}$ bit goes to a zero and no P2 sequence is detected, the $\overline{\text{CDET}}$ bit goes to zero within 5 to 25 ms indicating that the receiver has entered the data state without a training sequence.</td></tr>
<tr><td>DDIS</td><td>Descramble Disable</td><td>1:7:5</td><td>When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.</td></tr>
<tr><td>DDR</td><td>Dial Digit Register</td><td>0:0:0–7</td><td>DDR is used to tell the modem which DTMF digit to transmit (see Transmitter Data).</td></tr>
<tr><td>D3L</td><td>Delay 3-Link Select</td><td>0:5:0</td><td>D3L is used in conjunction with LDEN When D3L is a one the Japanese 3 link equalizer is selected and when D3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
</table>

Table 8. R96DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>EPT</td><td>Echo Protector Tone</td><td>0:7:3</td><td>When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. This option is available in the V.27 and V.29 Configurations, although it is not specified in the CCITT V 29 recommendation.</td></tr>
<tr><td>$\overline{\text{FED}}$</td><td>Fast Energy Detector</td><td>1:9:6</td><td>When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband, and the receiver is searching for the training sequence.</td></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0–7,
0:3:0–7</td><td>The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below:

FREQM Register (0:3)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr></table>
FREQL Register (0:2)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr></table>
The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%

Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below:

<table><tr><th>FREQM</th><th>FREQL</th><th>Frequency (Hz)</th></tr><tr><td>0C</td><td>52</td><td>462</td></tr><tr><td>1D</td><td>55</td><td>1100</td></tr><tr><td>2C</td><td>00</td><td>1650</td></tr><tr><td>31</td><td>55</td><td>1850</td></tr><tr><td>38</td><td>00</td><td>2100</td></tr></table></td></tr>
<tr><td>IFIX</td><td>Eye Fix</td><td>1:6:7</td><td>When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB.</td></tr>
<tr><td>LAEN</td><td>Link Amplitude Equalizer Enable</td><td>0:5:3</td><td>The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table:

<table><tr><th>LAEN</th><th>A3L</th><th>Curve Matched</th></tr><tr><td>0</td><td>X</td><td>No Equalizer</td></tr><tr><td>1</td><td>0</td><td>U.S. Survey Long</td></tr><tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr></table>
The link amplitude equalizer responses are given in the following table.

Link Amplitude Equalizer
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr><tr><td>1000</td><td>−0.27</td><td>−0.13</td></tr><tr><td>1400</td><td>−0.16</td><td>−0.08</td></tr><tr><td>2000</td><td>+0.33</td><td>+0.16</td></tr><tr><td>2400</td><td>+1.54</td><td>+0.73</td></tr><tr><td>2800</td><td>+5.98</td><td>+2.61</td></tr><tr><td>3000</td><td>+8.65</td><td>+3.43</td></tr></table></td></tr>
</table>

Table 8. R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5:2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN / D3L / Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link The link delay equalizer responses are given in the following table. **Link Delay Equalizer** **Frequency (Hz) / Delay Relative to 1700 Hz (Microseconds): U.S. Survey Long / Japanese 3-Link** 800 / −498.1 / −653.1 1200 / −188.3 / −398.5 1600 / −15.1 / −30.0 1700 / +0.0 / +0.0 2000 / −39.8 / +11.7 2400 / −423.1 / −117.1 2800 / −672.4 / −546.3
L2ACT	Remote Digital Loopback Activate	0:4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2.
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0:4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4:5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
$\overline{\text{PNDET}}$	Period N Detector	1:B:6	When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence.
$\overline{\text{P2DET}}$	Period Two Detector	1:8:2	When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a P2 sequence has been detected. This bit sets to a one at the start of the PN sequence.
(None)	RAM Access T	0:F:0–7	Contains the RAM access code used in reading or writing chip 0 RAM locations via word Y (0:1 and 0:0).
(None)	RAM Access XB	2:5:0–7	Contains the RAM access code used in reading or writing chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access XS	1:5:0–7	Contains the RAM access code used in reading or writing chip 1 RAM locations via word X (1:3 and 1:2).
(None)	RAM Access YB	2:4:0–7	Contains the RAM access code used in reading or writing chip 2 RAM locations via word Y (2:1 and 2:0).

Table 8. R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Access YS	1:4:0–7	Contains the RAM access code used in reading or writing chip 1 RAM locations via word Y (1:1 and 1:0).
(None)	RAM Data XBL	2:2:0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 2.
(None)	RAM Data XBM	2:3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 2.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 1.
(None)	RAM Data YBL	2:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YBM	2:1:0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YSL	1:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data.'
(None)	RAM Data YSM	1:1:0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1.
(None)	RAM Data YTL	0:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 0. It is shared by parallel data mode and DTMF dialing (see Transmitter Data).
(None)	RAM Data YTM	0:1:0–7	Most significant byte of 16-byte word Y used in reading or writing locations in chip 0.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low. In idle mode the interrupts from chip 2 occur at half the baud rate. During diagnostic access in data mode, the interrupts occur at the baud rate.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
(None)	Receiver Configuration	1:6:0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are: **Configuration Code (Hex) — Receiver Configuration** 14 — V.29 9600 12 — V.29 7200 11 — V.29 4800 22 — V.27 4800 Long 21 — V.27 2400 Long 02 — V.27 4800 Short 01 — V.27 2400 Short

Table 8. R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	Receiver Data	1:0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data. When using receiver parallel data mode, the registers 1:3 through 1·0 can not be used for reading the chip 1 RAM.
RPDM	Receiver Parallel Data Mode	1:7:4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1:0) as well as to the hardware serial data output. (See Receiver Data)
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective. Worst case setup time is 2 baud times.
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0. RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receiver Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one.
RTDIS	Receiver Training Disable	1:7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state.
RTH	Receiver Threshold Field	1:7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH / RLSD On / RLSD Off** 0 / > –43 dBm / < –48 dBm 1 / > –33 dBm / < –38 dBm 2 / > –26 dBm / < –31 dBm 3 / > –16 dBm / < –21 dBm
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector tone is 30 ms long rather than 185 ms.
SWRT	Sample Write	1:7:3	When control bit SWRT is a one, the RAM write operation is enabled for chip 1.
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one. During a RAM access in chip 0, when TBA is a one the host can perform either a RAM read or write depending on the state of bit 0:6:3 (see Transmitter Configuration).
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.

Table 8. R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** — **Transmitter Analog Output*** 0 — −1 dBm ±1 dB 1 — −3 dBm ±1 dB 2 — −5 dBm ±1 dB 3 — −7 dBm ±1 dB 4 — −9 dBm ±1 dB 5 — −11 dBm ±1 dB 6 — −13 dBm ±1 dB 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-on-Data	1:6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-date.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0). When TPDM is a zero channel data from the serial hardware input TXD is accepted and the chip 0 RAM access is enabled.
(None)	Transmitter Configuration*	0:6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB.) *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration Code (Hex)*** — **Transmitter Configuration** 14 — V.29 9600 12 — V.29 7200 11 — V.29 4800 22 — V.27 4800 Long 21 — V.27 2400 Long 02 — V.27 4800 Short 01 — V.27 2400 Short 80 — Tone Transmit 40 — DTMF Tone Transmit ***Note:** Beginning with the R5304-22 device, bit 3 of the transmitter configuration register is used in the RAM access operation for chip 0. When 0:6:3 is a one, a RAM write operation will occur when TPDM is a zero, and when 0:6:3 is a zero, a RAM read operation will occur when TPDM is a zero **Configuration Definitions** Definitions of the eight Transmitter Configurations are: 1. V.29. When a V.29 configuration has been selected, the modem operates as specified in the CCITT Recommendation V.29. 2. V.27. When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3. Tone Transmit. In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by two registers in the host interface memory space containing the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%. 4. DTMF Tone Transmit. In this configuration when the hex value of a DTMF digit is stored in register 0:0, a DTMF tone will be transmitted if RTS is enabled.

Table 8. R96DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter; DDR; RAM Data YTL</td><td>0:0:0–7</td><td>1. The host processor transmits data in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

NOTE

Data is transmitted bit zero first.

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.29 9600 bps</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.29 7200 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.29 4800 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="4">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table>
2. Register 0:0 is used to transmit DTMF digits when the transmitter is configured in the DTMF tone transmit mode.

3. Register 0:0 is a RAM data register used for reading or writing the least significant byte of the 16-bit Y word in Chip 0 when TPDM is a zero and no tone or DTMF tone transmission is occurring.</td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>1:7:1</td><td>When control bit T2 is a one, an adaptive equalizer with two taps per baud is used. When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a one, the transmitter timing is established by the external clock supplied at the hardware input XTCLK. The clock appearing at the XTCLK input will appear at the TDCLK output.</td></tr>
</table>

SIGNAL PROCESSOR RAM ACCESS

RAM and Data Organization

Each signal processor contains 128 words of random access memory (RAM). Each word is 32 bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16 bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. In the sample rate and baud rate devices the entire contents of XRAM and YRAM may be read from or written into by the host processor via the microprocessor interface. Access to the YRAM is possible only in the transmitter device.

Interface Memory

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit determines the RAM address to read from or write into by the code stored in the RAM ACCESS bits of interface memory registers. The SP logic unit normally transfers a word from RAM to interface memory once each cycle of the device code. Each RAM word transferred to the interface memory is 32 bits long (16 bits in the transmitter). These bits are written by the SP logic unit into interface memory registers 3, 2, 1, and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data, respectively. As previously described for parallel data mode, the data available bits set to a one when register 0 of the respective signal processor is written into by the device and resets to a zero when register 0 is read from by the host. Since the parallel data mode transmitter and receiver data register shares register 0 with the YRAM data, chip 0 and 1 RAM access are disabled in parallel data mode. However, chip 2 RAM access remains active in receiver parallel data mode.

The transmitter, sample rate device and the baud rate device allow data to be transferred from interface memory to RAM. When set to a one, bit SWRT (1:7:3) signals the chip 1 SP logic unit to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. Bit BWRT (1:7:2) performs the same function for chip 2 RAM. When writing into the RAM, 32 bits are transferred. The 16 bits written into XRAM come from registers 3 and 2, with register 3 being the more significant byte. The 16 bits written into YRAM come from registers 1 and 0, with register 1 being the more significant byte. When only 16 bits of data are to be written, FF (a dummy RAM location) must be stored in RAM ACCESS XS or RAM ACCESS YS to prevent writing the insignificant 16 bits of registers 1:3 through 1:0 into a valid RAM location. When the host processor writes into register 1:0 the RSDA bit (1:E:0) is reset to zero. When the SP logic unit reads data from register 1:0, the RSDA bit (1:E:0) is set to a one. In a similar manner, bit RBDA (2:E:0) resets to zero when the host processor writes into register 2:0 and sets to a one when the SP logic unit reads data from register 2:0.

When reading from RAM, or writing into RAM, the bits in registers 0:E, 1:E, 2:E can be used for handshaking or interrupt functions as in parallel data mode. When not in parallel data mode, the bits in register 1:E perform the handshake and interrupt functions for RAM access. In both serial and parallel data modes, the bits in register 2:E perform handshake and interrupt functions for RAM access. When set to one, bit RBIE (2:E:2) enables RBDA to drive the IRQ connector signal to zero volts when RBDA is a one. Bit RBIA (2:E:7) identifies chip 2, the baud rate device, as a source of IRQ interrupt. Bit RBIA is a one when both RBIE and RBDA are set to one. In the event that other system elements may cause IRQ to be driven low, the host must determine if modem chip 2 is causing an interrupt by reading RBIA.

Table 9 provides the available RAM access functions, codes, and registers.

Auto Dial Sequence

The Figure 6 flowchart defines the auto dial sequence via the microprocessor interface memory. The modem timing for the auto dialer accounts for DTMF tone duration and interdigit delay. The default tone duration is 95 ms and the default interdigit delay is 71 ms. The default amplitudes for the high and low frequencies are – 4 dBm and – 6 dBm, respectively. The above four parameters can be changed by performing a RAM write.

Table 9. RAM Access Codes

No.	Function	Chip	X Access Code (Hex)	Y Access Code (Hex)	Register
1	DTMF Low Frequency Amplitude[1]	0	—	88	0,1
2	DTMF High Frequency Amplitude[1]	0	—	08	0,1
3	Interdigit Delay[1]	0	—	89	0,1
4	DTMF Tone Duration[1]	0	—	09	0,1
5	Received Signal Samples	1	C0	Not Used	2,3
6	Demodulator Output	1	C2	42	0,1,2,3
7	Low Pass Filter Output	1	D4	54	0,1,2,3
8	Average Energy	1	DC	Not Used	2,3
9	AGC Gain Word	1	81	Not Used	2,3
10	Equalizer Input	2	C0	40	0,1,2,3
11	Equalizer Tap Coefficients	2	81 – A0	01 – 20	0,1,2,3
12	Unrotated Equalizer Output	2	E1	61	0,1,2,3
13	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
14	Decision Points Ideal Points	2	E2	62	0,1,2,3
15	Error	2	E3	63	0,1,2,3
16	Rotation Angle	2	Not Used	00	0,1
17	Frequency Correction	2	AA	Not Used	2,3
18	EQM	2	A7	Not Used	2,3
19	Dual Point	2	AE	2E	0,1,2,3

Note: 1. Added in transmitter device R5304-22.

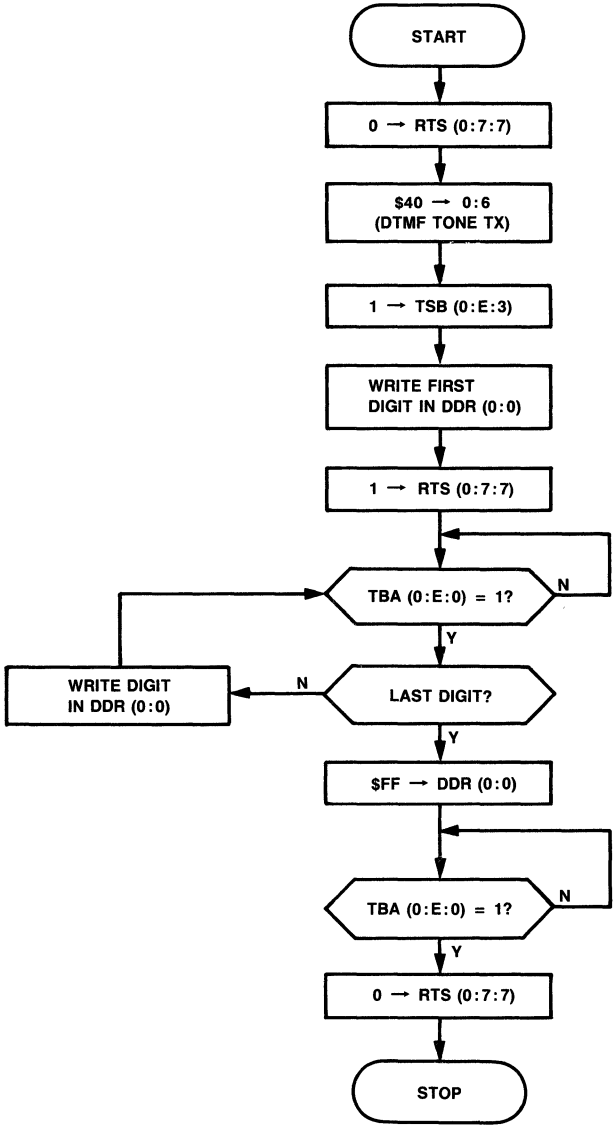


Figure 6. R96DP Auto Dial Sequence

PERFORMANCE

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

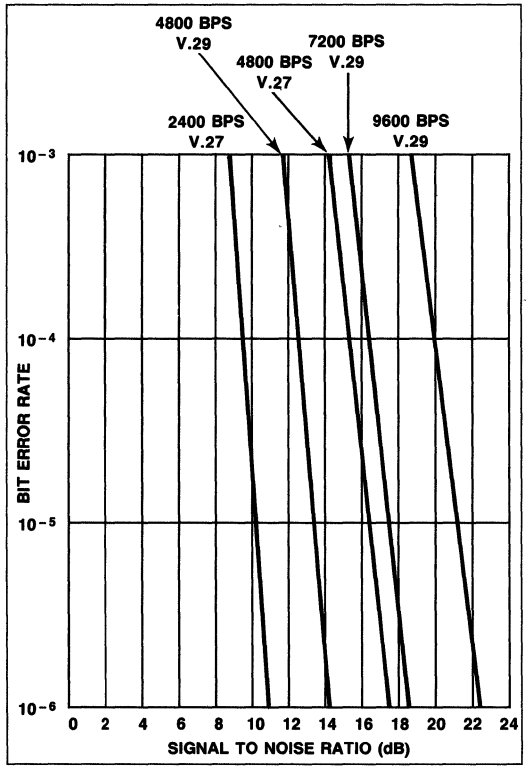
Typical BER performance is shown in Figure 7. The BER curves shown in Figure 7 were prepared from data obtained using a TAS 1010 system.

TYPICAL PHASE JITTER

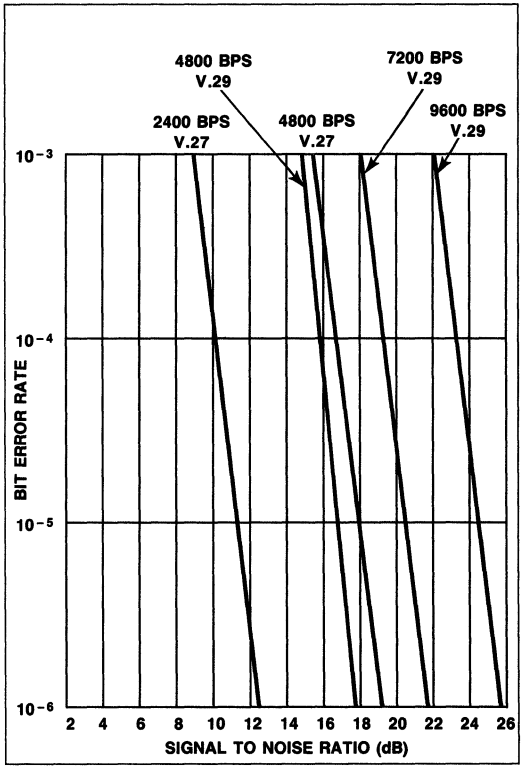
At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.



Typical BER Performance
Back-to-Back, −20 dBm Receive Signal Level



Typical BER Performance
3002 Unconditioned Line, −20 dBm Receive Signal Level

Figure 7. R96DP BER versus SNR

GENERAL SPECIFICATIONS

Table 10. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	<700 mA
+12 Vdc	±5%	5 mA	< 10 mA
−12 Vdc	±5%	25 mA	< 50 mA
Note: All voltages must have ripple ≤0 1 volts peak-to-peak.			

Table 11. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 12. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.937 in (100 mm)
Length	4.725 in. (120 mm)
Connector Height	0 437 in (11.1 mm)
Component Height	
Top (max.)	0.200 in. (5.1 mm)
Bottom (max.)	0 130 in. (3.3 mm)
Weight (max):	3 6 oz. (100 g)
Lead Extrusion (max.):	0 100 in. (2.54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3 228 in. (82 mm)
Length	3 937 in. (100 mm)
Component Height	
Top (max)	0.200 in. (5 1 mm)
Bottom (max.)	0.130 in. (3 3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.53 in (13.5 mm)

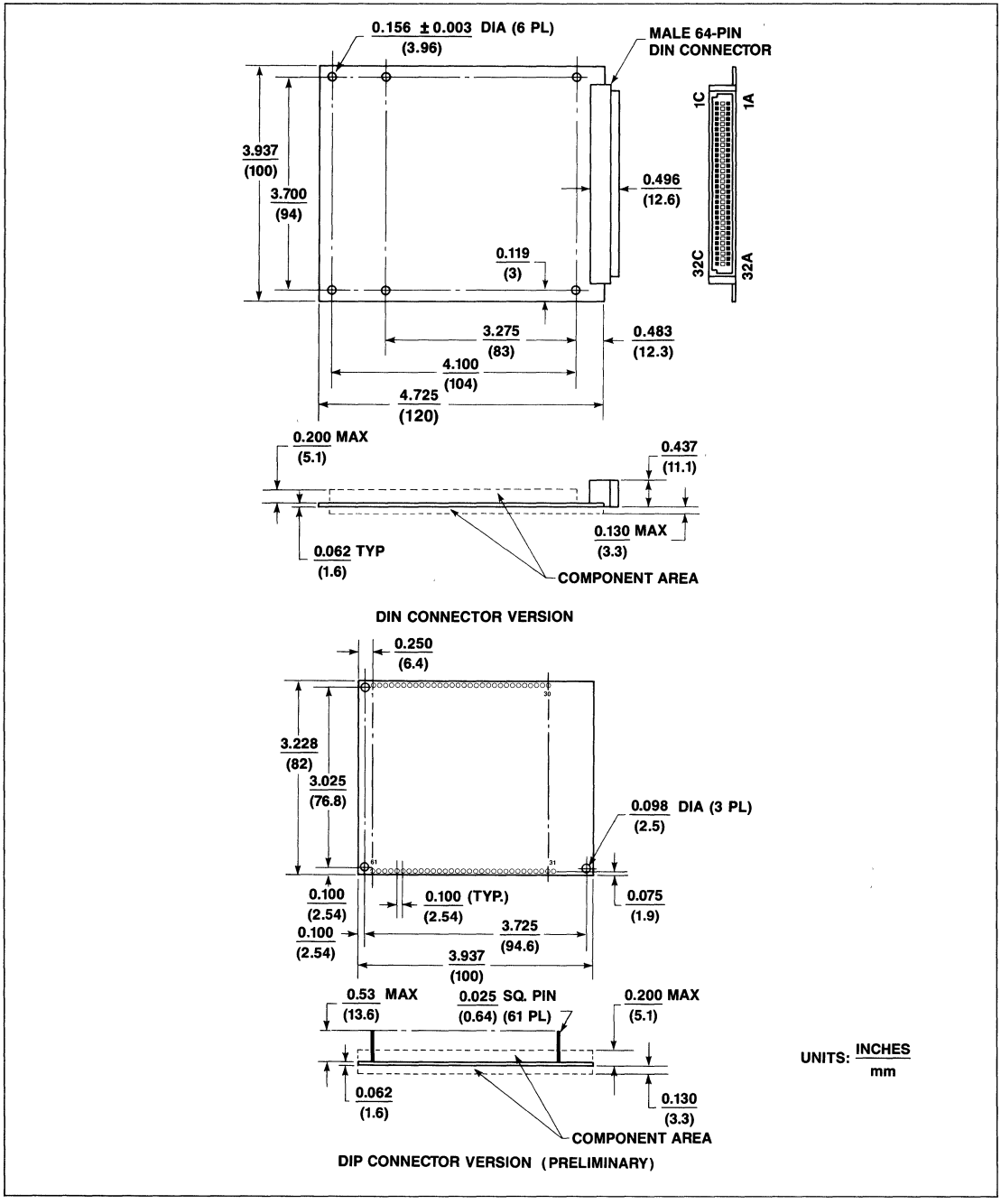


Figure 9. R96DP Modem Dimensions and Pin Locations

Rockwell

R96FT
9600 bps Fast Train Modem

INTRODUCTION

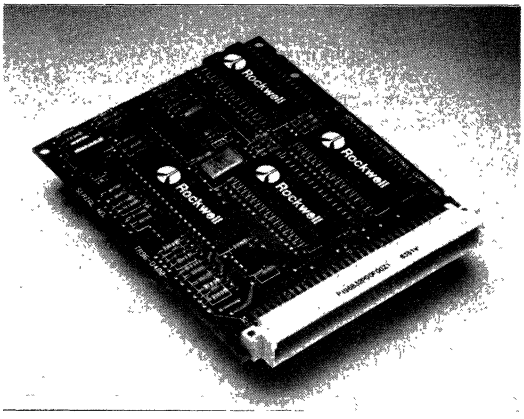
The Rockwell R96FT is a synchronous serial 9600 bps modem designed for multipoint and networking applications. The R96FT allows full-duplex operation over 4-wire dedicated unconditioned lines, or half-duplex operation over the public switched telephone network (PSTN).

Proprietary fast train configurations provide training times of 23 ms for V.29FT/9600/7200/4800, 22 ms for V.27FT/4800, and 30 ms for V.27FT/2400. A 2400/4800 bps Gearshift configuration provides a training time of 10 ms. For applications requiring operation with international standards, fallback configurations compatible with CCITT recommendations V.29 and V.27 bis/ter are provided. A 300 bps FSK configuration, compatible with CCITT V.21 Channel 2, is also provided.

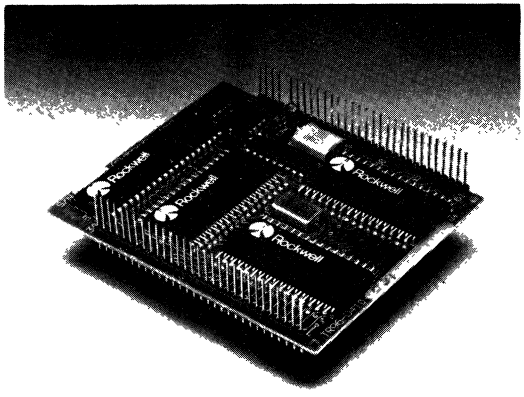
The small size and low power consumption of the R96FT offer the user flexibility in formulating a 9600 bps modem design customized for specific packaging and functional requirements.

FEATURES

- Proprietary Fast Train
- 2400/4800 bps Gearshift
- CCITT V.29, V.27 bis/ter and V.21 Channel 2 Compatible
- Train on Data
- 2-Wire Half Duplex, 4-Wire Full Duplex
- Programmable Tone Generation
- DTMF Tone Dialer
- Call Progress Tone Detection
- Dynamic Range −43 dBm to −5 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Loopbacks
  - — Local Analog
  - — Remote Analog and Digital
- Small Size
  - — DIN Connector Version:
    120 mm x 100 mm (4.73 in. x 3.94 in.)
  - — DIP Connector Version:
    82 mm x 100 mm (3.23 in. x 3.94)
- Low Power Consumption: 3W (typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R96FT DIN Connector Version



R96FT DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

Function	Frequency (Hz ±0.01%)
V.27 bis/ter Carrier	1800
V.27FT Carrier	1800
2400/4800 bps Gearshift	1800
V.29 Carrier	1700
V.29FT Carrier	1700/1800*
V.21 Channel 2:	
Mark	1650
Space	1850
*Selectable carrier frequency	

TONE GENERATION

Under control of the host processor, the R96FT can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

Parameter	Specification
Signaling Rate: Data Rate:	2400 baud 9600 bps 7200 bps 4800 bps
Signaling Rate: Data Rate:	1600 baud 4800 bps
Signaling Rate: Data Rate: Gearshift Data Rate:	1200 baud 2400 bps 2400/4800 bps
Signaling Rate: Data Rate:	300 baud 300 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 bis/ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 bis/ter.

For the Gearshift configuration, the signaling rate is 1200 baud. The 2400 bps data stream is encoded into dibits forming a 4-point structure, and the 4800 bps data stream is encoded into quadbits forming a 16-point structure. The first 32 bauds of data are transmitted at 2400 bps and the remaining message is transmitted at 4800 bps.

At 300 baud, the 300 bps data stream is encoded per CCITT V.21 Channel 2 into a mark frequency of 1650 Hz and a space frequency of 1850 Hz.

EQUALIZERS

The R96FT provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive T equalizer is provided in the receiver circuit.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96FT incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or V.29 depending on the selected configuration.

The scrambler/descrambler facilities for Gearshift can be selected to be in accordance with either V.27 bis/ter or V.29. The scrambler/descrambler selection is made by writing the appropriate configuration codes into the transmitter and receiver.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96FT can adapt to received frequency error of up to ±10 Hz with less than 0.2 dB degradation in BER performance.

During fast train polling, frequency offset must be less than ±2 Hz for successful training.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from –5 dBm to –43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

The R96FT provides a data derived Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a squarewave. The low-to-high transitions of this output coincide with the centers of received data bits. For the Gearshift configuration, the first 32 bauds of data are at 2400 bps followed by 4800 bps data for the remaining message. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. $\overline{\text{RDCLK}}$ duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is accurate to ±1.0 dB and is programmable from –1.0 dBm to –15.0 dBm in 2 dB steps.

TRANSMIT TIMING

The R96FT provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400 or 300 Hz (±0.01%). For the Gearshift Configuration, TDCLK is a 2400 Hz clock for the first 32 bauds of data, and a 4800 Hz clock for the remaining message.
2. *Duty Cycle.* 50% ±1%

Input data presented on TXD is sampled by the R96FT at the low-to-high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate ±0.01% with a duty cycle of 50% ±20%.

TRAIN ON DATA

When train on data is enabled (by setting a bit in the interface memory), the modem monitors the EQM signal. If EQM indicates a loss of equalization (i.e., BER approximately 10^{-3} for 0.5 seconds) the modem attempts to retrain on the data stream. The time for retrain is typically 3 to 15 seconds.

TURN-ON SEQUENCE

A total of 20 selectable turn-on sequences can be generated as defined in the following table:

No.	V.29 (bps)	V.27 bis/ter (bps)	Gearshift (bps)	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Response Time (milliseconds)	Comments
1	FT/9600			23	
2	FT/7200			24	Proprietary
3	FT/4800			23	Fast Train
4		FT/4800		22	
5		FT/2400		30	
6	9600			253	
7	7200			253	
8	4800			253	
9		4800 long		708	
10		2400 long		943	
11		4800 short		50	
12		2400 short		67	
13			2400/4800	10	
14	9600			438	Preceded[1]
15	7200			438	by Echo
16	4800			438	Protector
17		4800 long		913	Tone for
18		2400 long		1148	lines using
19		4800 short		255	echo
20		2400 short		272	suppressors.

1. For short echo protector tone, subtract 155 ms from values of $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ response time.
2. V.21 (300 bps FSK) $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ response time is <35 ms

TURN-OFF SEQUENCE

For V.27 bis/ter, V.27FT and 2400/4800 bps Gearshift configurations, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy (V.27 bis/ter only). For V.29 and V.29FT, the turn-off sequence consists of approximately 8 ms of remaining data and scrambled ones.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) when the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off.

RESPONSE TIMES OF CLEAR TO SEND ($\overline{\text{CTS}}$)

The time between the off-to-on transition of Request To Send ($\overline{\text{RTS}}$) and the off-to-on transition of Clear to Send ($\overline{\text{CTS}}$) is dictated by the length of the training sequence and the echo protector tone, if used. These times are given in the Turn-On Sequences table. If training is not enabled, $\overline{\text{RTS}}$/$\overline{\text{CTS}}$ delay is less than 2 baud times.

The time between the on-to-off transition of $\overline{\text{RTS}}$ and the on-to-off transition of $\overline{\text{CTS}}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVE LINE SIGNAL DETECTOR ($\overline{\text{RLSD}}$)

Response

For Fast Train and Gearshift configurations, the receiver enters the training state upon detecting a significant increase in the received signal power. If the received line signal power is greater than the selected threshold level at the end of the training state, the receiver enters the data state and $\overline{\text{RLSD}}$ is activated. If the received line signal power is less than the selected threshold level at the end of the training state, the receiver returns to the idle state and $\overline{\text{RLSD}}$ is not activated.

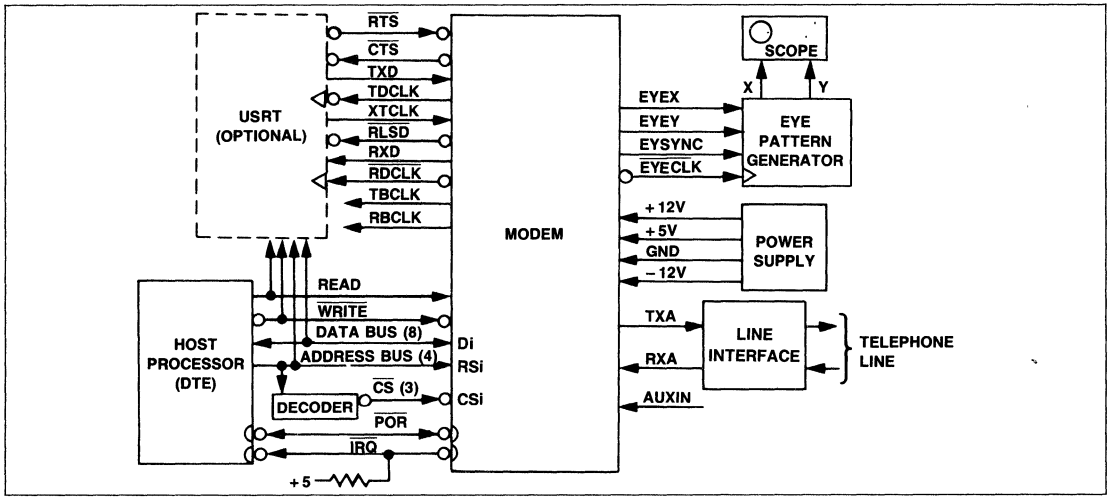
Also, in Fast Train and Gearshift configurations, the receiver initiates the turn-off delay upon detecting a significant decrease in the received signal power. If the received signal power is less than the selected threshold at the end of the turn-off delay, the receiver enters the idle state and $\overline{\text{RLSD}}$ is deactivated. If the received signal power is greater than the selected threshold at the end of the turn-off delay, the receiver returns to the data state and $\overline{\text{RLSD}}$ is left active.

For CCITT configurations, the receiver enters the training detection state when the received line signal power crosses the selected threshold level. $\overline{\text{RLSD}}$ is activated at the end of the training sequence. For V.21 Channel 2, a separate received line signal detector ($\overline{\text{FRLSD}}$) is provided. $\overline{\text{FRLSD}}$ is activated when energy above −43 dBm is present at the receiver's audio input (RXA). The $\overline{\text{FRLSD}}$ off-to-on response time is 15 ±5 ms and the on-to-off response time is 25 ±5 ms.

The $\overline{\text{RLSD}}$ on-to-off response times are:

Configuration	$\overline{\text{RLSD}}$ On-To-Off Response Time (ms)
V.29 Fast Train	6.5 ±1
V.27 Fast Train	8 ±1
Gearshift	6 ±1
V.29	30 ±9
V.27 bis/ter	10 ±5

$\overline{\text{RLSD}}$ response times are measured with a signal at least 3 dB above the actual $\overline{\text{RLSD}}$ on threshold or at least 5 dB below the actual $\overline{\text{RLSD}}$ off threshold.



R96FT Functional Interconnect Diagram

Threshold Options

Four threshold options are provided:

1. Greater than −43 dBm ($\overline{RLSD}$ on)
   Less than −48 dBm ($\overline{RLSD}$ off)
2. Greater than −33 dBm ($\overline{RLSD}$ on)
   Less than −38 dBm ($\overline{RLSD}$ off)
3. Greater than −26 dBm ($\overline{RLSD}$ on)
   Less than −31 dBm ($\overline{RLSD}$ off)
4. Greater than −16 dBm ($\overline{RLSD}$ on)
   Less than −21 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

For CCITT configurations, a minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R96FT is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R96FT has the capability of transferring channel data (up to eight bits at a time) via the microprocessor bus.

MODE SELECTION

For the transmitter, a control bit determines whether the source of transmitted data is the V.24 interface (serial mode) or the parallel transmitter data register (parallel mode). The transmitter automatically defaults to the serial mode at power-on.

The receiver simultaneously outputs received data via the V.24 interface and the parallel receiver data register.

In either parallel or serial mode, the R96FT is configured by the host processor via the microprocessor bus.

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96FT Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the following table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the

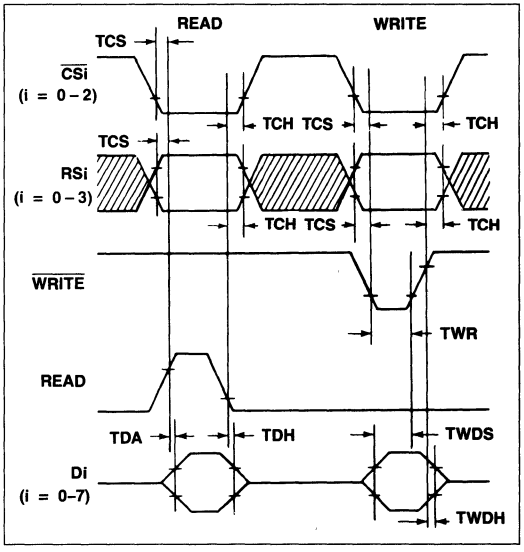
rising edge of the $\overline{\text{EYECLK}}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

R96FT Hardware Circuits

Name	Type	DIN Pin No.	DIP Pin No.	Description
A. OVERHEAD:				
Ground (A)	AGND	31C,32C	30,31	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	29,37,53	Digital Ground Return
+5 volts	PWR	19C,23C, 26C,30C	1,45,61	+5 Vdc Supply
+12 volts	PWR	15A	32	+12 Vdc Supply
−12 volts	PWR	12A	36	−12 Vdc Supply
$\overline{\text{POR}}$	I/OB	13C	2	Power-on-reset
B. MICROPROCESSOR INTERFACE:				
D7	I/OA	1C	3	Data Bus (8 Bits)
D6	I/OA	1A	4	
D5	I/OA	2C	5	
D4	I/OA	2A	6	
D3	I/OA	3A	7	
D2	I/OA	4C	8	
D1	I/OA	4A	9	
D0	I/OA	5C	10	
RS3	IA	6C	16	Register Select (4 Bits)
RS2	IA	6A	17	
RS1	IA	7C	18	
RS0	IA	7A	19	
$\overline{\text{CS0}}$	IA	10C	20	Chip Select—Transmitter Device
$\overline{\text{CS1}}$	IA	9C	21	Chip Select—Receiver Sample Rate Device
$\overline{\text{CS2}}$	IA	9A	13	Chip Select—Receiver Baud Rate Device
$\overline{\text{READ}}$	IA	12C	14	Read Enable
$\overline{\text{WRITE}}$	IA	11A	12	Write Enable
$\overline{\text{IRQ}}$	OB	11C	11	Interrupt Request
C. V.24 INTERFACE:				
$\overline{\text{RDCLK}}$	OC	21A	23	Receive Data Clock
TDCLK	OC	23A	46	Transmit Data Clock
$\overline{\text{XTCLK}}$	IB	22A	51	External Transmit Clock
$\overline{\text{RTS}}$	IB	25A	50	Request to Send
$\overline{\text{CTS}}$	OC	25C	49	Clear to Send
TXD	IB	24C	48	Transmitter Data
$\overline{\text{RXD}}$	OC	22C	26	Receiver Data
$\overline{\text{RLSD}}$	OC	24A	27	Received Line Signal Detector
D. ANCILLARY CIRCUITS:				
RBCLK	OC	26A	22	Receiver Baud Clock
$\overline{\text{TBCLK}}$	OC	27C	47	Transmitter Baud Clock
$\overline{\text{FRXD}}$	OD	16A	59	FSK Receiver Data (inverted data)
$\overline{\text{FRLSD}}$	OD	17C	52	FSK Received Line Signal Detector
E. ANALOG SIGNALS:				
TXA	AA	31A	34	Transmitter Analog Output
RXA	AB	32A	33	Receiver Analog Input
AUXIN	AC	30A	—	Auxiliary Analog Input
F. DIAGNOSTIC:				
EYEX	OC	15C	56	Eye Pattern Data—X Axis
EYEY	OC	14A	55	Eye Pattern Data—Y Axis
$\overline{\text{EYECLK}}$	OA	14C	57	Eye Pattern Clock
EYESYNC	OA	13A	58	Eye Pattern Synchronizing Signal

NOTES: 1. Pins not used on the DIP version: 15, 24, 25, 28, 35 38–44, 54 and 60.
2. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Microprocessor Timing



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{\text{CSi}}$, RSi setup time prior to Read or $\overline{\text{Write}}$	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
$\overline{\text{CSi}}$, RSi hold time after Read or $\overline{\text{Write}}$	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

Digital Interface Characteristics

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	OD	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.					2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.					0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.2 Min. [6]	2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max [2]	0.6 Max.[7]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.							±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.					
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.			
I_L	Output Current, Leakage	μA					±10 Max.				
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.			−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20					10	40
C_D	Capacitive Drive	pF				100	100	100		100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	TTL	3-State Transceiver	Open-Drain w/Pull-up

Notes 1. I Load = −100 μA 3. I Load = −40 μA 5. I Load = 0.36 mA 7. I Load = 2.0 mA
2. I Load = 1.6 mA 4. V_{IN} = 0.4 to 2 4 Vdc, V_{CC} = 5.25 Vdc 6. I Load = −400 μA

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604 ohms ± 1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is TLVL setting +0.6 dB −1.4 dB. If unused, this input must be grounded near the modem connector. If used, it must be driven from a low impedance source.

SOFTWARE CIRCUITS

The R96FT comprises three signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 1 update at half the modem sample rate (4800 bps). Registers in chip 0 and 2 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0–2), the register by Z(0–F), and the bit by Q(0–7, 0 = LSB).

Status Control Bits

The operation of the R96FT is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a dash (—) are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R96FT provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers in chip 2 allow user access to RAM locations via the X word registers (2:3 and 2:2) and the Y word register (2:1 and 2:0). The access code stored in RAM ACCESS X (2:5) selects the source of data for RAM DATA XM and RAM DATA XL (2:3 and 2:2). Similarly, the access code stored in RAM ACCESS Y (2:4) selects the source of data for RAM DATA YM and RAM DATA YL (2:1 and 2:0).

Reading of diagnostic RAM data is performed by storing the necessary access codes in 2:5 and 2:4, reading 2:0 to reset the associated data available bit (2:E:0), then waiting for the data available bit to return to a one. Data is now valid and may be read from 2:3 through 2:0.

An additional diagnostic is supplied by the sample rate processor (chip 1). Registers 1:2 and 1:3 supply a 16 bit AGC Gain Word. These two diagnostic data registers are updated at the sample rate during the data state and may be read by the host processor asynchronously.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

Baud Rate Processor (Chip 2) RAM Access Codes

No.	Function	X Access	Y Access	Register
1	Equalizer Input	C0	40	0,1,2,3
2	Equalizer Tap Coefficients	81–A0	01-20	0,1,2,3
3	Unrotated Equalizer Output	E1	61	0,1,2,3
4	Rotated Equalizer Output	E2	62	0,1,2,3
5	Decision Points (Ideal Data Points)	E8	68	0,1,2,3
6	Error Vector	E5	65	0,1,2,3
7	Rotation Angle	A7	Not Used	2,3
8	Frequency Correction	A5	Not Used	2,3
9	Eye Quality Monitor (EQM)	AC	Not Used	2,3

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	FSKT	ASCR	—	—	TCF	DDEE	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	—	—	—	—	—	—	—	—
0	DIAL DIGIT REGISTER (DDR)/TRANSMITTER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RIA	—	—	—	RSB	RIE	—	RDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	$\overline{CDET}$	—	—
8	$\overline{TONE}$	—	—	—	$\overline{P2DET}$	—	—	—
7	RTH		DDIS	—	—	RCF	RDIS	—
6	TOD	RECEIVER CONFIGURATION						
5	—	—	—	—	—	—	—	—
4	—	—	—	—	—	—	—	—
3	AGC GAIN WORD (MSB)							
2	AGC GAIN WORD (LSB)							
1	—	—	—	—	—	—	—	—
0	RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS X							
4	RAM ACCESS Y							
3	RAM DATA XM							
2	RAM DATA XL							
1	RAM DATA YM							
0	RAM DATA YL							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

R96FT Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
ASCR	Append Scrambled Ones	0:9:6	When control bit ASCR is a one, one baud of scrambled marks is included in the V.29FT and V.27FT training sequences The RTS-CTS delay is thus extended by one baud period when ASCR is a one.
A3L	Amplitude 3-Link Select	0:5.1	See LAEN.
$\overline{\text{CDET}}$	Carrier Detector	1:9:2	When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
CEQ	Cable Equalizer Field	0:5:(4,5)	The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following table lists the possible cable equalizer selection codes: **CEQ** — **Cable Length (0.4 mm diameter)** 0 — 0.0 1 — 1.8 km 2 — 3.6 km 3 — 7.2 km
DDEE	Digital Delay Equalizer Enable	0:9:2	When control bit DDEE is a one, a fourth order digital delay equalizer is inserted in the transmit path
DDIS	Descramble Disable	1:7:5	When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.
DDR	Dial Digit Register	0:0:0–7	DDR is used to tell the modem which DTMF digit to transmit (see Transmitter Data).
D3L	Delay 3-Link Select	0:5:0	See LDEN
EPT	Echo Protector Tone	0:7:3	When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. This option is available in the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 Recommendation.
$\overline{\text{FED}}$	Fast Energy Detector	1:9:6	When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband.
(None)	FREQL/FREQM	0:2:0–7, 0:3:0–7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below: *FREQM Register (0:3)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below: **Frequency (Hz)** — **FREQM** — **FREQL** 462 — 0C — 52 1100 — 1D — 55 1650 — 2C — 00 1850 — 31 — 55 2100 — 38 — 00
FSKT	FSK Transmitter Configuration	0:9:7	The V.21 Channel 2 (300 bps synchronous FSK) transmitter configuration is selected by setting the FSK control bit to a one (see TSB). While set to a one, this control bit overrides the configuration selected by the control code in register 0:6. The FSK data may be transmitted in parallel mode or in serial mode (see TPDM).

R96FT Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
LAEN	Link Amplitude Equalizer Enable	0:5:3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table: **LAEN** / **A3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5:2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN** / **D3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
L2ACT	Remote Digital Loopback Activate	0:4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT Recommendation V.54 loop 2.
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT Recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0:4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to CCITT Recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4:5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
$\overline{\text{P2DET}}$	Period 2 Detector	1:8:3	When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a period 2 sequence has been detected. This bit sets to a one at the start of the period N sequence. This bit is only significant for CCITT V.29 and V.27 bis/ter configurations.
(None)	RAM Access X	2:5:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access Y	2:4:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word Y (2:1 and 2:0).
(None)	RAM Data XL	2:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XM	2:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data YL	2:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YM	2:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 2.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{\text{IRQ}}$ low.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
RCF	Receiver Carrier Frequency	1:7:2	Control bit RCF selects the demodulator carrier frequency for V.29FT configurations as follows: **RCF** / **Demodulator Carrier Frequency** 0 / 1700 Hz 1 / 1800 Hz

R96FT Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Receiver Configuration</td><td>1:6:0–6</td><td>The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB).
Note: The receiver must be disabled prior to changing configurations. See RDIS.
Receiver Configuration Control Codes
Control codes for the modem receiver configuration are:
<table>
<tr><th colspan="2">Configuration</th><th rowspan="2">Configuration Code (Hex)</th></tr>
<tr><th>V29</th><th>V27 bis/ter</th></tr>
<tr><td>FT/9600</td><td></td><td>1C</td></tr>
<tr><td>FT/7200</td><td></td><td>1A</td></tr>
<tr><td>FT/4800</td><td></td><td>19</td></tr>
<tr><td></td><td>FT/4800</td><td>0A</td></tr>
<tr><td></td><td>FT/2400</td><td>09</td></tr>
<tr><td>9600</td><td></td><td>14</td></tr>
<tr><td>7200</td><td></td><td>12</td></tr>
<tr><td>4800</td><td></td><td>11</td></tr>
<tr><td></td><td>4800 long</td><td>22</td></tr>
<tr><td></td><td>2400 long</td><td>21</td></tr>
<tr><td></td><td>4800 short</td><td>02</td></tr>
<tr><td></td><td>2400 short</td><td>01</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.29 descrambler[1]</td><td>61</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.27 bis/ter descrambler[1]</td><td>41</td></tr>
<tr><td colspan="2">V.21 Channel 2</td><td>See Note 2</td></tr>
<tr><td colspan="2">250–650 Hz Tone Detector[3]</td><td>31</td></tr>
<tr><td colspan="2">2100 Hz Tone Detector[3]</td><td>33</td></tr>
</table>
1. The Receiver Configuration code automatically changes from a hex 61 (or hex 41) to a hex 64 (or hex 44) when the receiver transitions from the 2400 bps data state to the 4800 bps data state.
2. The FSK receiver is active at all times. Two ancillary hardware circuits, $\overline{\text{FRLSD}}$ and $\overline{\text{FRXD}}$, are supplied for FSK message reception. $\overline{\text{FRLSD}}$ is described under the Received Line Signal Detector section. $\overline{\text{FRXD}}$ provides inverted FSK received data. Timing extraction must be performed on the $\overline{\text{FRXD}}$ signal externally as no FSK receiver data clock is provided by the R96FT.
3. Added in B5413-11.</td></tr>
<tr><td>(None)</td><td>Receiver Data</td><td>1:0:0–7</td><td>The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data.</td></tr>
<tr><td>RDA</td><td>Receiver Data Available</td><td>1:E:0</td><td>Status bit RDA goes to a one when the receiver writes data to register 1:0. RDA goes to a zero when the host processor reads data from register 1:0.</td></tr>
<tr><td>RDIS</td><td>Receiver Disable</td><td>1:7:1</td><td>When control bit RDIS is a one, the receiver is disabled, $\overline{\text{RLSD}}$ is turned off and RXD is clamped to all marks. This bit can be used to squelch the receiver during half duplex transmissions over two wires. This bit must be set to a one prior to changing the receiver configuration.</td></tr>
<tr><td>RIA</td><td>Receiver Interrupt Active</td><td>1:E:7</td><td>This status bit is a one whenever the receiver sample rate device is driving $\overline{\text{IRQ}}$ to zero.</td></tr>
<tr><td>RIE</td><td>Receiver Interrupt Enable</td><td>1:E:2</td><td>When the host processor writes a one in the RIE control bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven to zero when status bit RDA is a one.</td></tr>
<tr><td>RSB</td><td>Receiver Setup Bit</td><td>1:E:3</td><td>When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective.</td></tr>
<tr><td>RTH</td><td>Receiver Threshold Field</td><td>1:7:6,7</td><td>The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB):
<table>
<tr><th>RTH</th><th>RLSD On</th><th>RLSD Off</th></tr>
<tr><td>0</td><td>> –43 dBm</td><td>< –48 dBm</td></tr>
<tr><td>1</td><td>> –33 dBm</td><td>< –38 dBm</td></tr>
<tr><td>2</td><td>> –26 dBm</td><td>< –31 dBm</td></tr>
<tr><td>3</td><td>> –16 dBm</td><td>< –21 dBm</td></tr>
</table></td></tr>
</table>

R96FT Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are OR'ed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector disable tone is 30 ms long rather than 185 ms. (See TSB.)
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one.
TCF	Transmitter Carrier Frequency	0:9:3	Control bit TCF selects the modulator carrier frequency for V.29FT configurations as follows: **TCF** — **Modulator Carrier Frequency** 0 — 1700 Hz 1 — 1800 Hz
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** — **Transmitter Analog Output*** 0 — −1 dBm ±1 dB 1 — −3 dBm ±1 dB 2 — −5 dBm ±1 dB 3 — −7 dBm ±1 dB 4 — −9 dBm ±1 dB 5 — −11 dBm ±1 dB 6 — −13 dBm ±1 dB 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-On-Data	1:6:7	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-data.
$\overline{TONE}$	Tone Detect	1:8:7	$\overline{TONE}$ indicates with a zero the presence of energy in the 250–650 ±10 Hz or 2100 ±20 Hz frequency range. For call progress purposes, the user may determine which tone is present by determining the duty cycle of the $\overline{TONE}$ bit.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0) rather than the serial hardware data input.

R96FT Interface Memory Definitions (Continued)

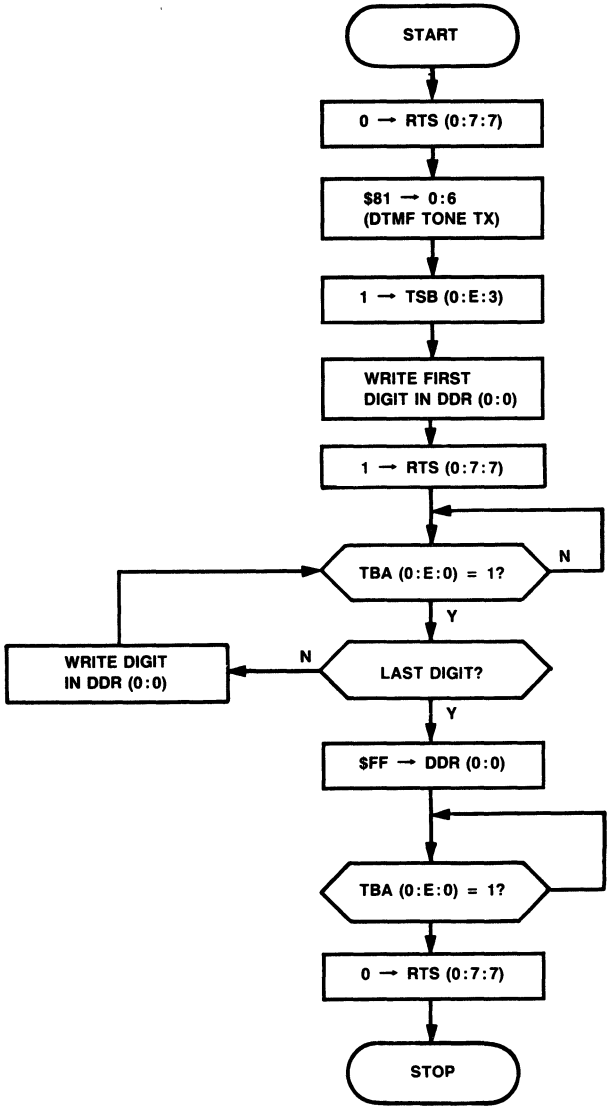
<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter Configuration</td><td>0:6:0–7</td><td>The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB.)
Transmitter Configuration Control Codes
Control codes for the modem transmitter configurations are:
<table>
<tr><th colspan="2">Configuration</th><th rowspan="2">Configuration Code (Hex)</th></tr>
<tr><th>V29</th><th>V27 bis/ter</th></tr>
<tr><td>FT/9600
FT/7200
FT/4800</td><td>

FT/4800
FT/2400</td><td>1C
1A
19
0A
09</td></tr>
<tr><td>9600
7200
4800</td><td>

4800 long
2400 long
4800 short
2400 short</td><td>14
12
11
22
21
02
01</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.29 Scrambler
2400/4800 bps Gearshift/V.27 bis/ter Scrambler</td><td>61
41</td></tr>
<tr><td colspan="2">V.21 Channel 2</td><td>See FSKT</td></tr>
<tr><td colspan="2">Tone transmit</td><td>80</td></tr>
<tr><td colspan="2">DTMF Tone Transmit*</td><td>81</td></tr>
<tr><td colspan="3">*Note: Added in R5339-11.</td></tr>
</table></td></tr>
<tr><td>(None)</td><td>Transmitter Data/ DDR</td><td>0:0:0–7</td><td>1. The host processor conveys output data to the transmitter in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:
2. Register 0:0 is used to transmit DTMF digits when the transmitter is configured in the DTMF tone transmit mode.
Note: Data is transmitted bit zero first.
<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.29 9600 bps</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.29 7200 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.29 4800 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>2400 bps Gearshift</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>4800 bps Gearshift</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
</table></td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the SEPT bit or the FSKT bit, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a one, the transmitter timing is established by the external clock supplied at the hardware input XTCLK.</td></tr>
</table>

Auto Dial Sequence

The R96FT Auto Dial Sequence flowchart defines the auto dial sequence via the microprocessor interface memory. The modem timing for the auto dialer accounts for DTMF tone duration and interdigit delay. The tone duration is 95 ms and the interdigit delay is 71 ms. The amplitudes for the high and low frequencies are −4 dBm and −6 dBm, respectively.



R96FT Auto Dial Sequence Flowchart

POWER-ON INITIALIZATION

When power is applied to the R96FT, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is generated.

At POR time the modem defaults to the following configuration: fast train, V.29, 9600 bps, no echo protector tone, 1700 Hz carrier frequency, scrambled ones segment disabled, serial data mode, internal clock, cable equalizers disabled, transmitter digital delay equalizer disabled, link amplitude equalizer disabled, link delay equalizer disabled, transmitter output level set to −1 dBm ±1 dB, interrupts disabled, receiver threshold set to −43 dBm, and train-on-data enabled.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after $\overline{POR}$ is removed.

PERFORMANCE

Whether functioning in V.27, V.29 or the proprietary fast train configurations, the R96FT provides the user with high performance.

POLLING SUCCESS

In the 9600 bps fast train configuration the modem approaches a 98% success rate over unconditioned 3002 lines for a signal-to-noise ratio of 26 dB, with a received signal level of −20 dBm.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal of −20 dBm.

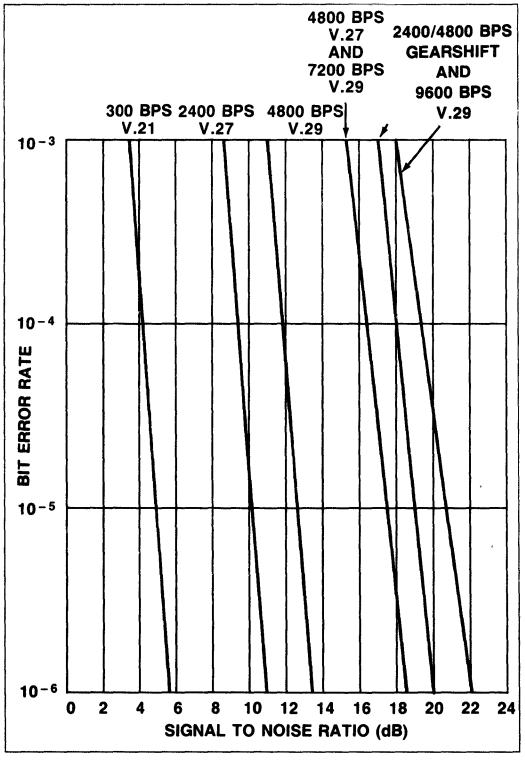
PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz, or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

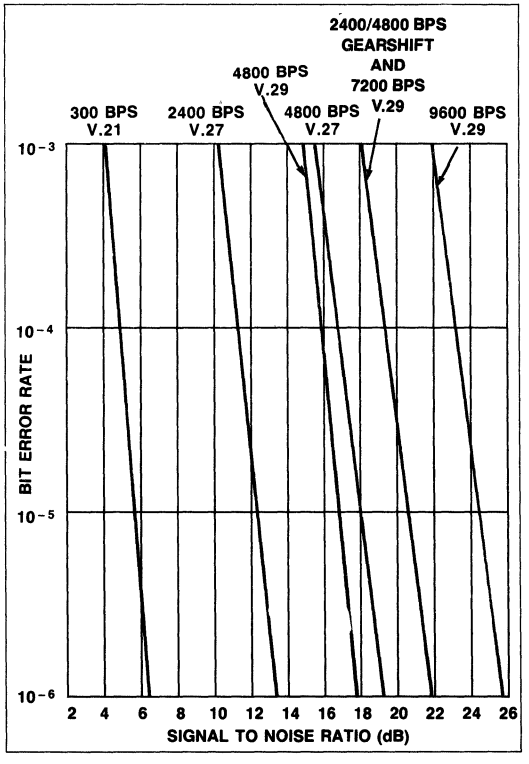
At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

Examples of the R96FT BER performance are shown below. The BER curves were prepared from data obtained using a TAS1010 test system.



Typical BER Performance
Back-to-Back, −20 dBm Receive Signal Level



Typical BER Performance
3002 Unconditioned Line, −20 dBm Receive Signal Level

GENERAL SPECIFICATIONS

Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	700 mA
+12 Vdc	±5%	20 mA	30 mA
−12 Vdc	±5%	50 mA	80 mA

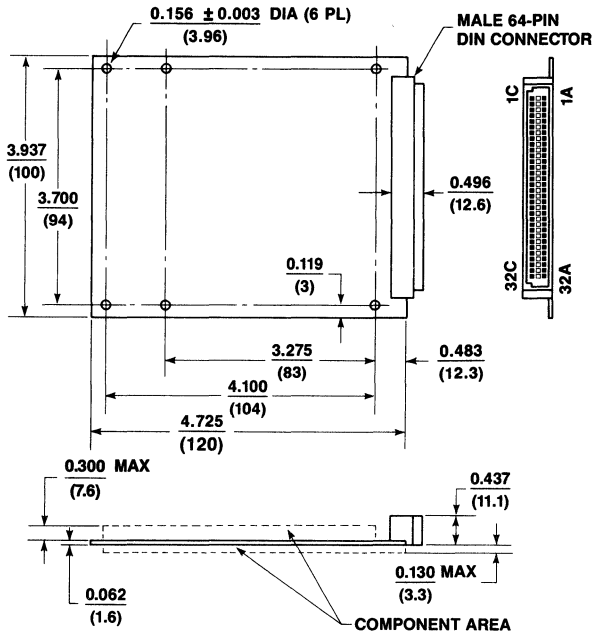
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Modem Environmental Restrictions

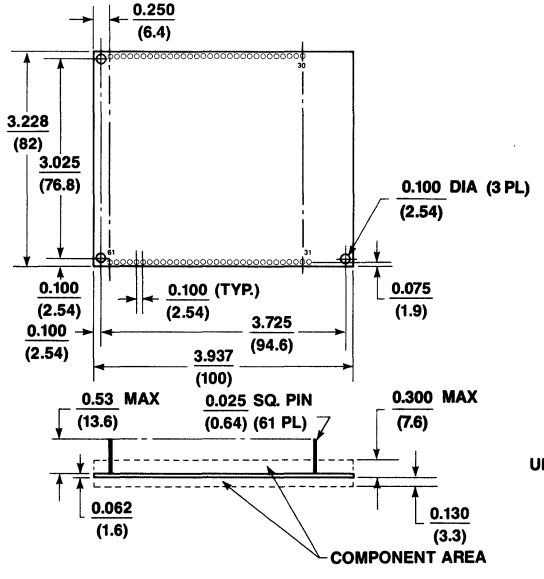
Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male, or 6 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating connector: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Height (max.)	0.30 in. (7.6 mm)
Weight (max):	3.6 oz. (100 g)
Lead Extrusion (max.):	0.100 in. (2.54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.937 in. (100 mm)
Length	3.228 in. (82 mm)
Height (max.)	0.30 in. (7.6 mm) above, 0.13 in. (3.30 mm) below
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.53 in. (13.5 mm)



DIN CONNECTOR VERSION



DIP CONNECTOR VERSION

R96FT Modem Dimensions and Pin Locations

Rockwell

R96FT/SC
9600 bps Fast Train Modem with Forward Secondary Channel

INTRODUCTION

The Rockwell R96FT/SC is a synchronous serial 9600 bps modem containing a 75 bps asynchronous FSK forward channel. This modem is designed for multipoint and networking applications. The R96FT/SC allows full-duplex operation over 4-wire dedicated unconditioned lines, or half-duplex operation over the general switched telephone network.

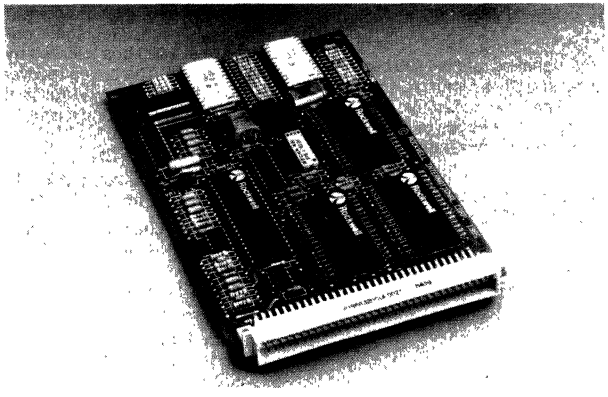
Proprietary fast train configurations provide training times of 23 ms for V.29FT/9600/7200/4800, 22 ms for V.27FT/4800, and 30 ms for V.27FT/2400. A 2400/4800 bps Gearshift configuration provides a training time of 10 ms. For applications requiring operation with international standards, fallback configurations compatible with CCITT Recommendations V.29 and V.27 bis/ter are provided. A 300 bps FSK configuration, compatible with CCITT V.21 Channel 2, is also provided.

The small size and low power consumption of the R96FT/SC offer the user flexibility in formulating a 9600 bps modem design customized for specific packaging and functional requirements.

This data sheet corresponds to assembly number TR96-D500-021.

FEATURES

- Proprietary Fast Train
- 75 bps Forward Channel
- 2400/4800 bps Gearshift
- User Compatibility:
  — CCITT V.29, V.27 bis/ter and V.21 Channel 2
- Train on Data
- Full-Duplex (4-Wire)
- Half-Duplex (2-Wire)
- Programmable Tone Generation
- Dynamic Range –43 dBm to –5 dBm
- Diagnostic Capability
- Equalization:
  — Automatic Adaptive
  — Compromise Cable (Selectable)
  — Compromise Link (Selectable)
- DTE Interface:
  — Microprocessor Bus
  — CCITT V.24 (RS-232-C Compatible)
- Loopbacks
  — Local Analog (V.54 Loop 3)
  — Remote Analog (Locally Activated)
  — Remote Digital (Locally Activated V.54 Loop 2)
- Small Size
  — 100 mm x 160 mm (3.94 in. x 6.3 in.)
- Low Power Consumption
  — 4 watts, typical
- Programmable Transmit Output Levels for Primary Channel and Forward Channel
- TTL and CMOS Compatible



R96FT/SC Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

Function	Frequency (Hz ±0.01%)
V.27 bis/ter Carrier	1800
V.27 FT Carrier	1800
2400/4800 bps Gearshift	1800
V.29 Carrier	1700
V.29 FT Carrier	1700*
V.21 Channel 2:	
Mark	1650
Space	1850

*1800 when used in conjunction with 75 bps Forward Channel.

TONE GENERATION

Under control of the host processor, the R96FT/SC can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

Parameter	Specification (±0.01%)
Signaling Rate: Data Rate:	2400 baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate: Data Rate:	1600 baud 4800 bps
Signaling Rate: Data Rate: Gearshift Data Rate:	1200 baud 2400 bps 2400/4800 bps
Signaling Rate: Data Rate:	300 baud 300 bps
Signaling Rate: Data Rate:	75 baud 75 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 bis/ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 bis/ter.

For the Gearshift Configuration, the signaling rate is 1200 baud. The 2400 bps data stream is encoded into dibits forming a 4-point structure, and the 4800 bps data stream is encoded into quadbits forming a 16-point structure. The first 32 bauds of data are transmitted at 2400 bps and the remaining message is transmitted at 4800 bps.

At 300 baud, the 300 bps data stream is encoded per CCITT V.21 channel 2 into a mark frequency of 1650 Hz and a space frequency of 1850 Hz.

At 75 baud, the 75 bps data stream is encoded to a mark frequency of 356 Hz and a space frequency of 300 Hz.

EQUALIZERS

The R96FT/SC provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive T equalizer is provided in the receiver circuit.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

NOTE

When used with the 75 bps Forward Channel the 2400 Baud filter is narrower.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96FT/SC incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or V.29 depending on the selected configuration.

The scrambler/descrambler facilities for Gearshift can be selected to be in accordance with either V.27 bis/ter or V.29. The scrambler/descrambler selection is made by writing the appropriate configuration codes into the transmitter and receiver.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96FT/SC can adapt to received frequency error of up to ±10 Hz with less than 0.2 dB degradation in BER performance.

During fast train polling, frequency offset must be less than ±2 Hz for successful training.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from –5 dBm to –43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING (Synchronous Configurations)

The R96FT/SC provides a data derived Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a squarewave. The low-to-high transitions of this output coincide with the centers of received data bits. For the Gearshift Configuration, the first 32 bauds of data are at 2400 bps followed by 4800 bps data for the remaining message. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. $\overline{\text{RDCLK}}$ duty cycle is 50% ±1%.

TRANSMIT LEVEL

The main channel output level is accurate to ±1.0 dB and is programmable from –1.0 dBm to –15.0 dBm in 2 dB steps.

The forward channel transmit level is set relative to the main channel as –6 dB, –10 dB, –14 dB, or –18 dB.

TRANSMIT TIMING (Synchronous Configurations)

The R96FT/SC provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400 or 300 Hz (±0.01%). For the Gearshift Configuration, TDCLK is a 2400 Hz clock for the first 32 bauds of data, and a 4800 Hz clock for the remaining message.
2. *Duty Cycle.* 50% ±1%

Input data presented on TXD is sampled by the R96FT/SC at the low-to-high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate ±0.01% with a duty cycle of 50% ±20%.

TRAIN ON DATA

When train on data is enabled (by setting a bit in the interface memory), the modem monitors the EQM signal. If EQM indicates a loss of equalization (i.e., BER approximately 10^{-3} for 0.5 seconds) the modem attempts to retrain on the data stream. The time for retrain is typically 3 to 15 seconds.

TURN-ON SEQUENCE

A total of 20 selectable turn-on sequences can be generated as defined in the following table:

No.	V.29 (bps)	V.27 bis/ter (bps)	Gearshift (bps)	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Response Time (milliseconds)	Comments
1	FT/9600			23	
2	FT/7200			24	Proprietary
3	FT/4800			23	Fast Train
4		FT/4800		22	
5		FT/2400		30	
6	9600			253	
7	7200			253	
8	4800			253	
9		4800 long		708	
10		2400 long		943	
11		4800 short		50	
12		2400 short		67	
13			2400/4800	10	
14	9600			438	Preceded[1]
15	7200			438	by Echo
16	4800			438	Protector
17		4800 long		913	Tone for
18		2400 long		1148	lines using
19		4800 short		255	echo
20		2400 short		272	suppressors.

1. For short echo protector tone, subtract 155 ms from values of $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ response time.
2. V.21 (300 bps FSK) $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ response time is <35 ms.
3. 75 bps forward channel $\overline{\text{SCRTS}}$-$\overline{\text{SCCTS}}$ response time is <500 ms.

TURN-OFF SEQUENCE

For V.27bis/ter, V.27FT and 2400/4800 bps Gearshift configurations, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy (V.27 bis/ter only). For V.29 and V.29FT, the turn-off sequence consists of approximately 8 ms of remaining data and scrambled ones.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) when the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off.

RESPONSE TIMES OF CLEAR TO SEND ($\overline{\text{CTS}}$)

The time between the off-to-on transition of Request To Send ($\overline{\text{RTS}}$) and the off-to-on transition of Clear to Send ($\overline{\text{CTS}}$) is dictated by the length of the training sequence and the echo protector tone, if used. These times are given in the Turn-On Sequences table. If training is not enabled, $\overline{\text{RTS}}$/$\overline{\text{CTS}}$ delay is less than 2 baud times.

The time between the on-to-off transition of $\overline{\text{RTS}}$ and the on-to-off transition of $\overline{\text{CTS}}$ in the data state is a maximum of 2 baud times for all configurations.

RESPONSE TIMES OF FORWARD CHANNEL CLEAR TO SEND ($\overline{\text{SCCTS}}$)

$\overline{\text{SCRTS}}$/$\overline{\text{SCCTS}}$ response times vary according to the transmit level set by the SCTLVL field.

SCTLVL (0:9:0-1)	TX Level Relative to Primary	$\overline{\text{SCCTS}}$ Response Time (ms)
0	-6 dB	378
1	-10 dB	238
2	-14 dB	150
3	-18 dB	95

RECEIVE LINE SIGNAL DETECTOR ($\overline{\text{RLSD}}$)

Response

For Fast Train and Gearshift configurations, the receiver enters the training state upon detecting a significant increase in the received signal power. If the received line signal power is greater than the selected threshold level at the end of the training state, the receiver enters the data state and $\overline{\text{RLSD}}$ is activated. If the received line signal power is less than the selected threshold level at the end of the training state, the receiver returns to the idle state and $\overline{\text{RLSD}}$ is not activated.

Also, in Fast Train and Gearshift configurations, the receiver initiates the turn-off delay upon detecting a significant decrease in the received signal power. If the received signal power is less than the selected threshold at the end of the turn-off delay, the receiver enters the idle state and $\overline{\text{RLSD}}$ is deactivated. If the received signal power is greater than the selected threshold at the end of the turn-off delay, the receiver returns to the data state and $\overline{\text{RLSD}}$ is left active.

For CCITT configurations, the receiver enters the training detection state when the received line signal power crosses the selected threshold level. $\overline{\text{RLSD}}$ is activated at the end of the training sequence. For V.21 Channel 2, a separate received line signal detector ($\overline{\text{FRLSD}}$) is provided. $\overline{\text{FRLSD}}$ is activated when energy above -43 dBm is present at the receiver's audio input (RXA). The $\overline{\text{FRLSD}}$ off-to-on response time is 15 ±5 ms and the on-to-off response time is 25 ±5 ms.

The $\overline{\text{RLSD}}$ on-to-off response times are:

Configuration	Response Time (ms)
V.29 Fast Train	6.5 ±1
V.27 Fast Train	8 ±1
Gearshift	6 ±1
V.29	30 ±9
V.27 bis/ter	10 ±5

$\overline{\text{RLSD}}$ response times are measured with a signal at least 3 dB above the actual $\overline{\text{RLSD}}$ on threshold or at least 5 dB below the actual $\overline{\text{RLSD}}$ off threshold.

Threshold Options

Four threshold options are provided:

1. Greater than −43 dBm ($\overline{RLSD}$ on)
   Less than −48 dBm ($\overline{RLSD}$ off)
2. Greater than −33 dBm ($\overline{RLSD}$ on)
   Less than −38 dBm ($\overline{RLSD}$ off)
3. Greater than −26 dBm ($\overline{RLSD}$ on)
   Less than −31 dBm ($\overline{RLSD}$ off)
4. Greater than −16 dBm ($\overline{RLSD}$ on)
   Less than −21 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

For CCITT configurations, a minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

FORWARD CHANNEL SIGNAL DETECTOR ($\overline{SCRLSD}$)

Response

Signal Level	$\overline{SCRLSD}$ Turn-On (ms)	$\overline{SCRLSD}$ Turn-Off (ms)
−7 dBm	140 ± 10	800 ± 10
−48 dBm	340 ± 10	550 ± 10

Threshold

The $\overline{SCRLSD}$ Turn-On threshold is −54 dBm. The $\overline{SCRLSD}$ Turn-Off threshold is −58 dBm.

MODES OF OPERATION

The R96FT/SC is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

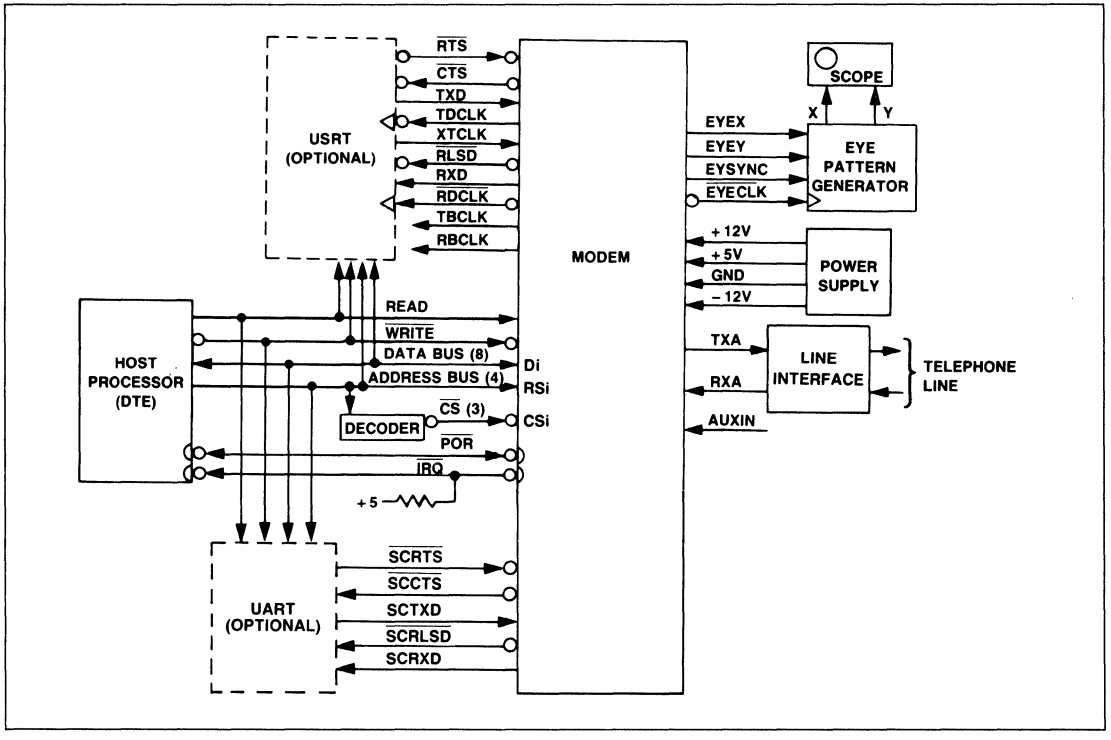
The R96FT/SC has the capability of transferring channel data (up to eight bits at a time) via the microprocessor bus.

MODE SELECTION

For the transmitter, a control bit determines whether the source of transmitted data is the V.24 interface (serial mode) or the parallel transmitter data register (parallel mode). The transmitter automatically defaults to the serial mode at power-on.

The receiver simultaneously outputs received data via the V.24 interface and the parallel receiver data register.

In either parallel or serial mode the R96FT/SC is configured by the host processor via the microprocessor bus.



R96FT/SC Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96FT/SC Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96FT/SC Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground (A)	AGND	31C,32C	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	+5 Vdc supply
+12 volts	PWR	15A	+12 Vdc supply
−12 volts	PWR	12A	−12 Vdc supply
POR	I/OB	13C	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	Data Bus (8 Bits)
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	Register Select (4 Bits)
RS2	IA	6A	
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select—Transmitter Device
$\overline{CS1}$	IA	9C	Chip Select—Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	Chip Select—Receiver Baud Rate Device
READ	IA	12C	Read Enable
WRITE	IA	11A	Write Enable
IRQ	OB	11C	Interrupt Request
C. V.24 INTERFACE:			
RDCLK	OC	21A	Receive Data Clock
TDCLK	OC	23A	Transmit Data Clock
XTCLK	IB	22A	External Transmit Clock
RTS	IB	25A	Request to Send
CTS	OC	25C	Clear to Send
TXD	IB	24C	Transmitter Data
RXD	OC	22C	Receiver Data
RLSD	OC	24A	Received Line Signal Detector
SCRTS	IB	21C	Forward Channel RTS
SCCTS	OC	20A	Forward Channel CTS
SCTXD	IB	19A	Forward Channel TXD
SCRLSD	OD	20C	Forward Channel RLSD
SCRXD	OD	18A	Forward Channel RXD
D. ANCILLARY CIRCUITS:			
RBCLK	OC	26A	Receiver Baud Clock
TBCLK	OC	27C	Transmitter Baud Clock
FRXD	OD	16A	FSK Receiver Data (inverted data)
$\overline{FRLSD}$	OD	17C	FSK Received Line Signal Detector
E. ANALOG SIGNALS:			
TXA	AA	31A	Transmitter Analog Output
RXA	AB	32A	Receiver Analog Input
AUXIN	AC	30A	Auxiliary Analog Input

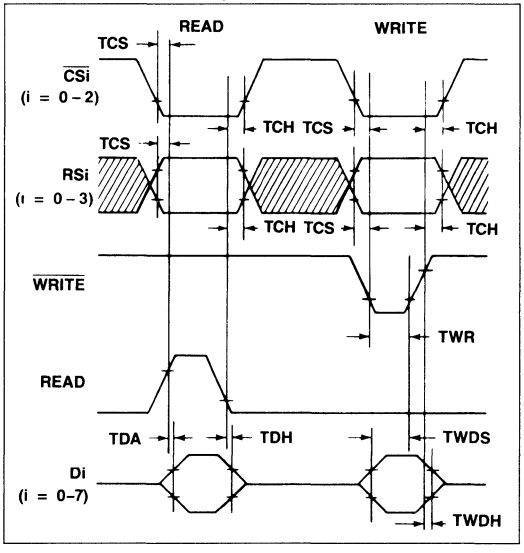
R96FT/SC Hardware Circuits (Continued)

Name	Type	Pin No.	Description
F. DIAGNOSTIC:			
EYEX	OC	15C	Eye Pattern Data—X Axis
EYEY	OC	14A	Eye Pattern Data—Y Axis
EYECLK	OA	14C	Eye Pattern Clock
EYESYNC	OA	13A	Eye Pattern Synchronizing Signal
Unused inputs tied to +5V or ground require individual 10K Ω series resistors.			

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the $\overline{EYECLK}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

Microprocessor Timing



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or Write	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
$\overline{CSi}$, RSi hold time after Read or Write	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type								
			IA	IB	IC	OA	OB	OC	OD	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.					2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.					0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.2 Min. [6]	2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.6 Max.[7]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.							±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.					
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.			
I_L	Output Current, Leakage	μA					±10 Max.				
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.			−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20					10	40
C_D	Capacitive Drive	pF				100	100	100		100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	TTL	3-State Transceiver	Open-Drain w/Pull-up

Notes 1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I Load = 0.36 mA
6. I Load = −400 μA
7. I Load = 2.0 mA

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604 ohms ±1%
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is TLVL setting +0.6 dB −1.4 dB. If unused, this input must be grounded near the modem connector. If used, it must be driven from a low impedance source.

SOFTWARE CIRCUITS

The R96FT/SC comprises three signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 1 update at half the modem sample rate (4800 bps). Registers in chip 0 and 2 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0–2), the register by Z(0–F), and the bit by Q(0–7, 0 = LSB).

Status Control Bits

The operation of the R96FT/SC is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a dash (—) are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R96FT/SC provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers in chip 2 allow user access to RAM locations via the X word registers (2:3 and 2:2) and the Y word register (2:1 and 2:0). The access code stored in RAM ACCESS X (2:5) selects the source of data for RAM DATA XM and RAM DATA XL (2:3 and 2:2). Similarly, the access code stored in RAM ACCESS Y (2:4) selects the source of data for RAM DATA YM and RAM DATA YL (2:1 and 2:0).

Reading of diagnostic RAM data is performed by storing the necessary access codes in 2:5 and 2:4, reading 2:0 to reset the associated data available bit (2:E:0), then waiting for the data available bit to return to a one. Data is now valid and may be read from 2:3 through 2:0.

An additional diagnostic is supplied by the sample rate processor (chip 1). Registers 1:2 and 1:3 supply a 16 bit AGC Gain Word. These two diagnostic data registers are updated at the sample rate during the data state and may be read by the host processor asynchronously.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

Baud Rate Processor (Chip 2) RAM Access Codes

No.	Function	X Access	Y Access	Register
1	Equalizer Input	C0	40	0,1,2,3
2	Equalizer Tap Coefficients	81–A0	01-20	0,1,2,3
3	Unrotated Equalizer Output	E1	61	0,1,2,3
4	Rotated Equalizer Output	E2	62	0,1,2,3
5	Decision Points (Ideal Data Points)	E8	68	0,1,2,3
6	Error Vector	E5	65	0,1,2,3
7	Rotation Angle	A7	Not Used	2,3
8	Frequency Correction	A5	Not Used	2,3
9	Eye Quality Monitor (EQM)	AC	Not Used	2,3

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	FSKT	ASCR	PCF	SCRTS	CF	DDEE	SCTLVL	
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	—	—	—	—	—	—	—	—
0	TRANSMITTER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RIA	—	—	—	RSB	RIE	—	RDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	$\overline{CDET}$	—	—
8	—	—	—	—	$\overline{P2DET}$	—	—	—
7	RTH		DDIS	—	—	SCEN	RDIS	—
6	TOD	RECEIVER CONFIGURATION						
5	—	—	—	—	—	—	—	—
4	—	—	—	—	—	—	—	—
3	AGC GAIN WORD (MSB)							
2	AGC GAIN WORD (LSB)							
1	—	—	—	—	—	—	—	—
0	RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS X							
4	RAM ACCESS Y							
3	RAM DATA XM							
2	RAM DATA XL							
1	RAM DATA YM							
0	RAM DATA YL							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

R96FT/SC Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
ASCR	Append Scrambled Ones	0:9:6	When control bit ASCR is a one, one baud of scrambled marks is included in the V.29FT and V.27FT training sequences. The RTS-CTS delay is thus extended by one baud period when ASCR is a one
A3L	Amplitude 3-Link Select	0:5:1	See LAEN
$\overline{\text{CDET}}$	Carrier Detector	1:9:2	When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
CEQ	Cable Equalizer Field	0:5:(4,5)	The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following table lists the possible cable equalizer selection codes: **CEQ** — **Cable Length (0.4 mm diameter)** 0 — 0.0 1 — 1.8 km 2 — 3.6 km 3 — 7.2 km
CF	Carrier Frequency	0:9:3	When control bit CF is a one, the transmitter carrier frequency for V.29FT changes from 1700 Hz to 1800 Hz.
DDEE	Digital Delay Equalizer Enable	0.9 2	When control bit DDEE is a one, a fourth order digital delay equalizer is inserted in the transmit path.
DDIS	Descramble Disable	1.7·5	When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path
D3L	Delay 3-Link Select	0:5.0	See LDEN
EPT	Echo Protector Tone	0:7:3	When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. This option is available in the V.27 and V 29 Configurations, although it is not specified in the CCITT V 29 recommendation.
$\overline{\text{FED}}$	Fast Energy Detector	1·9·6	When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband
(None)	FREQL/FREQM	0:2:0–7, 0.3:0–7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below· *FREQM Register (0:3)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below: **Frequency (Hz)** — **FREQM** — **FREQL** 462 — 0C — 52 1100 — 1D — 55 1650 — 2C — 00 1850 — 31 — 55 2100 — 38 — 00

R96FT/SC Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
FSKT	FSK Transmitter Configuration	0:9:7	The V.21 Channel 2 (300 bps synchronous FSK) transmitter configuration is selected by setting the FSKT control bit to a one (see TSB). While set to a one, this control bit overrides the configuration selected by the control code in register 0:6. The FSK data may be transmitted in parallel mode or in serial mode (see TPDM).
LAEN	Link Amplitude Equalizer Enable	0:5:3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table: **LAEN** / **A3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5:2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN** / **D3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
L2ACT	Remote Digital Loopback Activate	0:4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT Recommendation V.54 loop 2.
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT Recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0:4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to CCITT Recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4:5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
PCF	Primary Channel Filter	0:9:5	When control bit PCF is a one, the 2400 baud primary channel transmitter filter is set to a narrower bandwidth than normal.
$\overline{\text{P2DET}}$	Period 2 Detector	1:8:3	When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a period 2 sequence has been detected. This bit sets to a one at the start of the period N sequence. This bit is only significant for CCITT V.29 and V.27 bis/ter configurations.
(None)	RAM Access X	2:5:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access Y	2:4:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word Y (2:1 and 2:0).
(None)	RAM Data XL	2:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XM	2:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data YL	2:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YM	2:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 2.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{\text{IRQ}}$ low.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven to zero when status bit RBDA is a one.

R96FT/SC Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Receiver Configuration</td><td>1:6:0–6</td><td>
The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB).

Note: The receiver must be disabled prior to changing configurations. See RDIS.

Receiver Configuration Control Codes

Control codes for the modem receiver configuration are:

<table>
<tr><th colspan="2">Configuration</th><th rowspan="2">Configuration Code (Hex)</th></tr>
<tr><th>V29</th><th>V27 bis/ter</th></tr>
<tr><td>FT/9600
FT/7200
FT/4800</td><td>

FT/4800
FT/2400</td><td>1C
1A
19
0A
09</td></tr>
<tr><td>9600
7200
4800</td><td>

4800 long
2400 long
4800 short
2400 short</td><td>14
12
11
22
21
02
01</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.29 descrambler
2400/4800 bps Gearshift/V.27 bis/ter descrambler</td><td>61[1]
41[1]</td></tr>
<tr><td colspan="2">V.21 Channel 2</td><td>See Note 2</td></tr>
</table>
1. The Receiver Configuration code automatically changes from a hex 61 (or hex 41) to a hex 64 (or hex 44) when the receiver transitions from the 2400 bps data state to the 4800 bps data state.
2. The FSK receiver is active at all times. Two ancillary hardware circuits, $\overline{\text{FRLSD}}$ and $\overline{\text{FRXD}}$, are supplied for FSK message reception. $\overline{\text{FRLSD}}$ is described under the Received Line Signal Detector section. $\overline{\text{FRXD}}$ provides inverted FSK received data. Timing extraction must be performed on the $\overline{\text{FRXD}}$ signal externally as no FSK receiver data clock is provided by the R96FT/SC.
</td></tr>
<tr><td>(None)</td><td>Receiver Data</td><td>1:0:0–7</td><td>The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data</td></tr>
<tr><td>RDA</td><td>Receiver Data Available</td><td>1:E:0</td><td>Status bit RDA goes to a one when the receiver writes data to register 1:0. RDA goes to a zero when the host processor reads data from register 1:0.</td></tr>
<tr><td>RDIS</td><td>Receiver Disable</td><td>1:7:1</td><td>When control bit RDIS is a one, the receiver is disabled, $\overline{\text{RLSD}}$ is turned off and RXD is clamped to all marks. This bit can be used to squelch the receiver during half duplex transmissions over two wires. This bit must be set to a one prior to changing the receiver configuration.</td></tr>
<tr><td>RIA</td><td>Receiver Interrupt Active</td><td>1:E:7</td><td>This status bit is a one whenever the receiver sample rate device is driving $\overline{\text{IRQ}}$ to zero.</td></tr>
<tr><td>RIE</td><td>Receiver Interrupt Enable</td><td>1:E:2</td><td>When the host processor writes a one in the RIE control bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven to zero when status bit RDA is a one.</td></tr>
<tr><td>RSB</td><td>Receiver Setup Bit</td><td>1:E:3</td><td>When the host processor changes the receiver configuration, the FSKR bit or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective.</td></tr>
<tr><td>RTH</td><td>Receiver Threshold Field</td><td>1:7:6,7</td><td>
The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB):

<table>
<tr><th>RTH</th><th>$\overline{\text{RLSD}}$ On</th><th>$\overline{\text{RLSD}}$ Off</th></tr>
<tr><td>0</td><td>> –43 dBm</td><td>< –48 dBm</td></tr>
<tr><td>1</td><td>> –33 dBm</td><td>< –38 dBm</td></tr>
<tr><td>2</td><td>> –26 dBm</td><td>< –31 dBm</td></tr>
<tr><td>3</td><td>> –16 dBm</td><td>< –21 dBm</td></tr>
</table>
</td></tr>
</table>

R96FT/SC Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
SCEN	Forward Channel Enable	1:7:2	When control bit SCEN is a one, the forward channel demodulator is enabled and the primary channel receiver carrier frequency is changed from 1700 to 1800 Hz in V.29 FT configurations.
SCRTS	Forward Channel Request-to-Send	0:9:4	When control bit SCRTS is a one, the modem begins a forward channel transmit sequence. Transmission continues until SCRTS is a zero. SCRTS in the interface memory is ORed with signal $\overline{SCRTS}$ on the card connector
SCTLVL	Forward Channel Transmit Level	0:9:0-1	The forward channel transmit level is set relative to the main channel transmit level by the following SCTLVL codes: **SCTLVL Code** / **Forward Channel Transmit Level Relative to Primary Channel** 0 / −6 dB 1 / −10 dB 2 / −14 dB 3 / −18 dB
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector disable tone is 30 ms long rather than 185 ms. (See TSB.)
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0·0. When the transmitter empties register 0:0, this bit sets to a one.
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** / **Transmitter Analog Output*** 0 / −1 dBm ±1 dB 1 / −3 dBm ±1 dB 2 / −5 dBm ±1 dB 3 / −7 dBm ±1 dB 4 / −9 dBm ±1 dB 5 / −11 dBm ±1 dB 6 / −13 dBm ±1 dB 7 / −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-On-Data	1:6:7	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-data.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0) rather than the serial hardware data input.

R96FT/SC Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter Configuration</td><td>0:6:0–7</td><td>The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB.)

Transmitter Configuration Control Codes

Control codes for the modem transmitter configurations are:
<table>
<tr><th colspan="2">Configuration</th><th rowspan="2">Configuration Code (Hex)</th></tr>
<tr><th>V29</th><th>V27 bis/ter</th></tr>
<tr><td>FT/9600
FT/7200
FT/4800</td><td>

FT/4800
FT/2400</td><td>1C
1A
19
0A
09</td></tr>
<tr><td>9600
7200
4800</td><td>

4800 long
2400 long
4800 short
2400 short</td><td>14
12
11
22
21
02
01</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.29 Scrambler
2400/4800 bps Gearshift/V.27 bis/ter Scrambler</td><td>61
41</td></tr>
<tr><td colspan="2">V.21 Channel 2</td><td>See FSKT</td></tr>
<tr><td colspan="2">Tone transmit</td><td>80</td></tr>
</table></td></tr>
<tr><td>(None)</td><td>Transmitter Data</td><td>0:0:0–7</td><td>The host processor conveys output data to the transmitter in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

Note: Data is transmitted bit zero first.
<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.29 9600 bps</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.29 7200 bps</td><td colspan="2">Not Used</td><td colspan="2">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.29 4800 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td>Baud 0</td></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td>Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td>Baud 0</td></tr>
<tr><td>2400 bps Gearshift</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td>Baud 0</td></tr>
<tr><td>4800 bps Gearshift</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
</table></td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the SEPT bit or the FSKT bit, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a one, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A.</td></tr>
</table>

The following is a list of the configurations that may be used with the forward channel and the states of the various control bits.

	Transmitter Control		Receiver Control
Configuration	PCF 0:9:5	CF 0:9:3	SCEN 1:7:2
FT/V.29/9600	1	1	1
FT/V.29/7200	1	1	1
FT/V.29/4800	1	1	1
FT/V.27/4800	0	X	1
FT/V.27/2400	0	X	1
*V.27/4800	0	X	1
*V.27/2400	0	X	1
V.21 FSK	X	X	1

*Both V.27 long and short train may be used. X = Don't care.

Note that CCITT V.29 and Gearshift configurations cannot be used with the forward channel.

POWER-ON INITIALIZATION

When power is applied to the R96FT/SC, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is generated.

At POR time the modem defaults to the following configuration: fast train, V.29, 9600 bps, no echo protector tone, 1700 Hz carrier frequency, scrambled ones segment disabled, serial data mode, internal clock, cable equalizers disabled, transmitter digital delay equalizer disabled, link amplitude equalizer disabled, link delay equalizer disabled, transmitter output level set to -1 dBm ± 1 dB, interrupts disabled, receiver threshold set to -43 dBm, and train-on-data enabled.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after $\overline{POR}$ is removed.

PERFORMANCE

Whether functioning in V.27, V.29 or the proprietary fast train configurations, the R96FT/SC provides the user with high performance.

POLLING SUCCESS

In the 9600 bps fast train configuration the modem approaches a 98% success rate over unconditioned 3002 lines for a signal-to-noise ratio of 26 dB, with a received signal level of -20 dBm. When used in conjunction with the 75 bps forward channel, 9600 bps main channel polling performance degrades by approximately 2 dB.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of -20 dBm as illustrated.

The BER curves shown were prepared from data obtained using a TAS 1010 test system.

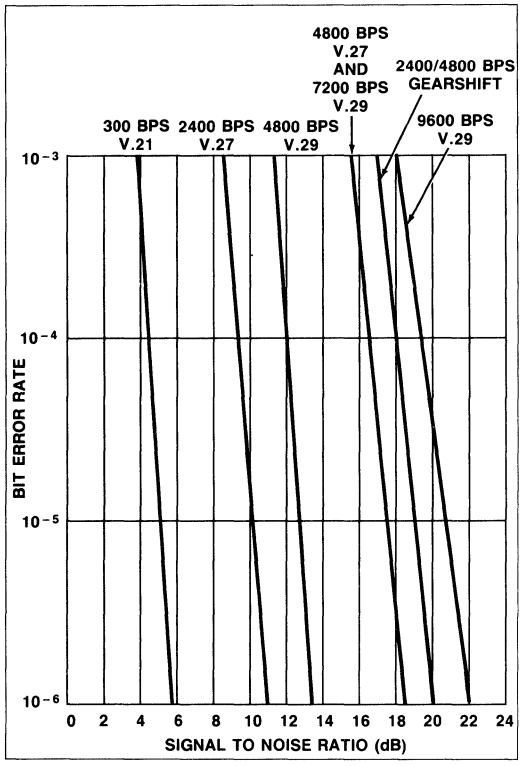
PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz, or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

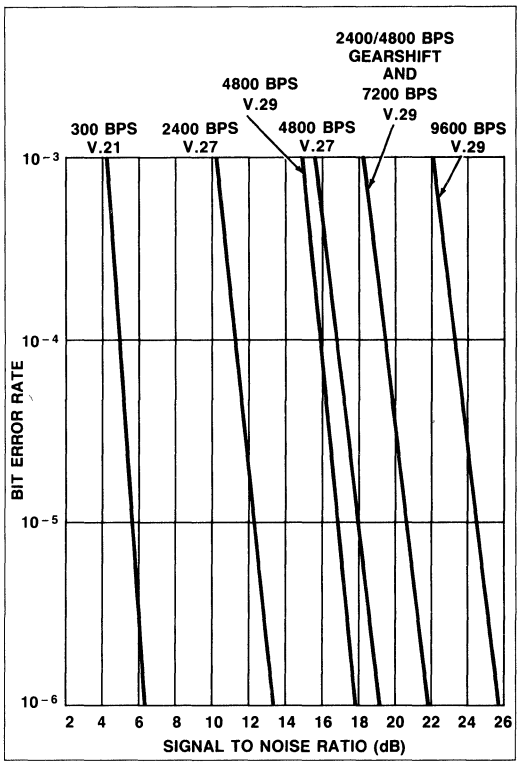
At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

An example of the BER performance capabilities is given in the following diagrams:



Typical BER Performance
Back-to-Back, –20 dBm Receive Signal Level



Typical BER Performance
3002 Unconditioned Line, –20 dBm Receive Signal Level

GENERAL SPECIFICATIONS

Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	650 mA	<820 mA
+12 Vdc	±5%	50 mA	< 80 mA
−12 Vdc	±5%	60 mA	< 90 mA

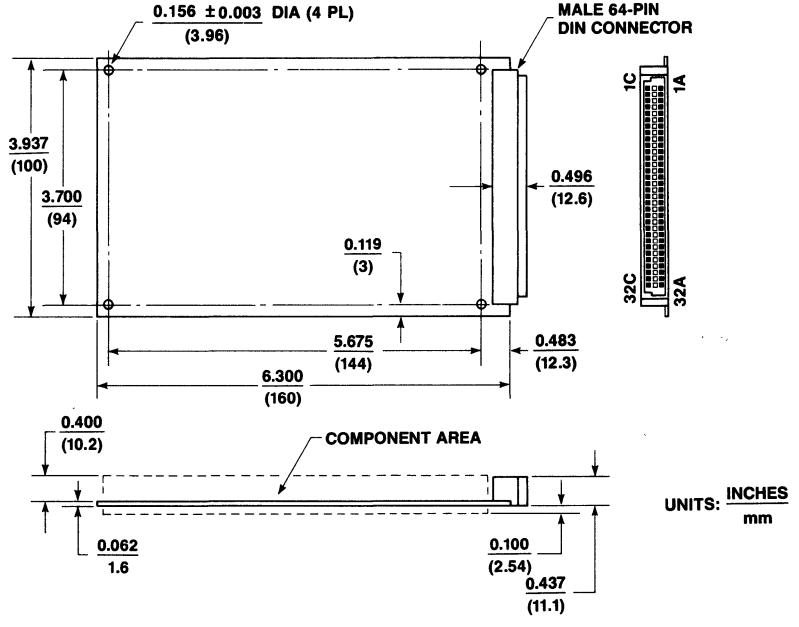
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Modem Mechanical Considerations

Parameter	Specification
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
PCB Dimensions:	
Width	3.937 in. (100 mm)
Length	6.300 in. (160 mm)
Height	0.40 in. (10.2 mm)
Weight (max):	5.5 oz (156 g)
Lead Extrusion (max.)	0.100 in. (2.54 mm)



R96FT/SC Modem Dimensions and Pin Locations

Rockwell

R144DP
V.33 14.4 kbps Full-Duplex Modem

INTRODUCTION

The Rockwell R144DP is a synchronous 14.4 Kbps data pump. It can operate over unconditioned or conditioned lines, through the appropriate line termination. It is packaged in a small module with a DIN connector, or a smaller module with dual- in-line pin (DIP) connection.

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.33, V.29 and V.27 bis/ter. The R144DP can operate at speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps.

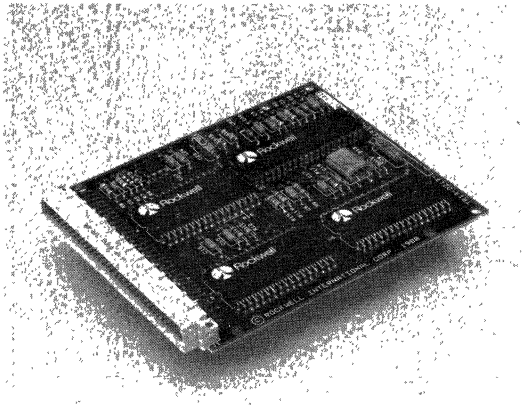
The R144DP is designed for use in ultra high speed data applications. The use of trellis-coded modulation (TCM) in the 9.6 Kbps and 7.2 Kbps modes, in addition to those modes specified by V.33, adds significantly to the performance of the modem under these operating conditions. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size and serial/parallel host interface simplify system development and reduce system production cost. The DIN connector version can be mated to a matching DIN receptacle on the host module, whereas the DIP connector version can be directly installed onto the host module.

CMOS digital signal processor (DSP) and integrated analog (IA) devices reduce modem power consumption.

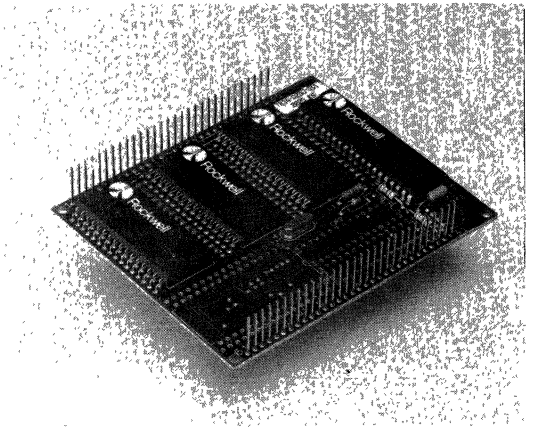
This data sheet applies to the R144DP with device numbers C5301-16, C5306-17, C5307-17 and subsequent.

FEATURES

- Compatibilities:
  — CCITT: V.33, V.29 and V.27 bis/ter
- 4-Wire Full-Duplex
- Trellis-Coded Modulation (TCM) at 14.4 Kbps, 12 Kbps, 9.6 Kbps and 7.2 Kbps
- DTE Interface
  — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  — Electrical: TTL and CMOS Compatible
- Dynamic Range: – 43 dBm to 0 dBm
- Equalization
  — Compromise Equalizer in Transmitter
  — Automatic Adaptive Equalizer in Receiver
- Auto-Dial and Auto-Answer Capability
- Diagnostic Capability
- Loopback
  — Local and Remote Analog
  — Remote Digital
- Small Size
  — 100 mm × 120 mm (3.94 in. × 4.73 in.) with DIN Connector
  — 82 mm × 100 mm (3.23 in. × 3.94 in.) with DIP Connection
- Low Power Consumption: 1.3 W (Typical)



R144DP DIN Connector Version



R144DP DIP Connector Version

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

TONE GENERATION

Under control of the host processor, the modem can generate single or dual voice-band tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

DATA ENCODING

The data encoding conforms to CCITT recommendations V.33, V.29 and V.27.

EQUALIZERS

Equalization functions are provided that improve performance when operating over low quality lines.

Compromise Equalizer — A 40-tap digital finite impulse response (FIR) filter in the transmitter provides compromise equalization. The filter taps can be changed in DSP RAM for varying line conditions. The default equalizer tap coefficients compensate for half the amplitude distortion of a 3002 unconditioned line and for half the group delay distortion of a 3002 unconditioned line. The filter can be enabled or disabled using the CEQ bit in the transmitter interface memory.

Automatic Adaptive Equalizer — A 48-tap automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer using the EQT2 bit in the chip 2 interface memory.

TRANSMITTED DATA SPECTRUM

When the compromise equalizer is disabled, the transmitter spectrum is shaped by raised cosine filter functions as follows:

Configuration	Raised Cosine Filter Function
V.33 and V.29	Square root of 12.5% or 20% as selected by the SHAP0 bit in the transmitter interface memory.
V.27 1600 baud	Square root of 50%
V.27 1200 baud	Square root of 90%

TURN-ON AND TURN-OFF SEQUENCES

Turn-on and turn-off sequence times are shown in Table 2.

Table 2. Turn-on and Turn-off Sequences

Configuration	RTS-CTS Delay Time	Turn-Off Time	
	Echo Protector Tone Disabled	Remaining Data and Scrambled 1s	No Transmitted Energy
V.33	1393 ms	15 ms	—
V.29	253 ms	12 ms	—
V.27 4800 bps long	708 ms	7 ms	20 ms
V.27 4800 bps short	50 ms	7 ms	20 ms
V.27 2400 bps long	943 ms	10 ms	20 ms
V.27 2400 bps short	67 ms	10 ms	20 ms

TRANSMIT LEVEL

The transmitter output level is selectable from −0.5 dBm to −15.5 dBm in 1 dB steps and is accurate to ±0.5 dB. The output level can also be fine tuned to a value within a 1 dB step by changing a gain constant in RAM.

TRANSMITTER TIMING

Transmitter timing is selectable between internal (±0.01%), external or loopback.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with V.33, V.29 or V.27 depending on the selected configuration.

RECEIVE LEVEL

The receiver satisfies performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the Receiver Analog (RXA) input.

RECEIVER TIMING

The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

CARRIER RECOVERY

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector ($\overline{RLSD}$) is off. $\overline{RLSD}$ can also be clamped to a mark by a bit in the receiver sample rate device interface memory.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits per Symbol		Constellation Points
					Data	TCM	
V.33 14400	TCM	1800 or 1700	14400	2400	6	1	128
V.33 12000	TCM	1800 or 1700	12000	2400	5	1	64
V.33 9600 TCM[2]	TCM	1800 or 1700	9600	2400	4	1	32
V.33 7200 TCM[2]	TCM	1800 or 1700	7200	2400	3	1	16
V.29 9600	QAM	1700	9600	2400	4	0	16
V.29 7200	QAM	1700	7200	2400	3	0	8
V.29 4800	QAM	1700	4800	2400	2	0	4
V.27 4800	QAM	1800	4800	1600	3	0	8
V.27 2400 Tone Transmit	QAM	1800	2400	1200	2	0	4

Notes:
1. Modulation legend: TCM: Trellis-Coded Modulation
   QAM: Quadrature Amplitude Modulation
2. Proprietary

AUTO-DIALING AND AUTO-ANSWERING CONTROL

General Description

Functions are provided to allow the host to perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection and a comprehensive supervisory tone detection scheme. The major parameters of these functions are host programmable, enabling the host to customize the modem to work on the public switched telephone network (PSTN).

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path. Therefore, the tone detect signal does not pass through the highpass section of the analog receive bandpass filter, enabling the tone detection to be largely independent of the receiver status.

There are, however, some restrictions depending on the receiver configuration and status:

1. When DATA1 bit (see Table 8) is a 0, then all three tone detectors are enabled.
2. When DATA1 bit is a 1, then tone detectors A and B are enabled and tone detector C is disabled.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit in interface memory causing tone detector C to be an eighth order filter.

Supervisory Tone Detectors, Default Characteristics

The default bandwidths and thresholds of the tone detectors are as follows:

Tone Detector	Bandwidth	Turn-On Threshold	Turn-Off Threshold
A	245–650 Hz	– 25 dBm	– 31 dBm
B	360–440 Hz	– 25 dBm	– 31 dBm
C Prefilter	0–500 Hz	N/A	N/A
C	50–110 Hz	*	*

*Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range – 1 dBm to – 26 dBm.

HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 1) shows the typical modem connection in a system. In this diagram, any point that is active low is represented by a small circle at the signal point.

Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signals TDCLK and $\overline{IRQ}$, respectively. Active low signals are named with an overscore (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high, (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals shown in Figure 1 are organizated into six functional groups: overhead, microprocessor interface, V.24 interface, ancillary, analog, and diagnostic. These signals, along with their connector pin numbers and interface circuit types, are listed in Table 3. The digital interface characteristics are defined in Table 4.

POWER-ON-RESET

When power is applied to the modem, the modem pulses Power-On-Reset ($\overline{POR}$) low to begin the POR sequence. The modem is ready to use 350 ms after the low-to-high transition of $\overline{POR}$. The POR sequence is reinitiated any time the + 5V supply drops below + 3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 μs. $\overline{POR}$ is not pulsed low by the modem when the POR sequence is initiated externally. The POR sequence initializes the modem interface memory to default values (Table 8). This action leaves the modem configured as follows:

- V.33 14,400 bps
- 1800 Hz carrier frequency
- Serial channel data
- T equalizer
- – 43 dBm receiver threshold
- Transmitter compromise equalizer enabled
- Train-on-data disabled

NOTE: If the modem is used in applications where the supply voltage can drop below + 4.75V but not low enough to cause a POR sequence (i.e., < + 3.5V), the host system should generate a $\overline{POR}$ signal upon supply voltage recovery to ensure modem initialization and operation.

MICROPROCESSOR INTERFACE

Nineteen address, data, control, and interrupt hardware interface signals allow modem connection to an 8086 or 6500 compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000.

The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The significance of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

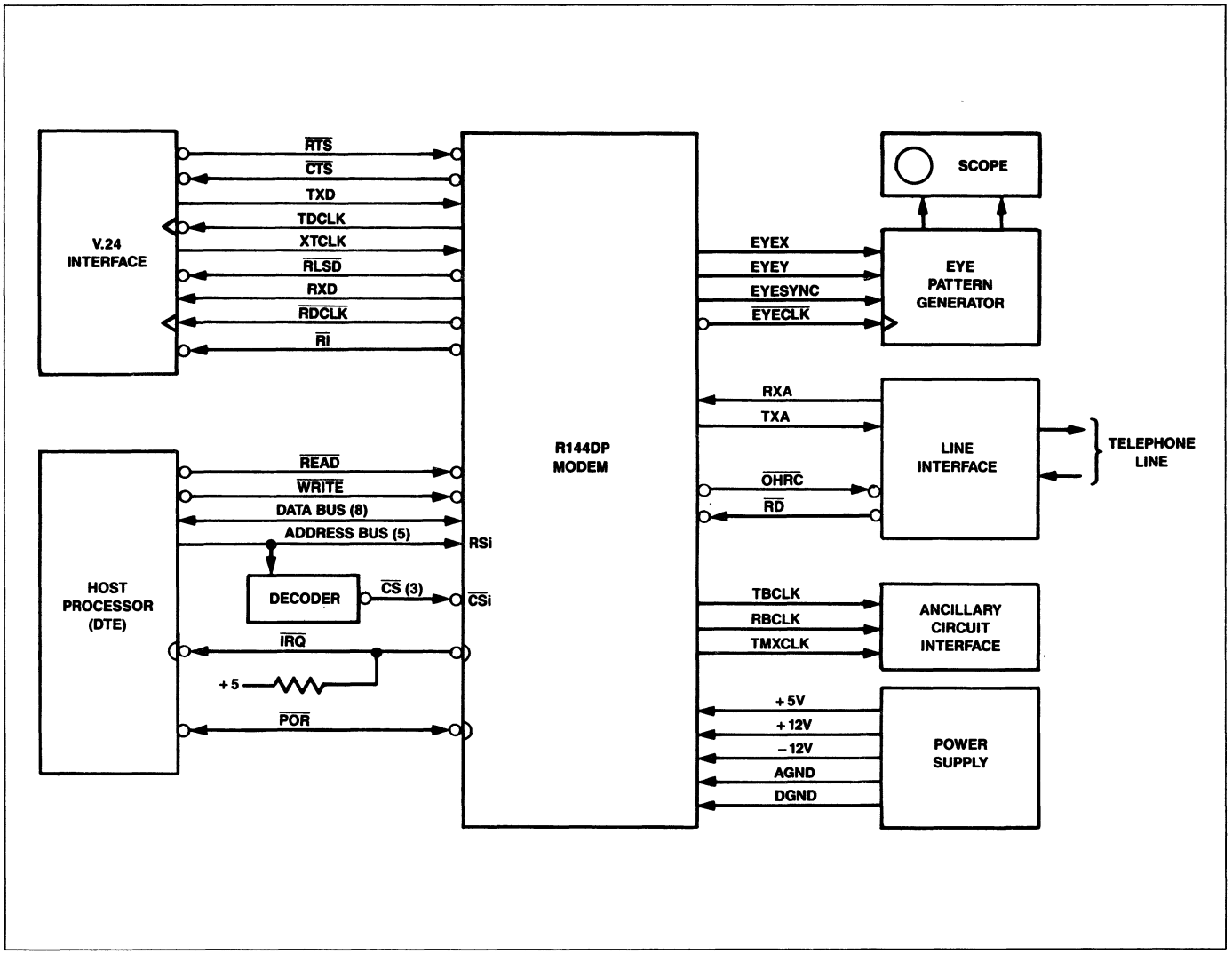


Figure 1. R144DP Functional Interconnect Diagram

Table 3. R144DP Hardware Interface Signals

Name	Type[1]	DIN[2] Pin No.	DIP[3] Pin No.	Description
A. OVERHEAD:				
Ground (A)	AGND	31C,32C	30,31	Analog Ground Return
Ground (D)	DGND	3C,8C, 5A,10A	29,37,53	Digital Ground Return
+5V	PWR	19C,23C, 26C,30C	1,45,61	+5 Volt Supply
+12V	PWR	15A	32	+12 Volt Supply
−12V	PWR	12A	36	−12 Volt Supply
$\overline{POR}$	IA/OB	13C	2	Power-On-Reset
B. MICROPROCESSOR INTERFACE:				
D7	IA/OB	1C	3	Data Bus (8 Bits)
D6	IA/OB	1A	4	
D5	IA/OB	2C	5	
D4	IA/OB	2A	6	
D3	IA/OB	3A	7	
D2	IA/OB	4C	8	
D1	IA/OB	4A	9	
D0	IA/OB	5C	10	
RS4	IA	8A	15	Register Select (5 Bits)
RS3	IA	6C	16	
RS2	IA	6A	17	
RS1	IA	7C	18	
RS0	IA	7A	19	
$\overline{CS0}$	IA	10C	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	13	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	12C	14	Read Enable
$\overline{WRITE}$	IA	11A	12	Write Enable
$\overline{IRQ}$	OC	11C	11	Interrupt Request
C. V.24 INTERFACE:				
$\overline{RDCLK}$	OA	21A	23	Receive Data Clock
TDCLK	OA	23A	46	Transmit Data Clock
XTCLK	IA	22A	51	External Transmit Clock
$\overline{RTS}$	IA	25A	50	Request-to-Send
$\overline{CTS}$	OA	25C	49	Clear-to-Send
TXD	IA	24C	48	Transmitter Data
RXD	OA	22C	26	Receiver Data
$\overline{RLSD}$	OA	24A	27	Received Line Signal Detector
$\overline{RI}$	OA	16A	25	Ring Indicator
D. ANCILLARY CIRCUITS:				
RBCLK	OA	26A	22	Receiver Baud Clock
TBCLK	OA	27C	47	Transmitter Baud Clock
TMXCLK	OA	18C	43	Transmitter Mux Clock
E. LINE INTERFACE:				
TXA	AA	31A	34	Transmitter Analog Output
RXA	AB	32A	33	Receiver Analog Input
$\overline{OHRC}$	OD	29A	35	Off-Hook Relay Control
$\overline{RD}$	IA	27A	24	Ring Detect
F. DIAGNOSTIC:				
EYEX	OA	15C	56	Eye Pattern Data—X Axis
EYEY	OA	14A	55	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	57	Eye Pattern Clock
EYESYNC	OA	13A	58	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 4 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. The following DIN pins should be left open: 17A, 17C, 18A, 20A, 20C, 28A, 28C and 30A.
3. The following DIP pins should be left open: 28, 39, 41, 44, 52, 59 and 60.
4. The following DIN pins are not used but should be connected to DGND through individual 10 KΩ series resistors: 16C, 19A, 21C and 29C.
5. The following DIP pins are not used but should be connected to DGND through individual 10 KΩ series resistors: 38, 40, 42 and 54.
6. Unused inputs tied to +5V or ground require individual 10 KΩ series resistors.

Table 4. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	OA	OB	OC	OD
V_{IH}	Input Voltage, High	V	2.0 Min.				
V_{IL}	Input Voltage, Low	V	0.8 Max.				
V_{OH}	Output Voltage, High	V		3.5 Min.[1]	3.5 Min.[1]		5.0 Max.
V_{OL}	Output Voltage, Low	V		0.4 Max.[2]	0.4 Max.[3]	0.4 Max.[2]	0.75 Typ.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.				
I_{OH}	Output Current, High	mA		−0.1 Max.	−0.1 Max		0[4]
I_{OL}	Output Current, Low	mA		1.6 Max.	0.8 Max.	1.6 Max.	15.0 Max.[5]
I_L	Output Current, Leakage	μA		±10 Max.	±10 Max.		
C_L	Capacitive Load	pF	5				
C_D	Capacitive Drive	pF		100	100	100	
	Circuit Type		TTL	TTL 3-state	TTL 3-state	Open-Drain	Open-Drain

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = 0.8 mA
4. μA leakage
5. Can drive a +5V relay with coil resistance greater than 360Ω.

Data Lines (D0–D7)

Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.

Chip Selects ($\overline{CS0}$–$\overline{CS2}$) and Register Selects (RS0-RS4)

The three active low chip select lines ($\overline{CS0}$–$\overline{CS2}$) select one of three modem digital signal processor (DSP) devices. The five active high register select lines (RS0–RS4) address interface memory registers within the selected DSP interface memory. All eight of these lines are typically connected to the host bus address lines; the register select lines to the five least significant lines (A0–A4) and the chip select lines to the next two significant lines (A5–A6) through a decoder.

The selected DSP decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7).

Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

During a read cycle, data from the selected DSP interface memory register is gated onto the data bus by means of three-state drivers in each DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

The read/write cycle timing waveforms are illustrated in Figure 2 and the timing requirements are specified in Table 5.

Table 5. Microprocessor Interface Timing Parameters

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$i Setup Time	TCS	0	—	ns
RSi Setup Time	TRS	25	—	ns
Data Access Time	TDA	—	75	ns
Data Hold Time	TDHR	10	—	ns
Control Hold Time	THC	10	—	ns
Write Data Setup Time	TWDS	20	—	ns
Write Data Hold Time	TDHW	10	—	ns

Interrupt Request ($\overline{IRQ}$)

The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in the DSP interface memory to indicate immediate change of conditions in any of the three modem DSP devices. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.

The DSP $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). Each of the individual DSP $\overline{IRQ}$ output lines is wire-ORed to form the modem $\overline{IRQ}$ output signal. The modem $\overline{IRQ}$ output can also be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25W, is sufficient.

2

V.24 INTERFACE

Nine pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels using 1489 receivers and 1488 drivers, or their equivalents.

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.

Received Data (RXD)

The modem presents received serial data to the local DTE on the Received Data (RXD) output.

Request To Send ($\overline{RTS}$)

Activating Request to Send ($\overline{RTS}$) causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The $\overline{RTS}$ pin is logically ORed with the RTS bit.

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) active indicates to the local DTE that the modem will transmit any data present on TXD. $\overline{CTS}$ response times from an active condition of $\overline{RTS}$ are shown in Table 2.

Received Line Signal Detector ($\overline{RLSD}$)

Received Line Signal Detector ($\overline{RLSD}$) active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that energy is not a training sequence.

For V.33, V.29 and V.27 bis/ter, $\overline{RLSD}$ goes active at the end of the training sequence. If energy is above threshold and training is not detected, the $\overline{RLSD}$ off-to-on response time is 15 ±10 ms. The $\overline{RLSD}$ on-to-off time is 40 ±10 ms for V.33, 30 ±9 ms for V.29, or 10 ±5 ms for V.27. The $\overline{RLSD}$ on-to-off time ensures that all valid data bits have appeared on RXD.

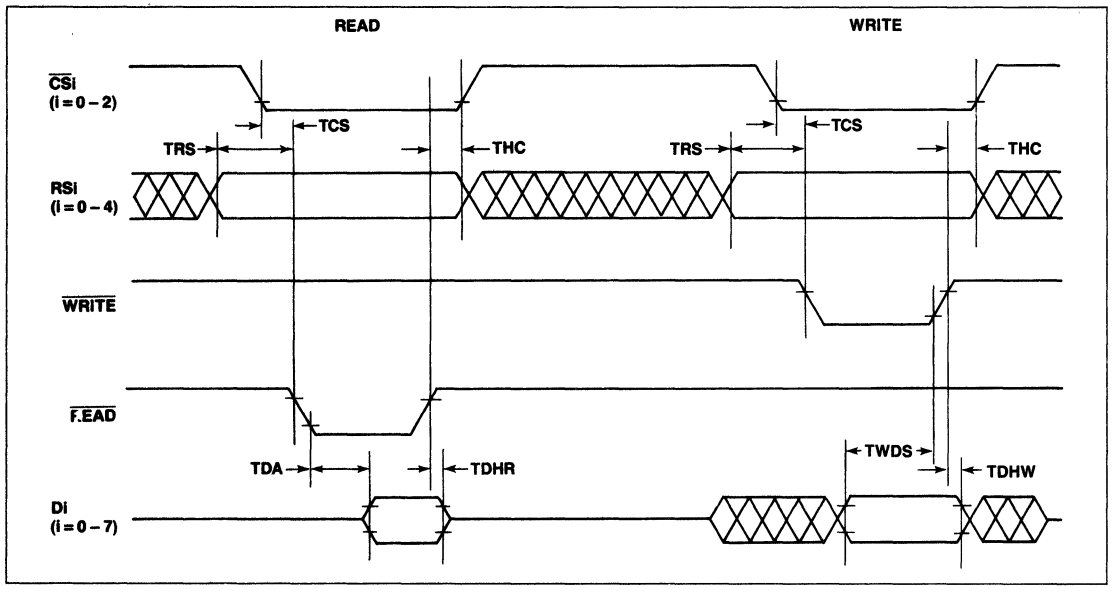


Figure 2. Microprocessor Interface Timing Waveforms

One of four $\overline{\text{RLSD}}$ receive level threshold options can be selected (Table 6). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than −43 dBm. The $\overline{\text{RLSD}}$ on and off thresholds are host programmable in DSP RAM.

Table 6. $\overline{\text{RLSD}}$ On and OFF Thresholds

Option	Receive Level	
	RLSD On	RLSD Off
0	> −43 dBm	< −48 dBm
1	> −33 dBm	< −38 dBm
2	> −26 dBm	< −31 dBm
3	> −16 dBm	< −21 dBm

Transmit Data Clock (TDCLK)

The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%.

Transmit Data (TXD) must be stable during the one μs periods immediately preceding the rising edge of TDCLK and following the rising edge of TDCLK. The TDCLK source can be internal, external (input on XTCLK) or slave (to $\overline{\text{RDCLK}}$) as selected by bits in the transmitter interface memory.

External Transmit Clock (XTCLK)

In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the sme characteristics of TDCLK. The XTCLK input is then reflected at the TDCLK output.

Receive Data Clock ($\overline{\text{RDCLK}}$)

The modem outputs a synchronous Receive Data Clock ($\overline{\text{RDCLK}}$) for USRT timing. The $\overline{\text{RDCLK}}$ frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The $\overline{\text{RDCLK}}$ low-to-high transitions coincide with the center of the received data bits. The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

Ring Indicator ($\overline{\text{RI}}$)

The Ring Indicator (RI) output follows the ringing signal present on the line with a low level (0V) during the ON time, and a high level (+5V) during the OFF time coincident with the ringing signal.

The RI status bit in chip 2 reflects the state of the $\overline{\text{RI}}$ output.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK) outputs have no counterpart in the V.24 or RS-232-C recommendations since they mark the baud interval rather than the data rate for the transmitter and receiver, respectively. These baud clocks are useful in identifying the order of data bits in a baud (e.g., for multiplexing data). Both signals are active high. The first bit in each baud begins with the falling edge of the corresponding baud clock.

Transmitter Multiplexer Clock (TMXCLK)

The Transmitter Multiplexer Clock (TMXCLK) output is a 288 kHz clock which is internally divided down to create the Transmitter Baud Clock (TBCLK). TMXCLK is also a common multiple of all the possible transmitter data clocks. The high-to-low transitions of TDCLK coincide with the high-to-low transitions of TMXCLK.

LINE INTERFACE

The Transmitter Analog (TXA) output and Receiver Analog (RXA) input allow modem connection to either a leased line or the public switched telephone network (PSTN) through an audio transformer or a data access arrangement. The analog signal characteristics of TXA and RXA are described in Table 7.

Table 7. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604 ohms ± 1%.
RXA	AB	The receiver input impedance is 66.5K ohms.

Transmitter Analog (TXA)

The Transmitter Analog (TXA) output can drive an audio transformer or data access arrangement. TXA is a low impedance amplifier output in series with an internal 604 ohm ± 1% resistor to match a standard telephone load of 600 ohms.

Receiver Analog (RXA)

The Receiver Analog (RXA) input can originate from an audio transformer or data access arrangement. The input impedance is nominally 66.5K ohms. The RXA input must be shunted by an external 604 ohm ±1% resistor in order match a 600 ohm source.

Transient protection for TXA and RXA is recommended when interfacing directly to a transformer. This protection may take the form of back-to-back zener diodes or a varistor across the transformer.

Ring Detect ($\overline{RD}$)

The Ring Detect ($\overline{RD}$) input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving $\overline{RD}$ should be a 4N35 optoisolator or equivalent. The circuit driving $\overline{RD}$ should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING.

DATA2 bit must be set to a 0 to enable ring detection. Detected ring signals are reflected on the $\overline{RI}$ output.

Off-Hook Relay Control ($\overline{OHRC}$)

$\overline{OHRC}$ is an output designed to directly drive a +5V relay coil with a worst case resistance of 360 ohm having a must operate voltage of 4.0 Vdc. A clamp diode is integrated in the modem which eliminates the need for the diode across the relay coil. An external transistor can be used to drive heavier loads (e.g., electromechanical relays). $\overline{OHRC}$ is controlled by the host by setting the RA bit in the interface memory.

DIAGNOSTIC SIGNALS

Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. Timing of these signals is illustrated in Figure 3.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

EYEX and EYEY outputs are 15-bit words, each with 8-bits of significance. The 15-bit data words are shifted out most significant bit first with the seven most significant bits equal to zero. EYEX and EYEY are clocked by the rising edge of $\overline{EYECLK}$.

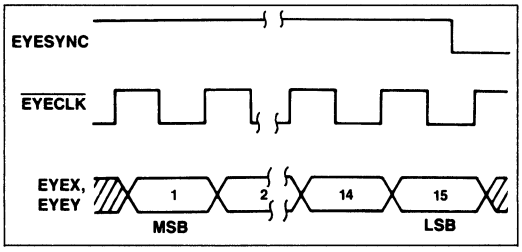


Figure 3. Eye Pattern Timing

$\overline{EYECLK}$

$\overline{EYECLK}$ is a clock for use by the serial-to-parallel converters. The $\overline{EYECLK}$ output is a 288 kHz clock which is internally divided down to create the Receiver Baud Clock (RBCLK). $\overline{EYECLK}$ is also a common multiple of all the possible receiver data clocks. The low-to-high transitions of RDCLK coincide with the low-to-high transitions of $\overline{EYECLK}$.

EYESYNC

EYESYNC is a strobe for loading the D/A converters.

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in three DSPs: transmitter device, receiver sample rate device, and receiver baud rate device.

INTERFACE MEMORY

Each DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in each DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus shared between the three DSPs.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAPS

Memory maps of the 96 addressable registers in the modem transmitter (chip 0), receiver sample rate (chip 1), and receiver baud rate (chip 2) devices are shown in Figure 4. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory.

INTERFACE MEMORY BIT DEFINITIONS

Table 8 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0,1 or 2), the register number by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

R144DP DSP Interface Memory (Chip 0)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA0	NCIA0	—	NSIE0	NEWS0	NCIE0	—	NEWC0
1E	—	DBIA0	—	—	—	DBIE0	—	DBA0
1D	XACC0	—	—	—	—	XCRD0	XWT0	XCR0
1C	X RAM ADDRESS (XADD0)							
1B	YACC0	—	—	—	—	YCRD0	YWT0	YCR0
1A	Y RAM ADDRESS (YADD0)							
19	X RAM DATA MSB (XDAM0)							
18	X RAM DATA LSB (XDAL0)							
17	Y RAM DATA MSB (YDAM0)							
16	Y RAM DATA LSB (YDAL0)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	TLVL				—	—	TXCLK	
12	TCONF							
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	—	—	CTS	—	—	—	—	—
0E	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	DTMF	—	—	—	—	—
08	—	TPDM	—	—	—	—	RTRN	RTS
07	—	—	L2ACT	—	L3ACT	L4ACT	RA	MHLD
06	—	—	—	—	—	—	—	—
05	—	—	—	TXSQ	CEQ	TTDIS	—	TSPA
04	—	—	—	—	—	—	—	—
03	—	—	—	—	ARC0	SDIS	—	—
02	—	—	—	—	SHAP0	CF330	SEPT	EPT
01	TSPY							
00	TBUFFER/TSPX							

(—) Indicates reserved for modem use only.

R144DP DSP Interface Memory (Chip 1)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA1	NCIA1	—	NSIE1	NEWS1	NCIE1	—	NEWC1
1E	—	DBIA1	—	—	—	DBIE1	—	DBA1
1D	XACC1	—	—	—	—	XCRD1	XWT1	XCR1
1C	X RAM ADDRESS (XADD1)							
1B	YACC1	—	—	—	—	YCRD1	YWT1	YCR1
1A	Y RAM ADDRESS (YADD1)							
19	X RAM DATA MSB (XDAM1)							
18	X RAM DATA LSB (XDAL1)							
17	Y RAM DATA MSB (YDAM1)							
16	Y RAM DATA LSB (YDAL1)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	—	—	—	—	RTH		—	—
12	RCONF							
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	RLSD	FED	—	—	—	—	—	—
0E	—	—	—	—	—	SPEED		
0D	P2DET	PNDET	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	RSEQ
0B	TONEA	TONEB	TONEC	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	—	—	—	DATA1	—	—
08	—	—	—	—	—	RTDIS	—	—
07	—	—	—	—	—	—	—	—
06	—	—	—	—	—	—	—	—
05	—	—	—	—	—	—	—	—
04	—	—	—	—	—	—	—	—
03	—	—	—	RLSDE	ARC1	—	—	—
02	—	SQDIS	—	—	SHAP1	CF331	—	—
01	RSEQM							
00	RBUFFER/RSEQL							

(—) Indicates reserved for modem use only.

R144DP Interface Memory (Chip 2)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA2	—	—	NSIE2	NEWS2	—	—	—
1E		DBIA2	—	—	—	DBIE2	—	DBA2
1D	XACC2	—	—	—	—	XCRD2	XWT2	XCR2
1C	X RAM ADDRESS (XADD2)							
1B	YACC2	—	—	—	—	YCRD2	YWT2	YCR2
1A	Y RAM ADDRESS (YADD2)							
19	X RAM DATA MSB (XDAM2)							
18	X RAM DATA LSB (XDAL2)							
17	Y RAM DATA MSB (YDAM2)							
16	Y RAM DATA LSB (YDAL2)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	—	—	—	—	—	—	—	—
12	—	—	—	—	—	—	—	—
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	—	—	—	—	RI	—	—	—
0E	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	—	—	—	DATA2	—	—
08	—	—	—	DDIS	—	—	—	—
07	—	—	—	—	—	—	—	—
06	—	—	—	—	—	—	—	—
05	—	—	—	—	—	—	—	—
04	EQRES	EQT2	—	RSPA	EQFZ	IFIX	TOD	—
03	—	—	—	—	—	—	—	—
02	—	—	AMTD	—	—	—	—	—
01	RSPY							
00	RSPX							

(—) Indicates reserved for modem use only.

Figure 4. R144DP DSP Interface Memory Map

Table 8. R144DP Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
AMTD	2:2:5	1	**Amplitude Modulation Tracker Disable.** When control bit AMTD is a 0, an adaptive amplitude modulation tracker is enabled in the receiver; when a 1, the tracker is disabled. The tracker operates only in V.33 configurations.
ARC0	0:3:3	1	**Automatic Rate Change Enable Chip 0.** In V.33 configurations, control bit ARC0 controls the transmit data rate. When ARC0 is a 1, the transmitter automatically conditions itself to transmit data at the highest common data rate according to the received rate sequence. When ARC0 is a 0, the host must check the rate sequence in registers RSEQM and RSEQL and set the transmitter configuration accordingly (see RSEQ). ARC0 must be 0 for the transmitter to operate in the proprietary TCM 9600 or TCM 7200 modes. The undefined bits in the rate sequence can be modified in DSP RAM.
ARC1	1:3:3	1	**Automatic Rate Change Enable Chip 1.** In V.33 configurations, control bit ARC1 controls the receive data rate. When ARC1 is a 1, the receiver automatically conditions itself to receive data at the highest common data rate according to the received rate sequence. When ARC1 is a 0, the host must check the rate sequence in registers RSEQM and RSEQL and set the receiver configuration accordingly (see RSEQ). ARC1 must be 0 for the receiver to operate in the proprietary TCM 9600 or TCM 7200 modes.
CEQ	0:5:3	1	**Compromise Equalizer Enable.** When control bit CEQ is a 1, the transmitter's digital compromise equalizer is inserted into the transmit path. This bandpass equalizer has host programmable taps in DSP RAM. CEQ should be a 0 during local analog loopback.
CF330	0:2:2	0	**Carrier Frequency V.33 Chip 0.** When control bit CF330 is a 1, the transmitter carrier frequency in V.33 configurations is 1700 Hz. When CF330 is a 0, the carrier frequency in V.33 configurations is 1800 Hz. The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band.
CF331	1:2:2	0	**Carrier Frequency V.33 Chip 1.** When control bit CF331 is a 1, the receiver carrier frequency in V.33 configurations is 1700 Hz. When CF331 is a 0, the carrier frequency in V.33 configurations is 1800 Hz. The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band.
CTS	0:F:5	—	**Clear To Send.** When set to a 1, status bit CTS indicates to the DTE that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM).
DATA1	1:9:2	1	**Data Chip 1.** When control bit DATA1 is a 0, the receiver is prevented from entering the training state. The receiver remains in idle mode. Tone detectors A, B and C are all active. When DATA1 is a 1 the receiver responds normally. Tone detectors A and B are active but tone detector C is disabled.
DATA2	2:9:2	1	**Data Chip 2.** When control bit DATA2 is a 0, the ringing detector is enabled, and when a 1, the ringing detector is disabled. This bit should be set to a 1 after the modem goes off-hook, otherwise the $\overline{RI}$ signal and RI bit will give spurious outputs.
DBA0	0:1E:0	—	**Data Buffer Available Chip 0.** When set to a 1, status bit DBA0 signifies that the transmitter has read register 0:0 (TBUFFER), or registers 0:1 (TSPY) and 0:0 (TSPX), and the host can write new data into register 0:0, or registers 0:1 and 0:0. This condition can also cause $\overline{IRQ}$ to be asserted. The host writing to register 0:0 resets the DBA0 and DBIA0 bits to 0. (See DBIE0 and DBIA0.)
DBA1	1:1E:0	—	**Data Buffer Available Chip 1.** When set to a 1, status bit DBA1 signifies that the receiver wrote valid data into register 1:0 (RBUFFER), or registers 1:1 (RSEQM) and 1:0 (RSEQL). This condition can also cause $\overline{IRQ}$ to be asserted. The host reading register 1:0 resets the DBA1 and DBIA1 bits to 0. (See DBIE1 and DBIA1.)
DBA2	2:1E:0	—	**Data Buffer Available Chip 2.** When set to a 1, status bit DBA2 signifies that the receiver wrote valid data into registers 2:1 (RSPY) and 2:0 (RSPX). This condition can also cause $\overline{IRQ}$ to be asserted. The host reading register 2:0 resets the DBA2 and DBIA2 bits to 0. (See DBIE2 and DBIA2.)
DBIA0	0:1E:6	—	**Data Buffer Interrupt Active Chip 0.** When the transmitter data buffer interrupt is enabled (DBIE0 is a 1) and register 0:0 is empty (DBA0 is set to a 1), the transmitter asserts $\overline{IRQ}$ and sets status bit DBIA0 to a 1 to indicate that DBA0 going to a 1 caused the interrupt. The host writing to register 0:0 resets the DBIA0 bit to a 0 and clears the interrupt request due to DBA0. (See DBIE0 and DBA0.)
DBIA1	1:1E:6	—	**Data Buffer Interrupt Active Chip 1.** When the receiver chip 1 data buffer interrupt is enabled (DBIE1 is a 1) and register 1:0 is written to by the DSP (DBA1 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets DBIA1 to a 1 to indicate that DBA1 going to a 1 caused the interrupt. The host reading register 1:0 resets the DBIA1 bit to a 0 and clears the interrupt request due to DBA1. (See DBA1 and DBIE1.)

Table 8. R144DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
DBIA2	2:1E:6	—	**Data Buffer Interrupt Active Chip 2.** When the receiver chip 2 data buffer interrupt is enabled (DBIE2 is a 1) and register 2:0 is written to by the DSP (DBA2 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets DBIA2 to a 1 to indicate that DBA2 going to a 1 caused the interrupt. The host reading register 2:0 resets the DBIA2 bit to a 0 and clears the interrupt request due to DBA2. (See DBA2 and DBIE2.)
DBIE0	0:1E:2	0	**Data Buffer Interrupt Enable Chip 0.** When control bit DBIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set the DBIA0 bit to a 1 when DBA0 is set to 1 by the DSP. When DBIE0 is a 0 (interrupt disabled), DBA0 has no effect on $\overline{IRQ}$ or DBIA0. (See DBA0 and DBIA0.)
DBIE1	1:1E:2	0	**Data Buffer Interrupt Enable Chip 1.** When control bit DBIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set the DBIA1 bit to a 1 when DBA1 is set to a 1 by the DSP. When DBIE1 is a 0 (interrupt disabled), DBA1 has no effect on $\overline{IRQ}$ or DBIA1. (See DBA1 and DBIA1.)
DBIE2	2:1E:2	0	**Data Buffer Interrupt Enable Chip 2.** When control bit DBIE2 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set the DBIA2 bit to a 1 when DBA2 is set to a 1 by the DSP. When DBIE2 is a 0 (interrupt disabled), DBA2 has no effect on $\overline{IRQ}$ or DBIA2. (See DBA2 and DBIA2.)
DDIS	2:8:4	0	**Descrambler Disable.** When control bit DDIS is a 1, the receiver's descrambler circuit is disabled; when a 0, the descrambler circuit is enabled.
DTMF	0:9:5	0	**DTMF Select.** When the modem is configured for dialing mode, the modem will dial using DTMF tones or pulses. When control bit DTMF is a 1, the modem will dial using DTMF tones. When DTMF is a 0, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. Dialing mode is selected by configuration code 81 in the Transmitter Configuration Register (TCONF). When in dialing mode, the data placed in the Transmitter Data Register is treated as digits to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the Transmitter Data Register). Also, see DBA0 bit. Dialing timing and power levels are host programmable in DSP RAM (Table 11).
EPT	0:2:0	0	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 185 ms (SEPT bit = 0) or 30 ms (SEPT bit = 1) followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence. The echo protector tone is typically used in V.27 and V.29 over dial-up lines. The tone is sent prior to the training sequence to ensure that the echo suppressors are pointing in the correct direction.
EQFZ	2:4:3	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.
EQRES	2:4:7	0	**Equalizer Reset.** When control bit EQRES is a 1, the receiver sets all of the adaptive equalizer's taps to zero. When EQRES is a 0, the equalizer taps are updated normally by the receiver. Setting EQRES to a 1 effectively clamps the receiver. EQRES along with RLSDE can be used to clamp the receiver off and turn off the $\overline{RLSD}$ pin. An equalizer reset is automatically done for a brief period of time at the beginning of the train-on-data state (TOD = 1). Therefore, the host does not have to manually set then clear this bit to reset the equalizer for line hits, etc., when TOD is active.
EQT2	2:4:6	0	**Equalizer T/2 Spacing Select.** When control bit EQT2 is a 1, the receiver's adaptive equalizer is T/2 fractionally spaced. When EQT2 is a 0, the equalizer is T spaced (T = 1 baud time).
FED	1:F:6	—	**Fast Energy Detector.** When status bit FED is a 1, energy in the passband above the selected receiver threshold has been detected (see RTH).
IFIX	2:4:2	1	**Eye Fix.** When control bit IFIX is a 1, the serial diagnostic data at the EYEX and EYEY pins reflects the Rotated Equalizer Output. When IFIX is a 0, the data on EYEX and EYEY is selected by the addresses in X RAM Address and Y RAM Address registers, respectively.
L2ACT	0:7:5	0	**Loop 2 Activate.** When control bit L2ACT is a 1, the receiver's digital output is connected to the transmitter's digital input (locally activated remote digital loopback) in accordance with CCITT Recommendation V.54.
L3ACT	0:7.3	0	**Loop 3 Activate.** When control bit L3ACT is a 1, the transmitter's analog output is coupled to the receiver's analog input through an attenuator (local analog loopback) in accordance with CCITT Recommendation V.54. The modem can be placed in loop 3 in either idle or data mode. If loop 3 is initiated in data mode, the connection to the other modem is terminated. The transmitter's compromise equalizer should be disabled, by setting CEQ to a 0, during local analog loopback.
L4ACT	0:7:2	0	**Loop 4 Activate.** When control bit L4ACT is a 1, the receiver's analog input is connected to the transmitter's analog output (remote analog loopback) in a manner similar to CCITT Recommendation V.54.
MHLD	0:7:0	0	**Mark Hold.** When control bit MHLD is a 1, the transmitter's digital input data is clamped to a mark. When MHLD is a 0, the transmitter's input is taken from TXD or TBUFFER (see TPDM).

Table 8. R144DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
NCIA0	0:1F:6	—	**NEWC0 Interrupt Active.** When the new configuration chip 0 interrupt is enabled (NCIE0 is a 1) and a new transmitter configuration is implemented (NEWC0 is reset to a 0), the DSP asserts $\overline{IRQ}$ and sets status bit NCIA0 to a 1 to indicate that NEWC0 going to a 0 caused the interrupt. NCIA0 and the interrupt request due to NEW0 are cleared by the host writing a 0 into NCIE0. (See NEWC0 and NCIE0.)
NCIA1	1:1F:6	—	**NEWC1 Interrupt Active.** When the new configuration chip 1 interrupt is enabled (NCIE1 is a 1) and a new receiver configuration is implemented (NEWC1 is reset to a 0), the DSP asserts $\overline{IRQ}$ and sets status bit NCIA1 to a 1 to indicate that NEWC1 going to a 0 caused the interrupt. NCIA1 and the interrupt request due to NEWC1 are cleared by the host writing a 0 into NCIE1. (See NEWC1 and NCIE1.)
NCIE0	0:1F:2	0	**NEWC0 Interrupt Enable.** When control bit NCIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set NCIA0 to a 1 when the NEWC0 bit is reset to a 0 by the DSP. When NCIE0 is a 0 (interrupt disabled), NEWC0 has no effect on $\overline{IRQ}$ or NCIA0. (See NEWC0 and NCIA0.)
NCIE1	1:1F:2	0	**NEWC1 Interrupt Enable.** When control bit NCIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA1 to a 1 when the NEWC1 bit is reset to a 0 by the DSP. When NCIE1 is a 0 (interrupt disabled), NEWC1 has no effect on $\overline{IRQ}$ or NCIA1. (See NEWC1 and NCIA1.)
NEWC0	0:1F:0	0	**New Configuration Chip 0.** Control bit NEWC0 must be set to a 1 by the host after the host changes the configuration code in TCONF (0:12) or the SHAP0 bit (0:2:3). This informs the transmitter to implement the new transmitter configuration. The DSP resets the NEWC0 bit to a 0 when the configuration change is implemented. A configuration change can also cause $\overline{IRQ}$ to be asserted. (See NCIE0 and NCIA0.)
NEWC1	1:1F:0	0	**New Configuration Chip 1.** Control bit NEWC1 must be set to a 1 by the host after the host changes the configuration code in RCONF (1:12), the SHAP1 bit (1:2:3), or RTH (1:13:2-3). This informs the receiver to implement the new receiver configuration and/or the new receiver threshold. The DSP resets the NEWC1 bit to a 0 when the change is implemented. A configuration/receiver threshold change can also cause $\overline{IRQ}$ to be asserted. (See NCIE1 and NCIA1.)
NEWS0	0:1F:3	—	**New Status Chip 0.** When set to a 1, status bit NEWS0 indicates that one or more status bits located in registers 0A to 0F have changed state, or a DSP RAM read or write has been completed, in the transmitter. This bit can be reset to a 0 only by the host. The host may mask the effect of individual status bits upon NEWS0 by writing a mask value to DSP RAM. A change of status can also cause $\overline{IRQ}$ to be asserted. (See NSIE0 and NSIA0.)
NEWS1	1:1F:3	—	**New Status Chip 1.** When set to a 1, status bit NEWS1 indicates that one or more status bits located in registers 0A to 0F have changed state, or a DSP RAM read or write has been completed, in receiver DSP chip 1. This bit can be reset to a 0 only by the host. The host may mask the effect of individual status bits upon NEWS1 by writing a mask value to DSP RAM. A change of status can also cause $\overline{IRQ}$ to be asserted. (See NSIE1 and NSIA1.)
NEWS2	2:1F:3	—	**New Status Chip 2.** When set to a 1, status bit NEWS2 indicates that a DSP RAM read or write has been completed in receiver DSP chip 2. This bit can be reset to a 0 only by the host. Completion of a RAM read or write cycle can also cause $\overline{IRQ}$ to be asserted. (See NSIE2 and NSIA2.)
NSIA0	0:1F:7	—	**NEWS0 Interrupt Active Chip 0.** When the new status interrupt chip 0 is enabled (NSIE0 is a 1) and a change of status occurs (NEWS0 is set to a 1), the transmitter asserts $\overline{IRQ}$ and sets status bit NSIA0 to a 1 to indicate that NEWS0 going to a 1 caused the interrupt. NSIA0 and the interrupt request due to NEWS0 are cleared when the host writes a 0 to NEWS0. (See NEWS0 and NSIE0.)
NSIA1	1:1F:7	—	**NEWS1 Interrupt Active Chip 1.** When the new status interrupt chip 1 is enabled (NSIE1 is a 1) and a change a status occurs (NEWS1 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets status bit NSIA1 to a 1 to indicate that NEWS1 going to a 1 caused the interrupt. NSIA1 and the interrupt request due to NEWS1 are cleared when the host writes a 0 to NEWS1. (See NEWS1 and NSIE1.)
NSIA2	2:1F:7	—	**NEWS2 Interrupt Active Chip 2.** When the new status interrupt chip 2 is enabled (NSIE2 is a 1) and a change of status occurs (NEWS2 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets status bit NSIA2 to a 1 to indicate that NEWS2 going to a 1 caused the interrupt. NSIA2 and the interrupt request due to NEWS2 are cleared when the host writes a 0 to NEWS2. (See NEWS2 and NSIE2.)
NSIE0	0:1F:4	0	**NEWS0 Interrupt Enable Chip 0.** When control bit NSIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set NSIA0 to a 1 when NEWS0 is set to a 1 by the DSP. When NSIE0 is a 0 (interrupt disabled), NEWS0 has no effect on $\overline{IRQ}$ or NSIA0. (See NEWS0 and NSIA0.)
NSIE1	1:1F:4	0	**NEWS1 Interrupt Enable Chip 1.** When control bit NSIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA1 to a 1 when NEWS1 is set to a 1 by the DSP. When NSIE1 is a 0 (interrupt disabled), NEWS1 has no effect on $\overline{IRQ}$ or NSIA1. (See NEWS1 and NSIA1.)

Table 8. R144DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
NSIE2	2:1F:4	0	**NEWS2 Interrupt Enable Chip 2.** When control bit NSIE2 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA2 to a 1 when NEWS2 is set to a 1 by the DSP. When NSIE2 is a 0 (interrupt disabled), NEWS2 has no effect on $\overline{IRQ}$ or NSIA2. (See NEWS2 and NSIA2.)
P2DET	1:D:7	—	**P2 Sequence Detected.** When status bit P2DET is a 1, the receiver is detecting the P2 portion of the training sequence. When P2DET is a 0, P2 is not being detected.
PNDET	1:D:6	—	**PN Sequence Detected.** When status bit PNDET is a 1, the receiver is detecting the PN portion of the training sequence. When PNDET is a 0, PN is not being detected.
RA	0:7:1	0	**Relay Activate.** When control bit RA is a 1, the output $\overline{OHRC}$ is activated (low); when a 0, the $\overline{OHRC}$ output is off (high).
RBUFFER	1:0:0–7	—	**Receive Buffer.** The host obtains channel data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER. The data is divided on the baud boundaries shown under TBUFFER. The RBUFFER reflects the received data when the RATE bit is a 0.
RCONF	1:12:0–7	31	**Receiver Configuration.** The RCONF control bits select one of the following receiver configurations:
RI	2:F:3	—	**Ring Indicator.** When set to a 1, status bit RI indicates that a ringing signal is being detected. Ringing is detected if pulses are present on the $\overline{RD}$ input in the 15 Hz–68 Hz frequency range. The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with $\overline{RI}$ output signal. The decision bounds are host programmable in DSP RAM. The bit is valid only when the receiver DATA2 bit (2:9:2) is an 0.
RLSD	1:F:7	—	**Received Line Signal Detector.** When status bit RLSD is a 1, the receiver has finished receiving the training sequence or has turned on due to detected energy above threshold, and is receiving data. RLSD is a 0 when the receiver is in the idle state and during the reception of a training sequence.
RLSDE	1:3:4	1	**RLSD Enable.** When control bit RLSDE is a 1, the $\overline{RLSD}$ pin reflects the RLSD bit. When RLSDE is a 0, the $\overline{RLSD}$ pin is clamped to a 1 (OFF condition) regardless of the state of the RLSD bit.
RSEQ	1:C:0	0	**Rate Sequence Received.** When status bit RSEQ is a 1, the 16-bit rate sequence included in the CCITT V.33 start-up procedure has been received and the 16-bit rate sequence word is available in RSEQM (1:1) and RSEQL (1:0). (V.33)
RSEQL	1:0:0–7	—	**Rate Sequence LSB.** When the RSEQ bit is a 1, register 1:0 holds the least significant byte of the 16-bit V.33 rate sequence word (RSEQL) received by the modem. When the RSEQ bit is a 0, register 1:0 holds the received data (see RBUFFER). (V.33)
RSEQM	1:1:0–7	—	**Rate Sequence MSB.** When the RSEQ bit is a 1, register 1:1 holds the most significant byte of the 16-bit V.33 rate sequence word (RSEQM) received by the modem. When the RSEQ bit is a 0, register 1:1 is not used. (V.33)
RSPA	2:4:4	1	**Receiver Signal Point Activate.** When control bit RSPA is a 1, the receiver writes the received signal point coordinates, after the decision processing, into registers RSPY (2:1) and RSPX (2:0). When RSPA is a 0, RSPY and RSPX do not contain the signal point coordinates.
RSPX	2:0:0–7	—	**Receiver Signal Point X.** RSPX holds the X (in-phase) coordinate of the received signal point. RSPX is valid only when RSPA is a 1.
RSPY	2:1:0–7	—	**Receiver Signal Point Y.** RSPY holds the Y (quadrature) coordinate of the received signal point. RSPY is valid only when RSPA is a 1.

Mode	Data Rate	RCONF (Hex)
V.33 TCM	14400	31
V.33 TCM	12000	32
TCM	9600	34
TCM	7200	38
V.29	9600	14
V.29	7200	12
V.29	4800	11
V.27	4800 Long	22
V.27	2400 Long	21
V.27	4800 Short	02
V.27	2400 Short	01

Table 8. R144DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
RTDIS	1:8:2	0	**Receiver Training Disable.** When control bit RTDIS is a 1, the receiver is prevented from recognizing a training sequence and entering the training state. When RTDIS is a 0, receiver training is enabled.
RTH	1·13·2,3	0	**Receiver Threshold.** The RTH control bits select the receiver energy detector threshold according to the following codes: RTH / RLSD ON / RLSD OFF 0 / –43 dBm / –48 dBm 1 / –33 dBm / –38 dBm 2 / –26 dBm / –31 dBm 3 / –16 dBm / –21 dBm
RTRN	0:8:1	0	**Retrain.** When the modem is in data mode, and control bit RTRN is set to a 1, a retrain sequence is initiated. RTRN resets to a 0 as soon as the initiation is acknowledged. Fall-back or fall-forward retrains may be accomplished in V.33 mode as follows: Change the Transmitter Configuration Register (TCONF) to the required configuration code. **Do not** set the NEWC bits in either the transmitter (NEWC0) or receiver chip 1 (NEWC1) and do not change the receiver configuration register (RCONF) code. Ensure that ARC0 and ARC1 bits are set to a 1. Finally, set the RTRN bit to a 1. If the remote modem can operate at the requested rate, the receiver configuration will be changed by the modem to reflect the new rate **after the retrain is completed.** If the remote modem cannot operate at the new rate, then no rate change will take place during the retrain and the transmitter configuration register will automatically revert back to its original configuration.
RTS	0:8:0	0	**Request To Send.** When control bit RTS is a 1, the modem transmits the training sequence before activating CTS. The RTS bit is ORed with the $\overline{RTS}$ pin.
SDIS	0:3:2	0	**Scrambler Disable.** When control bit SDIS is a 1, the transmitter scrambler circuit is disabled; when a 0, the scrambler circuit is enabled
SEPT	0:2:1	0	**Short Echo Protector Tone.** When control bit SEPT is a 1, the echo protector tone duration is 30 ms; when a 0, the echo protector tone duration is 185 ms.
SHAP0	0:2:3	0	**Transmitter Shaping Filter Select.** When control bit SHAP0 is a 0, the transmit spectrum is shaped by a square root of 12.5% raised cosine filter; when a 1, the transmit spectrum is shaped by a square root of 20% raised cosine filter. NEWC0 must be set after changing the SHAP0 bit. (V.33) The 20% option is provided for use in the V.29 configurations when communicating with other modems which use the 20% filter. The 12.5% option is for communicating over a channel which has a known narrow bandwidth. This option should be used when a secondary channel is added to the modem.
SHAP1	1:2:3	0	**Receiver Shaping Filter Select.** When control bit SHAP1 is a 0, the receiver low pass filter is square root of 12.5% raised cosine; when a 1, the low pass filter is square root of 20% raised cosine. NEWC1 must be set after changing the SHAP1 bit. (V.33) The 20% option is provided for use in the V.29 configurations when communicating with other modems which use the 20% filter. The 12.5% option is for communicating over a channel which has a known narrow bandwidth. This option should be used when a secondary channel is added to the modem.
SPEED	1:E:0–2	—	**Speed Indication.** The SPEED status bits indicate the receiver's data rate at the completion of the training sequence for V.33 configurations. SPEED / Data Rate 7 / V.33 14400 6 / V.33 12000 5 / V.33 9600
SQDIS	1 2:6	0	**Squarer Disable (Tone Detector C).** When control bit SQDIS is a 1, the squarer in front of tone detector C is disabled; when a 0, the squarer is enabled.

Table 8. R144DP Interface Memory Bit Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Memory Location</th><th>Default Value</th><th>Name/Description</th></tr>
<tr><td>TBUFFER</td><td>0:0:0–7</td><td>—</td><td>Transmitter Buffer/Transmitter Signal Point X. The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER.
The data is transmitted bit 0 first and is divided on the following baud boundaries:
<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.33 14400</td><td colspan="2">—</td><td colspan="6">Baud 0</td></tr>
<tr><td>V.33 12000</td><td colspan="2">—</td><td colspan="1">—</td><td colspan="5">Baud 0</td></tr>
<tr><td>TCM 9600</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>TCM 7200</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.29 9600</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.29 7200</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.29 4800</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 4800</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 2400</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table></td></tr>
<tr><td>TCONF</td><td>0:12:0–7</td><td>31</td><td>Transmitter Configuration. The TCONF control bits select one of the following transmitter configurations:
<table>
<tr><th>Mode</th><th>Data Rate</th><th>TCONF (Hex)</th></tr>
<tr><td>V.33 TCM</td><td>14400</td><td>31</td></tr>
<tr><td>V.33 TCM</td><td>12000</td><td>32</td></tr>
<tr><td>TCM</td><td>9600</td><td>34</td></tr>
<tr><td>TCM</td><td>7200</td><td>38</td></tr>
<tr><td>V.29</td><td>9600</td><td>14</td></tr>
<tr><td>V.29</td><td>7200</td><td>12</td></tr>
<tr><td>V.29</td><td>4800</td><td>11</td></tr>
<tr><td>V.27</td><td>4800 Long</td><td>22</td></tr>
<tr><td>V.27</td><td>2400 Long</td><td>21</td></tr>
<tr><td>V.27</td><td>4800 Short</td><td>02</td></tr>
<tr><td>V.27</td><td>2400 Short</td><td>01</td></tr>
<tr><td>Single Tone</td><td>—</td><td>80</td></tr>
<tr><td>Dual Tone</td><td>—</td><td>83</td></tr>
<tr><td>Dialing</td><td>—</td><td>81</td></tr>
<tr><td colspan="3">When a single tone or dual tone mode is selected, the modem transmits one or two tones respectively. The tone frequencies are host programmable in DSP RAM. Single tone transmit uses the Dual Tone 1 frequency and level.</td></tr>
</table></td></tr>
<tr><td>TLVL</td><td>0:13:4–7</td><td>0</td><td>Transmit Level. The TLVL code selects the transmitter analog output level at the TXA pin as follows:
<table>
<tr><th>TLVL Code (Hex)</th><th>TX Output Level (dBm ±0.5 dB)</th></tr>
<tr><td>0</td><td>–0.5</td></tr>
<tr><td>1</td><td>–1.5</td></tr>
<tr><td>2</td><td>–2.5</td></tr>
<tr><td>3</td><td>–3.5</td></tr>
<tr><td>4</td><td>–4.5</td></tr>
<tr><td>5</td><td>–5.5</td></tr>
<tr><td>6</td><td>–6.5</td></tr>
<tr><td>7</td><td>–7.5</td></tr>
<tr><td>8</td><td>–8.5</td></tr>
<tr><td>9</td><td>–9.5</td></tr>
<tr><td>A</td><td>–10.5</td></tr>
<tr><td>B</td><td>–11.5</td></tr>
<tr><td>C</td><td>–12.5</td></tr>
<tr><td>D</td><td>–13.5</td></tr>
<tr><td>E</td><td>–14.5</td></tr>
<tr><td>F</td><td>–15.5</td></tr>
</table>
The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.</td></tr>
</table>

Table 8. R144DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
TOD	2:4:1	0	**Train On Data.** When set to a 1, control bit TOD enables the train-on-data algorithm to converge the equalizer if the signal quality degrades A BER of 10^{-3} for 0.5 seconds initiates the train-on-data. The receiver can typically train-on-data in less than 15 seconds for V.33 or V.29 and less than 3.5 seconds for V.27. When TOD is a 1, the modem is still able to recognize an incoming training sequence.
TONEA	1:B:7	—	**Tone A Detected.** When set to a 1, status bit TONEA indicates that energy is present on the line within the tone detector A passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	1·B:6	—	**Tone B Detected.** When set to a 1, status bit TONEB indicates that energy is present on the line within the tone detector B passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	1:B:5	—	**Tone C Detected.** When set to a 1, status bit TONEC indicates that energy is present on the line within the tone detector C passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM. The TONEC filter is preceded by a squarer in order to facilitate detection of difference tones. The squarer may be disabled with the SQDIS bit (see SQDIS bit).
TPDM	0.8.6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is a 1, the transmitter accepts data for transmission from the TBUFFER (0:0) rather than the TXD input.
TSPA	0:5:0	0	**Transmitter Signal Point Activate.** When control bit TSPA is a 1, the transmitter uses the signal points X and Y directly from registers TSPX (0.0) and TSPY (0:1). The transmitter data input, TBUFFER and TXD, are ignored. When TSPA is a 0, the transmitter accepts data for transmission from the TBUFFER or the TXD input.
TSPX	0:0·0–7	00	**Transmitter Signal Point X.** When TSPA is a 1, register 0:0 is used to transmit the in-phase (X) coordinate of the transmitted signal point (TSPX).
TSPY	0·1·0–7	00	**Transmitter Signal Point Y.** When TSPA is a 1, register 0:1 is used to transmit the quadrature (Y) coordinate of the transmitted signal point (TSPY).
TTDIS	0·5.2	0	**Transmitter Training Disable.** When control bit TTDIS is a 1, the transmitter does not generate the training sequence at the start of transmission. With training disabled, the RTS/CTS delay is less than two baud times
TXCLK	0.13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock. **TXCLK** — **Transmit Clock** 0 — Internal 2 — External (XTCLK) 3 — Slave ($\overline{\text{RDCLK}}$) When the external clock is chosen, the host supplied clock must be connected to the XTCLK input pin. The external clock will then be reflected at the TDCLK output pin. When the slave clock is chosen, the transmitter clock (TDCLK) is phase locked to the receiver clock ($\overline{\text{RDCLK}}$).
TXSQ	0:5:4	0	**Transmitter Squelch.** When control bit TXSQ is a 1, the transmitter analog output is squelched. All other transmitter functions continue as normal. When TXSQ is a 0, the transmitter output functions normally. This bit is useful in 2-wire configurations where it is necessary to measure the spectrum and transmit level of a transmitter Setting the TXSQ bit to a 1 turns off the transmitter so that only one of the two carriers is present. After TXSQ is set to a 0, a retrain should be sent to reestablish the data transfer.
XACC0	0:1D:7	0	**X RAM Access Enable Chip 0.** When control bit XACC0 is a 1, DSP chip 0 accesses the X RAM associated with the address in XADD0 and the XCR0 bit. XWT0 determines if a read or write is performed The DSP resets XACC0 to a 0 upon RAM access completion.
XACC1	1.1D:7	0	**X RAM Access Enable Chip 1.** When control bit XACC1 is a 1, DSP chip 1 accesses the X RAM associated with the address in XADD1 and the XCR1 bit. XWT1 determines if a read or write is performed The DSP resets XACC1 to a 0 upon RAM access completion.
XACC2	2:1D·7	0	**X RAM Access Enable Chip 2.** When control bit XACC2 is a 1, DSP Chip 2 accesses the X RAM associated with the address in XADD2 and the XCR2 bit. XWT2 determines if a read or write is performed. The DSP resets XACC2 to a 0 upon RAM access completion.
XADD0	0·1C·0–7	00	**X RAM Address Chip 0.** XADD0 contains the X RAM address used to access DSP chip 0's X Data RAM (XCR0 = 0) or X Coefficient RAM (XCR0 = 1) via the X RAM Data LSB and MSB registers (0·18 and 0·19, respectively) (See Table 9.)

Table 8. R144DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
XADD1	1:1C:0-7	00	**X RAM Address Chip 1.** XADD1 contains the X RAM address used to access DSP chip 1's X Data RAM (XCR1 = 0) or X Coefficient RAM (XCR1 = 1) via the X RAM Data LSB and MSB registers (1:18 and 1:19, respectively) (See Table 9.)
XADD2	2:1C:0-7	00	**X RAM Address Chip 2.** XADD2 contains the X RAM address used to access DSP chip 2's X Data RAM (XCR2 = 0) or X Coefficient RAM (XCR2 = 1) via the X RAM Data LSB and MSB registers (2:18 and 2:19, respectively). (See Table 9.)
XCRD0	0:1D:2	0	**X RAM Continuous Read Chip 0.** When control bit XCRD0 is a 1, bits XACC0 and XWT0 are overridden and an X RAM read from chip 0 is performed every sample from the location addressed by XADD0 (see DSP RAM Access)
XCRD1	1:1D:2	0	**X RAM Continuous Read Chip 1.** When control bit XCRD1 is a 1, bits XACC1 and XWT1 are overridden and an X RAM read from chip 1 is performed every sample from the location addressed by XADD1 (see DSP RAM Access).
XCRD2	2:1D:2	0	**X RAM Continuous Read Chip 2.** When control bit XCRD2 is a 1, bits XACC2 and XWT2 are overridden and an X RAM read from chip 2 is performed every baud from the location addressed by XADD2 (see DSP RAM Access)
XCR0	0:1D:0	0	**X Coefficient RAM Select Chip 0.** When control bit XCR0 is a 1, XADD0 applies to DSP chip 0's X Coefficient RAM. When XCR0 is a 0, XADD0 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 10).
XCR1	1:1D:0	0	**X Coefficient RAM Select Chip 1.** When control bit XCR1 is a 1, XADD1 applies to DSP chip 1's X Coefficient RAM. When XCR1 is a 0, XADD1 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 10).
XCR2	2:1D:0	0	**X Coefficient RAM Select Chip 2.** When control bit XCR2 is a 1, XADD2 applies to DSP chip 2's X Coefficient RAM. When XCR2 is a 0, XADD2 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 10).
XDAL0	0:18:0-7	00	**X RAM Data LSB Chip 0.** XDAL0 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAL1	1:18:0-7	00	**X RAM Data LSB Chip 1.** XDAL1 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAL2	2:18:0-7	00	**X RAM Data LSB Chip 2.** XDAL2 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2
XDAM0	0:19:0-7	00	**X RAM Data MSB Chip 0.** XDAM0 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAM1	1:19:0-7	00	**X RAM Data MSB Chip 1.** XDAM1 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAM2	2:19:0-7	00	**X RAM Data MSB Chip 2.** XDAM2 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2.
XWT0	0:1D:1	0	**X RAM Write Chip 0.** When XWT0 is a 1 and XACC0 is set to a 1, DSP chip 0 copies data from the X RAM Data registers (0:18 and 0:19) into the X RAM location addressed by XADD0 and XCR0. When control bit XWT0 is a 0 and XACC0 is set to a 1, DSP chip 0 reads X RAM at the location addressed by XADD0 and XCR0. The read data is stored into the X RAM Data registers (0:18 and 0:19).
XWT1	1:1D:1	0	**X RAM Write Chip 1.** When XWT1 is a 1 and XACC1 is set to a 1, DSP chip 1 copies data from the X RAM Data registers (1:18 and 1:19) into the X RAM location addressed by XADD1 and XCR1. When control bit XWT1 is a 0 and XACC1 is set to a 1, DSP chip 1 reads X RAM at the location addressed by XADD1 and XCR1. The read data is stored into the X RAM Data registers (1:18 and 1:19).
XWT2	2:1D:1	0	**X RAM Write Chip 2.**When XWT2 is a 1 and XACC2 is set to a 1, DSP chip 2 copies data from the X RAM Data registers (2:18 and 2:19) into the X RAM location addressed by XADD2 and XCR2. When control bit XWT2 is a 0 and XACC2 is set to a 1, the DSP chip 2 reads X RAM at the location addressed by XADD2 and XCR2. The read data is stored in the X RAM Data registers (2:18 and 2.19).
YACC0	0:1B:7	0	**Y RAM Access Enable Chip 0.** When control bit YACC0 is a 1, DSP chip 0 accesses the Y RAM associated with the address in YADD0 and the YCR0 bit. YWT0 determines if a read or write is performed. The DSP resets YACC0 to a 0 upon RAM access completion.
YACC1	1:1B:7	0	**Y RAM Access Enable Chip 1.** When control bit YACC1 is a 1, DSP chip 1 accesses the Y RAM associated with the address in YADD1 and the YCR1 bit YWT1 determines if a read or write is performed. The DSP resets YACC1 to a 0 upon RAM access completion.

Table 8. R144DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
YACC2	2:1B:7	0	**Y RAM Access Enable Chip 2.** When control bit YACC2 is a 1, DSP chip 2 accesses the Y RAM associated with the address in YADD2 and the YCR2 bit YWT2 determines if a read or write is performed. The DSP sets YACC2 to a 0 upon RAM access completion
YADD0	0 1A:0-7	00	**Y RAM Address Chip 0.** YADD0 contains the Y RAM address used to access DSP chip 0's Y Data RAM (YCR0 = 0) or Y Coefficient RAM (YCR0 = 1) via the Y RAM Data LSB and MSB registers (0.16 and 0 17, respectively). (See Table 9.)
YADD1	1:1A:0-7	00	**Y RAM Address Chip 1.** YADD1 contains the Y RAM address used to access DSP chip 1's Y Data RAM (YCR1 = 0) or Y Coefficient RAM (YCR1 = 1) via the Y RAM Data LSB and MSB registers (1:16 and 1:17, respectively). (See Table 9.)
YADD2	2:1A:0-7	00	**Y RAM Address Chip 2.** YADD2 contains the Y RAM address used to access DSP chip 2's Y Data RAM (YCR2 = 0) or Y Coefficient RAM (YCR2 = 1) via the Y RAM Data LSB and MSB registers (2:16 and 2:17, respectively). (See Table 9.)
YCRD0	0:1B:2	0	**Y RAM Continuous Read Chip 0.** When control bit YCRD0 is a 1, bits YACC0 and YWT0 are overridden and a Y RAM read from chip 0 is performed every sample from the location addressed by YADD0 (see DSP RAM Access)
YCRD1	1:1B:2	0	**Y RAM Continuous Read Chip 1.** When control bit YCRD1 is a 1, bits YACC1 and YWT1 are overridden and a Y RAM read from chip 1 is performed every sample from the location addressed by YADD1 (see DSP RAM Access)
YCRD2	2:1B:2	0	**Y RAM Continuous Read Chip 2.** When control bit YCRD2 is a 1, bits YACC2 and YWT2 are overridden and a Y RAM read from chip 2 is performed every baud from the location addressed by YADD2 (see DSP RAM Access).
YCR0	0:1B:0	0	**Y Coefficient RAM Select Chip 0.** When control bit YCR0 is a 1, YADD0 applies to DSP chip 0's Y Coefficient RAM. When YCR0 is a 0, YADD0 applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 9)
YCR1	1:1B:0	0	**Y Coefficient RAM Select Chip 1.** When control bit YCR1 is a 1, YADD1 applies to DSP chip 1's Y Coefficient RAM. When YCR1 is a 0, YADD1 applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 9).
YCR2	2:1B:0	0	**Y Coefficient RAM Select Chip 2.** When control bit YCR2 is a 1, YADD2 applies to the DSP chip 2's Y Coefficient RAM. When YCR2 is a 0, YADD2 applies to the Y Data RAM This bit must be set according to the desired RAM address (Table 9).
YDAL0	0.16:0-7	00	**Y RAM Data LSB Chip 0.** YDAL0 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAL1	1:16:0-7	00	**Y RAM Data LSB Chip 1.** YDAL1 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAL2	2:16:0-7	00	**Y RAM Data LSB Chip 2.** YDAL2 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM location in DSP chip 2.
YDAM0	0:17:0-7	00	**Y RAM Data MSB Chip 0.** YDAM0 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAM1	1:17:0-7	00	**Y RAM Data MSB Chip 1.** YDAM1 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAM2	2:17:0-7	00	**Y RAM Data MSB Chip 2.** YDAM2 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 2.
YWT0	0:1B:1	0	**Y RAM Write Chip 0.** When YWT0 is a 1 and YACC0 is set to a 1, DSP chip 0 copies data from the Y RAM Data registers (0·16 and 0:17) into the Y RAM location addressed by YADD0 and YCR0. When control bit YWT0 is a 0 and YACC0 is set to a 1, DSP chip 0 reads Y RAM at the location addressed by YADD0 and YCR0. The read data is stored into the Y RAM Data registers (0:16 and 0:17).
YWT1	1:1B:1	0	**Y RAM Write Chip 1.** When YWT1 is a 1 and YACC1 is set to a 1, DSP chip 1 copies data from the Y RAM Data registers (1:16 and 1:17) into the Y RAM location addressed by YADD1 and YCR1 When control bit YWT1 is a 0 and YACC1 is set to a 1, DSP chip 1 reads Y RAM at the location addressed by YADD1 and YCR1. The read data is stored into the Y RAM Data registers (1:16 and 1:17).
YWT2	2:1B:1	0	**Y RAM Write Chip 2.** When YWT2 is a 1 and YACC2 is set to a 1, DSP chip 2 copies data from the Y RAM Data registers (2·16 and 2 17) into the Y RAM location addressed by YADD2 and YCR2 When control bit YWT2 is a 0 and YACC2 is set to a 1, DSP chip 2 reads Y RAM at the location addressed by YADD2 and YCR2 The read data is stored in the Y RAM Data registers (2:16 and 2:17)

DSP RAM ACCESS

DSP RAM Organization

Each DSP contains a 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously.

Interface Memory Access to DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in DSP interface memory RAM Access registers by the host, in conjunction with the data or coefficient RAM bit (e.g., XCR0) determines the DSP RAM address for data access.

One or two 16-bit words are transferred between DSP RAM and DSP interface memory once each device cycle. The transmitter device and the receiver sample rate device operate at the 9600 Hz sample rate. The receiver baud rate device operates at the baud rate of the selected data rate.

Two RAM access bits in each DSP interface memory tell the DSP to access the X RAM and/or Y RAM. For example, the transfer is initiated in the transmitter by the host setting the XACC0 and/or the YACC0 bit(s). The transmitter tests these bits each sample period. The receiver tests XACC1 and YACC1 each sample period and XACC2 and YACC2 each baud period.

The following procedure applies to DSP RAM access in the transmitter device. The procedure to access DSP RAM in the receiver devices is the same with the exception of the RAM access bit names.

DSP RAM Read Procedure (Transmitter)

Before reading from DSP interface memory, set XACC0 and YACC0 to a 0. Set XWT0 and/or YWT0 to a 0 to inform the DSP that a RAM read will occur when XACC0 and/or YACC0 is set to a 1. Load the RAM Address code into X RAM Address and/or Y RAM address register; then set XCR0 and/or YCR0 appropriately. Set XACC0 and/or YACC0 to a 1 to signal the DSP to perform the RAM read. When the DSP has transferred the contents of RAM into the interface memory RAM Data registers, the DSP sets the XACC0 and/or the YACC0 bit to a 0 and the NEWS0 bit to a 1 to indicate DSP RAM read completion.

If the NSIE0 bit is a 1, $\overline{IRQ}$ is also asserted when NEWS0 is set to a 1. When $\overline{IRQ}$ is asserted, NSIA0 goes to a 1 to inform the host that setting of the NEWS0 bit was the source of the interrupt. NSIA0 is cleared by writing a 0 into the NEWS0 bit, which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

DSP RAM Write Procedure (Transmitter)

Before writing to DSP interface memory, set XACC0 and YACC0 to a 0. Set XWT0 and/or YWT0 to a 1 to inform the DSP that a RAM write will occur when XACC0 and/or YACC0 is set to a 1. Load the RAM address into X RAM Address and/or Y RAM Address registers; then set XCR0 and/or YCR0 appropriately. Write the desired data into the interface memory RAM Data registers then set XACC0 and/or YACC0 to a 1 to signal the DSP to perform the RAM write. When the DSP has transferred the contents of the interface memory RAM Data registers into RAM, the DSP sets the XACC0 and/or the YACC0 bit to a 0 and the NEWS0 bit to a 1 to indicate DSP RAM write completion.

If the NSIE0 bit is a 1, $\overline{IRQ}$ is also asserted and NSIA0 is set to a 1 when NEWS0 is set to a 1. NSIA0 is cleared by writing a 0 into the NEWS0 bit, which also causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

CONTINUOUS RAM READ PROCEDURE

There are several diagnostic parameters that the host may wish to read every sample or every baud period. One example of this is the EQM (Eye Quality Monitor) value in chip 2 (receiver baud). The host may avoid having to set the XACC2/YACC2 bit every baud period by using the continuous read feature. Setting XCRD2 to a 1 overrides both XACC2 and XWT2 bits, while setting YCRD2 to a 1 overrides both YACC2 and YWT2 bits.

The RAM address registers 1A and 1C and the XCR2 and YCR2 bits must be set up as described in the general DSP RAM read procedure. Then set XCRD2 and YCRD2 to 1. The chip 2 DSP will then transfer data to the interface memory every baud. The NEWS2 bit is set as described in the general DSP RAM read procedure.

The transmitter (chip 0) and receiver (chip 1) can be similarly treated, however, data will be transferred every sample by each device.

Table 9 provides the RAM functions, address codes, and registers.

SOFTWARE INTERFACE CONSIDERATIONS

INTERRUPT REQUEST HANDLING

DSP interface memory registers registers 00, 1E and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER)/Rate Sequence Code LSB (RSEQL) in the receiver sample rate device and the Transmit Buffer (TBUFFER)/Transmit Signal Point X (TSPX) in the transmitter device. Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits. When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using $\overline{IRQ}$) or by being interrupted by $\overline{IRQ}$. When an interrupt enable bit is a 1, $\overline{IRQ}$ is asserted and the appropriate interrupt active bit set to a 1 when the corresponding interrupt condition occurs.

The basic sources for IRQ generation are status change detected, configuration change implemented, receive buffer full and transmit buffer empty. Each source is individually maskable. Table 10 identifies the interrupt sources and describes the interrupt clearing procedures.

Table 9. R144DP RAM Addresses

No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imaginary Part (Y)	CR Bit[1]	No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imaginary Part (Y)	CR Bit[1]
1	Transmitter Compromise Equalizer Coefficients:					21	Receiver Sample New Status Bit (NEWS1)				
	First Tap	0	5B	—	1		Masking Register for 1:A and 1:B	1	9B	—	1
	Last Tap	0	34	—	1		Masking Register for 1:C and 1:D	1	9C	—	1
2	V.33 Rate Sequence	0	93	—	1		Masking Register for 1:E and 1:F	1	9D	—	1
3	DTMF Tone Duration	0	9A	—	1	22	Received Signal Samples	1	03	—	0
4	DTMF Interdigit Delay	0	1A	—	1	23	Demodulator Output	1	04	84	0
5	DTMF Low Band Power Level	0	19	—	1	24	Low Pass Filter Output	1	00	80	0
6	DTMF High Band Power Level	0	99	—	1	25	Average Energy	1	02	—	0
7	Pulse Relay Make Time	0	9C	—	1	26	AGC Gain Word	1	01	—	1
8	Pulse Relay Break Time	0	1C	—	1	27	Timing Recovery Update	1	25	—	0
9	Pulse Interdigit Delay	0	1B	—	1	28	Equalizer Input	2	18	98	0
10	Transmitter Output Level Gain Constant	0	99	—	0	29	Equalizer Tap Coefficients:				
11	Dual Tone 1 Frequency	0	87	—	0		First Tap	2	18	98	1
12	Dual Tone 2 Frequency	0	90	—	1		Last Tap	2	47	C7	1
13	Dual Tone 1 Power Level	0	02	—	0	30	Unrotated Equalizer Output	2	01	81	0
14	Dual Tone 2 Power Level	0	82	—	0	31	Rotated Equalizer Output (Received Points)	2	02	82	1
15	Transmitter New Status Bit (NEWS0) Masking Register for 0:E and 0:F	0	11	—	1	32	Decision Points (Ideal Points)	2	02	82	0
16	Tone Detector A Bandpass Filter Coefficients	1	26	—	1	33	Equalizer Error	2	03	83	0
						34	Equalizer Rotation Angle	2	87	—	1
17	Tone Detector B Bandpass Filter Coefficients	1	2C	—	1	35	Equalizer Frequency Correction	2	0A	—	1
						36	Eye Quality Monitor (EQM)	2	07	—	1
18	Tone Detector C Bandpass Filter Coefficients	1	32	—	1	37	Maximum Period of Valid Ring Signal	2	17	—	0
						38	Minimum Period of Valid Ring Signal	2	97	—	0
19	RLSD On-to-Off Threshold	1	07	—	1	39	Receiver Chip 2 New Status Bit (NEWS2) Masking Register for 2:E and 2:F	2	7E	—	0
20	RLSD Off-to-On Threshold	1	01	—	0						

Note: 1. CR corresponds to XCR0, YCR0, XCR1, YCR1, XCR2, or YCR2 depending on the chip number and address code.

Table 10. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
Transmitter (DSP Chip 0)				
NSIA0	NSIE0	NEWS0	New status detected (NEWS0 transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A through 0F	Host writes a 0 into NEWS0 (Clears NSIA0 to a 0)
NCIA0	NCIE0	NEWC0	New transmitter configuration implemented by DSP (NEWC0 transitioned from a 1 to a 0)	Host writes a 0 into NCIE0 (Clears NCIA0 to a 0)
DBIA0	DBIE0	DBA0	Transmitter Data Buffer is empty and can be written (DBA0 transitioned from a 0 to a 1)	Host writes to register 0:0 (TBUFFER/TSPX) (Clears DBA0 and DBIA0 to 0)
Receiver (DSP Chip 1)				
NSIA1	NSIE1	NEWS1	New status detected (NEWS1 transitioned from a 0 to a 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A through 0F	Host writes a 0 into NEWS1 (Clears NSIA1 to a 0)
NCIA1	NCIE1	NEWC1	New receiver configuration or receiver threshold implemented by DSP (NEWC1 transitioned from a 1 to a 0)	Host writes a 0 into NCIE1 (Clears NCIA1 to a 0)
DBIA1	DBIE1	DBA1	Receiver Chip 1 Data Buffer is full and can be read (DBA1 transitioned from a 0 to a 1)	Host reads register 1:0 (RBUFFER/RSEQL) (Clears DBA1 and DBIA1 to 0)
Receiver (DSP Chip 2)				
NSIA2	NSIE2	NEWS2	New status detected (NEWS2 transitioned from a 0 to a 1) a. RAM read or RAM write occurred b. Status bit changed in register 0F	Host writes a 0 into NEWS2 (Clears NSIA2 to a 0)
TBIA2	DBIE2	DBA2	Receiver Chip 2 Data Buffer is full and can be read (DBA2 transitioned from a 0 to a 1)	Host reads register 2:0 (RSPX) (Clears DBA2 and DBIA2 to 0)

AUTO DIAL PROCEDURE

The host auto dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 5). The modem timing accounts for the DTMF tone duration and amplitude, pulse make/break ratio, and interdigit delay. These dialing parameters are host programmable in DSP RAM.

The levels of the high band and low band DTMF tones may be modified by the host in DSP RAM. The level of the high band DTMF tone should be 2 dBm greater than the level of the low band DTMF tone.

The auto dialer default parameters are given in Table 11.

Table 11. Auto Dialer Default Parameters

Parameter	Default Value
DTMF Tone Duration	95 ms
DTMF Interdigit Delay	70 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	– 4 dBm
DTMF High Band Power Level	– 2 dBm
Pulse Relay Make Time	36 ms
Pulse Relay Break Time	64 ms
Pulse Interdigit Delay	750 ms

Dial Digits

Hex	Dial Digits	Tone Pairs	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	#	941	1477

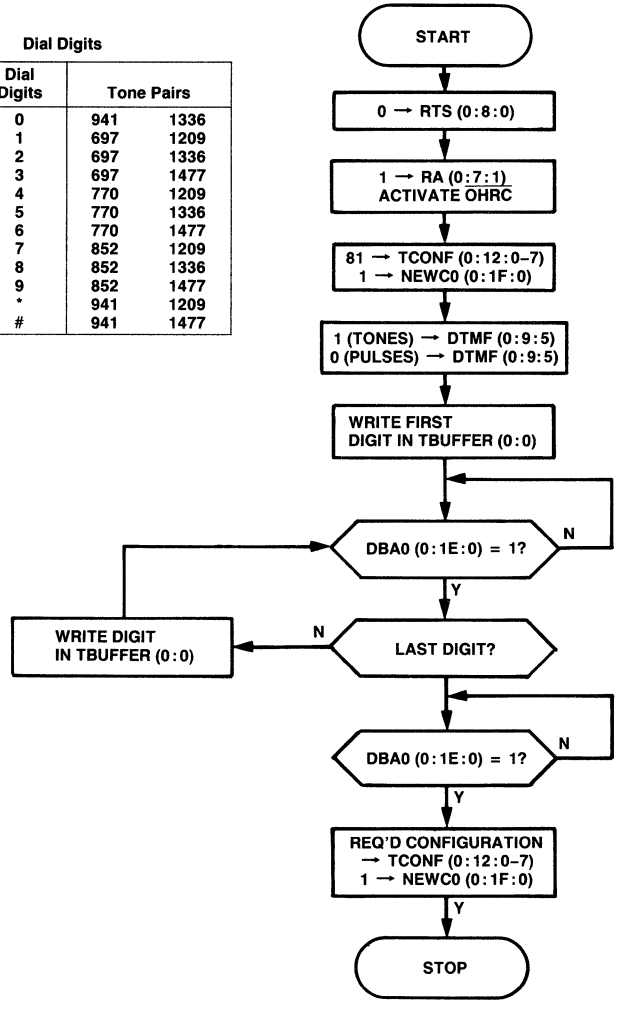


Figure 5. R144DP Auto Dial Sequence and Dial Digits

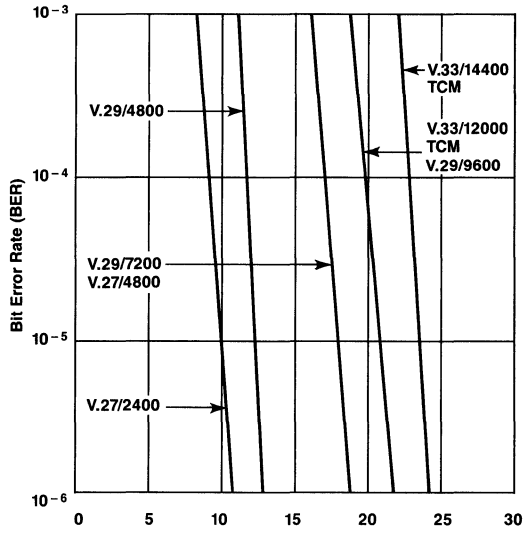
PERFORMANCE

TYPICAL BIT ERROR RATES

Typical modem bit error rate (BER) curves are shown in Figure 6 for a back-to-back connection.

TYPICAL BER TEST SETUP

The BER curves shown in Figure 6 were prepared from data obtained with a TAS 1002 test system.



a. Typical Bit Error Rate (Back-to-Back, –20 dBm Receive Level, T Equalizer, Compromise Equalizer Disabled)

Figure 6. Bit Error Rate Curves

GENERAL SPECIFICATIONS

Table 12. R144DP Modem Power Requirements

Voltage[1]	Tolerance	Current (Typical) @ 25°C	Current (Maximum) @ 0°C
+5 VDC	±5%	170 mA	325 mA
+12 VDC	±5%	3 mA	6 mA
−12 VDC	±5%	30 mA	36 mA

Note: 1. Input voltage ripple ≤0.1 volts peak-to-peak.

Table 13. R144DP Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to +70°C (32°F to 158°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 14. R144DP Modem Mechanical Dimensions

Parameter	Specification
DIN Connector Version	
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Connector Height	0.437 in. (11.1 mm)
Component Height	
Top (max.)	0.300 in. (7.62 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.):	3.6 oz (100 g)
Lead Extrusion (max.):	0.100 in. (2.54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.228 in (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0.300 in. (7.62 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.535 ±0.015 in. (13.6 ±0.4 mm), gold plated. 0.433 ±0.015 in (11.0 ±0.4 mm), gold plated. 0.315 ±0.015 in (8.0 ±0.4 mm), gold plated.

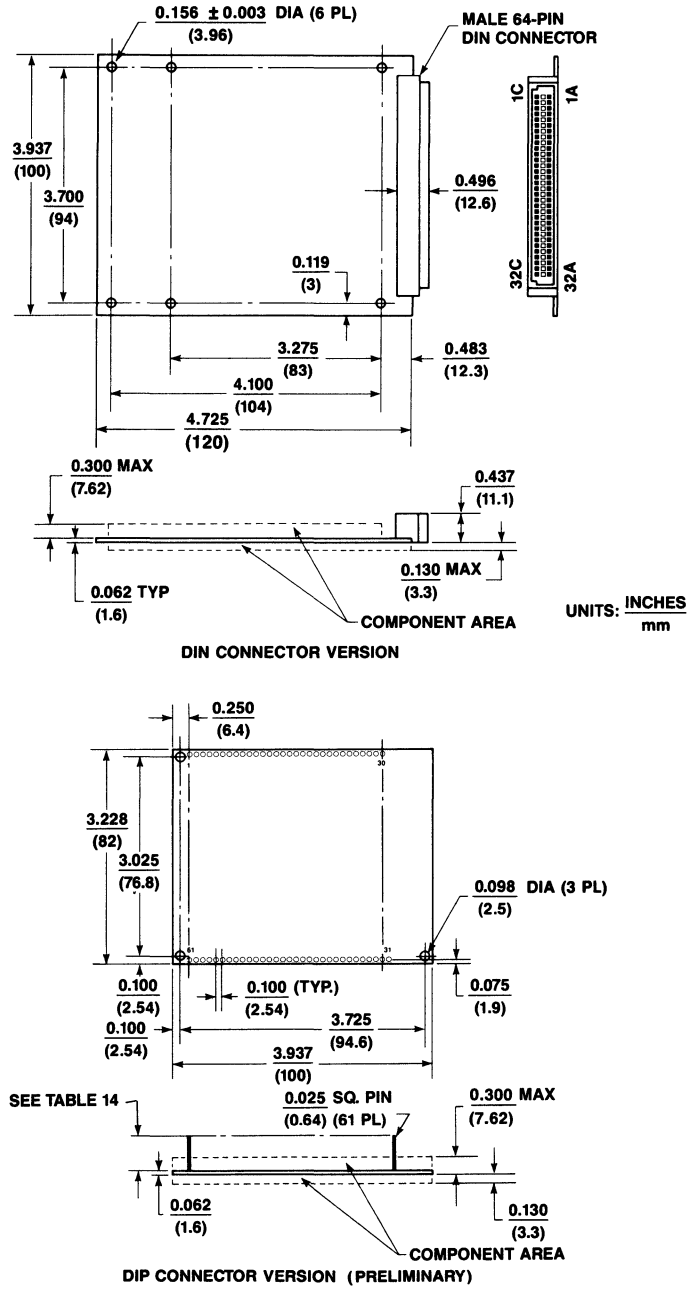


Figure 7. R144DP Modem Dimensions and Pin Locations

ELECTROMECHANICAL DESIGN CONSIDERATIONS

The area outlined by the analog ground plane in Figure 8 contains components which are sensitive to electromagnetic interference (EMI). When designing the host system, do not position radiating circuitry in the vicinity of this sensitive area. A ground plane adjacent to the modem analog circuitry is recommended.

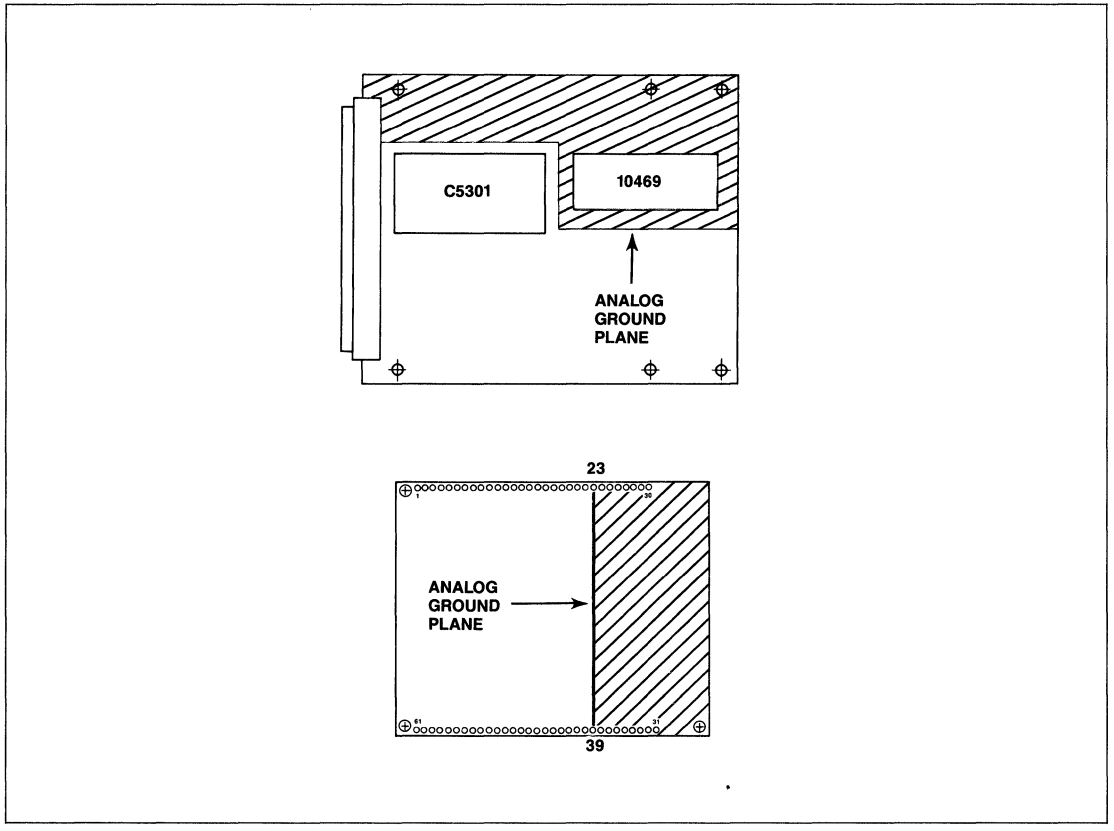


Figure 8. Analog Ground Plane Location

Rockwell

R1496DP
V.33 14.4 kbps/V.32 9600 bps Full-Duplex Modem

INTRODUCTION

The Rockwell R1496DP is a 14400 bps 4-wire/9600 bps 2-wire full-duplex, synchronous/asynchronous CCITT V.33 and V.32 modem data pump. It is designed to operate over leased lines, with dial backup, through the appropriate line termination. It is packaged in a small module with dual-in-line (DIP) connection for direct installation onto a host module.

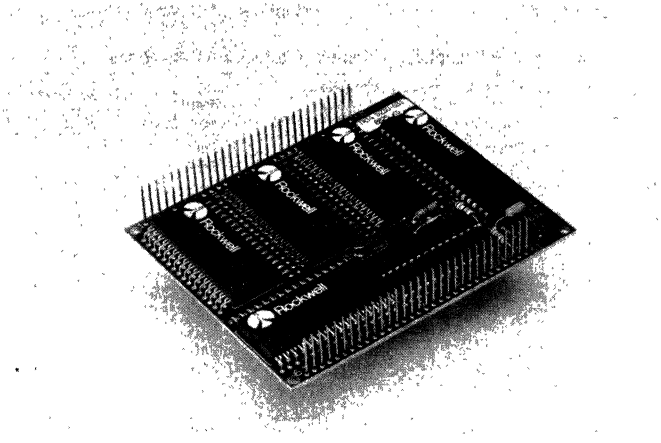
The modem satisfies the telecommunications requirements specified in CCITT recommendations V.33, V.32, V.29, and V.22 bis. The R1496DP can operate at speeds of 14400, 12000, 9600, 7200, 4800, 2400, or 1200 bps.

The R1496DP is designed for use in ultra high speed data applications. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size (less than 13 square inches), low power consumption, serial/parallel host interface, and DIP connection simplify system development and reduce system production cost.

This data sheet applies to the R1496DP with device numbers C5309-13, C5306-17, C5307-17, and subsequent.

FEATURES

- Compatibilities
  - — CCITT: V.33, V.32, V.29, V.22 bis
- Parallel synchronous
- Serial synchronous/asynchronous
- 4-Wire/2-Wire Full-Duplex Operation
- Trellis-Coded Modulation (TCM) at 14400, 12000, 9600 and 7200 bps
- 12000 bps data rate in V.32 (proprietary)
- Programmable Near and Far End Echo Cancellation
- Bulk Delay for Satellite Transmission
- Auto-Dial and Auto-Answer Capability
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Dynamic Range: – 43 dBm to 0 dBm
- Equalization
  - — Compromise Equalizer in Transmitter
  - — Automatic Adaptive Equalizer in Receiver
- Diagnostic Capability
- Loopback
  - — Local Analog
  - — Remote Digital
  - — Remote Analog (V.33, V.29)
- Small Size
  - — 82 mm x 100 mm (3.23 in. x 3.94 in.) with DIP Connection
- Low Power Consumption: 1.9 W (Typical)



R1496DP Modem

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

TONE GENERATION

Under control of the host processor, the modem can generate single or dual voice-band tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

DATA ENCODING

The data encoding conforms to CCITT recommendations V.33, V.32, V.29, and V.22 bis.

EQUALIZERS

Equalization functions are provided that improve performance when operating over low quality lines.

Compromise Equalizer — A 40-tap digital finite impulse response (FIR) filter in the transmitter provides compromise equalization. The filter taps can be changed in DSP RAM for varying line conditions. The default equalizer tap coefficients compensate for half the amplitude distortion of a 3002 unconditioned line and for half the group delay distortion of a 3002 unconditioned line. The filter can be enabled or disabled using the CEQ bit in the Chip 0 interface memory.

Automatic Adaptive Equalizer — A 48-tap automatic adaptive equalizer is provided in the receiver. The equalizer can be configured as either a T or a T/2 equalizer using the EQT2 bit in the Chip 2 interface memory.

TRANSMITTED DATA SPECTRUM

When the compromise equalizer is disabled, the transmitter spectrum is shaped by raised cosine filter functions as follows:

Configuration	Raised Cosine Filter Function
V.33, V.32, V.29	Square root of 12.5% or 20% as selected by the SHAP0 bit in the transmitter interface memory.
V.22 bis	Square root of 75%

RTS–CTS RESPONSE TIME

The response times of CTS relative to a corresponding transition of RTS are given in Table 2.

Table 2. RTS-CTS Response Time

Configuration	RTS-CTS Response[1]		Turn-Off Sequence[3]
	Constant Carrier	Controlled Carrier	
V.33	—	1393 ms[2]	15 ms
V.29	—	253 ms[2]	12 ms
V.32	≤2 ms	—	—
V.22 bis	≤2 ms	270 ms	—

Notes:
1. Times listed are CTS turn-on. CTS turn-off is less than 2 ms for all configuration.
2. Add echo protector tone duration plus 20 ms when echo protector tone is used.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones for controlled carrier operation.

— = not applicable

TRANSMIT LEVEL

The transmitter output level is selectable from −0.5 dBm to −15.5 dBm in 1 dB steps and is accurate to ± 0.5 dB. The output level can also be fine tuned to a value within a 1 dB step by changing a gain constant in RAM.

TRANSMITTER TIMING

Transmitter timing is selectable between internal (± 0.01%), external or loopback.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with the applicable CCITT recommendation.

ANSWER TONE

The transmitter generates a 2100 Hz answer tone for 3.6 seconds at the beginning of the answer handshake when the NV25 bit is a zero. This is applicable to V.32 and V.22 bis. The V.32 answer tone has 180 degree phase reversals every 0.45 seconds to disable network echo cancellers.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ± 0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits per Symbol		Constellation Points
					Data	TCM	
V.33 14400	TCM	1800 or 1700	14400	2400	6	1	128
V.33 12000	TCM	1800 or 1700	12000	2400	5	1	64
V.33 9600 TCM[2]	TCM	1800 or 1700	9600	2400	4	1	32
V.33 7200 TCM[2]	TCM	1800 or 1700	7200	2400	3	1	16
V.32 12000 TCM[2]	TCM	1800	12000	2400	5	1	64
V.32 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 9600	QAM	1800	9600	2400	4	0	16
V.32 4800	QAM	1800	4800	2400	2	0	4
V.32 7200 TCM[2]	TCM	1800	7200	2400	3	1	16
V.29 9600	QAM	1700	9600	2400	4	0	16
V.29 7200	QAM	1700	7200	2400	3	0	8
V.29 4800	QAM	1700	4800	2400	2	0	4
V.22 bis 2400	QAM	1200/2400	2400	600	4	0	16
V.22 bis 1200	QAM	1200/2400	1200	600	2	0	4
Tone Transmit							

Notes: 1. Modulation legend: TCM: Trellis-Coded Modulation
QAM: Quadrature Amplitude Modulation
FSK: Frequency Shift Keying
2. Proprietary

RECEIVE LEVEL

The receiver satisfies performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the Receiver Analog (RXA) input.

RECEIVER TIMING

The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

CARRIER RECOVERY

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off. $\overline{\text{RLSD}}$ can be clamped off by a bit in the receiver sample rate device interface memory (RLSDE).

ECHO CANCELLER

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full duplex V.32 operation. The combined echo span of near and far cancellers is host programmable with a default value of 53.3 ms (53.3 ms is also the maximum programmable value). The proportion allotted to each end is host programmable with default values of 23.3 ms for near-end and 30 ms for far-end. The delay between near-end and far-end echoes can be up to 1.7 seconds. The canceller can compensate for ±7 Hz frequency offset in the far-end echo.

The echo canceller error signal may be monitored through the transmitter DSP interface memory.

ASYNC/SYNC, SYNC/ASYNC CONVERSION

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converter operates in serial mode only. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character sizes, including all bits, are 7, 8, 9, 10 and 11 bits per character. Two ranges of signaling rates are provided:

- Basic range: +1% to −2.5%
- Extended overspeed range: +2.3% to −2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break is handled in the transmitter and receiver as described in V.22 bis.

Asynchronous characters are accepted by the transmitter on the TXD serial input and issued by the receiver on the RXD serial output. To configure the converters, the host must set up interface memory bits EXOS0, PEN0, STB0 and WDSZ0 bits before setting ASYN0 for the transmitter and EXOS1, PEN1, STB1 and WDSZ1 bits before setting ASYN1 for the receiver. (See description of these bits in Table 8.) Asynchronous data mode is not supported at data rates greater than 9600 bps.

AUTO-DIALING AND AUTO-ANSWERING CONTROL

General Description

Functions are provided to allow the host to perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection and a comprehensive supervisory tone detection scheme. The major parameters of these functions are host programmable, enabling the host to customize the modem to work on the public switched telephone network (PSTN).

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path. Therefore, the tone detect signal does not pass through the highpass section of the analog receive bandpass filter, enabling the tone detection to be largely independent of the receiver status. The tone detection bandwidth depends on the configuration:

Receiver Configuration	Tone Detection Bandwidth
V.33, V.32	0–3400 Hz
V.29	0–3400 Hz
V.22 bis Originate	0–2800 Hz
V.22 bis Answer	0–1700 Hz

There are, however, some restrictions depending on the receiver configuration and status:

1. When DATA1 bit (see Table 8) is a 0, all three tone detectors are enabled.
2. When DATA1 bit is a 1 and the receiver is in synchronous mode (except V.32 12000), tone detectors A and B are enabled and tone detector C is disabled.
3. When DATA1 bit is a 1, the receiver is in asynchronous mode or V.32 12000, and the TDAE bit is a 1, tone detector A is enabled and tone detectors B and C are disabled.
4. All three tone detectors are disabled during a V.32 handshake.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit in interface memory causing tone detector C to be an eighth order filter.

Supervisory Tone Detectors, Default Characteristics

The default bandwidths and thresholds of the tone detectors are as follows:

Tone Detector	Bandwidth	Turn-On Threshold	Turn-Off Threshold
A	245–650 Hz	−25 dBm	−31 dBm
B	360–440 Hz	−25 dBm	−31 dBm
C Prefilter	0–500 Hz	N/A	N/A
C	50–110 Hz	*	*

*Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range −1 dBm to −26 dBm.

HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 1) shows the typical modem connection in a system. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{IRQ}$). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high, (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals shown in Figure 1 are organized into six functional groups: overhead, microprocessor interface, V.24 interface, ancillary, analog, and diagnostic. These signals, along with their connector pin numbers and interface circuit types, are listed in Table 3. The digital interface characteristics are defined in Table 4.

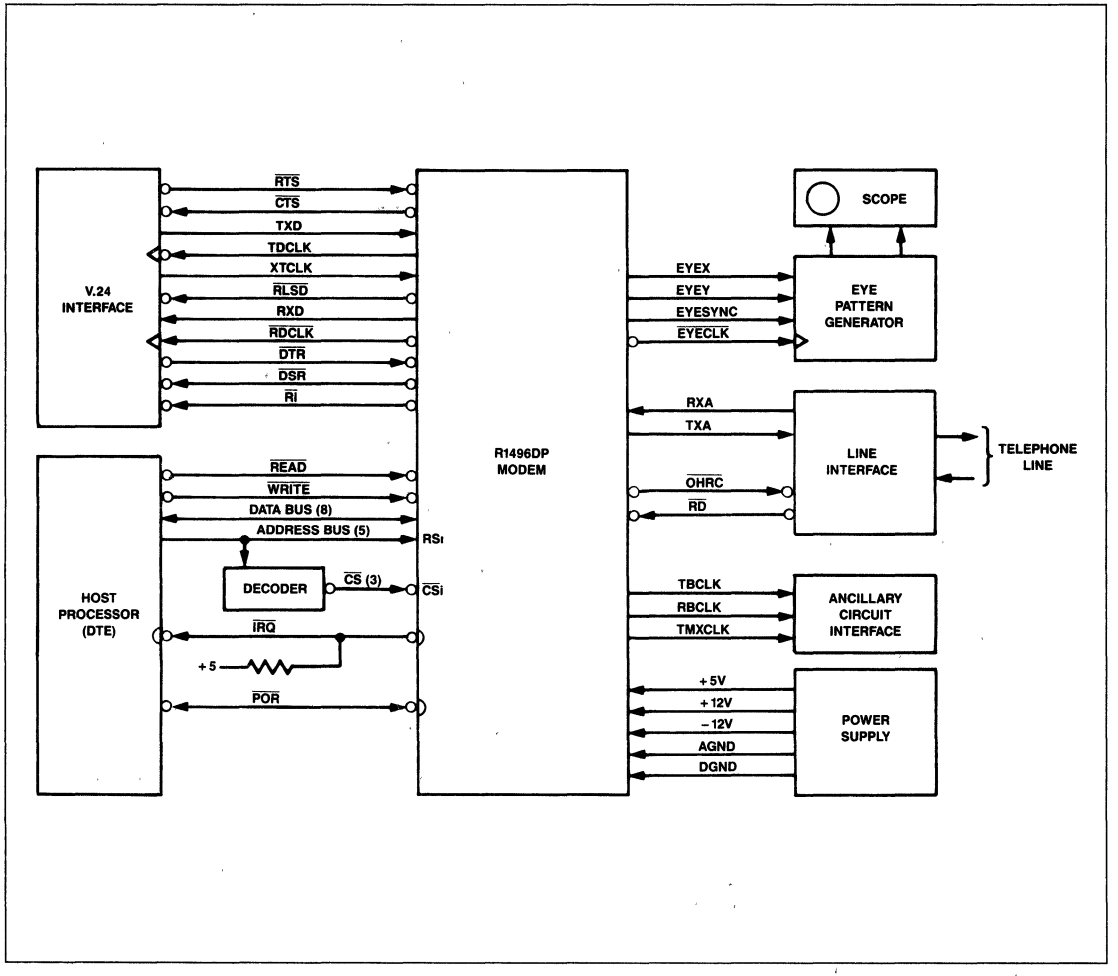


Figure 1. R1496DP Functional Interconnect Diagram

Table 3. R1496DP Hardware Interface Signals

Name	Type[1]	Pin No.[2]	Description
A. OVERHEAD:			
Ground (A)	AGND	30,31	Analog Ground Return
Ground (D)	DGND	29,37,53	Digital Ground Return
+5V	PWR	1,45,61	+5 Volt Supply
+12V	PWR	32	+12 Volt Supply
−12V	PWR	36	−12 Volt Supply
$\overline{POR}$	IA/OB	2	Power-On-Reset
B. MICROPROCESSOR INTERFACE:			
D7	IA/OB	3	Data Bus (8 Bits)
D6	IA/OB	4	
D5	IA/OB	5	
D4	IA/OB	6	
D3	IA/OB	7	
D2	IA/OB	8	
D1	IA/OB	9	
D0	IA/OB	10	
RS4	IA	15	Register Select (5 Bits)
RS3	IA	16	
RS2	IA	17	
RS1	IA	18	
RS0	IA	19	
$\overline{CS0}$	IA	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	13	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	14	Read Enable
$\overline{WRITE}$	IA	12	Write Enable
$\overline{IRQ}$	OC	11	Interrupt Request
C. V.24 INTERFACE:			
$\overline{RDCLK}$	OA	23	Receive Data Clock
TDCLK	OA	46	Transmit Data Clock
XTCLK	IA	51	External Transmit Clock
$\overline{RTS}$	IA	50	Request-to-Send
$\overline{CTS}$	OA	49	Clear-to-Send
TXD	IA	48	Transmitter Data
RXD	OA	26	Receiver Data
$\overline{RLSD}$	OA	27	Received Line Signal Detector
$\overline{DTR}$	IA	40	Data Terminal Ready
$\overline{DSR}$	OA	41	Data Set Ready
$\overline{RI}$	OA	25	Ring Indicator
D. ANCILLARY CIRCUITS:			
RBCLK	OA	22	Receiver Baud Clock
TBCLK	OA	47	Transmitter Baud Clock
TMXCLK	OA	43	Transmitter Mux Clock
E. LINE INTERFACE:			
TXA	AA	34	Transmitter Analog Output
RXA	AB	33	Receiver Analog Input
$\overline{OHRC}$	OD	35	Off-Hook Relay Control
$\overline{RD}$	IA	24	Ring Detect
F. DIAGNOSTIC:			
EYEX	OA	56	Eye Pattern Data—X Axis
EYEY	OA	55	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	57	Eye Pattern Clock
EYESYNC	OA	58	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 4 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. The following pins should be left open: 28, 39, 44, 52, 59 and 60.
3. The following pins are not used but should be connected to DGND through individual 10 KΩ series resistors: 38, 42 and 54.
4. Unused inputs tied to +5V or ground require individual 10 KΩ series resistors.

Table 4. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type				
			IA	OA	OB	OC	OD
V_{IH}	Input Voltage, High	V	2.0 Min.				
V_{IL}	Input Voltage, Low	V	0.8 Max.				
V_{OH}	Output Voltage, High	V		3.5 Min.[1]	3.5 Min.[1]		5.0 Max.
V_{OL}	Output Voltage, Low	V		0.4 Max.[2]	0.4 Max.[3]	0.4 Max.[2]	0.75 Typ.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.				
I_{OH}	Output Current, High	mA		−0.1 Max.	−0.1 Max		0[4]
I_{OL}	Output Current, Low	mA		1.6 Max.	0.8 Max.	1.6 Max.	15.0 Max.[5]
I_L	Output Current, Leakage	μA		±10 Max.	±10 Max.		
C_L	Capacitive Load	pF	5				
C_D	Capacitive Drive	pF		100	100	100	
	Circuit Type		TTL	TTL 3-state	TTL 3-state	Open-Drain	Open-Drain

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = 0.8 mA
4. μA leakage
5. Can drive a +5V relay with coil resistance greater than 360Ω.

POWER-ON-RESET

When power is applied to the modem, the modem pulses Power-On-Reset ($\overline{POR}$) low to begin the POR sequence. The modem is ready to use 350 ms after the low-to-high transition of $\overline{POR}$. The POR sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 μs. $\overline{POR}$ is not pulsed low by the modem when the POR sequence is initiated externally. The POR sequence initializes the modem interface memory to default values (Table 8). This action leaves the modem configured as follows:

- V.33 14400
- Synchronous mode
- Serial channel data
- T equalizer
- −43 dBm receiver threshold
- Transmitter compromise equalizer enabled
- Automatic rate change enabled
- Train-on-data disabled

NOTE: If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a POR sequence (i.e., < +3.5V), the host system should generate a $\overline{POR}$ signal upon supply voltage recovery to ensure proper modem initialization and operation.

MICROPROCESSOR INTERFACE

Nineteen address, data, control, and interrupt hardware interface signals allow modem connection to an 8086 compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000.

The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The significance of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

Data Lines (D0–D7)

Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.

Chip Selects ($\overline{CS0}$–$\overline{CS2}$) and Register Selects (RS0–RS4)

The three active low chip select lines ($\overline{CS0}$–$\overline{CS2}$) select one of three modem digital signal processor (DSP) devices. The five active high register select lines (RS0–RS4) address interface memory registers within the selected DSP interface memory. All eight of these lines are typically connected to the host bus address lines; the register select lines to the five least significant lines (A0–A4) and the chip select lines to the next two significant lines (A5–A6) through a decoder.

The selected DSP decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7 while the least significant data bit is D0.

Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

During a read cycle, data from the selected DSP interface memory register is gated onto the data bus by means of three-state drivers in each DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

The read/write cycle timing waveforms are illustrated in Figure 2 and the timing requirements are specified in Table 5.

Table 5. Microprocessor Interface Timing Parameters

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$i Setup Time	TCS	0	—	ns
RSi Setup Time	TRS	25	—	ns
Data Access Time	TDA	—	75	ns
Data Hold Time	TDHR	10	—	ns
Control Hold Time	THC	10	—	ns
Write Data Setup Time	TWDS	20	—	ns
Write Data Hold Time	TDHW	10	—	ns

Interrupt Request ($\overline{IRQ}$)

The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in the DSP interface memory to indicate immediate change of conditions in any of the three modem DSP devices. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.

The DSP $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). Each of the individual DSP $\overline{IRQ}$ output lines is wire-ORed to form the modem $\overline{IRQ}$ output signal. The modem $\overline{IRQ}$ output can also be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25W, is sufficient.

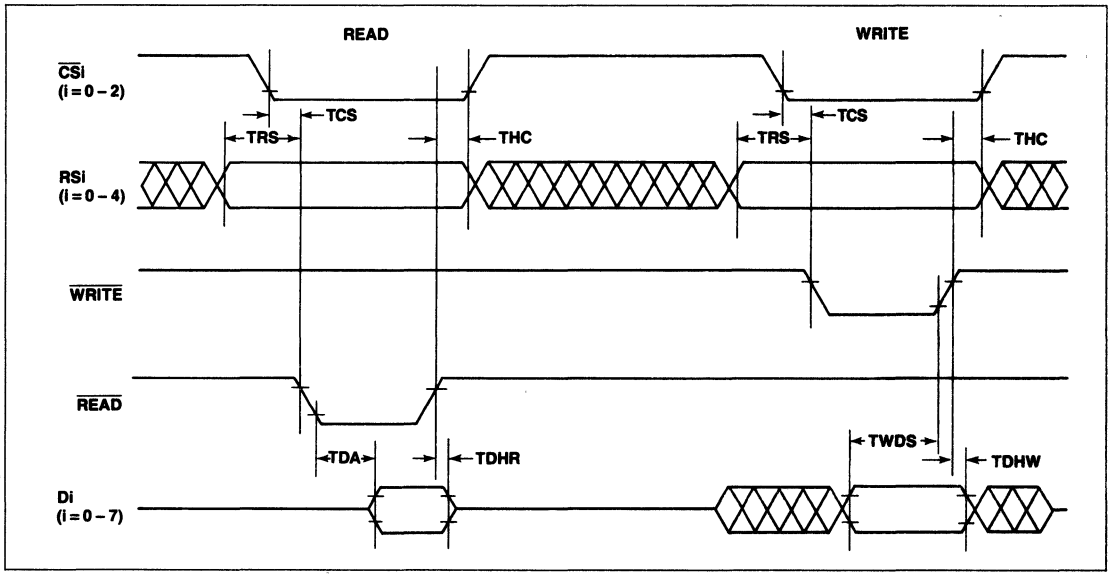


Figure 2. Microprocessor Interface Timing Waveforms

V.24 INTERFACE

Eleven pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels using 1489 receivers and 1488 drivers, or their equivalents.

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.

Received Data (RXD)

The modem presents received serial data to the local DTE on the Received Data (RXD) output.

Request To Send ($\overline{RTS}$)

Activating Request to Send ($\overline{RTS}$) causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The $\overline{RTS}$ pin is logically ORed with the RTS bit.

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) active indicates to the local DTE that the modem will transmit any data present on TXD. $\overline{CTS}$ response times from an active condition of $\overline{RTS}$ are shown in Table 2.

Received Line Signal Detector ($\overline{RLSD}$)

Received Line Signal Detector ($\overline{RLSD}$) active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence.

One of four $\overline{RLSD}$ receive level threshold options can be selected (Table 6). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than −43 dBm. The $\overline{RLSD}$ on and off thresholds are host programmable in DSP RAM.

Table 6. $\overline{RLSD}$ On and OFF Thresholds

	Receive Level	
Option	RLSD On	RLSD Off
0	> −43 dBm	< −48 dBm
1	> −33 dBm	< −38 dBm
2	> −26 dBm	< −31 dBm
3	> −16 dBm	< −21 dBm

Data Terminal Ready ($\overline{DTR}$)

In V.32 and V.22 bis configurations, activating Data Terminal Ready ($\overline{DTR}$) initiates the handshake sequence, provided that the DATA0 bit is a 1. If in answer mode, the transmitter will immediately send answer tone.

During the data mode, deactivating $\overline{DTR}$ causes the transmitter to turn-off and return to the idle state.

The $\overline{DTR}$ input and the DTR control bit in chip 0 are logically ORed.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) ON indicates that the modem is in the data transfer state. The OFF condition of $\overline{DSR}$ indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{RI}$). $\overline{DSR}$ is OFF when the modem is in a test mode (i.e., local analog or remote digital loopback).

The DSR status bit in chip 0 reflects the state of the $\overline{DSR}$ output.

Ring Indicator ($\overline{RI}$)

The Ring Indicator ($\overline{RI}$) output follows the ringing signal present on the line with a low level (0V) during the ON time, and a high level (+5V) during the OFF time coincident with the ringing signal.

The RI status bit in chip 2 reflects the state of the $\overline{RI}$ output.

Transmit Data Clock (TDCLK)

The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%.

Transmit Data (TXD) must be stable during the one μs periods immediately preceding the rising edge of TDCLK and following the rising edge of TDCLK. The TDCLK source can be internal, external (input on XTCLK) or slave (to $\overline{RDCLK}$) as selected by bits in the transmitter interface memory.

External Transmit Clock (XTCLK)

In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.

Receive Data Clock ($\overline{RDCLK}$)

The modem outputs a synchronous Receive Data Clock ($\overline{RDCLK}$) for USRT timing. The $\overline{RDCLK}$ frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The $\overline{RDCLK}$ low-to-high transitions coincide with the center of the received data bits. The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK) outputs have no counterpart in the V.24 or RS-232-C recommendations since they mark the baud interval rather than the data rate for the transmitter and receiver, respectively. These baud clocks are useful in identifying the order of data bits in a baud (e.g., for multiplexing data). Both signals are active high. The first bit in each baud begins with the falling edge of the corresponding baud clock.

Transmitter Multiplexer Clock (TMXCLK)

The Transmitter Multiplexer Clock (TMXCLK) output is a 288 kHz clock which is internally divided down to create the Transmitter Baud Clock (TBCLK). TMXCLK is also a common multiple of all the possible transmitter data clocks. The high-to-low transitions of TDCLK coincide with the high-to-low transitions of TMXCLK.

LINE INTERFACE

The Transmitter Analog (TXA) output and Receiver Analog (RXA) input allow modem connection to either a leased line or the public switched telephone network (PSTN) through an audio transformer or a data access arrangement. The analog signal characteristics of TXA and RXA are described in Table 7.

Table 7. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 66.5K ohms.

Transmitter Analog (TXA)

The Transmitter Analog (TXA) output can drive an audio transformer or data access arrangement. TXA is a low impedance amplifier output in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

Receiver Analog (RXA)

The Receiver Analog (RXA) input can originate from an audio transformer or data access arrangement. The input impedance is nominally 66.5K ohms. The RXA input must be shunted by an external 604 ohm ±1% resistor in order to match a 600 ohm source.

The maximum received signal at RXA is 0 dBm. The maximum near-end echo at RXA that the modem can cancel in V.32 mode is −5 dBm.

Transient protection for TXA and RXA is recommended when interfacing directly to a transformer. This protection may take the form of back-to-back zener diodes or a varistor across the transformer.

Ring Detect ($\overline{RD}$)

The Ring Detect ($\overline{RD}$) input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving $\overline{RD}$ should be a 4N35 optoisolator or equivalent. The circuit driving $\overline{RD}$ should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING.

DATA2 bit must be set to a 0 to enable ring detection. Detected ring signals are reflected on the $\overline{RI}$ output.

Off-Hook Relay Control ($\overline{OHRC}$)

$\overline{OHRC}$ is an output designed to drive directly a +5V reed relay coil with a worst case resistance of 360 ohms having a must operate voltage of 4.0 Vdc. A clamp diode integrated in the modem eliminates the need for a diode across the relay coil. An

external transistor can be used to drive heavier loads (e.g., electromechanical relays). $\overline{\text{OHCR}}$ is controlled by the host setting the RA bit in the interface memory.

Line Transformer Requirements for V.32

V.32 places high requirements upon the Data Access Arrangement (DAA) to the telephone line. V.32 uses the same bandwidth for transmission of data in both directions. Any non-linear distortion generated by the DAA in the transmit direction (known as near-end echo) cannot be canceled by the modem's echo canceller and interferes with data reception. The user must therefore ensure that the total harmonic distortion due to near-end echo at the RXA input to the modem is at least 27 dB below the minimum level of received signal at the same point. Note that the major source of non-linear distortion in a DAA is the line transformer. When designing a DAA the user should take into account a worst case subscriber line, giving very poor matching to the DAA hybrid circuit and resulting in a large near-end echo (to simulate worst case conditions it is suggested that an 1800 ohm resistor in series with a 0.47 μF capacitor be used in place of the two wire telephone line).

DIAGNOSTIC SIGNALS

Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. Timing of these signals is illustrated in Figure 3.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

EYEX and EYEY outputs are 15-bit words, each with 8-bits of significance. The 15-bit data words are shifted out most significant bit first with the seven most significant bits equal to zero. EYEX and EYEY are clocked by the rising edge of $\overline{\text{EYECLK}}$.

$\overline{\text{EYECLK}}$

$\overline{\text{EYECLK}}$ is a clock for use by the serial-to-parallel converters. The $\overline{\text{EYECLK}}$ output is a 288 kHz clock which is internally divided down to create the Receiver Baud Clock (RBCLK). $\overline{\text{EYECLK}}$ is also a common multiple of all the possible receiver data clocks. The low-to-high transitions of $\overline{\text{RDCLK}}$ coincide with the low-to-high transitions of $\overline{\text{EYECLK}}$. $\overline{\text{EYECLK}}$, therefore, can be used as a receiver multiplexer clock.

EYESYNC

EYESYNC is a strobe for loading the D/A converters.

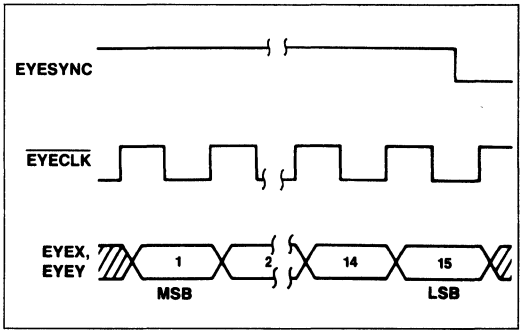


Figure 3. Eye Pattern Timing

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in three DSPs: transmitter device, receiver sample rate device, and receiver baud rate device.

INTERFACE MEMORY

Each DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in each DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus shared between the three DSPs.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAPS

Memory maps of the 96 addressable registers in the modem transmitter (chip 0), receiver sample rate (chip 1), and receiver baud rate (chip 2) devices are shown in Figure 4. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory.

INTERFACE MEMORY BIT DEFINITIONS

Table 8 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0,1 or 2), the register number by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

R1496DP DSP Interface Memory (Chip 0)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA0	NCIA0	—	NSIE0	NEWS0	NCIE0	—	NEWC0
1E	—	DBIA0	—	—	—	DBIE0	—	DBA0
1D	XACC0	—	—	—	—	XCRD0	XWT0	XCR0
1C	X RAM ADDRESS (XADD0)							
1B	YACC0	—	—	—	—	YCRD0	YWT0	YCR0
1A	Y RAM ADDRESS (YADD0)							
19	X RAM DATA MSB (XDAM0)							
18	X RAM DATA LSB (XDAL0)							
17	Y RAM DATA MSB (YDAM0)							
16	Y RAM DATA LSB (YDAL0)							
15	—	—	—	—	—	—	—	EARC0
14	—	—	—	—	—	—	—	—
13	TLVL				—	—	TXCLK	
12	TCONF							
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	—	—	CTS	DSR	—	TM	—	—
0E	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	HKAB0
0C	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	NV25	CC	DTMF	ORG	LL0	DATA0	—	DTR
08	ASYN0	TPDM	—	—	—	—	RTRN	RTS
07	—	RDL	L2ACT	—	L3ACT	L4ACT	RA	MHLD
06	—	EXOS0	—	—	PEN0	STB0	WDSZ0	
05	ECFZ	ECSQ	FECSQ	TXSQ	CEQ	TTDIS	—	TSPA
04	—	—	—	—	—	—	—	—
03	—	—	—	—	ARC0	SDIS	GTE	GTS
02	—	—	—	—	SHAP0	CF330	SEPT	EPT
01	TSPY							
00	TBUFFER/TSPX							

(—) Indicates reserved for modem use only.

R1496DP DSP Interface Memory (Chip 1)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA1	NCIA1	—	NSIE1	NEWS1	NCIE1	—	NEWC1
1E	—	DBIA1	—	—	—	DBIE1	—	DBA1
1D	XACC1	—	—	—	—	XCRD1	XWT1	XCR1
1C	X RAM ADDRESS (XADD1)							
1B	YACC1	—	—	—	—	YCRD1	YWT1	YCR1
1A	Y RAM ADDRESS (YADD1)							
19	X RAM DATA MSB (XDAM1)							
18	X RAM DATA LSB (XDAL1)							
17	Y RAM DATA MSB (YDAM1)							
16	Y RAM DATA LSB (YDAL1)							
15	—	—	—	—	—	—	—	EARC1
14	ABCODE							
13	—	—	—	—	RTH		—	—
12	RCONF							
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	RLSD	FED	—	—	—	—	—	—
0E	RTDET	—	—	—	—	SPEED		
0D	P2DET	PNDET	S1DET	SCR1	U1DET	SADET	—	HKAB1
0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	—	RSEQ
0B	TONEA	TONEB	TONEC	ATV25	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	—	—	LL1	DATA1	—	—
08	ASYN1	—	—	—	—	RTDIS	—	—
07	RDLE	—	—	—	—	—	—	—
06	—	EXOS1	—	—	PEN1	STB1	WDSZ1	
05	—	—	—	—	—	—	—	—
04	—	—	—	—	—	—	—	—
03	—	—	—	RLSDE	ARC1	—	—	—
02	TDAE	SQDIS	—	—	SHAP1	CF331	—	—
01	RSEQM							
00	RBUFFER/RSEQL							

(—) Indicates reserved for modem use only.

R1496DP Interface Memory (Chip 2)

Register \ Bit	7	6	5	4	3	2	1	0
1F	NSIA2	—	—	NSIE2	NEWS2	—	—	—
1E		DBIA2	—	—	—	DBIE2	—	DBA2
1D	XACC2	—	—	—	—	XCRD2	XWT2	XCR2
1C	X RAM ADDRESS (XADD2)							
1B	YACC2	—	—	—	—	YCRD2	YWT2	YCR2
1A	Y RAM ADDRESS (YADD2)							
19	X RAM DATA MSB (XDAM2)							
18	X RAM DATA LSB (XDAL2)							
17	Y RAM DATA MSB (YDAM2)							
16	Y RAM DATA LSB (YDAL2)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	—	—	—	—	—	—	—	—
12	—	—	—	—	—	—	—	—
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	—	—	—	—	RI	—	—	—
0E	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	—	—	—	DATA2	—	—
08	—	—	—	DDIS	—	—	—	—
07	—	—	—	—	—	—	—	—
06	—	—	—	—	—	—	—	—
05	—	—	—	—	—	—	—	—
04	EQRES	EQT2	—	RSPA	EQFZ	IFIX	TOD	—
03	—	—	—	—	—	—	—	—
02	—	—	AMTD	—	—	—	—	—
01	RSPY							
00	RSPX							

(—) Indicates reserved for modem use only.

Figure 4. R1496DP DSP Interface Memory Map

Table 8. R1496DP Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
AADET	1:C:7	—	**AA Detector.** When set to a 1, status bit AADET indicates that a V.32 AA sequence has been detected. This bit is reset to a 0 by the modem at the start of the CC sequence. (V.32)
ABCODE	1:14:0–7	00	**Abort Code.** If the V.32 handshake fails, status bit HSKAB is set to a 1 and an abort code is written into ABCODE. This code indicates the point in the handshake where the failure occurred. The abort code is not cleared by the modem but should be cleared by the host after it has been read. The abort codes and their meanings are listed in the table below. Refer to CCITT Recommendation V.32 for meanings of the signal mnemonics used. (V.32) **Abort Code** — **Reason for Aborting** 00 — No failure. 01 — Failed to detect AC/CA transition (calling). Failed to detect AA/CC transition (answering). 02 — Failed to detect CA/AC transition (calling). 03 — Not used. 04 — Timed out waiting for signal at the start of the S sequence. 05 — Failed to detect S sequence. 06 — Not used. 07 — Failed to detect Rate sequence (R1, R2 or R3). 08 — Failed to detect S/$\overline{S}$ transition. 09 — Failed to detect E sequence. 0A — Power loss during TRN or Rate sequence.
ACDET	1:C:6	—	**AC Detector.** When set to a 1, status bit ACDET indicates that a V.32 AC sequence has been detected. This bit is reset to a 0 by the modem when a CA sequence or an energy dropout is detected. (V.32)
AMTD	2:2:5	1	**Amplitude Modulation Tracker Disable.** When control bit AMTD is a 0, an adaptive amplitude modulation tracker is enabled in the receiver; when a 1, the tracker is disabled. (V.33, V.32, V.22 bis)
ARC0	0:3 3	1	**Automatic Rate Change Enable Chip 0.** When control bits ARC0 and ARC1 are a 1, the modem will automatically condition itself to transmit data at the highest common rate negotiated during the V.32 handshake. The host may specify the undefined bits in the rate sequence in DSP RAM. When ARC0 and ARC1 are a 0, the modem cannot change from the rate it is configured to before beginning the handshake. However, it is possible for the host to interact with the rate sequences during the handshake and then set the transmitter configuration as desired. (See EARC0). (V.32) When control bit ARC0 and ARC1 are a 1, the transmitter automatically conditions itself to transmit data at the highest common data rate according to the received rate sequence. The host may specify the undefined bits in the rate sequence in DSP RAM. When ARC0 and ARC1 are a 0, the host may check the received rate sequence in registers RSEQM and RSEQL and set the transmitter configuration acccordingly. For the transmitter to operate in the proprietary V.33 9600 or V.33 7200 modes then ARC0 and ARC1 must be 0. (V.33) When control bit ARC0 and ARC1 are a 1, then setting the RTRN bit will cause the modem to send a rate change sequence, rather than the normal retrain sequence. (V.22 bis) (See RTRN.)
ARC1	1:3:3	1	**Automatic Rate Change Enable Chip 1.** See ARC0 and EARC0.
ASYN0	0:8:7	0	**Asynchronous/Synchronous.** When configuration bit ASYN0 is a 1, asynchronous mode is selected in the transmitter; when 0, synchronous mode is selected. When the ASYN0 bit changes from 0 to 1, the transmitter's asynchronous to synchronous converter is configured according to the EXOS0, PEN0, STB0 and WDSZ0 bits at that time (EXOS0, PEN0, STB0 and WDSZ0 must be configured before ASYN0 changes from a 0 to a 1.) ASYN0 may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. Asynchronous operation is not available in V.32 12000 bps. (V.32, V.22 bis)
ASYN1	1:8:7	0	**Asynchronous/Synchronous.** When configuration bit ASYN1 is a 1, asynchronous mode is selected in the receiver; when 0, synchronous mode is selected. When the ASYN1 bit changes from 0 to 1, the receiver's synchronous to asynchronous converter is configured according to the EXOS1, PEN1, STB1 and WDSZ1 bits at that time (EXOS1, PEN1, STB1 and WDSZ1 must be configured before ASYN1 changes from a 0 to a 1.) ASYN1 may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. Asynchronous operation is not available in V.32 12000 bps. (V.32, V.22 bis)
ATV25	1:B:4	—	**V25 Answer Tone Detector.** When set to a 1, status bit ATV25 signifies that the modem receiver detected a 2100 Hz answer tone. The bit is set to a 1 when the answer tone is detected, and is cleared to a 0 when the tone ends. ATV25 is only active when the DATA1 bit is a 0 and the modem is in originate mode. (V.32, V.22 bis)
CADET	1:C:5	—	**CA Detector.** When set to a 1, status bit CADET indicates that a V.32 CA sequence has been detected. This bit is reset to a 0 by the modem when a AC sequence is detected. (V.32)

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
CC	0:9:6	0	**Controlled Carrier.** When control bit CC is a 1, the modem operates in controlled carrier; when 0, the modem operates in constant carrier. Controlled carrier allows the modem transmitter to be controlled by the $\overline{RTS}$ pin or the RTS bit (see Table 2). When the $\overline{RTS}$ pin goes to a 0, or the RTS bit set to a 1, the transmitter immediately sends scrambled ones for 270 ms and then turns on the $\overline{CTS}$ signal and the CTS bit. At 2400 bps, it is recommended that a retrain be sent once in the data mode to ensure that synchronization occurs. (V.22 bis)
CCDET	1:C:4	—	**CC Detector.** When set to a 1, status bit CCDET indicates that a V.32 CC sequence has been detected. This bit is reset to a 0 by the modem when an energy dropout is detected. (V.32)
CEQ	0:5:3	1	**Compromise Equalizer Enable.** When control bit CEQ is a 1, the transmitter's digital compromise equalizer is inserted into the transmit path. This bandpass equalizer has host programmable taps in DSP RAM. CEQ should be a 0 during local analog loopback.
CF330	0:2:2	0	**Carrier Frequency V.33 Chip 0.** When control bit CF330 is a 1, the transmitter carrier frequency in V.33 configurations is 1700 Hz. When control bit CF330 is a 0, the transmitter carrier frequency in V.33 configurations is 1800 Hz. (V.33) The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band.
CF331	1:2:2	0	**Carrier Frequency V.33 Chip 1.** When control bit CF331 is a 1, the receiver carrier frequency in V.33 configurations is 1700 Hz. When control bit CF331 is a 0, the receiver carrier frequency in V.33 configurations is 1800 Hz. (V.33) The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band.
CTS	0:F:5	—	**Clear To Send.** When set to a 1, status bit CTS indicates to the DTE that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 2. The CTS OFF-to-ON response time is programmable in DSP RAM. (V.32, V.22 bis)
DATA0	0:9:2	1	**Data Chip 0.** When control bit DATA0 is a 0, the transmitter is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering. (V.32, V.22 bis)
DATA1	1:9:2	1	**Data Chip 1.** When control bit DATA1 is a 0, the receiver is prevented from entering the training state. The receiver remains in idle mode. (V.33, V.29) When control bit DATA1 is a 0, the receiver is prevented from entering and proceeding with the handshake (start-up) sequence. If in originate mode, the answer tone detector is still active. Also, in V.32 the AC detector is active. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering. (V.32, V.22 bis) Recommended procedure for originating a call in V.32 using DATA1: Reset DATA1 and DTR to a 0 Establish a call Detect answer tone using ATV25 After receiving answer tone for 1 second, set DTR to a 1 When ATV25 equals 0 AND ACDET equals 1, set DATA1 to a 1 The handshake will now proceed
DATA2	2:9:2	1	**Data Chip 2.** When control bit DATA2 is a 0, the ringing detector is enabled, and when a 1, the ringing detector is disabled. This bit should be set to a 1 after the modem goes off-hook, otherwise the $\overline{RI}$ signal and RI bit will give spurious outputs. (V.32, V.22 bis)
DBA0	0:1E:0	—	**Data Buffer Available Chip 0.** When set to a 1, status bit DBA0 signifies that the transmitter has read register 0:0 (TBUFFER), or registers 0:1 (TSPY) and 0:0 (TSPX), and the host can write new data into register 0:0, or registers 0:1 and 0:0. This condition can also cause $\overline{IRQ}$ to be asserted. The host writing to register 0:0 resets the DBA0 and DBIA0 bits to 0. (See DBIE0 and DBIA0.)
DBA1	1:1E:0	—	**Data Buffer Available Chip 1.** When set to a 1, status bit DBA1 signifies that the receiver wrote valid data into register 1:0 (RBUFFER), or registers 1:1 (RSEQM) and 1:0 (RSEQL). This condition can also cause $\overline{IRQ}$ to be asserted. The host reading register 1:0 resets the DBA1 and DBIA1 bits to 0. (See DBIE1 and DBIA1.)
DBA2	2:1E:0	—	**Data Buffer Available Chip 2.** When set to a 1, status bit DBA2 signifies that the receiver wrote valid data into registers 2:1 (RSPY) and 2:0 (RSPX). This condition can also cause $\overline{IRQ}$ to be asserted. The host reading register 2:0 resets the DBA2 and DBIA2 bits to 0. (See DBIE2 and DBIA2.)

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
DBIA0	0:1E·6	—	**Data Buffer Interrupt Active Chip 0.** When the transmitter data buffer interrupt is enabled (DBIE0 is a 1) and register 0:0 is empty (DBA0 is set to a 1), the transmitter asserts $\overline{IRQ}$ and sets status bit DBIA0 to a 1 to indicate that DBA0 going to a 1 caused the interrupt The host writing to register 0:0 resets the DBIA0 bit to a 0 and clears the interrupt request due to DBA0. (See DBIE0 and DBA0.)
DBIA1	1:1E:6	—	**Data Buffer Interrupt Active Chip 1.** When the receiver chip 1 data buffer interrupt is enabled (DBIE1 is a 1) and register 1:0 is written to by the DSP (DBA1 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets DBIA1 to a 1 to indicate that DBA1 going to a 1 caused the interrupt The host reading register 1 0 resets the DBIA1 bit to a 0 and clears the interrupt request due to DBA1. (See DBA1 and DBIE1.)
DBIA2	2:1E:6	—	**Data Buffer Interrupt Active Chip 2.** When the receiver chip 2 data buffer interrupt is enabled (DBIE2 is a 1) and register 2:0 is written to by the DSP (DBA2 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets DBIA2 to a 1 to indicate that DBA2 going to a 1 caused the interrupt. The host reading register 2 0 resets the DBIA2 bit to a 0 and clears the interrupt request due to DBA2. (See DBA2 and DBIE2.)
DBIE0	0:1E:2	0	**Data Buffer Interrupt Enable Chip 0.** When control bit DBIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set the DBIA0 bit to a 1 when DBA0 is set to 1 by the DSP. When DBIE0 is a 0 (interrupt disabled), DBA0 has no effect on $\overline{IRQ}$ or DBIA0. (See DBA0 and DBIA0)
DBIE1	1:1E·2	0	**Data Buffer Interrupt Enable Chip 1.** When control bit DBIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set the DBIA1 bit to a 1 when DBA1 is set to a 1 by the DSP. When DBIE1 is a 0 (interrupt disabled), DBA1 has no effect on $\overline{IRQ}$ or DBIA1. (See DBA1 and DBIA1.)
DBIE2	2:1E:2	0	**Data Buffer Interrupt Enable Chip 2.** When control bit DBIE2 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set the DBIA2 bit to a 1 when DBA2 is set to a 1 by the DSP. When DBIE2 is a 0 (interrupt disabled), DBA2 has no effect on $\overline{IRQ}$ or DBIA2. (See DBA2 and DBIA2.)
DDIS	2:8:4	0	**Descrambler Disable.** When control bit DDIS is a 1, the receiver's descrambler circuit is disabled; when a 0, the descrambler circuit is enabled.
DSR	0:F:4	—	**Data Set Ready.** When set to a 1 (ON), status bit DSR indicates that the modem is in the data transfer state. When reset to a 0 (OFF), DSR indicates that the DTE is to disregard all signals appearing on the interchange circuits—except $\overline{RI}$. DSR will switch to the OFF state when the modem is in a test mode. (V.32, V.22 bis)
DTMF	0:9:5	0	**DTMF Select.** When the modem is configured for dialing mode, the modem will dial using DTMF tones or pulses. When control bit DTMF is a 1, the modem will dial using DTMF tones. When DTMF is a 0, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. Dialing mode is selected by configuration code 81 in the Transmitter Configuration Register (TCONF). When in dialing mode, the data placed in the Transmitter Data Register is treated as digits to be dialed. The number to be dialed must be represented by two hexadecimal digits (e g., if a 9 is to be dialed, then a 09 must be written to the Transmitter Data Register). Also, see DBA0 bit Dialing timing and power levels are host programmable in DSP RAM (Table 11).
DTR	0·9:0	0	**Data Terminal Ready.** In V.32 and V 22 bis modes, setting control bit DTR to a 1 initiates a handshake sequence, providing DATA0 bit is a 1 If in answer mode, the transmitter will immediately send answer tone. During the data mode, setting DTR to a 0 will cause the transmitter to turn off. The DTR bit parallels the operation of the hardware $\overline{DTR}$ control input. These inputs are ORed by the modem.
EARC0	0:15:0	0	**Extended Automatic Rate Change 0.** When control bits EARC0 and EARC1 are 1 (and also ARC0 and ARC1 are 1), then rate changes to the proprietary 12000 and 7200 TCM configurations are allowed during the V 32 handshake. The modem will condition itself to transmit data at the highest common rate negotiated during the V.32 handshake These rates include the proprietary 12000 and 7200 TCM configurations, if both calling and answering modems support these configurations. When EARC0 and EARC1 are 0, then rate changes are only allowed to standard CCITT V.32 configurations There are two methods for operating in the proprietary 12000 and 7200 TCM configurations. The first is to set bits ARC0, ARC1, EARC0 and EARC1 all to 0. TCONF and RCONF should then be set for the required configuration. The modem will then only be able to connect in the configuration selected. Both calling and answering modems have to be configured the same way for a successful connection. The second method is to set bits ARC0, ARC1, EARC0 and EARC1 all to 1. TCONF and RCONF should be set as desired, but in this case rate negotiation takes place during the V.32 handshake. Use of this method allows fall-back or fall-forward retrains in 2400 bps steps from 12000 bps to 4800 bps. In order to accomplish rate changes to the proprietary configurations, the modem uses two bits in the V 32 16 bit rate sequence that are undefined in CCITT Recommendation V.32. These are bits B9 and B10. (V 32)

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
EARC1	1:15:1	0	**Extended Automatic Rate Change Chip 1.** See EARC0. (V.32)
ECFZ	0:5:7	0	**Echo Canceller Freeze.** When control bit ECFZ is a 1, the updating of the echo canceller taps is inhibited. (V.32)
ECSQ	0:5:6	0	**Echo Canceller Squelch.** When control bit ECSQ is a 1, the echo canceller output is forced to zero. (V.32) ECSQ, along with TXSQ, can be used to determine if the line has been dropped by the remote modem. Many times due to the dropping of the line by the remote modem, a line mismatch occurs at the near end modem's line interface. This causes a large increase in near end echo. Many errors should be seen at this time. If this is the case, squelching both the echo canceller and the transmitter should cause RLSD to go inactive. The host should first freeze the echo canceller (this is done in case the line is not dropped) by setting ECFZ to a 1. Then set both ECSQ and TXSQ to a 1. If RLSD drops, then the line was dropped by the remote modem and the near end modem should then be disconnected from the line by the host. If RLSD does not drop, then the host should reset ECFZ, ECSQ, and TXSQ to a 0 and issue a retrain, if applicable.
EPT	0:2:0	0	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 185 ms (SEPT bit = 0) or 30 ms (SEPT bit = 1) followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence. (V.33, V.29) The echo protector tone is typically used in V.27 and V.29 over dial-up lines. The tone is sent prior to the training sequence to ensure that the echo suppressors are pointing in the correct direction.
EQFZ	2:4:3	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.
EQRES	2:4:7	0	**Equalizer Reset.** When control bit EQRES is a 1, the receiver resets all of the adaptive equalizer's taps to zero. When EQRES is a 0, the equalizer taps are updated normally by the receiver (chip 2). Setting EQRES to a 1 effectively clamps the receiver. EQRES along with RLSDE can be used to clamp the receiver off and turn off the $\overline{\text{RLSD}}$ pin. An equalizer reset is automatically done for a brief period of time at the beginning of the train-on-data state (TOD = 1). Therefore, the host does not have to manually set then clear this bit to reset the equalizer for line hits, etc., when TOD is active.
EQT2	2:4:6	0	**Equalizer T/2 Spacing Select.** When control bit EQT2 is a 1, the receiver's adaptive equalizer is T/2 fractionally spaced. When EQT2 is a 0, the equalizer is T spaced (T = 1 baud time). (V.33, V.32, V.29)
EXOS0	0:6:6	0	**Extended Overspeed Chip 0.** When control bit EXOS0 is a 1, Extended Overspeed mode is selected in the transmitter async-to-sync converter. This bit must be configured appropriately before the ASYN0 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis)
EXOS1	1:6:6	0	**Extended Overspeed Chip 1.** When control bit EXOS1 is a 1, Extended Overspeed mode is selected in the receiver sync-to-async converter. This bit must be configured appropriately before the ASYN1 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis)
FECSQ	0:5:5	0	**Far Echo Canceller Squelch.** When control bit FECSQ is a 1, the output of the far-end echo canceller is forced to zero; the near-end echo canceller continues to operate normally. (V.33, V.32, V.29) Squelching the far end echo canceller should only be done for testing purposes to manually characterize the far end echo.
FED	1:F:6	—	**Fast Energy Detector.** When status bit FED is a 1, energy in the passband above the selected receiver threshold has been detected (see RTH).
GTE	0:3:1	0	**Guard Tone Enable.** When set to a 1, control bit GTE causes the specified guard tone to be transmitted (CCITT configurations only), according to the state of the GTS bit. Note: The guard tone will only be transmitted by the answering modem. (V.22 bis)
GTS	0:3:0	0	**Guard Tone Select.** When set to a 1, control bit GTS selects the 550 Hz tone; when reset to a 0, GTE selects the 1800 Hz tone. The selected guard tone will be transmitted only when GTE is enabled. (V.22 bis)
HKAB0	0:D:0	—	**Handshake Abort Chip 0.** When set to a 1 status bit HKAB0 indicates that the V.32 handshake has failed. The transmitter remains in an abort state for 1 second after which HKAB0 is reset to 0 and the transmitter returns to idle mode. While in the abort state the transmitter output is silent. Normally this bit is set shortly after the HKAB1 bit with one exception. When the calling modem receives rate sequence R3 (refer to CCITT Recommendation V.32) and ARC0 is set to a 1, then if no common rates are found or R3 is calling for a GSTN cleardown then HKAB0 will be set before HKAB1. (V.32)
HKAB1	1:D:0	—	**Handshake Abort.** When set to a 1, status bit HKAB1 indicates that the V.32 handshake has failed. At the same time an abort code is written into ABCODE (see ABCODE). The receiver remains in an abort state for 0.5 seconds after which HKAB1 is reset to 0 and the receiver returns to idle mode. (V.32)

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
IFIX	2:4:2	1	**Eye Fix.** When control bit IFIX is a 1, the serial diagnostic data at the EYEX and EYEY pins reflects the Rotated Equalizer Output. When IFIX is a 0, the data on EYEX and EYEY is selected by the addresses in X RAM ADDRESS and Y RAM ADDRESS registers in chip 2, respectively.
LL0	0:9:3	0	**Leased Line Chip 0.** When control bit LL0 is a 1, the transmitter is in leased line operation; when 0, the transmitter is in switched line operation. When LL0 is set to a 1 and the CC bit is a 0, the modem immediately sends scrambled ones and goes into data mode. (V.22 bis) At 2400 bps it is recommended that a retrain be sent once in the data state to ensure that synchronization occurs.
LL1	1:9:3	0	**Leased Line Chip 1.** When control bit LL1 is a 1, the receiver is in leased line operation; when 0, the receiver is in switched line operation. (V.22 bis)
L2ACT	0:7 5	0	**Loop 2 Activate.** When control bit L2ACT is a 1, the receiver's digital output is connected to the transmitter's digital input (locally activated remote digital loopback) in accordance with CCITT Recommendation V.54
L3ACT	0:7:3	0	**Loop 3 Activate.** When control bit L3ACT is a 1, the transmitter's analog output is coupled to the receiver's analog input through an attenuator (local analog loopback) in accordance with CCITT Recommendation V.54 In V.33 and V.29 modes, the modem can be placed in loop 3 in either idle or data mode. If loop 3 is initiated in data mode, the connection to the other modem is terminated. In V.32 and V 22 bis modes, the modem may only be placed into loop 3 mode when in idle mode ($\overline{DTR}$ signal is OFF and the DTR bit is 0). NEWC0 and NEWC1 must be set after any change in the L3ACT bit. Set NEWC0 to a 1 and wait until the modem resets it to a 0. Wait 2 ms. Set the NEWC1 bit to a 1 and wait for the modem to reset it to a 0. The loopback is then completed (terminated) by setting the $\overline{DTR}$ signal ON (OFF) or the DTR bit to a 1 (0). The transmitter's compromise equalizer should be disabled, by setting CEQ to a 0, during local analog loopback.
L4ACT	0:7:2	0	**Loop 4 Activate.** When control bit L4ACT is a 1, the receiver's analog input is connected to the transmitter's output (remote analog loopback) in a manner similar to CCITT Recommendation V.54. (V.33, V.29)
MHLD	0:7:0	0	**Mark Hold.** When control bit MHLD is a 1, the transmitter's digital input data is clamped to a mark. When MHLD is a 0, the transmitter's input is taken from TXD or TBUFFER (see TPDM).
NCIA0	0:1F:6	—	**NEWC0 Interrupt Active.** When the new configuration chip 0 interrupt is enabled (NCIE0 is a 1) and a new transmitter configuration is implemented (NEWC0 is reset to a 0), the DSP asserts $\overline{IRQ}$ and sets status bit NCIA0 to a 1 to indicate that NEWC0 going to a 0 caused the interrupt. NCIA0 and the interrupt request due to NEWC0 are cleared by the host writing a 0 into NCIE0. (See NEWC0 and NCIE0.)
NCIA1	1:1F:6	—	**NEWC1 Interrupt Active.** When the new configuration chip 1 interrupt is enabled (NCIE1 is a 1) and a new receiver configuration is implemented (NEWC1 is reset to a 0), the DSP asserts $\overline{IRQ}$ and sets status bit NCIA1 to a 1 to indicate that NEWC1 going to a 0 caused the interrupt. NCIA1 and the interrupt request due to NEWC1 are cleared by the host writing a 0 into NCIE1. (See NEWC1 and NCIE1.)
NCIE0	0:1F:2	0	**NEWC0 Interrupt Enable.** When control bit NCIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set NCIA0 to a 1 when the NEWC0 bit is reset to a 0 by the DSP. When NCIE0 is a 0 (interrupt disabled), NEWC0 has no effect on $\overline{IRQ}$ or NCIA0 (See NEWC0 and NCIA0.)
NCIE1	1:1F:2	0	**NEWC1 Interrupt Enable.** When control bit NCIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA1 to a 1 when the NEWC1 bit is reset to a 0 by the DSP. When NCIE1 is a 0 (interrupt disabled), NEWC1 has no effect on $\overline{IRQ}$ or NCIA1. (See NEWC1 and NCIA1.)
NEWC0	0:1F:0	0	**New Configuration Chip 0.** Control bit NEWC0 must be set to a 1 by the host after the host changes the configuration code in TCONF (0:12), the SHAP0 bit (0:2:3), the L3ACT bit (0:7:3) (in V.32 or V 22 bis), or the ORG bit (0:9:4) This informs the transmitter to implement the new transmitter configuration and/or shaping filter. The DSP resets the NEWC0 bit to a 0 when the configuration change is implemented. A configuration change can also cause $\overline{IRQ}$ to be asserted. (See NCIE0 and NCIA0.)
NEWC1	1:1F:0	0	**New Configuration Chip 1.** Control bit NEWC1 must be set to a 1 by the host after the host changes the configuration code in RCONF (1:12), the SHAP1 bit (1:2:3), the L3ACT bit (0:7:3), RTH (1.13:2-3), or the ORG bit (0:9:4). This informs the receiver to implement the new receiver configuration, the new receiver threshold, and/or the receiver shaping filter. The DSP resets the NEWC1 bit to a 0 when the change is implemented A configuration/receiver threshold change can also cause $\overline{IRQ}$ to be asserted. (See NCIE1 and NCIA1)
NEWS0	0:1F:3	—	**New Status Chip 0.** When set to a 1, status bit NEWS0 indicates that one or more status bits located in registers 0E or 0F have changed state, or a DSP RAM read or write has been completed, in the transmitter. This bit can be reset to a 0 only by the host. The host may mask the effect of individual status bits upon NEWS0 by writing a mask value to DSP RAM. When set to a 1, this bit can cause $\overline{IRQ}$ to be asserted. (See NSIE0 and NSIA0.)

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
NEWS1	1:1F:3	—	**New Status Chip 1.** When set to a 1, status bit NEWS1 indicates that one or more status bits located in registers 0A to 0F have changed state, or a DSP RAM read or write has been completed, in receiver DSP chip 1. This bit can be reset to a 0 only by the host. The host may mask the effect of individual status bits upon NEWS1 by writing a mask value to DSP RAM. When set to a 1, this bit can cause $\overline{IRQ}$ to be asserted. (See NSIE1 and NSIA1.)
NEWS2	2:1F:3	—	**New Status Chip 2.** When set to a 1, status bit NEWS2 indicates that the RI status bit in register 0F has changed state, or a DSP RAM read or write has been completed, in receiver DSP chip 2. This bit can be reset to a 0 only by the host. The host may mask the effect of the RI status bit upon NEWS2 by writing a mask value to DSP RAM. When set to a 1, this bit can cause $\overline{IRQ}$ to be asserted. (See NSIE2 and NSIA2.)
NSIA0	0:1F:7	—	**NEWS0 Interrupt Active Chip 0.** When the new status interrupt chip 0 is enabled (NSIE0 is a 1) and a change of status occurs (NEWS0 is set to a 1), the transmitter asserts $\overline{IRQ}$ and sets status bit NSIA0 to a 1 to indicate that NEWS0 going to a 1 caused the interrupt. NSIA0 and the interrupt request due to NEWS0 are cleared when the host writes a 0 to NEWS0. (See NEWS0 and NSIE0.)
NSIA1	1:1F:7	—	**NEWS1 Interrupt Active Chip 1.** When the new status interrupt chip 1 is enabled (NSIE1 is a 1) and a change a status occurs (NEWS1 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets status bit NSIA1 to a 1 to indicate that NEWS1 going to a 1 caused the interrupt. NSIA1 and the interrupt request due to NEWS1 are cleared when the host writes a 0 to NEWS1. (See NEWS1 and NSIE1.)
NSIA2	2:1F:7	—	**NEWS2 Interrupt Active Chip 2.** When the new status interrupt chip 2 is enabled (NSIE2 is a 1) and a change of status occurs (NEWS2 is set to a 1), the receiver asserts $\overline{IRQ}$ and sets status bit NSIA2 to a 1 to indicate that NEWS2 going to a 1 caused the interrupt. NSIA2 and the interrupt request due to NEWS2 are cleared when the host writes a 0 to NEWS2. (See NEWS2 and NSIE2.)
NSIE0	0:1F:4	0	**NEWS0 Interrupt Enable Chip 0.** When control bit NSIE0 is a 1 (interrupt enabled), the transmitter will assert $\overline{IRQ}$ and set NSIA0 to a 1 when NEWS0 is set to a 1 by the DSP. When NSIE0 is a 0 (interrupt disabled), NEWS0 has no effect on $\overline{IRQ}$ or NSIA0. (See NEWS0 and NSIA0.)
NSIE1	1:1F:4	0	**NEWS1 Interrupt Enable Chip 1.** When control bit NSIE1 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA1 to a 1 when NEWS1 is set to a 1 by the DSP. When NSIE1 is a 0 (interrupt disabled), NEWS1 has no effect on $\overline{IRQ}$ or NSIA1. (See NEWS1 and NSIA1.)
NSIE2	2:1F:4	0	**NEWS2 Interrupt Enable Chip 2.** When control bit NSIE2 is a 1 (interrupt enabled), the receiver will assert $\overline{IRQ}$ and set NSIA2 to a 1 when NEWS2 is set to a 1 by the DSP. When NSIE2 is a 0 (interrupt disabled), NEWS2 has no effect on $\overline{IRQ}$ or NSIA2. (See NEWS2 and NSIA2.)
NV25	0:9:7	0	**No V.25 Answer Tone.** When control bit NV25 is a 1, the modem will not transmit the 2100 Hz CCITT answer tone when a handshake sequence is initiated and the modem is in answer mode. (V.32, V.22 bis)
ORG	0:9:4	1	**Originate.** When configuration bit ORG is a 1, the modem is in originate mode; when a 0, the modem is in answer mode. Since this is a configuration bit, the NEWC0 and NEWC1 bits must be set after any change in the ORG bit. Set NEWC0 to a 1 and wait until the modem resets it to a 0. Wait 2 ms. Set the NEWC1 bit to a 1 and wait for the modem to reset it to a 0. (V.32, V.22 bis)
PEN0	0:6:3	0	**Parity Enable Chip 0.** When control bit PEN0 is a 1, parity is enabled in asynchronous mode in the transmitter. This bit must be configured appropriately before the ASYN0 bit changes from a 0 to a 1 for asynchronous mode (V.32, V.22 bis)
PEN1	1:6:3	0	**Parity Enable Chip 1.** When control bit PEN1 is a 1, parity is enabled in asynchronous mode in the receiver. This bit must be configured appropriately before the ASYN1 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V 22 bis)
PNDET	1:D:6	—	**PN Sequence Detected.** When status bit PNDET is a 1, the receiver is detecting the PN portion of the training sequence When PNDET is a 0, PN is not being detected. (V.33, V.29)
P2DET	1:D:7	—	**P2 Sequence Detected.** When status bit P2DET is a 1, the receiver is detecting the P2 portion of the training sequence. When P2DET is a 0, P2 is not being detected. (V.33, V 29)
RA	0:7:1	0	**Relay Activate.** When control bit RA is a 1, the output $\overline{OHRC}$ is activated (low); when a 0, the $\overline{OHRC}$ output is off (high).
RBUFFER	1:0:0–7	—	**Receive Buffer.** The host obtains channel data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER. The data is divided on the baud boundaries shown under TBUFFER The RBUFFER reflects the received data when the RSEQ bit is a 0.

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
RCONF	1:12:0–7	31	**Receiver Configuration.** The RCONF control bits select one of the following receiver configurations:

Mode	Data Rate	RCONF (Hex)
V.33 TCM	14400	31
V.33 TCM	12000	32
V.33 TCM	9600	34
V.33 TCM	7200	38
V.32 TCM	12000	72
V.32 TCM	9600	74
V.32	9600	75
V.32	4800	71
V.32 TCM	7200	78
V.29	9600	14
V.29	7200	12
V.29	4800	11
V.22 bis	2400	84

RDL	0:7:6	0	**Remote Digital Loopback.** When set to a 1, control bit RDL causes the modem to initiate a request for the modem to go into digital loopback; RXD is clamped to a mark and the CTS bit and $\overline{\text{CTS}}$ signal will be reset until the loop is established. The TM bit is not set in this case, since the local modem initiated the request. (V.22 bis)
RDLE	1:7:7	1	**Remote Digital Loopback Response Enable.** When set to a 1, control bit RDLE enables the modem to respond to another modem's remote digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS, DSR and RLSD bits to a 0, and turns the $\overline{\text{CTS}}$, $\overline{\text{DSR}}$ and $\overline{\text{RLSD}}$ signals to a logic 1. The TM bit is set to a 1, to inform the host of the test status. When the RDLE bit is a 0, no response will be generated. (V.22 bis)
RI	2:F:3	—	**Ring Indicator.** When set to a 1, status bit RI indicates that a ringing signal is being detected. Ringing is detected if pulses are present on the $\overline{\text{RD}}$ input in the 15 Hz – 68 Hz frequency range. The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with $\overline{\text{RI}}$ output signal. The decision bounds are host programmable in DSP RAM. The bit is valid only when the receiver DATA2 bit (2:9:2) is a 0.
RLSD	1:F:7	—	**Received Line Signal Detector.** When status bit RLSD is a 1, the receiver has finished receiving the training sequence or has turned on due to detected energy above threshold, and is receiving data. RLSD is a 0 when the receiver is in the idle state and during the reception of a training sequence.
RLSDE	1:3:4	1	**RLSD Enable.** When control bit RLSDE is a 1, the $\overline{\text{RLSD}}$ pin reflects the RLSD bit. When RLSDE is a 0, the $\overline{\text{RLSD}}$ pin is clamped to a 1 (OFF condition) regardless of the state of the RLSD bit.
RSEQ	1:C:0	0	**Rate Sequence Received.** When status bit RSEQ is a 1, the 16-bit rate sequence included in the CCITT V.33 or V.32 start-up procedure has been received and the 16-bit rate sequence word is available in RSEQM (1:1) and RSEQL (1:0). (V.33, V.32)
RSEQL	1:0:0–7	—	**Rate Sequence LSB.** When the RSEQ bit is a 1, register 1:0 holds the least significant byte of the 16-bit V.33 or V.32 rate sequence word (RSEQL) received by the modem. When the RSEQ bit is a 0, register 1:0 holds the received data (see RBUFFER). (V.33, V.32)
RSEQM	1:1:0–7	—	**Rate Sequence MSB.** When the RSEQ bit is a 1, register 1:1 holds the most significant byte of the 16-bit V.33 or V.32 rate sequence word (RSEQM) received by the modem. When the RSEQ bit is a 0, register 1:1 is not used. (V.33, V.32)
RSPA	2:4:4	1	**Receiver Signal Point Activate.** When control bit RSPA is a 1, the receiver writes the received signal point coordinates, after the decision processing, into registers RSPY (2:1) and RSPX (2:0). When RSPA is a 0, RSPY and RSPX do not contain the signal point coordinates.
RSPX	2:0:0–7	—	**Receiver Signal Point X.** RSPX holds the X (in-phase) coordinate of the received signal point. RSPX is valid only when RSPA is a 1. (See RSPA.)
RSPY	2:1:0–7	—	**Receiver Signal Point Y.** RSPY holds the Y (quadrature) coordinate of the received signal point. RSPY is valid only when RSPA is a 1. (See RSPA.)

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
RTDET	1:E:7	—	**Retrain Detector.** When set to a 1, status bit RTDET indicates that a training sequence has been detected. This bit parallels the operation of the following: Mode — Detector Bit V.33, V.29 — P2DET V.32 Originate — ACDET V.32 Answer — AADET V.22 bis — S1DET
RTDIS	1:8:2	0	**Receiver Training Disable.** When control bit RTDIS is a 1, the receiver is prevented from recognizing a training sequence and entering the training state. When RTDIS is a 0, receiver training is enabled. (V.33, V.29)
RTH	1:13:2,3	0	**Receiver Threshold.** The RTH control bits select the receiver energy detector threshold according to the following codes: RTH — RLSD ON — RLSD OFF 0 — −43 dBm — −48 dBm 1 — −33 dBm — −38 dBm 2 — −26 dBm — −31 dBm 3 — −16 dBm — −21 dBm
RTRN	0:8:1	0	**Retrain.** When the modem is in data mode, and control bit RTRN is set to a 1, a retrain sequence is initiated. RTRN resets to a 0 as soon as the initiation is acknowledged. Fall-back or fall-forward retrains may be accomplished in V.33, V.32 or V.22 bis modes as follows: Change the Transmitter Configuration Register (TCONF) to the required configuration code. Note that the mode cannot be changed, only the data rate within a given mode. (For example, it is not possible to fall-back from V.32 to V.22 bis.) **Do not** set the NEWC bits in either the transmitter (NEWC0) or receiver chip 1 (NEWC1) and do not change the receiver configuration register (RCONF) code. Ensure that ARC0 and ARC1 bits are set to a 1. If it is desired to fall-back or fall-forward to one of the proprietary V.32 configurations, then also ensure that EARC0 and EARC1 are set to a 1. Finally, set the RTRN bit to a 1. If the remote modem can operate at the requested rate, the receiver configuration will be changed by the modem to reflect the new rate **after the retrain is completed**. If the remote modem cannot operate at the new rate, then no rate change will take place during the retrain and the transmitter configuration register will automatically revert back to its original configuration. If the modem reconfigures from V.22 bis 2400 bps to V.22 1200 bps during a handshake or as a result of a retrain, the TCONF and RCONF registers will contain the hex number 82.
RTS	0:8:0	0	When control bit RTS is a 1, the modem transmits any data on TXD when CTS becomes active. In V.33 mode, when control bit RTS is set to 1, the modem transmits the training sequence before activating CTS. In V.22 bis constant carrier and V.32 modes, RTS controls data transmission and DTR controls the carrier. For ease of use, RTS can be turned ON at the same time as DTR. In V.22 bis controlled carrier mode, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, the modem then transmits 270 ms of scrambled 1s before turning CTS ON. The RTS bit parallels the operation of the $\overline{RTS}$ hardware control input. These inputs are ORed by the modem. (See descriptions of CTS and DTR bits)
SADET	1:D:2	—	**Scrambled Alternating Sequence Detector.** When set to a 1, status bit SADET indicates that scrambled alternating data is being received. This bit is intended to be used for the automatic rate change sequence. (See ARC0 and ARC1) This bit is reset to 0 at the end of the alternating sequence. (V.22 bis)
SCR1	1:D:4	—	**Scrambled Ones Detector.** When set to a 1, status bit SCR1 indicates that V.22 bis scrambled 1s have been detected during handshake. This bit is reset to 0 at the end of the scrambled 1s sequence. (V.22 bis)
SDET	1:C:3	—	**S Detector.** When set to a 1, status bit SDET indicates that a V.32 S sequence has been detected. This bit is reset to a 0 by the modem at the end of the S sequence. (V.32)
SEPT	0:2:1	0	**Short Echo Protector Tone.** When control bit SEPT is a 1, the echo protector tone duration is 30 ms; when a 0, the echo protector tone duration is 185 ms. (V.33, V.29)

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
SDIS	0:3·2	0	**Scrambler Disable.** When control bit SDIS is a 1, the transmitter scrambler circuit is disabled; when a 0, the scrambler circuit is enabled. (V.32,V.22 bis.)
SHAP0	0:2:3	0	**Transmitter Shaping Filter Select.** When control bit SHAP0 is a 0, the transmit spectrum is shaped by a square root of 12.5% raised cosine filter; when a 1, the transmit spectrum is shaped by a square root of 20% raised cosine filter. NEWC0 must be set after changing the SHAP0 bit. (V.33, V.32, V.29) The 20% option is provided for use in the V.29 configurations when communicating with other modems which use the 20% filter. The 12.5% option is for communicating over a channel which has a known narrow bandwidth. This option should be used when a secondary channel is added to the modem.
SHAP1	1:2:3	0	**Receiver Shaping Filter Select.** When control bit SHAP1 is a 0, the receiver low pass filter is square root of 12.5% raised cosine; when a 1, the low pass filter is square root of 20% raised cosine. NEWC1 must be set after changing the SHAP1 bit. (V.33, V.32, V.29) The 20% option is provided for use in the V.29 configurations when communicating with other modems which use the 20% filter. The 12.5% option is for communicating over a channel which has a known narrow bandwidth. This option should be used when a secondary channel is added to the modem.
SNDET	1:C:2	—	**S Negative Detector.** When set to a 1, status bit SNDET indicates that a V.32 $\overline{S}$ sequence has been detected. This bit is reset to a 0 at the end of the $\overline{S}$ sequence. (V.32)
SPEED	1:E:0–2	—	**Speed Indication.** The SPEED status bits indicate the receiver's data rate at the completion of a handshake. Data Rate / SPEED (Hex): 1200 / 2; 2400 / 3; 4800 / 4; 9600 / 5; 12000 / 6; 14400 / 7
SQDIS	1:2:6	0	**Square Disable (Tone Detector C).** When control bit SQDIS is a 1, the squarer in front of tone detector C is disabled; when a 0, the squarer is enabled.
STB0	0:6:2	0	**Stop Bit Number Chip 0.** When control bit STB0 is a 0, one stop bit is selected in asynchronous mode in the transmitter; when a 1, two stop bits are selected. This bit must be configured appropriately before the ASYN0 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis)
STB1	1:6:2	0	**Stop Bit Number Chip 1.** When control bit STB1 is a 1, one stop bit is selected in asynchronous mode in the receiver; when a 1, two stop bits are selected. This bit must be configured appropriately before the ASYN1 bit changes from a 0 to a 1 for asynchronous mode. (V.32, V.22 bis)
S1DET	1:D:5	—	**S1 Detector.** When set to a 1, status bit S1DET indicates that a V.22 bis S1 sequence has been detected. This bit is reset to a 0 by the modem at the end of the S1 sequence. (V.22 bis)
TBUFFER	0:0:0–7	00	**Transmitter Buffer/Transmitter Signal Point X.** The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. Parallel data mode is available only in synchronous mode. The data is transmitted bit 0 first and is divided on the following baud boundaries:

	Bits							
Configuration	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
V.33 14400	—	—	Baud 0					
V.33, V.32 12000	—	—	—	Baud 0				
TCM 9600	Baud 1				Baud 0			
TCM 7200	—	—	Baud 1			Baud 0		
V.32 TCM 9600	Baud 1				Baud 0			
V.32 9600	Baud 1				Baud 0			
V.32 4800	Baud 3		Baud 2		Baud 1		Baud 0	
V.32 TCM 7200	—	—	Baud 1			Baud 0		
V.22 bis 2400	Baud 1				Baud 0			
V.22 bis 1200	Baud 3		Baud 2		Baud 1		Baud 0	
V.29 9600	Baud 1				Baud 0			
V.29 7200	—	—	Baud 1			Baud 0		
V.29 4800	Baud 3		Baud 2		Baud 1		Baud 0	

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Memory Location</th><th>Default Value</th><th>Name/Description</th></tr>
<tr><td>TCONF</td><td>0:12:0–7</td><td>31</td><td>Transmitter Configuration. The TCONF control bits select one of the following transmitter configurations:
<table>
<tr><th>Mode</th><th>Data Rate</th><th>TCONF (Hex)</th></tr>
<tr><td>V.33 TCM</td><td>14400</td><td>31</td></tr>
<tr><td>V.33 TCM</td><td>12000</td><td>32</td></tr>
<tr><td>V.33 TCM</td><td>9600</td><td>34</td></tr>
<tr><td>V.33 TCM</td><td>7200</td><td>38</td></tr>
<tr><td>V.32 TCM</td><td>12000</td><td>72</td></tr>
<tr><td>V.32 TCM</td><td>9600</td><td>74</td></tr>
<tr><td>V.32</td><td>9600</td><td>75</td></tr>
<tr><td>V.32</td><td>4800</td><td>71</td></tr>
<tr><td>V.32 TCM</td><td>7200</td><td>78</td></tr>
<tr><td>V.29</td><td>9600</td><td>14</td></tr>
<tr><td>V.29</td><td>7200</td><td>12</td></tr>
<tr><td>V.29</td><td>4800</td><td>11</td></tr>
<tr><td>V.22 bis</td><td>2400</td><td>84</td></tr>
<tr><td>Single Tone</td><td>—</td><td>80</td></tr>
<tr><td>Dual Tone</td><td>—</td><td>83</td></tr>
<tr><td>Dialing</td><td>—</td><td>81</td></tr>
<tr><td colspan="3">When single tone or dual tone mode is selected, the modem transmits one or two tones respectively. The tone frequencies are host programmable in DSP RAM. Single tone transmit uses the Dual Tone 1 frequency and level.</td></tr>
</table></td></tr>
<tr><td>TDAE</td><td>1:2:7</td><td>1</td><td>Tone Detector A Enable. When control bit TDAE is a 1, tone detector A is enabled; when a 0, tone detector A is disabled. This bit only has an effect when DATA1 bit is a 1 and the receiver is in asynchronous mode or V.32 12000 bps.</td></tr>
<tr><td>TLVL</td><td>0:13:4–7</td><td>0</td><td>Transmit Level. The TLVL code selects the transmitter analog output level at the TXA pin as follows:
<table>
<tr><th>TLVL Code (Hex)</th><th>TX Output Level (dBm ±0.5 dB)</th></tr>
<tr><td>0</td><td>–0.5</td></tr>
<tr><td>1</td><td>–1.5</td></tr>
<tr><td>2</td><td>–2.5</td></tr>
<tr><td>3</td><td>–3.5</td></tr>
<tr><td>4</td><td>–4.5</td></tr>
<tr><td>5</td><td>–5.5</td></tr>
<tr><td>6</td><td>–6.5</td></tr>
<tr><td>7</td><td>–7.5</td></tr>
<tr><td>8</td><td>–8.5</td></tr>
<tr><td>9</td><td>–9.5</td></tr>
<tr><td>A</td><td>–10.5</td></tr>
<tr><td>B</td><td>–11.5</td></tr>
<tr><td>C</td><td>–12.5</td></tr>
<tr><td>D</td><td>–13.5</td></tr>
<tr><td>E</td><td>–14.5</td></tr>
<tr><td>F</td><td>–15.5</td></tr>
</table>
The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.</td></tr>
<tr><td>TM</td><td>0:F:2</td><td>—</td><td>Test Mode. When set to a 1, status bit TM indicates that the modem has completed the handshake and is in the Loop 3 or RDL test mode. (V.22 bis)</td></tr>
<tr><td>TOD</td><td>2:4:1</td><td>0</td><td>Train On Data. When set to a 1, control bit TOD enables the train-on-data algorithm to converge the equalizer if the signal quality degrades. A BER of 10^{-3} for 0.5 seconds initiates the train-on-data. When TOD is a 1, the modem is still able to recognize an incoming training sequence. (V.33, V.32, V.29)</td></tr>
<tr><td>TONEA</td><td>1:B:7</td><td>—</td><td>Tone A Detected. When set to a 1, status bit TONEA indicates that energy is present on the line within the tone detector A passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.</td></tr>
</table>

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
TONEB	1:B:6	—	**Tone B Detected.** When set to a 1, status bit TONEB indicates that energy is present on the line within the tone detector B passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	1:B:5	—	**Tone C Detected.** When set to a 1, status bit TONEC indicates that energy is present on the line within the tone detector C passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM. The TONEC filter is preceded by a squarer in order to facilitate detection of difference tones. This squarer may be disabled with the SQDIS bit (see SQDIS bit).
TPDM	0:8:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is a 1, the transmitter accepts data for transmission from the TBUFFER (0:0) rather than the TXD input.
TSPA	0:5:0	0	**Transmitter Signal Point Activate.** When control bit TSPA is a 1, the transmitter uses the signal points X and Y directly from registers TSPX (0:0) and TSPY (0:1). The transmitter data input, TBUFFER and TXD, are ignored. When TSPA is a 0, the transmitter accepts data for transmission from the TBUFFER or the TXD input
TSPX	0:0:0–7	00	**Transmitter Signal Point X.** When TSPA is a 1, register 0:0 is used to transmit the in-phase (X) coordinate of the transmitted signal point (TSPX).
TSPY	0·1·0–7	00	**Transmitter Signal Point Y.** When TSPA is a 1, register 0:1 is used to transmit the quadrature (Y) coordinate of the transmitted signal point (TSPY).
TTDIS	0:5:2	0	**Transmitter Training Disable.** When control bit TTDIS is a 1, the transmitter does not generate the training sequence at the start of transmission. With training disabled, the RTS/CTS delay is less than two baud times. (V.33, V 29)
TXCLK	0:13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock. **TXCLK** — **Transmit Clock** 0 — Internal 2 — External (XTCLK) 3 — Slave ($\overline{\text{RDCLK}}$) When the external clock is chosen, the host supplied clock must be connected to the XTCLK input pin The external clock will then be reflected at the TDCLK output pin. When the slave clock is chosen, the transmitter clock (TDCLK) is phase locked to the receiver clock ($\overline{\text{RDCLK}}$).
TXSQ	0:5:4	0	**Transmitter Squelch.** When control bit TXSQ is a 1, the transmitter analog output is squelched. All other transmitter functions continue as normal. When TXSQ is a 0, the transmitter output functions normally. This bit is useful in 2-wire configurations where it is necessary to measure the spectrum and transmit level of a transmitter. Setting the TXSQ bit to a 1 turns off the transmitter so that only one of the two carriers is present. After TXSQ is set to a 0, a retrain should be sent to reestablish the data transfer.
U1DET	1:D:3	—	**Unscrambled 1s Detector.** When set to a 1, status bit U1DET indicates that V.22 bis unscrambled 1s sequence has been detected This bit is reset to a 0 by the modem at the end of the unscrambled 1s sequence U1DET is not active when DATA1 is a 0. (V 22 bis)
WDSZ0	0:6:0,1	0	**Data Word Size Chip 0.** The WDSZ0 field sets the number of data bits per character in asynchronous mode in the transmitter as follows (V 32, V 22 bis): **Data Bits/Character** — **WDSZ0 (Hex)** 5 — 0 6 — 1 7 — 2 8 — 3 This bit must be configured appropriately before the ASYN0 bit changes from a 0 to a 1 for asynchronous mode.
WDSZ1	1:6:0,1	0	**Data Word Size Chip 1.** The WDSZ1 field sets the number of data bits per character in asynchronous mode in the receiver as follows (V.32, V.22 bis): **Data Bits/Character** — **WDSZ1 (Hex)** 5 — 0 6 — 1 7 — 2 8 — 3 This bit must be configured appropriately before the ASYN1 bit changes from a 0 to a 1 for asynchronous mode.

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
XACC0	0:1D:7	0	**X RAM Access Enable Chip 0.** When control bit XACC0 is a 1, DSP chip 0 accesses the X RAM associated with the address in XADD0 and the XCR0 bit. XWT0 determines if a read or write is performed. The DSP resets XACC0 to a 0 upon RAM access completion.
XACC1	1:1D:7	0	**X RAM Access Enable Chip 1.** When control bit XACC1 is a 1, DSP chip 1 accesses the X RAM associated with the address in XADD1 and the XCR1 bit. XWT1 determines if a read or write is performed. The DSP resets XACC1 to a 0 upon RAM access completion.
XACC2	2:1D:7	0	**X RAM Access Enable Chip 2.** When control bit XACC2 is a 1, DSP Chip 2 accesses the X RAM associated with the address in XADD2 and the XCR2 bit. XWT2 determines if a read or write is performed. The DSP resets XACC2 to a 0 upon RAM access completion.
XADD0	0:1C:0–7	00	**X RAM Address Chip 0.** XADD0 contains the X RAM address used to access DSP chip 0's X Data RAM (XCR0 = 0) or X Coefficient RAM (XCR0 = 1) via the X RAM Data LSB and MSB registers (0:18 and 0:19, respectively) (See Table 9.)
XADD1	1:1C:0–7	00	**X RAM Address Chip 1.** XADD1 contains the X RAM address used to access DSP chip 1's X Data RAM (XCR1 = 0) or X Coefficient RAM (XCR1 = 1) via the X RAM Data LSB and MSB registers (1:18 and 1:19, respectively) (See Table 9.).
XADD2	2:1C:0–7	00	**X RAM Address Chip 2.** XADD2 contains the X RAM address used to access DSP chip 2's X Data RAM (XCR2 = 0) or X Coefficient RAM (XCR2 = 1) via the X RAM Data LSB and MSB registers (2:18 and 2:19, respectively). (See Table 9.)
XCRD0	0:1D:2	0	**X RAM Continuous Read Chip 0.** When control bit XCRD0 is a 1, bits XACC0 and XWT0 are overridden and an X RAM read from chip 0 is performed every sample from the location addressed by XADD0 (see DSP RAM Access).
XCRD1	1:1D:2	0	**X RAM Continuous Read Chip 1.** When control bit XCRD1 is a 1, bits XACC1 and XWT1 are overridden and an X RAM read from chip 1 is performed every sample from the location addressed by XADD1 (see DSP RAM Access)
XCRD2	2:1D:2	0	**X RAM Continuous Read Chip 2.** When control bit XCRD2 is a 1, bits XACC2 and XWT2 are overridden and an X RAM read from chip 2 is performed every baud from the location addressed by XADD2 (see DSP RAM Access).
XCR0	0:1D:0	0	**X Coefficient RAM Select Chip 0.** When control bit XCR0 is a 1, XADD0 applies to DSP chip 0's X Coefficient RAM. When XCR0 is a 0, XADD0 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 9).
XCR1	1:1D:0	0	**X Coefficient RAM Select Chip 1.** When control bit XCR1 is a 1, XADD1 applies to DSP chip 1's X Coefficient RAM. When XCR1 is a 0, XADD1 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 9).
XCR2	2:1D:0	0	**X Coefficient RAM Select Chip 2.** When control bit XCR2 is a 1, XADD2 applies to DSP chip 2's X Coefficient RAM. When XCR2 is a 0, XADD2 applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 9).
XDAL0	0:18:0–7	00	**X RAM Data LSB Chip 0.** XDAL0 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAL1	1:18:0–7	00	**X RAM Data LSB Chip 1.** XDAL1 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAL2	2:18:0–7	00	**X RAM Data LSB Chip 2.** XDAL2 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2
XDAM0	0:19:0–7	00	**X RAM Data MSB Chip 0.** XDAM0 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
XDAM1	1:19:0–7	00	**X RAM Data MSB Chip 1.** XDAM1 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAM2	2:19:0–7	00	**X RAM Data MSB Chip 2.** XDAM2 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2.
XWT0	0:1D:1	0	**X RAM Write Chip 0.** When XWT0 is a 1 and XACC0 is set to a 1, DSP chip 0 copies data from the X RAM Data registers (0:18 and 0:19) into the X RAM location addressed by XADD0 and XCR0. When control bit XWT0 is a 0 and XACC0 is set to a 1, DSP chip 0 reads X RAM at the location addressed by XADD0 and XCR0. The read data is stored into the X RAM Data registers (0:18 and 0:19).
XWT1	1:1D:1	0	**X RAM Write Chip 1.** When XWT1 is a 1 and XACC1 is set to a 1, DSP chip 1 copies data from the X RAM Data registers (1:18 and 1:19) into the X RAM location addressed by XADD1 and XCR1. When control bit XWT1 is a 0 and XACC1 is set to a 1, DSP chip 1 reads X RAM at the location addressed by XADD1 and XCR1. The read data is stored into the X RAM Data registers (1:18 and 1:19).
XWT2	2:1D:1	0	**X RAM Write Chip 2.**When XWT2 is a 1 and XACC2 is set to a 1, DSP chip 2 copies data from the X RAM Data registers (2:18 and 2:19) into the X RAM location addressed by XADD2 and XCR2. When control bit XWT2 is a 0 and XACC2 is set to a 1, the DSP chip 2 reads X RAM at the location addressed by XADD2 and XCR2. The read data is stored in the X RAM Data registers (2:18 and 2:19).
YACC0	0:1B:7	0	**Y RAM Access Enable Chip 0.** When control bit YACC0 is a 1, DSP chip 0 accesses the Y RAM associated with the address in YADD0 and the YCR0 bit. YWT0 determines if a read or write is performed. The DSP resets YACC0 to a 0 upon RAM access completion.
YACC1	1:1B:7	0	**Y RAM Access Enable Chip 1.** When control bit YACC1 is a 1, DSP chip 1 accesses the Y RAM associated with the address in YADD1 and the YCR1 bit. YWT1 determines if a read or write is performed. The DSP resets YACC1 to a 0 upon RAM access completion.
YACC2	2:1B:7	0	**Y RAM Access Enable Chip 2.** When control bit YACC2 is a 1, DSP chip 2 accesses the Y RAM associated with the address in YADD2 and the YCR2 bit. YWT2 determines if a read or write is performed. The DSP sets YACC2 to a 0 upon RAM access completion.
YADD0	0:1A:0–7	00	**Y RAM Address Chip 0.** YADD0 contains the Y RAM address used to access DSP chip 0's Y Data RAM (YCR0 = 0) or Y Coefficient RAM (YCR0 = 1) via the Y RAM Data LSB and MSB registers (0:16 and 0:17, respectively). (See Table 9.)
YADD1	1:1A:0–7	00	**Y RAM Address Chip 1.** YADD1 contains the Y RAM address used to access DSP chip 1's Y Data RAM (YCR1 = 0) or Y Coefficient RAM (YCR1 = 1) via the Y RAM Data LSB and MSB registers (1:16 and 1:17, respectively). (See Table 9.)
YADD2	2:1A:0–7	00	**Y RAM Address Chip 2.** YADD2 contains the Y RAM address used to access DSP chip 2's Y Data RAM (YCR2 = 0) or Y Coefficient RAM (YCR2 = 1) via the Y RAM Data LSB and MSB registers (2:16 and 2:17, respectively). (See Table 9.)
YCRD0	0:1B:2	0	**Y RAM Continuous Read Chip 0.** When control bit YCRD0 is a 1, bits YACC0 and YWT0 are overridden and a Y RAM read from chip 0 is performed every sample from the location addressed by YADD0 (see DSP RAM Access).
YCRD1	1:1B:2	0	**Y RAM Continuous Read Chip 1.** When control bit YCRD1 is a 1, bits YACC1 and YWT1 are overridden and a Y RAM read from chip 1 is performed every sample from the location addressed by YADD1 (see DSP RAM Access).
YCRD2	2:1B:2	0	**Y RAM Continuous Read Chip 2.** When control bit YCRD2 is a 1, bits YACC2 and YWT2 are overridden and a Y RAM read from chip 2 is performed every baud from the location addressed by YADD2 (see DSP RAM Access).

Table 8. R1496DP Interface Memory Bit Definitions (Continued)

Mnemonic	Memory Location	Default Value	Name/Description
YCR0	0:1B:0	0	**Y Coefficient RAM Select Chip 0.** When control bit YCR0 is a 1, YADD0 applies to DSP chip 0's Y Coefficient RAM. When YCR0 is a 0, YADD0 applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 9).
YCR1	1:1B:0	0	**Y Coefficient RAM Select Chip 1.** When control bit YCR1 is a 1, YADD1 applies to DSP chip 1's Y Coefficient RAM When YCR1 is a 0, YADD1 applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 9).
YCR2	2:1B:0	0	**Y Coefficient RAM Select Chip 2.** When control bit YCR2 is a 1, YADD2 applies to the DSP chip 2's Y Coefficient RAM. When YCR2 is a 0, YADD2 applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 9).
YDAL0	0:16:0–7	00	**Y RAM Data LSB Chip 0.** YDAL0 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAL1	1:16:0–7	00	**Y RAM Data LSB Chip 1.** YDAL1 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAL2	2:16:0–7	00	**Y RAM Data LSB Chip 2.** YDAL2 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM location in DSP chip 2.
YDAM0	0:17:0–7	00	**Y RAM Data MSB Chip 0.** YDAM0 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAM1	1:17:0–7	00	**Y RAM Data MSB Chip 1.** YDAM1 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAM2	2:17:0–7	00	**Y RAM Data MSB Chip 2.** YDAM2 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 2.
YWT0	0:1B:1	0	**Y RAM Write Chip 0.** When YWT0 is a 1 and YACC0 is set to a 1, DSP chip 0 copies data from the Y RAM Data registers (0:16 and 0:17) into the Y RAM location addressed by YADD0 and YCR0. When control bit YWT0 is a 0 and YACC0 is set to a 1, DSP chip 0 reads Y RAM at the location addressed by YADD0 and YCR0. The read data is stored into the Y RAM Data registers (0:16 and 0:17).
YWT1	1.1B:1	0	**Y RAM Write Chip 1.** When YWT1 is a 1 and YACC1 is set to a 1, DSP chip 1 copies data from the Y RAM Data registers (1.16 and 1:17) into the Y RAM location addressed by YADD1 and YCR1. When control bit YWT1 is a 0 and YACC1 is set to a 1, DSP chip 1 reads Y RAM at the location addressed by YADD1 and YCR1. The read data is stored into the Y RAM Data registers (1:16 and 1:17).
YWT2	2:1B:1	0	**Y RAM Write Chip 2.** When YWT2 is a 1 and YACC2 is set to a 1, DSP chip 2 copies data from the Y RAM Data registers (2:16 and 2:17) into the Y RAM location addressed by YADD2 and YCR2. When control bit YWT2 is a 0 and YACC2 is set to a 1, DSP chip 2 reads Y RAM at the location addressed by YADD2 and YCR2 The read data is stored in the Y RAM Data registers (2:16 and 2:17).

DSP RAM ACCESS

GENERAL

DSP RAM Organization

Each DSP contains a 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously.

Interface Memory Access to DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in DSP interface memory RAM Access registers by the host, in conjunction with the data or coefficient RAM bit (e.g., XCR0) determines the DSP RAM address for data access.

One or two 16-bit words are transferred between DSP RAM and DSP interface memory once each device cycle. The transmitter device and the receiver sample rate device operate at the 9600 Hz sample rate. The receiver baud rate device operates at the baud rate of the selected data rate.

Two RAM access bits in each DSP interface memory tell the DSP to access the X RAM and/or Y RAM. For example, the transfer is initiated in the transmitter by the host setting the XACC0 and/or the YACC0 bit(s). The transmitter tests these bits each sample period. The receiver tests XACC1 and YACC1 each sample period and XACC2 and YACC2 each baud period.

The following procedure applies to DSP RAM access in the transmitter device. The procedure to access DSP RAM in the receiver devices is the same with the exception of the RAM access bit names.

DSP RAM Write Procedure (Transmitter)

Before writing to DSP interface memory, set XACC0 and YACC0 to a 0. Set XWT0 and/or YWT0 to a 1 to inform the DSP that a RAM write will occur when XACC0 and/or YACC0 is set to a 1. Load the RAM address into X RAM Address and/or Y RAM Address registers; then set XCR0 and/or YCR0 appropriately. Write the desired data into the interface memory RAM Data registers then set XACC0 and/or YACC0 to a 1 to signal the DSP to perform the RAM write. When the DSP has transferred the contents of the interface memory RAM Data registers into RAM, the DSP sets the XACC0 and/or the YACC0 bit to a 0 and the NEWS0 bit to a 1 to indicate DSP RAM write completion.

If the NSIE0 bit is a 1, $\overline{IRQ}$ is also asserted and NSIA0 is set to a 1 when NEWS0 is set to a 1. NSIA0 is cleared by writing a 0 into the NEWS0 bit, which also causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

DSP RAM Read Procedure (Transmitter)

Before reading from DSP interface memory, set XACC0 and YACC0 to a 0. Set XWT0 and/or YWT0 to a 0 to inform the DSP that a RAM read will occur when XACC0 and/or YACC0 is set to a 1. Load the RAM Address code into X RAM Address and/or Y RAM address register; then set XCR0 and/or YCR0 appropriately. Set XACC0 and/or YACC0 to a 1 to signal the DSP to perform the RAM read. When the DSP has transferred the contents of RAM into the interface memory RAM Data registers, the DSP sets the XACC0 and/or the YACC0 bit to a 0 and the NEWS0 bit to a 1 to indicate DSP RAM read completion.

If the NSIE0 bit is a 1, $\overline{IRQ}$ is also asserted when NEWS0 is set to a 1. When $\overline{IRQ}$ is asserted, NSIA0 goes to a 1 to inform the host that setting of the NEWS0 bit was the source of the interrupt. NSIA0 is cleared by writing a 0 into the NEWS0 bit, which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

CONTINUOUS RAM READ PROCEDURE

There are several diagnostic parameters that the host may wish to read every sample or every baud period. One example of this is the EQM (Eye Quality Monitor) value in chip 2 (receiver baud). The host may avoid having to set the XACC2/YACC2 bit every baud period by using the continuous read feature. Setting XCRD2 to a 1 overrides both XACC2 and XWT2 bits, while setting YCRD2 to a 1 overrides both YACC2 and YWT2 bits.

The RAM address registers 1A and 1C and the XCR2 and YCR2 bits must be set up as described in the general DSP RAM read procedure. Then set XCRD2 and YCRD2 to 1. The chip 2 DSP will then transfer data to the interface memory every baud. The NEWS2 bit is set as described in the general DSP RAM read procedure.

The transmitter (chip 0) and receiver (chip 1) can be similarly treated, however, data will be transferred every sample by each device.

Table 9 provides the RAM functions, address codes, and registers.

SOFTWARE INTERFACE CONSIDERATIONS

INTERRUPT REQUEST HANDLING

DSP interface memory registers registers 00, 1E and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER)/Rate Sequence Code LSB (RSEQL) in the receiver sample rate device and the Transmit Buffer (TBUFFER)/Transmit Signal Point X (TSPX) in the transmitter device. Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits. When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using $\overline{IRQ}$) or by being interrupted by $\overline{IRQ}$. When an interrupt enable bit is a 1, $\overline{IRQ}$ is asserted and the appropriate interrupt active bit set to a 1 when the corresponding interrupt condition occurs.

The basic sources for $\overline{IRQ}$ generation are status change detected, configuration change implemented, receive buffer full and transmit buffer empty. Each source is individually maskable. Table 10 identifies the interrupt sources and describes the interrupt clearing procedures.

Table 9. R1496DP RAM Addresses

No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imaginary Part (Y)	CR Bit[1]	No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imaginary Part (Y)	CR Bit[1]
1	Transmitter Compromise Equalizer Coefficients:					26	Tone Detector A Bandpass Filter Coefficients	1	26	—	1
	First Tap	0	5B	—	1	27	Tone Detector B Bandpass Filter Coefficients	1	2C	—	1
	Last Tap	0	34	—	1						
2	V.33/V.32 Rate Sequence	0	93	—	1	28	Tone Detector C Bandpass Filter Coefficients	1	32	—	1
3	DTMF Tone Duration	0	9A	—	1						
4	DTMF Interdigit Delay	0	1A	—	1	29	RLSD On-to-Off Threshold	1	07	—	1
5	DTMF Low Band Power Level	0	19	—	1	30	RLDS Off-to-On Threshold	1	01	—	0
6	DTMF High Band Power Level	0	99	—	1	31	Receiver Chip 1 New Status Bit (NEWS1)				
7	Pulse Relay Make Time	0	9C	—	1		Masking Register for 1:A and 1:B	1	9B	—	1
8	Pulse Relay Break Time	0	1C	—	1		Masking Register for 1:C and 1:D	1	9C	—	1
9	Pulse Interdigit Delay	0	1B	—	1		Masking Register for 1:E and 1:F	1	9D	—	1
10	Transmitter Output Level Gain Constant	0	99	—	0	32	Received Signal Samples	1	03	—	0
11	Dual Tone 1 Frequency	0	87	—	0	33	Demodulator Output	1	04	84	0
12	Dual Tone 2 Frequency	0	90	—	1	34	Low Pass Filter Output	1	00	80	0
13	Dual Tone 1 Power Level	0	02	—	0	35	Average Energy	1	02	—	0
14	Dual Tone 2 Power Level	0	82	—	0	36	AGC Gain Word	1	01	—	1
15	Transmitter New Status Bit (NEWS0) Masking Register for 0:E and 0:F	0	11	—	1	37	Timing Recovery Update	1	25	—	0
						38	Equalizer Input	2	18	98	0
16	Total Span of Echo Canceller	0	9D	—	0	39	Equalizer Tap Coefficients:				
17	Echo Canceller Dividing Point	0	A0	—	0		First Tap	2	18	98	1
18	Far End Echo Canceller Center Tap Position	0	24	—	0		Last Tap	2	47	C7	1
						40	Unrotated Equalizer Output	2	01	81	0
19	Echo Canceller Update Coefficient (Training Mode)	0	24	—	1	41	Rotated Equalizer Output (Received Points)	2	02	82	1
						42	Decision Points (Ideal Points)	2	02	82	0
20	Echo Canceller Update Coefficient (Data Mode)	0	A4	—	1	43	Equalizer Error	2	03	83	0
						44	Equalizer Rotation Angle	2	87	—	1
21	CTS OFF-to-ON Response Time (RTS–CTS Delay)	0	10	—	1	45	Equalizer Frequency Correction	2	0A	—	1
						46	Eye Quality Monitor (EQM)	2	07	—	1
22	Round Trip Far Echo Delay	0	9E	—	0	47	Maximum Period of Valid Ring Signal	2	17	—	0
23	Echo Canceller Error	0	20	—	0	48	Minimum Period of Valid Ring Signal	2	97	—	0
24	Far End Echo Frequency Offset	0	20	—	1	49	Receiver Chip 2 New Status Bit (NEWS2)	2	7E	—	0
25	Far End Echo Level	0	25	—	0		Masking Register for 2:E and 2:F				

Note: 1. CR corresponds to XCR0, YCR0, XCR1, YCR1, XCR2, or YCR2 depending on the chip number and address code.

Table 10. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
Transmitter (DSP Chip 0)				
NSIA0	NSIE0	NEWS0	New status detected (NEWS0 transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A through 0F	Host writes a 0 into NEWS0 (Clears NSIA0 to a 0)
NCIA0	NCIE0	NEWC0	New transmitter configuration implemented by DSP (NEWC0 transitioned from a 1 to a 0)	Host writes a 0 into NCIE0 (Clears NCIA0 to a 0)
DBIA0	DBIE0	DBA0	Transmitter Data Buffer is empty and can be written (DBA0 transitioned from a 0 to a 1)	Host writes to register 0:0 (TBUFFER/TSPX) (Clears DBA0 and DBIA0 to 0)
Receiver (DSP Chip 1)				
NSIA1	NSIE1	NEWS1	New status detected (NEWS1 transitioned from a 0 to a 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A through 0F	Host writes a 0 into NEWS1 (Clears NSIA1 to a 0)
NCIA1	NCIE1	NEWC1	New receiver configuration or receiver threshold implemented by DSP (NEWC1 transitioned from a 1 to a 0)	Host writes a 0 into NCIE1 (Clears NCIA1 to a 0)
DBIA1	DBIE1	DBA1	Receiver Chip 1 Data Buffer is full and can be read (DBA1 transitioned from a 0 to a 1)	Host reads register 1:0 (RBUFFER/RSEQL) (Clears DBA1 and DBIA1 to 0)
Receiver (DSP Chip 2)				
NSIA2	NSIE2	NEWS2	New status detected (NEWS2 transitioned from a 0 to a 1) a. RAM read or RAM write occurred b. Status bit changed in register 0F	Host writes a 0 into NEWS2 (Clears NSIA2 to a 0)
TBIA2	DBIE2	DBA2	Receiver Chip 2 Data Buffer is full and can be read (DBA2 transitioned from a 0 to a 1)	Host reads register 2:0 (RSPX) (Clears DBA2 and DBIA2 to 0)

AUTO DIAL PROCEDURE

The host auto dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 5). The modem timing accounts for the DTMF tone duration and amplitude, pulse make/break ratio, and interdigit delay. These dialing parameters are host programmable in DSP RAM.

The levels of the high band and low band DTMF tones may be modified by the host in DSP RAM. The level of the high band DTMF tone should be 2 dB greater than the level of the low band DTMF tone.

The auto dialer default parameters are given in Table 11.

Table 11. Auto Dialer Default Parameters

Parameter	Default Value
DTMF Tone Duration	95 ms
DTMF Interdigit Delay	70 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	−4 dBm
DTMF High Band Power Level	−2 dBm
Pulse Relay Make Time	36 ms
Pulse Relay Break Time	64 ms
Pulse Interdigit Delay	750 ms

Dial Digits

Hex	Dial Digits	Tone Pairs	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	#	941	1477

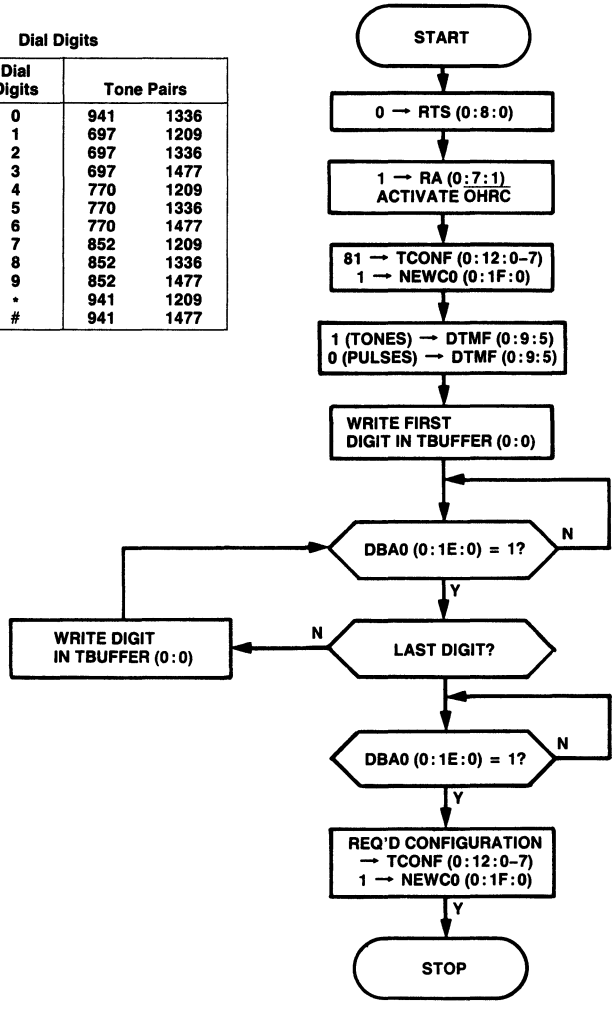


Figure 5. R1496DP Auto Dial Sequence and Dial Digits

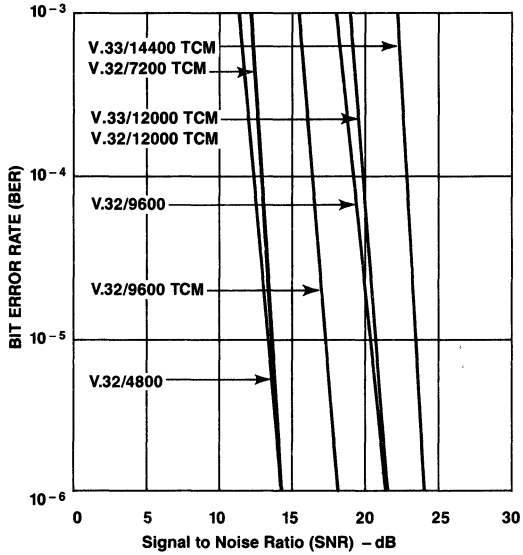
PERFORMANCE

TYPICAL BIT ERROR RATES

Typical modem bit error rate (BER) curves are shown in Figure 6 for a back-to-back connection.

TYPICAL BER TEST SETUP

The BER curves shown in Figure 6 were prepared from data obtained with a TAS 1002 test system.



a. Typical Bit Error Rate (Back-to-Back, –20 dBm Receive Level, T Equalizer, Compromise Equalizer Disabled)

Figure 6. Bit Error Rate Curves

ELECTROMECHANICAL DESIGN CONSIDERATIONS

The area outlined by the analog ground plane in Figure 7 contains components which are sensitive to electromagnetic interference (EMI). When designing the host system, do not position radiating circuitry in the vicinity of this sensitive area. A ground plane adjacent to the modem analog circuitry is recommended.

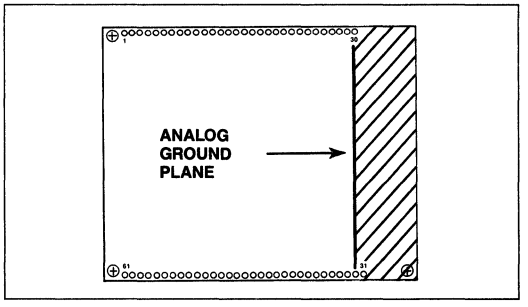


Figure 7. Analog Ground Plane Location

GENERAL SPECIFICATIONS

Table 12. R1496DP Modem Power Requirements

Voltage[1]	Tolerance	Current (Typical) @ 25°C	Current (Maximum) @ 0°C
+5 VDC	±5%	300 mA	585 mA
+12 VDC	±5%	3 mA	6 mA
−12 VDC	±5%	30 mA	36 mA

Note: 1. Input voltage ripple ≤0.1 volts peak-to-peak.

Table 13. R1496DP Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to +70°C (32°F to 158°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 14. R1496DP Modem Mechanical Dimensions

Parameter	Specification
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.228 in. (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0.300 in. (7.62 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.535 ±0.015 in. (13.6 ±0.4 mm), gold plated.
	0.433 ±0.015 in. (11.0 ±0.4 mm), gold plated.
	0.315 ±0.015 in. (8.0 ±0.4 mm), gold plated

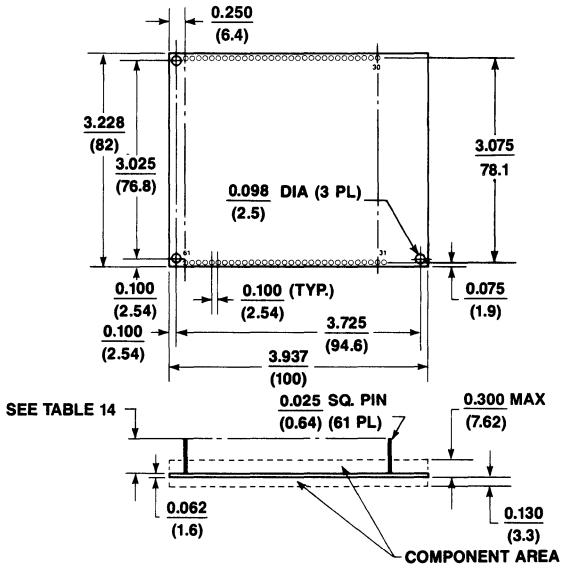


Figure 7. R1496DP Modem Dimensions and Pin Locations

SECTION 3
Image Modems

Product Family Overview 3-2
R24MFX 2400 bps MONOFAX Modem 3-3
R24BKJ 2400 bps V.26 bis Modem 3-19
R48MFX 4800 bps MONOFAX Modem 3-35
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IMAGE MODEMS

LEADING THE WORLD IN FACSIMILE MODEMS

Rockwell is the world leader in the production and sale of highly integrated 9600 bps Group 3 facsimile modems. Because Rockwell has been a key factor in "driving" signal processor (SP) and integrated analog (IA) technology, Rockwell is a major OEM supplier to Japanese facsimile manufacturers.

Rockwell's R96F/FI — a half-duplex, dial-up 9600 bps synchronous modem — is the industry standard for facsimile image transmission. Its compact size, unsurpassed performance and proven reliability have made it the choice of every major facsimile manufacturer since its introduction in 1984. The R96FI is designed for use in Group 3 facsimile machines and is also compatible with Group 2 machines.

In response to market demands for smaller facsimile machines, Rockwell has introduced a line of single device, 64-pin QUIP, facsimile modems. The R96MFX MONOFAX® operating at 9600 bps, the R48MFX MONOFAX operating at 4800 bps, and the R24MFX MONOFAX operating at 2400 bps, are the world's first single device modems designed for emerging personal facsimile market. Rockwell's latest addition to the family is the R96EFX, which incorporates HDLC error detection for higher quality image transmission and V.27ter short train for PC to PC communication applications.

In addition, Rockwell offers single device modems for other image applications. The R48PCJ, a V.27 ter modem with both long and short training options, is designed for applications in personal computer communication, teletex, and intelligent workstations. The R24BKJ, a V.26 bis modem, is designed for applications in banking terminals and intelligent workstations.

Continuing our digital communications leadership role, Rockwell has introduced a 14.4 kbps half-duplex modem, the R144HD, for public switched telephone line operation. In addition to facsimile applications, the R144HD can be used for half-duplex data transmission, which provides a cost effective method of transferring large data blocks. This high performance, ultra-high speed product further establishes Rockwell as the leader in setting standards for the facsimile modem industry.

Model	Data Speed (bps)	Compliance
R24MFX	2400, 300	CCITT V.27 ter Fallback, V.21 Channel 2, T.4
R48MFX	4800, 2400, 300	CCITT V.27 ter, V.21 Channel 2, T.4, T.30
R96MFX	9600, 7200, 4800, 2400, 300	CCITT V.29, V.27 ter, V.21 Channel 2, T.4, T.30, T.3
R96FI	9600, 7200, 4800, 2400, 300	CCITT V.29, V.27 ter, V.21 Channel 2, T.3, T.4, T.30
R96MD	9600, 7200, 4800, 2400, 300	CCITT V.29, V.27 ter, V.21 Channel 2, T.3, T.4, T.30
R144HD	14400, 12000, 9600, 7200, 4800, 2400, 300	CCITT V.33, V.29, V.27 ter w/Short Train, V.21 Channel 2, T.3, T.4, T.30
R24BKJ	2400	CCITT V.26 bis, Bell 201C
R48PCJ	4800, 2400, 300	CCITT V.27 ter Short Train, V.21 Channel 2, T.4, T.30

R24MFX
2400 bps MONOFAX™ Modem

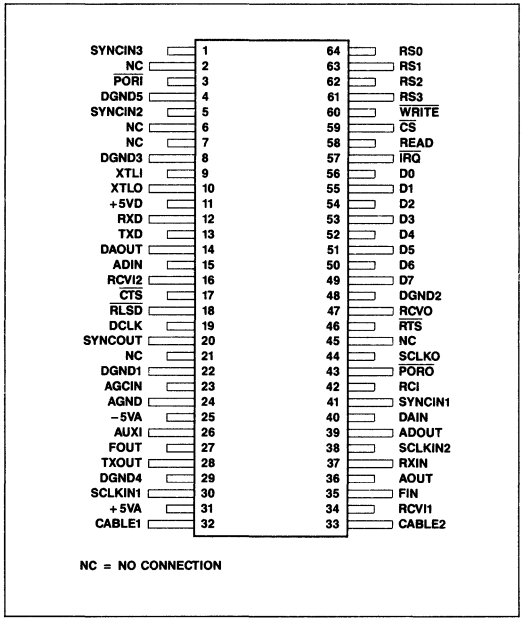
INTRODUCTION

The R24MFX MONOFAX 24 is a synchronous, serial/parallel, 2400 bps modem in a single 64-pin quad in-line package (QUIP). The modem is designed for operation over the public switched telephone network with appropriate line terminations, such as a data access arrangement, provided externally.

The R24MFX satisfies the telecommunications requirements specified in CCITT Recommendation V.27 ter fallback (2400 bps), T.4 and the binary signaling capabilities of Recommendation T.30.

The R24MFX is optimized for use in compact Group 3 facsimile machines. Its small size and low power consumption offer the user flexibility in creating a 2400 bps modem customized for specific packaging and functional requirements.

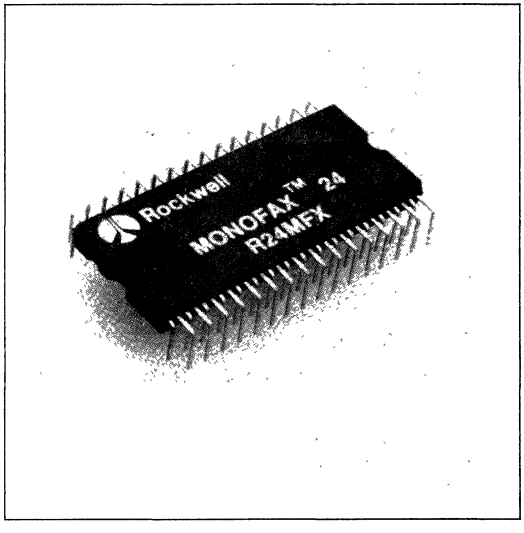
™MONOFAX is a trademark of Rockwell International



R24MFX Pin Assignments

FEATURES

- Single 64-Pin QUIP
- CCITT V.27 ter Fallback, T.30, V.21 Channel 2, T.4
- Group 3 Facsimile Transmission/Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: -43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R24MFX 2400 bps MONOFAX Modem

TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R24MFX can generate single or dual frequency voice band tones up to 3600 Hz with a resolution of 0.11 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Date Rates

Configuration	Parameter	Specification (±0.01%)
V.27	Signaling Rate Data Rate	1200 Baud 2400 bps
V.21	Signaling Rate Data Rate	300 Baud 300 bps

DATA ENCODING

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

At 300 baud, the data stream is 300 bps FSK per CCITT V.21 channel 2.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R24MFX provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	-0.99	-2.39	-3.93
1500	-0.20	-0.65	-1.22
2000	+0.15	+0.87	+1.90
3000	+1.43	+3.06	+4.58

TRANSMITTED DATA SPECTRUM

When operating at 1200 baud, the transmitter spectrum is shaped by a square root of 90% raised cosine filer.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R24MFX incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V,27 ter.

RECEIVE LEVEL

The receiver circuit of the R24MFX satisfies all specified performance requirements for received line signal levels from 0 dBm to -43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R24MFX RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R24MFX provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R24MFX TXOUT pin and the transmitter analog output (TXA). The default level at TXA is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide -1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R24MFX provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Selected data rate of 2400 or 300 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

Three turn-on sequences are generated by the R24MFX, as defined in the following table:

Turn-On Sequences

No.	Bit Rate.	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Time (ms)	Comments
1	300 bps	<14	No Training Sequence
2	2400 bps[2]	943	No Echo Protector Tone
3	2400 bps[2]	1148	Preceded[1] By Echo Protector Tone

Notes:
1. Turn-on sequence 3 is used on lines with protection against talker echo.
2. V.27 ter long training sequence only.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud, followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{\text{RTS}}$ goes false.

CLAMPING

The following clamps are provided with the R24MFX:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{\text{RLSD}}$ is off.
2. *Received Line Signal Detector ($\overline{\text{RLSD}}$).* $\overline{\text{RLSD}}$ is clamped off (squelched) whenever $\overline{\text{RTS}}$ is on.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{\text{CTS}}$)

The time between the off-to-on transition of $\overline{\text{RTS}}$ and the off-to-on transition of $\overline{\text{CTS}}$ is dictated by the length of the training sequence. Response time is 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{\text{CTS}}$ turns on in 14 ms or less.

The time between the on-to-off transition of $\overline{\text{RTS}}$ and the on-to-off transition of $\overline{\text{CTS}}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{\text{RLSD}}$)

$\overline{\text{RLSD}}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{\text{RLSD}}$ off-to-on response time is 674 ± 10 ms. The $\overline{\text{RLSD}}$ on-to-off response time is 10 ± 5 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{\text{RLSD}}$ on threshold or at least 5 dB below the actual $\overline{\text{RLSD}}$ off threshold.

The $\overline{\text{RLSD}}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

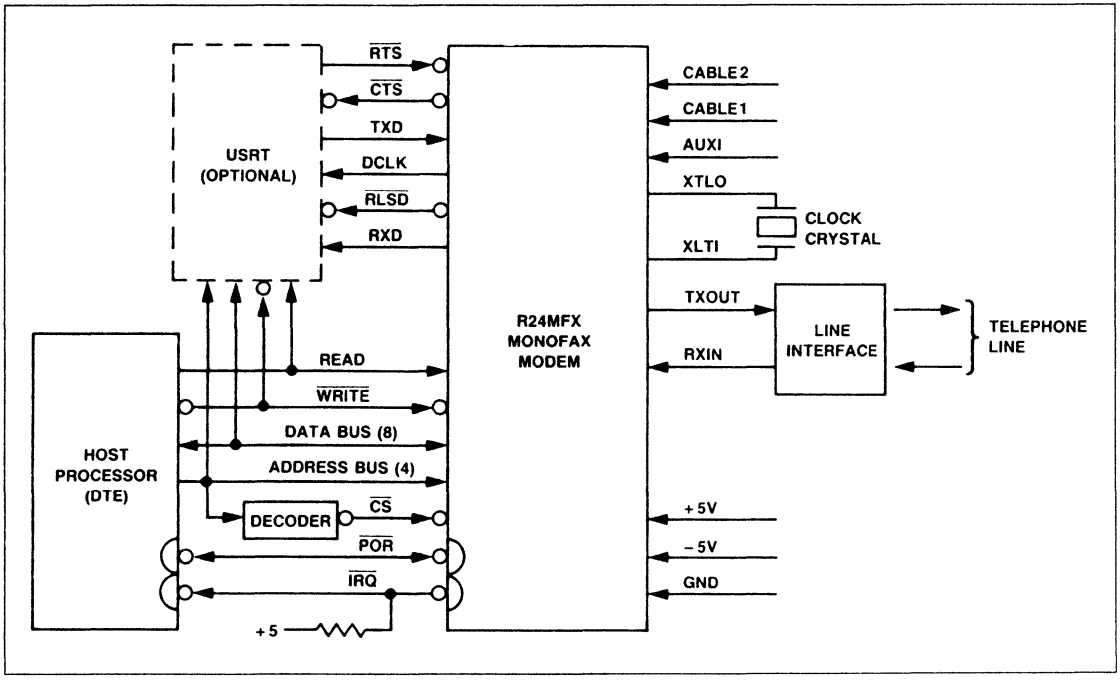
POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	250 mA @ 5.0 Vdc	225 mA @ 5.0 Vdc
−5 Vdc	±5%	25 mA @ −5.0 Vdc	25 mA @ −5.0 Vdc

Note: All voltages must have ripple ≤0.1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in suitable antistatic container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.



R24MFX Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R24MFX Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R24MFX Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0 − F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
$\overline{READ}$	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
$\overline{RLSD}$	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

*R = Required overhead connection; no connection to host equipment.

Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Digital Interface Characteristics

Symbol	Parameter	Units	Type							
			Input			Output			Input/Output	
			IA	IB	IC	OA	OB	OC	I/OA	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current	μA		−240 max.	−240 max.			−240 max.		−260 max.
	(Short Circuit)			−10 min.	−10 min.			−10 min.		−100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

3

Analog Interface Characteristics

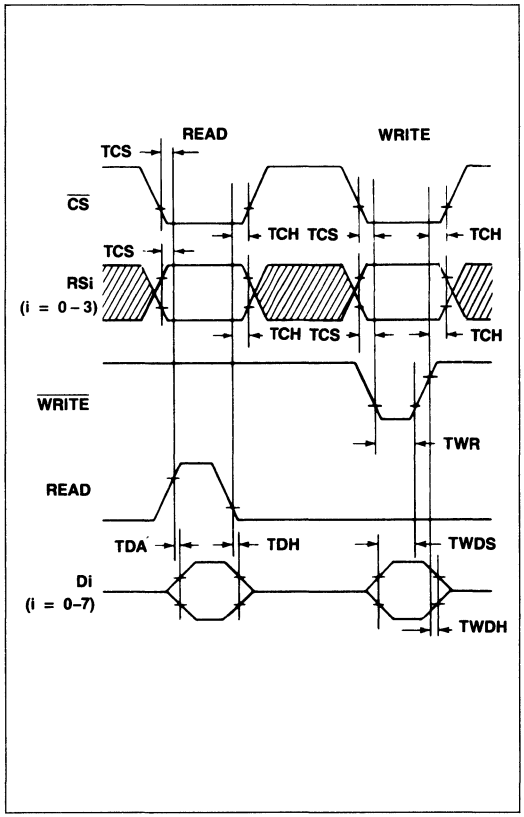
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3.03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726.43/(S+11542.44) and 604 Ω series resistor are required.
RXIN	AB	The receiver input impedance is greater than 1M Ω. An external antialiasing filter with a transfer function of 19533.88/(S+11542.44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 3600 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are: $(-5\ VA - 0.3) \leq V_{IN} \leq (+5\ VA + 0.3)$

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE1	CABLE2	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R24MFX contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R24MFX Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R24MFX is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R24MFX Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

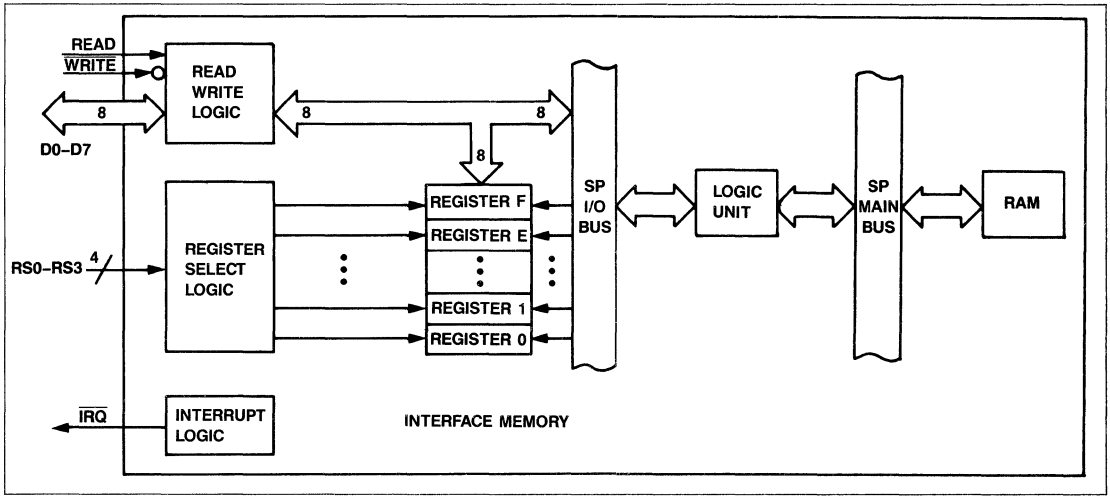
Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

Three configurations are available in the R24MFX modem: V.27, V.21, and Tone. These three configurations are selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is: 0 = V.21, 4 = V.27, and 8 = Tone. All other codes represent invalid states.

When the modem is initialized by power-on-reset, the configuration defaults to V.27. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at either 1200 times per second or 7200 times per second depending on configuration. In V.21, the rate is 7200 times per second. In both V.27 and Tone configuration, the rate is 1200 times per second.



R24MFX Host Processor Interface

R24MFX Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	EPT	TPDM	TDIS	EQSV	EQFZ	—	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	PN	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register / Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection. The transmitter operates in either serial or parallel mode as selected by mode control bit C:5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1. The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R24MFX is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{RTS}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R24MFX Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
CDET	Carrier Detector	8:5	The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{\text{RLSD}}$ and deactivates one baud time after $\overline{\text{RLSD}}$.
CDIE	Channel Data Interrupt Enable	E:6	When set to a one, CDIE enables an $\overline{\text{IRQ}}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.
CDREQ	Channel Data Request	E:5	Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.
CONF	Configuration	D:0-7	The 8-bit field CONF controls the configuration of the modem according to the following table: **Hex Code** — **Configuration** 0 — V.21 4 — V.27 8 — Tone All else — Invalid **Configuration Definitions** *V.21*—The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 Channel 2 modulation system. *Tone*—The modem sends single or dual frequency tones in response to the $\overline{\text{RTS}}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations. *V.27*—The modem operates as specified in CCITT Recommendation V.27 for a 2400 bps data rate.
DDIE	Diagnostic Data Interrupt Enable	E:2	When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.
DDREQ	Diagnostic Data Request	E:0	DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.
DDXL	Diagnostic Data X Least	2:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDXM	Diagnostic Data X Most	3:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDYL	Diagnostic Data Y Least	0:0-7	Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DDYM	Diagnostic Data Y Most	1:0-7	Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
EPT	Echo Protector Tone	C:6	When EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence.
EQFZ	Equalizer Freeze	C:2	When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.
EQSV	Equalizer Save	C:3	When EQSV is a one, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state.
FED	Fast Energy Detector	B:5,6	FED consists of a 2-bit field that indicates the level of received signal according to the following code. **Code** — **Energy Level** 0 — None 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold While receiving a signal, FED normally alternates between Codes 2 and 3.

R24MFX Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct. GHIT returns to zero when the AGC output returns to normal.
IA	Interrupt Active	E:7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level.
PN	Period N	8:3	PN sets to a one at the start of the received PN sequence. PN resets to zero at the start of the receiver data state. PN does not operate when EQFZ (C:2), EQSV (C:3) or TDIS (C:4) is set to one.
RAMA	RAM Access	F:0-7	The RAMA register is written by the host when reading or writing diagnostic data. The RAMA code determines the RAM location with which the diagnostic read or write is performed.
RAMW	RAM Write	C:0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM. RAMW is set to a zero by the host when reading RAM diagnostic data.
RTSP	Request to Send Parallel	C:7	The one state of RTSP begins a transmit sequence. The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem
RXCD	Receiver Channel Data	5:0-7	RXCD is written to by the modem every eight bit times. This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ).
RX	Receive State	B:7	RX is a one when the modem is in the receive state (i.e., not transmitting).
SETUP	Setup	E:3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i.e., when changing CONF (D:0-7).
TDET	Tone Detected	A:7	The one state of TDET indicates reception of a tone. The filter can be retuned by means of the diagnostic write routine.
TDIS	Training Disable	C:4	If TDIS is a one in the receive state, the modem is prevented from entering the training phase If TDIS is a one when $\overline{RTS}$ or RTSP go active, the generation of a training sequence is prevented at the start of transmission.
TPDM	Transmitter Parallel Data Mode	C:5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input.
TXCD	Transmitter Channel Data	4:0-7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one. Data is transmitted as single bits in V.21 or as dibits in V.27 starting with bit 0 or dibit 0,1.

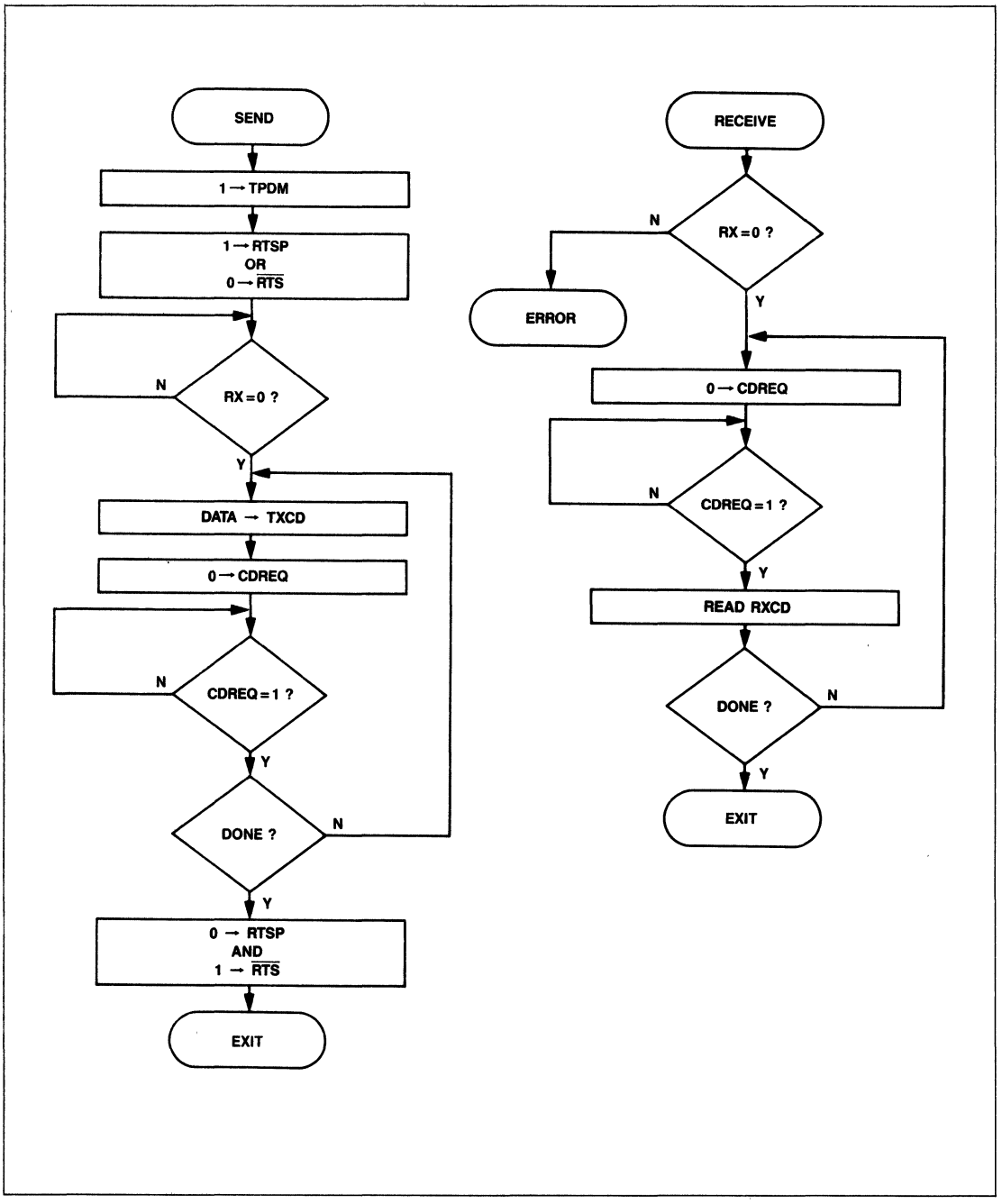
Diagnostic Data Transfer

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R24MFX RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R24MFX Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long. These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

R24MFX RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	B1	2,3
2	Average Power	F2	2,3
3	Receiver Sensitivity	F1	2,3
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	5B	0,1,2,3
6	Equalizer Tap Coefficients	1B-2A	0,1,2,3
7	Unrotated Equalizer Output	6B	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	6C	0,1,2,3
10	Error Vector	6D	0,1,2,3
11	Rotation Angle	87	2,3
12	Frequency Correction	8B	2,3
13	EQM	B0	2,3
14	Alpha (α)	36	0,1
15	Beta One (β_1)	37	0,1
16	Beta Two (β_2)	38	0,1
17	Alpha Prime (α')	39	0,1
18	Beta One Prime (β_1')	3A	0,1
19	Beta Two Prime (β_2')	3B	0,1
20	Alpha Double Prime (α'')	B6	2,3
21	Beta Double Prime (β'')	B7	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1

R24MFX Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 – [(AGC Gain Word/64) × 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$, For –43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code F1
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = $[65.4\ (10^A)]^2/2$ where: A = (P_{OFF} – P_{ON} – 0.5)/20 P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84.

R24MFX Diagnostic Data Scaling

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers. Y ●2 ●1 X ●3 ●4 **Point** X Y 1 1600 1600 2 EA00 1600 3 EA00 EA00 4 1600 EA00
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) × 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) × Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application.
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668. Use a sample rate of 7200 samples per second for all calculations.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 9.1022 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.

POWER-ON INITIALIZATION

When power is applied to the R24MFX, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.27/2400 bps, serial mode, training enabled, echo protector tone enabled, interrupts disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for –43.5 dBm, receiver turn-off threshold set for –47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V.21 type modem, the R24MFX provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm.

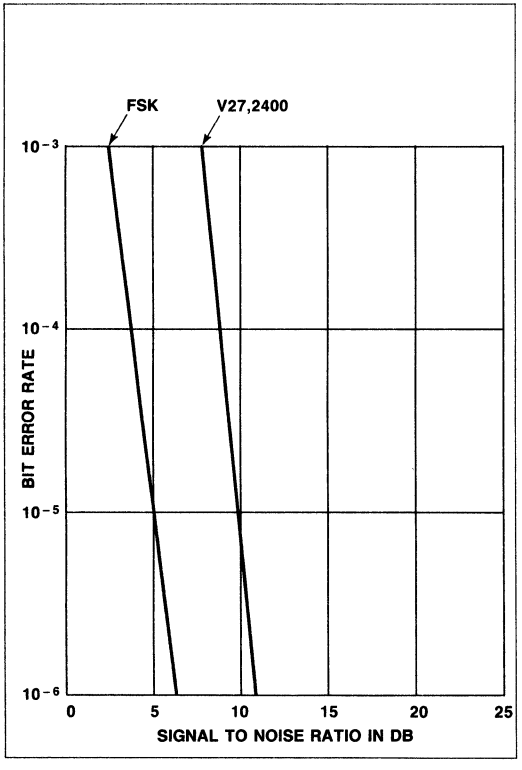
RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R24MFX can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

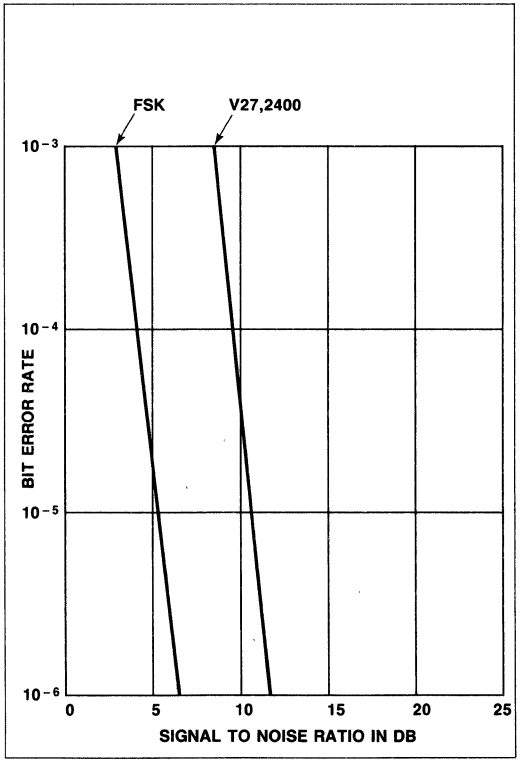
TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

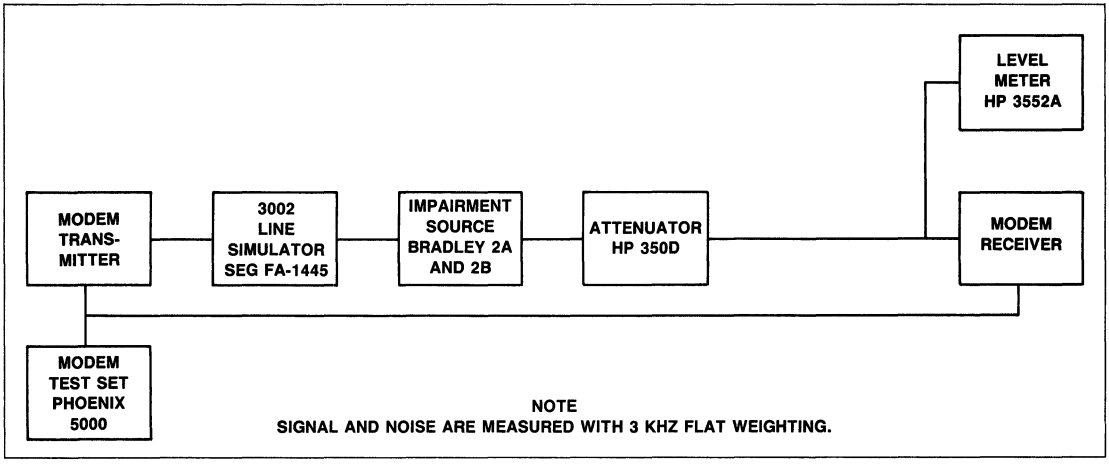


Typical Bit Error Rate (Back-to-Back, Level –20 dBm)



Typical Bit Error Rate (Unconditioned 3002 Line, Level –20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

APPLICATION

Recommended Modem Interface Circuit

The R24MFX is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C2	N511BY100JW	San Fernando/ Wescap
C1	C114C330J2G5CA	Kemet
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434.0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I.T.T
R9	CRB¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R24MFX and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R24MFX, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R24MFX package. Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R24MFX package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R24MFX package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
11. Routing of R24MFX signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
	51	47		
	52	48		
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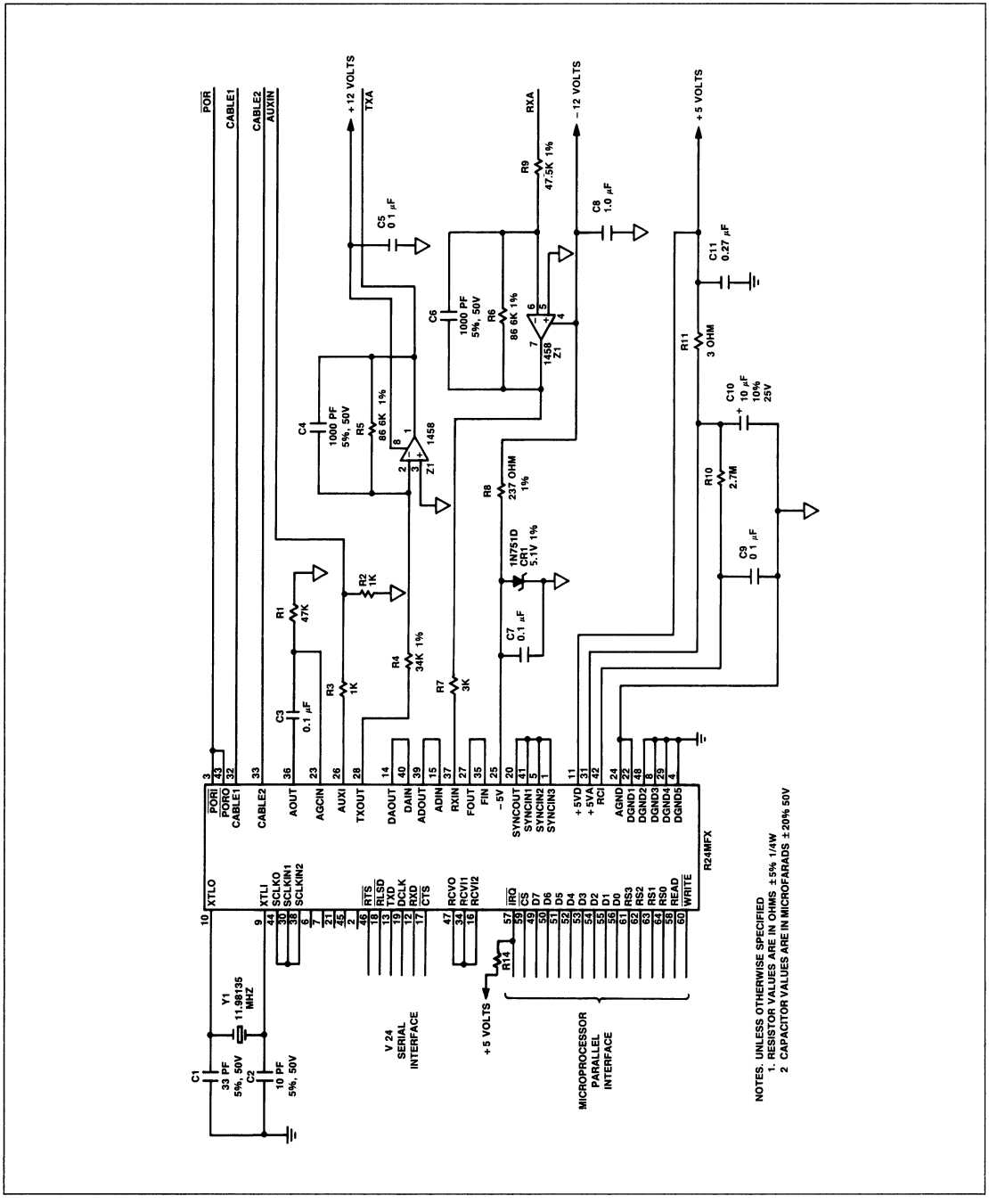
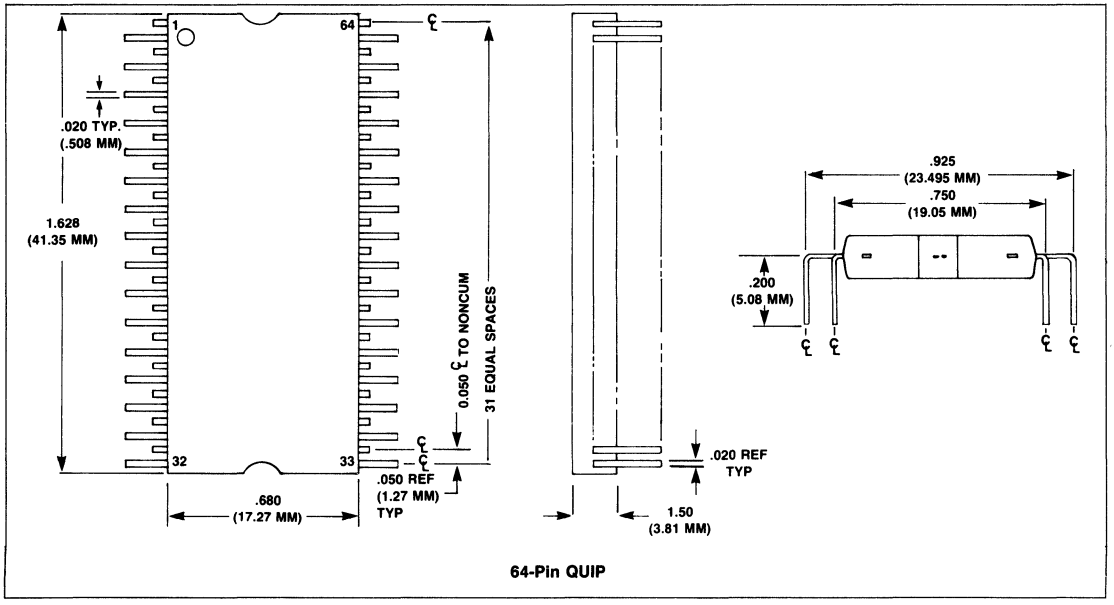


Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



64-Pin QUIP

R24BKJ
2400 bps V.26 bis, Bell 201B/C Modem

INTRODUCTION

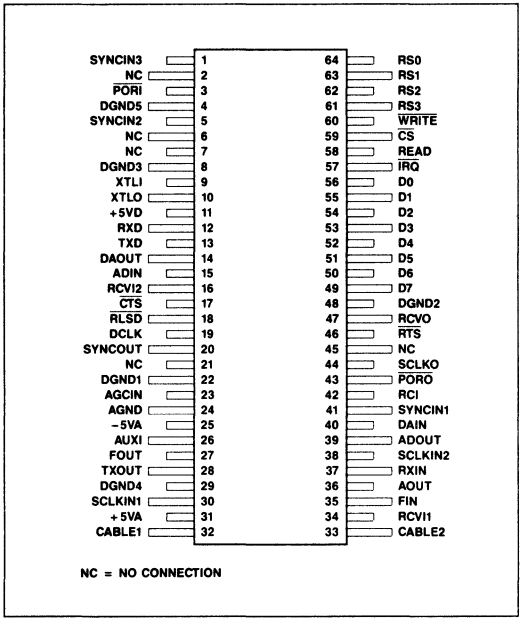
The R24BKJ is a synchronous, serial/parallel, 2400 bps modem in a single 64-pin quad in-line package (QUIP). The modem is designed for operation over the public switched telephone network with appropriate line terminations, such as a data access arrangement, provided externally.

The R24BKJ satisfies the telecommunications requirements specified in CCITT Recommendation V.26 bis Alternate A or B and Bell 201B/C.

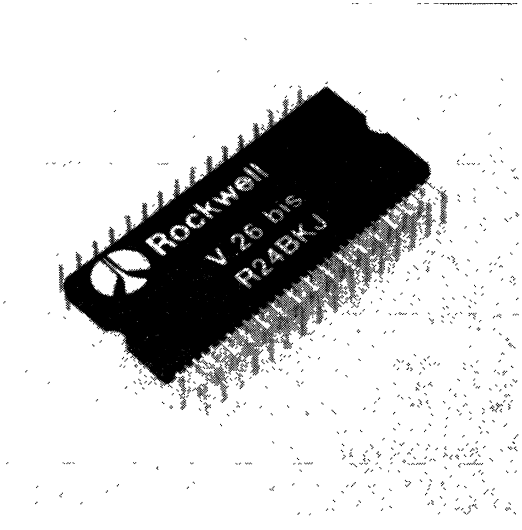
The R24BKJ is optimized for use in compact original equipment manufacturer (OEM) systems. Its small size and low power consumption offer the user flexibility in creating a 2400 bps modem customized for specific packaging and functional requirements.

FEATURES

- Single 64-Pin QUIP
- CCITT V.26 bis Alternate A or B
- Bell 201B/C
- Half-Duplex (2-Wire)
- Programmable RTS/CTS Delay
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: −43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R24BKJ Pin Assignments



R24BKJ 2400 bps V.26 bis/Bell 201B/C Modem

TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R24BKJ can generate single or dual frequency voice band tones up to 3600 Hz with a resolution of 0.11 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate	1200 Baud
Data Rate	2400 bps

DATA ENCODING

The 2400 bps data stream is encoded into dibits per CCITT V.26 bis Alternate A or B and Bell 201B/C.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R24BKJ provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	−0.99	−2.39	−3.93
1500	−0.20	−0.65	−1.22
2000	+0.15	+0 87	+1.90
3000	+1.43	+3.06	+4.58

TRANSMITTED DATA SPECTRUM

The transmitter spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R24BKJ incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V.27 ter. The scrambler can be disabled by setting a bit in interface memory.

RECEIVE LEVEL

The receiver circuit of the R24BKJ satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R24BKJ RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R24BKJ provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R24BKJ TXOUT pin and the transmitter analog output (TXA). The default level at TXA, when sending pseudorandom data, is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R24BKJ provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Data rate of 2400 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

SYNCHRONIZING SEQUENCE

The synchronizing sequence of the R24BKJ consists of two segments: a fixed segment of unscrambled ones, and an open segment which may be either unscrambled or scrambled ones, depending on the configuration selected. Both segments are programmable by allowing the synchronizing sequence to be varied for specific applications.

TURN-OFF SEQUENCE

The turn-off sequence consists of approximately 10 ms of remaining data and scrambled or unscrambled ones at 1200 baud.

CLAMPING

The following clamps are provided with the R24BKJ:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{\text{RLSD}}$ is off.
2. *Received Line Signal Detector ($\overline{\text{RLSD}}$).* $\overline{\text{RLSD}}$ is clamped off (squelched) whenever $\overline{\text{RTS}}$ is on.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of RTS and the off-to-on transition of CTS is dictated by the length of the synchronizing signal. The response time is programmable. The choice of response times depends upon the system application: a) limited protection against line echoes; b) protection given against line echoes.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

RLSD turns on whenever energy is detected on the line. The RLSD off-to-on response time is 10 ±5 ms.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD. The on-to-off response time is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

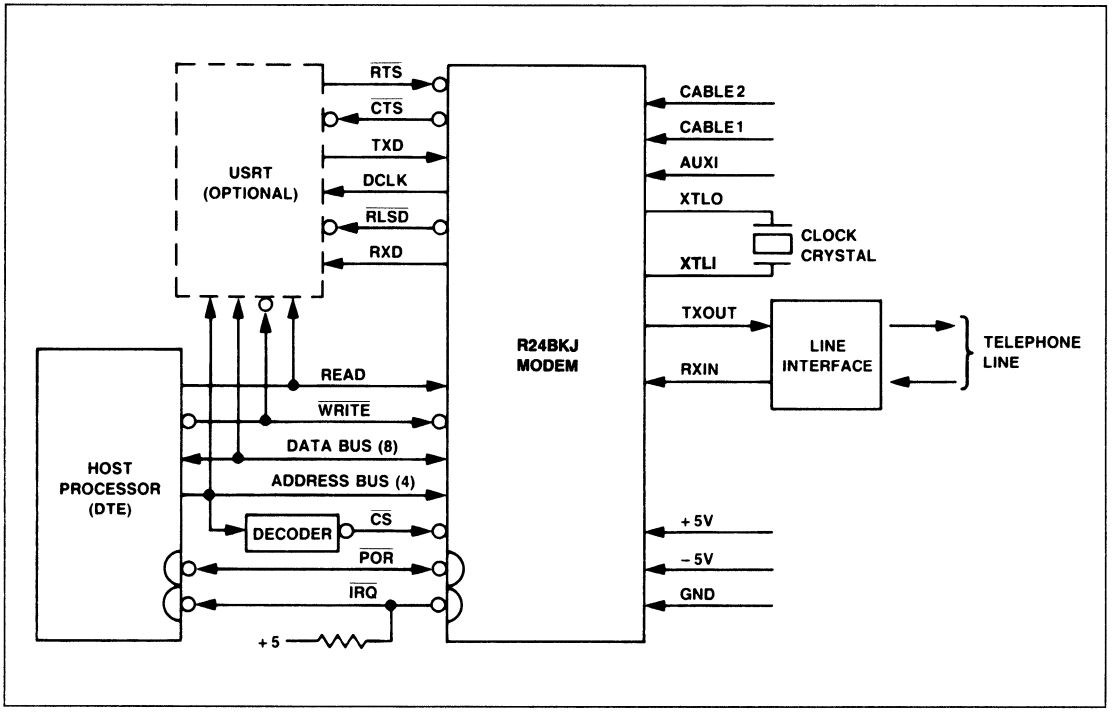
POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	250 mA @ 5.0 Vdc	225 mA @ 5.0 Vdc
−5 Vdc	±5%	25 mA @ −5.0 Vdc	25 mA @ −5.0 Vdc

Note: All voltages must have ripple ≤0.1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in suitable antistatic container).
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.



R24BKJ Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R24BKJ Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R24BKJ Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0−F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
$\overline{READ}$	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
$\overline{RLSD}$	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

*R = Required overhead connection; no connection to host equipment. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Digital Interface Characteristics

Symbol	Parameter	Units	Type							
			Input			Output			Input/Output	
			IA	IB	IC	OA	OB	OC	I/OA	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

3

Analog Interface Characteristics

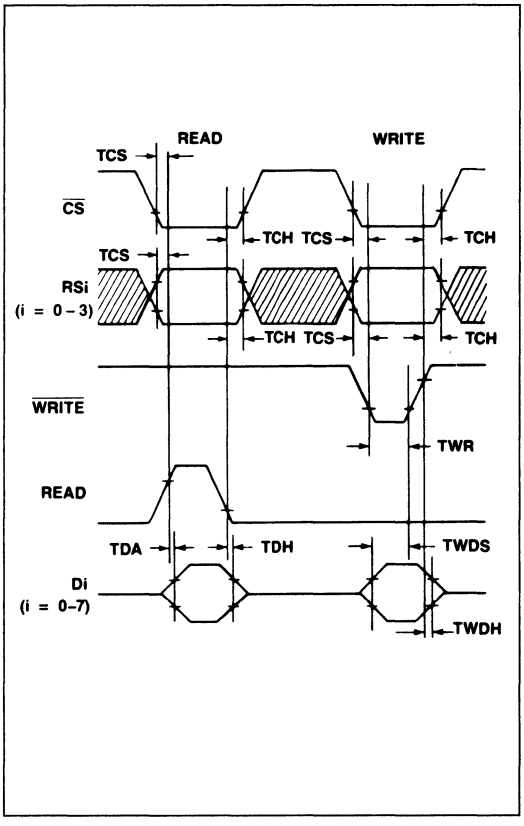
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3.03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726.43/(S+11542.44) and 604 Ω series resistor are required.
RXIN	AB	The receiver input impedance is greater than 1M Ω. An external antialiasing filter with a transfer function of 19533.88/(S+11542.44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 3600 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are: $(-5\ VA - 0.3) \leq V_{IN} \leq (+5\ VA + 0.3)$

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE2	CABLE1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R24BKJ contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R24BKJ Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R24BKJ is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R24BKJ Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

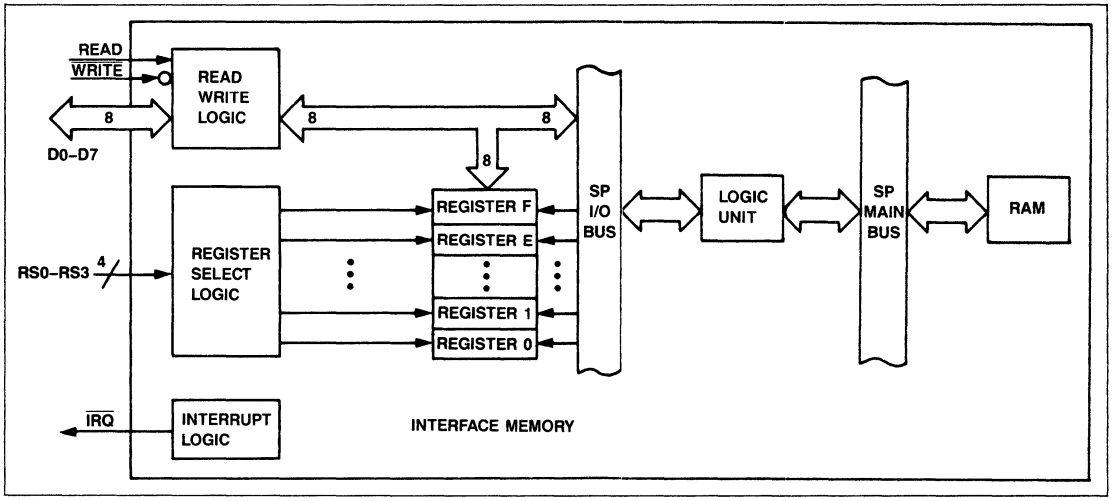
Five configurations are available in the R24BKJ modem. The configuration is selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is shown in the following table. All other codes represent invalid states.

Configuration Codes

CONF Code	Configuration	Scrambler/ Descrambler
04*	V.26B	disabled
44	V.26A	disabled
84	V.26B	enabled
C4	V.26A	enabled
0C	Tone	Not applicable
*Default value at POR with 220 ms synchronizing sequence.		

When the modem is initialized by power-on-reset, the configuration defaults to V.26B with scrambler disabled and 220 ms synchronizing signal. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at 1200 times per second.



R24BKJ Host Processor Interface

R24BKJ Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	—	TPDM	1	—	EQFZ	DEQFZ	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register \ Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection. The transmitter operates in either serial or parallel mode as selected by mode control bit C:5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1. The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R24BKJ is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{RTS}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R24BKJ Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
CDET	Carrier Detector	8:5	The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{\text{RLSD}}$ and deactivates one baud time after $\overline{\text{RLSD}}$.
CDIE	Channel Data Interrupt Enable	E:6	When set to a one, CDIE enables an $\overline{\text{IRQ}}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.
CDREQ	Channel Data Request	E:5	Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.
CONF	Configuration	D:0–7	The 8-bit field CONF controls the configuration of the modem according to the following table: **Hex Code** / **Configuration** 04* — V.26B, Bell 201B/C, Scrambler/descrambler disabled 44 — V.26A, Scrambler/descrambler disabled 84 — V.26B, Bell 201B/C, Scrambler/descrambler enabled C4 — V.26A, Scrambler/descrambler enabled 0C — Tone *Default value at POR with 220 ms turn-on sequence. **Configuration Definitions** *V.26/Bell 201*—The modem operates as specified in CCITT Recommendation V.26 bis Alternate A or B, and Bell 201B/C, at a 2400 bps data rate. *Tone*—The modem sends single or dual frequency tones in response to the $\overline{\text{RTS}}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations.
DDIE	Diagnostic Data Interrupt Enable	E:2	When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.
DDREQ	Diagnostic Data Request	E:0	DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.
DDXL	Diagnostic Data X Least	2:0–7	Least significant byte of 16-bit word used in reading XRAM locations.
DDXM	Diagnostic Data X Most	3:0–7	Least significant byte of 16-bit word used in reading XRAM locations.
DDYL	Diagnostic Data Y Least	0:0–7	Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DDYM	Diagnostic Data Y Most	1:0–7	Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DEQFZ	Delayed Equalizer Freeze	C:1	The DEQFZ bit sets the receiver's equalizer in a delayed freeze mode. If DEQFZ = 1, the equalizer will be frozen when a programmable baud count expires after carrier detection. The power-on default value is 600 ms; a lower number is not recommended since the equalizer adapts slowly on data.
EQFZ	Equalizer Freeze	C:2	When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.
FED	Fast Energy Detector	B:5,6	FED consists of a 2-bit field that indicates the level of received signal according to the following code. **Code** / **Energy Level** 0 — None 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold While receiving a signal, FED normally alternates between Codes 2 and 3.

R24BKJ Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct. GHIT returns to zero when the AGC output returns to normal.
IA	Interrupt Active	E:7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level.
RAMA	RAM Access	F:0–7	The RAMA register is written by the host when reading or writing diagnostic data. The RAMA code determines the RAM location with which the diagnostic read or write is performed.
RAMW	RAM Write	C:0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM. RAMW is set to a zero by the host when reading RAM diagnostic data.
RTSP	Request to Send Parallel	C:7	The one state of RTSP begins a transmit sequence. The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
RXCD	Receiver Channel Data	5:0–7	RXCD is written to by the modem every eight bit times. This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ).
RX	Receive State	B:7	RX is a one when the modem is in the receive state (i.e., not transmitting).
SETUP	Setup	E:3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i.e., when changing CONF (D·0–7).
TDET	Tone Detected	A·7	The one state of TDET indicates reception of a tone. The filter can be retuned by means of the diagnostic write routine.
TPDM	Transmitter Parallel Data Mode	C:5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input.
TXCD	Transmitter Channel Data	4:0–7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one. Data is transmitted as single bits in V.21 or as dibits in V.27 starting with bit 0 or dibit 0,1.

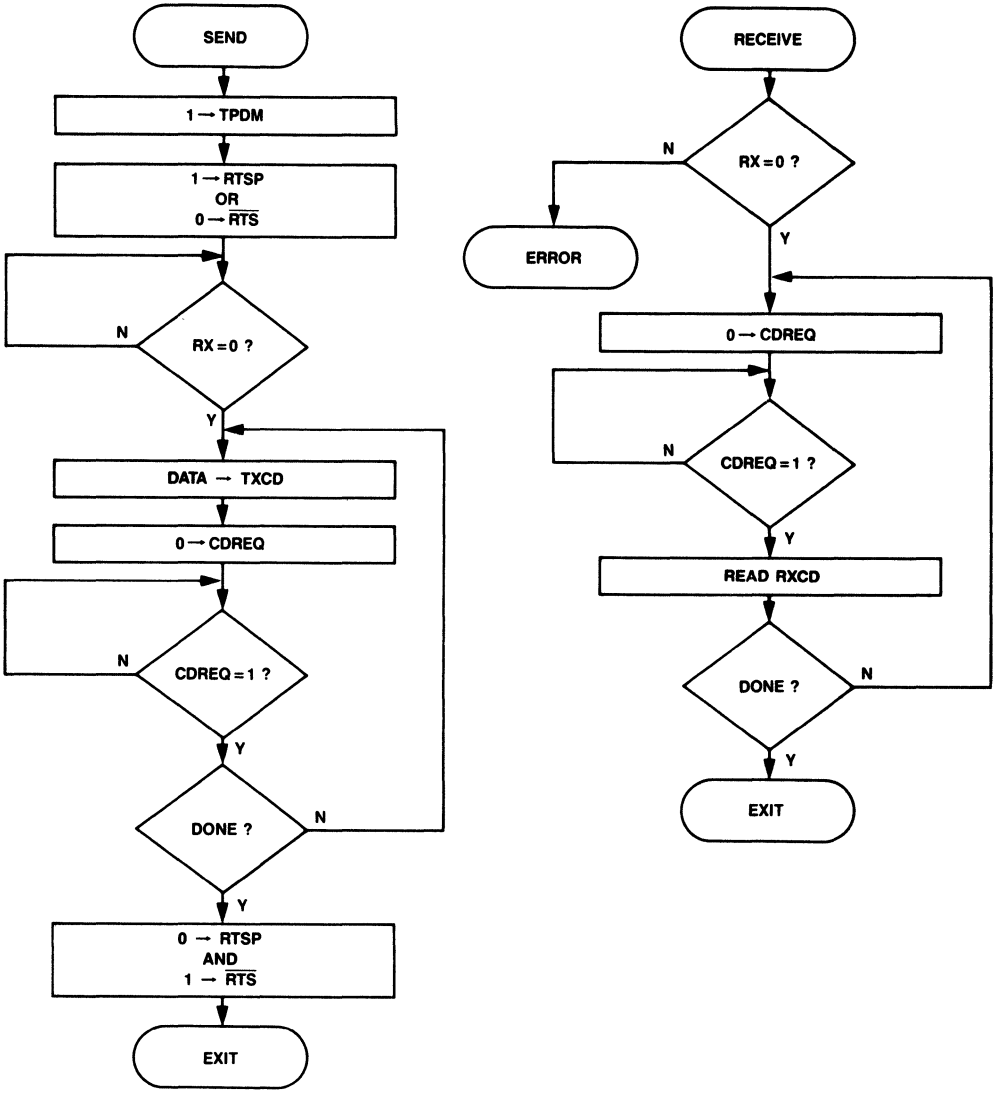
Diagnostic Data Transfer

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R24BKJ RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R24BKJ Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long. These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

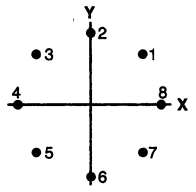
R24BKJ RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	B1	2,3
2	Average Power	F2	2,3
3	Receiver Sensitivity	F1	2,3
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	5B	0,1,2,3
6	Equalizer Tap Coefficients	1B-2A	0,1,2,3
7	Unrotated Equalizer Output	6B	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	6C	0,1,2,3
10	Error Vector	6D	0,1,2,3
11	Rotation Angle	87	2,3
12	Frequency Correction	8B	2,3
13	EQM	B0	2,3
14	Alpha (α)	36	0,1
15	Beta One (β_1)	37	0,1
16	Beta Two (β_2)	38	0,1
17	Alpha Prime (α')	39	0,1
18	Beta One Prime (β_1')	3A	0,1
19	Beta Two Prime (β_2')	3B	0,1
20	Alpha Double Prime (α'')	B6	2,3
21	Beta Double Prime (β'')	B7	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1
28	Fixed Synchronizing Segment	91	2,3
29	Open Synchronizing Segment	11	0,1

R24BKJ Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 – [(AGC Gain Word/64) × 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$, For –43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code F1
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = $[65.4\ (10^A)]^2/2$ where: $A = (P_{OFF} - P_{ON} - 0.5)/20$ P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84.

R24BKJ Diagnostic Data Scaling

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers. Value (hex): Point 1: X 1600, Y 1600; Point 2: X 0000, Y 1F1C; Point 3: X EA00, Y 1600; Point 4: X E0E4, Y 0000; Point 5: X EA00, Y EA00; Point 6: X 0000, Y E0E4; Point 7: X 1600, Y EA00; Point 8: X 1F1C, Y 0000 
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) × 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) × Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application.
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668. Use a sample rate of 7200 samples per second for all calculations.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 9.1022 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.
28,29	**Fixed and Open Synchronizing Segments** (16-bit unsigned) Synchronizing Sequence = [Fixed + (Open + 1)] baud times (± 1 baud time) $7FFF_{16} \geq$ Fixed, Open baud times ≥ 0 (baud time = 1/1200 = 0.833 ms) Fixed = unscrambled ones Open = unscrambled or scrambled ones

3

POWER-ON INITIALIZATION

When power is applied to the R24BKJ, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.26B, scrambler disabled, serial mode, 221 ms synchronizing signal, interrupt disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for –43.5 dBm, receiver turn-off threshold set for –47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

The R24BKJ provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm.

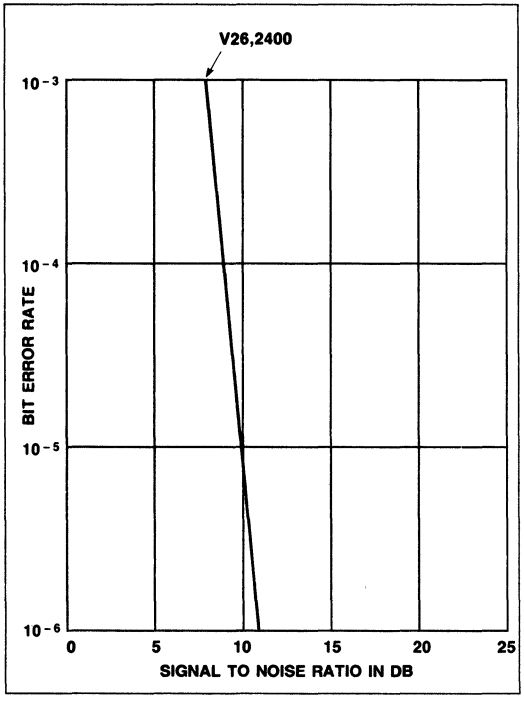
RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R24BKJ can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

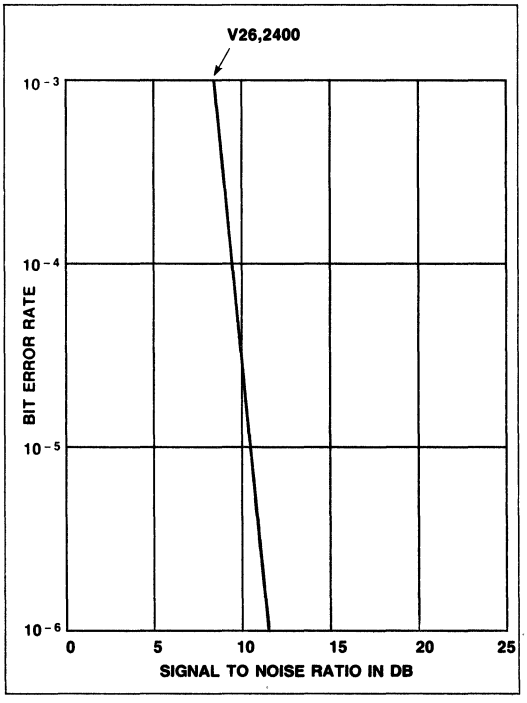
TYPICAL PHASE JITTER

The modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

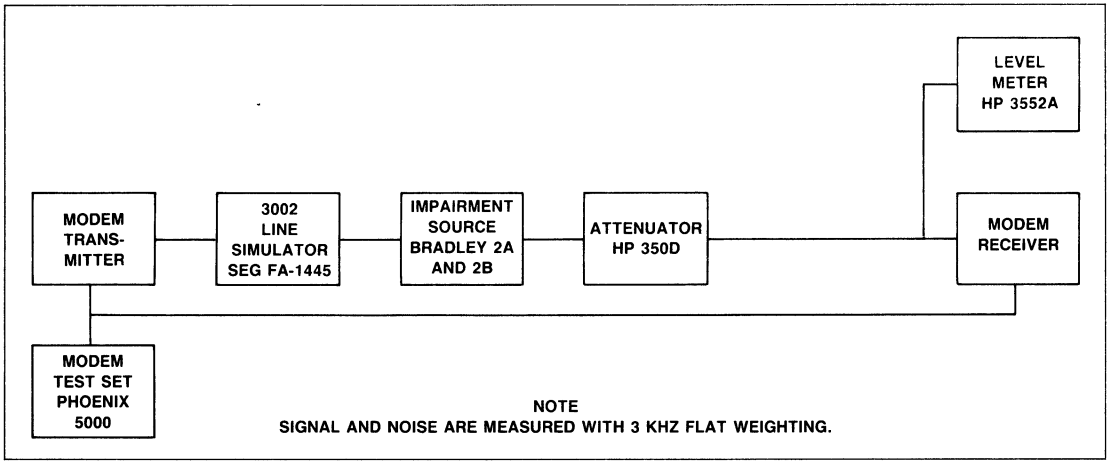


Typical Bit Error Rate (Back-to-Back, Level –20 dBm)



Typical Bit Error Rate (Unconditioned 3002 Line, Level –20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

APPLICATION

Recommended Modem Interface Circuit

The R24BKJ is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C2	N511BY100JW	San Fernando/ Wescap
C1	C114C330J2G5CA	Kemet
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434.0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I.T.T.
R9	CRB¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R24BKJ and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R24BKJ, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R24BKJ package. Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R24BKJ package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R24BKJ package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
11. Routing of R24BKJ signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
	51	47		
	52	48		
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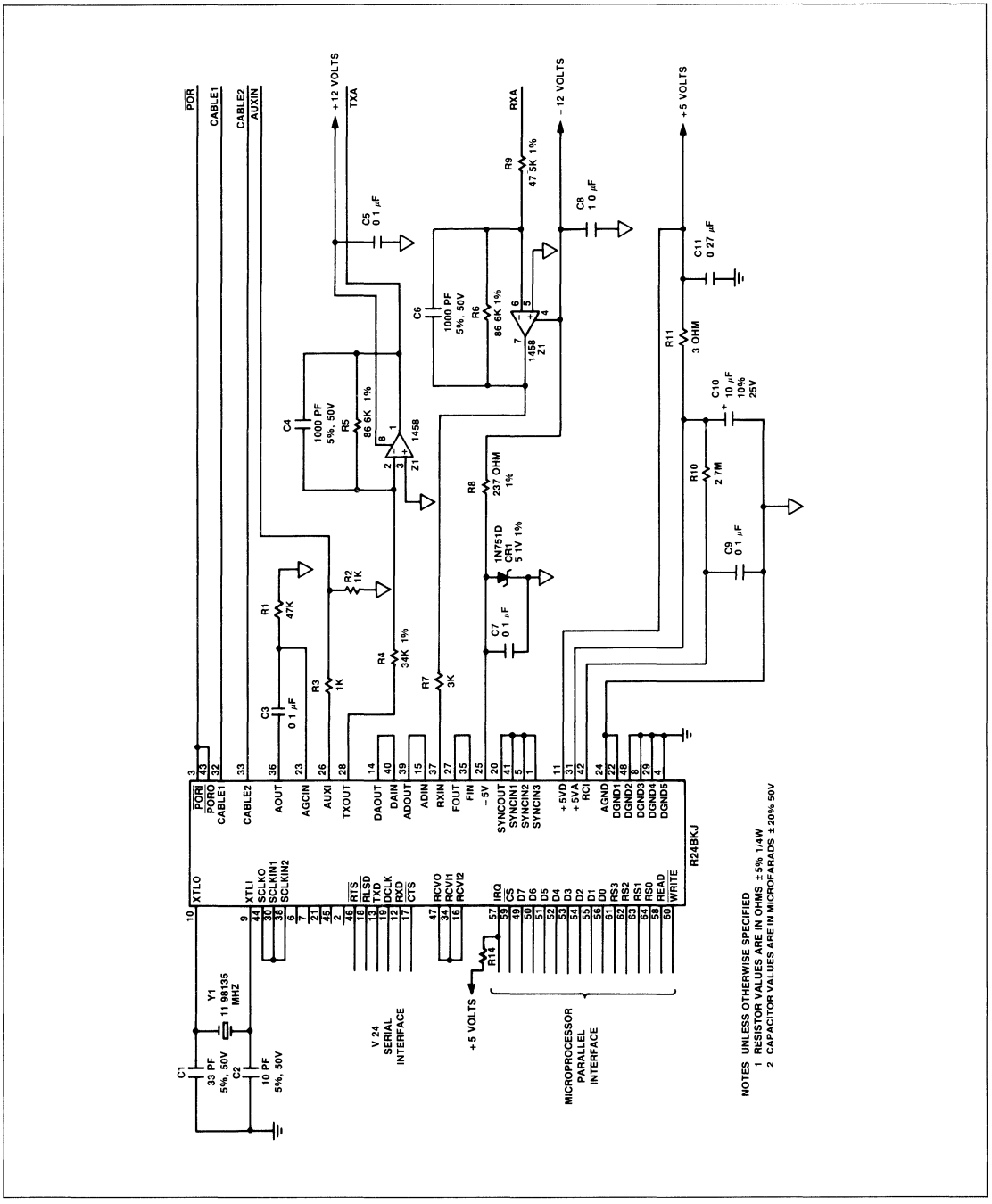
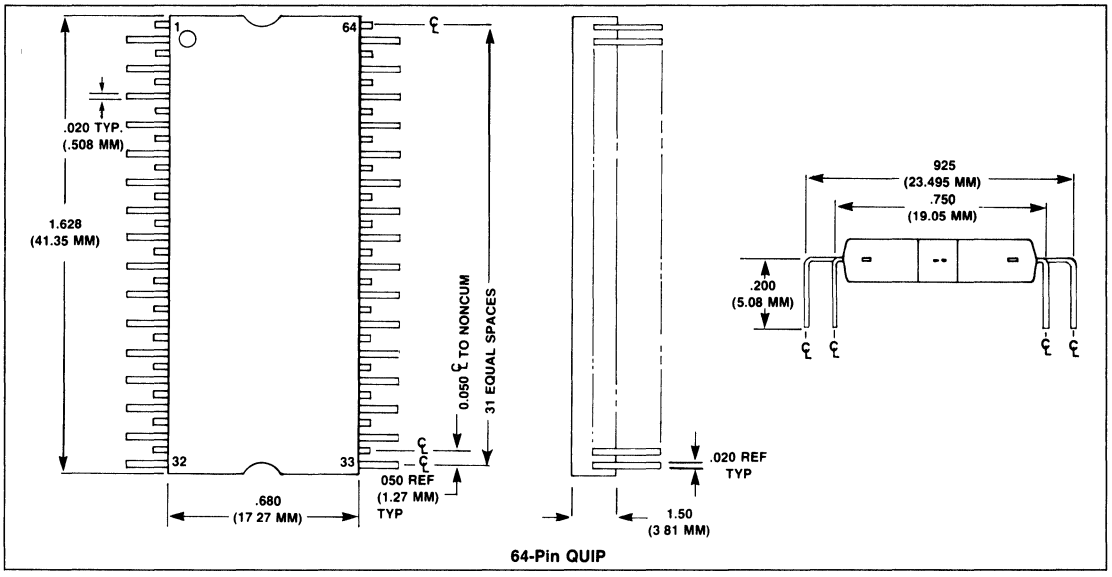


Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



64-Pin QUIP

R48MFX
4800 bps MONOFAX™ Modem

INTRODUCTION

The R48MFX MONOFAX 48 is a synchronous, serial/parallel, 4800 bps modem in a single 64-pin quad in-line package (QUIP). The modem is designed for operation over the public switched telephone network with appropriate line terminations, such as a data access arrangement, provided externally.

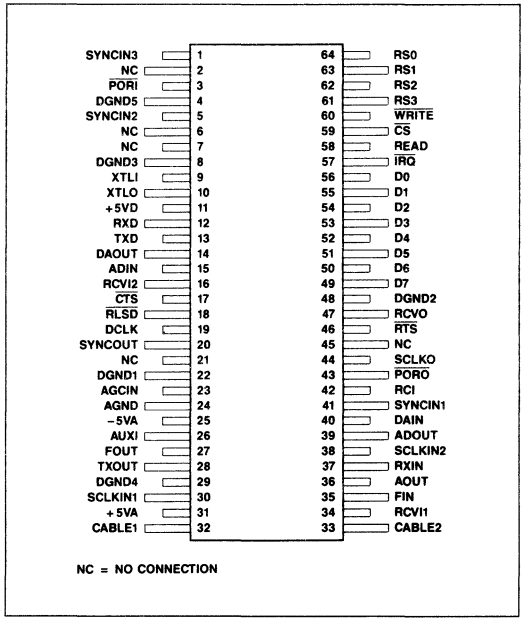
The R48MFX satisfies the telecommunications requirements specified in CCITT Recommendation V.27 ter, T.4 and the binary signaling capabilities of Recommendation T.30.

The R48MFX is optimized for use in compact Group 3 facsimile machines. Its small size and low power consumption offer the user flexibility in creating a 4800 bps modem customized for specific packaging and functional requirements.

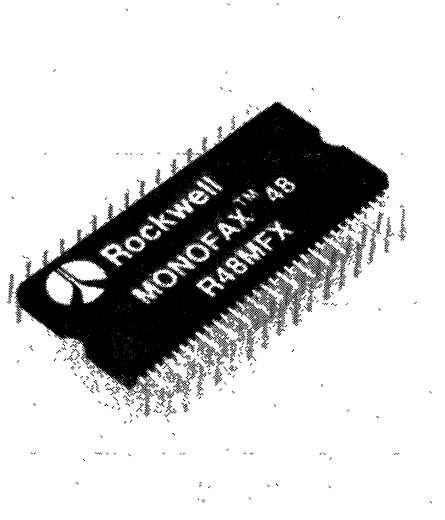
™MONOFAX is a trademark of Rockwell International

FEATURES

- Single 64-Pin QUIP
- CCITT V.27 ter, T.30, V.21 Channel 2, T.4
- Group 3 Facsimile Transmission/Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: −43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R48MFX Pin Assignments



R48MFX 4800 bps MONOFAX Modem

TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R48MFX can generate single or dual frequency voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Configuration	Parameter	Specification (±0.01%)
V.27	Signaling Rate Data Rate	1600 Baud 4800 bps
	Signaling Rate Data Rate	1200 Baud 2400 bps
V.21	Signaling Rate Data Rate	300 Baud 300 bps

DATA ENCODING

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

At 300 baud, the data stream is 300 bps FSK per CCITT V.21 channel 2.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R48MFX provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	−0.99	−2.39	−3.93
1500	−0.20	−0.65	−1.22
2000	+0.15	+0.87	+1.90
3000	+1.43	+3.06	+4.58

TRANSMITTED DATA SPECTRUM

When operating at 1600 baud, the transmitter spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitter spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R48MFX incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V.27 ter. The scrambler can be disabled by setting a bit in interface memory.

RECEIVE LEVEL

The receiver circuit of the R48MFX satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R48MFX RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R48MFX provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R48MFX TXOUT pin and the transmitter analog output (TXA). The default level at TXA is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R48MFX provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Selected data rate of 4800, 2400 or 300 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

Seven turn-on sequences are generated by the R48MFX, as defined in the following table:

Turn-On Sequences[1]

No.	Bit Rate (bps)	$\overline{RTS}$ On-$\overline{CTS}$ On Time[1] (ms)	Comments
1	300	<14	No Training Sequence, No Echo Tone
2	2400	943	Long Train, No Echo Tone
3	2400	1148	Long Train, with Echo Tone[2]
4	2400	<10	Training Disabled
5	4800	708	Long Train, No Echo Tone
6	4800	913	Long Train, with Echo Tone[2]
7	4800	<10	Training Disabled

Notes:

1. Assumes the receiver is in idle; if not, add receiver turn-off time.
2. For use on lines with protection against talker echo.

TURN-OFF SEQUENCE

Five turn-off sequences are generated by the R48MFX:

Turn-Off Sequences

No.	Bit Rate (bps)	$\overline{RTS}$ Off-Energy Off Time (ms)	Silence Time (ms)
1	300	<7	0
2	2400 serial	7.5	20
3	2400 parallel	7.5-10	20
4	4800 serial	5.4	20
5	4800 parallel	5.4-6.7	20

CLAMPING

The following clamps are provided with the R48MFX:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector ($\overline{RLSD}$).* $\overline{RLSD}$ is clamped off (squelched) whenever $\overline{RTS}$ is on.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the bit rate, the length of the training sequence, and the presence of the echo tone. The Turn-On Sequences table on page 2 lists the $\overline{CTS}$ response times.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

$\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 801 bauds (V.27) or <10 ms (300 bps). The $\overline{RLSD}$ on-to-off response time is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

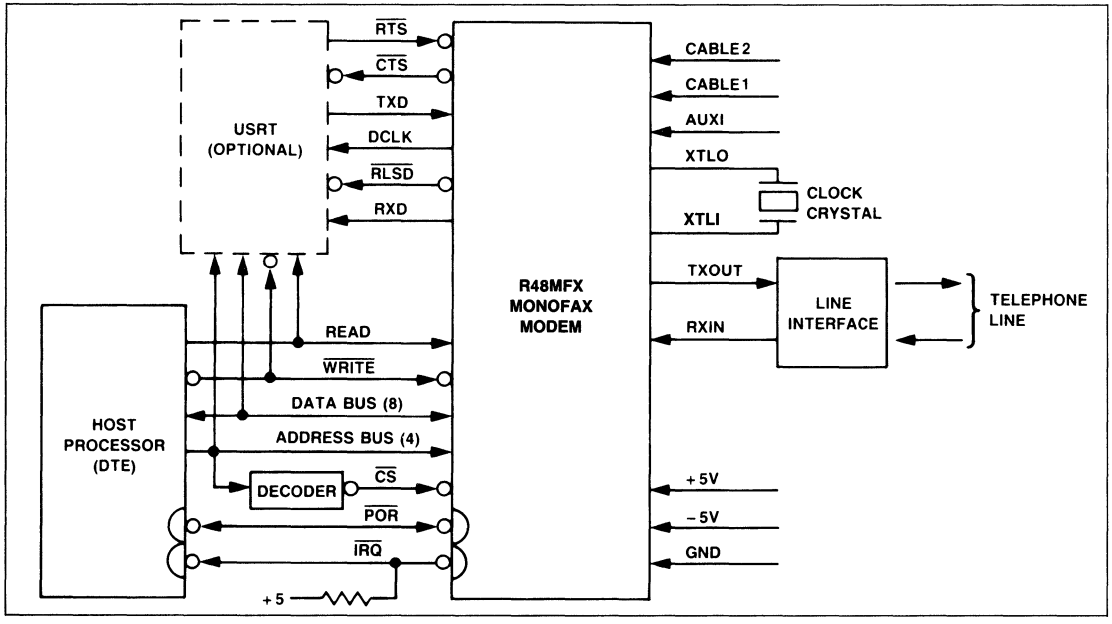
POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	250 mA @ 5.0 Vdc	225 mA @ 5.0 Vdc
−5 Vdc	±5%	25 mA @ −5.0 Vdc	25 mA @ −5.0 Vdc

Note: All voltages must have ripple ≤0.1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in suitable antistatic container).
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less



R48MFX Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R48MFX Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R48MFX Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0−F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
$\overline{READ}$	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
$\overline{RLSD}$	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

*R = Required overhead connection; no connection to host equipment.

Unused inputs tied to +5V or ground require individual 10K Ω series resistors

Digital Interface Characteristics

Symbol	Parameter	Units	Type							
			Input			Output			Input/Output	
			IA	IB	IC	OA	OB	OC	I/OA	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current	μA		−240 max.	−240 max.			−240 max.		−260 max.
	(Short Circuit)			−10 min.	−10 min.			−10 min.		−100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5 25 Vdc
5. I load = 0 36 mA

3

Analog Interface Characteristics

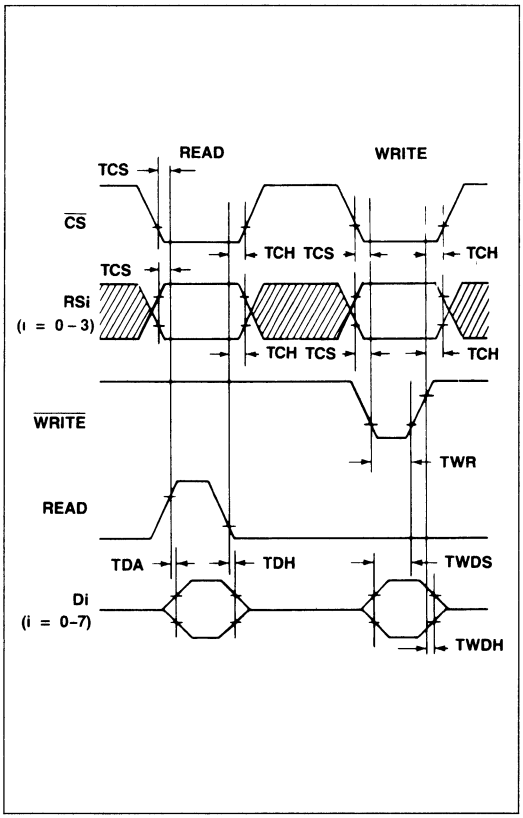
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3.03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726.43/(S + 11542.44) and 604 Ω series resistor are required.
RXIN	AB	The receiver input impedance is greater than 1M Ω. An external antialiasing filter with a transfer function of 19533.88/(S + 11542.44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are: (−5 VA − 0.3) ≤ V_{IN} ≤ (+5 VA + 0.3)

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE2	CABLE1	Length of 0.4mm Diameter Cable
0	0	0 0
0	1	1 8 km
1	0	3 6 km
1	1	7 2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R48MFX contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R48MFX Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R48MFX is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R48MFX Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

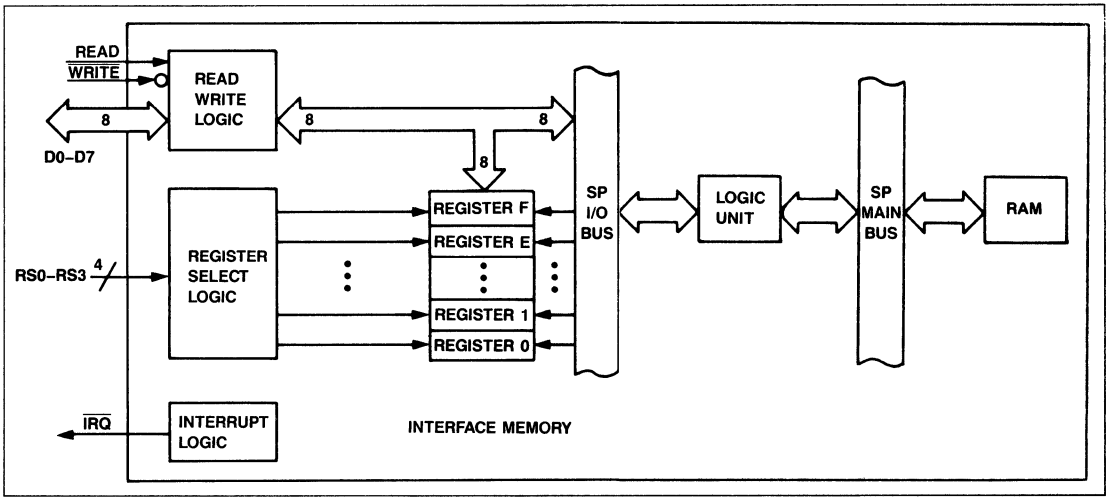
Four configurations are available in the R48MFX modem: V.27 4800/2400 bps long train, V.21, and Tone. The configuration is selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is shown in the following table. All other codes represent invalid states.

Configuration Codes

CONF Code	Configuration
00	V.21
04	V 27, 2400 Long Train
06*	V 27, 4800 Long Train
08	Tone Mode
* Default value at POR	

When the modem is initialized by power-on-reset, the configuration defaults to V.27 4800 bps. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at the baud rate (V.27 and V.21), 9600 times per second (tone generator), or 1600 times per second (tone detector).



R48MFX Host Processor Interface

R48MFX Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	EPT	TPDM	TDIS	EQSV	EQFZ	SDIS	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	PN	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register \ Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection. The transmitter operates in either serial or parallel mode as selected by mode control bit C:5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1. The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R48MFX is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{RTS}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R48MFX Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
CDET	Carrier Detector	8:5	The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{\text{RLSD}}$ and deactivates one baud time after $\overline{\text{RLSD}}$.
CDIE	Channel Data Interrupt Enable	E:6	When set to a one, CDIE enables an $\overline{\text{IRQ}}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.
CDREQ	Channel Data Request	E:5	Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.
CONF	Configuration	D:0-7	The 8-bit field CONF controls the configuration of the modem according to the following table: **Hex Code** — **Configuration** 00 — V.21 04 — V.27, 2400 Long Train 06 — V.27, 4800 Long Train (Default) 08 — Tone All else — Invalid **Configuration Definitions** *V.21*—The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 Channel 2 modulation system. *Tone*—The modem sends single or dual frequency tones in response to the $\overline{\text{RTS}}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations. *V.27*—The modem is compatible with CCITT Recommendation V.27 ter.
DDIE	Diagnostic Data Interrupt Enable	E:2	When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.
DDREQ	Diagnostic Data Request	E:0	DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.
DDXL	Diagnostic Data X Least	2:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDXM	Diagnostic Data X Most	3:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDYL	Diagnostic Data Y Least	0:0-7	Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DDYM	Diagnostic Data Y Most	1:0-7	Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
EPT	Echo Protector Tone	C:6	When EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. EPT is not active if TDIS is on.
EQFZ	Equalizer Freeze	C:2	When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.
EQSV	Equalizer Save	C:3	When EQSV is a one, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training.
FED	Fast Energy Detector	B:5,6	FED consists of a 2-bit field that indicates the level of received signal according to the following code. **Code** — **Energy Level** 0 — None 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold While receiving a signal, FED normally alternates between Codes 2 and 3.

R48MFX Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct. GHIT returns to zero when the AGC output returns to normal.
IA	Interrupt Active	E:7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level.
PN	Period N	8:3	PN sets to a one at the start of the received PN sequence. PN resets to zero at the start of the received scrambled ones. PN does not operate when TDIS is set to a one.
RAMA	RAM Access	F:0-7	The RAMA register is written by the host when reading or writing diagnostic data. The RAMA code determines the RAM location with which the diagnostic read or write is performed.
RAMW	RAM Write	C:0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM. RAMW is set to a zero by the host when reading RAM diagnostic data.
RTSP	Request to Send Parallel	C:7	The one state of RTSP begins a transmit sequence. The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
RXCD	Receiver Channel Data	5:0-7	RXCD is written to by the modem every eight bit times. This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ).
RX	Receive State	B:7	RX is a one when the modem is in the receive state (i.e., not transmitting).
SDIS	Scrambler Disable	C:1	When SDIS is a one, the scrambler/descrambler is disabled. When SDIS is a zero, the scrambler/descrambler is enabled (default).
SETUP	Setup	E:3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i.e., when changing CONF (D:0-7).
TDET	Tone Detected	A:7	The one state of TDET indicates reception of a tone. The filter can be retuned by means of the diagnostic write routine.
TDIS	Training Disable	C:4	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one when $\overline{RTS}$ or RTSP go active, the generation of a training sequence is prevented at the start of transmission.
TPDM	Transmitter Parallel Data Mode	C:5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input.
TXCD	Transmitter Channel Data	4:0-7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one. Data is transmitted as single bits in V.21 or as dibits in V.27 starting with bit 0 or dibit 0,1.

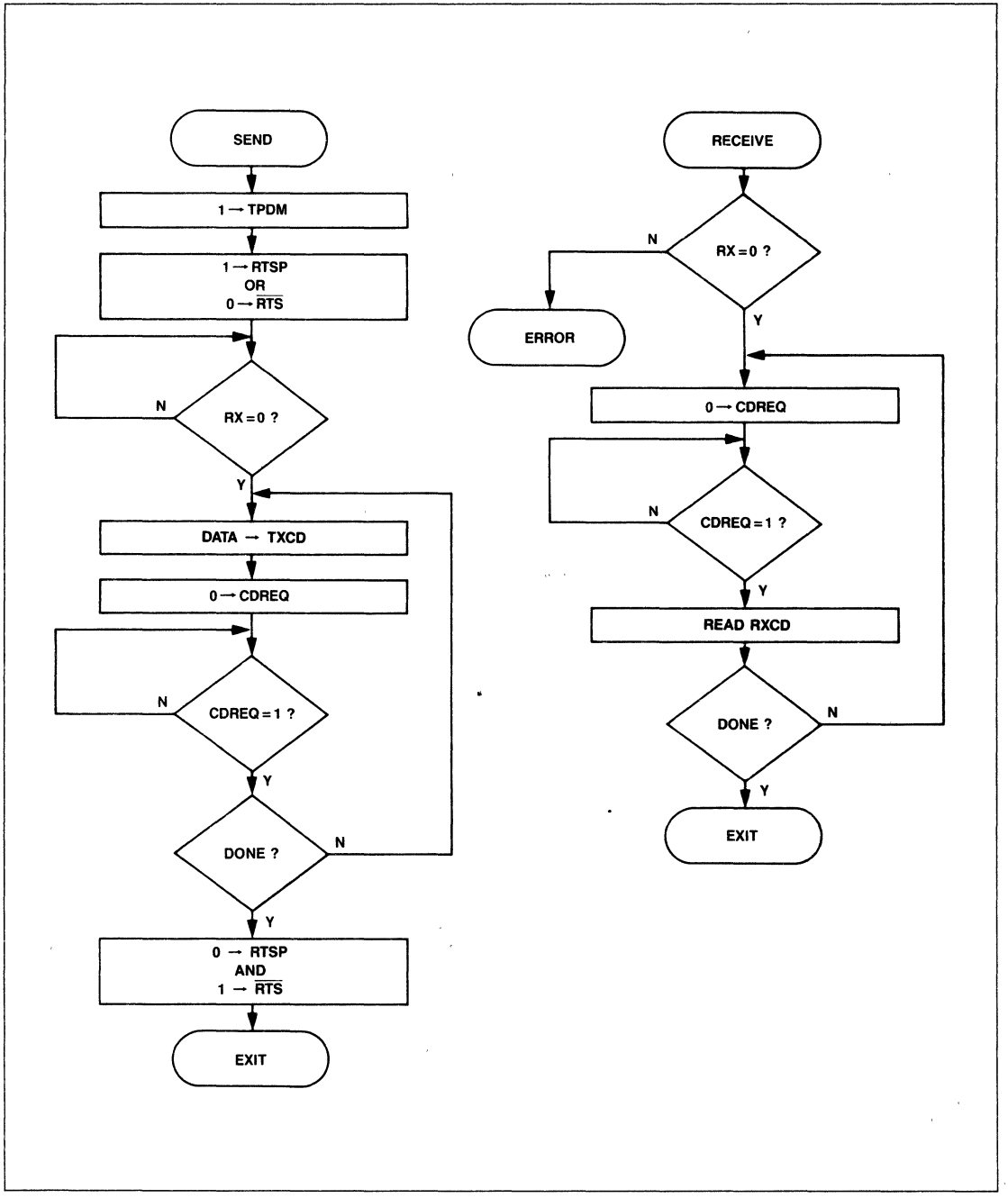
Diagnostic Data Transfer

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R48MFX RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R48MFX Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long. These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

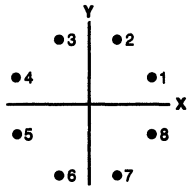
R48MFX RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	87	2,3
2	Average Power	91	2,3
3	Receiver Sensitivity	47	0,1
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	63	0,1,2,3
6	Equalizer Tap Coefficients	23-32	0,1,2,3
7	Unrotated Equalizer Output	73	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	74	0,1,2,3
10	Error Vector	75	0,1,2,3
11	Rotation Angle	B3	2,3
12	Frequency Correction	8B	2,3
13	EQM	89	2,3
14	Alpha (α)	38	0,1
15	Beta One (β_1)	39	0,1
16	Beta Two (β_2)	3A	0,1
17	Alpha Prime (α')	3B	0,1
18	Beta One Prime (β_1')	3C	0,1
19	Beta Two Prime (β_2')	3D	0,1
20	Alpha Double Prime (α'')	B8	2,3
21	Beta Double Prime (β'')	B9	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1

R48MFX Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 – [(AGC Gain Word/64) × 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$, For –43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code 47
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = $[65.4\ (10^A)]^2/2$ where: A = (P_{OFF} – P_{ON} – 0.5)/20 P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84.

R48MFX Diagnostic Data Scaling (Cont'd)

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers. Point / Value (Hex) X / Y: 1: 1D00, 0C00 2: 0C00, 1D00 3: F400, 1D00 4: E300, 0C00 5: E300, F400 6: F400, E300 7: 0C00, E300 8: 1D00, F400 
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) × 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) × Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application.
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 6.8267 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.

POWER-ON INITIALIZATION

When power is applied to the R48MFX, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.27/4800 bps, serial mode, training enabled, echo protector tone enabled, interrupts disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for -43.5 dBm, receiver turn-off threshold set for -47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V.21 type modem, the R48MFX provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of -20 dBm.

RECEIVED SIGNAL FREQUENCY TOLERANCE

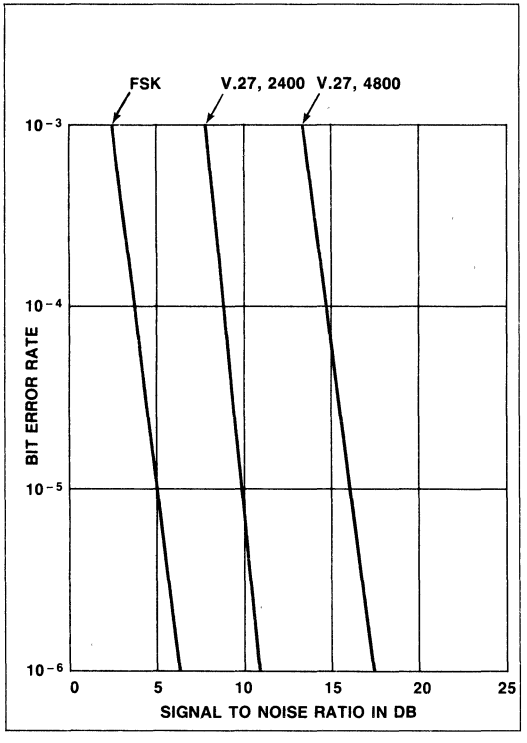
The receiver circuit of the R48MFX can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

TYPICAL PHASE JITTER

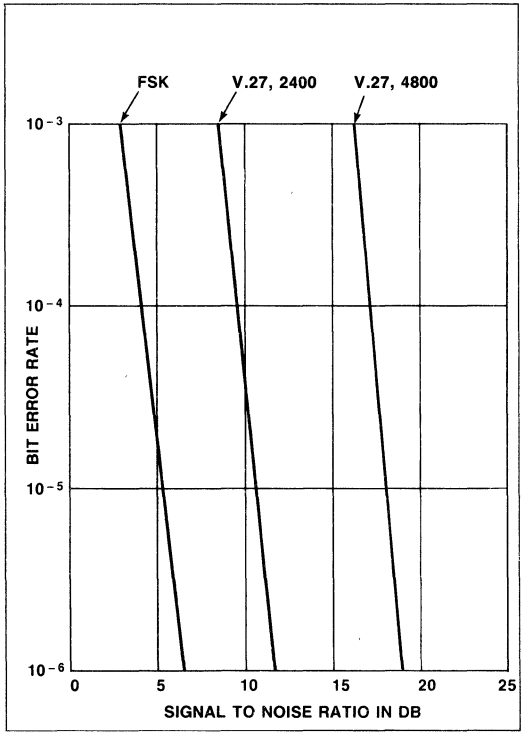
At 4800 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 2400 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

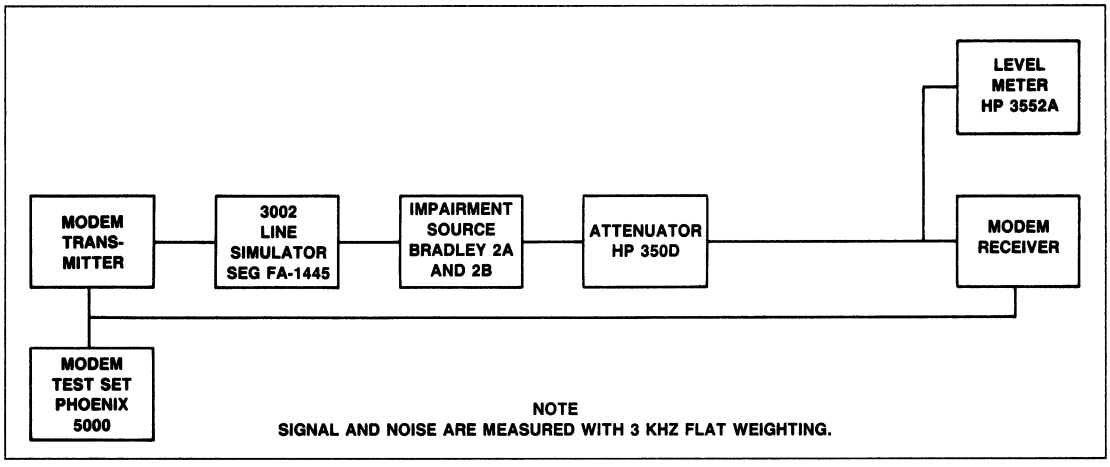


Typical Bit Error Rate (Back-to-Back, Level -20 dBm)



Typical Bit Error Rate (Unconditioned 3002 Line, Level -20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

APPLICATION

Recommended Modem Interface Circuit

The R48MFX is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434.0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I.T.T.
R9	CRB¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R48MFX and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R48MFX, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R48MFX package. Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R48MFX package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R48MFX package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
11. Routing of R48MFX signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
	51	47		
	52	48		
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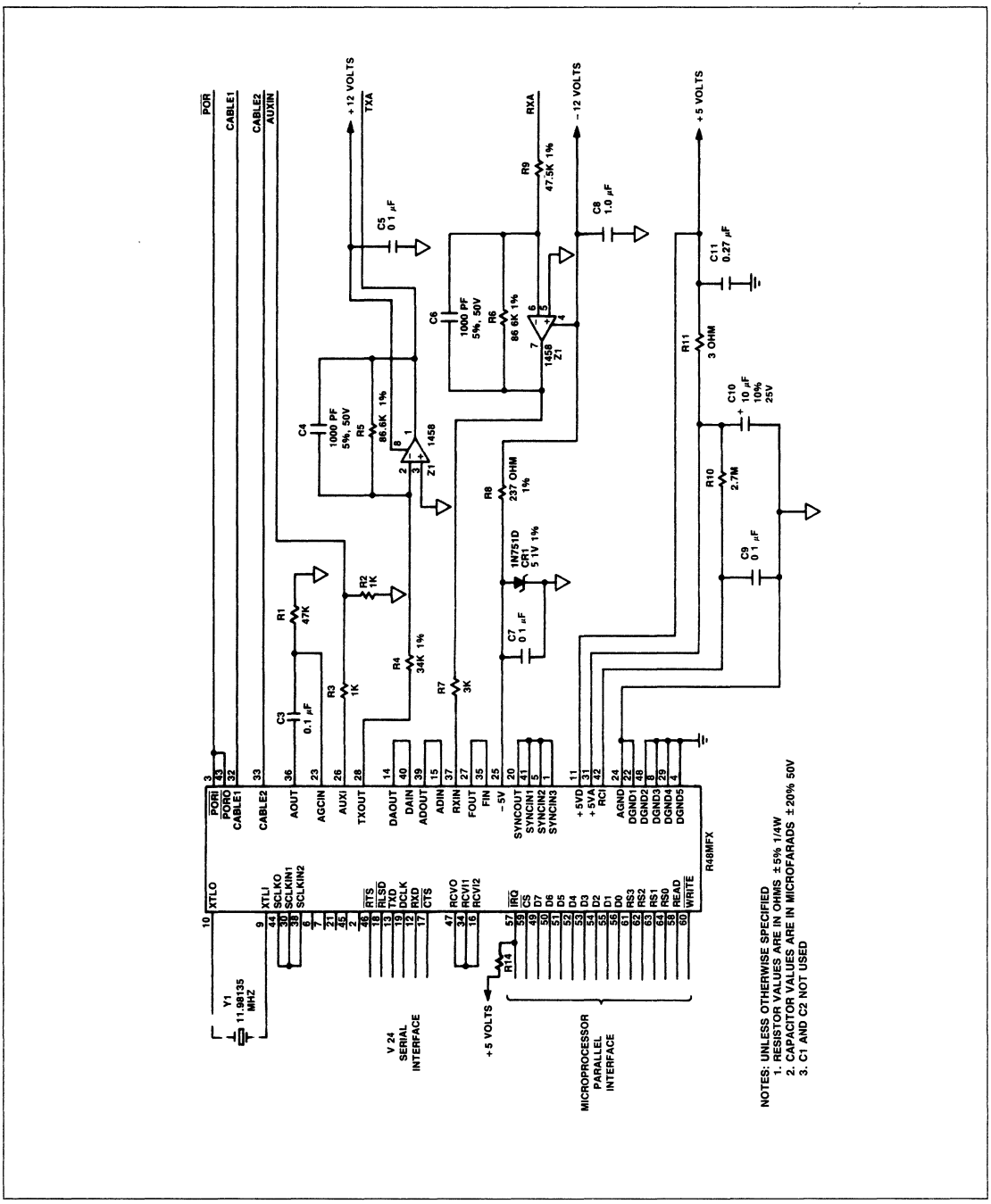
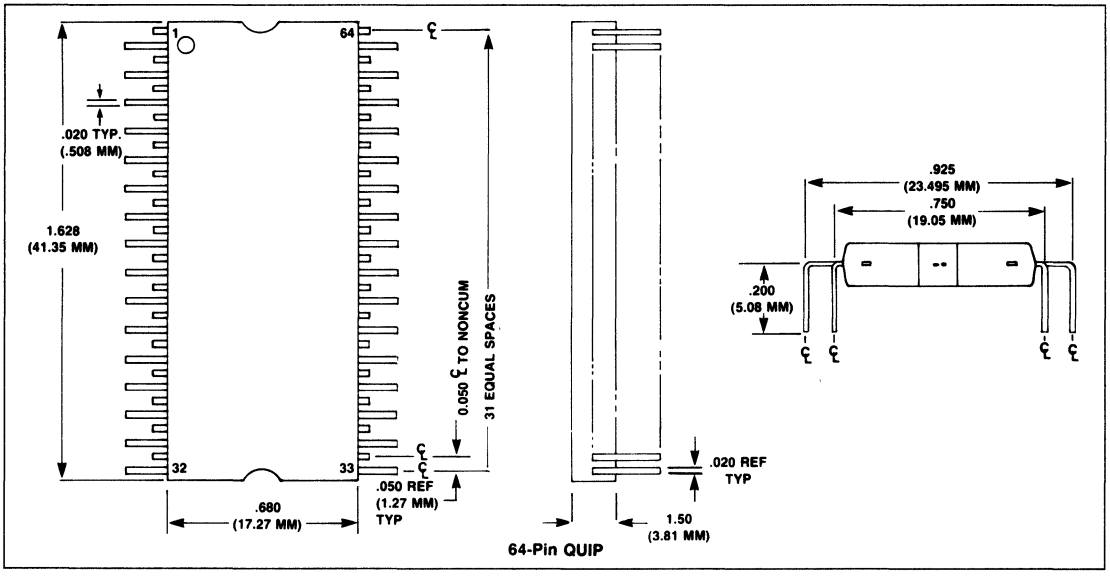


Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



64-Pin QUIP

R48PCJ
4800 bps PC Communication Modem

INTRODUCTION

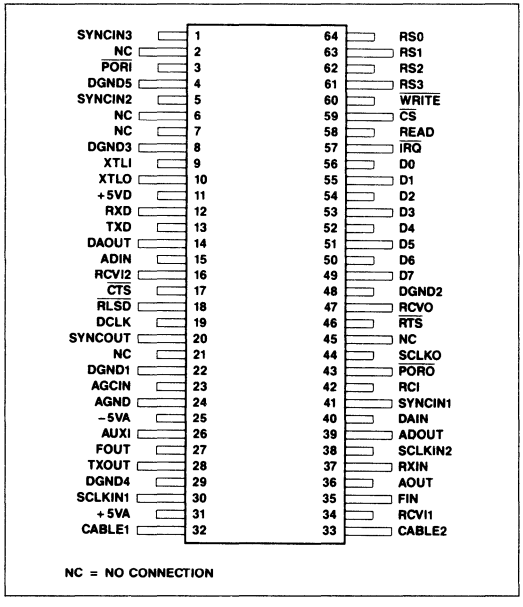
The Rockwell R48PCJ is a synchronous 4800 bits per second (bps) modem in a single 64-pin quad in-line package (QUIP). It is designed for operation over the public switched telephone network through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.27 ter, T.4 and the binary signaling capabilities of T.30. The R48PCJ can operate at speeds of 4800, 2400 and 300 bps, and includes the V.27 ter short training sequence option. Employing advanced signal processing techniques, the R48PCJ can transmit and receive data even under extremely poor line conditions.

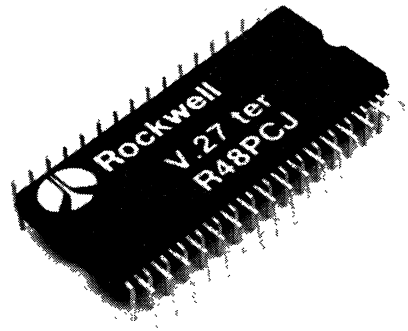
User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The R48PCJ is optimized for incorporation into an original equipment manufacturer (OEM) developed system. The modem's single device package, low power consumption, and serial/parallel host interface simplify system design and allow direct installation on the host module.

FEATURES

- Single 64-Pin QUIP
- CCITT V.27 ter, T.30, V.21 Channel 2, T.4
- Group 3 Facsimile Transmission/Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: −43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R48PCJ Pin Assignments



R48PCJ 4800 bps Modem

TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R48PCJ can generate single or dual frequency voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Configuration	Parameter	Specification (±0.01%)
V.27	Signaling Rate Data Rate	1600 Baud 4800 bps
	Signaling Rate Data Rate	1200 Baud 2400 bps
V.21	Signaling Rate Data Rate	300 Baud 300 bps

DATA ENCODING

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

At 300 baud, the data stream is 300 bps FSK per CCITT V.21 channel 2.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R48PCJ provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	−0.99	−2.39	−3.93
1500	−0.20	−0.65	−1.22
2000	+0.15	+0.87	+1.90
3000	+1.43	+3.06	+4.58

TRANSMITTED DATA SPECTRUM

When operating at 1600 baud, the transmitter spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitter spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R48PCJ incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V.27 ter. The scrambler can be disabled by setting a bit in interface memory.

RECEIVE LEVEL

The receiver circuit of the R48PCJ satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R48PCJ RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R48PCJ provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R48PCJ TXOUT pin and the transmitter analog output (TXA). The default level at TXA is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R48PCJ provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Selected data rate of 4800, 2400 or 300 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

Eleven turn-on sequences are generated by the R48PCJ, as defined in the following table:

Turn-On Sequences

No.	Bit Rate (bps)	$\overline{RTS}$ On-$\overline{CTS}$ On Time[1] (ms)	Comments
1	300	<14	No Training Sequence, No Echo Tone
2	2400	66	Short Train, No Echo Tone
3	2400	271	Short Train, with Echo Tone[2]
4	2400	943	Long Train, No Echo Tone
5	2400	1148	Long Train, with Echo Tone[2]
6	2400	<10	Training Disabled
7	4800	50	Short Train, No Echo Tone
8	4800	255	Short Train, with Echo Tone[2]
9	4800	708	Long Train, No Echo Tone
10	4800	913	Long Train, with Echo Tone[2]
11	4800	<10	Training Disabled

Notes:

1. Assumes the receiver is in idle; if not, add receiver turn-off time.
2. For use on lines with protection against talker echo.

TURN-OFF SEQUENCE

Five turn-off sequences are generated by the R48PCJ:

Turn-Off Sequences

No.	Bit Rate (bps)	$\overline{RTS}$ Off-Energy Off Time (ms)	Silence Time (ms)
1	300	<7	0
2	2400 serial	7.5	20
3	2400 parallel	7.5-10	20
4	4800 serial	5.4	20
5	4800 parallel	5.4-6.7	20

CLAMPING

The following clamps are provided with the R48PCJ:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector ($\overline{RLSD}$).* $\overline{RLSD}$ is clamped off (squelched) whenever $\overline{RTS}$ is on.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the bit rate, the length of the training sequence, and the presence of the echo tone. The Turn-On Sequences table on page 2 lists the $\overline{CTS}$ response times.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

$\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 801 bauds (V.27 long train), 481 bauds (V.27 short train), or <10 ms (300 bps). The $\overline{RLSD}$ on-to-off response time is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

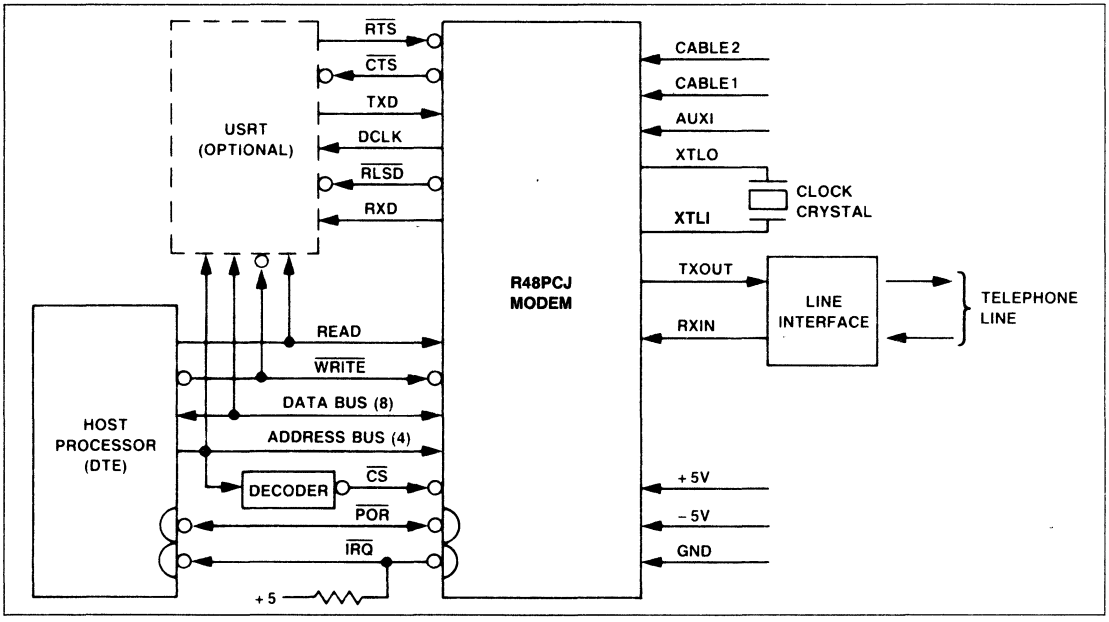
POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	270 mA @ 5.0 Vdc	245 mA @ 5 0 Vdc
−5 Vdc	±5%	25 mA @ −5.0 Vdc	25 mA @ −5 0 Vdc

Note: All voltages must have ripple ≤0 1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−55°C to +150°C (−67°F to +302°F) (Stored in suitable antistatic container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less



R48PCJ Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R48PCJ Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R48PCJ Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0−F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
$\overline{READ}$	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
$\overline{RLSD}$	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

*R = Required overhead connection; no connection to host equipment.

Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Digital Interface Characteristics

Symbol	Parameter	Units	Type: Input IA	Input IB	Input IC	Output OA	Output OB	Output OC	Input/Output I/OA	Input/Output I/OB
V_{IH}	Input Voltage, High	V	2 0 min	2 0 min	2.0 min				2 0 min.	5 25 max. 2 0 min.
V_{IL}	Input Voltage, Low	V	0 8 max.	0 8 max	0.8 max.				0 8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max [2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0 4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2 5 max						±12 5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min	−240 max −10 min.			−240 max −10 min.		−260 max −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1 6 mA
3. I load = −40 μA
4. V_{IN} = 0 4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0 36 mA

3

Analog Interface Characteristics

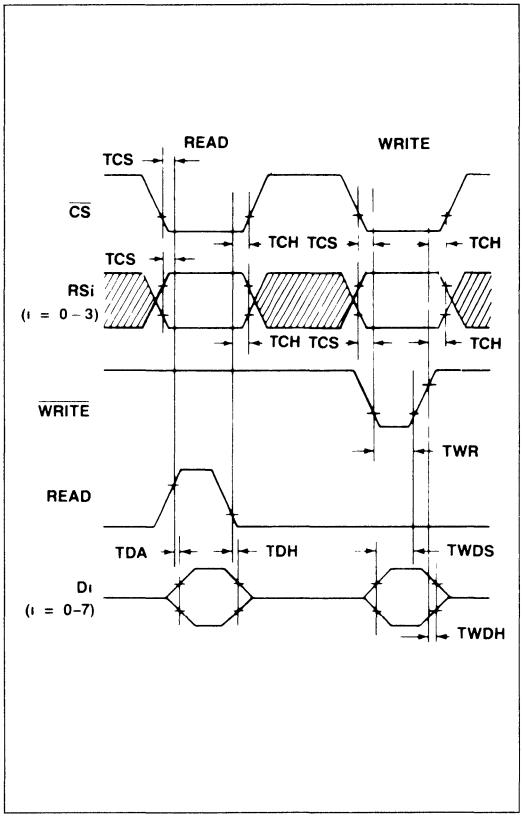
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3 03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726 43/(S + 11542 44) and 604 Ω series resistor are required
RXIN	AB	The receiver input impedance is greater than 1M Ω An external antialiasing filter with a transfer function of 19533 88/(S + 11542 44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are. $(-5\ VA - 0\ 3) \le V_{IN} \le (+5\ VA + 0.3)$

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE2	CABLE1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3 6 km
1	1	7 2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R48PCJ contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R48PCJ Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R48PCJ is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R48PCJ Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

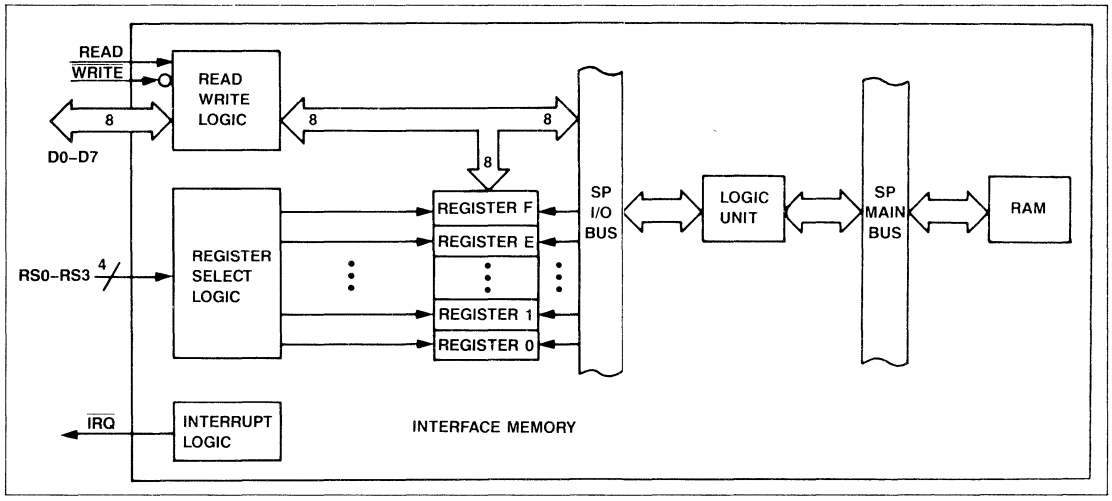
Six configurations are available in the R48PCJ modem: V.27 4800/2400 bps long/short train (four variations), V.21, and Tone. The configuration is selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is shown in the following table. All other codes represent invalid states.

Configuration Codes

CONF Code	Configuration
00	V.21
04	V.27, 2400 Long Train
05	V.27, 2400 Short Train
06*	V.27, 4800 Long Train
07	V.27, 4800 Short Train
08	Tone Mode
* Default value at POR.	

When the modem is initialized by power-on-reset, the configuration defaults to V.27 4800 bps long train. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at the baud rate (V.27 and V.21), 9600 times per second (tone generator), or 1600 times per second (tone detector).



R48PCJ Host Processor Interface

R48PCJ Interface Memory Map

Bit / Register	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	EPT	TPDM	TDIS	EQSV	EQFZ	SDIS	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	PN	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register / Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection The transmitter operates in either serial or parallel mode as selected by mode control bit C 5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1 The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R48PCJ is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{RTS}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R48PCJ Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
CDET	Carrier Detector	8:5	The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{\text{RLSD}}$ and deactivates one baud time after $\overline{\text{RLSD}}$.
CDIE	Channel Data Interrupt Enable	E:6	When set to a one, CDIE enables an $\overline{\text{IRQ}}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.
CDREQ	Channel Data Request	E:5	Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.
CONF	Configuration	D:0-7	The 8-bit field CONF controls the configuration of the modem according to the following table: **Hex Code** — **Configuration** 00 — V.21 04 — V.27, 2400 Long Train 05 — V.27, 2400 Short Train 06 — V.27, 4800 Long Train (Default) 07 — V.27, 4800 Short Train 08 — Tone All else — Invalid **Configuration Definitions** *V.21*—The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 Channel 2 modulation system. *Tone*—The modem sends single or dual frequency tones in response to the $\overline{\text{RTS}}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations. *V.27*—The modem is compatible with CCITT Recommendation V.27 ter.
DDIE	Diagnostic Data Interrupt Enable	E:2	When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.
DDREQ	Diagnostic Data Request	E:0	DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.
DDXL	Diagnostic Data X Least	2:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDXM	Diagnostic Data X Most	3:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDYL	Diagnostic Data Y Least	0:0-7	Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DDYM	Diagnostic Data Y Most	1:0-7	Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
EPT	Echo Protector Tone	C:6	When EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. EPT is not active if TDIS is on.
EQFZ	Equalizer Freeze	C:2	When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.
EQSV	Equalizer Save	C:3	When EQSV is a one, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training.
FED	Fast Energy Detector	B:5,6	FED consists of a 2-bit field that indicates the level of received signal according to the following code. **Code** — **Energy Level** 0 — None 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold While receiving a signal, FED normally alternates between Codes 2 and 3.

R48PCJ Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct GHIT returns to zero when the AGC output returns to normal
IA	Interrupt Active	E 7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level
PN	Period N	8:3	PN sets to a one at the start of the received PN sequence PN resets to zero at the start of the received scrambled ones. PN does not operate when TDIS is set to a one
RAMA	RAM Access	F·0-7	The RAMA register is written by the host when reading or writing diagnostic data. The RAMA code determines the RAM location with which the diagnostic read or write is performed.
RAMW	RAM Write	C.0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM RAMW is set to a zero by the host when reading RAM diagnostic data
RTSP	Request to Send Parallel	C.7	The one state of RTSP begins a transmit sequence The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem
RXCD	Receiver Channel Data	5 0-7	RXCD is written to by the modem every eight bit times This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ)
RX	Receive State	B 7	RX is a one when the modem is in the receive state (i e , not transmitting)
SDIS	Scrambler Disable	C 1	When SDIS is a one, the scrambler/descrambler is disabled. When SDIS is a zero, the scrambler/descrambler is enabled (default)
SETUP	Setup	E·3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i e , when changing CONF (D·0-7)
TDET	Tone Detected	A·7	The one state of TDET indicates reception of a tone The filter can be retuned by means of the diagnostic write routine.
TDIS	Training Disable	C·4	If TDIS is a one in the receive state, the modem is prevented from entering the training phase If TDIS is a one when $\overline{RTS}$ or RTSP go active, the generation of a training sequence is prevented at the start of transmission
TPDM	Transmitter Parallel Data Mode	C 5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input
TXCD	Transmitter Channel Data	4 0-7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one Data is transmitted as single bits in V.21 or as dibits in V 27 starting with bit 0 or dibit 0,1.

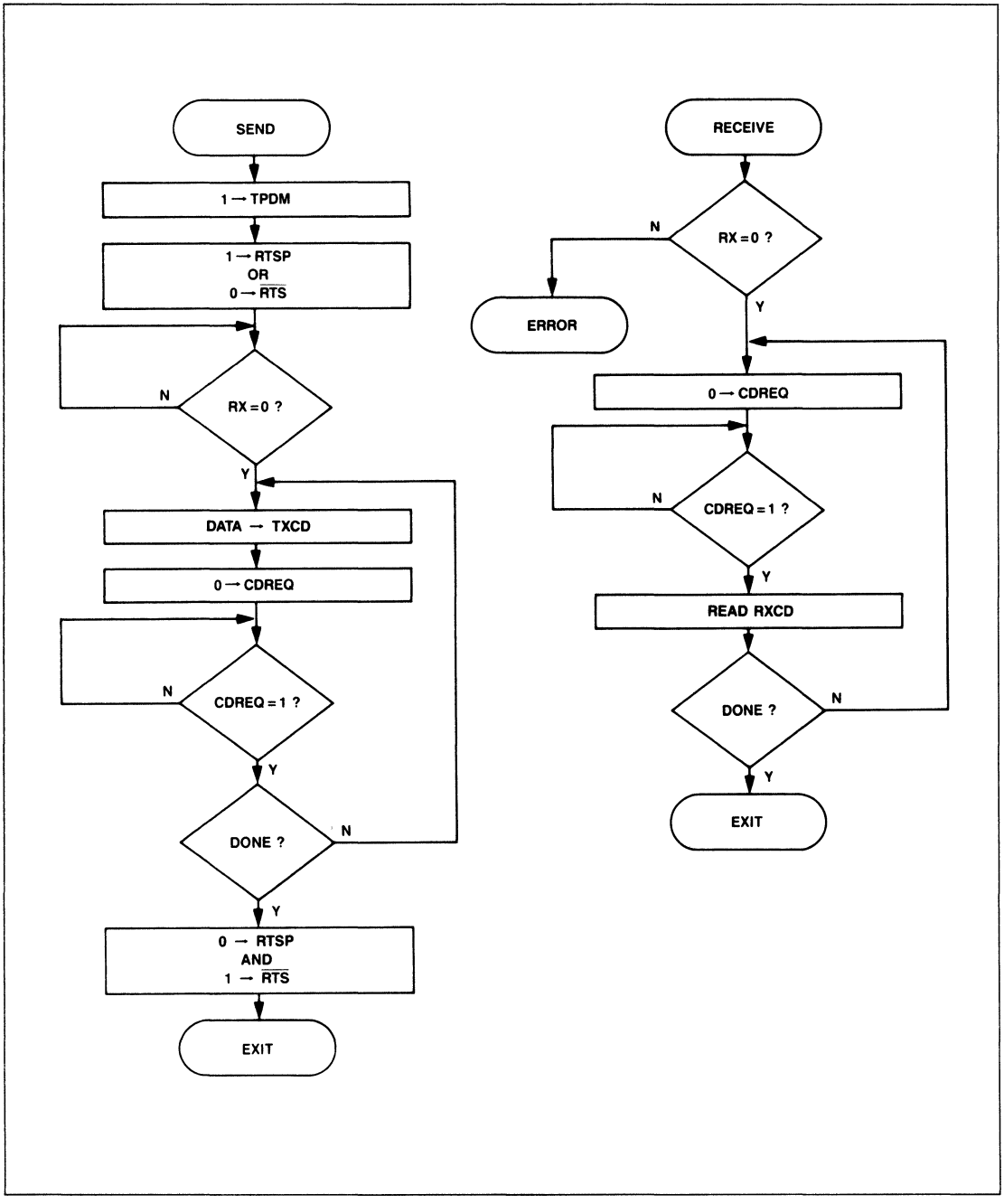
Diagnostic Data Transfer

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R48PCJ RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R48PCJ Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long. These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

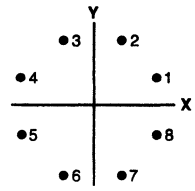
R48PCJ RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	87	2,3
2	Average Power	91	2,3
3	Receiver Sensitivity	47	0,1
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	63	0,1,2,3
6	Equalizer Tap Coefficients	23-32	0,1,2,3
7	Unrotated Equalizer Output	73	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	74	0,1,2,3
10	Error Vector	75	0,1,2,3
11	Rotation Angle	B3	2,3
12	Frequency Correction	8B	2,3
13	EQM	89	2,3
14	Alpha (α)	38	0,1
15	Beta One (β_1)	39	0,1
16	Beta Two (β_2)	3A	0,1
17	Alpha Prime (α')	3B	0,1
18	Beta One Prime (β_1')	3C	0,1
19	Beta Two Prime (β_2')	3D	0,1
20	Alpha Double Prime (α'')	B8	2,3
21	Beta Double Prime (β'')	B9	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1

R48PCJ Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 – [(AGC Gain Word/64) × 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$, For –43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code 47
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = $[65.4\ (10^A)]^2/2$ where: $A = (P_{OFF} - P_{ON} - 0.5)/20$ P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84.

R48PCJ Diagnostic Data Scaling (Cont'd)

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers. Value (Hex) Point X Y 1 1D00 0C00 2 0C00 1D00 3 F400 1D00 4 E300 0C00 5 E300 F400 6 F400 E300 7 0C00 E300 8 1D00 F400 
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) × 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) × Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application.
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 6.8267 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.

POWER-ON INITIALIZATION

When power is applied to the R48PCJ, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.27/4800 bps, serial mode, training enabled, echo protector tone enabled, interrupts disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for -43.5 dBm, receiver turn-off threshold set for -47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V 21 type modem, the R48PCJ provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of -20 dBm.

RECEIVED SIGNAL FREQUENCY TOLERANCE

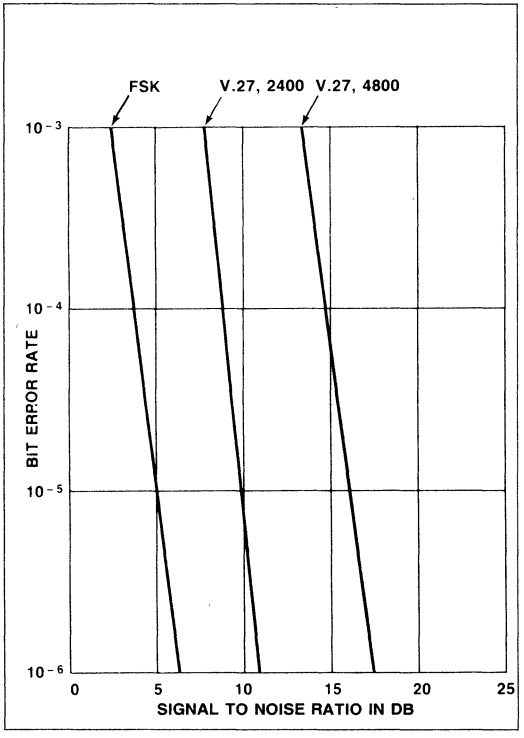
The receiver circuit of the R48PCJ can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

TYPICAL PHASE JITTER

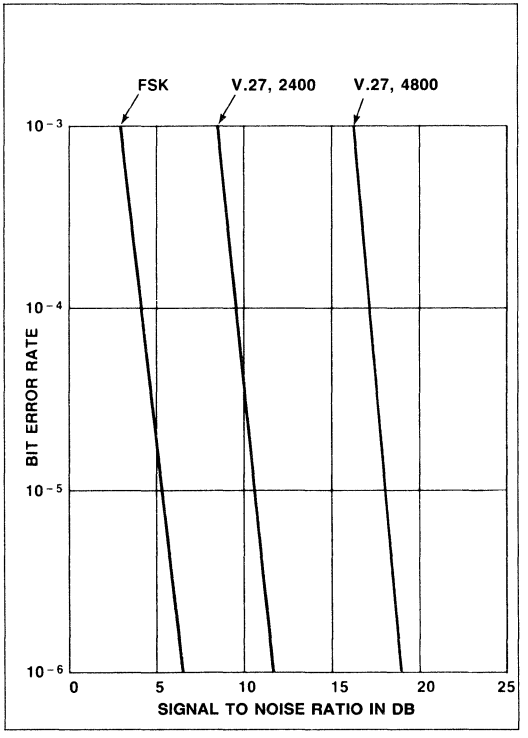
At 4800 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 2400 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

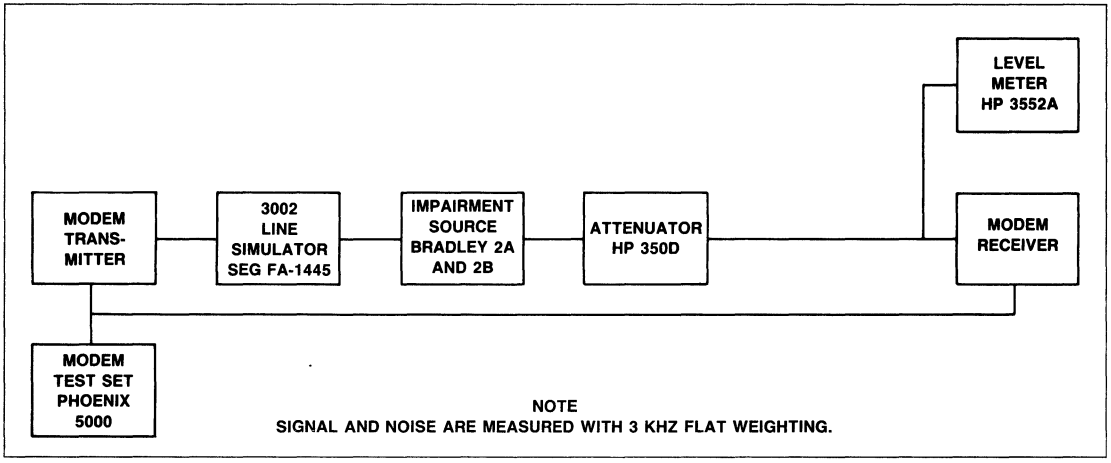


Typical Bit Error Rate (Back-to-Back, Level -20 dBm)



Typical Bit Error Rate (Unconditioned 3002 Line, Level -20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

APPLICATION

Recommended Modem Interface Circuit

The R48PCJ is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434 0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I T T
R9	CRB¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R48PCJ and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R48PCJ, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R48PCJ package Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R48PCJ package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R48PCJ package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side The sides may be reversed to match a particular OEM requirement.
11. Routing of R48PCJ signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
	51	47		
	52	48		
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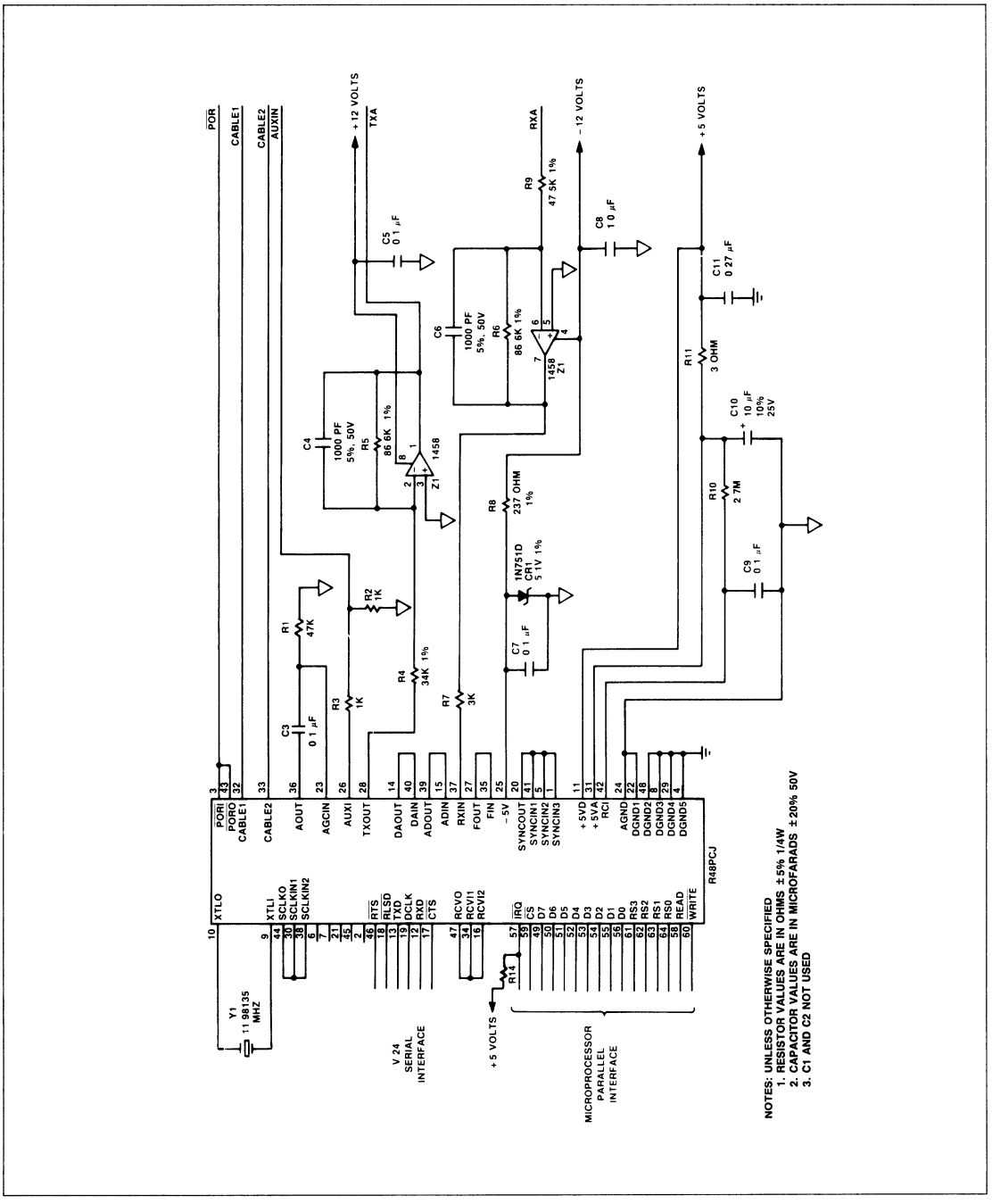
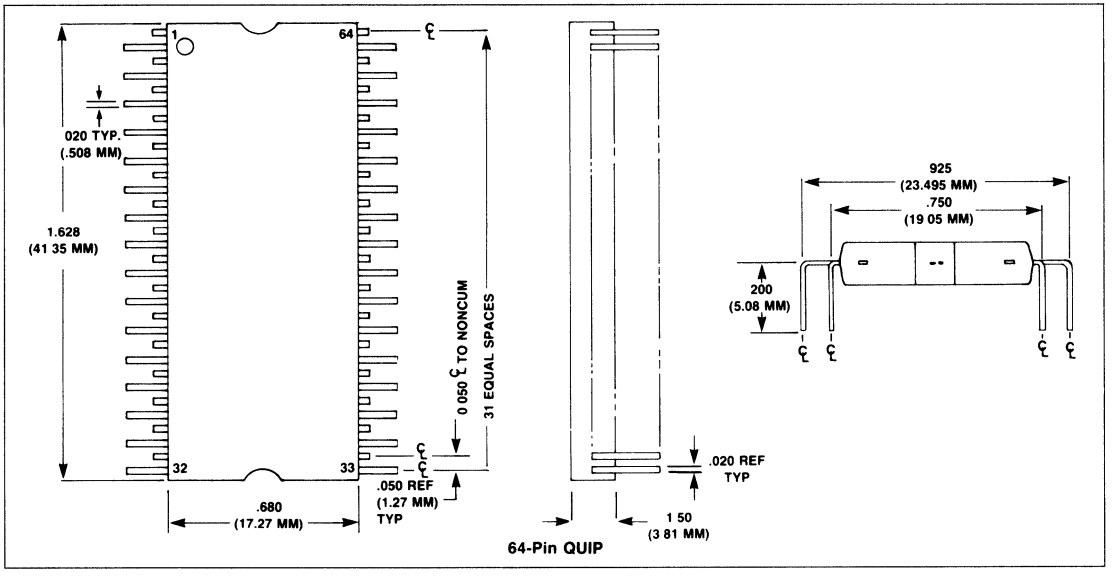


Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



Rockwell

R24/48MEB
Modem Evaluation Board

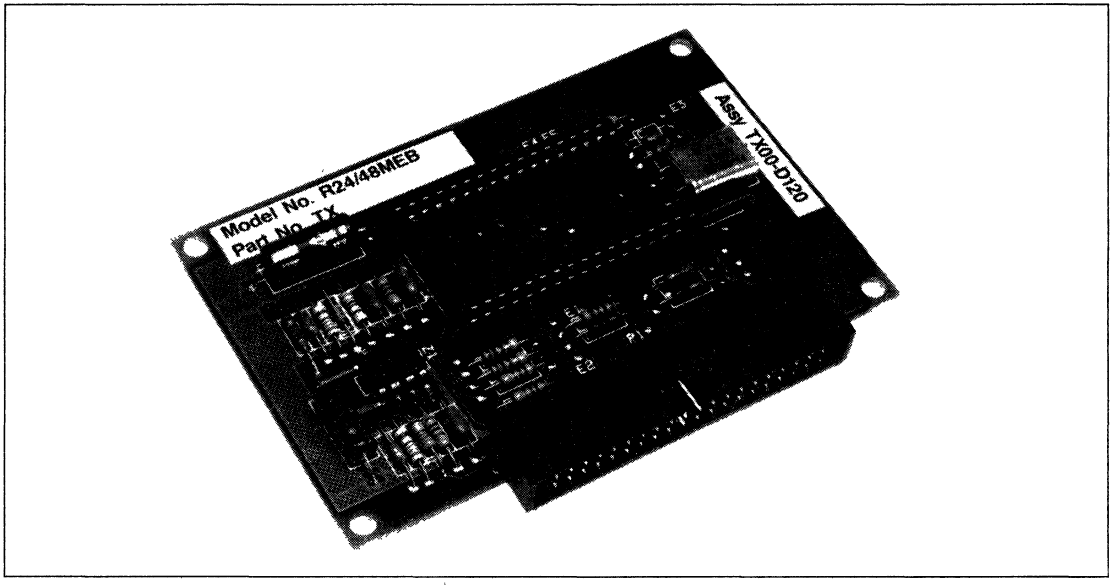
INTRODUCTION

The Rockwell R24/48MEB Modem Evaluation Board (MEB) aids the original equipment manufacturer (OEM) during the evaluation and design in phases of product development. Modems supported by the R24/48MEB include the R24MFX, R24BKJ, R48MFX, and R48PCJ. The Modem Evaluation Board contains a socket (U1) for mounting the 64-pin quad in-line package (QUIP) of the selected modem, plus support circuitry to configure a complete data pump. For operation over the public switched telephone network (PSTN), an appropriate line termination, such as a data access arrangement (DAA), must be provided externally.

The R24/48MEB physical and electrical interface is compatible with the Rockwell R96FAX modem. For users of the R96FAX, this feature provides a rapid means of preparing to evaluate a 64-pin QUIP modem. Equipment previously developed for use with the R96FAX can be converted for use with the R24/48MEB by changing only the software.

FEATURES

- Convenient evaluation method for
  - R24MFX
  - R24BKJ
  - R48MFX
  - R48PCJ
- Exercises all modem functions
- Easily integrated into a prototype system
- Cost effective for low volume production applications
- Standard 40-pin flat ribbon connector
- Backward compatible with R96FAX hardware
- Low power consumption: 1.5W (typical)
- Small size: 100 mm x 65 mm (3.94 in. x 2.56 in.).



R24/48MEB Modem Evaluation Board

TECHNICAL SPECIFICATION

For a description of the R24/48MEB characteristics with a 64-pin QUIP modem installed in socket U1, refer to the corresponding modem data sheet.

Modem Number	Data Sheet Order Number
R24MFX	MD17
R24BKJ	MD20
R48MFX	MD19
R48PCJ	MD21

CIRCUIT DESCRIPTION

INTERFACE CIRCUITS

The circuitry and design rules used to create the R24/48MEB follow the recommended modem interface and PC board layout considerations published in the associated 64-pin QUIP modem data sheet. The circuit card can be used as a guide in host PC board design.

Refer to the R24/48MEB schematic diagram (Figure 2) during the following description. The modem being evaluated is inserted in the 64-pin QUIP socket (U1). Various overhead connections between QUIP pins are completed by circuits on the evaluation board. Some of these overhead signals are connected to test points (E3, E4, E5) or connector pins (P1-11, P1-12, P1-22, P1-24) for use in Rockwell production test. These signals are not intended for use by the host equipment.

Modem signals that form the user interface on connector P1 (Table 1) are divided into five categories: Power, Microprocessor Interface, V.24 Interface, Cable Equalizer, and Analog Signals. The column titled "Type" refers to designations found in the digital and analog interface characteristics tables (Tables 2 and 3). The five categories are defined in the following paragraphs.

Power

Power signals include ± 12 volts, +5 volts, ground and $\overline{POR}$. The ± 12 volt supplies provide power for analog circuits and should be free from switching transients normally associated with digital circuits. The +5 volt source provides power for digital circuits and can be driven by the host logic supply.

The common reference point for all signals, both digital and analog, is modem ground (pins 14 and 39). These pins provide the power supply return points for all voltages and should be used as reference for transmitter and receiver signals. To minimize noise problems, circuits that interface to the modem should maintain their ground references as close as possible to the same potential as modem pins 14 and 39. Digital signals and analog signals should be referenced to modem ground via separate connections to prevent digital noise from appearing on analog signals due to a common ground impedance.

In order to reduce the effect of noise coupled through direct current (DC) power lines, decoupling capacitors are recommended on all power inputs. Each supply input should be decoupled to signal ground (pins 14 and 39) by a parallel set of capacitors.

Table 1. R24/48MEB Connector Interface Signals

Name	Type	Pin No.	Description
A. POWER:			
Ground	GND	14, 39	Power Supply Return
+5 volts	PWR	3, 4	+5 volt supply
+12 volts	PWR	26	+12 volt supply
−12 volts	PWR	37	−12 volt supply
$\overline{POR}$	I/OB	36	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	7	Data Bus (8 Bits)
D6	I/OA	5	
D5	I/OA	9	
D4	I/OA	31	
D3	I/OA	15	
D2	I/OA	28	
D1	I/OA	23	
D0	I/OA	29	
RS3	IA	30	Register Select (4 Bits)
RS2	IA	8	
RS1	IA	27	
RS0	IA	10	
$\overline{CS}$	IA	6	Chip Select
$\overline{READ}$	IA	1	Read Enable
$\overline{WRITE}$	IA	2	Write Enable
$\overline{IRQ}$	OB	32	Interrupt Request
C. V.24 INTERFACE:			
$\overline{DCLK}$	OC	13	Data Clock
$\overline{RTS}$	IB	19	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	20	Transmitter Data
RXD	OC	21	Receiver Data
$\overline{RLSD}$	OC	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IC	33	Cable Select 1
CABS2	IC	34	Cable Select 2
E. ANALOG SIGNALS:			
TXA	AA	38	Transmitter Analog Output
RXA	AB	40	Receiver Analog Input
AUXIN	AC	35	Auxiliary Analog Input

Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

A large value capacitor of 10 microfarads or greater should be paralleled by a low inductance small value capacitor of 0.1 microfarads.

Because the modem uses switched capacitor filters, the noise floor can be degraded as the result of high frequency noise aliased into the passband by beating with the switched capacitor clock. For this reason, use of linear power supplies, rather than switching power supplies, is recommended where low level reception (i.e., around −40 dBm) is anticipated. If switching power supplies are used, extra care must be taken to keep switching noise out of the modem. The following techniques have proven helpful in designing systems using switching supplies.

1. In addition to the decoupling capacitors on all modem power inputs, the power supply output leads should be wrapped around a toroidal core to increase series inductance. This technique blocks the conducted high frequency noise from the switching supply.

Table 2. Digital Interface Characteristics

Symbol	Parameter	Units	Type							
			Input			Output			Input/Output	
			IA	IB	IC	OA	OB	OC	I/OA	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current	μA		−240 max.	−240 max.			−240 max.		−260 max.
	(Short Circuit)			−10 min.	−10 min.			−10 min.		−100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

Table 3. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 47.5K ohms ±1%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above half the sample rate will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −0.4 dB ±1 dB.

2. A ground plane should be inserted between the modem and the power supply. This technique reduces radiated EMI pickup by modem circuits.

3. Shield analog signals in coaxial wire. Signals TXA (pin 38), RXA (pin 40), and AUXIN (pin 35) should be shielded. Signal AUXIN should be tied to ground (pin 39) if not used.

By following these procedures, satisfactory performance over the full dynamic range should be realized even when switching power supplies must be used.

When the modem is initially energized a signal called Power-On Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives pin 36 to ground during the beginning of the POR sequence. Approximately 10 milliseconds after the low to high transition of pin 36, the modem is ready for normal use. The POR sequence is reinitialized anytime the +5 volt supply drops below +3.0 volts for more than 30 milliseconds, or an external device drives pin 36 low for at least 3 microseconds.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0–RS3), data (D0–D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. The microprocessor interface timing waveforms are shown in Figure 1 and the microprocessor interface timing requirements are listed in Table 4. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the referenced data sheet of each 64-pin QUIP modem.

V.24 Interface

Six hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels. These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

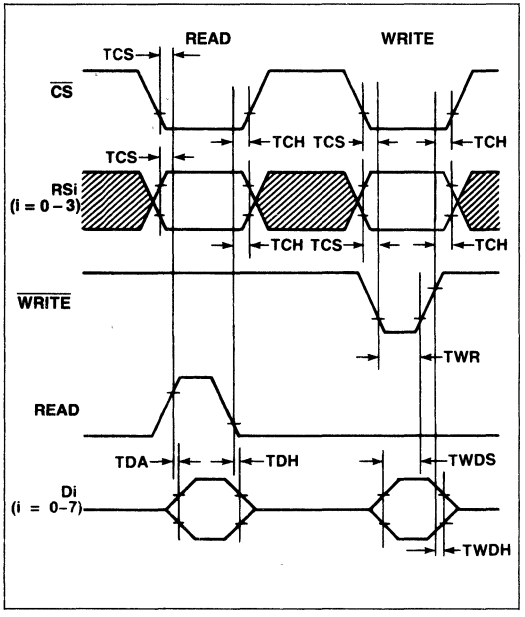


Figure 1. Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. The low (0) and high (1) states of signals CABS1 and CABS2 that are necessary to select each of the cable equalizer options are defined in Table 5.

Analog Signals

Three connector pins are devoted to analog audio signals: TXA, RXA, and AUXIN. The TXA (transmitter analog) line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier. In order to match this output to a standard telephone load of 600 ohms, a series resistor is required. A value of 604 ohms ±1% is recommended.

The RXA (receiver analog) line is an input to the receiver from an audio transformer or data access arrangement. The input impedance is 47.5K ohms ±1%. The RXA input must be shunted by an external resistor in order to match a 600 ohms source. The 604 ohms ±1% resistor recommended for the transmitter is also suitable for the receiver.

The last analog connection is the input AUXIN. This line provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit. Any signal above half the sample rate on the AUXIN line will be aliased back into the passband as noise.

Table 4. Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to Read or $\overline{WRITE}$	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
$\overline{WRITE}$ strobe pulse width	TWR	75	—	NS

Table 5. Cable Equalizer Selection

CABLE1	CABLE2	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

MEB SUPPORT CIRCUITS

The modem evaluation board with a 64-pin QUIP modem installed forms a complete data pump ready for interfacing to a host microprocessor (Figure 3). The host electronics must provide data and timing on the microprocessor interface pins to allow normal modem configuration and option selection plus status monitoring. Additional circuitry is recommended to allow generation of an eye pattern for diagnostic purposes (Figure 6). A commercially available modem test set (e.g., Phoenix 5000) can be connected directly to the V.24 serial interface (using TTL levels) or can be buffered with DS1488 and DS1489 type drivers and receivers for operation with standard RS-232 levels.

Schematic diagrams are provided for the RS-232 buffer circuit (Figure 4) and the microprocessor bus interface with eye pattern output (Figure 5). Note that the data clock signal must drive both the transmitter clock and the receiver clock and is therefore buffered to reduce the load on the R24/48MEB pin 13. Also note that an SN74121 is used to shorten the write pulse in order to meet data hold time requirements for the NE5018 devices. The 100 ohm resistors in series with modem signals are required only when driving several feet of cable where excessive ringing may require damping. The address decode logic places the modem registers between locations 9000 and 900F hexadecimal. The eye pattern DAC's are at locations 9071 and 9072.

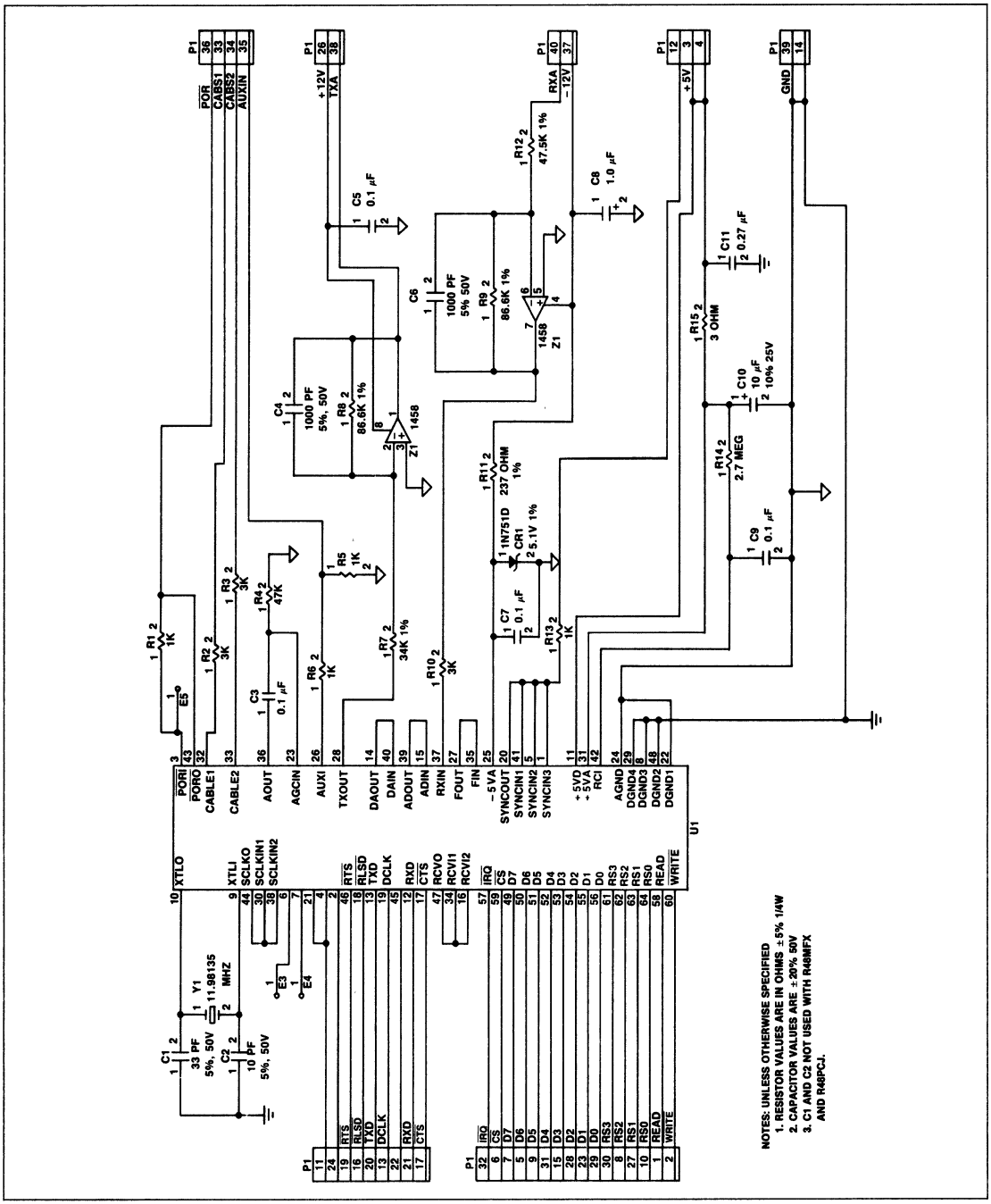


Figure 2. R24/48MEB Schematic Diagram

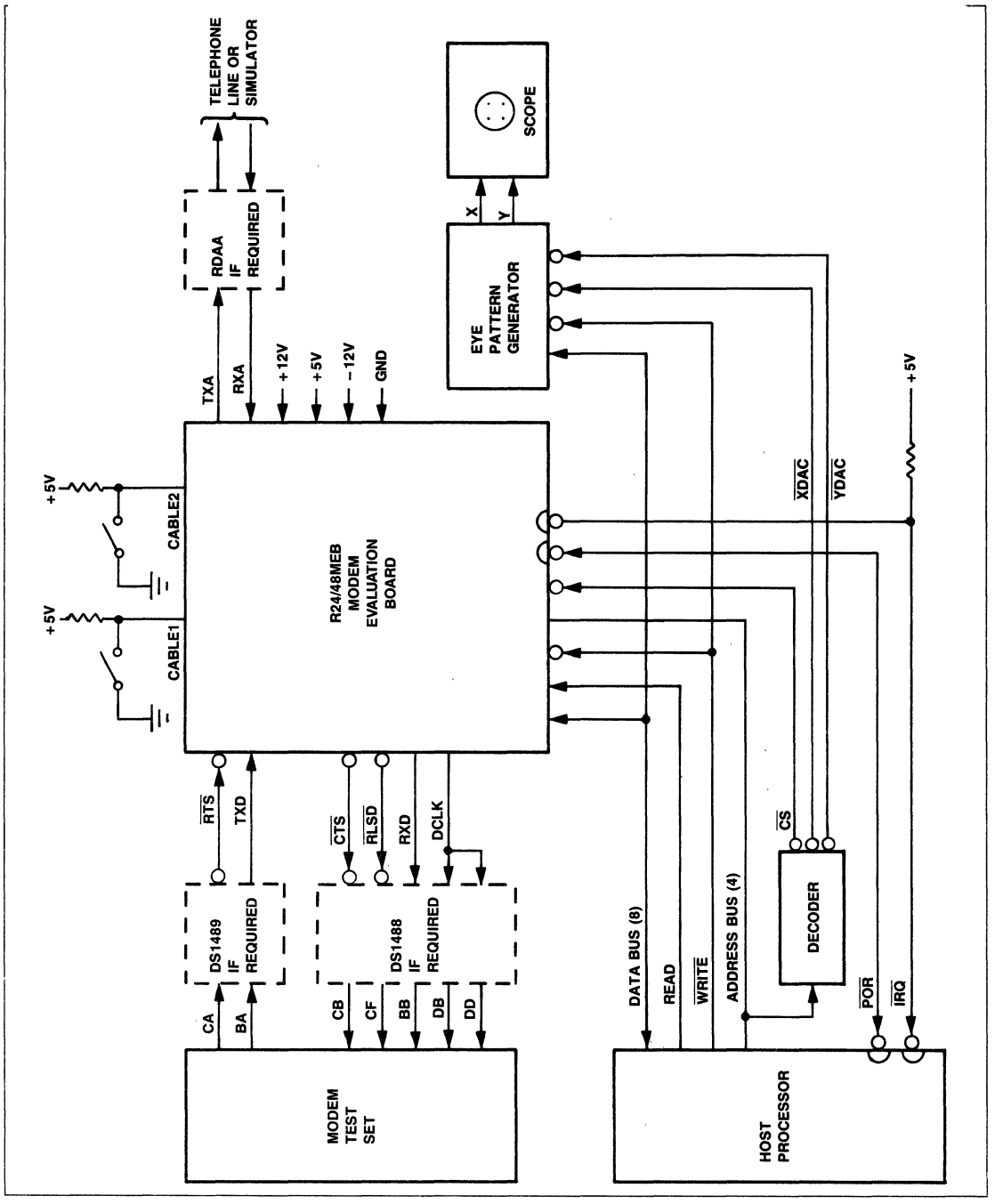


Figure 3. R24/48MEB Functional Interconnect Diagram

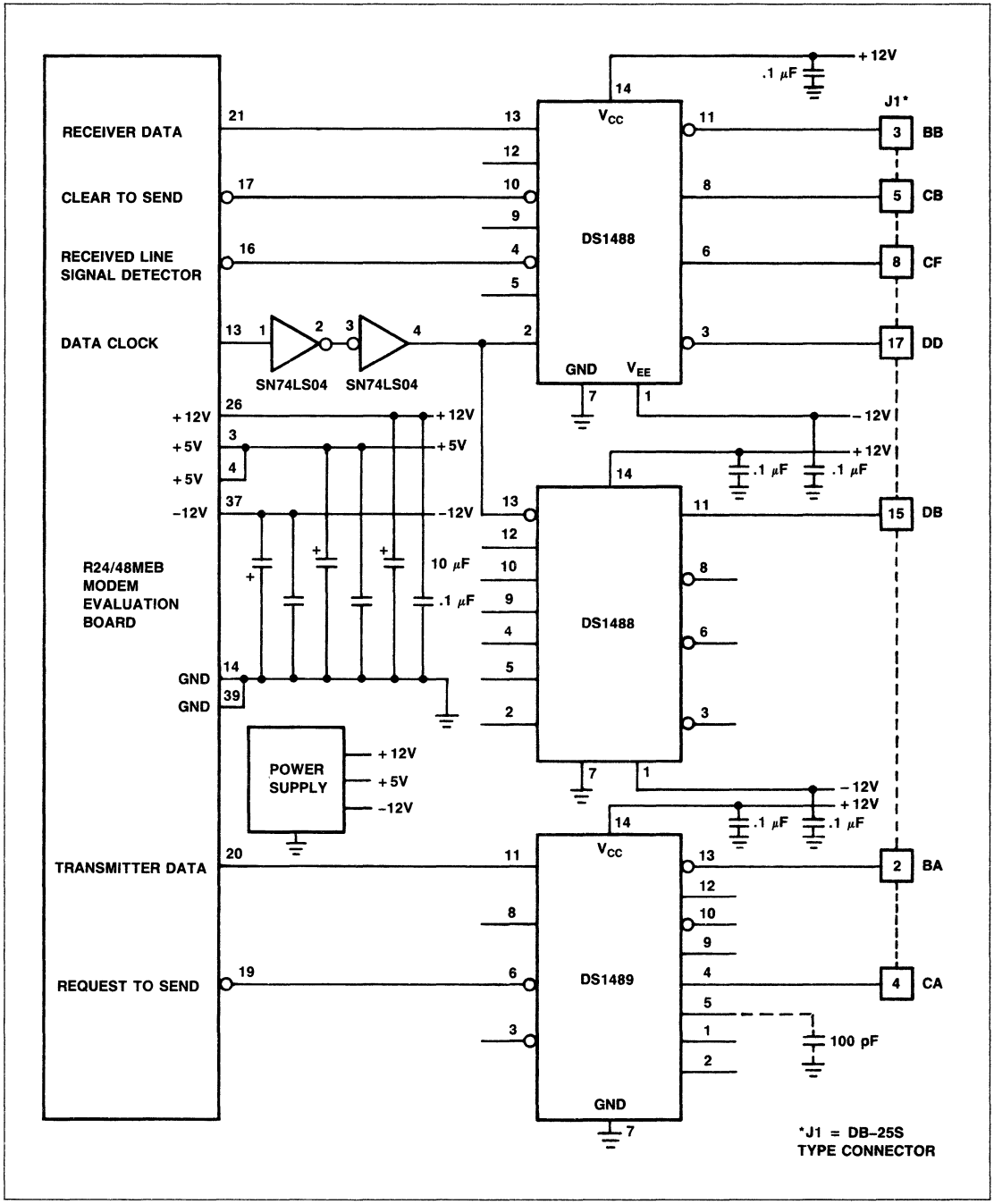


Figure 4. RS-232 Buffer Circuit

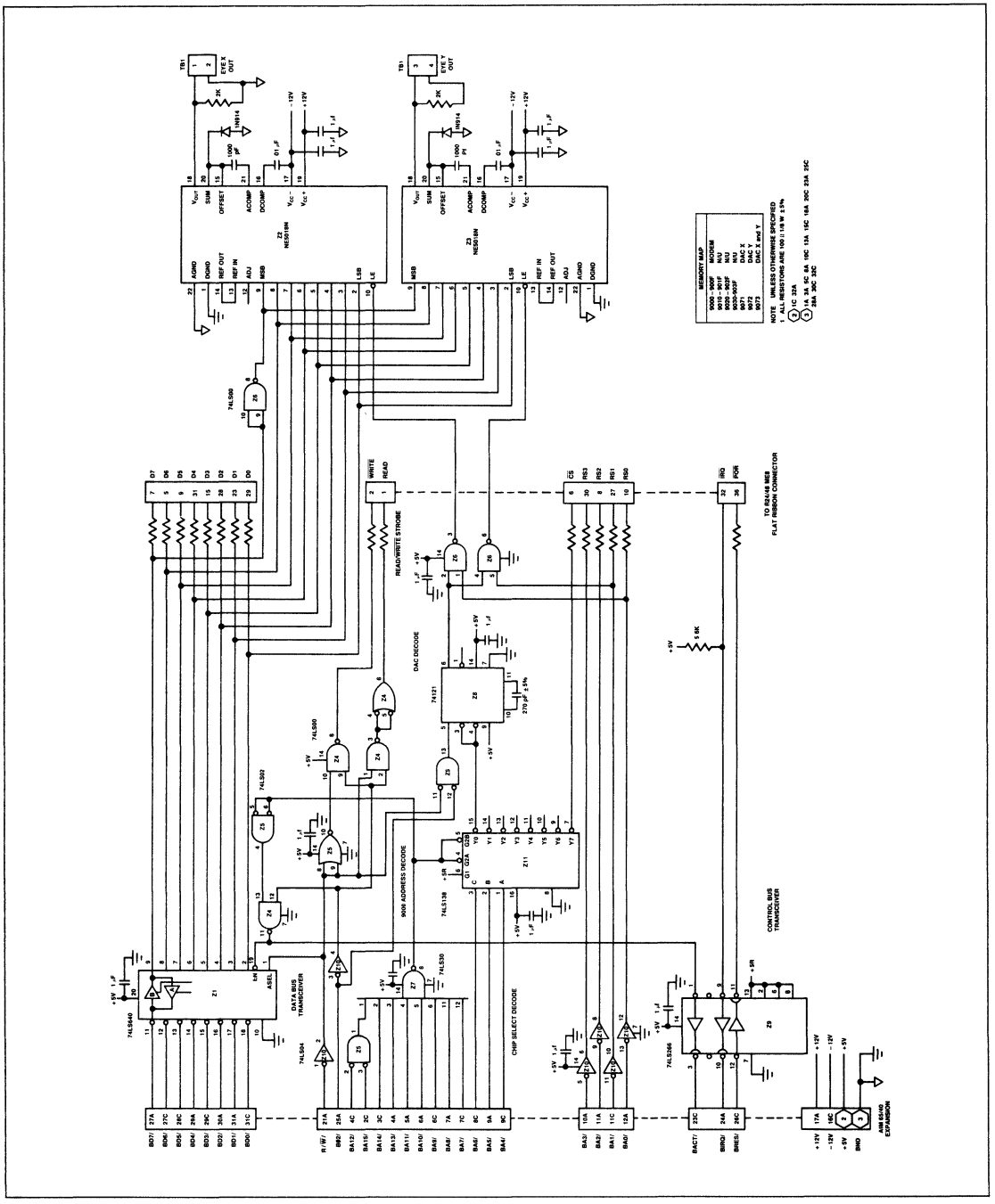


Figure 5. R24/48MEB Microprocessor Bus Interface with Eye Pattern Output

MODEM EVALUATION

EYE PATTERN

The eye pattern is an oscilloscope display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

In quadrature amplitude modulation (QAM), two multilevel amplitude modulated (AM) carriers are transmitted simultaneously. Interference between these two modulated carriers is minimized by using carriers of identical frequency with a constant 90° relative phase angle. After demodulation, the multilevel baseband signals can be displayed on an oscilloscope with the set of levels received on one carrier displayed on the X axis and the set of levels received on the other carrier displayed on the Y axis. Since these signals consist of discrete levels sent at high data rates, the resulting oscilloscope pattern appears to be a fixed set of points.

Figures 6a through 6d illustrate four examples of an eye pattern. Figure 6a shows the location of four ideal points corresponding to a signal structure using 0 and ±1 for the three amplitude levels. One such signal structure is CCITT Recommendation V.27 at 2400 bits per second. The dashed lines superimposed on the eye pattern represent decision boundaries used by the receiver in deciding which ideal point corresponds to the actual received point. Although the transmitter sends ideal points, line impairments cause the received points to be misaligned. Figure 6b shows the effect of random noise. The received points cluster around the ideal location, but are randomly offset from the ideal point by the noise causing undesired signal modulation. The random offsets are a result of the random nature of the noise. If the line impairment is not random but periodic or is a function of the received signal itself (e.g., harmonic distortion) then the distribution of points around the ideal location is not random. Figure 6c illustrates the tangential smearing resulting from phase jitter and Figure 6d shows the effect of amplitude distortion (either gain jitter or harmonic distortion). The magnitude of the spreading is directly proportional to the severity of the impairment, and represents the quality of the signal or the likelihood of errors in the received data.

Consult the Eye Pattern Generation Flowchart (Figure 7) for an example of eye pattern generation using the address structure indicated in the eye pattern output schematic.

BIT ERROR RATE

Bit Error Rate (BER) is a measure of the steady-state transfer of data on the communication channel. It is the ratio of the number of received bits in error to the number of transmitted bits. This number increases with decreasing signal-to-noise ratio (SNR). The type of line disturbance and the modem configuration also affect the BER.

The BER Performance Test Set-up (Figure 8) illustrates a method of measuring BER in accordance with CCITT Recommendation V.56. The band-limited noise level should be adjusted by the noise attenuator to give the desired signal to noise ratio for the selected received signal level. The modem transmitter is then caused to send a 511-bit pseudo random test pattern. The signal attenuator is set for a received signal level of −20 dBm to simulate leased line operation or −30 dBm to simulate switched network operation. In leased line testing the line simulator should be 3002-C1 or 3002-C2 conditioned.

Once the receiver has trained (as indicated by a stable eye pattern) the BER test can begin. A large enough number of bits should be sent to cause at least 10 bit errors to be recorded. BER is calculated by dividing the number of bits in error by the number of bits sent.

The impairment source can be adjusted to provide phase-jitter or frequency offset, etc. The BER tests can be repeated in the presence of these line impairments to determine the amount by which performance has degraded. All BER tests should be conducted under steady-state conditions; i.e., after the adaptive equalizer has stabilized.

Transient response can be measured by using very short polling messages and comparing the number of attempts to send a message with the number of error free messages received for a specific signal to noise ratio and line condition. This type of testing is called block-error-rate (BLER) and can be performed using the same test set-up as bit-error-rate.

Data throughput for a specific application is determined by a combination of bit-error-rate and block-error-rate. Depending on system architecture, line conditions, error control method used, etc., an optimum message length can be chosen to maximize throughput. As messages become shorter, block-error-rate becomes the limiting factor. As messages become longer, bit-error-rate becomes the limiting factor.

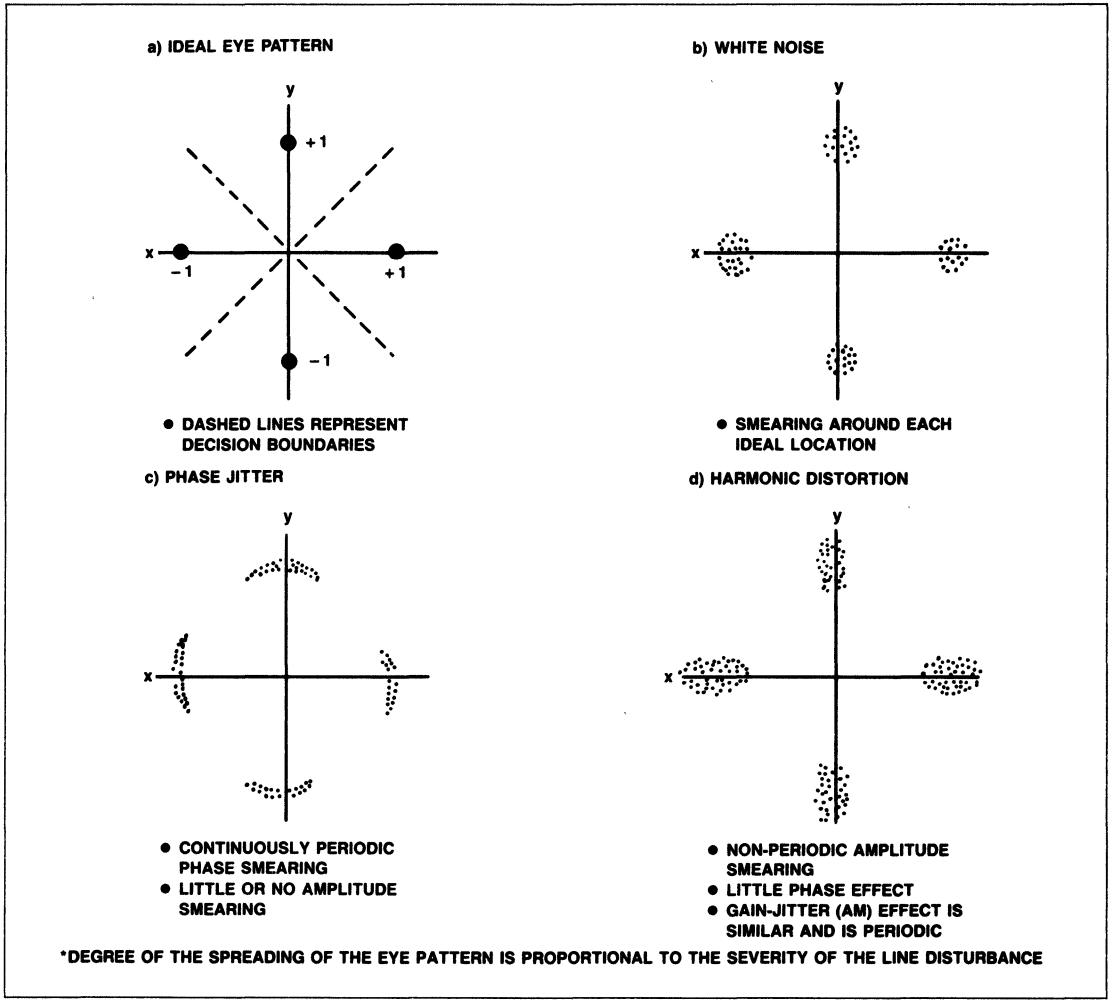


Figure 6. Four Point Eye Patterns

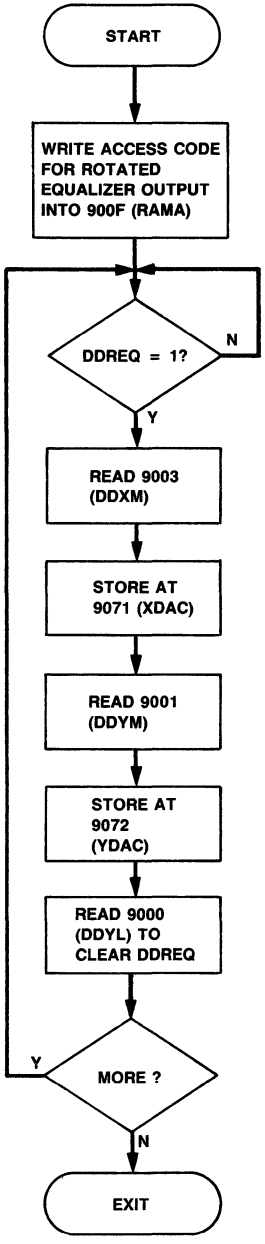


Figure 7. Eye Pattern Generation Flowchart

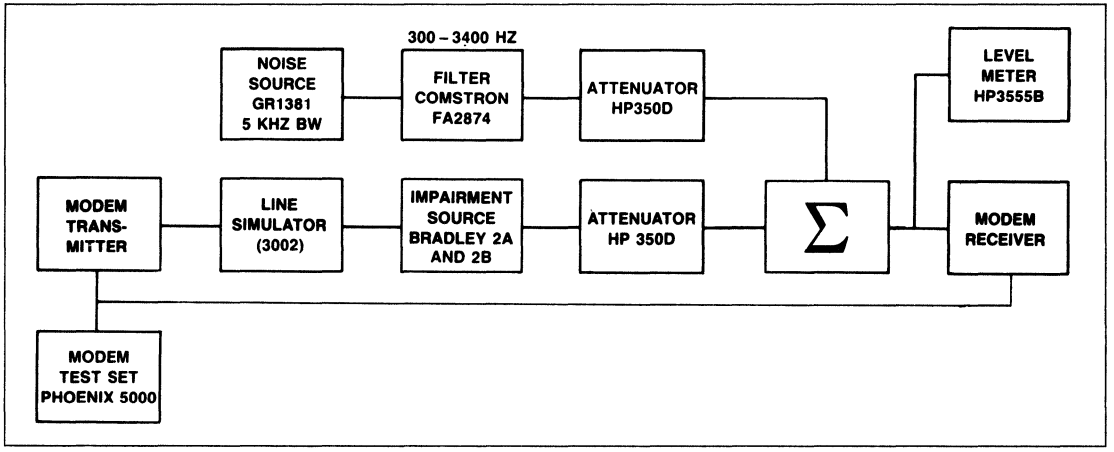


Figure 8. BER Performance Test Set-up

GENERAL SPECIFICATIONS

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	200 mA	<300 mA
+12 Vdc	±5%	5 mA	<10 mA
−12 Vdc	±5%	30 mA	<50 mA

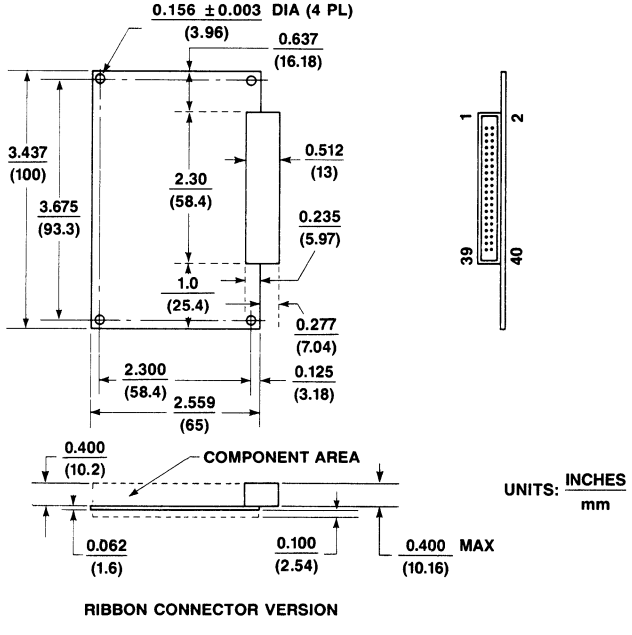
Note: All voltages must have ripple ≤0 1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins Burndy FRS 40BS8P or equivalent mating connector
Dimensions	
Width	3.937 in (100 mm)
Length	2.559 in (65 mm)
Height	0.40 in. (10 2 mm)
Weight (max.)	2.6 oz. (73 g)
Lead Extrusion (max.)	0.100 in (2.54 mm)



RIBBON CONNECTOR VERSION

R24/48MEB Dimensions and Pin Locations

R96MFX
9600 bps MONOFAX® Modem

INTRODUCTION

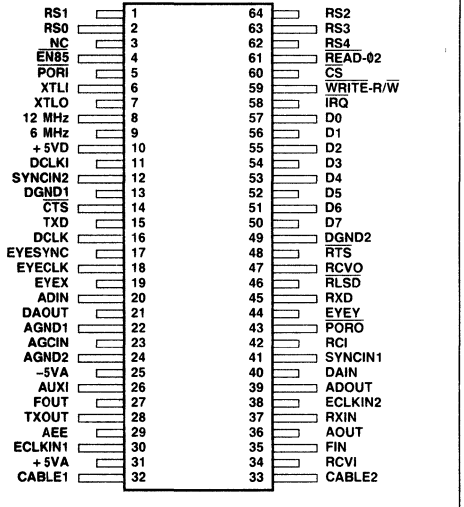
The Rockwell R96MFX MONOFAX is a synchronous 9600 bits per second (bps) half-duplex modem in a single 64-pin quad-in-line package (QUIP). The R96MFX can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, V.21 Channel 2, T.3, and T.4, and the binary signaling requirements of T.30. The R96MFX can operate at speeds of 9600, 7200, 4800, 2400 and 300 bps.

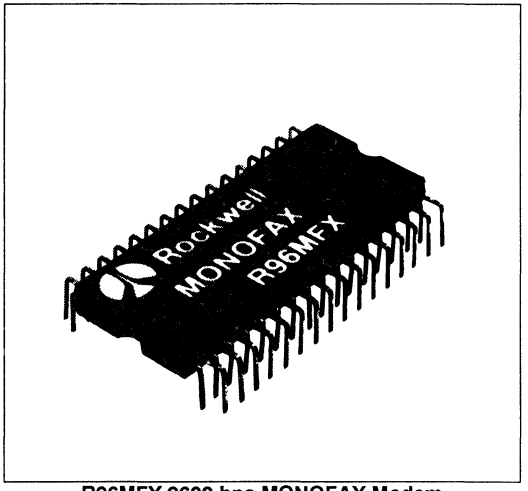
The R96MFX is designed for use in Group 3 and Group 2 facsimile machines. The modem's small size and low power consumption allow the design of compact system enclosures for use in both office and home environments.

FEATURES

- Single 64-pin QUIP
- CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
- Group 3 and Group 2 Facsimile Transmission/ Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Programmable Turn-on and Turn-off Thresholds
- Programmable Transmit Output Level
- Diagnostic Capability
  - Allows Telephone Line Quality Monitoring
- Equalization
  - Automatic Adaptive
  - Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - Selectable Microprocessor Bus (6500 or 8085)
  - CCITT V.24 (RS-232-C Compatible) Interface
- TTL and CMOS Compatible
- Low Power Consumption: 500 mW (Typical)



R96MFX Pin Assignments



R96MFX 9600 bps MONOFAX Modem

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

TONE GENERATION

Under control of the host processor, the modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

DATA ENCODING

The data encoding conforms to CCITT recommendations V.29, V.27, V.21 Channel 2, and T.3.

CABLE EQUALIZERS

Equalization functions are provided that improve performance when operating over low quality lines.

The integrated analog section of the R96MFX has selectable cable equalizers with the characteristics shown in Table 2. Choose specific cable equalizers by strapping CABLE1 and CABLE2 to either +5V or GND (see Hardware Interface). The chosen filter functions in both transmit and receive paths depending on operating mode.

ADAPTIVE EQUALIZER

An adaptive equalizer in V.29 and V.27 modes compensates for transmission line amplitude and group delay distortion.

TRANSMITTED DATA SPECTRUM

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response (FIR) filter with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter. This filter shapes the spectrum so that with continuous binary ones applied, the resulting transmitted spectrum has a substantially linear phase characteristic over the band of 700 Hz to 2700 Hz, and the energy density at 500 Hz and 2900 Hz is attenuated 4.5 ± 2.5 dBm with respect to the maximum energy density between 500 Hz and 2900 Hz.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter. This filter shapes the spectrum so that with continuous binary ones applied, the resulting transmitted spectrum has a substantially linear phase characteristic, and the energy density at 1000 Hz and 2600 Hz is attenuated 3.0 ± 2.0 dBm with respect to the maximum energy density between 1000 Hz and 2600 Hz.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter. This filter shapes the spectrum so that with continuous binary ones applied, the resulting transmitted spectrum has a substantially linear phase characteristic, and the energy density at 1200 Hz and 2400 Hz is attenuated 3.0 ± 2.0 dBm with respect to the maximum energy density between 1200 Hz and 2400 Hz.

Table 2. Cable Equalizer Characteristics

Frequency (Hz)	Gain dB Relative to 1700 Hz for Length of 0.4 mm Cable			
	0	1.8 km	3.6 km	7.2 km
700	0.00	–0.99	–2.39	–3.93
1500	0.00	–0.20	–0.65	–1.22
2000	0.00	+0.15	+0.87	+1.90
3000	0.00	+1.43	+3.06	+4.58

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits per Symbol	Constellation Points
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 4800	DPSK	1800	4800	1600	3	8
V.27 2400	DPSK	1800	2400	1200	2	4
V.21 300	FSK	1650,1850	300	300	1	–
T.3 (Group2) Single and Dual Tone Transmit	VSAMPM	2100	–	–	–	–

Notes: 1. Modulation legend:
QAM Quadrature Amplitude Modulation
DPSK Differential Phase Shift Keying
FSK Frequency Shift Keying
VSAMPM Vestigial Sideband Amplitude Modulation - Phase Modulation

The transmit spectrum characteristics assume that the cable equalizers are disabled.

The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range are below –55.0 dBm.

TURN-ON AND TURN-OFF SEQUENCES

Transmitter turn-on and turn-off sequence times are shown in Table 3.

TRANSMIT LEVEL

The transmitter output level is programmable in the DSP RAM from 0 dBm to –15.0 dBm and is accurate to ± 1.0 dBm. The output level is adjusted by the modem by digitally scaling the output to the transmitters digital-to-analog converter.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with CCITT V.29 or V.27 recommendations, depending on the selected configuration.

RECEIVE LEVEL

The receiver satisfies V.29 and V.27 performance requirements for received line signal levels from 0 dBm to –43 dBm. An external input buffer and filter must be supplied between the Receiver Analog Input (RXA) and RXIN. The received line signal level is measured at the RXA input. The default turn on and turn off $\overline{\text{RLSD}}$ threshold levels are – 43 dBm and – 48 dBm, respectively. These levels are measured with an unmodulated 2100 Hz tone at RXA.

The RLSD threshold levels can be programmed over the following range:

Turn on: –10 dBm to –47 dBm
Turn off: –10 dBm to –52 dBm

RECEIVER TIMING

The timing recovery circuit can track a ± 0.01% frequency error in the associated transmit timing source.

CARRIER RECOVERY

The carrier recovery circuit can track a ± 7 Hz frequency offset in the received carrier with less than a 0.2 dBm degradation in bit error rate (BER).

Table 3. Turn-Off/Turn-On Sequences

	$\overline{\text{RTS}}$ On to $\overline{\text{CTS}}$ On		Turn Off Time from $\overline{\text{RTS}}$ Off*	
Configuration	Echo Protector Tone Disabled	Echo Protector Tone Enabled	Remaining Data and Scrambled 1s	No Transmitted Energy
V.29 (All Speeds)	253 ms	441 ms	5 ms	20 ms
V.27 4800 bps	708 ms	913 ms	7 ms	20 ms
V.27 2400 bps	943 ms	1148 ms	10 ms	20 ms
V.21 300 bps	≤14 ms	≤14 ms	–	–
Group 2	≤400 µs	≤400 µs	–	–

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off.

TONE DETECTION

The tone detector signal path is separate from the main received signal path enabling tone detection to be independent of the receiver status. Tone detector 3 operates in all receive modes.

The filter coefficients of each filter are host programmable in RAM. The output of the tone detector filter goes to an energy detector.

GENERAL SPECIFICATIONS

The modem power and environmental requirements are shown in Tables 4 and 5, respectively.

HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 1) shows the typical modem connection in a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or –12 VDC for RS-232-C) is called active low and is represented by a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol.

Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal $\overline{\text{IRQ}}$). Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$).

Table 4. Power Requirements

Voltage	Current (Typ.) @ 25° C	Current (Max.) @ 0° C
+5 VDC ±5%	85 mA	< 125 mA
– 5 VDC ±5%	15 mA	≤ 30 mA

Note: All voltages must have ripple less then 0.1 volts peak-to-peak. If a switching supply is chosen, the user may select any frequency between 20 KHz and 150 KHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 µV peak.

Table 5. Environmental Requirements

Parameter	Specification
Temperature	
Operating	0° C to +70° C (32° F to 158° F)
Storage	–40° C to +80° C (–40° F to 176° F) (Stored in a suitable anti-static container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35° C, whichever is less.

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals shown in Figure 1 are organized into eight functional groups: power, microprocessor interface, V.24 interface, cable equalizer, analog signals, overhead, reserved, and serial diagnostic interface. These signals, along with their connector pin numbers and interface circuit types, are listed in Table 6. The digital interface characteristics are defined in Table 7.

POWER-ON-RESET

When power is applied to the modem, the modem pulses Power-On-Reset (POR) low to begin the POR sequence. 350 ms after the low-to-high transition of $\overline{POR}$, the modem is ready to use. The POR sequence is reinitiated any time the + 5V supply drops below + 3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 µs. $\overline{POR}$ is not pulsed low by the modem when the POR sequence is initiated externally. The POR sequence initializes the modem interface memory (Table 10) to default values. This action leaves the modem configured as follows:

- V.29 9600 bps
- Serial channel data
- T Equalizer
- Standard echo suppressor tone
- –43 dBm receiver turn-on threshold

3

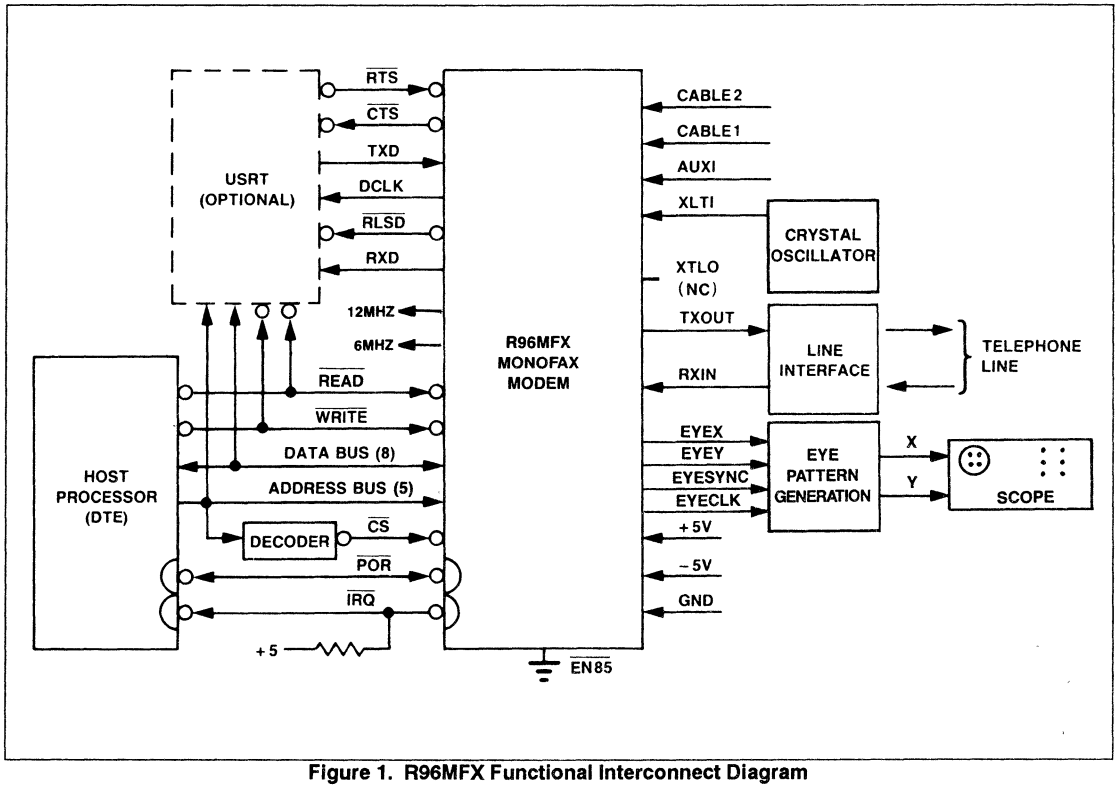


Figure 1. R96MFX Functional Interconnect Diagram

Microprocessor Interface

Seventeen address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 8080 or 68000.

The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The significance of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

Table 6. R96MFX Hardware Interface Signals

Name	Type*	Pin No.	Description
Power			
AGND1	GND	22	Connect to Analog Ground
AGND2	GND	24	Connect to Analog Ground
DGND1	GND	13	Connect to Digital Ground
DGND2	GND	49	Connect to Digital Ground
+5VA	PWR	31	Connect to Analog +5V Power
+5VD	PWR	10	Connect to Digital +5V Power
–5VA	PWR	25	Connect to Analog –5V Power
Microprocessor Interface			
D7	IA/OB	50	Data Bus Line 7
D6	IA/OB	51	Data Bus Line 6
D5	IA/OB	52	Data Bus Line 5
D4	IA/OB	53	Data Bus Line 4
D3	IA/OB	54	Data Bus Line 3
D2	IA/OB	55	Data Bus Line 2
D1	IA/OB	56	Data Bus Line 1
D0	IA/OB	57	Data Bus Line 0
RS4	IA	62	Register Select 4
RS3	IA	63	Register Select 3
RS2	IA	64	Register Select 2
RS1	IA	1	Register Select 1
RS0	IA	2	Register Select 0
$\overline{CS}$	IA	60	Chip Select
$\overline{READ}$-ϕ2	IA	61	Read Strobe (808X), ϕ2 Clock (65XX)
$\overline{WRITE}$-R/$\overline{W}$	IA	59	Write Strobe (808X), R/$\overline{W}$ (65XX)
$\overline{IRQ}$	OC	58	Interrupt Request
V.24 Interface			
$\overline{RTS}$	IA	48	Request to Send
$\overline{CTS}$	OA	14	Clear to Send
TXD	IA	15	Transmit Data
RXD	OA	45	Received Data
$\overline{RLSD}$	OA	46	Received Line Signal Detected
DCLK	OA	16	Transmit and Receive Data Clock
Cable Equalizer			
CABLE1	IB	32	Cable Select 1
CABLE2	IB	33	Cable Select 2
Analog Signals			
TXOUT	AA	28	Connect to Smoothing Filter Input
RXIN	AB	37	Connect to Anti-aliasing Filter Output
AUXI	AC	26	Auxiliary Analog Input

Chip Select ($\overline{CS}$) and Register Selects (RS0-RS4).

The Chip Select ($\overline{CS}$) input enables the modem digital signal processor (DSP) device. The five active high register select lines (RS0-RS4) address interface memory registers within the selected DSP interface memory. All six of these lines are typically connected to the host bus address lines; the register select lines to the five least significant lines (A0-A4), and the chip select line to the next significant line (A5) through a decoder. The DSP decodes RS0 through RS4 to address one of 32 internal interface memory registers (00-1F). The most significant address bit is RS4 and the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0-D7). The most significant data bit is D7 and the least significant data bit is D0.

Table 6. R96MFX Hardware Interface Signals (Cont'd)

Name	Type*	Pin No.	Description
Overhead			
$\overline{PORO}$	OE	43	Power-On-Reset Output
$\overline{PORI}$	IA	5	Power-On-Reset Input
DCLKI	R	11	Connect to DCLK
ECLKIN1	R	30	Connect to EYECLK
ECLKIN2	R	38	Connect to EYECLK
SYNCIN1	R	41	Connect to EYESYNC
SYNCIN2	R	12	Connect to EYESYNC
XTLI	IC	6	Connect to Crystal Circuit or Oscillator
XTLO	R	7	Connect to Crystal Circuit or Float
12 MHZ	OD	8	12 MHz Output
6 MHZ	OD	9	6 MHz Output
RCVI	R	34	Connect to RCVO
RCVO	R	47	Mode Select Output
ADIN	R	20	Connect to ADOUT
ADOUT	R	39	ADC Output
DAIN	R	40	Connect to DAOUT
DAOUT	R	21	DAC/AGC Output
$\overline{EN85}$	R	4	Connect to Resistor for Bus Selection
AEE	R	29	Connect to Analog Ground
AGCIN	R	23	AGC Input
AOUT	R	36	Smoothing Filter Output
FIN	R	35	Connect to FOUT
FOUT	R	27	Smoothing Filter Output
RCI	R	42	RC Junction for POR Time Constant
Reserved			
	R	3	Do Not Connect
Serial Diagnostic Interface			
EYEX	OA	19	Serial Eye Pattern X Output
EYEY	OA	44	Serial Eye Pattern Y Output
EYECLK	OA	18	Serial Eye Pattern Clock (230.4 kHz)
EYESYNC	OA	17	Serial Eye Pattern Strobe (9600 Hz)

Notes:

* Digital signals are described in Table 7. Analog signals are described in Table 9.

R = Required overhead connector; no connection to host equipment.

Read Enable-φ2 (READ-φ2) and Write Enable-R/W (WRITE/R/W)

During a read cycle, data from the selected DSP interface memory register is gated onto the data bus by means of three-state drivers in each DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

The read/write cycle timing waveforms are illustrated in Figure 2 and the timing requirements are shown in Table 8.

Interrupt Request ($\overline{IRQ}$)

The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem DSP device. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.

The DSP $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The modem $\overline{IRQ}$ output can be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25 W, is sufficient.

V.24 INTERFACE

Seven pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels. The transmit and receive timing is shown in Figures 3 and 4, respectively.

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.

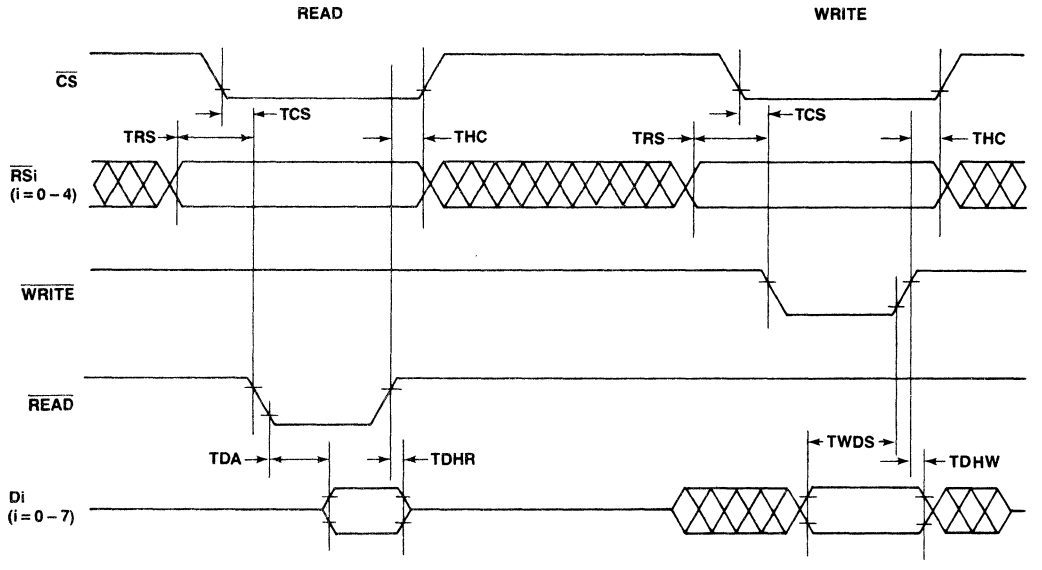
Table 8. Microprocessor Interface Timing

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$ Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	–	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns

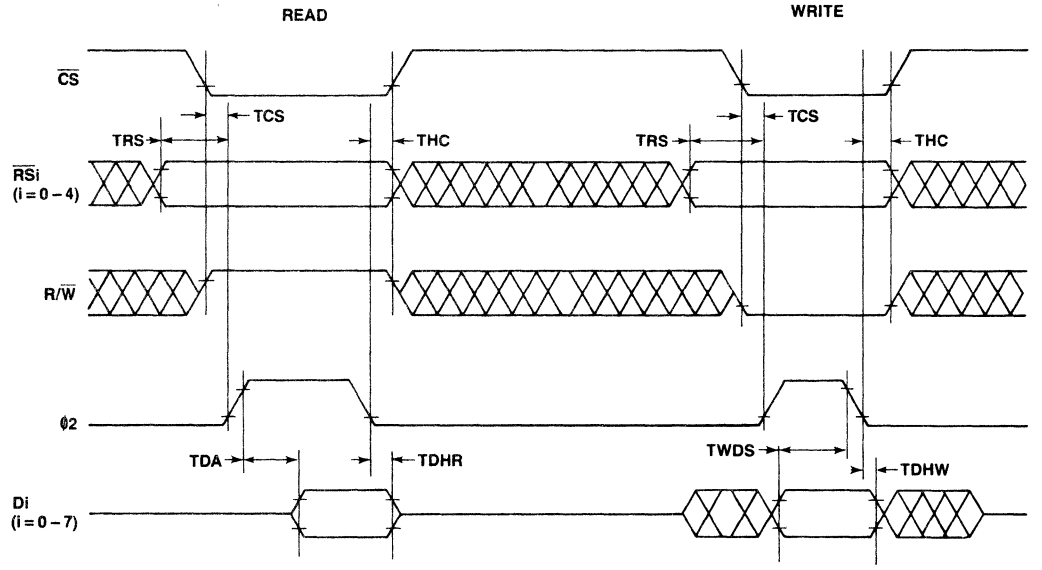
Table 7. Digital Interface Characteristics

			Input/Output Type							
Symbol	Parameter	Units	IA	IB	IC	OA	OB	OC	OD[4]	OE
V_{IH}	Input High Voltage	V	2.0 min.	2.0 min.	(See Note 3					
V_{IL}	Input Low Voltage	V	0.8 max.	0.8 max.	in Fig. 9)					
I_{IH}	Input High Current	µA		40 max.						
I_{IL}	Input Low Current	mA		–0.4 max.						
I_{LI}	Input Leakage Current	µA	±2.5 max.		11 max.					
V_{OH}	Output High Voltage	V				3.5 min.[1]	3.5 min.[1]			2.4 min.[1]
V_{OL}	Output Low Voltage	V				0.4 max.[2]	0.4 max.[3]	0.4 max.[2]		0.4 max.[2]
I_{OH}	Output High Current	mA				– 0.1 max.	– 0.1 max.		– 0.001 max.	40 min.
I_{OL}	Output Low Current	mA				1.6 max.	0.8 max.	1.6 max.	0.001 max.	0.4 max.
I_{LO}	Output Leakage Current	µA				±10 max.	± 10 max.			
C_L	Capacitive Load	pF	5	20	10					
C_D	Capacitive Drive	pF				100	100	100	50	
	Circuit Type		TTL	TTL w/pull-up	CLK	TTL 3-state	TTL 3-state	Open drain	CLK	TTL

Notes:
1. I Load = – 100 mA
2. I Load = 1.6 mA
3. I Load = 0.8 mA
4. Loads on 12 MHz and 6 MHz outputs must be balanced within 20%.



a. 8085 Bus Compatible ($\overline{EN85}$ = L)



b. 6500 Bus Compatible ($\overline{EN85}$ = H)

Figure 2. Microprocessor Interface Waveforms

Received Data (RXD)

The modem presents received serial data to the local DTE on the Received Data (RXD) output.

Request To Send ($\overline{RTS}$)

Request to Send ($\overline{RTS}$) active allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The responses to $\overline{RTS}$ are shown in Table 3.

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) active indicates to the local DTE that the modem will transmit any data present on TXD. $\overline{CTS}$ response times from an active condition of $\overline{RTS}$ are shown in Table 4.

Received Line Signal Detector ($\overline{RLSD}$)

For V.29 and V.27, Received Line Signal Detector ($\overline{RLSD}$) goes active at the end of the training sequence. If energy is above the turn on threshold and training is not detected, the $\overline{RLSD}$ off-to-on response time is 804 baud times. The $\overline{RLSD}$ on-to-off time for V.29 is 30 ± 9 ms. The V.27 $\overline{RLSD}$ on-to-off time is 11.6 ± 5 ms. The $\overline{RLSD}$ on-to-off time ensures that all valid data bits have appeared on RXD.

The $\overline{RLSD}$ receive level thresholds default to –43 dBm for the off-to-on threshold and to –48 dBm for the on-to-off threshold. A minimum hysteresis action of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm. The $\overline{RLSD}$ on and off thresholds are host programmable in DSP RAM.

Data Clock (DCLK)

The modem provides a single Data Clock (DCLK) output which performs the function of a transmitter data clock when the modem is transmitting and a receiver data clock when the modem is receiving.

DCLK as the Transmit Data Clock:

The modem outputs a synchronous transmit Data Clock, for USRT timing, when the modem is transmitting. The DCLK frequency is 9600, 7200, 4800, 2400, or 300 Hz (±0.01%) with a duty cycle of 50 ± 1%. In Group 2, the DCLK frequency is 10368 Hz ± 5 ppm when a precision oscillator (Y2 in Table 12) is used.

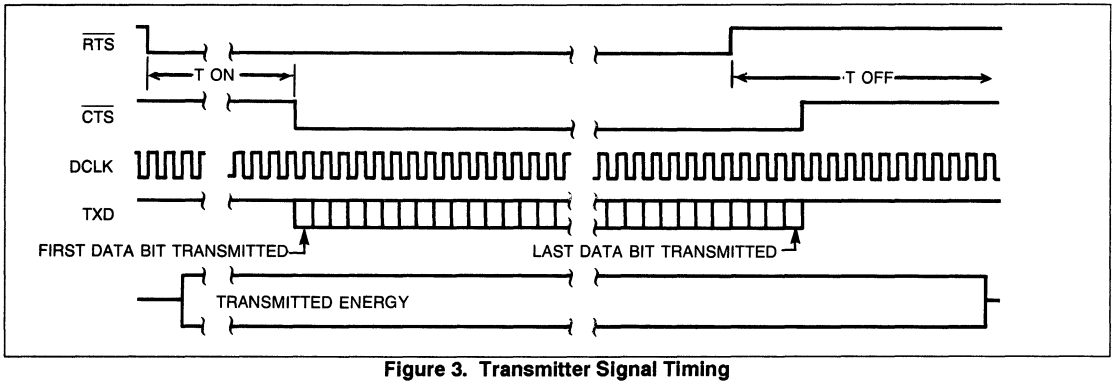


Figure 3. Transmitter Signal Timing

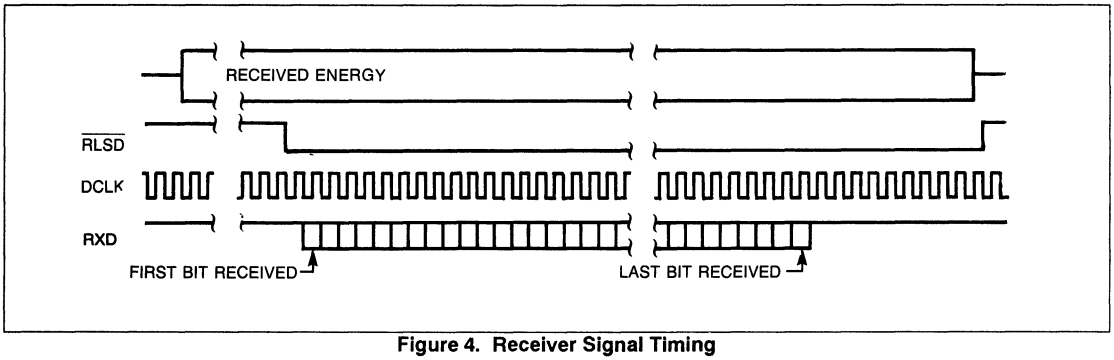


Figure 4. Receiver Signal Timing

Transmit Data (TXD) must be stable during the one μs period immediately preceding the rising edge of DCLK and following the rising edge of DCLK.

DCLK as the Receive Data Clock:

The modem outputs a synchronous receive data clock, for USRT timing, when the modem is receiving. The DCLK frequency is 9600, 7200, 4800, 2400, or 300 Hz (± 0.01%) with a duty cycle of 50 ±1%. In Group 2, the DCLK frequency is 10368 Hz ± 5 ppm when a precision oscillator (Y2 in Table 12) is used.

ANCILLARY SIGNALS

Enable 85 ($\overline{EN85}$)

The Enable 85 ($\overline{EN85}$) input selects the modem microprocessor bus compatibility. When $\overline{EN85}$ is low, the modem can interface directly to an 8085 compatible microprocessor bus using $\overline{READ}$ and $\overline{WRITE}$. When $\overline{EN85}$ is high, the modem can interface directly to a 6500 compatible microprocessor bus using φ2 and R/$\overline{W}$. In the 6500 configuration, the $\overline{READ}$ input becomes φ2 and the $\overline{WRITE}$ input becomes R/$\overline{W}$. This selection is performed when power is turned on or when $\overline{POR}$ is activated.

Cable Equalizer Select 1 and 2 (CABLE1 and CABLE2)

Modems may be connected by direct wiring, such as leased telephone cable or through the PSTN, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable, the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at the lower frequencies than at the higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. When selected, the equalizers are inserted in the transmit path when transmitting, and in the receive path when receiving. Table 2 shows the cable equalization.

The cable length equalization is selected from the CABLE1 and CABLE2 input lines as follows:

CABLE2	CABLE1	Length
0	0	0.0 km
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

ANALOG SIGNALS

The Transmitter Analog Output (TXOUT) and Receiver Analog Input (RXIN) allow modem connection to either a leased line or the PSTN through the appropriate buffering and an audio transformer or a data access arrangement. The Auxiliary Input (AUXI) provides access to the transmitter for summing audio signals with the modem's transmitter analog output. The analog signal characteristics are described in Table 9.

Table 9. Analog Interface Characteristics

Name	Type	Characteristic
TXOUT	AA	Maximum output: ±3.03 volts Minimum load: 10K Ω Smoothing filter transfer function: 28735.63/(s + 11547.34)
RXIN	AB	Input impedance: 1M Ω Anti-aliasing filter transfer function: 21551.72/(s + 11547.34)
AUXI	AC	Maximum input frequency: 4800 Hz Input Impedance: 1M Ω Gain to TXOUT: +5.6 dBm ±1 dBm

Transmitter Analog Output (TXOUT)

TXOUT can supply a maximum of ± 3.03 volts into a load resistance of 10K ohms minimum. A 600 ohm line impedance can be matched using an external smoothing filter with a 604 ohm series resistor in its output. The smoothing filter should have a transfer function of 28735.63/(s + 11547.34).

Receiver Analog Input (RXIN)

The RXIN input impedance is greater than 1M ohms. RXIN requires an external anti-aliasing filter between the modem and the line interface, with a transfer function of 21551.72/(s + 11547.34). The maximum input level into the anti-aliasing filter should not be greater than 0 dBm.

The filters required for anti-aliasing on the receiver input and the smoothing filter on the transmitter output have a single pole within the modem's passband (11,542 radians). Internal filters compensate for its presence, therefore, the pole location must not be changed. Some variation from the recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10K ohms (see Recommended Modem Interface Circuit.)

Auxiliary Analog Input (AUXI)

AUXI allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled input, any signal above 4800 Hz will cause aliasing errors. The input impedance is >1M ohm, and the gain to TXOUT is +5.6 dBm ± 1 dBm.

DIAGNOSTIC SIGNALS

Four signals provide the timing necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. Timing of these signals is illustrated in Figure 5 and an example eye pattern generation schematic is shown in Figure 6.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

EYEX and EYEY outputs are 15-bit words, each with 8-bits of significance. The 15-bit data words are shifted out most significant bit first with the seven most significant bits set equal to zero. EYEX and EYEY are clocked by the rising edge of EYECLK.

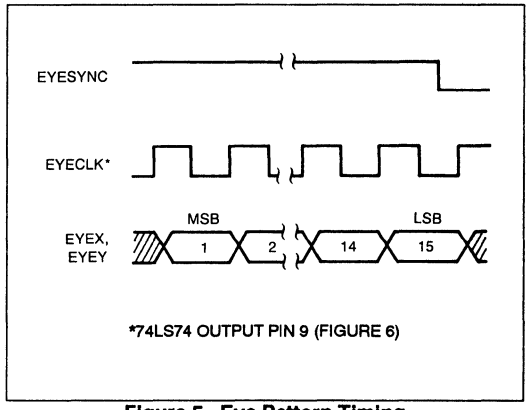


Figure 5. Eye Pattern Timing

EYECLK

EYECLK is a clock provided to create a clock which can be used by the serial-to-parallel converters to shift in the EYEX and EYEY data (see Figure 5).

EYESYNC

EYESYNC is a strobe for loading the D/A converters.

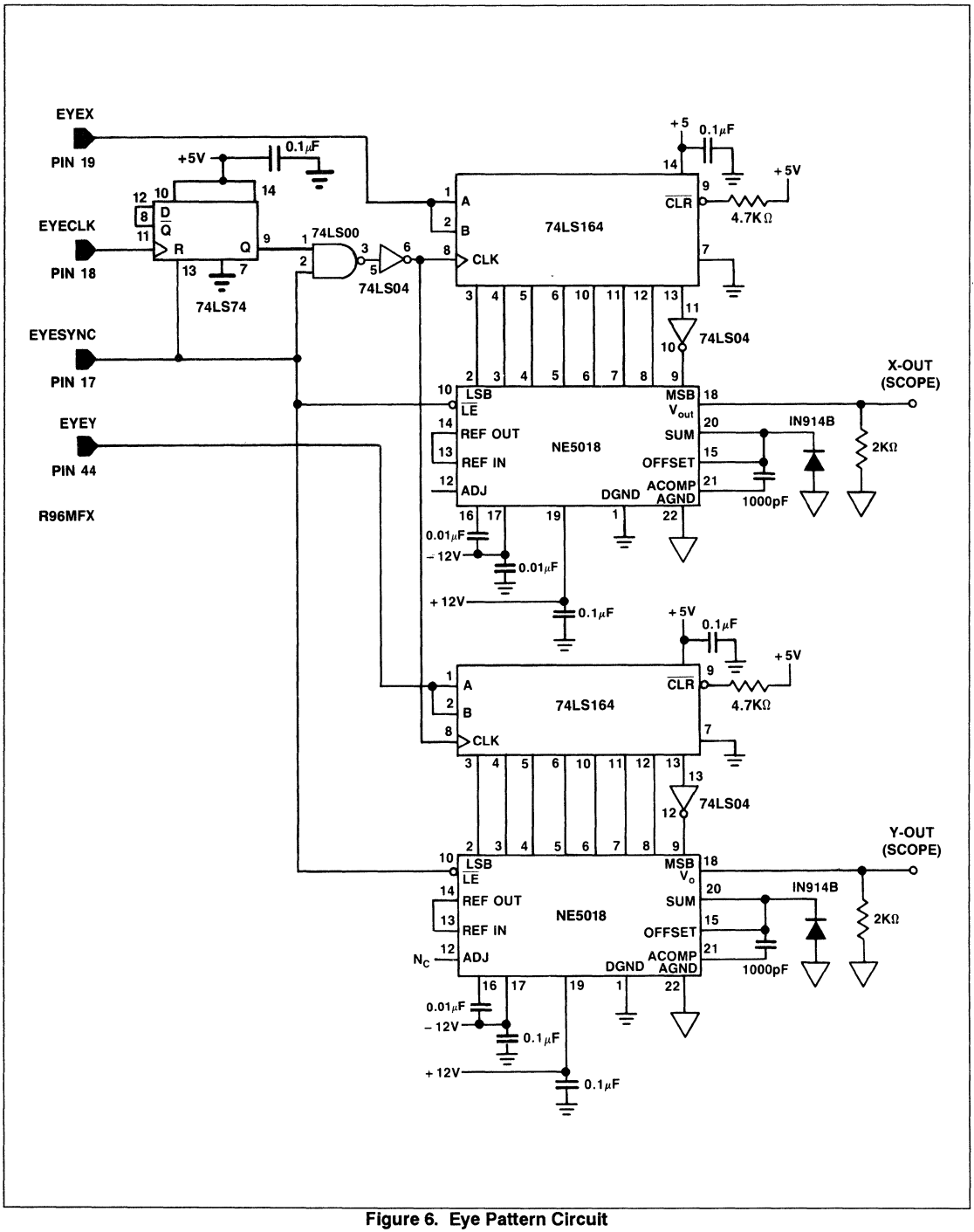


Figure 6. Eye Pattern Circuit

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in a single DSP.

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAPS

A memory map of the 32 addressable registers in the modem is shown in Figure 7. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register and then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, the entire register (8-bits) must first be read, the necessary bits must be set or reset without altering the other register bits, then the byte (8-bits) containing both the unaltered and modified bits must be written back into the interface memory.

INTERFACE MEMORY BIT DEFINITIONS

Table 10 defines the individual bits in the interface memory. In the Table 10 descriptions, bits in the interface memory are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

Register	Bit 7	6	5	4	3	2	1	0
1F	—	—	—	—	—	—	—	SETUP
1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1
1D	—	—	—	—	—	—	—	—
1C	—	—	—	—	—	—	—	—
1B	—	—	—	—	—	—	—	—
1A	—	—	—	—	—	—	—	—
19	—	—	—	—	—	—	—	—
18	—	—	—	—	—	—	—	—
17	—	—	—	—	—	—	—	—
16	—	—	—	—	—	—	—	—
15	ACC2	0	0	0	0	BR2	WRT2	CR2
14	RAM ADDRESS 2 (ADD2)							
13	X RAM DATA 2 MSB (XDAM2)							
12	X RAM DATA 2 LSB (XDAL2)							
11	Y RAM DATA 2 MSB (YDAM2)							
10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)							
0F	FED		—	—	—	—	CTSP	CDET
0E	—	—	—	—	—	—	—	—
0D	RX	PN	—	—	G2FGC	—	—	—
0C	—	—	—	—	—	—	—	—
0B								
0A								
09	—	—	EQFZ	—	—	—	—	—
08	FR3	FR2	FR1	12TH	—	—	—	—
07	RTSP	TDIS	PDM	—	EPT	SQEXT	T2	—
06	CONF							
05	ACC1	0	0	0	0	BR1	WRT1	CR1
04	RAM ADDRESS 1 (ADD1)							
03	X RAM DATA 1 MSB (XDAM1)							
02	X RAM DATA 1 LSB (XDAI1)							
01	Y RAM DATA 1 MSB (YDAM1)							
00	Y RAM DATA 1 LSB (YDAL1)							

(—) Indicates reserved for modem use only.

Figure 7. R96MFX DSP Interface Memory Map

Table 10. R96MFX Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
12TH	8:4	0	**Select 12th Order.** The one state of 12TH operates the tone detectors as one 12th order filter (uses FR3). The zero state of 12TH operates the tone detectors as three parallel independent 4th order filters (FR1, FR2, FR3). 12TH is operable in FSK, Group 2, and tone modes. (i.e., CONF = 20, 40, 80; with $\overline{RTS}$ off.)
ACC1	5:7	1	**RAM Access 1.** When control bit ACC1 is a 1, the modem accesses the RAM associated with the address in ADD1 and the CR1 bit. WRT1 determines if a read or write is performed.
ACC2	15:7	1	**RAM Access 2.** When control bit ACC2 is a 1, the modem accesses the RAM associated with the address in ADD2 and the CR2 bit. WRT2 determines if a read or write is performed.
ADD1	4:0-7	17	**RAM Address 1.** ADD1 contains the RAM address used to access the modem's X and Y Data RAM (CR1 = 0) or X and Y Coefficient RAM (CR1 = 1) via the X RAM Data 1 LSB and MSB words (2:0-7 and 3:0-7, respectively) and the Y RAM Data 1 LSB and MSB words (0:0-7 and 1:0-7, respectively).
ADD2	14:0-7	11	**RAM Address 2.** ADD2 contains the RAM address used to access the modem's X and Y Data RAM (CR2 = 0) or X and Y Coefficient RAM (CR2 = 1) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7, respectively) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
BA1	1E:0	–	**Buffer Available 1.** When set to a 1, status bit BA1 signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) register (0:0-7). This condition can also cause $\overline{IRQ}$ to be asserted (see IE1 and IA1). The host writing to or reading from register 00 resets the BA1 and IA1 bits to 0. (See IE1 and IA1.)
BA2	1E:3	–	**Buffer Available 2.** When set to a 1, status bit BA2 signifies that, when the modem is in parallel data mode, it has read register 10:0-7 (DBUFF) when transmitting (buffer becomes empty), or it has written register 10:0-7 (DBUFF) when receiving (buffer becomes full). When the modem is not in parallel data mode, the setting of BA2 to a 1 by the modem signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) register (10:0-7). These conditions can also cause $\overline{IRQ}$ to be asserted (see IE2 and IA2). The host writing to or reading from register 10 resets the BA2 and IA2 bits to 0. (See IE2 and IA2.)
BR1	5:2	0	**Baud Rate 1.** When control bit BR1 is a 1, RAM access associated with ADD1 occurs at the modem baud rate; when BR1 is a 0, RAM access occurs at the modem sample rate. This bit must be reset to a zero in G2, FSK, or Tone mode (CONF = 40, 20, or 80, respectively).
BR2	15:2	0	**Baud Rate 2.** When control bit BR2 is a 1, RAM access associated with ADD2 occurs at the modem baud rate; when BR2 is a 0, RAM access occurs at the modem sample rate. This bit must be reset to a zero in G2, FSK, or Tone mode (CONF = 40, 20, or 80, respectively).
CDET	F:0	–	**Carrier Detected.** When status bit CDET is a 1, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is a 0, the receiver is in the idle state or in the process of training.

Table 10. R96MFX Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CONF	6:0-7	14	**Configuration.** The CONF control bits select one of the following transmitter/receiver configurations: **CONF** **Configuration** 14 V.29 9600 bps 12 V.29 7200 bps 11 V.29 4800 bps 0A V.27 4800 bps 09 V.27 2400 bps 20 V.21 Channel 2 300 bps (FSK) 40 Group 2 (G2) 80 Tone Transmit ($\overline{\text{RTS}}$ or RTSP on), Tone Detect ($\overline{\text{RTS}}$ and RTSP off) **Configuration Definitions:** 1. **V.29.** When a V.29 configuration is selected, the modem operates as specified in CCITT Recommendation V.29. 2. **V.27.** When a V.27 configuration is selected, the modem operates as specified in CCITT Recommendation V.27. 3. **V.21.** Channel 2 When the V.21 Channel 2 configuration is selected, the modem operates as specified in CCITT Recommendation V.21 channel 2. 4. **Group 2.** When the Group 2 configuration is selected, the modem operates as specified in CCITT Recommendation T.3. 5. **Tone Transmit.** When the Tone Transmit configuration is selected, the modem transmits single or dual frequency tones in response to $\overline{\text{RTS}}$ or RTSP. Tone frequencies and amplitudes are programmable in the RAM. 6. **Tone Detect.** When the Tone Detect configuration is selected and 12th is set to a 1, the three 4th order tone detect filters are combined into a single 12th order tone detect filter (FR3). If 12th is not set to a 1, the three tone detect filters are placed in parallel and are independent (FR1, FR2, and FR3). All tone detect filters are programmable.
CR1	5:0	0	**Coefficient RAM 1 Select.** When control bit CR1 is a 1, ADD1 addresses Coefficient RAM. When CR1 is a 0, ADD1 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CR2	15:0	0	**Coefficient RAM 2 Select.** When control bit CR2 is a 1, ADD2 addresses Coefficient RAM. When CR2 is a 0, ADD2 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CTSP	F:1	–	**Clear To Send Parallel.** When set to a 1, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at TXD will be transmitted. CTSP parallels the operation of the CTS pin.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode, the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first.
EPT	7:3	0	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 which transmits 20 ms of silence at the beginning of training.
EQFZ	9:5	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.

Table 10. R96MFX Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
FED	F:7,6	–	**Fast Energy Detector.** Status bits FED indicates the level of the received signal according to the following codes. **FED** **Energy Level** 0 No energy 1 Invalid 2 Above Turn-off Threshold 3 Above Turn-on Threshold
FR1	8:5	0	**Frequency No. 1.** The one state of FR1 indicates that energy is above tone detector 1's detected turn on threshold (default detection range = 2100 Hz ± 25 Hz in non-Group 2 mode). FR1 is operable in FSK, Group 2, and tone modes. (i.e., CONF = 20, 40, 80; with RTSP and $\overline{RTS}$ off.)
FR2	8:6	0	**Frequency No. 2.** The one state of FR2 indicates that energy is above tone detector 2's detected turn on threshold (default detection range = 1100 Hz ± 30 Hz in non-Group 2 mode). FR2 is operable in FSK, Group 2, and tone modes. (i.e., CONF = 20, 40, 80; with RTSP and $\overline{RTS}$ off.)
FR3	8:7	0	**Frequency No.3.** The one state of FR3 indicates that energy is above tone detector 3's detected turn on threshold (default detection range = 462 Hz ±14 Hz in non-Group 2 mode). FR3 is operable in FSK, high speed, Group 2, and tone modes. (i.e., CONF = 14, 12, 11, 0A, 09, 20, 40, 80; with RTSP and $\overline{RTS}$ off.)
G2FGC	D:3	0	**Group 2 Fast Gain Control.** The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group 2 Facsimile.
IA1	1E:6	–	**Interrupt Active 1.** When Interrupt Enable 1 is enabled (IE1 is a 1) and BA1 is set to a 1 by the modem, the modem asserts $\overline{IRQ}$ and sets status bit IA1 to a 1 to indicate that BA1 going to a 1 caused the interrupt. The host writing to or reading from register 0:0 resets IA1 to a 0. (See IE1 and BA1.)
IA2	1E:7	–	**Interrupt Active 2.** When Interrupt Enable 2 is enabled (IE2 is a 1) and BA2 is set to a 1 by the modem, the modem asserts $\overline{IRQ}$ and sets status bit IA2 to a 1 to indicate that BA2 going to a 1 caused the interrupt. The host writing to or reading from register 10:0 resets IA2 to a 0. (See IE2 and BA2.)
IE1	1E:2	0	**Interrupt Enable 1.** When control bit IE1 is a 1 (interrupt enabled), the modem will assert $\overline{IRQ}$ and set IA1 to a 1 when $\overline{BA1}$ is set to 1 by the DSP. When IE1 is a 0 (interrupt disabled), BA1 has no effect on $\overline{IRQ}$ and IA1. (See BA1 and IA1.)
IE2	1E:5	0	**Interrupt Enable 2.** When control bit IE2 is a 1 (interrupt enabled), the modem will assert $\overline{IRQ}$ and set IA2 to a 1 when $\overline{BA2}$ is set to 1 by the DSP. When IE2 is a 0 (interrupt disabled), BA2 has no effect on $\overline{IRQ}$ and IA2. (See BA2 and IA2.)
PDM	7:5	0	**Parallel Data Mode.** When control bit PDM is a 1 and the modem is a transmitter, it accepts data for transmission from DBUFF (10:0-7) rather than the TXD input. When PDM is a 1 and the modem is a receiver, the modem provides the received data to the host using DBUFF (10:0-7).
PN	D:6	–	**PN Sequence Detected.** When status bit PN is a 1, the receiver is detecting the PN portion of the training sequence. When PN is a 0, PN is not being detected.
RTSP	7:7	0	**Request To Send Parallel.** The one state of RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is turned off, and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTSP}$ control input. These inputs are "ORed" by the modem.

Table 10. R96MFX Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RX	D:7	–	**Receive State.** When status bit RX is a 1, the modem is in the receive state and is not transmitting.
SETUP	1F:0	0	**Setup.** Control bit SETUP bit must be set to a 1 by the host after the host writes a configuration code into the CONF bits (register 6:0-7) or changes a bit in 7:0-6 (register 7 bits 0 through 6). This informs the modem to implement the configuration change. The modem resets the SETUP bit to a 0 when the configuration change is implemented.
SQEXT	7:2	0	**Squelch Extend.** When control bit SQEXT is a 1, the modem's receiver is inhibited from the reception of any signal for 140 ms after the transmitter turn-off.
T2	7:1	0	**T/2 Equalizer Select.** When control bit T2 is a 1, the linear section of the receiver's adaptive equalizer is T/2 fractionally spaced. When T2 is a 0, the equalizer is T spaced (T = 1 baud time).
TDIS	7:6	0	**Training Disable.** When control bit TDIS is a 1, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when RTS or RTSP is activated.
WRT1	5:1	0	**RAM Write 1.** When control bit WRT1 is a 1 and ACC1 is set to a 1, the modem writes the data from the Y RAM Data 1 registers into its internal RAM at the location addressed by ADD1 and CR1. (When the most significant bit of ADD1 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT1 is a 0 and ACC1 is set to a 1, the modem reads data from its internal RAM from the locations addressed by ADD1 and CR1 and stores it into the X RAM Data 1 registers and Y RAM Data 1 registers, respectively.
WRT2	15:1	0	**RAM Write 2.** When control bit WRT2 is a 1 and ACC2 is set to a 1, the modem writes the data from the Y RAM Data 2 registers into its internal RAM at the location addressed by ADD2 and CR2. (When the most significant bit of ADD2 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT2 is a 0 and ACC2 is set to a 1, the modem reads data from its internal RAM from the locations addressed by ADD2 and CR2 and stores it into the X RAM Data 2 registers and Y RAM Data 2 registers, respectively.
XDAL1	2:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the least significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the least significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	3:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	0:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the least significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the least significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
YDAM1	1:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the most significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the most significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.

DSP RAM ACCESS

Table 11 provides the RAM access functions, codes, and registers.

DSP RAM Organization

The DSP contains 16-bit words of random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM.

Interface Memory Access to DSP RAM

The interface memory acts as an intermediary during host to DSP RAM, or DSP RAM to host, data exchanges. The address stored in DSP interface memory RAM Address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud or sample time, as selected by the BR1 and BR2 bits. The baud rate is determined by the selected configuration, but the sample rate is fixed at 9600 Hz, except in Group 2 where the sample rate is 10368 Hz.

Two RAM Access bits in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The transfer is initiated by the host setting the ACC1 and/or the ACC2 bit(s). The DSP tests these bits each baud or sample period, except in G2, FSK and Tone mode where these bits are always tested at the sample period, except in G2, FSK or Tone mode where these bits are always tested at the sample period.

If parallel data mode is selected, RAM access associated with RAM Address 2 is disabled and only RAM access associated with RAM Address 1 is available.

Table 11. R96MFX RAM Access Codes

Function	BRx	CRx	ADDx	Read Reg. No.
Received Signal Samples	0	0	15	2,3
Received Signal Samples FSK	0	0	31	2,3
Demodulator Output	0	0	13	0,1,2,3
Lowpass Filter Output	0	0	02	0,1,2,3
Average Energy	0	0	14	2,3
AGC Gain Word	0	1	15	2,3
Tone 1 Frequency	0	1	21	2,3
Tone 1 Level	0	0	22	2,3
Tone 2 Frequency	0	1	22	2,3
Tone 2 Level	0	0	23	2,3
Output Level	0	0	21	2,3
Equalizer Input (Real)	1	0	1E	0,1
Equalizer Input (Imag)	1	1	1E	0,1
Equalizer Tap Coefficients	1	1	38 - 5F	0,1,2,3
Unrotated Equalizer Output	1	0	1C	0,1,2,3
Rotated Equalizer Output (Eye Pattern)	1	1	17	0,1,2,3
Decision Points (Ideal)	1	0	17	0,1,2,3
Error Vector	1	1	1D	0,1,2,3
Rotation Angle	1	1	0C	0,1
Frequency Correction	1	1	18	2,3
Eye Quality Monitor (EQM)	1	1	0D	2,3
Turn-on Threshold (RLSD)	0	1	37	2,3
Turn-off Threshold (RLSD)	0	1	B7	0,1
Group 2 PLL Frequency Correction	0	0	0D	2,3
Group 2 Zero Crossing Threshold (Negative)	0	0	19	2,3
Group 2 Zero Crossing Threshold (Positive)	0	0	99	0,1
Group 2 AGC Slew Rate	0	1	05	2,3
Group 2 Black-White Threshold	0	0	24	2,3
Group 2 Phase Limit Value	0	0	1A	2,3
Receiver Sensitivity	0	1	24	2,3

DSP RAM Read Procedure

The RAM read procedure is a 32-bit transfer from DSP RAM to the interface memory which transfers both the X RAM and Y RAM simultaneously. Before reading from DSP interface memory, set ACC1 and/or ACC2 to a 0, then reset BA1 or BA2 by reading YDAL1 or YDAL2. Set WRT1 and/or WRT2 to a 0 to inform the DSP that a RAM read will occur when ACC1 and/or ACC2 is set to a 1. Load the RAM address into RAM Address 1 and/or RAM Address 2, then set CR1 and/or CR2 appropriately. Set ACC1 and/or ACC2 to a 1 to signal the DSP to perform the RAM read. When the DSP has transferred the contents of RAM into the interface memory RAM Data registers, BA1 and/or BA2 will be set.

If IE1 and/or the IE2 is a 1, $\overline{IRQ}$ is also asserted when BA1 and/or BA2 set to a 1 by the DSP. When $\overline{IRQ}$ is asserted, IA1 and/or IA2 goes to a 1 to inform the host that setting of BA1 and/or BA2 was the cause. IA1 and/or IA2 is cleared by the host reading YDAL1 and/or YDAL2, which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

DSP RAM Write Procedure

The RAM write procedure is a 16-bit transfer from interface memory to DSP RAM allowing the transfer of X RAM data or Y RAM data to occur each baud or sample time. Before writing to DSP interface memory, set ACC1 and/or ACC2 to a 0; then reset BA1 or BA2 by reading YDAL1 or YDAL2, respectively. Set WRT1 and/or WRT2 to a 1 to inform the DSP that a RAM write will occur when ACC1 and/or ACC2 is set to a 1. Load the RAM address into RAM Address 1 and/or RAM Address 2, then set CR1 and/or CR2 appropriately. Write the desired data into the interface memory RAM Data registers YDAL1 and YDAM1 and/or YDAL2 and YDAM2, then set ACC1 and/or ACC2 to a 1 to signal the DSP to perform the RAM write. When the DSP has transferred the contents of the interface memory RAM Data registers into RAM, BA1 or BA2 will be set.

If IE1 and/or IE2 is a 1, $\overline{IRQ}$ is also asserted and IA1 and/or IA2 is set to a 1 when BA1 and/or BA2 is set to a 1 by the DSP. IA1 and/or IA2 is cleared by writing into YDAL1 and/or YDAL2, which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

PERFORMANCE

TYPICAL BIT ERROR RATES

The bit error rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm as illustrated.

Typical BER performance is shown in Figure 8.

The curves shown in Figure 8 were prepared from data obtained using a TAS 1000 communication test system.

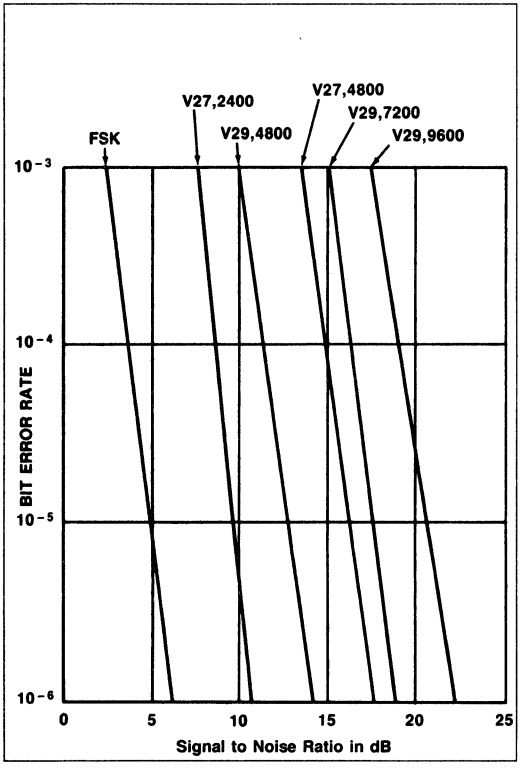
TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-noise phase jitter at 120 Hz.

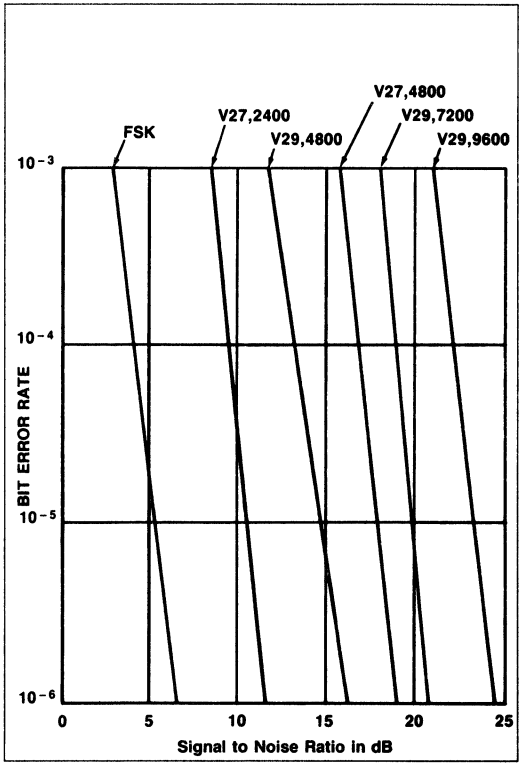
At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12 peak-to-peak phase jitter at 300 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.



Typical Bit Error Rate
(Back-to-Back, T Equalizer, Level −20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer Level −20 dBm)

Figure 8. R96MFX Typical Bit Error Rate (BER) Curves

APPLICATION

RECOMMENDED MODEM INTERFACE CIRCUIT

The R96MFX is supplied as a 64-pin QUIP (Quad In-line Package) device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit (Figure 9) and parts list (Table 12) illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R10 and R16 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3K ohm series resistor should be used on each input (pins 32 and 33) for isolation.

Resistors R7 and R17 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more that 99.8% of the units.

Table 13. TC0-706AB Oscillator Specifications

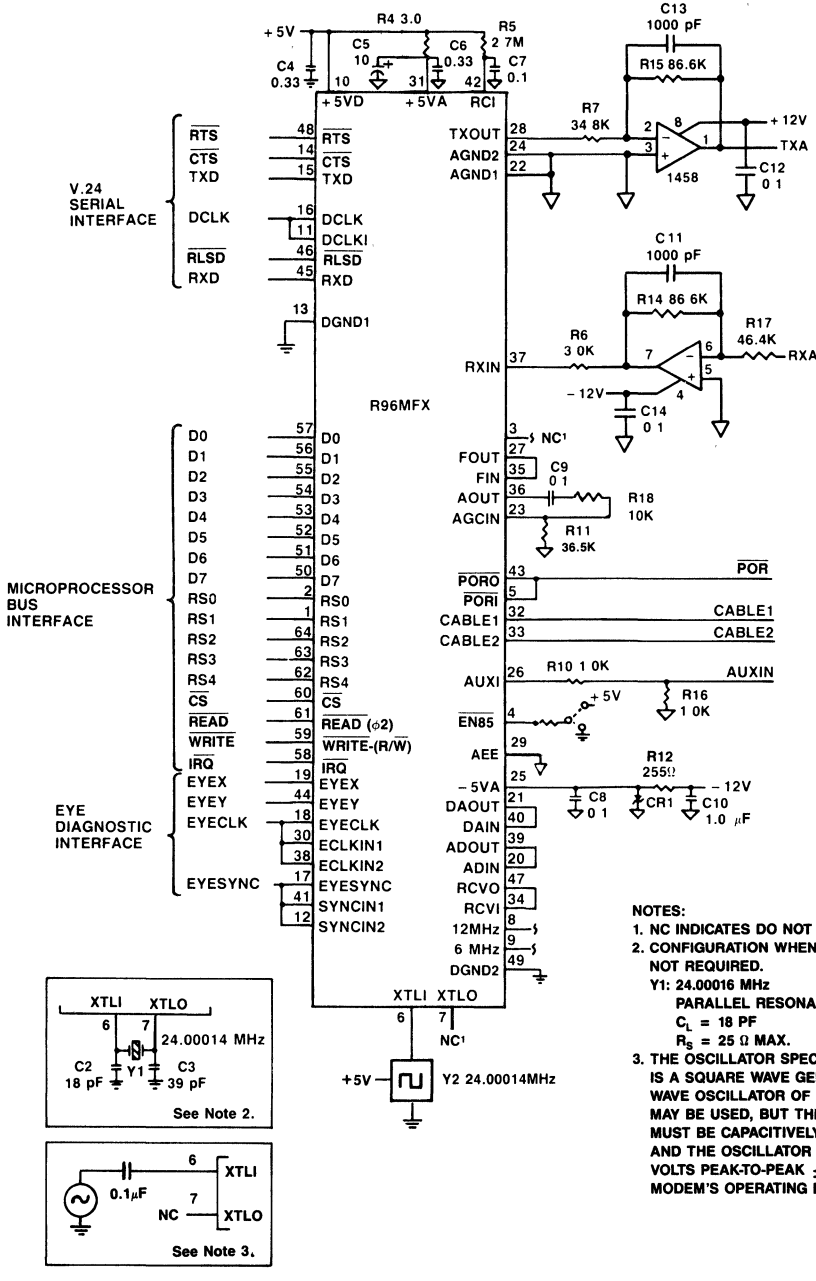
Characteristic	Value
Frequency	24.00014 MHz
Frequency Stability	
vs. Temperature	± 5 ppm (0°C - 60°C)
vs. Input Voltage	± 1 ppm at 4.75 V - 5.25 V
vs. Aging	1 ppm/year
Frequency Tolerance	± 2 ppm
Frequency Adjustment by Internal Trimmer	± 5 ppm min.
Operating Temperature	0°C - 60° C
Input Voltage	5.0 V ± 0.5% (4.75 V - 5.25 V)
Output	
Symmetry	50% ± 10% (40% - 60%)
Drive	CL = 15 pF
Type	CMOS: Low = 0.5 V, High = Vcc (4.5 V)
Package	14-pin DIP

3

Table 12. Typical R96MFX Modem Interface Parts List

Component Designation	Component Value	Manufacturer's Part Number	Suggested Manufacturer
C11, C13	1000 pF ±5%, 50V	C124C102J5G5CA	Kemet
C7, C8, C9, C12, C14	0.1 µF ±20%, 50V	592CX7R104M050B	Sprague
C4, C6	0.33 µF ±20%, 50V		
C10	1.0 µF ±20%, 50V	SMC50T1R0M5X12	United Chem-con
C5	10.0 µF ±10%, 25V	ECEBEF100	Panasonic
C2	18 pF ±5%, 50V		
C3	39 pF ±5%, 50V		
R4	3 Ω ± 5%, 1/4W	43CX3R000J	Mepco Electra
R12	255 Ω ±1%, 1/4W		
R10, R16	1 KΩ±5%, 1/4W	5043CX1K00J	Mepco Electra
R2, R6	3 KΩ ±5%, 1/4W	5043CX3K00J	Mepco Electra
R18	10 KΩ ±1%, 1/4W		
R7	34.8 KΩ±1%, 1/4W		
R17	46.4 KΩ±1%, 1/4W	CRB1/4XF46K4	R–Ohm
R11	36.5 KΩ±1%, 1/4W	CRB1/4XF36K5	R-Ohm
R14, R15	86.6 KΩ±1%, 1/4W	CML 1/10 T86.6 KΩ ±1%	Dale Electronics
R5	2.7 MΩ± 5%, 1/4W	5043CX2M700J	Mepco Eletra
CR1	–5.1V 1%, regulator	1N4625D	Motorola
Y1	24.00014, MHz		
Y2	24.00014, MHz	TC0-706AB[1]	Toyocom

Note: 1. See Table 13 for specifications. The TC0-706AB1 is the only square wave generator recommended. A sine wave oscillator may alternativly be used (See Note 3 in Figure 9).



NOTES:

1. NC INDICATES DO NOT CONNECT.
2. CONFIGURATION WHEN GROUP 2 NOT REQUIRED.
   Y1: 24.00016 MHz
   PARALLEL RESONANT
   C_L = 18 PF
   R_S = 25 Ω MAX.
3. THE OSCILLATOR SPECIFIED IN TABLE 13 IS A SQUARE WAVE GENERATOR. A SINE WAVE OSCILLATOR OF EQUAL ACCURACY MAY BE USED, BUT THE INPUT TO PIN 6 MUST BE CAPACITIVELY COUPLED (e.g., 0.1μF) AND THE OSCILLATOR OUTPUT MUST BE 3.5 VOLTS PEAK-TO-PEAK ± 14% OVER THE MODEM'S OPERATING ENVIRONMENTAL RANGE.

Figure 9. Recommended R96MFX Modem Interface Circuit

PC BOARD LAYOUT CONSIDERATIONS

1. The R96MFX and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board.
2. All power traces should be at least a 0.1 inch width.
3. If the power source is located more than approximately 5 inches from the modem, a decoupling capacitor of 10 µF or greater should be placed in parallel with C4 near pins 10 and 49.
4. All circuitry connected to pins 6 and 7 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the modem package. Pin 24 should tie directly, by a dedicated path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and to all analog ground points shown in Figure 10.
7. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 49 and to all digital ground points shown in Figure 10, plus the crystal-can ground.
8. The modem package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
9. As a general rule, digital signals should be routed on the component side of the PCB while the analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
10. Routing of the modem signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to Table 14 for the noise characteristics of each modem pin.

Table 14. Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	High	Low
1	6	3	23	26
2	7	4	27	28
12	8	5	32	
17	9	10	33	
18	11	13	35	
19	14	22	36	
20	15	24	37	
21	16	25		
30	45	29		
38	46	31		
39	48	34		
40		42		
41		43		
44		47		
50		49		
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54				
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PC BOARD LAYOUT CONSIDERATIONS

1. The R96MFX and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board.
2. All power traces should be at least a 0.1 inch width.
3. If the power source is located more than approximately 5 inches from the modem, a decoupling capacitor of 10 μF or greater should be placed in parallel with C4 near pins 10 and 49.
4. All circuitry connected to pins 6 and 7 should be kept short to prevent stray capacitance from affecting the oscillator.
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18	11	13	35	
19	14	22	36	
20	15	24	37	
21	16	25		
30	45	29		
38	46	31		
39	48	34		
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Rockwell

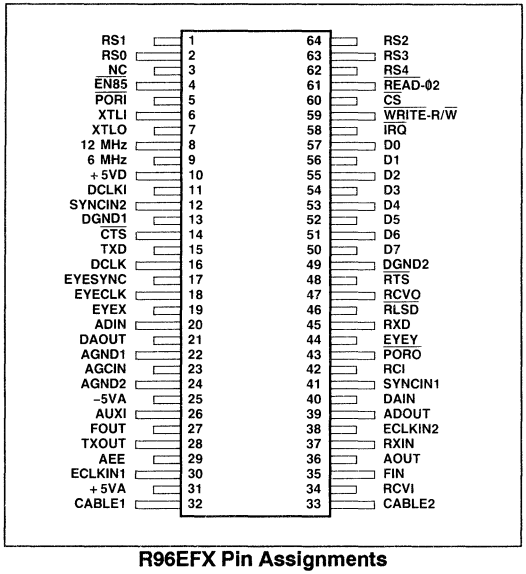
R96EFX 9600 bps MONOFAX® Modem with Error Detection

INTRODUCTION

The Rockwell R96EFX MONOFAX is a synchronous 9600 bits per second (bps) half-duplex modem with error detection in a single 64-pin quad-in-line package (QUIP). The R96EFX can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, V.21 Channel 2, T.3, and T.4, and the binary signaling requirements of T.30. The R96EFX can operate at speeds of 9600, 7200, 4800, 2400, and 300 bps, and also includes the V.27 ter short training sequence option. The R96EFX can also perform HDLC framing according to T.30 at speeds of 9600, 7200, 4800, 2400, and 300 bps.

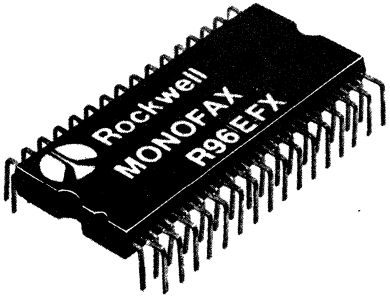
The R96EFX is designed for use in Group 3 and Group 2 facsimile machines. The modem's small size and low power consumption allow the design of compact system enclosures for use in both office and home environments.



R96EFX Pin Assignments

FEATURES

- Single 64-pin QUIP
- CCITT V.29, V.27 ter and V.27 ter short train option, T.30, V.21 Channel 2, T.4, T.3
- Group 3 and Group 2 Facsimile Transmission/ Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Programmable Turn-on and Turn-off Thresholds
- Programmable Transmit Output Level
- HDLC Framing at All Speeds
- Programmable Interface Memory Interrupt
- Diagnostic Capability
  - Allows Telephone Line Quality Monitoring
- Equalization
  - Automatic Adaptive
  - Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - Selectable Microprocessor Bus (6500 or 8085)
  - CCITT V.24 (RS-232-C Compatible) Interface
- TTL and CMOS Compatible
- Low Power Consumption: 500 mW (Typical)



R96EFX 9600 bps MONOFAX Modem with Error Detection

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

TONE GENERATION

Under control of the host processor, the modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

DATA ENCODING

The data encoding conforms to CCITT recommendations V.29, V.27, V.21 Channel 2, and T.3.

CABLE EQUALIZERS

Equalization functions are provided that improve performance when operating over low quality lines.

The integrated analog section of the R96EFX has selectable cable equalizers with the characteristics shown in Table 2. Choose specific cable equalizers by strapping CABLE1 and CABLE2 to either +5V or GND (see Hardware Interface). The chosen filter functions in both transmit and receive paths depending on operating mode.

ADAPTIVE EQUALIZER

An adaptive equalizer in V.29 and V.27 modes compensates for transmission line amplitude and group delay distortion.

TRANSMITTED DATA SPECTRUM

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response (FIR) filter with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter. This filter shapes the spectrum so that with continuous binary ones applied, the resulting transmitted spectrum has a substantially linear phase characteristic over the band of 700 Hz to 2700 Hz, and the energy density at 500 Hz and 2900 Hz is attenuated 4.5 ± 2.5 dBm with respect to the maximum energy density between 500 Hz and 2900 Hz.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter. This filter shapes the spectrum so that with continuous binary ones applied, the resulting transmitted spectrum has a substantially linear phase characteristic, and the energy density at 1000 Hz and 2600 Hz is attenuated 3.0 ± 2.0 dBm with respect to the maximum energy density between 1000 Hz and 2600 Hz.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter. This filter shapes the spectrum so that with continuous binary ones applied, the resulting transmitted spectrum has a substantially linear phase characteristic, and the energy density at 1200 Hz and 2400 Hz is attenuated 3.0 ± 2.0 dBm with respect to the maximum energy density between 1200 Hz and 2400 Hz.

The transmit spectrum characteristics assume that the cable equalizers are disabled.

Table 2. Cable Equalizer Characteristics

Frequency (Hz)	Gain dB Relative to 1700 Hz for Length of 0.4 mm Cable			
	0	1.8 km	3.6 km	7.2 km
700	0.00	–0.99	–2.39	–3.93
1500	0.00	–0.20	–0.65	–1.22
2000	0.00	+0.15	+0.87	+1.90
3000	0.00	+1.43	+3.06	+4.58

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits per Symbol	Constellation Points
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 4800	DPSK	1800	4800	1600	3	8
V.27 2400	DPSK	1800	2400	1200	2	4
V.21 300	FSK	1650,1850	300	300	1	–
T.3 (Group2) Single and Dual Tone Transmit	VSAMPM	2100	–	–	–	–

Notes: 1. Modulation legend:
QAM Quadrature Amplitude Modulation
DPSK Differential Phase Shift Keying
FSK Frequency Shift Keying
VSAMPM Vestigial Sideband Amplitude Modulation - Phase Modulation

The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range are below –55.0 dBm.

TURN-ON SEQUENCE

Transmitter turn-on sequence times are shown in Table 3.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V.21, the transmitter turns off within 7 ms after RTS goes false. In Group 2 the transmitter turns off within 200 µs after RTS goes false. When operating in parallel data mode, the turn-off sequence may be extended by 8 bit times.

TRANSMIT LEVEL

The transmitter output level is programmable in the DSP RAM from 0 dBm to –15.0 dBm and is accurate to ± 1.0 dBm. The output level is adjusted by the modem by digitally scaling the output to the transmitters digital-to-analog converter.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with CCITT V.29 or V.27 recommendations, depending on the selected configuration.

RECEIVE LEVEL

The receiver satisfies V.29 and V.27 performance requirements for received line signal levels from 0 dBm to –43 dBm. An external input buffer and filter must be supplied between the Receiver Analog Input (RXA) and RXIN. The received line signal level is measured at the RXA input. The default turn on and turn off RLSD threshold levels are – 43 dBm and – 48 dBm, respectively. These levels are measured with an unmodulated 2100 Hz tone at RXA.

Table 3. Turn-On Sequences

Configuration	RTS On to CTS On	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.29 (All Speeds)	253 ms	441 ms
V.27 4800 bps Long Train	708 ms	913 ms
V.27 4800 bps Short Train	50 ms	255 ms
V.27 2400 bps Long Train	943 ms	1148 ms
V.27 2400 bps Short Train	67 ms	272 ms
V.21 300 bps	≤14 ms	≤14 ms
Group 2	≤400 µs	≤400 µs

The RLSD threshold levels can be programmed over the following range:

Turn on: –10 dBm to –47 dBm
Turn off: –10 dBm to –52 dBm

RECEIVER TIMING

The timing recovery circuit can track a ± 0.01% frequency error in the associated transmit timing source.

CARRIER RECOVERY

The carrier recovery circuit can track a ± 7 Hz frequency offset in the received carrier with less than a 0.2 dBm degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (RLSD) is off.

TONE DETECTION

The tone detector signal path is separate from the main received signal path enabling tone detection to be independent of the receiver status. Tone detector 3 operates in all receive modes.

The filter coefficients of each filter are host programmable in RAM. The output of the tone detector filter goes to an energy detector.

GENERAL SPECIFICATIONS

The modem power and environmental requirements are shown in Tables 4 and 5, respectively.

Table 4. Power Requirements

Voltage	Current (Typ.) @ 25° C	Current (Max.) @ 0° C
+5 VDC ±5% – 5 VDC ±5%	85 mA 15 mA	< 125 mA ≤ 30 mA

Note: All voltages must have ripple less then 0.1 volts peak-to-peak. If a switching supply is chosen, the user may select any frequency between 20 KHz and 150 KHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 µV peak.

Table 5. Environmental Requirements

Parameter	Specification
Temperature	
Operating	0° C to +70° C (32° F to 158° F)
Storage	–40° C to +80° C (–40° F to 176° F) (Stored in a suitable anti-static container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35° C, whichever is less.

HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 1) shows the typical modem connection in a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or –12 VDC for RS-232-C) is called active low and is represented by a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol.

Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal $\overline{IRQ}$). Active low signals are named with an overscore (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals shown in Figure 1 are organized into eight functional groups: power, microprocessor interface, V.24 interface, cable equalizer, analog signals, overhead, reserved, and serial diagnostic interface. These signals, along with their connector pin numbers and interface circuit types, are listed in Table 6. The digital interface characteristics are defined in Table 7.

POWER-ON-RESET

When power is applied to the modem, the modem pulses Power-On-Reset ($\overline{POR}$) low to begin the $\overline{POR}$ sequence. 350 ms after the low-to-high transition of $\overline{POR}$, the modem is ready to use. The POR sequence is reinitiated any time the + 5V supply drops below + 3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 µs. $\overline{POR}$ is not pulsed low by the modem when the POR sequence is initiated externally. The POR sequence initializes the modem interface memory (Table 10) to default values. This action leaves the modem configured as follows:

- V.29 9600 bps
- Serial channel data
- T Equalizer
- Standard echo suppressor tone
- –43 dBm receiver turn-on threshold

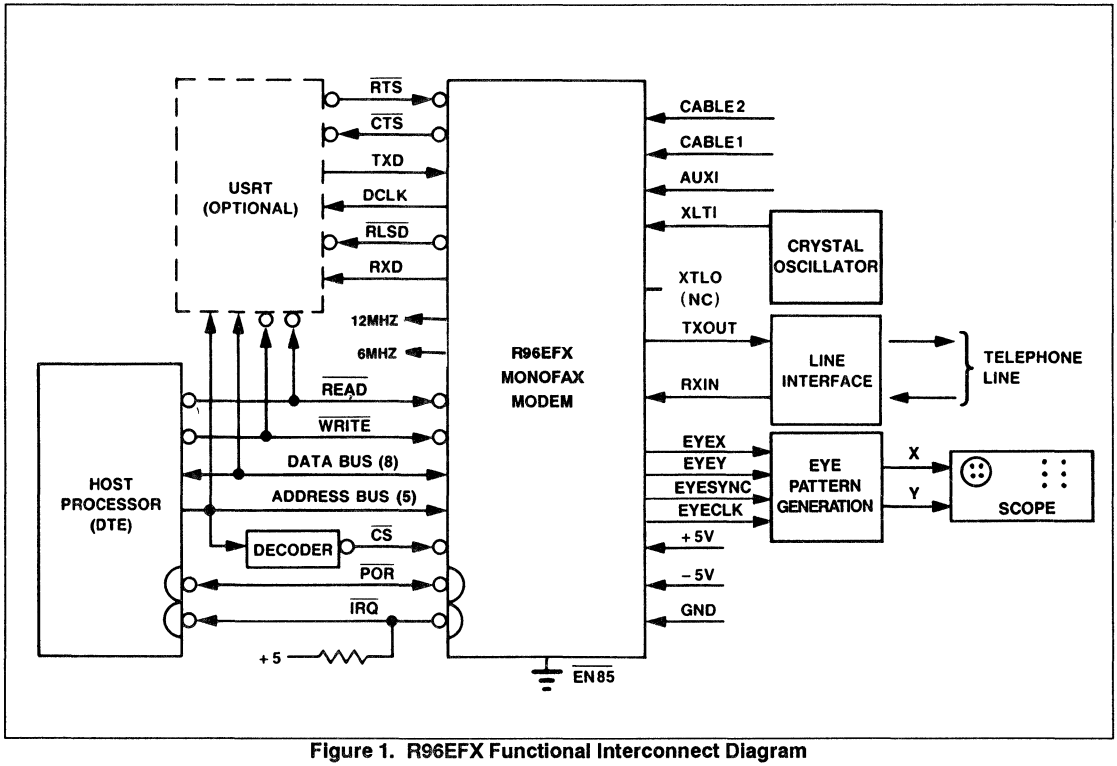


Figure 1. R96EFX Functional Interconnect Diagram

Microprocessor Interface

Seventeen address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 8080 or 68000.

The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The significance of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

Chip Select ($\overline{CS}$) and Register Selects (RS0-RS4).

The Chip Select ($\overline{CS}$) input enables the modem digital signal processor (DSP) device. The five active high register select lines (RS0-RS4) address interface memory registers within the selected DSP interface memory. All six of these lines are typically connected to the host bus address lines; the register select lines to the five least significant lines (A0-A4), and the chip select line to the next significant line (A5) through a decoder. The DSP decodes RS0 through RS4 to address one of 32 internal interface memory registers (00-1F). The most significant address bit is RS4 and the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0-D7). The most significant data bit is D7 and the least significant data bit is D0.

Table 6. R96EFX Hardware Interface Signals

Name	Type*	Pin No.	Description
Power			
AGND1	GND	22	Connect to Analog Ground
AGND2	GND	24	Connect to Analog Ground
DGND1	GND	13	Connect to Digital Ground
DGND2	GND	49	Connect to Digital Ground
+5VA	PWR	31	Connect to Analog +5V Power
+5VD	PWR	10	Connect to Digital +5V Power
−5VA	PWR	25	Connect to Analog −5V Power
Microprocessor Interface			
D7	IA/OB	50	Data Bus Line 7
D6	IA/OB	51	Data Bus Line 6
D5	IA/OB	52	Data Bus Line 5
D4	IA/OB	53	Data Bus Line 4
D3	IA/OB	54	Data Bus Line 3
D2	IA/OB	55	Data Bus Line 2
D1	IA/OB	56	Data Bus Line 1
D0	IA/OB	57	Data Bus Line 0
RS4	IA	62	Register Select 4
RS3	IA	63	Register Select 3
RS2	IA	64	Register Select 2
RS1	IA	1	Register Select 1
RS0	IA	2	Register Select 0
$\overline{CS}$	IA	60	Chip Select
$\overline{READ}$-φ2	IA	61	Read Strobe (808X), φ2 Clock (65XX)
$\overline{WRITE}$-R/$\overline{W}$	IA	59	Write Strobe (808X), R/$\overline{W}$ (65XX)
$\overline{IRQ}$	OC	58	Interrupt Request
V.24 Interface			
$\overline{RTS}$	IA	48	Request to Send
$\overline{CTS}$	OA	14	Clear to Send
TXD	IA	15	Transmit Data
$\overline{RXD}$	OA	45	Received Data
$\overline{RLSD}$	OA	46	Received Line Signal Detected
DCLK	OA	16	Transmit and Receive Data Clock
Cable Equalizer			
CABLE1	IB	32	Cable Select 1
CABLE2	IB	33	Cable Select 2
Analog Signals			
TXOUT	AA	28	Connect to Smoothing Filter Input
RXIN	AB	37	Connect to Anti-aliasing Filter Output
AUXI	AC	26	Auxiliary Analog Input

Table 6. R96EFX Hardware Interface Signals (Cont'd)

Name	Type*	Pin No.	Description
Overhead			
$\overline{PORO}$	OE	43	Power-On-Reset Output
$\overline{PORI}$	IA	5	Power-On-Reset Input
DCLKI	R	11	Connect to DCLK
ECLKIN1	R	30	Connect to EYECLK
ECLKIN2	R	38	Connect to EYECLK
SYNCIN1	R	41	Connect to EYESYNC
SYNCIN2	R	12	Connect to EYESYNC
XTLI	IC	6	Connect to Crystal Circuit or Oscillator
XTLO	R	7	Connect to Crystal Circuit or Float
12 MHz	OD	8	12 MHz Output
6 MHz	OD	9	6 MHz Output
RCVI	R	34	Connect to RCVO
RCVO	R	47	Mode Select Output
ADIN	R	20	Connect to ADOUT
ADOUT	R	39	ADC Output
DAIN	R	40	Connect to DAOUT
DAOUT	R	21	DAC/AGC Output
$\overline{EN85}$	R	4	Connect to Resistor for Bus Selection
AEE	R	29	Connect to Analog Ground
AGCIN	R	23	AGC Input
AOUT	R	36	Smoothing Filter Output
FIN	R	35	Connect to FOUT
FOUT	R	27	Smoothing Filter Output
RCI	R	42	RC Junction for POR Time Constant
Reserved			
	R	3	Do Not Connect
Serial Diagnostic Interface			
EYEX	OA	19	Serial Eye Pattern X Output
EYEY	OA	44	Serial Eye Pattern Y Output
EYECLK	OA	18	Serial Eye Pattern Clock (230.4 kHz)
EYESYNC	OA	17	Serial Eye Pattern Strobe (9600 Hz)

Notes:

* Digital signals are described in Table 7. Analog signals are described in Table 9.

R = Required overhead connectors; no connection to host equipment.

Read Enable-φ2 (READ-φ2) and Write Enable-R/W (WRITE/R/W)

During a read cycle, data from the selected DSP interface memory register is gated onto the data bus by means of three-state drivers in each DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

The read/write cycle timing waveforms are illustrated in Figure 2 and the timing requirements are shown in Table 8.

Interrupt Request (IRQ)

The modem Interrupt Request (IRQ) output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The IRQ output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem DSP device. The use of IRQ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the programmable interrupt feature and modem interrupt bits, interrupt conditions and interrupt clearing procedures.

The DSP IRQ output structure is an open-drain field-effect-transistor (FET). The modem IRQ output can be wire-ORed with other IRQ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all IRQ lines have returned high).

Because of the open-drain structure of IRQ, an external pull-up resistor to +5V is required at some point on the IRQ line. The resistor value should be small enough to pull the IRQ line high when all IRQ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem IRQ output is used, a resistor value of 5.6K ohms ±20%, 0.25 W, is sufficient.

V.24 INTERFACE

Seven pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels. The transmit and receive timing is shown in Figures 3 and 4, respectively.

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.

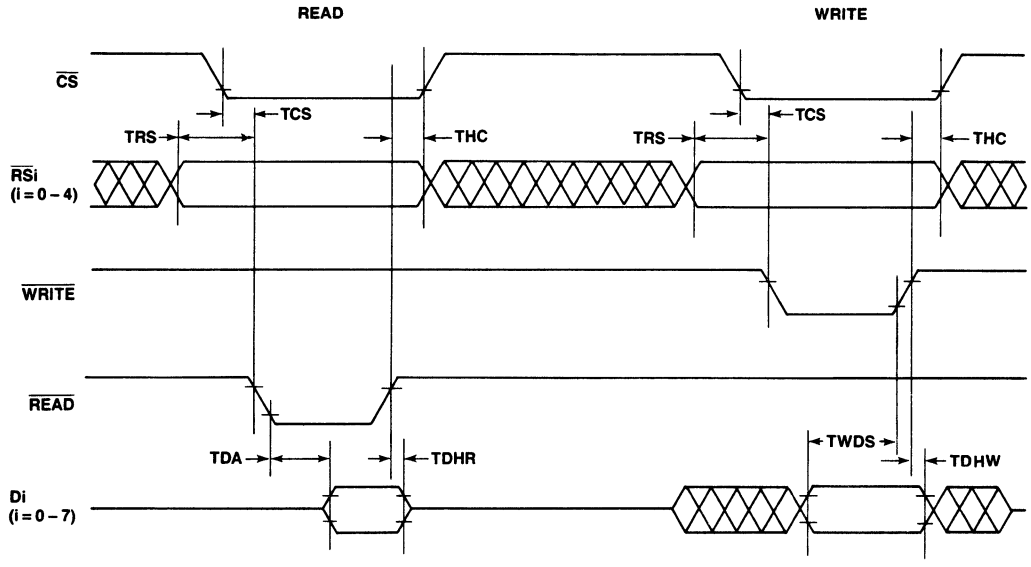
Table 8. Microprocessor Interface Timing

Parameter	Symbol	Min.	Max.	Units
CS Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	-	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns

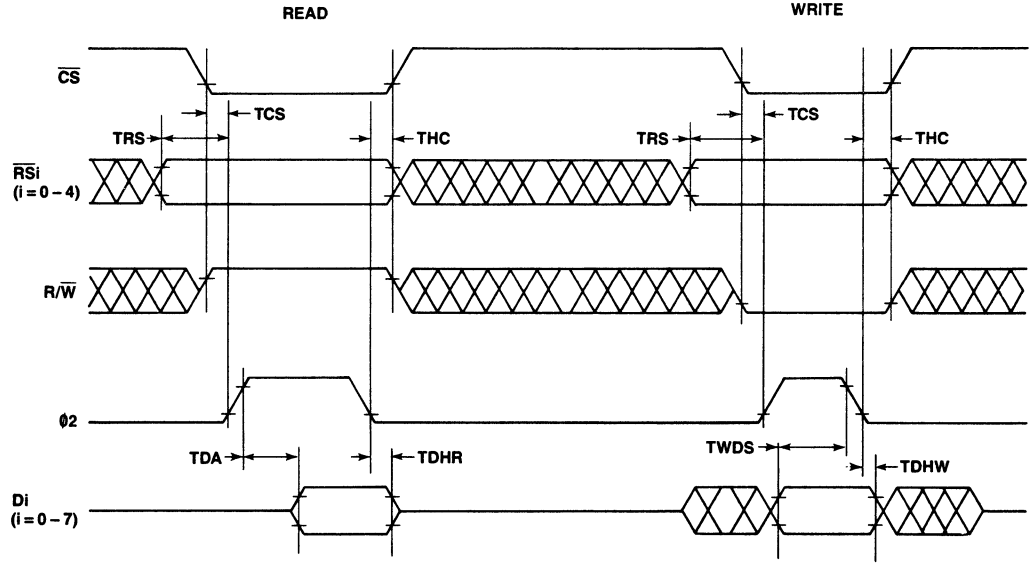
Table 7. Digital Interface Characteristics

			Input/Output Type							
Symbol	Parameter	Units	IA	IB	IC	OA	OB	OC	OD[4]	OE
V_{IH}	Input High Voltage	V	2.0 min.	2.0 min.	(See Note 3					
V_{IL}	Input Low Voltage	V	0.8 max.	0.8 max.	in Fig. 9)					
I_{IH}	Input High Current	µA		40 max.						
I_{IL}	Input Low Current	mA		–0.4 max.						
I_{LI}	Input Leakage Current	µA	±2.5 max.		11 max.					
V_{OH}	Output High Voltage	V				3.5 min.[1]	3.5 min.[1]			2.4 min.[1]
V_{OL}	Output Low Voltage	V				0.4 max.[2]	0.4 max.[3]	0.4 max.[2]		0.4 max.[2]
I_{OH}	Output High Current	mA				– 0.1 max.	– 0.1 max.		– 0.001 max.	40 min.
I_{OL}	Output Low Current	mA				1.6 max.	0.8 max.	1.6 max.	0.001 max.	0.4 max.
I_{LO}	Output Leakage Current	µA				±10 max.	± 10 max.			
C_L	Capacitive Load	pF	5	20	10					
C_D	Capacitive Drive	pF				100	100	100	50	
	Circuit Type		TTL	TTL w/pull-up	CLK	TTL 3-state	TTL 3-state	Open drain	CLK	TTL

Notes:
1. I Load = – 100 mA
2. I Load = 1.6 mA
3. I Load = 0.8 mA
4. Loads on 12 MHz and 6 MHz outputs must be balanced within 20%.



a. 8085 Bus Compatible ($\overline{EN85}$ = L)



b. 6500 Bus Compatible ($\overline{EN85}$ = H)

Figure 2. Microprocessor Interface Waveforms

Received Data (RXD)

The modem presents received serial data to the local DTE on the Received Data (RXD) output.

Request To Send ($\overline{RTS}$)

Request to Send ($\overline{RTS}$) active allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The responses to $\overline{RTS}$ are shown in Table 3.

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) active indicates to the local DTE that the modem will transmit any data present on TXD. $\overline{CTS}$ response times from an active condition of $\overline{RTS}$ are shown in Table 3.

Received Line Signal Detector ($\overline{RLSD}$)

For V.29 and V.27, Received Line Signal Detector ($\overline{RLSD}$) goes active at the end of the training sequence. If energy is above the turn on threshold and training is not detected, the $\overline{RLSD}$ off-to-on response time is 804 baud times. The $\overline{RLSD}$ on-to-off time for V.29 is 30 ± 9 ms. The V.27 $\overline{RLSD}$ on-to-off time is 11.6 ± 5 ms. The $\overline{RLSD}$ on-to-off time ensures that all valid data bits have appeared on RXD.

The $\overline{RLSD}$ receive level thresholds default to –43 dBm for the off-to-on threshold and to –48 dBm for the on-to-off threshold. A minimum hysteresis action of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm. The $\overline{RLSD}$ on and off thresholds are host programmable in DSP RAM.

Data Clock (DCLK)

The modem provides a single Data Clock (DCLK) output which performs the function of a transmitter data clock when the modem is transmitting and a receiver data clock when the modem is receiving.

DCLK as the Transmit Data Clock:

The modem outputs a synchronous transmit Data Clock, for USRT timing, when the modem is transmitting. The DCLK frequency is 9600, 7200, 4800, 2400, or 300 Hz (±0.01%) with a duty cycle of 50 ± 1%. In Group 2, the DCLK frequency is 10368 Hz ± 5 ppm when a precision oscillator (Y2 in Table 12) is used.

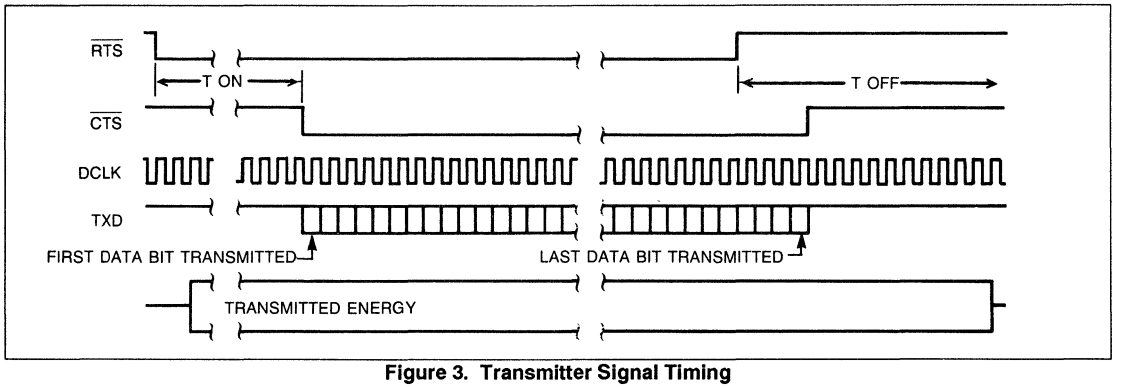


Figure 3. Transmitter Signal Timing

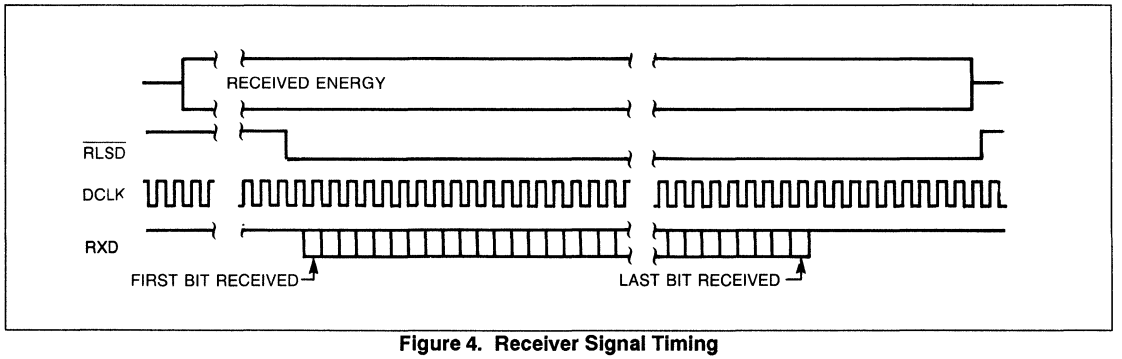


Figure 4. Receiver Signal Timing

Transmit Data (TXD) must be stable during the one µs period immediately preceding the rising edge of DCLK and following the rising edge of DCLK.

DCLK as the Receive Data Clock:

The modem outputs a synchronous receive data clock, for USRT timing, when the modem is receiving. The DCLK frequency is 9600, 7200, 4800, 2400, or 300 Hz (± 0.01%) with a duty cycle of 50 ±1%. In Group 2, the DCLK frequency is 10368 Hz ± 5 ppm when a precision oscillator (Y2 in Table 12) is used.

ANCILLARY SIGNALS

Enable 85 ($\overline{EN85}$)

The Enable 85 ($\overline{EN85}$) input selects the modem microprocessor bus compatibility. When $\overline{EN85}$ is low, the modem can interface directly to an 8085 compatible microprocessor bus using $\overline{READ}$ and $\overline{WRITE}$. When $\overline{EN85}$ is high, the modem can interface directly to a 6500 compatible microprocessor bus using $\phi 2$ and R/$\overline{W}$. In the 6500 configuration, the $\overline{READ}$ input becomes $\phi 2$ and the $\overline{WRITE}$ input becomes R/$\overline{W}$. This selection is performed when power is turned on or when $\overline{POR}$ is activated.

Cable Equalizer Select 1 and 2 (CABLE1 and CABLE2)

Modems may be connected by direct wiring, such as leased telephone cable or through the PSTN, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable, the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at the lower frequencies than at the higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. When selected, the equalizers are inserted in the transmit path when transmitting, and in the receive path when receiving. Table 2 shows the cable equalization.

The cable length equalization is selected from the CABLE1 and CABLE2 input lines as follows:

CABLE2	CABLE1	Length
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

ANALOG SIGNALS

The Transmitter Analog Output (TXOUT) and Receiver Analog Input (RXIN) allow modem connection to either a leased line or the PSTN through the appropriate buffering and an audio transformer or a data access arrangement. The Auxiliary Input (AUXI) provides access to the transmitter for summing audio signals with the modem's transmitter analog output. The analog signal characteristics are described in Table 9.

Table 9. Analog Interface Characteristics

Name	Type	Characteristic
TXOUT	AA	Maximum output: ±3.03 volts Minimum load: 10K Ω Smoothing filter transfer function: 28735.63/(s + 11547.34)
RXIN	AB	Input impedance: 1M Ω Anti-aliasing filter transfer function: 21551.72/(s + 11547.34)
AUXI	AC	Maximum input frequency: 4800 Hz Input Impedance: 1M Ω Gain to TXOUT: +5.6 dBm ±1 dBm

Transmitter Analog Output (TXOUT)

TXOUT can supply a maximum of ± 3.03 volts into a load resistance of 10K ohms minimum. A 600 ohm line impedance can be matched using an external smoothing filter with a 604 ohm series resistor in its output. The smoothing filter should have a transfer function of 28735.63/(s + 11547.34).

Receiver Analog Input (RXIN)

The RXIN input impedance is greater than 1M ohms. RXIN requires an external anti-aliasing filter between the modem and the line interface, with a transfer function of 21551.72/(s + 11547.34). The maximum input level into the anti-aliasing filter should not be greater than 0 dBm.

The filters required for anti-aliasing on the receiver input and the smoothing filter on the transmitter output have a single pole within the modem's passband (11,542 radians). Internal filters compensate for its presence, therefore, the pole location must not be changed. Some variation from the recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10K ohms (see Recommended Modem Interface Circuit.)

Auxiliary Analog Input (AUXI)

AUXI allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled input, any signal above 4800 Hz will cause aliasing errors. The input impedance is >1M ohm, and the gain to TXOUT is +5.6 dBm ± 1 dBm.

DIAGNOSTIC SIGNALS

Four signals provide the timing necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. Timing of these signals is illustrated in Figure 5 and an example eye pattern generation schematic is shown in Figure 6.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

EYEX and EYEY outputs are 15-bit words, each with 8-bits of significance. The 15-bit data words are shifted out most significant bit first with the seven most significant bits set equal to zero. EYEX and EYEY are clocked by the rising edge of EYECLK.

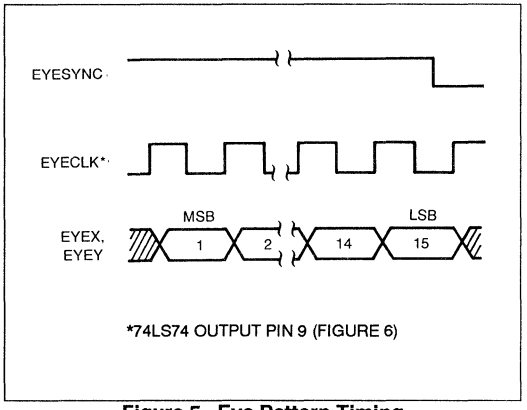


Figure 5. Eye Pattern Timing

EYECLK

EYECLK is a clock provided to create a clock which can be used by the serial-to-parallel converters to shift in the EYEX and EYEY data (see Figure 5).

EYESYNC

EYESYNC is a strobe for loading the D/A converters.

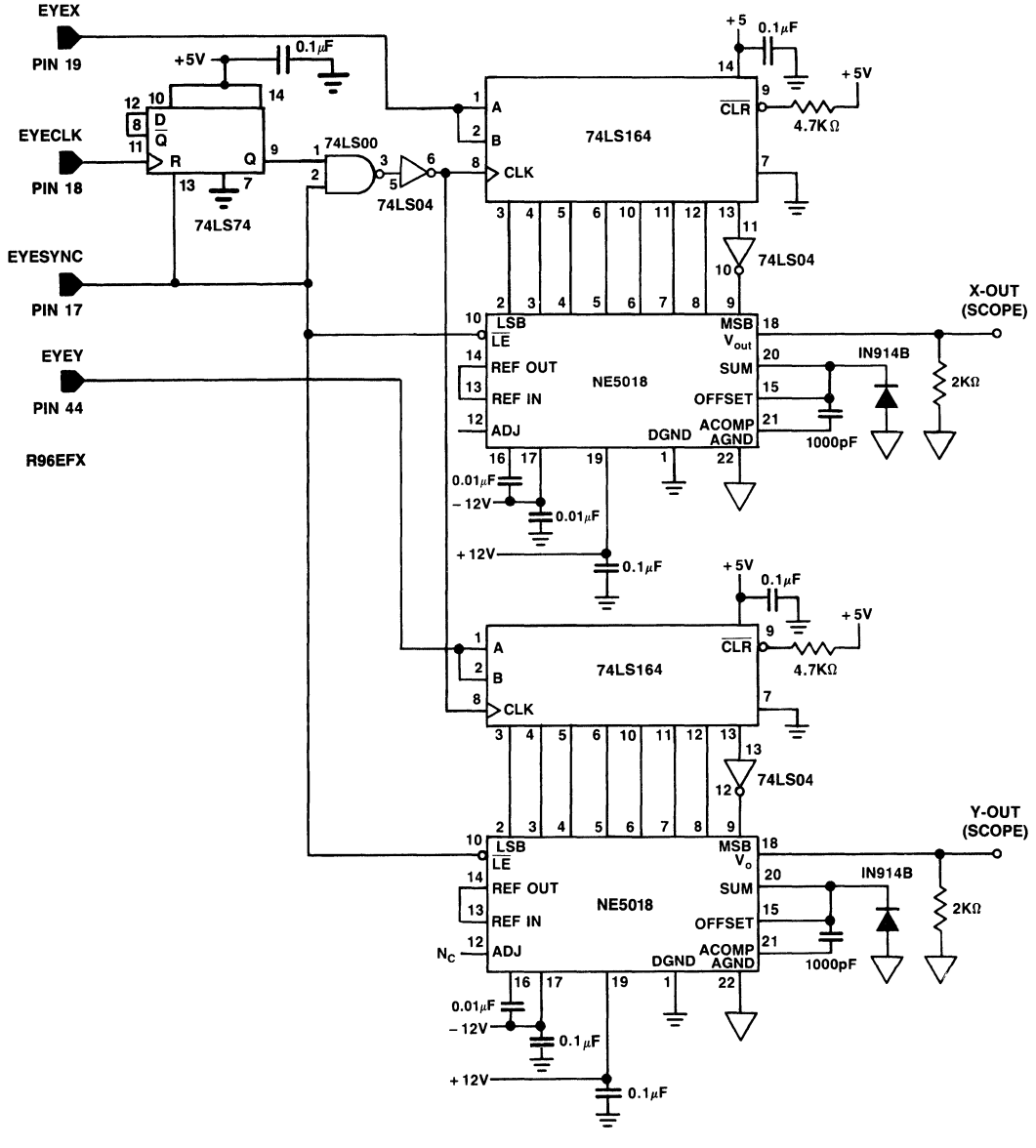


Figure 6. Eye Pattern Circuit

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in a single DSP.

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAPS

A memory map of the 32 addressable registers in the modem is shown in Figure 7. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register and then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, the entire register (8-bits) must first be read, the necessary bits must be set or reset without altering the other register bits, then the byte (8-bits) containing both the unaltered and modified bits must be written back into the interface memory.

INTERFACE MEMORY BIT DEFINITIONS

Table 10 defines the individual bits in the interface memory. In the Table 10 descriptions, bits in the interface memory are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

Figure 5. R96EFX Interface Memory

Register	Bit 7	6	5	4	3	2	1	0
1F	PIA	—	—	PIE	PIREQ	—	—	SETUP
1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1
1D	—	—	—	—	—	—	—	—
1C	—	—	—	—	—	—	—	—
1B	—	—	—	—	—	—	—	—
1A	—	—	—	—	—	—	—	—
19	—	—	—	—	—	—	—	—
18	—	—	—	—	—	—	—	—
17	—	—	—	—	—	—	—	—
16	—	—	—	—	—	—	—	—
15	ACC2	0	0	0	0	BR2	WRT2	CR2
14	RAM ADDRESS 2 (ADD2)							
13	X RAM DATA 2 MSB (XDAM2)							
12	X RAM DATA 2 LSB (XDAL2)							
11	Y RAM DATA 2 MSB (YDAM2)							
10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)							
0F	FED		—	—	—	—	CTSP	CDET
0E	—	—	—	—	—	—	—	—
0D	RX	PN	—	—	G2FGC	—	—	—
0C	—	—	—	—	—	—	—	—
0B	ITBMSK							
0A	TRIG		ANDOR	ITADRS				
09	OVRUN	EQSV	EQFZ	ZEROC	ABIDL	EOF	CRC	FLAG
08	FR3	FR2	FR1	12TH	—	—	—	—
07	RTSP	TDIS	PDM	SHTR	EPT	SQEXT	T2	HDLC
06	CONF							
05	ACC1	0	0	0	0	BR1	WRT1	CR1
04	RAM ADDRESS 1 (ADD1)							
03	X RAM DATA 1 MSB (XDAM1)							
02	X RAM DATA 1 LSB (XDAL1)							
01	Y RAM DATA 1 MSB (YDAM1)							
00	Y RAM DATA 1 LSB (YDAL1)							

(—) Indicates reserved for modem use only.

Figure 7. R96EFX DSP Interface Memory Map

Table 10. R96EFX Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
12TH	8:4	0	**Select 12th Order.** The one state of 12TH operates the tone detectors as one 12th order filter (uses FR3). The zero state of 12TH operates the tone detectors as three parallel independent 4th order filters (FR1, FR2, FR3). 12TH is operable in FSK, Group 2, and tone modes. (i.e., CONF = 20, 40, 80; with $\overline{RTS}$ off.)
ABIDL	9:3	–	**Abort/Idle.** When the modem is configured as a transmitter and control/status bit ABIDL is a 1, the modem will finish sending the current DBUFF byte. The modem will then send continuous ones if ZEROC is a 0, or continuous zeros if ZEROC is a 1. When ABIDL is a 0, the modem will not send continuous ones or zeros. If ABIDL is reset one DCLK cycle after being set, the modem will transmit eight continuous ones if ZEROC is a 0, or eight continuous zeros if ZEROC is a 1. ABIDL is also set by the modem when the underrun condition occurs (bit OVRUN is set) and the modem will send at least eight continuous ones (if ZEROC is 0) or eight continuous zeros (if ZEROC is 1). To stop continuous one or zero transmission, ABIDL must be reset by the host. (HDLC mode only) When the modem is configured as a receiver and status bit ABIDL is a 1, the modem has received a minimum of seven consecutive ones. To recognize further occurrences of this abort condition, ABIDL must be reset by the host. (HDLC mode only)
ACC1	5:7	1	**RAM Access 1.** When control bit ACC1 is a 1, the modem accesses the RAM associated with the address in ADD1 and the CR1 bit. WRT1 determines if a read or write is performed.
ACC2	15:7	1	**RAM Access 2.** When control bit ACC2 is a 1, the modem accesses the RAM associated with the address in ADD2 and the CR2 bit. WRT2 determines if a read or write is performed.
ADD1	4:0-7	17	**RAM Address 1.** ADD1 contains the RAM address used to access the modem's X and Y Data RAM (CR1 = 0) or X and Y Coefficient RAM (CR1 = 1) via the X RAM Data 1 LSB and MSB words (2:0-7 and 3:0-7, respectively) and the Y RAM Data 1 LSB and MSB words (0:0-7 and 1:0-7, respectively).
ADD2	14:0-7	11	**RAM Address 2.** ADD2 contains the RAM address used to access the modem's X and Y Data RAM (CR2 = 0) or X and Y Coefficient RAM (CR2 = 1) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7, respectively) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
ANDOR	A:5	–	**AND/OR Bit Mask Function.** When control bit ANDOR is a 1and the programmable interrupt is enabled, the modem will assert $\overline{IRQ}$ if all the bits in the register specified by ITADRS and masked by ITBMSK are ones. When ANDOR is a 0 and the programmable interrupt is enabled, the modem will assert $\overline{IRQ}$ if any one of the bits in the register specified by ITADRS and masked by ITBMSK is a one.
BA1	1E:0	–	**Buffer Available 1.** When set to a 1, status bit BA1 signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) register (0:0-7). This condition can also cause $\overline{IRQ}$ to be asserted (see IE1 and IA1). The host writing to or reading from register 00 resets the BA1 and IA1 bits to 0. (See IE1 and IA1.)
BA2	1E:3	–	**Buffer Available 2.** When set to a 1, status bit BA2 signifies that, when the modem is in the parallel data mode or the HDLC mode, it has read register 10:0-7 (DBUFF) when transmitting (buffer becomes empty), or it has written register 10:0-7 (DBUFF) when receiving (buffer becomes full). When the modem is not in parallel data mode, the setting of BA2 to a 1 by the modem signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) register (10:0-7). These conditions can also cause $\overline{IRQ}$ to be asserted (see IE2 and IA2). The host writing to or reading from register 10 resets the BA2 and IA2 bits to 0. (See IE2 and IA2.)
BR1	5:2	0	**Baud Rate 1.** When control bit BR1 is a 1, RAM access associated with ADD1 occurs at the modem baud rate; when BR1 is a 0, RAM access occurs at the modem sample rate. This bit must be reset to a zero in G2, FSK, or Tone mode (CONF = 40, 20, or 80, respectively).
BR2	15:2	0	**Baud Rate 2.** When control bit BR2 is a 1, RAM access associated with ADD2 occurs at the modem baud rate; when BR2 is a 0, RAM access occurs at the modem sample rate. This bit must be reset to a zero in G2, FSK, or Tone mode (CONF = 40, 20, or 80, respectively).

Table 10. R96EFX Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CDET	F:0	–	**Carrier Detected.** When status bit CDET is a 1, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is a 0, the receiver is in the idle state or in the process of training.
CONF	6:0-7	14	**Configuration.** The CONF control bits select one of the following transmitter/receiver configurations: **CONF — Configuration** 14 — V.29 9600 bps 12 — V.29 7200 bps 11 — V.29 4800 bps 0A — V.27 4800 bps 09 — V.27 2400 bps 20 — V.21 Channel 2 300 bps (FSK) 40 — Group 2 (G2) 80 — Tone Transmit ($\overline{RTS}$ or RTSP on), Tone Detect ($\overline{RTS}$ and RTSP off) **Configuration Definitions:** 1. **V.29.** When a V.29 configuration is selected, the modem operates as specified in CCITT Recommendation V.29. 2. **V.27.** When a V.27 configuration is selected, the modem operates as specified in CCITT Recommendation V.27. 3. **V.21 Channel 2.** When the V.21 Channel 2 configuration is selected, the modem operates as specified in CCITT Recommendation V.21 channel 2. 4. **Group 2.** When the Group 2 configuration is selected, the modem operates as specified in CCITT Recommendation T.3. 5. **Tone Transmit.** When the Tone Transmit configuration is selected, the modem transmits single or dual frequency tones in response to $\overline{RTS}$ or RTSP. Tone frequencies and amplitudes are programmable in the RAM. 6. **Tone Detect.** When the Tone Detect configuration is selected and 12th is set to a 1, the three 4th order tone detect filters are combined into a single 12th order tone detect filter (FR3). If 12th is not set to a 1, the three tone detect filters are placed in parallel and are independent (FR1, FR2, and FR3). All tone detect filters are programmable.
CRC	9:1	–	**Cyclic Redundancy Check error.** When status bit CRC is a 1 and status bit EOF is a 1, the received frame is in error. When CRC is a 0 and EOF is a 1, the received frame is correct. CRC only changes immediately before EOF is set to a 1. (HDLC mode only)
CR1	5:0	0	**Coefficient RAM 1 Select.** When control bit CR1 is a 1, ADD1 addresses Coefficient RAM. When CR1 is a 0, ADD1 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CR2	15:0	0	**Coefficient RAM 2 Select.** When control bit CR2 is a 1, ADD2 addresses Coefficient RAM. When CR2 is a 0, ADD2 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CTSP	F:1	–	**Clear To Send Parallel.** When set to a 1, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at TXD will be transmitted. CTSP parallels the operation of the CTS pin.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode, the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first

Table 10. R96EFX Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
EOF	9:2	–	**End Of Frame.** When the modem is configured as a transmitter, the EOF bit is a control bit. To convey to the modem that it is time to send the FCS and ending flag of a HDLC frame, the host must set the EOF bit after the modem has taken the last byte of data (resides in DBUFF) of the frame (BA2 sets again). EOF will be reset by the modem after it has recognized the setting of EOF by the host. (HDLC mode only) When the modem is configured as a receiver and status bit EOF is a 1, the modem has received a frame ending flag and bit CRC is updated. EOF must be reset by the host before receiving the ending flag of a following frame. (HDLC mode only)
EPT	7:3	0	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 which transmits 20 ms of silence at the beginning of training.
EQFZ	9:5	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.
EQSV	9:6	0	**Equalizer Save.** When control bit EQSV is a 1, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training. This bit is used in conjunction with the SHTR bit and must be followed by the setting of the SETUP bit.
FED	F:7,6	–	**Fast Energy Detector.** Status bits FED indicates the level of the received signal according to the following codes. **FED** — **Energy Level** 0 — No energy 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold
FLAG	9:0	0	**FLAG Mode.** When the modem is configured as a transmitter and status bit FLAG is a 1, the modem is transmitting a flag sequence. (HDLC mode only) When the modem is configured as a receiver and status bit FLAG is a 1, the modem has received a flag sequence. (HDLC mode only)
FR1	8:5	0	**Frequency No. 1.** The one state of FR1 indicates that energy is above tone detector 1's detected turn-on threshold (default detection range = 2100 Hz ± 25 Hz in non-Group 2 mode). FR1 is operable in FSK, Group 2, and tone modes. (i.e., CONF = 20, 40, 80; with RTSP and $\overline{\text{RTS}}$ off.)
FR2	8:6	0	**Frequency No. 2.** The one state of FR2 indicates that energy is above tone detector 2's detected turn-on threshold (default detection range = 1100 Hz ± 30 Hz in non-Group 2 mode). FR2 is operable in FSK, Group 2, and tone modes. (i.e., CONF = 20, 40, 80; with RTSP and $\overline{\text{RTS}}$ off.)
FR3	8:7	0	**Frequency No.3.** The one state of FR3 indicates that energy is above tone detector 3's detected turn-on threshold (default detection range = 462 Hz ±14 Hz in non-Group 2 mode). FR3 is operable in FSK, high speed, Group 2, and tone modes. (i.e., CONF = 14, 12, 11, 0A, 09, 20, 40, 80; with RTSP and $\overline{\text{RTS}}$ off.)
G2FGC	D:3	0	**Group 2 Fast Gain Control.** The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group 2 Facsimile.
HDLC	7:0	0	**HDLC mode.** When control bit HDLC is a 1, the modem performs HDLC framing. To become active, the host must set HDLC and PDM followed by the setting of SETUP. When control bit HDLC is a 0, the modem does not perform HDLC framing provided SETUP was set following the resetting of HDLC.

Table 10. R96EFX Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
IA1	1E:6	–	**Interrupt Active 1.** When Interrupt Enable 1 is enabled (IE1 is a 1) and BA1 is set to a 1 by the modem, the modem asserts IRQ and sets status bit IA1 to a 1 to indicate that BA1 going to a 1 caused the interrupt. The host writing to or reading from register 0:0 resets IA1 to a 0. (See IE1 and BA1.)
IA2	1E:7	–	**Interrupt Active 2.** When Interrupt Enable 2 is enabled (IE2 is a 1) and BA2 is set to a 1 by the modem, the modem asserts IRQ and sets status bit IA2 to a 1 to indicate that BA2 going to a 1 caused the interrupt. The host writing to or reading from register 10:0 resets IA2 to a 0. (See IE2 and BA2.)
IE1	1E:2	0	**Interrupt Enable 1.** When control bit IE1 is a 1 (interrupt enabled), the modem will assert IRQ and set IA1 to a 1 when BA1 is set to 1 by the DSP. When IE1 is a 0 (interrupt disabled), BA1 has no effect on IRQ and IA1. (See BA1 and IA1.)
IE2	1E:5	0	**Interrupt Enable 2.** When control bit IE2 is a 1 (interrupt enabled), the modem will assert IRQ and set IA2 to a 1 when BA2 is set to 1 by the DSP. When IE2 is a 0 (interrupt disabled), BA2 has no effect on IRQ and IA2. (See BA2 and IA2.)
ITADRS	A:0-4	–	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take affect. The address of the byte on which the modem asserts IRQ on a bit or bits in that byte is specified below: **Host Register (Hex) / ITADRS (Hex) / Host Register (Hex) / ITADRS (Hex)** 00 / 00 / 10 / 08 01 / 10 / 11 / 18 02 / 01 / 12 / 09 03 / 11 / 13 / 19 04 / 02 / 14 / 0A 05 / 12 / 15 / 1A 06 / 03 / 16 / 0B 07 / 13 / 17 / 1B 08 / 04 / 18 / 0C 09 / 14 / 19 / 1C 0A / 05 / 1A / 0D 0B / 15 / 1B / 1D 0C / 06 / 1C / 0E 0D / 16 / 1D / 1E 0E / 07 / 1E / 0F 0F / 17 / 1F / 1F
ITBMSK	B:0-7	–	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert IRQ on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset by the host.
OVRUN	9:7	–	**Overrun/Underrun.** When the modem is configured as a transmitter, and status bit OVRUN is a 1, a transmit underrun condition has occurred. If the host does not load in a new byte of data in DBUFF within eight bit times of loading the previous byte into DBUFF, OVRUN and ABIDL will set. The modem will then automatically send eight continuous ones. The transmission of these ones will continue until the host resets ABIDL. The modem will then finish sending the current group of eight ones and will either start sending another frame (if BA2 is reset) or will transmit continuous flags. The modem will reset OVRUN every time it sets BA2. (HDLC mode only) When the modem is configured as a receiver and status bit OVRUN is a 1, an overrun condition has occurred. To detect the next overrun condition, the host must reset this bit. (HDLC mode only)

Table 10. R96EFX Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
PDM	7:5	0	**Parallel Data Mode.** When control bit PDM is a 1 and the modem is a transmitter, it accepts data for transmission from DBUFF (10:0-7) rather than the TXD input. When PDM is a 1 and the modem is a receiver, the modem provides the received data to the host using DBUFF (10:0-7).
PIA	1F:7	–	**Programmable Interrupt Active.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. PIA is reset when the host resets PIREQ.
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. When PIE is a 0 (interrupt disabled), ITBMSK, ITADRS, TRIG, ANDOR, and PIREQ have no effect on IRQ and PIA.
PIREQ	1F:3	–	**Programmable Interrupt Request.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if control bit PIREQ has been previously reset by the host. PIREQ is set by the modem when the programmable interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the modem will not assert IRQ.
PN	D:6	–	**PN Sequence Detected.** When status bit PN is a 1, the receiver is detecting the PN portion of the training sequence. When PN is a 0, PN is not being detected.
RTSP	7:7	0	**Request To Send Parallel.** The one state of RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is turned off, and the turn-off sequence has been completed. RTSP parallels the operation of the hardware RTSP control input. These inputs are "ORed" by the modem.
RX	D:7	–	**Receive State.** When status bit RX is a 1, the modem is in the receive state and is not transmitting.
SETUP	1F:0	0	**Setup.** Control bit SETUP bit must be set to a 1 by the host after the host writes a configuration code into the CONF bits (register 6:0-7) or changes a bit in 7:0-6 (register 7 bits 0 through 6). This informs the modem to implement the configuration change. The modem resets the SETUP bit to a 0 when the configuration change is implemented.
SHTR	7:4	0	**Short Train.** When SHTR is a 1 and CONF is either 0A or 09, the modem will perform a V.27 ter short training sequence. A successful V.27 ter long train at the same data rate must precede the short train. The setting of the SHTR bit, along with the setting of the EQSV bit, must be followed by the setting of the SETUP bit.
SQEXT	7:2	0	**Squelch Extend.** When control bit SQEXT is a 1, the modem's receiver is inhibited from the reception of any signal for 140 ms after the transmitter turn-off.
T2	7:1	0	**T/2 Equalizer Select.** When control bit T2 is a 1, the linear section of the receiver's adaptive equalizer is T/2 fractionally spaced. When T2 is a 0, the equalizer is T spaced (T = 1 baud time).
TDIS	7:6	0	**Training Disable.** When control bit TDIS is a 1, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when RTS or RTSP is activated.

Table 10. R96EFX Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
TRIG	A:6-7	–	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled. The user has the option to be continuously interrupted whenever the interrupt condition is true (DC triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true or from true to false (edge triggered): **TRIG** **Description** 00 DC 01 Positive Edge 10 Negative Edge 11 Edge
WRT1	5:1	0	**RAM Write 1.** When control bit WRT1 is a 1 and ACC1 is set to a 1, the modem writes the data from the Y RAM Data 1 registers into its internal RAM at the location addressed by ADD1 and CR1. (When the most significant bit of ADD1 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT1 is a 0 and ACC1 is set to a 1, the modem reads data from its internal RAM from the locations addressed by ADD1 and CR1 and stores it into the X RAM Data 1 registers and Y RAM Data 1 registers, respectively.
WRT2	15:1	0	**RAM Write 2.** When control bit WRT2 is a 1 and ACC2 is set to a 1, the modem writes the data from the Y RAM Data 2 registers into its internal RAM at the location addressed by ADD2 and CR2. (When the most significant bit of ADD2 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT2 is a 0 and ACC2 is set to a 1, the modem reads data from its internal RAM from the locations addressed by ADD2 and CR2 and stores it into the X RAM Data 2 registers and Y RAM Data 2 registers, respectively.
XDAL1	2:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the least significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the least significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	3:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	0:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the least significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the least significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
YDAM1	1:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the most significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the most significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
ZEROC	9:4	0	**Zero Clamp.** When control bit ZEROC is a 1 and ABIDL is a 1, the modem will transmit continuous zeros. When ZEROC is a 0 and ABIDL is a 1, the modem will transmit continuous ones. If ABIDL is 0, ZEROC is disabled. (HDLC mode only)

DSP RAM ACCESS

Table 11 provides the RAM access functions, codes, and registers.

DSP RAM Organization

The DSP contains 16-bit words of random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM.

Interface Memory Access to DSP RAM

The interface memory acts as an intermediary during host to DSP RAM, or DSP RAM to host, data exchanges. The address stored in DSP interface memory RAM Address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud or sample time, as selected by the BR1 and BR2 bits. The baud rate is determined by the selected configuration, but the sample rate is fixed at 9600 Hz, except in Group 2 where the sample rate is 10368 Hz.

Two RAM Access bits in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The transfer is initiated by the host setting the ACC1 and/or the ACC2 bit(s). The DSP tests these bits each baud or sample period, except in G2, FSK or Tone mode where these bits are always tested at the sample period.

If parallel data mode is selected, RAM access associated with RAM Address 2 is disabled and only RAM access associated with RAM Address 1 is available.

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Table 11. R96EFX RAM Access Codes

Function	BRx	CRx	ADDx	Read Reg. No.
Received Signal Samples	0	0	15	2,3
Received Signal Samples FSK	0	0	31	2,3
Demodulator Output	0	0	13	0,1,2,3
Lowpass Filter Output	0	0	02	0,1,2,3
Average Energy	0	0	14	2,3
AGC Gain Word	0	1	15	2,3
Tone 1 Frequency	0	1	21	2,3
Tone 1 Level	0	0	22	2,3
Tone 2 Frequency	0	1	22	2,3
Tone 2 Level	0	0	23	2,3
Output Level	0	0	21	2,3
Equalizer Input (Real)	1	0	1E	0,1
Equalizer Input (Imag)	1	1	1E	0,1
Equalizer Tap Coefficients	1	1	38 - 5F	0,1,2,3
Unrotated Equalizer Output	1	0	1C	0,1,2,3
Rotated Equalizer Output (Eye Pattern)	1	1	17	0,1,2,3
Decision Points (Ideal)	1	0	17	0,1,2,3
Error Vector	1	1	1D	0,1,2,3
Rotation Angle	1	1	0C	0,1
Frequency Correction	1	1	18	2,3
Eye Quality Monitor (EQM)	1	1	0D	2,3
Turn-on Threshold (RLSD)	0	1	37	2,3
Turn-off Threshold (RLSD)	0	1	B7	0,1
Group 2 PLL Frequency Correction	0	0	0D	2,3
Group 2 Zero Crossing Threshold (Negative)	0	0	19	2,3
Group 2 Zero Crossing Threshold (Positive)	0	0	99	0,1
Group 2 AGC Slew Rate	0	1	05	2,3
Group 2 Black-White Threshold	0	0	24	2,3
Group 2 Phase Limit Value	0	0	1A	2,3
Receiver Sensitivity	0	1	24	2,3

DSP RAM Read Procedure

The RAM read procedure is a 32-bit transfer from DSP RAM to the interface memory which transfers both the X RAM and Y RAM simultaneously. Before reading from DSP interface memory, set ACC1 and/or ACC2 to a 0, then reset BA1 or BA2 by reading YDAL1 or YDAL2. Set WRT1 and/or WRT2 to a 0 to inform the DSP that a RAM read will occur when ACC1 and/or ACC2 is set to a 1. Load the RAM address into RAM Address 1 and/or RAM Address 2, then set CR1 and/or CR2 appropriately. Set ACC1 and/or ACC2 to a 1 to signal the DSP to perform the RAM read. When the DSP has transferred the contents of RAM into the interface memory RAM Data registers, BA1 and/or BA2 will be set.

If IE1 and/or the IE2 is a 1, $\overline{IRQ}$ is also asserted when BA1 and/or BA2 set to a 1 by the DSP. When $\overline{IRQ}$ is asserted, IA1 and/or IA2 goes to a 1 to inform the host that setting of BA1 and/or BA2 was the cause. IA1 and/or IA2 is cleared by the host reading YDAL1 and/or YDAL2, which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

DSP RAM Write Procedure

The RAM write procedure is a 16-bit transfer from interface memory to DSP RAM allowing the transfer of X RAM data or Y RAM data to occur each baud or sample time. Before writing to DSP interface memory, set ACC1 and/or ACC2 to a 0; then reset BA1 or BA2 by reading YDAL1 or YDAL2, respectively. Set WRT1 and/or WRT2 to a 1 to inform the DSP that a RAM write will occur when ACC1 and/or ACC2 is set to a 1. Load the RAM address into RAM Address 1 and/or RAM Address 2, then set CR1 and/or CR2 appropriately. Write the desired data into the interface memory RAM Data registers YDAL1 and YDAM1 and/or YDAL2 and YDAM2, then set ACC1 and/or ACC2 to a 1 to signal the DSP to perform the RAM write. When the DSP has transferred the contents of the interface memory RAM Data registers into RAM, BA1 and/or BA2 will be set.

If IE1 and/or IE2 is a 1, $\overline{IRQ}$ is also asserted and IA1 and/or IA2 is set to a 1 when BA1 and/or BA2 is set to a 1 by the DSP. IA1 and/or IA2 is cleared by writing into YDAL1 and/or YDAL2, which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

PROGRAMMABLE INTERRUPT FEATURE

An interface memory interrupt feature is included in the R96EFX. This feature enables the user to select an interrupt to occur on any combination of bits within interface memory register.

The programmable interrupt routine runs at the sample rate in all transmitter and receiver modes. If the host sets the Programmable Interrupt Enable bit 1F:3 (PIE), the modem sets the Programmable Interrupt Active bit 1F:7 (PIA) and $\overline{IRQ}$ goes low when the interrupt condition is true. The Programmable Interrupt Request bit 1F:3 (PIREQ) is set by the modem whenever the interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem is unable to reset this bit.

An interrupt may occur only within a single interface memory register based upon any combination of bits. For example, the host may select register 9 and generate an interrupt whenever bits 9:3, 9:4, and 9:7 are set, but may not select bits 8:7 and 9:2 to generate an interrupt. The register is selected by specifying the interrupt address A:0-4 (ITADRS) (see ITADRS).

The interrupt bit mask register B:0-7 (ITBMSK) selects the bits to be tested in the interface memory register specified by ITADRS. For example, if ITBMSK is equal to FF all the bits are selected; if ITBMSK is equal to 0F, the four least significant bits are selected.

There are two operating modes with each mode having four options. The user may choose to OR the selected bits, or to AND the selected bits. Whenever any of the selected bits are set, the OR mode is true. The AND mode is true whenever all the selected bits are set, and false otherwise. When bit A:5 (ANDOR) is set to a 1, the AND mode is chosen; when ANDOR is reset to a 0, the OR mode is chosen. The user has the option to be continuously interrupted whenever the mode is true (DC triggered), to be interrupted only when the mode transitions from true to false (negative edge triggered), to be interrupted only when the mode transitions from false to true (positive edge triggered), or to be interrupted when the mode transitions from false to true and when the mode transitions from true to false (edge triggered). The host selects one of the above options by specifying bits A:6-7 (TRIG) (see TRIG).

HDLC OPERATION

Data and control information on an HDLC link are transmitted via frames. These frames organize the information into a format specified by ISO that enables the transmitting and receiving station to synchronize with each other. This format is shown in below.

HDLC TRANSMITTER

The R96EFX HDLC transmitter works at all Group 3 speeds. The modem will automatically transmit the beginning and ending flags as well as the 16-bit Frame Check Sequence (FCS). The host must wait until $\overline{CTS}$ or CTSP is set by the modem before loading in the first byte of data. When BA2 is set by the modem, the host can load in the next byte of data. As soon as the host is finished with all the bytes in the frame and the modem has taken the last byte of the frame (BA2 sets), the host must set EOF to tell the modem it is time to end the frame. When the modem recognizes EOF being high, the modem will reset EOF and will transmit the FCS and closing flag. Once the host sets EOF, the host may load in the first byte of the next frame. If the host wants to end transmission, the host must wait for EOF to return low before turning off RTS or RTSP.

Further detail is given in the R96EFX HDLC and Programmable Interrupt Features Application Note (Order No. 826).

HDLC RECEIVER

The R96EFX HDLC receiver also works at all Group 3 speeds. The modem will automatically strip off flags and the 16 bit FCS sequence and only present the host with data. At the end of a frame (EOF is set), the host must check bit CRC to determine if the frame had an error. Thus, error detection is accomplished.

PERFORMANCE

TYPICAL BIT ERROR RATES

The bit error rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm as illustrated.

Typical BER performance is shown in Figure 8.

The curves shown in Figure 8 were prepared from data obtained using a TAS 1000 communication test system.

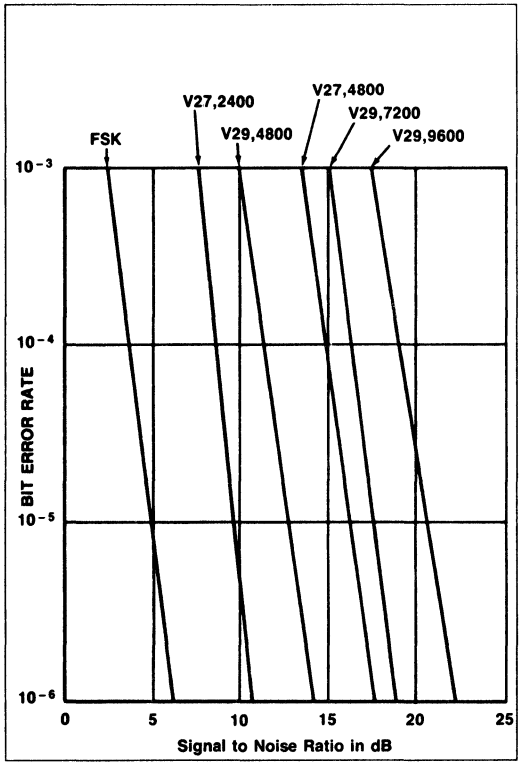
TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-noise phase jitter at 120 Hz.

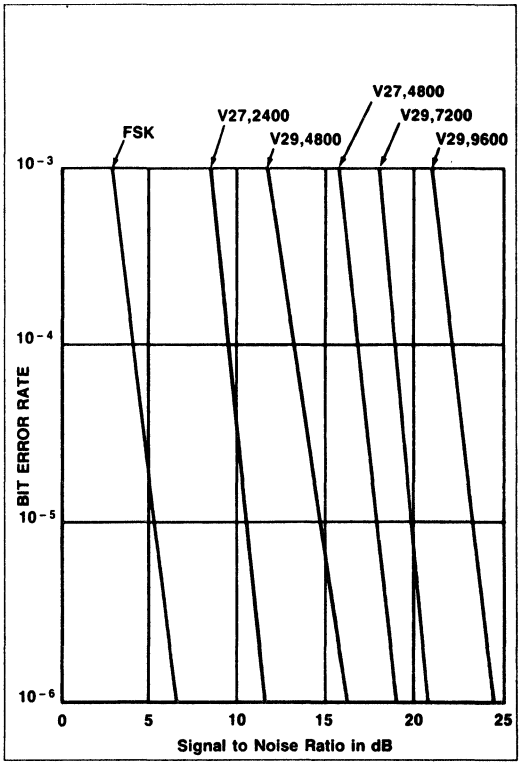
At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12 peak-to-peak phase jitter at 300 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.



Typical Bit Error Rate
(Back-to-Back, T Equalizer, Level – 20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer Level – 20 dBm)

Figure 8. R96EFX Typical Bit Error Rate (BER) Curves

APPLICATION

RECOMMENDED MODEM INTERFACE CIRCUIT

The R96EFX is supplied as a 64-pin QUIP (Quad In-line Package) device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit (Figure 9) and parts list (Table 12) illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R10 and R16 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3K ohm series resistor should be used on each input (pins 32 and 33) for isolation.

Resistors R7 and R17 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more that 99.8% of the units.

Table 13. TC0-706AB Oscillator Specifications

Characteristic	Value
Frequency	24.00014 MHz
Frequency Stability	
vs. Temperature	± 5 ppm (0°C - 60°C)
vs. Input Voltage	± 1 ppm at 4.75 V - 5.25 V
vs. Aging	1 ppm/year
Frequency Tolerance	± 2 ppm
Frequency Adjustment	
by Internal Trimmer	± 5 ppm min.
Operating Temperature	0°C - 60° C
Input Voltage	5.0 V ± 0.5% (4.75 V - 5.25 V)
Output	
Symmetry	50% ± 10% (40% - 60%)
Drive	CL = 15 pF
Type	CMOS: Low = 0.5 V, High = Vcc (4.5 V)
Package	14-pin DIP

3

Table 12. Typical R96EFX Modem Interface Parts List

Component Designation	Component Value	Manufacturer's Part Number	Suggested Manufacturer
C11, C13	1000 pF ±5%, 50V	C124C102J5G5CA	Kemet
C7, C8, C9, C12, C14	0.1 µF ±20%, 50V	592CX7R104M050B	Sprague
C4, C6	0.33 µF ±20%, 50V		
C10	1.0 µF ±20%, 50V	SMC50T1R0M5X12	United Chem-con
C5	10.0 µF ±10%, 25V	ECEBEF100	Panasonic
C2	18 pF ±5%, 50V		
C3	39 pF ±5%, 50V		
R4	3 Ω ± 5%, 1/4W	43CX3R000J	Mepco Electra
R12	255 Ω ±1%, 1/4W		
R10, R16	1 KΩ±5%, 1/4W	5043CX1K00J	Mepco Electra
R2, R6	3 KΩ ±5%, 1/4W	5043CX3K00J	Mepco Electra
R18	10 KΩ ±1%, 1/4W		
R7	34.8 KΩ±1%, 1/4W		
R17	46.4 KΩ±1%, 1/4W	CRB1/4XF46K4	R–Ohm
R11	36.5 KΩ±1%, 1/4W	CRB1/4XF36K5	R-Ohm
R14, R15	86.6 KΩ±1%, 1/4W	CML 1/10 T86.6 KΩ ±1%	Dale Electronics
R5	2.7 MΩ± 5%, 1/4W	5043CX2M700J	Mepco Eletra
CR1	–5.1V 1%, regulator	1N4625D	Motorola
Y1	24.00014, MHz		
Y2	24.00014, MHz	TC0-706AB[1]	Toyocom

Note: 1. See Table 13 for specifications. The TC0-706AB is the only square wave generator recommended. A sine wave oscillator may alternatively be used (see Note 3 in Figure 9).

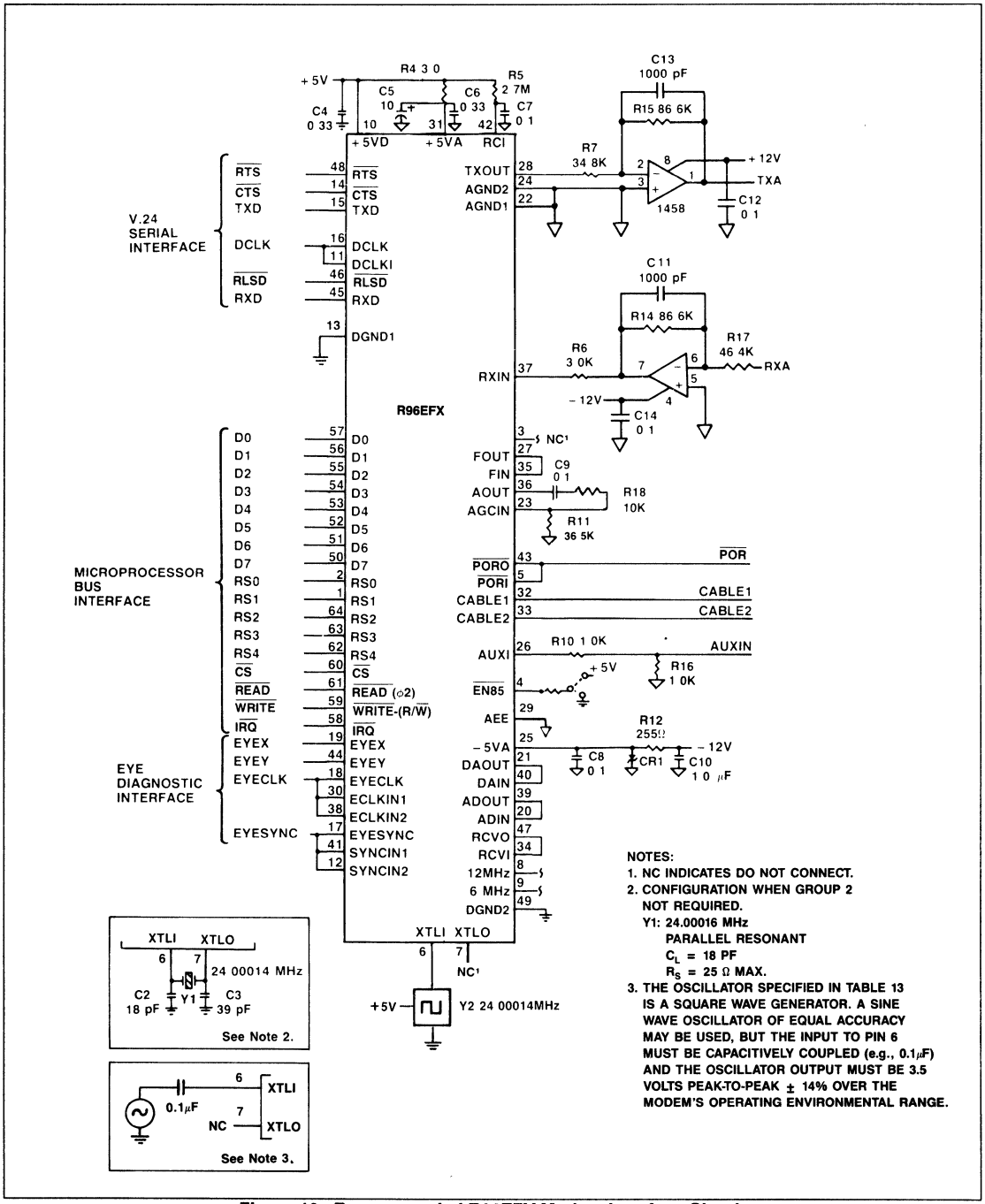


Figure 10. Recommended R96EFX Modem Interface Circuit

PC BOARD LAYOUT CONSIDERATIONS

1. The R96EFX and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board.
2. All power traces should be at least a 0.1 inch width.
3. If the power source is located more than approximately 5 inches from the modem, a decoupling capacitor of 10 μF or greater should be placed in parallel with C4 near pins 10 and 49.
4. All circuitry connected to pins 6 and 7 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the modem package. Pin 24 should tie directly, by a dedicated path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and to all analog ground points shown in Figure 10.
7. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 49 and to all digital ground points shown in Figure 10, plus the crystal-can ground.
8. The modem package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
9. As a general rule, digital signals should be routed on the component side of the PCB while the analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
10. Routing of the modem signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to Table 14 for the noise characteristics of each modem pin.

Table 14. Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	High	Low
1	6	3	23	26
2	7	4	27	28
12	8	5	32	
17	9	10	33	
18	11	13	35	
19	14	22	36	
20	15	24	37	
21	16	25		
30	45	29		
38	46	31		
39	48	34		
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Rockwell

R96MEB Modem Evaluation Board

INTRODUCTION

The Rockwell R96MEB (Modem Evaluation Board) aids the original equipment manufacturer (OEM) during the evaluation and design in phases of product development. The R96MEB supports the R96MFX and the R96EFX modems. The Modem Evaluation Board contains a socket (U1) for mounting the 64-pin quad in-line package (QUIP) of the modem, plus support circuitry to configure a complete data pump. For operation over the public switched telephone network (PSTN), an appropriate line termination, such as a data access arrangement (DAA), must be provided externally.

The R96MEB physical and electrical interface is compatible with the Rockwell R96FI/R96MD modem. For users of the R96FI or R96MD, this feature provides a rapid means of preparing to evaluate a 64-pin QUIP modem.

The R96FI version of the modem evaluation board is the R96MEB/F. Equipment previously developed for use with the R96FI can be converted for use with the R96MEB by changing only the software.

The R96MD version is the R96MEB/D. The R96MEB/D hardware is similar to the R96MD except for the addition and use of pins 35, 36, 37, 40, and 41. Pin 41 is used for ground and the other pins are used for the serial eye. The R96MD does not use these pins, therefore, the software and hardware must be changed.

FEATURES

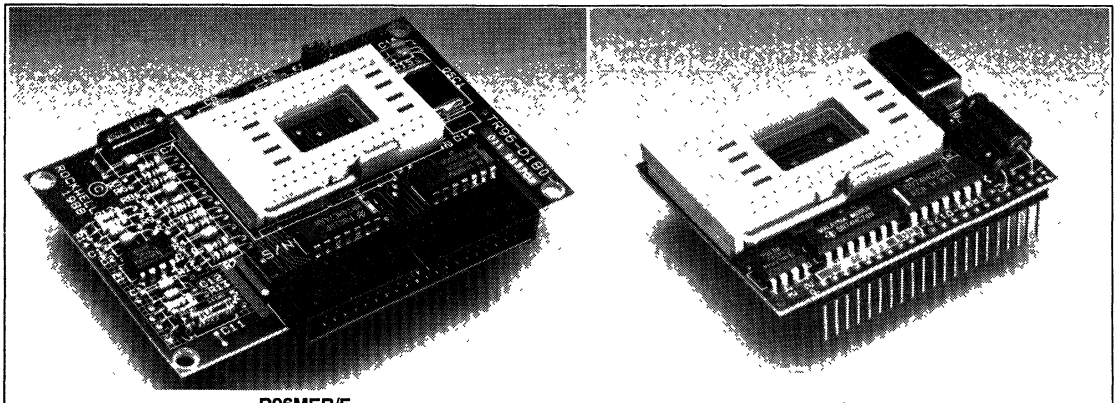
- Convenient evaluation method for the R96MFX and R96EFX
- Easily integrated into a prototype system
- Cost effective for low volume production applications (R96MEB/F only)
- Simple connection

  R96MEB/F: Standard 40-pin flat ribbon connector

  R96MEB/D: Direct connect dual-in-line pins
- Backward compatible with R96FI hardware (R96MEB/F)
- Low power consumption: 845 mW (typical)
- Small size:

  R96MEB/F: 100 mm x 65 mm (3.94 in. x 2.56 in.)

  R96MEB/D: 50.8 mm x 65.4 mm (2.00 in. x 2.575 in.)



R96MEB/F R96MEB/D

R96MEB Modem Evaluation Board

TECHNICAL SPECIFICATION

For a description of the R96MEB characteristics with a 64-pin QUIP modem installed in socket U1, refer to the R96MFX Modem Data Sheet (Order No. MD47) or the R96EFX Modem Data Sheet (Order No. MD49).

CIRCUIT DESCRIPTION

INTERFACE CIRCUITS

The circuitry and design rules used to create the R96MEB follow the recommended modem interface and PC board layout consideration published in the associated 64-pin QUIP modem data sheet. The circuit card can be used as a guide in host PC board design.

Refer to the R96MEB/F schematic diagram (Figure 1) during the following description. The modem being evaluated is inserted in the 64-pin QUIP socket (U1). The overhead connections between QUIP pins are completed by circuits on the evaluation board. The signals labeled NC (no connection) are not intended for use by the host equipment.

Modem signals that form the user interface on connector P1 (Table 1) are divided into six categories: Power, Microprocessor Interface, V.24 Interface, Cable Equalizer, Analog Signals, and Eye Pattern. The column titled "Type" refers to designations found in the digital and analog interface characteristics tables (Tables 2 and 3, respectively).

Power

Power signals include +5 volts, ±12 volts, ground and $\overline{\text{POR}}$. The +5 volt source provides power for digital circuits and can be driven by the host logic supply. The ±12 volt supplies provide power for analog circuits and should be free from switching transients normally associated with digital circuits. The ripple on all input voltages must be ≤0.1 volts peak-to-peak. If a switching supply is chosen, the user may select any frequency between 20 kHz and 150 kHz as long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

The common reference point for all signals, both digital and analog, is modem signal ground (pins 14 and 39 on R96MEB/F; pins 17, 18, and 41on the R96MEB/D). These pins provide the power supply return points for all voltages and should be used as reference for transmitter and receiver signals. To minimize noise problems, circuits that interface to the modem should maintain their ground references as close as possible to the same potential as these modem pins. Digital signals and analog signals should be referenced to modem signal ground via separate connections to prevent digital noise from appearing on analog signals due to a common ground impedance.

Table 1. R96MEB Connector Interface Signals

Name	I/O Type	MEB/F Pin No.	MEB/D Pin No.	Description
Power				
Ground	GND	14, 39	17, 18, 41	Power Supply Return
+ 5 volts	PWR	3, 4	33, 34	+5 volt supply
+12 volts	PWR	26	21	+12 volt supply
–12 volts	PWR	37	19	–12 volt Supply
$\overline{\text{POR}}$	IA/OD	36	39	Power-On Reset
Microprocessor Interface				
D7	IA/OB	7	9	Data Bus Line 7
D6	IA/OB	5	8	Data Bus Line 6
D5	IA/OB	9	2	Data Bus Line 5
D4	IA/OB	31	3	Data Bus Line 4
D3	IA/OB	15	4	Data Bus Line 3
D2	IA/OB	28	5	Data Bus Line 2
D1	IA/OB	23	6	Data Bus Line 1
D0	IA/OB	29	7	Data Bus Line 0
RS3	IA	30	13	Register Select 3
RS2	IA	8	14	Register Select 2
RS1	IA	27	15	Register Select 1
$\overline{\text{RS0}}$	IA	10	16	Register Select 0
$\overline{\text{CS0}}$	IA	6	11	Chip Select 0 (Registers 0-F)
$\overline{\text{CS1}}$	IA	18	38	Chip Select 1 (Registers 10-1F)
$\overline{\text{READ-}\phi 2}$	IA	1	10	Read Enable
$\overline{\text{WRITE-R/W}}$	IA	2	12	Write Enable
$\overline{\text{IRQ}}$	OC	32	1	Interrupt Request
V.24 Interface				
DCLK	OA	13	30	Data Clock
$\overline{\text{RTS}}$	IA	19	32	Request-to-Send
$\overline{\text{CTS}}$	OA	17	28	Clear-to-Send
TXD	IA	20	27	Transmitter Data
RXD	OA	21	26	Receiver Data
$\overline{\text{RLSD}}$	OA	16	29	Received Line Signal Detector
Cable Equalizer				
CABS1	IB	33	24	Cable Select 1
CABS2	IB	34	25	Cable Select 2
Analog Signals				
TXA	AA	38	23	Transmitter Analog Output
RXA	AB	40	22	Receiver Analog Input
AUXIN	AC	35	20	Auxiliary Analog Input
Eye Pattern Signals				
$\overline{\text{EYECLK}}$	OA	11	36	Eye Pattern Clock (230.4 kHz)
EYESYNC	OA	12	37	Eye Pattern Sync (9600 Hz)
EYEX	OA	24	35	Eye Pattern X Data
EYEY	OA	25	40	Eye Pattern Y Data

In order to reduce the effect of noise coupled through direct current (DC) power lines, decoupling capacitors are recommended on all power inputs. Each supply input should be decoupled to modem signal ground by a parallel set of capacitors. A large value capacitor of 10 microfarads or greater should be paralleled by a low inductance, small value capacitor of 0.1 microfarads.

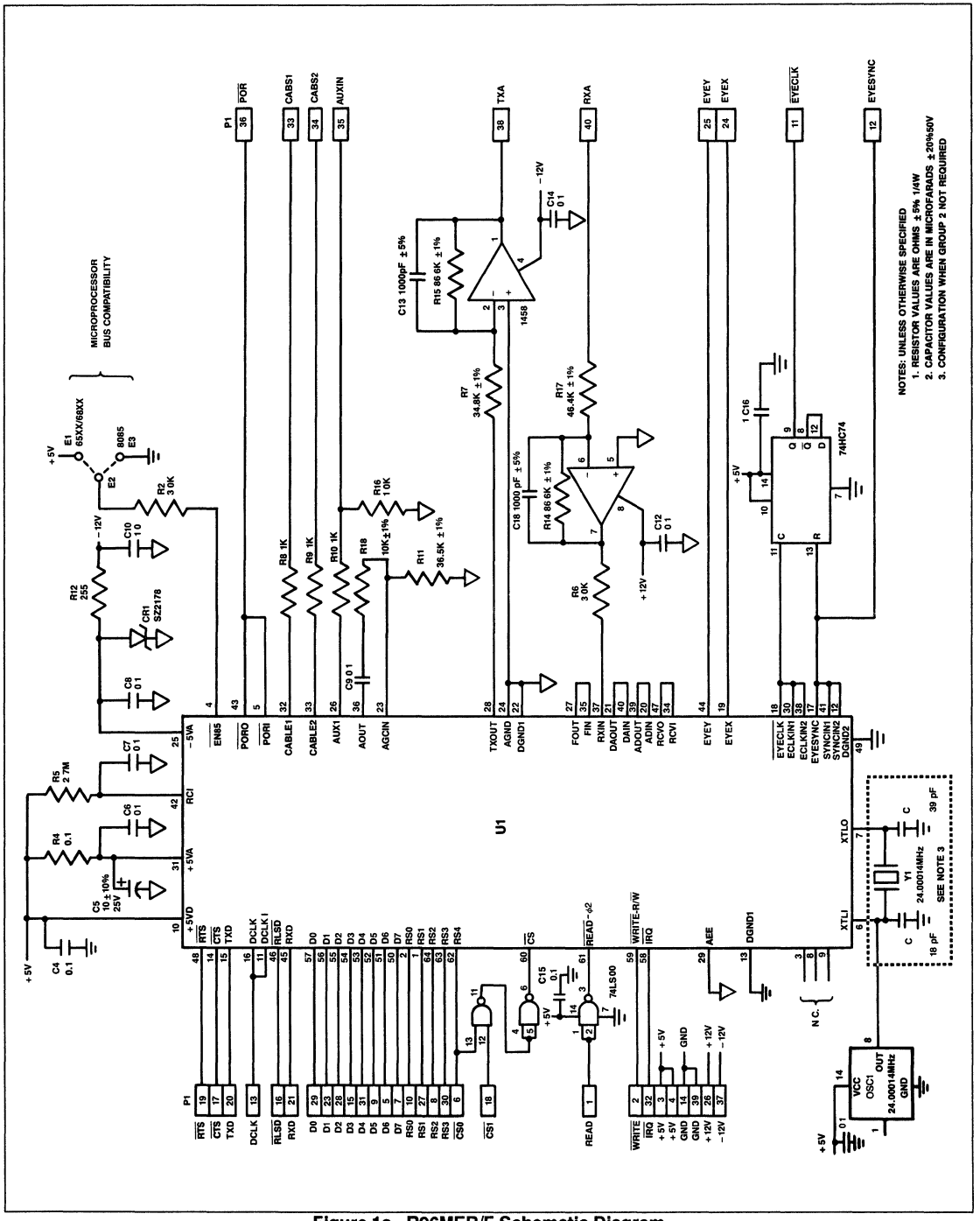


Figure 1a. R96MEB/F Schematic Diagram

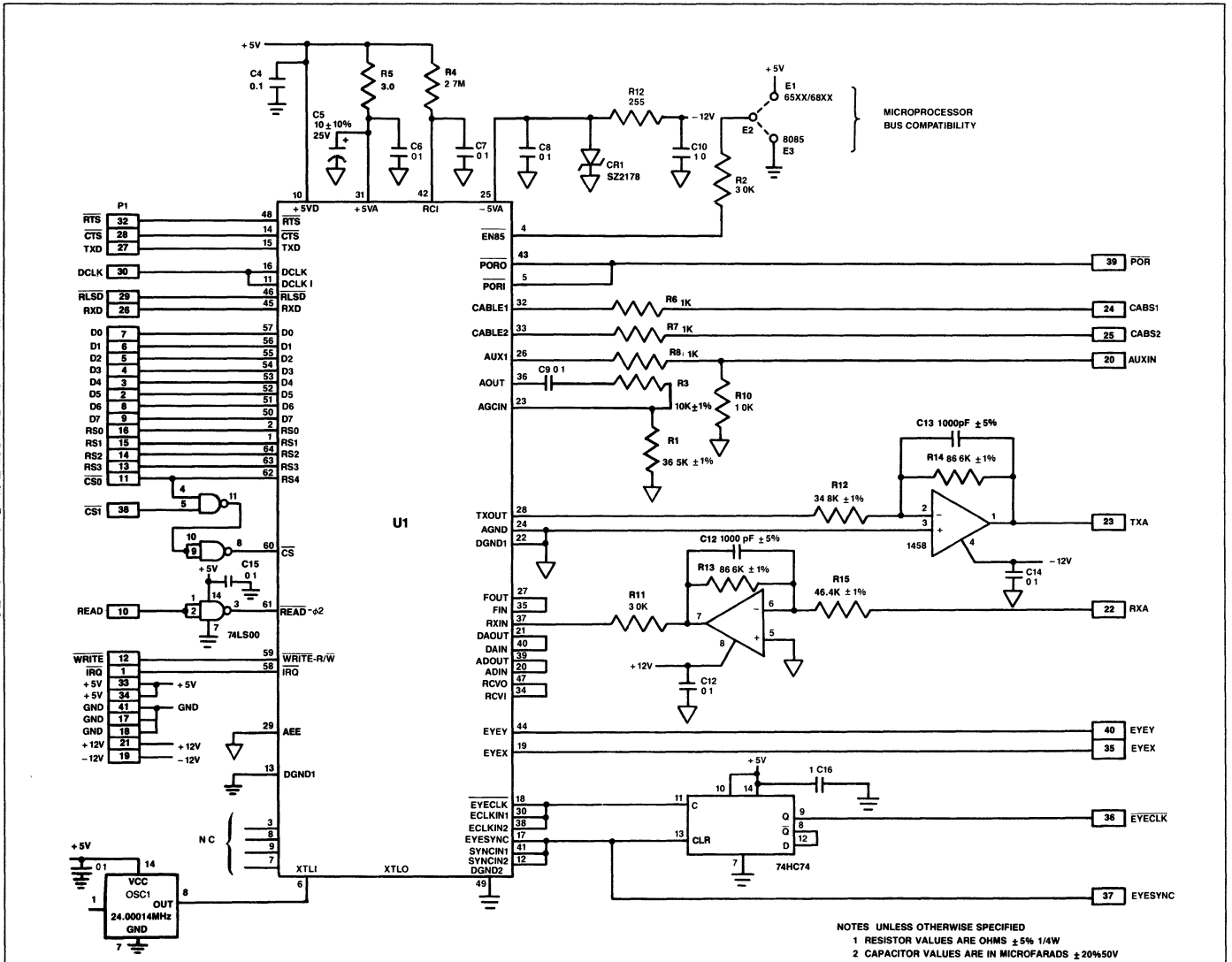


Figure 1b. R96MEB/D Schematic Diagram

Table 2. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	OA	OB	OC	OD
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.				
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.				
V_{OH}	Output Voltage, High	V			3.5 Min.[1]	3.5 Min.[1]		2.4 Min.[1]
V_{OL}	Output Voltage, Low	V			0.4 Max.[2]	0.4 Max.[3]	0.4 Max.[2]	0.4 Max.[2]
I_{IN}	Input Current, Leakage	µA	±2.5 Max.					
I_{OH}	Output Current, High	mA			–0.1 Max.	– 0.1 Max.		40 Min.
I_{OL}	Output Current, Low	mA			1.6 Max.	0.8 Max.	1.6 Max.	0.4 Max.
I_L	Output Current, Leakage	µA			±10 Max.	±10 Max.		
C_L	Capacitive Load	pF	5	20				
C_D	Capacitive Drive	pF			100	100	100	

Notes
1. I Load =–100 mA
2. I Load = 1.6 mA
3. I Load = 0.8 mA

Table 3. Analog Interface Characteristics

Name	Type	Characteristic
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 46.4K ohms ±1%.
AUXIN	AC	The auxillary analog input allows access to the transmitter for the purpose of interfacing with user-provided equipment. Because this is a sampled data input, any signal above half the sample rate (4800 Hz) will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is –0.4 dB ±1 dB.

Because the modem uses switched capacitor filters, the noise floor can be degraded as the result of high frequency noise aliased into the passband by beating with the switched capacitor clock. For this reason, use of linear power supplies, rather than switching power supplies, is recommended where low level reception (i.e., around –40 dBm) is anticipated. If switching power supplies are used, extra care must be taken to keep switching noise out of the modem.

The following techniques have proven helpful in designing systems using switching supplies. By following these procedures, satisfactory performance over the full dynamic range should be realized even when switching power supplies must be used.

1. In addition to the decoupling capacitors on all modem power inputs, wrap the power supply output leads around a toroidal core to increase series inductance. This technique blocks the conducted high frequency noise from the switching supply.
2. Insert a ground plane between the modem and the power supply. This technique reduces radiated EMI pickup by modem circuits.
3. Shield analog signals in coaxial wire. Signals TXA, RXA, and AUXIN should be shielded. Signal AUXIN should be tied to ground if not used.

When the modem is initially energized, the Power-On Reset ($\overline{POR}$) signal causes the modem to assume a valid operational state. The modem drives $\overline{POR}$ to ground during the beginning of the POR sequence. Approximately 10 milliseconds after the low-to-high transition of $\overline{POR}$, the modem is ready for normal use. The POR sequence is reinitialized anytime the +5 volt supply drops below +3.0 volts for more than 30 milliseconds, or an external device drives $\overline{POR}$ low for at least 3 microseconds.

Microprocessor Interface

Seventeen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS0}$, $\overline{CS1}$, $\overline{READ}$-ϕ2, and $\overline{WRITE}$-R/$\overline{W}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. The microprocessor interface timing waveforms are shown in Figure 2 and the microprocessor interface timing requirements are listed in Table 4. External logic gates can be jumpered to be compatible with a variety of microprocessor buses (i.e., 6500, 6800, or 8085).

Table 4. Microprocessor Interface Timing

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$ Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	–	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the data sheet for each 64-pin QUIP modem.

V.24 Interface

Six hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels. These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

If the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins except $\overline{RTS}$ may remain unterminated. $\overline{RTS}$ should be pulled high with a 3KΩ resistor between $\overline{RTS}$ and +5V.

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the PSTN, by means of a data access arrangement (DAA). In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable, the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. The low (0) and high (1) states of signals CABS1 and CABS2 that are necessary to select each of the cable equalizer options are defined in Table 5.

Table 5. Cable Equalizer Selection

CABS2	CABS1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three connector pins are devoted to analog audio signals: TXA, RXA, and AUXIN. The TXA (transmitter analog) line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier. In order to match this output to a standard telephone load of 600 ohms, a series resistor is required. A value of 604 ohms ±1% is recommended.

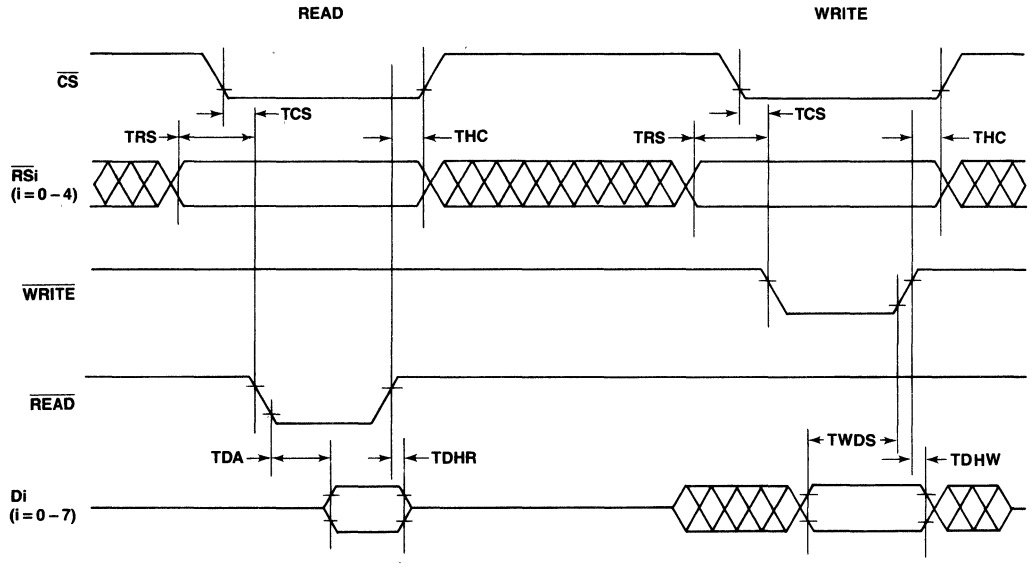
The RXA (receiver analog) line is an input to the receiver from an audio transformer or data access arrangement. The input impedance is 46.4K ohms ±1%. The RXA input must be shunted by an external resistor in order to match a 600 ohms source. The value of 604 ohms ±1% recommended for the transmitter resistor is also suitable for the receiver resistor.

The last analog connection is the input AUXIN. This line provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit. Any signal above half the sample rate (i.e., 4800 Hz) on the AUXIN line will be aliased back into the passband.

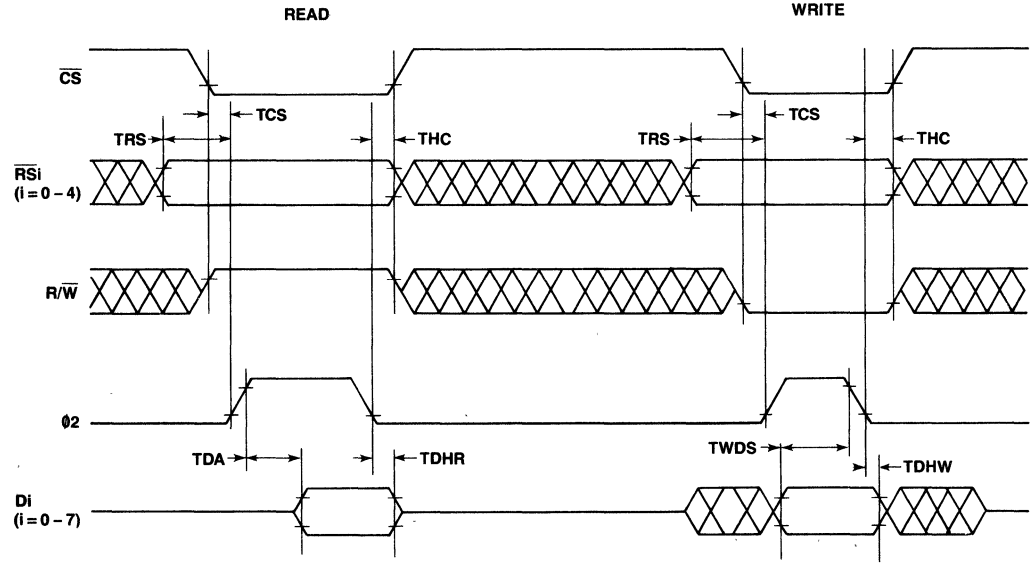
MEB SUPPORT CIRCUITS

The modem evaluation board with a 64-pin QUIP modem installed forms a complete data pump ready for interfacing to a host microprocessor (Figure 3). The host electronics must provide data and timing on the microprocessor interface pins to allow normal modem configuration and option selection plus status monitoring. Additional circuitry is recommended to allow generation of an eye pattern for diagnostic purposes (Figures 6 and 7). A commercially available modem test set (e.g., Phoenix 5000) can be connected directly to the V.24 serial interface (using TTL levels) or can be buffered with DS1488 and DS1489 type drivers and receivers for operation with standard RS-232 levels.

Schematic diagrams are provided for the RS-232 buffer circuit (Figure 4) and the microprocessor bus interface with eye pattern output (Figure 5). Note that the data clock signal must drive both the transmitter clock and the receiver clock and is therefore buffered to reduce the load. Also note that an SN74121 is used to shorten the write pulse in order to meet data hold time requirements for the NE5018 devices. The 100 ohm resistors in series with modem signals are required only when driving several feet of cable where excessive ringing may require damping. The address decode logic places the modem registers between locations 9000 and 901F hexadecimal. The eye pattern digital-to-analog converters (DACs) are at locations 9071 and 9072.



a. 8085 Bus Compatible



b. 6500 Bus Compatible

Figure 2. R96MFX/R96EFX Microprocessor Interface Waveforms

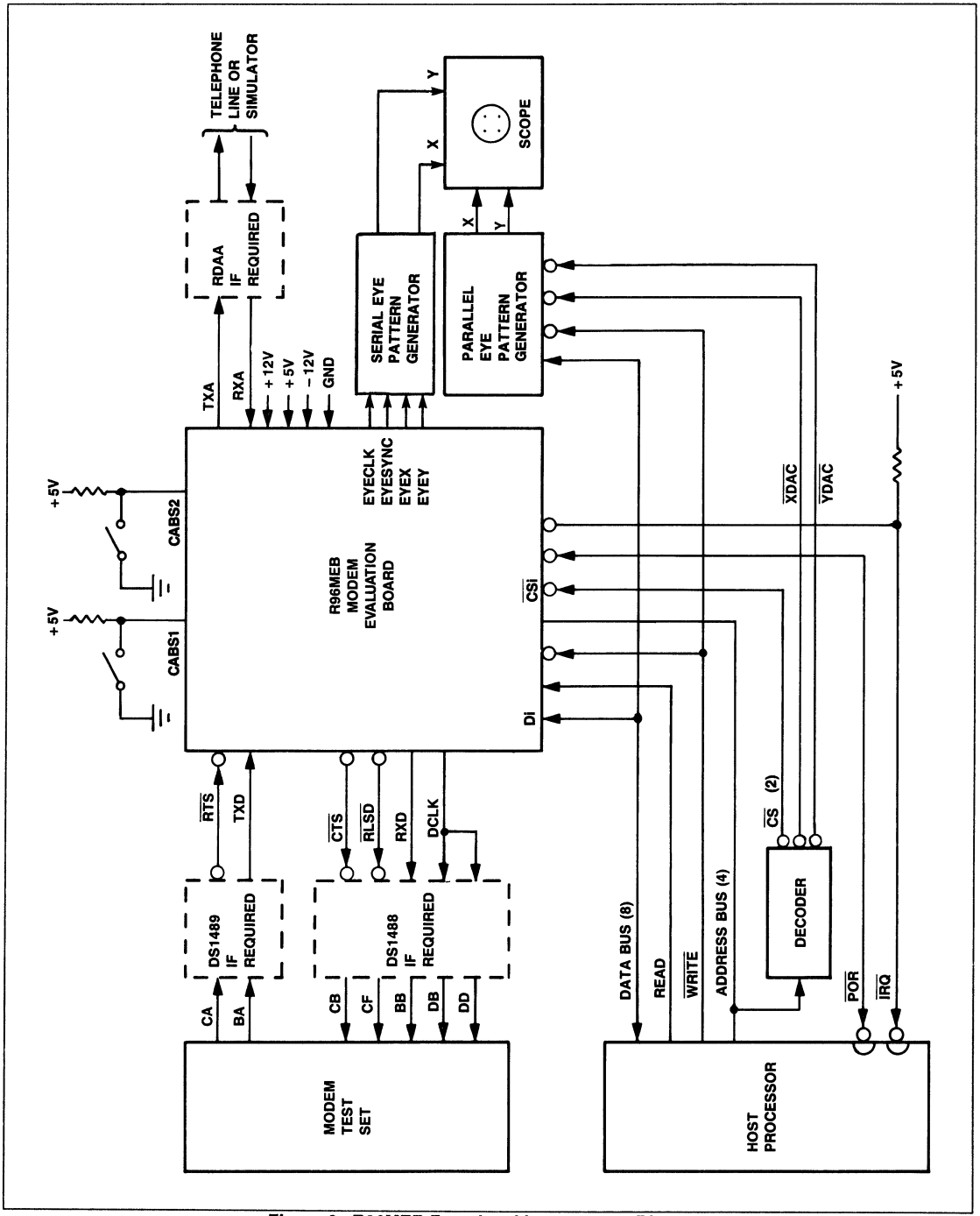


Figure 3. R96MEB Functional Interconnect Diagram

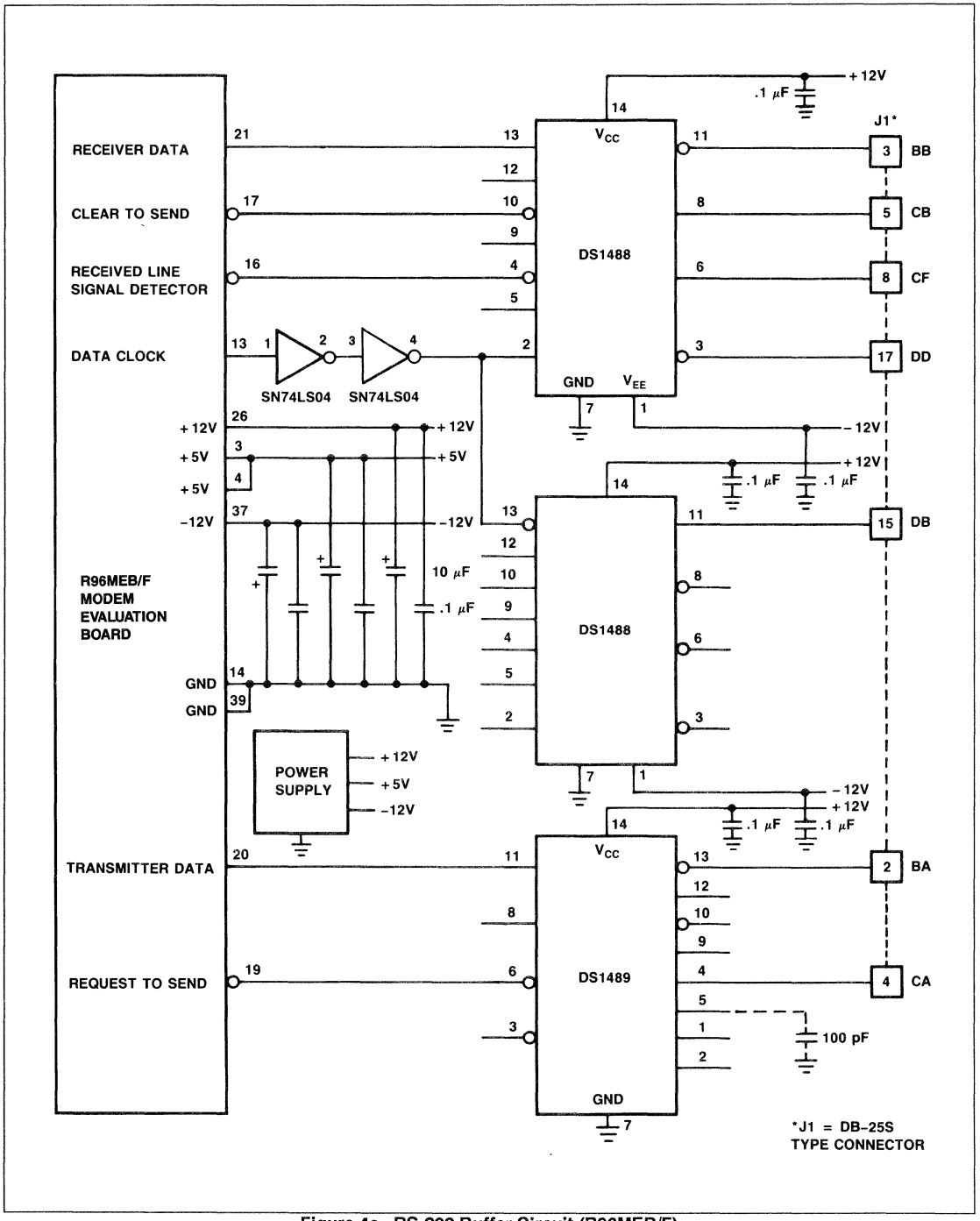


Figure 4a. RS-232 Buffer Circuit (R96MEB/F)

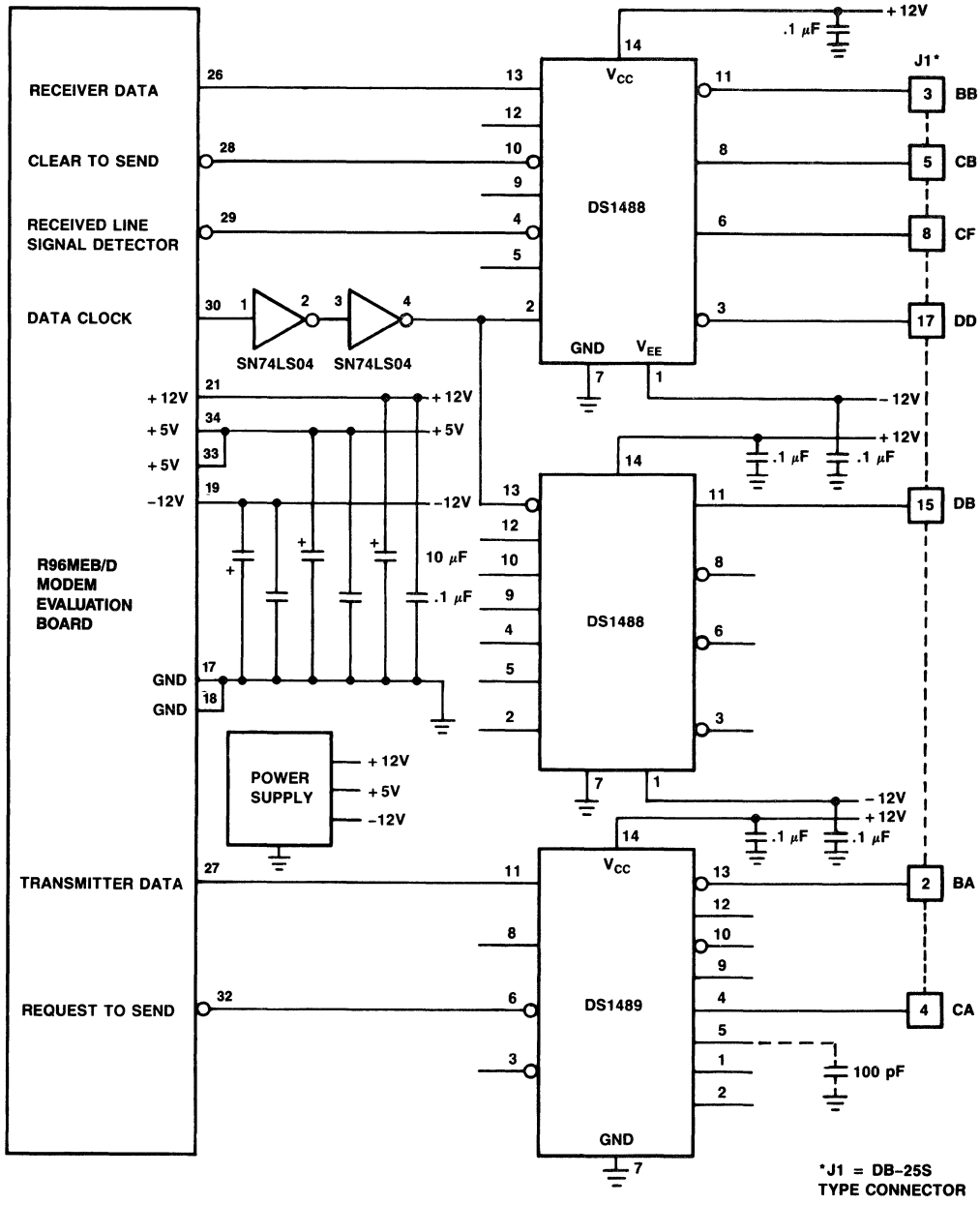


Figure 4b. RS-232 Buffer Circuit (R96MEB/D)

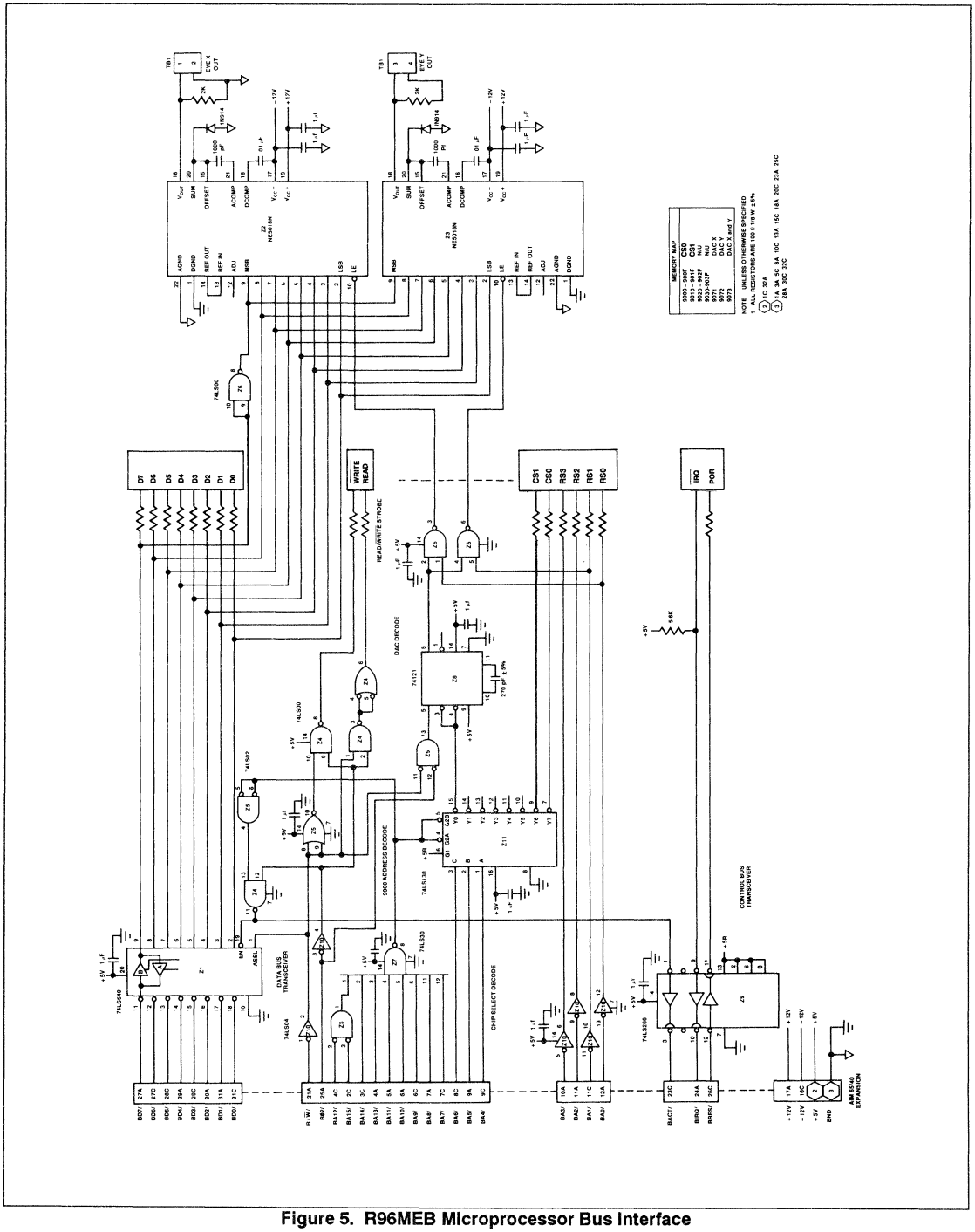


Figure 5. R96MEB Microprocessor Bus Interface

MODEM EVALUATION

EYE PATTERN

The eye pattern is an oscilloscope display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances, as well as defects in the modulation/demodulation process.

In quadrature amplitude modulation (QAM), two multilevel amplitude modulated (AM) carriers are transmitted simultaneously. Interference between these two modulated carriers is minimized by using carriers of identical frequency with a constant 90 degree relative phase angle. After demodulation, the multilevel baseband signals can be displayed on an oscilloscope with the set of levels received on one carrier displayed on the X axis and the set of levels received on one carrier displayed on the Y axis. Since these signals consist of discrete levels sent at high data rates, the resulting oscilloscope pattern appears to be a fixed set of points.

Figures 6a through 6d illustrate four examples of an eye pattern. Figure 6a shows the location of four ideal points corresponding to a signal structure using 0 and + 1 for the three amplitude levels. One such signal structure is CCITT Recommendation V.27 at 2400 bits per second. The dashed lines superimposed on the eye pattern represent decision boundaries used by the receiver in deciding which ideal point corresponds to the actual received point. Although the transmitter sends ideal points, line impairments cause the received points to be misaligned.

Figure 6b shows the effect of random noise. The received points cluster around the ideal location, but are randomly offset from the ideal point by the noise causing undesired signal modulation. The random offsets are a result of the random nature of the noise. If the line impairment is not random, but is periodic or is a function of the received signal itself (e.g., harmonic distortion), then the distribution of points around the ideal location is not random.

Figure 6c illustrates the tangential smearing resulting from phase jitter and Figure 6d shows the effect of amplitude distortion (either gain jitter or harmonic distortion). The magnitude of the spreading is directly proportional to the severity of the impairment, and represents the quality of the signal or the likelihood of errors in the received data.

Consult Figure 5 for an example of eye pattern generation using the microprocessor bus interface and Figure 7 for the generation of an eye pattern using the serial diagnostic interface.

BIT ERROR RATE

Bit Error Rate (BER) is a measure of the steady-state transfer of data on the communication channel. It is the ratio of the number of received bits in error to the number of transmitted bits. This number increases with decreasing signal-to-noise ratio (SNR). The type of line disturbance and the modem configuration also affect the BER.

The BER Performance Test Set-up (Figure 8) illustrates a method of measuring BER in accordance with CCITT Recommendation V.56. The band-limited noise level should be adjusted by the noise attenuator to give the desired signal to noise ratio for the selected received signal level. The modem transmitter is then caused to send a 511-bit pseudo random test pattern. The signal attenuator is set for a received signal level of –20 dBm to simulate leased line operation or –30 dBm to simulate switched network operation. In leased line testing, the line simulator should be 3002-C1 or 3002-C2 conditioned.

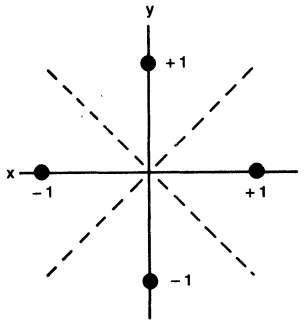
Once the receiver has trained (as indicated by a stable eye pattern) the BER test can begin. A large enough number of bits should be sent to cause at least 10 bit errors to be recorded. BER is calculated by dividing the number of bits in error by the number of bits sent.

The impairment source can be adjusted to provide phase-jitter or frequency offset, etc. The BER tests can be repeated in the presence of these line impairments to determine the amount by which performance has degraded. All BER tests should be conducted under steady-state conditions; i.e., after the adaptive equalizer has stabilized.

Transient response can be measured by using very short polling messages and comparing the number of attempts to send a message with the number of error free messages received for a specific signal-to-noise ratio and line condition. This type of testing is called block-error-rate (BLER) and can be performed using the same test set-up as bit-error-rate.

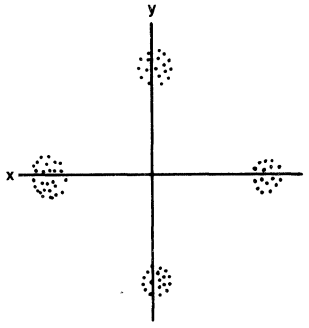
Data throughput for a specific application is determined by a combination of bit-error-rate and block-error-rate. Depending on system architecture, line conditions, error control method used, etc., an optimum message length can be chosen to maximized throughput. As messages become shorter, block-error-rate becomes the limiting factor. As messages become longer, bit-error-rate becomes the limiting factor.

a) IDEAL EYE PATTERN



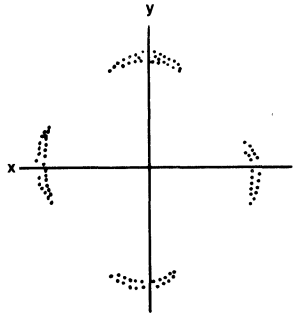
- DASHED LINES REPRESENT DECISION BOUNDARIES

b) WHITE NOISE



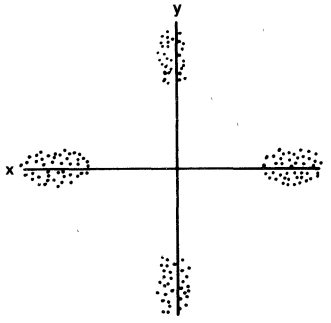
- SMEARING AROUND EACH IDEAL LOCATION

c) PHASE JITTER



- CONTINUOUSLY PERIODIC PHASE SMEARING
- LITTLE OR NO AMPLITUDE SMEARING

d) HARMONIC DISTORTION



- NON-PERIODIC AMPLITUDE SMEARING
- LITTLE PHASE EFFECT
- GAIN-JITTER (AM) EFFECT IS SIMILAR AND IS PERIODIC

*DEGREE OF THE SPREADING OF THE EYE PATTERN IS PROPORTIONAL TO THE SEVERITY OF THE LINE DISTURBANCE

Figure 6. Four-Point Eye Patterns

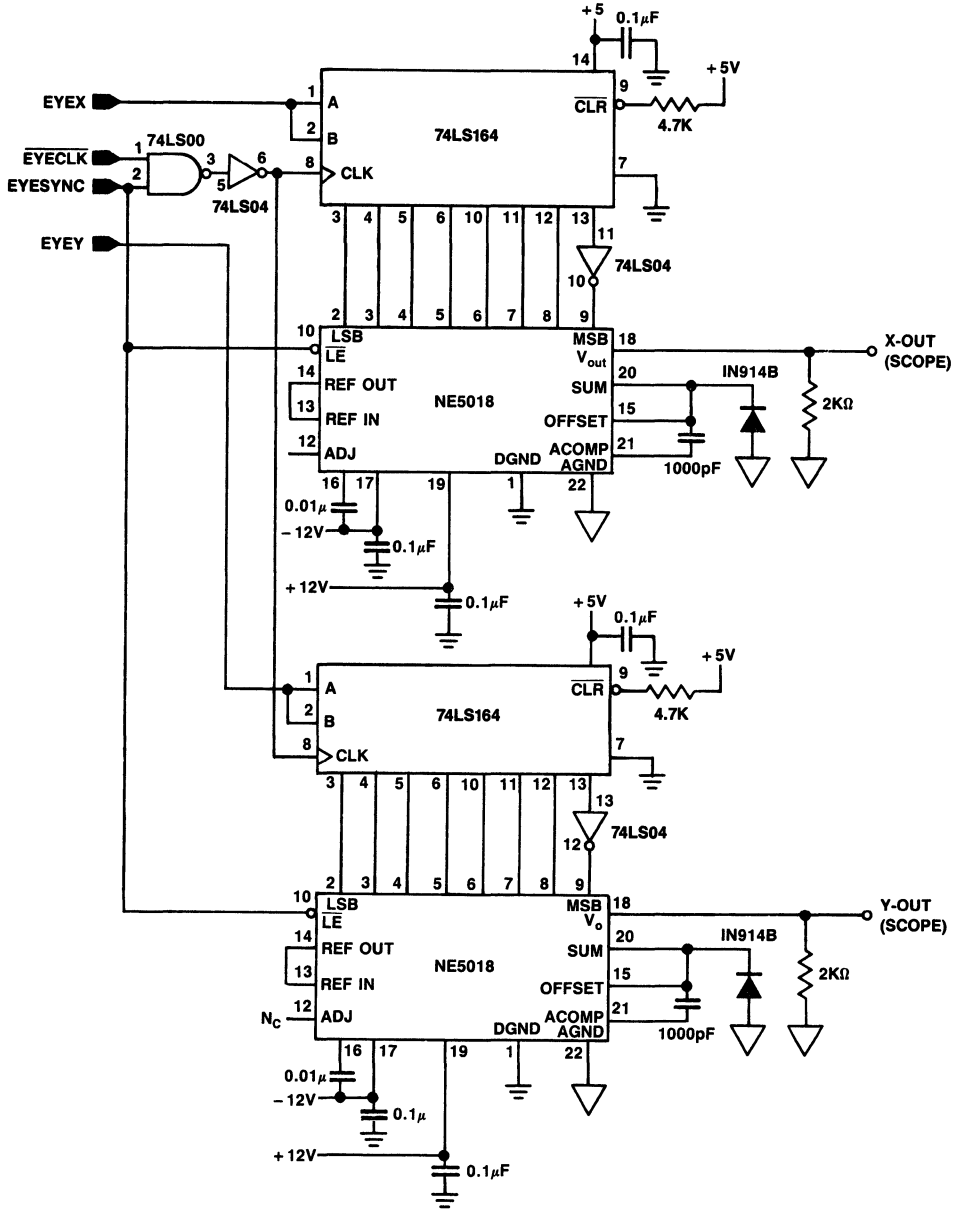


Figure 7. Serial Eye Pattern Generation Schematic

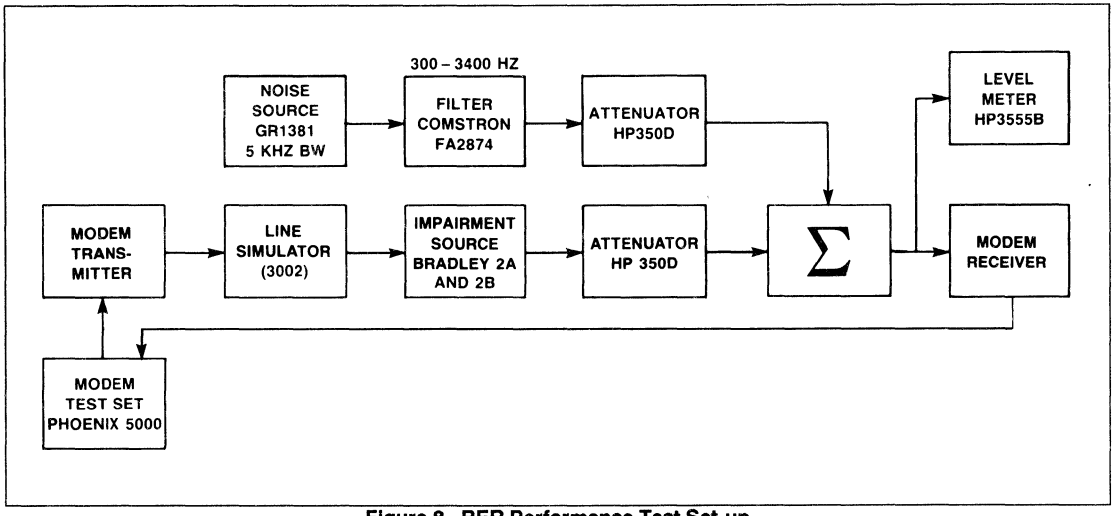


Figure 8. BER Performance Test Set-up

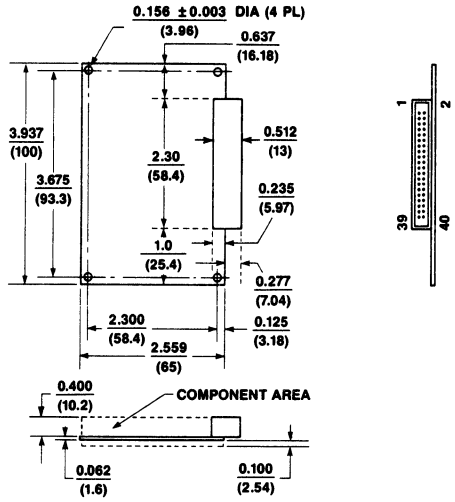
GENERAL SPECIFICATIONS

Voltage*	Tolerance	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
+ 5 VDC	± 5%	85 mA	100 mA
+ 12 VDC	± 5%	5 mA	10 mA
– 12 VDC	± 5%	30 mA	50 mA

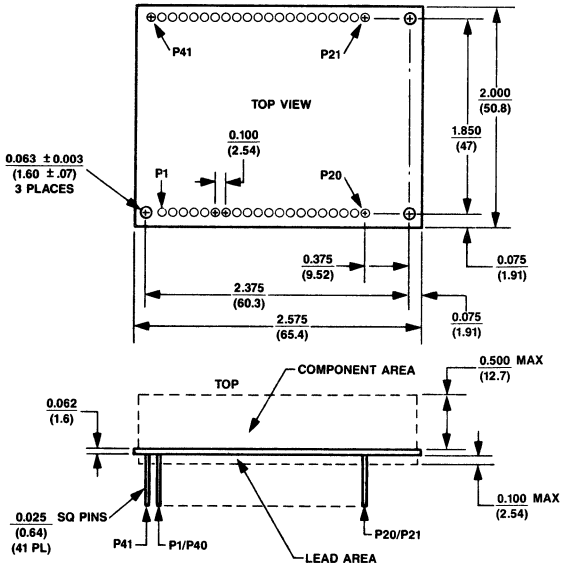
* Input voltage ripple ≤ 0.1 volts peak-to-peak.

Parameter	Specification
Temperature	
Operating	0° C to + 60° C (32° F to 140° F).
Storage	– 40° C to + 80° C (–40° F to 176° F). (Stored in heat sealed antistatic bag and shipping container.)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35° C, whichever is less.

Parameter	Specification
R96MEB/F	
Board Structure:	Single PC board with single right angle header with 40 pins. Hirose HIF3F-40PA-2.54DS or equivalent mating connector.
Dimensions:	
Length	2.56 in. (65 mm)
Width	3.94 in. (100 mm)
Height	0.40 in. (10.2 mm)
Weight (max.)	2.6 oz. (73 g)
Lead Extrusion (max.)	0.100 in. (2.54 mm)
R96MEB/D	
Board Structure:	Single PC board with a row of 20 pins and a row of 20 pins in a dual-in-line pin configuration.
Dimensions:	
Length	2.575 in. (65.4 mm)
Width	2.00 in. (50.8 mm)
Weight (max.)	2.6 oz. (73 g)
Pins:	
Length	0.535 in. (13.6 mm) gold
Thickness	0.025 in. (0.64 mm) square



a. R96MEB/F



b. R96MEB/D

R96MEB Dimensions

Rockwell

R96PCJ
9600 bps PC Communication Modem

INTRODUCTION

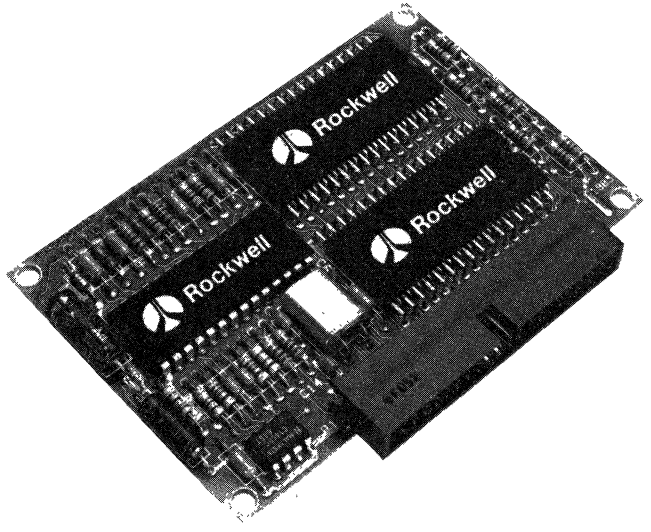
The Rockwell R96PCJ is a synchronous 9600 bits per second (bps) modem designed for operation over the public switched telephone network through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, V.21, T.4 and the binary signaling capabilities of T.30. The R96PCJ can operate at speeds of 9600, 7200, 4800, 2400 and 300 bps, and includes the V.27 ter short training sequence option. Employing advanced signal processing techniques, the R96PCJ can transmit and receive data even under extremely poor line conditions.

User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, and serial/parallel host interface simplify system design and allow installation in a small enclosure.

FEATURES

- Ultimate User Compatibility:
  — CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4
- Half-Duplex (2-Wire)
- Programmable Tone Generation and Detection
- Dynamic Range: −47 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
  — Automatic Adaptive
  — Compromise Cable (Selectable)
  — Compromise Link Amplitude (Selectable)
- DTE Interface:
  — Microprocessor Bus
  — CCITT V.24 (RS-232-C Compatible)
- Small Size: 100 mm × 65 mm (3.94 in. × 2.56 in.)
- Low Power Consumption: 2W (typical)
- Transmit Output Level: +5 dBm ±1 dB
- TTL and CMOS Compatible



R96PCJ Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T.30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01 Hz)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100

Carrier Frequencies

Function	Frequency (Hz ±0.01 Hz)
V 27 ter Carrier	1800
V.29 Carrier	1700

TONE GENERATION

Under control of the host processor, the R96PCJ can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory of the R96PCJ.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate· Data Rate	2400 baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate· Date Rate.	1600 baud 4800 bps
Signaling Rate. Data Rate.	1200 baud 2400 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 ter

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

EQUALIZERS

The R96PCJ provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Amplitude Equalizer — The selectable compromise amplitude equalizer may be inserted into the transmit and/or receive paths under control of the transmit amplitude equalizer enable and the receive amplitude equalizer enable bits in the interface memory. The amplitude select bit controls which of two amplitude equalizers is selected.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If neither the link amplitude nor cable equalizer is enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96PCJ incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96PCJ can adapt to received frequency error of up to ±10 Hz with less than a 0 2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R96PCJ satisfies all specified performance requirements for received line signal levels from 0 dBm to – 43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the R96PCJ provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is fixed at +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R96PCJ provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

A total of 14 selectable turn-on sequences can be generated as defined in the following table:

Turn-On Sequences

No.	V.29	V.27 ter	$\overline{CTS}$ [2] Response Time (milliseconds)	Comments
1	9600 bps		253	
2	7200 bps		253	
3	4800 bps		253	
4		4800 bps long	708	
5		2400 bps long	943	
6		4800 bps short	50	
7		2400 bps short	67	
8	9600 bps		438	Preceded by [1]
9	7200 bps		438	Echo Protector
10	4800 bps		438	Tone for lines
11		4800 bps long	913	using echo
12		2400 bps long	1148	suppressors
13		4800 bps short	255	
14		2400 bps short	272	

1. Turn-on sequences 8 through 14 are used on lines with protection against talker echo.
2. V.21 (300 bps FSK) $\overline{RTS}$-$\overline{CTS}$ delay is 14 ms or less.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{RTS}$ goes false.

CLAMPING

The following clamps are provided with the R96PCJ:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector (RLSD).* $\overline{RLSD}$ is clamped off (squelched) during the time when $\overline{RTS}$ is on.
3. *Extended Squelch.* Optionally, $\overline{RLSD}$ remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{CTS}$ turns on in 14 ms or less.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

For either V.27 ter or V.29, $\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 15 ±10 ms. The $\overline{RLSD}$ on-to-off response time for V.27 is 10 ±5 ms and for V.29 is 30 ±9 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1. Greater than −43 dBm ($\overline{RLSD}$ on)
   Less than −48 dBm ($\overline{RLSD}$ off)
2. Greater than −47 dBm ($\overline{RLSD}$ on)
   Less than −52 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R96PCJ is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

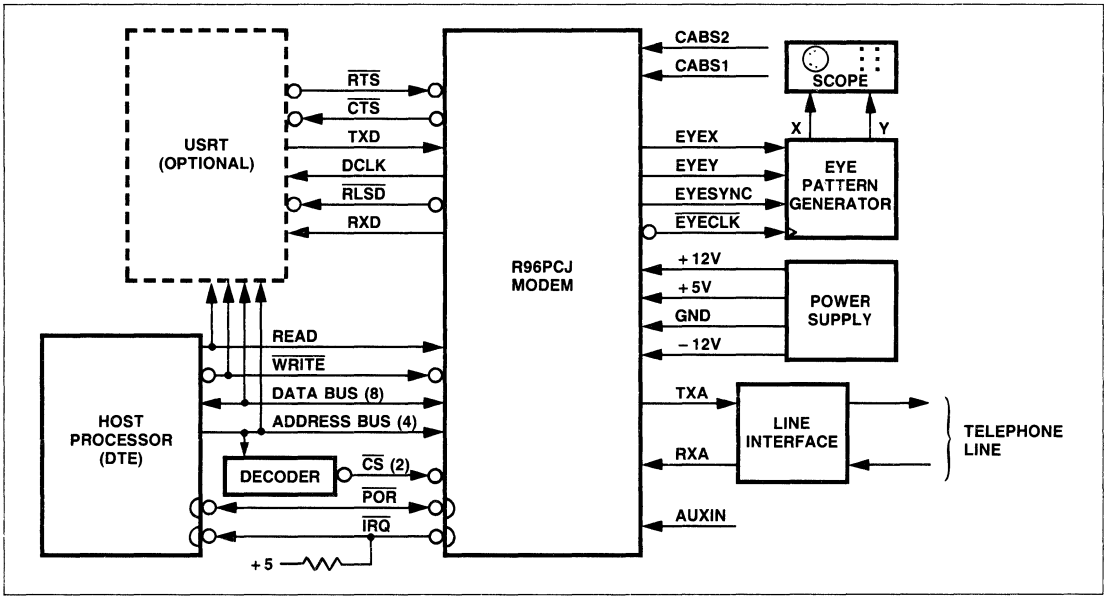
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the R96PCJ Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R96PCJ has the capability of transferring channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R96PCJ is configured by the host processor via the microprocessor bus.



R96PCJ Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 40-pin ribbon connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96PCJ Hardware Circuits table; the table column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96PCJ Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground	GND	14, 39	Power Supply Return
+5 volts	PWR	3, 4	+5 Vdc Supply
+12 volts	PWR	26	+12 Vdc Supply
−12 volts	PWR	37	−12 Vdc Supply
$\overline{POR}$	I/OA	36	Power-on-reset

R96PCJ Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	7	Data Bus (8 Bits)
D6	I/OA	5	
D5	I/OA	9	
D4	I/OA	31	
D3	I/OA	15	
D2	I/OA	28	
D1	I/OA	23	
D0	I/OA	29	
RS3	IA	30	Register Select (4 Bits) Select Reg 0 − F
RS2	IA	8	
RS1	IA	27	
RS0	IA	10	
$\overline{CS0}$	IA	6	Chip Select Sample Rate Device
$\overline{CS1}$	IA	18	Chip Select Baud Rate Device
$\overline{READ}$	IA	1	Read Enable
$\overline{WRITE}$	IA	2	Write Enable
$\overline{IRQ}$	OB	32	Interrupt Request
C. V.24 INTERFACE:			
$\overline{DCLK}$	OC	13	Data Clock
$\overline{RTS}$	IB	19	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	20	Transmitter Data
$\overline{RXD}$	OC	21	Receiver Data
$\overline{RLSD}$	OC	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IC	33	Cable Select 1
CABS2	IC	34	Cable Select 2
Unused inputs tied to +5V or ground require individual 10K Ω series resistors			

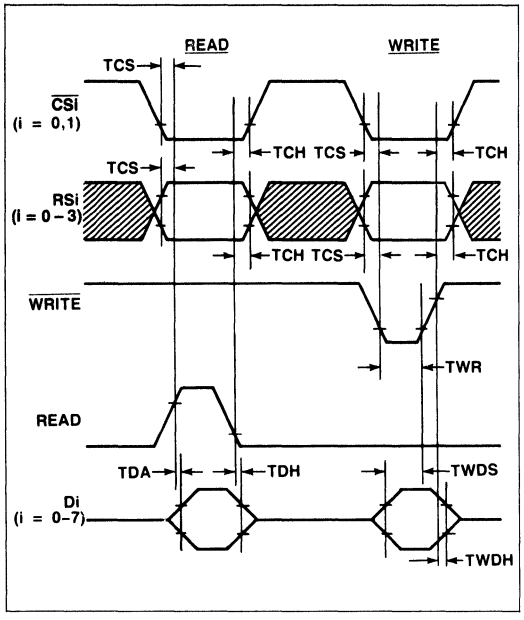
R96PCJ Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXA	AA	38	Transmitter Analog Output
RXA	AB	40	Receiver Analog Input
AUXIN	AC	35	Auxiliary Analog Input
F. DIAGNOSTIC:			
EYEX	OC	24	Eye Pattern Data — X Axis
$\overline{\text{EYEY}}$	OC	25	Eye Pattern Data — Y Axis
$\overline{\text{EYECLK}}$	OA	11	Eye Pattern Clock
EYESYNC	OA	12	Eye Pattern Synchronizing Signal

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words obtained from registers 1:3 and 1:1 (see RAM Data Access) are shifted out most significant bit first clocked by the rising edge of the $\overline{\text{EYECLK}}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

Microprocessor Timing



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{\text{CSi}}$, RSi setup time prior to Read or $\overline{\text{Write}}$	TCS	30	—	ns
Data Access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
$\overline{\text{CSi}}$, RSi hold time after Read or $\overline{\text{Write}}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Cable Equalizer Selection

Cable Equalizer Selection

CABS 2	CABS 1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Digital Interface Characteristics

The digital interface characteristics are listed in the table on the following page.

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −0.4 dB ±1 dB.

SOFTWARE CIRCUITS

The R96PCJ comprises two signal processor chips. Each chip contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data from or write data to these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem sample rate (9600 bps). Registers in chip 1 update at the selected baud rate.

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2 0 min.	2.0 min.	2.0 min				2.0 min	5.25 max. 2 0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max				0 8 max.	0 8 max
V_{OH}	Output Voltage, High	V				2 4 min [1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0 4 max.[2]	0.4 max [2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2 5 max						±12 5 max [4]	
I_{OH}	Output Current, High	mA				−0.1 max				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5 25 Vdc
5. I load = 0.36 mA

3

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Status/Control Bits

The operation of the R96PCJ is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'X' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by an '—' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R96PCJ provides the user with access to much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

Two RAM access registers are provided in the interface memory to allow user access to various RAM locations within the modem. The access code stored in 0:F selects the source of data for the RAM data registers in chip 0 (0:0 through 0:3). Similarly, the access code stored in 1:F selects the source of data for registers 1:0 through 1:3. Reading is performed by storing the desired access code in register 0:F (or 1:F), performing a read of 0:0 (or 1:0) to reset 0:E:0 (or 1:E:0), then waiting for 0:E:0 (or 1:E:0) to return to a one. The data may now be read from 0:3 through 0:0 (or 1:3–1:0).

Data in registers 1:3 and 1:1 are presented serially on EYEX and EYEY, respectively.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

R96PCJ RAM Access Codes

Node	Function	Access	Chip	Reg. No.
1	Received Signal Samples	40	0	2,3
2	Demodulator Output	42	0	0,1,2,3
3	Low Pass Filter Output	54	0	0,1,2,3
4	Average Energy	5C	0	2,3
5	AGC Gain Word	01	0	2,3
6	Equalizer Input	40	1	0,1,2,3
7	Equalizer Tap Coefficients	01-20	1	0,1,2,3
8	Unrotated Equalizer Output	61	1	0,1,2,3
9	Rotated Equalizer Output (Received Point—Eye Pattern)	22	1	0,1,2,3
10	Decision Points (Ideal)	62	1	0,1,2,3
11	Error Vector	63	1	0,1,2,3
12	Rotation Angle	00	1	0,1
13	Frequency Correction	A8	1	2,3
14	EQM	AB	1	,2,3

R96PCJ Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	X	X	EPT	SQEXT	T2	LRTH
4	CONFIGURATION							
3	RAM DATA XSM; FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register \ Bit	7	6	5	4	3	2	1	0

X = User available (not used by modem).
— = Reserved (modem use only).

R96PCJ Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	—	—	—	—	IE1	—	MDA1
D	X	TLE	RLE	J3L	X	X	X	—
C	X	X	X	X	X	X	X	X
B	FR3	FR2	FR1	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	—
4	—	—	—	—	—	$\overline{P2DET}$	—	—
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register \ Bit	7	6	5	4	3	2	1	0

X = User available (not used by modem).
— = Reserved (modem use only).

R96PCJ Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1 7 0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$
(None)	Configuration	0 4 0–7	The host processor configures the R96PCJ by writing a control code into the configuration register in the interface memory space (See SETUP) ***Configuration Control Codes*** Control codes for the four available R96PCJ configurations are **Configuration** — **Configuration Code (HEX)** V 29 9600 — 14 V 29 7200 — 12 V 29 4800 — 11 V 27 4800 Long — 0A V 27 2400 Long — 09 V 27 4800 Short — 4A V 27 2400 Short — 49 Tone Transmit — 80 FSK — 20 ***Configuration Definitions*** Definitions for the four available R96PCJ configurations are 1 *V 29.* When any of the V29 configurations has been selected, the modem operates as specified in CCITT Recommendation V29 2 *V 27* When any of the V27 configurations has been selected, the modem operates as specified in CCITT Recommendation V27 ter 3 *FSK.* The modem operates as a CCITT T30 compatible 300 bps FSK modem having characteristics of the CCITT V21 channel 2 modulation system 4 *Tone Transmit* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user Two registers in the host interface memory space contain the frequency code The most significant bits are specified in the FREQM register (0 3) The least significant bits are specified in the FREQL register (0 2) The least significant bit represents 0 146486 Hz ±0 01% The frequency generated is f = 0 146486 (256 FREQM + FREQL) Hz ±0 01%
EPT	Echo Protector Tone	0 5 3	If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence This option is available in both the V27 and V29 configurations, although it is not specified in the CCITT V29 Recommendation
$\overline{\text{FED}}$	Fast Energy Detector	1 5 6	The zero state of $\overline{\text{FED}}$ indicates energy is present above the receiver threshold in the passband
(None)	FREQL/FREQM	0 2 0-7, 0 3 0-7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below *FREQM Register (0 3)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0 2)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0}

3

R96PCJ Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
			The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below **Frequency (Hz) / FREQM / FREQL** 462 / 0C / 52 1100 / 1D / 55 1650 / 2C / 00 1850 / 31 / 55 2100 / 38 / 00
FR1 – FR3	Frequency 1,2,3	1:B·5,6,7	The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for FR1, FR2 and FR3 are: **Bit / Frequency (Hz)** FR1 / 2100 FR2 / 1100 FR3 / 462
IA1	Interrupt Active (One)	1 E:7	IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volts
IA0	Interrupt Active (Zero)	0:E·7	IA0 is a one when Chip 0 is driving $\overline{IRQ}$ to zero volts
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one
IE1	Interrupt Enable (One)	1·E.2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one
J3L	Japanese 3 Link	1.D.4	The one state of J3L selects this standard for link amplitude equalizer. The zero state of J3L selects U S survey long
LRTH	Lower Receive Threshold	0:5·0	The one state of LRTH lowers the receiver turn-on threshold from −43 dBm to −47 dBm. (See SETUP)
MDA0	Modem Data Available (Zero)	0:E:0	MDA0 goes to one when the modem reads or writes register 0:0 MDA0 goes to zero when the host processor reads or writes register 0:0. MDA0 is used for parallel mode as well as for diagnostic data retrieval.
MDA1	Modem Data Available (One)	1:E:0	MDA1 goes to one when the modem writes register 1·0 MDA1 goes to zero when the host processor reads register 1:0
PDM	Parallel Data Mode	0·F 7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.
$\overline{PNDET}$	Period 'N' Detector	1·7 6	The zero state of $\overline{PNDET}$ indicates a PN sequence has been detected. $\overline{PNDET}$ sets to a one at the end of the PN sequence.
$\overline{P2DET}$	Period '2' Detector	1:4:2	The zero state of $\overline{P2DET}$ indicates a P2 sequence has been detected $\overline{P2DET}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1 F 0–7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device)
(None)	RAM Access S	0·F 0–6	Contains the RAM access code used in reading RAM locations in Chip 0 (sample rate device)
(None)	RAM Data XBL	1:2·0–7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XBM	1.3 0–7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).

R96PCJ Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Data XSL	0 2 0–7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device)
(None)	RAM Data XSM	0 3 0–7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device)
(None)	RAM Data YBL	1 0 0–7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device) (See DA1)
(None)	RAM Data YBM	1 1·0–7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device)
(None)	RAM Data YSL	0 0 0–7	Least significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device) Shared by parallel data mode for presenting channel data to the host microprocessor bus (See Transceiver Data and DA0)
(None)	RAM Data YSM	0 1 0–7	Most significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device)
RLE	Receiver Link Equalizer	1 D 5	The one state of RLE enables the link amplitude equalizer in the receiver
RTS	Request-to-Send	0 5 7	The one state of RTS begins a transmit sequence The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed RTS parallels the operation of the hardware $\overline{\text{RTS}}$ control input These inputs are "ORed" by the modem
SETUP	Setup	0 E 3	The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for equalizer (0 5 1) and threshold (0·5:0) SETUP returns to zero when acted on by the modem The time required for the SETUP bit to cause a change depends on the current state of the modem The following table lists worst case delays.
SQEXT	Squelch Extend	0 5·2	The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.
TDIS	Training Disable	0 5 6	If TDIS is a one in the receive state, the modem is prevented from entering the training phase If TDIS is a one prior to $\overline{\text{RTS}}$ going on, the generation of a training sequence is prevented at the start of transmission
TLE	Transmitter Link Equalizer	1 D 6	The one state of TLE enables the link amplitude equalizer in the transmitter
(None)	Transceiver Data	0 0 0–7	In receive parallel data mode, the modem presents eight bits of channel data in register 0·0 for reading by the host microprocessor After the eight bits have been accumulated in register 0·C they are transferred to 0 0 and bit 0 E 0 goes to a one. When the host reads 0.0, bit 0:E:0 resets to a zero The first bit of received data is not necessarily located in bit 0.0:0. The host must frame the received data by searching for message sync characters Bit 0 E·0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations In transmit parallel data mode, the host stores data at location 0 0 This action causes bit 0 E 0 to reset to a 0 When the modem transfers the data from 0 0 to 0 2 bit 0·E 0 sets to a 1. The data is serially transmitted from register 0 2 least significant bit first Received data is shifted into register 0 C from MSB toward LSB
T2	T/2 Equalizer Select	0 5 1	If T2 is a one, an adaptive equalizer with two taps per baud is used If T2 is a zero, an adaptive equalizer with one tap per baud is used The number of taps remains the same for both cases. (See SETUP)

Current State	V.21	High Speed Receiver	High Speed Transmitter
DELAY	14 ms	2 BAUD	2 BAUD + TURNOFF Sequence + Training (if applicable) + SQUELCH (if applicable)

POWER-ON INITIALIZATION

When power is applied to the R96PCJ, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low-to-high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 ms, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.29/9600 bps, T/2 equalizer, serial mode, training enabled, echo protector tone on, no extended squelch, higher receive threshold, interrupts disabled, no link equalizer, and RAM access codes 00.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μs or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 ms after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V.29 type modem, the R96PCJ provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm as illustrated.

TYPICAL PHASE JITTER

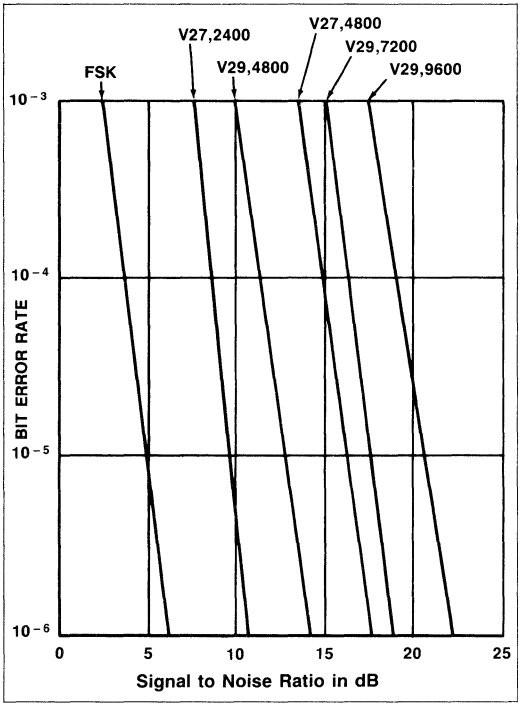
At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

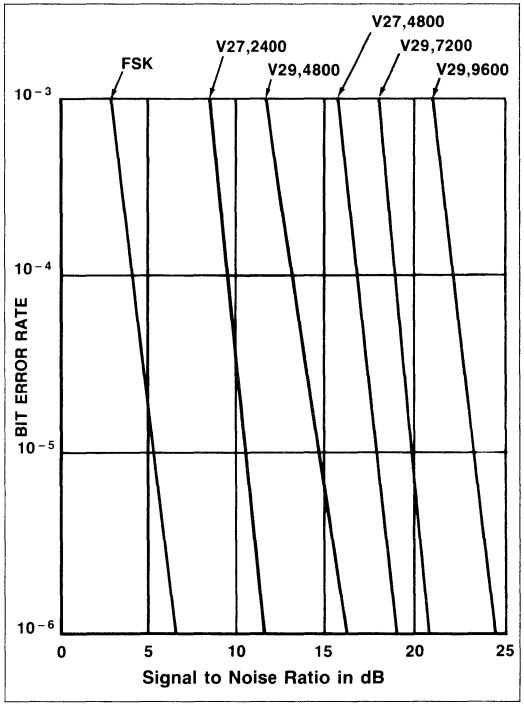
At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

An example of the BER performance capabilities is given in the following diagrams:

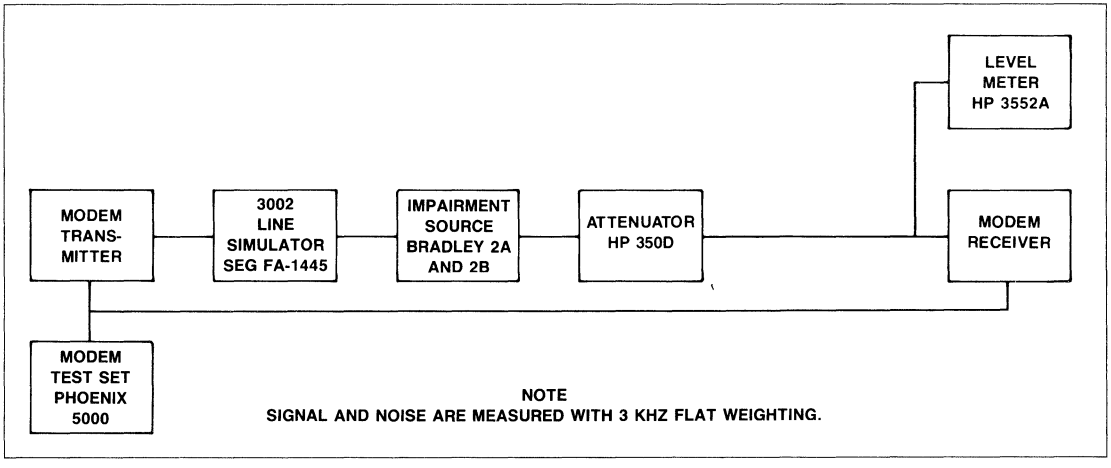


Typical Bit Error Rate
(Back to Back, T Equalizer, Level −20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer, Level −20 dBm)

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	400 mA	<500 mA
+12 Vdc	±5%	5 mA	<10 mA
−12 Vdc	±5%	30 mA	<50 mA

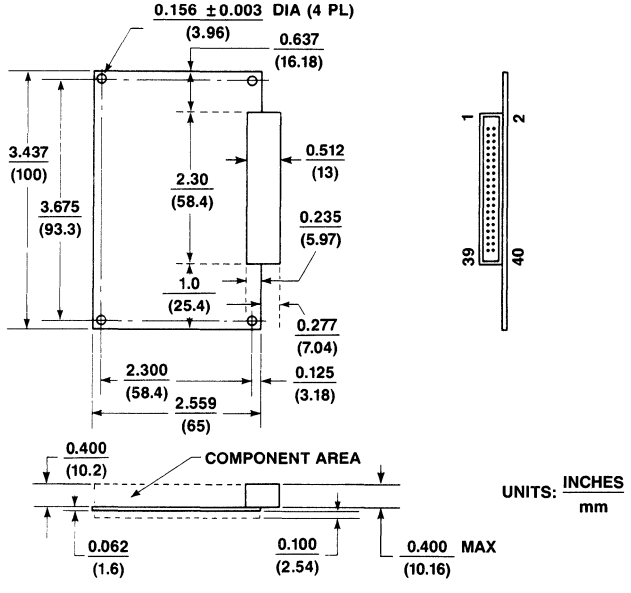
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins. Burndy FRS 40BS8P or equivalent mating connector
Dimensions	
Width	3.937 in. (100 mm)
Length	2 559 in (65 mm)
Height	0 40 in (10.2 mm)
Weight (max)	2.6 oz. (73 g)
Lead Extrusion (max)	0.100 in. (2.54 mm)



RIBBON CONNECTOR VERSION

R96PCJ Dimensions and Pin Locations

Rockwell

R96FI
9600 bps Facsimile Modem

INTRODUCTION

The Rockwell R96FI is a synchronous 9600 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

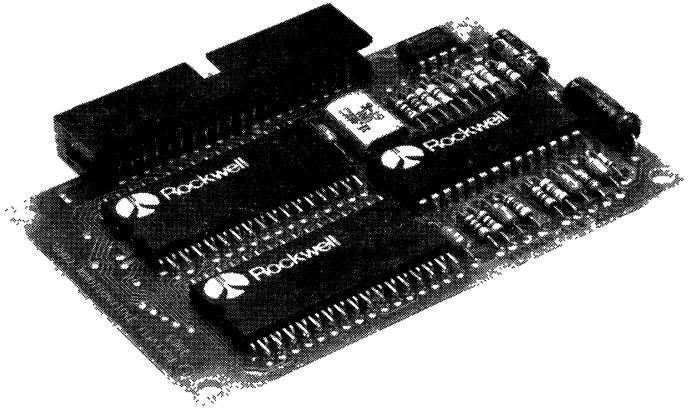
The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, T.30, T.4 and T.3. The R96FI can operate at speeds of 9600, 7200, 4800, 2400 and 300 bps. Employing advanced signal processing techniques, the R96FI can transmit and receive data even under extremely poor line conditions.

The R96FI is designed for use in Group 3 facsimile machines and is also compatible with Group 2 machines. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface, simplify system design.

The R96FI has fewer discrete components than the R96F and operates over a wider temperature range, i.e , up to 70°C. All other specifications in this data sheet apply to the R96F as well as the R96FI.

FEATURES

- Compatibility:
  — CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
- Group 3 and Group 2 Facsimile
- Half-Duplex (2-Wire)
- Tone Detection
- Programmable Tone Generation and Detection
- Dynamic Range: −47 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
  — Automatic Adaptive
  — Compromise Cable (Selectable)
  — Compromise Link Amplitude (Selectable)
- DTE Interface:
  — Microprocessor Bus
  — CCITT V.24 (RS-232-C Compatible)
- Small Size: 100 mm × 65 mm (3.94 in. × 2.56 in.)
- Low Power Consumption: 2W (Typical)
- Transmit Output Level: +5 dBm ±1 dB
- TTL and CMOS Compatible



R96FI Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T.30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01%)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group 2 Identification (C12)	1850
Group 2 Command (GC2)	2100
Group 2 Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462

Carrier Frequencies

Function	Frequency (Hz ±0.01%)
T 3 Carrier (Group 2)	2100
V 27 ter Carrier	1800
V 29 Carrier	1700

TONE GENERATION

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory of the modem.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate Data Rate	2400 baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate. Date Rate.	1600 baud 4800 bps
Signaling Rate Data Rate	1200 baud 2400 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29 At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 ter

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V 27 ter

EQUALIZERS

The modem provides the following equalization functions which can be used to improve performance when operating over poor lines

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0 4 mm diameter.

Link Amplitude Equalizer — The selectable compromise amplitude equalizer may be inserted into the transmit and/or receive paths under control of the transmit amplitude equalizer enable and the receive amplitude equalizer enable bits in the interface memory. The amplitude select bit controls which of two amplitude equalizers is selected.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer can be configured as either a T or a T/2 equalizer

TRANSMITTED DATA SPECTRUM

If neither the link amplitude nor cable equalizer is enabled, the transmitter spectrum is shaped by the following raised cosine filter functions·

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler This facility is in accordance with either V 27 ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The modem receiver circuit can adapt to received frequency error of up to ±10 Hz with less than a 0.2 dB degradation in BER performance Group 2 carrier recovery capture range is 2100 ±30 Hz. The Group 2 receiver operates properly when the carrier is varied by ±16 Hz at a 0.1 Hz per second rate.

RECEIVE LEVEL

The modem receiver circuit satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the modem provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%

TRANSMIT LEVEL

The transmitter output level is fixed at +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the modem provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (±0.01%). In Group 2, DCLK tracks an external 10368 Hz clock. If the external clock input (XCLK) is grounded, the Group 2 DCLK is 10372.7 Hz ±0.01%.
2. *Duty Cycle.* 50 ±1%

Transmit Data (TXD) must be stable during the 1 microsecond period immediately preceding and the 1 microsecond period immediately following the rising edge of DCLK.

TURN-ON SEQUENCE

A total of ten selectable turn-on sequences can be generated by the modem, as defined in the following table·

Turn-On Sequences

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V 29	253 ms	438 ms
V.27 4800 bps	708 ms	913 ms
V 27 2400 bps	943 ms	1148 ms
V 21 300 bps	≤14 ms	≤14 ms
Group 2	≤400 μs	≤400 μs

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{RTS}$ goes false. In Group 2 the transmitter turns off within 200 μs after $\overline{RTS}$ goes false.

CLAMPING

The following clamps are provided with the modem:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector (RLSD).* $\overline{RLSD}$ is clamped off (squelched) during the time when $\overline{RTS}$ is on
3. *Extended Squelch.* Optionally, $\overline{RLSD}$ remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{CTS}$ turns on in 14 ms or less. In Group 2 $\overline{CTS}$ turns on in 400 μs or less.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

For either V.27 ter or V.29, $\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 15 ±10 ms. The $\overline{RLSD}$ on-to-off response time for V.27 is 10 ±5 ms and for V.29 is 30 ±9 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1 Greater than −43 dBm ($\overline{RLSD}$ on)
  Less than −48 dBm ($\overline{RLSD}$ off)
2. Greater than −47 dBm ($\overline{RLSD}$ on)
  Less than −52 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The modem operates in either a serial or a parallel mode.

SERIAL MODE

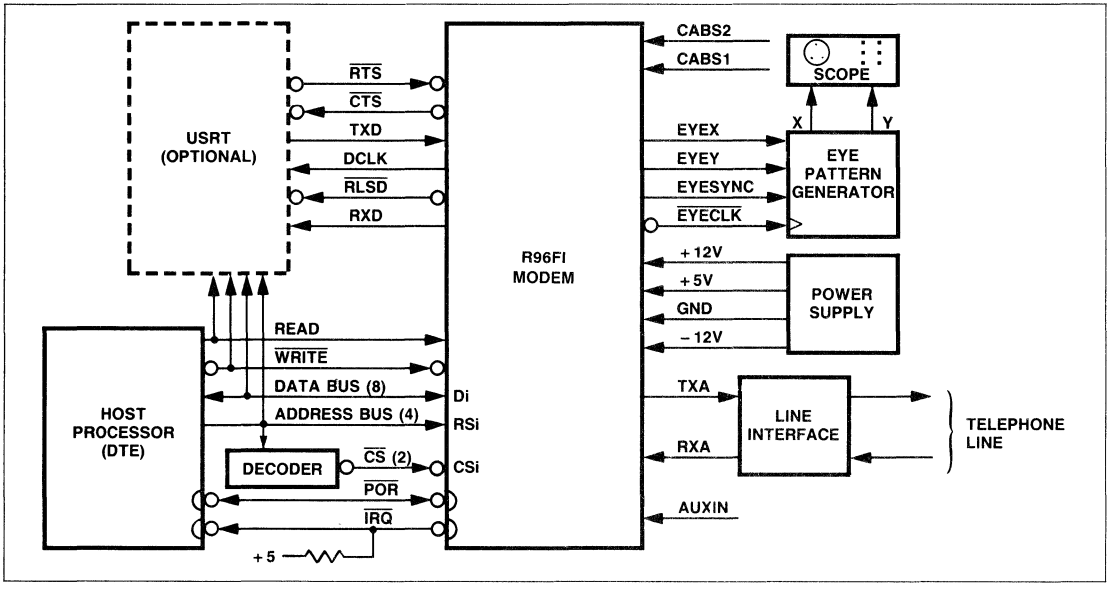
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Modem Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The modem can transfer channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the modem is configured by the host processor via the microprocessor bus.



Modem Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 40-pin ribbon connector or in a 41-pin dual in-line pin connector Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the Modem Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital or Analog Interface Characteristics.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0–RS3), data (D0–D7), control (CS, READ and WRITE) and interrupt (IRQ) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal The modem includes three such equalizers designed to compensate for cable distortion

Cable Equalizer Selection

CABS2	CABS1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs: TXA, RXA, and AUXIN.

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the PSTN. The output structure of TXA is a low impedance amplifier. In order to match this output to a standard telephone load of 600 ohms, a series resistor is required.

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may be back-to-back zener diodes across the transformer or a varistor across the transformer.

AUXIN provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit at a rate of 9600 samples-per-second. Any signal above 4800 Hz on the AUXIN line will be aliased back into the passband as noise. One application for AUXIN is to inject dual-tone multifrequency (DTMF) touch-tone signals for dialing, however, the source of these tones must be well filtered to eliminate components above 4800 Hz. The input impedance of AUXIN is 1K ohm. The gain from AUXIN to TXA is −0.4 dB ±1 dB.

Overhead

Except for the power-on-reset signal $\overline{POR}$, the overhead signals are dc power or ground points. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives the $\overline{POR}$ pin to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of the $\overline{POR}$ pin, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives the $\overline{POR}$ pin low for at least 3 μs. When an external low input is applied to the $\overline{POR}$ pin, the modem is ready for normal use approximately 10 ms after the low input is removed. The $\overline{POR}$ pin is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The POR sequence leaves the modem configures as follows:

- V.29/9600 bps
- T/2 equalizer
- Serial mode
- Training enabled
- Echo protector tone enabled
- No extended squelch
- Higher receive threshold
- Interrupts disabled
- No link equalizer
- RAM access codes 00

This configuration is suitable for performing high speed data transfer on the PSTN with the serial data port selected as the input and output point for data terminal equipment (DTE).

Modem Hardware Circuits

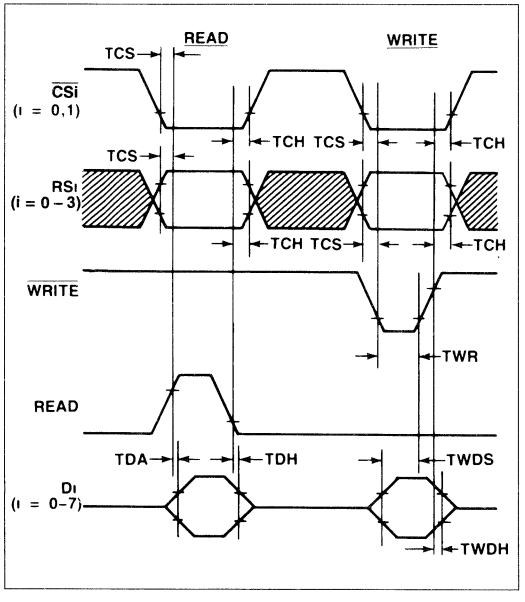
Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground	GND	14, 39	Power Supply Return
+5 volts	PWR	3, 4	+5 volt supply
+12 volts	PWR	26	+12 volt supply
−12 volts	PWR	37	−12 volt supply
$\overline{POR}$	I/OB	36	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	7	Data Bus (8 Bits)
D6	I/OA	5	
D5	I/OA	9	
D4	I/OA	31	
D3	I/OA	15	
D2	I/OA	28	
D1	I/OA	23	
D0	I/OA	29	
RS3	IA	30	Register Select (4 Bits) Select Reg 0−F
RS2	IA	8	
RS1	IA	27	
RS0	IA	10	
$\overline{CS0}$	IA	6	Chip Select Sample Rate Device
$\overline{CS1}$	IA	18	Chip Select Baud Rate Device
$\overline{READ}$	IA	1	Read Enable
$\overline{WRITE}$	IA	2	Write Enable
$\overline{IRQ}$	OB	32	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	13	Data Clock
XCLK	IB	22	External Clock for Group 2
$\overline{RTS}$	IB	19	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	20	Transmitter Data
RXD	OC	21	Receiver Data
$\overline{RLSD}$	OC	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IC	33	Cable Select 1
CABS2	IC	34	Cable Select 2

Modem Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXA	AA	38	Transmitter Analog Output
RXA	AB	40	Receiver Analog Input
AUXIN	AC	35	Auxiliary Analog Input
F. DIAGNOSTIC:			
EYEX	OC	24	Eye Pattern Data — X Axis
EYEY	OC	25	Eye Pattern Data — Y Axis
EYECLK	OA	11	Eye Pattern Clock
EYESYNC	OA	12	Eye Pattern Synchronizing Signal
Unused inputs tied to +5V or ground require individual 10K Ω series resistors			

Diagnostic

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the EYECLK output The EYESYNC output is provided for word synchronization The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
CSi, RSi setup time prior to Read or Write	TCS	30	—	ns
Data Access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
CSi, RSi hold time after Read or Write	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output In order to match to 600 ohms, an external 604 ohm series resistor is required
RXA	AB	The receiver input impedance is 60K ohms ±23%
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors The input impedance is 1K ohms, and the gain to transmitter output is −0 4 dB ±1 dB

SOFTWARE CIRCUITS

The modem includes two signal processor chips Each of these chips contains 16 registers to which an external (host) microprocessor has access Although these registers are within the modem, they may be addressed as part of the host processor's memory space The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem sample rate (9600 bps) Registers in chip 1 update at the selected baud rate.

When information in these registers is being discussed, the format Y.Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1

Status/Control Bits

Modem operation is affected by a number of software control inputs These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a '—' are reserved for modem use only and must not be changed by the host

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min	5.25 max 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

3

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

RAM Data Access

The user can access much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

Two RAM access registers are provided in the interface memory to allow user access to various RAM locations within the modem. The access code stored in 0:F selects the source of data for the RAM data registers in chip 0 (0:0 through 0:3). Similarly, the access code stored in 1:F selects the source of data for registers 1:0 through 1:3. Reading is performed by storing the desired access code in register 0:F (or 1:F), performing a read of 0:0 (or 1:0) to reset 0:E:0 (or 1:E:0), then waiting for 0:E:0 (or 1:E:0) to return to a one. The data may now be read from 0:3 through 0:0 (or 1:3–1:0).

Chip one also provides the capability to write data into RAM. When bit RAMW is set to a one, reading is suspended and a write cycle takes place once each time bit DA1 (1:E:0) is reset to zero.

Writing is performed by storing the desired access code in register 1:F, waiting for bit DA1 (1:E:0) to be a 1, setting bit RAMW (1:D:0) to a 1, then storing sixteen bits of data in registers 1:1 and 1:0. The eight bits in 1:1 are most significant. Writing to 1:0 resets bit 1:E:0 to a 0 and starts the write cycle, which ends by 1:E:0 returning to a 1. Bit RAMW (1:D:0) must remain set until the end of the cycle.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem. The access code stored in chip 1 (1:F) also selects the source of data for the serial outputs EYEX and EYEY. Diagnostic data is scaled as shown in the Diagnostic Data Scaling table.

RAM Access Codes

Node	Function	Access	Chip	Reg. No.
1	Received Signal Samples	40	0	2,3
2	Demodulator Output	42	0	0,1,2,3
3	Low Pass Filter Output	54	0	0,1,2,3
4	Average Power	5C	0	2,3
5	AGC Gain	01	0	2,3
6	Equalizer Input	40	1	0,1,2,3
7	Equalizer Tap Coefficients	01-20	1	0,1,2,3
8	Unrotated Equalizer Output	61	1	0,1,2,3
9	Rotated Equalizer Output (Received Point—Eye Pattern)	22	1	0,1,2,3
10	Decision Points (Ideal)	62	1	0,1,2,3
11	Error Vector	63	1	0,1,2,3
12	Rotation Angle	00	1	0,1
13	Frequency Correction	A8	1	2,3
14	Eye Quality Monitor (EQM)	AB	1	,2,3
15	G2 Baseband Signal	C8	1	2,3
16	G2 AGC Gain	AD	1	2,3
17	G2 AGC Slew Rate	AA	1	2,3
18	G2 PLL Frequency Correction	C2	1	2,3
19	G2 PLL Slew Rate	F0	1	,2,3
20	G2 Black/White Threshold	2A	1	0,1
21	G2 Phase Limit*	F2	1	2,3

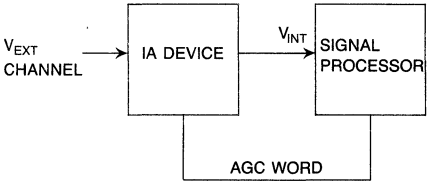
*Added in R5301-20

Diagnostic Data Scaling

Node 1

Parameter/Scaling

Received Signal Samples = A/D Sample Word (signed 16 bits, twos complement)



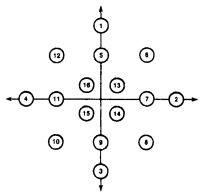
$$V_{INT} = \frac{(\text{A/D Sample Word})_{16}}{40_{16}} \times \frac{3}{256} \text{ Volts}$$

$$V_{EXT} = V_{INT} - LOG_{10}^{-1}\left[\frac{\text{AGC Gain (dB)}}{20}\right]$$

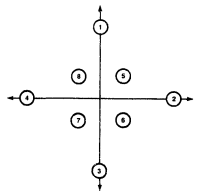
Nodes 2, 3, 6, 8, 9, 10

All Baseband Signal Nodes (32 bits, complex, twos complement)

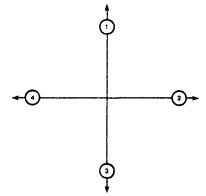
Point	Configuration			
	V.29/9600 x , y	**V.29/7200 x , y**	**V.29/4800 & V.27/2400 x , y**	**V.27/4800 x , y**
1	0000, 2800	0000, 2400	0000, 1C00	0000, 1C00
2	2800, 0000	2400, 0000	1C00, 0000	1400, 1400
3	0000, D800	0000, DC00	0000, E400	1C00, 0000
4	D800, 0000	DC00, 0000	E400, 0000	1400, EC00
5	0000, 1800	0C00, 0C00		0000, E400
6	1800, 1800	0C00, F400		EC00, EC00
7	1800, 0000	F400, F400		E400, 0000
8	1800, E800	F400, 0C00		EC00, 1400
9	0000, E800			
10	E800, E800			
11	E800, 0000			
12	E800, 1800			
13	0800, 0800			
14	0800, F800			
15	F800, F800			
16	F800, 0800			



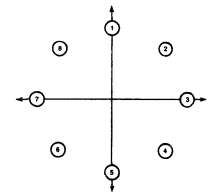
V.29/9600 BPS



V.29/7200 BPS



V.29/4800 BPS and V.27/2400 BPS



V.27/4800 BPS

Node 4

Average Power (16 bits, unsigned)

Typical value: 0889_{16} (corresponding to 0 dBm)

$$\text{Post-AGC Average Power in dBm} = 10 \text{ Log } \frac{(\text{Average Power Word})_{16}}{889_{16}}$$

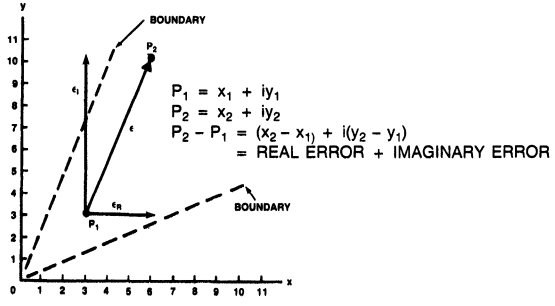
Pre-AGC Average Power in dBm = Post-AGC Avg. Power in dBm – AGC gain in dB

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
5	**AGC Gain (16 bits, unsigned)** Range: $0FC0_{16}$ to $7FFF_{16}$ for LRTH = 0 (– 43 dBm Threshold) 0640_{16} to $7FFF_{16}$ for LRTH = 1 (– 47 dBm Threshold) $\text{AGC Gain in dB} = 50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0.098$
7	**Equalizer Taps (32 bits, complex, twos complement)** Node 7 is not a single point but is actually a set of RAM locations containing adaptive equalizer tap coefficients. In V.29 configuration, access codes 01 through 20 hexadecimal represent 32 complex taps. In V 27 configuration, access codes 01 through 10 hexadecimal represent 16 complex taps, since the equalizer for V.27 is only half as long as the equalizer for V.29. The equalizer tap access codes can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers they require two write operations per tap, one for the real part and one for the imaginary part When writing the real part, the access codes 01 through 20 must be changed to 81 through A0. When writing the imaginary part, or when reading the complex number, the access codes 01 through 20 are correct. Registers 1:1 and 1:0 hold the most and least significant bytes, respectively, of the 16 bits during a write operation.
11	**Error Vector (32 bits, complex, twos complement)** Represents the difference between the received point (P2) and the nearest ideal point (P1).

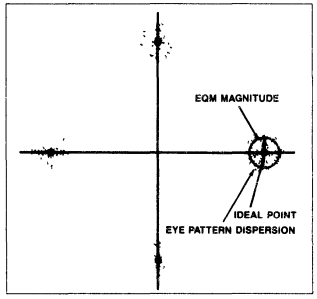
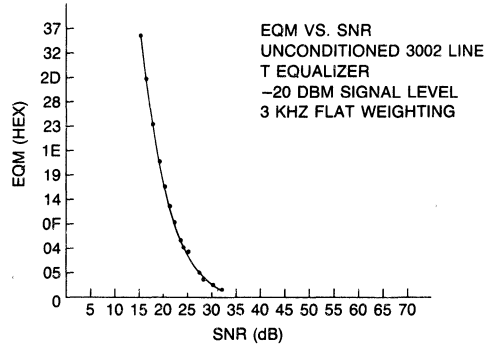
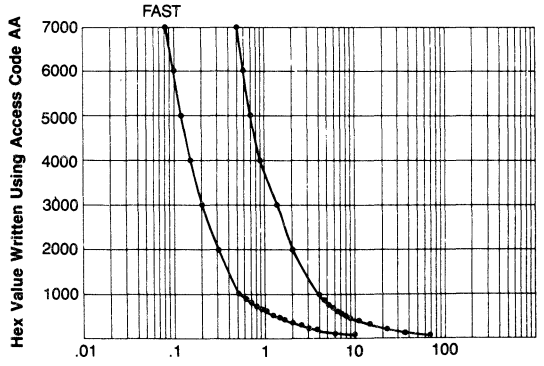
Configuration	Bit Rate (BPS)	Registers 3 and 2 Real Error	Registers 1 and 0 Imag. Error	Magnitude $\sqrt{Re^2 + Im^2}$
V.29	9600	$<0C00_{16}$	$<0C00_{16}$	$<0E66_{16}$
V.29	7200	$<2400_{16}$	$<2400_{16}$	$<1AD4_{16}$
V.29	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V 27	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	2400	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$

Error Vector Maximum Values

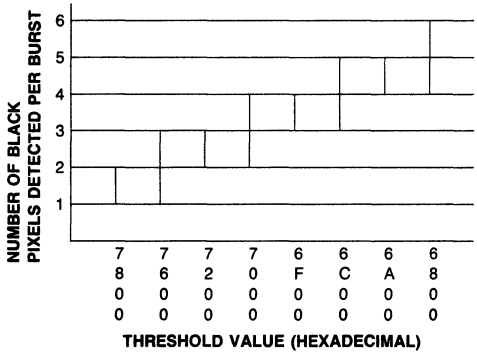


12	**Rotation Angle (16 bits, twos complement)** Represents instantaneous correction for phase and frequency errors. $\text{Rotation Angle in degrees} = \frac{(\text{Rot. Angle Word})_{16}}{10000_{16}} \times 180$

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
13	**Frequency Correction (16 bits, twos complement)** Represents component of rotation angle caused by frequency error Range: $FC00_{16}$ to 0400_{16} representing ±37.5 Hz Freq Correction in Hz = $\frac{(\text{Freq. Correction Word})_{16}}{10000_{16}} \times$ Baud Rate in Hz
14	**Eye Quality Monitor, EQM (16 bits, unsigned)** Equals the filtered squared magnitude of the error vector. Proportionality to bit error rate is determined by particular application. Stabilizes in approximately 700 baud times from $\overline{\text{RLSD}}$ going active  **Relationship of EQM to Eye Pattern**  **Typical Eye-Quality Versus Signal-to-Noise Ratio for V.29/9600**
15	***Group 2 Baseband Signal (16 bits, unsigned)** Range: 0000_{16} to 0600_{16} represents black 1000_{16} to 2100_{16} represents white
16	***Group 2 AGC Gain (16 bits, unsigned)** (AGC Gain in dB = $50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0.098$
17	***Group 2 AGC Slew Rate** Can be adjusted by the host. Range: 0000_{16} to $7FFF_{16}$  **Seconds to Stabilize AGC for –55 DBM to 0 DBM Step**

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
18	***Group 2 PLL Frequency Correction (16 bits, twos complement)** Range: $FC6A_{16}$ to 0346_{16} representing ±140 Hz Frequency correction in Hz = Frequency correction number (0.167)
19	***Group 2 PLL Slew Rate** Represents gain of first order term in phase locked loop. Range: 0010_{16} to 7000_{16} for stable operation Directly proportional to PLL slew rate
20	***Group 2 Black/White Threshold (16 bits, unsigned)** Default value: $(7800)_{16}$  **NOTE:** **1. 100 WHITE PIXELS SENT FOLLOWED BY 4 BLACK PIXELS SENT.** **2. RESULTS OBTAINED AT 0 DBM, NO COMPROMISE EQUALIZERS IN BACK TO BACK CONNECTION.**
21	***Group 2 Phase Limit (16 bits, twos complement)** When phase error exceeds this limit, PLL updating is suspended. Default: 5000_{16} representing ±67.5 degrees Phase limit = $180° - \left[\frac{(\text{Phase Limit})_{16}}{7FFF_{16}} \times 180° \right]$. Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits, etc.
	*See Rockwell Application Note, R96F Modem Recommended Receive Sequence for Group 2 Facsimile (Order No. 655, Rev. 3).

Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	—	—	EPT	SQEXT	T2	LRTH
4	CONFIGURATION							
3	RAM DATA XSM, FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register \ Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only)

Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	—	—	—	—	IE1	—	MDA1
D	—	TLE	RLE	J3L	—	—	FRT*	RAMW
C	—	—	—	—	—	—	—	G2FGC
B	FR3	FR2	FR1	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	—
4	—	—	—	—	—	$\overline{P2DET}$	—	—
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register \ Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).
* = Added in 5301-20

Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1:7 0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present. $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$
(None)	Configuration	0 4.0–7	The host processor configures the modem by writing a control code into the configuration register in the interface memory space (See SETUP) ***Configuration Control Codes*** Control codes for the five available modem configurations are **Configuration** — **Configuration Code (HEX)** V 29 9600 — 14 V 29 7200 — 12 V 29 4800 — 11 V.27 4800 — 0A V.27 2400 — 09 FSK — 20 Group 2 — 40 Tone Transmit — 80 ***Configuration Definitions*** Definitions for the five available modem configurations are: 1 *V 29.* When any of the V.29 configurations has been selected, the modem operates as specified in CCITT Recommendation V.29. 2 *V.27* When any of the V.27 configurations has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3 *FSK.* The modem operates as a CCITT T30 compatible 300 bps FSK modem having characteristics of the CCITT V 21 channel 2 modulation system. 4 *Group 2* The modem operates as a CCITT T3 compatible AM modem This configuration permits transmission to and reception from Group 2 facsimile apparatus A carrier frequency of 2100 Hz is used A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black When in the receive state, the modem recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal. This technique allows a baseband of 3400 Hz to be recovered The recovered baseband signal is available on the microprocessor bus The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number This number may be changed by the user. Receiver data is presented to the RXD output at a rate of 10368 samples per second The user should strobe the data on the rising edge of the data clock (DCLK) A logical 1 level (high voltage) represents white A logical 0 level (low voltage) represents black. 5 *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0 146486 Hz ±0 01% The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%.
EPT	Echo Protector Tone	0 5:3	If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V 27 and V 29 configurations, although it is not specified in the CCITT V.29 Recommendation.
$\overline{\text{FED}}$	Fast Energy Detector	1 5:6	The zero state of $\overline{\text{FED}}$ indicates energy is present above the receiver threshold in the passband. $\overline{\text{FED}}$ is not used for Group 2 facsimile

3

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
(None)	FREQL/FREQM	0:2:0-7, 0:3:0-7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below. *FREQM Register (0:3)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01%. Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below: **Frequency (Hz) / FREQM / FREQL** 462 / 0C / 52 1100 / 1D / 55 1650 / 2C / 00 1850 / 31 / 55 2100 / 38 / 00
FRT	Freeze Taps		When FRT is a one, adaptive equalization taps are prevented from changing.
FR1 – FR3	Frequency 1,2,3	1:B:5,6,7	The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for FR1, FR2 and FR3 are: **Bit / Frequency (Hz)** FR1 2100 FR2 1100 FR3 462
G2FGC	Group 2 Fast Gain Control	1:C:0	The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group 2 Facsimile.
IA1	Interrupt Active (One)	1:E:7	IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volts.
IA0	Interrupt Active (Zero)	0:E:7	IA0 is a one when Chip 0 is driving $\overline{IRQ}$ to zero volts.
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one.
IE1	Interrupt Enable (One)	1:E:2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one.
J3L	Japanese 3 Link	1:D:4	The one state of J3L selects this standard for link amplitude equalizer. The zero state of J3L selects U.S. survey long.
LRTH	Lower Receive Threshold	0:5:0	The one state of LRTH lowers the receiver turn-on threshold from – 43 dBm to – 47 dBm. (See SETUP)
MDA0	Modem Data Available (Zero)	0:E:0	MDA0 goes to one when the modem reads or writes register 0:0. MDA0 goes to zero when the host processor reads or writes register 0:0. MDA0 is used for parallel mode as well as for diagnostic data retrieval.
MDA1	Modem Data Available (One)	1:E:0	MDA1 goes to one when the modem writes register 1:0. MDA1 goes to zero when the host processor reads register 1:0.
PDM	Parallel Data Mode	0:F:7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
$\overline{\text{PNDET}}$	Period 'N' Detector	1 7:6	The zero state of $\overline{\text{PNDET}}$ indicates a PN sequence has been detected. $\overline{\text{PNDET}}$ sets to a one at the end of the PN sequence
$\overline{\text{P2DET}}$	Period '2' Detector	1:4·2	The zero state of $\overline{\text{P2DET}}$ indicates a P2 sequence has been detected. $\overline{\text{P2DET}}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1.F·0 – 7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Access S	0·F:0 – 6	Contains the RAM access code used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XBL	1.2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XBM	1·3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XSL	0 2·0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device)
(None)	RAM Data XSM	0·3·0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data YBL	1.0·0 – 7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device) See DA1
(None)	RAM Data YBM	1:1:0 – 7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Data YSL	0.0·0 – 7	Least significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device) Shared by parallel data mode for presenting channel data to the host microprocessor bus. See Transceiver Data and DA0.
(None)	RAM Data YSM	0:1 0 – 7	Most significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device).
RAMW	RAM Write Chip 1 (baud rate device)	1:D·0	RAMW is set to a one by the host processor when performing diagnostic writes to the baud rate device (Chip 1). RAMW is set to a zero by the host when reading RAM diagnostic data from Chip 1.
RLE	Receiver Link Equalizer	1.D·5	The one state of RLE enables the link amplitude equalizer in the receiver.
RTS	Request-to-Send	0:5:7	The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed. RTS parallels the operation of the hardware $\overline{\text{RTS}}$ control input These inputs are "ORed" by the modem.
SETUP	Setup	0 E:3	The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for equalizer (0·5·1) and threshold (0·5:0). SETUP returns to zero when acted on by the modem. The time required for the SETUP bit to cause a change depends on the current state of the modem. The following table lists worst case delays.
SQEXT	Squelch Extend	0:5·2	The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.
TDIS	Training Disable	0:5:6	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one prior to $\overline{\text{RTS}}$ going on, the generation of a training sequence is prevented at the start of transmission.
TLE	Transmitter Link Equalizer	1·D:6	The one state of TLE enables the link amplitude equalizer in the transmitter

Current State	V.21	G2	High Speed Receiver	High Speed Transmitter
DELAY	14 ms	400 μs	2 BAUD	2 BAUD + TURNOFF Sequence + Training (if applicable) + SQUELCH (if applicable)

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
(None)	Transceiver Data	0:0:0–7	In receive parallel data mode, the modem presents eight bits of channel data in register 0:0 for reading by the host microprocessor. After the eight bits have been accumulated in register 0:C they are transferred to 0:0 and bit 0:E:0 goes to a one. When the host reads 0:0, bit 0:E:0 resets to a zero. The first bit of received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync characters. Bit 0:E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations. In transmit parallel data mode the host stores data at location 0:0. This action causes bit 0:E:0 to reset to a 0. When the modem transfers the data from 0:0 to 0:2 bit 0:E:0 sets to a 1. The data is serially transmitted from register 0:2 least significant bit first. Received data is shifted into register 0:C from MSB toward LSB.
T2	T/2 Equalizer Select	0:5:1	If T2 is a one, an adaptive equalizer with two taps per baud is used. If T2 is a zero, an adaptive equalizer with one tap per baud is used. The number of taps remains the same for both cases. (See SETUP)

PERFORMANCE

Whether functioning in V.27 ter or V.29 configuration, the modem provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm as illustrated.

TYPICAL PHASE JITTER

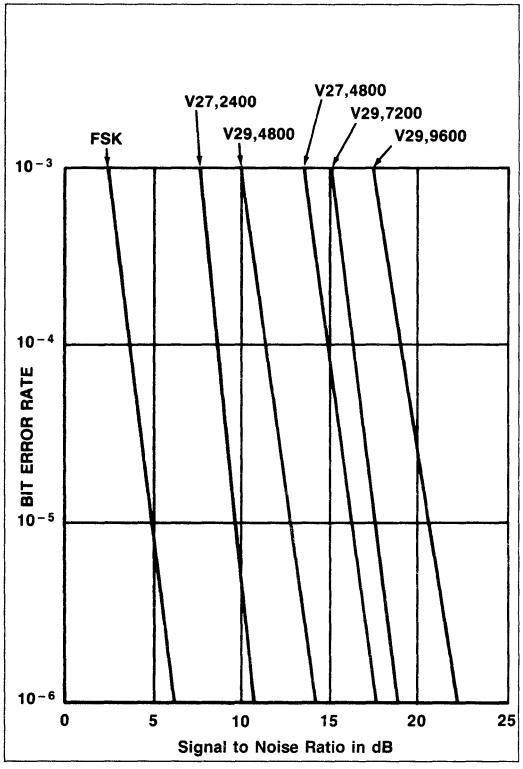
At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

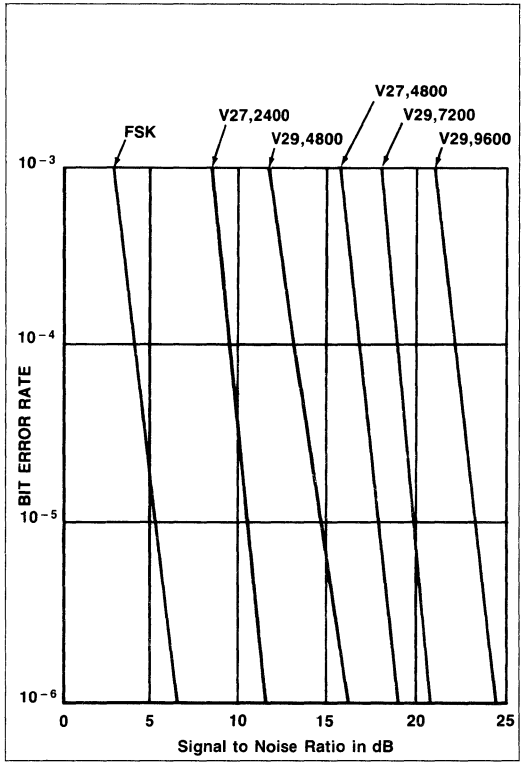
At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

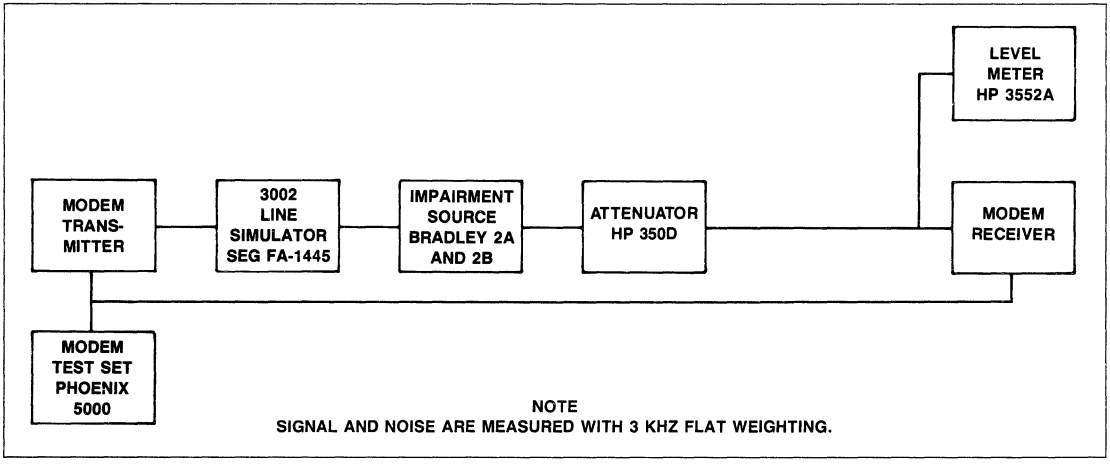
An example of the BER performance capabilities is given in the following diagrams:



Typical Bit Error Rate
(Back-to-Back, T Equalizer, Level –20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer Level –20 dBm)



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	400 mA	<500 mA
+12 Vdc	±5%	5 mA	< 10 mA
−12 Vdc	±5%	30 mA	< 50 mA

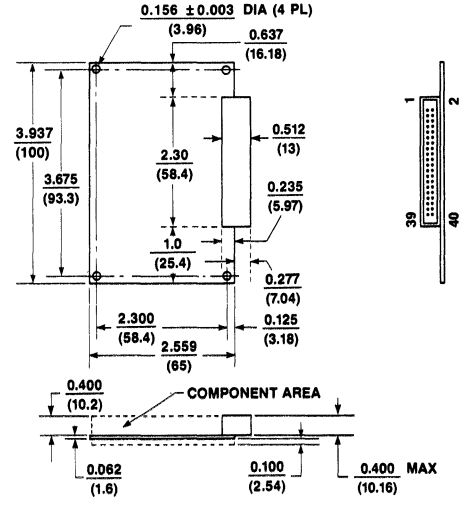
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature	
Operating	
R96F	0°C to +60°C (32°F to 140°F)
R96FI	0°C to +70°C (32°F to 158°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins. Burndy FRS 40BS8P or equivalent mating connector.
Dimensions	
Width	3.94 in. (100 mm)
Length	2.56 in. (65 mm)
Height	0 40 in. (10.2 mm)
Weight (max.)	2.6 oz. (73 g)
Lead Extrusion (max.)	0 100 in (2 54 mm)



RIBBON CONNECTOR VERSION

R96FI Dimensions and Pin Locations

R96MD
9600 bps Facsimile Modem

INTRODUCTION

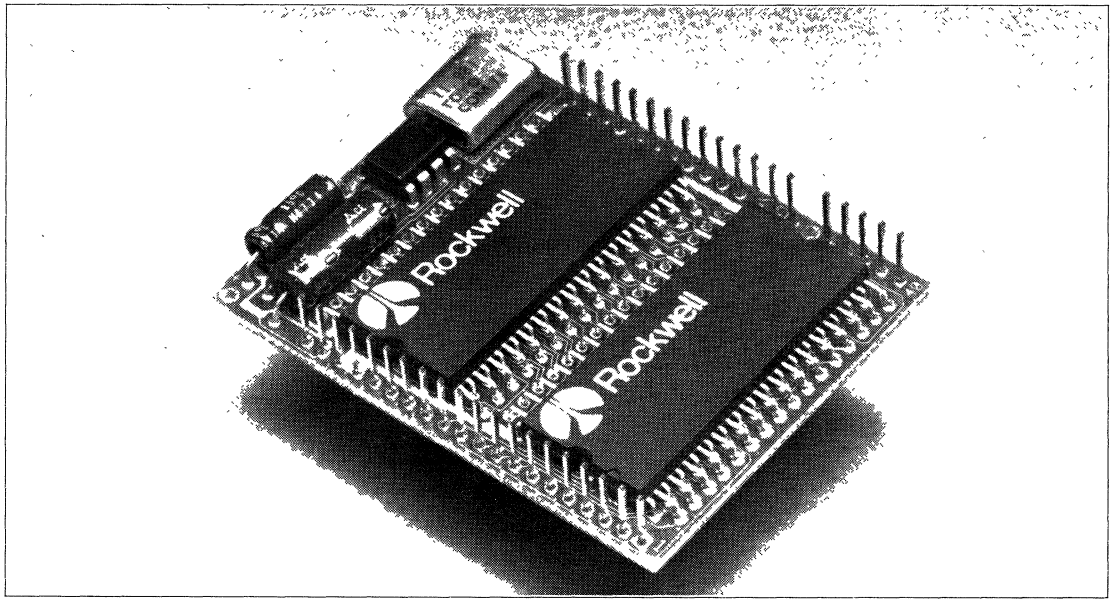
The Rockwell R96MD is a synchronous 9600 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, T.30, T 4 and T.3. The R96MD can operate at speeds of 9600, 7200, 4800, 2400 and 300 bps. Employing advanced signal processing techniques, the R96MD can transmit and receive data even under extremely poor line conditions.

The R96MD is designed for use in Group 3 facsimile machines and is also compatible with Group 2 machines. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface, and dual in-line pin (DIP) interface simplify system design and allow direct installation on the host module.

FEATURES

- Compatible with:
  - — CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
- Group 3 and Group 2 Facsimile
- Half-Duplex (2-Wire)
- Programmable Tone Detection
- Programmable Dual/Single Tone Generation
- Dynamic Range: −47 dBm to 0 dBm
- Programmable Transmit Levels
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Small Size: 50.8 mm x 65.4 mm (2.0 in. x 2.575 in.)
- Low Power Consumption: 2 W (Typical)
- Transmit Output Level: +5 dBm ±1 dB
- TTL and CMOS Compatible



R96MD Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T.30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01%)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group 2 Identification (C12)	1850
Group 2 Command (GC2)	2100
Group 2 Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462

Carrier Frequencies

Function	Frequency (Hz ±0.01%)
T.3 Carrier (Group 2)	2100
V.27 ter Carrier	1800
V.29 Carrier	1700

TONE GENERATION

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Specification	Baud Rate (Symbols/Sec.)	Bits Per Baud	Data Rate (BPS) (±0.01%)	Symbol Points
V.29	2400	4	9600	16
V.29	2400	3	7200	8
V.27	1600	3	4800	8
V.27	1200	2	2400	4

DATA ENCODING

The modem data encoding conforms to CCITT recommendations V.29 and V.27 ter.

EQUALIZERS

The modem provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

The transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the modem can adapt to received frequency error of up to ±10 Hz with less than a 0.2 dB degradation in BER performance. Group 2 carrier recovery capture range is 2100 ±30 Hz. The Group 2 receiver operates properly when the carrier is varied by ±16 Hz at a 0.1 Hz per second rate.

RECEIVE LEVEL

The modem receiver circuit satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the modem provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level defaults to +5 dBm ±1 dB at power on. When using the default transmit level and driving a 600 ohm load, the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load. The output level can be programmed over a 10 dB range by performing a RAM write operation

TRANSMIT TIMING

In the transmit state, the modem provides a Data Clock (DCLK) output with the following characteristics:

1 *Frequency* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (±0.01%). In Group 2, DCLK tracks an external 10368 Hz clock. If the external clock input (XCLK) is grounded the Group 2 DCLK is 10372.7 Hz ±0 01%
2. *Duty Cycle.* 50 ±1%

Transmit Data (TXD) must be stable during the 1 microsecond period immediately preceding and the 1 microsecond period immediately following the rising edge of DCLK.

TURN-ON SEQUENCE

A total of ten selectable turn-on sequences can be generated by the modem, as defined in the following table·

Turn-On Sequences

Specification	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V 29	253 ms	438 ms
V 27 4800 bps	708 ms	913 ms
V 27 2400 bps	943 ms	1148 ms
V 21 300 bps	≤14 ms	≤14 ms
Group 2	≤400 μs	≤400 μs

TURN-OFF SEQUENCE

For V 27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V 21 the transmitter turns off within 7 ms after $\overline{\text{RTS}}$ goes false. In Group 2 the transmitter turns off within 200 μs after $\overline{\text{RTS}}$ goes false.

CLAMPING

The following clamps are provided with the modem·

1 *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{\text{RLSD}}$ is off.
2 *Received Line Signal Detector (RLSD).* $\overline{\text{RLSD}}$ is clamped off (squelched) during the time when $\overline{\text{RTS}}$ is on.
3 *Extended Squelch.* Optionally, $\overline{\text{RLSD}}$ remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{\text{CTS}}$)

The time between the off-to-on transition of $\overline{\text{RTS}}$ and the off-to-on transition of $\overline{\text{CTS}}$ is dictated by the length of the training sequence Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps In V.21 $\overline{\text{CTS}}$ turns on in 14 ms or less In Group 2 $\overline{\text{CTS}}$ turns on in 400 μs or less.

The time between the on-to-off transition of $\overline{\text{RTS}}$ and the on-to-off transition of $\overline{\text{CTS}}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{\text{RLSD}}$)

For either V.27 ter or V 29, $\overline{\text{RLSD}}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{\text{RLSD}}$ off-to-on response time is 15 ±10 ms The $\overline{\text{RLSD}}$ on-to-off response time for V 27 is 10 ±5 ms and for V.29 is 30 ±9 ms Response times are measured with a signal at least 3 dB above the actual $\overline{\text{RLSD}}$ on threshold or at least 5 dB below the actual $\overline{\text{RLSD}}$ off threshold.

The $\overline{\text{RLSD}}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided·

1 Greater than −43 dBm ($\overline{\text{RLSD}}$ on)
  Less than −48 dBm ($\overline{\text{RLSD}}$ off)
2 Greater than −47 dBm ($\overline{\text{RLSD}}$ on)
  Less than −52 dBm ($\overline{\text{RLSD}}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA)

MODES OF OPERATION

The modem operates in either a serial or a parallel mode.

SERIAL MODE

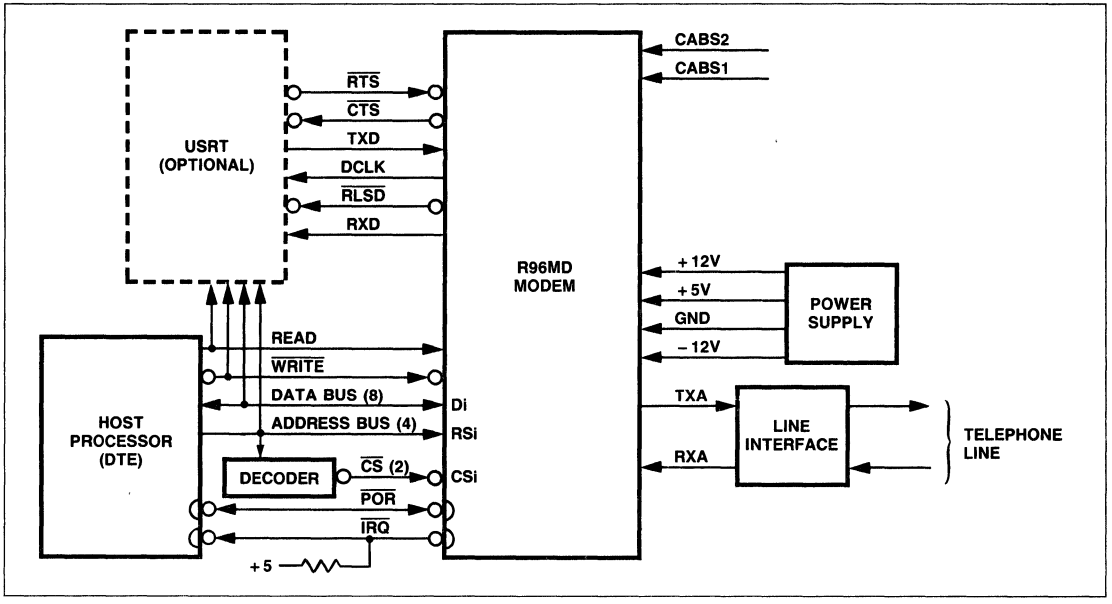
The serial mode uses standard V 24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Modem Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The modem can transfer channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on In either mode the modem is configured by the host processor via the microprocessor bus.



Modem Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 40-pin dual in-line pin (DIP) connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the Modem Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital or Analog Interface Characteristics.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0–RS3), data (D0–D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABS2	CABS1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Two analog signals, TXA and RXA, provide the interface point for telephone company audio circuits.

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the PSTN. The output structure of TXA is a low impedance amplifier. A series resistor is required in order to match this output to a standard telephone load of 600 ohms.

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may be back-to-back zener diodes across the transformer or a varistor across the transformer.

Overhead

Except for the power-on-reset signal $\overline{POR}$, the overhead signals are dc power or ground points. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives pin 39 to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 39, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 39 low for at least 3 μs. When an external low input is applied to pin 39, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 39 is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The POR sequence leaves the modem configures as follows:

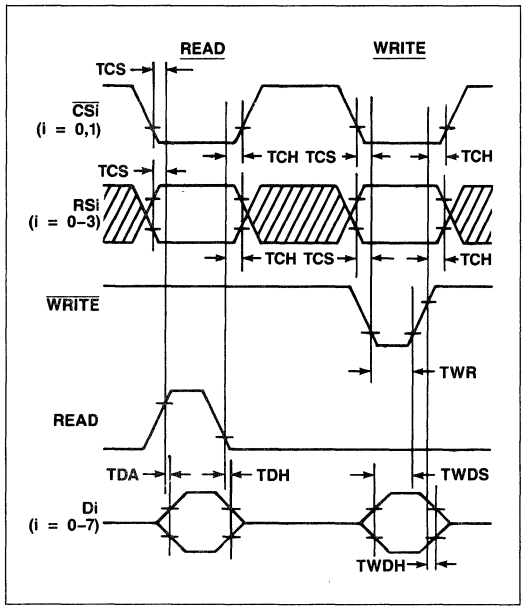
- V.29/9600 bps
- T/2 equalizer
- Serial mode
- Training enabled
- Echo protector tone enabled
- No extended squelch
- Higher receive threshold
- Interrupts disabled
- RAM Access S = 00
- RAM Access B = 22

This configuration is suitable for performing high speed data transfer on the PSTN with the serial data port selected as the input and output point for data terminal equipment (DTE).

Modem Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground	GND	17,18	Power Supply Return
+5 volts	PWR	33,34	+5 volt supply
+12 volts	PWR	21	+12 volt supply
−12 volts	PWR	19	−12 volt supply
$\overline{POR}$	I/OB	39	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	9	Data Bus (8 Bits)
D6	I/OA	8	
D5	I/OA	2	
D4	I/OA	3	
D3	I/OA	4	
D2	I/OA	5	
D1	I/OA	6	
D0	I/OA	7	
RS3	IA	13	Register Select (4 Bits) Select Reg 0−F
RS2	IA	14	
RS1	IA	15	
RS0	IA	16	
$\overline{CS0}$	IA	11	Chip Select Sample Rate Device
$\overline{CS1}$	IA	38	Chip Select Baud Rate Device
$\overline{READ}$	IA	10	Read Enable
$\overline{WRITE}$	IA	12	Write Enable
$\overline{IRQ}$	OB	1	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	30	Data Clock
XCLK	IB	31	External Clock for Group 2
$\overline{RTS}$	IB	32	Request-to-Send
$\overline{CTS}$	OC	28	Clear-to-Send
TXD	IB	27	Transmitter Data
RXD	OC	26	Receiver Data
$\overline{RLSD}$	OC	29	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IB	24	Cable Select 1
CABS2	IB	25	Cable Select 2
E. ANALOG SIGNALS			
TXA	AA	23	Transmitter Analog Output
RXA	AB	22	Receiver Analog Input
AUX	AC	20	Auxiliary Analog Input

Notes: 1 Pin 35 is removed for keying connector.
2 Unused inputs tied to +5V or ground require individual 10K Ω series resistors.



Microprocessor Interface Timing Diagram

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data Access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
CSi, RSi hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 60K ohms ±23%
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors The input impedance is 1K ohms, and the gain to the transmitter is −0.4 dB ±1 dB.

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type						
			IA	IB	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.				2.0 min.	5.25 max. 2 0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V			2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V			0.4 max [2]	0.4 max.[2]	0.4 max [2]	0.4 max.[2] ±12 5 max.[4]	0 4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2 5 max.						
I_{OH}	Output Current, High	mA			−0.1 max.				
I_{OL}	Output Current, Low	mA			1 6 max	1 6 max ± 10 max.	1.6 max.		
I_L	Output Current, Leakage	μA							
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.			−240 max. −10 mın		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5				10	40
C_D	Capacitive Drive	pF			100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3 I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5 25 Vdc
5 I load = 0.36 mA

SOFTWARE CIRCUITS

The modem includes two signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem sample rate (9600 bps). Registers in chip 1 update at the selected baud rate except in Group 2 and FSK configurations when they update at the sample rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Status/Control Bits

Modem operation is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a '—' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

RAM Data Access

The user can access much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register 0:F (RAM ACCESS S) or 1:F (RAM ACCESS B). The RAM Access Codes table lists access codes for storage in registers 0:F or 1:F and the corresponding diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long.

These bits are written into interface memory registers 0:3, 0:2, 0:1 and 0:0, or 1:3, 1:2, 1:1 and 1:0, in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit 0:5:5 (RAMWS) or bit 1:D:0 (RAMWB) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM in chip 0 or in chip 1, respectively. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the most significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAM Access B bits of register 1:F for chip 1, or by means of 0:5:4 (RAE) and 0:F (RAM Access S) for chip 0. When bit 1:F:7 or 0:5:4 is set to one, the XRAM is selected. When 1:F:7 or 0:5:4 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the modem data available bit 0:E:0 or 1:E:0 (MDAi) is reset to zero. When the modem reads or writes register 0, MDAi is set to a one. When set to a one by the host, bit 0:E:2 or 1:E:1 (IEi) enables the MDAi bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit 0:E:7 or 1:E:7 (IAi) goes to a one.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem. This information is scaled as shown in the Diagnostic Data Scaling table.

RAM Access Codes

Node	Function	Access	RAE	Chip	Read Reg. No.
1	Received Signal Samples	40	X	0	2,3
2	Demodulator Output	42	X	0	0,1,2,3
3	Low Pass Filter Output	54	X	0	0,1,2,3
4	Average Power	5C	X	0	2,3
5	AGC Gain	3C	X	0	2,3
6	Tone 1 Frequency	71	1	0	2,3
7	Tone 1 Level	72	1	0	2,3
8	Tone 2 Frequency	71	0	0	0,1
9	Tone 2 Level	72	0	0	0,1
10	Output Level	4C	0	0	0,1
11	Equalizer Input	40	N.A	1	0,1,2,3
12	Equalizer Tap Coefficients	01-20	N.A.	1	0,1,2,3
13	Unrotated Equalizer Output	61	N A.	1	0,1,2,3
14	Rotated Equalizer Output (Received Point—Eye Pattern)	22	N.A.	1	0,1,2,3
15	Decision Points (Ideal)	62	N A	1	0,1,2,3
16	Error Vector	63	N A.	1	0,1,2,3
17	Rotation Angle	00	N.A	1	0,1
18	Frequency Correction	A8	N.A	1	2,3
19	Eye Quality Monitor (EQM)	AB	N A.	1	2,3
20	G2 Baseband Signal	C8	N.A.	1	2,3
21	G2 AGC Gain	AD	N A.	1	2,3
22	G2 AGC Slew Rate	AA	N.A.	1	2,3
23	G2 PLL Frequency Correction	C2	N.A.	1	2,3
24	G2 PLL Slew Rate	F0	N.A	1	2,3
25	G2 Black/White Threshold	2A	N.A.	1	0,1
26	G2 Phase Limit	F2	N.A.	1	2,3
27	Checksum	2D	N.A.	1	2,3

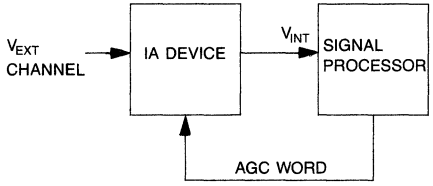
RAE = X is don't care since this location should only be read from, and *not* written to, by the host. N.A. is not applicable since RAE is not used in chip one.

Diagnostic Data Scaling

Node 1

Parameter/Scaling

Received Signal Samples = A/D Sample Word (signed 16 bits, twos complement)



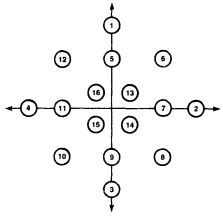
$$V_{INT} = \frac{(\text{A/D Sample Word})_{16}}{(40)_{16}} \times \frac{3}{256} \text{ Volts}$$

$$V_{EXT} = V_{INT} - LOG_{10}^{-1}\left[\frac{\text{AGC Gain (dB)}}{20}\right]$$

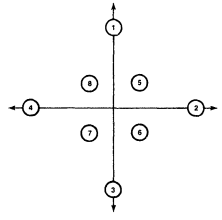
Nodes 2, 3, 11, 13, 14, 15

All Baseband Signal Nodes (32 bits, complex, twos complement)

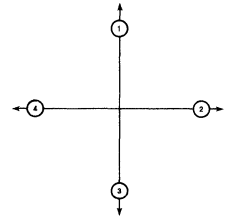
Point	Configuration			
	V.29/9600 x , y	V.29/7200 x , y	V.29/4800 & V.27/2400 x , y	V.27/4800 x , y
1	0000, 2800	0000, 2400	0000, 1F00	0000, 1F00
2	2800, 0000	2400, 0000	1F00, 0000	1600, 1600
3	0000, D800	0000, DC00	0000, E100	1F00, 0000
4	D800, 0000	DC00, 0000	E100, 0000	1600, EA00
5	0000, 1800	0C00, 0C00		0000, E100
6	1800, 1800	0C00, F400		EA00, EA00
7	1800, 0000	F400, F400		E100, 0000
8	1800, E800	F400, 0C00		EA00, 1600
9	0000, E800			
10	E800, E800			
11	E800, 0000			
12	E800, 1800			
13	0800, 0800			
14	0800, F800			
15	F800, F800			
16	F800, 0800			



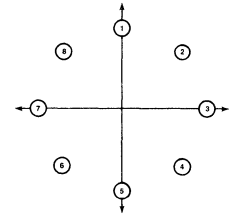
V.29/9600 BPS



V.29/7200 BPS



V.29/4800 BPS and V.27/2400 BPS



V.27/4800 BPS

Node 4

Average Power (16 bits, unsigned)

Typical value: 0889_{16} (corresponding to 0 dBm)

$$\text{Post-AGC Average Power in dBm} = 10 \text{ Log} \frac{(\text{Average Power Word})_{16}}{889_{16}}$$

Pre-AGC Average Power in dBm = Post-AGC Avg Power in dBm – AGC gain in dB

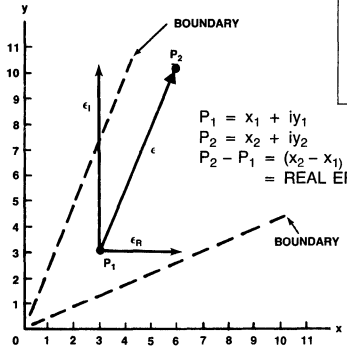
Diagnostic Data Scaling (continued)

<table>
<tr><th>Node</th><th>Parameter/Scaling</th></tr>
<tr><td>5</td><td>AGC Gain (16 bits, unsigned)

Range:
$0FC0_{16}$ to $7FFF_{16}$ for LRTH = 0 (– 43 dBm Threshold)
0640_{16} to $7FFF_{16}$ for LRTH = 1 (– 47 dBm Threshold)

$\text{AGC Gain in dB} = 50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0.098$</td></tr>
<tr><td>6, 8</td><td>Tone 1 and 2 Frequency (16 bits, unsigned)
N = 6.8267 (Frequency in Hz)
Convert N to hexadecimal then store in RAM.</td></tr>
<tr><td>7, 9</td><td>Tone 1 and Tone 2 Level
Calculate the power of each tone independently by using the equation for Output Number given at node 10. Convert these numbers to hexadecimal then store in RAM. Total power transmitted in tone configuration is the result of both tone 1 power and tone 2 power.</td></tr>
<tr><td>10</td><td>Output Level (16 bits, unsigned)
Output Number = $M\ [10^{(Po/20)}]$
Po = output power in dBm with series 600 ohm resistor into 600 ohm load.
Convert Output Number to hexadecimal and store in RAM
M varies depending on configuration.
The output level can only be changed after RTS is active.

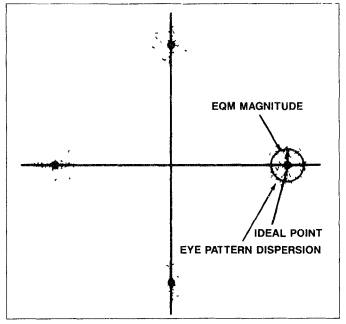
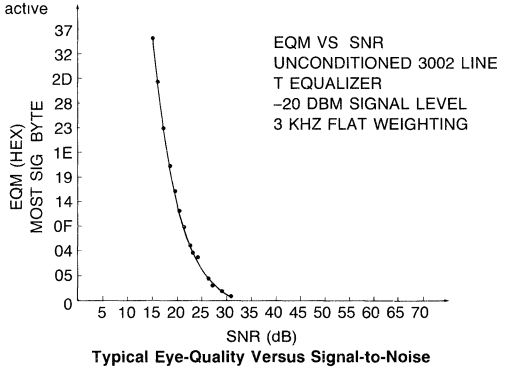
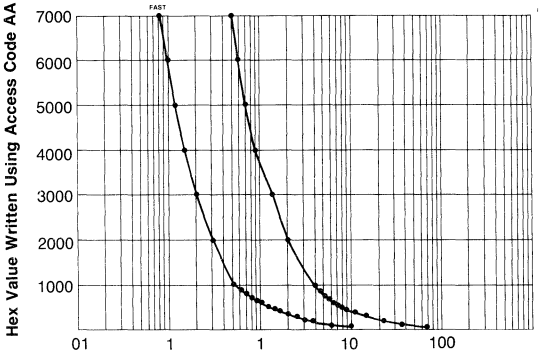
<table><tr><th>Configuration</th><th>M</th></tr><tr><td>V.29/9600</td><td>17408</td></tr><tr><td>V.29/7200</td><td>26880</td></tr><tr><td>V.27/4800</td><td>16640</td></tr><tr><td>V.27/2400</td><td>16640</td></tr><tr><td>FSK</td><td>16337</td></tr><tr><td>Group 2</td><td>30976</td></tr></table></td></tr>
<tr><td>12</td><td>Equalizer Taps (32 bits, complex, twos complement)
Node 12 is not a single point but is actually a set of RAM locations containing adaptive equalizer tap coefficients. In V.29 configuration, access codes 01 through 20 hexadecimal represent 32 complex taps. In V.27 configuration, access codes 01 through 10 hexadecimal represent 16 complex taps, since the equalizer for V.27 is only half as long as the equalizer for V.29.
The equalizer tap access codes can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers they require two write operations per tap, one for the real part and one for the imaginary part. When writing the real part, the access codes 01 through 20 must be changed to 81 through A0. When writing the imaginary part, or when reading the complex number, the access codes 01 through 20 are correct.
Registers 1:1 and 1:0 hold the most and least significant bytes, respectively, of the 16 bits during a write operation.</td></tr>
<tr><td>16</td><td>Error Vector (32 bits, complex, twos complement)
Represents the difference between the received point (P2) and the nearest ideal point (P1).

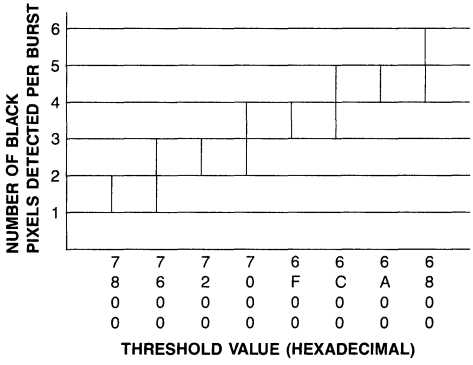
$P_1 = x_1 + iy_1$
$P_2 = x_2 + iy_2$
$P_2 - P_1 = (x_2 - x_1) + i(y_2 - y_1)$
= REAL ERROR + IMAGINARY ERROR

Error Vector Maximum Values
<table><tr><th>Configuration</th><th>Bit Rate (BPS)</th><th>Registers 3 and 2 Real Error</th><th>Registers 1 and 0 Imag. Error</th><th>Magnitude $\sqrt{Re^2 + Im^2}$</th></tr><tr><td>V 29</td><td>9600</td><td>$<0C00_{16}$</td><td>$<0C00_{16}$</td><td>$<0E66_{16}$</td></tr><tr><td>V.29</td><td>7200</td><td>$<2400_{16}$</td><td>$<2400_{16}$</td><td>$<1AD4_{16}$</td></tr><tr><td>V.29</td><td>4800</td><td>$<1C00_{16}$</td><td>$<1C00_{16}$</td><td>$<1C00_{16}$</td></tr><tr><td>V.27</td><td>4800</td><td>$<1C00_{16}$</td><td>$<1C00_{16}$</td><td>$<1C00_{16}$</td></tr><tr><td>V.27</td><td>2400</td><td>$<1C00_{16}$</td><td>$<1C00_{16}$</td><td>$<1C00_{16}$</td></tr></table></td></tr>
</table>

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
17	**Rotation Angle (16 bits, twos complement)** Represents instantaneous correction for phase and frequency errors Rotation Angle in degrees = $\frac{(\text{Rot Angle Word})_{16}}{10000_{16}} \times 180$
18	**Frequency Correction (16 bits, twos complement)** Represents component of rotation angle caused by frequency error Range $FC00_{16}$ to 0400_{16} representing ±37 5 Hz Freq Correction in Hz = $\frac{(\text{Freq Correction Word})_{16}}{10000_{16}} \times$ Baud Rate in Hz
19	**Eye Quality Monitor, EQM (16 bits, unsigned)** Equals the filtered squared magnitude of the error vector Proportionality to bit error rate is determined by particular application Stabilizes in approximately 700 baud times from $\overline{\text{RLSD}}$ going active  **Relationship of EQM to Eye Pattern**  **Typical Eye-Quality Versus Signal-to-Noise Ratio for V.29/9600**
20	***Group 2 Baseband Signal (16 bits, unsigned)** Range 0000_{16} to 0600_{16} represents black 1000_{16} to 2100_{16} represents white
21	***Group 2 AGC Gain (16 bits, unsigned)** AGC Gain in dB = $50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0\ 098$
22	***Group 2 AGC Slew Rate** Can be adjusted by the host Range 0000_{16} to $7FFF_{16}$  **Seconds to Stabilize AGC for -55 DBM to 0 DBM Step**

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
23	***Group 2 PLL Frequency Correction (16 bits, twos complement)** Range: $FC6A_{16}$ to 0346_{16} representing ±140 Hz Frequency correction in Hz = Frequency correction number (0167)
24	***Group 2 PLL Slew Rate** Represents gain of first order term in phase locked loop Range: 0010_{16} to 7000_{16} for stable operation Directly proportional to PLL slew rate
25	***Group 2 Black/White Threshold (16 bits, unsigned)** Default value $(7800)_{16}$  **NOTE:** **1. 100 WHITE PIXELS SENT FOLLOWED BY 4 BLACK PIXELS SENT.** **2. RESULTS OBTAINED AT 0 DBM, NO COMPROMISE EQUALIZERS IN BACK TO BACK CONNECTION.**
26	***Group 2 Phase Limit (16 bits, twos complement)** When phase error exceeds this limit, PLL updating is suspended. Default. 5000_{16} representing ±675 degrees Phase limit = $180° - \left[\frac{(\text{Phase Limit})_{16}}{(7FFF)_{16}} \times 180° \right]$. Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits.
27	**Checksum (16-bit unsigned)** ROM checksum number determined by revision level
	*See Rockwell Application Note, R96F Modem Recommended Receive Sequence for Group 2 Facsimile (Order No. 655, Rev. 3).

Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	RAMWS	RAE	EPT	SQEXT	T2	LRTH
4	CONFIGURATION							
3	RAM DATA XSM, FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL, TRANSCEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only)

Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	—	—	—	—	IE1	—	MDA1
D	—	—	—	—	—	—	FRT	RAMWB
C	—	—	—	—	—	—	—	G2FGC
B	FR3	FR2	FR1	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	—
4	—	—	—	—	—	$\overline{P2DET}$	—	—
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only)

Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1:7:0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present. $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
(None)	Configuration	0:4:0–7	The host processor configures the modem by writing a control code into the configuration register in the interface memory space. (See SETUP) ***Configuration Control Codes*** Control codes for the eight available modem configurations are: **Configuration** — **Configuration Code (HEX)** V.29 9600* — 14 V.29 7200 — 12 V.27 4800 — 0A V.27 2400 — 09 FSK — 20 Group 2 — 40 Tone Transmit — 80 DTMF Transmit — 81 *Default at POR. ***Configuration Definitions*** 1. *V.29.* When a V.29 configuration has been selected, the modem operates as specified in CCITT Recommendation V.29. 2. *V.27.* When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3. *FSK.* The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system. 4. *Group 2.* The modem operates as a CCITT T.3 compatible AM modem. This configuration permits transmission to and reception from Group 2 facsimile apparatus. A carrier frequency of 2100 Hz is used. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black. When in the receive state, the modem recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal. This technique allows a baseband of 3400 Hz to be recovered. The recovered baseband signal is available on the microprocessor bus. The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number. This number may be changed by the user. Receiver data is presented to the RXD output at a rate of 10368 samples per second. The user should strobe the data on the rising edge of the data clock (DCLK). A logical 1 level (high voltage) represents white. A logical 0 level (low voltage) represents black. 5. *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2) The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%. 6. *DTMF Transmit.* In this configuration, activating RTS causes the modem to transmit two tones at frequencies and output levels specified by the user By using the RAM Data Access routines, the user can program the tones and levels

Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
EPT	Echo Protector Tone	0.5.3	If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 recommendation.
$\overline{FED}$	Fast Energy Detector	1.5:6	The zero state of $\overline{FED}$ indicates energy is present above the receiver threshold in the passband. $\overline{FED}$ is not used for Group 2 Facsimile.
(None)	FREQL/FREQM	0:2:0-7, 0:3 0-7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below *FREQM Register (0:3)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01%. Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below: **Frequency (Hz) / FREQM / FREQL** 462 / 0C / 52 1100 / 1D / 55 1650 / 2C / 00 1850 / 31 / 55 2100 / 38 / 00
FRT	Freeze Taps		When FRT is a one, adaptive equalization taps are prevented from changing.
FR1 – FR3	Frequency 1,2,3	1:B:5,6,7	The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for FR1, FR2 and FR3 are: **Bit / Frequency (Hz)** FR1 / 2100 FR2 / 1100 FR3 / 462
G2FGC	Group 2 Fast Gain Control	1:C 0	The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group 2 Facsimile.
IA1	Interrupt Active (One)	1:E:7	IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volts.
IA0	Interrupt Active (Zero)	0:E:7	IA0 is a one when Chip 0 is driving $\overline{IRQ}$ to zero volts.
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one.
IE1	Interrupt Enable (One)	1:E:2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one.
LRTH	Lower Receive Threshold	0:5 0	The one state of LRTH lowers the receiver turn-on threshold from – 43 dBm to – 47 dBm (See SETUP)
MDA0	Modem Data Available (Zero)	0:E 0	MDA0 goes to one when the modem reads or writes register 0:0. MDA0 goes to zero when the host processor reads or writes register 0 0. MDA0 is used for parallel mode as well as for diagnostic data retrieval

Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
MDA1	Modem Data Available (One)	1:E:0	MDA1 goes to one when the modem writes register 1·0. MDA1 goes to zero when the host processor reads register 1:0.
PDM	Parallel Data Mode	0:F:7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.
$\overline{\text{PNDET}}$	Period 'N' Detector	1:7:6	The zero state of $\overline{\text{PNDET}}$ indicates a PN sequence has been detected. $\overline{\text{PNDET}}$ sets to a one at the end of the PN sequence.
$\overline{\text{P2DET}}$	Period '2' Detector	1:4:2	The zero state of $\overline{\text{P2DET}}$ indicates a P2 sequence has been detected. $\overline{\text{P2DET}}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1:F:0 – 7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Access S	0:F:0 – 6	Contains the RAM access code used in reading or writing RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XBL	1:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XBM	1:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XSL	0:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XSM	0:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data YBL	1:0:0 – 7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device). See DA1.
(None)	RAM Data YBM	1:1:0 – 7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Data YSL	0:0:0 – 7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 0 (sample rate device). Shared by parallel data mode for presenting channel data to the host microprocessor bus. See Transceiver Data and DA0.
(None)	RAM Data YSM	0:1:0 – 7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 0 (sample rate device).
RAE	RAM Address Extension	0:5:4	This bit is an extension of RAM Access S when RAMWS is a one. During a RAM write to Chip 0, when RAE is a 1 the XRAM is selected and when RAE is a 0 the YRAM is selected.
RAMWB	RAM Write Chip 1 (baud rate device)	1:D:0	RAMWB is set to a one by the host processor when performing diagnostic writes to the baud rate device (Chip 1). RAMWB is set to a zero by the host when reading RAM diagnostic data from Chip 1.
RAMWS	RAM Write Chip 0 (sample rate device)	0:5:5	RAMWS is set to a one by the host processor when performing diagnostic writes to the sample rate device (Chip 0). RAMWS is set to a zero by the host when reading RAM diagnostic data from Chip 0.
RTS	Request-to-Send	0:5:7	The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed. RTS parallels the operation of the hardware $\overline{\text{RTS}}$ control input. These inputs are "ORed" by the modem.
SETUP	Setup	0:E:3	The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for equalizer (0:5:1) and threshold (0:5:0). SETUP returns to zero when acted on by the modem. The time required for the SETUP bit to cause a change depends on the current state of the modem. The following table lists worst case delays.

Current State	V.21	G2	High Speed Receiver	High Speed Transmitter
DELAY	14 ms	400 μs	2 BAUD	2 BAUD + TURNOFF Sequence + Training (if applicable) + SQUELCH (if applicable)

Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
SQEXT	Squelch Extend	0.5·2	The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.
TDIS	Training Disable	0:5:6	If TDIS is a one in the receive state, the modem is prevented from entering the training phase If TDIS is a one prior to $\overline{RTS}$ going on, the generation of a training sequence is prevented at the start of transmission.
(None)	Transceiver Data	0.0.0–7	In receive parallel data mode, the modem presents eight bits of channel data in register 0 0 for reading by the host microprocessor. After the eight bits have been accumulated in register 0·C they are transferred to 0 0 and bit 0·E.0 goes to a one. When the host reads 0:0, bit 0.E:0 resets to a zero The first bit of received data is not necessarily located in bit 0.0:0. The host must frame the received data by searching for message sync characters Bit 0·E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations. In transmit parallel data mode the host stores data at location 0:0 This action causes bit 0:E:0 to reset to a 0. When the modem transfers the data from 0·0 to 0:2 bit 0:E:0 sets to a 1. The data is serially transmitted from register 0.2 least significant bit first. Received data is shifted into register 0·C from MSB toward LSB.
T2	T/2 Equalizer Select	0.5·1	If T2 is a one, an adaptive equalizer with two taps per baud is used. If T2 is a zero, an adaptive equalizer with one tap per baud is used. The number of taps remains the same for both cases (See SETUP)

PERFORMANCE

Whether functioning in V.27 ter or V.29 configuration, the modem provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of – 20 dBm as illustrated.

TYPICAL PHASE JITTER

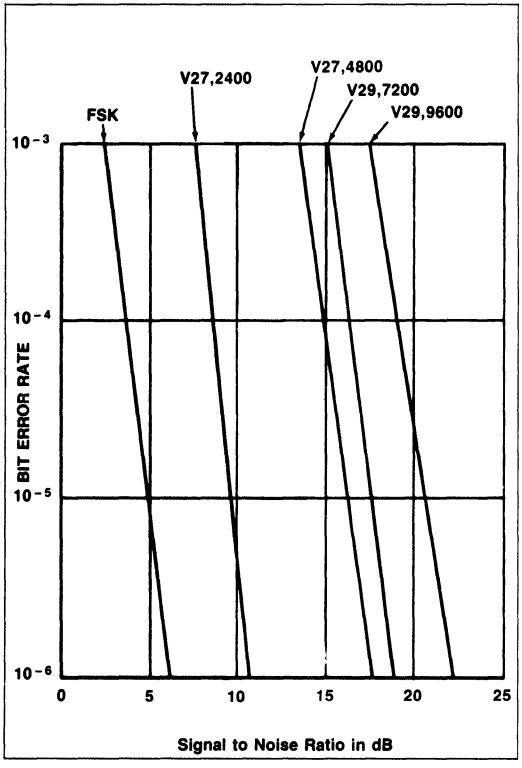
At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

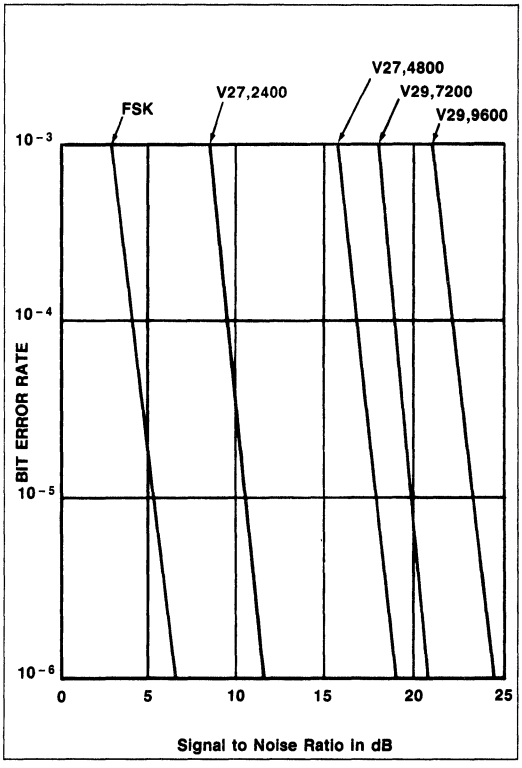
At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

The BER curves shown were prepared from data obtained using a TAS 1000 communication test system.



Typical Bit Error Rate
(Back-to-Back, T Equalizer, Level −20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer, Level −20 dBm)

3

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	350 mA	<500 mA
+12 Vdc	±5%	5 mA	< 10 mA
−12 Vdc	±5%	30 mA	< 50 mA

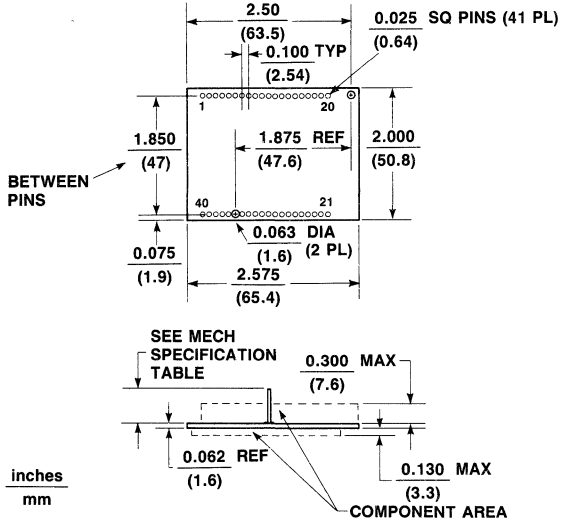
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical

Parameter	Specification
Board Structure	Single PC board with a row of 20 pins and a row of 20 pins in a dual-in-line pin configuration. Mates with Berg 65780 or equivalent
Dimensions	
Width	2.0 in (50.8 mm)
Length	2.575 in (65.4 mm)
Component Height	0.30 in (7.6 mm) above, 0.13 in. (3.30 mm) below
Weight (max.)	2.6 oz. (73 g)
Pins	
Length above PCB	0.300 in. ±0.015 in. (7.6 ±0.38 mm), 0.433 ±0.015 in. (11 ±0.38 mm), 0.535 ±0.015 (13.6 ±0.38 mm)
Thickness	0.025 in (0.64 mm) square
Plating	Gold



R96MD Dimensions and Pin Locations

Rockwell

R144HD
14400 bps Half-Duplex Modem

INTRODUCTION

The Rockwell R144HD is a synchronous 14400 bits per second (bps) half-duplex modem. It is designed for operation over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

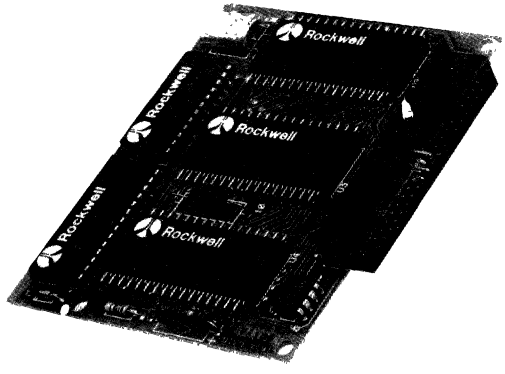
The modem satisfies the telecommunications requirements specified in CCITT recommendations V.33, V.29, V.27 ter, T.30, T.4 and T.3. The R144HD can operate at speeds of 14400, 12000, 9600, 7200, 4800, 2400 and 300 bps.

The R144HD is designed for use in Group 3 facsimile machines and is also compatible with Group 2 machines. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface, and standard connector simplify system design and allow installation in a compact enclosure. A proprietary V.33 short train feature provides faster connection time at the high speeds required for facsimile transmission.

FEATURES

- Compatibility:
  - — CCITT V.33, V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
  - — Trellis Coded Modulation (TCM) at 14400, 12000, 9600 and 7200 bps
  - — Short Train in TCM Configurations
- Group 3 and Group 2 Facsimile
- Half-Duplex (2-Wire)
- Programmable Tone Detection
- Programmable Dual/Single Tone Generation
- Dynamic Range: −43 dBm to 0 dBm; also available from −43 dBm to −6 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Transmit Output Level: +5 dBm ±1 dBm
- Small Size: 100 mm × 82 mm (3.94 in. × 3.23 in.)
- Power Consumption: 4.2W (Typical)
- TTL and CMOS Compatible

3



R144HD Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T.30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01%)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group 2 Identification (GI2)	1850
Group 2 Command (GC2)	2100
Group 2 Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462
MF1 Confirmation (CFR)	1080
MF1 Procedure Interrupt (PIS)	462

Carrier Frequencies

Function	Frequency (Hz ±0.01%)
T.3 (Group 2)	2100
V.27 ter, V.33, TCM96, TCM72	1800
V.29, (V.33, TCM96, TCM72)[1]	1700
1. Selectable option	

TONE GENERATION

Under control of the host processor, the R144HD can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Specification	Baud Rate (Symbols/Sec.)	Bits Per Baud	Data Rate (BPS) (±0.01%)	Symbol Points
V.33	2400	6	14400	128
V.33	2400	5	12000	64
TCM96	2400	4	9600	32
TCM72	2400	3	7200	16
V.29	2400	4	9600	16
V.29	2400	3	7200	8
V.29	2400	2	4800	4
V.27	1600	3	4800	8
V.27	1200	2	2400	4

DATA ENCODING

The R144HD data encoding conforms to CCITT recommendations V.33, V.29, and V.27 ter.

EQUALIZERS

The R144HD provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Amplitude Equalizer — The selectable compromise amplitude equalizer may be inserted into the transmit and/or receive paths under control of the transmit amplitude equalizer enable and the receive amplitude equalizer enable bits in the interface memory. The amplitude select bit controls which of two amplitude equalizers is selected.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for high speed data configurations.

TRANSMITTED DATA SPECTRUM

If neither the link amplitude nor cable equalizer is enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R144HD incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter, V.29, or V.33 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R144HD can adapt to received frequency error of up to ±10 Hz with less than a 0.2 dB degradation in BER performance. Group 2 carrier recovery capture range is 2100 ±30 Hz. The Group 2 receiver operates properly when the carrier is varied by ±16 Hz at a 0.1 Hz per second rate.

RECEIVE LEVEL

The receiver circuit of the R144HD satisfies all specified performance requirements for received line signal levels from −0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the R144HD provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50 ±3%.

TRANSMIT LEVEL

The transmitter output level defaults to +5 dBm ±1 dB at power on. When using the default transmit level and driving a 600 ohm load, the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load. The output level can be programmed from −1 dBm to −10 dBm by performing a RAM write operation.

TRANSMIT TIMING

In the transmit state, the R144HD provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 14400, 12000, 9600, 7200, 4800, 2400, or 300 Hz (±0.01%). In Group 2, DCLK tracks an external 10368 Hz clock. If the external clock input (XCLK) is grounded the Group 2 DCLK is 10372.7 Hz ±0.01%.
2. *Duty Cycle.* 50 ±3%

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

The selectable turn-on sequences of the R144HD are defined in the following table:

Turn-On Sequences

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.33	1393 ms	1598 ms
V.33 Short	142.5 ms	347.5 ms
TCM96	1393 ms	1598 ms
TCM96 Short	142.5 ms	347.5 ms
TCM72	1393 ms	1598 ms
TCM72 Short	142.5 ms	347.5 ms
V.29	253 ms	438 ms
V.27 4800 bps	708 ms	913 ms
V.27 2400 bps	943 ms	1148 ms
V.27 4800 Short	50 ms	255 ms
V.27 2400 Short	67 ms	272 ms
V.21 300 bps	≤14 ms	≤14 ms
Group 2	≤400 μs	≤400 μs

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 12 ms of remaining data and scrambled ones at 1200 baud or approximately 10 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.33, TCM96, TCM72, and V.29, the turn-off sequence consists of approximately 8 ms of remaining data and scrambled 1's followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{RTS}$ goes false. In Group 2 the transmitter turns off within 200 μseconds after $\overline{RTS}$ goes false.

CLAMPING

The following clamps are provided with the R144HD:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector ($\overline{RLSD}$).* $\overline{RLSD}$ is clamped off (squelched) during the time when $\overline{RTS}$ is on.
3. *Extended Squelch.* Optionally, $\overline{RLSD}$ remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the training sequence. Response time is 1393 ms for V.33 and TCM96, 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{CTS}$ turns on in 14 ms or less. In Group 2 $\overline{CTS}$ turns on in 400 μs or less.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

For V.33, TCM96, V.29 or V.27 ter, $\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, $\overline{RLSD}$ will not turn on.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD. The threshold levels are:

Greater than −43 dBm ($\overline{RLSD}$ on)
Less than −48 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R144HD is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

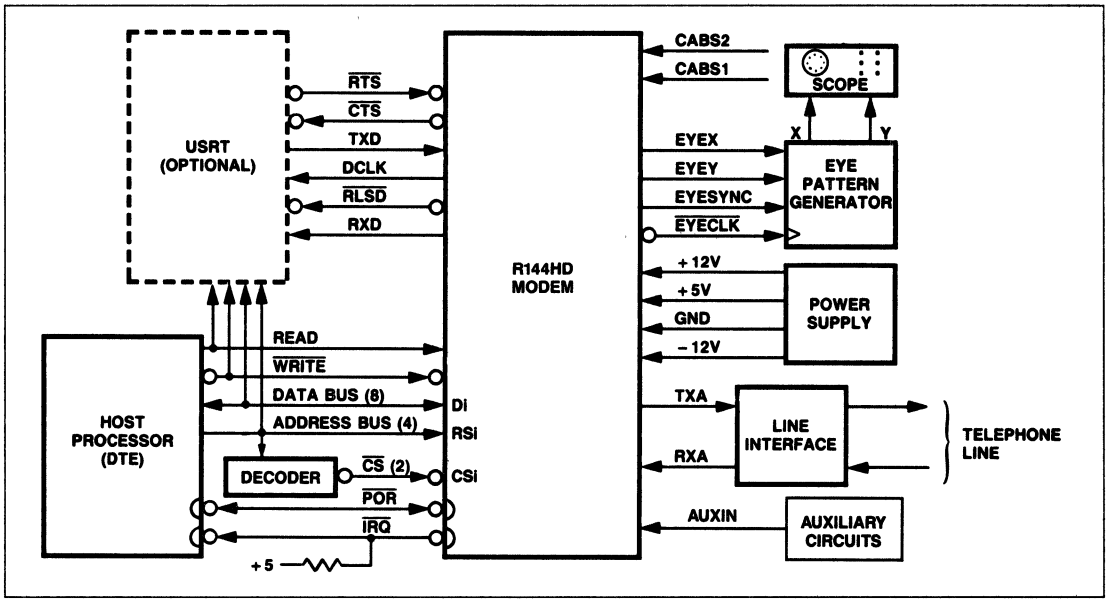
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the R144HD Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R144HD has the capability of transferring channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R144HD is configured by the host processor via the microprocessor bus.



R144HD Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in two rows of a 40-pin connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R144HD Hardware Circuits table; the table column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R144HD Hardware Supervisory Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground	GND	14, 39	Power Supply Return
+5 volts	PWR	3, 4	+5 volt supply
+12 volts	PWR	26	+12 volt supply
-12 volts	PWR	37	-12 volt supply
$\overline{POR}$	I/OB	36	Power-on-reset

R144HD Hardware Circuits (Continued)

Name	Type	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	7	Data Bus (8 Bits)
D6	I/OA	5	
D5	I/OA	9	
D4	I/OA	31	
D3	I/OA	15	
D2	I/OA	28	
D1	I/OA	23	
D0	I/OA	29	
RS3	IA	30	Register Select (4 Bits) Select Reg. 0-F
RS2	IA	8	
RS1	IA	27	
RS0	IA	10	
$\overline{CS0}$	IA	6	Chip Select Sample Rate Device
$\overline{CS1}$	IA	18	Chip Select Baud Rate Device
$\overline{READ}$	IA	1	Read Enable
$\overline{WRITE}$	IA	2	Write Enable
$\overline{IRQ}$	OB	32	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	13	Data Clock
XCLK	IB	22	External Clock for Group II
$\overline{RTS}$	IB	19	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	20	Transmitter Data
RXD	OC	21	Receiver Data
$\overline{RLSD}$	OC	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IB	33	Cable Select 1
CABS2	IB	34	Cable Select 2

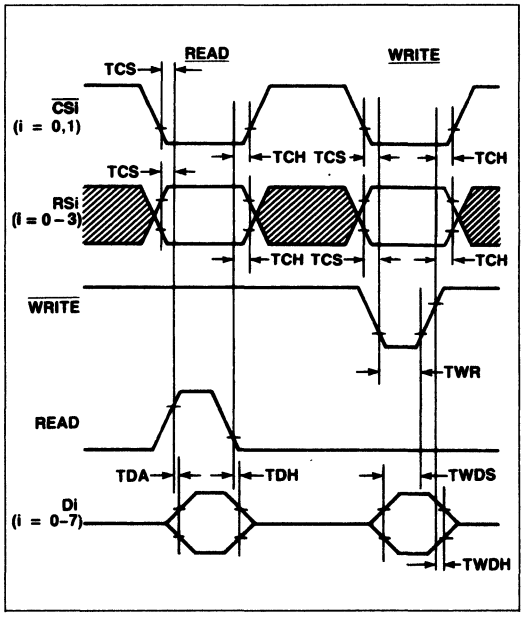
R144HD Hardware Circuits (Continued)

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXA	AA	38	Transmitter Analog Output
RXA	AB	40	Receiver Analog Input
AUXIN	AC	35	Auxiliary Analog Input
F. DIAGNOSTIC:			
EYEX	OC	24	Eye Pattern Data — X Axis
EYEY	OC	25	Eye Pattern Data — Y Axis
EYECLK	OA	11	Eye Pattern Clock
EYESYNC	OA	12	Eye Pattern Synchronizing Signal
Note: Unused inputs tied to +5V or ground require individual 10K Ω series resistors.			

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the EYECLK output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

Microprocessor Timing



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
CSi, RSi setup time prior to Read or Write	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
CSi, RSi hold time after Read or Write	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

Cable Equalizer Selection

Cable Equalizer Selection

CABS 2	CABS 1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Digital Interface Characteristics

The digital interface characteristics are listed in the table on the following page.

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The Transmitter Analog output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The Receiver Analog input impedance is 46.4K ohms ±23% or 23.2K ohms ±23% for dynamic range of −43 dBm to 0 dBm or −43 dBm to −6 dBm, respectively.
AUXIN	AC	The Auxiliary Analog input allows access to the transmitter by user-provided equipment. Because this signal is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −0.4 dB ±1 dB. If not used, this input should be grounded.

SOFTWARE CIRCUITS

The R144HD comprises three signal processor chips. Two of these chips contain 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Register in chip 0 update at the modem sample rate (9600 bps). Registers in chip 1 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0–F), and the bit by Q(0–7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type						
			IA	IB	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V			2.4 min.[1]			2.4 min.[1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V			0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.					±12.5 max.[4]	
I_{OH}	Output Current, High	mA			−0.1 max.				
I_{OL}	Output Current, Low	mA			1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA				±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5				10	40
C_D	Capacitive Drive	pF			100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

Status/Control Bits

The operation of the R144HD is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a '—' are reserved for modem use only and must not be changed by the host.

NOTE: The host must wait a minimum of 1 μs between successive writes to interface memory.

RAM Data Access

The R144HD provides the user with access to much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register 0:F (RAM ACCESS S) or 1:F (RAM ACCESS B). The R144HD RAM Access Codes table lists access codes for storage in registers 0:F or 1:F and the corresponding diagnostic functions. The R144HD Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long.

These bits are written into interface memory registers 0:3, 0:2, 0:1 and 0:0, or 1:3, 1:2, 1:1 and 1:0, in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit 0:5:5 (RAMWS) or bit 1:D:0 (RAMWB) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM in chip 0 or in chip 1, respectively. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the most significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAM Access B bits of register 1:F for chip 1, or by means of 0:5:4 (RAE) for chip 0. When bit 1:F:7 or 0:5:4 is set to one, the XRAM is selected. When 1:F:7 or 0:5:4 equals zero, YRAM is selected.

When the host reads or writes register 0, the modem resets the modem data available bit, 0:E:0 or 1:E:0 (MDAi), to a zero. When the modem reads or writes register 0, the modem sets the MDAi bit to a one. If an Interrupt Enable bit, 0:E:2 or 1:E:2 (IEi), is set to a one by the host and the corresponding MDAi bit is set, the $\overline{IRQ}$ output is asserted and the associated Interrupt Active bit, 1:E:7 or 0:E:7 (IAi), is set to a one by the modem.

NOTE: When writing to registers 1 and 0, the host must first write to register 1, then to register 0.

The default access codes are 28 for 1:F and 00 for 0:F, which allows data in registers 1:3 and 1:1 to be presented serially on EYEX and EYEY, respectively.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

RAM Access Codes

No.	Function	Access	RAE	Chip	Read Reg. No.
1	Received Signal Samples	40	X	0	2,3
2	Demodulator Output	52	X	0	0,1,2,3
3	Low Pass Filter Output	54	X	0	0,1,2,3
4	Average Power	5C	X	0	2,3
5	AGC Gain Word	3E	X	0	2,3
6	Tone 1 Frequency	71	1	0	2,3
7	Tone 1 Level	72	1	0	2,3
8	Tone 2 Frequency	71	0	0	0,1
9	Tone 2 Level	72	0	0	0,1
10	Output Level	7F	0	0	0,1
11	Checksum, Chip 0	3F	X	0	0,1
12	Checksum, Chip 1	7F		1	0,1
13	Equalizer Input	40		1	0,1,2,3
14	Equalizer Tap Coefficients	02-27		1	0,1,2,3
15	Unrotated Equalizer Output	74		1	0,1,2,3

Ram Access Codes (Continued)

No.	Function	Access	RAE	Chip	Read Reg. No.
16	Rotated Equalizer Output (Received Point—Eye Pattern)	28		1	0,1,2,3
17	Decision Points (Ideal)	68		1	0,1,2,3
18	Error Vector	69		1	0,1,2,3
19	Rotation Angle	00		1	0,1
20	Frequency Correction	AE		1	2,3
21	EQM	B1		1	2,3
22	G2 Base Band Signal	C8		1	2,3
23	G2 AGC Gain Word	AD		1	2,3
24	G2 AGC Slew Rate	AA		1	2,3
25	G2 PLL Frequency Correction	C2		1	2,3
26	G2 PLL Slew Rate	EF		1	2,3
27	G2 Black/White Threshold	6A		1	0,1
28	G2 Phase Limit	F1		1	2,3

RAE = X is don't care since this location should only be read from, and *not* written to, by the host.

3

R144HD Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	RAMWS	RAE	EPT	SQEXT	—	V33S
4	CONFIGURATION							
3	RAM DATA XSM; FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).

R144HD Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	—	—	—	—	IE1	—	MDA1
D	—	TLE	RLE	J3L	—	—	FRT	RAMWB
C	—	—	—	—	—	—	—	G2FGC
B	FR3	FR2	FR1	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	—
4	—	—	—	—	—	$\overline{P2DET}$	—	—
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).

R144HD Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1:7:0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present. $\overline{\text{CDET}}$ goes to zero at the end of a training sequence, and returns to one at the end of the received signal. $\overline{\text{CDET}}$ will not go to zero if the training sequence is not detected. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
(None)	Configuration	0:4:0–7	The host processor configures the R144HD by writing a control code into the configuration register in the interface memory space. (See SETUP) ***Configuration Control Codes*** Control codes for the R144HD configurations are: **Configuration** — **Configuration Code (HEX)** V.33 14400[1] — 31 V.33 12000 — 32 TCM96 9600 — 34 TCM72 7200 — 38 V.33 14400 (1700 Hz)[2] — 71 V.33 12000 (1700 Hz)[2] — 72 TCM96 9600 (1700 Hz)[2] — 74 TCM72 7200 (1700 Hz)[2] — 78 V.29 9600 — 14 V.29 7200 — 12 V.29 4800 — 11 V.27 4800 Long — 0A V.27 2400 Long — 09 V.27 4800 Short — 8A V.27 2400 Short — 89 FSK — 20 Group 2 — 40 Single Tone Transmit — 80 Dual Tone — 81 [1] Default at POR. [2] The 1700 Hz carrier frequency is non-standard. ***Configuration Definitions*** 1. *V.33.* When a V.33 configuration has been selected, the modem operates as specified in CCITT Recommendation V.33. 2. *TCM96 and TCM72.* When configuration TCM96 or TCM72 is selected, the training sequence is defined by V.33 and the modulation trellis coded is defined by V.32 (32 or 16 point constellation). 3. *V.29.* When a V.29 configuration has been selected, the modem operates as specified in CCITT Recommendation V.29. 4. *V.27.* When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 5. *FSK.* The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system. 6. *Group 2.* The modem operates as a CCITT T.3 compatible AM modem. This permits transmission to and reception from Group 2 facsimile apparatus. A carrier frequency of 2100 Hz is used. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black. When in the receive state, the R144HD recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal. This allows a baseband of 3400 Hz to be recovered. The recovered baseband signal is available on the microprocessor bus. The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number. This number may be changed by the user.

R144HD Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>Receiver data is presented to the RXD output at a rate of 10368 samples per second. The user should strobe the data on the rising edge of the data clock (DCLK). A logical 1 level (high voltage) represents white. A logical 0 level (low voltage) represents black.

7. Single Tone Transmit. In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%.

8 Dual Tone Transmit. In this configuration, activating RTS causes the modem to transmit two tones at frequencies and output levels specified by the user. By using the RAM Data Access routines, the user can program the tones and levels.</td></tr>
<tr><td>EPT</td><td>Echo Protector Tone</td><td>0:5:3</td><td>If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. This option is available in V.33, V.29, and V.27 configurations, although it is not specified in the CCITT V.33 or V.29 recommendations.</td></tr>
<tr><td>$\overline{\text{FED}}$</td><td>Fast Energy Detector</td><td>1·5:6</td><td>The zero state of $\overline{\text{FED}}$ indicates energy is present above the receiver threshold in the passband. $\overline{\text{FED}}$ is not used for Group 2 Facsimile.</td></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0–7,
0:3:0–7</td><td>The host processor conveys single tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below.

FREQM Register (0:3)
<table><tr><td>Bit:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr></table>
FREQL Register (0:2)
<table><tr><td>Bit:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr></table>
The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%.

Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below:

<table><tr><th>Frequency (Hz)</th><th>FREQM</th><th>FREQL</th></tr><tr><td>462</td><td>0C</td><td>52</td></tr><tr><td>1100</td><td>1D</td><td>55</td></tr><tr><td>1650</td><td>2C</td><td>00</td></tr><tr><td>1850</td><td>31</td><td>55</td></tr><tr><td>2100</td><td>38</td><td>00</td></tr></table></td></tr>
<tr><td>FRT</td><td>Freeze Taps</td><td>1·D·1</td><td>When FRT is a one, adaptive equalization taps are prevented from changing while in data mode.</td></tr>
<tr><td>FR1–FR3</td><td>Frequency 1,2,3</td><td>1·B·5,6,7</td><td>The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for FR1, FR2 and FR3 are:

<table><tr><th>Bit</th><th>Frequency (Hz)</th></tr><tr><td>FR1</td><td>2100</td></tr><tr><td>FR2</td><td>1100</td></tr><tr><td>FR3</td><td>462</td></tr></table></td></tr>
<tr><td>G2FGC</td><td>Group 2 Fast Gain Control</td><td>1:C:0</td><td>The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group 2 Facsimile.</td></tr>
<tr><td>IA1</td><td>Interrupt Active (One)</td><td>1:E:7</td><td>IA1 is a one when Chip 1 is driving $\overline{\text{IRQ}}$ to zero volts.</td></tr>
<tr><td>IA0</td><td>Interrupt Active (Zero)</td><td>0·E.7</td><td>IA0 is a one when Chip 0 is driving $\overline{\text{IRQ}}$ to zero volts.</td></tr>
</table>

R144HD Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the MDA0 bit is a one.
IE1	Interrupt Enable (One)	1:E:2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the MDA1 bit is a one.
J3L	Japanese 3 Link	1:D:4	The one state of J3L selects this standard for link amplitude equalizer. The zero state of J3L selects U.S. survey long.
MDA0	Modem Data Available (Zero)	0:E:0	MDA0 goes to one when the modem reads or writes register 0:0. MDA0 goes to zero when the host processor reads or writes register 0:0. MDA0 is used for parallel mode as well as for diagnostic data retrieval.
MDA1	Modem Data Available (One)	1:E:0	MDA1 goes to one when the modem writes register 1:0. MDA1 goes to zero when the host processor reads register 1:0.
PDM	Parallel Data Mode	0:F:7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.
$\overline{PNDET}$	Period 'N' Detector	1:7:6	The zero state of $\overline{PNDET}$ indicates a PN sequence has been detected. $\overline{PNDET}$ sets to a one at the end of the PN sequence, except for V.33, TCM96 and TCM72. $\overline{PNDET}$ sets to a one at the end of the rate sequence (PR) in these modes.
$\overline{P2DET}$	Period '2' Detector	1:4:2	The zero state of $\overline{P2DET}$ indicates a P2 sequence has been detected. $\overline{P2DET}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1:F:0 – 7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Access S	0:F:0 – 6	Contains the RAM access code used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XBL	1:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XBM	1:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XSL	0:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XSM	0:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data YBL	1:0:0 – 7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device). See MDA1.
(None)	RAM Data YBM	1:1:0 – 7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Data YSL	0:0:0 – 7	Least significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device). Shared by parallel data mode for presenting channel data to the host microprocessor bus. See Transceiver Data and MDA0.
(None)	RAM Data YSM	0:1:0 – 7	Most significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device).
RAE	RAM Address Extension	0:5:4	This bit is an extension of RAM Access S when RAMWS is a one. When RAE is a one, the XRAM in Chip 0 is selected for a RAM write operate, and when a zero the YRAM is selected.
RAMWB	RAM Write Chip 1 (baud rate device)	1:D:0	RAMWB is set to a one by the host processor when performing diagnostic writes to the baud rate device (Chip 1). RAMWB is set to a zero by the host when reading RAM diagnostic data from Chip 1.
RAMWS	RAM Write Chip 0 (sample rate device)	0:5:5	RAMWS is set to a one by the host processor when performing diagnostic writes to the sample rate device (Chip 0). RAMWS is set to a zero by the host when reading RAM diagnostic data from Chip 0.
RLE	Receiver Link Equalizer	1:D:5	The one state of RLE enables the link amplitude equalizer in the receiver.
RTS	Request-to-Send	0:5:7	The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed. RTS parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are "ORed" by the modem.

R144HD Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>SETUP</td><td>Setup</td><td>0:E:3</td><td>The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for the equalizer (0:5:1). SETUP returns to zero when acted on by the modem. The time required for the SETUP bit to cause a change depends on the current state of the modem. The following table lists worst case delays.
<table>
<tr><th>Current State</th><th>V.21</th><th>G11</th><th>High Speed Receiver</th><th>High Speed Transmitter</th></tr>
<tr><td>DELAY</td><td>14 ms</td><td>400 µs</td><td>2 BAUD</td><td>2 BAUD + TURNOFF Sequence + Training (if applicable) + SQUELCH (if applicable)</td></tr>
</table></td></tr>
<tr><td>SQEXT</td><td>Squelch Extend</td><td>0:5:2</td><td>The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.</td></tr>
<tr><td>TDIS</td><td>Training Disable</td><td>0:5:6</td><td>If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one prior to $\overline{RTS}$ going on, the generation of a training sequence is prevented at the start of transmission.</td></tr>
<tr><td>TLE</td><td>Transmitter Link Equalizer</td><td>1:D:6</td><td>The one state of TLE enables the link amplitude equalizer in the transmitter.</td></tr>
<tr><td>V33S</td><td>V.33 Short Train</td><td>0:5:0</td><td>Setting this bit allows the modem to retrain in 142.5 ms if the modem has previously trained in the V.33, TCM96, or TCM72 long train configurations. This bit must be reset before changing configurations, unless the new configuration is V.33, TCM96, TCM72 or FSK.

Once the modem has long trained in V.33, TCM96 or TCM72, it can short train in any of these configurations. Short train is also possible if the modem long trains, reconfigures to FSK with the short train bit set, and then reconfigures again to V.33, TCM96, or TCM72.</td></tr>
<tr><td>(None)</td><td>Transceiver Data</td><td>0:0:0–7</td><td>In receive parallel data mode, the modem presents eight bits of channel data in register 0:0 for reading by the host microprocessor. After the eight bits have been accumulated in register 0:C they are transferred to 0:0 and bit 0:E:0 goes to a one. When the host reads 0:0, bit 0:E:0 resets to a zero. The first bit of received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync characters. Bit 0:E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations.

In transmit parallel data mode the host stores data at location 0:0. This action causes bit 0:E:0 (MDA0) to reset to a 0. When the modem transfers the data from 0:0 to 0:2 bit 0:E:0 sets to a 1. The data is serially transmitted from register 0:2 least significant bit first. Received data is shifted into register 0:C from MSB toward LSB.</td></tr>
</table>

POWER-ON INITIALIZATION

When power is applied to the modem, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is repeated.

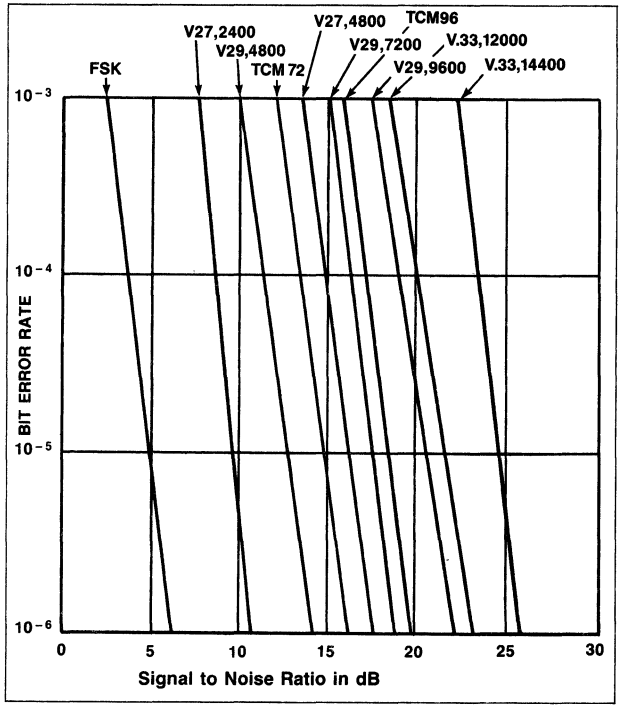
At POR time the modem defaults to the following configuration: V.33/14400 bps, serial mode, training enabled, no echo protector tone on, no extended squelch, interrupts disabled, no link equalizer, RAM Access B code 28.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 µsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of – 20 dBm, except for TCM72; V.29, 4800; and V.27, which are measured at a received line signal level of – 30 dBm.

The BER curves shown below were prepared from data obtained using a TAS 1000 communication test system.



Typical Bit Error Rate (Back-to-Back)

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	750 mA	800 mA
+12 Vdc	±5%	5 mA	10 mA
−12 Vdc	±5%	30 mA	50 mA

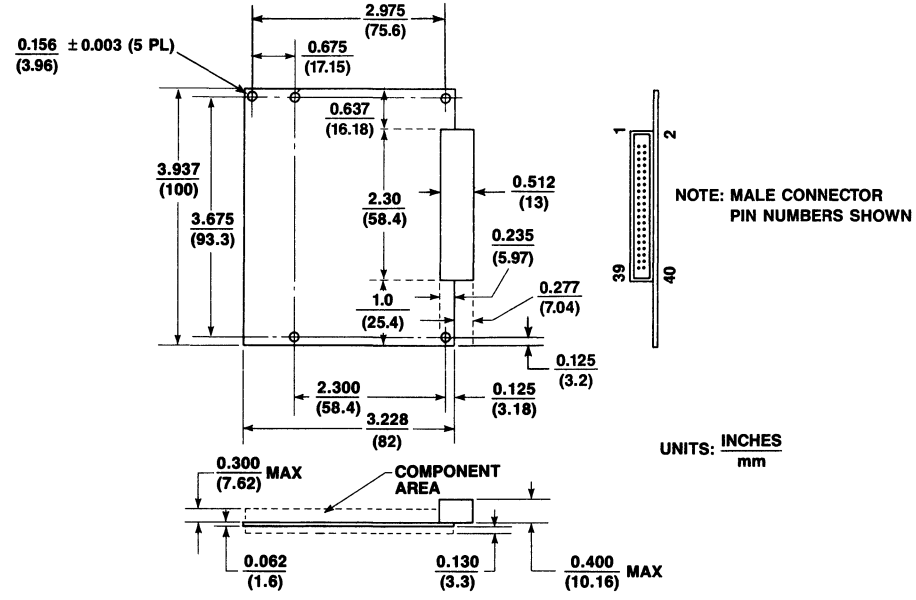
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature	
Operating	0°C to +70°C (32°F to 158°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins. Hirose HIF3F-40PA-2 5DS (male) or HIF3HA-40DA-2.54DSA (female), or equivalent mating connector.
Dimensions	
Width	3.937 in. (100 mm)
Length	3.228 in. (82 mm)
Component Height (max)	0.300 in. (7.62 mm) above, 0.130 in. (3.3 mm) below
Connector Height	0.400 in. (10.16 mm)
Weight (max)	3.6 oz. (100 g)



R144HD Dimensions and Pin Locations

SECTION 4
Data Modem Application Notes

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DIGITAL NETWORKS

T-1/ISDN SOLUTIONS

Rockwell's expanding line of digital network products provide a solid foundation for integrating voice and data. These products are the system building blocks for central office, customer premises and local area networks equipment. Applications for Rockwell's digital devices include channel banks, multiplexers, PBX, host computers, front-end processors and LANS gateways/bridges.

Rockwell offers systems designers of OEM equipment a total solution for the Physical and lower half of the Link Layer of the ISO/ISDN model. This "plug-in" solution allows OEM manufacturers the opportunity and the affordability to be in the T-1/ISDN market. In addition, these devices offer a high level of integration to help designers build a T-1 interface rapidly with considerable space and component savings, coupled with higher performance design and throughput.

The R8069 Line Interface Unit (LIU) features programmable line equalization, clock recovery for slave operation and meets AT&T Pub. 62411 specifications. The R8070 T-1/PCM-30 Transceiver offers TX and RX functions in a single chip and meets CEPT PCM-30, T-1 D4 and ESF formats with or without clear channel. In addition, the R8070 has B8ZS and HDB3 on-board. The R8071 supports ISDN and DMI data modes, ISDN signalling, has on-board buffer memory management and provides 32 full-duplex channels with HDLC formatting.

Future high speed digital network devices include the R8075 which adds the CRC-4 error checking capability that is required by CCITT for PCM-30. The RT9170 is an advanced T-1 transceiver with microprocessor interface and facility data link capabilities. These devices are a part of Rockwell's ongoing commitment to digital connectivity and ISDN.

Substantial support is provided to demonstrate the use of these highly integrated devices. Evaluation boards are available for the R8069, R8070 and R8071. These boards are a platform to show the performance, capabilities and functionality of the devices either singly or together to implement a high speed digital interface.

Rockwell's series of communication controllers provide fast execution speed and may interface with a variety of 68000 I/O and memory devices. The R68C560/61 Multi-Protocol Communications Controller (MPCC) operates up to 4 Mbits/sec and supports all major communications protocols. It is available to work with either a 16-bit or 8-bit bus and can be adapted to function with essentially any of today's more common busses.

The R68C552 Dual Asynchronous Interface Adapter (DACIA) provides an easily implemented, programmed controlled interface between 16-bit microprocessor-based systems and serial communications data sets and modems.

The R68802 Local Area Network Controller (LNET) is a universal CSMA/CD controller which is designed to support a variety of local network designs. The device can interface data terminal equipment to local networks with differing performance requirements.

Rockwell

An R6500/11 — R2424 Intelligent Modem Design

by Ron Collins and Joseph W. Hance
Product Applications Engineers
Semiconductor Products Division, Newport Beach, California

INTRODUCTION

The combination of single chip microcomputers and standard modems makes possible the implementation of sophisticated and flexible telecommunications systems. The intelligent modem has become the standard for personal microcomputers and provides access to many outside resources over standard telephone lines.

This application note describes the hardware and software design of a 300/1200/2400 bit-per-second (bps) modem based on the Rockwell R2424 single board modem and the R6500/11 single-chip microcomputer. The system design minimizes the number of devices used and provides the user adequate room for special features. The software implements the industry standard "AT" command set so that compatibility with commercial software packages is provided. This particular design is that of a stand-alone "Box Modem" but only minimal changes are needed in the configuration for a personal computer bus compatible modem.

HARDWARE DESIGN

The hardware used in this design (see the schematic in Figure 1) consists of an R6500/11 microcomputer (Z1), an R2424DC modem module (Z3), and a 16L8 type PAL (Z2). A complete parts list is tabulated in Table 1.

The R6500/11 controls the system and implements the high level command protocol. It has an internal UART which provides communications between the host computer and the modem. The R2424DC module is addressed as a peripheral on the abbreviated bus of the R6500/11. All modem configuration, dial, status, and commands are transmitted over the data bus. The serial interface to the R2424DC carries only the data transmitted or received over the telephone line.

Table 1. R6500/11—R2424 Intelligent Modem Parts List

Item	Part	Qty	Description
1	P1	1	RS-232C Connector, Female, DB-25
2	R1	1	4.7K Resistor, 5%
3	R2	1	3K Resistor, 5%
4	R3	1	3K Resistor, 5%
5	Y1	1	1.8432 MHz Crystal
6	Z1	1	R6500/11 Single-chip Microcomputer
7	Z2	1	PAL 16L8
8	Z3	1	R2424DC Modem Board
9	Z4	1	MC1488
10	Z5	1	MC1488
11	Z6	1	MC1489

The PAL* generates the proper bus control signals needed to interface the R2424DC to the R6500/11's bus. It also allows the R6500/11 to switch the serial data between the host and the line to accommodate the command and on-line modes. The 1488's (Z4, Z5) and the 1489 (Z6) provide a standard RS-232-C interface for the host computer. These devices would not be necessary in the design of a plug-in personal computer modem. Figure 2 shows the logic equivalent of the 16L8 PAL and Figure 3 shows the PALASM equations used to program the PAL.

SOFTWARE DESIGN

The Functional State diagram for the software is shown in Figure 4. An assembly listing of the program is included at the end of this application note. Notes are liberally included in the listing to assist the understanding of program operation. (Figure 7).

Note: In the discussion of the software and operation of this design, it is assumed the reader knows and understands the common "AT" commands. If not, refer to any of a number of source materials devoted to this subject.

There are five main sections to this program. In order of occurrance in the listing, they are:

Part 1: Baud rate and protocol determination	($F800–$F998)
Part 2: Reading in the command string	($F999–$F9E8)
Part 3: Processing the command string	($F9E9–$FA1B)
Part 4: Command definitions	($FB1E–$FEBA)
Part 5: Interrupt Service Routine	($FF57–$FF79)

Most of the software operates in the Command Mode, responding to inputs from the host system. The Command Mode section includes Parts 1–5, with the exception of the <CR> (Carriage Return) command in Part 4. The remaining sections of Figure 4 lie within the definition of the <CR> command. Figure 5 shows the flow chart of the Command Mode section.

After initialization, the software loops in Part 1, waiting for an attention code ("AT" or "A/") or for the phone to ring. Any system designed to run the "AT" command set must be able to operate at either 300 or 1200 (or, in this case, 2400) baud, using 7 or 8 bits per word, with even, odd or no parity, switching from one mode to another automatically. The method used to do this is outlined on page 0004 of the software listing, Figure 7. Figure 6 diagrams the bit patterns of the characters "A", "T" and "/" and shows how the relationship of bits 8 and 9 of each character determine the characteristics of the serial protocol.

**PAL and PALASM are registered trademarks of Monolithic Memories, Inc.*

In Part 2 the serial communications protocol as been established. ASCII command characters are read in one at a time and stored in a buffer (INBUFF), excepting <SPACE> and non-<CR> control characters, until a <CR> character is entered. Should more than 40 characters be received, a flag (BUFFLG) is set, indicating an error condition.

When the program recognizes a <CR> character it stops accepting commands and goes directly to command execution (Part 3). It processes each command in sequence until an "A", "O", "Z" or <CR> command. "A" and "O" forces an attempt to go on-line (examine RSLD/ for carrier signal and go on-line if present, otherwise it will go back to Command Mode.) "Z" performs a soft reset and returns to Command Mode. <CR> is the usual end to each command string. This is where error conditions are reported, on-line data are handled, and a return to Command Mode from Data Mode is made upon recognition of a valid escape code sequence.

This intelligent modem will recognize that it is being called only while it is waiting for an attention code (at label L1). If the PA0 flag goes high at this point, indicating the phone is "ringing", the program branches to RING then jumps to RINGNG, where a determination is made whether to answer the phone or not. If not ringing, it goes back to waiting for "AT" or "A/". If it is ringing, it then bypasses Part 2 and Part 3 and attempts to go to the Data Mode (depending on presence of a carrier signal) by executing the "A" (Answer) command.

When this modem is called, an assumption is made as to the proper baud rate and serial protocol, that the values determined by the most recent attention code are still valid. Should a call be received before the first attention code was entered, it defaults to 1200 baud, 8 bits, no parity. The call is not answered in this case, since S0 was not set to a non-zero value, however, the "RING" message is sent out to the host system at this rate.

Part 4 comprises the coding of each "AT" command. All but AAA, OOO, ZZZ and CR end in an RTS instruction, returning control back to the command string processor at NXTCMD. AAA and OOO transfer control directly to CR in an attempt to go on-line. CR always returns to Part 1 of the program, and ZZZ always jumps to the Power-On-Reset address at RESET.

Part 5 is divided into two parts: signal processing and delay timing (execution of one or the other is determined by the value of the INTFLG flag). The signal processing takes place while waiting for an attention code, echoing (if enabled) the incoming bits back to the host system, and is described on page 0004 of Figure 7. Delay timing is selected just before Part 2 (or if a call is answered). The delay routine is designed to allow a variable number of precise time delays, where the actual time interval is determined by the routine needing the delay. For example, the "," (comma) command tells the modem to do nothing for S8 number of seconds, so one time interval would be 1 second. The Carrier Detect Response time interval is 1/10 second and the Escape Code Guard time interval is 20 ms, each requiring different values for CNTR-B and DELAYT.

General notes on the software:

Liberal use was made of the available RAM for 1-bit flags and variables, primarily because no premium is placed on RAM space in this design. These could be compressed into byte-sized entities should more space be required.

No attempt was made to provide status information via the S13, S14, S15 or S17 pseudo-registers. These could be added if necessary.

The S10 (Loss of Carrier) and S11 (Touch-Tone) delay times are limited to 400 ms and 70 ms, respectively, due to the design of the R2424 Modem.

The "H2" command does nothing additional to the "H1" command since the R2424 Modem does not have an auxiliary relay.

This program implements the concepts of modularity and structured programming as much as was practical for assembly-level code. This allows easy customization and tailoring for a particular application. There are deviations from this guideline, however, so modifications should be made with this in mind.

Expansion might include detection of Dial tone, Ringing and Busy signals using the TONE bit of RCV8. For example, if a Busy signal is detected, the program could automatically re-dial after a suitable delay time.

Unlike some commercial intelligent modems, no default switches or status LEDs were implemented in this design, nor was an actual speaker circuit included (though a control line for one, SPKR-ON/, is provided) in the interests of simplicity.

Finally, this design has not been thoroughly tested to meet the "AT" specifications. This application note is presented only as a guide on how to control a R2424 Modem with a R6500/11 single-chip microcomputer.

SERIAL INTERFACE

The modem system supports the following data rates and asynchronous serial protocols:

Baud: 300, 1200 or 2400
No. of data bits: 7 or 8
No. of stop bits: 1 or 2
Parity: Odd, even or none

The baud rate is determined by the width of the start bit.

The number of data bits, the number of stop bits and parity type are determined by examining bit 8 and, sometimes, bit 9 in two consecutive data words comprising an "AT" or "A/" command. Figure 6 shows the serial stream waveforms for the "AT" or "A/" commands along with the message bits positions. Table 2 lists the six selectable protocol configurations.

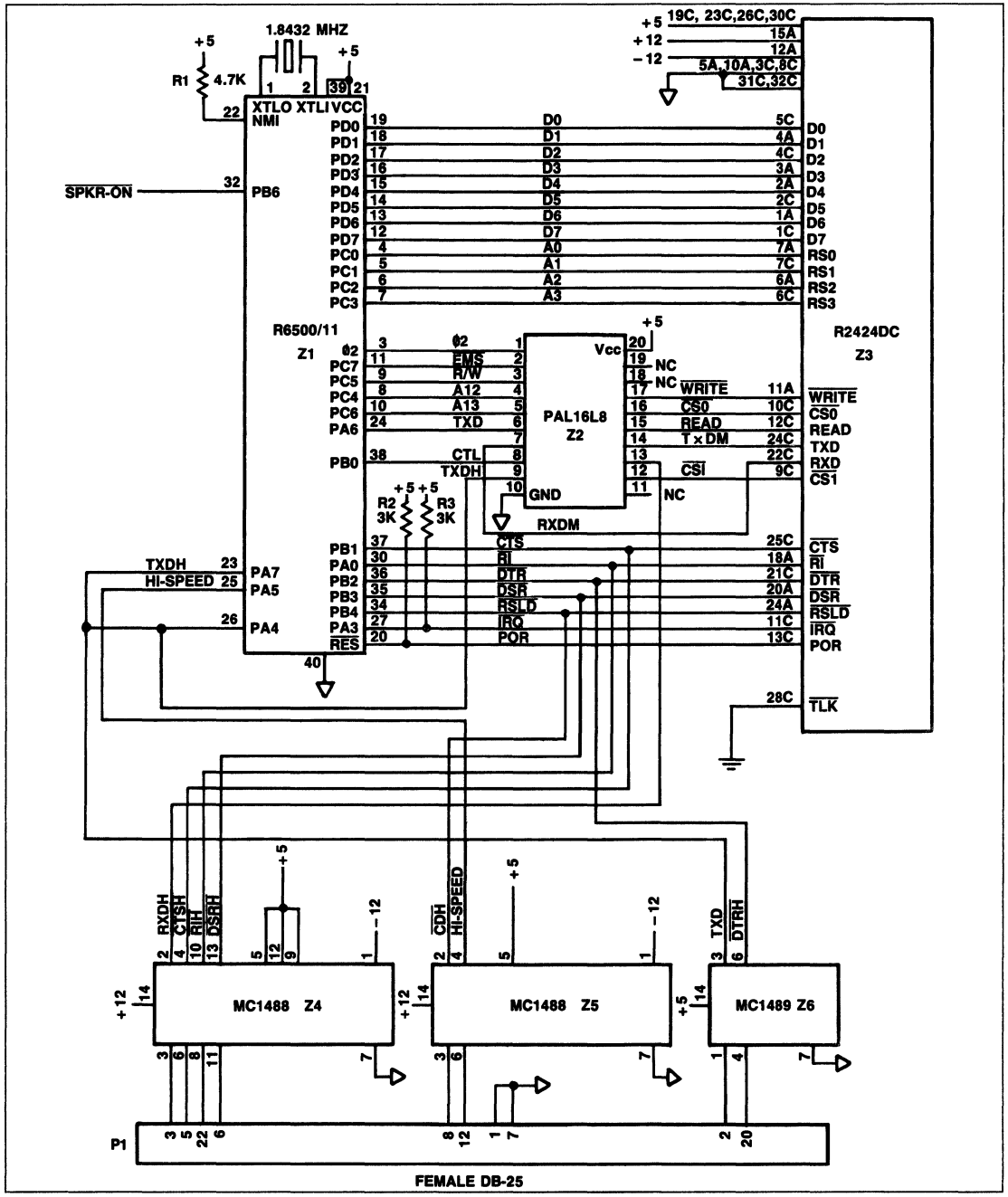

Figure 1. R6500/11-R2424 Intelligent Modem Schematic

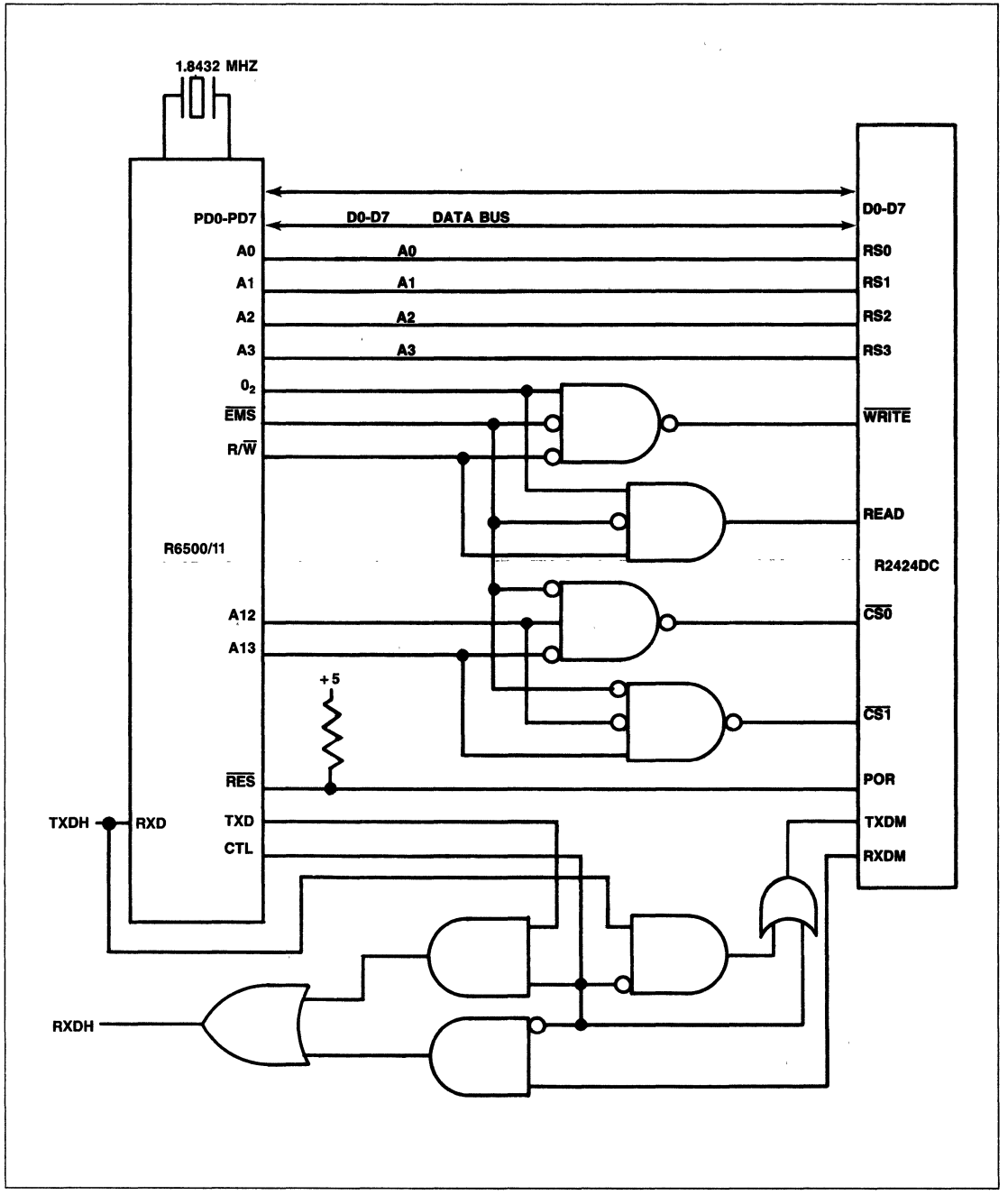

Figure 2. Logic for 16L8 PAL (Z2)

```
PAL16L8
MODEM
MODEM CONTROL CIRCUIT
JW HANCE
P2 EMS RW A12 A13 TXD RXDM CTL TXDH GND NC
/CS1 RXDH TXDM READ /CSO /WRITE NC NC VCC
IF (VCC) WRITE = P2 * /EMS * /RW
IF (VCC) /READ = /P2 + EMS + /RW
IF (VCC) CS0 = /EMS * A12 * /A13
IF (VCC) CS1 = /EMS * /A12 * A13
IF (VCC) /RXDH = /TXD * CTL + /TXD * /RXDM + /CTL * /RXDM
IF (VCC) /TXDM = /CTL * /TXDH
*END*
```

Figure 3. PAL16L8 (Z2) PALASM Equations

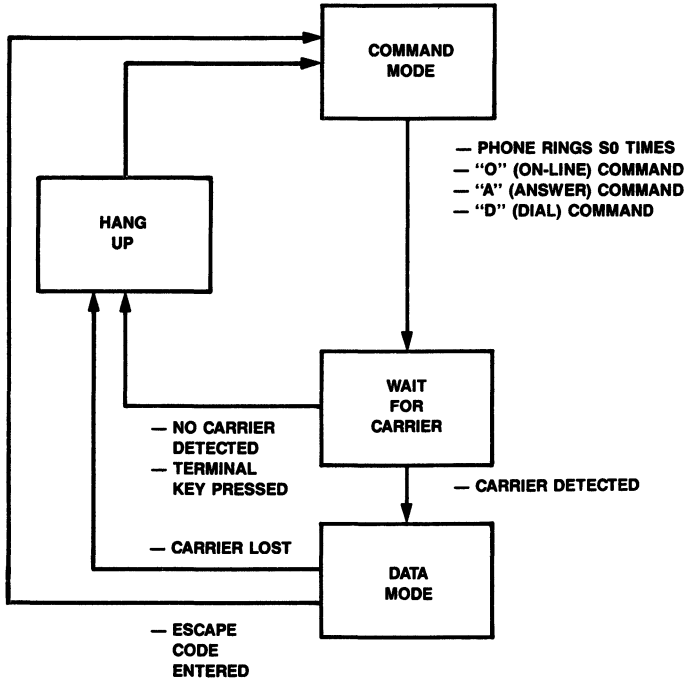

Figure 4. Modem Software Functional State Diagram

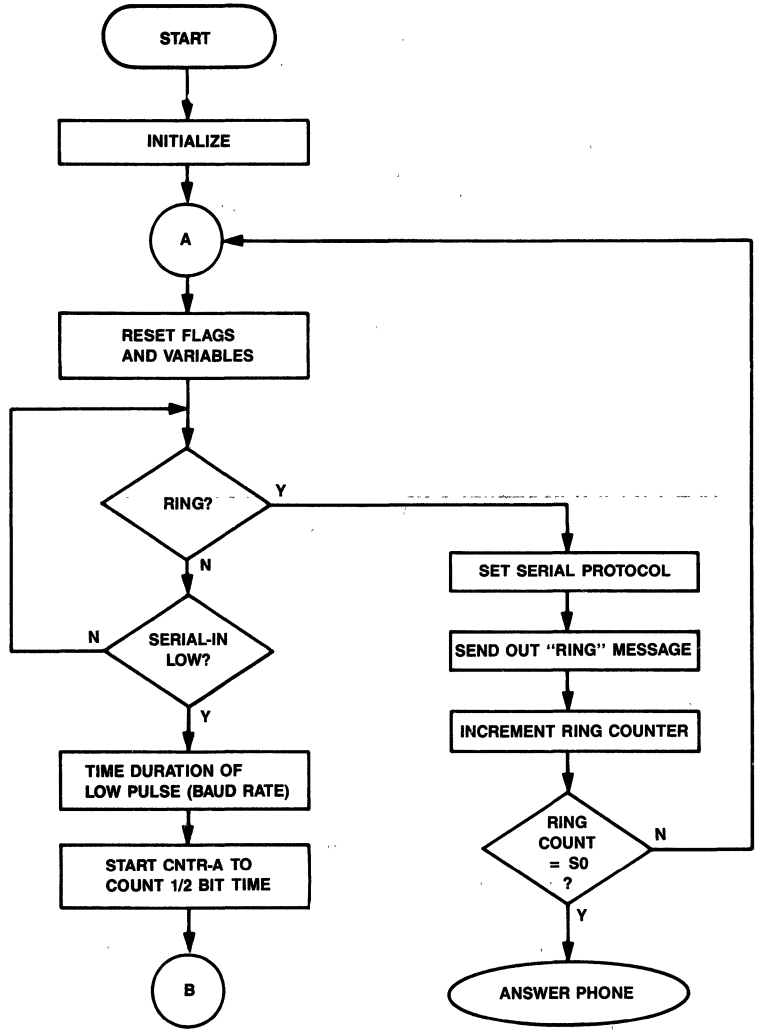

Figure 5. Command Mode Flowchart

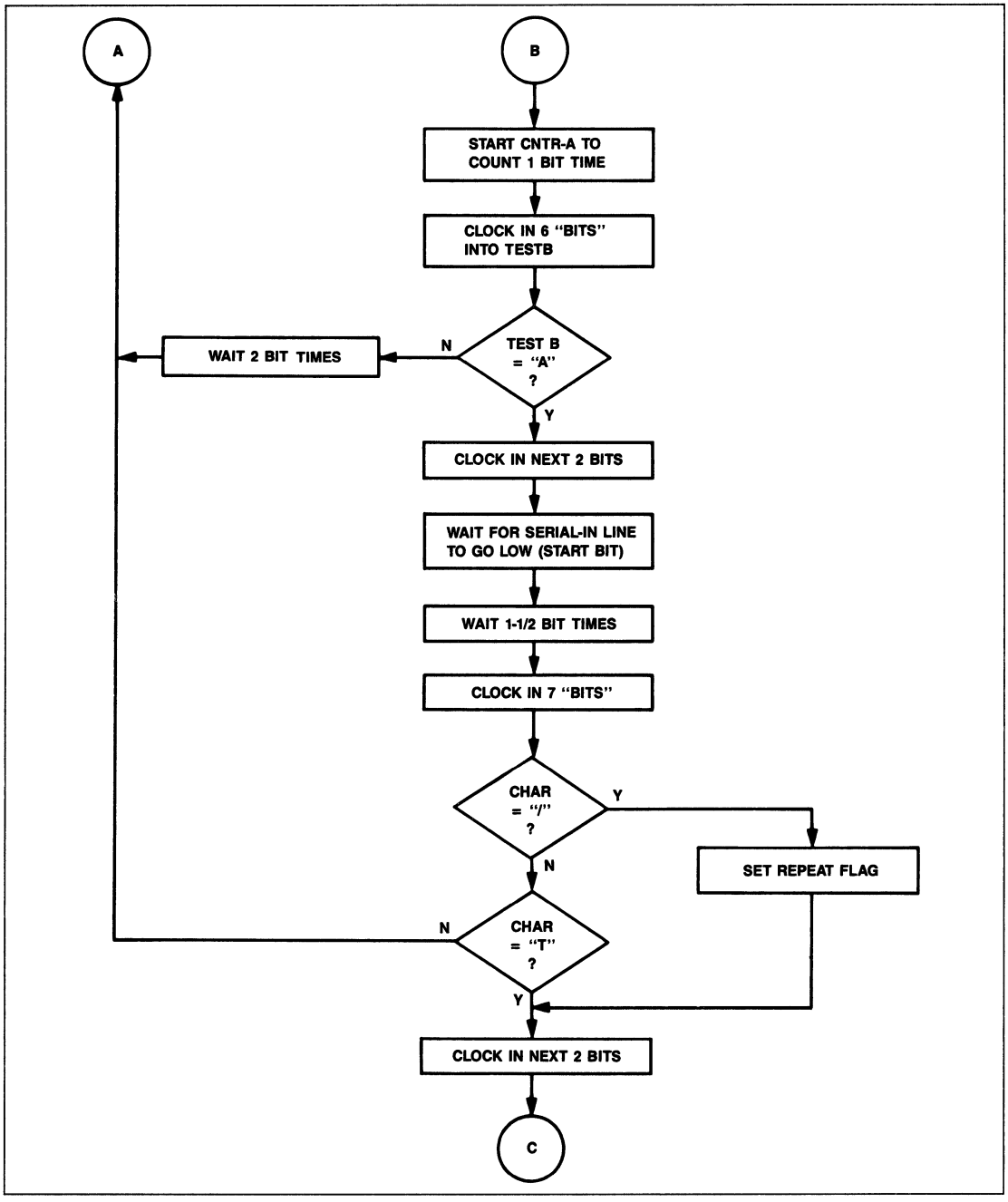

Figure 5. Command Mode Flowchart (Continued)

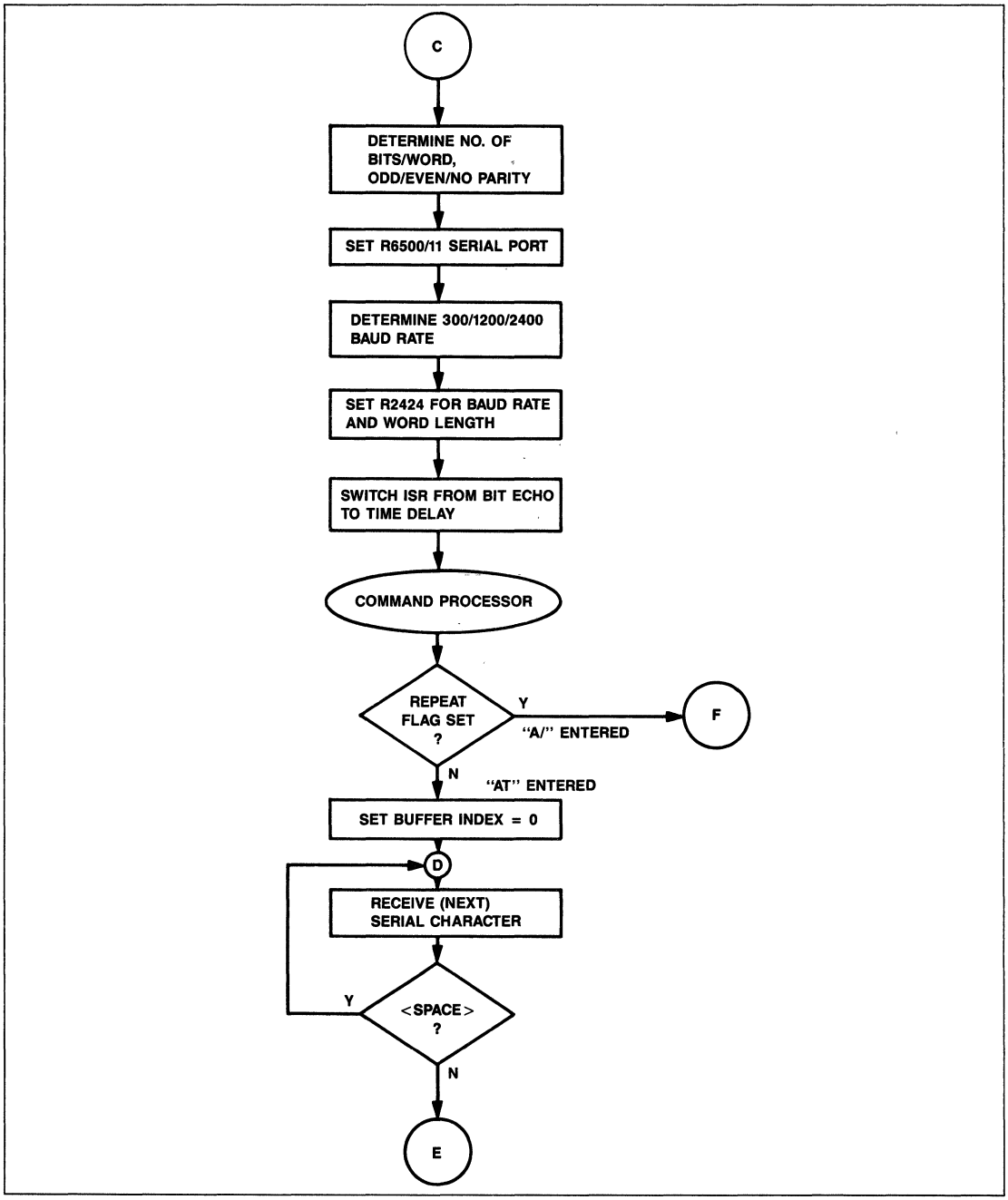

Figure 5. Command Mode Flowchart (Continued)

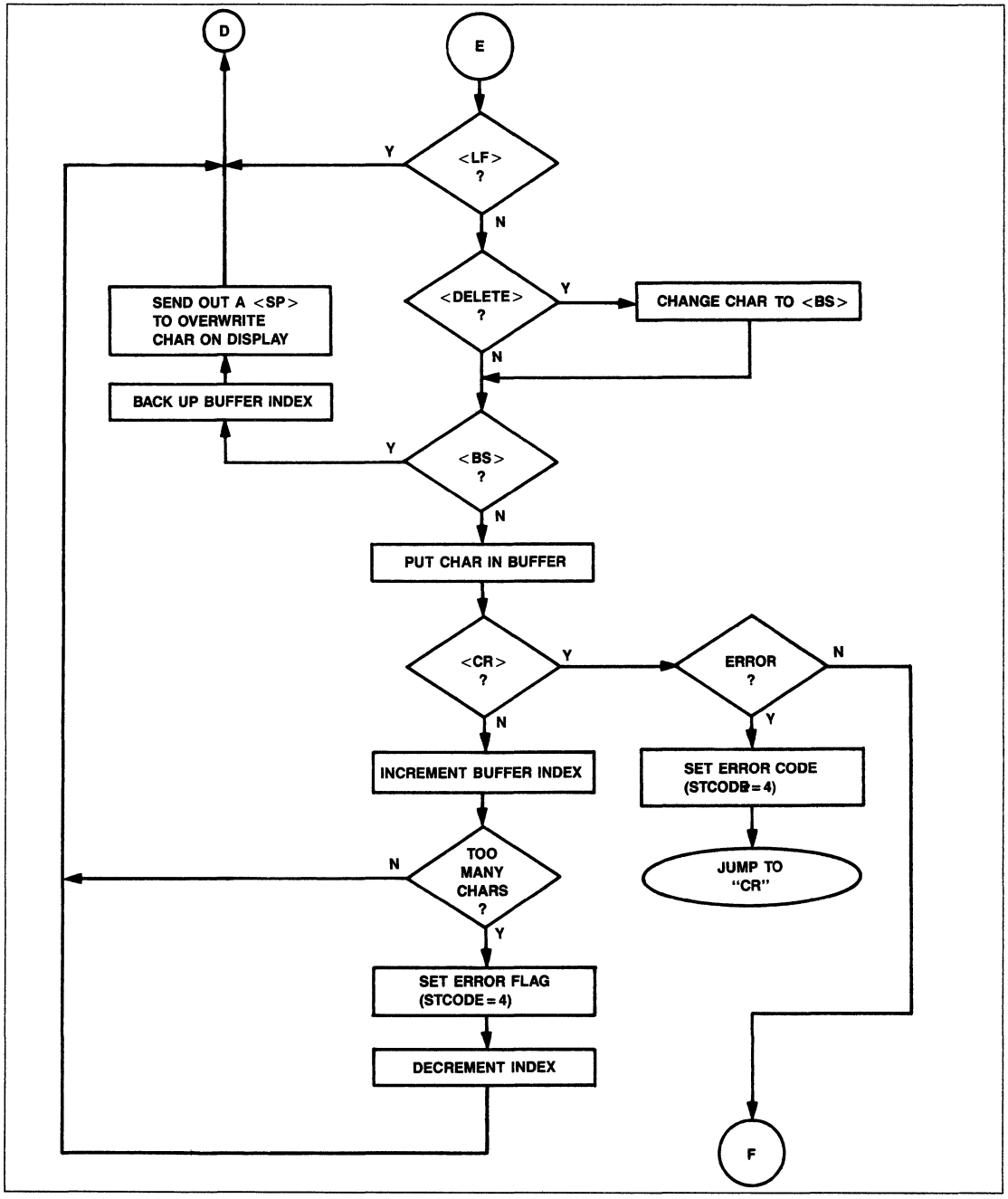

Figure 5. Command Mode Flowchart (Continued)

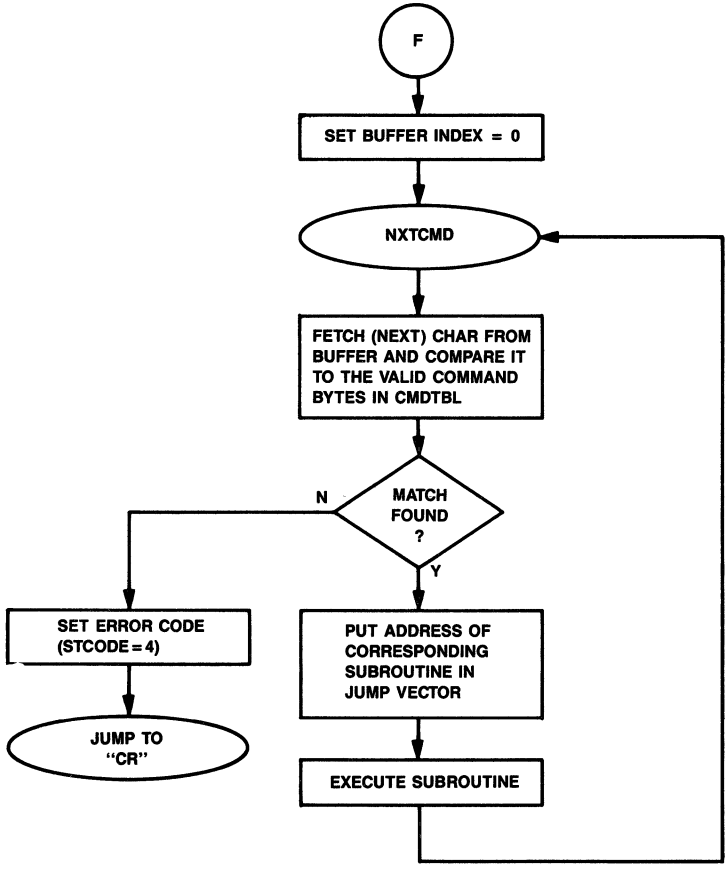

Figure 5. Command Mode Flowchart (Continued)

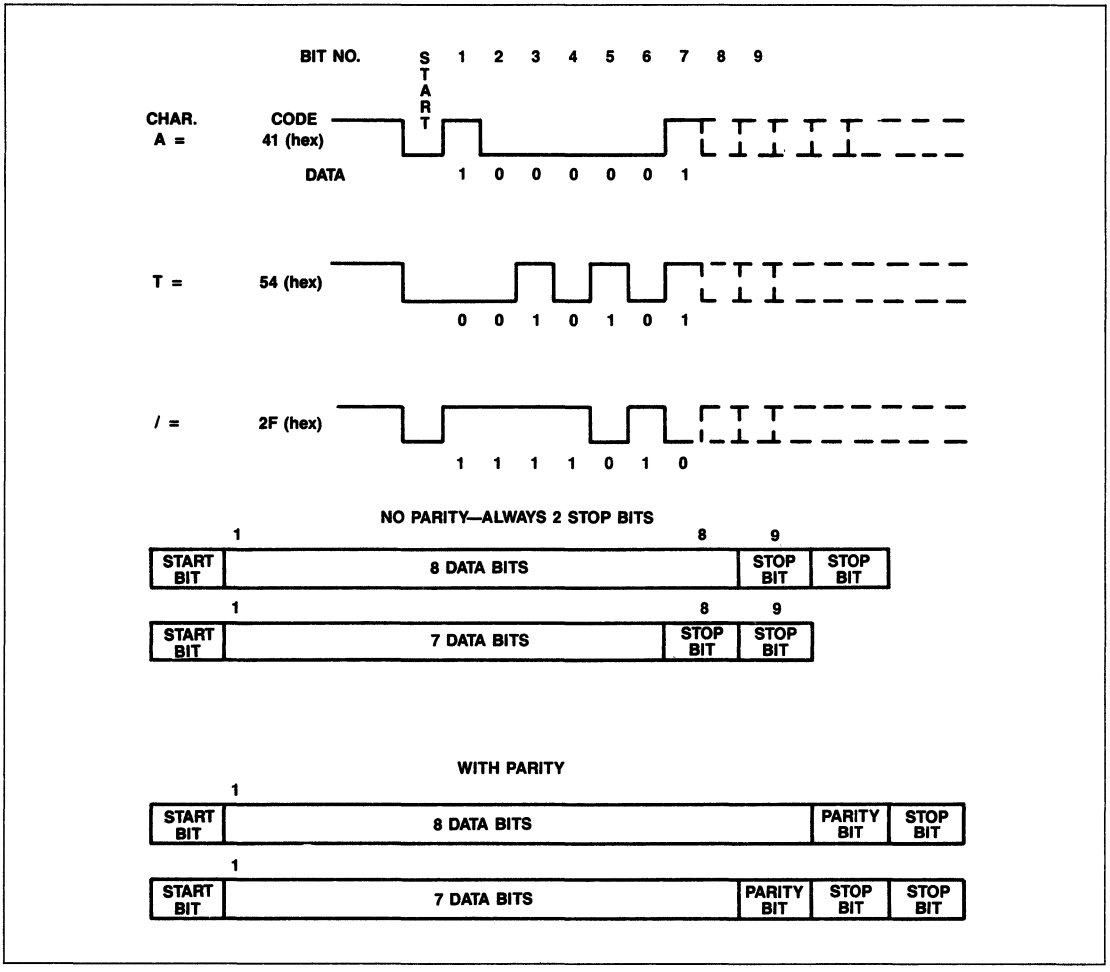

Figure 6. Serial Protocol Formats Data Length

Table 2. Selectable Serial Protocol Configurations

Command Word No.	Command ASCII Char. (Bits 1–7)	Command Word Bit 8	Command Word Bit 9	Message Protocol
1 2	A T or /	1 0	— —	Odd parity, 7 data bits, 2 stop bits
1 2	A T or /	0 1	— —	Even parity, 7 data bits, 2 stop bits
1 2	A T or /	1 1	— —	No parity, 7 data bits, 2 stop bits
1 2	A T or /	0 0	1 0	Odd parity, 8 data bits, 1 stop bit
1 2	A T or /	0 0	0 1	Even parity, 8 data bits, 1 stop bit
1 2	A T or /	0 0	1 1	No parity, 8 data bits, 2 stop bits

```
                                                    PAGE.0001

0001                ; THIS IS A PROGRAM FOR AN R6500/11 ACTING AS AN INTERFACE
0002                ;  BETWEEN A HOST COMPUTER WITH A SERIAL PORT AND AN R2424
0003                ;  MODEM.  IT IS DESIGNED TO RUN THE "AT" COMMAND SET.
0004
0005                ; ========================================================
0006
0007
0008                      .OPT   LLEN=132
0009                      .OPT   IVB
0010
0011 0000                 *=$0000
0012
0013 0000           PA    *=*+1
0014 0001           PB    *=*+1
0015
0016 0002                 *=$11
0017
0018 0011           IFR   *=*+1
0019 0012           IER   *=*+2
0020 0014           MCR   *=*+1
0021 0015           SCCR  *=*+1
0022 0016           SCSR  *=*+1
0023 0017           STDR  *=*+1
0024 0017           SRDR  =     STDR
0025 0018           CNTACL *=*+1
0026 0019           CNTAH *=*+1
0027 001A           CNTAL *=*+1
0028
0029 001B                 *=*+1
0030 001C           CNTBCL *=*+1
0031 001D           CNTBHC *=*+1
0032 001E           CNTBHL *=*+1
0033
0034 001F                 *     = $40              ; RAM VARIABLES
0035
0036 0040           DEFPRO *=*+1                   ; DEFAULT SERIAL PROTOCOL FOR AUTO-ANSWER COMMUNICATIONS
0037 0041           BAUD   *=*+1                   ; INDICATOR OF PRESENT TERMINAL BAUD RATE ( 3/12/24 )
0038 0042           BDRATL *=*+1                   ; LOW PART OF BAUD RATE, AS DETERMINED BY CNTR-A
0039 0043           BDRATH *=*+1                   ; HIGH PART OF BAUD RATE
0040 0044           DELAYC *=*+1                   ; IRQ COUNTER: COUNTS NUMBER OF TIMES IRQ ROUTINE IS CALLED
0041 0045           DELAYT *=*+1                   ; SET TO THE # OF TIMES THE IRQ ROUTINE IS TO BE CALLED
0042 0046           DELAYS *=*+1                   ; SET TO THE NUMBER OF SECONDS TO WAIT FOR
0043 0047           TESTB  *=*+1                   ; CONTAINS THE 7 SAMPLE BITS FROM THE SERIAL-IN LINE
0044 0048           ABIT8  *=*+1                   ; WHEN THE 7 BITS CLOCKED INTO "TESTB" MATCH THE "A" CHAR,
0045 0049           ABIT9  *=*+1                   ;   THE NEXT 2 BITS ARE CLOCKED IN AND STORED HERE.
0046 004A           TBIT8  *=*+1                   ; WHEN THE 7 SAMPLE BITS IN "TESTB" MATCH THE "T" CHAR, THE
0047 004B           TBIT9  *=*+1                   ;  NEXT 2 BITS ARE STORED IN "TBIT8" AND "TBIT9".
0048 004C           INBUFF *=*+40                  ; CONTAINS THE COMMAND STRING AS ENTERED FROM THE HOST SYS.
0049 0074           REPFLG *=*+1                   ; WHEN "A/" IS ENTERED AS COMMAND, THIS FLAG IS SET.
0050 0075           BUFFLG *=*+1                   ; THIS FLAG IS SET WHEN TOO MANY COMMAND CHARS ARE ENTERED
0051 0076           DILFLG *=*+1                   ; IS SET TO INDICATE ANY FOLLOWING NUMBERS ARE DIAL DIGITS
0052 0077           REVFLG *=*+1                   ; NORMAL ($00) OR REVERSE ($80) DIAL
0053 0078           IRQFLG *=*+1                   ; $00 ==> IRQ IS SERIAL-IN TIMER: $80 ==> IRQ IS DELAY TIMER
0054 0079           ECHOFG *=*+1                   ; $00 ==> DO NOT ECHO COMMAND CHARS: $80 ==> ECHO CHARS
```

Figure 7. Software Assembly Listing

```
0055 007A              DUPLEX  *=*+1          ; ECHO CHARS WHILE IN DATA MODE (ON-LINE) : 0=NO, $80=YES
0056 007B              RSLTFG  *=*+1          ; $00 ==> SEND OUT RESULT PROMPT: $80 ==> DON'T SEND IT OUT.
0057 007C              SPKRFG  *=*+1          ; USED TO CONTROL THE EXTERNAL SPEAKER
0058 007D              STCODE  *=*+1          ; RESULT (STATUS) CODE ( 0-4,5 )
0059 007E              VCODE   *=*+1          ; SEND RESULT PROMPT IN NUMERIC ( $00 ) OR VERBAL ( $80 ) FORM
0060 007F              XCODE   *=*+1          ; ALLOW EXTENDED RESULT CODES ?  ( $00 = NO / $80 = YES )
0061 0080              WAITFG  *=*+1          ; "WAIT-FOR-CARRIER ?" FLAG  (0 = NO / $80 = YES )


                                                        PAGE 0002

0062 0081              WAITC   *=*+1          ; INDICATES "WAIT-FOR-CARRIER" TIME INTERVAL HAS ELAPSED
0063 0082              ESCCNT  *=*+1          ; ESCAPE CODE COUNTER
0064 0083              SSETFG  *=*+1          ; INDICATES S-REG POINTER HAS BEEN SET TO SOME VALUE
0065 0084              SREGP   *=*+2          ; CONTAINS THE INDIRECT POINTER TO ONE OF THE S-REGISTERS
0066
0067                                          ;  THE FOLLOWING 17 BYTES CONTAIN THE VALUES FOR THE S-REGISTERS
0068
0069 0086              S0      *=*+1          ; RING TO ANSWER ON
0070 0087              S1      *=*+1          ; COUNTS THE NUMBER OF RINGS
0071 0088              S2      *=*+1          ; ESCAPE CODE CHARACTER
0072 0089              S3      *=*+1          ; CARRIAGE RETURN CHAR
0073 008A              S4      *=*+1          ; LINE FEED CHAR
0074 008B              S5      *=*+1          ; BACKSPACE CHAR
0075 008C              S6      *=*+1          ; WAIT-TIME FOR DIAL TONE
0076 008D              S7      *=*+1          ; WAIT-TIME FOR CARRIER (AFTER DIALING OR ANSWERING )
0077 008E              S8      *=*+1          ; PAUSE-TIME ( USED BY "COMMA" COMMAND )
0078 008F              S9      *=*+1          ; CARRIER-DETECT RESPONSE TIME
0079 0090              S10     *=*+1          ; DELAY-TIME BETWEEN LOSS OF CARRIER AND "HANG UP"
0080 0091              S11     *=*+1          ; DURATION AND SPACING OF TOUCH TONES
0081 0092              S12     *=*+1          ; ESCAPE CODE GUARD-TIME
0082 0093              S13     *=*+1          ; UART STATUS REGISTER
0083 0094              S14     *=*+1          ; OPTION REGISTER
0084 0095              S15     *=*+1          ; FLAG REGISTER
0085 0096              S16     *=*+1          ; 1=ENTER SELF-TEST / 0=STOP SELF-TEST
0086 0097              S17     *=*+1          ; GENERAL SYSTEM STATUS
0087
0088 0098              NUM     *=*+3          ; WORK AREA FOR ASCII-TO-HEX AND HEX-TO-ASCII CONVERSION
0089 009B              CMDVEC  *=*+2          ; INDIRECT POINTER TO THE NEXT COMMAND TO BE EXECUTED
0090 009D              TEMP    *=*+1          ; TEMPORARY STORAGE BYTE

                                                        PAGE 0003

0092 1000              RCV     =       $1000  ; BASE ADDRESS FOR RECEIVER REGISTERS
0093
0094 009E                      *=      RCV+2
0095 1002              RCV2    *=*+6
0096 1008              RCV8    *=*+1
0097 1009              RCV9    *=*+1
0098 100A              RCVA    *=*+1
0099 100B              RCVB    *=*+1
0100 100C              RCVC    *=*+1
0101 100D              RCVD    *=*+1
0102 100E              RCVE    *=*+1
```

```
0103 100F              RCVF   *=*+1
0104
0105 2000              XMT    =$2000              ; BASE ADDRESS FOR THE TRANSMITTER REGISTERS
0106
0107 1010                     *=     XMT
0108 2000              XMT0   *=*+2
0109 2002              XMT2   *=*+6
0110 2008              XMT8   *=*+1
0111 2009              XMT9   *=*+1
0112 200A              XMTA   *=*+1
0113 200B              XMTB   *=*+1
0114 200C              XMTC   *=*+1
0115 200D              XMTD   *=*+1
0116 200E              XMTE   *=*+1
0117 200F              XMTF   *=*+1
0118
0119 0010              DLYHIB =      $10           ; DELAY-TIME FACTOR
0120 E09C              DLYTIM =      $E09C         ; ( DLYTIM * DLYHIB @ 920KHZ = 1 SEC. )
0121 6760              TENTHD =      $6760         ; ( TENTHD * DLYHIB @ 920KHZ = 1/10 SEC. )
0122 0001              ESCDLY =      1
0123 479C              ESCTIM =      $479C         ; 1 COUNT FOR "ESCAPE" CODE GUARD TIME ( 20MS )
0124
0125 00BF              BAUD3  =      $00BF         ; CNTR-A VALUE FOR SERIAL-I/O BAUD RATE OF 300 BAUD ( @ 920KHz
0126 002F              BAUD12 =      $002F         ;  VALUE FOR 1200 BAUD
0127 0017              BAUD24 =      $0017         ;  VALUE FOR 2400 BAUD
0128
0129 0021              NUMCMD =      33            ; NUMBER OF COMMANDS IN "CMDTBL"
```



```
0131 2010                     *=$F800
0132
0133 F800  A2 FF       RESET  LDX    #$FF          ; INITIALIZE THE R6500/11
0134 F802  9A                 TXS
0135 F803  D8                 CLD
0136 F804  78                 SEI
0137 F805  A9 A0              LDA    #$A0          ; SET UP MODE REGISTER FOR ABBREVIATED BUS
0138 F807  85 14              STA    MCR
0139
0140 F809  20 BE FA           JSR    INITSW        ; INITIALIZE VARIABLES, ETC.
0141
0142 F80C  87 01              SMB    0,PB          ; CTL = 0  ( TRANSMIT TO MODEM )
0143 F80E  17 01              RMB    1,PB          ; CTS/ = 0
0144 F810  27 01              RMB    2,PB          ; DTR/ = 0  ( ACTIVE )
0145 F812  D7 01              SMB    5,PB          ; HISPEED = 1 ( HIGH SPEED )
0146 F814  E7 01              SMB    6,PB          ; DISABLE SPEAKER
0147
```

```
0148                    ; ********************************************************************
0149                    ;
0150                    ;       FIRST CHARS ACROSS SHOULD BE "AT" OR ""A/".  ASSUME AN "A"
0151                    ;  IS THE FIRST CHAR:  BY TIMING THE DURATION OF THE FIRST LOW
0152                    ;  PULSE (START BIT), THE BAUD RATE IS DETERMINED.  USING THIS AS
0153                    ;  THE WIDTH OF ONE BIT, 7 SAMPLES ARE MADE OF THE SERIAL INPUT LINE
0154                    ;  AT ONE-BIT INTERVALS, WITH EACH "BIT" SHIFTED INTO A TEST BUFFER
0155                    ;  ( "TESTB" ).  AFTER 7 SAMPLES, THE TEST BUFFER IS RIGHT-JUSTIFIED
0156                    ;  (SHIFTED RIGHT ONE MORE TIME) AND COMPARED TO THE ASCII "A" CHAR.
0157                    ;  IF A MATCH IS NOT MADE, WE WAIT 2 MORE "BITS", TIME THE NEXT LOW PULSE
0158                    ;    AND CLOCK IN 7 MORE BITS.
0159                    ;  IF A MATCH IS FOUND, AN "A" CHAR IS ASSUMED TO HAVE BEEN READ IN
0160                    ;  AND THE NEXT TWO BITS ARE SAVED FOR FUTURE DETERMINATION OF
0161                    ;  TRANSMISSION PROTOCOL (PARITY, BITS/CHAR).  THE NEXT CHAR IS
0162                    ;  CLOCKED IN AND COMPARED TO "T" AND "/".  IF A MATCH IS FOUND THEN
0163                    ;  THE PROTOCOL IS DETERMINED AND THE COMMAND BYTES FOR THE MODEM
0164                    ;  ( IF ANY ) ARE READ IN AND PROCESSED.
0165                    ;       IF A MATCH IS NOT FOUND FOR "AT" OR "A/" THEN WE START OVER AGAIN
0166                    ;  LOOKING FOR AN "A" CHAR.
0167                    ;       MEANWHILE, IF CHARACTER ECHOING HAS BEEN ENABLED ( AND BY DEFAULT
0168                    ;  IT IS ), TIMER B IS GENERATING INTERRUPTS AT A FREQUENCY SLIGHTLY
0169                    ;  GREATER THAN TWICE THE 2400 BAUD ( MAXIMUM ALLOWABLE BAUD RATE ) FREQUENCY.
0170                    ;  THE INTERRUPT ROUTINE SAMPLES THE LEVEL OF THE SERIAL INPUT LINE AND SETS
0171                    ;  THE SERIAL OUTPUT LINE TO MATCH.  THIS HAS THE EFFECT OF BLINDLY ECHOING
0172                    ;  INCOMING CHARACTERS BACK TO THE HOST COMPUTER.  THIS WILL BE DONE UNTIL
0173                    ;  "AT" OR "A/" HAS BEEN RECOGNIZED, AT WHICH POINT THE IRQ IS DISABLED
0174                    ;  AND CHARACTERS ARE ECHOED BACK AS CHARACTERS, NOT AS BITS.
0175
0176 F816  A9 00       RESTRT LDA   #00              ; DISABLE RECEIVER AND TRANSMITTER
0177 F818  85 15              STA   SCCR
0178 F81A  85 74              STA   REPFLG            ; CLEAR OUT WORKING VARIABLES
0179 F81C  85 48              STA   ABIT8
0180 F81E  85 49              STA   ABIT9
0181 F820  85 4A              STA   TBIT8
0182 F822  85 4B              STA   TBIT9
0183 F824  85 47              STA   TESTB
0184 F826  85 76              STA   DILFLG            ; PREVENT NUMBERS FROM DIALING UNTIL "DIAL" COMMAND
0185 F828  85 B0              STA   WAITFG
0186 F82A  85 75              STA   BUFFLG
0187 F82C  85 7D              STA   STCODE            ; ASSUME "OK" -- STCODE WILL BE RESET IF A PROBLEM ARISES
0188 F82E  AD 0D 10           LDA   RCVD              ; SET "LCD" BIT
0189 F831  09 04              ORA   #$04
0190 F833  8D 0D 10           STA   RCVD
0191 F836  20 D7 FD           JSR   NEWCR             ; UPDATE RECEIVER REGISTER
```



```
0192 F839  07 10              RMB   0,IFR-1           ; CLEAR "RING" FLAG BIT FROM FLAG REGISTER
0193 F83B  A9 03              LDA   #03               ; CNTR A = PULSE WIDTH TIMER
0194 F83D  05 14              ORA   MCR
0195 F83F  85 14              STA   MCR
0196 F841  7F 79 0C           BBR   7,ECHOFG,NOIRQ    ; NO ECHO IF FLAG TURNED OFF
0197 F844  A9 B0              LDA   #$B0              ; START TIMER B TO PERIODICALLY SAMPLE
0198 F846  85 1C              STA   CNTBCL            ;  THE SERIAL INPUT LINE AND ECHO BACK
```

```
0199 F848  A9 00          LDA   #00          ;  THE SAME LOGIC LEVEL ON THE OUTPUT
0200 F84A  85 1E          STA   CNTBHL       ;  LINE.
0201 F84C  D7 12          SMB   5,IER
0202 F84E  77 78          RMB   7,IRQFLG
0203 F850  A9 FF    NOIRQ LDA   #$FF
0204 F852  A8             TAY
0205 F853  85 18          STA   CNTACL       ; READY CNTR A FOR PULSE-WIDTH MEASUREMENT
0206 F855  84 1A          STY   CNTAL
0207 F857  8F 11 50  L1   BBS   0,IFR,RING   ; IF PHONE IS RINGING, GO SEE IF IT'S TIME TO ANSWER IT
0208 F85A  FF 00 FA       BBS   7,PA,L1      ; WAIT FOR RECEIVE LINE TO GO LOW
0209 F85D  67 00          RMB   6,PA         ; SET SERIAL-OUT LINE LOW TO MATCH
0210 F85F  7F 00 FD  L2   BBR   7,PA,L2      ; NOW WAIT FOR IT TO GO BACK HIGH ( THIS SHOULD
0211                                         ;   BE THE START BIT OF "A" )
0212 F862  58             CLI                ; ALLOW TIMER-B IRQ
0213 F863  A5 19          LDA   CNTAH        ; GET PULSE WIDTH COUNT
0214 F865  49 FF          EOR   #$FF         ; INVERT IT
0215 F867  85 43          STA   BDRATH       ; AND SAVE IT
0216 F869  A8             TAY
0217 F86A  A5 18          LDA   CNTACL
0218 F86C  49 FF          EOR   #$FF
0219 F86E  AA             TAX
0220 F86F  A9 FC          LDA   #$FC         ; SET CNTR A = TIME INTERVAL COUNTER
0221 F871  25 14          AND   MCR
0222 F873  85 14          STA   MCR
0223 F875  86 42          STX   BDRATL       ; SAVE LOW BYT OF COUNT
0224 F877  86 18          STX   CNTACL       ; SET LOW BYTE OF BAUD TIMER
0225 F879  98             TYA                ; SET UP COUNTER FOR 1/2 BIT WIDTH, TO
0226 F87A  4A             LSR   A            ;  POSITION SERIAL LINE SAMPLES APPROX.
0227 F87B  85 1A          STA   CNTAL        ;  IN MIDDLE OF BIT.
0228 F87D  4F 11 FD  L3   BBR   4,IFR,L3     ; WAIT FOR TIMER
0229 F880  84 1A          STY   CNTAL        ;  NOW START TIMER A WITH FULL DELAY  ( ALSO CLEARS FLAG )
0230 F882  A5 00          LDA   PA           ; GET VALUE OF SERIAL BIT (SHOULD BE HIGH)
0231 F884  0A             ASL   A            ; ROTATE RECEIVE BIT VALUE INTO CARRY BIT
0232 F885  66 47          ROR   TESTB        ;  AND ROTATE IT INTO TEST BYTE
0233 F887  A2 06          LDX   #06          ; CLOCK IN 6 MORE SERIAL BITS
0234 F889  4F 11 FD  L4   BBR   4,IFR,L4     ; WAIT FOR ONE BIT TIME
0235 F88C  A5 18          LDA   CNTACL       ; CLEAR FLAG
0236 F88E  A5 00          LDA   PA           ; GET SERIAL BIT
0237 F890  0A             ASL   A            ; AND ROTATE IT INTO TESTB
0238 F891  66 47          ROR   TESTB
0239 F893  CA             DEX                ; CLOCKED IN 6 BITS YET ?
0240 F894  D0 F3          BNE   L4           ; NO ==> GET NEXT BIT
0241 F896  A5 47          LDA   TESTB        ; YES==> IS CHAR AN "A" ?
0242 F898  4A             LSR   A            ;  ( RIGHT-JUSTIFY TEST CHAR )
0243 F899  C9 41          CMP   #'A'
0244 F89B  F0 10          BEQ   FOUNDA       ; YES==> CHECK NEXT CHAR FOR "T" OR "/"
0245 F89D  98             TYA                ; NO ==> WAIT 2 BIT TIMES
0246 F89E  0A             ASL   A            ;  THEN JUMP TO "RESTART"
0247 F89F  85 1A          STA   CNTAL        ;  TO READ IN ANOTHER TEST CHAR
0248 F8A1  4F 11 FD  L4A  BBR   4,IFR,L4A    ; WAIT FOR TIMER
0249 F8A4  7F 00 FD  L5   BBR   7,PA,L5      ; THEN MAKE SURE INPUT LINE IS HIGH
0250 F8A7  4C 16 F8  GO2RES JMP  RESTRT      ; ... AND READ IN ANOTHER 7 BITS
0251
0252 F8AA  4C 1C FA  RING  JMP   RINGNG      ; CHECK RING COUNT.  IF PHONE HAS RUNG ENOUGH TIMES
```

```
0253                                            ;  ( AS DETERMINED BY S-REG 0 ) THEN ANSWER IT.
0254                                            ;  OTHERWISE, GO BACK TO "RESTART"
0255
0256                    ; FOUND AN "A" CHAR.  NOW SAVE NEXT TWO BITS FOR PROTOCOL CHECK,
0257                    ;   THEN CHECK FOR "T" OR "/" CHARS.
0258
0259 F8AD   4F 11 FD    FOUNDA BBR    4,IFR,FOUNDA        ; WAIT ONE BIT TIME
0260 F8B0   A5 18              LDA    CNTACL              ; CLEAR FLAG
0261 F8B2   A5 00              LDA    PA                  ; GET BIT
0262 F8B4   0A                 ASL    A
0263 F8B5   66 48              ROR    ABIT8               ; SAVE IT AS BIT 8 OF "A" ( FOR FORMAT CHECKING LATER )
0264 F8B7   4F 11 FD    L6     BBR    4,IFR,L6            ; GET BIT 9  ( WAIT ONE MORE BIT TIME )
0265 F8BA   A5 18              LDA    CNTACL              ; CLEAR FLAG
0266 F8BC   A5 00              LDA    PA
0267 F8BE   0A                 ASL    A
0268 F8BF   66 49              ROR    ABIT9               ; AND SAVE "A" BIT 9
0269 F8C1   7F 00 FD    L7     BBR    7,PA,L7             ; WAIT FOR RECEIVE LINE TO GO HIGH
0270 F8C4   FF 00 FD    L8     BBS    7,PA,L8             ; NOW WAIT FOR IT TO GO LOW ( START BIT )
0271 F8C7   86 47              STX    TESTB               ; RESET "TESTB" FOR "T" AND "/" CHECK
0272 F8C9   98                 TYA                        ; DELAY APPROX. 1/2 BIT TIME
0273 F8CA   4A                 LSR    A                   ;  ( DIVIDE MSB OF DELAY TIME BY 2 )
0274 F8CB   85 1A              STA    CNTAL               ; START TIMER
0275 F8CD   4F 11 FD    L9     BBR    4,IFR,L9            ; WAIT FOR TIMER
0276 F8D0   84 1A              STY    CNTAL               ; RESTART TIMER  ( AND CLEAR FLAG )
0277 F8D2   A2 07              LDX    #07                 ; CLOCK IN 7 BITS ONLY ( OF CHAR FOLLOWING "A" )
0278 F8D4   4F 11 FD    L10    BBR    4,IFR,L10           ; WAIT FOR TIMER
0279 F8D7   A5 18              LDA    CNTACL              ; CLEAR FLAG
0280 F8D9   A5 00              LDA    PA                  ; GET BIT
0281 F8DB   0A                 ASL    A
0282 F8DC   66 47              ROR    TESTB               ;  AND SHIFT IT IN "TESTB"
0283 F8DE   CA                 DEX                        ; 7 BITS YET ?
0284 F8DF   D0 F3              BNE    L10                 ; NO ==> GET NEXT BIT
0285 F8E1   A5 47              LDA    TESTB               ; YES==> SEE IF THIS CHAR MATCHES "T" OR "/"
0286 F8E3   4A                 LSR    A                   ; ( RIGHT-JUSTIFY CHAR )
0287 F8E4   C9 2F              CMP    #'/'                ; "/" ?
0288 F8E6   F0 07              BEQ    FOUNDS              ; YES==> "A/" CHARS RECEIVED --> FIGURE OUT PROTOCOL
0289 F8E8   C9 54              CMP    #'T'                ; NO ==> "T" ?
0290 F8EA   F0 05              BEQ    FOUNDT              ; YES==> "AT" CHARS RECEIVED --> FIGURE OUT PROTOCOL
0291 F8EC   4C 16 F8           JMP    RESTRT              ; NO ==> START OVER .....
0292
0293 F8EF   F7 74        FOUNDS SMB    7,REPFLG            ; INDICATE REPEAT OF LAST COMMAND STRING
0294
0295 F8F1   4F 11 FD    FOUNDT BBR    4,IFR,FOUNDT        ; WAIT ONE BIT TIME
0296 F8F4   A5 18              LDA    CNTACL              ; CLEAR FLAG
0297 F8F6   A5 00              LDA    PA                  ; SAVE BIT 8
0298 F8F8   0A                 ASL    A
0299 F8F9   66 4A              ROR    TBIT8
0300 F8FB   4F 11 FD    L12    BBR    4,IFR,L12           ; WAIT ONE LAST BIT TIME
0301 F8FE   A5 18              LDA    CNTACL              ; CLEAR BIT-WIDTH FLAG
0302 F900   A5 00              LDA    PA
0303 F902   0A                 ASL    A                   ; SAVE BIT 9
0304 F903   66 4B              ROR    TBIT9
0305
```

```
0306                    ; BAUD RATE DETERMINED.  NOW FIGURE OUT TRANSMISSION PROTOCOL
0307                    ;   ( NUMBER BITS/CHAR, ODD/EVEN/NO PARITY )
0308
0309 F905  24 49            BIT   ABIT9           ; IS BIT 9 OF "A" = 0 ?
0310 F907  10 14            BPL   EVEN8           ; YES==> PROTOCOL IS 8 BITS/CHAR, EVEN PARITY
0311 F909  24 4B            BIT   TBIT9           ; NO ==> IS BIT 9 OF "T" = 0 ?
0312 F90B  10 16            BPL   ODD8            ; YES==> PROTOCOL IS 8 BITS/CHAR, ODD PARITY
0313 F90D  A5 48            LDA   ABIT8           ; NO ==> ARE EIGHTH BITS OF "A" AND "T"
```



```
0314 F90F  45 4A            EOR   TBIT8           ;        THE SAME ?
0315 F911  F0 1C            BEQ   NOPAR           ; YES==> NO PARITY USED
0316 F913  24 48            BIT   ABIT8           ; NO ==> BIT 8 OF "A" = 0 ?
0317 F915  10 12            BPL   EVEN7           ; YES==> 7 BITS, EVEN PARITY, 2 STOP BITS
0318 F917  A9 C6      ODD7  LDA   #$C6            ; NO ==> 7 BITS, ODD PARITY,  2 STOP BITS
0319 F919  A0 10            LDY   #$10            ; SET VALUE FOR "RCVC"  ( 10 BITS/WORD )
0320 F91B  D0 20            BNE   LABEL1          ; ( BRANCH ALWAYS )
0321 F91D  A9 C3      EVEN8 LDA   #$C3
0322 F91F  A0 18            LDY   #$18            ; SET VALUE FOR "RCVC"  ( 11 BITS/WORD )
0323 F921  D0 1A            BNE   LABEL1          ; ( BRA )
0324 F923  A9 C2      ODD8  LDA   #$C2
0325 F925  A0 18            LDY   #$18            ; SET VALUE FOR "RCVC"  ( 11 BITS/WORD )
0326 F927  D0 14            BNE   LABEL1          ; ( BRA )
0327 F929  A9 C7      EVEN7 LDA   #$C7
0328 F92B  A0 10            LDY   #$10            ; SET VALUE FOR "RCVC"  ( 10 BITS/WORD )
0329 F92D  D0 0E            BNE   LABEL1          ; ( BRA )
0330 F92F  24 48      NOPAR BIT   ABIT8           ; IS BIT 8 OF "A" = 1 ?
0331 F931  30 06            BMI   NOPAR7          ; YES==> 7 BITS, NO PARITY
0332 F933  A9 C0      NOPAR8 LDA  #$C0            ; NO ==> 8 BITS, NO PARITY
0333 F935  A0 10            LDY   #$10            ; SET VALUE FOR "RCVC"  ( 10 BITS/WORD )
0334 F937  D0 04            BNE   LABEL1          ; ( BRA )
0335 F939  A9 C4      NOPAR7 LDA  #$C4
0336 F93B  A0 08            LDY   #$08            ; SET VALUE FOR "RCVC"  ( 9 BITS/WORD )
0337
0338 F93D  85 15      LABEL1 STA  SCCR            ; SET UP SERIAL COMMAND REGISTER FOR
0339 F93F  85 40            STA   DEFPRO          ;   BAUD RATE AND PROTOCOL  [ SAVE PRESENT PROTOCOL ]
0340 F941  A2 04            LDX   #04             ; DIVIDE BIT-WIDTH TIME BY 16
0341 F943  46 43      ROTATE LSR  BDRATH          ;  TO GET BAUD RATE VALUE
0342 F945  66 42            ROR   BDRATL
0343 F947  CA               DEX
0344 F948  D0 F9            BNE   ROTATE
0345 F94A  A5 42            LDA   BDRATL          ; SET UP BAUD RATE TIMER
0346 F94C  85 18            STA   CNTACL
0347 F94E  A5 43            LDA   BDRATH
0348 F950  85 1A            STA   CNTAL
0349 F952  57 12            RMB   5,IER           ; DISABLE IRQS
0350 F954  A5 42            LDA   BDRATL          ; DETERMINE WHAT BAUD RATE WE'RE RUNNING AT
0351 F956  C9 B5            CMP   #BAUD3-10       ; IS IT GREATER THAN 300 ?
0352 F958  90 08            BCC   GT300           ; YES==> BRANCH
0353 F95A  A2 03      B03   LDX   #03             ; NO ==> BAUD = 300
0354 F95C  57 01            RMB   5,PB            ; SET "HISPEED" TO 0 ( LOW SPEED )
0355 F95E  A9 04            LDA   #$04            ; SET R2424 "MODE" CODE  ( BELL 212A ASYNC )
0356 F960  D0 12            BNE   BD2             ; ( BRANCH ALWAYS )
```

```
0357 F962  C9 25       GT300  CMP   #BAUD12-10        ; IS BAUD GREATER THAN 1200 ?
0358 F964  90 08              BCC   B24               ; YES==> MUST BE 2400
0359 F966  A2 0C       B12    LDX   #12               ; NO ==> MUST BE 1200
0360 F968  D7 01              SMB   5,PB              ; SET "HISPEED" TO 1 (HIGH SPEED )
0361 F96A  A9 03              LDA   #$03              ; SET R2424 "MODE" CODE  ( BELL 212A ASYNC )
0362 F96C  D0 06              BNE   BD2               ; ( BRA )
0363 F96E  A2 18       B24    LDX   #24               ; 2400 BAUD
0364 F970  D7 01              SMB   5,PB
0365 F972  A9 0D              LDA   #$0D              ; SET R2424 "MODE" CODE  ( V.22 BIS ASYNC )
0366 F974  85 9D       BD2    STA   TEMP              ; SAVE "MODE" CODE IN TEMPORARY LOCATION
0367 F976  AD 0A 10           LDA   RCVA              ; CHANGE "MODE" IN R2424 MODEM REGISTERS
0368 F979  29 F0              AND   #$F0              ;  - CLEAR OUT PREVIOUS MODE
0369 F97B  05 9D              ORA   TEMP              ;  - SET NEW MODE
0370 F97D  8D 0A 10           STA   RCVA              ;  - AND PROGRAM RECEIVER
0371 F980  AD 0A 20           LDA   XMTA              ; CHANGE TRANSMITTER BAUD RATE ...
0372 F983  29 F0              AND   #$F0              ;  - CLEAR OUT PREVIOUS MODE
0373 F985  05 9D              ORA   TEMP              ;  - SET NEW MODE
0374 F987  8D 0A 20           STA   XMTA              ;  - AND PROGRAM TRANSMITTER
```



```
0375 F98A  8C 0C 10           STY   RCVC              ;   AND SET MODEM
0376 F98D  8C 0C 20           STY   XMTC
0377 F990  20 CB FD           JSR   NEWCXR            ; UPDATE R2424 REGISTERS WITH NEW VALUES
0378 F993  86 41              STX   BAUD              ; SAVE BAUD CODE
0379
0380 F995  F7 78              SMB   7,IRQFLG          ; SET ISR TO PROCESS DELAY TIME FOR WAIT-FOR-CARRIER
0381 F997  D7 16              SMB   5,SCSR            ; SET "DATA REG EMPTY" FLAG FOR 'LAST BIT OUT'
```



```
0383                   ; BAUD RATE DETERMINED.  NOW IN COMMAND MODE.  READ COMMAND
0384                   ;  CHARACTERS INTO BUFFER ( INBUFF ).  TERMINATE ON <CR>.
0385
0386 F999  FF 74 4B           BBS   7,REPFLG,REPEAT   ; BRANCH IF "A/" RECEIVED
0387 F99C  A2 00       SETPTR LDX   #00               ; "AT" RECEIVED --> SET BUFFER INDEX TO 0
0388 F99E  A5 16       WAITIN LDA   SCSR              ; CHECK RECEIVER STATUS
0389 F9A0  29 0F              AND   #$0F
0390 F9A2  F0 FA              BEQ   WAITIN            ; NO BITS SET ==> NO RECEIVED CHAR, TRY AGAIN
0391
0392 F9A4  A5 17       GETCHR LDA   SRDR              ; GET CHAR FROM RECEIVER BUFFER
0393 F9A6  7F 79 03           BBR   7,ECHOFG,CTLCOD    ; BRANCH IF ECHO DISABLED
0394 F9A9  20 51 FF           JSR   CHROUT            ; ECHO CHAR BACK TO HOST COMPUTER
0395 F9AC  C5 89       CTLCOD CMP   S3                ; IS CHAR A <CR> ?
0396 F9AE  F0 1D              BEQ   GOTCHR            ; YES==> SAVE IT AND PROCEED TO "ALLIN"
0397 F9B0  C9 20              CMP   #$20              ; IS INCHAR A <SP> ?
0398 F9B2  F0 EA              BEQ   WAITIN            ; YES==> IGNORE IT
0399 F9B4  90 E8              BCC   WAITIN            ; CHAR IS LESS THAN $20 ( CONTROL CODE ) --> IGNORE IT
0400 F9B6  C9 7F              CMP   #$7F              ; IS IT A "DELETE" CHAR ?   <-- REMOVE THESE FOUR LINES IF THE
0401 F9B8  D0 05              BNE   BS                ; NO ==> CHECK FOR <BS>       <-- <DELETE> KEY ON THE PARTICULAR
0402 F9BA  A5 8B              LDA   S5                ; YES==> CHANGE IT TO <BS>    <-- TERMINAL USED WITH THIS DESIGN
0403 F9BC  20 51 FF           JSR   CHROUT            ; SEND OUT <BACKSPACE>    <-- BACKSPACES THE CURSOR.
```

```
0404 F9BF  C5 8B      BS     CMP   S5              ; IS IT A <BACK-SPACE> ?
0405 F9C1  D0 0A             BNE   GOTCHR          ; NO ==> ACCEPT CHAR
0406 F9C3  CA         DELETE DEX                   ; YES==> OVERWRITE PREVIOUS CHAR IN BUFFER
0407 F9C4  10 D8             BPL   WAITIN          ; BRANCH IF BUFF POINTER NOT LESS THAN 0
0408 F9C6  A9 20             LDA   #$20            ; OUTPUT A <SP>
0409 F9C8  20 51 FF          JSR   CHROUT
0410 F9CB  30 CF             BMI   SETPTR          ; LIMIT LOWEST VALUE OF POINTER TO 0  ( BRA )
0411
0412 F9CD  95 4C      GOTCHR STA   INBUFF,X        ;  SAVE CHAR IN BUFFER
0413 F9CF  C5 89             CMP   S3              ; IS IT A <CR> ?
0414 F9D1  F0 0A             BEQ   ALLIN           ; YES==> ALL CHARS RECEIVED
0415 F9D3  E8                INX                   ; NO ==> INC POINTER AND GET NEXT CHAR
0416 F9D4  E0 29             CPX   #41             ; IS BUFFER FULL ?
0417 F9D6  D0 C6             BNE   WAITIN          ; NO ==> GET NEXT CHAR
0418 F9D8  F7 75             SMB   7,BUFFLG        ; YES==> SET FLAG TO INDICATE ERROR
0419 F9DA  CA                DEX                   ; KEEP READING UNTIL <CR>
0420 F9DB  D0 C1             BNE   WAITIN          ; ( BRA )
0421
0422 F9DD  7F 75 07   ALLIN  BBR   7,BUFFLG,REPEAT  ; BRANCH IF 40 OR LESS CHARS READ IN
0423 F9E0  A9 04             LDA   #04             ; TOO MANY CHARS ENTERED --> ERROR
0424 F9E2  85 7D             STA   STCODE          ; SET STATUS CODE TO INDICATE ERROR
0425 F9E4  4C E0 FD          JMP   CR              ; AND TERMINATE COMMAND STRING
0426
0427 F9E7  A2 00      REPEAT LDX   #00             ; SET COMMAND STRING POINTER TO ZERO
```



```
0429                  ; ALL COMMANDS AND PARAMETERS HAVE BEEN RECEIVED.  NOW EXECUTE
0430                  ;  EACH COMMAND, IN ORDER, UNTIL <CR> OR UNRECOGNIZED COMMAND (ERROR) .
0431
0432 F9E9  20 F5 F9   NXTCMD JSR   FNDCMD           ; FIND CORRESPONDING SUBROUTINE ADDRESS AND
0433                                                ;  SET UP JUMP VECTOR
0434 F9EC  20 F2 F9          JSR   DOCMD           ; EXECUTE COMMAND.
0435 F9EF  4C E9 F9          JMP   NXTCMD          ; FETCH NEXT COMMAND
0436 F9F2  6C 9B 00   DOCMD  JMP   (CMDVEC)        ; JMP TO COMMAND ROUTINE.

0438                  ;           EACH COMMAND ROUTINE ASSUMES THE X-REG POINTS
0439                  ;            TO THE CHAR IN "INBUFF" FOLLOWING THE COMMAND
0440                  ;            CHAR, AND LEAVES X-REG POINTING TO THE NEXT
0441                  ;            COMMAND CHAR.  THE Y-REG IS FREE FOR USE AS
0442                  ;            A GENERAL SCRATCH-PAD REGISTER.
0443
0444 F9F5  A0 00      FNDCMD LDY   #00              ; SET UP TABLE INDEX
0445 F9F7  B5 4C             LDA   INBUFF,X        ; FETCH COMMAND BYTE
0446 F9F9  C5 89             CMP   S3              ; IS IT A <CR> ?
0447 F9FB  F0 0E             BEQ   GOCR            ; YES==> TERMINATE COMMAND STRING
0448 F9FD  D9 47 FA   LOOP2  CMP   CMDTBL,Y        ; NO ==> A MATCH FOUND ?
0449 FA00  F0 0B             BEQ   FOUND           ; YES==> GET VECTOR
0450 FA02  C8                INY                   ; NO ==> TRY NEXT TABLE ENTRY
0451 FA03  C0 21             CPY   #NUMCMD         ; END OF TABLE ?
0452 FA05  D0 F6             BNE   LOOP2           ; NO ==> GO AGAIN
0453 FA07  A9 04             LDA   #04             ; YES==> ERROR ...
0454 FA09  85 7D             STA   STCODE
```

```
0455 FA0B  A0 21     GOCR  LDY  #NUMCMD          ; SET POINTER TO <CR> COMMAND
0456
0457 FA0D  98        FOUND TYA                   ; COMMAND FOUND.  GET ASSOCIATED VECTOR
0458 FA0E  0A              ASL  A                ; MULT INDEX BY 2
0459 FA0F  A8              TAY
0460 FA10  B9 69 FA        LDA  VECTBL,Y         ; GET VECTOR
0461 FA13  85 9B           STA  CMDVEC           ; AND SET UP COMMAND JUMP
0462 FA15  B9 6A FA        LDA  VECTBL+1,Y
0463 FA18  85 9C           STA  CMDVEC+1
0464 FA1A  E8              INX                   ; INC INBUFF INDEX TO POINT TO FIRST
0465 FA1B  60              RTS                   ;  BYTE FOLLOWING COMMAND BYTE
```

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```
0467                ;        PHONE IS RINGING.  ANSWER IT ?
0468
0469 FA1C  57 12    RINGNG RMB  5,IER            ; DISABLE IRQ
0470 FA1E  07 10           RMB  0,IFR-1          ; RESET PA0 ( "PHONE IS RINGING" ) FLAG
0471 FA20  A9 A0           LDA  #$A0             ; SET MCR FOR SERIAL I/O
0472 FA22  85 14           STA  MCR
0473 FA24  A5 40           LDA  DEFPRO           ; SET SERIAL PROTOCOL TO MOST RECENT VALUE
0474 FA26  85 15           STA  SCCR
0475 FA28  A5 42           LDA  BDRATL           ; SET SERIAL CLOCK TO MOST RECENT VALUE
0476 FA2A  85 18           STA  CNTACL
0477 FA2C  A5 43           LDA  BDRATH
0478 FA2E  85 1A           STA  CNTAL
0479 FA30  A9 02           LDA  #$02             ; SET "STCODE" TO "RING" RESPONSE
0480 FA32  85 7D           STA  STCODE
0481 FA34  20 EB FE        JSR  RESPNS           ; AND OUTPUT APPROPRIATE MESSAGE
0482 FA37  E6 87           INC  S1               ; ADD 1 TO RING COUNTER
0483 FA39  A4 87           LDY  S1               ; NOW CHECK FOR RING COUNT
0484 FA3B  C4 86           CPY  S0               ; IS THE RING COUNT UP TO THE SET LIMIT YET ?
0485 FA3D  F0 03           BEQ  ANSWER           ; YES==> GO ANSWER THE PHONE !
0486 FA3F  4C 16 F8        JMP  RESTRT           ; NO==> START OVER READING IN CHARS FROM HOST SYSTEM
0487
0488 FA42  F7 78    ANSWER SMB  7,IRQFLG         ; CHANGE ISR TO PROCESS DELAY TIME FOR WAIT-FOR-CARRIER
0489 FA44  20 0D FC        JSR  AAA              ; NOW GO ANSWER PHONE  ( "JSR" WILL PUT 2 RETURN
0490                                             ;   ADDRESS BYTES ON THE STACK.  THESE WILL BE
0491                                             ;   DISCARDED AT THE END OF THE <CR> COMMAND
0492                                             ;   -- AT LABLE "NOWAIT" -- FOLLOWED BY
0493                                             ;   A "JMP RESTRT" )
```

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```
0496                ;                  ----- THE ORDER OF THESE TWO TABLES MUST MATCH ----
0497 FA47  2C       CMDTBL .BYT  ','
0498 FA48  30              .BYT  '0123456789+@'
0499 FA54  3B              .BYT  $3B,'=?'
0500 FA57  41              .BYT  'ACDEFH'
0501 FA5D  49              .BYT  'IMOPQR'
0502 FA63  53              .BYT  'STVXZ'
0503 FA68  00              .BYT  $00             ; MARKER FOR <CR> COMMAND
```

```
0504
0505 FA69  1E FB     VECTBL .WOR   COMMA
0506 FA6B  3C FB            .WOR   DIGIT,DIGIT,DIGIT,DIGIT,DIGIT,DIGIT
0507 FA77  3C FB            .WOR   DIGIT,DIGIT,DIGIT,DIGIT,DIGIT,DIGIT
0508 FA83  5B FB            .WOR   SEMIC,EQUAL,QUESTN
0509 FA89  0D FC            .WOR   AAA,CCC,DDD,EEE,FFF,HHH
0510 FA95  BB FC            .WOR   III,MMM,OOO,PPP,QQQ,RRR
0511 FAA1  3A FD            .WOR   SSS,TTT,VVV,XXX,ZZZ
0512 FAAB  E0 FD            .WOR   CR                ; ---------> MUST BE LAST ENTRY IN TABLE
0513
0514
0515                ;  INITIAL VALUES FOR S-REGISTERS, IN ORDER FROM 0 TO 16
0516
0517 FAAD  00       STBL   .BYT   0,0,43,13,10
0518 FAB2  08              .BYT   8,2,30,02
0519 FAB6  06              .BYT   6,7,70,50
0520 FABA  FF              .BYT   $FF,$FF,$FF
0521 FABD  00              .BYT   0
```



```
0523                ;   THIS ROUTINE INITIALIZES PROGRAM VARIABLES AND
0524                ;    CPU REGISTERS.
0525
0526 FABE  A9 00    INITSW LDA    #$00               ; DISABLE ALL IRQS
0527 FAC0  85 11           STA    IFR
0528 FAC2  85 12           STA    IER
0529 FAC4  8D 0D 20        STA    XMTD               ; SET UP R2424 TO DEFAULT VALUES
0530 FAC7  8D 0B 20        STA    XMTB
0531 FACA  A9 04           LDA    #$04
0532 FACC  8D 0D 10        STA    RCVD
0533 FACF  A9 03           LDA    #$03
0534 FAD1  8D 0A 10        STA    RCVA
0535 FAD4  8D 0A 20        STA    XMTA
0536 FAD7  A9 08           LDA    #$08
0537 FAD9  8D 0C 10        STA    RCVC
0538 FADC  8D 0C 20        STA    XMTC
0539 FADF  8D 0E 10        STA    RCVE
0540 FAE2  8D 0E 20        STA    XMTE
0541
0542 FAE5  A9 00           LDA    #00
0543 FAE7  85 83           STA    SSETFG             ; SET FLAG TO INDICATE S-REG HAS NOT BEEN SET
0544 FAE9  85 87           STA    S1                 ; SET RING COUNT TO 0
0545 FAEB  85 7F           STA    XCODE              ; STANDARD "CARRIER" RESPONSE
0546 FAED  85 76           STA    DILFLG             ; DISABLE DIALING
0547 FAEF  85 7B           STA    RSLTFG             ; ENABLE RESULT RESPONSE
0548 FAF1  A9 80           LDA    #$80               ; ENABLE ECHO
0549 FAF3  85 79           STA    ECHOFG
0550 FAF5  85 7A           STA    DUPLEX             ; FULL DUPLEX
0551 FAF7  85 7E           STA    VCODE              ; SET UP FOR VERBAL RESPONSE
0552 FAF9  85 7C           STA    SPKRFG             ; SET SPEAKER FOR "M1" COMMAND OPERATION
0553 FAFB  A9 2F           LDA    #<BAUD12           ; SET DEFAULT BAUD RATE TO 1200 BAUD
0554 FAFD  85 42           STA    BDRATL
0555 FAFF  A9 00           LDA    #>BAUD12
0556 FB01  85 43           STA    BDRATH
```

```
0557 FB03   A9 C0          LDA   #$C0          ; SET DEFAULT SERIAL PROTOCOL TO 8 BITS, NO PARITY
0558 FB05   85 40          STA   DEFPRO
0559 FB07   A9 86          LDA   #<S0          ; BASE POINTER FOR S-REGISTERS
0560 FB09   85 84          STA   SREGP
0561 FB0B   A9 00          LDA   #>S0          ; SET UP HIGH-BYTE OF S-REG POINTER
0562 FB0D   85 85          STA   SREGP+1
0563 FB0F   A0 11          LDY   #17           ; INITIALIZE S-REGS
0564 FB11   B9 AD FA  SLOOP LDA   STBL,Y
0565 FB14   91 84          STA   (SREGP),Y
0566 FB16   88             DEY
0567 FB17   10 FB          BPL   SLOOP
0568 FB19   A5 89          LDA   S3
0569 FB1B   85 4C          STA   INBUFF        ; INITIALIZE COMMAND STRING TO [NULL]
0570 FB1D   60             RTS
0571                       .FILE MDM10B


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0573                  ; THE FOLLOWING ARE ALL THE COMMAND ROUTINES TO EXECUTE THE
0574                  ;  "AT" COMMANDS....
0575
0576
0577                  ;  "," COMMAND   --- WAIT FOR ONE PAUSE TIME
0578
0579 FB1E   86 9D     COMMA  STX   TEMP          ; SAVE INBUFF POINTER
0580 FB20   A6 8E            LDX   S8            ; GET VALUE OF S-REG 8 ( DELAY TIME )
0581 FB22   F0 15            BEQ   NODLAY        ; IF ZERO THEN NO DELAY
0582 FB24   A9 9C            LDA   #<DLYTIM
0583 FB26   85 1C            STA   CNTBCL        ; START TIMER-B
0584 FB28   A9 E0            LDA   #>DLYTIM
0585 FB2A   85 1E            STA   CNTBHL
0586 FB2C   A0 10     ONESEC LDY   #DLYHIB
0587 FB2E   5F 11 FD  WAITB  BBR   5,IFR,WAITB   ; IS TIMER B DONE YET ?
0588 FB31   A5 1C            LDA   CNTBCL        ; YES ==> CLEAR TIMER FLAG
0589 FB33   88               DEY                 ; DONE COUNTING YET ?
0590 FB34   D0 F8            BNE   WAITB         ; NO ==> KEEP GOING
0591 FB36   CA               DEX                 ; ANY MORE 1-SEC DELAYS ?
0592 FB37   D0 F3            BNE   ONESEC        ; YES==> ONE MORE TIME ....
0593 FB39   A6 9D     NODLAY LDX   TEMP          ; RESTORE INBUFF POINTER
0594 FB3B   60               RTS
0595
0596                  ;*************************************************************************
0597
0598
0599                  ; DIAL A NUMBER
0600
0601 FB3C   7F 76 15  DIGIT  BBR   7,DILFLG,DIGERR ; IF NUMBER IS NOT TO BE DIALED --> ERROR
0602 FB3F   A9 01            LDA   #$01          ; WAIT UNTIL DIAL BUFFER EMPTY
0603 FB41   2C 0E 20  WAITRE BIT   XMTE
0604 FB44   F0 FB            BEQ   WAITRE
0605 FB46   B5 4B            LDA   INBUFF-1,X    ; GET ASCII NUMBER FROM BUFFER.  IN THIS CASE, THE
0606                                              ;  COMMAND BYTE IS THE PARAMETER.  SINCE THE X-REG
0607                                              ;  HAS ALREADY BEEN UPDATED TO POINT TO THE BYTE
0608                                              ;  FOLLOWING THIS DIGIT/COMMAND, THE BASE OF THE
0609                                              ;  COMMAND BUFFER HAS TO BE SHIFTED DOWN ONE BYTE
```

```
0610                                            ;  TO COMPENSATE.
0611 FB48  C9 23          CMP   #'#'            ; IS THE DIAL DIGIT A "#" ?
0612 FB4A  D0 02          BNE   DIG2            ; NO ==> BRANCH
0613 FB4C  A9 0E          LDA   #$0E            ; YES==> EXCHANGE CHAR FOR R2424'S "#" NUMBER
0614 FB4E  29 0F    DIG2  AND   #$0F            ; MAKE IT ABSOLUTE
0615 FB50  8D 00 20       STA   XMTO            ;  AND DIAL ...
0616 FB53  60       QDIGIT RTS
0617
0618 FB54  A9 04    DIGERR LDA  #04             ;   "ERROR "
0619 FB56  85 7D          STA   STCODE
0620 FB58  4C E0 FD       JMP   CR              ; TERMINATE COMMAND STRING PROCESSING
0621
0622               ;*************************************************************************
0623
0624
0625               ; SEMICOLON COMMAND   ---   DONE DIALING - RETURN TO COMMAND MODE
0626
0627 FB5B  7F 76 11 SEMIC  BBR   7,DILFLG,SEMERR  ; BRANCH IF ";" ENTERED WHILE NOT DIALING (ERROR)
0628 FB5E  06 76          ASL   DILFLG          ; TURN OFF DIAL FLAG ( $80 --> $00 )
0629 FB60  A9 01          LDA   #01             ; WAIT UNTIL DIAL REGISTER IS EMPTY
0630 FB62  2C 0E 20 SEMI2 BIT   XMTE            ; EMPTY YET ?
0631 FB65  F0 FB          BEQ   SEMI2           ; NO ==> KEEP WAITING
0632 FB67  A9 FF          LDA   #$FF            ; YES==> FINISH DIALING
0633 FB69  8D 00 20       STA   XMTO
```



```
0634 FB6C  77 80          RMB   7,WAITFG        ; PREVENT <CR> COMMAND FROM GOING ON-LINE (REMAIN IN
0635 FB6E  60             RTS                   ;   COMMAND MODE)
0636
0637 FB6F  A9 04    SEMERR LDA  #$04            ; SET STCODE FOR ERROR
0638 FB71  85 7D          STA   STCODE
0639 FB73  4C E0 FD       JMP   CR              ;  ... AND TERMINATE COMMAND STRING EXECUTION
0640
0641               ;*************************************************************************
0642
0643               ; "=" COMMAND   ---   SET S-REGISTER TO A VALUE
0644
0645 FB76  7F 83 DB EQUAL  BBR   7,SSETFG,DIGERR  ; IF FLAG IS CLEAR --> "ERROR"
0646 FB79  A9 00          LDA   #00             ; CLEAR OUT TEMP BUFFER
0647 FB7B  85 98          STA   NUM
0648 FB7D  85 99          STA   NUM+1
0649 FB7F  85 9A          STA   NUM+2
0650 FB81  20 8E FD       JSR   GETNUM          ; GET FIRST CHAR FROM BUFFER
0651 FB84  B0 36          BCS   EQ4             ; IF IT IS NOT A NUMBER, THEN ASSUME ZERO
0652 FB86  85 98          STA   NUM             ; SAVE NUMBER IN TEMP BUFF
0653 FB88  20 8E FD       JSR   GETNUM          ; IS THERE ANOTHER NUMBER ?
0654 FB8B  B0 15          BCS   EQ2             ; NO ==> ONES DIGIT ONLY --> BRANCH
0655 FB8D  A4 98          LDY   NUM             ; YES==> MOVE ONES DIGIT OVER
0656 FB8F  84 99          STY   NUM+1           ;        AND INSERT TENS DIGIT
0657 FB91  85 98          STA   NUM
0658 FB93  20 8E FD       JSR   GETNUM          ; IS THERE A THIRD NUMBER ( HUNDREDS DIGIT ) ?
0659 FB96  B0 0A          BCS   EQ2             ; NO ==> ALL NUMBERS FETCHED --> BRANCH
0660 FB98  A4 99          LDY   NUM+1           ; YES==> MOVE ONES AND TENS DIGITS
```

```
0661 FB9A  84 9A        STY   NUM+2          ;        OVER AND INSERT HUNDREDS
0662 FB9C  A4 98        LDY   NUM            ;        DIGIT IN FRONT
0663 FB9E  84 99        STY   NUM+1
0664 FBA0  85 98        STA   NUM
0665 FBA2  A5 99   EQ2  LDA   NUM+1          ; GET TENS DIGIT
0666 FBA4  F0 07        BEQ   EQ3            ; IGNORE IT IF IT'S ZERO
0667 FBA6  20 EC FB     JSR   MULT10         ; IF > 0 , MULTIPLY BY 10
0668 FBA9  65 98        ADC   NUM            ; ADD IN ONES DIGIT
0669 FBAB  85 98        STA   NUM            ; AND SAVE TENS+ONES
0670 FBAD  A5 9A   EQ3  LDA   NUM+2          ; GET HUNDREDS DIGIT; IS IT = 0 ?
0671 FBAF  F0 0B        BEQ   EQ4            ; YES==> FINISHED CONVERTING TO HEX
0672 FBB1  20 EC FB     JSR   MULT10         ; NO ==> MULTIPLY HUNDREDS DIGIT BY 10
0673 FBB4  20 EC FB     JSR   MULT10         ;  AND BY 10  AGAIN  ( * 100  )
0674 FBB7  18           CLC
0675 FBB8  65 98        ADC   NUM            ;  ADD IN TENS+ONES DIGIT
0676 FBBA  85 98        STA   NUM
0677 FBBC  A5 98   EQ4  LDA   NUM
0678 FBBE  A0 00        LDY   #00
0679 FBC0  91 84        STA   (SREGP),Y      ; SAVE TOTAL HEX VALUE
0680 FBC2  A5 96        LDA   S16            ; GO TO SELF-TEST ?
0681 FBC4  D0 12        BNE   SLFTST         ; NO => STOP SELF TEST
0682 FBC6  A9 EF   NOSLFT LDA   #$EF         ; NO SELF TEST -- RETURN TO NORMAL OPERATING MODE
0683 FBC8  2D 0A 10     AND   RCVA           ;  DISABLE SELF-TEST BITS IN R2424
0684 FBCB  8D 0A 10     STA   RCVA
0685 FBCE  A9 EF        LDA   #$EF
0686 FBD0  2D 0A 20     AND   XMTA
0687 FBD3  8D 0A 20     STA   XMTA
0688 FBD6  D0 10        BNE   QEQ            ; ( BRANCH ALWAYS )
0689
0690 FBD8  A9 10   SLFTST LDA   #$10         ; START SELF-TEST
0691 FBDA  0D 0A 10     ORA   RCVA           ;  SET SELF-TEST BITS IN R2424
0692 FBDD  8D 0A 10     STA   RCVA
0693 FBE0  A9 10        LDA   #$10
0694 FBE2  0D 0A 20     ORA   XMTA
```



```
0695 FBE5  8D 0A 20     STA   XMTA
0696 FBE8  20 CB FD  QEQ  JSR   NEWCXR       ; UPDATE R2424 SCRATCH-PAD REGISTERS
0697 FBEB  60           RTS
0698
0699 FBEC  85 9D   MULT10 STA   TEMP         ; SAVE VALUE IN TEMP STORAGE
0700 FBEE  0A           ASL   A              ; MULTIPLY BY 2   ( * 2 )
0701 FBEF  0A           ASL   A              ;  AND BY 2 AGAIN ( * 4 )
0702 FBF0  65 9D        ADC   TEMP           ; THEN ADD IN ORIGINAL VALUE  ( CARRY FLAG ALWAYS CLEAR )
0703 FBF2  0A           ASL   A              ; MULTIPLY BY 2 AGAIN ( * 10 )
0704 FBF3  60           RTS
0705
0706               ;*********************************************************************************
0707
0708               ; "?" COMMAND  ---  SEND BACK CONTENTS OF S-REGISTER
0709
0710 FBF4  20 40 FF  QUESTN JSR   CRLF       ; PREFACE OUTPUT WITH <CR/LF>
0711 FBF7  A0 00        LDY   #00
```

```
0712 FBF9  B1 84          LDA   (SREGP),Y        ; GET VALUE OF S-REG
0713 FBFB  20 9F FD       JSR   HX2ASC           ; AND CONVERT IT TO ASCII
0714 FBFE  A0 02          LDY   #02              ; SEND OUT 3 CHARS
0715 FC00  B9 98 00  QUES3 LDA  NUM,Y            ; GET CHAR FROM "NUM" BUFFER
0716 FC03  20 51 FF       JSR   CHROUT
0717 FC06  88             DEY                    ; LAST CHAR ?
0718 FC07  10 F7          BPL   QUES3            ; NO ==> SEND OUT NEXT ONE
0719 FC09  20 40 FF       JSR   CRLF             ; YES==> SEND OUT <CR/LF>
0720 FC0C  60             RTS
0721
0722               ;*************************************************************************
0723
0724               ; "A" COMMAND  ---  SET MODEM TO ANSWER AN INCOMING CALL
0725
0726 FC0D  20 95 FC  AAA  JSR   H1AND2           ; PICK UP PHONE ( GO OFF-HOOK )
0727 FC10  A9 10          LDA   #$10             ; SET R2424 TO ANSWER MODE
0728 FC12  0D 0D 20       ORA   XMTD
0729 FC15  8D 0D 20       STA   XMTD
0730 FC18  A9 DF          LDA   #$DF             ; SET "ORG" BIT TO 0
0731 FC1A  2D 09 20       AND   XMT9
0732 FC1D  8D 09 20       STA   XMT9
0733 FC20  20 CE FD       JSR   NEWCX            ; UPDATE R2424 STATUS
0734 FC23  F7 80          SMB   7,WAITFG         ; SET FLAG TO INDICATE WE ARE TO WAIT FOR CARRIER
0735 FC25  4C EE FD       JMP   CR2              ;  AND GO DIRECTLY TO CARRIER-DETECT
0736                                             ;  -- DO NOT ACCEPT ANY MORE COMMANDS
0737
0738               ;*************************************************************************
0739
0740               ; "C" COMMAND  --- TOGGLE TRANSMITTER
0741
0742
0743 FC28  20 8E FD  CCC  JSR   GETNUM          ; GET PARAMETER, IF ANY
0744 FC2B  B0 0B          BCS   CCZERO           ; BRANCH IF NO PARAMETER ( ASSUME ZERO )
0745 FC2D  F0 09          BEQ   CCZERO           ; BRANCH IF PARAMETER = 0
0746 FC2F  A9 04    CCONE LDA   #04              ; PARAMETER =1 --> TURN ON "CC" BIT
0747 FC31  0D 09 20       ORA   XMT9             ;  IN MODEM REGISTER
0748 FC34  D0 07          BNE   QCCC
0749 FC36  D0 05          BNE   QCCC             ; ( BRANCH ALWAYS )
0750 FC38  A9 FB    CCZERO LDA  #$FB             ; PARAMETER =0 --> TURN OFF "CC" BIT
0751 FC3A  2D 09 20       AND   XMT9
0752 FC3D  8D 09 20  QCCC STA   XMT9
0753 FC40  20 CE FD       JSR   NEWCX            ; UPDATE MODEM REGISTERS
0754 FC43  60             RTS
0755
```



```
0756               ;*************************************************************************
0757
0758               ;  "D" COMMAND  ---  DIAL A NUMBER
0759
0760 FC44  A9 20    DDD   LDA   #$20             ; PUT MODEM IN ORIGINATE MODE
0761 FC46  0D 09 20       ORA   XMT9             ; AND SET TO DIAL
0762 FC49  8D 09 20       STA   XMT9
```

```
0763 FC4C  AD 0D 20          LDA   XMTD
0764 FC4F  29 EF             AND   #$EF
0765 FC51  09 48             ORA   #$48
0766 FC53  8D 0D 20          STA   XMTD              ; SET CRQ=1 AND DTR=1
0767 FC56  20 CE FD          JSR   NEWCX             ; UPDATE TRANSMITTER REGISTERS
0768 FC59  2C 08 20    WAITDL BIT   XMT8
0769 FC5C  10 FB             BPL   WAITDL            ; WAIT UNTIL DLO=1
0770 FC5E  A5 8E             LDA   S8                ; DELAY "S6" NUMBER OF SECONDS.   USE "COMMA"
0771 FC60  48                PHA                     ;  COMMAND FOR DELAY ROUTINE.  TO DO THIS, WE HAVE TO
0772 FC61  A5 8C             LDA   S6                ;  SAVE THE ORIGINAL VALUE OF "S8" ( IN THIS CASE ON
0773 FC63  85 8E             STA   S8                ;  THE STACK ) AND THEN SUBSTITUTE THE VALUE FOR "S6"
0774 FC65  20 1E FB          JSR   COMMA             ;  INTO "S8".  THIS WILL DELAY "S6" SECONDS.  AFTER
0775 FC68  68                PLA                     ;  THE DELAY IS FINISHED, WE POP THE ORIGINAL "S8"
0776 FC69  85 8E             STA   S8                ;  VALUE OFF THE STACK AND RETURN IT TO "S8".
0777 FC6B  F7 76             SMB   7,DILFLG          ; SET "DIAL FLAG" TO DIAL SUBSEQUENT NUMBERS
0778 FC6D  F7 80             SMB   7,WAITFG          ; ENABLE WAIT-FOR-CARRIER DELAY
0779 FC6F  77 77             RMB   7,REVFLG          ; SET FOR NORMAL DIALING
0780 FC71  60                RTS
0781
0782                   ;*************************************************************************
0783
0784                   ; "E" COMMAND   ---   TOGGLE ECHOING CHARS BACK TO HOST SYSTEM
0785
0786 FC72  20 8E FD    EEE   JSR   GETNUM              ; GET PARAMETER, IF ANY
0787 FC75  B0 06             BCS   EZERO             ; BRANCH IF NO PARAMETER ( ASSUME ZERO )
0788 FC77  F0 04             BEQ   EZERO             ; BRANCH IF PARAMETER = 0
0789 FC79  F7 79       EONE  SMB   7,ECHOFG          ; SET ECHO FLAG
0790 FC7B  D0 02             BNE   QECHO             ; ( BRA )
0791 FC7D  77 79       EZERO RMB   7,ECHOFG          ; CLEAR ECHO FLAG ( NO ECHO )
0792 FC7F  60          QECHO RTS
0793
0794                   ;*************************************************************************
0795
0796                   ; "F" COMMAND   ---   SET HALF/FULL DUPLEX
0797
0798 FC80  20 8E FD    FFF   JSR   GETNUM              ; GET PARAMETER, IF ANY
0799 FC83  B0 06             BCS   FZERO             ; IF NONE, ASSUME ZERO
0800 FC85  F0 04             BEQ   FZERO             ; BRANCH IF = 0
0801 FC87  F7 7A       FONE  SMB   7,DUPLEX          ; SET FOR FULL DUPLEX
0802 FC89  D0 02             BNE   QFFF              ; ( BRANCH ALWAYS )
0803 FC8B  77 7A       FZERO RMB   7,DUPLEX          ; SET FOR HALF DUPLEX
0804 FC8D  60          QFFF  RTS
0805
0806                   ;*************************************************************************
0807
0808                   ; "H" COMMAND   ---   ON/OFF HOOK
0809
0810 FC8E  20 8E FD    HHH   JSR   GETNUM              ; GET PARAMETER, IF ANY
0811 FC91  B0 14             BCS   HHZERO            ; IF NO PARAMETER, ASSUME ZERO
0812 FC93  F0 12             BEQ   HHZERO            ; BRANCH IF PARAMETER = 0
0813 FC95  AD 0D 20    H1AND2 LDA   XMTD              ; PARAMETER MUST BE 1 OR 2 (ON THE R2424, THEY
0814                                                  ;  FUNCTION THE SAME)
0815 FC98  09 40             ORA   #$40
0816 FC9A  8D 0D 20          STA   XMTD              ; SET XMIT CRQ = 1
```

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```
0817 FC9D  AD 0D 10          LDA   RCVD
0818 FCA0  09 40             ORA   #$40
0819 FCA2  8D 0D 10          STA   RCVD              ; SET RCV CRQ = 1
0820 FCA5  D0 10             BNE   HHSET             ; ( BRANCH ALWAYS )
0821 FCA7  AD 0D 20    HHZERO LDA   XMTD             ; GO OFF-LINE  ( HANG UP )
0822 FCAA  29 AF             AND   #$AF
0823 FCAC  8D 0D 20          STA   XMTD              ; SET XMIT CRQ = 0
0824 FCAF  AD 0D 10          LDA   RCVD
0825 FCB2  29 BF             AND   #$BF
0826 FCB4  8D 0D 10          STA   RCVD              ; SET RCV CRQ = 0
0827 FCB7  20 CB FD    HHSET JSR   NEWCXR            ; UPDATE MODEM'S INTERNAL REGISTERS
0828 FCBA  60          QHHH  RTS
0829
0830
0831                   ;*************************************************************************
0832
0833                   ; "I" COMMAND  ---  RESPOND WITH CHECKSUM OR PRODUCT CODE
0834
0835 FCBB  20 40 FF    III   JSR   CRLF              ; MOVE DOWN TO NEXT LINE
0836 FCBE  20 8E FD          JSR   GETNUM            ; GET PARAMETER, IF ANY
0837 FCC1  B0 06             BCS   IIZERO            ; BRANCH IF NO PARAMETER ( ASSUME ZERO )
0838 FCC3  F0 04             BEQ   IIZERO            ; BRANCH IF PARAMTER = 0
0839 FCC5  A0 2D       IIONE LDY   #CHKSUM-MSG       ; SEND OUT CHECKSUM
0840 FCC7  D0 02             BNE   QII
0841 FCC9  A0 31       IIZERO LDY   #PCODE-MSG       ; SEND OUT PRODUCT CODE
0842 FCCB  20 33 FF    QII   JSR   MSGOUT
0843 FCCE  60                RTS
0844
0845
0846                   ;*************************************************************************
0847
0848                   ; "M" COMMAND  ---  ENABLE/DISABLE SPEAKER
0849
0850 FCCF  77 7C       MMM   RMB   7,SPKRFG          ; DISABLE SPEAKER FLAG
0851 FCD1  20 8E FD          JSR   GETNUM            ; GET PARAMETER, IF ANY
0852 FCD4  B0 0D             BCS   MMZERO            ; IF NONE, ASSUME ZERO
0853 FCD6  F0 0B             BEQ   MMZERO            ;  BRANCH IF = 0
0854 FCD8  C9 01             CMP   #01               ; IS IT ONE ?
0855 FCDA  D0 02             BNE   MMTWO             ; NO ==> LEAVE SPEAKER FLAG DISABLED
0856 FCDC  F7 7C       MMONE SMB   7,SPKRFG          ; YES==> ENABLE FLAG TO TURN SPEAKER OFF AT CARRIER TONE
0857 FCDE  67 01       MMTWO RMB   6,PB              ;  TURN ON SPEAKER
0858 FCE0  4C E5 FC          JMP   QMMM
0859 FCE3  E7 01       MMZERO SMB   6,PB             ; DISABLE SPEAKER
0860 FCE5  60          QMMM  RTS
0861
0862
0863                   ;*************************************************************************
0864
0865
0866                   ; "O" COMMAND  ---  GO ON-LINE
0867
0868 FCE6  20 95 FC    OOO   JSR   H1AND2            ; PICK UP PHONE  ( GO OFF-HOOK )
C869 FCE9  F7 80             SMB   7,WAITFG          ; ENABLE CARRIER TEST
0870 FCEB  4C F6 FD          JMP   CARTIM            ;  AND GO DIRECTLY TO CARRIER-DETECT ...
```

```
0871
0872                    ;*****************************************************************************
0873
0874                    ;  "P" COMMAND   ---   PULSE DIAL
0875
0876 FCEE  AD 0B 20     PPP    LDA    XMTB              ; SET PULSE/TONE BIT TO 0
0877 FCF1  29 FD               AND    #$FD
```



```
0878 FCF3  8D 0B 20             STA    XMTB
0879 FCF6  20 CE FD             JSR    NEWCX             ; UPDATE TRANSMITTER REGISTERS
0880 FCF9  60                   RTS
0881
0882                    ;*****************************************************************************
0883
0884                    ;  "Q" COMMAND   ---   TOGGLE SENDING RESULT CODE/MESSAGE
0885
0886 FCFA  20 BE FD     QQQ    JSR    GETNUM            ; GET PARAMETER, IF ANY
0887 FCFD  B0 06               BCS    QQZERO            ; BRANCH IF NO PARAMETER ( ASSUME ZERO )
0888 FCFF  F0 04               BEQ    QQZERO            ; BRANCH IF PARAMETER = 0
0889 FD01  F7 7B        QQONE  SMB    7,RSLTFG          ; SET FLAG  ( ENABLE PROMPTS )
0890 FD03  D0 02               BNE    QQ                ; ( BRA )
0891 FD05  77 7B        QQZERO RMB    7,RSLTFG          ; CLEAR FLAG  ( DISABLE PROMPTS )
0892 FD07  60           QQ     RTS
0893
0894                    ;*****************************************************************************
0895
0896                    ; "R" COMMAND   ---   SET DIAL FOR REVERSE MODE
0897                    ;               ( TO DIAL AN ORIGINATE-ONLY MODEM )
0898
0899 FD08  7F 76 28     RRR    BBR    7,DILFLG,RERROR   ; BRANCH IF "R" ENTERED WHILE NOT DIALING (ERROR)
0900 FD0B  A5 41               LDA    BAUD              ; ARE WE RUNNING AT 2400 BAUD ?
0901 FD0D  C9 18               CMP    #24
0902 FD0F  F0 21               BEQ    QRRR              ; YES==> "REVERSE" MODE NOT EASILY DONE AT 2400 SINCE
0903                                                     ;        "ANSWER" TONE GOES AWAY AFTER 3 SECONDS.
0904 FD11  77 76               RMB    7,DILFLG          ; NO ==> 300/1200 --> DISABLE FURTHER DIALING
0905 FD13  F7 77               SMB    7,REVFLG          ; SET FLAG TO INDICATE REVERSE DIALING
0906 FD15  A9 20               LDA    #$20              ; SET "ORG" BIT TO 1
0907 FD17  0D 09 20            ORA    XMT9
0908 FD1A  8D 09 20            STA    XMT9
0909 FD1D  A9 BF               LDA    #$BF              ; SET RECEIVER'S "CRQ" BIT TO 0
0910 FD1F  2D 0D 10            AND    RCVD
0911 FD22  8D 0D 10            STA    RCVD
0912 FD25  A9 BF               LDA    #$BF              ; SET TRANSMITTER'S "CRQ" BIT TO 0
0913 FD27  2D 0D 20            AND    XMTD
0914 FD2A  09 20               ORA    #$20              ;   AND "DATA" BIT TO 1
0915 FD2C  8D 0D 20            STA    XMTD
0916 FD2F  20 CB FD            JSR    NEWCXR            ; UPDATE REGISTERS
0917 FD32  60           QRRR   RTS                      ;  AND RETURN .....
0918
0919 FD33  A9 04        RERROR LDA    #$04              ; SET STCODE FOR ERROR
0920 FD35  85 7D               STA    STCODE
0921 FD37  4C E0 FD            JMP    CR                ;    AND TERMINATE COMMAND STRING EXECUTION
```

```
0922
0923                    ;*************************************************************************
0924
0925                    ; "S" COMMAND   ---   IDENTIFY S-REGISTER FOR FUTURE ACCESS
0926
0927 FD3A  A9 86        SSS     LDA     #<S0            ; START WITH BASE ADDRESS
0928 FD3C  85 84                STA     SREGP
0929 FD3E  20 8E FD             JSR     GETNUM          ; GET NUMBER OF S-REGISTER
0930 FD41  B0 14                BCS     QSSS            ; BRANCH IF NO PARAMETER FOUND
0931 FD43  F0 12                BEQ     QSSS            ; BRANCH IF PARAMETER = 0 ( ALREADY SET UP )
0932 FD45  85 98                STA     NUM             ;  SAVE VALUE
0933 FD47  20 8E FD             JSR     GETNUM          ; GET ONES DIGIT, IF ANY
0934 FD4A  B0 04                BCS     SS2             ; BRANCH IF ONLY ONE DIGIT
0935 FD4C  69 0A                ADC     #10             ; TENS DIGIT COULD ONLY BE A "1"
0936 FD4E  85 98                STA     NUM
0937 FD50  A5 98        SS2     LDA     NUM
0938 FD52  18                   CLC
```



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0939 FD53  65 84                ADC     SREGP           ; ADD IN BASE ADDRESS
0940 FD55  85 84                STA     SREGP           ;  AND STORE IN POINTER
0941 FD57  F7 83        QSSS    SMB     7,SSETFG        ; SET FLAG TO INDICATE AN S-REG HAS BEEN SET
0942 FD59  60                   RTS
0943
0944                    ;*************************************************************************
0945
0946                    ; "T" COMMAND   ---   TOUCH-TONE DIAL
0947
0948 FD5A  AD 0B 20     TTT     LDA     XMTB            ; SET PULSE/TONE BIT TO 1
0949 FD5D  09 02                ORA     #$02
0950 FD5F  8D 0B 20             STA     XMTB
0951 FD62  20 CE FD             JSR     NEWCX           ; UPDATE TRANSMITTER REGISTERS
0952 FD65  60                   RTS
0953
0954                    ;*************************************************************************
0955
0956                    ; "V" COMMAND   ---   SET VERBAL/NUMERIC RESPONSE
0957
0958 FD66  20 8E FD     VVV     JSR     GETNUM          ; GET PARAMETER, IF ANY
0959 FD69  B0 06                BCS     VZERO           ; IF NONE, ASSUME ZERO
0960 FD6B  F0 04                BEQ     VZERO           ; BRANCH IF = 0
0961 FD6D  F7 7E        VONE    SMB     7,VCODE         ; SET FOR VERBAL RESPONSE
0962 FD6F  D0 02                BNE     QVVV            ; ( BRANCH ALWAYS )
0963 FD71  77 7E        VZERO   RMB     7,VCODE         ; SET FOR NUMERIC RESPONSE
0964 FD73  60           QVVV    RTS
0965
0966                    ;*************************************************************************
0967
0968                    ; "X" COMMAND   ---   ENABLE/DISABLE EXTENDED RESPONSE CODES
0969
0970 FD74  20 8E FD     XXX     JSR     GETNUM          ; GET PARAMETER, IF ANY
0971 FD77  B0 06                BCS     XZERO           ; ASSUME ZERO, IF NONE
0972 FD79  F0 04                BEQ     XZERO           ; BRANCH IF = 0
```

```
0973 FD7B  F7 7F     XONE   SMB   7,XCODE          ; SET FOR EXTENDED CODES
0974 FD7D  D0 02            BNE   QXXX
0975 FD7F  77 7F     XZERO  RMB   7,XCODE          ; SET FOR NORMAL CODES
0976 FD81  60        QXXX   RTS
0977
0978               ;*************************************************************************
0979
0980               ;  "Z" COMMAND  ---  SOFTWARE RESET
0981
0982 FD82  20 E8 FE  ZZZ    JSR   RESPNS          ; SEND OUT RESPONSE, IF ENABLED
0983 FD85  20 40 FF         JSR   CRLF
0984 FD88  7F 16 FD  ZZWAIT BBR   7,SCSR,ZZWAIT   ; WAIT UNTIL ALL CHARS HAVE BEEN SENT OUT
0985 FD8B  4C 00 F8         JMP   RESET           ; THEN RESTART


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0987               ; CHECK THE NEXT CHAR IN "INBUFF".  IF IT IS AN ASCII NUMBER (0-9),
0988               ;    FETCH IT, MASK OFF MSN, INCREMENT COMMAND STRING POINTER  ( REG-X ),
0989               ;    CLEAR CARRY AND RETURN.
0990               ;  IF CHAR IS NOT A NUMBER, SET CARRY AND RETURN.
0991
0992 FD8E  B5 4C     GETNUM LDA   INBUFF,X         ; GET CHAR FROM BUFFER
0993 FD90  C9 30            CMP   #'0'             ; IS IT LESS THAN '0' ?
0994 FD92  90 09            BCC   NOTNUM          ; YES==> QUIT
0995 FD94  C9 3A            CMP   #'9'+1          ; NO ==> IS IT GREATER THAN '9' ?
0996 FD96  B0 06            BCS   QGETN           ; YES==> QUIT
0997 FD98  E8               INX                   ; NO ==> INCREMENT INBUFF POINTER
0998 FD99  29 0F            AND   #$0F            ; MASK OFF TOP-MOST 4 BITS
0999 FD9B  90 01            BCC   QGETN           ; AND RETURN
1000 FD9D  38        NOTNUM SEC                   ; INDICATE CHAR IS NOT AN ASCII NUMBER
1001 FD9E  60        QGETN  RTS                   ; AND RETURN
1002               ;*************************************************************************
1003               ;  ROUTINE TO CONVERT FROM HEX BYTE TO 3-DIGIT ASCII DECIMAL
1004               ;    ( PAGE 154 '6502 SOFTWARE DESIGN' ) .
1005
1006 FD9F  A0 00     HX2ASC LDY   #00
1007 FDA1  C9 64     HX2    CMP   #100             ; FIND NUMBER OF HUNDREDS
1008 FDA3  90 05            BCC   GOTHUN
1009 FDA5  E9 64            SBC   #100
1010 FDA7  C8               INY
1011 FDA8  D0 F7            BNE   HX2
1012 FDAA  20 C4 FD  GOTHUN JSR   HCONV            ; CONVERT TO ASCII
1013 FDAD  84 9A            STY   NUM+2           ; AND SAVE IT
1014 FDAF  A0 00            LDY   #00
1015 FDB1  C9 0A     HX3    CMP   #10              ; FIND NUMBER OF TENS
1016 FDB3  90 05            BCC   GOTTEN
1017 FDB5  E9 0A            SBC   #10
1018 FDB7  C8               INY
1019 FDB8  D0 F7            BNE   HX3
1020 FDBA  20 C4 FD  GOTTEN JSR   HCONV            ; CONVERT TO ASCII
1021 FDBD  84 99            STY   NUM+1           ; SAVE TENS DIGIT
1022 FDBF  09 30            ORA   #$30
1023 FDC1  85 98            STA   NUM             ; SAVE ONES DIGIT
1024 FDC3  60               RTS
1025
```

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1026 FDC4  48          HCONV  PHA
1027 FDC5  98                 TYA
1028 FDC6  09 30              ORA   #$30              ; CONVERT ABSOLUTE NUMBER TO ASCII
1029 FDC8  A8                 TAY
1030 FDC9  68                 PLA
1031 FDCA  60                 RTS
1032                   ;*********************************************************************
1033
1034 FDCB  20 D7 FD    NEWCXR JSR   NEWCR              ; UPDATE BOTH RECEIVER AND TRANSMITTER REGS
1035
1036 FDCE  A9 08       NEWCX  LDA   #$08               ; UPDATE MODEM'S TRANSMITTER REGISTERS
1037 FDD0  0D 0E 20           ORA   XMTE
1038 FDD3  8D 0E 20           STA   XMTE
1039 FDD6  60                 RTS
1040
1041 FDD7  A9 08       NEWCR  LDA   #$08               ; UPDATE MODEM'S RECEIVER REGISTERS
1042 FDD9  0D 0E 10           ORA   RCVE
1043 FDDC  8D 0E 10           STA   RCVE
1044 FDDF  60                 RTS
```

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```
1046                   ;*********************************************************************
1047                   ; "<CR>" COMMAND  ---   CARRIAGE RETURN:  SEND OUT RESPONSE MESSAGE
1048                   ;                        OR GO INTO DATA MODE IF REQUESTED AND
1049                   ;                        IF CARRIER SIGNAL ACTIVE.
1050
1051 FDE0  A5 7D       CR     LDA   STCODE             ; CHECK STATUS OF PREVIOUS COMMANDS
1052 FDE2  D0 31              BNE   HOP                ; BRANCH IF NOT "OK"
1053 FDE4  7F 80 2E           BBR   7,WAITFG,HOP       ; BRANCH IF WE ARE NOT TO WAIT FOR A CARRIER SIGNAL
1054 FDE7  A9 01              LDA   #$01               ; WAIT UNTIL DIAL REGISTER IS EMPTY
1055 FDE9  2C 0E 20    WAITDB BIT   XMTE               ; EMPTY YET ?
1056 FDEC  F0 FB              BEQ   WAITDB             ; NO ==> CHECK AGAIN ...
1057 FDEE  FF 77 05    CR2    BBS   7,REVFLG,CARTIM    ; YES==> CHECK FOR "REVERSE" DIAL --> BRANCH IF
1058                                                   ;        WE ARE REVERSE DIALING ( DON'T CLOSE OUT DIALING JUST YET)
1059 FDF1  A9 FF              LDA   #$FF               ;  MUST BE 2400 OR NORMAL 300/1200 BAUD DIAL.
1060 FDF3  8D 00 20           STA   XMTO               ;   --> CLOSE DIAL MODE AND GO TO DATA MODE.
1061
1062                                                   ;    IF WE WERE AT 300 BAUD AND DIALING "REVERSE"
1063                                                   ;  MODE THEN WE WOULD HAVE TO WAIT FOR A CARRIER
1064                                                   ;  SIGNAL BEFORE REVERSING THE MODEM TO "ANSWER"
1065                                                   ;  MODE.  THEN WE WRITE AN $FF TO "XMTO" TO CLOSE
1066                                                   ;  OUT THE DIAL SEQUENCE.
1067
1068 FDF6  20 D3 FE    CARTIM JSR   STRTB3              ; START CNTR-B FOR SECONDS-LONG TIME INTERVAL
1069 FDF9  A5 8D              LDA   S7                 ; SET UP SECONDS COUNTER ( SET BY "COMMA" COMMAND )
1070 FDFB  85 46              STA   DELAYS
1071 FDFD  4F 01 18    WCARIR BBR   4,PB,GOTCAR        ; BRANCH IF CARRIER DETECTED
1072 FE00  8F 16 03           BBS   0,SCSR,NOCARR      ; BRANCH (EXIT) IF A KEY HAS BEEN TYPED
1073 FE03  7F 81 F7           BBR   7,WAITC,WCARIR     ; BRANCH IF WAIT TIME HAS NOT EXPIRED
1074 FE06  57 12       NOCARR RMB   5,IER              ; DISABLE TIMER B IRQ
```

```
1075 FE08  A5 1C           LDA   CNTBCL            ;  AND CLEAR CNTB FLAG
1076 FE0A  77 B0           RMB   7,WAITF6          ; TURN OFF WAIT FLAG
1077 FE0C  87 01           SMB   0,PB              ; DIRECT ALL OUTPUT TO HOST SYSTEM
1078 FE0E  A9 03           LDA   #$03              ; INDICATE "NO CARRIER"
1079 FE10  85 7D           STA   STCODE
1080 FE12  20 A7 FC        JSR   HHZERO            ; HANG UP THE PHONE ....
1081 FE15  4C AF FE  HOP   JMP   NOWAIT            ;  AND RETURN TO "RESTRT"
1082
1083 FE18  57 12     GOTCAR RMB   5,IER            ; GOT A CARRIER --> DISABLE TIMER B IRQ
1084 FE1A  A9 FF           LDA   #$FF              ; FINISH UP DIALING (IN CASE OF REVERSE DIAL)
1085 FE1C  8D 00 20        STA   XMTO
1086 FE1F  A9 01           LDA   #$01              ; INDICATE CARRIER DETECTED
1087 FE21  85 7D           STA   STCODE
1088 FE23  7F 7C 02        BBR   7,SPKRF6,GOTCR1   ; LEAVE SPEAKER ALONE IF FLAG IS NOT SET
1089 FE26  E7 01           SMB   6,PB              ; CARRIER DETECTED --> TURN SPEAKER OFF
1090 FE28  20 E8 FE  GOTCR1 JSR   RESPNS           ;  AND OUTPUT " CONNECT" MESSAGE, IF ENABLED
1091 FE2B  07 01           RMB   0,PB              ; THEN DIRECT ALL OUTPUT TO MODEM
1092 FE2D  A9 00     GOTCR2 LDA   #00               ; RESET ESCAPE CODE COUNTER
1093 FE2F  85 82           STA   ESCCNT
1094 FE31  20 BB FE  GOTCR3 JSR   STRTB1           ; START TIMER-B FOR GUARD-TIME COUNTER
1095 FE34  4F 01 11  INCHAR BBR   4,PB,INCHR2      ; BRANCH IF CARRIER STILL DETECTED
1096 FE37  20 C9 FE        JSR   STRTB2            ; CARRIER LOST --> WAIT FOR S10 TENTHS-OF-SECONDS
1097 FE3A  A5 90           LDA   S10               ;   FOR CARRIER TO RETURN -- OTHERWISE INDICATE
1098 FE3C  85 46           STA   DELAYS            ;   LOSS OF CARRIER AND RETURN TO COMMAND MODE
1099 FE3E  FF 81 C5  CARCK2 BBS   7,WAITC,NOCARR   ; BRANCH IF THE TIME-OUT FLAG GOES TRUE
1100 FE41  CF 01 FA        BBS   4,PB,CARCK2       ; BRANCH IF CARRIER STILL LOST
1101 FE44  A5 16           LDA   SCSR              ; CARRIER DETECTED AGAIN BEFORE TIME-OUT-->CLEAR SERIAL FLAGS
1102 FE46  57 12           RMB   5,IER             ; DISABLE IRQ
1103 FE48  A5 16     INCHR2 LDA   SCSR              ; WAIT FOR RECEIVED CHAR FROM HOST COMPUTER
1104 FE4A  29 0F           AND   #$0F              ; CHAR RECEIVED ?
1105 FE4C  F0 E6           BEQ   INCHAR            ; NO ==> CHECK AGAIN
1106 FE4E  4A        CHKCHR LSR   A                ; YES==> CHECK FOR PROPER RECEPTION
```



```
1107 FE4F  B0 06           BCS   CHKOK             ; BRANCH IF CHAR OK
1108 FE51  A9 04           LDA   #04               ; CHAR NOT OK --> ERROR ....
1109 FE53  85 7D           STA   STCODE
1110 FE55  D0 58           BNE   NOWAIT            ; INDICATE ERROR AND START OVER  ( BRA )
1111
1112 FE57  A5 17     CHKOK LDA   SRDR              ; CHAR OK --> FETCH IT
1113 FE59  20 51 FF        JSR   CHROUT            ;  AND SEND IT TO MODEM
1114 FE5C  FF 7A 0A        BBS   7,DUPLEX,ESCCHK   ; BRANCH IF CHAR IS NOT TO BE ECHOED BACK
1115 FE5F  87 01           SMB   0,PB              ; ECHO --> DIRECT OUTPUT TO HOST COMPUTER
1116 FE61  20 51 FF        JSR   CHROUT            ; ECHO CHAR BACK
1117 FE64  6F 16 FD  WAITDP BBR   6,SCSR,WAITDP    ; WAIT UNTIL CHAR IS SENT OUT
1118 FE67  07 01           RMB   0,PB              ;  AND REDIRECT OUTPUT BACK TO MODEM
1119
1120                 ;  NOW CHECK FOR POSSIBLE ESCAPE CODE SEQUENCE ....
1121
1122 FE69  C5 88     ESCCHK CMP   S2               ; WAS CHAR AN "ESCAPE" CHAR ?
1123 FE6B  D0 C4           BNE   GOTCR3            ; NO ==> GET NEXT CHAR
1124 FE6D  A5 82           LDA   ESCCNT            ; YES==> IS IT THE FIRST "ESCAPE" CHAR ?
1125 FE6F  F0 06           BEQ   ESCHK2            ; YES==> CHECK FOR ELAPSED TIME SINCE PREV CHAR
```

```
1126 FE71  24 81          BIT   WAITC           ; HAS GUARD TIME ELAPSED ?
1127 FE73  30 B8          BMI   GOTCR2          ; YES==> WAITED TOO LONG; ESCAPE NO LONGER VALID
1128 FE75  10 03          BPL   ESCHK3          ; NO ==> ADD 1 TO ESCAPE COUNT ( BRANCH ALWAYS )
1129 FE77  7F 81 B7 ESCHK2 BBR  7,WAITC,GOTCR3  ; BRANCH IF GUARD TIME HAS NOT ELAPSED
1130 FE7A  E6 82    ESCHK3 INC  ESCCNT          ; INCREMENT ESCAPE CODE COUNTER
1131 FE7C  A5 82          LDA   ESCCNT          ; IS THIS THE THIRD SEQUENTIAL "ESCAPE" CODE ?
1132 FE7E  C9 03          CMP   #03
1133 FE80  D0 AF          BNE   GOTCR3          ; NO ==> GET NEXT CHAR
1134 FE82  20 BB FE       JSR   STRTB1          ; YES==> RESTART GUARD-TIMER
1135 FE85  4F 01 13 LSTCHK BBR  4,PB,LSTCK2     ; NOW WAIT FOR 1 GUARD-TIME INTERVAL FOR A CHARACTER
1136                                            ; ( BRANCH IF CARRIER IS OK )
1137 FE88  20 C9 FE       JSR   STRTB2          ; CARRIER LOST --> WAIT FOR S10 TENTHS-OF-SECONDS
1138 FE8B  A5 90          LDA   S10             ;   FOR CARRIER TO RETURN -- OTHERWISE INDICATE
1139 FE8D  85 46          STA   DELAYS          ;   LOSS OF CARRIER AND RETURN TO COMMAND MODE
1140 FE8F  FF 81 AC CARCK3 BBS  7,WAITC,CARCK2  ; BRANCH IF THE TIME-OUT FLAG GOES TRUE
1141 FE92  CF 01 FA       BBS   4,PB,CARCK3     ; BRANCH IF CARRIER STILL LOST
1142 FE95  A5 16          LDA   SCSR            ; CARRIER DETECTED AGAIN BEFORE TIME-OUT-->CLEAR SERIAL FLAGS
1143 FE97  57 12          RMB   5,IER           ; DISABLE IRQ
1144 FE99  D0 92          BNE   GOTCR2          ; LOSS OF CARRIER ABORTS ESCAPE SEQUENCE --> BRANCH ALWAYS
1145
1146 FE9B  A5 16 LSTCK2 LDA   SCSR
1147 FE9D  29 0F          AND   #$0F            ; IF A CHARACTER HAS BEEN ENTERED BEFORE
1148 FE9F  D0 8C          BNE   GOTCR2          ; THE GUARD-TIME INTERVAL HAS ELAPSED, THEN THE ESCAPE
1149 FEA1  7F 81 E1       BBR   7,WAITC,LSTCHK  ; SEQUENCE IS ABORTED AND CHAR IS HANDLED IN THE
1150                                            ;  USUAL FASHION ( AT "CHKCHR" ).  IF TIMER HAS
1151                                            ;  ELAPSED THEN ESCAPE SEQUENCE IS COMPLETED WITH A
1152                                            ;  RETURN TO COMMAND MODE.
1153
1154 FEA4  57 12 ESCAPE RMB   5,IER             ; STOP TIMER B IRQ
1155 FEA6  6F 16 FD ESC2  BBR   6,SCSR,ESC2     ; WAIT UNTIL ALL CHARS ARE TRANSMITTED OUT
1156 FEA9  87 01          SMB   0,PB            ; THEN DIRECT OUTPUT TO HOST COMPUTER
1157
1158
1159 FEAB  A9 00          LDA   #00             ; RESET RESULT CODE TO "OK"
1160 FEAD  85 7D          STA   STCODE
1161 FEAF  68       NOWAIT PLA                  ; GET RID OF RETURN ADDRESS FROM "JSR DOCMD"
1162 FEB0  68              PLA                  ;  ( OR "JSR AAA" AT LABLE "ANSWER" )
1163 FEB1  20 E8 FE        JSR   RESPNS         ; SEND OUT RESPONSE, IF ENABLED
1164 FEB4  A9 00           LDA   #00            ; RESET RING COUNTER TO ZERO
1165 FEB6  85 87           STA   S1
1166 FEB8  4C 16 F8        JMP   RESTRT         ; AND START ALL OVER AGAIN
1167
```

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```
1168                ; ********************************************************************************
1169
1170                ;    1/50 SEC (20MS) DELAY
1171
1172 FEBB  A5 92 STRTB1 LDA   S12               ; SET DELAY COUNTER FOR NUMBER OF 20MS GUARD-TIME INTERVALS
1173 FEBD  85 46        STA   DELAYS
1174 FEBF  57 12        RMB   5,IER             ; DISABLE IRQ
1175 FEC1  A9 01        LDA   #ESCDLY           ; SET UP DELAY PARAMETERS
1176 FEC3  A2 9C        LDX   #<ESCTIM
```

```
1177 FEC5  A0 47          LDY   #>ESCTIM
1178 FEC7  D0 12          BNE   STRTIM          ;  ... AND START TIMER ...
1179
1180               ;   1/10 SEC DELAY
1181
1182 FEC9  57 12     STRTB2 RMB   5,IER         ; DISABLE IRQ
1183 FECB  A9 10          LDA   #DLYHIB         ; SET UP DELAY PARAMETERS FOR 1/10 SEC
1184 FECD  A2 60          LDX   #<TENTHD
1185 FECF  A0 67          LDY   #>TENTHD
1186 FED1  D0 08          BNE   STRTIM          ;  ... AND START TIMER ...  ( BRA )
1187
1188               ;   1 SECOND DELAY
1189
1190 FED3  57 12     STRTB3 RMB   5,IER         ; DISABLE IRQ
1191 FED5  A9 10          LDA   #DLYHIB         ; SET UP DELAY PARAMETERS FOR 1 SEC. DELAY
1192 FED7  A2 9C          LDX   #<DLYTIM
1193 FED9  A0 E0          LDY   #>DLYTIM
1194 FEDB  86 1C     STRTIM STX   CNTBCL         ; LOAD COUNTER-B
1195 FEDD  84 1E          STY   CNTBHL
1196 FEDF  85 44          STA   DELAYC          ; SET IRQ COUNTER
1197 FEE1  85 45          STA   DELAYT
1198 FEE3  77 81          RMB   7,WAITC         ; SET TIME-OUT FLAG FALSE
1199 FEE5  D7 12          SMB   5,IER           ; ENABLE CNTR-B IRQ
1200 FEE7  60             RTS
```

4

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```
1202 FEE8  20 40 FF  RESPNS JSR   CRLF
1203 FEEB  FF 7B 1E       BBS   7,RSLTF6,QRSP   ; BRANCH IF STATUS RESPONSE IS DISABLED
1204 FEEE  A5 7D          LDA   STCODE          ; GET CODE VALUE
1205 FEF0  C9 01          CMP   #$01            ; IF "CARRIER" RESPONSE, CHECK FOR EXTENDED CODE
1206 FEF2  D0 0D          BNE   RSP2            ; NOT "CARRIER" --> BRANCH ...
1207 FEF4  7F 7F 0A       BBR   7,XCODE,RSP2    ; BRANCH IF EXTENDED CODE SET IS NOT TO BE USED
1208 FEF7  A4 41          LDY   BAUD            ; IS SYSTEM RUNNING AT 1200 BAUD ?
1209 FEF9  C0 03          CPY   #$03            ;
1210 FEFB  F0 04          BEQ   RSP2            ; NO ==> BRANCH ...
1211 FEFD  A9 05          LDA   #$05            ; YES==> INDICATE 1200/2400 BAUD CARRIER
1212 FEFF  85 7D          STA   STCODE          ;  AND SAVE IT
1213 FF01  FF 7E 09  RSP2 BBS   7,VCODE,VERBAL  ; BRANCH IF RESPONSE IS TO BE VERBAL
1214 FF04  09 30     NUMERC ORA   #$30          ; CONVERT RESPONSE CODE TO ASCII
1215 FF06  20 51 FF       JSR   CHROUT          ;  AND SEND IT OUT
1216 FF09  20 40 FF       JSR   CRLF            ;  FOLLOWED BY <CR/LF>
1217 FF0C  60        QRSP RTS                   ; RETURN
1218
1219 FF0D  A4 7D     VERBAL LDY   STCODE        ; DETERMINE WHICH MESSAGE TO SEND OUT
1220 FF0F  F0 20          BEQ   RSPOK           ; 0 ==> "OK"
1221 FF11  88             DEY
1222 FF12  F0 19          BEQ   RSPCAR          ; 1 ==> "CARRIER"
1223 FF14  88             DEY
1224 FF15  F0 12          BEQ   RSPRNG          ; 2 ==> "RING"
1225 FF17  88             DEY
1226 FF18  F0 0B          BEQ   RSPNC           ; 3 ==> "NO CARRIER"
1227 FF1A  88             DEY
1228 FF1B  F0 04          BEQ   RSPERR          ; 4 ==> "ERROR"
```

```
1229
1230 FF1D  A0 1C     RSPC12 LDY   #CON12M-MSG      ; 5 ==> "CONNECT 1200/2400"
1231 FF1F  D0 12            BNE   MSGOUT
1232 FF21  A0 17     RSPERR LDY   #ERRMSG-MSG
1233 FF23  D0 0E            BNE   MSGOUT
1234 FF25  A0 0D     RSPNC  LDY   #NOCARM-MSG
1235 FF27  D0 0A            BNE   MSGOUT
1236 FF29  A0 09     RSPRNG LDY   #RNGMSG-MSG
1237 FF2B  D0 06            BNE   MSGOUT
1238 FF2D  A0 02     RSPCAR LDY   #CARMSG-MSG
1239 FF2F  D0 02            BNE   MSGOUT
1240 FF31  A0 00     RSPOK  LDY   #OKMSG-MSG
1241
1242 FF33  B9 7A FF  MSGOUT LDA   MSG,Y           ; GET CHAR FROM MESSAGE TABLE
1243 FF36  48               PHA                   ; SAVE CHARACTER
1244 FF37  C8               INY                   ; POINT TO NEXT CHAR
1245 FF38  29 7F            AND   #$7F            ; MASK OFF MSB
1246 FF3A  20 51 FF         JSR   CHROUT          ; AND SEND OUT CHAR
1247 FF3D  68               PLA                   ; RESTORE SIGN BIT
1248 FF3E  10 F3            BPL   MSGOUT          ; BRANCH IF MORE CHARS TO BE SENT
1249 FF40  A5 89     CRLF   LDA   S3              ; ( S3 CONTAINS CURRENT <CR> )
1250 FF42  20 51 FF         JSR   CHROUT          ; SEND OUT <CR>
1251 FF45  7F 7E 05         BBR   7,VCODE,WAITLF  ; BYPASS <LF> IF NUMERIC RESPONSE SELECTED
1252 FF48  A5 8A            LDA   S4              ; ( S4 CONTAINS CURRENT <LF> )
1253 FF4A  20 51 FF         JSR   CHROUT          ; OUTPUT <LF>
1254 FF4D  7F 16 FD  WAITLF BBR   7,SCSR,WAITLF   ; WAIT UNTIL <LF> IS FINISHED
1255 FF50  60               RTS                   ;  THEN RETURN
1256
1257 FF51  6F 16 FD  CHROUT BBR   6,SCSR,CHROUT   ; WAIT TILL TRANSMITTER BUFFER IS EMPTY
1258 FF54  85 17            STA   STDR            ;  THEN SEND OUT CHAR
1259 FF56  60               RTS
```



```
1261
1262                ; INTERRUPT SERVICE ROUTINE
1263
1264 FF57  48       ISR    PHA
1265 FF58  A5 1C            LDA   CNTBCL          ; CLEAR TIMER B FLAG
1266 FF5A  FF 7B 0D         BBS   7,IRQFLG,CARIER ; BRANCH IF IRQ IS FOR WAIT-FOR-CARRIER DELAY
1267 FF5D  A5 00            LDA   PA              ;  ECHO SERIAL IN TO SERIAL OUT
1268 FF5F  0A               ASL   A
1269 FF60  90 04            BCC   SET0
1270 FF62  E7 00     SET1   SMB   6,PA
1271 FF64  B0 12            BCS   QISR            ;  (BRANCH ALWAYS)
1272 FF66  67 00     SET0   RMB   6,PA
1273 FF68  90 0E            BCC   QISR            ;  (BRANCH ALWAYS)
1274
1275 FF6A  C6 44     CARIER DEC   DELAYC          ; IS TIMER COUNTER = 0 ?
1276 FF6C  D0 0A            BNE   QISR            ; NO ==> RETURN
1277 FF6E  A5 45            LDA   DELAYT          ; YES==> RESET IT
```

```
1278 FF70   85 44            STA   DELAYC
1279 FF72   C6 46            DEC   DELAYS              ; IS SECONDS COUNTER = 0 ?
1280 FF74   D0 02            BNE   QISR                ; NO ==> RETURN
1281 FF76   F7 81            SMB   7,WAITC             ; YES==> SET TIME-OUT FLAG
1282 FF78   68          QISR  PLA
1283 FF79   40          NMIRTN RTI

1285 FF7A               MSG   =     *
1286
1287 FF7A   4F          OKMSG .SBY  'OK'
1288 FF7C   43          CARMSG .SBY 'CONNECT'
1289 FF83   52          RNGMSG .SBY 'RING'
1290 FF87   4E          NOCARM .SBY 'NO CARRIER'
1291 FF91   45          ERRMSG .SBY 'ERROR'
1292 FF96   43          CON12M .SBY 'CONNECT 1200/2400'
1293
1294 FFA7   2A          CHKSUM .SBY '****'
1295 FFAB   36          PCODE  .SBY '6500'
1296
1297 FFAF                     *=$FFFA
1298
1299 FFFA   79 FF             .WOR  NMIRTN
1300 FFFC   00 F8             .WOR  RESET
1301 FFFE   57 FF             .WOR  ISR
1302
1303                          .END  MDM10A

ERRORS = 0000 <0000>
```


SYMBOL TABLE

```
AAA     FC0D    0489  0509 #0726
ABIT8   0048   #0044  0179  0263  0313  0316  0330
ABIT9   0049   #0045  0180  0268  0309
ALLIN   F9DD    0414 #0422
ANSWER  FA42    0485 #0488
BAUD    0041   #0037  0378  0900  1208
BAUD12  002F   #0126  0357  0553  0555
BAUD24  0017   #0127
BAUD3   00BF   #0125  0351
BDRATH  0043   #0039  0215  0341  0347  0477  0556
BDRATL  0042   #0038  0223  0342  0345  0350  0475  0554
BD2     F974    0356  0362 #0366
BS      F9BF    0401 #0404
BUFFLG  0075   #0050  0186  0418  0422
B03     F95A   #0353
B12     F966   #0359
B24     F96E    0358 #0363
CARCK2  FE3E   #1099  1100  1140
CARCK3  FE8F   #1140  1141
CARIER  FF6A    1266 #1275
CARMSG  FF7C    1238 #1288
```

```
CARTIM FDF6    0870  1057 #1068
CCC    FC28    0509 #0743
CCONE  FC2F   #0746
CCZERO FC38    0744  0745 #0750
CHKCHR FE4E   #1106
CHKOK  FE57    1107 #1112
CHKSUM FFA7    0839 #1294
CHROUT FF51    0394  0403  0409  0716  1113  1116  1215  1246  1250  1253
              #1257  1257
CMDTBL FA47    0448 #0497
CMDVEC 009B   #0089  0436  0461  0463
CNTACL 0018   #0025  0205  0217  0224  0235  0260  0265  0279  0296  0301
               0346  0476
CNTAH  0019   #0026  0213
CNTAL  001A   #0027  0206  0227  0229  0247  0274  0276  0348  0478
CNTBCL 001C   #0030  0198  0583  0588  1075  1194  1265
CNTBHC 001D   #0031
CNTBHL 001E   #0032  0200  0585  1195
COMMA  FB1E    0505 #0579  0774
CON12M FF96    1230 #1292
CR     FDE0    0425  0512  0620  0639  0921 #1051
CRLF   FF40    0710  0719  0835  0983  1202  1216 #1249
CR2    FDEE    0735 #1057
CTLCOD F9AC    0393 #0395
DDD    FC44    0509 #0760
DEFPRO 0040   #0036  0339  0473  0558
DELAYC 0044   #0040  1196  1275  1278
DELAYS 0046   #0042  1070  1098  1139  1173  1279
DELAYT 0045   #0041  1197  1277
DELETE F9C3   #0406
DIGERR FB54    0601 #0618  0645
DIGIT  FB3C    0506  0507 #0601
DIG2   FB4E    0612 #0614
DILFLG 0076   #0051  0184  0546  0601  0627  0628  0777  0899  0904
DLYHIB 0010   #0119  0586  1183  1191
DLYTIM E09C   #0120  0582  0584  1192  1193
DOCMD  F9F2    0434 #0436
DUPLEX 007A   #0055  0550  0801  0803  1114
ECHOFG 0079   #0054  0196  0393  0549  0789  0791
```

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SYMBOL TABLE

```
EEE    FC72    0509 #0786
EONE   FC79   #0789
EQUAL  FB76    0508 #0645
EQ2    FBA2    0654  0659 #0665
EQ3    FBAD    0666 #0670
EQ4    FBBC    0651  0671 #0677
ERRMSG FF91    1232 #1291
ESCAPE FEA4   #1154
ESCCHK FE69    1114 #1122
ESCCNT 0082   #0063  1093  1124  1130  1131
ESCDLY 0001   #0122  1175
```

```
ESCHK2 FE77    1125 #1129
ESCHK3 FE7A    1128 #1130
ESCTIM 479C   #0123  1176  1177
ESC2   FEA6   #1155  1155
EVEN7  F929    0317 #0327
EVEN8  F91D    0310 #0321
EZERO  FC7D    0787  0788 #0791
FFF    FC80    0509 #0798
FNDCMD F9F5    0432 #0444
FONE   FC87   #0801
FOUND  FA0D    0449 #0457
FOUNDA F8AD    0244 #0259  0259
FOUNDS F8EF    0288 #0293
FOUNDT F8F1    0290 #0295  0295
FZERO  FC8B    0799  0800 #0803
GETCHR F9A4   #0392
GETNUM FD8E    0650  0653  0658  0743  0786  0798  0810  0836  0851  0886
               0929  0933  0958  0970 #0992
GOCR   FA0B    0447 #0455
GOTCAR FE18    1071 #1083
GOTCHR F9CD    0396  0405 #0412
GOTCR1 FE28    1088 #1090
GOTCR2 FE2D   #1092  1127  1144  1148
GOTCR3 FE31   #1094  1123  1129  1133
GOTHUN FDAA    1008 #1012
GOTTEN FDBA    1016 #1020
GO2RES F8A7   #0250
GT300  F962    0352 #0357
HCONV  FDC4    1012  1020 #1026
HHH    FC8E    0509 #0810
HHSET  FCB7    0820 #0827
HHZERO FCA7    0811  0812 #0821  1080
HOP    FE15    1052  1053 #1081
HX2    FDA1   #1007  1011
HX2ASC FD9F    0713 #1006
HX3    FDB1   #1015  1019
H1AND2 FC95    0726 #0813  0868
IER    0012   #0019  0201  0349  0469  0528  1074  1083  1102  1143  1154
               1174  1182  1190  1199
IFR    0011   #0018  0192  0207  0228  0234  0248  0259  0264  0275  0278
               0295  0300  0470  0527  0587
III    FCBB    0510 #0835
IIONE  FCC5   #0839
IIZERO FCC9    0837  0838 #0841
INBUFF 004C   #0048  0412  0445  0569  0605  0992
INCHAR FE34   #1095  1105
INCHR2 FE48    1095 #1103
INITSW FABE    0140 #0526
IRQFLG 0078   #0053  0202  0380  0488  1266
```

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SYMBOL TABLE

```
ISR     FF57    #1264  1301
LABEL1  F93D     0320  0323  0326  0329  0334 #0338
LOOP2   F9FD    #0448  0452
LSTCHK  FE85    #1135  1149
LSTCK2  FE9B     1135 #1146
L1      F857    #0207  0208
L10     F8D4    #0278  0278  0284
L12     F8FB    #0300  0300
L2      F85F    #0210  0210
L3      F87D    #0228  0228
L4      F889    #0234  0234  0240
L4A     F8A1    #0248  0248
L5      F8A4    #0249  0249
L6      F8B7    #0264  0264
L7      F8C1    #0269  0269
L8      F8C4    #0270  0270
L9      F8CD    #0275  0275
MCR     0014    #0020  0138  0194  0195  0221  0222  0472
MMM     FCCF     0510 #0850
MMONE   FCDC    #0856
MMTWO   FCDE     0855 #0857
MMZERO  FCE3     0852  0853 #0859
MSG     FF7A     0839  0841  1230  1232  1234  1236  1238  1240  1242 #1285
MSGOUT  FF33     0842  1231  1233  1235  1237  1239 #1242  1248
MULT10  FBEC     0667  0672  0673 #0699
NEWCR   FDD7     0191  1034 #1041
NEWCX   FDCE     0733  0753  0767  0879  0951 #1036
NEWCXR  FDCB     0377  0696  0827  0916 #1034
NMIRTN  FF79    #1283  1299
NOCARM  FF87     1234 #1290
NOCARR  FE06     1072 #1074  1099
NODLAY  FB39     0581 #0593
NOIRQ   F850     0196 #0203
NOPAR   F92F     0315 #0330
NOPAR7  F939     0331 #0335
NOPARB  F933    #0332
NOSLFT  FBC6    #0682
NOTNUM  FD9D     0994 #1000
NOWAIT  FEAF     1081  1110 #1161
NUM     0098    #0088  0647  0648  0649  0652  0655  0656  0657  0660  0661
                 0662  0663  0664  0665  0668  0669  0670  0675  0676  0677
                 0715  0932  0936  0937  1013  1021  1023
NUMCMD  0021    #0129  0451  0455
NUMERC  FF04    #1214
NXTCMD  F9E9    #0432  0435
ODD7    F917    #0318
ODD8    F923     0312 #0324
OKMSG   FF7A     1240 #1287
ONESEC  FB2C    #0586  0592
OOO     FCE6     0510 #0868
PA      0000    #0013  0208  0209  0210  0230  0236  0249  0261  0266  0269
                 0270  0280  0297  0302  1267  1270  1272
PB      0001    #0014  0142  0143  0144  0145  0146  0354  0360  0364  0857
                 0859  1071  1077  1089  1091  1095  1100  1115  1118  1135
```

```
                1141  1156
PCODE   FFAB     0841 #1295
PPP     FCEE     0510 #0876
QCCC    FC3D     0748  0749 #0752
QDIGIT  FB53    #0616
QECHO   FC7F     0790 #0792



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SYMBOL TABLE

QEQ     FBE8     0688 #0696
QFFF    FC8D     0802 #0804
QGETN   FD9E     0996  0999 #1001
QHHH    FCBA    #0828
QII     FCCB     0840 #0842
QISR    FF78     1271  1273  1276  1280 #1282
QMMM    FCE5     0858 #0860
QQ      FD07     0890 #0892
QQDNE   FD01    #0889
QQQ     FCFA     0510 #0886
QQZERO  FD05     0887  0888 #0891
QRRR    FD32     0902 #0917
QRSP    FF0C     1203 #1217
QSSS    FD57     0930  0931 #0941
QUESTN  FBF4     0508 #0710
QUES3   FC00    #0715  0718
QVVV    FD73     0962 #0964
QXXX    FD81     0974 #0976
RCV     1000    #0092  0094
RCVA    100A    #0098  0367  0370  0534  0683  0684  0691  0692
RCVB    100B    #0099
RCVC    100C    #0100  0375  0537
RCVD    100D    #0101  0188  0190  0532  0817  0819  0824  0826  0910  0911
RCVE    100E    #0102  0539  1042  1043
RCVF    100F    #0103
RCV2    1002    #0095
RCV8    1008    #0096
RCV9    1009    #0097
REPEAT  F9E7     0386  0422 #0427
REPFLG  0074    #0049  0178  0293  0386
RERROR  FD33     0899 #0919
RESET   F800    #0133  0985  1300
RESPNS  FEE8     0481  0982  1090  1163 #1202
RESTRT  F816    #0176  0250  0291  0486  1166
REVFLG  0077    #0052  0779  0905  1057
RING    F8AA     0207 #0252
RINGNG  FA1C     0252 #0469
RNGMSG  FF83     1236 #1289
ROTATE  F943    #0341  0344
RRR     FD08     0510 #0899
RSLTFG  007B    #0056  0547  0889  0891  1203
RSPCAR  FF2D     1222 #1238
RSPC12  FF1D    #1230
RSPERR  FF21     1228 #1232
```

```
RSPNC  FF25    1226 #1234
RSPOK  FF31    1220 #1240
RSPRNG FF29    1224 #1236
RSP2   FF01    1206  1207  1210 #1213
SCCR   0015   #0021  0177  0338  0474
SCSR   0016   #0022  0381  0388  0984  1072  1101  1103  1117  1142  1146
               1155  1254  1257
SEMERR FB6F    0627 #0637
SEMIC  FB5B    0508 #0627
SEMI2  FB62   #0630  0631
SETPTR F99C   #0387  0410
SET0   FF66    1269 #1272
SET1   FF62   #1270
SLFTST FBD8    0681 #0690
SLOOP  FB11   #0564  0567
SPKRFG 007C   #0057  0552  0850  0856  1088
```



```
SYMBOL TABLE

SRDR   0017   #0024  0392  1112
SREGP  0084   #0065  0560  0562  0565  0679  0712  0928  0939  0940
SSETFG 0083   #0064  0543  0645  0941
SSS    FD3A    0511 #0927
SS2    FD50    0934 #0937
STBL   FAAD   #0517  0564
STCODE 007D   #0058  0187  0424  0454  0480  0619  0638  0920  1051  1079
               1087  1109  1160  1204  1212  1219
STDR   0017   #0023  0024  1258
STRTB1 FEBB    1094  1134 #1172
STRTB2 FEC9    1096  1137 #1182
STRTB3 FED3    1068 #1190
STRTIM FEDB    1178  1186 #1194
S0     0086   #0069  0484  0559  0561  0927
S1     0087   #0070  0482  0483  0544  1165
S10    0090   #0079  1097  1138
S11    0091   #0080
S12    0092   #0081  1172
S13    0093   #0082
S14    0094   #0083
S15    0095   #0084
S16    0096   #0085  0680
S17    0097   #0086
S2     0088   #0071  1122
S3     0089   #0072  0395  0413  0446  0568  1249
S4     008A   #0073  1252
S5     008B   #0074  0402  0404
S6     008C   #0075  0772
S7     008D   #0076  1069
S8     008E   #0077  0580  0770  0773  0776
S9     008F   #0078
TBIT8  004A   #0046  0181  0299  0314
TBIT9  004B   #0047  0182  0304  0311
TEMP   009D   #0090  0366  0369  0373  0579  0593  0699  0702
```

```
TENTHD 6760    #0121  1184  1185
TESTB  0047    #0043  0183  0232  0238  0241  0271  0282  0285
TTT    FD5A     0511 #0948
VCODE  007E    #0059  0551  0961  0963  1213  1251
VECTBL FA69     0460  0462 #0505
VERBAL FF0D     1213 #1219
VONE   FD6D    #0961
VVV    FD66     0511 #0958
VZERO  FD71     0959  0960 #0963
WAITB  FB2E    #0587  0587  0590
WAITC  0081    #0062  1073  1099  1126  1129  1140  1149  1198  1281
WAITDB FDE9    #1055  1056
WAITDL FC59    #0768  0769
WAITDP FE64    #1117  1117
WAITFG 0080    #0061  0185  0634  0734  0778  0869  1053  1076
WAITIN F99E    #0388  0390  0398  0399  0407  0417  0420
WAITLF FF4D     1251 #1254  1254
WAITRE FB41    #0603  0604
WCARIR FDFD    #1071  1073
XCODE  007F    #0060  0545  0973  0975  1207
XMT    2000    #0105  0107
XMTA   200A    #0112  0371  0374  0535  0686  0687  0694  0695
XMTB   200B    #0113  0530  0876  0878  0948  0950
XMTC   200C    #0114  0376  0538
XMTD   200D    #0115  0529  0728  0729  0763  0766  0813  0816  0821  0823
                0913  0915
```

4

SYMBOL TABLE

```
XMTE   200E    #0116  0540  0603  0630  1037  1038  1055
XMTF   200F    #0117
XMT0   2000    #0108  0615  0633  1060  1085
XMT2   2002    #0109
XMT8   2008    #0110  0768
XMT9   2009    #0111  0731  0732  0747  0751  0752  0761  0762  0907  0908
XONE   FD7B    #0973
XXX    FD74     0511 #0970
XZERO  FD7F     0971  0972 #0975
ZZWAIT FD88    #0984  0984
ZZZ    FD82     0511 #0982
.NARG  ****
```

END OF ASSEMBLY

Rockwell

Interfacing Rockwell Signal Processor-Based Modems To An Apple IIe Computer

by Carlos A. Laiz, Product Applications Engineer
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INTRODUCTION

This application note describes the electrical design of a module that interfaces an Apple IIe* computer to a Rockwell Signal Processor (SP)-based modem. The design incorporates an USART (8251A) for asynchronous/synchronous serial data transfer and control, and two digital-to-analog converters (DACs) for quadrature eye pattern generation. Memory mapped input/output (I/O) allows easy access to the modem interface memory for parallel control and data transfer. The interface module connects directly to the following modems with minor software differences required to switch between them:

- R1212M or R1212DC
- R2424M or R2424DC
- R48DP
- R96DP
- R96FT

Two assembly listings of sample software subroutines for R1212/R2424 automatic dialing and R48DP/R96DP eye pattern generation are also included.

HARDWARE DESIGN

The interface module schematic (Figure 1) shows the routing of signals between an Apple IIe peripheral slot, the USART, and the modem. The modem can physically be located outside the Apple IIe and connected by a short 64-conductor ribbon cable to a 64-pin DIN connector (with the same pin assignments) installed on the interface module.

The major devices on the interface module are the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) and two NE5018 DACs. The USART (U1) allows the microprocessor to transfer data and control to the modem via the serial interface. This USART supports both asynchronous and synchronous data transfer modes. The two DACs, U8 and U9, generate the analog voltages to drive the eye pattern X-OUT and Y-OUT signals, respectively.

Address lines A0–A3 are directly connected to the modem register select inputs RS0-RS3. The Apple's partially decoded $\overline{\text{I/O SELECT}}$ (pin 1 in the Apple peripheral connector) is used to gate R/$\overline{\text{W}}$ to produce two separate READ and $\overline{\text{WRITE}}$ signals with the proper timing as required by the modem and the USART. $\overline{\text{I/O SELECT}}$ is active during ϕ0 clock when the microprocessor references page $Cn, where n is a peripheral slot number (1–7) in the Apple.

The data lines are buffered by U2 and routed to multiple destinations (U1, U8, U9 and the interfacing modem). U2 is enabled by $\overline{\text{I/O SELECT}}$ and the data direction is controlled by READ.

Address lines A4–A6 are decoded (U3) into eight chip select signals ($\overline{\$Cn0R}$–$\overline{\$Cn3R}$ and $\overline{\$Cn4X}$–$\overline{\$Cn7X}$). Addresses $Cn0R–$Cn3R correspond to the modem chip select inputs ($\overline{CS0}$–$\overline{CS3}$). Writing to address $\overline{\$Cn4X}$ triggers U4 to generate a low level pulse (4 μs min.) causing the modem to initiate a Power On Reset (POR) cycle. Addresses $\overline{\$Cn5X}$ and $\overline{\$Cn6X}$ are used to write eye pattern data into the X-DAC and Y-DAC, respectively.

The USART's input line Control/$\overline{\text{Data}}$ (C/$\overline{\text{D}}$) is controlled by the address line A7. Address $\overline{\$Cn7X}$ (A7 = 0) is used to write to the transmitter register or to read the receiver register in the USART. Address $\overline{\$CnFX}$ (A7 = 1) is used to write to the USART Control register or to read its status register. The USART is supplied with ϕ1 clock directly from the Apple bus.

The I/O addresses and their functions are summarized in Table 1.

Table 1. Interface Module Memory Map

Address	Device Addressed/Function Performed
$\overline{\$Cn0R}$	Chip Select 0 (CS0)
$\overline{\$Cn1R}$	Chip Select 1 (CS1)
$\overline{\$Cn2R}$	Chip Select 2 (CS2)
$\overline{\$Cn3R}$	Chip Select 3 (CS3)
$\overline{\$Cn4X}$	POR (Power-On-Reset)
$\overline{\$Cn5X}$	X-DAC Latch Enable (XLE)
$\overline{\$Cn6X}$	Y-DAC Latch Enable (YLE)
$\overline{\$Cn7X}$	USART Chip Select (C/$\overline{\text{D}}$ = A7 = ϕ)
$\overline{\$CnFX}$	USART Chip Select (C/$\overline{\text{D}}$ = A7 = 1)

Notes:
n = Apple IIe peripheral slot number (1–7)
R = Modem register number (0–F)
X = Irrelevant

*Apple and Apple IIe are registered trademarks of Apple Computer, Inc.

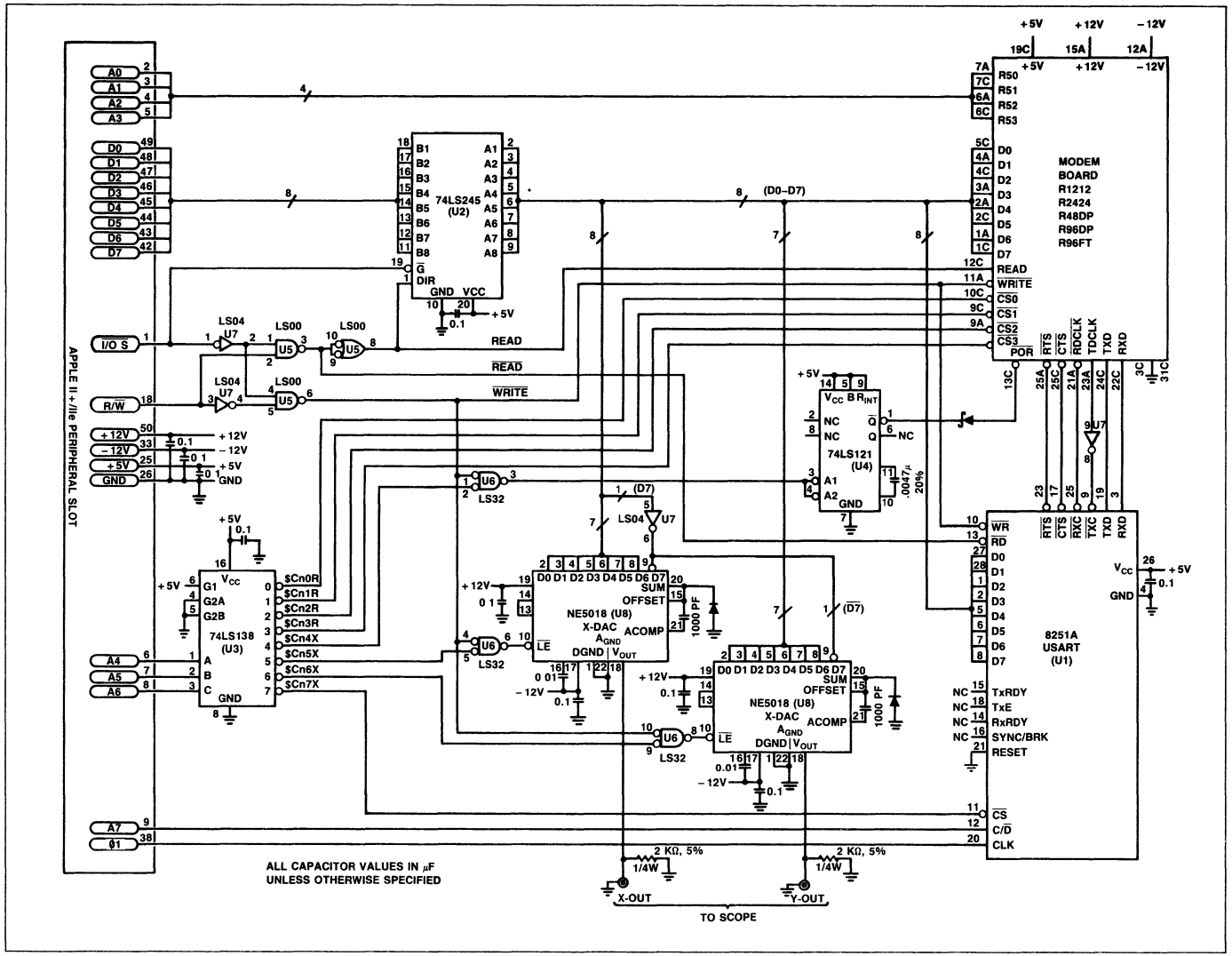

Figure 1. Apple IIe to Rockwell SP Modem Interface Schematic

SOFTWARE CONSIDERATIONS

Application software can easily control the modem, the USART and the two DACs via the addresses decoded on the interface module (Table 1). The location of bits and registers as well as diagnostic access codes vary between modems. Refer to the appropriate data sheet for specific bit and register locations and access codes.

Two example software subroutines are included in this application note for interfacing to an SP-based modem. These routines are written in 6502 assembly language.

The Automatic Dialer subroutine for the R1212/R2424 (Figure 2) implements the same function described and flowcharted in the R1212 and R2424 data sheets. The subroutine, as shown, starts at address $6000 but can be easily relocated. As written, it assumes that the interface module is installed in Apple IIe peripheral slot 4. The number to be dialed should be stored at $6100 and terminated with an $FF character.

The Eye Pattern Generator subroutine for the R48DP/R96DP (Figure 3) generates a continuous eye pattern in loop 3 (local analog loopback) by reading a signal point once per baud. The subroutine starts at $0300 and can also be easily relocated. Execution is halted and control returned to the calling routine when a key is pressed. The comments in the listing describe the detail operation.

```
                        1000        ORG $6000
                        1008 *
                        1016 ********************************************
                        1024 *     R1212/R2424 AUTOMATIC DIALER ROUTINE     *
                        1032 ********************************************
                        1040 *
                        1048 ********************************************
                        1056 * THE NUMBER TO BE DIALED SHOULD BE STORED AT  *
                        1064 * $6100.  THIS PROGRAM ASSUMES THAT THE       *
                        1072 * INTERFACE BOARD IS IN SLOT 4.  IT MAY BE     *
                        1080 * EXECUTED AS A SUBROUTINE FROM BASIC WITH A  *
                        1088 * "CALL 24576" OR A "JSR $6000" FROM ASSEMBLY. *
                        1096 ********************************************
                        1104 *
6000- AD 1B C4          1112        LDA $C41B
6003- 29 FD             1120        AND #$FD        ;SET PULSE DIALING
6005- 8D 1B C4          1128        STA $C41B
6008- AD 1D C4          1136        LDA $C41D
600B- 09 C8             1144        ORA #$C8        ;SET DRO=1, RUS=1, DTR=1
600D- 8D 1D C4          1152        STA $C41D
6010- AD 1E C4          1160        LDA $C41E
6013- 09 08             1168        ORA #$08        ;SET NEWC (TRANSMITTER)
6015- 8D 1E C4          1176        STA $C41E
6018- AD 18 C4          1184 DLO    LDA $C418
601B- 29 80             1192        AND #$80
601D- F0 F9             1200        BEQ DLO         ;DLO= 1?
601F- A2 00             1208        LDX #$00        ;INITIALIZE DIGIT COUNTER
6021- AD 1E C4          1216 DORE   LDA $C41E
6024- 29 01             1224        AND #$01        ;DDRE=1 ?
6026- F0 F9             1232        BEQ DORE
6028- BD 00 61          1240        LDA $6100,X     ;GET DIGIT FROM BUFFER AT $6100
602B- 8D 1C C4          1248        STA $C41C       ;STORE DIGIT IN DDR
602E- E8                1256        INX
602F- E0 FF             1264        CMP #$FF        ;LAST DIGIT ?
6031- D0 EE             1272        BNE DORE        ;IF NO, DIAL NEXT DIGIT
6033- 60                1280        RTS             ;ELSE, RETURN FROM SUBROUTINE

SYMBOL  TABLE

DLO     6018    DORE    6021
```

Figure 2. R2424 Automatic Dialer Routine

```
                        1000        ORG $300
                        1008 *
                        1016 ************************************************
                        1024 *    R48DP/R96DP EYE PATTERN GENERATION ROUTINE    *
                        1032 ************************************************
                        1040 *                                              *
                        1048 * THIS ROUTINE GENERATES A CONTINUOUS EYE PATTERN *
                        1056 * READING A SIGNAL POINT ONCE PER BAUD.         *
                        1064 * EXECUTION IS HALTED AND CONTROL IS RETURNED TO  *
                        1072 * THE CALLING PROGRAM WHEN A KEY IS PRESSED.     *
                        1080 *                                              *
                        1088 ************************************************
                        1096 *
0300- AD 10 C0          1104        LDA $C010       ;CLEAR KBRD.
0303- 8D 40 C4          1112        STA $C440       ;POR
0306- A9 A2             1120        LDA #$A2
0308- 8D 25 C4          1128        STA $C425       ;WRITE RAM ACCESS XB
030B- A9 22             1136        LDA #$22
030D- 8D 24 C4          1144        STA $C424       ;WRITE RAM ACCESS YB
0310- AD 04 C4          1152        LDA $C404
0313- 09 80             1160        ORA #$80
0315- 8D 04 C4          1168        STA $C404       ;SET LOOPBACK ANALOG LOOPBACK
0318- AD 07 C4          1176        LDA $C407
031B- 09 80             1184        ORA #$80
031D- 8D 07 C4          1192        STA $C407       ;RTS ON
0320- AD 2E C4          1200 RBDA   LDA $C42E       ;READ RBDA
0323- 29 01             1208        AND #$01
0325- F0 F9             1216        BEQ RBDA        ;WAIT UNTIL RBDA=1
0327- AD 23 C4          1224        LDA $C423       ;READ RAM DATA XBM
032A- 8D 50 C4          1232        STA $C450       ;WRITE TO X-DAC
032D- AD 21 C4          1240        LDA $C421       ;READ RAM DATA YBM
0330- 8D 60 C4          1248        STA $C460       ;WRITE TO Y-DAC
0333- AD 20 C4          1256        LDA $C420       ;READ REG. 2:0 TO CLEAR RBDA
0336- AD 00 C0          1264        LDA $C000       ;KEYBOARD ACTIVE ?
0339- 29 80             1272        AND #$80
033B- F0 E3             1280        BEQ RBDA        ;IF YES, CLEAR DACS AND RETURN
033D- A9 00             1288        LDA #$00
033F- 8D 50 C4          1296        STA $C450
0342- 8D 60 C4          1304        STA $C460
0345- 60                1312        RTS
```

Rockwell

2400/1200/300 bps International Modem Design

by Malcolm B. Waters, Product Applications Engineer
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INTRODUCTION

This application note presents a design for a 2400/1200/300 bps international modem which meets CCITT recommendations V.21, V.22, V.22 bis and V.23. The design is based on the Rockwell R2424 2400/bps full duplex modem which provides the 2400 bps V.22 bis and 1200 bps V.22 modes, and the Am7910 FSK modem which provides 1200 bps half duplex V.23 and 300 bps full duplex V.21 modes. The modes supported are listed in Table 1.

The hardware design, along with software described in this application note, demonstrates a complete functional unit for asynchronous operation. The application note software supports five operating modes:

Originate 2400 bps in V.22 bis
Originate 1200 bps in V.22
Originate 1200 bps in V.23
Originate 300 bps in V.21
Universal Auto Answer

The modem design includes the complete interface to an IBM PC (or compatible) host computer. The application hardware was built on a full-size prototyping card which can be installed into any spare PC expansion slot. The Am7910 modem and other peripheral and TTL devices are installed on one third of the prototyping card. A Rockwell R2424M, a small (4 in. x 3.5 in.) self-contained modem module, is mounted over one third of the prototyping card. A Rockwell Data Access Arrangement (RDAA) module (3.94 in. x 3.94 in.) is mounted over the middle third of the prototyping card. Figure 1 shows the basic layout of the major hardware components.

The Rockwell R2424 modem is also available as a device set (R2424DS). By using modem devices and an integral DAA in a production design, this application note design can be incorporated onto a single full-size IBM PC printed circuit board.

HARDWARE DESIGN

The major components of the international modem are:

R2424M 2400/1200 Full Duplex Modem module
Am7910 1200/300 FSK Modem
Z8530 Serial Communications Controller (SCC)
82C55 Programmable Peripheral Interface (PPI)
Rockwell Data Access Arrangement (RDAA) module

A functional block diagram showing major data and control signal flow is shown in Figure 2. In addition to supplying the 2400 bps (V.22 bis) and 1200 (V.22) full duplex modes, the R2424 modem provides the primary control interface with the telephone line. The Am7910 modem supplies 1200 bps half duplex (V.23) and 300 bps full duplex (V.21) functions. The R2424 is controlled directly from the host computer data bus, whereas the Am7910 has control pins which are driven from the 82C55 PPI. Control signals select which modem is in operation and route the data along specific paths. A schematic detailing all signal routing and connections is shown in Figure 3.

Host Interface

The IBM PC address, data and control bus signals are buffered by devices U1-U4. The modem uses I/O address space 200H-23FH. Table 2 allocates the addresses used by the various devices in the application design. Decoder U5 generates four chip select signals ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$) from address lines A0-A9. The U13a output enables U5 when a valid address (200H-23FH) occurs.

The I/O Read ($\overline{IOR}$) and I/O Write ($\overline{IOW}$) lines are gated with a valid I/O address to generate read and write inputs to the R2424 modem, the Z8530 SCC (U6) and the 82C55 PPI (U7) as the chip select lines are not selected at a unique address range. An inverter (U14c) is included in the read line to make it active high for the R2424.

Table 1. International Modem Modes

Recommendation	Rate	Full Duplex/ Half Duplex	Originate/ Answer	Modulation Scheme	Modem
V.22 bis	2400 bps	Full Duplex	Originate	PSK	R2424
V.22 bis	2400 bps	Full Duplex	Answer	PSK	R2424
V.22	1200 bps	Full Duplex	Originate	PSK	R2424
V.22	1200 bps	Full Duplex	Answer	PSK	R2424
V.23	1200 bps	Half Duplex	Mode 2	FSK	Am7910
V.23	1200 bps	Half Duplex	Mode 2 with Equalizer	FSK	Am7910
V.21	300 bps	Full Duplex	Originate	FSK	Am7910
V 21	300 bps	Full Duplex	Answer	FSK	Am7910

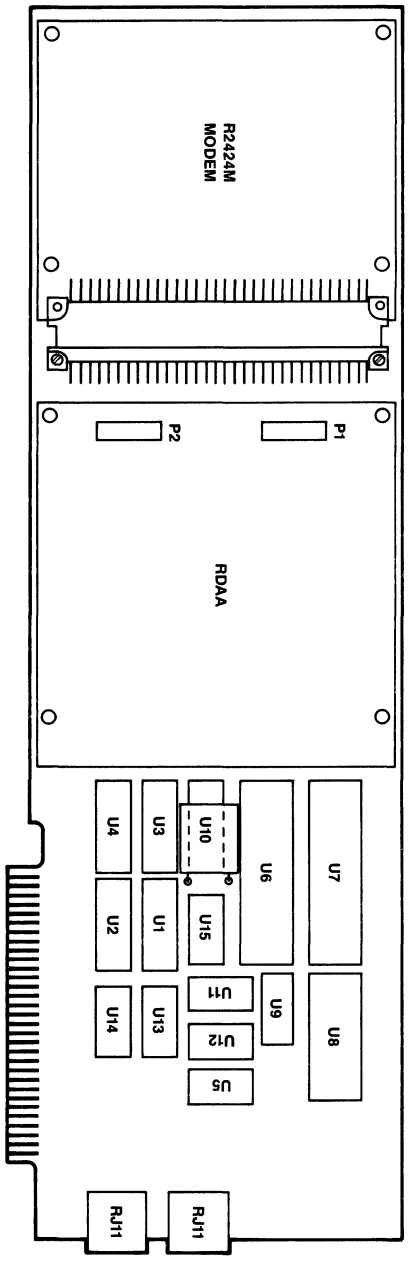

Figure 1. International Modem Prototype Layout

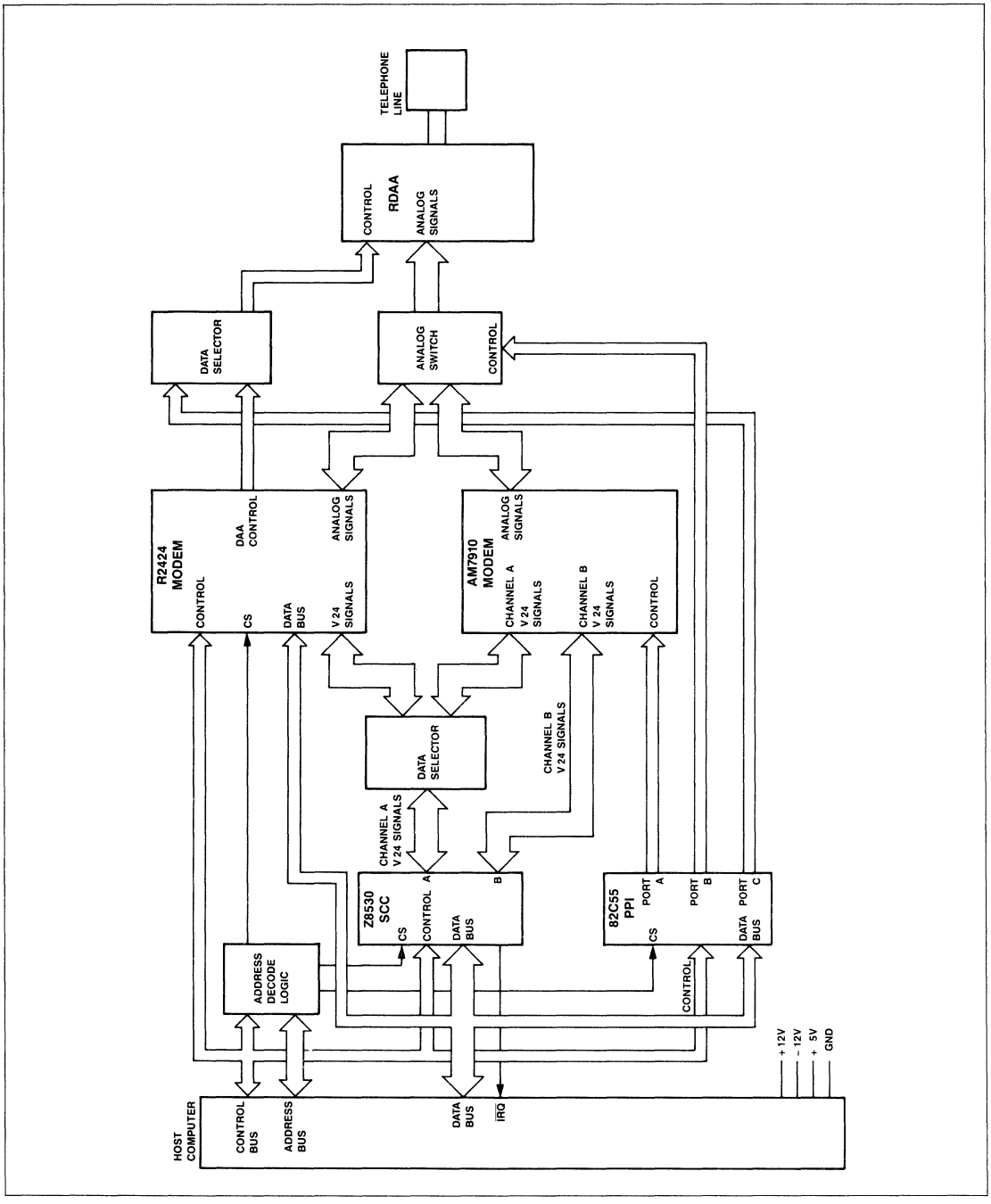

Figure 2. International Modem Hardware Block Diagram

Table 2. International Modem I/O Addresses

Address (Hex)	Register Description
200	R2424 Receiver Reserved
201	R2424 Receiver Reserved
202	R2424 Receiver Diagnostic 1
203	R2424 Receiver Diagnostic 2
204	R2424 Receiver Diagnostic 3
205	R2424 Receiver Diagnostic 4
206	R2424 Receiver Reserved
207	R2424 Receiver Reserved
208	R2424 Receiver Status 1
209	R2424 Receiver Status 2
20A	R2424 Receiver Configuration 1
20B	R2424 Receiver Configuration 2
20C	R2424 Receiver Configuration 3
20D	R2424 Receiver Configuration 4
20E	R2424 Receiver Handshake
20F	R2424 Receiver Diagnostic Control
210	R2424 Transmitter Dial Digit Register
211	R2424 Transmitter Reserved
212	R2424 Transmitter Diagnostic 1
213	R2424 Transmitter Diagnostic 2
214	R2424 Transmitter Diagnostic 3
215	R2424 Transmitter Diagnostic 4
216	R2424 Transmitter Reserved
217	R2424 Transmitter Reserved
218	R2424 Transmitter Status 1
219	R2424 Transmitter Configuration 1
21A	R2424 Transmitter Configuration 2
21B	R2424 Transmitter Configuration 3
21C	R2424 Transmitter Configuration 4
21D	R2424 Transmitter Configuration 5
21E	R2424 Transmitter Handshake
21F	R2424 Transmitter Diagnostic Control
220	Z8530 Channel B Command
221	Z8530 Channel B Data
222	Z8530 Channel A Command
223	Z8530 Channel A Data
224–	Not Used
22F	Not Used
230	82C55 Port A
231	82C55 Port B
232	82C55 Port C
233	82C55 Control Register
234–	Not Used
23F	Not Used

All data between the host computer and the modem is transferred over the bidirectional data bus (D0-D7). The data bus carries data to be transmitted to the modem (TXD) and to be received from the modem (RXD) via the Z8530 SCC, as well as control/status signals to/from the R2424 modem, the Z8530 SCC and the 82C55 PPI. U13b, U13c and U13d enable data bus buffer U3 when an I/O read or I/O write occurs in a valid address range. The direction of the data bus buffer is controlled by the host computer I/O read line ($\overline{IOR}$) gated with the valid I/O address signal appearing at U13d/11.

Z8530 SCC

The Z8530 SCC (U6) transfers the data from the modems to the data bus and converts the data from parallel to serial and serial to parallel between the host computer and the modem devices and provides asynchronous formatting and unformatting. The SCC has two I/O channels (A and B). Channel A is used for all full duplex modes; channel B is used in a V.23 half duplex mode where a secondary channel is used.

Outgoing data (TXD) written from the host computer is serialized and formatted by the Z8530 SCC (U6). It is then output on the TXDA or TXDB pin in serial form.

Incoming data (RXD) from the modem is input to the SCC on the RXDA or RXDB pin and is read via the data bus from the SCC data register. The data is then routed to the PC display (application note software), or it may be routed to a different destination (user-provided software).

The SCC A/$\overline{B}$ input selects channel A or B. The SCC $\overline{C}$/D input determines if control or data information is being accessed. The $\overline{WR}$ and $\overline{RD}$ inputs determine if data is being written to or read from the SCC, respectively. The $\overline{CE}$ input is low at address 220-223 to enable the SCC.

R2424 Modem

The R2424 is mapped into the PC I/O addresses 200H-21FH. The R2424 receiver is enabled by $\overline{CS0}$ (200H-20FH) and the transmitter is enabled by $\overline{CS1}$ (210H-21FH). This enables access to the 32 locations required by the receiver and transmitter interface memories. Host computer address lines A0-A3 are routed to R2424 register select inputs R0-R3, respectively, to access the required interface memory location.

For more information on the R2424 refer to the R2424 Data Sheet (Order No. MD11) and Section 4 (R1212/R2424 Modem Functional Characteristics) in the Modem Interface Guide (Order No. 685), both available from Rockwell International.

Am7910 Modem

Operation of the Am7910 modem is controlled by five configuration inputs (MC0-MC4). Table 3 lists the available modes and identifies the modes used in this application note. The Am7910 configuration signals are controlled by PPI (U7) ports PA0-PA4 since there is no direct host computer bus interface.

The V.24 control signals are routed from the Z8530 SCC (U6). The primary channel (used for all full duplex modes) is routed to the SCC channel A and the Am7910 secondary channel (used for the 1200 half duplex mode) is routed to the SCC channel B.

The clock for the Am7910 is provided by the SCC output TRxCA.

V.24 Interface

TTL V.24 signals are routed to/from the R2424/Am7910 modems as selected by U9 and U10. The $\overline{RLSD}$, $\overline{CTS}$ and RXD outputs from either the R2424 or the Am7910 are switched through U9 to Z8530 SCC (U6) channel A inputs $\overline{DCDA}$, $\overline{CTSA}$ and RXDA, respectively. PPI PA5 output high selects Am7910 signals; PPI PA5 output low selects R2424 signals.

The TXD input to both the R2424 and the Am7910 is routed directly from the SCC TXDA output. The $\overline{RTS}$ input to the R2424 and/or the Am7910 is routed from the SCC $\overline{RTSA}$ output through U10. The $\overline{RTS}$ input to the R2424 is enabled through U10 by PPI PA6 output low. The $\overline{RTS}$ input to the Am7910 is enabled through U10 by PPI PA7 output low.

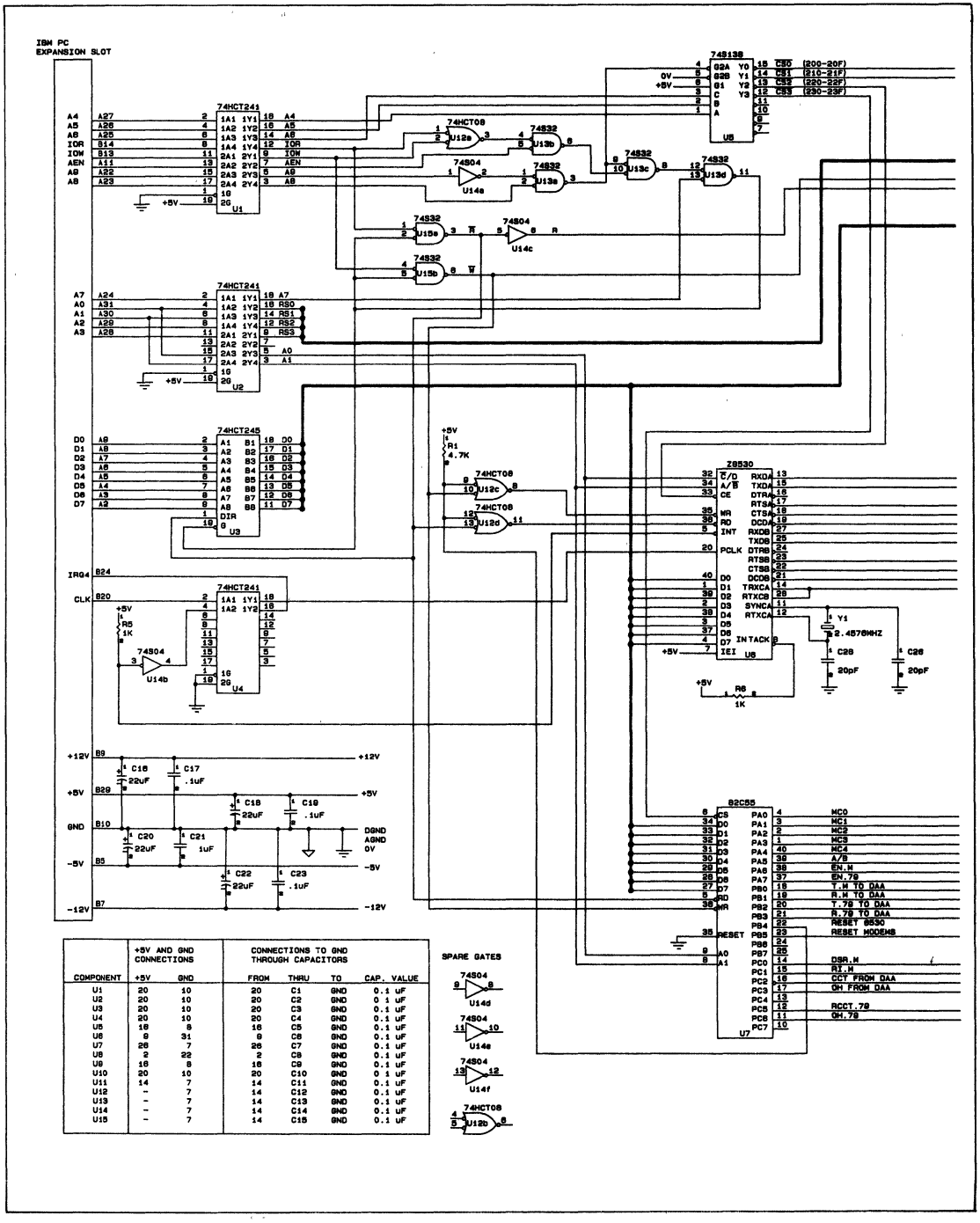

Figure 3. International Modem Schematic

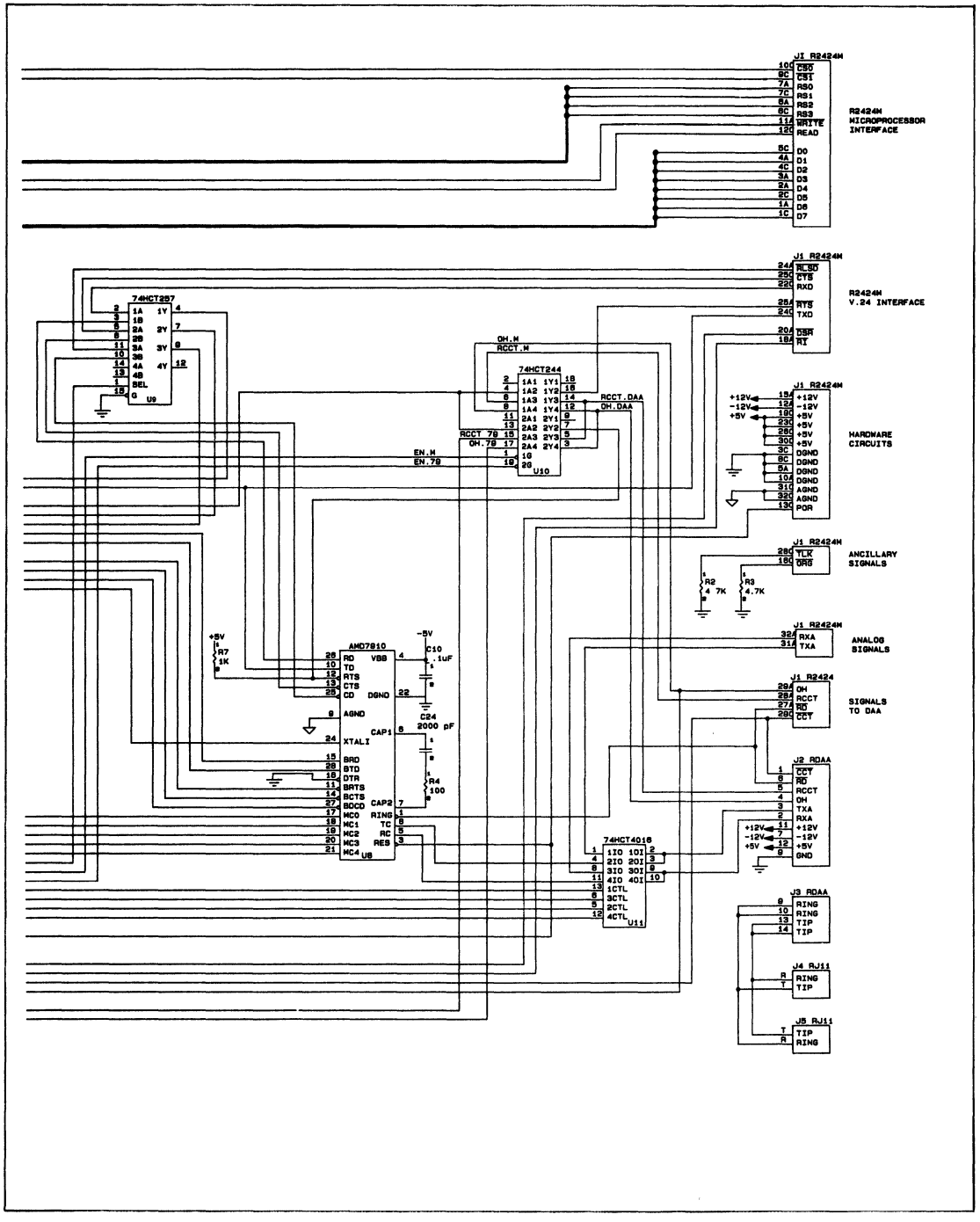

Figure 3. International Modem Schematic (Continued)

Table 3. Am7910 Mode Selection

MC4	MC3	MC2	MC1	MC0	Mode
0	0	0	0	0	Bell 103 Originate 300 bps Full Duplex
0	0	0	0	1	Bell 103 Answer 300 bps Full Duplex
0	0	0	1	0	Bell 202 1200 bps Half Duplex
0	0	0	1	1	Bell 202 with Equalizer 1200 bps Full Duplex
0	0	1	0	0	V.21 Originate 300 bps Full Duplex*
0	0	1	0	1	V.21 Answer 300 bps Full Duplex*
0	0	1	1	0	V.23 Mode 2 1200 bps Half Duplex*
0	0	1	1	1	V.23 Mode 2 with Equalizer 1200 bps Half Duplex
0	1	0	0	0	V.23 Mode 1 600 bps Half Duplex
1	0	0	0	0	Bell 103 Originate Loopback
1	0	0	0	1	Bell 103 Answer Loopback
1	0	0	1	0	Bell 202 Main Loopback
1	0	0	1	1	Bell 202 with Equalizer Loopback
1	0	1	0	0	V.21 Originate Loopback
1	0	1	0	1	V 21 Answer Loopback
1	0	1	1	0	V.23 Mode 2 Main Loopback
1	0	1	1	1	V.23 Mode 2 with Equalizer Loopback
1	1	0	0	0	V.23 Mode 1 Main Loopback
1	1	0	0	1	V.23 Back Loopback

* Modes implemented in application note software.

82C55 PPI

The 82C55 PPI handles control signals between the host computer and the Am7910 modem and various TTL switches, data selectors/multiplexers and buffers. The functions of the bits in the PPI registers are listed in Table 4.

Port A signals control the Am7910 configuration and the U10 switch. Port B output signals control U11 to select the routing of TXA and RXA between the RDAA and either the R2424 or the Am7910. Port B output signals also control the resetting of the modems and the PPI. Port C inputs monitor $\overline{RTS}$ and $\overline{CTS}$ from the R2424 and OH and $\overline{CCT}$ signals from the R2424. The Port C outputs issue OH and $\overline{CCT}$ to the RDAA via U10.

RDAA Interface

Routing selection of TXA to the RDAA and RXA from the RDAA is controlled by U11. TXA is routed from the R2424 (TXA) or the Am7910 (TC) and RXA is routed to the R2424 (RXA) or the Am7910 (RC). OH and RCCT originate from the R2424 (OH and RCCT) or from the 82C55 PPI (OH.79 on PC6 and RCCT.79 on PC7) as selected by U10. $\overline{RD}$ is routed from the RDAA to the R2424 ($\overline{RD}$) and Am7910 ($\overline{RING}$) in parallel. CCT is routed to the R2424 ($\overline{CCT}$) and to the PPI (CCT on PC2).

MODEM OPERATION

Originate Mode

Modem operation is divided into two parts: originate and answer. In the originate mode, the R2424 always does the dialing, regardless of the final configuration. If a V.22 or V.22 bis connection is desired, the default hardware setup (initialized by application software) permits the R2424 to stay on line after dialing and connect with the remote modem. If a V.21 or V.23 connection is desired, then the R2424 dials the call. After dialing, a set of control signals (OH and $\overline{CCT}$) is generated to keep the DAA connected to the phone line. Meanwhile, the R2424 is disconnected and the Am7910 is configured for the desired mode. When the remote modem answers the Am7910 has control of the line and is set up to be in originate mode. The connection places the modem in data mode in either V.21 or V.23.

Answer Mode

In the answer mode, the modem must be capable of answering an incoming call from a modem of unknown configuration. The R2424 always answers the call, regardless of the final configuration. Because the default setup condition exists, the R2424 sends out the CCITT answertone and waits for the response from the remote modem. The software determines the configuration of the remote modem within one second of Data Set Ready becoming active in the R2424. It does this by first examining the SPEED bits.

If the SPEED bits are set to 11 (binary), then the modem is connected in V.22 bis mode at 2400 bps. If the SPEED bits are set to 10, then the modem is connected in V.22 mode at 1200 bps. If the SPEED bits are set to 00 then the calling modem is a V.21 or V.23 type. The RLSD bit of the R2424 is then examined. If it is set to 1, then the calling modem is a V.23 modem, otherwise it is a V.21 modem. At this time the Am7910 is already in data mode, although not connected to the line. (The ringing signal supplied by the DAA is shared by the R2424 and the Am7910, so both go off hook in answer mode.) When the software determines that a V.21 or V.23 connection is in progress, it holds the line by generating a set of control signals for the DAA. The R2424 is switched out and the Am7910 is switched in to the line, already in data mode. The remote modem received 2100 Hz answertone from the R2424. Now the Am7910 completes the handshake and the modems enter the data mode.

OPERATING PROCEDURE

The procedure to operate the modem using the application note software is described in this section. It is assumed that the user has entered, edited and stored the FORTH screens listed in Figure 15. It also assumes that the FORTH command level has been invoked.

Table 4. 82C55 Port Functions

Port	Bit	Function	7910	R2424
Port A—8 Outputs (0-7)				
PA0	0	7910 Configuration Pin MC0	X	
PA1	1	7910 Configuration Pin MC1	X	
PA2	2	7910 Configuration Pin MC2	X	
PA3	3	7910 Configuration Pin MC3	X	
PA4	4	7910 Configuration Pin MC4	X	
PA5	5	RXD, $\overline{CTS}$, $\overline{DCD}$ Modem Select 1 = 7910 0 = 2424	X	X
PA6	6	$\overline{DTR}$, $\overline{RTS}$, RCCT, OH Disable to R2424 1 = Disable 0 = Enable	X	X
PA7	7	$\overline{DTR}$, $\overline{RTS}$, RCCT, OH Disable to 7910 1 = Disable 0 = Enable	X	X
Port B—8 Outputs (0-7)				
PB0	0	R2424 TXA to DAA 1 = Enable 0 = Disable	X	X
PB1	1	R2424 RXA to DAA 1 = Enable 0 = Disable	X	X
PB2	2	7910 TC to DAA 1 = Enable 0 = Disable	X	X
PB3	3	7910 RC to DAA 1 = Enable 0 = Disable	X	X
PB4	4	Reset Z8530 (Pulse) 1 = Normal 0 = Reset		
PB5	5	Reset Modems (Pulse) 1 = Normal 0 = Reset	X	X
PB6	6	Not Used		X
PB7	7	Not Used		X
Port C—4 Inputs (0-3), 4 Outputs (4-7)				
PC0	0	Read R2424 $\overline{DSR}$		X
PC1	1	Read R2424 $\overline{RI}$		X
PC2	2	Read Status of $\overline{CCT}$ from DAA		X
PC3	3	Read Status of OH from DAA		
PC4	4	Not Used		
PC5	5	Set RCCT on DAA for 7910 1 = Set 0 = Off	X	
PC6	6	Set OH on DAA for 7910 1 = Off-Hook 0 = On-Hook	X	
PC7	7	Not Used		

Type 70 LOAD and press RETURN.

When loading is complete, the software initializes and configures all devices for the default settings. A menu screen is then displayed on the terminal. This menu is function key driven and prompts the user for a choice of five keys to press for different options. Four originate modes are presented and one universal auto answer mode. The four originate modes allow the modem to connect at 300 bps in V.21 mode, 1200 bps in V.22, 2400 bps in V.22 bis and 1200 bps in V.23. The universal auto answer mode connects at the speed and configuration of the calling modem (initially unknown).

The displayed menu is:

INTERNATIONAL MODEM

F1 V.21 ORIGINATE
F2 V.22 ORIGINATE 1200
F3 V.22 ORIGINATE 2400
F4 V.23 ORIGINATE
F5 UNIVERSAL AUTO ANSWER

When the menu screen is displayed, the modem is in idle mode and the program is waiting for a function to be requested. To initiate a mode, press the corresponding function key.

Originate Mode

If an originate key is pressed, the user is prompted to enter the phone number to call. Upon number entry, the call is placed (always by the R2424). If a V.22 or V.22 bis configuration was selected then the R2424 stays connected to the line after placing the call. Otherwise, the Am7910 is switched in to complete the handshake with the remote modem. Once the modem is in data mode the program enters the dumb terminal routine.

After an originate mode is selected, the system will display one of the following messages depending on the selected mode:

V.21 300 BPS MODE
V.22 1200 BPS MODE
V.22 2400 BPS MODE
V.23 1200 BPS MODE*

followed by

ENTER PHONE NUMBER

Enter the telephone number to call and press ENTER.

Upon carrier detection and line connection the system will display:

CARRIER DETECTED . . . ON LINE
TERMINAL ON LINE

To terminate the mode anytime during the operation, press CTRL BREAK. After connection is established, pressing ' (single quote) will also terminate the mode. After terminating the mode, press RETURN to return to FORTH command entry level. Now type MENU and press RETURN to disconnect the modem from the line and to display the mode menu.

*V23 call origination results in a half duplex data mode connection. This application note software configures the originate modem for transmitting by asserting $\overline{RTS}$. In order to receive data, $\overline{RTS}$ must be made inactive.

Auto Answer Mode

In the universal auto answer mode, the program waits for the phone to ring. It then answers the call with the R2424 which sends out a 2100 Hz answertone. The R2424 decides the speed and configuration of the calling modem from the response from the calling modem. Depending on the response, the line is left connected to the R2424 or switched to the Am7910. When the handshake is complete, the program enters the dumb terminal routine.

When the universal auto answer mode is selected, the system will display:

```
UNIVERSAL AUTO ANSWER MODE
WAITING TO BE CALLED
```

Place the call from the remote modem. Upon ring detection and Data Set Ready assertion, the system will display:

```
RING DETECTED
DATA SET READY ON
```

followed by one of the following messages when the corresponding connection is made:

```
CONNECTED TO V.21 MODEM AT 300 BPS
CONNECTED TO V.22 MODEM AT 1200 BPS
CONNECTED TO V.22 MODEM AT 2400 BPS
CONNECTED TO V.23 MODEM AT 1200 BPS*
```

then

```
TERMINAL ON LINE . . .
```

To terminate the mode anytime during the operation, press CTRL BREAK. After connection is established, pressing ' (single quote) will also terminate the mode. After terminating the mode, press RETURN to return to FORTH command entry level. Now type MENU and press RETURN to disconnect the modem from the line (if not terminated by the remote modem) and to display the mode menu.

*Answering a call from a V.23 modem results in a half duplex data mode connection. This application note software configures the modem for receiving by keeping $\overline{RTS}$ inactive. In order to transmit data after the remote modem has finished transmitting, $\overline{RTS}$ must be made active.

Dumb Terminal

The dumb terminal routine is used once the modem has completed a connection. Data entered on the PC keyboard is sent to the modem to be transmitted to the remote modem. Incoming data is displayed on the terminal. In order to capture all received data at 2400 bps, it is necessary to interrupt the PC so that the data can be stored in a buffer. (This is because the scrolling actions of the screen take too much time and data would be lost if a polling method were used.) The dumb terminal routine interacts with the USART function in the Z8530 SCC device (U6) on the modem board. There are two main actions running continuously. Keyboard data, if available, is written to the data port of channel A of the Z8530. Then it is sent to the modem via the TXD line. The received data buffer in memory is checked to see if there are any characters waiting in the queue to be displayed. If there are, it displays them.

When the modem receives a character, it is passed to the RXD line of the Z8530. This causes an interrupt to be generated.

The interrupt handling routine services the interrupt by transferring the received data byte from the data port to the next location in the buffer in memory. Housekeeping is done on the buffer pointers and the loop then repeats itself.

SOFTWARE

Structure

The overall operation of the software is flowcharted in Figure 4. Figures 5 through 8 show subsections of the main routines, such as basic default settings for the devices. The command flow to control the modem in each of its configurations is shown in Figures 9 through 13.

If an originate connection is selected from the menu, then the flowcharts of Figure 11 and Figure 12 show the actions which are performed to set up the modem, make the call and enter the data state. The algorithm for the universal auto answer mode is given in Figure 13. This allows the modem to connect with an unknown calling modem which may be one of four different standards; V.21, V.22, V.22 bis or V.23. The modem automatically reconfigures itself and connects to the remote modem.

Programming

The application note software is programmed in FORTH. The FORTH screens are listed in Figure 15. Any FORTH system implementing the FORTH '83 standard for execution on the IBM PC should be compatible. The compiled screens presented here add the extra customized FORTH primitives to the Kernel dictionary. Operation of the modem is governed by routines using these words to control the hardware circuits from software. The software can be user-customized for a particular application. Alternatively, the listing is complete as supplied. There is an interrupt driven dumb terminal program included, which is capable of handling 2400 bps full duplex communications.

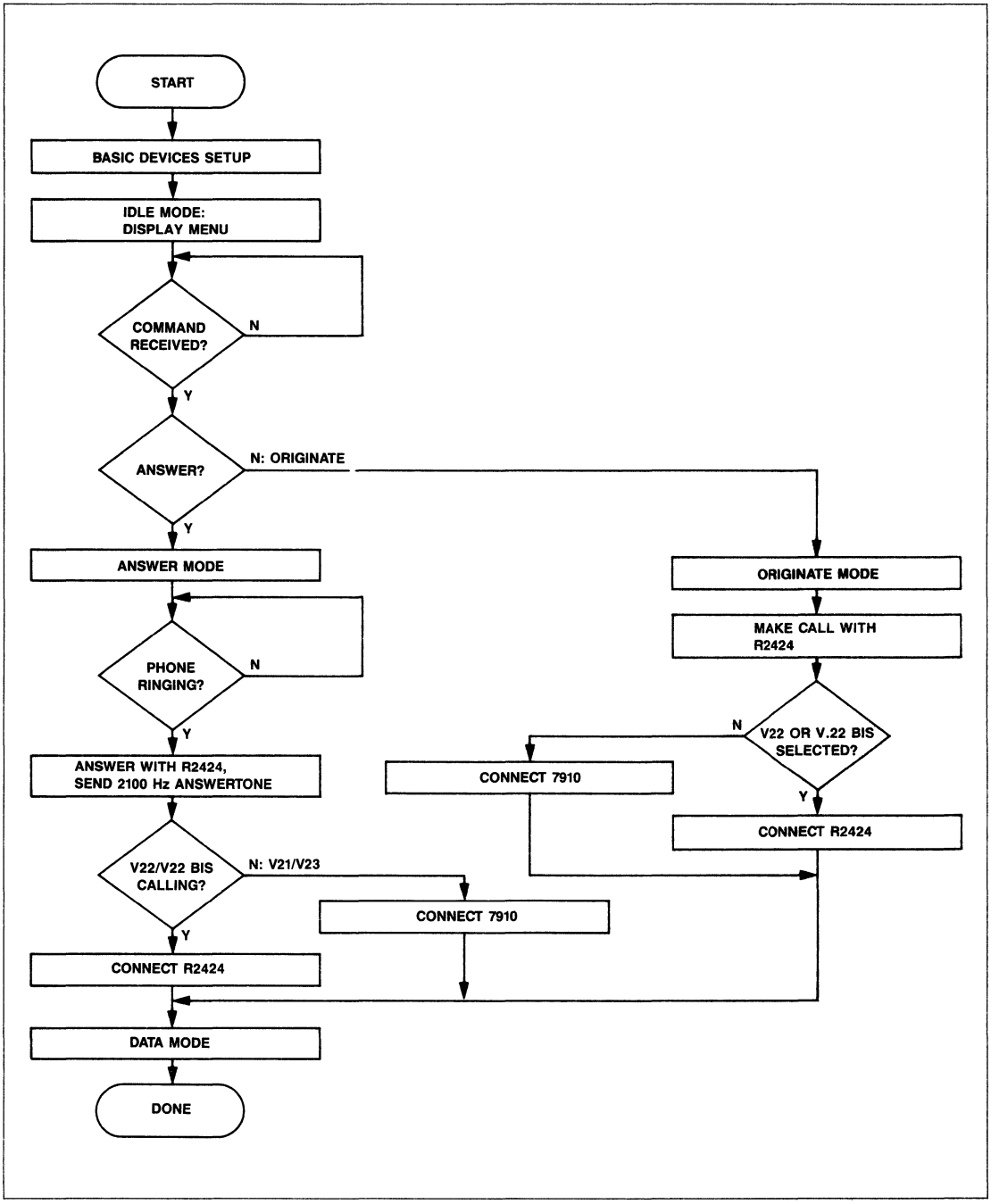

Figure 4. Flowchart — International Modem Software Overview

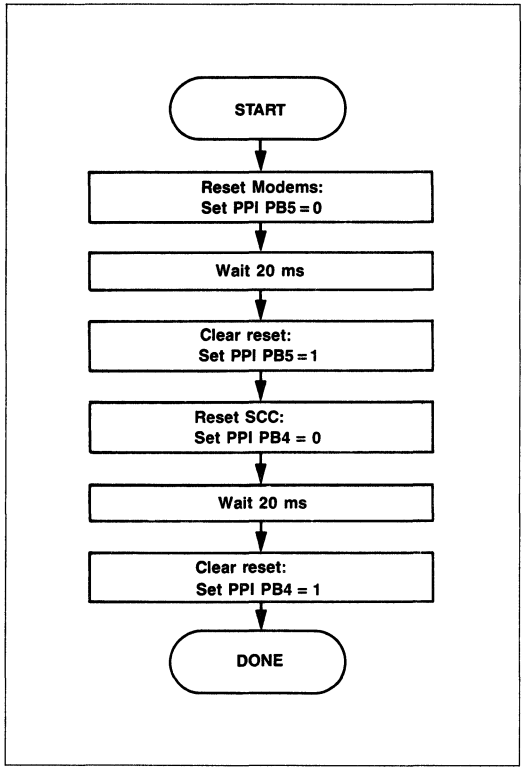

Figure 5. Flowchart — Reset Devices

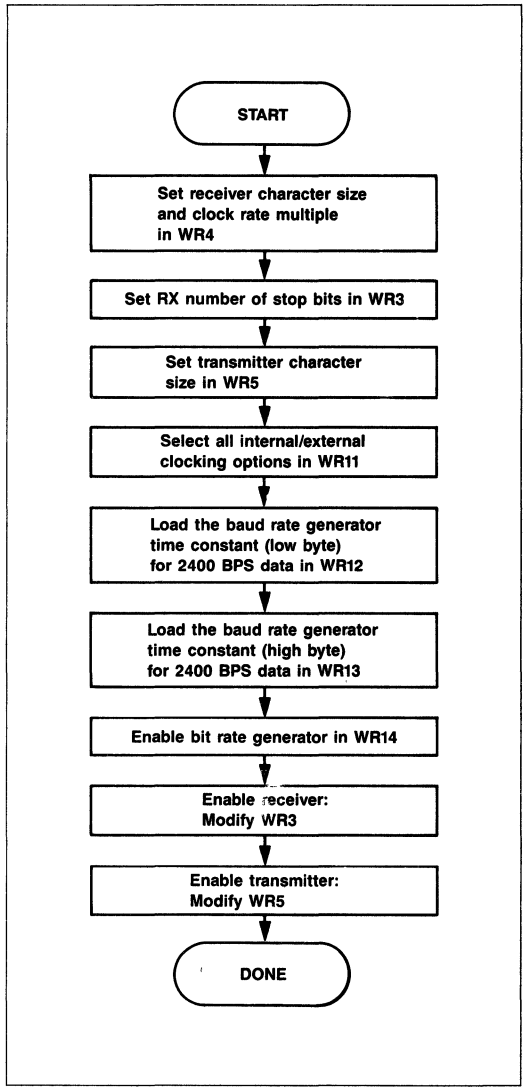

Figure 6. Flowchart — Basic Devices Setup: 8530

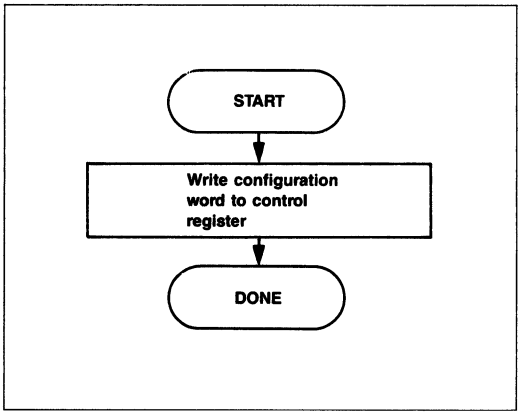

Figure 7. Flowchart — Basic Devices Setup: 82C55

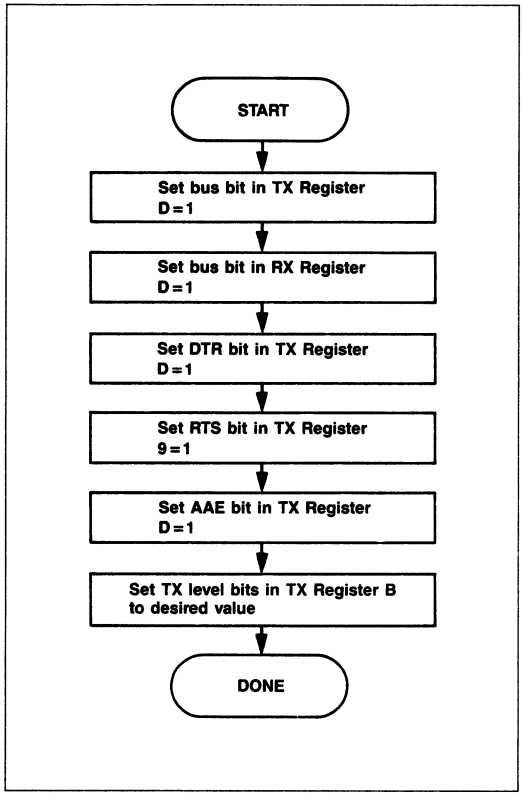

Figure 8. Flowchart — Basic Devices Setup: R2424

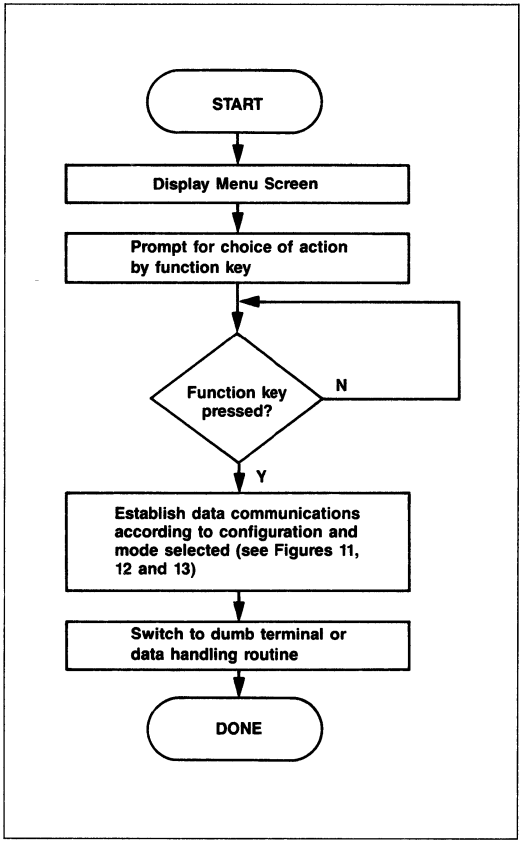

Figure 9. Flowchart — Main Operation

4

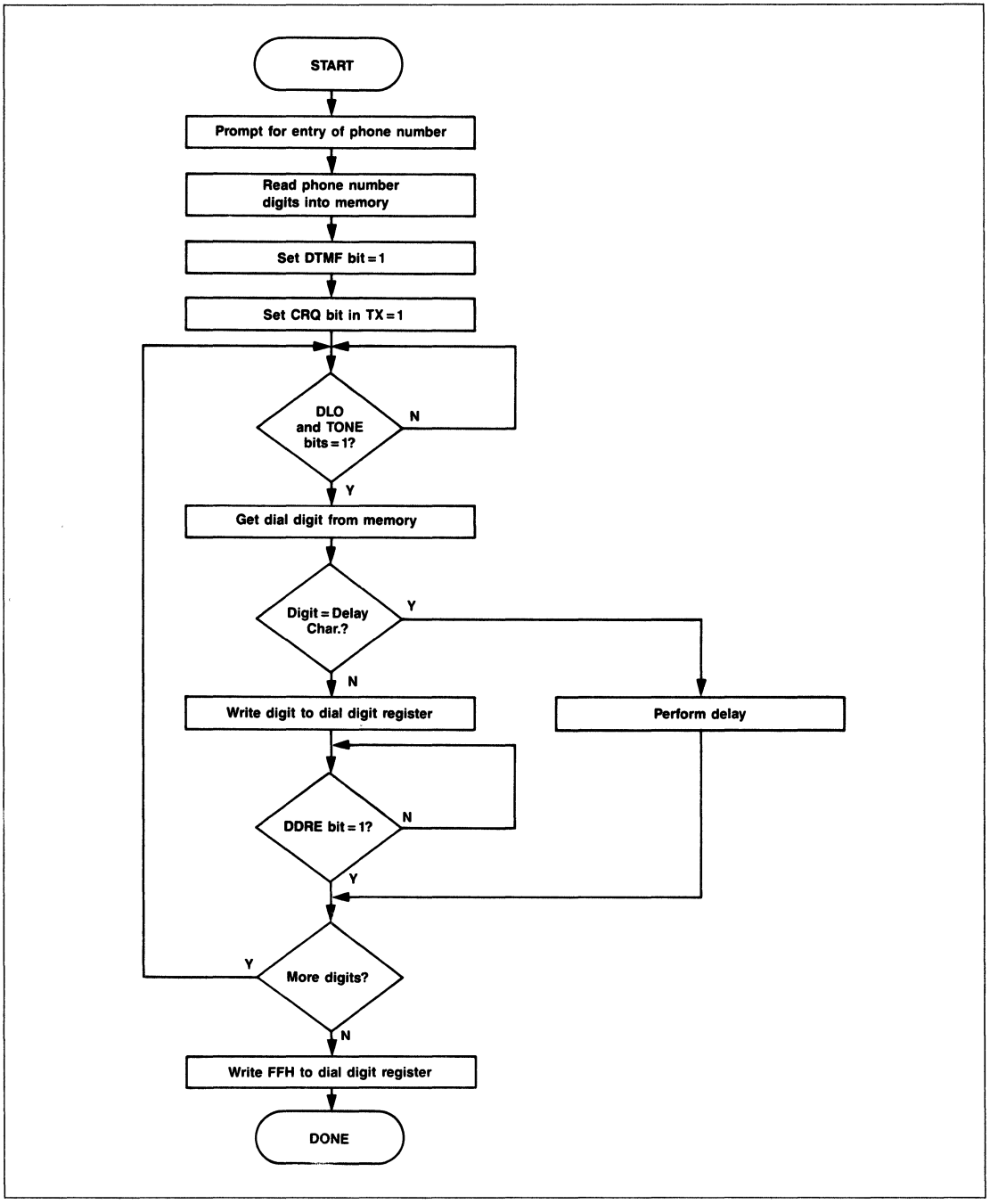

Figure 10. Flowchart — Auto Dial

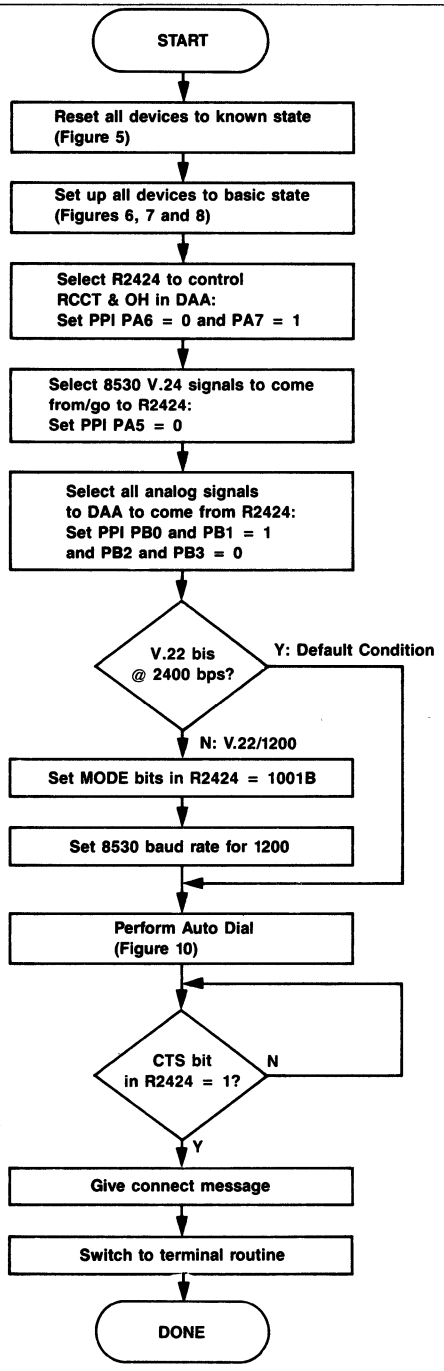

Figure 11. Flowchart — V.22 or V.22 bis Call Origination

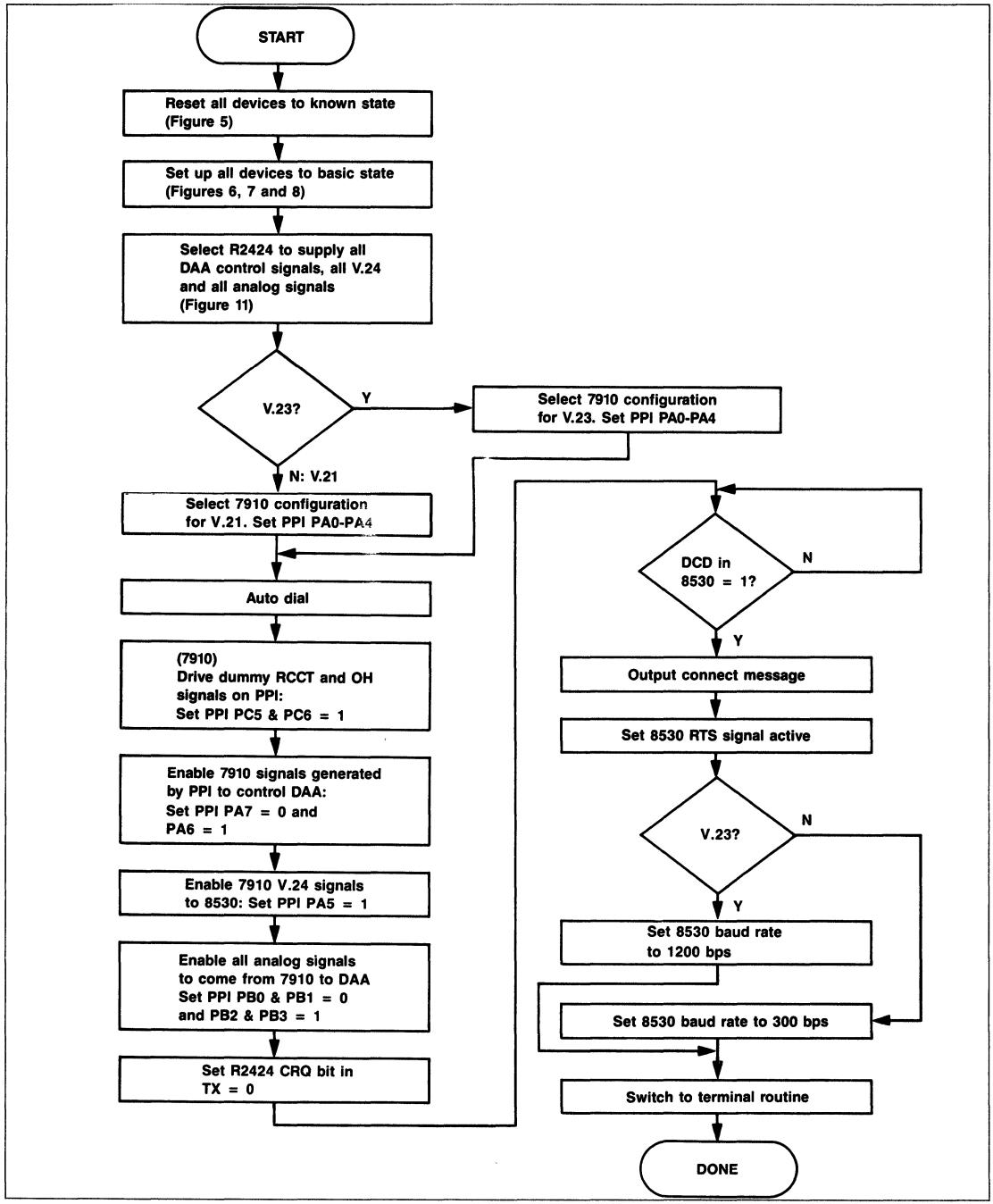

Figure 12. Flowchart — V.21 or V.23 Call Origination

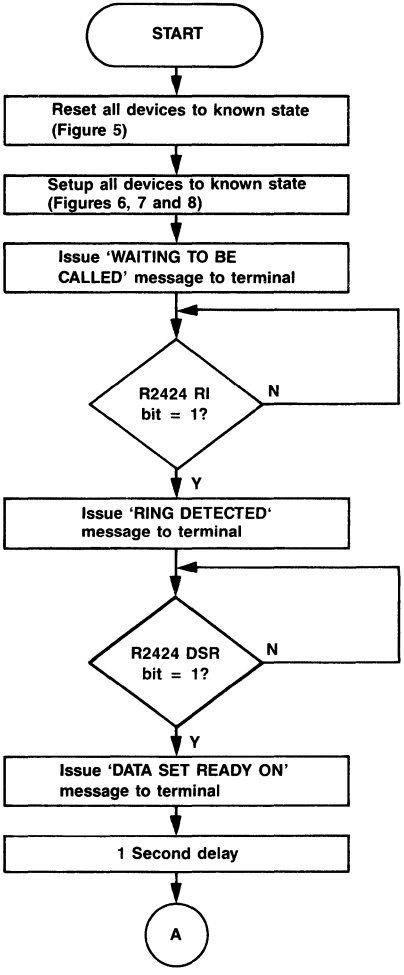

Figure 13. Flowchart — Universal Auto Answer Mode

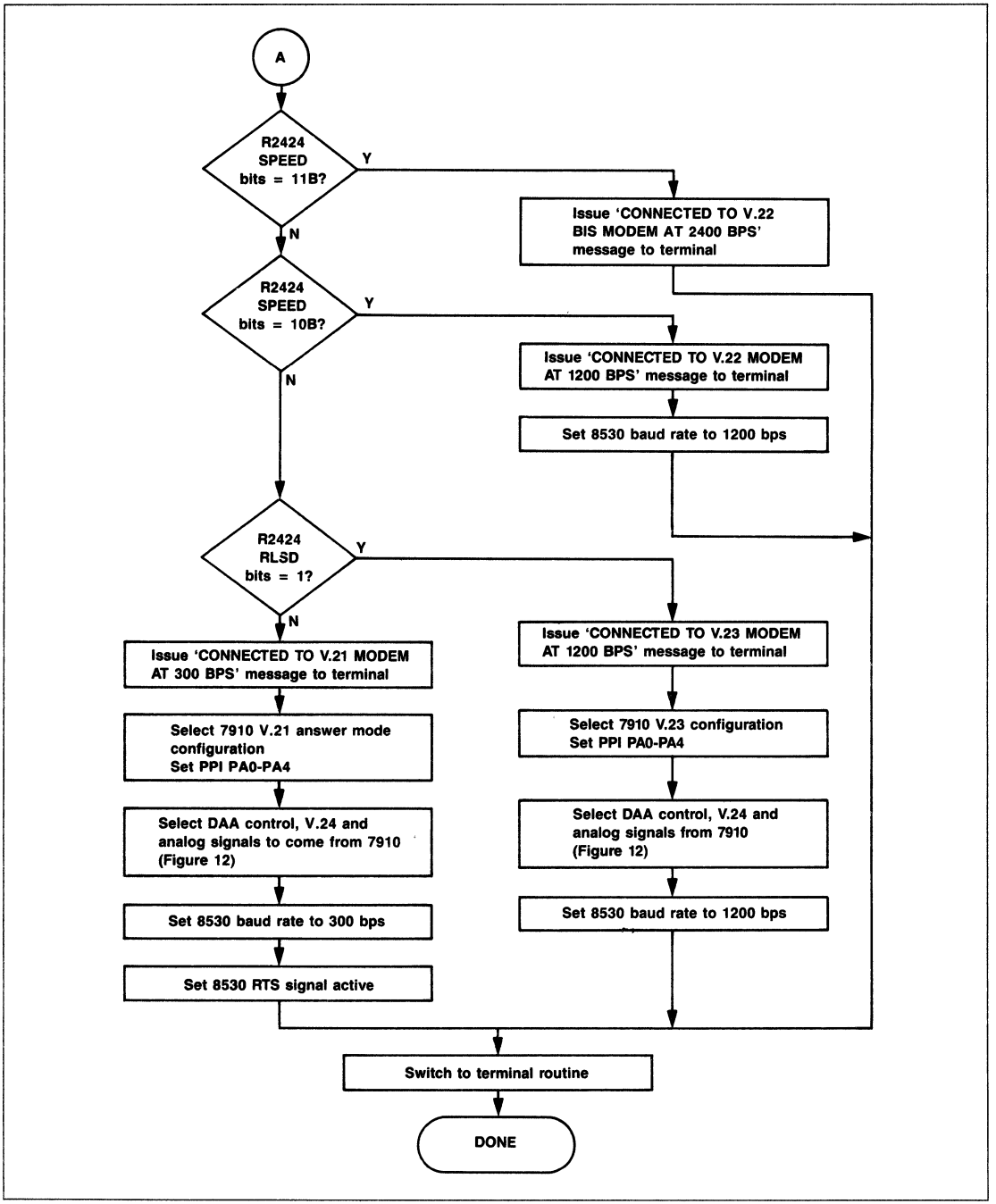

Figure 13. Flowchart — Universal Auto Answer Mode (Continued)

```
Screen # 69
  0
  1
  2
  3
  4
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15


Screen # 70
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 FORTH DEFINITIONS HEX
  2
  3  -1 CONSTANT COM1?
  4   0 CONSTANT COM2?
  5
  6 COM1? .IF
  7   0223 CONSTANT ASC_PORT
  8   0010 CONSTANT INT_MASK        ( IRQ4 )
  9   000C CONSTANT INT_#
 10 .THEN  COM2? .IF
 11   0223 CONSTANT ASC_BASE
 12   0008 CONSTANT INT_MASK        ( IRQ3 )
 13   000B CONSTANT INT_#
 14 .THEN
 15 -->


Screen # 71
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 DECIMAL
  2
  3 2VARIABLE LINKS
  4 VARIABLE X VARIABLE V
  5
  6 : FIX-VOC-LINKS
  7         VOC-LINK DUP  X !   @ V !
  8         BEGIN   V @
  9         WHILE   V @ HERE U<
 10                 IF    V @ X @ !  V @ X !  X @ @ V !
 11                 ELSE  V @ @ V !  THEN
 12         REPEAT ;
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens

```
Screen # 72
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 : BEGIN-MOD    1 ?DEPTH HERE LINKS !
  2         LATEST NAME> LINKS 4+ !
  3         LIMIT 500 - SWAP - DP ! ;
  4
  5 : END-MOD  LINKS @ DP ! ;
  6
  7 : FORGET-MOD    LINKS 4+ @
  8         SHR4
  9         LINKS @ 32 0 SKIP DROP
 10         N>LINK W!  FIX-VOC-LINKS ;
 11
 12
 13
 14
 15 -->
Screen # 73
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 DECIMAL  17000 BEGIN-MOD  ASM86  END-MOD
  3
  4 HEX
  5
  6 2000 CONSTANT ASC_BUF_SIZE
  7
  8 CREATE  ASC_BUF  ASC_BUF_SIZE ALLOT
  9         ASC_BUF  ASC_BUF_SIZE ERASE
 10
 11 VARIABLE ASC_IN
 12 VARIABLE ASC_OUT
 13
 14
 15 -->
Screen # 74
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 0 INT_# 4 * 2CONSTANT INT-VEC
  3
  4 2VARIABLE PREV_ASC_VEC
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 75
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 : INCR_PTR       ROT
  3                  2 PICK @ +
  4                  2DUP <=
  5                  IF   SWAP -
  6                  ELSE SWAP DROP
  7                  THEN SWAP ! ;
  8
  9 : +ASC_IN        ASC_IN  ASC_BUF_SIZE INCR_PTR ;
 10 : +ASC_OUT       ASC_OUT ASC_BUF_SIZE INCR_PTR ;
 11
 12
 13
 14
 15 -->
Screen # 76
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 : ?ASC           ASC_IN @  ASC_OUT @  <> ;
  3
  4 : @ASC           BEGIN ?ASC
  5                  UNTIL ASC_OUT @ ASC_BUF + C@  1 +ASC_OUT ;
  6
  7 : #ASC           ASC_OUT @ ASC_IN @ 2DUP U>
  8                  IF    ASC_BUF_SIZE +   THEN  - NEGATE ;
  9
 10
 11
 12
 13
 14
 15 -->
Screen # 77
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2 CREATE ASC_INT   ASSEMBLER
  3                  STI
  4                  AX PUSH  BX PUSH
  5                  DX PUSH  DS PUSH
  6                  AX, CS MOV  DS, AX MOV
  7                  DX, # ASC_PORT MOV
  8                  AL, DX IN
  9                  CLI
 10                  BX, ASC_IN 2+ MOV
 11                  ASC_BUF [BX], AL MOV
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 78
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2                  BX INC
  3                  BX, # ASC_BUF_SIZE CMP
  4                  1$ JNZ
  5                  BX, BX XOR
  6          1$:     ASC_IN 2+ , BX MOV
  7                  STI
  8                  AL, # 20 MOV
  9                  # 20 , AL OUT
 10                  DS POP  DX POP
 11                  BX POP  AX POP
 12                  IRET
 13 FORTH
 14
 15 -->
Screen # 79
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2 : ASC-TRAP       PREV_ASC_VEC 2@ OR 0=
  3                  IF   INT-VEC @L
  4                       INT-VEC 2+ @L
  5                       PREV_ASC_VEC 2!
  6                  THEN
  7                  ?CS:  INT-VEC 2+ !L
  8                  ASC_INT INT-VEC !L  ;
  9
 10
 11
 12
 13
 14
 15 -->
Screen # 80
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 : ASC-RELEASE    PREV_ASC_VEC 2@
  3                  INT-VEC 2+ !L
  4                  INT-VEC !L ;
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 81
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2 : ASC-ENB
  3                  21 PC@
  4                  INT_MASK NOT  AND
  5                  21 PC!
  6
  7                  ASC_IN OFF ASC_OUT OFF
  8                  ASC_BUF ASC_BUF_SIZE ERASE ;
  9
 10
 11
 12
 13
 14
 15 -->
Screen # 82
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2
  3 : ASC-DSB        21 PC@
  4                  INT_MASK OR
  5                  21 PC! ;
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->
Screen # 83
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 : ASC-ON         ASC-TRAP   ASC-ENB ;
  3
  4 : ASC-OFF        ASC-DSB  ASC-RELEASE ;
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 84
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2
  3 : ASC_TX_WAIT   BEGIN  ASC_PORT 1 -  PC@  40 AND
  4                 UNTIL ;
  5
  6 : !ASC          ASC_TX_WAIT   ASC_PORT PC! ;
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->

Screen # 85
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 HEX HERE 0FFF0 U>
  3
  4 .IF     CR
  5         CR
  6         CR
  7         CR
  8
  9         FORGET COM1?  ." ERROR....MUST BE LOADED BELOW FFF0 "
 10
 11 .THEN   DECIMAL  FORGET-MOD
 12 -->
 13
 14
 15

Screen # 86
  0 ( V21/V23 MODEM  DUMB TERMINAL                        27/1/86 MBW )
  1 FORTH DEFINITIONS DECIMAL
  2 HEX
  3 ( --- )
  4 : TALK       CR ." TERMINAL ON LINE . . . ." CR CR ASC-ON
  5         BEGIN   ?ASC
  6                 IF    @ASC  7F AND EMIT
  7                 THEN
  8                 ?TERMINAL
  9                 IF    KEY  DUP 27 =
 10                       IF   DROP CLS QUIT
 11                       ELSE !ASC
 12                       THEN
 13                THEN
 14         AGAIN ;
 15 DECIMAL -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 87
  0 ( V21/V23 MODEM   TIMERS                                  27/1/86 MBW )
  1 DECIMAL
  2 : ALL ;
  3 : MS
  4   0 DO 22 0 DO LOOP LOOP ;
  5 : SEC
  6   1000 * MS ;
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 88
  0 ( V21/V23 MODEM   INITIALISATION                          27/1/86 MBW )
  1 HEX
  2 : INIT.8255   81 233 PC! ; ( 2 1/2 OUTPUT PORTS 1/2 INPUT )
  3 : RESET.MODEMS   231 PC@ DUP DF AND ( SET PB5 TO 0 )
  4                  231 PC!
  5                  20 MS
  6                  20 OR 231 PC!       ( SET PB5 TO 1 )
  7                  50 MS ;
  8 : RESET.8530   231 PC@ DUP EF AND ( SET PB4 TO 0 )
  9                231 PC!
 10                20 MS
 11                10 OR 231 PC!
 12                20 MS ;
 13 : INIT   INIT.8255 RESET.MODEMS RESET.8530 ; ( EVERYTHING )
 14 DECIMAL
 15 -->
Screen # 89
  0 ( V21/V23 MODEM   ENABLES/DISABLES                        27/1/86 MBW )
  1 HEX
  2 : EN.RCCT/OH.M   230 PC@ BF AND              ( MAKE PA6=0 )
  3                      80 OR  230 PC!          ( MAKE PA7=1 ) ;
  4 : EN.RCCT/OH.79  230 PC@ 7F AND              ( MAKE PA7=0 )
  5                      40 OR  230 PC!          ( MAKE PA6=1 ) ;
  6 : EN.V24.79      230 PC@ 20 OR  230 PC!      ( MAKE PA5=1 ) ;
  7 : EN.V24.M       230 PC@ DF AND 230 PC!      ( MAKE PA5=0 ) ;
  8 : EN.ANALOG.M    231 PC@ 03 OR               ( PB0/ PB1=1 )
  9                  F3 AND 231 PC!              ( PB2/ PB3=0 ) ;
 10 : EN.ANALOG.79   231 PC@ 0C OR               ( PB0/ PB1=0 )
 11                  FC AND 231 PC!              ( PB2/ PB3=1 ) ;
 12 : ENABLE.INT.8530   1 222 PC! 10 222 PC!     ( SET INT ON RX )
 13                     9 222 PC! 0A 222 PC! ;   ( MIE          )
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 90
  0 ( V21/V23 MODEM   ENABLES/DISABLES                    27/1/86 MBW )
  1 HEX
  2 : EN.M    EN.RCCT/OH.M  EN.V24.M  EN.ANALOG.M
  3           ( ENABLE ALL R2424 SIGNALS ) ;
  4
  5 : EN.79   EN.RCCT/OH.79 EN.V24.79 EN.ANALOG.79
  6           ( ENABLE ALL 7910 SIGNALS ) ;
  7
  8
  9
 10 : NEWC.R    20E PC@ 08 OR 20E PC!
 11             BEGIN 20E PC@ 8 = NOT UNTIL ;
 12 : NEWC.T    21E PC@ 08 OR 21E PC!
 13             BEGIN 21E PC@ 8 = NOT UNTIL ;
 14 DECIMAL
 15 -->

Screen # 91
  0 ( V21/V23 MODEM   R2424 BIT SETTING  1 OF 2           27/1/86 MBW )
  1 HEX
  2 : NOW    ( FLAG REGISTER MASK -- )
  3   SWAP DUP 2SWAP SWAP ROT ROT
  4          ROT 0 = IF
  5                       FF SWAP - SWAP DUP PC@
  6                       ROT AND SWAP PC!
  7                  ELSE
  8                       SWAP DUP PC@ ROT
  9                       OR SWAP PC!
 10                  THEN
 11
 12
 13
 14
 15 -->

Screen # 92
  0 ( V21/V23 MODEM   R2424 BIT SETTING  2 OF 2           27/1/86 MBW )
  1   DUP 20A >= IF
  2             DUP 20D <= IF
  3                         NEWC.R ELSE
  4                                 DUP 219 >= IF
  5                                          DUP 21D <= IF
  6                                                     NEWC.T
  7                                                  THEN
  8                                          THEN
  9                         THEN
 10             THEN  DROP  ;
 11
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 93
  0 ( V21/V23 MODEM   R2424 BIT CHECKING                    27/1/86 MBW )
  1 HEX
  2 : IS    ( REGISTER MASK -- BIT VALUE )
  3
  4   SWAP PC@ AND IF 1 ELSE 0 THEN ;
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 94
  0 ( V21/V23 MODEM   R2424 RECEIVER BIT MASKS               27/1/86 MBW )
  1 HEX
  2 : BUS.R     20D  80 ;
  3 : CRQ.R     20D  40 ;
  4 : LCD       20D  04 ;
  5 : AL.R      20B  01 ;
  6 : ERDL.R    20A  80 ;
  7 : RDL.R     20A  40 ;
  8 : DL.R      20A  20 ;
  9 : ST.R      20A  20 ;
 10 : TONE      208  80 ;
 11 : ATD       208  40 ;
 12 : TM        208  02 ;
 13 : RLSD      208  01 ;
 14 DECIMAL
 15 -->
Screen # 95
  0 ( V21/V23 MODEM   R2424 TRANSMITTER BIT MASKS            27/1/86 MBW )
  1 HEX
  2 : DDRE      21E  01 ;
  3 : BUS.T     21D  80 ;
  4 : CRQ.T     21D  40 ;
  5 : DATA      21D  20 ;
  6 : AAE       21D  10 ;
  7 : DTR       21D  08 ;
  8 : DSRA      21C  80 ;
  9 : GTE       21B  10 ;
 10 : GTS       21B  08 ;
 11 : 3DB       21B  04 ;
 12 : DTMF      21B  02 ;
 13 : AL.T      21B  01 ;
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 96
  0 ( V21/V23 MODEM   R2424 TRANSMITTER BIT MASKS      27/1/86 MBW )
  1 HEX
  2 : ERDL.T    21A  80 ;
  3 : RDL.T     21A  40 ;
  4 : DL.T      21A  20 ;
  5 : ST.T      21A  10 ;
  6 : RTRN      219  40 ;
  7 : ORG       219  20 ;
  8 : LL        219  10 ;
  9 : RTS       219  08 ;
 10 : CC        219  04 ;
 11 : EF        219  02 ;
 12 : DLO       218  80 ;
 13 : CTS       218  40 ;
 14 DECIMAL
 15 -->

Screen # 97
  0 ( V21/V23 MODEM   R2424 TRANSMITTER BIT MASKS      27/1/86 MBW )
  1 HEX
  2 : DSR       218  20 ;
  3 : RI        218  10 ;
  4
  5
  6
  7
  8
  9
 10
 11
 12
 13 DECIMAL
 14 -->
 15

Screen # 98
  0 ( V21/V23 MODEM   R2424 MULTIPLE BITS              27/1/86 MBW )
  1 HEX
  2 : V.22/1200    20A PC@ F9 AND 09 OR 20A PC! ( SET RX MODE BITS )
  3                NEWC.R
  4                21A PC@ F9 AND 09 OR 21A PC! ( SET TX MODE BITS )
  5                NEWC.T ;
  6 : V.22/2400    20A PC@ FD AND 0D OR 20A PC!
  7                NEWC.R
  8                21A PC@ FD AND 0D OR 21A PC!
  9                NEWC.T ;
 10 : SPEED?       209 PC@ 10 / DUP 4 / 4 * - ; ( -- VALUE OF BITS )
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 99
  0 ( V21/V23 MODEM   R2424 TRANSMIT LEVEL              27/1/86 MBW )
  1 HEX
  2 : 0DB    21B PC@ 0F AND 00 OR 21B PC! NEWC.T ;
  3 : -2DB   21B PC@ 3F AND 20 OR 21B PC! NEWC.T ;
  4 : -4DB   21B PC@ 5F AND 40 OR 21B PC! NEWC.T ;
  5 : -6DB   21B PC@ 7F AND 60 OR 21B PC! NEWC.T ;
  6 : -8DB   21B PC@ 9F AND 80 OR 21B PC! NEWC.T ;
  7 : -10DB  21B PC@ BF AND A0 OR 21B PC! NEWC.T ;
  8 : -12DB  21B PC@ DF AND C0 OR 21B PC! NEWC.T ;
  9 : -14DB  21B PC@ FF AND E0 OR 21B PC! NEWC.T ;
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 100
  0 ( V21/V23 MODEM  8530 SETUP                         27/1/86 MBW )
  1 ( THIS DEFAULT SETTING CONFIGURES THE 8530 FOR 8 BIT DATA,      )
  2 ( 1 STOPBIT,  ENABLES THE TRANSMITTER & RECEIVER, SETS DTR, RTS)
  3 ( SETS THE CLOCKS, XTAL I/P,AND THE BIT RATE GENERATOR FOR 2400)
  4 HEX
  5 : DEFAULT.8530      ENABLE.INT.8530
  6   4 222 PC! 44 222 PC! ( SET RX 8 BITS X16 CLOCK )
  7   3 222 PC! C0 222 PC! ( 1 STOPBIT               )
  8   5 222 PC! 60 222 PC! ( SET TX 8 BITS           )
  9   B 222 PC! D4 222 PC! ( CLOCK OPTIONS           )
 10   C 222 PC! 1E 222 PC! ( BAUD RATE GEN LOW FOR 2400 )
 11   D 222 PC! 00 222 PC! ( BAUD RATE GEN HI FOR ALL   )
 12   E 222 PC! 01 222 PC! ( ENABLE BIT RATE GEN     )
 13   3 222 PC! C1 222 PC! ( ENABLE RX               )
 14   5 222 PC! 68 222 PC! ( ENABLE TX               ) ;
 15 DECIMAL -->
Screen # 101
  0 ( V21/V23 MODEM  CHANGE 8530 PARAMETERS             27/1/86 MBW )
  1 HEX
  2 : RX.ENABLE          3 222 PC!  C1 222 PC! ;
  3 : RX.DISABLE         3 222 PC!  C0 222 PC! ;
  4 : RTS.8530.ON        5 222 PC!  EA 222 PC! ;
  5 : RTS.8530.OFF       5 222 PC!  E8 222 PC! ;
  6 : 300BPS.8530        C 222 PC!  FE 222 PC! ;
  7 : 1200BPS.8530       C 222 PC!  3E 222 PC! ;
  8 : 2400BPS.8530       C 222 PC!  1E 222 PC! ;
  9 : DTR/RTS.8530.OFF   5 222 PC!  68 222 PC! ;
 10 : DTR.8530.ON        5 222 PC!  E8 222 PC! ;
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 102
  0 ( V21/V23 MODEM  DAA CONTROL  MASKS                  27/1/86 MBW )
  1 HEX
  2 : CCT       232  04 ;   (     -- FLAG )
  3 : OH        232  08 ;   (     -- FLAG )
  4 : RCCT.79   232  20 ;   ( FLAG   --  )
  5 : OH.79     232  40 ;   ( FLAG   --  )
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->

Screen # 103
  0 ( V21/V23 MODEM   R2424 BASIC MODEM SETUP            27/1/86 MBW )
  1 HEX
  2 : DEFAULT.2424
  3   INIT
  4   EN.M
  5   V.22/2400
  6   1 BUS.R NOW 1 BUS.T NOW
  7   1 DTR NOW
  8   1 RTS NOW
  9   1 AAE NOW
 10   0DB         ( NO ATTENUATION BEFORE DAA )
 11   DEFAULT.8530 ;
 12
 13
 14 DECIMAL
 15 -->

Screen # 104
  0 ( V21/V23 MODEM   8530 STATUS                        27/1/86 MBW )
  1 HEX
  2 : RXREADY?   BEGIN 222 PC@ 1 AND 1 = UNTIL ;
  3 : TXREADY?   BEGIN 222 PC@ 4 AND 4 = UNTIL ;
  4 : DCD.8530?  BEGIN 222 PC@ 08 AND 08 = UNTIL ;
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 105
  0 ( V21/V23 MODEM   PHONE NUMBER ENTERING              27/1/86 MBW )
  1 HEX
  2 0 VARIABLE PHONE.NUMBER 20 ALLOT
  3 : PHONE.NUMBER.PROMPT
  4   ." ENTER PHONE NUMBER "  ;
  5
  6 : READY.TO.DIAL?
  7   BEGIN DDRE IS UNTIL ;
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->

Screen # 106
  0 ( V21/V23 MODEM   DIALER                            27/1/86 MBW )
  1 HEX
  2 : DIAL  PHONE.NUMBER.PROMPT
  3   PHONE.NUMBER 20 EXPECT CR
  4       1 DTMF NOW 1 CRQ.T NOW ." DIALING # " 1 SEC  PHONE.NUMBER
  5   BEGIN DUP 1+ SWAP C@ DUP DUP 0=
  6   IF
  7     DROP DROP 1
  8                ELSE DUP 44 = IF
  9                                  2 SEC DROP DROP 0
 10                                       ELSE READY.TO.DIAL?
 11                                       0F AND 210 PC! EMIT 0
 12                                THEN
 13  THEN
 14  UNTIL DROP READY.TO.DIAL? FF 210 PC! -14DB  CLS ;
 15 DECIMAL -->

Screen # 107
  0 ( V21/V23 MODEM   7910 CONFIGURATION                27/1/86 MBW )
  1 HEX
  2 : V21.ANS.7910   230 PC@ E0 AND 05 OR 230 PC! ;
  3 : V21.ORG.7910   230 PC@ E0 AND 04 OR 230 PC! ;
  4 : V23.7910       230 PC@ E0 AND 06 OR 230 PC! ;
  5 : V23.EQU.7910   230 PC@ E0 AND 07 OR 230 PC! ;
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 108
  0 ( V21/V23 MODEM   7910 CONNECT V.21                  27/1/86 MBW )
  1 HEX
  2 : CONNECT.V21.ORG
  3   CLS ." V.21 300BPS MODE "  CR
  4   DEFAULT.2424
  5   V21.ORG.7910
  6   DIAL
  7   1 RCCT.79 NOW 1 OH.79 NOW EN.79
  8   0 CRQ.T NOW
  9   DTR.8530.ON
 10   DCD.8530? ." CARRIER DETECTED  . . . ON LINE "  CR CR
 11   RTS.8530.ON
 12   300BPS.8530 TALK     ;
 13
 14 DECIMAL
 15 -->

Screen # 109
  0 ( V21/V23 MODEM   7910 CONNECT V.23                  27/1/86 MBW )
  1 HEX
  2 : CONNECT.V23.ORG
  3   CLS ." V.23 1200BPS MODE "  CR
  4   DEFAULT.2424
  5   V23.7910
  6   DIAL
  7   1 RCCT.79 NOW 1 OH.79 NOW EN.79
  8   0 CRQ.T NOW
  9   DTR.8530.ON
 10   DCD.8530? ." CARRIER DETECTED  . . . ON LINE "  CR CR
 11   RTS.8530.ON   1200BPS.8530
 12   TALK     ;
 13
 14 DECIMAL
 15 -->

Screen # 110
  0 ( V21/V23 MODEM   2424 CONNECT V.22                  27/1/86 MBW )
  1 HEX
  2 : CONNECT.V22.ORG
  3   CLS ." V.22 1200BPS MODE "  CR
  4   DEFAULT.2424  V.22/1200 1200BPS.8530
  5   DIAL
  6   BEGIN CTS IS 1 = UNTIL  ." CARRIER DETECTED  . . . ON LINE "
  7   CR CR TALK     ;
  8 : CONNECT.V22.2400
  9   CLS ." V.22 2400BPS MODE "  CR
 10   DEFAULT.2424
 11   DIAL
 12   BEGIN CTS IS 1 = UNTIL  ." CARRIER DETECTED  . . . ON LINE "
 13   CR CR TALK     ;
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 111
  0 ( V21/V23 MODEM   V.22 ANSWER MODE CONNECTIONS     27/1/86 MBW )
  1 HEX
  2 : V22BIS.CONNECTION
  3   ." CONNECTED TO V.22 BIS MODEM AT 2400 BPS " CR CR
  4   TALK      ;
  5
  6 : V22.CONNECTION
  7   ." CONNECTED TO V.22 MODEM AT 1200 BPS "  CR CR
  8   1200BPS.8530
  9   TALK      ;
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 112
  0 ( V21/V23 MODEM  V.21/V.23 ANSWER MODE CONNECTIONS 27/1/86 MBW )
  1 HEX
  2 : V21.CONNECTION
  3   ." CONNECTED TO V.21 MODEM AT 300BPS " CR CR
  4   V21.ANS.7910
  5   1 RCCT.79 NOW 1 OH.79 NOW EN.79
  6   DTR.8530.ON RTS.8530.ON
  7   300BPS.8530
  8   TALK      ;
  9 : V23.CONNECTION
 10   ." CONNECTED TO V.23 MODEM AT 1200BPS "  CR CR
 11   V23.7910
 12   1 RCCT.79 NOW 1 OH.79 NOW EN.79
 13   DTR.8530.ON
 14   1200BPS.8530
 15   TALK      ;  DECIMAL -->
Screen # 113
  0 ( V21/V23 MODEM   AUTO ANSWER MODE  1 OF 2         27/1/86 MBW )
  1 HEX
  2 : AUTO.ANSWER
  3   DEFAULT.2424
  4   CLS ." UNIVERSAL ANSWER MODE " CR
  5       ." WAITING TO BE CALLED " CR
  6   BEGIN RI IS UNTIL
  7       ." RING DETECTED . . .  " CR
  8   BEGIN DSR  IS UNTIL
  9       ." DATA SET READY  ON   " CR
 10   1 SEC
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 114
  0 ( V21/V23 MODEM   AUTO ANSWER MODE  2 OF 2          27/1/86 MBW )
  1 HEX
  2   SPEED? DUP 3 = IF V22BIS.CONNECTION ELSE
  3          DUP 2 = IF V22.CONNECTION    ELSE
  4   THEN THEN DROP
  5   RLSD IS IF V23.CONNECTION ELSE V21.CONNECTION THEN ;
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->


Screen # 115
  0 ( V21/V23 MODEM   MENU SCREEN                         27/1/86 MBW )
  1 HEX
  2 : MENU INIT  BEGIN
  3   CLS  A 3  GOTOXY  ." ROCKWELL INTERNATIONAL'S    " CR
  4   CR   A SPACES     ." INTERNATIONAL MODEM ....    " CR
  5   CR CR A  SPACES   ." F1  V.21 ORIGINATE          " CR
  6         A  SPACES   ." F2  V.22 ORIGINATE 1200     " CR
  7         A  SPACES   ." F3  V.22 ORIGINATE 2400     " CR
  8         A  SPACES   ." F4  V.23 ORIGINATE          " CR
  9         A  SPACES   ." F5  AUTO ANSWER/CONFIGURE   " CR
 10 PCKEY DROP DUP 3B = IF CONNECT.V21.ORG  ELSE
 11            DUP 3C = IF CONNECT.V22.ORG  ELSE
 12            DUP 3D = IF CONNECT.V22.2400 ELSE
 13            DUP 3E = IF CONNECT.V23.ORG  ELSE
 14            DUP 3F = IF AUTO.ANSWER
 15 THEN THEN THEN THEN THEN SWAP DROP UNTIL ; MENU DECIMAL -->


Screen # 116
  0
  1
  2
  3
  4
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15
```

Figure 14. International Modem FORTH Screens (Continued)

Rockwell

Quality of Received Data for Signal Processor-Based Modems

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INTRODUCTION

This application note provides the modem design engineer with detailed information on the generation and interpretation of diagnostic data featured in Rockwell's signal processor (SP)-based modems.

Rockwell's plug-compatible SP-based modems can generate a variety of diagnostic data. This data is extremely useful in the evaluation of modem performance and line conditions. A microprocessor interface can readily access diagnostic data and other useful signals via the SP interface memory.

The diagnostic capabilities of specific Rockwell modems are summarized in Table 1.

ACCESSING DIAGNOSTIC DATA

Diagnostic data can be readily accessed via the microprocessor interface. The host processor must store the access code corresponding to the desired data in the RAM access register (See Table 2). The signal processor then stores the desired data in diagnostic data registers. The data available flag (R48DP, R96DP, R96FT and R96FAX only) in the respective interface memory sets when the signal processor writes data into diagnostic register zero and resets when the host reads data from register zero and is used to handshake with the diagnostic data registers. Diagnostic data is generated in 16-bit double precision form, although for most applications only the most significant byte of data is necessary. The RAM access codes for the SP-based modems are shown in Table 2. Functional block diagrams that relate the RAM access codes to specific functions are shown in Figures 1 through 4. Refer to the applicable modem data sheet for specific details regarding an individual modem.

EYE PATTERN

A quadrature eye pattern is an extremely useful diagnostic tool. The visual display of an eye pattern can be monitored to identify common line disturbances, as well as defects in the modulation/demodulation processes.

The ideal eye patterns or signal constellations for the various encoding methods are illustrated in Figures 5 through 10. By performing digital-to-analog (D/A) conversion of the received signal point data (refer Table 2, Node 9), an eye pattern can be displayed on an oscilloscope. Two methods of eye pattern generation are available:

1. The microprocessor can read the received signal points and then write this data into two memory mapped D/A converters. Figure 11 shows a typical microprocessor interface eye pattern generator. A typical parallel eye pattern algorithm is shown in Figure 12.
2. High speed modems (4800 bps and above) can generate diagnostic data serially through hardware pins in the modem connector.

4

Table 1. Summary of Diagnostic Capabilities for SP-Based Modems

Modem	Eye Pattern		EQM Value	Error Vector	Phase Error	Access to SP RAM Space[2]
	Serial	Parallel MPU Bus				
R1212M		X	1	X	X	X
R1212DC		X	1	X	X	X
R2424M		X	1	X	X	X
R2424DC		X	1	X	X	X
R48DP	X	X	X	X		X
R96DP	X	X	X	X		X
R96FT	X	X	X	X		X
R96FAX	X	X	X	X		X

Notes:
1. EQM may be computed by the host processor from the error vector data.
2. See RAM access codes (Table 2) and block diagrams (Figures 1–4).

Table 2. RAM Access Codes

Node No.	Function	R1212M/DC R2424M/DC			R48DP/R96DP				R96FT				R96FAX		
		Access Codes	Chip No.	Reg. No.	RAM Access X	RAM Access Y	Chip No.	Reg. No.	RAM Access X	RAM Access Y	Chip No.	Reg. No.	RAM Access	Chip No.	Reg. No.
1	Received Signal Samples (and Output)				C0	—	1	2,3	DC	—	1	2,3	C0	0	2,3
2	Demodulator Output	56	0	2,3,4,5	C2	42	1	0,1,2,3	C0	40	1	0,1,2,3	42	0	0,1,2,3
3	Low Pass Filter Output	40	0	2,3,4,5	D4	54	1	0,1,2,3	DD	5D	1	0,1,2,3	54	0	0,1,2,3
4	Average Energy				—	04	1	0,1	—	32	1	0,1	DC	0	2,3
5	AGC Gain Word				81	—	1	2,3		2E	1	2,3	81	0	2,3
6	Equalizer Input				C0	40	2	0,1,2,3	C0	40	2	0,1,2,3	40	1	0,1,2,3
7	Equalizer Taps	01-0D	0	2,3,4,5	81-A0	01-20	2	0,1,2,3	81-A0	01-20	2	0,1,2,3	01-20	1	0,1,2,3
8	Unrotated Equalizer Output				E1	61	2	0,1,2,3	E1	61	2	0,1,2,3	61	1	0,1,2,3
9	Rotated Equalizer Output (Received Point Eye Pattern)	11	0	2,3,4,5	A2	22	2	0,1,2,3	E2	62	2	0,1,2,3	22	1	0,1,2,3
10	Decision Points (Ideal Eye Pattern Points)	51	0	2,3,4,5	E2	62	2	0,1,2,3	E8	68	2	0,1,2,3	62	1	0,1,2,3
11	Error Vector (Rotated Error)	52	0	2,3,4,5	E3	63	2	0,1,2,3	E5	65	2	0,1,2,3	63	1	0,1,2,3
12	Rotation Angle	12	0	4,5	—	00	2	0,1	A7	—	2	2,3	00	1	0,1
13	Frequency Correction				AA	—	2	2,3					A8	1	2,3
14	EQM	*			A7	—	2	2,3	AC	—	2	2,3	AB	1	2,3
15	Dual Point				AE	2E	2	0,1,2,3					—		
16	Group II Baseband Signal												C8	1	2,3
17	Group II AGC Gain Word												AD	1	2,3
18	Group II AGC Slew Rate												AA	1	2,3
19	Group II PLL Frequency Correction												C2	1	2,3
20	Group II PLL Slew Rate												F0	1	2,3
21	Group II Black/White Level												2A	1	0,1
22	Self Test Error Counter	00	0	2,3,4,5											
23	Phase Error	10	0	2,3											
24	Input Signal to Equalizer Taps	41-4D	0	2,3,4,5											
25	Equalizer Output	53	0	2,3,4,5											

Note: * EQM value may be computed by the host processor from error vector data, node 11.

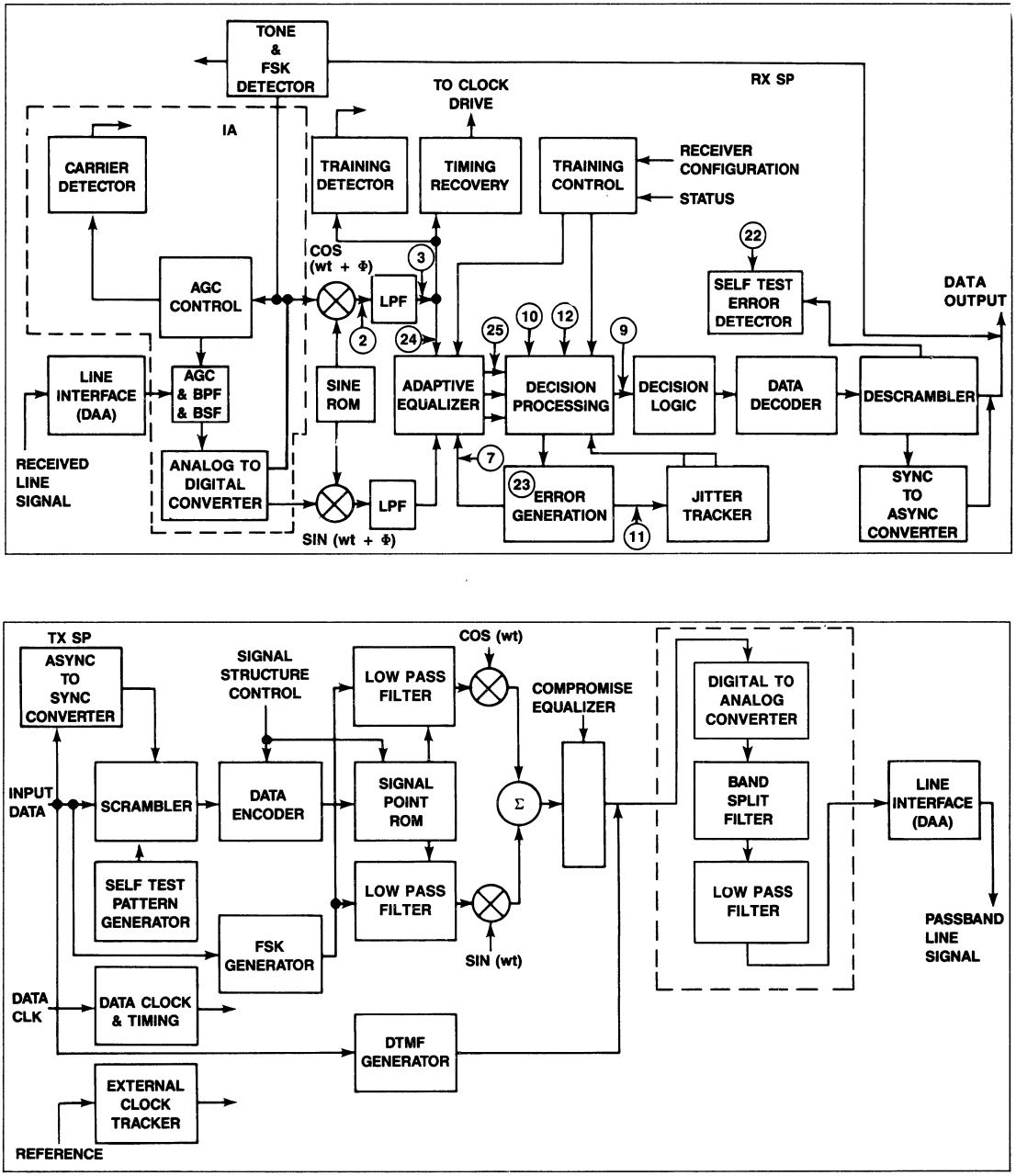


Figure 1. R1212/R2424 Processing Flow Diagram

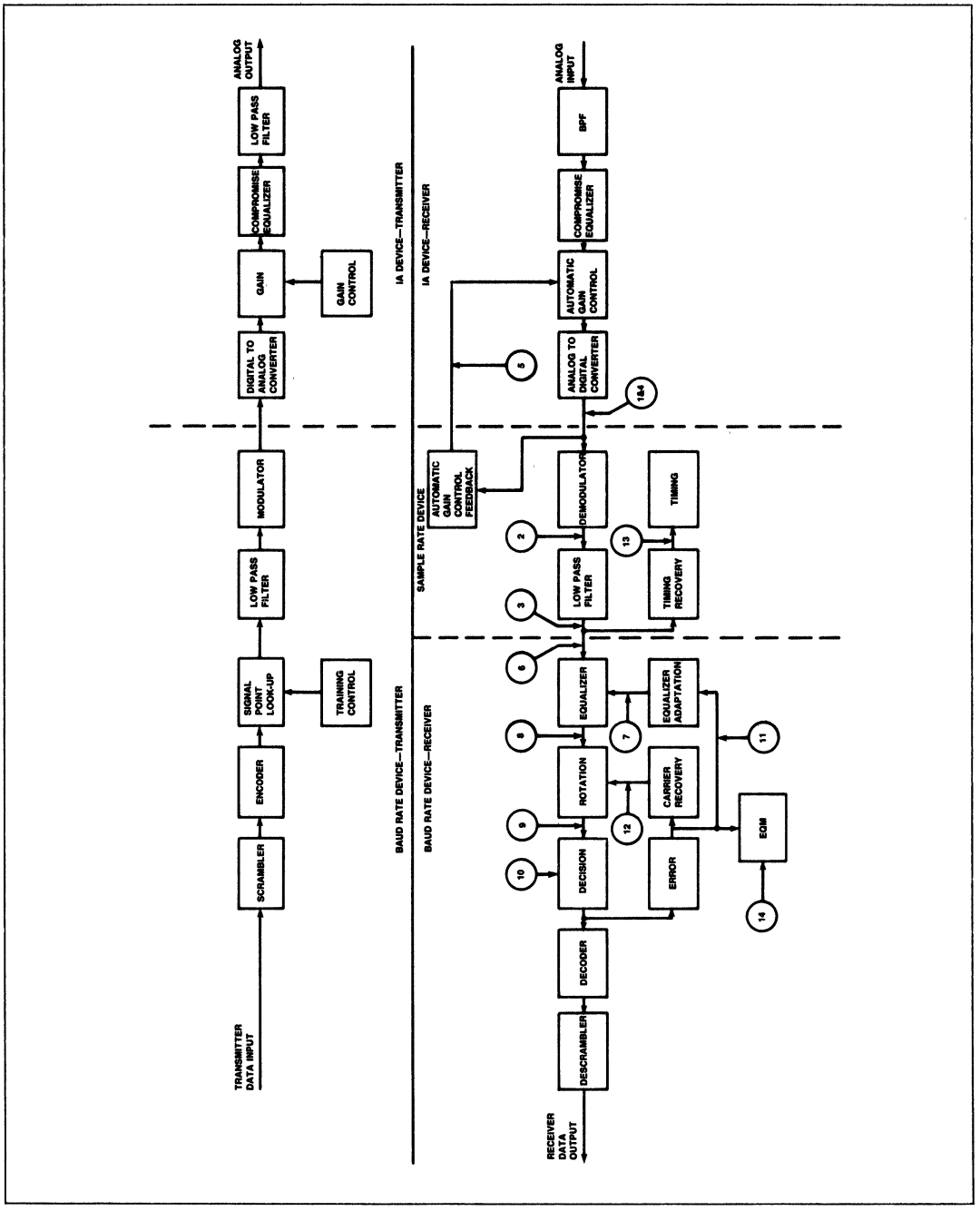


Figure 2. R48DP/R96DP/R96FT/R96FAX (Group 3) Processing Flow Diagram

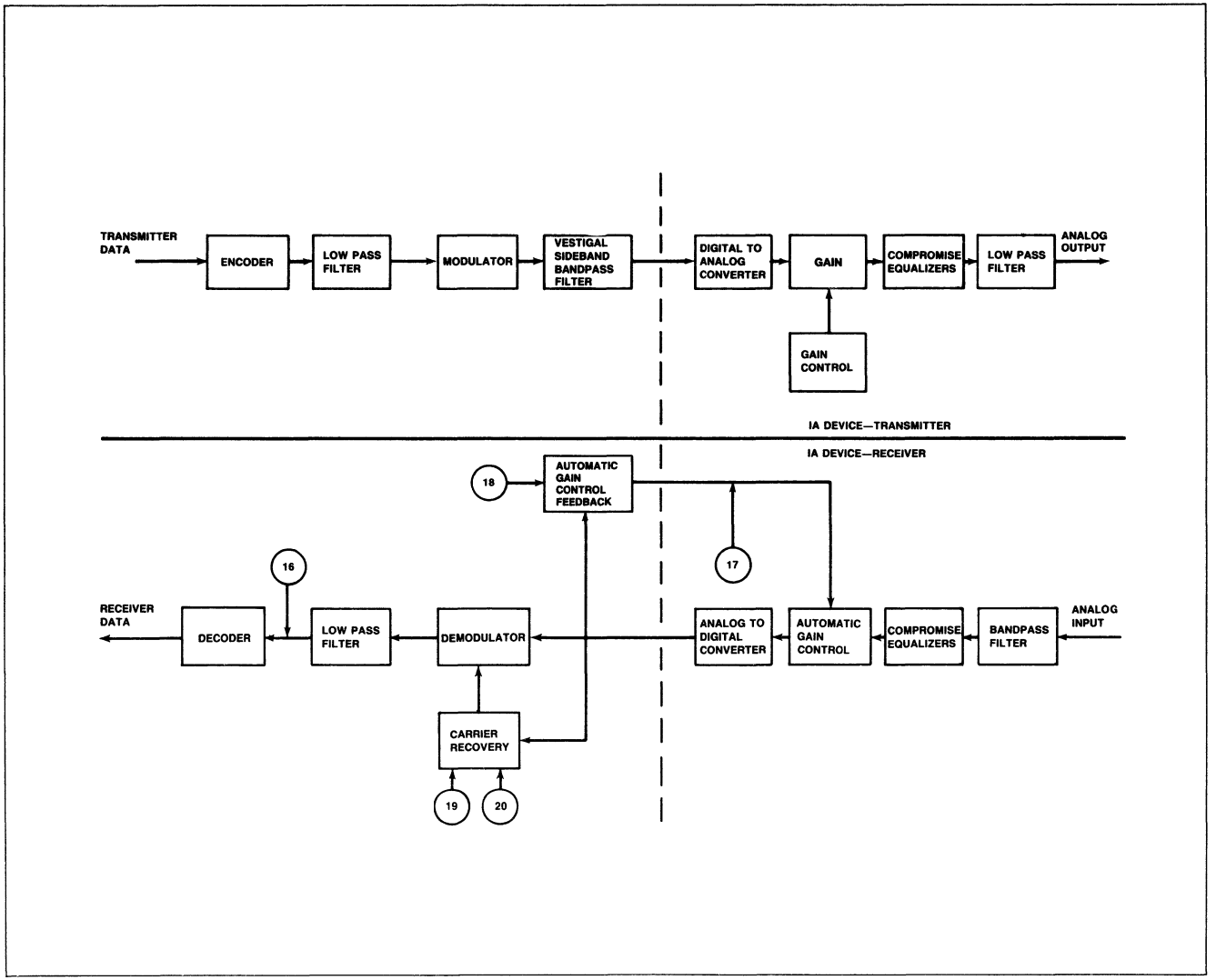


Figure 3. R96FAX (Group 2) Processing Flow Diagram

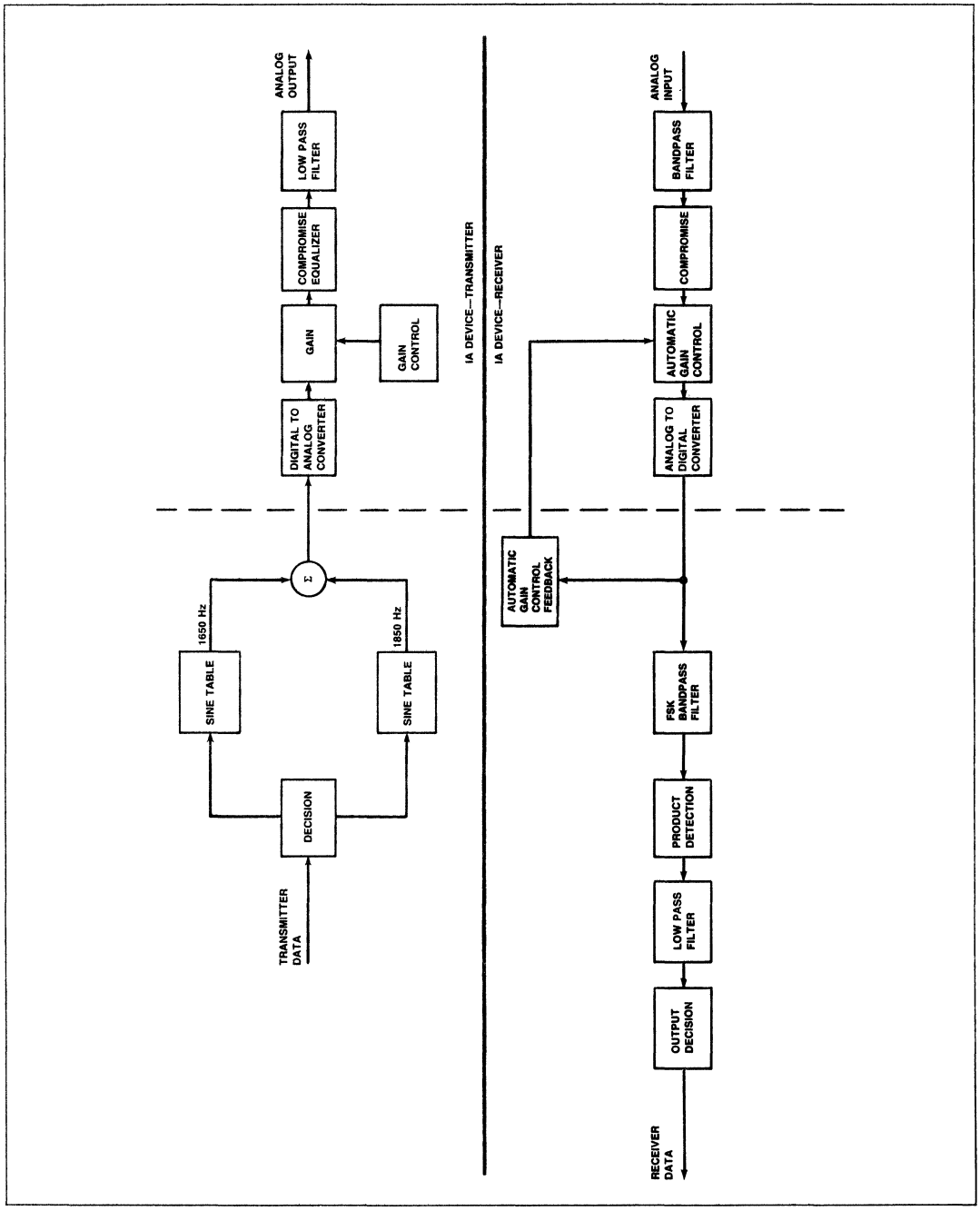
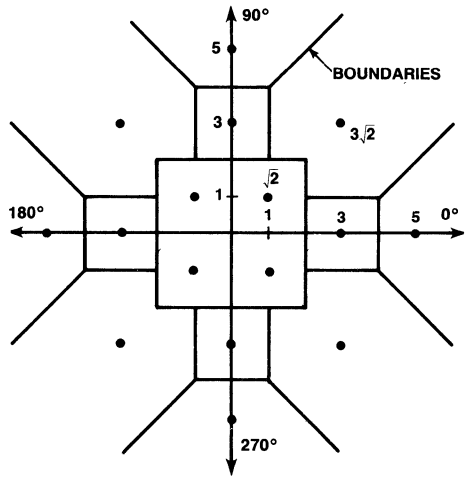
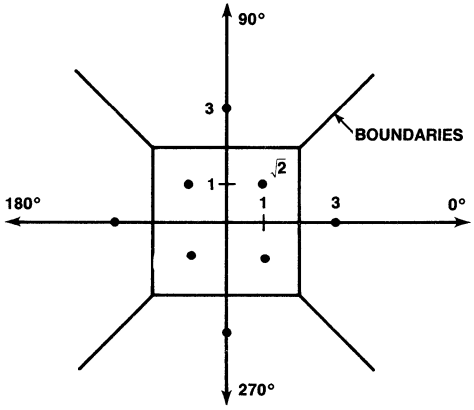


Figure 4. R96FAX FSK Processing Flow Diagram



Q2	Q3	Q4	PHASE CHANGE	ABSOLUTE PHASE	Q1	RELATIVE AMPLITUDE
0	0	1	0°	0°, 90°, 180°, 270°	0	3
0	0	0	45°			
0	1	0	90°		1	5
0	1	1	135°			
1	1	1	180°	45°, 135°, 225°, 315°	0	√2
1	1	0	225°			
1	0	0	270°		1	3√2
1	0	1	315°			

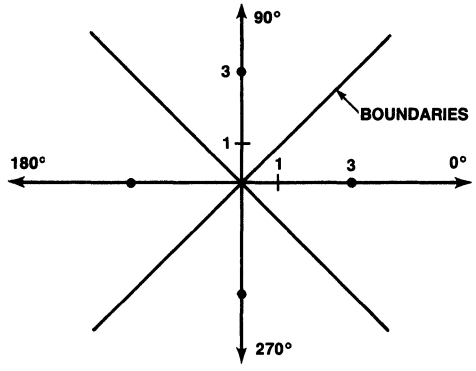
Figure 5. Ideal Eye Pattern—V.29/9600 bps



TRIBIT ENCODING:

IN V.29/7200 BPS FALLBACK MODE, DATA IS ENCODED IN GROUPS OF 3 BITS OR TRIBITS. THE ENCODING IS AS FOR V.29/9600 BPS ABOVE EXCEPT THAT: THE FIRST DATA BIT IN TIME DETERMINES Q2 OF THE MODULATOR QUADBIT. THE SECOND AND THIRD BITS IN TIME DETERMINE Q3 AND Q4, RESPECTIVELY. Q1 = 0 FOR ALL EIGHT SIGNAL ELEMENTS.

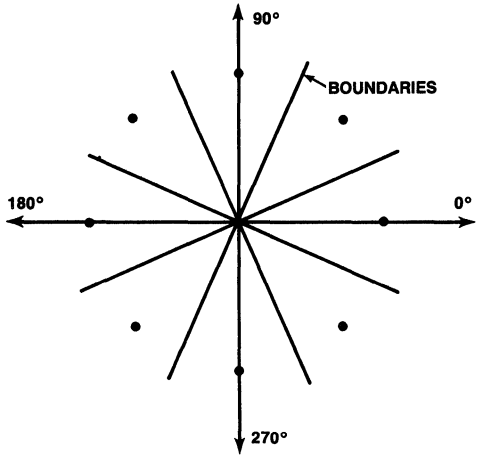
Figure 6. Ideal Eye Pattern—V.29/7200 bps



DIBIT ENCODING:

DATA BITS	PHASE CHANGE	RELATIVE AMPLITUDE
00	0°	CONSTANT
01	90°	
11	180°	
10	270°	

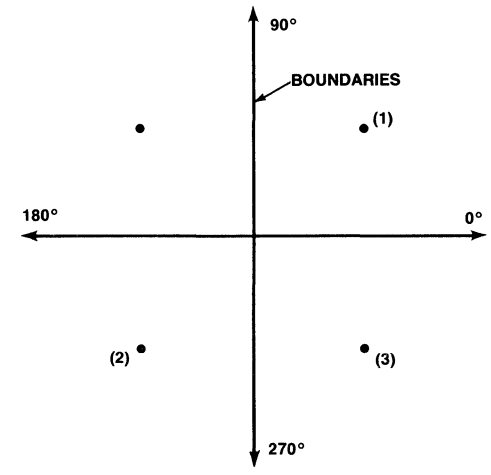
Figure 7. Ideal Eye Pattern—V.29/4800 bps and V.27/BIS/TER/2400 bps



TRIBIT ENCODING:

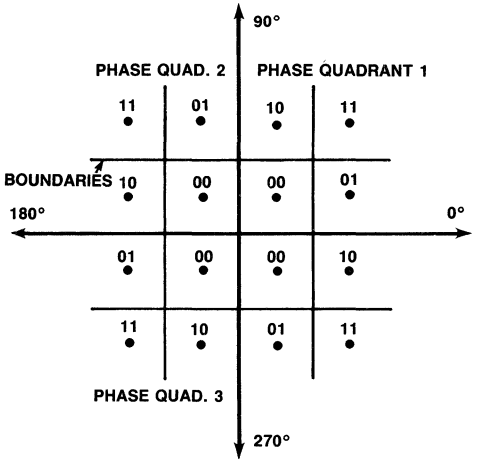
TRIBIT VALUE	PHASE CHANGE	RELATIVE AMPLITUDE
0 0 1	0°	CONSTANT
0 0 0	45°	
0 1 0	90°	
0 1 1	135°	
1 1 1	180°	
1 1 0	225°	
1 0 0	270°	
1 0 1	315°	

Figure 8. V.27 BIS/TER/4800 bps



DIBIT VALUES (1200)	BIT VALUES (600 BPS)	PHASE CHANGE
00	0	+90°
01	—	0°
11	1	+270°
10	—	+180°

Figure 9. V.22 A/B 1200 bps/600 bps



DATA IS ENCODED IN QUADBITS. THE FIRST TWO BITS OR DIBIT SELECT ONE OF FOUR QUADRANTS. THE SECOND DIBIT SELECTS ONE OF FOUR POINTS IN THAT QUADRANT, AS SHOWN BELOW.

FIRST TWO BITS IN QUADBIT [2400 BIT(S)] OR DIBIT VALUES [1200 BIT(S)]	PHASE QUADRANT CHANGE	
00	1 → 2 2 → 3 3 → 4 4 → 1	90°
01	1 → 1 2 → 2 3 → 3 4 → 4	0°
11	1 → 4 2 → 1 3 → 2 4 → 3	270°
100	1 → 3 2 → 4 3 → 1 4 → 2	180°

Figure 10. V.22 BIS/4800 bps

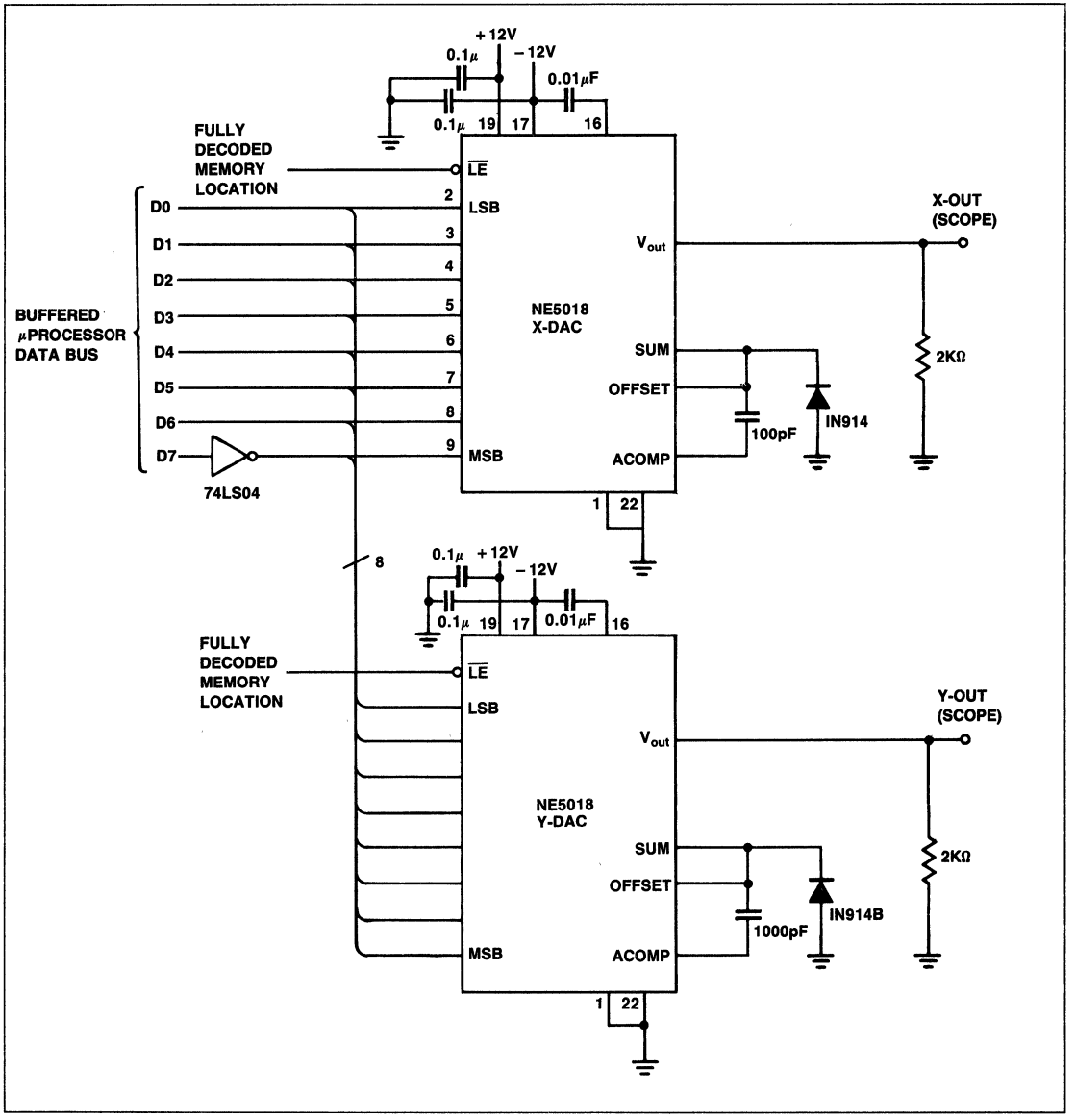


Figure 11. Typical Microprocessor Bus Eye Pattern Generator

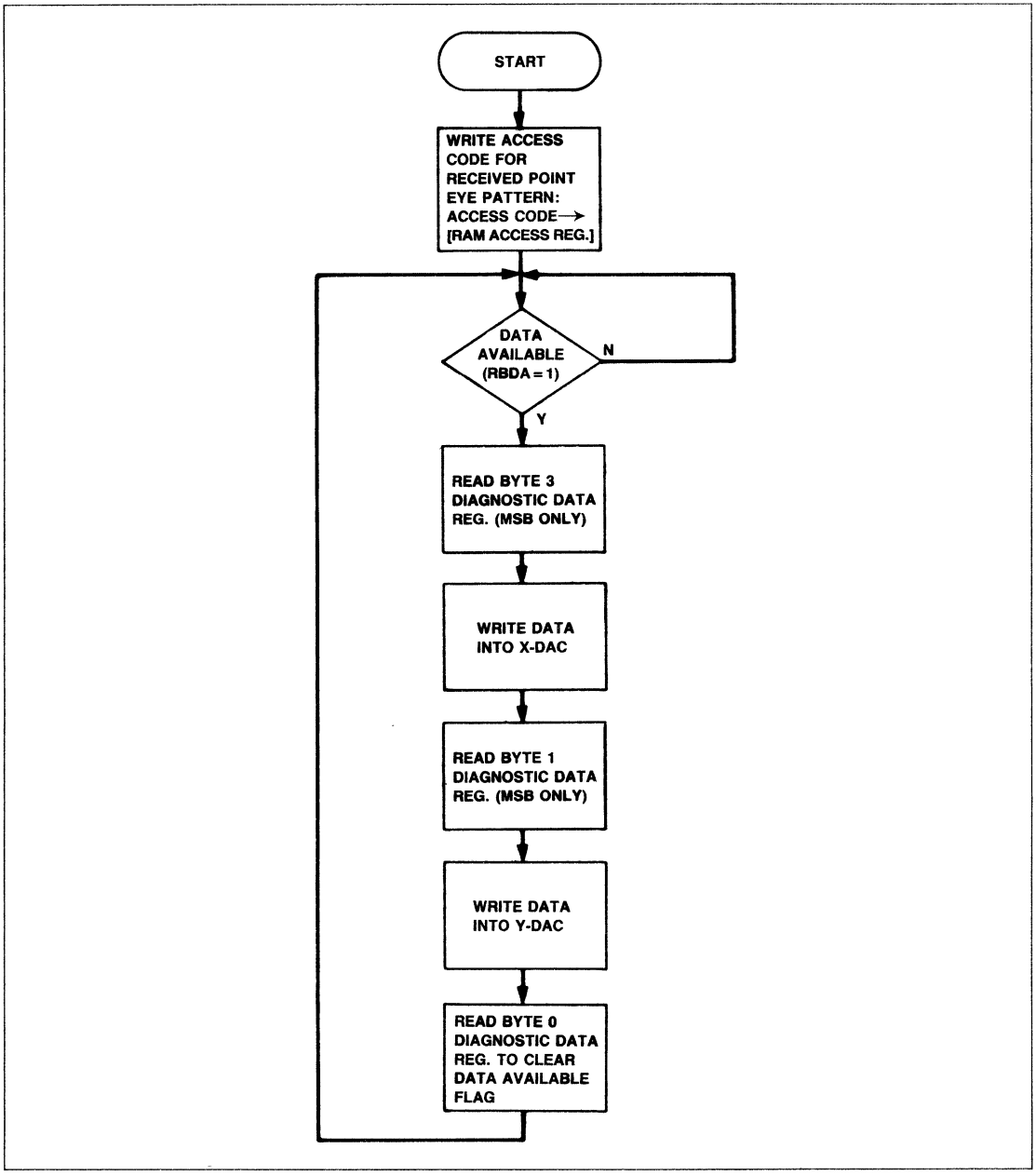


Figure 12. Typical Microprocessor Eye Pattern Generation Loop (R96DP/R48DP)

The hardware necessary to generate a serial eye pattern along with the relevant timing signals are shown in Figures 13 and 14.

The eye pattern consists of dots or received signal points. Each point represents the location of a received signal element in the

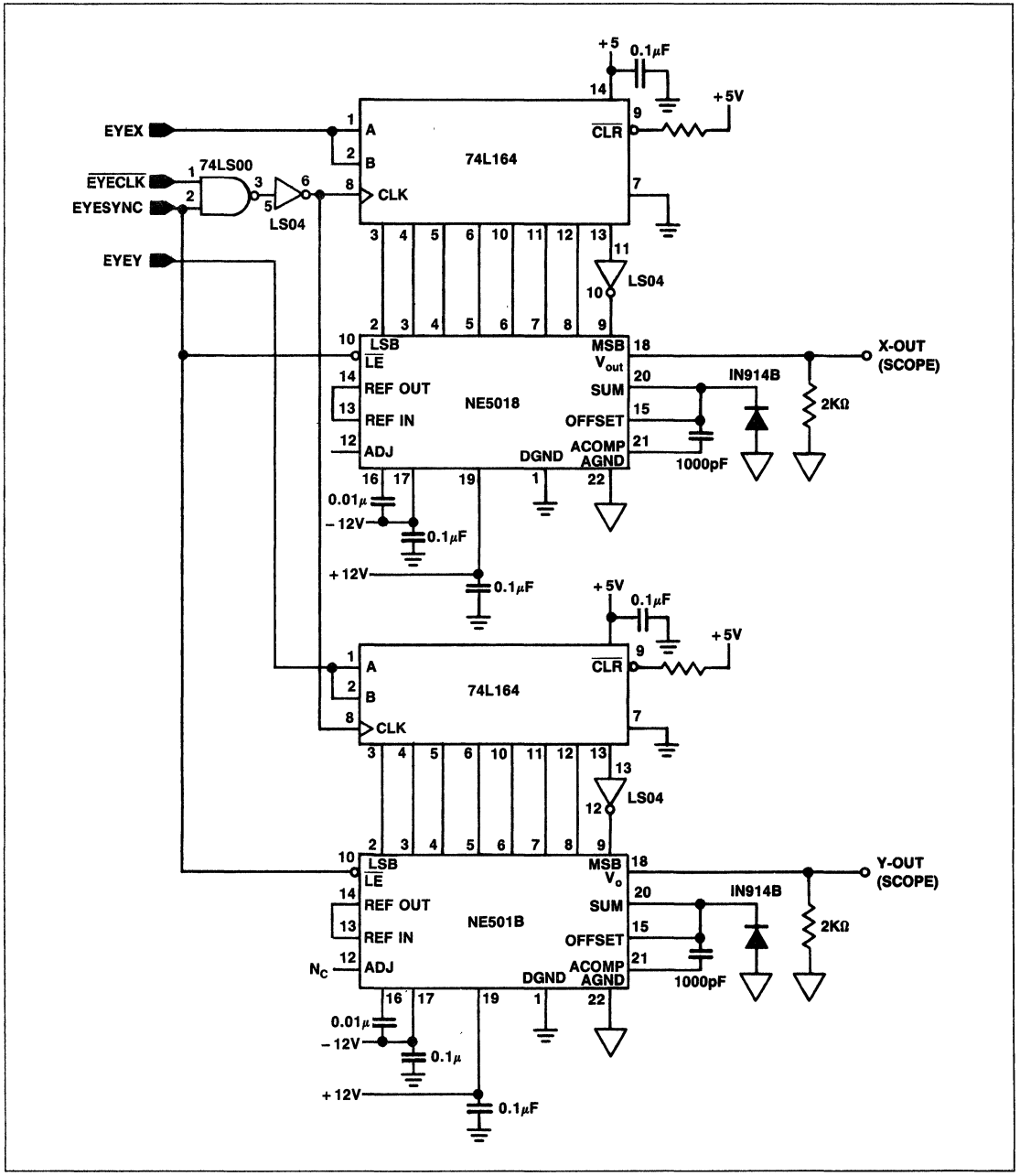


Figure 13: Serial Eye Pattern Generator

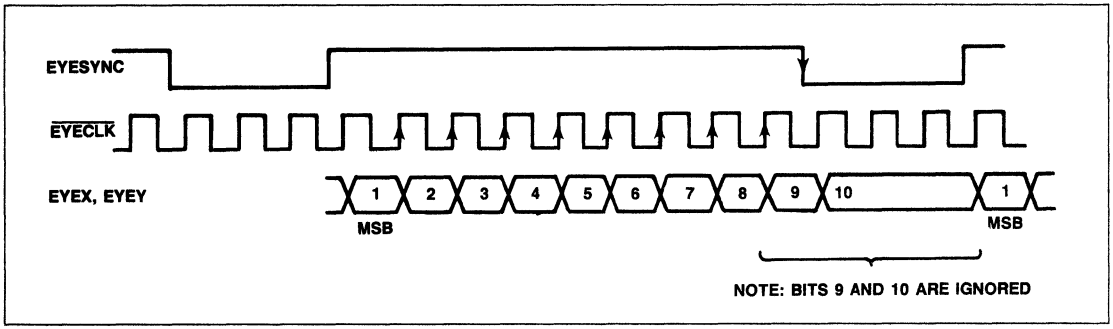


Figure 14. Serial Eye Pattern Signal Timing

baseband signal plane. In polar coordinates each point represents a magnitude and differential phase shift. Eye pattern data is updated at the baud rate so the oscilloscope display appears to be a continuous signal constellation.

For a DPSK (Differential Phase Shift Keyed) modem, the phase shift from one signal element to the next is decoded to recover data. For a QAM (Quadrature Amplitude Modulation) modem, both amplitude and differential phase shift are decoded to recover data.

Assume a V.22/1200 bps configuration (R1212 modem), and that initially a dot is displayed at point 1 of Figure 9. If the first dibit received is 10, the point displayed will be point 2, corresponding to a 180° shift in phase. If the second dibit is a 00 (90°), point 3 will be displayed. In this fashion a continuous stream of random data produces the display of Figure 9.

TYPICAL LINE DISTURBANCES

Actual received signal points are distorted by one or more types of line disturbances such as noise, phase or amplitude hits, phase or amplitude jitter, harmonic distortion and drop-outs.

White noise produces a smearing of each signal constellation point around its ideal location (see Figure 15A).

Phase jitter produces periodic phase smearing with little or no amplitude effect (see Figure 15B).

Harmonic distortion produces a non-periodic amplitude smearing with little phase effect (see Figure 15C).

Amplitude jitter produces an effect similar to harmonic distortion, but in this case the disturbance is periodic.

An amplitude (or phase) hit is associated with an instantaneous high error in the amplitude (or phase) signal component.

The degree of smearing in the eye pattern is proportional to the severity of the particular disturbance. These disturbances may occur in combination producing more complex smearing of the eye pattern.

A point falling within the signal space delimited by boundaries is decoded by the modem as if it were located at the ideal point within that space. When a line disturbance causes the signal point to cross a decision boundary, the received signal point is incorrectly decoded.

ERROR VECTOR AND EQM VALUES

Transient phenomena are difficult to observe in a quadrature eye pattern. Also, the proper interpretation of the eye pattern is a function of the observer's training and requires constant attention. Rockwell's signal processor modems generate error vector and Eye Quality Monitor (EQM) data that are more suitable for microprocessor manipulation and interpretation.

The error vector is defined as the angle and magnitude difference between an actual received signal point and its ideal location in the baseband signal plane (refer to Figure 16). Error vectors are represented as complex numbers whose real and imaginary components may be read out of the modem's diagnostic registers once per baud. An EQM value may be obtained by processing the error vector data to obtain a positive hexadecimal value whose magnitude is an indicator of the quality of the received signal or probability of error of received signal points. In the case of high speed modems (R48DP, R96DP, R96FT, and R96FAX), the error vector is processed by the SP devices and the EQM value is available through the diagnostic data registers. For medium speed modems (R1212 and R2424), the EQM value may be computed by the host processor using the error vector data. An algorithm for computing EQM values is given below.

It is desirable to have a quantity whose magnitude is proportional to the time average of the error vector magnitude. The error vector magnitude may be approximated by its squared magnitude eliminating the computation of a square root:

$$\text{Re (ERROR)}^2 + \text{Im (ERROR)}^2 \qquad \text{(Eq. 1)}$$

The squared magnitude may then be averaged by a digital filter of transfer function (see Figure 17):

$$H(Z) = \frac{\alpha}{1 - \beta Z^{-1}} \qquad \text{(Eq. 2)}$$

The coefficients α and β may be computed by a Z-domain approximation to an RC network of transfer function (see Figure 18):

$$H(s) = \frac{1}{1 + S\tau}, \tau = RC \qquad \text{(Eq. 3)}$$

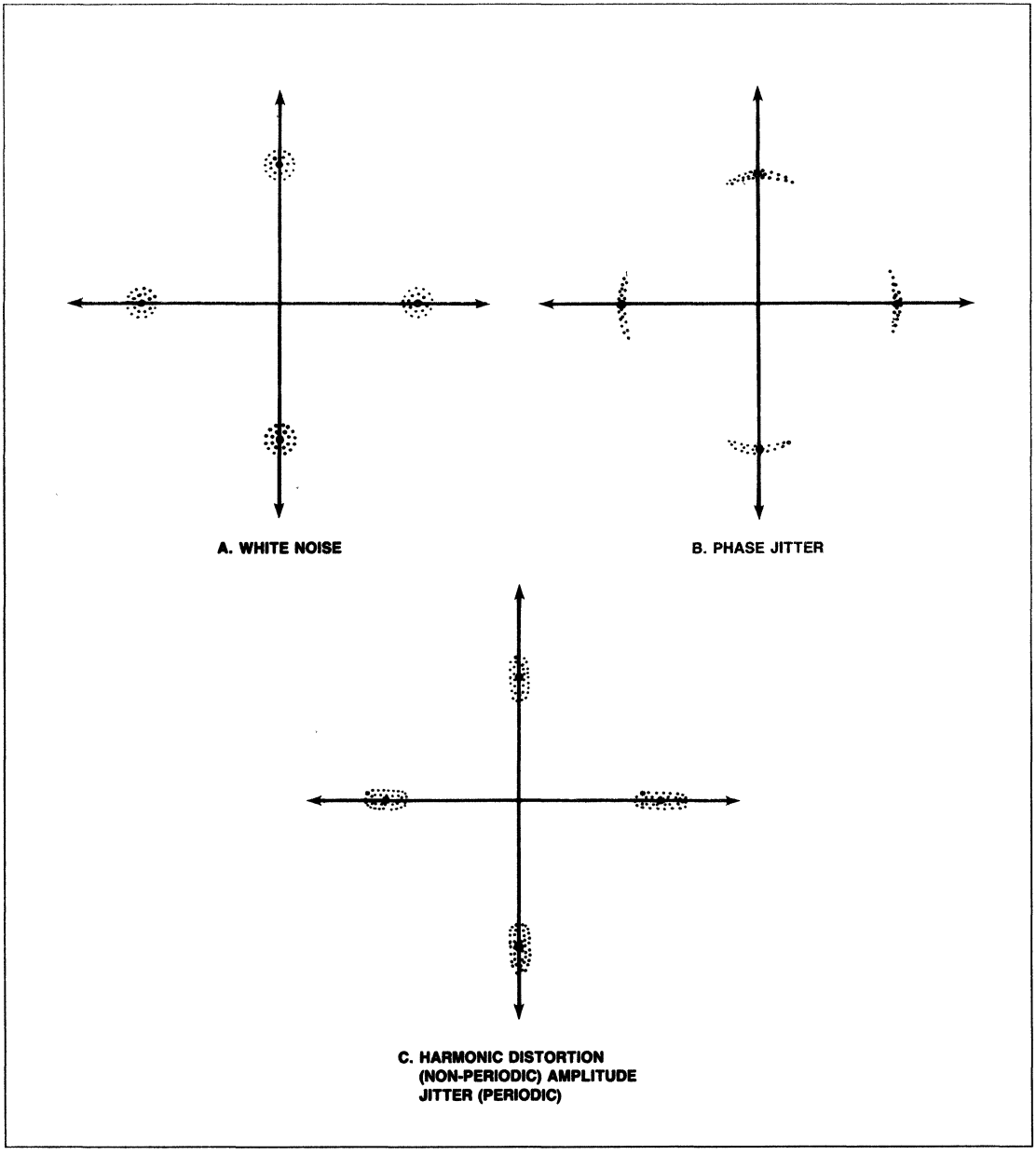


Figure 15. Typical Line Disturbances

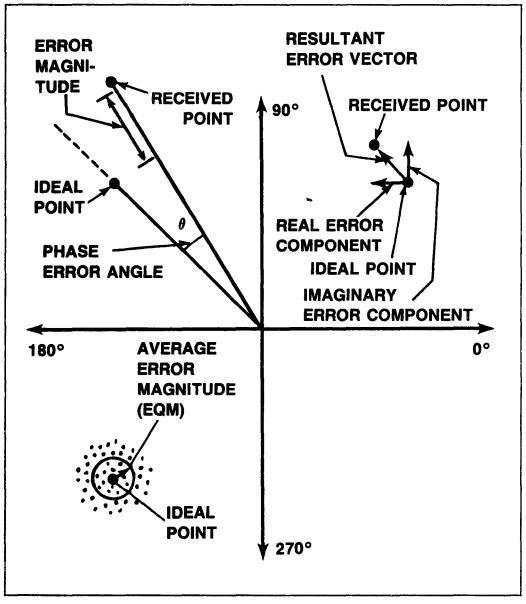


Figure 16. Error Vector Phase Error/EQM

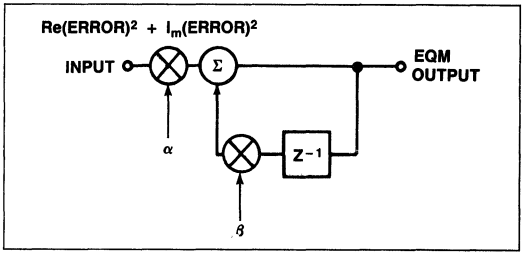


Figure 17. Digital Energy Averaging Filter

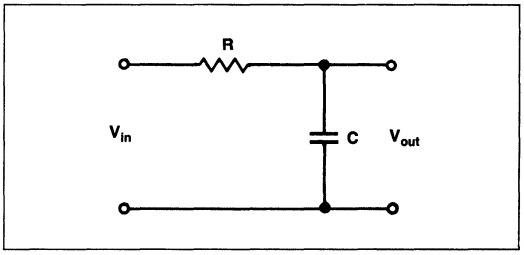


Figure 18. Equivalent Analog RC-Network

Substituting variables (first backward difference approximation) $S = 1 - Z^{-1}/T$ yields α and β (τ = RC, T = sampling period 1/T = 7200 Hz for R1212/R2424):

$$\alpha = \frac{1}{1 + \tau/T} = \frac{1}{1 + 7200\tau} \qquad \text{(Eq. 4)}$$

$$\beta = \frac{\tau/T}{1 + \tau/T} = \frac{1}{1 + \frac{1}{7200\tau}} \qquad \text{(Eq. 5)}$$

Re-writing the transfer function H(Z) (Equation 1) as a difference equation:

$$y(n) = \alpha u(n) + \beta y(n-1) \qquad \text{(Eq. 6)}$$

Letting the input sequence $u(n) = Re\,(ERROR\ (n))^2 + Im\,(ERROR\ (n))^2$ and the output $y(n) = EQM(n)$ we obtain:

$$EQM(n) = \alpha\left[Re(ERROR(n))^2 + Im(ERROR(n))^2\right] + \beta EQM(n-1) \qquad \text{(Eq. 7)}$$

where: EQM(n) = Current EQM value.
EQM(n − 1) = EQM value delayed by one sample period.
Re (ERROR (n)) = Real component of the error vector.
Re (ERROR (n)) = Imaginary component of the error vector.

If we choose τ = 0.1 seconds and 1/T = 7200 Hz then, α = 0.001386962 and β = 0.998613037. Note that $\alpha + \beta = 1$ and $\alpha \ll \beta < 1$.

The EQM value is the filtered squared magnitude of the error vector. These values represent the probability of error and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of CCITT recommendation V.24 or circuit CG of RS-232-C recommendation) by comparing the EQM value against an experimentally obtained criteria (refer to Figures 19 and 20).

Bit Error Rate (BER) curves as a function of the signal-to-noise ratio (SNR) are used to establish a criteria for determining the acceptance of EQM values. Figure 20 is a typical BER curve showing the meaning of a given EQM value in terms of BER and SNR. From an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the modem to fall-back to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbance present on the line and with the various configurations. A given magnitude of EQM in V.29/9600 does not represent the same BER as in V.29/4800. The former configuration has 16 signal points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given level of noise or jitter. Also, the type of disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Recalling that EQM is an average of the squared magnitude of the error vector, it can be seen that the correspondence of EQM to SNR (and hence BER) is dependent upon the signal structure of the modulation being used and the type of line disturbance present.

4

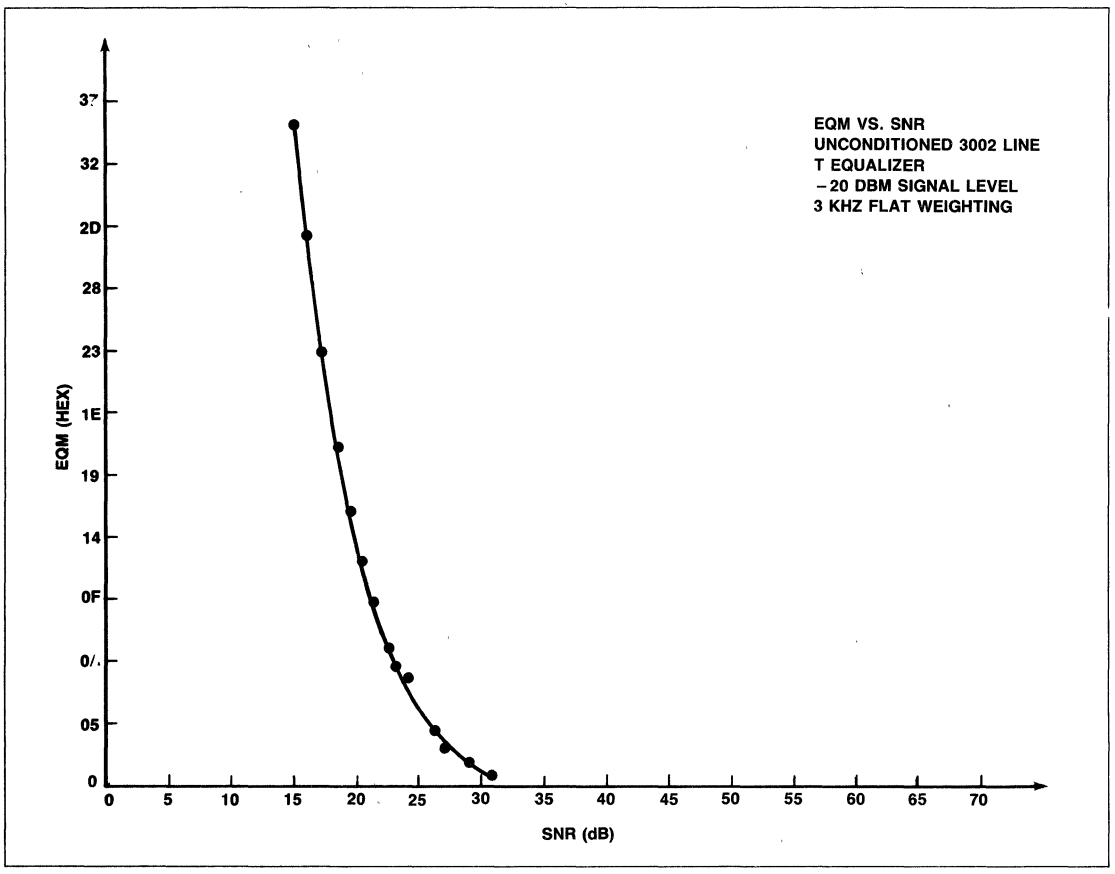


Figure 19. Typical Eye-Quality Versus Signal-To-Noise Ratio for V.29/9600 (R96FAX)

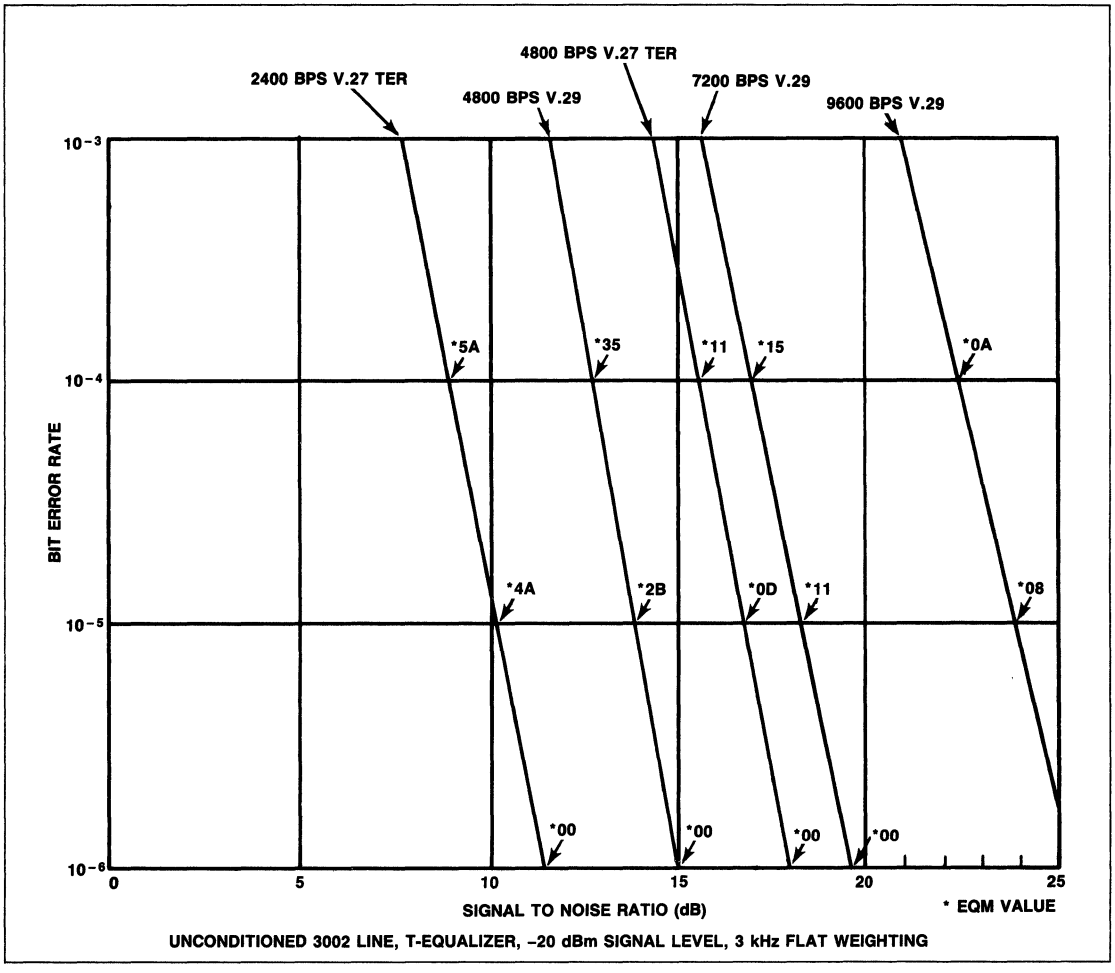


Figure 20. Typical Bit Error Rate Versus SNR and EQM

SCALING OF SP SIGNALS (R48DP, R96DP, R96FT, AND R96FAX)

The following list of formulas can be used to obtain diagnostic data in engineering units. Typical values or ranges for the data are also given.

CONVERSION FORMULAS, RANGES AND TYPICAL VALUES FOR R48DP, R96DP AND R96FAX MODEMS

1. **AGC Gain Word (16 bits unsigned)—Node 5**

   Range:
   $0F00_{16}$ – $7FFF_{16}$ for LRTH = 0 (–43 dBm Threshold)
   0640_{16} – $7FFF_{16}$ for LRTH = 1 (–47 dBm Threshold)

$$\text{AGC Gain in dB} = 50 - \frac{\text{AGC Gain Word}}{(100)_8} \times 0.097 \text{ dB}$$

2. **Average Power Word (16 bits)—Node 4**

   Typical value: $4211_8 = 0889_{16}$ (corresponding to 0 dBm)

$$\text{Post-AGC Average Power in dBm} = 10 \text{ Log} \left(\frac{\text{Average Power Word}}{(889)_{16}} \right) \text{dBm}$$

$$\text{Pre-AGC Average Power in dBm} = \text{(Post AGC Avg. Power in dBm – AGC gain in dB) dBm}$$

3. **A/D Sample Word (16 bits two's complement)—Node 1**

   (Refer to Figure 21 for the location of V_{INT} and V_{EXT} signals)

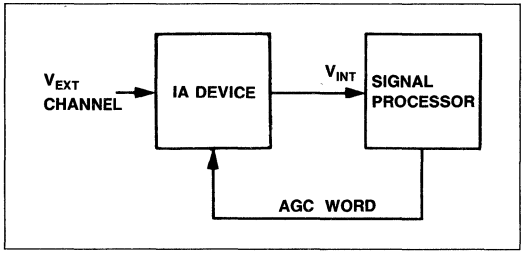


Figure 21. External and Internal Voltages

$$V_{INT} = \frac{\text{Signed, two's complement 16-bit A/D Word}}{(100)_8} \times \frac{3}{256} \text{Volts}$$

$$V_{EXT} = V_{INT} \div LOG_{10}^{-1} \left[\frac{\text{AGC Gain (dB)}}{20}\right]$$

4. **Rotation Angle Word (16 bits two's complement)—Node 12**

   Range: $-180° — +180°$

   Rotation Angle in degrees $= \frac{\text{Rot. Angle Word}}{2^{16}} \times 180°$

5. **Frequency Correction Word (16 bits two's complement)—Node 13** (Deviation from carrier in Hz)

   Range: $FC01_{16} - 0400_{16}$ (± 37.5Hz)

   Freq. Correction in Hz $= \left(\frac{\text{Freq. Correction word}}{2^{16}}\right)$ × (Baud Rate in Hz) Hz

6. **Error Vector Real (16 bits two's complement) and Imaginary (16 bits two's complement) Words**

   (Refer to Table 3.)

7. **Scaled Signal Points (16 bits two's complement) (V.29 to V.27)**

   (Refer to Figure 22 and Table 4.)

Table 3. Error Vector Maximum Values

Configuration	Bit Rate (BPS)	Real Error	Imag. Error	Magnitude $\sqrt{Re^2 + Im^2}$
V.29	9600	$<C00_{16}$	$<C00_{16}$	$<E66_{16}$
V.29	7200	$<2400_{16}$	$<2400_{16}$	$<1AD4_{16}$
V.29	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	2400	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$

Table 4. R48DP/R96DP/R96FAX Scaled Signal Points (Hex)

Point	Modem			
	V.29/9600 x , y	V.29/7200 x , y	V.29/4800 & V.27/2400 x , y	V.27/4800 x , y
1	0000, 2800	0000, 2400	0000, 1F00	0000, 1F00
2	2800, 0000	2400, 0000	1F00, 0000	1600, 1600
3	0000, D800	0000, DC00	0000, E100	1F00, 0000
4	D800, 0000	DC00, 0000	E100, 0000	1600, EA00
5	0000, 1800	0C00, 0C00		0000, E100
6	1800, 1800	0C00, F400		EA00, EA00
7	1800, 0000	F400, F400		E100, 0000
8	1800, E800	F400, 0C00		EA00, 1600
9	0000, E800			
10	E800, E800			
11	E800, 0000			
12	E800, 1800			
13	0800, 0800			
14	0800, F800			
15	F800, F800			
16	F800, 0800			

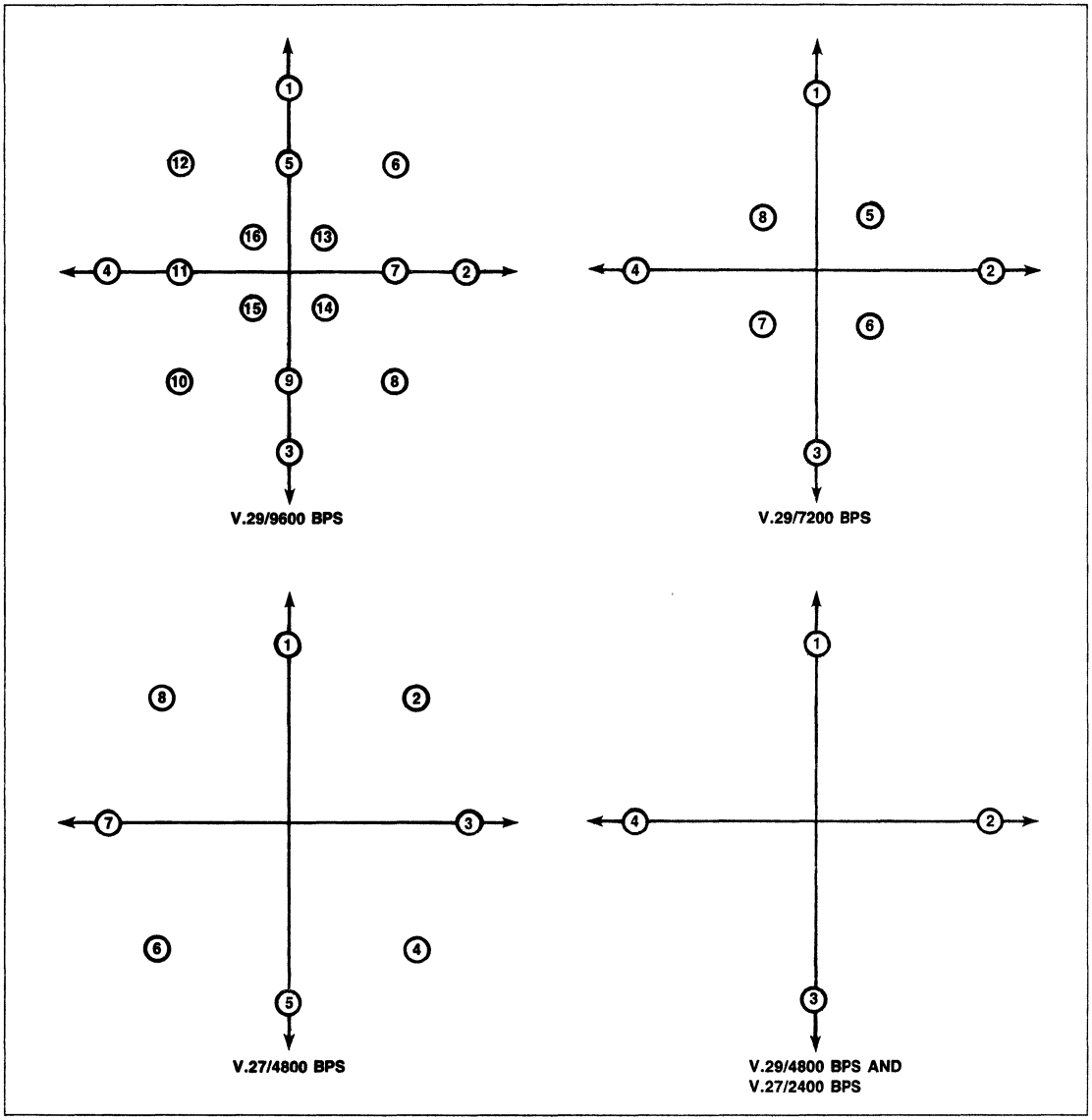


Figure 22. Scaled Signal Points

SCALING OF SP SIGNALS (R1212 AND R2424)

1. **Rotation Angle (16 bits unsigned)—Node 12**
   Range: 0° — 360°

$$\text{Rotated Angle} = \left[\left(\frac{\text{16 Bit Rotated Angle Word}}{2}\right) \bullet 7FFF_{16}\right] \times 5B_{16}$$

2. **Phase Error (16 bits two's complement)—Node 22**

$$\text{Phase Error}° = \frac{\text{16 Bit Phase Error Word}}{K}$$

Where: $-45° \leq$ Phase Error $\leq 45°$

$K = 28_{16}$ for 2400 bps
$K = 14_{16}$ for 1200 bps

3. **Scaled Signal Points (16 bit two's complement)**
   (Refer to Figure 23 and Table 5.)

Table 5. R1212 and R2424 Scaled Signal Points (Hex)

	Modem		
Point	V.22 bis/2400 bps x , y	V.22 A/B, Bell 212A/1200 bps x , y	V.22 A/B 600 bps x , y
1	1800, 1800	1100, 1100	EF00, 1100
2	800, 1800	EF00, 1100	1100, EF00
3	800, 800	EF00, EF00	
4	1800, 800	1100, EF00	
5	F800, 1800		
6	E800, 1800		
7	E800, 800		
8	F800, 800		
9	F800, F800		
10	E800, F800		
11	E800, E800		
12	F800, E800		
13	1800, F800		
14	800, F800		
15	800, E800		
16	1800, E800		

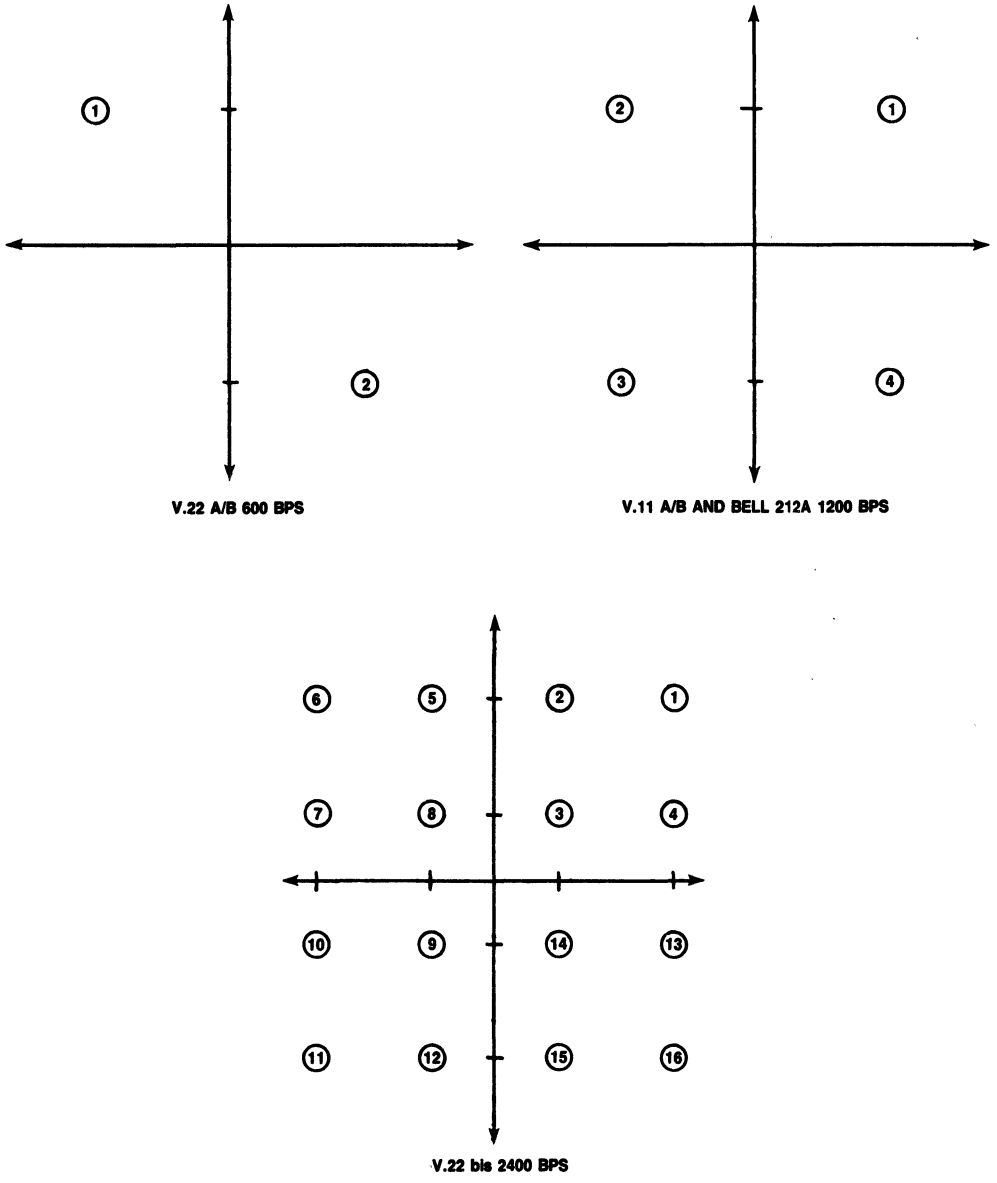


Figure 23. Scaled Signal Points

Rockwell

R2424 and R1212 Modems Auto Dial and Tone Detection

by Jeffrey T. Higgins and Malcolm B. Waters, Product Applications Engineers
Semiconductor Products Division, Newport Beach, California

INTRODUCTION

The R2424 and R1212 modems provide auto dial and tone detection capabilities. These functions aid the designer in creating an intelligent modem subsystem. The auto dialer can be designed to dial both normally and in reverse fashion. Tone detection, a subset of an intelligent auto dialer, can provide call progress monitoring of ringback, busy, and answer tones. This application note presents examples of auto dial and tone detection routines and the problems they overcome.

R2424/R1212 AUTO DIALER

The auto dialer flowchart (Figure 1) shows the typical command flow to cause the modem to dial and then enter the tone detection state. The sequence shown assumes that the modem is in serial control (BUS bits = 0) and that the NEWC bits are set at the appropriate time.

To auto dial the $\overline{\text{DTR}}$ signal must be active. In a constant carrier application where $\overline{\text{RTS}}$ must be on before the end of the handshake, it is recommended that $\overline{\text{RTS}}$ be activated the first time $\overline{\text{DTR}}$ is active and then left on permanently. ($\overline{\text{RTS}}$ may also be hardwired to DTR for constant carrier applications.)

During the time the modem is initialized for auto dialing and the telephone number is being entered, both CRQ bits should be 0. After touch tone or pulse dialing is selected using the DTMF bit and the telephone number is entered, both CRQ bits should be set to a one.

Note:

The CRQ bit in the transmitter enables the auto dialer. The CRQ bit in the receiver enables tone detection when CRQ in the transmitter is enabled. If no tone detection is wanted, CRQ in the receiver does not have to be set.

Following a short delay to allow the relay to close, the DLO and TONE bit are checked. The DLO bit when active tells the user that the relay is closed. If the CRQ bit in the receiver is enabled, the TONE bit at this time will be a one signifying that dial tone is being detected. If both bits are active the actual dialing can begin.

First, the dial digit register is checked to see if it is empty. If it is, the first dial digit is taken from memory and examined. If it is a character that represents a delay then a delay occurs and the second dial digit is taken from memory. If it was not a delay character then it is loaded into the dial digit register. The modem will take the digit and dial it according to the state of the DTMF bit. (The DTMF bit can be changed during the dialing process to allow both tone and pulse dialing of consecutive digits.) The modem also accounts for interdigit delay. After the digit is dialed and the interdigit delay time has elapsed the DDRE bit will be a one signifying that the next digit can be loaded. The interdigit delay can be lengthened by not loading the dial digit register immediately after the DDRE bit is active. This process is continued until the last digit is dialed.

At this point the user can put the modem into data mode by loading $FF into the dial digit register (assuming the CRQ bit in the receiver is 0) or the tone detection routine can begin. If tone detection is desired, $FF should not be loaded at this time. The loading of $FF tells the modem to go into the data mode and start the 30 second abort timer. Once this action is taken the dialing process and tone detection is ended. CRQ in the transmitter must be a one during data mode or the modem will go on-hook. When $FF is loaded, CRQ in the receiver must be a zero.

ANSWER TONE DETECTION—NO RINGBACK

If tone detection is attempted, the software which determines the call progress status must be able to compensate for the many inconsistencies in the dial-up network. One of the problems is no ringback.

Since the tone detector in the modem has a passband from 345 to 635 Hz it is unable to detect answer tone if no ringback occurs. Figure 2 is a flowchart of a routine which switches back and forth between data mode and tone detection mode to catch answer tone if no ringback occurs. Figure 4 shows the worst case example of no ringback and the timing of the software routine which tries to keep the modem from missing the answer tone.

After the last digit is dialed, a 4.5 second watchdog timer is started. During this time the TONE bit is being monitored for call progress tones. If the TONE bit becomes active then the routine of Figure 3 is implemented. If the timer times out and no tone was detected the routine continues and looks for answer tone. (If the answer sequence started immediately after the last digit was dialed then approximately 500 milliseconds of answer tone would remain. This is enough time for the originating modem to detect answer tone.) CRQ in the receiver is reset to zero and $FF is loaded into the dial digit register. This action puts both the transmitter and receiver in data mode. The receiver can now detect answer tone. A 750 ms watchdog timer is started. The DSR bit is monitored during this time. If DSR becomes active then answer tone was detected and the modem will continue with the handshake. If the timer times out and DSR is not active the program can exit and abort the call (depending on how many tries are desired for tone detection) or it can go back into tone detection looking for call progress tones.

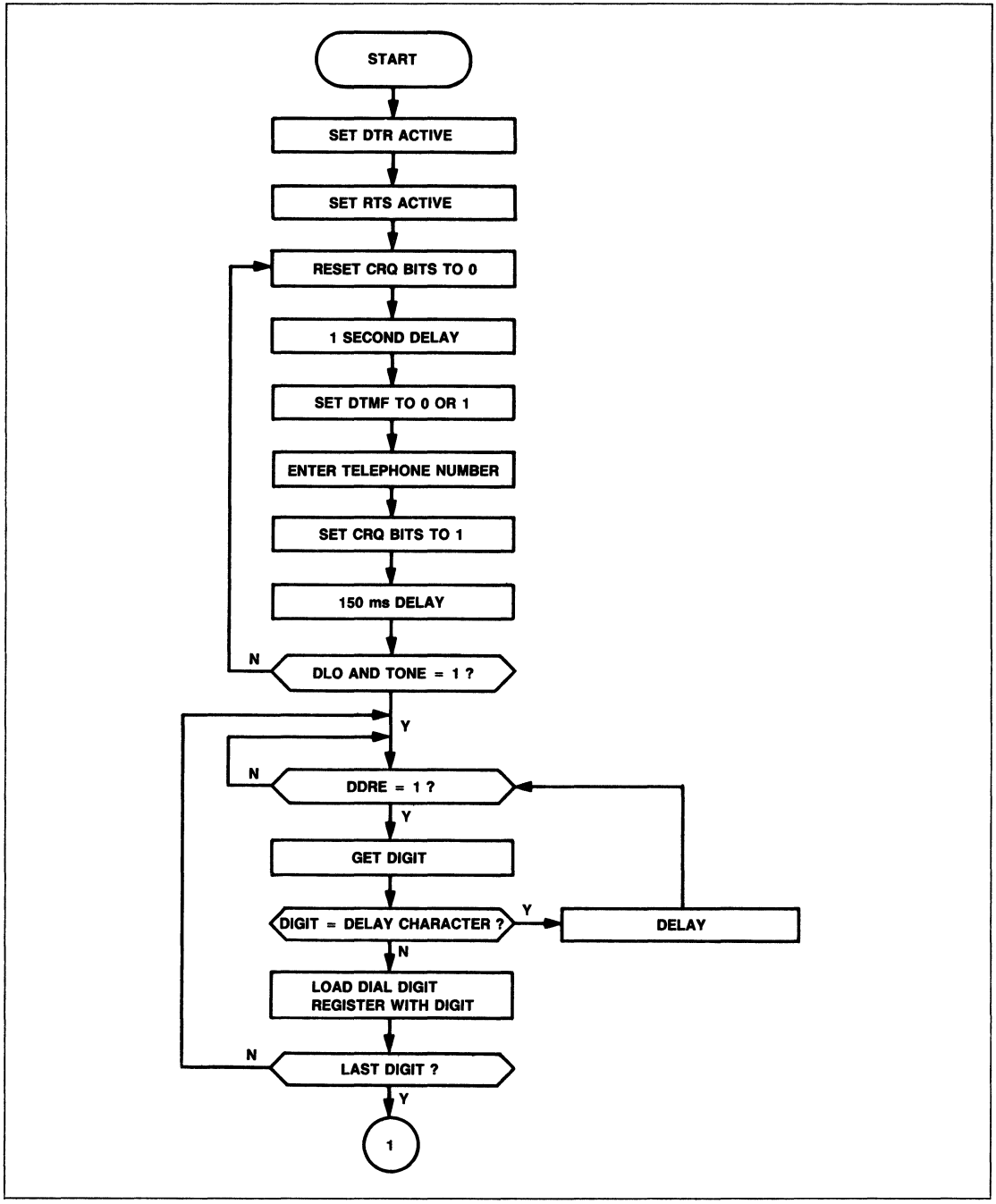


Figure 1. R1212 and R2424 Auto Dial Routine

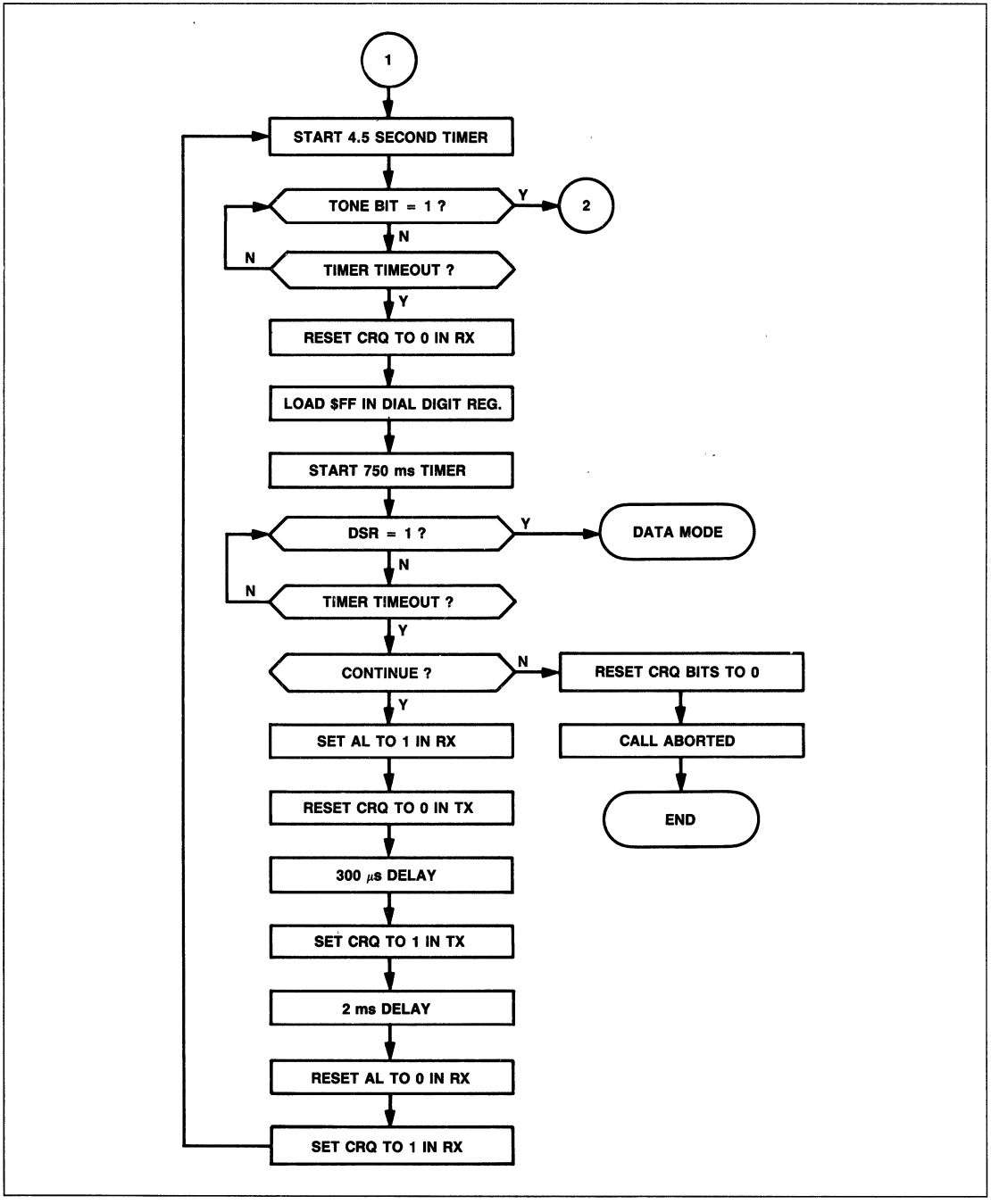


Figure 2. Answer Tone Detection When No Ringback Occurs

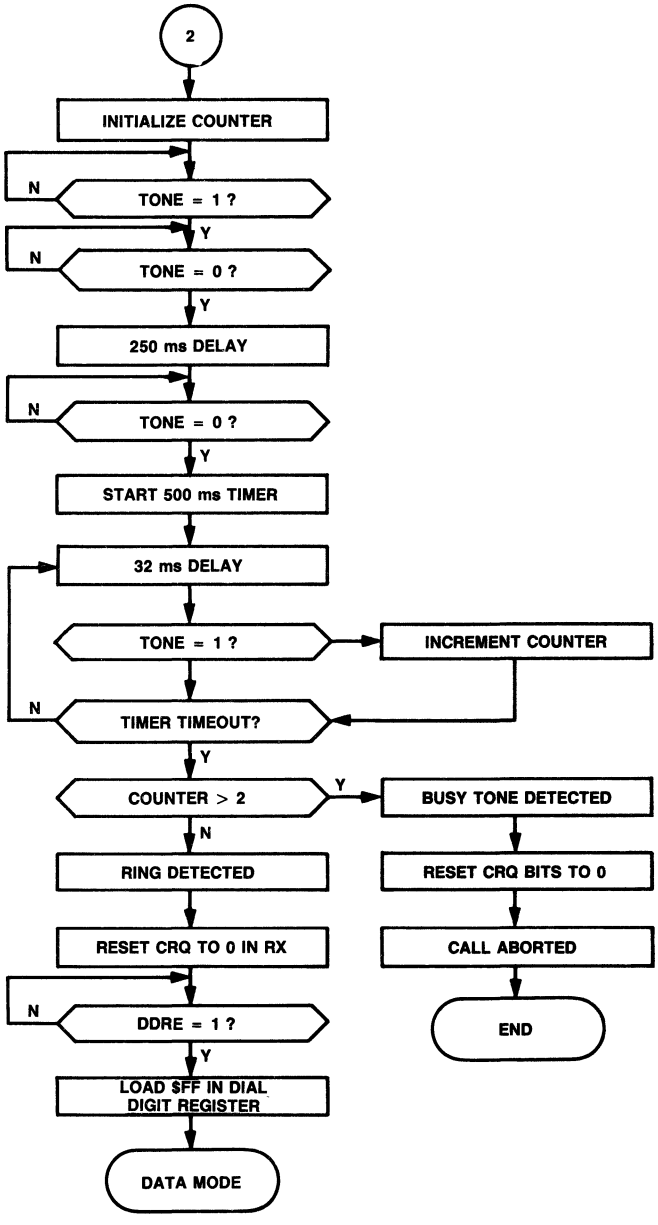


Figure 3. Call Progress Detection of Ringback and Busy Tones

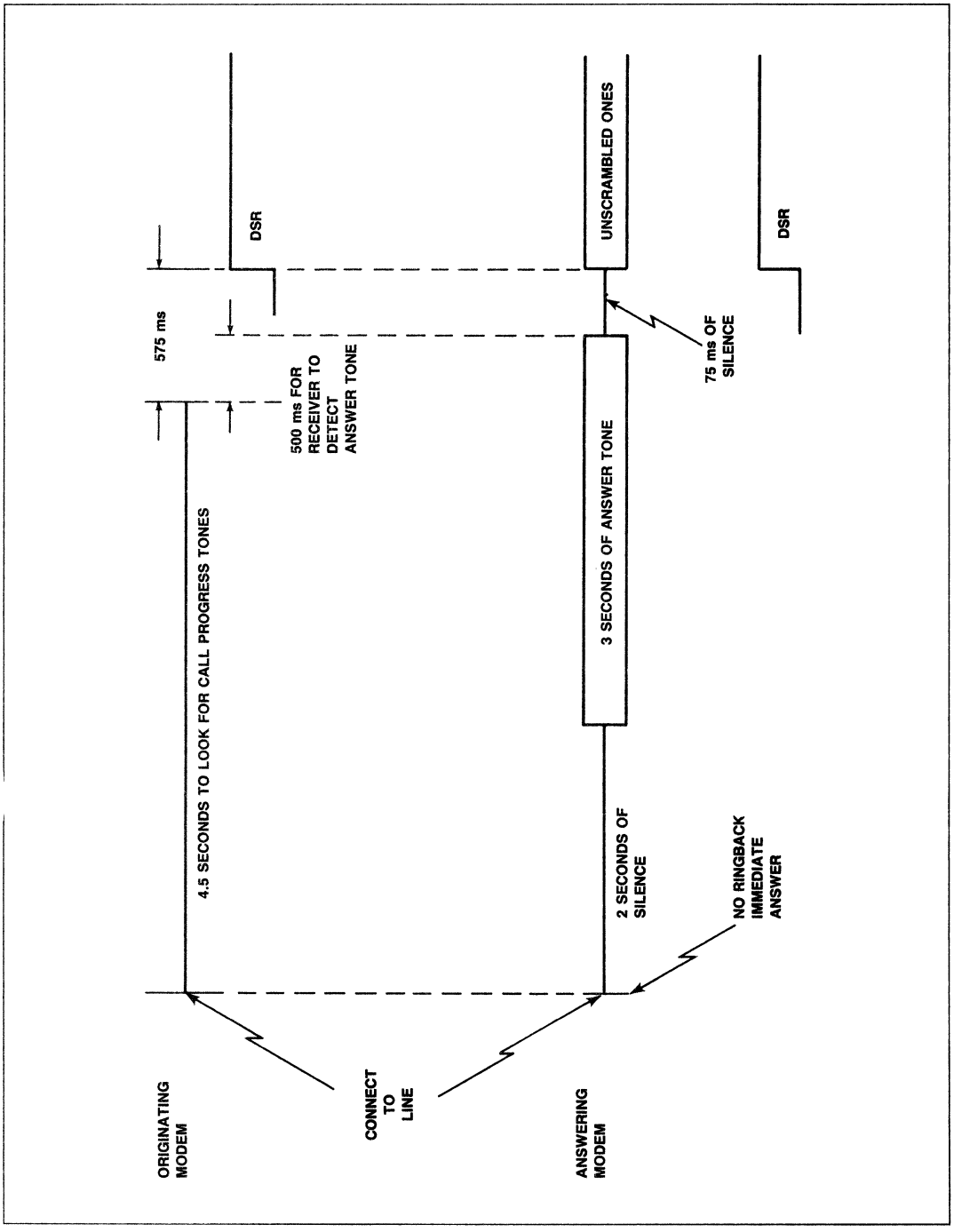


Figure 4. Worst Case Tone Detection Example: No Ringback, Immediate Answer

If it is desired to go back into the tone detect mode, the following sequence must be followed. Set the AL bit in the receiver to a one. Reset CRQ in the transmitter to a zero and after 2 sample times (approximately 300 microseconds) set CRQ in the transmitter to a one. This action resets the transmitter, without opening the relay. One baud time later (approximately 2 ms) reset AL in the receiver to a zero. (Although setting and resetting the AL bit in the receiver does not seem to make sense, it does help to ensure internal flags are properly set so the modem does not lock-up by switching back and forth between data and tone detect mode. After AL in the receiver is reset, set CRQ in the receiver to a one. At this point the modem is back in tone detect mode and the routine begins again.

If after a number of passes through the routine no call progress or answer tones have been detected, the call can be aborted by resetting both CRQ bits to a zero.

CALL PROGRESS DETECTION

If the TONE bit becomes active during the 4.5 second period of Figure 2, the call progress tone detection routine of Figure 3 should be implemented. This routine monitors the duty cycle of the TONE bit and reports what tone is being detected.

The difficulty with any tone detection routine is the fact that the tones provided by the telephone network are not always according to specification. Figure 5 shows both ideal and nonideal tone detection situations. It is the nonideal tones that create the timing problems in the tone detection routine, and those situations must be dealt with. The routine of Figure 3 provides a possible solution to catch the nonideal call progress tones.

The call progress detection routine makes its decisions after the on-to-off period of any tone. After a 250 ms delay the TONE bit is monitored for 500 ms. During this time samples of the TONE bit are taken every 32 ms (see Figure 6). If the TONE bit is active when sampled, a counter is incremented. If the counter was incremented more than two times it is assumed that a busy tone was detected. CRQ should then be reset in both the transmitter and receiver to zero. This puts the modem back on-hook and the call is aborted. If the counter was incremented two times or less a ring was detected and the modem must go into data mode. This is accomplished by resetting CRQ in the receiver to zero and loading $FF into the dial digit register.

Note:

It is assumed that the answering modem will answer after one ring. Therefore, the tone detection routine must decide the call progress status before the remote modem answers.

R2424/R1212 REVERSE AUTO DIALER

The R2424 and R1212 can be used to call an originate-only modem. This application provides a higher level of security in dial-up environments. With the increasing problem of data security in dial-up computer systems it is necessary to prevent unauthorized users from connecting to the network. Reverse auto dialing helps solve the problem.

The central site modem would be set up to monitor a ringing signal, but would be configured for originate mode. The remote modem would dial, switch to the answer mode and send the answering sequence. The central site would answer the call and detect answer tone as though it had originated the call. The handshake would then proceed as normal.

If an authorized modem which was not configured to send answertone after dialing, tried to connect, the central site modem would not respond after answering, because it would be expecting answer tone.

The reverse auto dialer flowchart (Figure 7) shows the command flow to cause the modem to dial and then enter the answer state and send answer tone. The sequence shown assumes that the modem is in parallel control (BUS bits = 1) and that the NEWC bits are set at the appropriate time.

The routine initializes the modem and prepares it for dialing. The ORG bit is set to a zero (manual answer) but is ignored during the dialing process. The dialing is identical to Figure 1 except that CRQ in the receiver is not set to a one. No tone detection can be done with the reverse dialing because CRQ in the transmitter is disabled after the last digit is dialed. After CRQ in the transmitter is reset to a zero the DATA bit is immediately set to a one. Since the ORG bit was set previously, the result is the OH relay stays closed, the modem switches from originate to answer configuration, and the answer sequence is transmitted according to the specification of the modem configuration.

The modem will send the answering sequence for 30 seconds or until the other modem responds.

R2424/R1212 REVERSE AUTO ANSWER

The R2424 and R1212 provides the capability to auto answer in the originate configuration. This feature complements the reverse auto dialing described previously.

The flowchart of Figure 8 shows the method to perform the reverse auto answering. The sequence shown assumes that the modem is in parallel control (BUS bits = 1) and that the NEWC bits are set at the appropriate time.

The ORG bit is set to a one, configuring the modem to originate. On detection of the ring using the RI bit, the DATA bit is set to a 1. This sequence causes the modem to answer, but remain in the originate mode looking for the answer sequence.

A more comprehensive description of R1212/R2424 modem operation is contained in Section 4 of the Modem Interface Guide (Order No. 685)

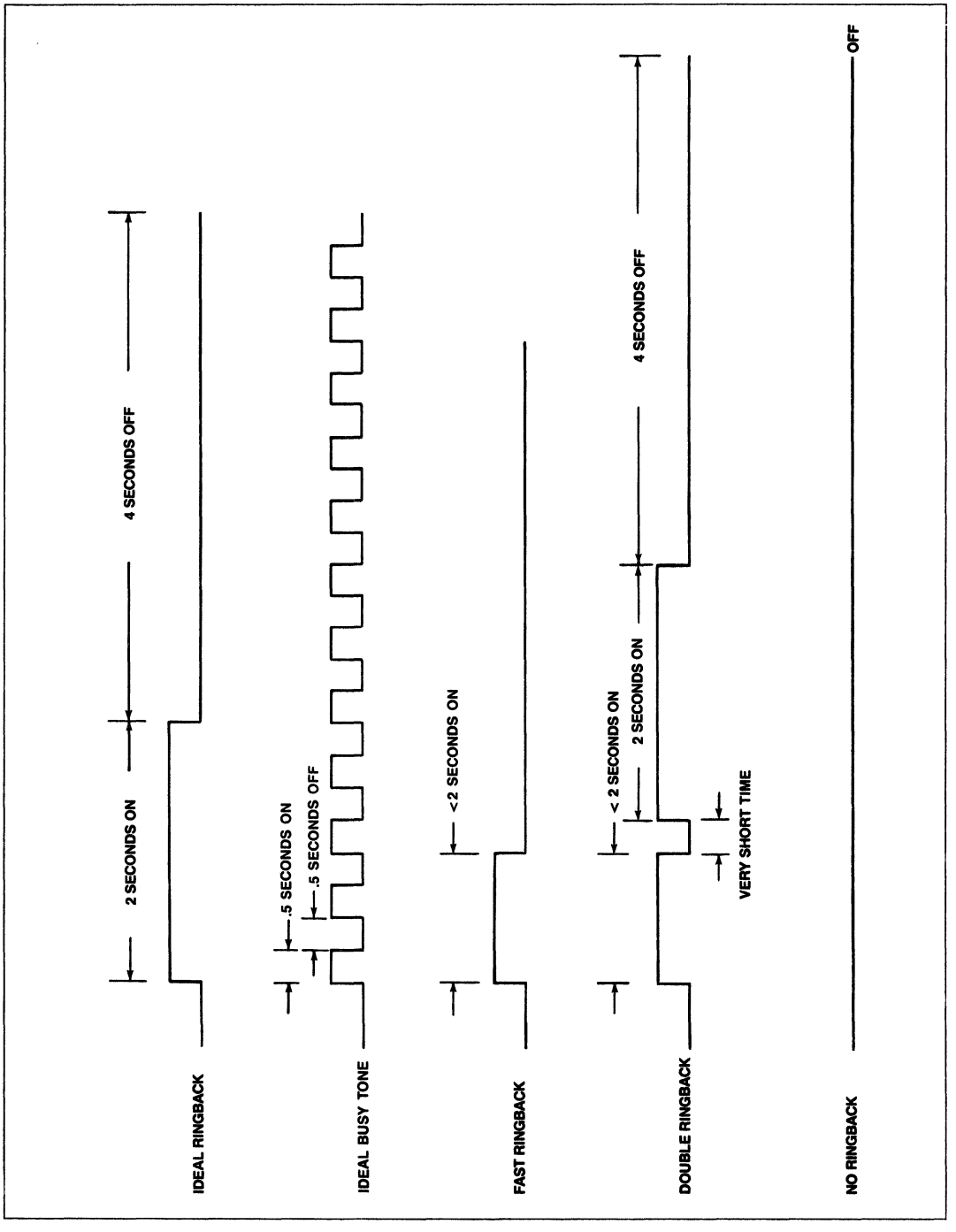


Figure 5. Call Progress Tones Timing Problems

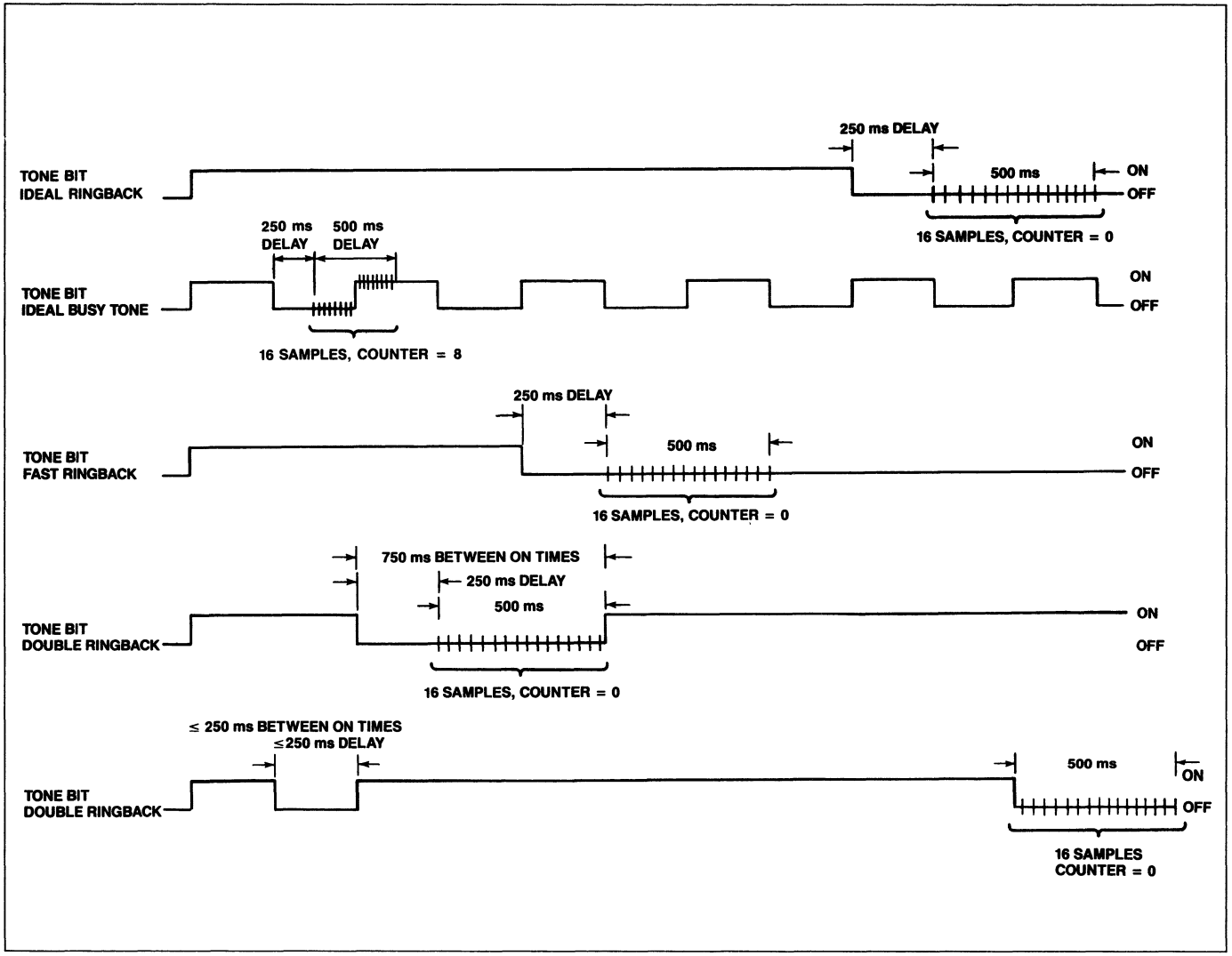


Figure 6. Timing for Call Progress Tone Detection Routine

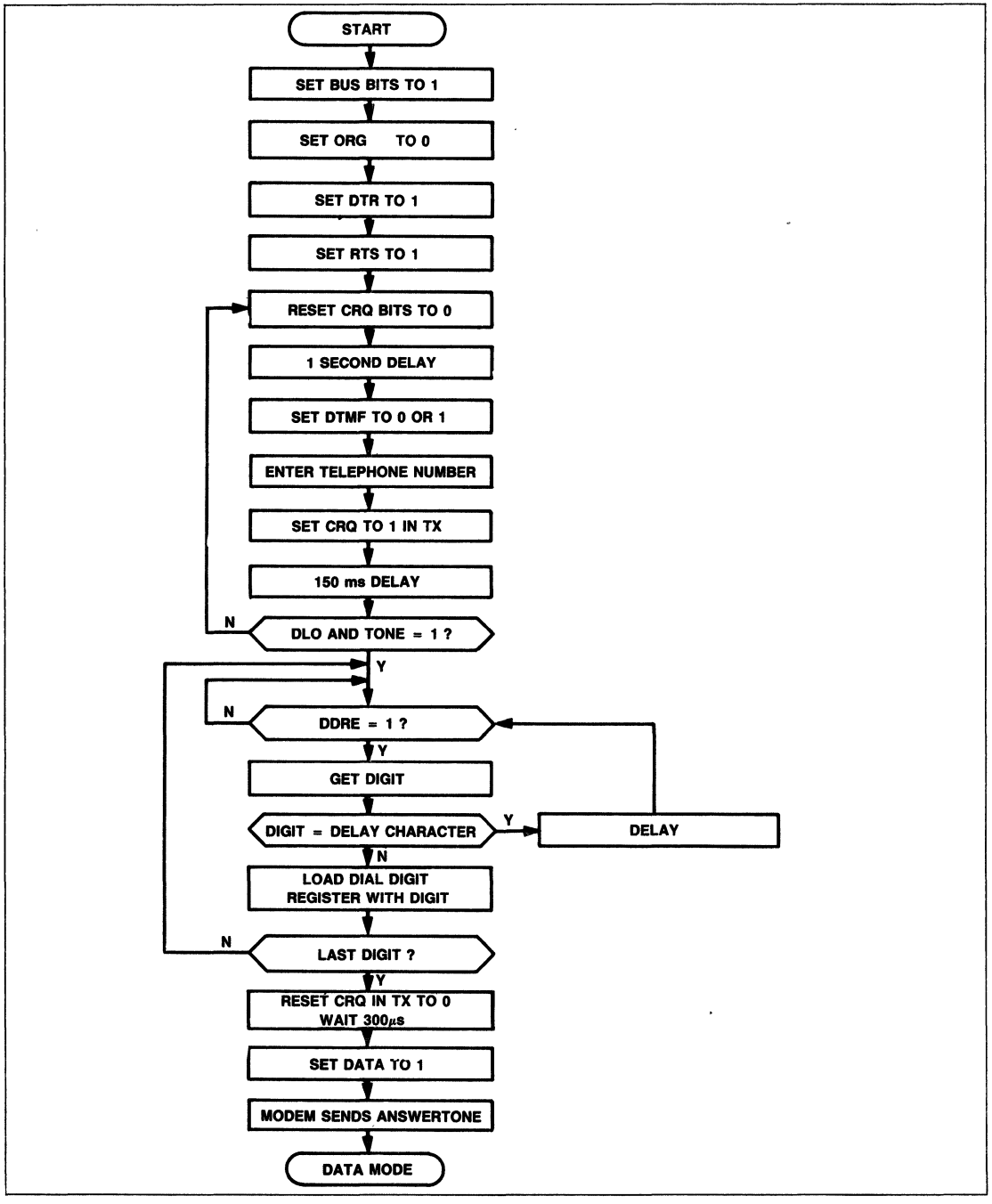


Figure 7. R1212 and R2424 Reverse Auto-Dial Routine

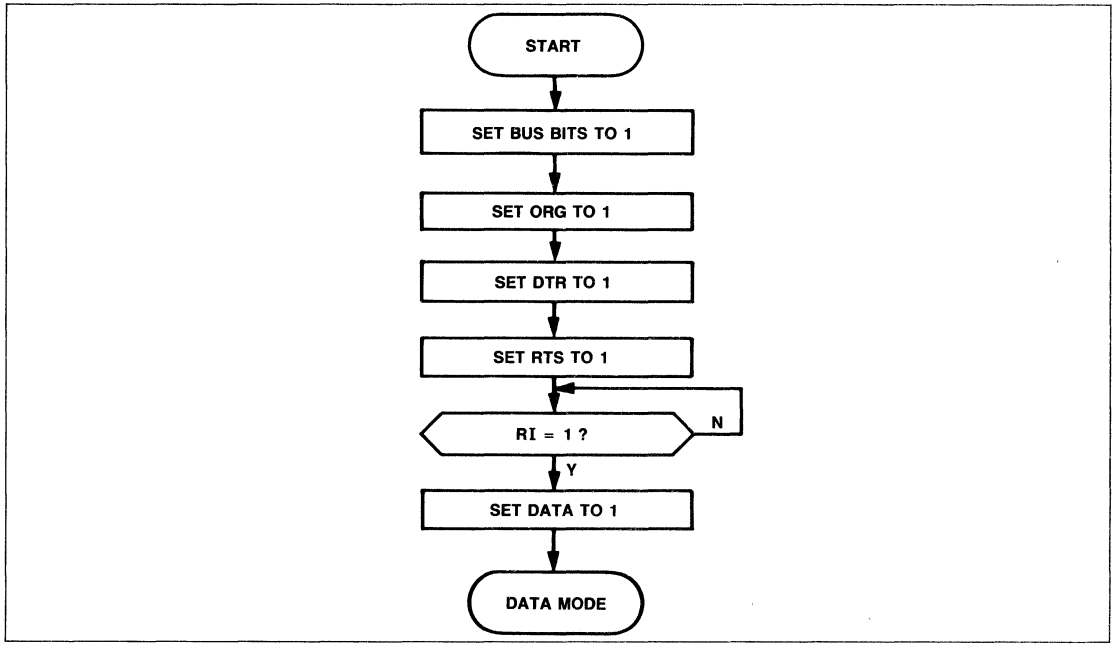


Figure 8. R1212 and R2424 Reverse Auto Answer

Rockwell

8088 Microprocessor to R1212/R2424 Modem Interface

INTRODUCTION

This application note details the connections and circuitry needed to interface a Rockwell R1212 1200 BPS or R2424 2400 BPS Full-Duplex Modem to an 8088 microprocessor-based system. Also included is an assembly language level computer program that performs an auto dialer function.

8088 INTERFACE

The basic interface signals between an R1212/R2424 and an 8088-based system are summarized in Figure 1. A schematic detailing the components and connections necessary to interface an R1212/R2424 modem to an expansion slot in an IBM PC (or equivalent) personal computer is shown in Figure 2. This particular circuit was used with a COMPAQ Personal Computer but should be able to be used with an IBM PC or other compatible computer with little or no modification.

The R1212/R2424 modem is mapped into the memory space allocated for the prototype board in the IBM PC input/output map. The chip select logic places the modem in the following address space:

Chip Select Line	Address Range
$\overline{CS0}$	$300-$30F
$\overline{CS1}$	$310-$31F

The INS8250 UART provides the asynchronous communications between the R1212/R2424 modem and the 8-bit microprocessor data bus.

AUTO DIALER SOFTWARE

The 8088 assembly language instructions (and assembled hmachine code that performs an auto dialer function is listed starting on page 3.

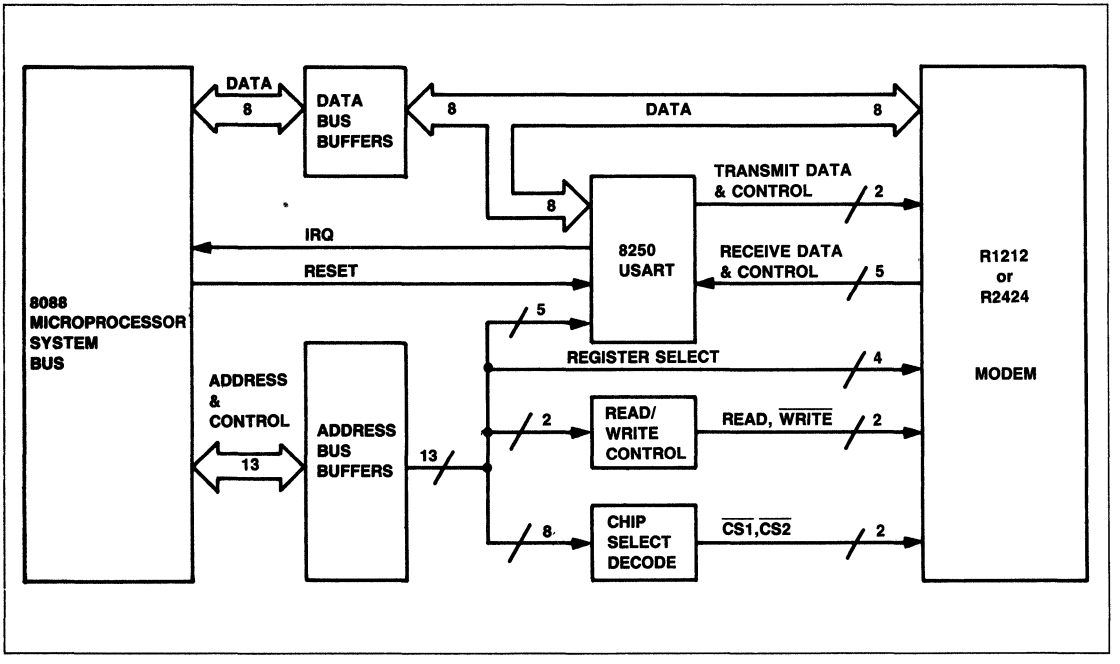


Figure 1. IBM PC to R1212/R2424 Modem Interface

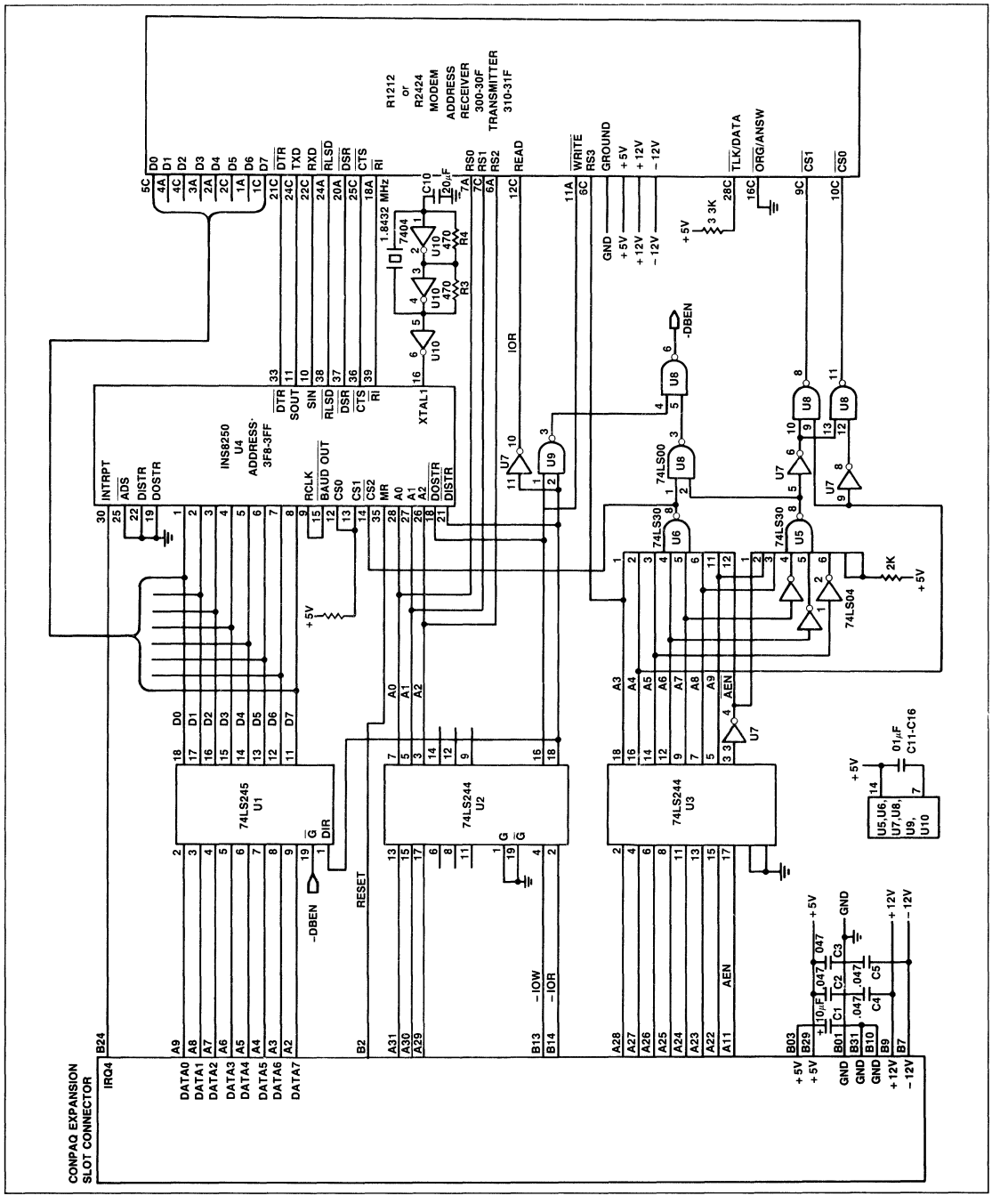


Figure 2. IBM PC to R1212/R2424 Modem Schematic

8088 AUTO DIALER ASSEMBLY LISTING

```
                                TITLE   8088 AUTO DIALER (DIAL1.ASM)
                                COMMENT*

                                        Rockwell Applications Lab 5/15/84

                                        This is written as an example of an auto-dialer in 8088
                                        Assembly Language.  It was written using the Micosoft
                                        Macro Assembler which runs under the IBM Disk Operating
                                        System.

                                        The hardware used places the interface memory Bank 0
                                        and Bank 1 at locations 300-30F and 310-31F respectively.
                                        This is the space allocated for the Prototype Card in the
                                        IBM I/O Address Map.
                                *
                                ;
                                ;Macro pseudo-op for use in setting req bits in the interface memory
                                ;
                                ;The address and bit to be set/reset is sent to the Macro.
                                ;The Macro then gets the appropriate byte from the R1224.
                                ;This byte is ORed with the bit to be set to change only that
                                ;bit.  The byte is then sent back to the R1224.
                                ;
                                SET     MACRO   ADDR,BIT
                                        MOV     DX,ADDR
                                        IN      AL,DX
                                        OR      AL,BIT
                                        OUT     DX,AL
                                        ENDM
                                ;
                                ;
0000                            STACK   SEGMENT STACK
0000  0100 [                            DB      256     DUP (?)
            ??
                ]

0100                            STACK   ENDS
                                ;
0000                            DATA    SEGMENT
0000  14 15 [                   BUF     DB      20,21 DUP(0)    ;Set up a buffer for the phone number
            00
                ]

0016  20 45 4E 54 45 52         MSG     DB        ENTER PHONE NUMBER:$
      20 50 48 4F 4E 45
      20 4E 55 4D 42 45
      52 3A 24 20
002C  20 20 44 49 41 4C         MES1    DB          DIALING $
      49 4E 47 20 24 20
0038                            DATA    ENDS
                                ;
0000                            CODE    SEGMENT
0000                            START   PROC    FAR
                                ;
                                ;Standard Program Prologue
                                ;
                                        ASSUME  CS:CODE,DS:DATA,SS:STACK
0000  1E                                PUSH    DS
0001  BB 0000                          MOV     AX,0
0004  50                                PUSH    AX
0005  BB  ---- R                       MOV     BX,DATA ;Get data segment base address
0008  8E DB                             MOV     DS,BX
000A  E8 000E R                         CALL    MAIN
000D  CB                                RET
000E                            START   ENDP
```

8088 AUTO DIALER ASSEMBLY LISTING (Continued)

```
                                ;
000E                            MAIN    PROC NEAR
                                ;
                                ;Dial set-up
                                ;
                                        SET     31DH,00H        ;Assure that DTR is a 0
000E  BA 031D                 +         MOV     DX,31DH
0011  EC                      +         IN      AL,DX
0012  0C 00                   +         OR      AL,00H
0014  EE                      +         OUT     DX,AL
                                        SET     31EH,08H        ;Set NEWC
0015  BA 031E                 +         MOV     DX,31EH
0018  EC                      +         IN      AL,DX
0019  0C 08                   +         OR      AL,08H
001B  EE                      +         OUT     DX,AL
                                ;
                                        SET     30DH,80H        ;Set the BUS bit, receiver
001C  BA 030D                 +         MOV     DX,30DH
001F  EC                      +         IN      AL,DX
0020  0C 80                   +         OR      AL,80H
0022  EE                      +         OUT     DX,AL
                                ;
                                        SET     31DH,80H        ;Set the BUS bit, transmitter
0023  BA 031D                 +         MOV     DX,31DH
0026  EC                      +         IN      AL,DX
0027  0C 80                   +         OR      AL,80H
0029  EE                      +         OUT     DX,AL
                                ;
                                        SET     31BH,02H        ;Set DTMF for tone dialing
002A  BA 031B                 +         MOV     DX,31BH
002D  EC                      +         IN      AL,DX
002E  0C 02                   +         OR      AL,02H
0030  EE                      +         OUT     DX,AL
                                ;
                                        SET     30DH,40H        ;Set CRQ bit, receiver
0031  BA 030D                 +         MOV     DX,30DH
0034  EC                      +         IN      AL,DX
0035  0C 40                   +         OR      AL,40H
0037  EE                      +         OUT     DX,AL
                                ;
                                        SET     31DH,40H        ;Set CRQ bit, transmitter
0038  BA 031D                 +         MOV     DX,31DH
003B  EC                      +         IN      AL,DX
003C  0C 40                   +         OR      AL,40H
003E  EE                      +         OUT     DX,AL
                                ;
                                ;Wait at least 50 msec between reset and set of DTR
                                ;
003F  B3 FF                             MOV     BL,0FFH
0041  FE CB                     TIME1:  DEC     BL
0043  80 FB 00                         CMP     BL,00H
0046  75 F9                            JNZ     TIME1
                                ;
                                        SET     31DH,08H        ;Set DTR
0048  BA 031D                 +         MOV     DX,31DH
004B  EC                      +         IN      AL,DX
004C  0C 08                   +         OR      AL,08H
004E  EE                      +         OUT     DX,AL
                                ;
                                        SET     30EH,08H        ;Set NEWC, Receiver
004F  BA 030E                 +         MOV     DX,30EH
0052  EC                      +         IN      AL,DX
0053  0C 08                   +         OR      AL,08H
0055  EE                      +         OUT     DX,AL
                                        SET     31EH,08H        ;Set NEWC bit, Transmitter
0056  BA 031E                 +         MOV     DX,31EH
0059  EC                      +         IN      AL,DX
005A  0C 08                   +         OR      AL,08H
005C  EE                      +         OUT     DX,AL
                                ;
                                ;Check that we are off-hook and ready to dial
                                ;
005D  BA 0318                   WAIT:   MOV     DX,318H
0060  EC                               IN      AL,DX
0061  24 80                            AND     AL,80H
0063  3C 80                            CMP     AL,80H          ;Check to see if DLO is set
0065  75 F6                            JNZ     WAIT            ;If not, wait for it
                                ;
```

8088 AUTO DIALER ASSEMBLY LISTING (Continued)

```
                                ;Wait for dial-tone on the line
                                ;
0067  BA 0308                           MOV     DX,308H
006A  EC                                IN      AL,DX
006B  24 80                             AND     AL,80H
006D  3C 80                             CMP     AL,80H
006F  75 EC                             JNZ     WAIT
                                ;
0071  B4 09                             MOV     AH,9
0073  BA 0016 R                         MOV     DX,OFFSET MSG   ;Print prompt for phone # input
0076  CD 21                             INT     21H
                                ;
                                ; Read the number and display it.
                                ;
0078  B4 0A                             MOV     AH,0AH
007A  BA 0000 R                         MOV     DX,OFFSET BUF   ;Buffered Keyboard Input
007D  CD 21                             INT     21H
                                ;
007F  B2 0A                             MOV     DL,0AH          ;Line feed
0081  B4 02                             MOV     AH,02           ;Display function
0083  CD 21                             INT     21H             ;DOS call
                                ;
0085  B4 09                             MOV     AH,9
0087  BA 002C R                         MOV     DX,OFFSET MES1  ;Print DIALING message
008A  CD 21                             INT     21H
                                ;
                                ; Loop and redisplay telephone number as it is dialed
                                ;
008C  BE 0000                           MOV     SI,0
008F  B9 0000                           MOV     CX,0
0092  8A 0E 0001 R                      MOV     CL,BUF+1        ;Get number of digits read
0096  8A 94 0002 R              PAD:    MOV     DL,BUF[SI+2]
                                ;DL now contains the dial digit
009A  52                                PUSH    DX      ;Preserve the dial digit on the stack
                                ;
                                ;Check to see that the dial digit register is empty
                                ;
009B  BA 031E                   FULL1:  MOV     DX,31EH
009E  EC                                IN      AL,DX
009F  24 01                             AND     AL,01H
00A1  3C 01                             CMP     AL,01H
00A3  75 F6                             JNZ     FULL1
                                ;
                                ;Get the dial digit off the stack
                                ;
00A5  5A                                POP     DX
                                ;
                                ;Check to see if it's a carriage return
                                ;
00A6  80 FA 0D                          CMP     DL,0DH
00A9  74 10                             JZ      DONE            ;If it is, end the dialing sequence
                                ;
                                ;Feedback for dialing
                                ;
00AB  B4 02                             MOV     AH,2            ;Print the digits as they are dialed
00AD  CD 21                             INT     21H
                                ;
                                ;Send the dial digit to the R1224
                                ;
00AF  80 E2 0F                          AND     DL,0FH
00B2  8A C2                             MOV     AL,DL           ;Dial Digit must be in AL to be sent
00B4  BA 0310                           MOV     DX,310H         ;to the I/O port
00B7  EE                                OUT     DX,AL           ;Send it
00B8  46                                INC     SI              ;Point to the next digit
00B9  E2 DB                             LOOP    PAD
                                ;
                                ;Go here to end the dial sequence by putting FF
                                ;into the dial digit register
                                ;
                                ;Assure DDRE empty again
                                ;
00BB  BA 031E                   DONE:   MOV     DX,31EH
00BE  EC                                IN      AL,DX
00BF  24 01                             AND     AL,01H
00C1  3C 01                             CMP     AL,01H
00C3  75 F6                             JNZ     DONE
                                ;
00C5  BA 0310                           MOV     DX,310H
00C8  B0 FF                             MOV     AL,0FFH
00CA  EE                                OUT     DX,AL
                                ;
00CB  C3                                RET
00CC                            MAIN    ENDP
00CC                            CODE    ENDS
                                END     START
```

Rockwell

RC2424DP/DS
Diagnostic Data Scaling

INTRODUCTION

This application note is a supplement to the RC2424DP/DS data sheet. It provides information on parameters accessible in DSP RAM shown in Table 1, and on Checksum verfication available after Power-on or Reset.

POWER-ON/RESET DSP TEST MODE

After Power-on or Reset, the RC2424DP/DS DSP enters into a test mode and calculates Checksum on ROM. The result of the Checksum verification is written into Host Interface memory bytes 15 and 14. The valid checksum is a constant $412B. At the same time, ASCII values for the "part number" are written into Host Interface memory bytes 13 and 12, and ASCII values for the "code revision lettter" are written into Host Interface memory bytes 11 and 10.

For example, on the C5308-15 "D" code, the number "08" is the part number and "D" is the code revision letter. The values written into Host Interface memory would be as follows:

Register	Value	Contents
15	$41	Checksum Upper word
14	$2B	Checksum Lower word
13	$30	ASCII value of "0"
12	$38	ASCII value of "8 "
11	$20	ASCII value of " "
10	$44	ASCII value of "D"

After the DSP writes to byte 10, the TDBE bit will be set. This indicates to the host that the self-test information can be read. The DSP will wait 20 ms or until the host reads or writes Host Interface Memory byte 10. After this, the DSP will execute the Initialization sequence.

DSP RAM ACCESS

DSP RAM ORGANIZATION

The DSP contains four sections of 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) sections, as well as data and coefficient sections. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously in either the data or coefficient section.

INTERFACE MEMORY ACCESS TO DSP RAM

The DSP interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The addresses stored in DSP interface memory RAM Address registers (i.e., XADD and YADD) by the host, in conjunction with the data or coefficient RAM bits (i.e., XCR and YCR) determine the DSP RAM addresses for data access.

One or two 16-bit words are transferred between DSP RAM and DSP interface memory once each internal DSP cycle. The transmitter and the receiver sample rate functions operate at the 7200 Hz sample rate. The receiver baud rate functions operate at 600 Hz.

Two RAM access bits (XACC and YACC) in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The RAM tests these bits each sample period (139 microseconds).

READING AND WRITING THE DSP RAM

The procedure for reading and writing the DSP RAM is described in the RC2424DP/DS data sheet (Order No. MD53). The parameters shown in Table 1 are described on the following pages. The format for all parameters is 16 bits, twos complement.

Table 1. DSP RAM Parameters

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
1	1	0	–	1st Equalizer Tap, Real
1	1	C	–	Last Equalizer Tap, Real
2	1	–	0	1st Equalizer Tap, Imaginary
2	1	–	C	Last Equalizer Tap, Imaginary
3	0	12	–	Rotated Error, Real
4	0	–	12	Rotated Error, Imaginary
5	0	14	–	Max AGC Gain Word
6	0	6C	–	Pulse Dial Interdigit Time
7	0	–	6C	Tone Dial Interdigit Time
8	0	6D	–	Pulse Dial Relay Make Time
9	0	–	6D	Pulse Dial Relay Break Time
10	0	–	6E	DTMF Duration
11	0	6F	–	Tone 1 Angle Increment Per Sample
12	0	–	6F	Tone 2 Angle Increment Per Sample
13	0	71	–	Tone 1 Amplitude
14	0	–	71	Tone 2 Amplitude
15	0	74	–	Max Samples Per Ring Frequency Period
16	0	–	74	Min Samples Per Ring Frequency Period
17	1	0E	–	Real Part of Error
18	1	–	0E	Imaginary Part of Error
19	1	–	10	Rotation Angle for Carrier Recovery
20	1	11	–	Rotated Equalizer Output Real
21	1	–	11	Rotated Equalizer Output Imaginary
22	1	12	–	Lower Part of Phase Error
23	1	–	12	Upper Part of Phase Error
24	1	14	–	Upper Part of AGC Gain Word
25	1	–	14	Lower Part of AGC Gain Word
26	1	1C	–	Average Power
27	1	2A	–	Phase Error

Table 1. DSP RAM Parameters (Cont'd)

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
28	1	2C	–	Tone Power (ATBELL, BEL103 or TONEA)
29	1	–	2C	Tone Detect Threshold (Call Progress Energy)
30	1	2D	–	Tone Power (ATV25 or TONEB)
31	1	2E	–	Tone Power (TONEC)
32	1	33	–	Tone Detect Threshold (ATBELL, BEL103, or TONEA)
33	1	34	–	Tone Detect Threshold (ATV25 or TONEB)
34	1	35	–	Tone Detect Threshold (TONEC)
35	1	38	–	Zero Crossing Counter
36	1	52	–	Eye Quality Monitor (EQM)
37	1	–	2E	Filter 1 Coefficient $\alpha 0$
38	1	–	2F	Filter 1 Coefficient $\alpha 1$
39	1	–	30	Filter 1 Coefficient $\alpha 2$
40	1	–	31	Filter 1 Coefficient $\beta 1$
41	1	–	32	Filter 1 Coefficient $\beta 2$
42	1	–	34	Filter 2 Coefficient $\alpha 0$
43	1	–	35	Filter 2 Coefficient $\alpha 1$
44	1	–	36	Filter 2 Coefficient $\alpha 2$
45	1	–	37	Filter 2 Coefficient $\beta 1$
46	1	–	38	Filter 2 Coefficient $\beta 2$
47	1	–	3A	Filter 3 Coefficient $\alpha 0$
48	1	–	3B	Filter 3 Coefficient $\alpha 1$
49	1	–	3C	Filter 3 Coefficient $\alpha 2$
50	1	–	3D	Filter 3 Coefficient $\beta 1$
51	1	–	3E	Filter 3 Coefficient $\beta 2$
52	1	–	45	Filter 4 Coefficient $\alpha 0$
53	1	–	46	Filter 4 Coefficient $\alpha 1$
54	1	–	47	Filter 4 Coefficient $\alpha 2$
55	1	–	48	Filter 4 Coefficient $\beta 1$
56	1	–	49	Filter 4 Coefficient $\beta 2$

*XCR if an XRAM address is listed; YCR if a YRAM address is listed.

No. 1 - Equalizer Tap Coefficients, Real **XCR: 1 XRAM Addr: 0 - C**

The adaptive equalizer is a transversal filter (Figure 1). The filter is tuned by varying the weighting coefficients, C_0 through C_N. The RC2424DP/DS has 13 taps. Since the baseband signal is complex it requires both X and Y coefficients for each tap. The delay between taps is 1/2 baud time. The adaptive process attempts to adjust all coefficients to minimize the mean squared error.

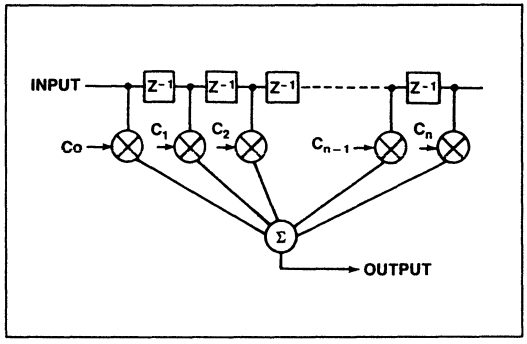


Figure 1. Equalizer Structure

No. 2 - Equalizer Tap Coefficients, Imaginary **YCR: 1 YRAM Addr: 0 - C**

These values represent the imaginary component of the equalizer tap coefficients. (See above.)

No. 3 - Rotated Error, Real **XCR: 0 XRAM Addr: 12**

The Rotated Error vector is the angle and magnitude difference between an actual received signal point (P2) and the nearest ideal point (P1) in the baseband signal plane (Figure 2). The real and imaginary components are calculated once per baud time. See Real Part of Error (No. 17) and Imaginary Part of Error (No. 19).

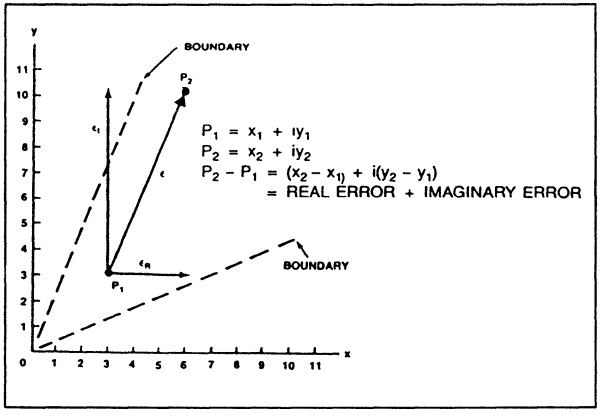


Figure 2. Rotated Error

No. 4 - Rotated Error, Imaginary YCR: 0 YRAM Addr: 12

These values represent the imaginary component of the Rotated Error vector. (See No. 3.)

No. 5 - Max AGC Gain Word YCR: 0 YRAM Addr: 14

Default: $2500 (31.95 dB)

This value represents the maximum AGC gain, and can be varied by the host.

Formula:

Max AGC Gain Word = (46.4 - Max AGC Gain (dB)) x 32768/50

Convert value to hex to store in RAM.

No. 6 - Pulse Dial Interdigit Time XCR: 0 XRAM Addr: 6C

Default: $1518 (750 ms)

This value represents the amount of delay in samples between digits dialed when in pulse dial mode (DTMF = 0).

Formula:

Interdigit time (samples) = Interdigit time (sec) x 7200 (samples/sec)

Convert sample value to hex to store in RAM.

No. 7 - Tone Dial Interdigit Time YCR: 0 YRAM Addr: 6C

Default: $01F8 (70 ms)

This value represents the amount of delay in samples between digits dialed when in tone dial mode (DTMF = 1).

Formula:

Interdigit Time (samples) = Interdigit Time (sec) x 7200 (samples/sec)

Convert sample value to hex to store in RAM.

No. 8 - Pulse Dial Relay Make Time XCR: 0 XRAM Addr: 6D

Default: $0120 (40 ms)

This value represents the time (in number of samples) that the $\overline{\text{OHRELAY}}$ will close for each digit dialed.

Formula:

Pulse Make Time (samples) = Pulse Make Time (sec) x 7200 (samples/sec)

Convert sample value to hex to store in RAM.

No. 9 - Pulse Dial Relay Break Time YCR: 0 YRAM Addr: 6D

Default: $01B0 (60 ms)

This value represents the time (in number of samples) that the $\overline{\text{OHRELAY}}$ will open for each digit dialed.

Formula:

Pulse Break Time (samples) = Pulse Break Time (sec) x 7200 (samples/sec)

Convert sample value to hex to store in RAM.

No. 10 - DTMF Duration **YCR: 0 YRAM Addr: 6E**

Default: $01F8 (70 ms)

This value represents the time duration of each DTMF digit dialed.

Formula:

DTMF duration (samples) = DTMF duration (sec) x 7200 (samples/sec)

Convert value to hex to store in RAM.

No. 11- Tone 1 Angle Increment per Sample **XCR: 0 XRAM Addr: 6F**

No. 12 - Tone 2 Angle Increment per Sample **YCR: 0 YRAM Addr: 6F**

Default: $00

When the host enters Tone Generation/Detection mode (CONF = 80), the transmitter immediately begins sending the dual tone frequencies specified by addresses XRAM 6F and YRAM 6F, with amplitudes specified by XRAM 71 and YRAM 71, respectively. The tones will remain on as long as Tone Generation/Detection mode is specified and the amplitudes are greater than zero. If the host reconfigures directly from Dial/Call Progress mode to Tone Generation/Detection mode after dialing a digit, the RC2424DP/DS will send the dual tone of the last digit dialed until the values in XRAM 71 and YRAM 71 are set to 0.

Frequencies from 0 Hz to 1675 Hz can only be sent when the ORG bit is set, and frequencies from 1925 Hz to 2875 Hz can only be sent when the ORG bit is cleared. 1800 Hz frequency can be sent by setting the GTE bit with GTS=0 and ORG = 0.

To calculate the frequency value to store in RAM, follow the steps below:

1. Find Phase Angle Increment in degrees/sample:
   Angle (degrees/sample) = Frequency (Hz) x (360 degrees/cycle)/7200 (samples/second)
2. Scale result as follows:
   Angle Increment (increment/sample) = Angle (degrees/sample) x (32768/180 degrees)
3. Round off Angle Increment.
4. Convert to hex and store in RAM.

Example: For 1300 Hz,

1. Angle (degrees/sample) = 1300 Hz x 360 (degrees/cycle)/7200 samples/sec = 65 (degrees/sample).
2. Angle Increment (increment/sample) = 65 (degrees/sample) x (32768/180 degrees) = 11832.9 increment/sample.
3. Value to store in RAM = $2E39 (11833).

Note: The ORG bit must be set to generate 1300 Hz tone.

No. 13 - Tone 1 Amplitude **XCR: 0 XRAM Addr: 71**

No. 14 - Tone 2 Amplitude **YCR: 0 YRAM Addr: 71**

Default: $00

These values determine the amplitude of the two tones that are immediately sent when the host enters into Tone Generation/Tone Detection mode. The amplitude of each tone can range from 9.1 dBm down to approximately –50 dBm. The relationship between the output in dBm and the RAM amplitude value for a single tone frequency is shown in Figure 3 for a TLVL (13:4-7) value of 0. Changing TLVL further adjusts the output tone level. Setting one of the two amplitudes to zero selects single tone frequency.

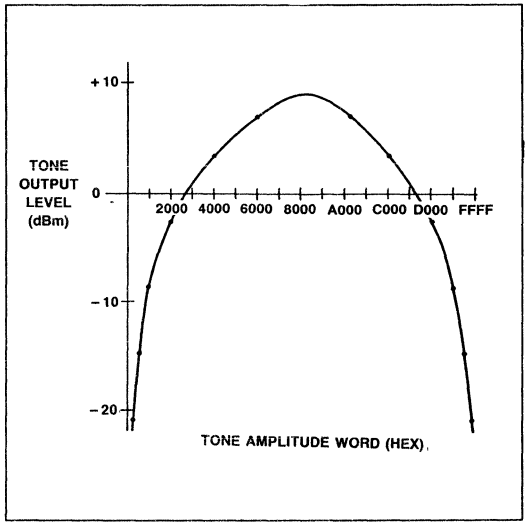


Figure 3. Tone Output Level versus Tone Amplitude

No. 15 - Maximum Samples per Ring Frequency Period **XCR: 0 XRAM Addr: 74**

Default: $0202 (71.4 ms)

This value determines the maximum period of the signal on RD that will be indicated on RI and $\overline{RI}$. The default value of 71.4 ms corresponds to a minimum ring frequency of 14 Hz. This allows proper detection of frequencies as low as 15 Hz.

Formula:

Maximum period samples = 7200 (samples/sec)/minimum ring frequency (Hz)

Convert maximum samples to hex to store in RAM.

No. 16 - Minimum Samples per Ring Frequency Period **YCR: 0 YRAM Addr: 74**

Default: $0064 (13.9 ms)

This value determines the minimum period of the signal on RD that will be indicated on RI and $\overline{RI}$. The default value of 13.9 ms corresponds to a maximum ring frequency of 72 Hz. This allows proper detection of frequencies as high as 68 Hz.

Formula:

Minimum period samples = 7200 (samples/sec)/maximum ring frequency (Hz)

Convert minimum samples to hex to store in RAM.

No. 17 - Real part of Error **XCR: 1 XRAM Addr: 0E**

No. 18 - Imaginary Part of Error **YCR: 1 YRAM Addr: 0E**

The Error Vector is the angle and magnitude difference between the received signal point and the nearest ideal point before the signal has been corrected for rotational error (see Rotated Error, No. 3 and No. 4). Rotational error is caused by phase and frequency differences between the transmitter and receiver carrier signals.

No. 19 - Rotation Angle for Carrier Recovery YCR: 1 YRAM Addr: 10

The Rotation Angle represents correction for both absolute phase differences and continuously changing phase differences.

Formula:

Rotation Angle (degrees) = [(Rotation Angle Word/$FFFF)$_{DEC}$ x 360

Where 0° ≤ Rotated Angle ≤ 360°

No. 20 - Real Rotated Equalizer Output YCR: 1 XRAM Addr: 11
No. 21 - Imaginary Rotated Equalizer Output XCR: 1 YRAM Addr: 11

These values represent the received points after decoding by the decision logic. The points are compared to the ideal points stored in ROM. Figures 4 through 6 show the locations of the ideal baseband points. The machine unit values represent signal scaling for all baseband signals.

No. 22 - Lower Part of Phase Error XCR: 1 XRAM Addr: 12
No. 23 - Upper Part of Phase Error YCR: 1 YRAM Addr: 12

This Phase Error value is the intermediate output of the second order carrier recovery loop.

No. 24 - Upper Part of AGC Gain Word XCR: 1 XRAM Addr: 14
No. 25 - Lower Part of AGC Gain Word YCR: 1 YRAM Addr: 14

This information represents the gain of the AGC amplifier. The upper part of the AGC gain uses the same formula as the Max AGC Gain Word (No. 5). The lower part of the AGC gain can be used for better precision.

Formula:

AGC Gain (dB) = 46.4 - (Upper part of AGC Gain word)$_{DEC}$ x 50/32768

No. 26 - Average Power XCR: 1 XRAM Addr: 1C

This value represents the average received signal power. It can be scaled from engineering units to units of dBm. Use AGC Gain Word (No. 24 and No. 25) to calculate the pre-AGC gain word.

Formula:

Post-AGC Average Power (dBm) = 10 LOG [(Power Word)/(2 x $889)]$_{DEC}$
Pre-AGC Gain Average Power (dBm) = Post AGC Gain Power - AGC Gain

XRAM Address 1C is also used to measure call progress energy detect power in the call detection mode for the Tone A bit.

No. 27 Phase Error XCR: 1 XRAM Addr: 2A

This Phase Error is the input to the second order carrier recovery loop.

No. 26 - Tone Power (TONEA/CALL PROGRESS MODE) XCR: 1 XRAM Addr: 1C
No. 28 - Tone Power (ATBELL, BEL103, or TONEA/TONE MODE) XCR: 1 XRAM Addr: 2C
No. 30 - Tone Power (ATV25, TONEB) XCR: 1 XRAM Addr: 2D
No. 31 - Tone Power (TONEC) XCR: 1 XRAM Addr: 2E

These values represent Post-AGC tone power measurement. Since the tone filters are available only in certain modes, these RAM locations are shared for tone power. Table 2 lists the tone power locations for each mode. See the RC2424DP/DS Data Sheet (Order No. MD543) for more information on the tone filters.

Formula:

Post-AGC Tone Power (dBm) = 10 LOG [(Tone Power Word)/(2 x $889)]$_{DEC}$

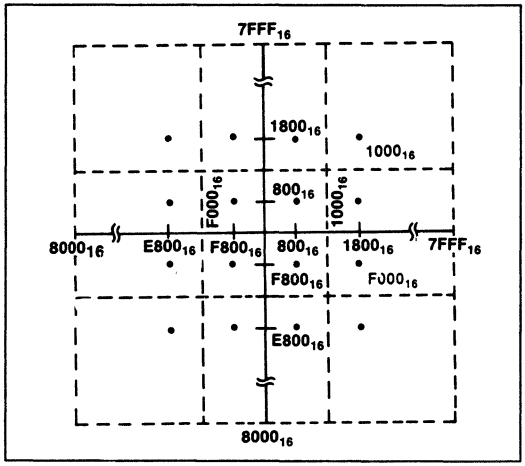


Figure 4. Ideal Points - V.22 bis 2400 bps

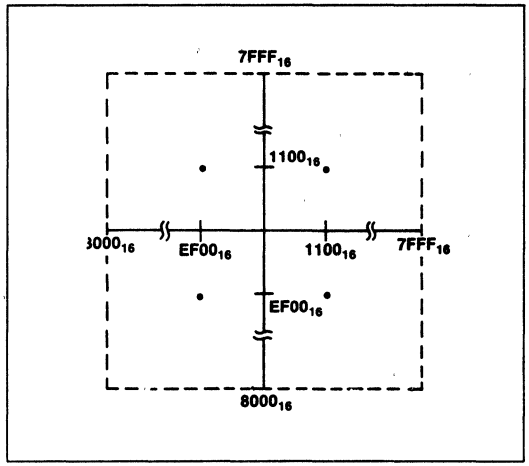


Figure 5. Ideal Points - V.22 A/B, Bell 212A 1200 bps

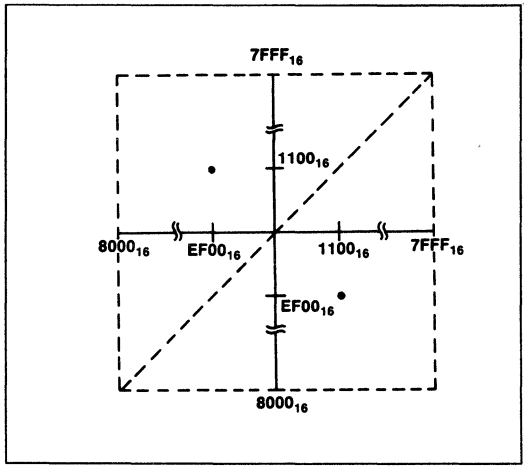


Figure 6. Ideal Points - V.22 A/B 600 bps

No. 29 - Tone Detect Threshold (Call Progress Energy) YCR: 1 YRAM Addr: 2C
No. 32 - Tone Detect Threshold (ATBELL, BEL103, or TONEA) XCR: 1 XRAM Addr: 33
No. 33 - Tone Detect Threshold (ATV25 or TONEB) XCR: 1 XRAM Addr: 34
No. 34 - Tone Detect Threshold (TONEC) XCR: 1 XRAM Addr: 35

Some RAM locations are shared for the tone detect threshold in different modes. Table 2 lists the tone detect threshold locations for each mode. The threshold word is defined as a function of the change in threshold level.

Formula:

New Threshold Word = (Old Threshold Word)$_{DEC}$ EXP (change in dB/10)

Convert value to hex to store in RAM

The host has only limited control of the tone detect threshold with these access codes. To vary the threshold to a greater degree, the host must write to the Max AGC Gain Word (No. 5).

Table 2. Digital Filter Access Codes

Mode	Tone Detect Threshold Address	Tone Power Address	Filter Status Bit	Filter Coefficient	Default Tone Detect (Hz)
Dial/Call Progress	2C	1C	TONEA	1, 2	335-645
	33	2C	ATBELL (ORG=1)	3	2225
	33	2C	BEL103 (ORG=0)	3	1270
	34	2D	ATV25	4	2100
Tone Generation/ Detection	33	2C	TONEA	1	1300
	34	2D	TONEB	2	390
	35	2E	TONEC	3	980 (ORG=0) 1650 (ORG=1)
Handshake	33	2C	ATBELL (ORG=1)	3	2225
	33	2C	BEL103 (ORG=0)	3	1270
	34	2D	ATV25	4	2100

Note: The host should set/clear the ORG bit before entering into Tone Generation/Detection mode.

No. 35 - Zero Crossing Detector XCR: 1 XRAM Addr: 38

The zero crossing detector is always available. The detector can measure tone frequencies between 100 Hz and 3000 Hz, and increments for both positive and negative zero crossings. To use the detector, the host writes $00 to the detector at location 38, delays for some amount of time, and then reads the value at location 38. The value read is ±1 crossing of the actual value. Note that the zero crossing detector will increment any time the received signal crosses zero.

No 36 - Eye Quality Monitor Output XCR: 1 XRAM Addr: 52

The error vector formed by the decision logic can be used to indicate relative signal quality. As signal quality deteriorates, the average error vector increases in magnitude. By calculating the magnitude of the error vector and filtering the results, a number inversely proportional to signal quality is derived. This number is called the Eye Quality Monitor (EQM). Because of the filter time constant, EQM should be allowed to stabilize for approximately 700 baud times following RLSD going active.

The EQM value is the filtered squared magnitude of the error vector and represents the average signal power contained in the error component. The power is directly proportional to the probability of errors occurring in the received data and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of CCITT Recommendation V.24 or circuit CG of the RS-232-C standard) by comparing the EQM value against experimentally determined criteria (bit error rate curves). Figure 7 illustrates the relationship of the EQM number to an eye pattern created by a four-point signal structure (e.g., Bell 212A/1200 bps) in the presence of high level white noise. The EQM value is proportional to the square of the radius of the disk around any ideal point. The radius increases when signal-to-noise ratio (SNR) decreases. As the radius approaches the ideal points' boundary values, the bit error rate (BER) increases. Curves of BER as a function of the SNR are used to establish a criteria for determining the acceptability of EQM values. Therefore, from an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the modem to fall back to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbances present on the line and with the various configurations. A given magnitude of EQM in V.22 bis/2400 does not represent the same BER as in V.22/1200. The former configuration has 16 points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given level of noise or jitter. Also, the type of line disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Since EQM is dependent upon the signal structure of the modulation being used and the type of line disturbance, EQM must be determined empirically in each application.

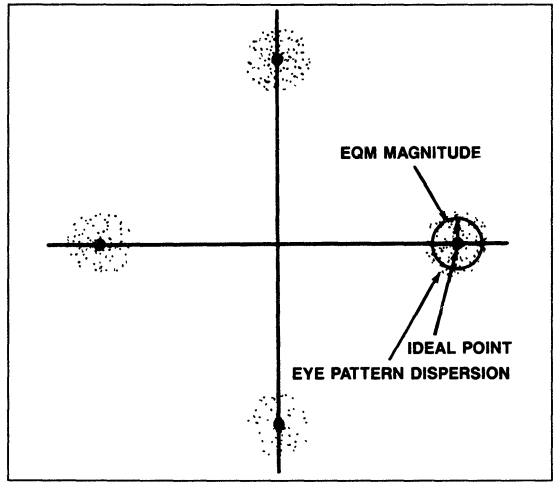


Figure 7. Relationship of EQM to Eye Pattern

Nos. 37 - 51 Digital Filter Coefficients **YCR: 1 YRAM Addr: (See Table 1)**

The digital filters in all modes are fully programmable Single Biquad IIR filters, except for the call progress monitor - Tone A in Dial/Call Progress mode which is a Dual Biquad IIR filter. All of the biquads follow the following transfer function:

$$H(z) = 2\,(\alpha_0 + \alpha_1 Z^{-1} + \alpha_2 Z^{-2})/(1 - 2\,\beta_1 Z^{-1} \beta_2 Z^{-2})$$

Table 2 shows which filter coefficients correspond to the tone detect status bits in each mode. The modem will load default values each time the host changes modes. Table 3 shows calculate coefficient values for default tone detect filters.

Table 3. Calculated Tone Detect Values

Frequency Detected (Hz)	Coefficient Values				
	α_0	α_1	α_2	β_1	β_2
2225	0666	02A6	0418	D28A	C289
2100	0666	03B6	0418	DF89	C289
1650	044E	FD17	02C1	105F	C28A
1300	05D1	FA77	03B9	3502	C289
1270	05D1	FA72	05D1	37F8	C289
980	0572	FC52	037C	524B	C28A
390	06EC	F4F3	046E	763D	C28A

Rockwell

RC2424DP/DS HDLC Features

INTRODUCTION

The HDLC (High Level Data Link Control) protocol is a standard procedure used for data communications. SDLC (Synchronous Data Link Control) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The RC2424DP/DS uses the SDLC protocol but it is referred to as HDLC to avoid confusion.

HDLC FRAMES

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving station to synchronize with each other. This format is shown in Figure 1. Flags and the frame check sequence are distinguished from the other fields by status bits in the RC2424DP/DS Interface memory.

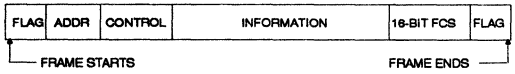


Figure 1. HDLC Frame

FLAGS

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7E). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as "zero-sharing". The zero-sharing bit pattern is 011111101111110.

ADDRESS FIELD

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the "basic" format.

For the "extended" format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

CONTROL FIELD

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format
2. Supervisory Format
3. Unnumbered Format

This field is normally 8 bits in length. Certain protocols allow for an extended control field of 16 bits in length.

INFORMATION FIELD

The RC2424DP/DS does not distinguish between the address field, the control field, or the information field. The information field does not have a set length; however, this field follows the SDLC protocol in being in the format of eight bit bytes.

ZERO INSERTION

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

The RC2424DP/DS transmitter always performs zero insertion when in HDLC mode.

ZERO DELETION

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (i.e., at least seven ones with no zero insertion) or a flag (i.e., 01111110). The sixth one is, therefore, not removed.

The RC2424DP/DS receiver always performs zero deletion when in HDLC mode.

FRAME CHECK SEQUENCE

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

The FCS computation is done on all fields within the frame but does not include the flags. Cyclic Redundancy Check (CRC) is the method used. The polynomial is specified in SDLC and X.25 as follows:

$$x^{16} + x^{12} + x^5 + 1$$

The polynomial is implemented as shown in Figure 2.

The Frame Check Sequence is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS register is transmitted as the 16-bit FCS. The FCS is transmitted with the highest order bit (x^{15}) first.

FRAME ABORTION, FRAME IDLE, AND TIME FILL

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

Interframe time fill is accomplished by transmitting continuous flags. Therefore, the transmitter must be capable of sending multiple flags to maintain the active state in the receiver if any time fill is required.

IMPLEMENTATION

A representation of the HDLC process is shown in Figure 3. The events are numbered in order of occurrence from one to four.

1. The beginning flag is transmitted. The receiver sees the flag and now becomes aligned with the transmitter. Both the receive and the transmitter FCS registers are preset to FFFF (hex).
2. The information field is transmitted. The data is also run through the FCS register before zero insertion. At the receive end, after the zero deletion algorithm, the data is presented to the user and then run through the FCS register.
3. The FCS is inverted and then transmitted. The transmitted FCS is passed through the receiver's FCS register. The shift register will contain 1111000010111000 if the frame has been received correctly.
4. The ending flag is transmitted.

TRANSMITTER AND RECEIVER IMPLEMENTATION

In order to use HDLC in the RC2424DP/DS, the host processor must:

1. Set up the modem configuration.
2. Set the transmitter parallel data mode bit (TPDM). Received data is always available in parallel.
3. Switch into synchronous mode by resetting the ASYNC bit, if not already in synchronous mode.
4. Set the SYNCMD bits for SDLC/HDLC mode (01).

Note: The user should enter into SDLC/HDLC mode only after the handshake is complete.

HDLC transmission cannot be performed using the serial interface. The format of the data input to the RC2424DP/DS is in groups of eight bit bytes. As in the normal synchronous parallel data mode, the least significant bit of the byte is transmitted first.

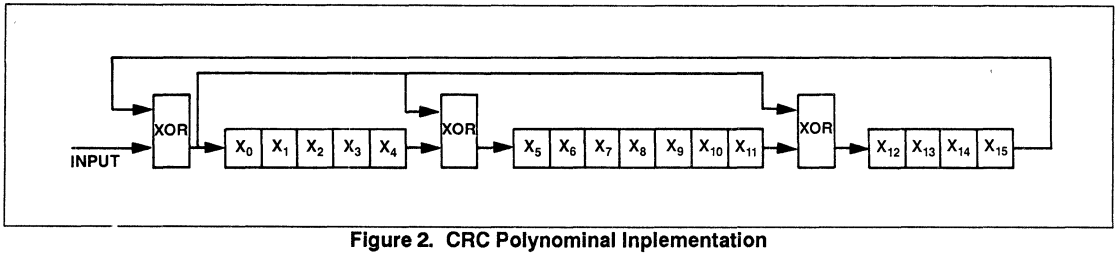


Figure 2. CRC Polynominal Inplementation

TRANSMISSION AND RECEPTION RATE

The HDLC as implemented in the RC2424DP/DS can be used in all of the transmitter and receiver data modes, except for all FSK modes.

FLAG TRANSMISSION AND RECEPTION

Once in HDLC mode, the modem will send continuous flags with no zero sharing (i.e., 0111111001111..) until the user loads data into the transmit data buffer TBUFFER (register 10). Thus, the transmitter defaults to transmitting time-fill and keeps the receiving link station active. The status bit FLAGS (0F:0) indicates that the modem is transmitting the flag sequence.

When in HDLC mode, the RC2424DP/DS receiver continually searches for the flag data pattern. When one or more flags are detected, the interface memory status bit SYNCD (0F:1) is set. The flags themselves are not presented to the host through the receiver data buffer RBUFFER (register 00).

The RC2424DP/DS also has the capability to detect consecutive flags with zero-sharing.

INFORMATION FIELD TRANSMISSION AND RECEPTION

The host must load the data into TBUFFER and then wait for the transmit data buffer available bit TDBE (1E:3) to be set by the modem before loading in the next byte of data. If the next byte is not loaded into TBUFFER within the next eight bit times, the modem interprets this as the end of a frame and will send the CRC sequence.

In the receiver, data between flags is passed to the user through the RBUFFER register by the use of the handshaking bit RDBF (1E:0). The user must wait for RDBF to be set by the modem and then take the data. If the host does not read the data within eight bit times, the data in RBUFFER will be overwritten by the next byte and the Overrun Error bit (0E:3) will be set. The flag sequence and abort/idle sequence are not presented to the user. The receiver determines where the FCS field is by detecting the ending flag. There is at least a 16-bit time delay in the reception of data.

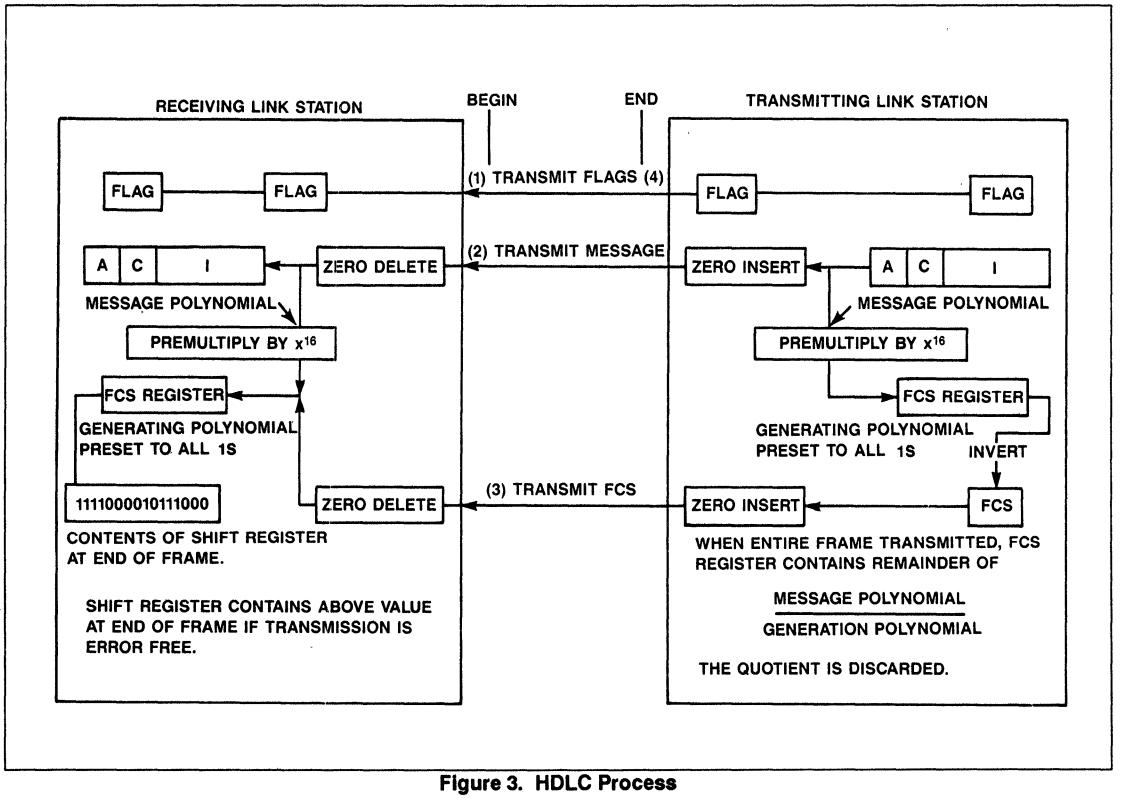


Figure 3. HDLC Process

FCS AND ENDING FLAG TRANSMISSION AND RECEPTION

Following the detection of no new data loaded into the TBUFFER register within the next eight bit times, the modem automatically sends the FCS and ending flag. Status bit CRCS (0A:0) in the interface memory is set just before the highest order bit (x^{15}) is sent to indicate that the FCS is being transmitted. Once the host sees this bit set, the first byte of the next frame can be loaded. In this case, the ending flag serves as the beginning flag for the next frame. The CRCS bit is reset when the ending flag is transmitted. At the same time, the FLAGS bit is set.

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the receiver checks the data in the FCS register. If the FCS register remainder is correct, the PE (0E:5) bit in the interface memory is left a zero. If the remainder is incorrect, the PE bit is set. The FCS field is also passed to the host, in case the host wishes to do his own CRC checking. The receiver will set the SYNCD bit and the PE bit (if the modem detected a frame with a bad CRC) after sending the FCS to the host. The modem does not change the PE bit until the end of the next frame when a correct or incorrect frame is determined. However, the user can reset this bit anytime. The RC2424DP/DS presets the FCS register to all ones after one or more flags are received.

After the FCS transmission (immediately following bit x^0), one flag is sent to signify the end of the current frame and the beginning of the next frame. After the final zero in a flag is transmitted, the modem looks to see if the user has loaded new data into TBUFFER. If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag between frames is desired, the host must wait N-1 multiples of eight bit times after FLAGS is set by the modem to load new data into TBUFFER, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAGS is set by the modem.

ABORT/IDLE SEQUENCE TRANSMISSION AND RECEPTION

An abort/idle sequence can be sent by the host setting the bit MHLD (07:0) in the interface memory. This stops any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. After the setting of MHLD is detected, the modem first completes the transmission of the current byte of data. Immediately after this transmission, the modem sends seven consecutive ones. After these seven bit times, if MHLD is still set, the modem continues to send ones until MHLD is reset. To discontinue this sequence, MHLD must be reset. Then, if no new data is loaded into TBUFFER, continuous flags are sent. If new data is loaded into TBUFFER, the modem sends a beginning flag and then the data in TBUFFER.

The RC2424DP/DS receiver not only continually searches for flags, but also continually searches for an abort/idle sequence. When the receive modem encounters this data pattern, it sets the FE bit (0E:4). After the modem sets the FE bit, it does not change the bit until the end of the next frame when the abort/idle sequence is again determined. However, the user can reset the FE bit anytime. Then, if an abort/idle sequence is detected during the next frame, the modem will again set the FE bit. The reception of data following the abort/idle sequence is treated as invalid data and is not presented to the user. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. Remember, the abort/idle sequence is not output through the RBUFFER register.

AN EXAMPLE IMPLEMENTATION

Refer to RC2424DP/DS data sheet (Order No. MD53) for a description of the bits associated with the HDLC functions.

Transmitter Example

1. After handshake, reset the ASYNC bit. Then set the SYNCMD bits for SDLC/HDLC and set RTS.
2. The modem starts transmitting flags immediately and continues with flags until the first byte of data is loaded into TBUFFER.
3. Place the first byte of data into TBUFFER. The modem finishes transmitting the current flag followed by this byte of data.
4. As soon as TDBE is set, load in the next byte of data. This must occur within eight bit times of TDBE being set.
5. After all information but the last byte is given to the modem, load in the last byte of data in the frame as in step 4.
6. Wait until CRCS is reset to load in the first byte of the next frame. The modem follows the last byte of the current frame with the 16-bit FCS and a flag.
7. Repeat steps 4 through 6 for all frames to be transmitted.

Receiver Example

The steps to perform a typical HDLC reception are:

1. After handshake, reset the ASYNC bit. Then monitor, through interrupts, the RDBF, OE, SYNCD, PE and FE bits in the interface memory.
2. Wait for an interrupt. If it is caused by the modem setting RDBF (RDBIA is also set by the modem), read the data in RBUFFER. The modem will set the NEWS and NSIA bits if any of the other bits caused the interrupt. An interrupt caused by OE indicates that RBUFFER was loaded with new data before the host read the old data. SYNCD indicates that the modem is receiving flags. PE indicates that the FCS had an incorrect CRC. FE indicates that an abort/idle sequence is detected, and the frame that was aborted is invalid. The RC2424DP/DS does not set the SYNCD bit or the PE bit in this case since no FCS checking is done.
3. Continue waiting for interrupts and take appropriate action when the interrupts are received.

Rockwell

Data Access Arrangement (DAA) Design for R1496MM, R9696DP, and R144DP

INTRODUCTION

This application note provides an example of a data access arrangement (DAA) suitable for use with an R1496MM, R9696DP, or R144DP modem. A description of the DAA, the schematic, parts list, and layout are included. A 4-to-2 wire hybrid schematic, parts list, and layout are also provided.

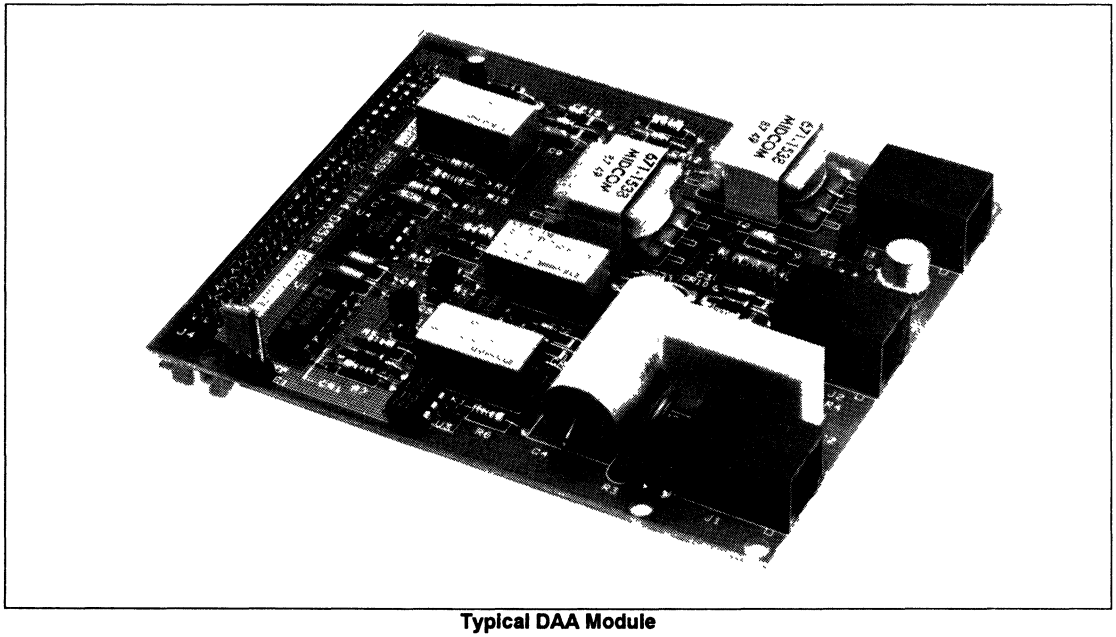
NOTE:

This interface is designed for use in the United States where F.C.C. Part 68 approval is necessary. The DAA interface provided in this application note has not been F.C.C. Part 68 certified. Rockwell International, therefore, assumes no responsibility for the use of the information provided in this application note.

FEATURES

- Supports 2-wire dial-up as well as 4-wire leased lines
- Can be used with V.32 configurations where minimal harmonic distortion is critical.
- Pulse dialing capability using the Off-Hook relay
- Ring detection provided
  - Supports 2-wire and 4-wire leased lines
- Supports a 4-wire leased line environment with 2-wire dial backup
- Automatic connection/disconnection of telephone handset
- Small board area required: 100 mm x 120 mm (3.94 in. x 4.73 in.) approximately

4



Typical DAA Module

DAA INTERFACE DESCRIPTION

The DAA interface signals are shown in Figure 1. Figure 1 shows an example of how the R1496MM can be interfaced to the DAA for a 4-wire leased-line/2-wire dial backup application. A schematic of the DAA is shown in Figure 2. The digital and analog interface signals are described in Tables 1 and 2, respectively.

The DAA is controlled and monitored via five digital interface signals. Two signals interface directly with the modem and three signals originate from a parallel port of either a microprocessor parallel interface adapter peripheral or a microcontroller.

TXA, RXA, $\overline{\text{OHRC}}$, and $\overline{\text{RD}}$ are direct connections from the modem to the DAA. $\overline{\text{PD}}$, $\overline{\text{4W}}$, and $\overline{\text{LL}}$ must be configured using a microprocessor peripheral device or by switches. For 4-wire leased line configuration, $\overline{\text{OH}}$ and $\overline{\text{PD}}$ should be at 5 volts and $\overline{\text{4W}}$ and $\overline{\text{LL}}$ should be at ground. J3 is then the active jack. For 2-wire dial configuration, $\overline{\text{OH}}$ should at ground ($\overline{\text{PD}}$ is only low during pulse dialing) and $\overline{\text{PD}}$, $\overline{\text{LL}}$, and $\overline{\text{4W}}$ should be at 5 volts. J1 is then the active jack.

$\overline{\text{OHRC}}$ can be controlled by setting the RA bit in the interface memory of Chip 0 of the R1496MM. $\overline{\text{RD}}$ can be monitored by reading the $\overline{\text{RI}}$ bit in the interface memory of Chip 2 or by monitoring the $\overline{\text{RI}}$ pin.

Impedance Specifications

Table 3 lists the on-hook and off-hook impedance specifications for the DAA J1 jack.

DAA Power Requirements

Table 4 specifies the power requirements for two different DAA configurations.

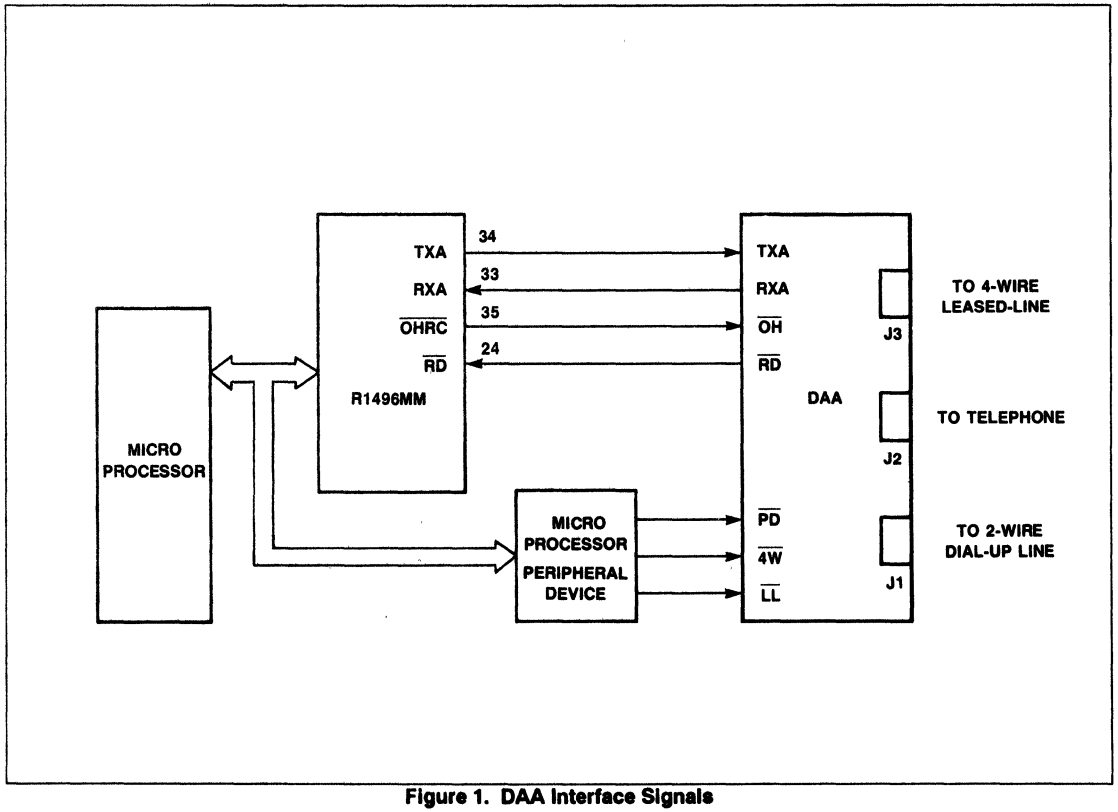


Figure 1. DAA Interface Signals

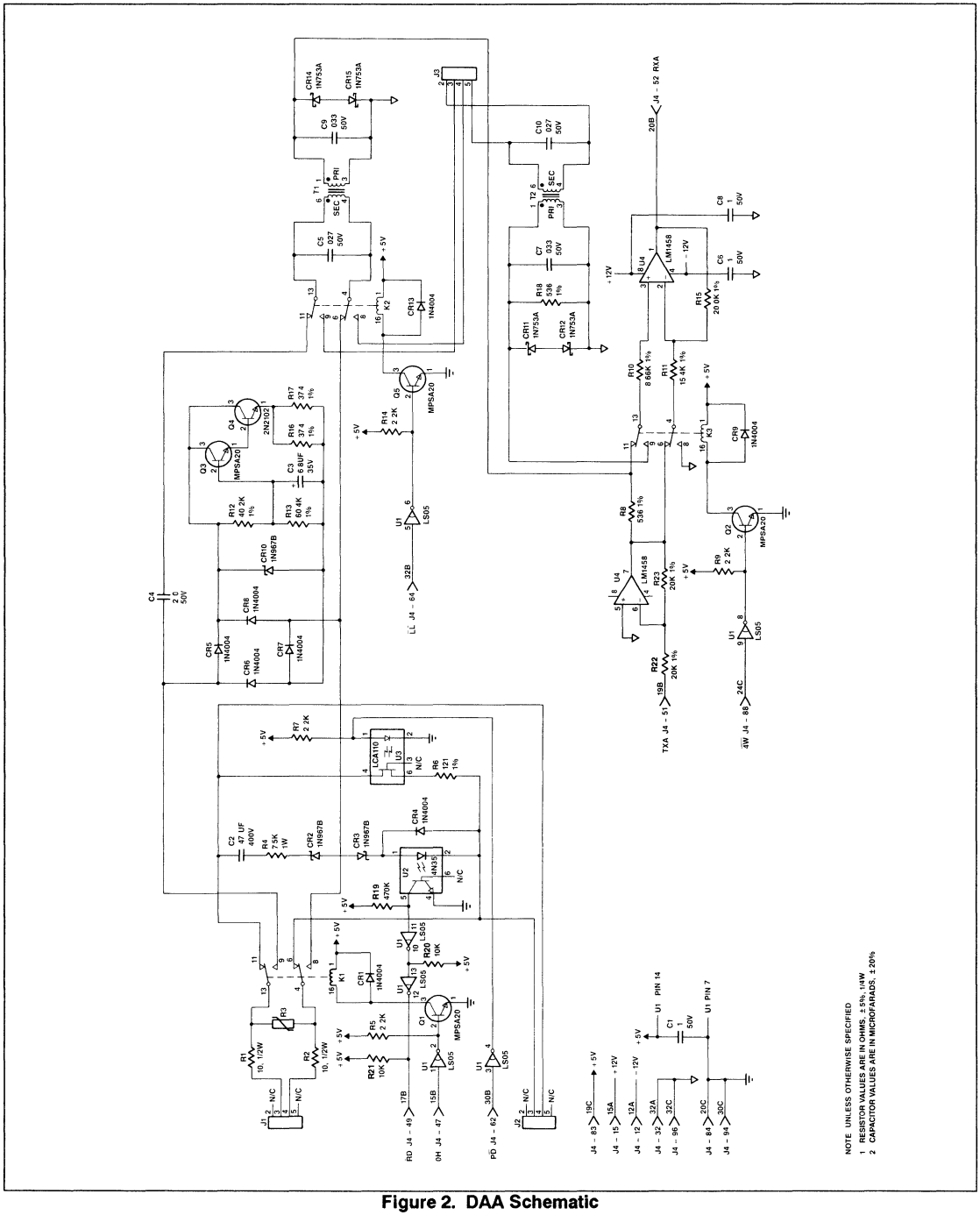


Figure 2. DAA Schematic

Table 1. DAA Digital Interface Signal Description

Signal	Name	Description
$\overline{LL}$	Leased-Line	$\overline{LL}$ is an active low input which configures the DAA for a leased-line application. J3 is then the active jack used for the leased line connection. When $\overline{LL}$ is high, the DAA is configured for a dial-up application and J1 is the active jack. The typical delay from $\overline{LL}$ active to the close of the leased line relay is 3 ms. $\overline{LL}$ is an input to a 74LS05.
$\overline{OH}$	Off-Hook	$\overline{OH}$ is an active low input which closes the off-hook relay connecting the dial-up line to the DAA circuitry. $\overline{OH}$ is used in conjunction with $\overline{PD}$ to pulse dial a telephone number. The typical delay from $\overline{OH}$ active to the close of the off-hook relay is 3 ms. $\overline{OH}$ is an input to a 74LS05.
$\overline{PD}$	Pulse Dial	$\overline{PD}$ is an active low input which should be active when the user wants to use $\overline{OH}$ to pulse dial a a telephone number. When $\overline{PD}$ is active, the $\overline{RD}$ signal is prevented from going active. $\overline{PD}$ should be high when not pulse dialing. $\overline{PD}$ is an input to a 74LS05.
$\overline{RD}$	Ring Detector	$\overline{RD}$ is an active low output which signals when a ringing signal is present on the line. $\overline{RD}$ is a square wave output which follows the ringing signal which appears across Tip and Ring on J1. $\overline{RD}$ is an output from a 74LS05 which is pulled-up to 5V through a 10K Ω resistor.
$\overline{4W}$	4-Wire	$\overline{4W}$ is an active low input which configures J3 as a 4-wire interface. When $\overline{4W}$ is high, J3 is configured as a 2-wire interface. The typical delay from $\overline{4W}$ active to the close of $\overline{4W}$ relay is 3 ms. $\overline{4W}$ is an input to a 74LS05.

Table 2. DAA Analog Interface Signal Description

Signal	Name	Description
TXA	Transmit Analog	TXA is the Transmitted Analog signal input to the DAA. Its input impedance is 20K Ω. The gain from TXA to Tip/Ring of J1 and J3 is -6 dB (assuming there is a 600 Ω load on J1 or J3). No signal level limiter is included in the transmit path. The user must either attenuate or amplify the TXA output of the modem so that the signal level at J1/J3 complies with FCC Part 68 (or other appropriate) specification.
RXA	Receive Analog	RXA is the Received Analog signal output of the DAA for the. Its output impedance is that of a 1458 operational amplifier.
J1	Dial-up Jack	Pins 3 and 4 are Tip and Ring, respectively, for the 2-wire dial-up jack. This jack is active when the $\overline{OH}$ input is low.
J2	Telephone Jack	Pins 4 and 3 are Tip and Ring, respectively, for connection of a telephone to the 2-wire telephone line. This jack is active when the $\overline{OH}$ input is high.
J3	Leased-line Jack	When the DAA is configured for 2-wire leased-line pins 3 and 4 are Tip and Ring, respectively, for the transmit and receive signal paths. When the DAA is configured for 4-wire leased-line, pins 3 and 4 are Tip and Ring, respectively, for the transmit path, and pins 5 and 2 are Tip and Ring, respectively, for the receive path.

Transformer Specifications

The electrical and mechanical specifications of the transformer shown in the DAA are given below. Table 5 provides the electrical specification and Figure 3 shows the mechanical specifications.

The transformer equivalent circuit is shown in Figure 4. Equivalent circuit parameters are listed in Table 6.

DAA DESIGN CONSIDERATIONS

Hazardous Voltage Protection

Lightning induced surge voltages and other hazardous voltages are limited to 7 volts peak between the secondary leads of the coupling transformers T1 and T2. The isolation between the relay contacts and coils provides the protection of the telephone line from hazardous voltages appearing on any control lead.

Table 3. On-hook and Off-hook Impedance

Parameter	Specification
On-hook DC	Greater than 10M Ω for DC voltages up to 100 volts measured between Tip and Ring and between either Tip or Ring and signal ground.
On-hook AC	Less than 40K Ω (15.3 Hz minimum) measured between Tip and Ring.
Off-hook DC	Meets the DOC and EIA standards.
Off-hook AC	600 Ω nominal when measured between Tip and Ring.

Table 4. DAA Power Requirements

	Current (Typical) @ 25°C	
Voltage	**2-Wire Dial-Up**	**4-Wire Leased-Line**
+5V	50 mA	85 mA
+12V	3 mA	3 mA
–12V	20 mA	20 mA

Note:
1. 2-wire dial-up/leased-line uses only one of the three relays.
2. 4-wire leased-line uses two relays.
3. Ripple ≤100 mV peak-to-peak .

DAA MODULE CONSTRUCTION

Table 7 lists the components required to build the DAA module.

Figures 5 through 8 provide the silkscreen and layout of the DAA circuit board. The layouts show the correct routing of signals and component placement to minimize noise, crosstalk, and other problems which occur when analog and digital circuitry are close to each another.

Table 5. Transformer Electrical Specification

Parameter	Values
D.C. Resistance	45 Ω ±10% each winding
D.C. Unbalance	0 mADC max.
Dielectric	1500 VAC between windings (To meet or exceed FCC Part 68 requirements)
Distortion	300 Hz +4.7 dBm: –71 dB max.
Frequency Response	±0.2 dB, 300 Hz-3000 Hz
Impedance	Primary: 600 Ω Secondary: 530 Ω ref.
Insertion Loss	0.85 dB max., 1 kHz
Longitudinal Balance	60 dB min., 200 Hz -1000 Hz 40 dB min., 1 kHz-4 kHz
Return Loss	26 dB min., 300 Hz-3000 Hz R_L = 530 Ω
Turns Ratio	1:1 ±2%

Table 6. Transformer Parameters

Ref.	Parameter	Value	Units
1	Network		
2	Network Resistance	0	Ω
3	Network Capacitance	0	F
4	Network Inductance	0	H
5	Primary Capacitance	80	pF
6	Primary DCR	45	Ω
7	Primary Inductance	4.2	H
8	Ind. Ratio	2.215	200:1 kHz
9	Parametric Resistance.	25.2	Ω
10	Leakage Inductance	2.62	mH
11	Turns Ratio	1	PRI:SEC
12	Secondry DCR	45	Ω
13	Secondary Para. Capacitance	90	pF
14	Secondary Serial Capacitance	0	F
15	Load Resistance	530	Ω
16	Load Capacitance.	0	F
17	Reference Resistance	600	Ω
18	Reference Capacitance	0	F
19	Low Frequency	300	Hz
20	High Frequency	3000	Hz
21	Reference Frequency	1000	Hz

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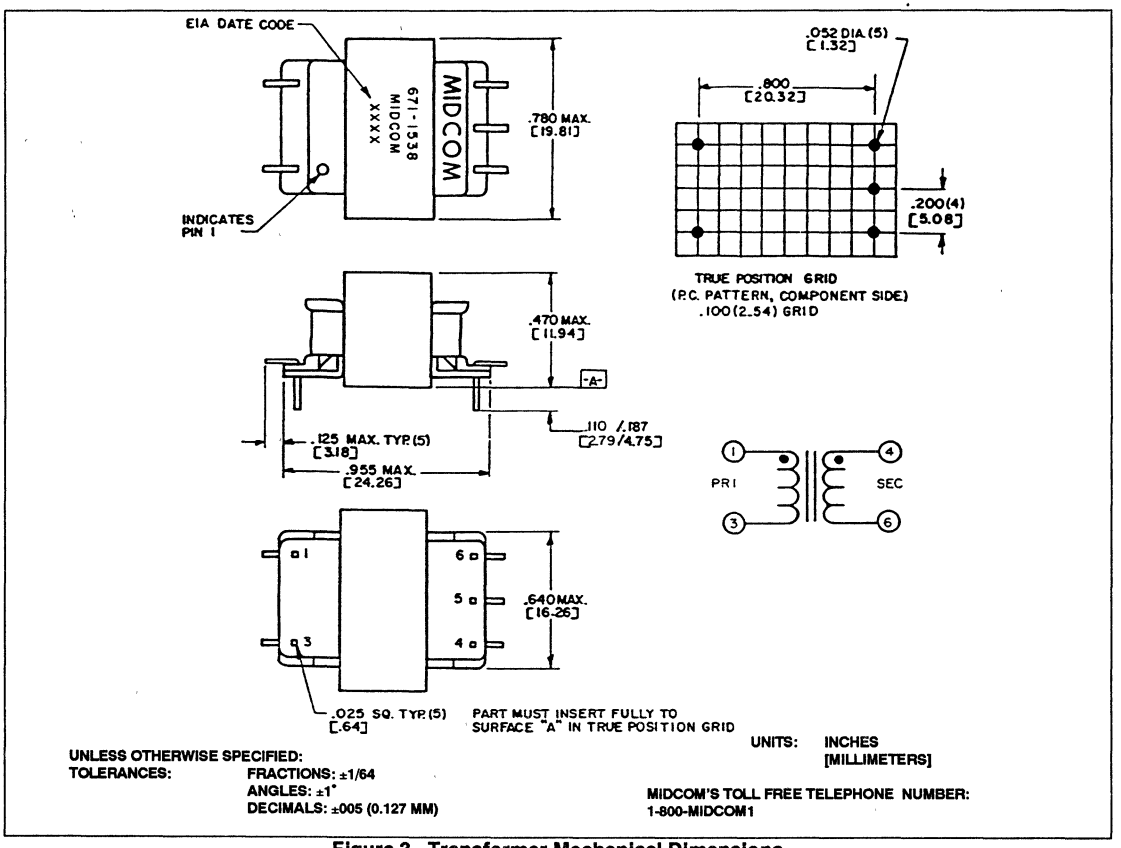


Figure 3. Transformer Mechanical Dimensions

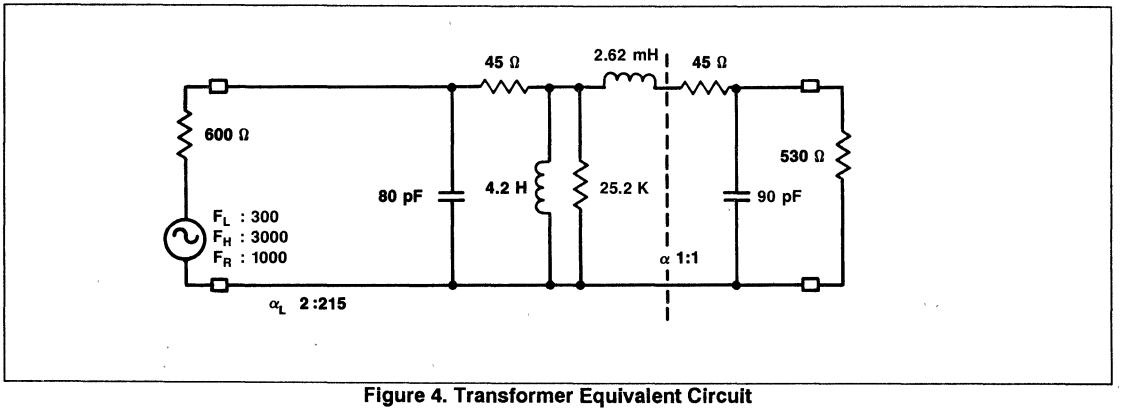


Figure 4. Transformer Equivalent Circuit

Table 7. DAA Module Parts List

Designation	Quantity	Type	Description
C1, C6, C8	3	Capacitor	.1 µF ± 20% 50V, Z5U Ceramic
C2	1	Capacitor	.47 µF ± 20% 400V, Metalized poly.
C3	1	Capacitor	6.8 µF ± 20% 35V, Alum. electro.
C4	1	Capacitor	2 µF ± 20% 50V, Poly
C5, C10	2	Capacitor	.027 µF ± 5% 50V, Ceramic
C7, C9	2	Capacitor	.033 µF ± 5% 50V, Ceramic
CR1, CR4-CR9, CR13	8	Diode	1N4004
CR2, CR3, CR10	3	Zener diode	1N967B
CR11, CR12, CR14, CR15	4	Zener diode	1N753A
J1, J2, J3	3	Telephone jack	RJ11C, 6-position, R/A
J4	1	Connector	DIN, 96-pin, plug
K1, K2, K3	3	Relay	DPDT, 5V, 2 Form C
Q1, Q2, Q3, Q5	4	Transistor	MPSA20
Q4	1	Transistor	2N2102 (T0-5 case)
R1, R2	2	Resistor	10 Ω ± 5% 1/2W
R3	1	Varistor	4.5A
R4	1	Resistor	7.5K Ω ± 5% 1W
R5, R7, R9, R14	4	Resistor	2.2K Ω ± 5% 1/4W
R6	1	Resistor	121 Ω ± 1% 1/4W
R8, R18	2	Resistor	536 Ω ± 1% 1/4W
R10	1	Resistor	8.66K Ω ± 1% 1/4W
R11	1	Resistor	15.4K Ω ± 1% 1/4W
R12	1	Resistor	40.2K Ω ± 1% 1/4W
R13	1	Resistor	60.4K Ω ± 1% 1/4W
R15, R22, R23	3	Resistor	20.0K Ω ± 1% 1/4W
R16, R17	2	Resistor	37.4 Ω ± 1% 1/4W
R19	1	Resistor	470K Ω ± 1% 1/4W
R20, R21	2	Resistor	10K Ω ± 1% 1/4W
T1, T2	2	Transformer	Midcom # 671-1538
U1	1	IC	74LS05, Open-collector hex inverter
U2	1	IC	4N35, Photo coupled isolator
U3	1	Opto relay	LCA110
U4	1	IC	LM1458 Dual operational amplifier

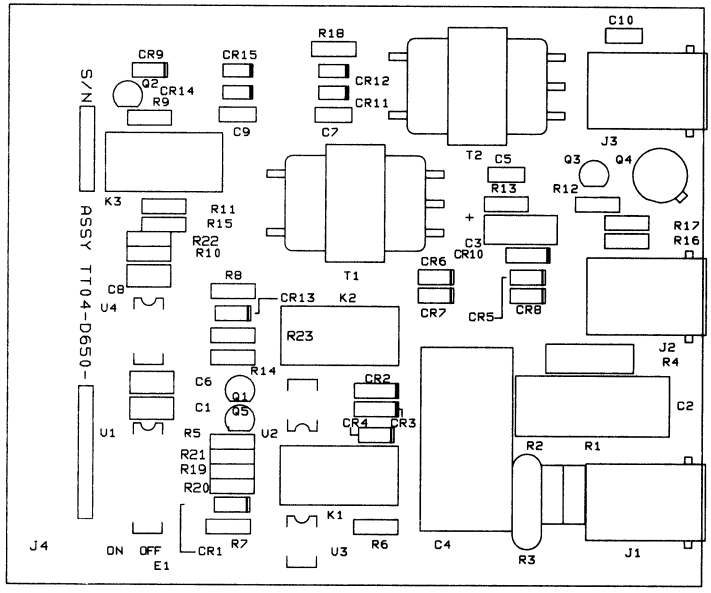


Figure 5. DAA Module Silkscreen

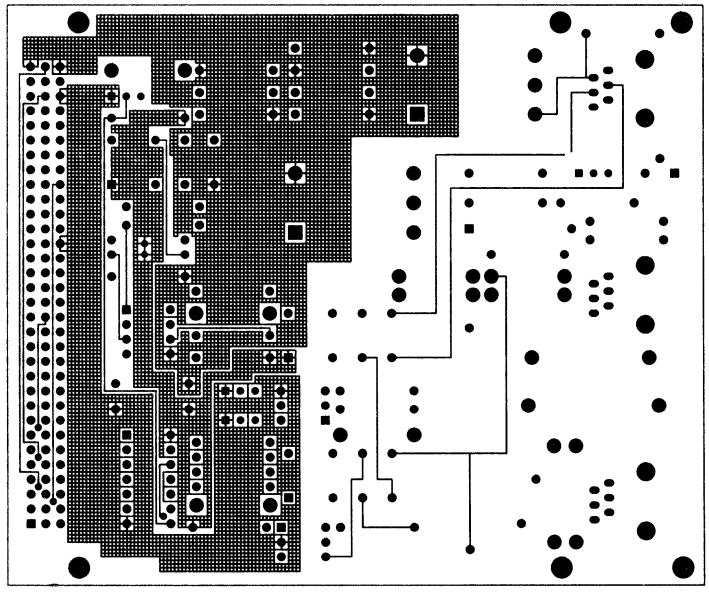


Figure 6. DAA Module Component Side Layout

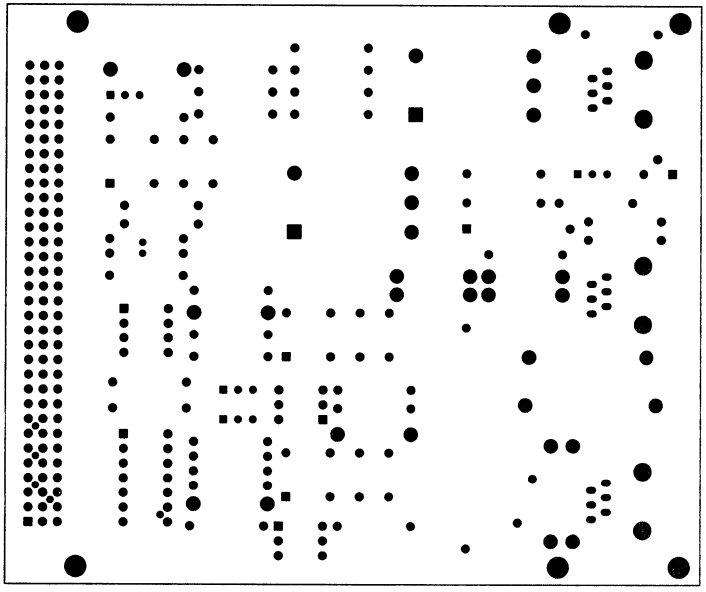


Figure 7. DAA Module Padmaster Layout

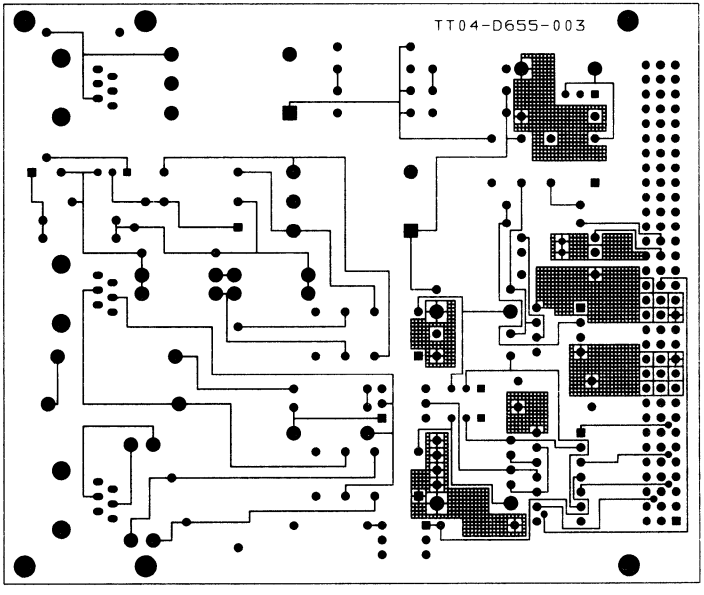


Figure 8. DAA Module Solder Side Layout

HYBRID INTERFACE DESCRIPTION

Hybrid Transformer Requirements

The hybrid interface signals are shown in Figure 9. A schematic of the hybrid circuit is shown in Figure 10.

HYBRID DESIGN CONSIDERATIONS

The specifications for hybrid transformer is the same as for the DAA (see Table 5 and Figures 3 and 4).

Hybrid Power Requirements

Table 8 specifies the hybrid power requirements.

Table 8. Hybrid Power Requirements

Voltage	Current (Typical) @ @25°C
+12V	2.5 mA
–12V	2.5 mA
Note: Input voltage ripple ≤100 mV peak-to-peak.	

HYBRID MODULE CONSTRUCTION

Table 9 lists the components required to build the hybrid module.

Figures 11 through 14 provide the silkscreen and layout of the hybrid circuit board.

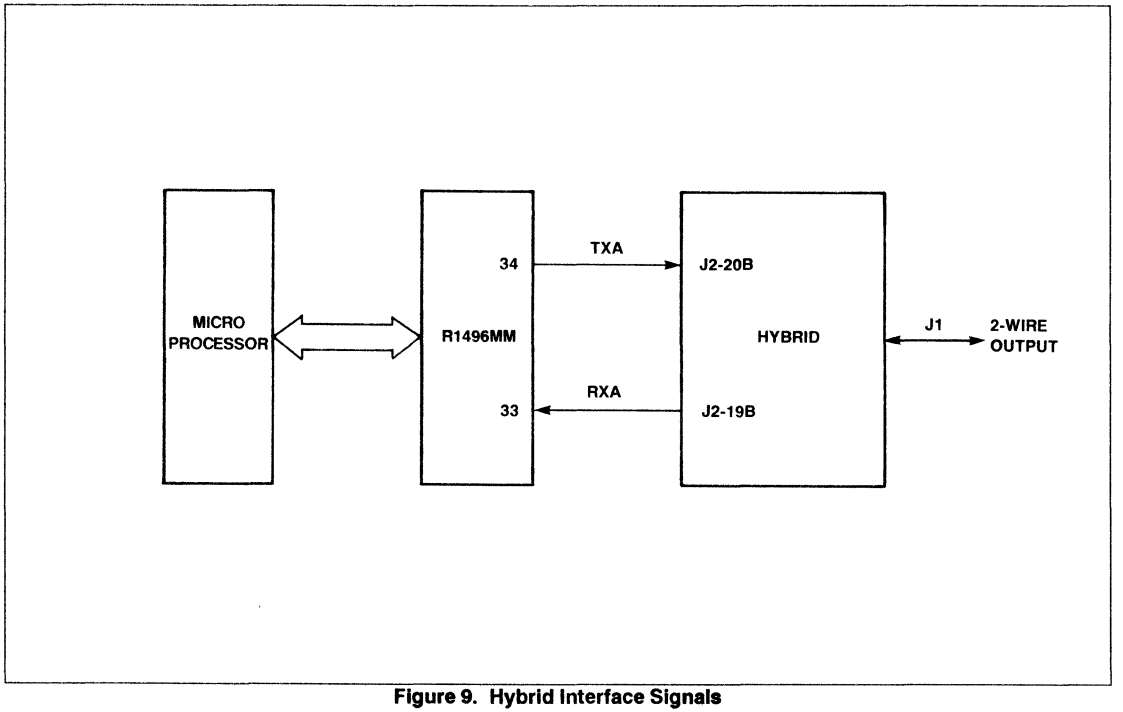
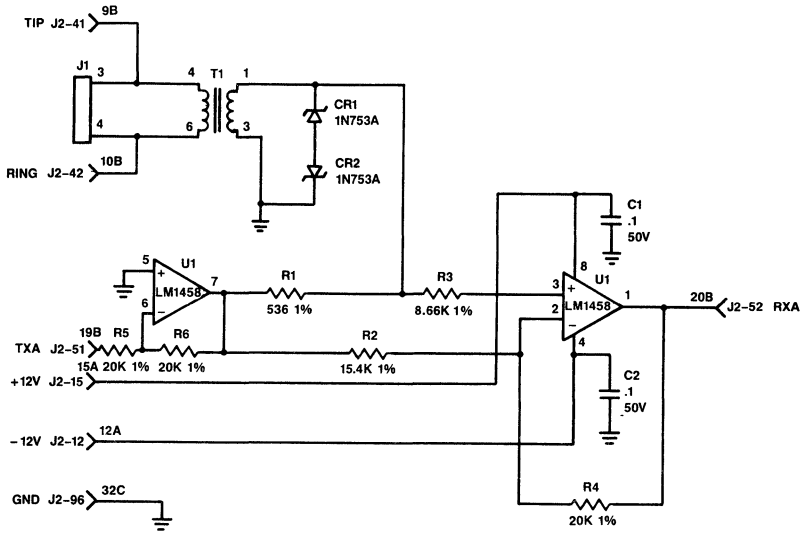


Figure 9. Hybrid Interface Signals



NOTE: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS, 1/4W
2. CAPACITOR VALUES ARE IN MICROFARADS, ±20%

Figure 10. Hybrid Schematic

Table 9. Hybrid Parts List

Designation	Quantity	Type	Description
C1,C2	2	Capacitor	0.1 μF ±20% 50V, Z5U Ceramic
CR1,CR2	2	Zener diode	1N753A
J1	1	Telephone jack	RJ11C, 6-position, R/A
J2	1	Connector	DIN, 96-pin, plug
R1	1	Resistor	536 Ω ±1% 1/4W
R2	1	Resistor	15.4K Ω ±1% 1/4W
R3	1	Resistor	8.66K Ω ±1% 1/4W
R4,R5,R6	3	Resistor	20.0K Ω ±1% 1/4W
T1	1	Transformer	Midcom #671-1538
U1	1	IC	LM1458,Dual operational amplifier

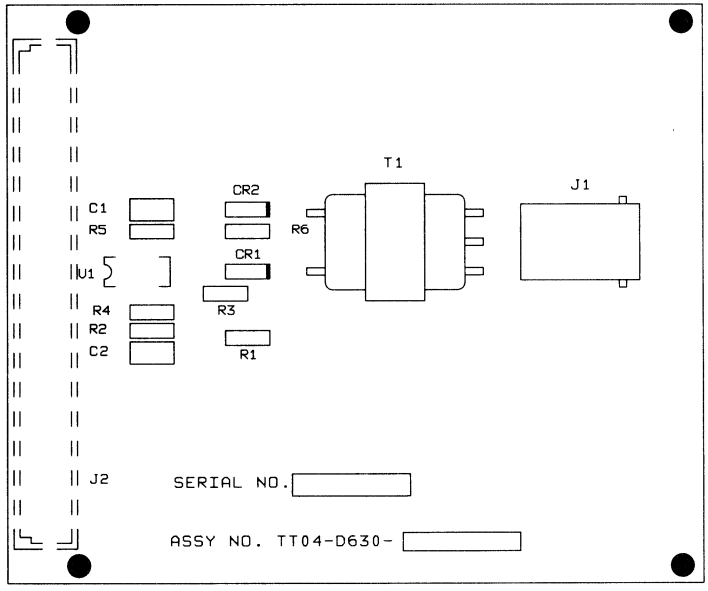


Figure 11. Hybrid Module Silkscreen

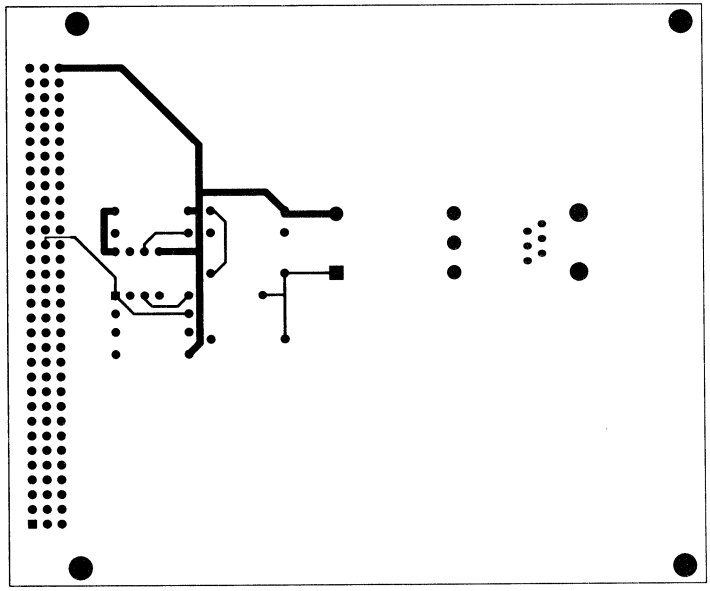


Figure 12. Hybrid Module Component Side Layout

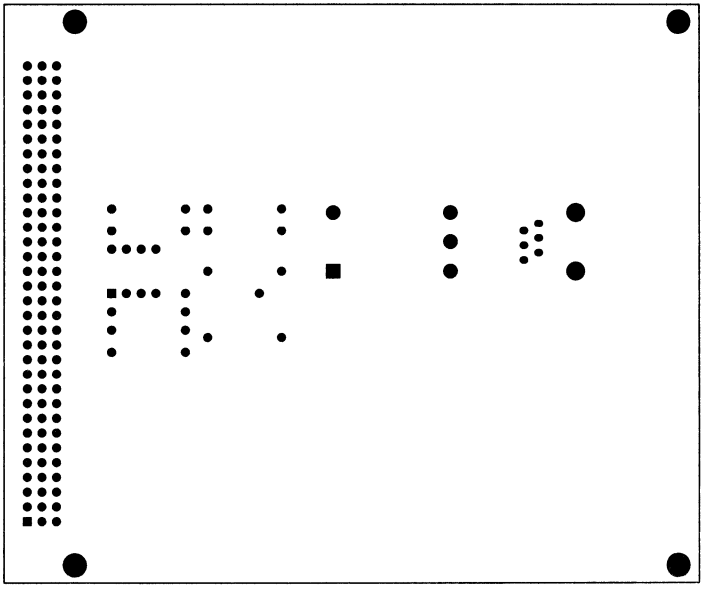


Figure 13. Hybrid Module Padmaster Layout

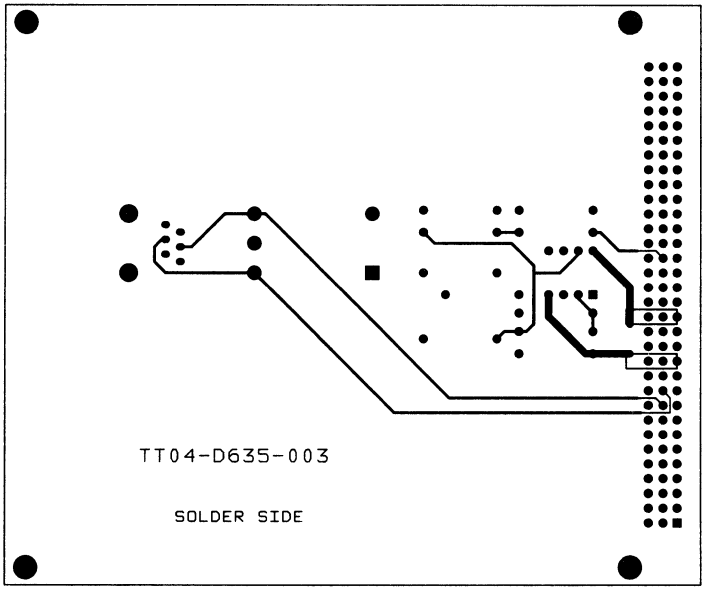


Figure 14. Hybrid Module Solder Side Layout

Rockwell

R1496DP, R9696DP, and R144DP Programmer's Guide

INTRODUCTION

This programmer's guide is a supplement to the R144DP, R9696DP, and R1496DP data sheets. The information provided in this guide will aid the programmer in the design of an end product using the Rockwell ultra high speed modem products.

The following information is provided:

- DSP RAM Address Information
- Handshake Timeout Timers
- V.22bis/V.32 Interworking
- Retrain and Automatic Rate Change Procedures
- Reading Device Revision Information

DSP RAM ADDRESS INFORMATION

The DSP RAM addresses are listed in Table 1.

Table 1 a superset of the RAM information within the three ultra high speed modems. Consult the appropriate data sheet for the addresses which apply to the modem being used.

READING AND WRITING THE DSP RAM

The procedure for reading and writing the DSP RAM is described in the R1496DP, R9696DP, and R144DP data sheets.

Table 1. DSP RAM Addresses

No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imaginary Part (Y)	CR Bit[1]
1	Transmitter Compromise Equalizer Coefficients				
	First Tap	0	5B	—	1
	Last Tap	0	34	—	1
2	V 33/V 32 Rate Sequence	0	93	—	1
3	DTMF Tone Duration	0	9A	—	1
4	DTMF Interdigit Delay	0	1A	—	1
5	DTMF Low Band Power Level	0	19	—	1
6	DTMF High Band Power Level	0	99	—	1
7	Pulse Relay Make Time	0	9C	—	1
8	Pulse Relay Break Time	0	1C	—	1
9	Pulse Interdigit Delay	0	1B	—	1
10	Transmitter Output Level Gain Constant	0	99	—	0
11	Tone Transmit Frequency	0	87	—	0
12	Transmitter New Status Bit (NEWS0) Masking Register for 0 E and 0 F	0	11	—	1
13	Total Span of Echo Canceller	0	9D	—	0
14	Echo Canceller Dividing Point	0	A0	—	0
15	Far End Echo Canceller Center Tap Position	0	24	—	0
16	Echo Canceller Update Coefficient (Training Mode)	0	24	—	1
17	Echo Canceller Update Coefficient (Data Mode)	0	A4	—	1
18	CTS OFF-to-ON Response Time (RTS-CTS Delay)	0	10	—	1
19	Round Trip Far Echo Delay	0	9E	—	0
20	Echo Canceller Error	0	20	—	0
21	Far End Echo Frequency Offset	0	20	—	1
22	Far End Echo Level	0	25	—	0
23	Tone Detector A Bandpass Filter Coefficients	1	26	—	1
24	Tone Detector B Bandpass Filter Coefficients	1	2C	—	1
25	Tone Detector C Bandpass Filter Coefficients	1	32	—	1
26	RLSD On-to-Off Threshold	1	07	—	1
27	RLDS Off-to-On Threshold	1	01	—	0
28	Receiver Chip 1 New Status Bit (NEWS1)				
	Masking Register for 1 A and 1 B	1	9B	—	1
	Masking Register for 1 C and 1 D	1	9C	—	1
	Masking Register for 1 E and 1 F	1	9D	—	1
29	Received Signal Samples	1	03	—	0
30	Demodulator Output	1	04	84	0
31	Low Pass Filter Output	1	00	80	0
32	Average Energy	1	02	—	0
33	AGC Gain Word	1	01	—	1
34	Timing Recovery Update	1	25	—	0
35	Equalizer Input	2	18	98	0
36	Equalizer Tap Coefficients				
	First Tap	2	18	98	1
	Last Tap	2	47	C7	1
37	Unrotated Equalizer Output	2	01	81	0
38	Rotated Equalizer Output (Received Points)	2	02	82	1
39	Decision Points (Ideal Points)	2	02	82	0
40	Equalizer Error	2	03	83	0
41	Equalizer Rotation Angle	2	87	—	1
42	Equalizer Frequency Correction	2	0A	—	1
43	Eye Quality Monitor (EQM)	2	07	—	1
44	Maximum Period of Valid Ring Signal	2	17	—	0
45	Minimum Period of Valid Ring Signal	2	97	—	0
46	Receiver Chip 2 New Status Bit (NEWS2) Masking Register for 0 E and 0 F	2	7E	—	0

Note: 1 CR corresponds to XCR0, YCR0, XCR1, YCR1, XCR2, or YCR2 depending on the chip number and address code

RAM addresses which are specified as having a real (or X) part only, can be loaded in the YRAM Address register as well. The RAM address specifies whether or not the DSP should do an X access or a Y access, not the register in which the address is stored. This allows two different RAM accesses to occur when the result is not a complex number.

Example:

If the user wants to read the pulse relay make and break times simultaneously, the RAM address for the make time can be stored in the XRAM0 Address register and the RAM address for the break time can be stored in the YRAM0 Address register. Both the XCR0 and YCR0 bits should be set to a 1. The XWT0 and the YWT0 bits should be reset to a 0. The XACC0 and YACC0 bits should then be set to a 1. When they are reset to a 0 by the DSP, the pulse make time data will be in the XDAM0 and XDAL0 registers and the pulse break time data will be in the YDAM0 and YDAL0 registers.

Function 1: Transmitter Compromise Equalizer Coefficients

The transmitter compromise equalizer can be programmed by the user. The equalizer is a 40-tap finite impulse response (FIR) digital filter. The first tap is at address $5B ($ denotes a hexadecimal number) and the last tap is at $34. The sampling rate for the filter is 9600 Hz (except V.21 which has a 7680 Hz sampling rate). New coefficients should be loaded while the modem is in idle mode before turning on DTR (2-wire full duplex modes) or RTS (4-wire full duplex modes). The coefficients have to be loaded only once. They are re-initialized only if a POR occurs. The user should ensure that the overall gain of any filter designed is 1. The coefficients are 16-bit 2s complement numbers.

Function 2: Rate Sequence

CCITT defines the V.32 rate sequence bits as follows:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	X	1

B0 = MSB; B15 = LSB

B0-B3, B7, B11, B15	for synchronizing on the rate sequence
B4	a 1 denotes the ability to receive at 2400 bps
B5	a 1 denotes the ability to receive at 4800 bps
B6	a 1 denotes the ability to receive at 9600 bps
B4-B6	0 0 0 calls for a GSTN cleardown
B8	a 1 denotes the ability of trellis encoding and decoding at the highest data rate indicated in B3-B6.
B9-B14	0 0 1 0 0 0 denotes absence of special operational modes.

CCITT defines the V.33 rate sequence bits as follows:

Bit 14 = 0:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	0	1

B0 = MSB; B15 = LSB

B0-B3, B7, B11, B15	for synchronizing on the rate sequence
B4-B6	not defined
B10, B12	not defined
B13	not defined
B8	a 1 denotes the ability to receive at 12000 bps
B9	a 1 denotes the ability to receive at 14400 bps

Bit 14 = 1:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	1	1

B0 = MSB; B15 = LSB

B0-B3, B7, B11, B15	for synchronizing on the rate sequence
B4, B5	a 00 denotes that B6, B10, B12, and B13 define multiplexer configuration selection
B8	a 1 denotes the ability to transmit and receive at 12000 bps
B9	a 1 denotes the ability to transmit and receive at 14400 bps
B6, B10, B12, B13	multiplexer configuration selection (see the V.33 specification for multiplexer configurations)

The V.32 and V.33 rate sequences contain undefined codes and/or bits. The user can use these bits to convey information to the remote modem during training (e.g., remote configuration, multiplexer configuration, test mode configuration, etc). This section discusses how to use these bits.

The 16-bit rate sequence word in the modem's RAM corresponds exactly to the 16-bit rate sequences defined in V.32 and V.33. The MSB of the word in RAM is B0 of the rate sequence and the LSB is B15 of the rate sequence.

Modem Configuration	Rate Sequence (Hex)
V.32T/9600	0791
V.32/9600	0711
V.32/7200	0711
V.32/4800	0591
V.33/14400	01D1
V.33/12000	0191
V.33/9600	0111
V.33/7200	0111

V.32 Rate Sequence

In the V.32 rate sequence, bits B9, B10, B12, B13 and B14 are not used by the Rockwell modems. (Note that the V.32 specification says that if B9-B14 = 001000, then this "denotes absence of special operational modes".) These bits are initialized to 0 by the modem. To use these bits, a read-modify-write of the rate sequence RAM location must be performed while the modem is in idle mode (DTR inactive). Do not alter any of the defined bits in the rate sequence (B0-B8, B11, or B15). The bits can be read out of the interface memory at the receiving modem. The rate sequence is available in RSEQM (1:1:0-7) and RSEQL (1:0:0-7) during the handshake when status bit RSEQ (1:C:0) is a 1. RSEQM contains B0-B7 (1:1:7 = B0) and RSEQL contains B8-B15 (1:0:0 = B15).

To use bits B9, B10, B12, B13 and B14 during a retrain, the rate sequence must be modified after initiating a retrain (with the RTRN bit), since the rate sequence is initialized at the start of a retrain. The rate sequence can be modified any time after detecting the first part of the retrain handshake (ACDET in originate mode, AADET in answer mode) and before sending the rate sequence (R2 in originate mode, R1 in answer mode).

V.33 Rate Sequence

In the V.33 rate sequence, bits B4, B5, B6, B10, B12, B13 and B14 are not used by the Rockwell modems. These bits are initialized to 0 by the modem. Note that the modem does not support the multiplexer configuration codes defined in Table 4B of the V.33 specification (when B14= 1). It is left for the user to implement this feature. To use bits B9, B10, B12, B13, or B14, a read-modify-write of the rate sequence RAM location must be performed while the modem is in idle mode (RTS inactive). Do not alter any of the defined bits in the rate sequence (B0-B3, B7-B9, B11, and B15). The bits can be read out of the interface memory at the receiving modem. The rate sequence is available in RSEQM (1:1:0-7) and RSEQL (1:0:0-7) during the training sequence when status bit RSEQ (1:C:0) is a 1. RSEQM contains B0-B7 (1:1:7 = B0) and RSEQL contains B8-B15 (1:0:0 = B15).

To use bits B9, B10, B12, B13, and B14 during a retrain, the rate sequence must be modified after initiating a retrain (with the RTRN bit), since the rate sequence is initialized at the start of a retrain. The rate sequence can be modified any time after detecting the first part of the retrain sequence (P2DET) and before sending the rate sequence.

Function 3-9: Dialing Parameters

The dialing parameters are listed in Table 2.

Table 2. Function 3 - 9 Dialing Parameters

Function	Parameter	Default Value (Hex)	(Dec)	Units
3	DTMF Tone Duration	$0390	95	ms
4	DTMF Interdigit Delay	$02A9	71	ms
5	DTMF Low Band Power Level	$1F70	–4	dBm
6	DTMF High Band Power Level	$2650	–2	dBm
7	Pulse Relay Make Time	$0159	36	ms
8	Pulse Relay Break Time	$0266	64	ms
9	Pulse Interdigit Delay	$1C20	750	ms

For Functions 3, 4, 7, 8, and 9, the time T (in seconds) is calculated as follows:

$N = T \times 9600$

where: N is the decimal equivalent of the hex number that should be written into RAM.

For Function 5, the DTMF low band power level (L) in dBm is calculated as follows:

$N = \log^{-1}[(L + 4)/20] \times 8048$

where: N is the decimal equivalent of the hex number that should be written in RAM.

L (dBm)	N (decimal)	N (hex)
+6	25450	636A
+5	22682	589A
+4	20216	4EF8
+3	18017	4661
+2	16058	3EBA
+1	14312	37E8
0	12755	31D3
–1	11368	2C68
–2	10132	2794
–3	9030	2346
–4	8048	1F70
–5	7173	1C05
–6	6393	18F9

For Function 6, the DTMF high band power level (H) in dBm is calculated as follows:

$N = \log^{-1}[(H + 2)/20] \times 9808$

where: N is the decimal equivalent of the hex number that should be written in RAM.

H (dBm)	N (decimal)	N (hex)
+6	24637	603D
+5	21957	55C5
+4	19570	4C72
+3	17441	4421
+2	15545	3CB9
+1	13854	361E
0	12348	303C
–1	11005	2A5D
–2	9808	2650
–3	8741	2225
–4	7791	1E6F
–5	6944	1B20
–6	6188	182C

NOTE:

The compromise equalizer should be off (CEQ = 0) to output the correct DTMF levels. The transmit level bits (TLVL) also affect the DTMF levels. The transmit level bit attenuate the DTMF tones an additional amount to that specified by Functions 5 and 6.

Function 10: Transmitter Output Level Gain Constant

The transmitter output level gain constant (G) in dBm is calculated as follows:

$N = \log^{-1} [G / 20] \times 32767 \ (G \leq 0)$

where: N is the decimal equivalent of the hex number that should be written in RAM.

G (dBm)	N (decimal)	N (hex)
0	32767	7FFF
–0.1	32392	7E88
–0.2	32021	7D15
–0.3	31655	7BA7
–0.4	31292	7A3C
–0.5	30934	78D6
–0.6	30580	7774
–0.7	30230	7616
–0.8	29884	74BC
–0.9	29542	7366

The default gain is 0 (N = $7FFF).

The transmitter output level gain constant directly controls the output level of all configurations. It is used for fine tuning the output level which is controlled by the TLVL bits. Therefore,

Output Level = TLVL Setting + Transmitter Output Gain in dBm

Function 11: Tone Transmit Frequency

Frequency F (in Hz) is calculated as follows:

N = F / 0.146486

where: N is the decimal equivalent of the hex number which should be written into RAM.

F (Hz)	N (decimal)	N (hex)
300	2048	800
400	2731	AAB
445	3038	BDE
600	4096	1000
1200	8192	2000
1800	12288	3000
2100	14336	3800
2250	15360	3C00
2400	16384	4000
3000	20480	5000
3600	24576	6000
4000	27306	6AAA

Transmission of a single tone is accomplished by writing an $80 into the TCONF register, programming the tone transmit location in RAM, and then activating RTS. The tone will be transmitted as long as RTS is active.

Function 12: Transmitter NEWS0 Masking Register

Writing a 1 in the bit location corresponding to the desired bit will cause NEWS0 to go active when a status change occurs for the selected bit. All bits default to 0 at power-on-reset. Figure 1 shows the applicable masking register bits. status bits.

Functions 13 - 17 and 19 - 22: Echo Cancellation

The echo canceller has a total span of 53.3 ms (128 bauds). This is divided between near-end and far-end cancellers. The default value for the dividing point is 56 bauds (Function 14), giving a near-end canceller of 23.3 ms and a far-end canceller of 30 ms.

NT = NN + NF = Total span of echo canceller in number of bauds (Function 13)

NN = Echo canceller dividing point in number of bauds (Function 14). NN is also the span of the near-end canceller in number of bauds.

NF = NT – NN = Span of far-end canceller in number of bauds

NC = Far end echo canceller center tap position in number of bauds (Function 15)

Modem Register	Bit 7	6	5	4	3	2	1	0	RAM Register
0:0F	–	–	CTS	DSR	–	TM	–	–	DAM0
0:0E	–	–	–	–	–	–	–	–	DAL0

Figure 1. NEWS0 Masking Register

The Echo Canceller Dividing Point

A common requirement is to shorten the span of the near-end canceller (NN). The default span is quite large. This was mainly chosen to help deal with the effects of intermediate echo in the United States. However, if during the V.32 handshake the round-trip delay is found to be less than the span of the near-end canceller, the far-end canceller simply concatenates with the near-end canceller. In other words, part, or all, of the impulse response of the far-end echo falls within the span of the near-end canceller.

This could be a problem in Europe. The near-end canceller is unable to deal with frequency offset (phase roll) on the echo. However, this type of impairment is common in European networks. Round-trip delays will also be fairly short. Hence if a significant far-end echo is present which is impaired by frequency offset and the round-trip delay is less than the span of the near-end canceller, there will be a performance degradation. Note that if there is no frequency offset then there is no problem with the near-end canceller cancelling far-end echos.

The span of the near-end canceller is changed by programming Function 14, the Echo Canceller Dividing Point. A more useful span for Europe may be in the range 10 ms - 15 ms. For example, if a 12.5 ms near-end canceller is required, then the Echo Canceller Dividing Point should be set to $001E.

Far End Canceller Center Tap Position

Changing the Echo Canceller Dividing Point also affects the span of the far-end canceller. For example, if the dividing point is changed to $001E, then the span of the near-end canceller is 12.5 ms and the span of the far-end canceller is 40.8 ms (assuming the default total span of 53.3 ms). It is recommended that if the dividing point is changed, then Function 15, the Far End Canceller Center Tap Position, should also be changed.

The Center T6ap, NC, should be set as follows:

$$NC = (NT - NN) / 2$$

Total Span of Echo Canceller

Even more flexibility is available by allowing the user to reduce the Total Span of the Echo Canceller (NT), Function 13.

For example, if a 12.5 ms near-end canceller and a 30 ms far-end canceller are required, parameters NT, NN and NC should be set as follows:

NT = $0066 (42.5 ms)

NN = $001E (12.5 ms)

NC = $0024

If the total span is reduced by a significant amount from the default value, it may be necessary to change the Echo Canceller Update Coefficients, Functions 15 and 16. However, unless the total span is reduced to 30 ms or less, this should not be necessary.

Table 3 lists the echo canceller parameters.

Table 3. Function 13-17 Parameters

Function	Parameter	Default Value		
		Hex	Dec.	Units
13	Total Span of the Echo Canceller	$0080	53.3	ms
14	Echo Canceller Dividing Point	$0038	23.3	ms
15	Far End Echo Canceller Center Tap Position	$0024		
16	Echo Canceller Update Coefficient (Training)	$0004		
17	Echo Canceller Update Coefficient (Data)	$000D		

When to change echo canceller functions:

Functions 13,14, and 15 should only be changed when the modem is in idle mode before turning on DTR. The parameters have to be written into RAM only once. They will be altered only if a power-on-reset to the modem occurs.

Restrictions on echo canceller parameters:

There are some restrictions on the values of Functions 13 and 14 (NT and NN).

NT value restrictions:

- value must be even
- minimum value = (NN + 6) if there is a far-end canceller
- minimum value = NN if no far-end canceller is required
- maximum value = 128 ($0080)

NN value restrictions:

- value must be even
- minimum value = 6 if there is a near-end canceller
- minimum value = 0 if no near-end canceller is required
- maximum value = NT

Note that it is possible to make the canceller completely near-end (NN = NT) or completely far-end (NN = 0).

Function 13: Total Span of the Echo Canceller

NT = Total Span of Echo Canceller x 2.4 ms

where: NT is the decimal equivalent of the hex number which should be written into RAM.

(Note: programmable function is not available in B code)

Function 14: Echo Canceller Dividing Point

NN = Echo Canceller Dividing Point x 2.4 ms

where: NN is the decimal equivalent of the hex number which should be written into RAM.

Function 19: Round Trip Far Echo Delay

Function 19 provides the value of the round-trip delay measured during the V.32 handshake.

Round Trip Far Echo Delay = RT x 0.416667 ms

where: N is the decimal equivalent of the hex number which should be read from RAM.

This parameter can be read any time after the completion of the first part of the V.32 handshake for measuring the round-trip delay (see the V.32 specification).

Function 20: Echo Canceller Error

Function 20 is the input to the receiver before the AGC in V.32 configurations. It is a 9600 Hz sampled signal. Note that it is sampled at the transmitter timing and not receiver timing. The parameter is a 16-bit 2s complement number.

Function 21: Far End Echo Frequency Offset

Function 21 provides the far-end echo frequency offset (FO), sometimes known as phase roll, in V.32 configurations.

Far End Echo Frequency Offset = FO/1749 Hz

where: N is the decimal equivalent of the hex number which should be read from RAM.

Function 21 is a 16-bit 2s complement number. It is not valid until rate sequence R3 is detected in the originate modem, or rate sequence R2 is detected in the answer modem.

Function 22: Far End Echo Level

Function 22 provides the far-end echo power level at RXA in V.32 configurations.

Far End Echo Level = –83.7 + 20 x log N dBm

where: N is the decimal equivalent of the hex number which should be read from RAM.

Function 22 is not valid until rate sequence R3 is detected in the originate modem or rate sequence R2 is detected in the answer modem.

Function 18: CTS OFF-to-ON Response Time (RTS-CTS Delay)

Function 18 determines the CTS off-to-on response time in 2-wire full-duplex configurations. The response time equation varies according to the configuration selected.

Configuration	Response time equation
V.32	N = (Response time x 2.4 ms) –1
V.22 bis, V.22,Bell 212A	N = (Response time x 0.6 ms) –1
V.23,Bell 103	N = Response time x 9.6 ms
V.21	N = Response time x 7.68 ms

where: N is the decimal equivalent of the hex number which should be written into RAM.

The default values are listed in Table 4.

4

Table 4. Function 18 Parameters (RTS-CTS Delay)

Function	Configuration	Default Value Hex.	Dec.	Units
18				
	V.32	$0000	0.4	ms
	V.22bis,V.22,Bell 212A	$0000	1.6	ms
	V.23,Bell 103	$07E0	210	ms
	V.21	$0F00	500	ms

Table 5. DSP RAM Address for TONEA, TONEB, and TONEC

	TONEA		TONEB		TONEC		Prefilter	
	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2
A3	27	A7	2D	AD	33	B3	38	B8
A2	28	A8	2E	AE	34	B4	39	B9
A1	29	A9	2F	AF	35	B5	3A	BA
B2	2A	AA	30	B0	36	B6	3B	BB
B1	2B	AB	31	B1	37	B7	3C	BC
LPFBK	A6		AC		B2			
LPGAIN	26		2C		32			
THRESHU	23		24		25			
THRESHL	A3		A4		A5			

Function 23 through 25: Tone Detector Filter Tuning

A block diagram of the three tone detectors is shown in Figure 2. Tone detector C is preceded by a prefilter and a squarer. The purpose of the low pass filter (LPF) and squarer is to allow the user to detect dual tones while rejecting the main channel energy. The user would program TONEC to detect a difference frequency generated by the squarer for detection of, for example, 350 Hz and 440 Hz. The prefilter would be designed to reject the energy in the 600 to 3000 Hz band. If the dual tone pair of 350 and 440 Hz appeared (or unfortunately any other frequency pair in the range of 300 to 600 Hz with a difference of 90 Hz) TONEC would turn on.

A control bit has been added in D code. This bit, called SQDIS (1:2:6), allows the squarer in front of tone detector C to be disabled. If the squarer is disabled then tone detector C will have four cascaded biquads (since there is a prefilter consisting of two biquads), forming an eight order IIR filter with user programmable coefficients.

The implementation of the filters in the ultra high speed modems allows user definition of the characteristics of the prefilter and the three tone detectors. Table 5 provides the DSP RAM Address codes for the filter coefficients. Figure 3 shows that the prefilter and the main filter sections of the tone detectors are fourth order (two-second order biquads in cascade), thereby allowing a wide variety of filter characteristics to the synthesized. The only limitation on these user-definable shapes is that their gain should be around unity at the pass frequencies to avoid problems of saturation at one extreme (gain too high) and digital noise at the other (gain too low). Computation of the filter coefficients can be performed by any infinite impulse response (IIR) filter design program which outputs the coefficients in cascaded second-order sections.

For tone detectors A and B, there is a rule of thumb for choosing the gain of a user-designed filter. If the user wishes to use the default threshold value and designs the filter for 0 dB gain in the passband, then the absolute turn-on threshold will be –30 dBm. Therefore, to get a turn-on threshold of –43 dBm, the filter should have a gain of 13 dB in the passband.

The level detector in each of the tone detectors flags the detection of a tone if it is in the tone detector passband and if it is above a certain threshold defined by THRESHU. The tone detected flag will remain set until, or unless, the tone falls below a lower threshold defined by THRESHL.

The first-order low pass filter in each level detector, defined by the coefficients LPGAIN and LPFBK, controls the response time of each tone detector. Normally, these coefficients will not require alteration but if, for example, a rapid cadence must be detected on a tone, then the 3dB

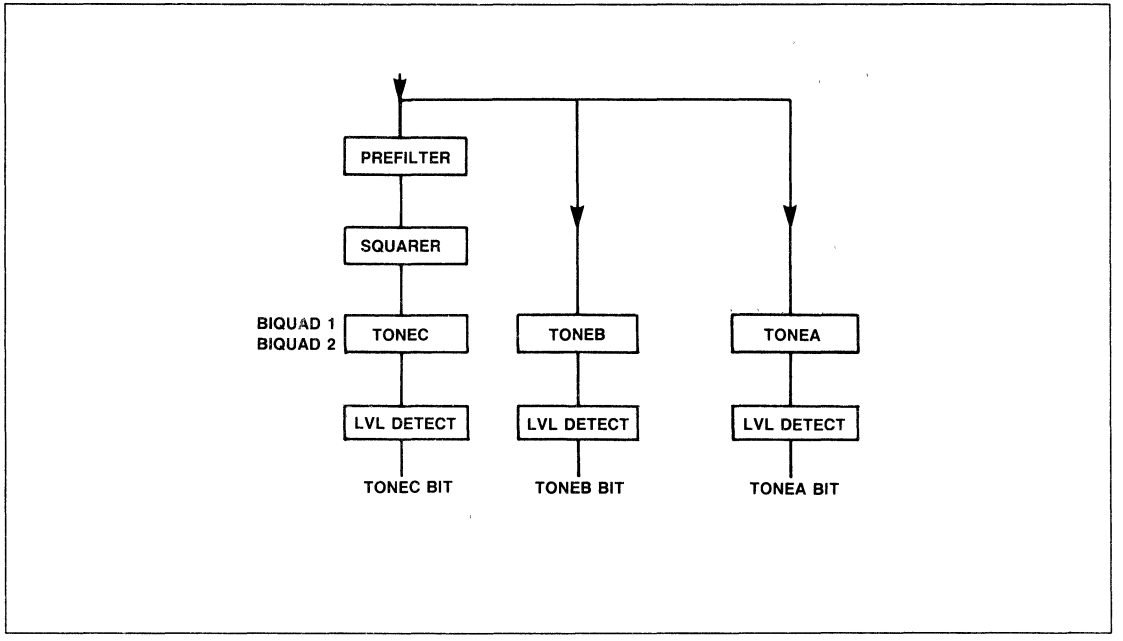


Figure 2. Tone Detectors

cutoff is the on-time or off-time of the tone, whichever is shorter. The gain of the filter should be set to unity.

Example:

A call-progress tone detector is required for the U.S. telephone network and should detect the appropriate tones only if the exceed –25 dBm.

Solution:

The requirement can be met by detecting tones in the range 250 Hz-650 Hz. A bandpass filter with a passband of 245 Hz-650 Hz must be designed. Any filter up to fourth order can be implemented and, normally, it is best to choose the highest order available, especially for bandpass designs. A design package such as FILSYN could carry out this function by defining the passband frequencies, the filter order, the filter gain (chose unity) and the filter sampling rate (9600 Hz). An example of suitable coefficients is:

	A1	A2	A3	B1	B2
Biquad 1	0.0436	0	–0.0437	1.7369	–0.8836
Biquad 2	0.0874	–0.1242	0.0874	1.8145	–0.8556

The first modification to make to these values is to divide them by two because coefficients greater than one are unrealized in the actual filter implementation. This division should be done even if none of the coefficients in the design are greater than one. This is because the biquad sections have been implemented as shown in Figure 3. The modified values are, therefore:

	A1'	A2'	A3'	B1'	B2'
Biquad 1	0.0219	0	–0.0219	0.8684	–0.4418
Biquad 2	0.0437	–0.0621	0.0437	0.9072	–0.4278

The last step is to convert the above numbers to fractional 2s complement numbers, in this case:

	A1"	A2"	A3"	B1"	B2"
Biquad 1	02CC	0	FD34	6F28	C774
Biquad 2	0598	F80C	0598	741F	C93E

The second part of the requirement is to detect tones only if they exceed –25 dBm. The values of THRESHU and the corresponding tone level detected are:

THRESHU	Tone Level Detected (dBm)
$1000	+3
$0800	–3
$0400	–10
$0220	–15
$0090	–25

THRESHU should be $90. If no hysteresis is required in the tone detector, then set THRESHL to $90. If 6 dB of hysteresis is required, set THRESHL to $48 (–31 dB). This value represents half of THRESHU. Many other values of THRESHU and THRESHL are allowable, but, normally,

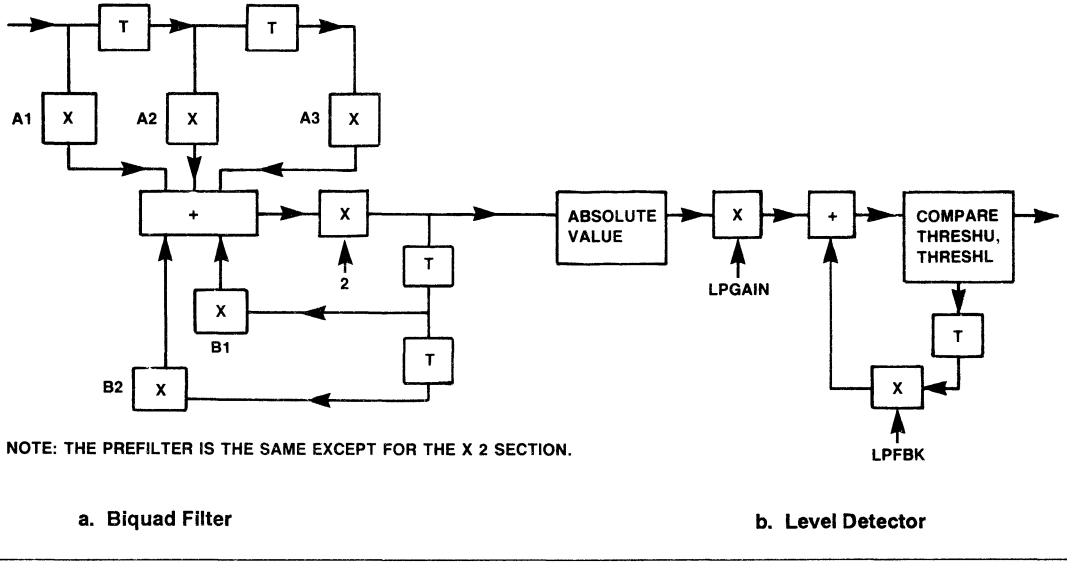


Figure 3. Biquad Filter and Level Detector

THRESHU = THRESHL for reliable operation. Other filter designs may require different values to those shown above.

Table 6 shows the filter coefficient values for specific filters.

Function 26: RLSD On-to-Off Threshold

The number calculated for Function 26 may not give an accurate threshold. The threshold will vary from configuration to configuration and the number may need fine tuning by trial and error to achieve the desired threshold. The number should only be written into RAM when the modem is in data mode with RLSD on.

$N = \log^{-1}[(TOFF - TON)/10] \times 1946$ (B and D code)

$N = \log^{-1}[(TOFF - TON)/10] \times 1735$ (after D code)

where: TOFF is the RLSD On-to-Off threshold

TON is the RLSD Off-to-On threshold in dBm.

N is the decimal equivalent of the hex number which should be written into RAM.

Function 27: RLSD Off-to-On Threshold

The number calculated for Function 27 may not give an accurate threshold. The threshold will vary from configuration to configuration and the number may need fine tuning by trial and error to achieve the desired threshold. The number should be written into RAM every time the modem is in idle mode.

$N = [1024 \times int(X)] + [6456.3\ (1 - 10E(-Y/20))]$

where: $X = (47 + TON)/1.5$ (B and D code)

$X = (47.5 + TON)/1.5$ (after D code)

$Y = 47 + TON - (1.5 \times int(X))$ (B and D code)

$Y = 47.5 + TON - (1.5 \times int(X))$ (after D code)

TON is the desired threshold in dBm

int(X) is the truncated integer part of expression X.

N is the decimal equivalent of the hex number which should be written into RAM.

Example :

If is desired to set the RLSD Off-to-On threshold to –43.5 dBm.

Then:

$X = (47 - 43.5)/1.5 = 3.5/1.5$

$int(X) = 2$

$Y = 47 - 43.5 - (2 \times 1.5) = 0.5$

Therefore:

$Y = (1024 \times 2) + 6456.3\ (1 - 10E(-1/40))$

$Y = 2048 + 361 = 2409 = \$0969$

Function 28: Receiver NEWS1 Masking Register

Writing a 1 in the bit location corresponding to the desired bit will cause NEWS1 to go active when a status change occurs for the selected bit. Function 28 defaults to $0000. Figure 4 shows the applicable NEWS1 masking register bits.

Function 32: Average Energy

Function 32 provides the post-AGC power level. If the receive level is above the RLSD on-to-off threshold this value should be fairly constant and will be in the region of $079A (B and D code) or $06C7 (after D code). This cor-

Table 6. DSP RAM Filter Coefficients

	Biquad1					Biquad2				
Filter	A3	A2	A1	B2	B1	A3	A2	A1	B2	B1
1800 Hz	0372	FEA6	0372	C063	30D6	00C4	FFDA	00C4	C063	30D6
2250 Hz	0119	FE72	0130	C063	0C82	02D9	FEE3	02D9	C063	0C82
245-650 Hz	FD34	0000	02CC	C774	6F28	0630	F018	0630	C93E	741F
360-440 Hz	01AA	FEBC	01AA	C7CD	7438	FF5C	0000	00A4	C148	7A66

Modem	Bit								RAM
Register	7	6	5	4	3	2	1	0	Register
1:0F	RLSD	FED	–	–	–	–	–	–	DAM0
1:0E	RTDET	–	–	–	–	–	SPEED	–	DAL0
1:0D	P2DET	PNDET	S1DET	SCR1	U1DET	SADET	–	–	DAM0
1:0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	–	RSEQ	DAL0
1:0B	TONEA	TONEB	TONEC	ATV25	–	–	–	–	DAM0
1:0A	–	–	–	–	–	–	–	–	DAL0

Figure 4. NEWS1 Status Bits

responds to a level of –0.5 dBm (B and D code) or –1 dBm (after D code). If the receive level is below the RLSD off-to-on threshold then this parameter indicates how far below the threshold the receive level is.

Receive level = TON + 10 x log (N/1946) dBm

where: TON is the RLSD off-to-on threshold in dBm.

N is the decimal equivalent of the hex number which should be read from RAM.

Function 33: AGC Gain Word

Function 33 is useful for determining the receive level at the Receive Analog (RXA) input. The number in RAM is related to the receive level as follows:

Receive level =

$(1.5 \times Y - 47) - 20 * \log_{10}(1 - ((N - Y \times 1024)/6456.3))$ dBm (B and D code)

Receive level =

$(1.5 \times Y - 47.5) - 20 \times \log_{10}(1 - ((X - Y \times 1024)/6456.3))$ dBm (after D code)

where: Y = int (N/1024)

N is the decimal equivalent of the hex number which should be read from RAM.

This formula is only valid if the receive level is above the RLSD off-to-on threshold. If the receive level is below the RLSD off-to-on threshold then the formula given under Average Energy (see function 32) must be used for calculating the receive level.

If the receive level is only required to be known within 1.5 dB then just the first part of this expression (1.5 x Y – 47) can be used.

Function 43: Eye Quality Monitor

In V.32 4800 bps, V.29, V.27, V.22bis, V.22 and Bell 212A modes, EQM is the filtered squared magnitude of the error vector. However, for all TCM modes (V.33 modes and V.32 9600 and 7200 bps modes), EQM is the filtered minimum trellis path length (or metric). This gives a better indication of signal quality for trellis modes.

The error vector formed by the decision logic can be used to indicate relative signal quality. As signal quality deteriorates, the average error vector increases in magnitude. By calculating the magnitude of the error vector and filter the results, a number inversely proportional to signal quality is derived. This number is called the eye quality monitor (EQM). Because of the filter time constant, EQM should be allowed to stabilize for approximately 700 baud times following RLSD going active.

The EQM value for the non-trellis configurations is the filtered squared magnitude of the error vector and represents the average signal power contained in the error component. The power is directly proportional to the probability of errors occurring in the received data and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of CCITT Recommendation V.24 or circuit CG of the RS-232-C standard) by comparing the EQM value against experimentally determined criteria (Bit Error Rate curves). Figure 6 illustrates the relationship of the EQM number to an eye pattern created by a four point signal structure (e.g. V.29/4800 bps) in the presence of high level white noise. The EQM value is proportional to the square of the radius of the disk around any ideal point. The radius increases when signal to noise ratio (SNR) decreases. As the radius approaches the ideal point's boundary values, the bit error rate (BER) increases. Curves of BER as a function of the SNR are used to establish a criteria for determining the acceptability of EQM values. Therefore, from an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the modem to fallback to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbance present on the line and with the various configurations. A given magnitude of EQM in V.29/9600 does not represent the same BER as in V.27/4800. The former configuration has 16 points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given

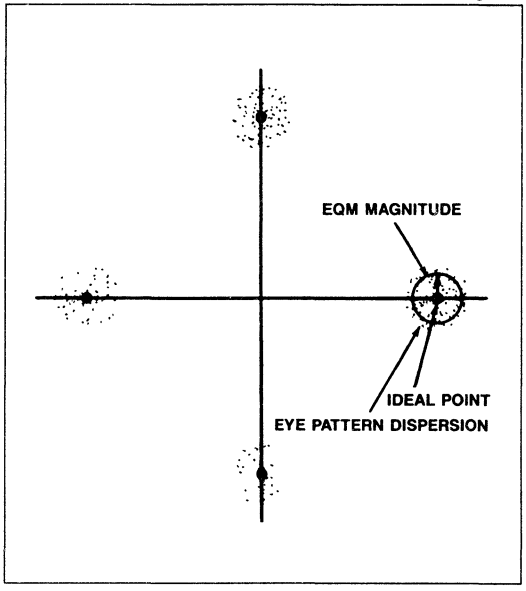


Figure 6. Relationship of EQM to Eye Pattern

level of noise or jitter. Also, the type of line disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Since EQM is dependent upon the signal structure of the modulation being used and the type of line disturbance, EQM must therefore be determined empirically in each application.

Function 44 and 45: Ring Detection Parameters

The ring detector measures the period of pulses on the ring detect input and determines whether the pulses are within the frequency range specified by the Maximum and Minimum Period of Valid Ring Signal functions. Since maximum period corresponds to minimum frequency, the formula for calculating these functions is given in terms of frequency.

Frequency F (in Hz) is calculated as follows:

N = 9600/F

where: N is the decimal equivalent of the hex number that should be written into RAM.

Table 7 lists the Function 44 and 45 parameters.

Table 7. Function 44 and 45 Parameters

Function	Parameter	Default Value		
		Hex.	Dec.	Units
44	Maximum Period of Valid Ring Signal	$0280	15	Hz
45	Minimum Period of Valid Ring Signal	$008D	68	Hz

Function 46 Receiver NEWS2 Masking Register

Writing a 1 in the bit location corresponding to the desired bit will cause NEWS2 to go active when a status change occurs for the selected bit. Function 46 defaults to $0000. Figure 5 shows the applicable NEWS2 masking register bits.

HANDSHAKE TIMEOUT TIMERS

The modem has time-outs on each successive state of the V.32 handshake. Unfortunately, the B code has one missing which could cause a lock-up of the AA/AC sequence. It should be possible to clear this by turning off DTR and then setting both the NEWC0 and NEWC1 bits. This has been corrected in D code.

If the modem fails to detect any part of the handshake it will timeout and abort the handshake. The transmitter will immediately stop sending the training sequence. Also, Chip 1 when it times out loads an error code into the interface memory that indicates that point in the handshake the time-out occurred. This code is put into register 14. The code is not cleared even if the modem immediately goes into a new handshake after aborting. The user can observe this register during the handshake to determine if an abort occurred.

It is a good idea for the user to successively observe the handshake detector bits (AADET, ACDET, CCDET, etc.). This will tell him how the handshake is progressing. The user can be interrupted then for each step of the handshake to be certain of its progression.

The V.32 Handshake Error codes and their meanings are:

Error Code	Reason For Aborting (Time-out)
0	No error
1	Failed to detect AC/CA transition (calling)
2	Failed to detect AA/CC transition (answering)
3	not used
4	Timed out waiting for power to come up at the start of the S sequence.
5	Failed to detect the S sequence
6	not used
7	Failed to detect the Rate Sequence (R1,R2, or R3)
8	Failed to detect S/S\ transition
9	Failed to detect E sequence
A	Power loss during TRN of Rate Sequence

Modem Register	Bit								RAM Register
	7	6	5	4	3	2	1	0	
2:0F	–	–	–	–	RI	–	–	–	DAM0
2:0E	–	–	–	–	–	–	–	–	DAL0

Figure 5. NEWS2 Status Bits

V.22BIS/V.32 INTERWORKING

Suggestions for a possible interworking scheme.

Answer Modem

1. (a) Configure for V.22 bis.
   (b) Set up TONEA for 1800 Hz detection, –43 dBm threshold.

1800 Hz Tone Detection

RAM Address	RAM Data
27	0372
28	FEA6
29	0372
2A	C063
2B	30D6
A7	00C4
A8	FFDA
A9	00C4
AA	C063
AB	30D6

2. Upon going off hook and initiating the handshake, monitor TONEA. Note that the billing delay has to be implemented by the user. The R1496DP/R9696DP will start to send answer tone as soon as DTR and DATA0 are both valid.

   If a V.32 modem is calling, it should send an 1800 Hz carrier at least 1 second after detecting answer tone. If this is the case TONEA should be on. If 1800 Hz is not detected by the end of the answer tone, then assume the calling modem is V.22 bis and set DATA1 to a 1 and allow the handshake to proceed. If 1800 Hz is detected, then immediately after the answer tone ends (answer tone is sent for 2.7 seconds), reconfigure to V.32, set NV25 to a 1 to ensure that the answer tone is not sent again, and start the V.32 handshake. In this case, the user will have to implement the 75 ms silence period following the answer tone.

   This scheme would have problems if the calling modem delays in sending 1800 Hz, for instance, if there is a manual calling modem. However, TONEA continues to operate during a V.22 bis handshake and TONEA is not set by a V.22 bis calling signal at any time so if 1800 Hz is detected after the start of the V.22 bis unscrambled ones sequence, then it should still be possible to reconfigure to V.32.

Calling Modem

1. (a) Configure V.32.
   (b) Set up TONEA for 2250 Hz detection, –43 dBm threshold.

2250 Hz Tone Detection

RAM Address	RAM Data
27	0119
28	FE72
29	0130
2A	C063
2B	0C82
A7	02D9
A8	FEE3
A9	02D9
AA	C063
AB	0C82

2. Upon detecting answer tone using the ATV25 bit initiate a V.32 handshake in the normal manner according to V.32. After the answer tone ends and the answering modem handshake signal begins then monitor ACDET and TONEA for 215 ms (the time limit is necessary because TONEA can be falsely set when random data is sent by a V.32 answer modem, so it should only be tested up to the end of the first S segment in the answer handshake). If ACDET comes on during this time then a V.32 modem is answering. If TONEA comes on then a V.22 bis unscrambled ones sequence has been detected, so reconfigure to V.22 bis and start the handshake.

Coefficient Values for TONEA

The default threshold detect values are correct for detection of signals = –43 dBm using the above coefficients.

RETRAIN AND AUTOMATIC RATE CHANGE

Both V.33 and V.32 define retrain and automatic rate change. This section explains how to perform the retrain and rate change.

RETRAIN WITHOUT A RATE CHANGE

V.33 Configurations

When the RTRN bit is set to a 1 and the automatic rate change bits are set to a 0, the modem will send the training sequence. The modem for which the retrain is intended will detect the training sequence and will retrain. This can be monitored at the transmitter by watching the state of CTS (CTS off means going through training sequence) and at the receiver by watching the RLSD, P2DET, and PNDET bits. Once the retrain is completed, the process is complete. The modem which was retrained does not respond with a retrain. It is up to the user to set the retrain bit for this to occur.

V.32 and V.22 bis Configurations

When the RTRN bit is set to a 1, the modem will initiate the retrain sequence. The modem which detects the retrain sequence will respond with training, and both modems will proceed with the proper training sequence. The retrain process can be monitored by observing the appropriate status bits in the transmitter and receiver.

Retrain with a Rate Change (V.33, V.32, and V.22 Bis)

To obtain a rate change (V.33 and V.32) along with a retrain the following procedure should be followed. The rate change only occurs with CCITT V.33 and V.32 defined configurations and not with the proprietary configurations.

Steps 1 and 2 are do not apply to V.22bis

1. Set the automatic rate change bits to a 1 (ARC0, ARC1).
2. Store the desired configuration in the TCONF and RCONF registers

   NOTE: Do not set the NEWC bits.
3. Set the RTRN bit to a 1.

The modem will then send the retrain sequence at the correct operating speed as selected in the configuration registers. The rate sequence is automatically changed in the training sequence to tell the other modem what speed to operate at. When the modem detects the retrain, it will retrain and then it will respond with retrain. This will then retrain the modem which initiated the retrain procedure. The status bits will change as mentioned above and the retrain bit will be reset to a 0 when the retrain sequence is completed.

READING DEVICE INFORMATION FROM THE INTERFACE MEMORY

Each DSP provides, at a specific time, the ROM checksum, device number, and revision number. This information is available (when bit N:1E:3 is a 1) for a maximum of 5 ms after the low-to-high edge of power-on-reset. The information is located in the following registers. Register N:10:0-7 should be the last register read to obtain the correct information.

Register	Information
N:15:0-7	ROM Checksum MSB
N:14:0-7	ROM Checksum LSB
N:13:0-7	Device Number MSB
N:12:0-7	Device Number LSB
N:11:0-7	Revision Number MSB
N:10:0-7	Revision Number LSB

where: N = 0, 1, or 2

The information is formatted in ASCII.

The ROM checksum will remain a constant from device to device and from revision to revision. Its value is 412B.

An example of a typical device number is 3036. This represents a device number of 06.

An example of a typical revision number is 2042. This represents a revision of B (space B or B Code).

Rockwell

R9696DP "AT" Command Set Capabilities

INTRODUCTION

The "AT" command set is a popular method to control a modem which has an asynchronous interface. The interface can be serial or over a microprocessor bus through an 8250/16450-type UART. This application note identifies the "AT" commands used in the Hayes Smartmodem 2400, 1200 (the original 1200), and the Hayes V-series Smartmodem 9600, and compares these commands to the capabilities of the Rockwell R9696DP V.32/V.22 bis Full-Duplex Modem.

Consult the R9696DP Data Sheet (Order No. MD30) and the R1496DP, R9696DP, and R144DP Programmer's Guide Application Note (Order No. 831) for detailed modem information.

AT COMMAND SET SUMMARY

Table 1 summarizes the AT commands. If the Micro and/or R9696 column contains a C or an M, respectively, the command is implemented by the microprocessor (**C**ontroller) and/or R9696 (**M**odem). If an S is in a **S**martmodem column, then that particular modem has the command implemented. If the command modifiers for a particular command are not listed, then all of the modifiers associated with that command are implemented for the various modems.

S REGISTER SUMMARY

Table 2 summarizes the S registers. If the Micro and/or R9696 column contains a C or an M, respectively, the S register is implemented by the microprocessor (**C**ontroller) and/or R9696 (**M**odem). If an S is in a **S**martmodem column, then that particular modem has the S register implemented.

AT COMMAND SET DETAIL

Table 3 describes the AT commands. The following fields are used to describe each of the commands and how they should be implemented:

- Command: Identifies and names the AT command.
- Modifier: Identifies and describes the command modifiers.
- Function: Is the command a microprocessor or modem (R9696DP) function?
- R9696DP?: If the AT command is a modem function, can the R9696DP perform the command?
- Details: Describes the implementation details.

S REGISTERS DETAIL

The S registers provide special access to the system configurations. The registers offer flexibility in the system to tailor it to the user's system.

Table 4 describes the S registers. The following fields are used to describe each of the S registers and how they should be implemented:

- Register: Identifies and names the S register.
- Range: Provides the operational range of the function.
- Default: Provides the default range of the S Register
- Function: Is the command a microprocessor or modem function?
- R9696DP?: If the S register is a modem function, can the R9696DP perform it?
- Details: Describes the implementation details.

4

Table 1. AT Command Summary

	Implemented by		Smartmodem		
AT Command	Micro	R9696	1200	2400	9600
AT	C		S	S	S
A/	C		S	S	S
A		M	S	S	S
B		M	S	S	S
C0		M	S		
C1		M	S		S
D	C	M	S	S	S
E	C		S	S	S
F0	C		S		
F1	C		S		S
H		M	S	S	S
I	C		S	S	S
L	C		S	S	S
M	C		S	S	S
N	C	M			S
O	C	M	S	S	S
Q0	C		S	S	S
Q1	C		S	S	S
Q2	C				S
Sr=n	C	M	S	S	S
Sr?	C	M	S	S	S
V	C		S	S	S
W	C				S
X	C	M	S	S	S
Y	C	M	S	S	S
Z	C	M	S	S	S
Z0	C	M			S
Z1	C	M			S
&C	C	M		S	S
&D	C	M		S	S
&F	C			S	S
&G		M		S	S
&J	C			S	S
&K	C				S
&L		M		S	S
&M	C	M		S	S
&P		M		S	S
&Q	C	M			S
&R	C	M		S	S
&S	C	M		S	S
&T	C	M		S	S
&V	C				S
&W	C			S	S
&W0	C				S
&W1	C				S
&X		M		S	S
&Y	C				S
&Zn	C			S	
&Zn=x	C				S
+++	C		S	S	S

Table 2. S Registers Summary

	Implemented by		Smartmodem		
S Register	Micro	R9696	1200	2400	9600
S0	C	M	S	S	S
S1	C	M	S	S	S
S2	C		S	S	S
S3	C		S	S	S
S4	C		S	S	S
S5	C		S	S	S
S6	C		S	S	S
S7	C	M	S	S	S
S8	C		S	S	S
S9	C	M	S	S	S
S10	C	M	S	S	S
S11		M	S	S	S
S12	C		S	S	S
S13			S	S	S
S14			S	S	S
S15			S	S	S
S16			S	S	S
S17				S	S
S18	C			S	S
S19				S	S
S20				S	S
S21				S	S
S22				S	S
S23				S	S
S24				S	S
S25	C			S	S
S26	C	M		S	S
S27				S	S
S28					S
S29					S
S30					S
S31					S
S32					S
S33					S
S34					S
S35					S
S36	C				S
S37	C	M			S
S38	C	M			S

Table 3. AT Commands

Command:	**AT**	
Modifier:		Various commands
Function:		Microprocessor
R9696DP?:		N/A
Details:		Signals the beginning of a command flow. Used for auto speed and character format determination.
Command:	**A/**	**Repeat Last Command Line**
Modifier:		none
Function:		Microprocessor
R9696DP?:		N/A
Details:		Repeats the last command.
Command:	**A**	**Answer Immediately**
Modifier:		none
Function:		Modem
R9696DP?:		Yes
Details:		The relay driver of the modem is controlled using the RA bit. When DTR and RA are set to a 1 and ORG is reset to a 0 the modem will answer immediately.
Command:	**B**	
Modifier:		B0 CCITT configuration B1 Bell configuration
Function:		Modem
R9696DP?		Yes
Details:		The following are the configurations in the R9696DP: **CCITT** **Bell** V.32 Bell 212A V.22 bis Bell 103 V.22 V.23 V.21
Command:	**C**	**Transmitter Carrier Signal**
Modifier:		C0 Transmit carrier off C1 Transmit carrier on
Function:		Modem
R9696DP?:		Yes
Details:		If the modem is in V.22, leased-line, controlled carrier, then RTS controls carrier turn-on and turn-off. Otherwise, the transmitter is off when the TXSQ bit is a 1, or the transmitter is on when TXSQ is a 0.

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Table 3. AT Commands (Cont'd)

Command:	D	**Dial**
Modifier:		0,1,2,3,4, 5,6,7,8, 9,,*,A,B, C,D Dial Digits T Tone dial P Pulse dial R Reverse dial S Dial stored number W Wait for dial tone @ Quiet answer , Pause ! Flash ; Return to command state
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The modem can dial 0-9, #, and * When the DTMF bit is a 1, the modem dials with DTMF tones; when DTMF is a 0, the mode dials with pulses. Reverse dial is accomplished by resetting the ORG bit to a 0 so the modem answers after it dials. Dial a stored number is a microprocessor function. Tone detect filter A can be used to detect dial tone and for waiting for 5 seconds of quiet. Pause is implemented by the microprocessor. Flash can be performed by resetting, delaying, and then setting the RA bit. Return to command state is a microprocessor function.
Command:	E	**Character Echo**
Modifier:		E0 Disables command state character echo E1 Enables command state character echo
Function:		Microprocessor
R9696DP?:		N/A
Details:		This option determines if the terminal is to echo or if the modem does the echoing.
Command:	F	**Duplex**
Modifier:		F0 Full-duplex F1 Half-duplex
Function:		Microprocessor
R9696DP?:		N/A
Details:		This function provides for the echoing or not echoing of commands depending on the terminal configuration.
Command:	H	**Hang-up**
Modifier:		H0 Hangs the modem up (puts the modem on-hook) H1 Places the modem off-hook
Function:		Modem
R9696DP?:		Yes
Details:		Disconnecting/connecting the modem from the line can be accomplished using the RA bit.

Table 3. AT Commands (Cont'd)

Command:	I	**Testing Internal Memory**
Modifier:		I0 Product Code
		I1 Firmware Checksum
		I2 Firmware Checksum compared to a stored number; a result code of OK or ERROR is returned.
Function:		Microprocessor
R9696DP?:		N/A
Details:		This function determines if the system ROM is functional.
Command:	L	**Speaker Volume**
Modifier:		L0 Low volume
		L1 Low volume
		L2 Medium volume
		L3 High volume
Function:		Microprocessor
R9696DP?:		N/A
Details:		The microprocessor controls the volume of the line monitor speaker.
Command:	M	**Speaker Control**
Modifier:		M0 Always off
		M1 On until carrier detected
		M2 On continuously
		M3 On after dialing until carrier detected
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The microprocessor controls the squelching and the unsquelching of the speaker. The RLSD bit in the modem can be used to detect carrier.
Command:	N	**Modulation Handshake**
Modifier:		N0 Speed of the connection is determined by S37. If S37 = 0, then the speed must match the speed of the last AT command.
		N1 Speed is determined by the DCE speed supported by both modems.
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The microprocessor performs the speed detection from the AT command. The modem can be set to many configurations by setting the TCONF and RCONF bits appropriately.
Command:	O	**On-line**
Modifier:		O0 Returns modem from command state to on-line state.
		O1 Returns modem from command state to on-line state and initiates a modem retrain (2400 bps and higher).
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The microprocessor handles switching from command state to on-line state. Setting the RTRN bit in the modem to a 1 causes a retrain to be initiated.

Table 3. AT Commands (Cont'd)

Command:	**Q**	**Result Code Display**
Modifier:		Q0 Results codes
		Q1 No result codes
		Q2 Result codes in originate mode only
Function:		Microprocessor
R9696DP?:		N/A
Details:		This command determines if results codes are sent to the terminal.
Command:	**Sr=n**	**Change an S Register Value**
Modifier:		r = S register number,
		n = S register value
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		Some of the S registers deal with microprocessor functions and some with modem functions. See Table 4 for the S register functions.
Command:	**Sr?**	**Reading an S Register Value**
Modifier:		r = S register number
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		Some of the S registers deal with microprocessor functions and some with modem functions. See Table 4 for the S register functions.
Command:	**V**	**Result Code Form**
Modifier:		V0 Result codes displayed in numeric form
		V1 Result codes displayed in English form
Function:		Microprocessor
R9696DP?:		N/A
Details:		V1 is usually selected if the modem is to be used with a terminal; V0 is usually used if the modem is used with a software package on a computer.
Command:	**W**	**Negotiating Progress Reporting**
Modifier:		W0 Error-control call progress not reported
		W1 Error-control call progress reported
Function:		Microprocessor
R9696DP?:		N/A
Details:		If selected the microprocessor returns the protocol used.

Table 3. AT Commands (Cont'd)

Command: **X** **Result Codes and Dialing Capability**

Modifier:
- X0 Codes 0-4 enabled, blind dialing
- X1 Codes 0-5,10-12,14 enabled, blind dialing
- X2 Codes 0-6,10-12,14 enabled, dial tone detected
- X3 Codes 0-5,7,10-12,14 enabled, busy tone detected
- X4 Codes 0-7,10-12,14 enabled, dial and busy tone detected

Function: Microprocessor and modem

R9696DP?: Yes

Details: The microprocessor sends the result codes. The modem can detect the call progress tones by using TONEA. The protocol is performed by the microprocessor. 19200 bps is possible if compression is used by the microprocessor.

Result code definitions:

Numeric	Verbose	Description
0	OK	Command executed
1	CONNECT	Connection at 0-300 bps
2	RING	Ring detected
3	NO CARRIER	Carrier not detected or lost
4	ERROR	Invalid command etc.
5	CONNECT 1200	Connection at 1200 bps
6	NO DIALTONE	No dial tone detected
7	BUSY	Busy signal detected
8	NO ANSWER	No answer at remote modem
10	CONNECT 2400	Connection at 2400 bps
11	CONNECT 4800	Connection at 4800 bps
12	CONNECT 9600	Connection at 9600 bps
14	CONNECT 19200	Connection at 19200 bps
40	CARRIER 300	Carrier detected at 300 bps
46	CARRIER 1200	Carrier detected at 1200 bps
47	CARRIER 2400	Carrier detected at 2400 bps
48	CARRIER 4800	Carrier detected at 4800 bps
50	CARRIER 9600	Carrier detected at 9600 bps
70	PROTOCOL:NONE	Asynchronous mode
71	PROTOCOL:ERROR-CONTROL/LAP-B	Error-control with LAP-B
72	PROTOCOL:ERROR-BUSY CONTROL/LAP-B/HDX	Busy signal detected Error-control with LAP-B HDX
73	PROTOCOL:ERROR-CONTROL/AFT	Error-control with AFT

Command: **Y** **Long Space Disconnect**

Modifier:
- Y0 No recognition or respond to a long space disconnect
- Y1 Recognize and respond to a long space disconnect

Function: Microprocessor and modem

R9696DP?: No long space disconnect function but can implement

Details: The transmission of a long space disconnect sequence can be accomplished by sending a long break sequence or by reconfiguring the modem to synchronous mode and send spaces. If the microprocessor detects the long space sequence, it should clamp the RXD signal to the terminal to a space and then disconnect the modem from the line.

Table 3. AT Commands (Cont'd)

Command:	**Z**	**Recalling a Stored User Profile**
Modifier:		Z0 Resets the modem and recalls user profile 0
		Z1 Resets the modem and recalls user profile 1
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The microprocessor must drive the $\overline{\text{POR}}$ input low then high to reset the modem, and then get the profile and reconfigure the system.
Command:	**&C**	**Carrier Detect Option**
Modifier:		&C0 Carrier detect to the terminal is always active
		&C1 Carrier detect of the modem is provided to the terminal
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The two methods are possible for implementing this function. The microprocessor can drive the DCD pin of the RS-232 connector directly so that it can clamp the line active if that option is selected. The microprocessor, however, will have to monitor the RLSD bit in the modem and drive the RS-232 line appropriately when the bit goes active and inactive. Another method is to gate the RLSD hardware signal with a microprocessor output. The microprocessor output can drive the input of the gate to one polarity to cause DCD to always be active and it can drive the output the other direction to allow DCD to follow the modem's RLSD output.
Command:	**&D**	**Data Terminal Ready Option**
Modifier:		&D0 DTR from the terminal is ignored
		&D1 DTR going on-to-off causes modem to enter command state
		&D2 DTR going on-to-off causes modem to enter command state, hang-up, and disable auto answer
		&D3 DTR going on-to-off causes modem to enter command state and reset the modem
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The microprocessor controls the entering and exiting of the command state as well as implementing the auto answer routine. The microprocessor must control the DTR input of the modem (this can be the bit or the pin) since DTR is the mechanism by which the modem is told to start or terminate a handshake. A modem reset is performed by toggling the $\overline{\text{POR}}$ input.
Command:	**&F**	**Retrieving The Factory Configuration**
Modifier:		none
Function:		Microprocessor
R9696DP?:		N/A
Details:		This command recalls the factory configuration stored in ROM and completely replaces the current configuration.

Table 3. AT Commands (Cont'd)

Command:	&G	**Guard Tone Selection**
Modifier:		&G0 No guard tones &G1 550 Hz guard tone &G2 1800 Hz guard tone
Function:		Modem
R9696DP?:		Yes
Details:		The modem bit GTE, when set to a 1, enables guard tones. When GTS is a 1, 550 Hz guard tone is selected; when GTS is a 0, 1800 Hz guard tone is selected.
Command:	&J	**Telephone Jack Selection**
Modifier:		&J0 RJ11, RJ41S, or RJ45S type &J1 RJ12 or RJ13 type
Function:		Microprocessor
R9696DP?:		N/A
Details:		Option &J0 is for typical use. Option &J1 is for key telephone systems.
Command:	&K	**DTE Flow Control**
Modifier:		&K0 Local flow control disabled &K1 Reserved &K2 Reserved &K3 RTS/CTS local flow control &K4 XON/XOFF flow control &K5 Transparent XON/XOFF flow control
Function:		Microprocessor
R9696DP?:		N/A
Details:		This option is used for error control.
Command:	&L	**Line Type**
Modifier:		&L0 Dial-up line &L1 Leased line
Function:		Modem
R9696DP?:		Yes
Details:		The R9696DP provides a leased-line controlled carrier operation for the V.22 and V.22 bis configurations. Setting the LLn, and CCn bits to a 1 will accomplish this. RTS will then control the state of the carrier whether it is on of off. All the other configurations operate the same whether the modem is in a leased line or dial-up line environment.
Command:	&M	**Communications Mode**
Modifier:		&M0 Asynchronous mode &M1 Asynchronous command mode, synchronous data mode &M2 Synchronous mode, dial a stored number &M3 Synchronous mode, manual dial with talk/data switch
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		Synchronous modem is selected by resetting the ASYNn bits to a 0. Setting the ASYNn bits to a 1 configures the modem for asynchronous mode. WDSZn, STBn, PENn, and EXOSn configure the modem for the correct word size, stop bit number, number of parity bits used, and extended overspeed, respectively.

Table 3. AT Commands (Cont'd)

Command: **&P** **Pulse Dial Parameters**

Modifier:
&P0 39%/61% make/break ratio
&P1 33%/67% make/break ratio

Function: Modem

R9696DP?: Yes

Details: The R9696DP defaults to 36%/64% make/break time. The make and break times for the autodialer can be changed via the RAM write facility of the modem.

RAM Data = Time (sec) * 9600

Function	RAM Address	CR0 bit	Time	Data
Make time	$9C	1	33%	$013D
Make time	$9C	1	39%	$0176
Break time	$1C	1	61%	$024A
Break time	$1C	1	67%	$0283

The pulse dialer in the D code version of the R9696DP does not function. The microprocessor, in this case, will have to pulse the off-hook relay directly using the RA bit.

Command: **&Q** **Communications Mode and Error Control**

Modifier:
&Q0 Asynchronous mode
&Q1 Asynchronous command mode, synchronous data mode
&Q2 Synchronous mode, dial a stored number
&Q3 Synchronous mode, manual dial with talk/data switch
&Q4 AutoSync
&Q5 Error Control

Function: Microprocessor and modem

R9696DP?: Yes

Details: Synchronous modem is selected by resetting the ASYNn bits to a 0. Setting the ASYNn bits to a 1 configures the modem for asynchronous mode. WDSZn, STBn, PENn, and EXOSn configure the modem for the correct word size, stop bit number, number of parity bits used, and extended overspeed respectively.

Command: **&R** **RTS/CTS Option**

Modifier:
&R0 Command state-RTS ignored, On-line CTS follows RTS
&R1 RTS is ignored and CTS is alway active

Function: Microprocessor and modem

R9696DP?: Yes

Details: The two methods are possible for implementing this function. The microprocessor can drive the CTS pin of the RS-232 connector directly so that it can clamp the line active if that option is selected. The microprocessor, however, will have to monitor the CTS bit in the modem and drive the RS-232 line appropriately when the bit goes active and inactive. Another method is to gate the $\overline{CTS}$ hardware signal with a microprocessor output. The microprocessor output can drive the input of the gate to one polarity to cause CTS to always be active and it can drive the output the other direction to allow CTS to follow the modem's CTS output.

Table 3. AT Commands (Cont'd)

Command:	**&S**	**DSR Options**
Modifier:		&S0 DSR always active $S1 DSR operates according to the appropriate specification
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The two methods are possible for implementing this function. The microprocessor can drive the DSR pin of the RS-232 connector directly so that it can clamp the line active if that option is selected. The microprocessor, however, will have to monitor the DSR bit in the modem and drive the RS-232 line appropriately when the bit goes active and inactive. Another method is to gate the DSR hardware signal with a microprocessor output. The microprocessor output can drive the input of the gate to one polarity to cause DSR to always be active and it can drive the output the other direction to allow DSR to follow the modem's DSR output.
Command:	**&T**	**Tests**
Modifier:		&T0 Terminate a test in progress &T1 Local analog loopback &T3 Local digital loopback &T4 Grant remote digital loopback request from remote modem &T5 Deny remote digital loopback request from remote modem &T6 Remote digital loopback &T7 Remote digital loopback with self test &T8 Local analog loopback with self test
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The R9696DP does not generate and test a self test pattern. This function must be performed in the microprocessor. Local digital loopback must also be performed by the microprocessor. The tests are established and terminated using the following bits.

Bit	Function
L2ACT	Locally activated remote digital loopback
L3ACT	Local analog loopback
RDL	Remote digital loopback
RDLE	Remote digital loopback enable

V.22, V.22 bis, and Bell 212A are the only configurations which support the RDL bit. To obtain a remotely activated digital loopback for the remaining configuration, a signalling scheme must be developed between the modems. In this case, the L2ACT bit would be used.

Command:	**&V**	**View Active Configuration and User Profiles**
Modifier:		none
Function:		Microprocessor
R9696DP?:		N/A
Details:		The microprocessor must display the active configuration, user profiles 0 and 1, and stored telephone numbers.

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Table 3. AT Commands (Cont'd)

Command:	**&W**	**Write a Profile to Memory**
Modifier:		&W0 Write the storable parameters of the active configuration to profile 0
		&W1 Write the storable parameters of the active configuration to profile 1
Function:		Microprocessor
R9696DP?:		N/A
Details:		Saves the active configuration of the system.
Command:	**&X**	**Transmit Clock Source**
Modifier:		&X0 Modem generates the transmit clock
		&X1 Terminal generates the transmit clock
		&X2 Modem uses the receive clock as the transmit clock
Function:		Modem
R9696DP?:		Yes
Details:		The TXCLK bits in the R9696DP can be used for this command.
		TXCLK **Function**
		0 Modem generates the transmit clock
		2 Terminal provides the transmit clock
		3 Modem uses the receive clock as the transmit clock
Command:	**&Y**	**Designating The Default User Profile**
Modifier:		&Y0 Profile 0 is designated as the default profile
		&Y1 Profile 1 is designated as the default profile
Function:		Microprocessor
R9696DP?:		N/A
Details:		The microprocessor must use the selected profile on power-up.
Command:	**&Zn=x**	**Store Telephone Number**
Modifier:		n = number location (0-3)
		x = telephone number
Function:		Microprocessor
R9696DP?:		N/A
Details:		This command allows the storage of up to four telephone numbers.
Command:	**+++**	**Escape Code**
Modifier:		none
Function:		Microprocessor
R9696DP?:		N/A
Details:		Used to exit from on-line mode to command mode.
Command:	**<CR>**	**Carrage Return**
Modifier:		none
Function:		Microprocessor
R9696DP?:		N/A
Details:		Used to terminate a command line

Table 4. S Registers

Register:	**S0**	**Rings to Answer On**
Range:		0 - 255 rings
Default:		0
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The R9696DP has a ring detector which can be monitored by the microprocessor. When the desired amount of rings are detected, the microprocessor can place the modem off-hook by setting the RA bit in the modem. When S0 is 0, auto answer is disabled.
Register:	**S1**	**Ring Count**
Range:		0 - 255 rings
Default:		0
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The R9696DP has a ring detector which can be monitored by the microprocessor. When the rings are detected, the microprocessor can increment the S1 location.
Register:	**S2**	**Escape Sequence Character**
Range:		0 - 127 ASCII
Default:		43 (+)
Function:		Microprocessor
R9696DP?:		N/A
Details:		Used to exit from on-line mode to command mode. A value greater than 127 disables the escape sequence preventing the modem from returning to the command state.
Register:	**S3**	**Carriage Return Character**
Range:		0 - 127 ASCII
Default:		13
Function:		Microprocessor
R9696DP?:		N/A
Details:		Used to terminate a command line.
Register:	**S4**	**Line Feed Character**
Range:		0 - 127 ASCII
Default:		10
Function:		Microprocessor
R9696DP?:		N/A
Details:		Used to terminate a command line.
Register:	**S5**	**Backspace Character**
Range:		0 - 32, 127 ASCII
Default:		8
Function:		Microprocessor
R9696DP?:		N/A
Details:		Used to delete characters in the command line.

Table 4. S Registers (Cont'd)

Register:	**S6**	**Wait Time Before Blind Dialing**
Range:		2 - 255 seconds
Default:		2 seconds
Function:		Microprocessor
R9696DP?:		N/A
Details:		After the off-hook relay is closed, a delay specified by S6 should be performed before dialing the first digit. This delay is to ensure that dial tone is present on the line before dialing the first digit.
Register:	**S7**	**Wait Time for Carrier/Dial Tone**
Range:		1 - 255 seconds
Default:		30 seconds
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		S7 determines the wait time between dialing and responding to an incoming carrier signal. S7 also is used for the W dial modifier as the time the dialer will wait for the detection of dial tone. RLSD can be used for carrier detection and TONEA is preprogrammed for the bandwidth which contains the dial tone frequencies.
Register:	**S8**	**Duration of Comma Dial Modifier**
Range:		0 - 255 seconds
Default:		2 seconds
Function:		Microprocessor
R9696DP?:		N/A
Details:		This is the delay time used for the comma dial modifier.
Register:	**S9**	**Carrier Detect Response Time**
Range:		1 - 255 1/10 seconds
Default:		6 seconds
Function:		Microprocessor and modem
R9696DP?:		No
Details:		S9 determines how many seconds a carrier must be present before the modem will recognize it as a carrier. The user can monitor FED and RLSD and can make a determination whether or not the DCD signal should be activated or not. The RLSD response time can not be changed in the R9696DP.
Register:	**S10**	**Delay Between Carrier Loss and Hang-up**
Range:		1 - 255 1/10 seconds
Default:		1.4 seconds
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		S10 specifies the delay between the loss of the remote carrier and the local modem disconnecting from the line. This can be done by monitoring RLSD. When RLSD goes inactive, delay the amount of time specified in S10 and check RLSD again. If RLSD is still inactive, write a 0 into RA to open the off-hook relay. Setting S10 to 255 causes the modem to ignore the actual carrier status and assume the carrier is always present.

Table 4. S Registers (Cont'd)

Register:	S11	**DTMF Tone Duration and Interdigit Delay**
Range:		50 - 255 milliseconds
Default:		95 milliseconds
Function:		Modem
R9696DP?:		Yes
Details:		The DTMF tone duration and interdigit delay can be programmed via the RAM write facility in the R9696DP. The default duration is 95 ms and the default interdigit delay is 70 ms.
		RAM Data = Duration (sec) * 9600

Function	RAM Address	CR0 bit	Duration	Data
DTMF Duration	$9A	1	95 ms	$0390
Interdigit Delay	$1A	1	95 ms	$0390

Register:	S12	**Escape Sequence Guard Time**
Range:		0 - 255 1/50 seconds
Default:		1 second
Function:		Microprocessor
R9696DP?:		N/A
Details:		S12 holds the delay required prior to and following the escape sequence.
Register:	S13 - S17	
Range:		none
Default:		N/A
Function:		N/A
R9696DP?:		N/A
Details:		Reserved
Register:	S18	**Modem Test Timer**
Range:		0 - 255 seconds
Default:		0
Function:		Microprocessor
R9696DP?:		N/A
Details:		This register establishes the length of the modem tests.
Register:	S19 - S24	
Range:		none
Default:		N/A
Function:		N/A
R9696DP?:		N/A
Details:		Reserved

Table 4. S Registers (Cont'd)

Register: **S25** **DTR Detection**
Range: 0 - 255 1/100 seconds
Default: 5 seconds
Function: Microprocessor
R9696DP?: N/A
Details: In synchronous mode 1 and 4, the time specified by this register is the amount of time DTR from the terminal is ignored after a connection is established. During this time the units are seconds, not 1/100 seconds. This allows the user to disconnect an asynchronous terminal and connect a synchronous terminal to the modem. Once the connection is made (this applies to the other modes as well) the units are 1/100. Any change of DTR which is shorter than the time specified by S25 is ignored.

Register: **S26** **RTS to CTS Interval**
Range: 0 - 255 1/100 seconds
Default: .01 seconds
Function: Microprocessor and modem
R9696DP?: Yes
Details: S26 is used to specify the RTS active to CTS active delay. This value takes effect when the &R0 command has been executed. This applies to synchronous mode 1, 2, and 3 only.

The RTS to CTS delay can be programmed via the RAM write facility of the R9696DP.

Function	RAM Address	CR0 Bit
RTS/CTS delay	$10	1

Response Time Equations

Configuration	Equation
V.32	N=(time*2.4)ms –1
V.22 bis, V.22, Bell 212A	N=(time*0.6)ms –1
V.23, Bell 103	N=time*9.6 ms
V.21	N=time*7.68

Response Time Values

Configuration	Default (Dec.)	Value (Hex.)	Min. (Dec.)	Value (Hex.)
V.32	0.4 ms	$0000	0.4 ms	$0000
V.22 bis, V.22, Bell 212A	1.6 ms	$0000	1.6 ms	$0000
V.23, Bell 103	210 ms	$07E0	0 ms	$0000
V.21	500 ms	$0F00	0 ms	$0000

To obtain the minimum time specified by S26, the RTS to CTS delay seen at the RS-232 connector must be controlled by the microprocessor instead of the R9696DP for those configurations which do not have a minimum RTS to CTS response time of 0 ms.

Table 4. S Registers (Cont'd)

Register:	S27 - S35	
Range:		none
Default:		N/A
Function:		N/A
R9696DP?:		N/A
Details:		Reserved
Register:	S36	**Negotiation Failure Treatment**
Range:		0,1
Default:		1
Function:		Microprocessor
R9696DP?:		N/A
Details:		This register tells the modem how to respond if an error correction connection fails.
Register:	S37	**DCE Line Speed**
Range:		0 - 9
Default:		0
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		The modem attempts to connect with a remote modem at the highest supported DCE data rate that does not exceed the value specified by S37. 0 = Connect at speed of last AT command 1-3 = Connect at 300 bps 4 = Reserved 5 = Connect at 1200 bps 6 = Connect at 2400 bps 7 = Connect at 4800 bps 8 = Reserved 9 = Connect at 9600 bps The R9696DP can automatically fallback and fall forward in V.32. The modem also can fallback and fall forward from V.22bis to V.22. Any other interworking must be performed manually by the microprocessor detecting what the remote modem is. This can be done by programming the tone detectors to recognize the beginning of various handshakes. After a handshake is recognized the microprocessor can reconfigure the modem.
Register:	S38	**Delay Before Forced Hang-up**
Range:		0 - 255 seconds
Default:		20 seconds
Function:		Microprocessor and modem
R9696DP?:		Yes
Details:		S38 specifies the delay between a command to hang-up (or the on-to-off transistion of DTR if programmed) and the actual disconnection of the line. This is useful in the error correction configuration to ensure that all the data in the transmit buffer is transmitted. If the value in S38 is 255, the modem does not timeout and will continue to transmit until the connection is lost.

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Image Modem Application Notes

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Rockwell

R96FI/R96MD Modem Tone Detector Filter Tuning

INTRODUCTION

The Rockwell R96FI and R96MD modems include three independent tone detectors (FR1, FR2 and FR3). These tone detectors are operational when the modem is configured for V.21 FSK, and are centered upon power-up to 2100 Hz (FR1), 1100 Hz (FR2), and 462 Hz (FR3). This application note presents a method of tuning these detectors to any desired frequency in the 400 Hz - 3 kHz band.

COMPUTATION OF TONE DETECTOR COEFFICIENTS

Each tone detector consists of two second-order filters in cascade, an energy averaging filter, and a threshold comparator. A diagram of the tone detector is shown in Figure 1.

Filter 1 has a transfer function:

$$H_1(Z) = \frac{2\alpha}{1 - 2\beta_1 Z^{-1} - 2\beta_2 Z^{-2}} \qquad \text{(Eq. 1)}$$

Filter 2 has a transfer function:

$$H_2(Z) = \frac{2\alpha'}{1 - 2\beta'_1 Z^{-1} - 2\beta'_2 Z^{-2}} \qquad \text{(Eq. 2)}$$

The energy averaging filter has a transfer function:

$$H_3(Z) = \frac{2\alpha''}{1 - \beta'' Z^{-1}} \qquad \text{(Eq. 3)}$$

The output of the energy averager is fed to a threshold comparator which sets, or resets, the appropriate bit (FR1, FR2 and FR3) in the signal processor (SP) scratchpad memory if the energy output is equal to or greater than 1/8, or less than 1/8, respectively.

Filters 1 and 2 have a typical frequency response as shown in Figure 2. When cascaded, they form a bandpass filter with a narrow bandwidth as shown in Figure 3.

Given the transfer functions $H_1(Z)$ and $H_2(Z)$, an analytical method is required to compute their coefficients for any desired frequency in the 400 Hz - 3 kHz band. First, consider $H_1(Z)$. This transfer function can be rewritten as:

$$H_1(Z) = \frac{2\alpha Z^2}{Z^2 - 2\beta_1 Z - 2\beta_2} \qquad \text{(Eq. 4)}$$

which has a conjugate pair of poles:

$$P_1 = \beta_1 + j\sqrt{(\beta_1^2 + 2\beta_2)}$$

$$P_2 = \beta_1 - j\sqrt{(\beta_1^2 + 2\beta_2)}$$

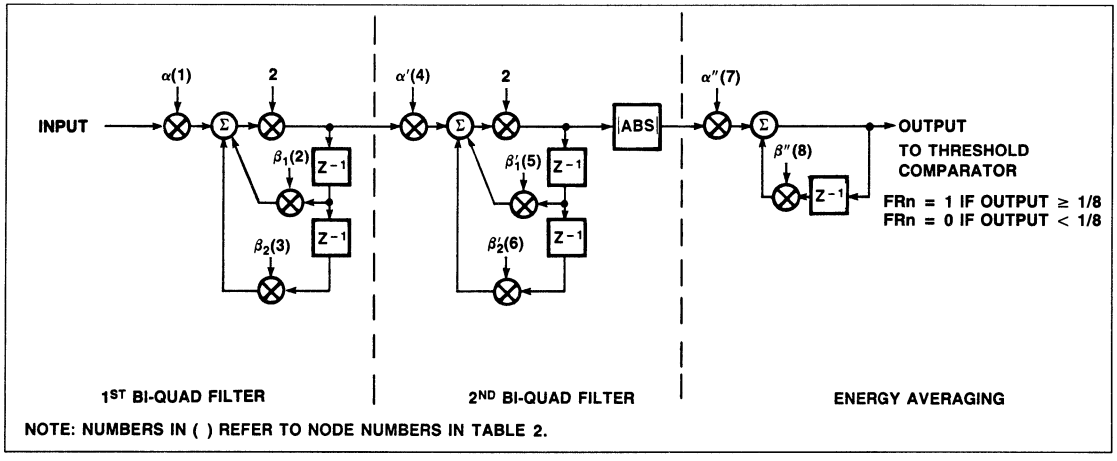

Figure 1. Tone Detector Diagram

These poles lie on a circle of radius 0.994030884 on the Z-plane. The radius of the tone detector circle was chosen so that each filter has a high Q without being unstable (i.e., poles must lie inside the unit circle for stability). Figure 4 shows a Z-plane pole-zero diagram for an arbitrary conjugate pole pair on the tone detector circle. The angle $\theta = 360^\circ \times f_O/f_S$, where f_O is the desired center frequency and f_S is the sampling rate (f_S = 9600 Hz). The following equations are derived from the angle and magnitude of the position vector pointing to a pole pair located at the desired angle:

$$\cos^{-1}(\beta_1/r) = \theta = 360^\circ \times f_O/f_S \quad \text{(Eq. 5)}$$

$$\sqrt{[\beta_1^2 + (-\beta_1^2 - 2\beta_2)]} = r = 0.994030884 \quad \text{(Eq. 6)}$$

Solving for β_1 and β_2:

$$\beta_1 = r \cos (360^\circ \times f_O/f_S) \quad \text{(Eq. 7)}$$

$$\beta_2 = -r^2/2 \quad \text{(Eq. 8)}$$

In deriving these equations, only $H_1(Z)$ was considered. However, the tone detector consists of two identical filters in cascade. Referring to figure 5, shifting filter 1 and filter 2 above and below the desired center frequency, a response with the desired bandwidth is achieved. Furthermore, since α controls the amplitude response, one may set $\alpha = \alpha'$ to uniformly raise or lower the overall cascade response.

From Equation 8, we see that:

$$\beta_2 = \beta'_2 = -r^2/2 = -0.494048699$$

Rewriting Equation 7 in terms of the offsets f_A and f'_A:

$$\beta_1 = r \cos [360^\circ (f_O - f_A)/f_S] \quad \text{(Eq. 9)}$$

$$\beta'_1 = r \cos [360^\circ (f_O + f'_A)/f_S] \quad \text{(Eq. 10)}$$

The frequency offset is approximately 72% of B/2 (half the bandwidth):

$$f'_A \cong 0.72\ (B/2) \quad \text{(Eq. 11)}$$

The value of f_A should be equal to f'_A. However, f_A may be chosen 1% smaller than f'_A to compensate for the fact that the overall cascade response is not prefectly symmetrical (see Figure 5).

The values for the coefficient α and α' that set $|H(f_O)|$ = 0 dB in equations 1 and 2 were measured and plotted versus center frequency f_O as shown in Figure 6.

Three equations corresponding to three linear approximations result:

$$\alpha = \alpha' = \frac{(104/319)f_O - 78.62}{32767}$$

$$400 \le f_O \le 1100 \text{ Hz} \quad \text{(Eq. 12a)}$$

$$\alpha = \alpha' = \frac{(44/275)f_O + 104}{32767}$$

$$1100 \le f_O \le 1650 \text{ Hz} \quad \text{(Eq. 12b)}$$

$$\alpha = \alpha' = \frac{(4/45)f_O + 221}{32767}$$

$$1650 \le f_O \le 3000 \text{ Hz} \quad \text{(Eq. 12c)}$$

ENERGY AVERAGING FILTER

The coefficients of the energy averaging filter are determined by a Z-domain approximation to an RC circuit of transfer function: $H(S) = 1/1 + S\tau$.

$$\alpha'' = \frac{1}{1 + 9600\tau} \quad \text{(Eq. 13)}$$

$$\beta'' = \frac{1}{(1 + 1/9600\tau)} \quad \text{(Eq. 14)}$$

Upon power-up, α'' and β'' are set for τ = 0.1 seconds. Unless different tone detector response times are required, these coefficients need not be changed.

Table 1 contains the computed values of the filter coefficients, including those of default frequencies 462 Hz, 1100 Hz, and 2100 Hz. The value 32767 (hex 7FFF) is full scale in the SP's machine untis (i.e., 32767 = unity). Coefficients may range from -1 to +1 (or FFFF to 7FFF in machine units).

WRITING NEW COEFFICIENTS INTO THE SIGNAL PROCESSOR (SP) RAM

The RAM ACCESS B register (1:F) allows the host processor to specify an access code for RAM data registers. The access code specifies the RAM location being written. Table 2 contains the RAM access codes for all filter coefficients.

The proper procedure for writing new coefficients into the SP RAM is as follows:

1. Store the desired access code into register 1:F.
2. Read Register 1:0 to reset MDA1.
3. Wait for bit MDA1 (1:E:0) to be a 1.
4. Set the RAM write bit (1:D:0)
5. Write the two halves of the 16-bit coefficient into registers 1:1 and 1:0. (Register 1:1 is the MSB.)
6. Wait for bit MDA1 (1:E:0) to be a 1.
7. If more data is to be written, change RAM access code and go to step 5.
8. Reset RAM write bit (1:D:0).

Writing to Register 1:0 resets MDA1 (1:E:0) to a 0 and starts the write cycle, which ends by MDA1 returning to a 1. The RAM write bit (1:D:0) must remain set until the end of the cycle.

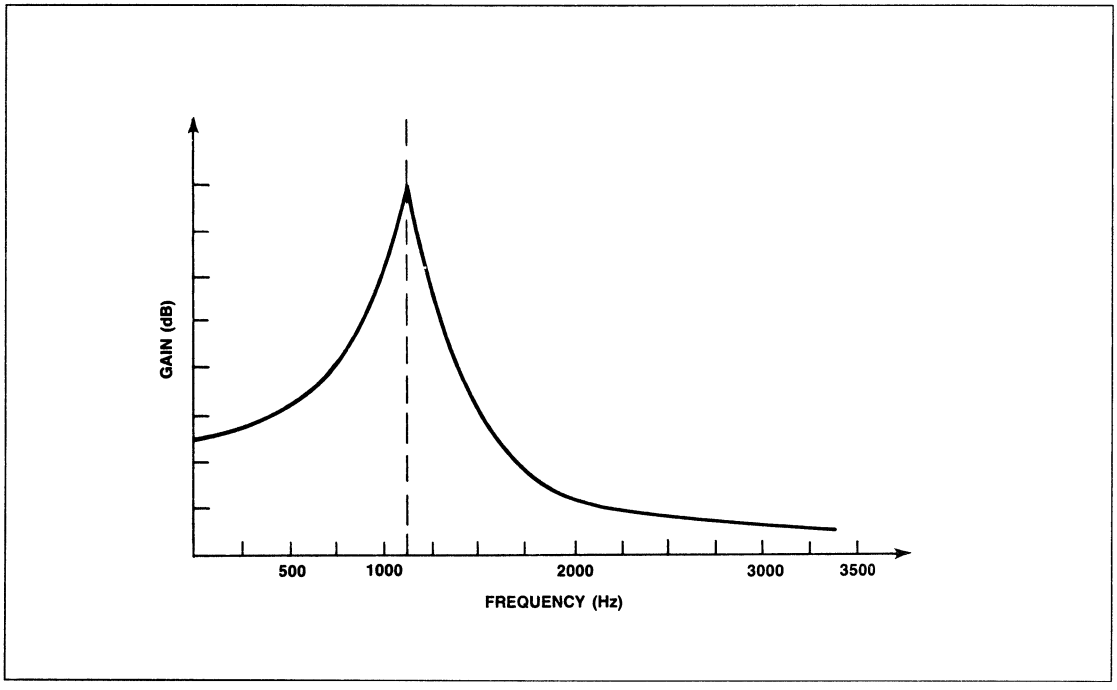

Figure 2. Typical Single Filter Response

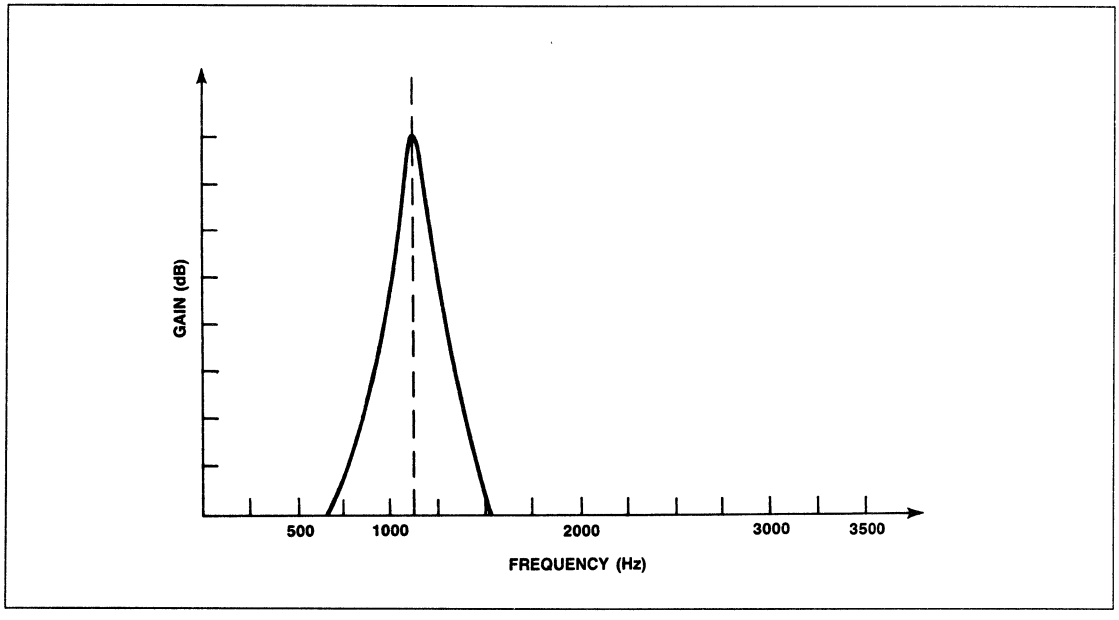

Figure 3. Typical Cascade Filter Response

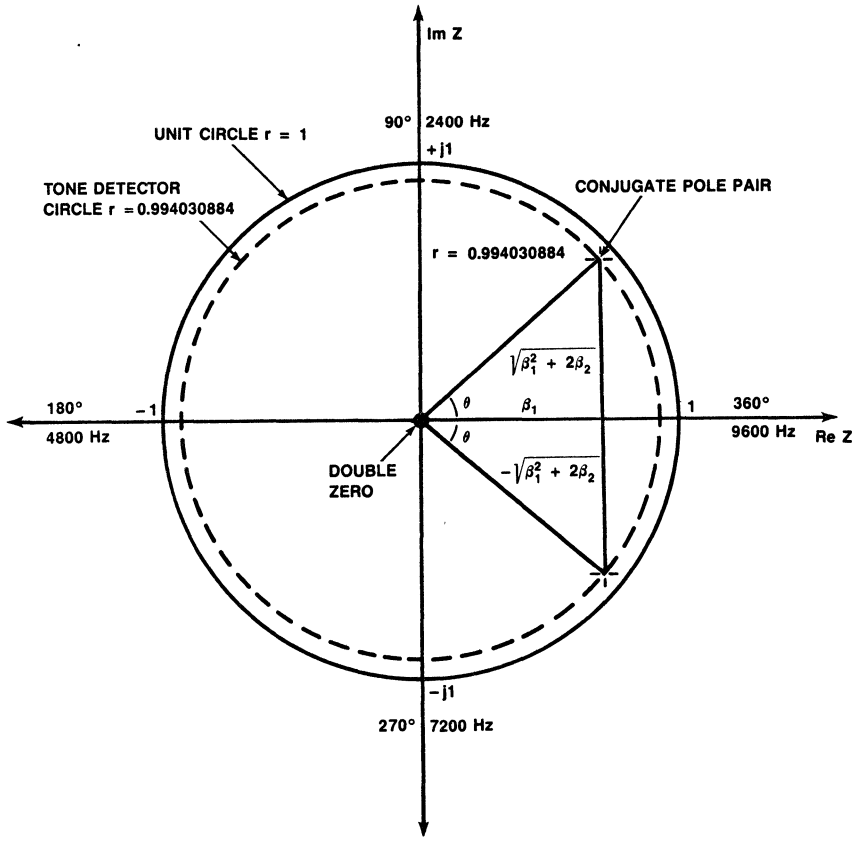

Figure 4. Z-Plane Pole-Zero Diagram

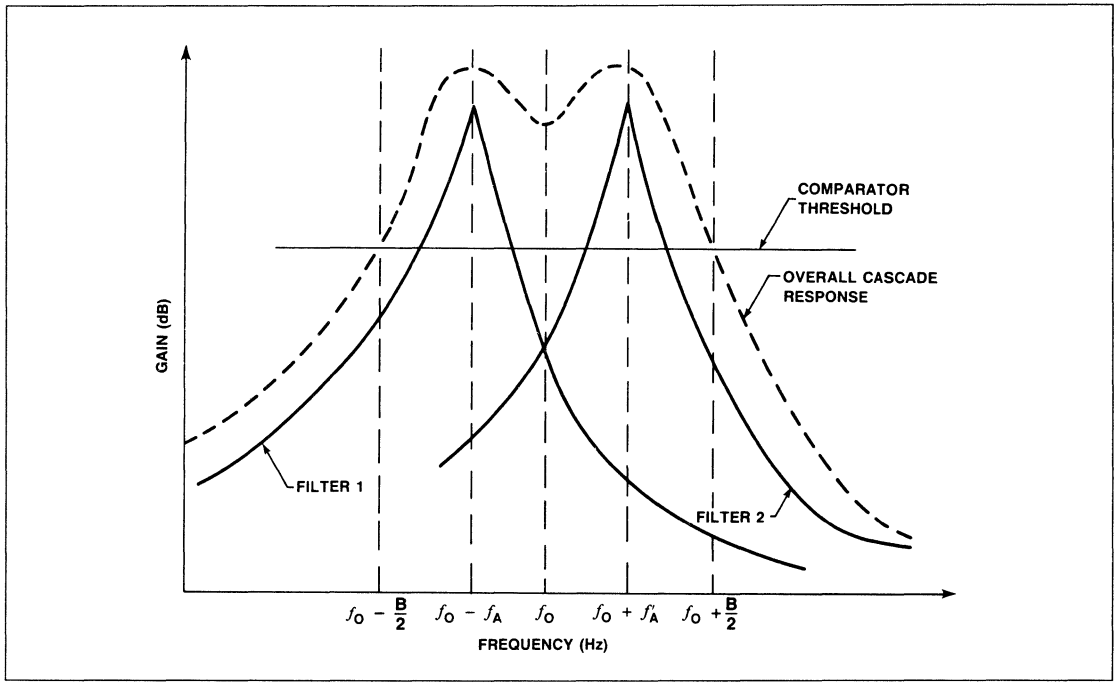

Figure 5. Bandwidth and Offset Frequencies

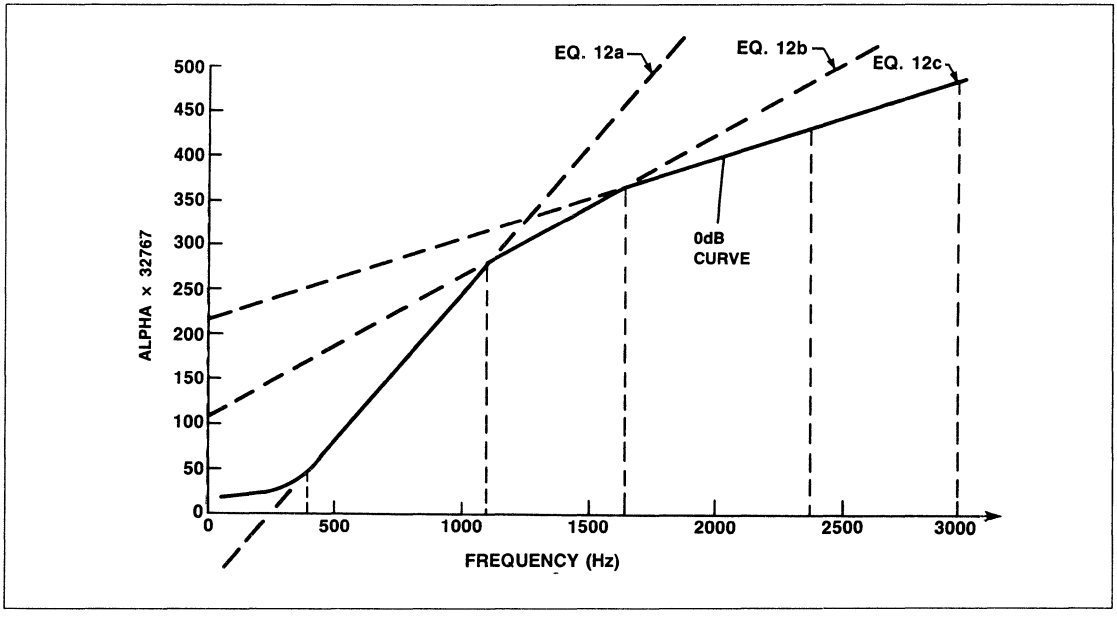

Figure 6. Alpha-zero Center Frequency

Table 1. Calculated Coefficient Values

Frequency Detected	Coefficient Name	Coefficient Value	
		Hex	Decimal
2100 Hz ±25 Hz	$\alpha = \alpha'$	0198	408/32767
	β_1	1A4A	6730/32767
$f_A \approx 18$ Hz	β'_1	175A	5978/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
1850 Hz ±24 Hz	$\alpha = \alpha'$	0180	384/32767
	β_1	2E37	11831/32767
$f_A \approx 18$ Hz	β'_1	2B69	11113/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
1650 Hz ±23 Hz	$\alpha = \alpha'$	0170	368/32767
	β_1	3D48	15688/32767
$f_A \approx 18$ Hz	β'_1	3AA6	15014/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
1100 Hz ±30 Hz	$\alpha = \alpha'$	0118	280/32767
	β_1	60BE	24754/32767
$f_A \approx 19$ Hz	β'_1	5E9C	24220/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
462 Hz ±14 Hz	$\alpha = \alpha'$	0048	72/32767
	β_1	79F3	31219/32767
$f_A \approx 10$ Hz	β'_1	7974	31092/32767
	$\beta_2 = \beta'_2$	C083	–16253/32767

Table 2. Filter Coefficients Access Codes

Node No. (n)	Name	Access Code (Hex)		
		FR1	FR2	FR3
1	α	2E	34	3A
2	β_1	2F	35	3B
3	β_2	30	36	3C
4	α'	2B	31	37
5	β'_1	2C	32	38
6	β'_2	2D	33	39
7	α''	B7	B9	BB
8	β''	B8	BA	BC

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R96FI/R96MD Modem Recommended Receive Sequence for Group 2 Facsimile

INTRODUCTION

The R96FI and R96MD include a transmit and receive configuration that is compatible with the transmission scheme of Group 2 facsimile equipment. In order to achieve the best results with Group 2 reception, the following procedure is recommended. The step numbers are keyed to points in Figure 1. Refer to the respective data sheets, R96FI (MD06) and R96MD (MD34) for details on how to configure the modem and write modem data to chip one.

METHOD

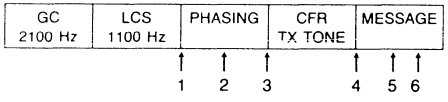

Figure 1. Group 2 Facsimile Sequence

1. Enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Write hex 0038 using access code C2. This action sets the Group 2 phase-locked-loop (PLL) for a frequency correction of 9 Hz, causing the phase term to drift rapidly to overcome any tendency to slow phase recovery.
   b. Write hex 4000 using access code F1, and hex 7FFF using access code 71. This action allows the Group 2 PLL to accept the greatest number of samples for carrier recovery during phasing.
   c. Write hex 2000 using access code AA. This action sets the AGC slew rate for very fast acquisition.
   d. Set control bit G2FGC (1:C:0) to a one to select fast AGC state.
2. After phasing is detected, wait approximately 2 seconds for the AGC circuit to settle. Then:
   a. Write hex 0000 using access code AA. This action stops AGC tracking in order to preserve the present AGC setting.
   b. Reset control bit G2FGC (1:C:0) to a zero to select slow AGC state. This action changes the Group 2 PLL characteristics to match reduced AGC response.
   c. Read and save the 16-bit value from registers 1:3 and 1:2 using access code C2. This value represents the frequency error term from the Group 2 PLL.
   d. Verify that phasing signal is still being received. This action guarantees that AGC value was frozen during phasing signal.
   e. If step d above determines that phasing signal is present, allow transmission of CFR. If phasing signal is not present, suppress CFR.
3. Exit Group 2 configuration.
4. At completion of CFR transmission, re-enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Repeat step 1.b.
   b. Repeat step 2.a.
   c. Add hex 0038 to the value saved in step 2.c above and write the sum using access code C2. This action forces a 9 Hz error as in step 1.a.
5. Wait for start of Group 2 message transmission. Then:
   a. Write hex 0400 using access code AA. This action restores the AGC slew rate to the default value.
   b. After 2 lines, write the value saved in step 2.c using access code C2. This action removes the 9 Hz forced frequency error without waiting for the phase-locked-loop to complete the correction. This step is optional as the correction will eventually be completed, but, depending on the percentage of white in the document being sent, the correction may take from 4 to 16 lines (100 ms of white required).

5

6. After approximately 6 to 10 seconds of message reception, perform either step a or step b below:
   a. Write hex 6100 using access code F1, and hex 0600 using access code 71. This action places narrow limits on the received signal used for carrier recovery during message reception and reduces the chance of errors caused by repeated patterns in the message.
   b. Synchronize the modem's Group 2 PLL to the facsimile machine's blanking signal as follows:
      (1) Freeze the phase-locked-loop during data by:
         (a) Writing hex 7FFF using access code F1.
         (b) Writing hex 0000 using access code 71.
      (2) Enable the phase-locked-loop during the white margins by:
         (a) Writing hex 4000 using access code F1.
         (b) Writing hex 7FFF using access code 71.
         (c) The sequence of writing in step 6.b is important and must be performed as described. Option 6.b requires more action by the host processor, but it eliminates the possibility of data patterns affecting carrier recovery.

PARAMETER SCALING

1. Access code C2 represents frequency error, i.e., the deviation of received carrier from 2100 Hz.

   LSB = 0.167 Hz; Range = ± 140 Hz

2. Access code F0 represents the Group 2 PLL slew rate for the first order term. The number is directly proportional to slew rate. The range of stable operating values is 0010 to 7000 in hexadecimal.
3. Access code AA represents the AGC slew rate.

   Range = 0000 to 7FFF in hexadecimal

   Scaling: See Figure 2.

4. Access codes F1 and 71 represent limits on acceptable zero crossing for use by the carrier recovery loop. The carrier recovery loop uses several nonlinear controls in attempting to lock the zero crossing of the local carrier to those of the transmitter. Since Group 2 facsimile uses VSB transmission, it is necessary to either reconstruct the upper sideband or exclude those zero crossings that represent frequencies other than 2100 Hz. The modem excludes unwanted zero crossings by testing the effective slope of the waveform as it crosses zero. In Figure 3, points A and B represent samples taken about a zero crossing over a sample period T, where T = 1/10,368 seconds.

   The magnitude of |A| + |B| is directly proportional to the slope of line segment AB and is, therefore, an indicator of frequency. If H represents the value stored at F1 and L represents the value at 71, then 1 – [|A| + |B|] + H must be less than positive full scale or the frequency is excluded for being too low. Also, 1 – [|A| + |B|] + H + L must be greater than positive full scale or the frequency is excluded for being too high.

   The average value for 1 – [|A| + |B|] with an all white transmission and back-to-back connection is hex 19A1 ± 0543.

5. Access code hex 00F2 in chip 1 allows host control of the limits placed on phase error correction. When the phase error exceeds the limit set by F2, PLL updating is suspended. The default value of 5000 corresponds to a limit of ± 67.5 degrees. A zero in F2 causes the PLL to update for any phase error. By resetting F2 to a zero, it may be unnecessary to force a frequency offset in the receive sequence.

   For systems using step 6.a in the receive sequence, reception of messages containing a large amount of black may be improved by setting F2 to zero. F2 scaling is:

   Phase limit = 180° – [(F2 value/7FFF) x 180°]

   Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits, etc.

BLACK/WHITE THRESHOLD

The R96FI/R96MD receives a Group 2 baseband signal that contains density (gray scale) information in the amplitude modulation. In order for this information to be used on a Group 3 facsimile machine, the modem converts the gray scale to black/white baseband form. The threshold at which the black/white decision is made determine the density of the received page.

Access code 2A represents the Group 2 black/white threshold. This location defaults to hex 7800 at POR time. The number may be increased or decreased by the host to achieve a page weighted more toward white or toward black, respectively.

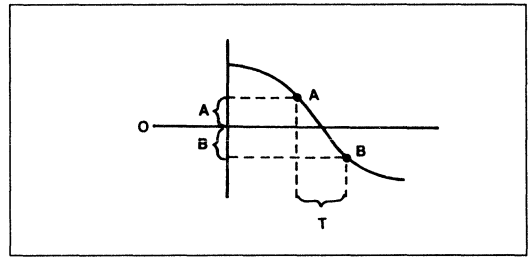

Figure 3. Samples of Zero Crossing

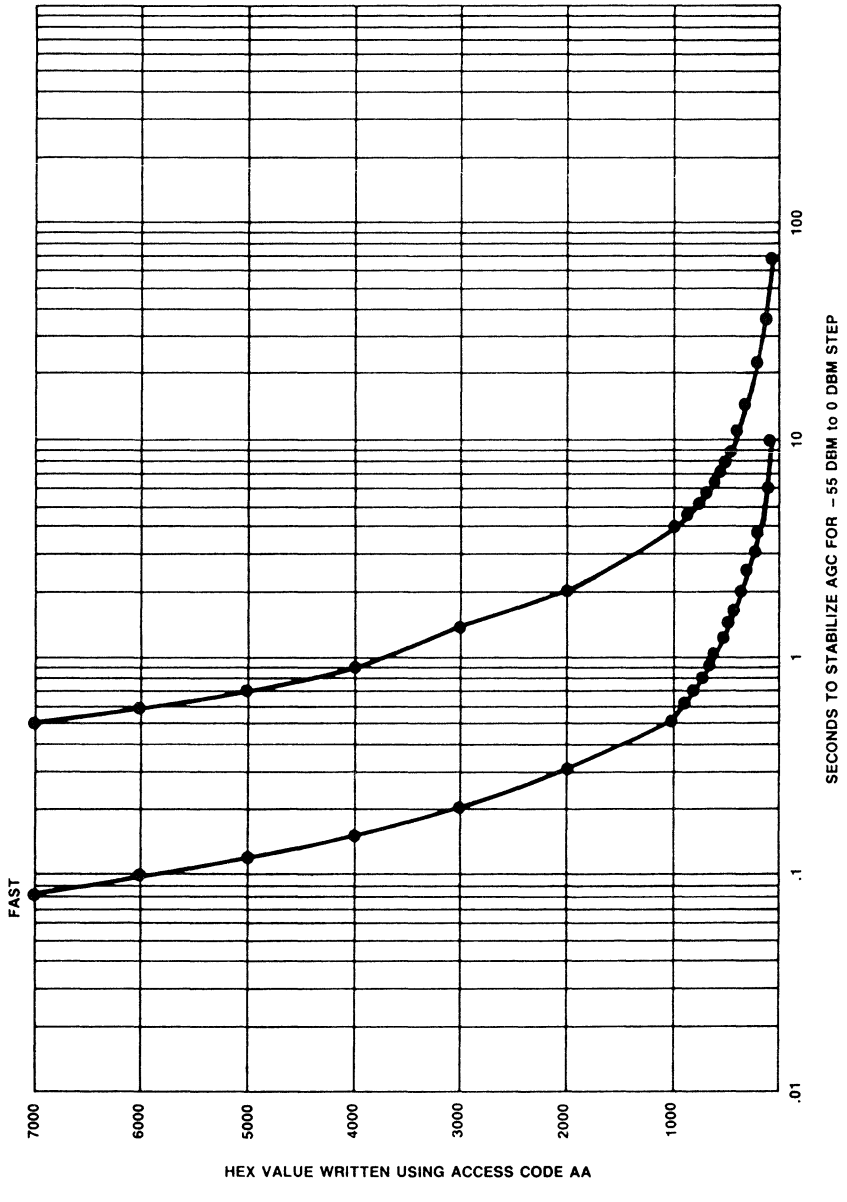

Figure 2. AGC Slew Gain

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DTMF Dialing Using the R96MD Modem

INTRODUCTION

The R96MD modem includes tunable oscillators that can be used to perform dual-tone multi-frequency (DTMF) dialing. The frequency and amplitude of each oscillator output is under host control. A programmable tone detector can also be used in call establishment to recognize an answer tone.

This application note describes the method of oscillator and filter tuning by the host processor and provides an example of an autodialer routine that may be programmed into the host.

DTMF REQUIREMENTS

EIA Standard RS-496, paragraph 4.3.2, specifies requirements that ensure proper DTMF signaling through the public switched telephone network (PSTN). These tones consist of two sinusoidal signals, one from a high group of three frequencies and one from a low group of four frequencies, that represent each of the standard pushbutton telephone characters shown in Table 1.

Table 1. DTMF Signals

Low Frequency	High Frequency		
	1209 Hz	1336 Hz	1477 Hz
697 Hz	1	2	3
770 Hz	4	5	6
852 Hz	7	8	9
941 Hz	*	0	#

Signal power is defined for the combined tones as well as for the individual tones. Both maximum and minimum power requirements are functions of loop current. By combining the various requirements of RS-496, compromise power levels can be determined that meet the power specification for all U.S. lines (when driving the PSTN from a 600 ohm resistive source). The high frequency tone should be at a higher power level than the low frequency tone by approximately 2 dB. The maximum combined power, averaged over the pulse duration, should not exceed +1 dBm. The minimum steady state power of the high frequency tone should not be less than –8 dBm. When connecting the modem circuit to the PSTN by means of a data access arrangement (DAA) set for permissive mode, the DAA gain is –9 dB. The modem circuit must, therefore,drive the DAA input with +1 dBm of steady state high frequency power and –1 dBm of steady state low frequency power in order to meet all of the listed conditions. Since +0.5 dBm is the maximum undistorted power level for individual tones generated by the modem, the user may need to add gain in front of the DAA during DTMF dialing.

The required duration of the DTMF pulse is 50 ms minimum. By experience, a pulse duration of approximately 95 ms is more reliable. The required interval between DTMF pulses is 45 ms minimum and 3 seconds maximum. Again, by experience, an interdigit delay of approximately 70 ms is preferred.

The remaining requirements of RS-496, relative to DTMF dialing, are not influenced by the host processor. These requirements are all met by the modem's oscillators.

SETTING OSCILLATOR PARAMETERS

The oscillator frequency and output power are set by the host computer in DSP RAM using the microprocessor bus and diagnostic data routine. For a description of the microprocessor bus and other interface considerations, refer to the R96MD modem data sheet (Order Number MD34).

When setting the frequency of tone 1, the host must write a 16-bit hexadecimal number into RAM using RAM access code 71 with bit RAE = 1. When setting the frequency of tone 2, a 16-bit hexadecimal number must be written into RAM using RAM access code 71 with bit RAE = 0. The power levels of tone 1 and tone 2 are set by writing 16-bit hexadecimal numbers into RAM using RAM access code 72 with bit RAE = 1, and with RAE = 0, respectively. The hexadecimal numbers written into these RAM locations are scaled as follows:

Frequency number = 6.8267 (desired frequency in Hz)

Power number = $15360\ [10^{(Po/20)}]$

Where Po = output power in dBm with a series 600 ohm resistor into a 600 ohm load.

These decimal numbers must be converted to hexadecimal form then stored in RAM by following the RAM data write routine illustrated by Figure 1. Hex 3FFF is the maximum value of Power level number without harmonic distortion.

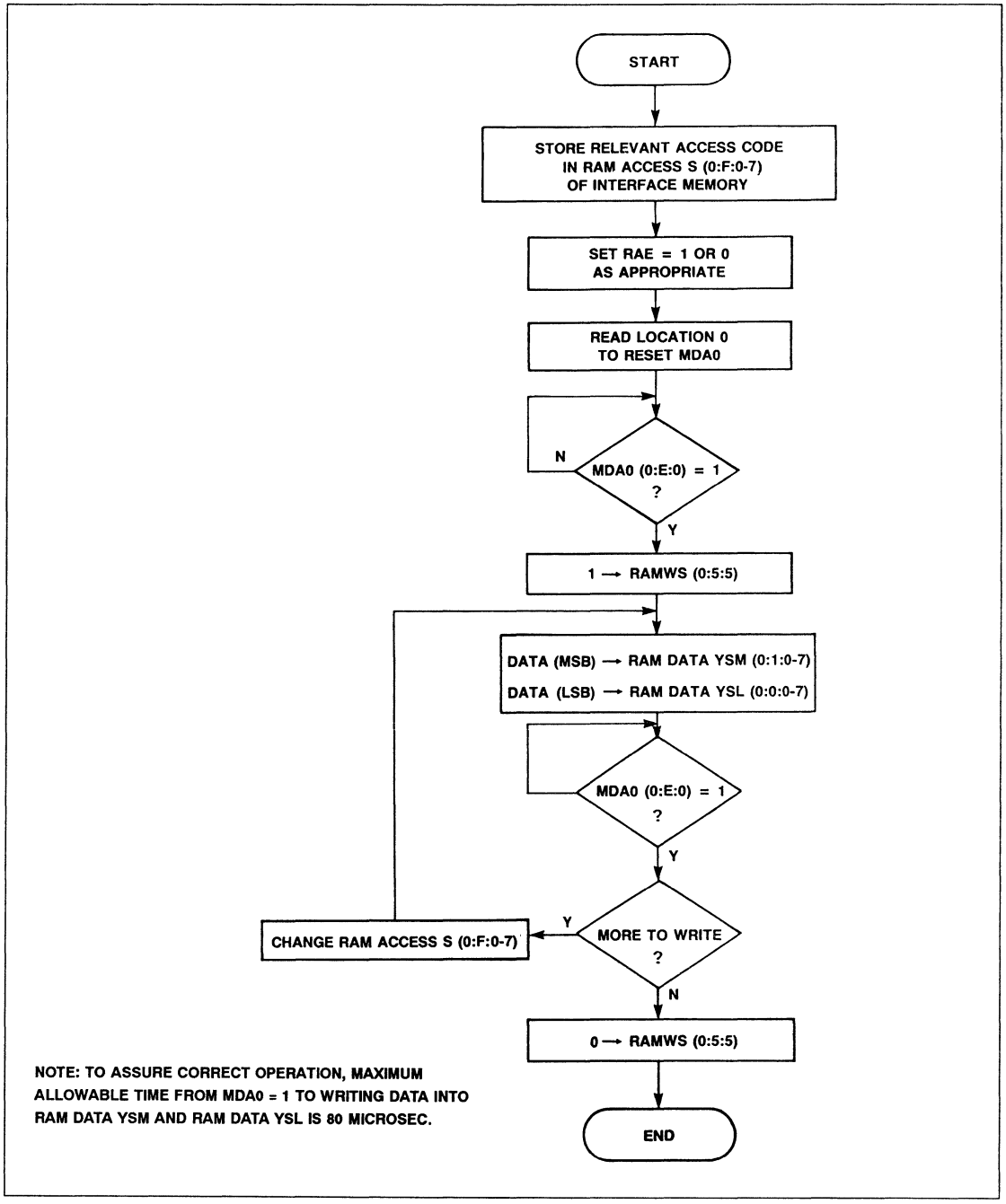

Figure 1. RAM Data Write Routine

Hexadecimal numbers for DTMF generation are listed in Table 2. Power levels are selected to give the desired output power for each tone (0 dBm for the high frequency tone and –2 dBm for the low frequency tone) while compensating for modem filter characteristics.

Table 2. DTMF Parameters

Digit	RAM Access S	RAE	Value (Hex)
	71	1	1918
	71	0	23A0
0	72	1	32BE
	72	0	3FBE
	71	1	1296
	71	0	203D
1	72	1	32F1
	72	0	3FFF
	71	1	1296
	71	0	23A0
2	72	1	32F1
	72	0	3FBE
	71	1	1296
	71	0	2763
3	72	1	32F1
	72	0	3F6C
	71	1	1488
	71	0	203D
4	72	1	3327
	72	0	3FFF
	71	1	1488
	71	0	23A0
5	72	1	3327
	72	0	3FBE
	71	1	1488
	71	0	2763
6	72	1	3327
	72	0	3F6C
	71	1	16B8
	71	0	203D
7	72	1	330B
	72	0	3FFF
	71	1	16B8
	71	0	23A0
8	72	1	330B
	72	0	3FBE
	71	1	16B8
	71	0	2763
9	72	1	330B
	72	0	3F6C

DETECTING ANSWER TONE

Frequency detector bit FR1 (1:B:5) can be used to detect a 2100 Hz answer tone when connection to the remote modem is successful. Bit FR1 goes active (one) when energy above the turn-on threshold is present at 2100 Hz ±25 Hz. At the end of the answer tone, FR1 returns to zero and data transmission can begin.

COMPLETE CALLING SEQUENCE

A complete calling sequence consists of several steps including modem configuration, telephone number selection, DTMF transmission, and answer tone detection. A sample flow chart for implementing an auto-dialer in host software is illustrated in Figure 2.

The auto-dialer routine may be entered at one of two points; either AUTO DIAL or REDIAL. When entering at AUTO DIAL, the host prompts the user to enter a phone number, which is then stored in the phone number buffer. When entering at REDIAL, the routine dials the number previously stored in the phone number buffer and does not issue a user prompt.

Interrupts not required during dialing are disabled to prevent errors in real time delays. Interrupt status is saved to allow restoring these interrupts when dialing is complete. The current modem configuration is saved prior to selecting the DTMF Transmit configuration, then restored at the completion of the auto-dialer routine to allow data transfer.

The commands for off-hook and request coupler cut through are typical of signals required by data access arrangements that may be connected to the modem for switched network operation.

Since the number to be dialed varies in length depending on the requirements of various PBX equipment, domestic telephone companies, and foreign PTTs, the number buffer must allow for numbers of different length. The method used in Figure 2 to determine the end of valid bytes in the buffer is zero recognition. After the last digit is entered, the carriage return must place a hexadecimal 00 (ASCII NUL character) in the buffer. All other bytes must be non-NUL ASCII characters. Only numeric characters (ASCII 30 through 39) are printed and dialed. Non-numeric characters are tested for comma and NUL. Comma causes a 2-second pause in dialing to allow for known delays in the telephone network or PBX. NUL ends the dialing portion of the routine and begins the answer tone detection portion. All other characters are ignored.

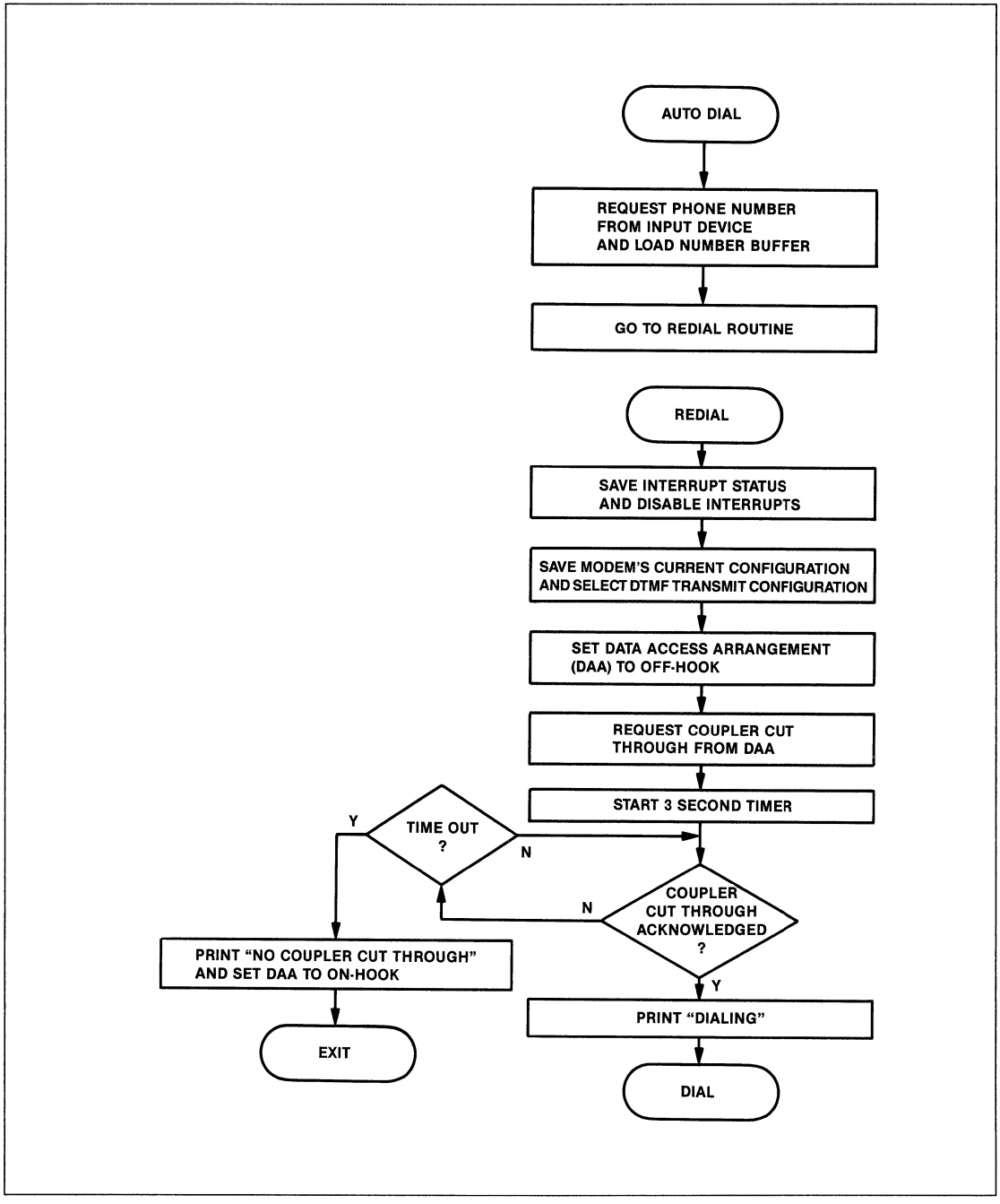

Figure 2. Autodialer Flow Chart

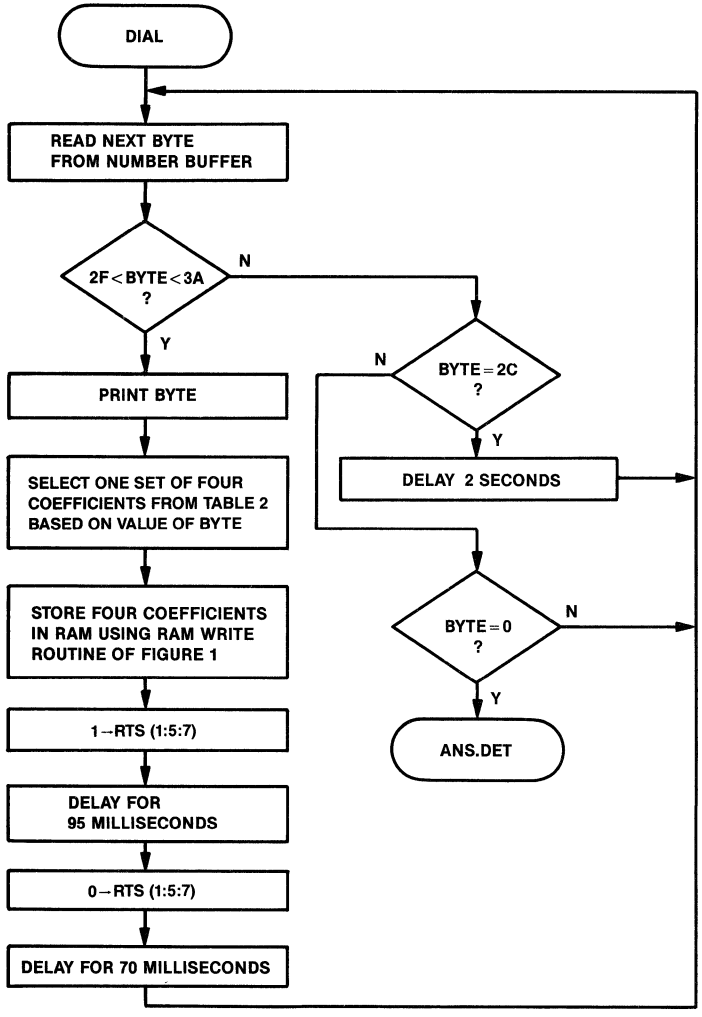

Figure 2. Autodialer Flow Chart (Cont'd)

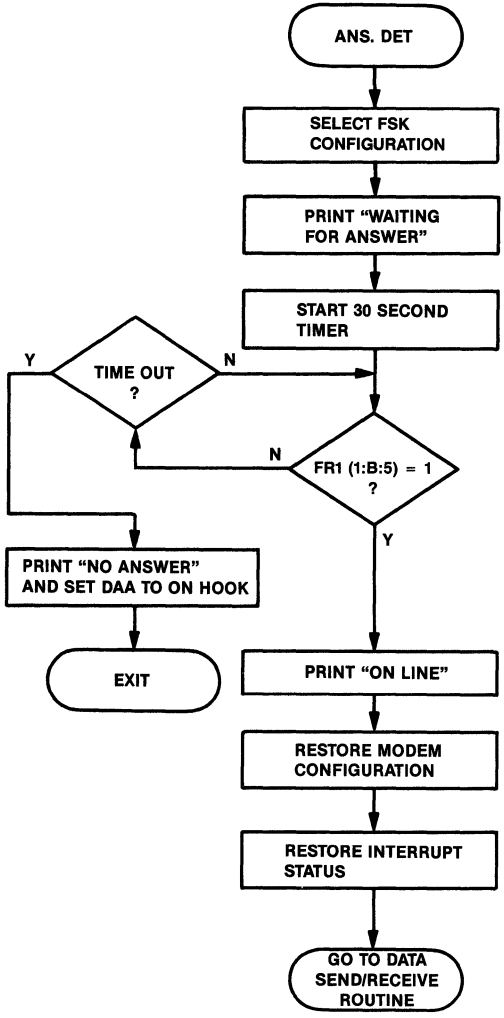

Figure 2. Autodialer Flow Chart (Cont'd)

The answer tone detection logic allows 30 seconds for 2100 Hz recognition. If answer tone is not recognized within this time limit, the call is aborted. If answer tone is recognized, the routine jumps to the data handling software.

SINGLE TONE GENERATION

In OEM equipment that combines the features of a modem with those of a telephone handset, the tone generators may be used to generate a caller reassurance tone (or even music) while the caller is kept on hold. To generate a single tone, set one of the oscillators to zero frequency or zero amplitude while the other oscillator is keyed on by the RTS bit. This technique is also applicable for generating a 2100 Hz answer tone when the modem is used to automatically answer a call. The parameters for 2100 Hz answer tone generation are listed in Table 3.

Table 3. 2100 Hz Answer Tone Parameters

Frequency	RAM Access S	RAE	Value
2100 Hz	71	1	3800
	71	0	0000
	72	1	5FFF
	72	0	5FFF

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DTMF Dialing Using the R24MFX, R24BKJ, R48MFX, or R48PCJ Modem

INTRODUCTION

The R24MFX, R24BKJ, R48MFX, and R48PCJ modems include tunable oscillators that can be used to perform dual-tone multi-frequency (DTMF) dialing. The frequency and amplitude of each oscillator output is under host control. A programmable tone detector can also be used in call establishment to recognize an answer tone.

This application note describes the method of oscillator and filter tuning by the host processor and provides an example of an auto-dialer routine that may be programmed into the host.

DTMF REQUIREMENTS

EIA Standard RS-496, paragraph 4.3.2, specifies requirements that ensure proper DTMF signaling through the public switched telephone network (PSTN). These tones consist of two sinusoidal signals, one from a high group of three frequencies and one from a low group of four frequencies, that represent each of the standard pushbutton telephone characters shown in Table 1.

Table 1. DTMF Signals

High Frequency / Low Frequency	1209 Hz	1336 Hz	1477 Hz
697 Hz	1	2	3
770 Hz	4	5	6
852 Hz	7	8	9
941 Hz	*	0	#

Signal power is defined for the combined tones as well as for the individual tones. Both maximum and minimum power requirements are functions of loop current. By combining the various requirements of RS-496, compromise power levels can be determined that meet the power specification for all U.S. lines (when driving the PSTN from a 600 ohm resistive source). The high frequency tone should be at a higher power level than the low frequency tone by approximately 2 dB. The maximum combined power, averaged over the pulse duration, should not exceed +1 dBm. The minimum steady state power of the high frequency tone should not be less than −8 dBm. When connecting the modem circuit to the PSTN by means of a data access arrangement (DAA) set for permissive mode, the DAA gain is −9 dB. The modem circuit must, therefore, drive the DAA input with +1 dBm of steady state high frequency power and −1 dBm of steady state low frequency power in order to meet all of the listed conditions.

The required duration of the DTMF pulse is 50 ms minimum. By experience, a pulse duration of approximately 95 ms is more reliable. The required interval between DTMF pulses is 45 ms minimum and 3 seconds maximum. Again by experience, an interdigit delay of approximately 70 ms is preferred.

The remaining requirements of RS-496, relative to DTMF dialing, are not influenced by the host processor. These requirements are all met by the modem's oscillators.

SETTING OSCILLATOR PARAMETERS

The oscillator frequency and output power are set by the host computer using the microprocessor bus and diagnostic data routine. For a description of the microprocessor bus and other interface considerations, refer to the R24/48MEB modem evaluation board data sheet and the relevant modem data sheet listed in Table 2.

Table 2. Data Sheet Order Numbers

Title	Order Number
R24/48MEB Data Sheet	MD22
R24MFX Data Sheet	MD17
R24BKJ Data Sheet	MD20
R48MFX Data Sheet	MD19
R48PCJ Data Sheet	MD21

When setting the frequency of tone 1, the host must write a 16-bit hexadecimal number into RAM using RAMA code 8E. When setting the frequency of tone 2, a 16-bit hexadecimal number must be written into RAM using RAMA code 8F. The power levels of tone 1 and tone 2 are set by writing 16-bit hexadecimal numbers into RAM using RAMA codes 44 and 45, respectively. The hexadecimal numbers written into these RAM locations are scaled as follows:

R24MFX AND R24BKJ

Frequency number = 9.1022 (desired frequency in Hz).

R48MFX AND R48PCJ

Frequency number = 6.8267 (desired frequency in Hz).

R24MFX, R24BKJ, R48MFX, AND R48PCJ

Power number = $27573.6\ [10^{(P_O/20)}]$

Where P_o = output power in dBm with a series 600 ohm resistor into a 600 ohm load.

These decimal numbers must be converted to hexadecimal form then stored in RAM by following the RAM data write routine illustrated by Figure 1.

Hexadecimal numbers for DTMF generation on the R24MFX and R48MFX are listed in Table 3. These numbers are also suitable for use with the R24BKJ and R48PCJ. Numbers used for setting the frequency of tone 1 and tone 2 are larger in the 2400 bps products than in the 2400/4800 bps products. This variation is due to the sample rate difference between these modems. Power levels are selected to give the desired output power for each tone while compensating for modem filter characteristics.

Table 3. DTMF Parameters

Digit	RAMA	R24XXX	R48XXX
0	8E	2174	1918
	8F	2F80	23A0
	44	6184	6184
	45	7A80	7A80
1	8E	18C8	1296
	8F	2AFC	203D
	44	61E8	61E8
	45	7AFC	7AFC
2	8E	18C8	1296
	8F	2F80	23A0
	44	61E8	61E8
	45	7A80	7A80
3	8E	18C8	1296
	8F	3483	2763
	44	61E8	61E8
	45	79E3	79E3
4	8E	1B60	1488
	8F	2AFC	203D
	44	6250	6250
	45	7AFC	7AFC
5	8E	1B60	1488
	8F	2F80	23A0
	44	6250	6250
	45	7A80	7A80
6	8E	1B60	1488
	8F	3483	2763
	44	6250	6250
	45	79E3	79E3
7	8E	1E4A	16B8
	8F	2AFC	203D
	44	621A	621A
	45	7AFC	7AFC
8	8E	1E4A	16B8
	8F	2F80	23A0
	44	621A	621A
	45	7A80	7A80
9	8E	1E4A	16B8
	8F	3483	2763
	44	621A	621A
	45	79E3	79E3

DETECTING ANSWER TONE

The modem tone detect bit, TDET (A:7), can be used to detect the presence of answer tone when connection to the remote modem is successful. Bit TDET goes active (one) when energy is detected by the associated tone detect filter. This filter is illustrated in Figure 2.

A set of eight coefficients determines the filter response. Table 2 lists the RAM access codes and filter coefficient values to be written using the RAM Data Write routine of Figure 1. These values tune the filter to detect 2100 Hz ± 25 Hz.

Once TDET turns on, the calling modem knows the call has been answered. At the end of the answer tone, TDET returns to zero and data transmission can begin.

COMPLETE CALLING SEQUENCE

A complete calling sequence consists of several steps including modem configuration, telephone number selection, DTMF transmission, and answer tone detection. A sample flow chart for implementing an auto-dialer in host software is illustrated in Figure 3.

The auto-dialer routine may be entered at one of two points; either AUTO DIAL or REDIAL. When entering at AUTO DIAL, the host prompts the user to enter a phone number, which is then stored in the phone number buffer. When entering at REDIAL, the routine dials the number previously stored in the phone number buffer and does not issue a user prompt.

Interrupts not required during dialing are disabled to prevent errors in real time delays. Interrupt status is saved to allow restoring these interrupts when dialing is complete. The current modem configuration is saved prior to selecting the tone configuration, then restored at the completion of the auto-dialer routine to allow data transfer.

The commands for off-hook and request coupler cut through are typical of signals required by data access arrangements that may be connected to the modem for switched network operation.

Since the number to be dialed varies in length depending on the requirements of various PBX equipment, domestic telephone companies, and foreign PTTs, the number buffer must allow for numbers of different length. The method used in Figure 3 to determine the end of valid bytes in the buffer is zero recognition. After the last digit is entered, the carriage return must place a hexadecimal 00 (nul character) in the buffer. All other bytes must be non-zero ASCII characters. Only numeric characters (ASCII 30 through 39) are printed and dialed. Non-numeric characters are tested for comma and nul. Comma causes a 2-second pause in dialing to allow for known delays in the telephone network or PBX. Nul ends the dialing portion of the routine and begins the answer tone detection portion. All other characters are ignored.

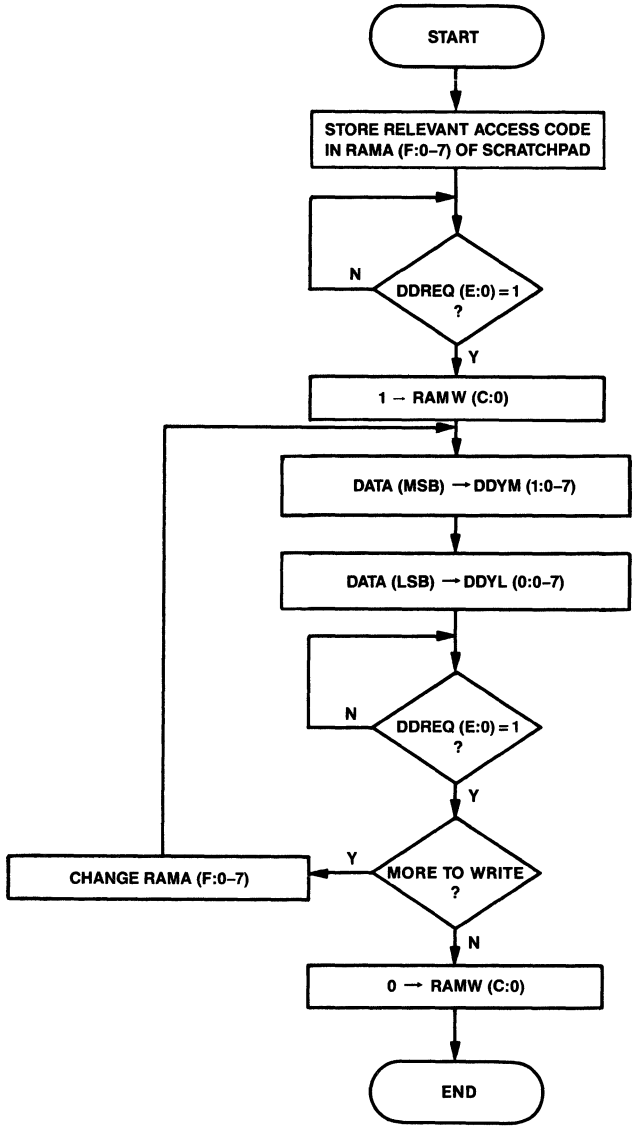

Figure 1. RAM Data Write Routine

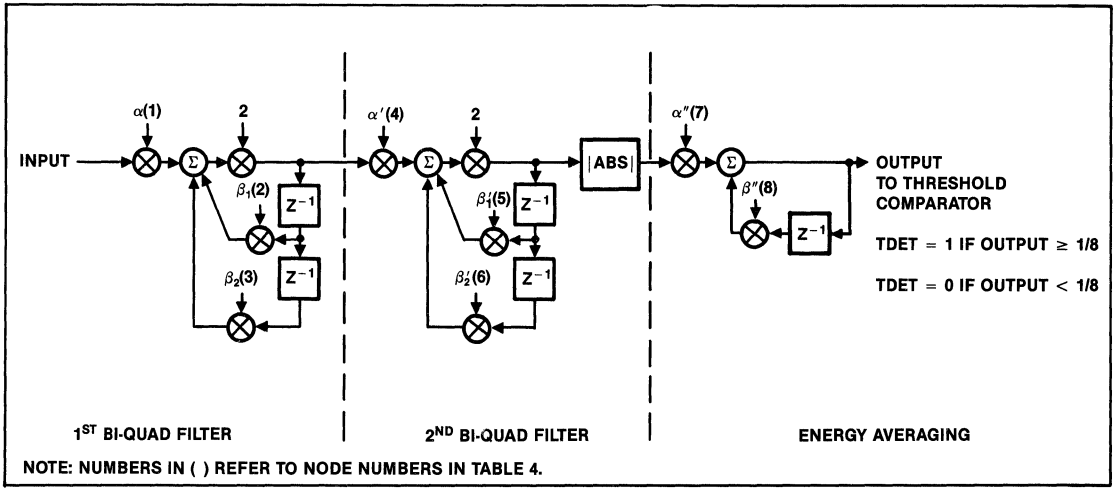

Figure 2. Tone Detector Diagram

Table 4. Tone Detector Coefficients for 2100 Hz

Node	Coefficient Name	R24XX RAMA	R24XX Coefficient Value	R48XX RAMA	R48XX Coefficient Value
1	α	36	0198	38	0198
2	β_1	37	E0F4	39	1A4A
3	β_2	38	C0C5	3A	C0C5
4	α'	39	0198	3B	0198
5	β'_1	3A	DD33	3C	175A
6	β'_2	3B	C0C5	3D	C0C5
7	α''	B6	002D	B8	0022
8	β''	B7	7FD1	B9	7FDC

The answer tone detection logic allows 30 seconds for 2100 Hz recognition. If answer tone is not recognized within this time limit, the call is aborted. If answer tone is recognized, the routine jumps to the data handling software.

ADDED FEATURES

The application of modem tone generation and detection to DTMF dialing and answer tone recognition can be extended to include additional features. For example, the tone detector can monitor call progress for dial tone, busy signal or ringback tone. The detector filter must be returned to detect different frequencies used in call progress signaling. Table 5 lists tones for various lines in the Bell network. These call progress signals vary according to the telephone networks of each country. For details on tuning the tone detector for other frequencies, refer to Application Note Order No. 668. That note refers to the R96F filters but is also applicable to R24XXX and R48XXX modems for coefficient calculation. When applying Application Note 668 to R24XXX modems, the sample rate used should be 7200 samples per second rather than 9600 samples per second.

In OEM equipment that combines the features of a modem with those of a telephone handset, the tone generators may be used to generate a caller reassurance tone (or even music) while the caller is kept on hold. To generate a single tone, set one of the oscillators to zero frequency or zero amplitude while the other oscillator is keyed on by the RTSP bit. This technique is also applicable for generating a 2100 Hz answer tone when the modem is used to automatically answer a call. The parameters for 2100 Hz answer tone generation are listed in Table 6.

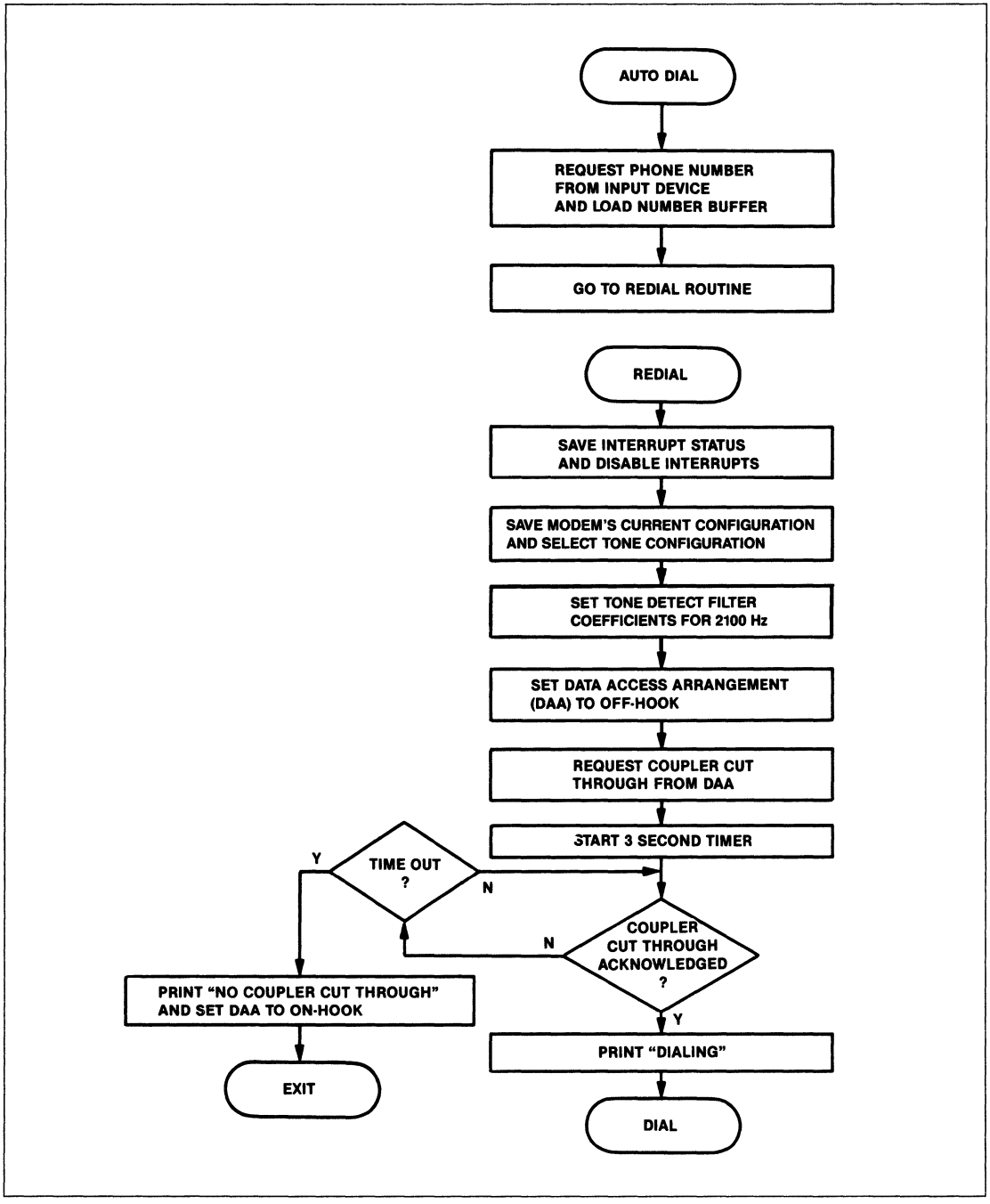

Figure 3. Autodialer Flow Chart

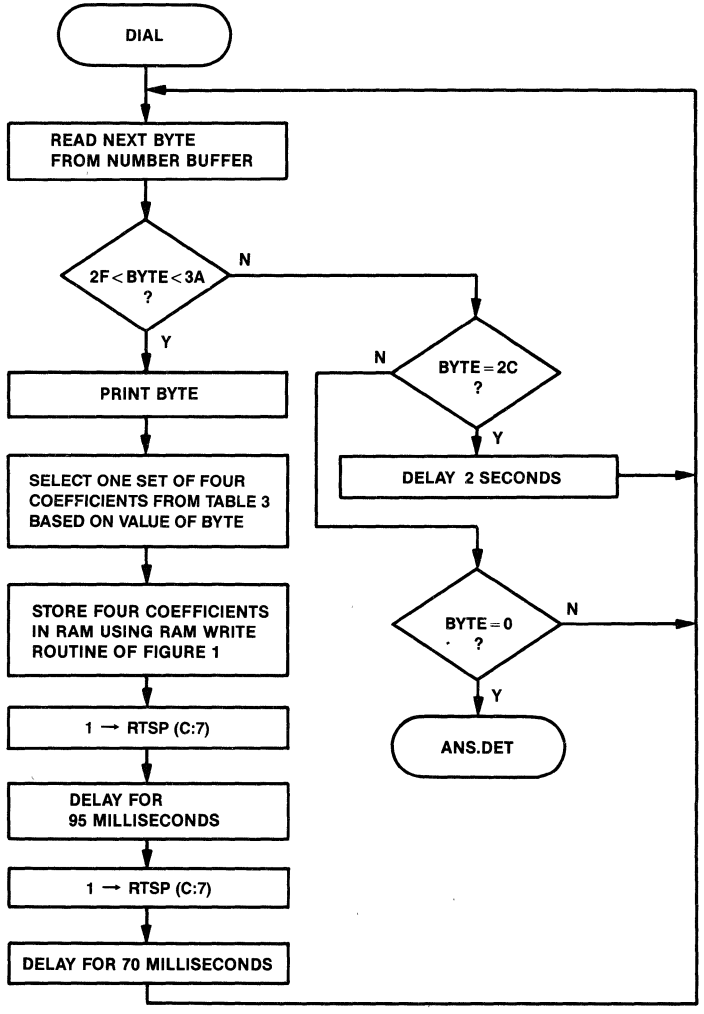

Figure 3. Autodialer Flow Chart (Cont'd)

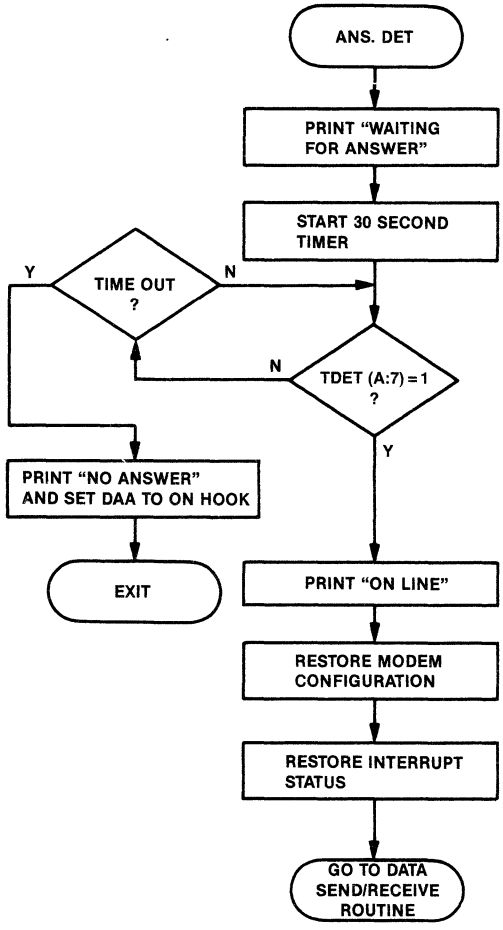

Figure 3. Autodialer Flow Chart (Cont'd)

Table 5. Call Progress Signals

Tone	Frequency (Hz)*	Interruption Rates	Use
Precision Dial Tone	350 +440	Continuous	Dialing may commence
Old Dial Tones	600 +120 or 133, and other combinations	Continuous	Dialing may commence
Precision Busy	480 +620	0 5 Sec. On 0.5 Sec. Off	Called line busy
Old Busy	600 +120	0.5 Sec. On 0.5 Sec. Off	Called line busy
Precision Reorder Old Reorder	480 +620 600 +120	0 3 Sec. On } Local 0.2 Sec Off } Reorder 0.2 Sec. On } Toll 0.3 Sec. Off } Reorder 0.25 Sec. On } Toll 0.25 Sec. Off } Local	All local switching paths busy, all trunks busy, all paths or trunks busy
Precision Audible Ringing	440 +480	2 Sec. On 4 Sec. Off	To calling customer
Old Audible Ringing	420 +40, and other combinations	2 Sec. On 4 Sec. Off	To calling customer
Call Waiting	440	0.3 Sec On	Call waiting service; an incoming call is waiting
Precision Receiver Off-Hook (ROH)	1400 +2060 +2450 +2600	On and Off 5 Times per Sec	To cause off-hook customers to go on-hook
Precision High Tone Old High Tone	480 480, 400 or 540	Continuous	To cause off-hook customers to go on-hook
Recorder Connector Tone	1400	On 0 5 Sec. Every 15 Seconds	To indicate call is being recorded by distant customer

*A "+" sign indicates either superposition (precision tones) or modulation (old tones).

Table 6. 2100 Hz Answer Tone Parameters

Frequency	RAMA	R24XXX	R48XXX
2100 Hz	8E	4AAA	3800
	8F	0000	0000
	44	5FFF	5FFF
	45	5FFF	5FFF

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R96MFX Modem Recommended Receive Sequence for Group 2 Facsimile

INTRODUCTION

The R96MFX includes a transmit and receive configuration that is compatible with the transmission scheme of Group 2 facsimile equipment. In order to achieve the best results with Group 2 reception, the following procedure is recommended. The step numbers are keyed to points in Figure 1. Refer to Data Sheet MD47 for details on how to configure the modem and write modem data.

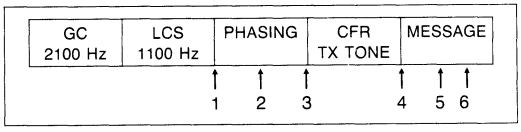

Figure 1. Group 2 Facsimile Sequence

METHOD

1. Enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Write hex 0038 using access code 0D, CRx = 0. This action sets the Group 2 phase-locked-loop for a frequency correction of 9 Hz, causing the phase term to drift rapidly to overcome any tendency to slow phase recovery.
   b. Write hex 4000 using access code 19, CRx = 0, and hex 7FFF using access code 99, CRx = 0. This action allows the Group 2 phase locked-loop to accept the greatest number of samples for carrier recovery during phasing.
   c. Write hex 2000 using access code 05, CRx = 1. This action sets the AGC slew rate for very fast acquisition.
   d. Select fast AGC state by setting control bit G2FGC (0D:3) to a one.
2. After phasing is detected, wait approximately 2 seconds for the AGC circuit to settle. Then:
   a. Write hex 0000 using access code 05, CRx = 1. This action stops AGC tracking in order to preserve the present AGC setting.
   b. Reset control bit G2FGC (0D:3) to a zero to select slow AGC rate. This action changes the Group 2 phase-locked-loop characteristics to match reduced AGC response.
   c. Read and save the 16-bit value from registers 3 and 2 using access code 0D, CRx = 0. This value represents the frequency error term from the Group 2 phase-locked-loop.
   d. Verify that phasing signal is still being received. This action guarantees that AGC value was frozen during phasing signal.
   e. If step d above determines that phasing signal is present, allow transmission of CFR. If phasing signal is not present, suppress CFR.
3. Exit Group 2 configuration.
4. At completion of CFR transmission, re-enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Repeat step 1.b.
   b. Repeat step 2.a.
   c. Add hex 0038 to the value saved in step 2.c above and write the sum using access code 0D, CRx = 0. This action forces a 9 Hz error as in step 1.a.
5. Wait for start of Group 2 message transmission. Then:
   a. Write hex 0400 using access code 05, CRx = 1. This action restores the AGC slew rate to the default value.
   b. After 2 lines, write the value saved in step 2.c using access code 0D CRx = 0. This action removes the 9 Hz forced frequency error without waiting for the phase-locked-loop to complete the correction. This step is optional as the correction will eventually be completed, but, depending on the percentage of white in the document being sent, the correction may take from 4 to 6 lines (100 ms of white required).
6. After approximately 6 to 10 seconds of message reception, perform either step a or step b below:
   a. Write hex 6100 using access code 19, CRx = 0 and hex 0600 using access code 99, CRx = 0. This action places narrow limits on the received signal used for carrier recovery during message reception and

5

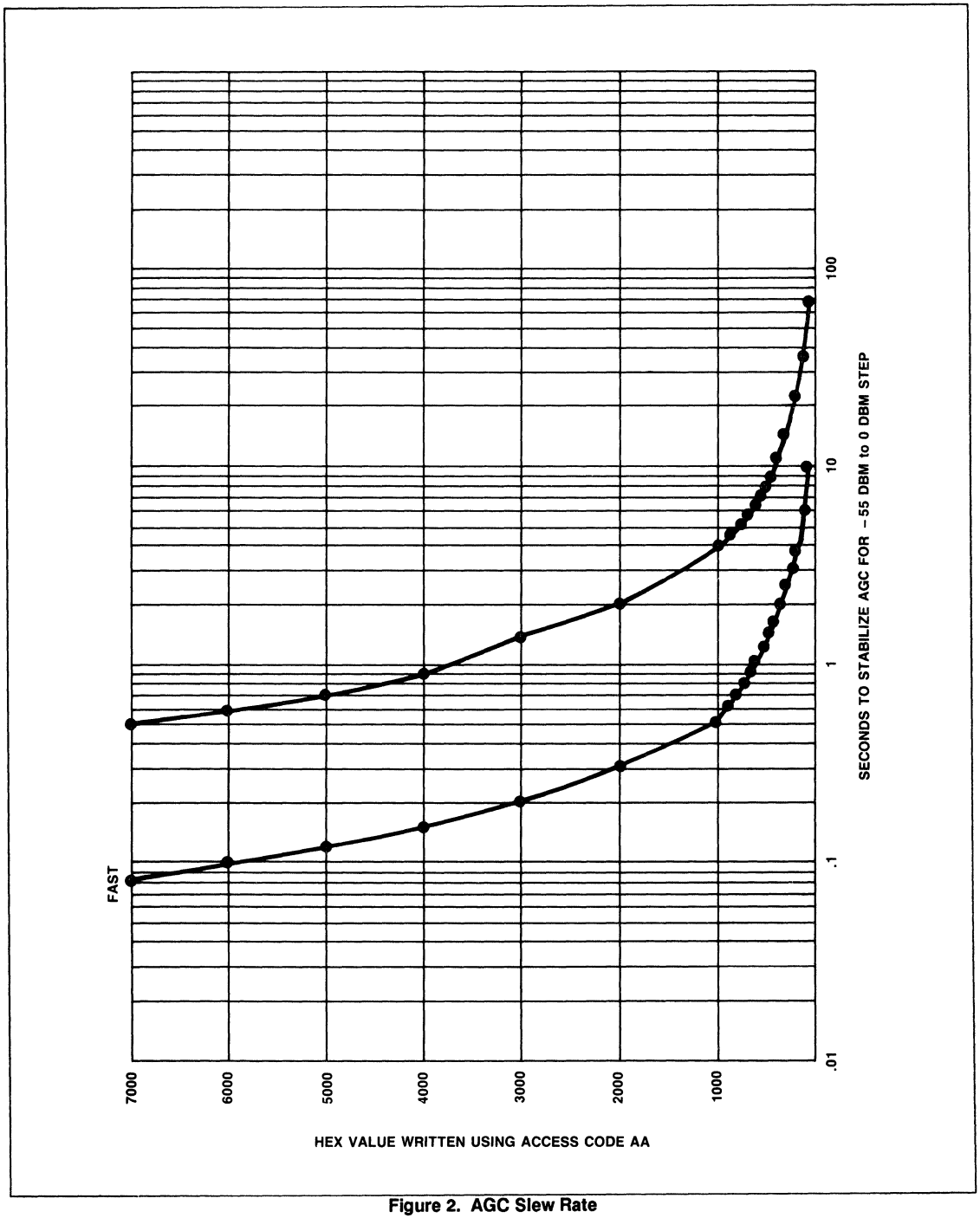

Figure 2. AGC Slew Rate

reduces the chance of errors caused by repeated patterns in the message.

b. Synchronize the modem's Group 2 phase-locked-loop to the facsimile machine's blanking signal as follows:

(1) Freeze the phase-locked-loop during data by:

(a) Writing hex 7FFF using access code 19, CRx = 0

(b) Writing hex 0000 using access code 99, CRx = 0

(2) Enable the phase-locked-loop during the white margins by:

(a) Writing hex 4000 using access code 19, CRx = 0

(b) Writing hex 7FFF using access code 99, CRx = 0

c. The sequence of writing in step 6.b is important and must be performed as described. Option 6.b requires more action by the host processor, but it eliminates the possibility of data patterns affecting carrier recovery.

PARAMETER SCALING

1. Access code 0D, CRX = 0 represents frequency error i.e., the deviation of received carrier from 2100 Hz.

   LSB = 0.167 Hz.; Range = ± 140 Hz.

2. Access code 18, CRx = 0 represents the Group 2 phase-locked-loop slew rate for the first order term. The number is directly proportional to slew rate. The range of stable operating values is 0010 to 7000 in hexidecimal.

3. Access code 05, CRx = 1 represents the AGC slew rate.

   Range = 0000 to 7FFF in hexidecimal.
   Scaling: See Figure 2.

4. Access codes 19 and 99, CRx = 0 represent limits on acceptable zero crossing for use by the carrier recovery loop. The carrier recovery loop uses several nonlinear controls in attempting to lock the zero crossing of the local carrier to those of the transmitter. Since Group 2 facsimile uses VSB transmission, it is necessary to either reconstruct the upper sideband or exclude those zero crossings that represent frequencies other than 2100 Hz. The R96MFX excludes unwanted zero crossings by testing the effective slope of the waveform as it crosses zero. In Figure 3, points A and B represent samples taken about a zero crossing over a sample period T, where T = 1/10,368 seconds.

The magnitude of [|A| + |B|] is directly proportional to the slope of line segment AB and is therefore an indicator

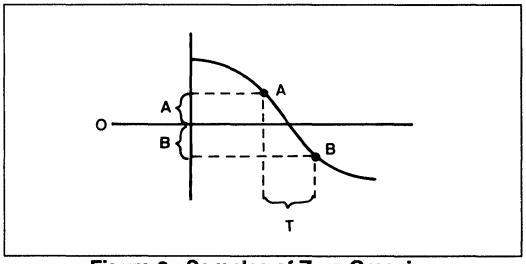

Figure 3. Samples of Zero Crossing

of frequency. If H represents the value stored at 19, CRx = 0 and L represents the value at 99, CRx = 0, then 1 – [|A| + |B|] + H + L must be greater than positive full scale or the frequency is excluded for being too high.

The average value for 1 – [|A| + |B|] with an all white transmission and back-to-back connection is hex 19A1 ± 0543.

5. Access code 1A, CRx = 0 allows host control of the limits placed on phase error correction. When the phase error exceeds the limit set by 1A, CRx = 0, PLL updating is suspended. The default value of 5000 corresponds to a limit of ± 27.34 degrees. A zero in 1A, CRx = 0 causes the PLL to update for any phase error. By setting 1A, CRx = 0 to zero, it may be unnecessary to force a frequency offset in the receive sequence. For systems using step 6.a in the receive sequence, reception of messages containing a large amount of black may be improved by setting 1A, CRx = 0 to zero. 1A, CRx = 0 scaling is:

   Phase limit = 360° x (2100/10368) x A
   where A = [7FFF – (1A, CRx = 0 value)]/7FFF

Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits, etc.

BLACK/WHITE THRESHOLD

The R96MFX receives a Group 2 baseband signal that contains density (gray scale) information in the amplitude modulation. In order for this information to be used on a Group 3 facsimile machine the R96MFX converts the gray scale to black/white baseband form. The threshold at which the black/white decision is made determines the density of the received page.

Access code 24, CRx = 0 represents the Group 2 black/white threshold. This location defaults to hex 7200 at POR time. The number may be increased or decreased by the host to achieve a page weighted more toward white or toward black, respectively.

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R96EFX HDLC and Programmable Interrupt Features

INTRODUCTION

The HDLC (High Level Data Link Control) protocol is a standard procedure used for data communications. SDLC (Synchronous Data Link Control) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The R96EFX 9600 bps MONOFAX® Modem with Error Detection uses the SDLC eight-bit octet format.

A programmable interface memory interrupt is featured in the R96EFX. This feature allows the user to select an interrupt to occur on any combination of bits within the interface memory registers.

HDLC FRAMES

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving station to synchronize with each other. This format is shown in Figure 1.

FLAGS

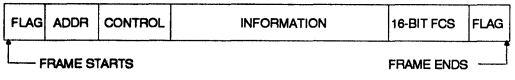

Figure 1. HDLC Frame

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7E). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as "zero-sharing". The zero-sharing bit pattern is 011111101111110.

ADDRESS FIELD

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the "basic" format.

For the "extended" format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

1. The Broadcast Address 11111111
2. The Null Address 00000000

CONTROL FIELD

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format
2. Supervisory Format
3. Unnumbered Format

This field is normally 8 bits in length. However, certain protocols allow for an "extended" control field. For example, it is 16 bits in length for modulo 128 operation of the LAP and LAPB procedures.

INFORMATION FIELD

The R96EFX treats the address field, the control field, and any other transmitted data, except for the flags and the Frame Check Sequence, as the information field. The information field does not have a set length; however, this field follows the SDLC protocol in being in the format of eight bit bytes.

ZERO INSERTION

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

ZERO DELETION

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (i.e., at least seven ones with no zero insertion) or a flag (i.e., 01111110). The sixth one is, therefore, not removed.

FRAME CHECK SEQUENCE

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

The FCS computation is done on all fields within the frame but does not include the flags. Cyclic Redundancy Check (CRC) is the method used. The polynomial is specified in CCITT T.30 and X.25 as follows:

$$x^{16} + x^{12} + x^5 + 1$$

The polynomial is implemented as shown in Figure 2.

The Frame Check Sequence is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS register is transmitted as the 16-bit FCS. The FCS is transmitted with the highest order bit (x^{15}) first.

FRAME ABORTION, FRAME IDLE, AND TIME FILL

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

Interframe time fill is accomplished by transmitting continuous flags without zero-sharing between flags. Therefore, the transmitter must be capable of sending multiple flags to maintain the active state in the receiver if any time fill is required.

IMPLEMENTATION

A representation of the HDLC process is shown in Figure 3. The events are numbered in order of occurrence from one to four.

1. The beginning flag is transmitted. The receiver sees the flag and now becomes aligned with the transmitter. Both the receive and the transmitter FCS registers are preset to FFFF (hex).
2. The information field is transmitted. The data is also run through the FCS register before zero insertion. At the receive end, after the zero deletion algorithm, the data is presented to the user and then run through the FCS register.
3. The FCS is inverted and then transmitted. The transmitted FCS is passed through the receiver's FCS register. The shift register will contain 1111000010111000 if the frame has been received correctly.
4. The ending flag is transmitted.

The signal timing is illustrated in Figure 4.

TRANSMITTER AND RECEIVER IMPLEMENTATION

In order to use HDLC in the R96EFX, the host processor must:

1. Set up the modem configuration.
2. Set the parallel data mode bit (PDM).
3. Set the HDLC mode bit.

RAM Access 1 (using ADD1) remains available while RAM Access 2 (using ADD2) is unusable in the parallel data mode. HDLC transmission cannot be performed using the serial interface.

The format of the data input to the R96EFX is in groups of eight bit bytes. As in the parallel data mode, the least significant bit of the byte is transmitted first.

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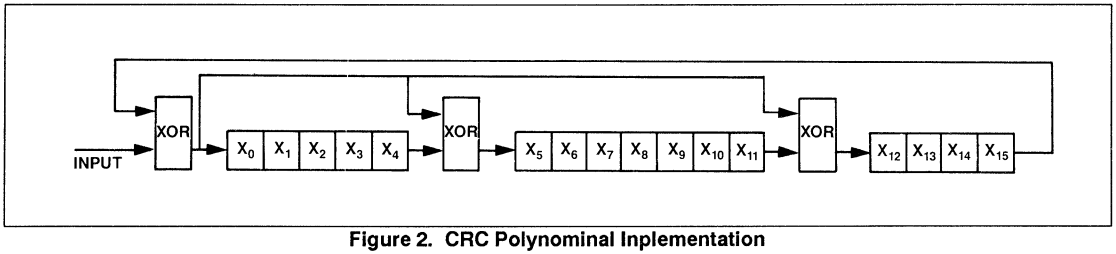


Figure 2. CRC Polynominal Inplementation

TRANSMISSION AND RECEPTION RATE

The HDLC as implemented in the R96EFX runs under the following transmitter and receiver modes:

V.29, 9600 bps
V.29, 7200 bps
V.29, 4800 bps
V.27, 4800 bps
V.27, 2400 bps
V.21, 300 bps

In addition to the above configurations, the programmable interrupt runs under the following transmitter and receiver configurations:

Group 2
Tone Detect
Dual Tone Transmitter

Note: In the high speed modes, any data patterns referred to in this application note are transmitted scrambled and received descrambled.

TRANSMITTER AND RECEIVER INITIALIZATION

The HDLC transmitter and receiver is initialized differently than other modes upon power-up, reconfiguration, or turning on $\overline{\text{RTS}}$ input or RTSP bit. Table 1 shows the states of the interface memory bits for HDLC initialization.

Table 1. Transmitter and Receiver Initialization

Transmitter		Receiver	
ABIDL =	0 (Note 2)	ABIDL =	0 (Note 2)
BA2 =	1	BA2 Not Initialized	
CRC =	0 (Note 1, 2)	CRC =	0 (Note 2)
EOF =	0 (Note 2)	EOF =	0 (Note 2)
FLAG =	0	FLAG =	0
ZEROC =	0 (Note 2)	ZEROC =	0 (Note 2, 3)

Notes:
1. Not applicable in the transmitter.
2. Zeroed only upon power-up; unchanged elsewhere.
3. Not applicable in the receiver.

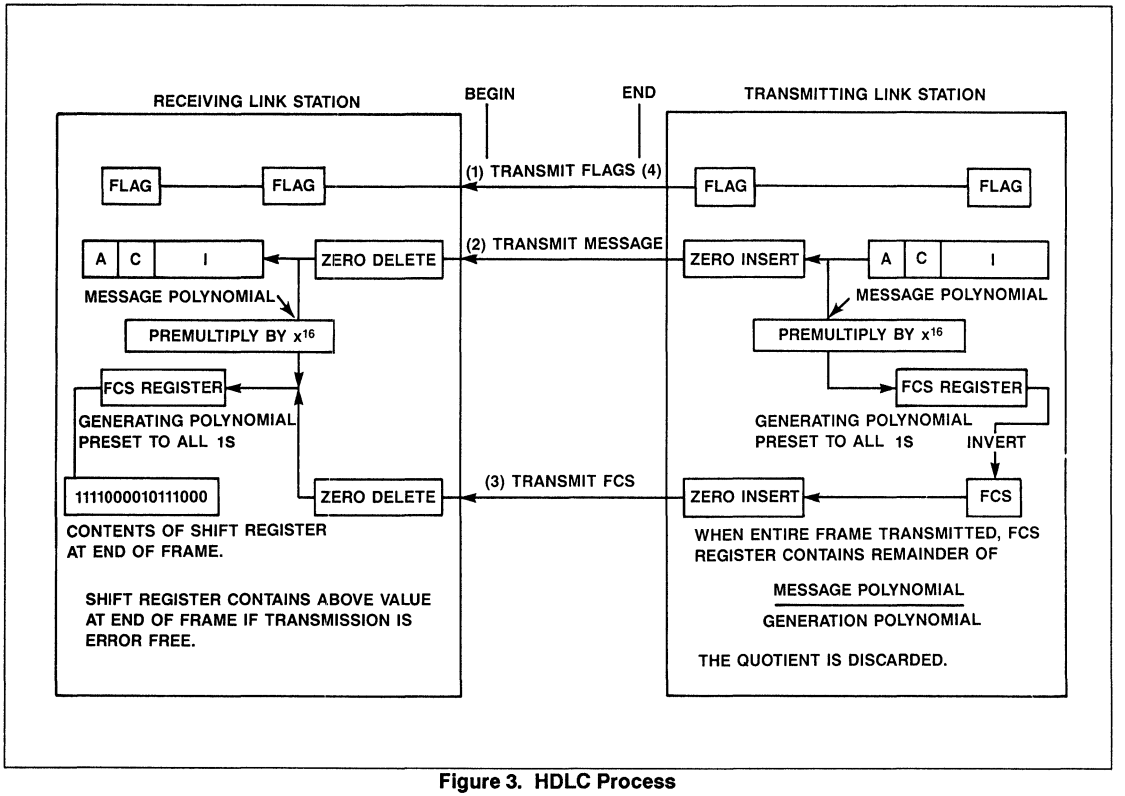
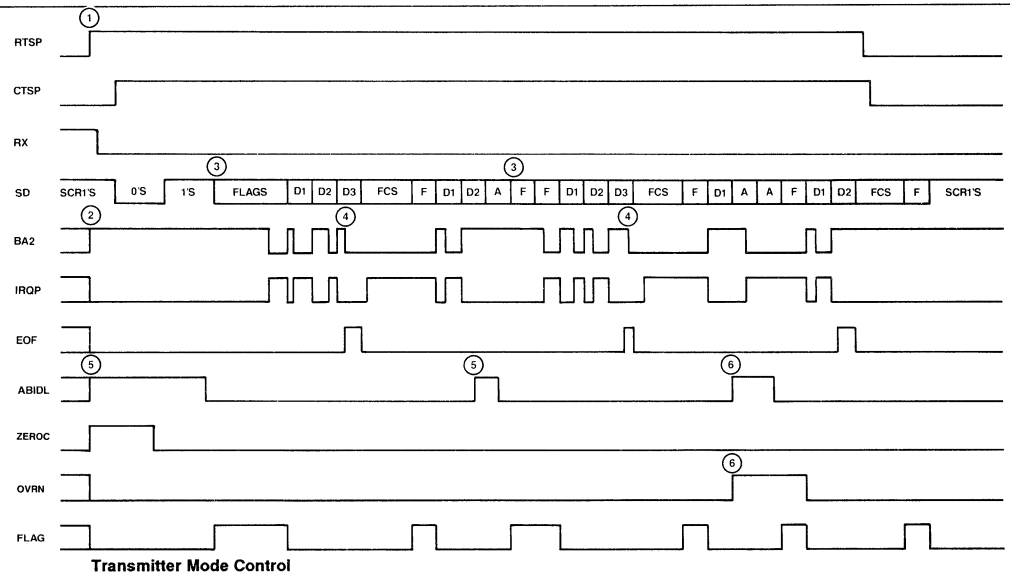


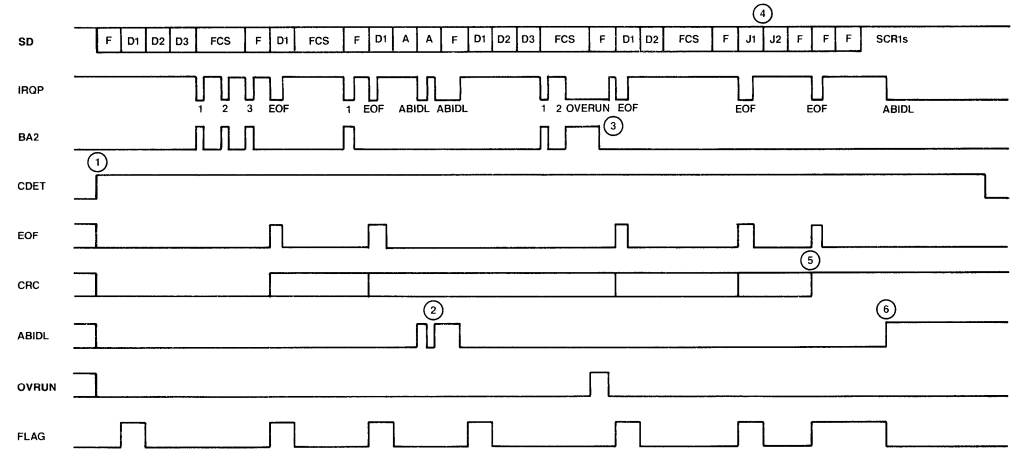
Figure 3. HDLC Process



Transmitter Mode Control

1. Upon setting RTSP, the host should initialize EOF, ABIDL, ZEROC, and OVRUN to the desired values.
2. BA2 is forced high 0.7 µs before RX(0D:7) goes low.
3. The host can send multiple flags by either waiting to load data into DBUFF or by doing a diagnostics write to RAM (see "Flag Transmission and Reception" Section). The host can then load the first byte when RX goes low for the first frame or after setting EOF for subsequent frames.
4. Load the first byte of the next frame after setting EOF.
5. The host sets and resets ABIDL here.
6. A transmit underrun occurs here. The modem sets ABIDL. The host must reset ABIDL.

a. Transmitter



Receiver Notes

1. EOF, ABIDL, and OVRUN should be a known value before the data appears on RD.
2. The host resets ABIDL in the middle of receiving an abort/idle sequence.
3. A receive overrun condition has occurred.
4. J1, J2 are junk (invalid) data.
5. CRC sets and EOF sets in response to the junk data between flags.
6. ABIDL remains high due to the incoming scrambled 1's turnoff sequence for high speed modes.

b. Receiver

Figure 4. HDLC Signal Timing Diagrams

FLAG TRANSMISSION AND RECEPTION

The R96EFX transmitter sends at least one flag as the opening flag of the first frame. As long as the user does not load the 8-bit transmit data register, DBUFF (register 10), with data, the modem sends continuous flags with no zero-sharing (i.e., 0111111001111...). This facilitates transmission of the preamble as specified in T.30. Thus, the transmitter defaults to transmitting time-fill and, therefore, keeps the receiving link station active.

To assist the user in transmitting more than one flag between frames or at the end of the final frame, a counter can be accessed through modem diagnostics. This counter is decremented directly in the signal processor's RAM. This means that the number written will only last for one group of flags. For example, FSK should have at least two beginning flags for the first frame and at least two ending flags for the final frame. However, frames between these two require only one flag. This is why the counter is decremented directly and one flag is transmitted as a default. Diagnostics should be setup as shown below:

ADD1= 85
BR1= 0
CR1= 1
WRT1 = 1

The value to write into YDAM1 and YDAL1 should be 1 less than the number of flags desired. This value can be written anytime after the RX bit returns to zero and before FLAG is set by the modem.

Using the FSK example above, assume three flags are to be transmitted at the beginning of the first frame and at the end of the final frame.

1. Turn on RTS.
2. Wait until the RX bit is reset by the modem.
3. Disable diagnostics 1 (reset ACC1).
4. Setup diagnostics 1 as above, write 00 into YDAM1, and write 02 into YDAL1.
5. Enable diagnostics 1 (set ACC1).
6. Wait until BA1 is set before resetting WRT1.
7. For the ending flag of the final frame, immediately after loading in the final byte of data or after setting EOF, again setup diagnostics 1 as above, write 00 into YDAM1, and write 02 into YDAL1.

Another method exists for sending extra flags. The host must simply do nothing since flags are transmitted as the default condition. In other words, after the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into DBUFF (BA2 is reset). If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag is desired, the host must wait N-1 multiples of eight bit times after FLAG is set by the modem to load new data into DBUFF, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAG is set by the modem.

As the default condition, the R96EFX receiver continually searches for the flag data pattern. When one or more flags are detected, the interface memory status bit FLAG (09:0) is set. The flags themselves are not presented to the host through the DBUFF register. Therefore, as soon as a flag is observed, the modem examines the next byte of received data. If it is a flag, an abort/idle sequence, or a FCS, it is not given to the user. Instead, the appropriate status bits are set or reset.

The R96EFX also has the capability to detect consecutive flags with zero-sharing.

INFORMATION FIELD TRANSMISSION AND RECEPTION

For information field transmission, the host should wait for CTSP (0F:1) to transition high. The host must then load the data into DBUFF and then wait for the data available bit BA2 (1E:3) to be set by the modem before loading in the next byte of data. If the next byte is not loaded into DBUFF within the next eight bit times, the modem will set OVRUN (09:7), indicating an underrun condition has occurred. To tell the modem that the host wants to end the frame, the host must set EOF as soon as the modem has taken the last byte of the frame (BA2 sets). When the modem recognizes EOF being high, the modem will reset EOF and will transmit the FCS and closing flag. Once the host sets EOF, the host may load in the first byte of data of the next frame into DBUFF. If the host wants to end transmission, the host must wait for EOF to return low before turning off RTS or RTSP.

In the receiver, only the information field data between flags is passed to the user through the DBUFF register by the use of the handshaking bit BA2. The user must wait for BA2 to be set by the modem and then take the data. If the host does not read the data within eight bit times, OVRUN will set indicating an overrun condition, and the data in DBUFF will be overwritten by the next byte.

Furthermore, no flags, abort/idle sequence, or FCSs are given to the user via the DBUFF register. Since these fields are not presented to the user, there is at least a 16-bit time delay in the reception of data when receiving these fields. This allows the FCS and ending flag, continuous flags, or the abort/idle sequence to be flushed out of the internal buffers.

FCS AND ENDING FLAG TRANSMISSION AND RECEPTION

The host ends a frame by loading in his last byte of data into DBUFF, waiting until the modem has taken it (BA2 sets), and then setting EOF. After setting EOF, the host may load in the first byte of data of the next frame into DBUFF. When the modem recognizes that the host wants to end the frame, the modem will reset EOF. To terminate data transmission, the host may turnoff RTS or RTSP when the modem resets EOF. After resetting EOF, the modem will automatically transmit the 16-bit FCS and at least one flag that signifies the end of the current frame and, if another frame follows, the beginning of the next frame.

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the modem examines the data in the FCS register and compares it to the remainder. If the FCS register remainder is correct, CRC (09:1) is reset. Conversely, if the remainder is incorrect, the CRC bit is set. This is the only time CRC is updated (except upon power-up). Following this determination, the modem sets EOF. Thus, once the modem sets EOF, the host can examine CRC to determine whether or not an erred frame was received. It is left to the host to reset the EOF bit. If the user does not reset EOF before the end of the next frame, the host will not get any indication that the following frame has ended.

ABORT/IDLE SEQUENCE TRANSMISSION AND RECEPTION

An abort/idle sequence can be sent by the host setting the bit ABIDL (09:3) in the interface memory. This stops any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. After the setting of ABIDL is detected, the modem first completes the transmission of the current byte of data. Immediately after this transmission, the modem sends eight consecutive ones. After these eight bit times, if ABIDL is still set, eight ones are sent again. To discontinue this sequence, ABIDL must be reset. Then, if no new data is loaded into DBUFF, continuous flags are sent. If new data is loaded into DBUFF (BA2 is reset), the modem sends a beginning flag and then the data in DBUFF. The modem will also recognize the setting of ABIDL while transmitting the FCS, thereby allowing the receiver to recognize that the transmitted frame should be discarded.

The R96EFX also has the ability to send continuous zeros. To accomplish this, ABIDL and ZEROC (09:4) must be set. The modem completes the transmission of the current byte and then sends eight consecutive zeros. After this time, if ABIDL remains set, eight zeros are sent again. To discontinue this sequence, ABIDL must be reset or, if continuous ones are desired, ZEROC only must be reset. However, if no new data is loaded in DBUFF and ABIDL is reset, continuous flags are sent regardless of the state of ZEROC. Then, if new data is loaded into DBUFF (BA2 is reset), the modem sends a beginning flag and then the data in DBUFF.

The R96EFX in HDLC mode not only continually searches for flags, but also continually searches for an abort/idle sequence. When the receive modem encounters this data pattern, it sets the abort/idle receive bit ABIDL. It is left up to the host to reset this bit. However, receiver processing will continue unaffected by the state of this bit.

The reception of data immediately following the abort/idle sequence is treated as invalid and is not presented to the user. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. At least one flag and three bytes of data must be received following the abort sequence before any data is given to the host.

UNDERRUN AND OVERRUN CONDITIONS

A bit in the interface memory OVRUN (09:7) is used to indicate to the host processor that a transmit underrun condition has occurred. If the host does not load in a new byte of data within eight bit times, OVRUN and ABIDL will be set by the modem and the modem will automatically send a minimum of eight continuous ones. This abort sequence will continue until the host resets ABIDL. After the host resets ABIDL, the modem will finish sending the current byte of ones and will then send a flag. At the end of sending a flag, if BA2 is reset, the modem will interpret the data in DBUFF as being the first byte of the next frame. After uploading this data for the first byte of the frame, the modem will reset OVRUN. The modem will always reset OVRUN every time it sets BA2, except upon transmitter HDLC initialization.

In the receiver, the OVRUN bit will inform the host that an overrun condition occurred. The overrun condition takes place when the receiver fails to take the byte of data in DBUFF within eight bit times. The modem will thus overwrite the data in DBUFF and, if the host has not taken the data (BA2 is not reset), the modem will set OVRUN. To detect further overrun occurrences, the host must reset this bit.

TRANSMIT MODE CONTROL

After power-up, reconfiguration, or turning $\overline{\text{RTS}}$ input or RTSP bit on, the host must wait for $\overline{\text{CTS}}$ output or CTSP bit to turn on before starting frame transmission.

There are two ways in which the user can signal the modem to exit current HDLC execution. The first way is by setting the SETUP bit which tells the modem that a new configuration is desired. The second way is by turning off $\overline{\text{RTS}}$ input or by resetting the RTSP bit in the interface memory. In both cases, the following events will occur:

1. **If exiting after making sure the modem took the data in DBUFF and then setting EOF,** the modem sends the last byte of data followed by the 16-bit FCS sequence and a closing flag. The

modem then either goes through the turn-off sequence (if RTS output or RTSP bit is turned off), or sets up the new configuration (if SETUP is set).

2. **If exiting during the transmission of an abort sequence**, the modem finishes sending the last byte of the abort sequence, then either goes through the turn-off routine or sets up to a new configuration.

INTERRUPT PROCESSING

Since the R96EFX will be used in an interrupt driven system, a very flexible scratch pad interrupt feature is provided. This feature enables the user to select an interrupt to occur on any combination of bits within an interface memory register.

Interrupt Bits

The programmable interrupt routine runs at the sample rate in all transmitter and receiver modes (9600 Hz). The programmable interrupt request bit, PIREQ (1F:3), is set by the modem whenever the interrupt condition is true. If the programmable interrupt enable bit, PIE (1F:4), is set, the modem sets the programmable interrupt active bit PIA (1F:7). The IRQ output pin then goes low when the PIA bit is set. The host must reset PIREQ after servicing the interrupt.

An interrupt may occur only within a single interface memory register based upon any combination of bits. For example, the host may select register 08 and generate an interrupt whenever bits 08:5, 08:6, and 08:7 are set, but may not select 08:5 and 09:2 to generate an interrupt. The register is selected by specifying the interrupt address ITADRS (0A:4 to 0A:0) as shown in Table 2.

The interrupt bit mask register ITBMSK (0B) selects the bits to be tested in the interface memory register specified by ITADRS. For example, if ITBMSK is equal to FF, all the bits are selected; if ITBMSK is equal to 0F, the four least significant bits are selected.

Operating Modes

There are two operating modes with each mode having four options. The user may choose to OR the selected bits, or to AND the selected bits. Whenever any of the selected bits are set, the OR mode is true, else it is false. The AND mode is true whenever all the selected bits are set, and false otherwise. When bit ANDOR (0A:5) is set, the AND mode is chosen; when it is reset, the OR mode is chosen. The user has the option to be continuously interrupted whenever the mode is true (DC triggered), to be interrupted only when the mode transitions from true to false (negative edge triggered), to be interrupted only when the mode transitions from false to true (positive edge triggered), or to be interrupted when the mode transitions from either false to true or true to false (edge triggered). The host selects one of the options by specifying the TRIG bits (0A:7 and 0A:6) as shown in Table 3.

Table 2. Interrupt Register Addresses

Host Register (Hex)	ITADRS (Hex)	Host Register (Hex)	ITADRS (Hex)
00	00	10	08
01	10	11	18
02	01	12	09
03	11	13	19
04	02	14	0A
05	12	15	1A
06	03	16	0B
07	13	17	1B
08	04	18	0C
09	14	19	1C
0A	05	1A	0D
0B	15	1B	1D
0C	06	1C	0E
0D	16	1D	1E
0E	07	1E	0F
0F	17	1F	1F

Table 3. Interrupt Options

TRIG	Description
00	DC Level Triggered
01	Positive Edge Triggered
10	Negative Edge Triggered
11	Positive or Negative Edge Triggered

AN EXAMPLE IMPLEMENTATION

Refer to R96EFX data sheet (Order No. MD49) for a description of the bits associated with the HDLC and Programmable Interrupt functions.

Transmitter Example

1. Set the modem configuration to the desired speed for transmitting, enable HDLC, parallel data mode, and RTSP.
2. Wait until CTSP goes low and returns to a high level.
3. Place the first byte of data into DBUFF. The modem transmits a flag followed by this byte of data.
4. As soon as BA2 is set, load in the next byte of data. This must occur within eight bit times of BA2 being set.
5. After all information but the last byte is given to the modem, load in the last byte of data in the frame as in step 4.
6. To end the frame, the host must load in the last byte of data into DBUFF, wait for BA2 to be set, and then set EOF.
7. Repeat steps 3 through 6 for all frames to be transmitted.

8. When the last byte of the final frame is loaded into register DBUFF, wait for BA2 to return high. Then set EOF and wait for EOF to return low before resetting RTSP. The modem transmits the last byte followed by the 16-bit FCS and at least one closing flag, depending upon if diagnostics was used to write into the flag counter RAM location as mentioned previously. The modem then goes through its normal turn-off routine.

Receiver Example

The steps to perform a typical HDLC reception are:

1. Set the modem configuration to the desired speed for receiving, enable HDLC, and parallel data mode.
2. Perform a dummy read of DBUFF to reset BA2.
3. Wait until the modem has properly configured.
4. Monitor, through interrupts, the EOF, ABIDL, and BA2 bits in the interface memory.
5. Wait for an interrupt. If it is caused by BA2 being set, read the data in DBUFF. This indicates that the first byte of the first frame is ready for host reading. If the interrupt is caused by EOF being set, check CRC to determine if the current frame is in error and reset EOF. If the interrupt is caused by ABIDL, the modem is receiving the abort/idle sequence. The current frame that was aborted is invalid. The R96EFX does not set the CRC bit or the EOF bit in this case since no FCS checking is done.
6. Continue waiting for interrupts and take appropriate action when the interrupts are received.

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R144HD DSP Programming Guide for the Host Computer

There are software parameters located in the R144HD modem digital signal processor (DSP) that can be accessed and altered by the host computer. These parameters, also referred to as diagnostic data, are accessible via the microprocessor bus. This application note describes information about the DSP parameters in the following catagories:

1. Diagnostic data accessing and scaling
2. DTMF dialing using the dual tone generation configuration
3. Tone detector filter tuning
4. Recommended receive sequence for Group 2
5. Filter characteristics

Refer to the R144HD Data Sheet (Order No. MD33) for additional modem information.

DIAGNOSTIC DATA ACCESSING AND SCALING

DSP RAM DATA ACCESS

The modem contains 256 words of accessible random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a 16-bit real part and a 16-bit imaginary part. Each part can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The contents of XRAM and YRAM may be read or written by the host processor via the microprocessor interface.

The DSP interface memory acts as an intermediary during these host to DSP RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register 0:F (RAM ACCESS S) or 1:F (RAM ACCESS B).

DSP RAM is accessed at internal locations specified by DSP RAM addresses (called access codes) written to DSP interface memory registers 0:F and 1:F. The DSP RAM parameters and their corresponding access codes are listed in Table 1.

When the host reads or writes register 1:0 or 0:0, the modem resets the modem data available bit ,0:E:0 or 1:E:0 (MDAi), to a zero. When the modem reads or writes register 0, the modem sets the MDAi bit to a one. If an Interrupt Enable bit, 0:E:2 or 1:E:2 (IEi), is set to a one by the host and the corresponding MDAi bit is set, the $\overline{IRQ}$ output is asserted and the associated Interrupt Active bit, 1:E:7 or 0:E:7 (IAi), is set to a one by the modem.

The default access codes are 28 for 1:F and 00 for 0:F, which allow the received point eye pattern to be presented serially on EYEX and EYEY, respectively.

READING FROM DSP RAM

When bit 0:5:5 (RAMWS) or bit 1:D:0 (RAMWB) is reset to a zero, data is transferred from DSP RAM onto the microprocessor bus through the DSP interface memory. Each word transferred from DSP RAM to the interface memory is 32 bits long. The 32 bits are written into interface memory registers 0:3, 0:2, 0:1 and 0:0, or 1:3, 1:2, 1:1 and 1:0, in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data, respectively.

WRITING TO DSP RAM

When set to a one, bit 0:5:5 (RAMWS) or bit 1:D:0 (RAMWB) causes the modem to transfer data from interface memory to RAM in chip 0 or in chip 1, respectively. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the most significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAM Access B bits of register 1:F for chip 1, or by means of 0:5:4 (RAE) for chip 0. When bit 1:F:7 or 0:5:4 is set to a one, the XRAM is selected. When bit 1:F:7 or 0:5:4 equals zero, YRAM is selected.

NOTE: When writing to registers 1 and 0, the host must first write to register 1, then to register 0.

Writing to Register 0 resets MDAi to a 0 and starts the write cycle, which ends by MDAi returning to a 1. The RAM Write Bit must remain set until the end of the cycle. A flowchart showing the RAM Write procedure for Chip 0 is shown in Figure 1. The RAM Write procedure for Chip 1 is similar.

Note: To assure correct operation, the maximum allowable time from MDAi (i = 0 or 1) = 1 to writing data into RAM is 80 microseconds.

DIAGNOSTIC DATA SCALING

Table 2 describes the scaling of the modem diagnostic data.

Table 1. R144HD Modem Access Codes

Ref. No.	Function	Access	RAE	Chip	Read Reg. No.
1	Received Signal Samples	40	X	0	2,3
2	Demodulator Output	52	X	0	0,1, 2,3
3	Low Pass Filter Output	54	X	0	0,1, 2,3
4	Average Power	5C	X	0	2,3
5	AGC Gain Word	3E	X	0	2,3
6	Tone 1 Frequency	71	1	0	2,3
7	Tone 1 Power Level	72	1	0	2,3
8	Tone 2 Frequency	71	0	0	0, 1
9	Tone 2 Power Level	72	0	0	0, 1
10	Output Level	7F	0	0	0, 1
11	Checksum, Chip 0	3F	X	0	0, 1
12	Checksum, Chip 1	7F		1	0, 1
13	Equalizer Input	40		1	0,1, 2,3
14	Equalizer Tap Coefficients	02-27		1	0,1, 2,3
15	Unrotated Equalizer Output	74		1	0,1, 2,3
16	Rotated Equalizer Output (Received Point-Eye Pattern)	28		1	0,1, 2,3
17	Decision Points (Ideal)	68		1	0,1, 2,3
18	Error Vector	69		1	0,1, 2,3
19	Rotation Angle	00		1	0,1
20	Frequency Correction	AE		1	2,3
21	Eye Equality Monitor (EQM)	B1		1	2,3
22	G2 Baseband Signal	C8		1	2,3
23	G2 AGC Gain Word	AD		1	2,3
24	G2 AGC Slew Rate	AA		1	2,3
25	G2 PLL Frequency Correction	C2		1	2,3
26	G2 PLL Slew Rate	EF		1	2,3
27	G2 Black/White Threshold	6A		1	0,1
28	G2 Phase Limit	F1		1	2,3

RAE = X is don't care since this location should only be read from,and not written to, by the host.

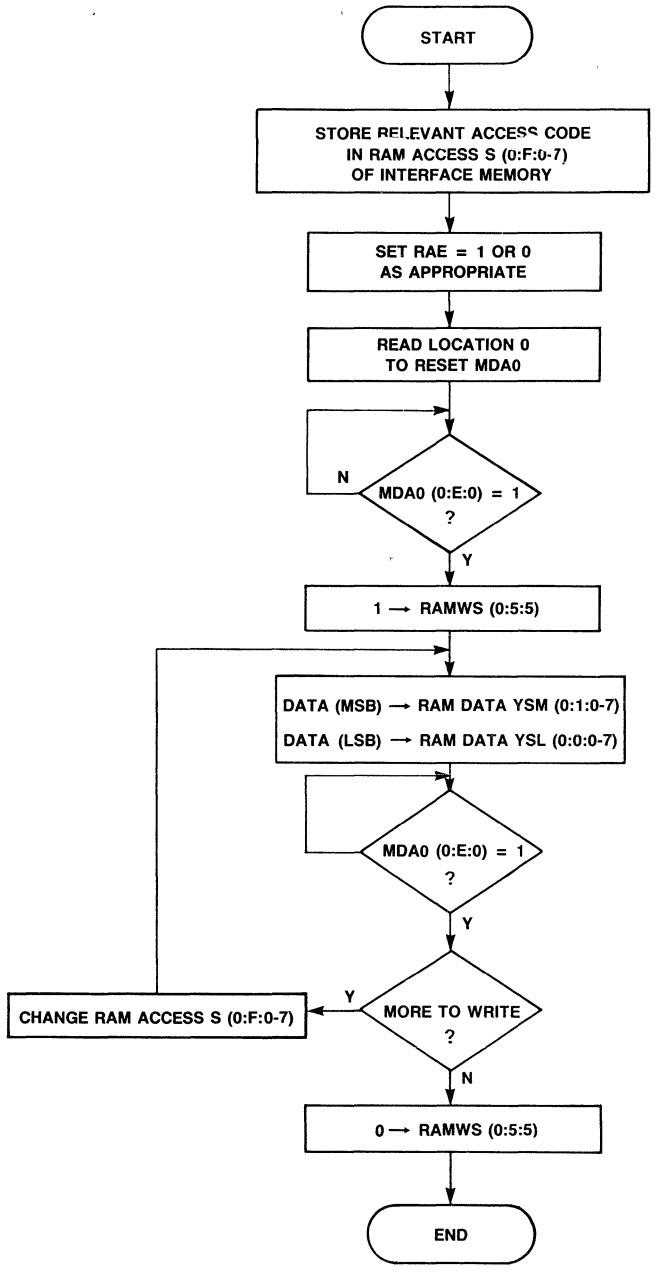


Figure 1. RAM Data Write Routine for DSP Chip 0

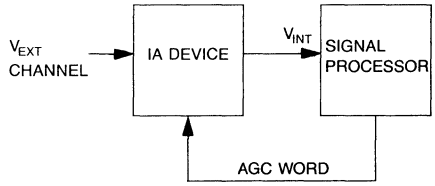
Table 2. Diagnostic Data Scaling

No. 1 – Received Signal Samples = A/D Sample Word

Format: 16 bits, signed, twos complement

Equation: V_{INT} (Volts)= $[(A/D\ Sample\ Word)_{16}/40_{16}] \times (3/256)$

$V_{EXT} = V_{INT} + LOG_{10}^{-1}$ [AGC Gain (dB)/20]



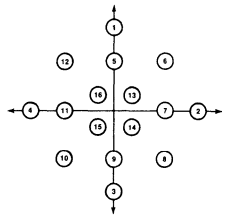
No. 2, 3, 13, 15, 16, and 17 – All Baseband Signal Nodes

Format: 32 bits, complex, twos complement

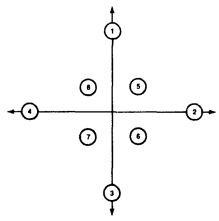
Ideal Baseband Signal Points

	Configuration			
	V.29/9600	V.29/7200	V.29/4800 & V.27/2400	V.27/4800
Point	x (Hex) y (Hex)	x (Hex) y (Hex)	x (Hex) y (Hex)	x (Hex) y (Hex)
1	0000 2800	0000 2400	0000 1C00	0000 1C00
2	2800 0000	2400 0000	1C00 0000	1400 1400
3	0000 D800	0000 DC00	0000 E400	1C00 0000
4	D800 0000	DC00 0000	E400 0000	1400 EC00
5	0000 1800	0C00 0C00		0000 E400
6	1800 1800	0C00 F400		EC00 EC00
7	1800 0000	F400 F400		E400 0000
8	1800 E800	F400 0C00		EC00 1400
9	0000 E800			
10	E800 E800			
11	E800 0000			
12	E800 1800			
13	0800 0800			
14	0800 F800			
15	F800 F800			
16	F800 0800			

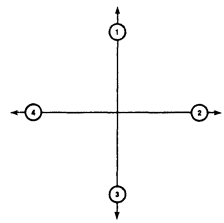
NOTE: V.33 14400, V.33 12000, TCM9600, and TCM7200 constellations are not included.



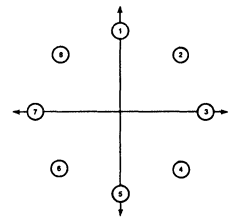
V.29/9600 BPS



V.29/7200 BPS



V.29/4800 BPS and V.27/2400 BPS



V.27/4800 BPS

5

Table 2. Diagnostic Data Scaling (Cont'd)

No. 4 – Average Power

Format: 16 bits, unsigned

Equation: Post-AGC Average Power (dBm) = 10 Log [(Average Power Word)$_{16}$/0889$_{16}$]

Pre-AGC Average Power (dBm) = Post-AGC Average Power –AGC Gain

Typical value: 0889$_{16}$ (corresponding to 0 dBm)

No. 5 – AGC Gain

Format: 16-bits, unsigned

Equation: AGC Gain (dB) = 50 – [(AGC Gain Word)$_{16}$/0040$_{16}$ x 0.098]

Range: 0FC0$_{16}$ to 7FFF$_{16}$ for – 43 dBm Threshold

No. 6 and 8 – Tone 1 and Tone 2 Frequency

Format: 16 bits, unsigned

Equation: N = 6.8267 x (Frequency in Hz)

Convert N to hexadecimal then store in RAM.

No. 7 and 9 – Tone 1 and Tone 2 Power Level

Calculate the power of each tone independently. The total power transmitted in tone configuration is the result of both tone 1 power and tone 2 power.

Format: 16 bits, unsigned

Equation: Output Number = 15033 [$10^{(Po/20)}$]

Where: Po = output power in dBm with series 600 ohm resistor into a 600 ohm load.

Convert Output Number to hexadecimal and store in RAM.

No. 10 – Output Level

Format: 16-bits, unsigned

Equation: Output Number = 36765 [$10^{(Po/20)}$]

Where: Po = output power in dBm with series 600 ohm resistor into a 600 ohm load.

Convert Output Number to hexadecimal and store in RAM.

No. 11 and 12 – Checksum

ROM checksum number determined by revision level.

Format: 16-bits, unsigned

Example: Chip 0 B5410-17: Checksum = 69CF
Chip 1 B5411-16: Checksum = 9FF9

Table 2. Diagnostic Data Scaling (Cont'd)

No. 14 – Equalizer Taps

No. 14 is a set of RAM locations containing adaptive equalizer tap coefficients.

The equalizer tap access codes can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers they require two write operations per tap, one for the real part and one for the imaginary part. When writing or reading the tap coefficients, follow the table below.

Registers 1:1 and 1:0 hold the most and least significant bytes, respectively, of the 16 bits during a write operation.

Format: 32 bits, complex, twos complement

Configuration	Number of Equalizer Taps	Read Access Codes	Write Access Codes X Access	Write Access Codes Y Access
V.33	38	02-27	82-A7	02-27
V.29	38	02-27	82-A7	02-27
V.27	16	02-11	82-91	02-11

No. 18 – Error Vector

Represents the difference between the received point (P2) and the nearest ideal point (P1).

Format: 32 bits, complex, twos complement

Error Vector Maximum Values

Configuration	Bit Rate (bps)	Real Error Registers 3 and 2 (Hex)	Imaginary Error Registers1 and 0 (Hex)	Magnitude $\sqrt{(Re^2 + Im^2)}$ (Hex)
V.29	9600	<0C00	<0C00	<0E66
V.29	7200	<2400	<2400	<2400
V.29	4800	<1C00	<1C00	<1C00
V.27	4800	<1C00	<1C00	<1C00

Note: Due to the trellis coding in V.33, error vectors are not applicable in V.33 configurations.

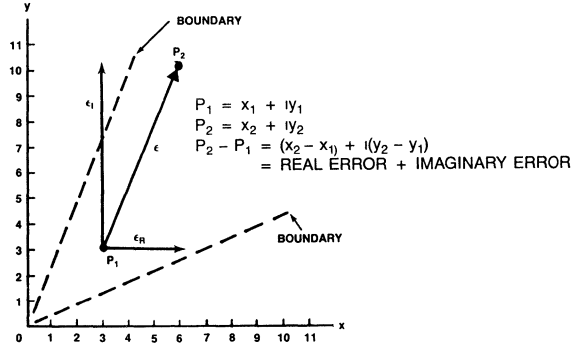


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Table 2. Diagnostic Data Scaling (Cont'd)

No. 19 – Rotation Angle

Represents instantaneous correction for phase and frequency errors.

Format: 16-bits, twos complement

Equation: Rotation Angle (degrees) = $[(\text{Rot. Angle Word})_{16}/10000_{16}] \times 180$

No. 20 – Frequency Correction

Represents component of rotation angle caused by frequency error.

Format: 16 bits, twos complement

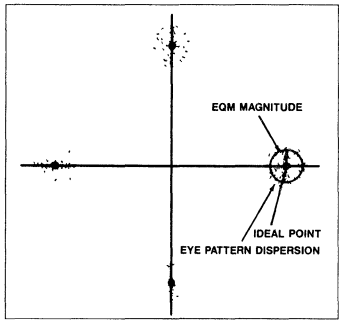
Equation: Freq. Correction (Hz) = $[(\text{Freq. Correction Word})_{16}/10000_{16}]$ x Baud in Hz

Range: $FC00_{16}$ to 0400_{16} representing ±37.5 Hz

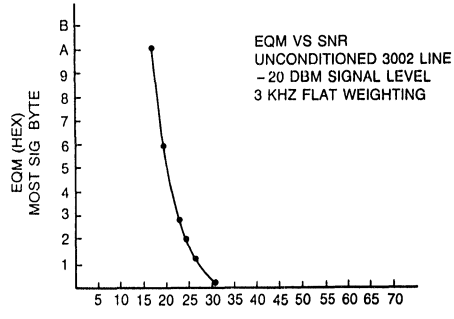
No. 21 – Eye Quality Monitor (EQM)

EQM equals the filtered squared magnitude of the error vector for V.29 and V.27 and is related to the path length for V.33. Proportionality to bit error rate is determined by particular application. EQM stabilizes in approximately 700 baud times from $\overline{\text{RLSD}}$ going active for V.29 and V.27, and approximately 1200 baud times for V.33.

Format: 16 bits, unsigned



Relationship of EQM to Eye Pattern



Typical Eye-Quality Versus Signal-to-Noise Ratio for V.29/9600

No. 22 – Group 2 Baseband Signal

Format: 16 bits, unsigned

Range: 0000_{16} to 0600_{16} represents black
1000_{16} to 2100_{16} represents white

No. 23 – Group 2 AGC Gain

Format: 16-bits, unsigned

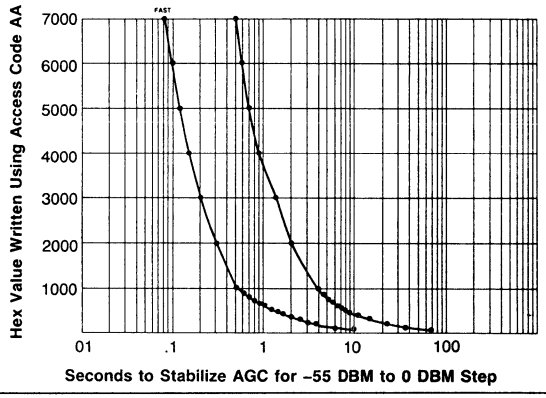
Equation: AGC Gain Word = $50 - [(\text{AGC Gain Word})_{16}/40_{16} \times 0.098]$

Table 2. Diagnostic Data Scaling (Cont'd)

Node 24 – Group 2 AGC Slew Rate

Can be adjusted by the host.

Range: 0000_{16} to $7FFF_{16}$



No. 25 – Group 2 PLL Frequency Correction

Format: 16 bits, twos complement

Range: $FCBA_{16}$ to 0346_{16} representing ±140 Hz

Equation: Frequency correction (Hz) = Frequency correction number x (0.167)

No. 26 – Group 2 PLL Slew Rate

Represents gain of first order term in phase locked loop. Directly proportional to PLL slew rate

Range: 0010_{16} to 7000_{16} for stable operation

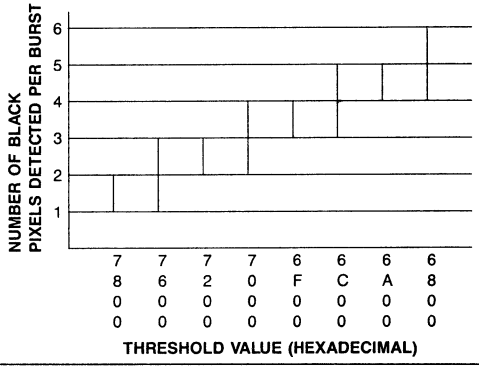
No. 27 – Group 2 Black/White Threshold

Format: 16 bits, unsigned

Default value: 7800_{16}

Graph Notes:

1. 100 white pixels sent followed by 4 black pixels sent.
2. Results obtained at 0 dBm, no compromise equalizers in back-to-back connection.



No. 28 – Group 2 Phase Limit

When phase error exceeds this limit, PLL updating is suspended. Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits.

Format: 16 bits, twos complement

Default value: 5000_{16} representing ±27.34°

Equation: Phase Limit = 360° x (2100/10368) x [7FFF – $(\text{Phase Limit})_{16}$]/7FFF

5

DTMF DIALING

The R144HD includes tunable oscillators that can be used to perform dual-tone multi-frequency (DTMF) dialing. The frequency and amplitude of each oscillator output is under host control. A programmable tone detector can also be used in call establishment to recognize an answer tone.

This section describes the method of oscillator and filter tuning by the host processor and provides an example of an autodialer routine that may be programmed in the host.

DTMF REQUIREMENTS

EIA Standard RS-496, paragraph 4.3.2, specifies requirements that ensure proper DTMF signaling through the public switched telephone network (PSTN). These tones consist of two sinusoidal signals, one from a high group of three frequencies and one from a low group of four frequencies, that represent each of the standard pushbutton telephone characters shown in Table 3.

Signal power is defined for the combined tones as well as for the individual tones. Both maximum and minimum

Table 3. DTMF Signals

Low Frequency	High Frequency		
	1209 Hz	1336 Hz	1447 Hz
697 Hz	1	2	3
770 Hz	4	5	6
852 Hz	7	8	9
941 Hz	*	0	#

power requirements are functions of loop current. By combining the various requirements of RS-496, compromise power levels can be determined that meet the power specification for all U.S. lines (when driving the PSTN from a 600 ohm resistive source). The high frequency tone should be at a higher power level than the low frequency tone by approximately 2 dB. The maximum combined power, averaged over the pulse duration, should not exceed +1 dBm. The minimum steady state power of the high frequency tone should not be less than –8 dBm. When connecting the modem circuit to the PSTN by means of a data access arrangement (DAA) set for permissive mode, the DAA gain is –9 dB. The modem circuit must, therefore, drive the DAA input with +1 dBm of steady state high frequency power and –1 dBm of steady state low frequency power in order to meet all of the listed conditions.

The required duration of the DTMF pulse is 50 ms minimum. By experience, a pulse duration of approximately 95 ms is more reliable. The required interval between DTMF pulses is 45 ms minimum and 3 seconds maximum. Again, by experience, an interdigit delay of approximately 70 ms is preferred.

The remaining requirements of RS-496, relative to DTMF dialing, are not influenced by the host processor. These requirements are all met by the modem's oscillators.

SETTING OSCILLATOR PARAMETERS

The oscillator frequency and output power are set by the host computer in DSP RAM using the microprocessor bus and diagnostic data routine.

When setting the frequency of tone 1, the host must write a 16-bit hexadecimal number into RAM using RAM access code 71 with bit RAE = 1. When setting the frequency of tone 2, a 16-bit hexadecimal number must be written into RAM using RAM access code 71 with bit RAE = 0. The power levels of tone 1 and tone 2 are set by writing 16-bit hexadecimal numbers into RAM using RAM access code 72 with bit RAE = 1, and with RAE = 0, respectively. The hexadecimal numbers written into these RAM locations are scaled as shown for nodes 6 through 9 in Table 2.

These decimal numbers must be converted to hexadecimal form then stored in RAM by following the RAM data write routine illustrated by Figure 1. Hex 3FFF is the maximum value of power level number without harmonic distortion.

Hexadecimal numbers for DTMF generation are listed in Table 4. Power levels are selected to give the desired output power for each tone (0 dBm for the high frequency tone and –2 dBm for the low frequency tone) while compensating for modem filter characteristics.

DETECTING ANSWER TONE

Frequency detector bit FR1 (1:B:5) can be used to detect a 2100 Hz answer tone when connection to the remote modem is successful. Bit FR1 goes active (one) when energy above the turn-on threshold is present at 2100 Hz ±25 Hz. At the end of the answer tone, FR1 returns to zero and data transmission can begin.

COMPLETE CALLING SEQUENCE

A complete calling sequence consists of several steps including modem configuration, telephone number selection, DTMF transmission, and answer tone detection. A sample flow chart for implementing an auto-dialer in host software is illustrated in Figure 2.

The auto-dialer routine may be entered at one of two points; either AUTO DIAL or REDIAL. When entering at AUTO DIAL, the host prompts the user to enter a phone number, which is then stored in the phone number buffer. When entering at REDIAL, the routine dials the number

previously stored in the phone number buffer and does not issue a user prompt.

Table 4. DTMF Parameters

Digit	RAM Access S	RAE	Value (Hex)
	71	1	1918
	71	0	23A0
0	72	1	2D46
	72	0	3900
	71	1	1296
	71	0	203D
1	72	1	2D46
	72	0	3900
	71	1	1296
	71	0	23A0
2	72	1	2D46
	72	0	3900
	71	1	1296
	71	0	2763
3	72	1	2D46
	72	0	3900
	71	1	1488
	71	0	203D
4	72	1	2D46
	72	0	3900
	71	1	1488
	71	0	23A0
5	72	1	2D46
	72	0	3900
	71	1	1488
	71	0	2763
6	72	1	2D46
	72	0	3900
	71	1	16B8
	71	0	203D
7	72	1	2D46
	72	0	3900
	71	1	16B8
	71	0	23A0
8	72	1	2D46
	72	0	3900
	71	1	16B8
	71	0	2763
9	72	1	2D46
	72	0	3900
	71	1	1918
	71	0	203D
*	72	1	2D46
	72	0	3900
	71	1	1918
	71	0	2763
#	72	1	2D46
	72	0	3900

Interrupts not required during dialing are disabled to prevent errors in real time delays. Interrupt status is saved to allow restoring these interrupts when dialing is complete. The current modem configuration is saved prior to selecting the DTMF Transmit configuration, then restored at the completion of the auto-dialer routine to allow data transfer.

The commands for off-hook and request coupler cut through are typical of signals required by data access arrangements that may be connected to the modem for switched network operation.

Since the number to be dialed varies in length depending on the requirements of various PBX equipment, domestic telephone companies, and foreign PTTs, the number buffer must allow for numbers of different length. The method used in Figure 2 to determine the end of valid bytes in the buffer is zero recognition. After the last digit is entered, the carriage return must place a hexadecimal 00 (ASCII NUL character) in the buffer. All other bytes must be non-NUL ASCII characters. Only numeric characters (ASCII 30 through 39) are printed and dialed. Non-numeric characters are tested for comma and NUL. Comma causes a 2-second pause in dialing to allow for known delays in the telephone network or PBX. NUL ends the dialing portion of the routine and begins the answer tone detection portion. All other characters are ignored.

The answer tone detection logic allows 30 seconds for 2100 Hz recognition. If answer tone is not recognized within this time limit, the call is aborted. If answer tone is recognized, the routine jumps to the data handling software.

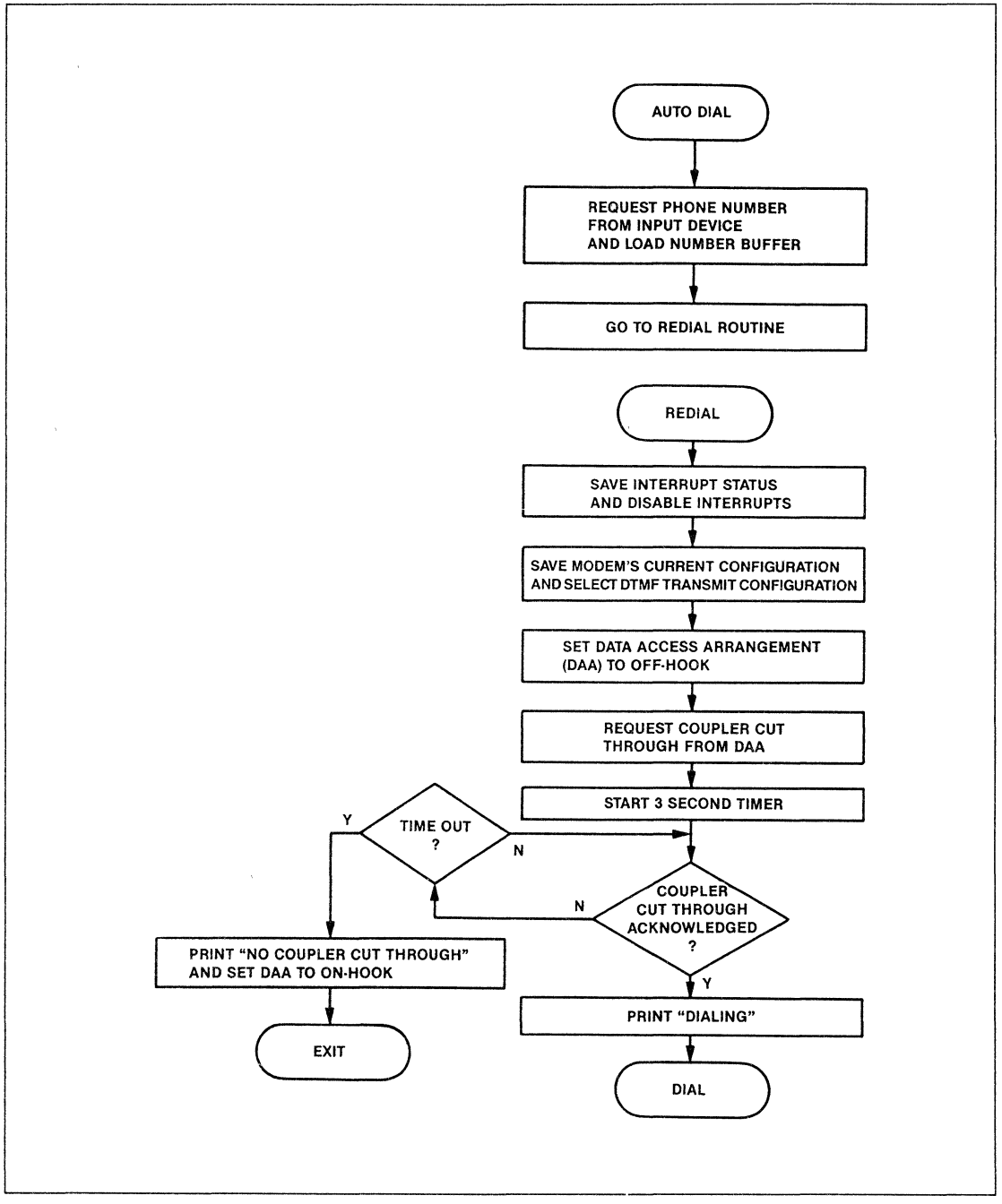


Figure 2. Autodialer Flow Chart

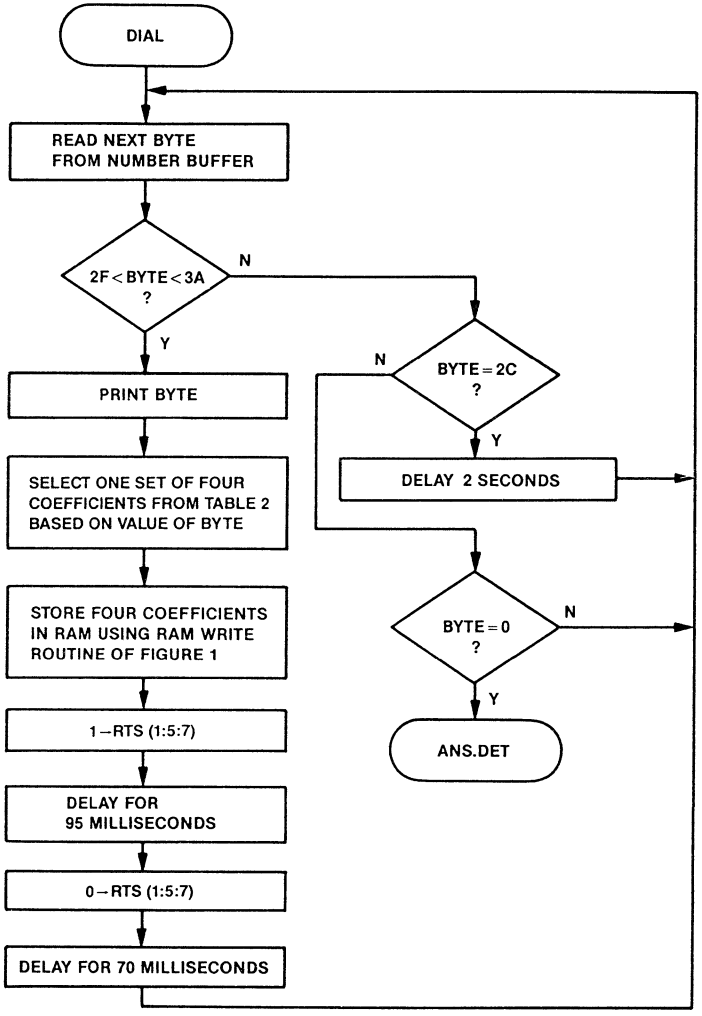


Figure 2. Autodialer Flow Chart (Cont'd)

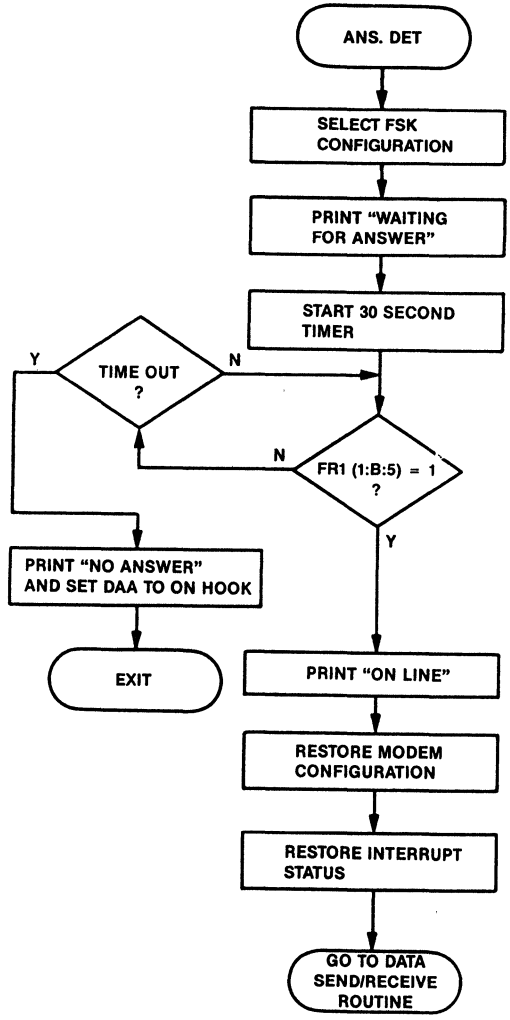


Figure 2. Autodialer Flow Chart (Cont'd)

ADDED FEATURES

The application of modem tone generation and detection to DTMF dialing and answer tone recognition can be extended to include additional features.

Call Progress Monitoring

The tone detector can monitor call progress for dial tone, busy signal or ringback tone. The detector filter must be retuned to detect different frequencies used in call progress signaling. Table 5 lists tones for various lines in the Bell network. These call progress signals vary according to the telephone networks of each country.

Single Tone Generation

In OEM equipment that combines the features of a modem with those of a telephone handset, the tone generators may be used to generate a caller reassurance tone (or even music) while the caller is kept on hold. To generate a single tone, set one of the oscillators to zero frequency or zero amplitude while the other oscillator is keyed on by the RTS bit. This technique is also applicable for generating a 2100 Hz answer tone when the modem is used to automatically answer a call. The parameters for 2100 Hz answer tone generation are listed in Table 6.

Table 6. 2100 Hz Answer Tone Parameters

Frequency	RAM Access S	RAE	Value
2100 Hz	71	1	3800
	71	0	0000
	72	1	3456
	72	0	0000

Table 5. Call Progress Signals

Tone	Frequency (Hz)*	Interruption Rates	Use
Precision Dial Tone	350 + 440	Continuous	Dialing may commence
Old Dial Tones	600 + 120 or 133, and other combinations	Continuous	Dialing may commence
Precision Busy	480 + 620	0.5 Sec. On 0 5 Sec. Off	Called line busy
Old Busy	600 + 120	0.5 Sec. On 0.5 Sec. Off	Called line busy
Precision Reorder	480 + 620	0.3 Sec. On } Local 0.2 Sec. Off } Reorder	All local switching paths busy, all trunks busy, all paths or trunks busy
Old Reorder	600 + 120	0 2 Sec. On } Toll 0.3 Sec Off } Reorder 0 25 Sec On } Toll 0 25 Sec Off } Local	
Precision Audible Ringing	440 + 480	2 Sec. On 4 Sec. Off	To calling customer
Old Audible Ringing	420 + 40, and other combinations	2 Sec. On 4 Sec. Off	To calling customer
Call Waiting	440	0.3 Sec. On	Call waiting service; an incoming call is waiting
Precision Receiver Off-Hook (ROH)	1400 + 2060 + 2450 + 2600	On and Off 5 Times per Sec	To cause off-hook customers to go on-hook
Precision High Tone	480	Continuous	To cause off-hook customers to go on-hook
Old High Tone	480, 400 or 540		
Recorder Connector Tone	1400	On 0 5 Sec Every 15 Seconds	To indicate call is being recorded by distant customer

*A " + " sign indicates either superposition (precision tones) or modulation (old tones).

5

TONE DETECTOR FILTER TUNING

The R144HD modem includes three independent tone detectors (F1, F2, and F3). These tone detectors are operational when the modem is configured for V.21 FSK, and are centered, upon power-up, to 2100 Hz (F1), 1100 Hz (F2), and 462 Hz (F3). This section presents a method of tuning these detectors to any desired frequency in the 400 Hz - 3 kHz band.

NOTE: F1, F2 and F3 should not be used as dual tone detectors (i.e., during call progress tone detection). Detecting one of the two tones is the preferred method for call progress monitoring.

COMPUTATION OF TONE DETECTOR COEFFICIENTS

Each tone detector consists of two second-order filters in cascade, an energy averaging filter and a threshold comparator. A diagram of a tone detector is shown in Figure 3.

Filter 1 has a transfer function:

$$H_1(Z) = \frac{2\alpha}{1 - 2\beta_1 Z^{-1} - 2\beta_2 Z^{-2}} \quad \text{(Eq. 1)}$$

Filter 2 has a transfer function:

$$H_2(Z) = \frac{2\alpha'}{1 - 2\beta'_1 Z^{-1} - 2\beta'_2 Z^{-2}} \quad \text{(Eq. 2)}$$

The energy averaging filter has a transfer function:

$$H_3(Z) = \frac{\alpha''}{1 - \beta'' Z^{-1}} \quad \text{(Eq. 3)}$$

The output of the energy averager is fed to a threshold comparator which sets or resets the appropriate bit in interface memory (FR1, FR2, or FR3) if the energy output is equal to or greater than 1/8, or less than 1/8, respectively.

Filters 1 and 2 have a typical frequency response as shown in Figure 4. When cascaded, they form a bandpass filter with a narrow bandwidth as shown in Figure 5.

Given the transfer functions $H_1(Z)$ and $H_2(Z)$, an analytical method is required to compute their coefficients for any desired frequency in the 300 Hz – 3 kHz band. First, consider $H_1(Z)$. This transfer function can be rewritten as:

$$H_1(Z) = \frac{2\alpha Z^2}{Z^2 - 2\beta_1 Z - 2\beta_2} \quad \text{(Eq. 4)}$$

which has a conjugate pair of poles:

$$P_1 = \beta_1 + j\sqrt{(\beta_1{}^2 + 2\beta_2)}$$

and

$$P_2 = \beta_1 - j\sqrt{(\beta_1{}^2 + 2\beta_2)}$$

These poles lie on a circle of radius 0.994030884 on the Z-plane. The radius of the tone detector circle was chosen so that each filter has a high Q without being unstable (i.e., poles must lie inside the unit circle for stability). Figure 4 shows a Z-plane pole-zero diagram for an arbitrary conjugate pole pair on the tone detector circle. The angle $\theta = 360° \times fo/fs$, where fo is the desired center frequency and fs is the sampling rate (fs = 9600 Hz). The following equations are derived from the angle and magnitude of the posi-

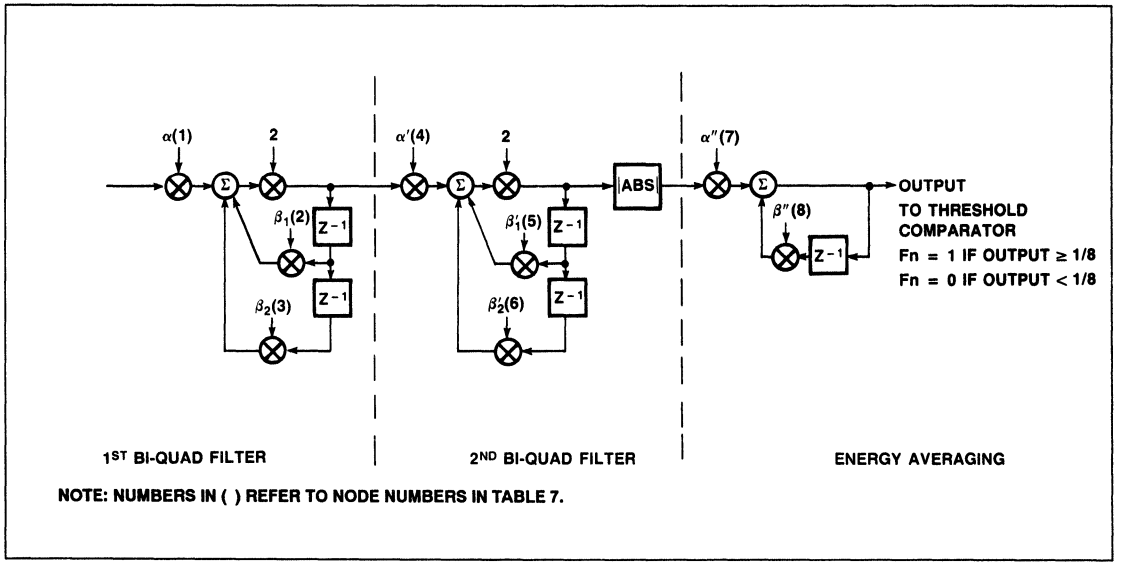


Figure 3. R144HD Tone Detector Diagram

tion vector pointing to a pole pair located at the desired angle:

$$\cos^{-1}(\beta_1/r) = \theta = 360^\circ \times f_O/f_S \quad \text{(Eq. 5)}$$

$$\sqrt{[\beta_1^2 + (-\beta_1^2 - 2\beta_2)]} = r = 0.994030884 \quad \text{(Eq. 6)}$$

solving for β_1 and β_2:

$$\beta_1 = r \cos (360^\circ \times f_O/f_S) \quad \text{(Eq. 7)}$$

$$\beta_2 = -r^2/2 \quad \text{(Eq. 8)}$$

In deriving these equations, only $H_1(Z)$ was considered. However, the tone detector consists of two identical filters in cascade. Referring to Figure 5, shifting filter 1 and filter 2 above and below the desired center frequency, a response with the desired bandwidth is achieved. Furthermore, since α controls the amplitude response, one may set $\alpha = \alpha'$ to uniformly raise or lower the overall cascade response.

From Equation 8, we see that:

$$\beta_2 = \beta'_2 = -r^2/2 = -0.494048699$$

Rewriting Equation 7 in terms of the offsets f_A and f'_A we obtain:

$$\beta_1 = r \cos [360^\circ (f_O - f_A)/f_S] \quad \text{(Eq. 9)}$$

$$\beta'_1 = r \cos [360^\circ (f_O + f'_A)/f_S] \quad \text{(Eq. 10)}$$

The frequency offset is approximately 72% of B/2 (half the bandwidth):

$$f_A \approx 0.72\ (B/2) \quad \text{(Eq. 11)}$$

The value of f_A should be equal to f'_A. However, f_A may be chosen 1% smaller than f'_A to compensate for the fact that the overall cascade response is not prefectly symmetrical (see Figure 7).

The values for the coefficients α and α' that set $|H(f_O)| =$ 0 dB in equations 1 and 2 were measured and plotted versus center frequency f_O as shown in Figure 8. Three equations corresponding to three linear approximations result:

$$\alpha = \alpha' = \frac{(104/319)f_O - 78.62}{32767}$$

$$400 \le f_O \le 1100 \text{ Hz} \quad \text{(Eq. 12a)}$$

$$\alpha = \alpha' = \frac{(44/275)f_O + 104}{32767}$$

$$1100 \le f_O \le 1650 \text{ Hz} \quad \text{(Eq. 12b)}$$

$$\alpha = \alpha' = \frac{(4/45)f_O + 221}{32767}$$

$$1650 \le f_O \le 3000 \text{ Hz} \quad \text{(Eq. 12c)}$$

ENERGY AVERAGING FILTER

The coefficients of the energy averaging filter are determined by a Z-domain approximation to an RC circuit of transfer function $H(S) = 1/1 + S\tau$:

$$\alpha'' = \frac{1}{1 + 9600\tau} \quad \text{(Eq. 13)}$$

$$\beta'' = \frac{1}{(1 + 1/9600\tau)} \quad \text{(Eq. 14)}$$

Upon power-up, α'' and β'' are set for $\tau = 0.1$ seconds. Unless different tone detector response times are required, these coefficients need not be changed.

FILTER COEFFICIENTS

Table 6 contains the computed values of the filter coefficients, including those of default frequencies 462 Hz, 1100 Hz, and 2100 Hz. The value 32767 (Hex 7FFF) is full scale in the SP's machine units (i.e., 32767 = unity). Coefficients may range from –1 to +1 (FFFF to 7FFF in machine units).

NOTE: Default coefficents are loaded into the DSP RAM each time the modem enters into Tone Detection mode (V.21 FSK Receiving mode). The procedure to load new coefficients after entering Tone Detection mode is:

1. Wait for the SETUP bit to be reset.
2. Wait a minimum of 1 ms.
3. Write new coefficients into DSP RAM.

The host should set the SETUP bit when changing from FSK transmitting mode to Tone Detection mode, as well as when reconfiguring the modem.

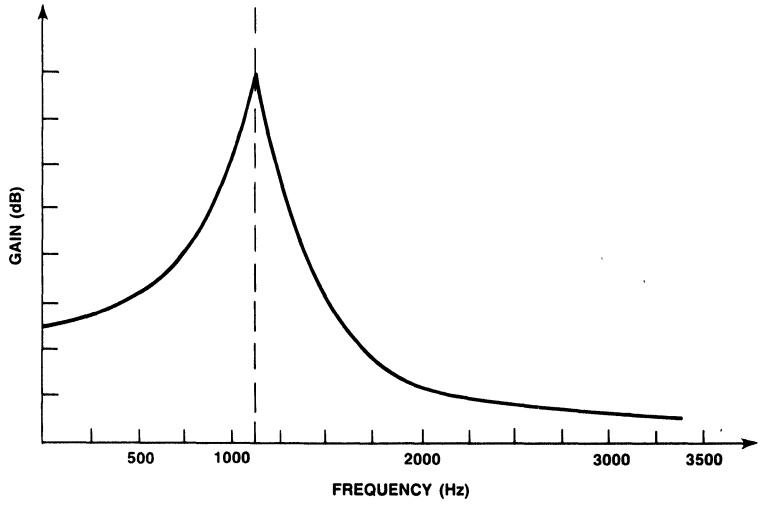


Figure 4. Typical Single Filter Response

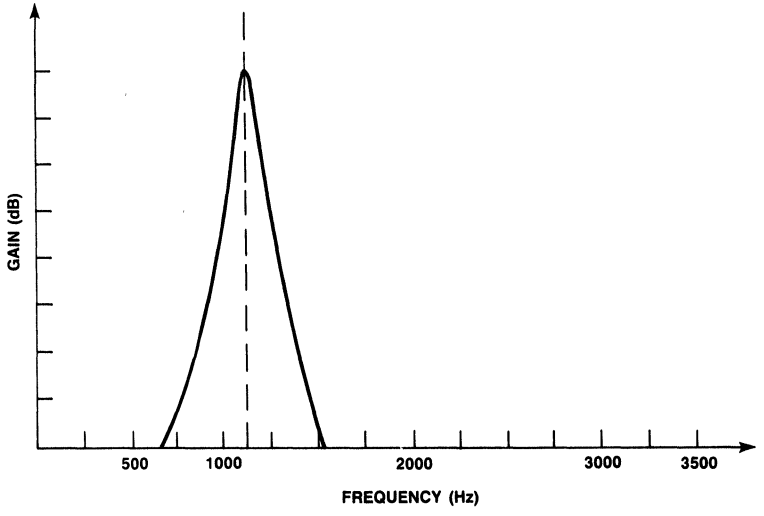


Figure 5. Typical Cascade Filter Response

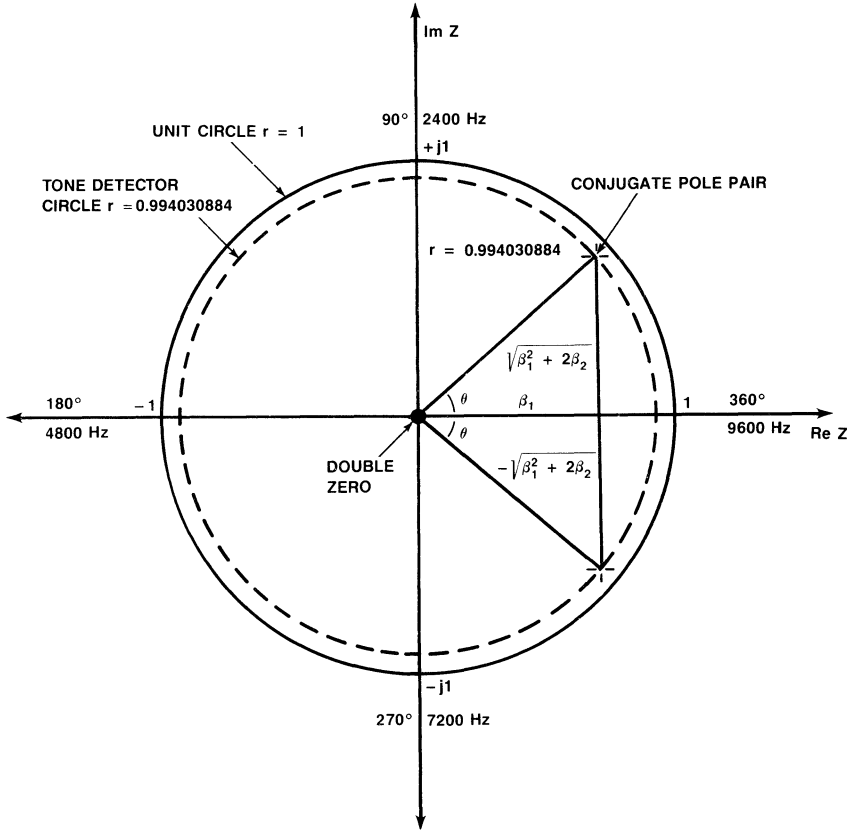


Figure 6. Z-Plane Pole-Zero Diagram

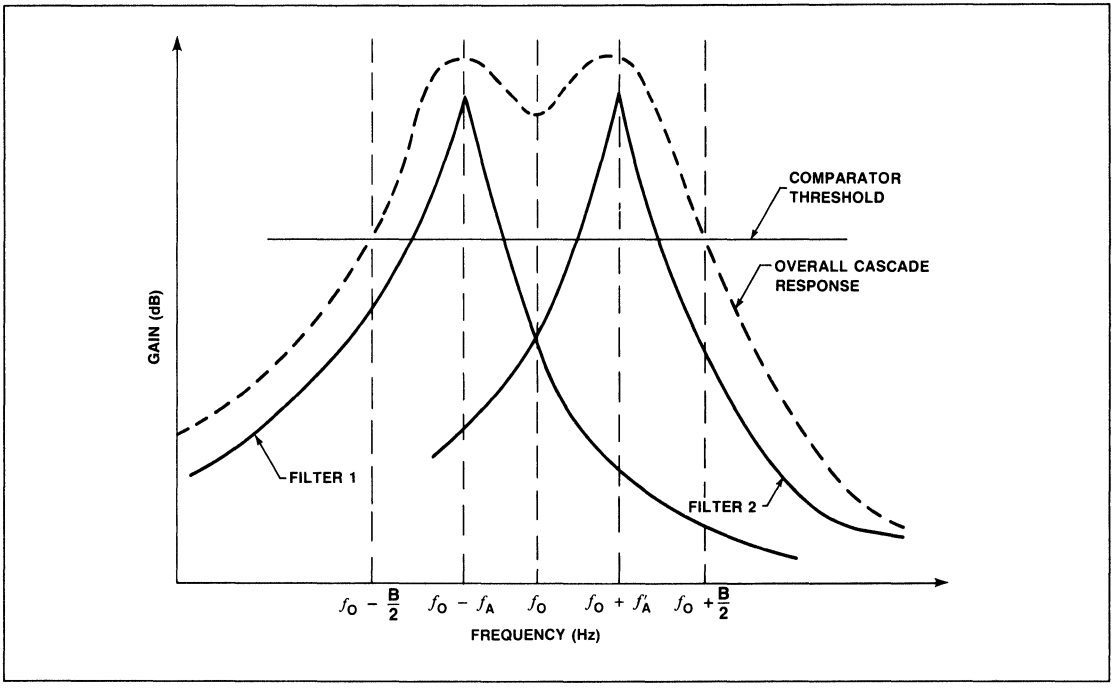


Figure 7. Bandwidth and Offset Frequencies

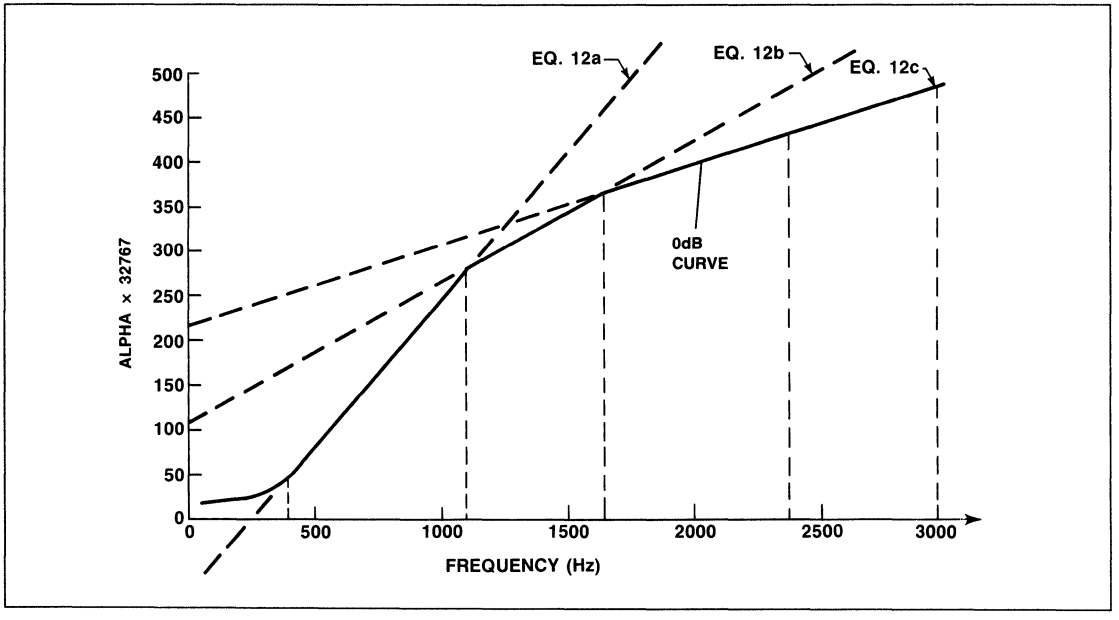


Figure 8. Alpha versus Center Frequency

Table 6. Calculated Coefficient Values

Frequency Detected	Coefficient Name	Coefficient Value	
		Hex	Decimal
2100 Hz ±25 Hz	$\alpha = \alpha'$	0198	408/32767
	β_1	1A4A	6730/32767
$f_A \cong 18$ Hz	β'_1	175A	5978/32767
	$\beta_2 = \beta'_2$	C0C5	−16187/32767
1850 Hz ±24 Hz	$\alpha = \alpha'$	0180	384/32767
	β_1	2E37	11831/32767
$f_A \cong 18$ Hz	β'_1	2B69	11113/32767
	$\beta_2 = \beta'_2$	C0C4	−16188/32767
1100 Hz ±30 Hz	$\alpha = \alpha'$	01F3	280/32767
	β_1	60B2	24754/32767
$f_A \cong 19$ Hz	β'_1	5E9C	24220/32767
	$\beta_2 = \beta'_2$	C0C4	−16188/32767
462 Hz ±14 Hz	$\alpha = \alpha'$	0048	72/32767
	β_1	79F3	31219/32767
$f_A \cong 10$ Hz	β'_1	7974	31092/32767
	$\beta_2 = \beta'_2$	C083	−16253/32767

Table 7. RAM Access Codes for Filter Coefficients

Node No. (n)	RAM Access Code (Hex)			
	Name	F1	F2	F3
1	α	2E	34	3A
2	β_1	2F	35	3B
3	β_2	30	36	3C
4	α'	2B	31	37
5	β'_1	2C	32	38
6	β'_2	2D	33	39
7	α''	B7	B9	BB
8	β''	B8	BA	BC

NOTE: Nodes 1-6 are read from registers 1:1 and 1:0. Nodes 7 and 8 are read from 1:2 and 1:3.

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RECOMMENDED RECEIVE SEQUENCE FOR GROUP 2 FACSIMILE

The R144HD includes a transmit and receive configuration that is compatible with the transmission scheme of Group 2 facsimile equipment. In order to achieve the best results with Group 2 reception, the following procedure is recommended. The step numbers are keyed to points in Figure 9.

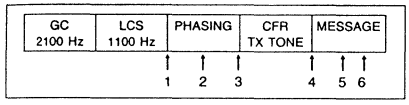

Figure 9. Group 2 Facsimile Sequence

METHOD

1. Enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Write hex 0038 using access code C2. This action sets the Group 2 phase-locked-loop (PLL) for a frequency correction of 9 Hz, causing the phase term to drift rapidly to overcome any tendency to slow phase recovery.
   b. Write hex 4000 using access code F0, and hex 7FFF using access code 70. This action allows the Group 2 PLL to accept the greatest number of samples for carrier recovery during phasing.
   c. Write hex 2000 using access code AA. This action sets the AGC slew rate for very fast acquisition.
   d. Set control bit G2FGC (1:C:0) to a one to select fast AGC state.

2. After phasing is detected, wait approximately 2 seconds for the AGC circuit to settle. Then:
   a. Write hex 0000 using access code AA. This action stops AGC tracking in order to preserve the present AGC setting.
   b. Reset control bit G2FGC (1:C:0) to a zero to select slow AGC state. This action changes the Group 2 PLL characteristics to match reduced AGC response.
   c. Read and save the 16-bit value from registers 1:3 and 1:2 using access code C2. This value represents the frequency error term from the Group 2 PLL.
   d. Verify that phasing signal is still being received. This action guarantees that AGC value was frozen during phasing signal.
   e. If step d above determines that phasing signal is present, allow transmission of CFR. If phasing signal is not present, suppress CFR.

3. Exit Group 2 configuration.

4. At completion of CFR transmission, re-enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Repeat step 1.b.
   b. Repeat step 2.a.
   c. Add hex 0038 to the value saved in step 2.c above and write the sum using access code C2. This action forces a 9 Hz error as in step 1.a.

5. Wait for start of Group 2 message transmission. Then:
   a. Write hex 0400 using access code AA. This action restores the AGC slew rate to the default value.
   b. After 2 lines, write the value saved in step 2.c using access code C2. This action removes the 9 Hz forced frequency error without waiting for the phase-locked-loop to complete the correction. This step is optional as the correction will eventually be completed, but, depending on the percentage of white in the document being sent, the correction may take from 4 to 6 lines (100 ms of white required).

6. After approximately 6 to 10 seconds of message reception, perform either step a or step b below:
   a. Write hex 6100 using access code F0, and hex 0600 using access code 70. This action places narrow limits on the received signal used for carrier recovery during message reception and reduces the chance of errors caused by repeated patterns in the message.
   b. Synchronize the modem's Group 2 PLL to the facsimile machine's blanking signal as follows:
      (1) Freeze the phase-locked-loop during data by:
         (a) Writing hex 7FFF using access code F0.
         (b) Writing hex 0000 using access code 70.

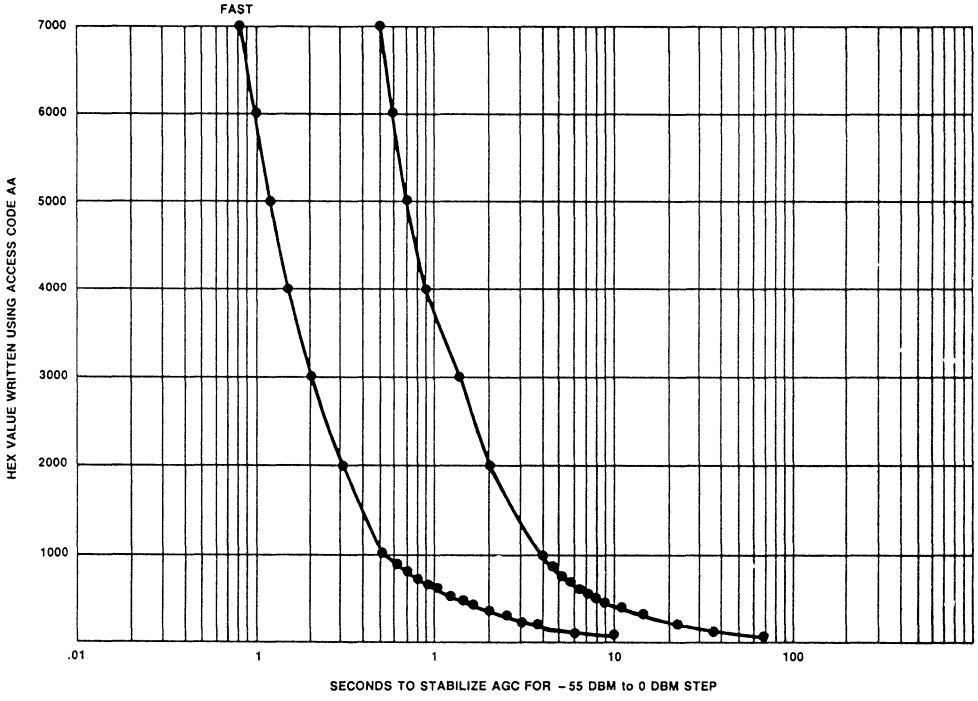

Figure 9. AGC Slew Rate

(2) Enable the phase-locked-loop during the white margins by:

(a) Writing hex 4000 using access code F0.

(b) Writing hex 7FFF using access code 70.

(c) The sequence of writing in step 6.b is important and must be performed as described. Option 6.b requires more action by the host processor, but it eliminates the possibility of data patterns affecting carrier recovery.

PARAMETER SCALING

1. Access code C2 represents frequency error, i.e., the deviation of received carrier from 2100 Hz.

   LSB = 0.167 Hz; Range = ± 140 Hz.

2. Access code EF represents the Group 2 PLL slew rate for the first order term. The number is directly proportional to slew rate. The range of stable operating values is 0010 to 7000 in hexadecimal.

3. Access code AA represents the AGC slew rate.

   Range = 0000 to 7FFF in hexadecimal.

   Scaling: See Figure 9.

4. Access codes F0 and 70 represent limits on acceptable zero crossing for use by the carrier recovery loop. The carrier recovery loop uses several nonlinear controls in attempting to lock the zero crossing of the local carrier to those of the transmitter. Since Group 2 facsimile uses VSB transmission, it is necessary to either reconstruct the upper sideband or exclude those zero crossings that represent frequencies other than 2100 Hz. The modem excludes unwanted zero crossings by testing the effective slope of the waveform as it crosses zero. In Figure 10, points A and B represent samples taken about a zero crossing over a sample period T, where T = 1/10,368 seconds.

   The magnitude of [|A| + |B|] is directly proportional to the slope of line segment AB and is, therefore, an indicator of frequency. If H represents the value stored at F0 and L represents the value at 70, then 1 – [|A| + |B|] + H + L must be greater than positive full scale or the frequency is excluded for being too high.

   The average value for 1 – [|A| + |B|] with an all white transmission and back-to-back connection is hex 19A1 ± 0543.

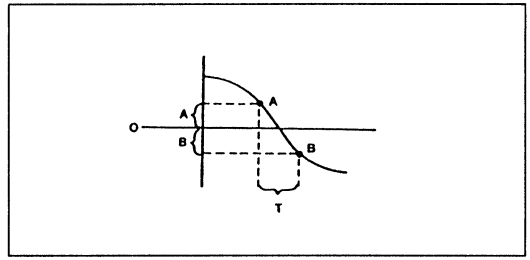

Figure 10. Samples of Zero Crossing

5. Access code F1 allows host control of the limits placed on phase error correction. When the phase error exceeds the limit set by F1, PLL updating is suspended. The default value of 5000 corresponds to a limit of ± 67.5 degrees. A zero in F1 causes the PLL to update for any phase error. By resetting F1 to a zero, it may be unnecessary to force a frequency offset in the receive sequence.

   For systems using step 6.a in the receive sequence, reception of messages containing a large amount of black may be improved by setting F1 to zero. F1 scaling is:

   $$\text{Phase limit} = 360° \times (2100/10368) \times [7FFF - (\text{Phase Limit})_{16}]/7FFF$$

   Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits, etc.

BLACK/WHITE THRESHOLD

The modem receives a Group 2 baseband signal that contains density (gray scale) information in the amplitude modulation. In order for this information to be used on a Group 3 facsimile machine, the modem converts the gray scale to black/white baseband form. The threshold at which the black/white decision is made determine the density of the received page.

Access code 6A represents the Group 2 black/white threshold. This location defaults to hex 7800 at POR time. The number may be increased or decreased by the host to achieve a page weighted more toward white or toward black, respectively.

FILTER CHARACTERISTICS

The modem includes an integrated analog device which uses switched capacitor filters to perform the functions of receiver input bandpass filtering, transmitter output low-pass filtering, and compromise equalization.

COMPROMISE EQUALIZATION DISABLED

The following tables illustrate the response of the receiver input bandpass and transmitter output low pass filters without compromise equalization.

A. Receiver Input Bandpass Filter

Parameter	Value
Test signal range	0 dBm to –45 dBm
Passband	400 Hz – 3000 Hz
Passband ripple	0.5 dB max.
Loss below 60 Hz	40 dB min.
Loss above 6000 Hz	40 dB min.
Passband gain	0.0 dB ±1.0
Delay distortion	
400 Hz – 1800 Hz	Less than 1000 μs
Delay distortion	
1800 Hz – 3000 Hz	Less than 150 μs

B. Transmitter Output Lowpass Filter

Parameter	Value
Test signal range	0 dBm to –16 dBm
Passband	400 Hz– 3000 Hz
Passband gain	–1 dB ±1 dB
Passband ripple	0.5 dB max.
Loss at 3600 Hz	5.5 dB min.
Loss at 7800 Hz	32 dB min.
Loss at 11400 Hz	33.5 dB min.
Loss at 12000 Hz	41 dB min.
Loss above 17400 Hz	45 dB min.
Delay distortion	
400 Hz – 3000 Hz	Less than 300 μs

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COMPROMISE EQUALIZER ENABLED

The following tables illustrate the change in filter response caused by enabling each of the compromise equalizers independently.

A. Receiver

1. Link Amplitude Equalizer (RLE, J3L)

Frequency (Hz)	Gain dB Relative to 1700 Hz	
	US Long	Japanese 3 Link
1000	–0.27	–0.13
1400	–0.16	–0.08
2000	+0.33	+0.16
2400	+1.54	+0.73
2800	+5.98	+2.61
3000	+8.65	+3.43

2. Cable Amplitude (CABS2, CABS1)

a. CODE 1

Frequency (Hz)	Gain dB Relative to 1700 Hz
700	–0.99
1500	–0.20
2000	+0.15
3000	+1.43

b. CODE 2

Frequency (Hz)	Gain dB Relative to 1700 Hz
700	–2.39
1500	–0.65
2000	+0.87
3000	+3.06

c. CODE 3

Frequency (Hz)	Gain dB Relative to 1700 Hz
700	–3.93
1500	–1.22
2000	+1.90
3000	+4.58

B. Transmitter

1. Link Amplitude Equalizer (TLE, J3L)

Frequency (Hz)	Gain dB Relative to 1700 Hz	
	US Long	Japanese 3 Link
1000	–0.27	–0.13
1400	–0.16	–0.08
2000	+ 0.33	+0.16
2400	+ 1.54	+0.73
2800	+ 5.98	+2.61
3000	+ 8.65	+3.43

2. Cable Amplitude (CABS2, CABS1)

a. CODE 1

Frequency (Hz)	Gain dB Relative to 1700 Hz
700	–0.99
1500	–0.20
2000	+0.15
3000	+1.43

b. CODE 2

Frequency (Hz)	Gain dB Relative to 1700 Hz
700	–2.39
1500	–0.65
2000	+0.87
3000	+3.06

c. CODE 3

Frequency (Hz)	Gain dB Relative to 1700 Hz
700	–3.93
1500	–1.22
2000	+1.90
3000	+4.58

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Digital Network Products

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Rockwell

R8040
T-1 TRI-PORT MEMORY

OVERVIEW

The Tri-Port Memory circuit is designed to function as an assembly point and temporary storage area for 8-bit T-1 data. It provides 64 8-bit locations of on-chip random access memory which can be accessed via external addresses or internal sequential addressing.

FEATURES

- 64 x 8 bit static memory
- Single +5V supply
- Two totally independent read ports
- Multiple Read access time < 430 ns (worst case)
- Selectable random- or sequential-address Write operation
- On-chip sequential address counter
- Tri-state drivers, for chip-selectable bus operation
- 40-pin plastic dual in-line package
- LSTTL Schottky-compatible (12KΩ pullup, to drive CMOS)

APPLICATIONS

Time-Division Multiplex (TDM) digital switching data and control stores

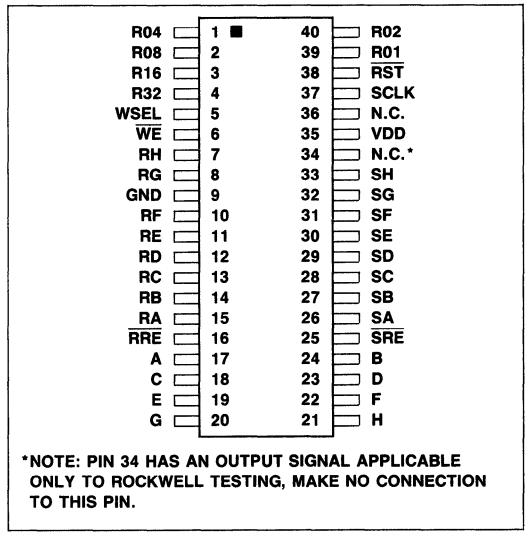
- TDM sequential machines
- Elastic stores
- Hardware/Software control interfaces
- I/O Buffers

TRI-PORT MEMORY OPERATION

The Tri-Port Memory device accepts 8-bit parallel input data on lines A through H. This data is stored in an internal memory location that is selected by either random address lines R01 through R32 or by the device's Sequential Address Counter. Write Select signal WSEL determines the source of the address; in the logic 0 state, WSEL selects the random address, in the logic 1 state, WSEL selects the internal sequential address.

The state of Write Enable signal $\overline{WE}$ determines whether or not the data on lines A through H will be written into memory. Data will only be written into memory when $\overline{WE}$ goes low (to a logic 0 state) and the address inputs have stabilized.

The on-chip, six-bit Sequential Address Counter is a binary counter that increments on each positive transition of Sequential Clock (SCLK). When the Counter attains binary 111111, the next positive transition on SCLK will clear it to binary 000000. The Counter will also be cleared unconditionally if Reset signal $\overline{RST}$ has been set to logic 0 when the positive transition of SCLK occurs.



*NOTE: PIN 34 HAS AN OUTPUT SIGNAL APPLICABLE ONLY TO ROCKWELL TESTING, MAKE NO CONNECTION TO THIS PIN.

Pin Configuration

The Sequential Read Enable signal, $\overline{SRE}$, enables sequentially-addressed read operations. If $\overline{SRE}$ is logic 0, the sequential accessed data outputs (SA through SH) will become valid within 430 ns after the next positive transition on SCLK. If $\overline{SRE}$ is logic 1, and 350 ns have elapsed since the positive transition of SCLK, the sequential accessed data outputs will become valid 80 ns after the negative transition of $\overline{SRE}$. The sequential read data will cease to be valid 100 ns after the negative transition of $\overline{SRE}$ or 20 ns after the next positive transition of SCLK, becoming valid with the content of the next sequential location within 430 ns of that SCLK transition.

The Random Read Enable signal, $\overline{RRE}$, enables random-accessed read operations. If $\overline{RRE}$ is logic 0, the random accessed data outputs (RA through RH) will become valid within 380 ns after the random address lines have stabilized. If $\overline{RRE}$ is logic 1, and 300 ns have elapsed since the random address lines have stabilized, the random accessed data outputs will

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become valid 80 ns after the negative transition of $\overline{RRE}$. The random accessed data outputs will cease to be valid 100 ns after a positive transition of $\overline{RRE}$ or 20 ns after the random address input lines change, becoming valid with the contents of the newly-addressed location within 380 ns after the random address inputs have stabilized.

In the case of a same location read/write cycle, the sequential and/or random data outputs will cease to be valid after a negative transition of $\overline{WE}$, and will become valid with the newly-written contents within 340 ns of that transition. Control of this parameter minimizes external circuitry required for resolution of read-write contention.

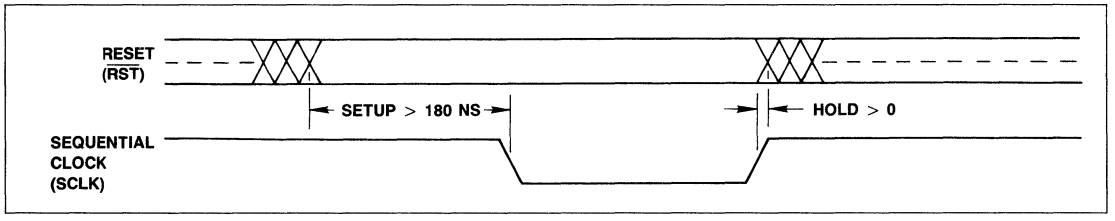
RECOMMENDED OPERATING CONDITIONS

Minimum Setup/Hold Times

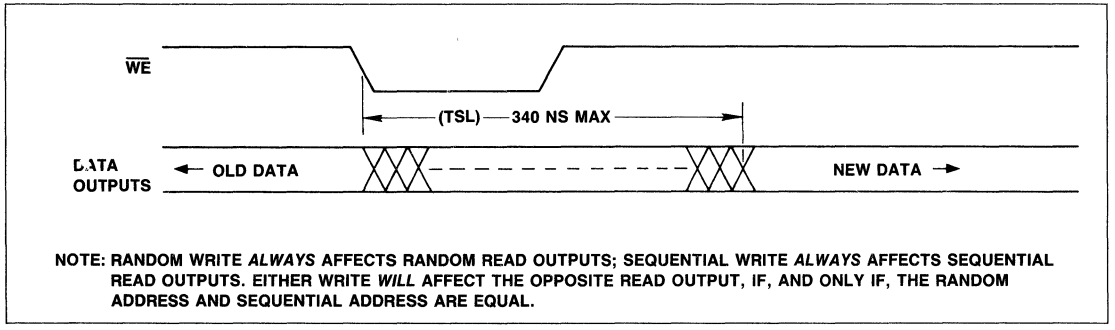
Signal	Setup		Hold	
	Measure to	ns	Measure to	ns
SCLK ↑	$\overline{WE}$ ↓	300	$\overline{WE}$ ↑	0
WSEL	$\overline{WE}$ ↓	280	$\overline{WE}$ ↑	0
R01-R32	$\overline{WE}$ ↓	250	$\overline{WE}$ ↑	0
A-H	$\overline{WE}$ ↑	150	$\overline{WE}$ ↑	100
$\overline{RST}$	SCLK ↓	180	SCLK ↑	0

Minimum Pulse Widths

Signal	Minimum Pulse Width
$\overline{WE}$ (= 0)	170 ns
SCLK	220 ns

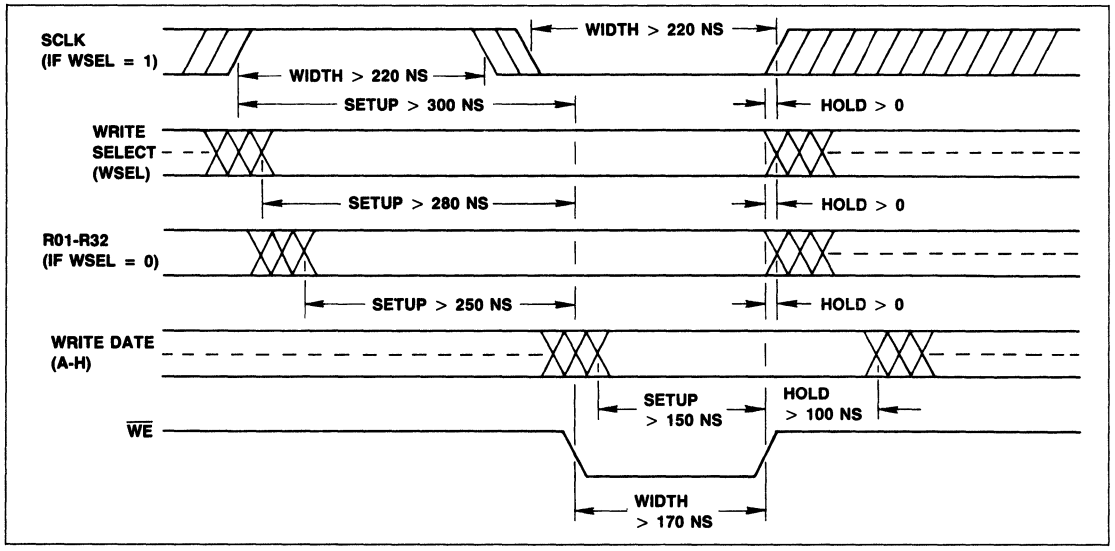


Sequential Counter Reset Setup and Hold Timing

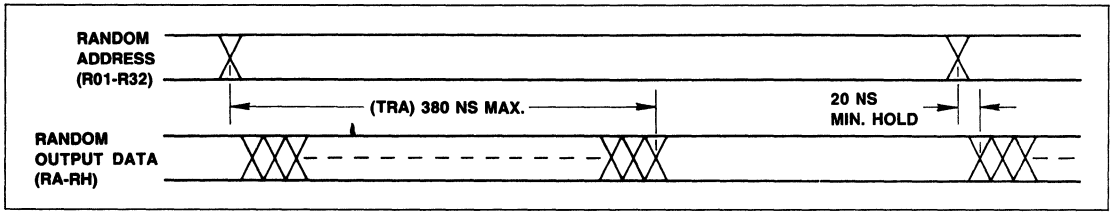


NOTE: RANDOM WRITE *ALWAYS* AFFECTS RANDOM READ OUTPUTS; SEQUENTIAL WRITE *ALWAYS* AFFECTS SEQUENTIAL READ OUTPUTS. EITHER WRITE *WILL* AFFECT THE OPPOSITE READ OUTPUT, IF, AND ONLY IF, THE RANDOM ADDRESS AND SEQUENTIAL ADDRESS ARE EQUAL.

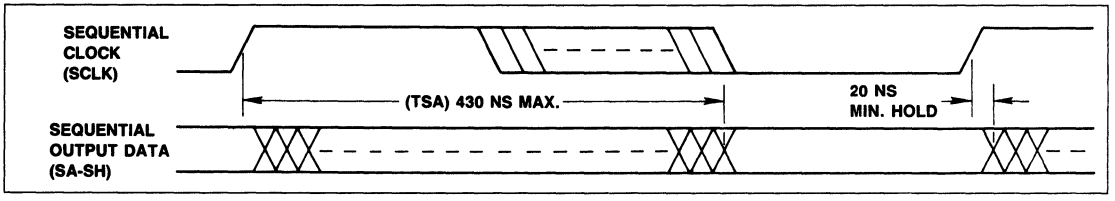
Read Outputs at Same Location as Write (All Other Inputs Stable)



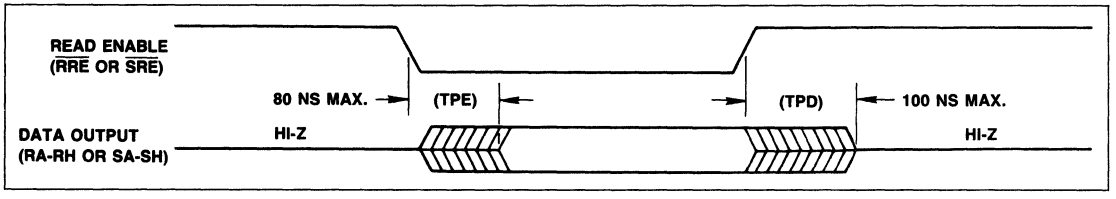
Write Setup and Hold Timing



Random Read ($\overline{RRE}$ = 0, $\overline{WE}$ = 1)



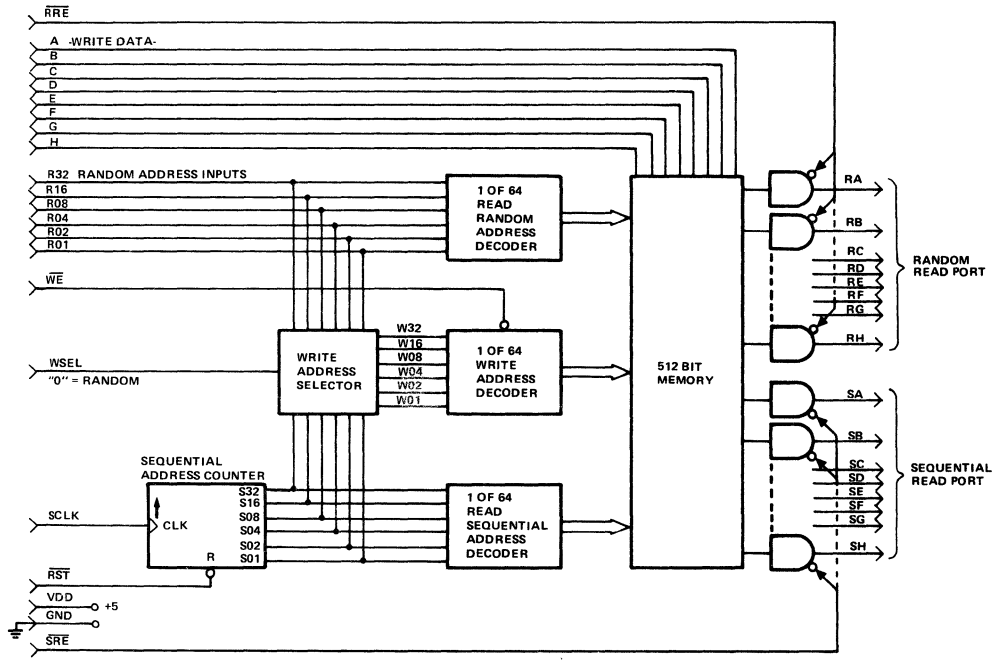
Sequential Read ($\overline{SRE}$ = 0, $\overline{WE}$ = 1)



Read Port Enable/Disable (Address Stable, $\overline{WE}$ = 1)

Propagation Delays

Parameter	Symbol	Min	Max	Unit
Random Read Access Time	t_{RA}	0	380	ns
Sequential Read Access Time	t_{SA}	0	430	ns
Read Port Disable (to HI-Z)	t_{PD}	0	100	ns
Read Port Enable	t_{PE}	0	80	ns
Same-Location Read After Write	t_{SL}	0	340	ns



Tri-Port Memory Block Diagram

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

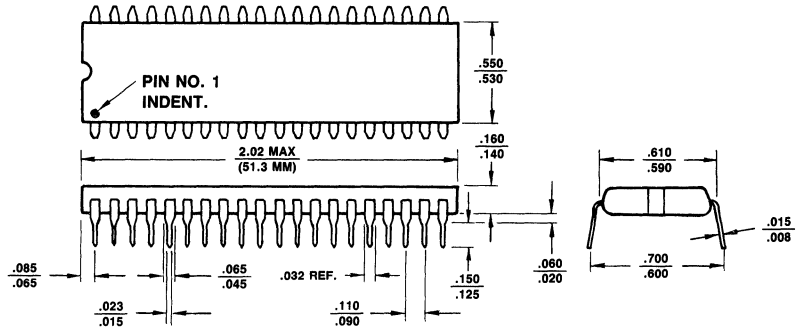
***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = 0V T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0		V
Input Logic "0" Voltage	V_{IL}		0.8	V
Input Logic "1" Voltage	V_{OL}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	−100		μA
Output Sink Current	I_{OL}	400		μA
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation (at 25°C)	P_{DSS}		300	mW

PACKAGE DIMENSIONS



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

Rockwell

R8050
T-1 SERIAL TRANSMITTER

DESCRIPTION

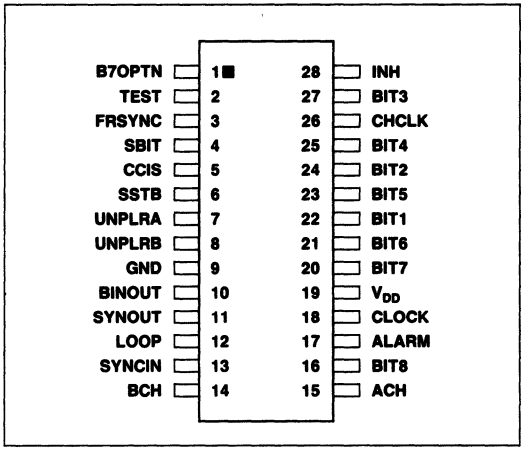
The Rockwell T-1 Serial Transmitter formats data to be serially transmitted according to T-1 D2 or T-1 D3 specifications, inserting framing and signalling bits along with 24 channels of 8-bit channel data. The T-1 Serial Transmitter also provides for alarm reporting via the Bit 2 inhibit method or, with minimal external logic, via the multiframe alignment signal (F_S) modification method.

Figure 1 is a functional block diagram of the T-1 Serial Transmitter. The Mod 193 counter is driven by the clock at 1.544 MHz and is either synchronized to the driving system by input signal SYNCIN or provides synchronization via output signal SYNOUT. Input signal FRSYNC applies synchronization to a Mod 12 counter, which identifies the frame of the 12-frame multiframe being processed.

The input data register latches data during each bit period, when the 8th bit of a channel sample is being transmitted. The data selector outputs the proper sequence of bits, as controlled by a bit count and frame count.

The zero channel monitor function causes Bit 8 or Bit 7 to be transmitted as a "one" if the channel data sample is all "zeros." Input INH provides a means to inhibit the zero channel monitor function. Input B7OPTN controls the particulars of the insertion method.

Two types of transmit formats are provided, a binary output and a paired unipolar output. The unipolar pair provides a means to externally create a single bipolar output with minimal logic.



Pin Configuration

FEATURES

- Single 5V supply, low power Schottky TTL compatible.
- Accepts 8 bits of parallel data as input.
- Generates output as 193 bit serial data stream in T-1, D2, D3 or D4 Mode 3 data format.
- Provides a channel and frame timing signal.
- Provides alternate control for alarm reporting and signalling.
- Provides automatic bit insertion for all-zero channel samples.

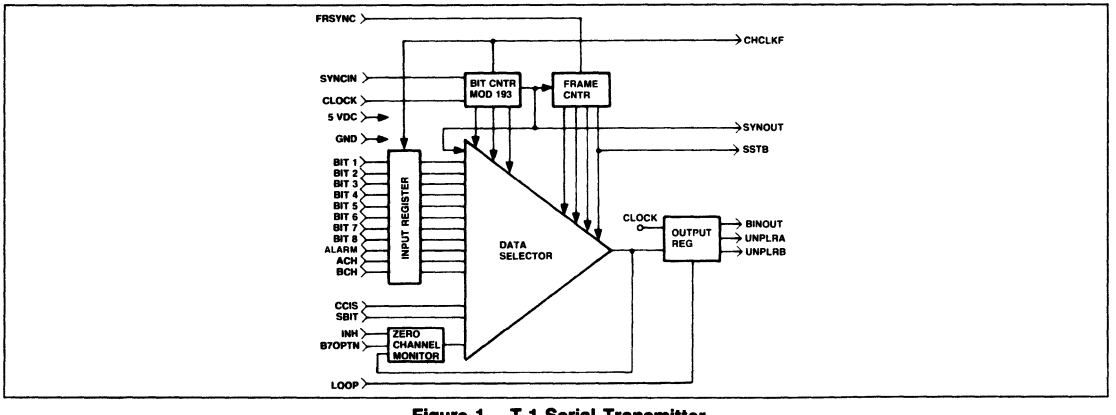


Figure 1. T-1 Serial Transmitter

T-1 TRANSMITTER INPUTS

Any input ≤0.8V = logic 0, low. Any input ≥2.0V = logic 1, high. The transition from a low level to a high level is called a rising edge, while the converse is defined as a falling edge.

FRSYNC: FRAME SYNCHRONIZATION

Frame sync allows external synchronization of the transmitter's internal frame counter. When FRSYNC becomes high, the frame counter is directly set to frame 1, the first of the twelve frames. If FRYSYNC is held high and does not return to zero before a rising edge of CLOCK, the subsequent states of BINOUT, UNPLRA and UNPLRB are high, high and low, respectively, regardless of the states of any other inputs. The latter mechanism is useful for device and/or board testing only and will cause bit errors and/or bipolar violations if used during field operations. See Figures 6 and 7.

SYNCIN: SYNCHRONIZATION INPUT

SYNCIN allows external synchronization of the internal Modulo 193 bit/channel counter. When SYNCIN becomes high, the Modulo 193 counter is directly set to the state corresponding to the output of the framing (F_T or F_S) bit. The first bit of channel one will be output on BINOUT (and UNPLRA or UNPLRB) as a result of the first rising edge of CLOCK following the return of SYNCIN to logic 0. See Figures 5 and 7.

TEST: ROCKWELL DEVICE TEST INPUT

Used only for Rockwell device testing. **Keep this input grounded.**

CLOCK: T-1 CLOCK

Maximum frequency = 1.6 MHz
Minimum pulse width = 275 ns
The T-1 bit period is bounded by the rising edges of this input.

INH: INHIBIT ZERO CHANNEL MONITOR

If INH is high, the zero channel monitor function is disabled, and Bits 7 and 8 are transmitted per corresponding inputs received. See Table 1.

For channels in signalling frames (6 or 12) in which the first six data bits and the signalling highway are all "zero," BIT 7 will be forced to one if INH is low. For any frame except a signalling frame Bit 8 or Bit 7 as selected by B7OPTN will be transmitted as a "one" if the channel input data is "zero" and INH is low.

BITS 1-8: PARALLEL CHANNEL DATA INPUTS

Bit 1, the sign bit, will be serially transmitted first, followed by Bits 2 through 8. The falling edge of CHCLKF indicates input channel data has been clocked into the input register and always occurs during the transmission of the final bit (Bit 8) of each channel data sample.

ACH: "A" CHANNEL HIGHWAY SIGNALLING

ACH allows the user to transmit one bit of signalling per channel as Bit 8 of each channel data sample in Frame 6 only. ACH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

BCH: "B" CHANNEL HIGHWAY SIGNALLING

BCH allows the user to transmit one bit of signalling per channel as Bit 8 of each channel data sample in Frame 12 only. BCH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

S-BIT: MULTIFRAME SIGNALLING BIT

SBIT, in conjunction with CCIS, provides an alternate way to control the multiframe signalling bit (F_S) transmission. The S-Bit input is transmitted as the multiframe signalling bit (F_S) if CCIS is held high. Refer to Table 2.

ALARM: LOCAL ALARM

Used for reporting alarm conditions. If the ALARM signal is high, Bit 2 (the most-significant bit) of every channel data sample of every frame is transmitting as a zero. This is commonly called remote alarm signalling. ALARM is clocked into the input register at the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

LOOP: LOOP STRAP

Provided to aid testing of user applications. When enabled to a high level, LOOP forces the unipolar outputs to transmit alternating ones and zeros, regardless of input conditions, while BINOUT continues to provide normal data outputs. Refer to Figure 3.

CCIS: COMMON CHANNEL INTEROFFICE SIGNALLING STRAP

Provides optional control for replacing the automatic F_S pattern with a 4-kilobit common channel signalling path. When CCIS is high, the SBIT input replaces the F_S pattern and the insertion of ACH and BCH is suspended. The CCIS input may also be used to provide the alternate method of alarm reporting. See Figure 4.

B7OPTN: BIT 7 OPTION

Provides Bit 7 as an alternate bit position for "one" stuffing, as programmed by the zero channel monitor function. Refer to Table 1.

VSS, VDD: GROUND AND POWER

V_{DD} = +5 ±0.25 Vdc
V_{SS} = Ground, 0 Vdc

T-1 TRANSMITTER OUTPUTS

Low power TTL Schottky compatible. "1" ≥ 2.4 Vdc, "0" ≤ 0.4 Vdc, CMOS — 12KΩ pullup to V_{DD} required.

SSTB: 4 kHz SIGNALLING CHANNEL STROBE

SSTB is the least-significant bit of the frame counter. Unless it is directly set by FRSYNC, SSTB will go high as each framing bit (F_T) is serially transmitted, and will return low as each multiframe alignment signal (F_S) is transmitted. Refer to Figure 2.

SYNOUT: CHANNEL SYNC OUTPUT

SYNOUT provides a means to synchronize to the internal bit counter (Mod 193). SYNOUT is high for one bit time, beginning just prior to the first data bit of a frame being serially transmitted. Refer to Figure 7. SYNOUT is the only output determined by the falling edge of CLOCK.

CHCLKF: CHANNEL CLOCK FALSE

The falling edge of CHCLKF, occurring as Bit 8 of any channel is being serially transmitted, indicates input data has been clocked into the input register. With the exception of an extra bit period extending the low level duration at frame bit time, CHCLKF is a divide-by-eight of CLOCK. Refer to Figure 2.

BINOUT: SERIAL DATA OUTPUT, BINARY FORMATTED

BINOUT is the binary formatted serial conversion of the parallel input data. The programmed format of BINOUT follows Tables 1 and 2.

BINOUT is synchronously transmitted as a high level if FRSYNC remains high during the rising edge of CLOCK. Refer to Figures 6 and 7.

UNPLRA, UNPLRB: T-1 SERIAL DATA UNIPOLAR OUTPUTS

Two paired unipolar outputs are provided for the purpose of creating a single serial data output transmission in bipolar format. The unipolar output register toggles for each "one" bit to be serially transmitted. UNPLRA and UNPLRB are transmitted as complements for "one" data bits and as low levels for "zero" data bits. See Figure 3.

The input signal LOOP, if high, forces the unipolar outputs to toggle every bit time, regardless of input data.

FRSYNC perturbs the current bits being transmitted by UNPLRA and UNPLRB. If FRSYNC remains high during the rising edge of CLOCK, UNPLRA will be transmitted as a high level and UNPLRB will be low. Refer to Figures 6 and 7.

Table 1. Serial Channel Sample Output Data Truth Table

Inputs X = don't care													Current Frame Number	Binout Serial Output Channel Bit Position								Notes
ALARM	INH	B7OPTN	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	ACH	BCH		1	2	3	4	5	6	7	8	
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
0	X	X	P	Q	R	S	T	U	V	X	A	X	6	P	Q	R	S	T	U	V	A	2
0	X	X	P	Q	R	S	T	U	V	X	X	B	12	P	Q	R	S	T	U	V	B	2
0	X	X	P	Q	R	S	T	U	V	W	X	X	Y	P	Q	R	S	T	U	V	W	2,3
0	1	X	0	0	0	0	0	0	0	X	A	X	6	0	0	0	0	0	0	0	A	
0	1	X	0	0	0	0	0	0	0	X	X	B	12	0	0	0	0	0	0	0	B	
0	1	X	0	0	0	0	0	0	0	W	X	X	Y	0	0	0	0	0	0	0	W	3
0	0	X	0	0	0	0	0	0	0	X	0	X	6	0	0	0	0	0	0	1	0	
0	0	X	0	0	0	0	0	0	0	X	X	0	12	0	0	0	0	0	0	1	0	
0	0	1	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	0	1	3

NOTES (1) ALARM = 1 has the same effect as BIT 2 = 0
(2) P, Q, R, S, T, U and V may not simultaneously be zero, unles A, B or W is 1
(3) Y is any frame $\neq$ 6 and $\neq$ 12 with CCIS = 0, or all frames with CCIS = 1

Table 2. Framing Bit (F_T & F_S) Output Data

Frame Number	Processed Bit	Binout	
		CCIS = 0	CCIS = 1
1	F_T	1	1
2	F_S	0	SBIT
3	F_T	0	0
4	F_S	0	SBIT
5	F_T	1	1
6	F_S	1	SBIT
7	F_T	0	0
8	F_S	1	SBIT
9	F_T	1	1
10	F_S	1	SBIT
11	F_T	0	0
12	F_S	0 (NOTE 1)	SBIT

Notes: (1) Alternate remote alarm reporting may be accomplished by holding SBIT and CCIS both high just prior to initiation of Frame 12.
(2) F_T bit insertion is automatic and no optional control is provided.

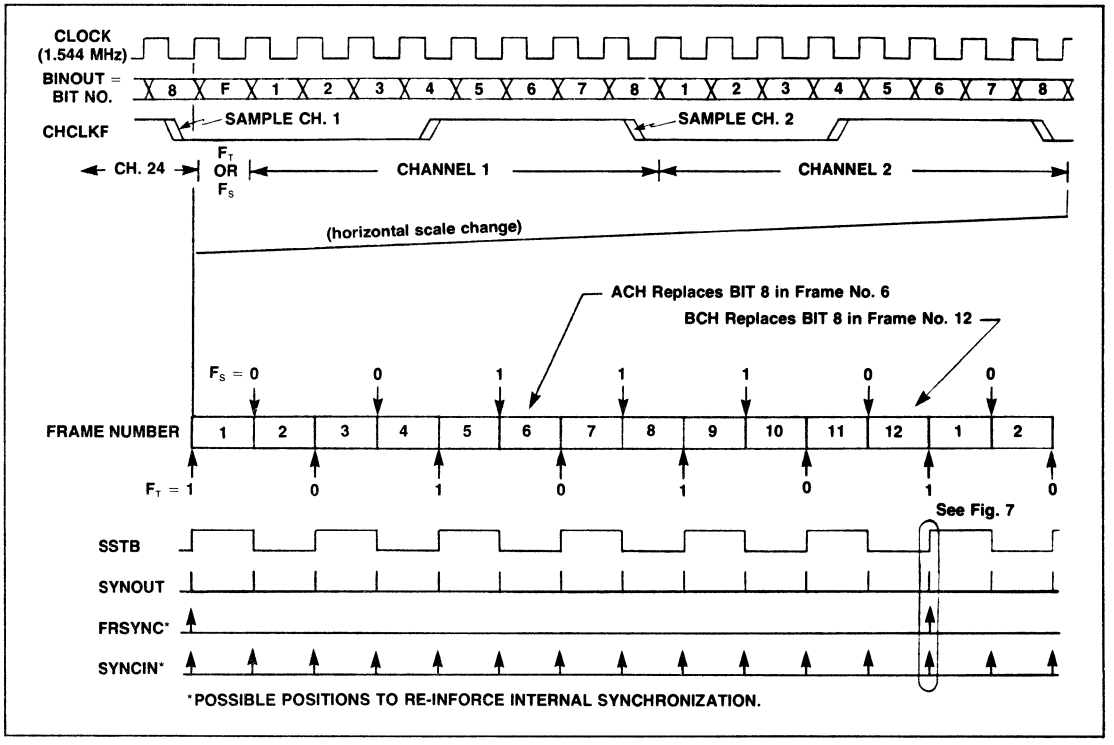


Figure 2. Transmitter Input-Output Signal Relationships

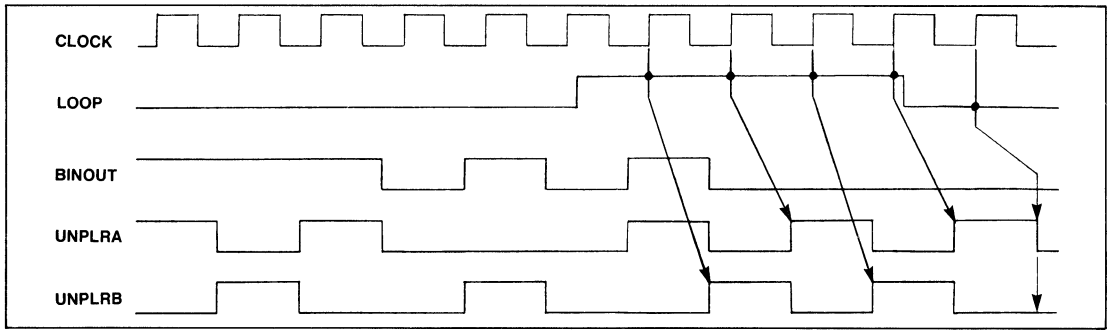


Figure 3. Transmitter Binary, Unipolar Outputs

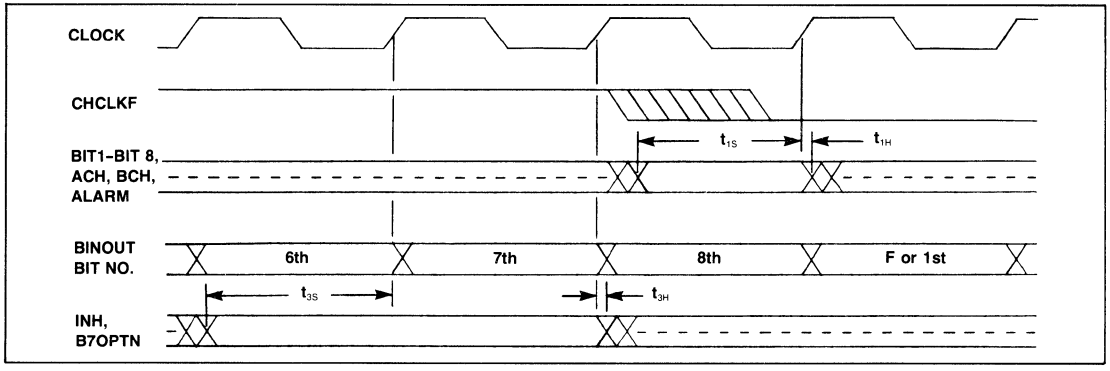


Figure 4 (a). Channel Input Timing

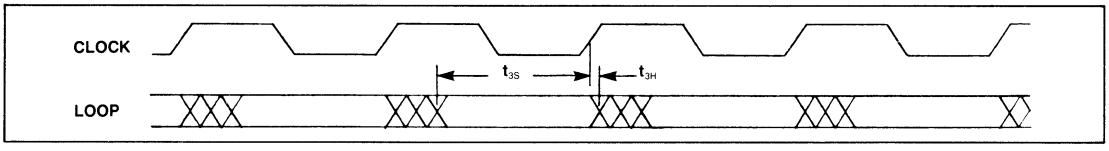
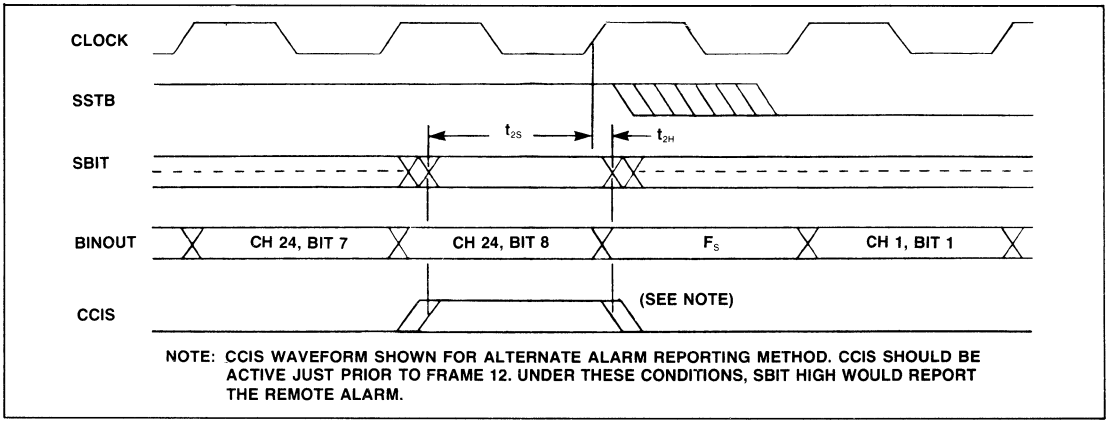


Figure 4 (b). LOOP Input Timing



NOTE: CCIS WAVEFORM SHOWN FOR ALTERNATE ALARM REPORTING METHOD. CCIS SHOULD BE ACTIVE JUST PRIOR TO FRAME 12. UNDER THESE CONDITIONS, SBIT HIGH WOULD REPORT THE REMOTE ALARM.

Figure 4 (c). Control Input Timing

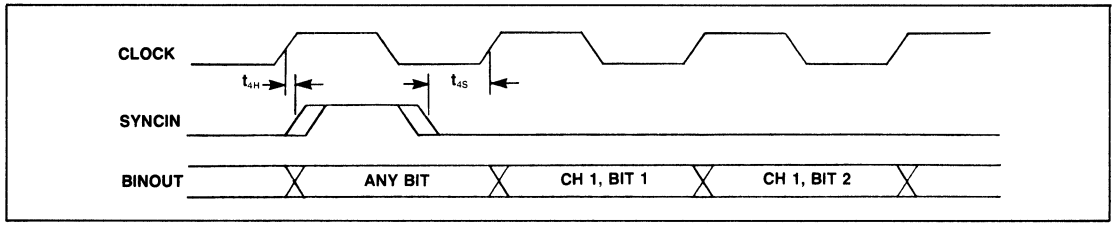


Figure 5. SYNCIN Timing Relationship

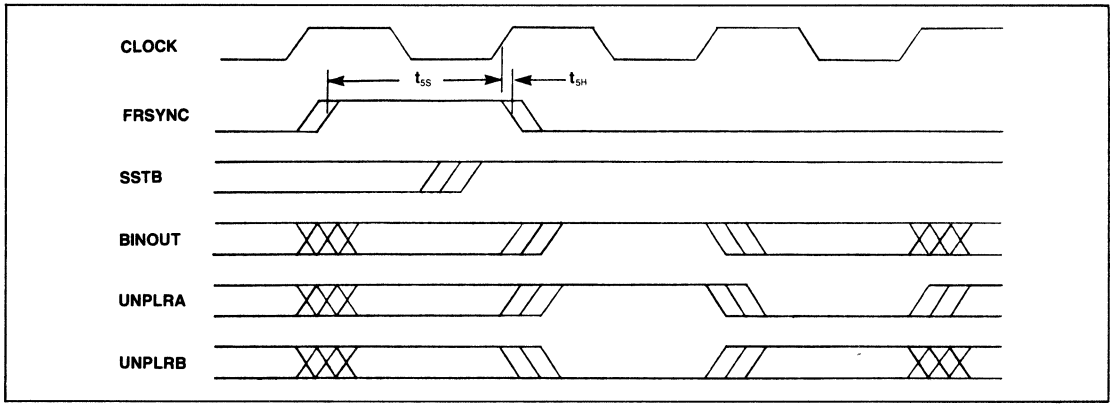


Figure 6. Non-return-to-zero FRSYNC Timing

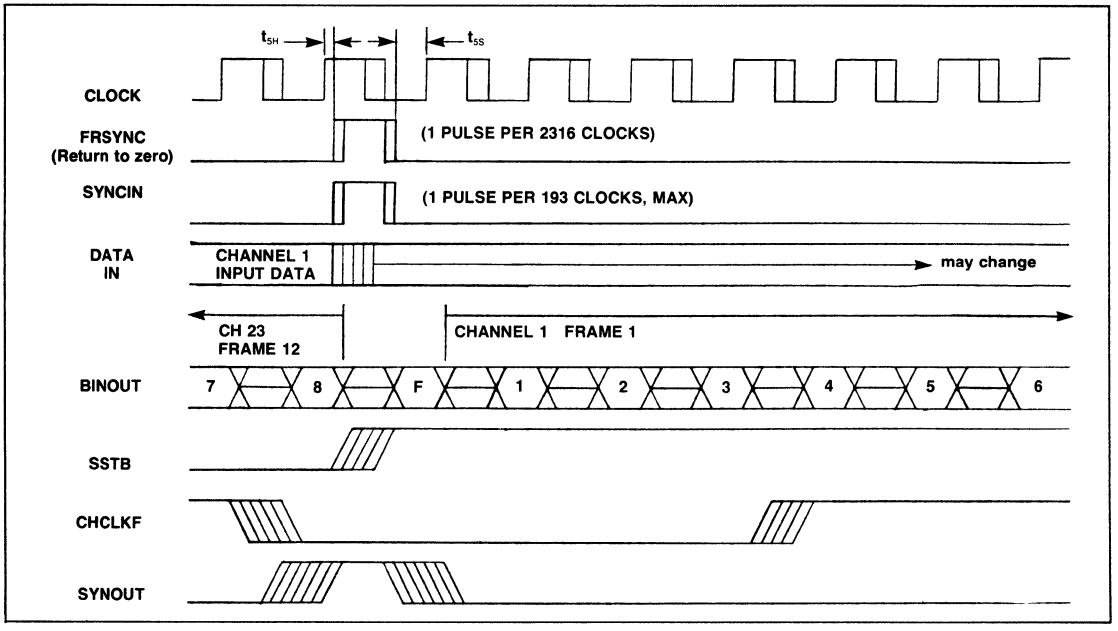


Figure 7. Transmitter External Synchronization (Return-to-zero FRSYNC)

Table 3. Input Timing

Symbol	Parameter	Min	Max	Unit
t_{1S}	Buffered Data Setup Time	450		ns
t_{1H}	Buffered Data Hold Time	0		ns
t_{2S}	Control Input Setup Time	400		ns
t_{2H}	Control Input Hold Time	20		ns
t_{3S}	Asynchronous Control Input Setup Time	350		ns
t_{3H}	Asynchronous Control Input Hold Time	20		ns
t_{4S}	SYNCIN Setup Time	200		ns
t_{4H}	SYNCIN Hold Time	20		ns
	SYNCIN Pulse Width	100		ns
t_{5S}	Frame Sync Setup Time (Return to Zero)	250		ns
t_{5H}	Frame Sync Hold Time (Return to Zero)	20		ns
	Frame Sync Pulse Width	200		ns
t_{5S}	Frame Sync Setup Time (Non-Return to Zero)	525		ns
t_{5H}	Frame Sync Hold Time (Non-Return to Zero)	20		ns

Table 4. Output Propagation Delay, Worst Case
(Measured from Rising Edge of Clock Unless Stated Otherwise)

Output	Max Delay	Unit
SSTB	500	ns
SYNOUT	500	ns
Ref from Falling Edge of Clock		
CHCLKF	500	ns
BINOUT	500	ns
UNPLRA	500	ns
UNPLRB	500	ns

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4 75 to +5.25	Vdc
Operating Temperature	T_{OP}	0 to 70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

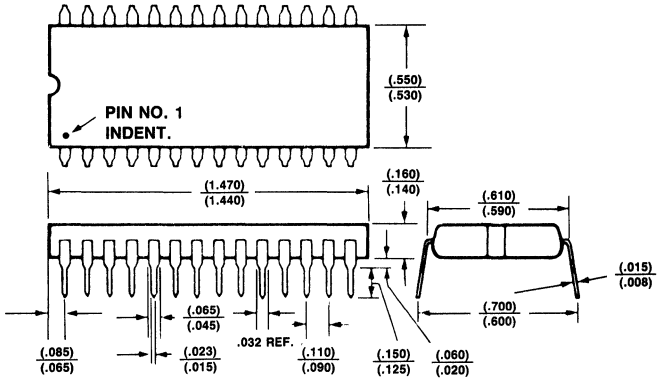
***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 ±5%)

Parameter	Symbol	Min	Max	Unit
Logical "1" Input Voltage	V_{OH}	2.0	V_{DD} + 0 3	V
Logicical "0" Input Voltage	V_{IL}	−0.3	0.8	V
Logicical "1" Output Voltage	V_{OH}	2.4	—	V
Logic "0" Output Voltage	V_{OL}	—	0 4	V
Output Source Current	I_{OH}	−100	—	μA
Output Sink Current	I_{OL}	400	—	μA
Capacitance Load (any output)	C	—	25	pF
Input Capacitance (any input)	C_{IN}	—	5	pF
Clock Frequency		—	1.6	MHz
Power Dissipation	P_D	—	250	mW

PACKAGE DIMENSIONS



R8060
T-1 SERIAL RECEIVER

DESCRIPTION

The Rockwell T-1 Receiver processes serial unipolar data of a T-1,D2 or T-1,D3 line from which data and a 1.544 MHz clock have been extracted

Frame synchronization is accomplished by locating the frame bit (F_T) alternating every 386 bits. Loss of frame sync is indicated if a frame bit error occurs within two to four F-Bit frames since the previous frame bit error

A loss of carrier is indicated if 31 consecutive bit times yield "zeros" at the input Carrier loss is reset and frame sync search begins when a "one" reappears at the TDATA input

Signaling bits, which occur 193 bit positions after a framing bit, are monitored to detect signaling frames. The signaling frame output, SIGFR, identifies the present frame as a signaling frame, and the S-Bit output at that time identifies which signaling frame is being processed.

Remote alarm reporting is detected by monitoring the second received bit of every channel sample of every frame. An alarm is indicated if 255 consecutive Bit 2 zeros are received.

Channel data bits are output by an eight-bit parallel register. The rising edge of the signal called channel clock (CHCLK) indicates the extraction of new output channel data.

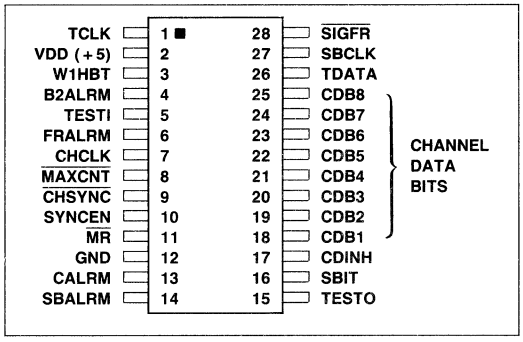
Several signals developed from a MOD 386 counter are provided to aid in the external processing and storage of channel data. Signals are provided to increment counters, synchronize counters, strobe data into memories, etc.

The Rockwell T-1 Receiver chip operates on a single 5 volt supply and directly interfaces to the low power TTL Schottky logic family. The Receiver is packaged in a 28 pin dual in-line (DIP).

Timing relationships are given in figures 3 through 5.

FEATURES

- Synchronizes serial T-1,D2 or T-1,D3 signals in less than 5 ms.
- Extracts 8-bit parallel channel data
- Provides timing signals to capture and synchronize channel and frame information
- Monitors and detects
  - — Errors in signaling bit pattern
  - — Loss of frame sync
  - — Loss of carrier
  - — Remote alarm reporting
- Single 5V supply
- LSTTL Schottky compatible



Pin Configuration

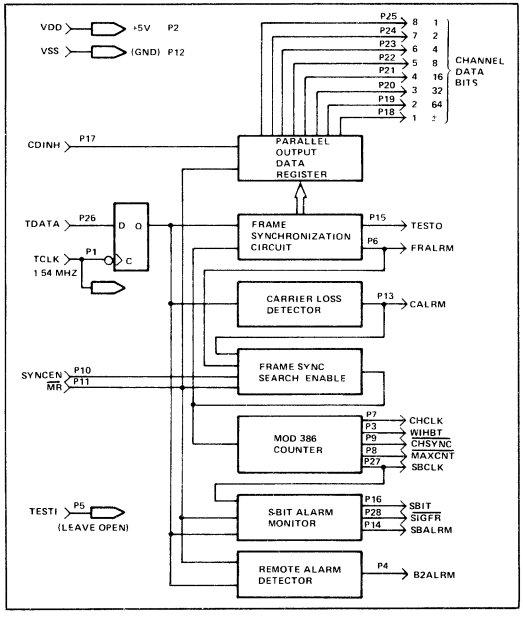


Figure 1. R8060 Block Diagram

T-1 RECEIVER INPUTS

Any input ≤0.8V = LOGIC 0, LOW, ZERO. Any input ≥2.0V = LOGIC 1, HIGH, ONE. A transition from a low level to a high level is called a rising edge, while the converse is true for the falling edge.

TDATA: UNIPOLAR T-1-D2, T-1-D3 SERIAL DATA INPUT

Unipolar T-1 Data is clocked in on the falling edge of TCLK. Thereafter, TDATA is processed on the rising edge of TCLK. TDATA must be stable 100 ns before and remain stable 100 ns after the falling edge of TCLK.

TCLK: T-1 CLOCK

Typical clock frequency is 1.544 MHz. Maximum clock frequency is 1.85 MHz. The T-1 bit period is bounded by the rising edges of TCLK. Input levels must be >2.4 volts for LOGIC 1 and ≤0.8 volts for LOGIC 0.

SYNCEN: FRAME SYNCHRONIZATION ENABLE

Provides a means to disable the automatic resync search initiated by a FRAME ALARM condition. If the SYNCEN signal is low, with synchronization function is inhibited and remains inhibited until SYNCEN transitions high. SYNCEN must be stable 200 ns before the rising edge of FRALRM, in order to inhibit the synchronization function.

MR: MASTER RESET

Master Reset, when low performs an initialization clear of the T-1 Receiver; SBALRM and CALRM are reset to low levels while FRALRM, CHCLK, WIHBT and CHSYNC are set to high levels. Frame synchronization search begins on the rising edge of MR provided that SYNCEN signal has been high for 200 ns. Minimum pulse width is one T-1 clock period.

CDINH: CHANNEL DATA INHIBIT

Provides a means to disable channel data bit outputs. When at a high level, CDINH forces channel data Bits 1 through 7 high. Bit 8, the least significant channel data bit, is not controlled by CDINH.

TESTI: ROCKWELL DEVICE TEST INPUT

Used only for Rockwell device testing, no connection to TESTI is required for normal operation.

VSS, VDD: GROUND AND POWER

VDD = +5.0 ±0.25 VDC
VSS = Ground, 0 VDC

T-1 RECEIVER OUTPUTS

Low Power TTL Schottky — compatible
"1" ≥ 2.4 Vdc; "0" ≤ 0.4 Vdc
CMOS — 12 K Ω pullup to VDD required.

CDB (1-8): CHANNEL DATA BIT 1 THROUGH 8

Bit 1 is the sign bit, Bit 2 is the most significant bit and Bit 8 is the least significant bit. If CDINH is low, new parallel channel data becomes valid within 200 ns after the rising edge of CHCLK and remains valid until the next rising edge of CHCLK. If CDINH is high, channel data Bits 1 through 7 are forced to a high level. Bit 8, the least significant bit, is not controlled by CDINH. Channel data Bits 1 through 7 are enabled or disabled within 300 ns (R8060) or 150 ns (R8060A) by CDINH. Refer to Figures 3 through 5.

CHCLK — CHANNEL CLOCK

The rising edge of CHCLK indicates a change of parallel output channel data. CHCLK is four TCLKS high then four TCLKS low except for when an "F" or "S" bit is received. Then CHCLK stretches to five TCLKS high and four TCLKS low. Refer to Figures 3 and 4.

$\overline{\text{CHSYNC}}$: CHANNEL SYNC

Channel Sync occurs one time in a 24 channel period, making it suitable for synchronizing external counters to the T-1 Frame rate. $\overline{\text{CHSYNC}}$ goes low one TCLK period before the falling edge of CHCLK at channel 24 date sample time. $\overline{\text{CHSYNC}}$ returns high 1 TCLK period after the next rising edge of CHCLK. Refer to Figures 3 through 5.

TESTO: ROCKWELL DEVICE TEST OUTPUT

Designed to aid in Rockwell device testing. No connection required for normal operation.

WIHBT: WRITE INHIBIT

WIHBT covers the parallel channel data transition period. WIHBT is suitable for clocking or strobing channel data into external memories. WIHBT is high for two TCLK periods, beginning one TCLK period before the rising edge of CHCLK. Refer to Figures 3 and 4.

$\overline{\text{MAXCNT}}$: MAXIMUM COUNT OF 386 MODULUS

$\overline{\text{MAXCNT}}$ is low for one TCLK period, marking the completion of a two-frame period corresponding to the expected receipt of an F-bit at the TDATA input. Refer to Figures 4 and 5.

SBCLK: S-BIT CLOCK

SBCLK will be high during the S-Bit frame and low during the F-bit frame. The transitions will occur within 300 ns after the rising edge of TCLK as channel 24 data is being transferred to the parallel channel outputs. Refer to Figures 3 through 5.

S-BIT: SIGNALING BIT OUTPUT

The S-Bit output will have the same digital level as the previous S-Bit received which occurred two frames before the receipt of the current S-Bit. An S-Bit output transition occurs one TCLK period after the rising edge of SBCLK.

During a signaling frame (SIGFR is low), frame 6 or "A" highway signaling is identified by S-Bit output being low If S-Bit is high during a signaling frame, frame 12 or "B" highway signaling is identified. Refer to Figures 3 through 5.

$\overline{\text{SIGFR}}$: SIGNALING FRAME

$\overline{\text{SIGFR}}$ identifies frame 6 or 12 when low. If the sequence of five consecutive received S-Bits is either 0111X or 1X001 (left to right, as received), $\overline{\text{SIGFR}}$ shall go low after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time. $\overline{\text{SIGFR}}$ returns high one frame later (193 bits). Refer to Figures 3 through 5.

SBALRM: S-BIT ALARM

SBALRM goes high if the sequence of the five S-Bits received contains four consecutive ones (01111), and remains high until three consecutive "zero" bits are preceded and followed by a "one" S-Bit (10001). The actual transition of SBALRM output occurs after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time.

B2ALRM: BIT 2 ALARM

B2ALRM goes high, detecting a remote alarm condition, if 255 consecutive channel data samples are received with Bit 2 low. B2ALRM returns low upon the receipt of any channel sample with Bit 2 high.

CALRM: CARRIER LOSS ALARM

A carrier loss is detected and CALRM is set high if 31 consecutive low level TDATA bits are received. CALRM is reset low, FRALRM is set high and frame sync search begins when the first TDATA high level is received.

FRALRM: FRAME ERROR ALARM

FRALRM detects an out-of-frame condition FRALRM goes high if:

A) The framing synchronization function is in progress.
B) Within 250 ns after the falling edge of MR.
C) An F-Bit is received which is not the inverse of the last F-Bit and the same condition also occurred two or three or four F-Bit frames earlier.
D) Within 250 ns after the falling edge of CALRM, (CALRM being reset by high level TDATA bit).

FRALRM goes low upon completion of the synchronization function or within 250 ns after the rising edge of CALRM. (Carrier loss condition during frame synchronization function).

OUTPUT CLOCK SIGNALS DURING FRAME SYNCHRONIZATION FUNCTION

Following the Declaration of Frame Sync loss (FRALRM goes high), output signals will continue normally for a two-frame period with the exception of CHSYNC, which has the above mentioned second frame sync pulse inhibited. Following the two-frame period CHCLK, CHSYNC, and WIHBT are held high until frame sync has been located, as indicated by the falling edge of FRALRM. With typical data patterns, frame synchronization takes less than five milliseconds. See Figure 2.

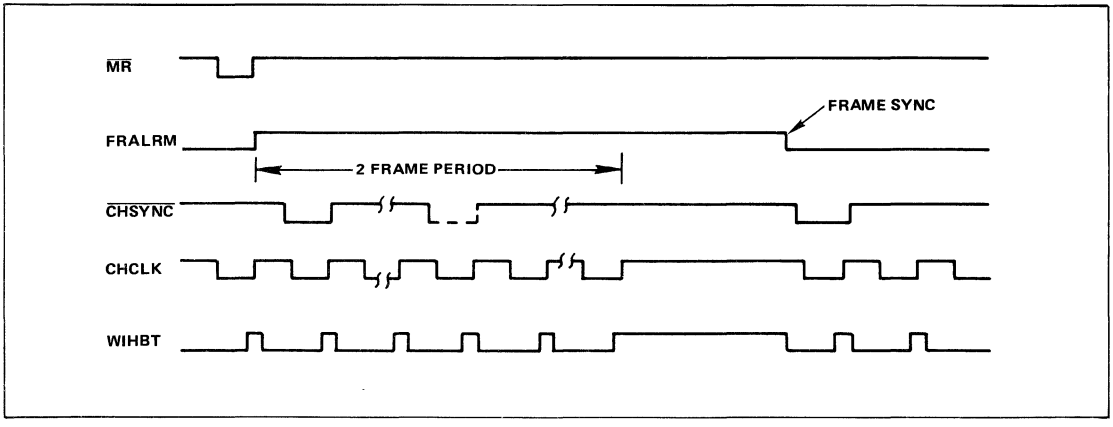


Figure 2. Signal Relationship During Frame Alarm and Search for Resynchronization

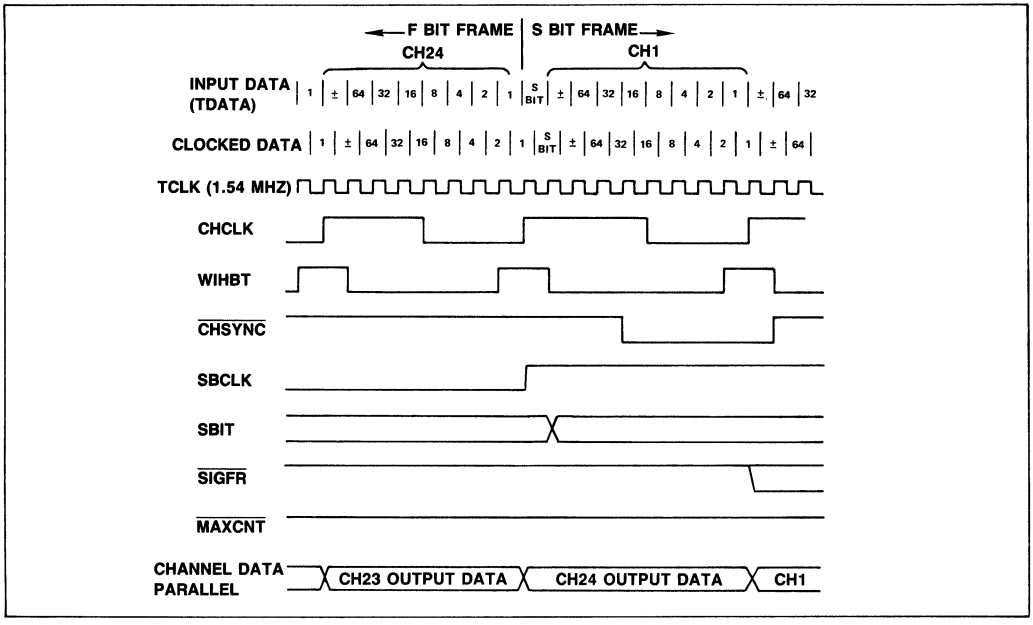


Figure 3. Signal Relationships at Beginning of F_S Frame (S-BIT)

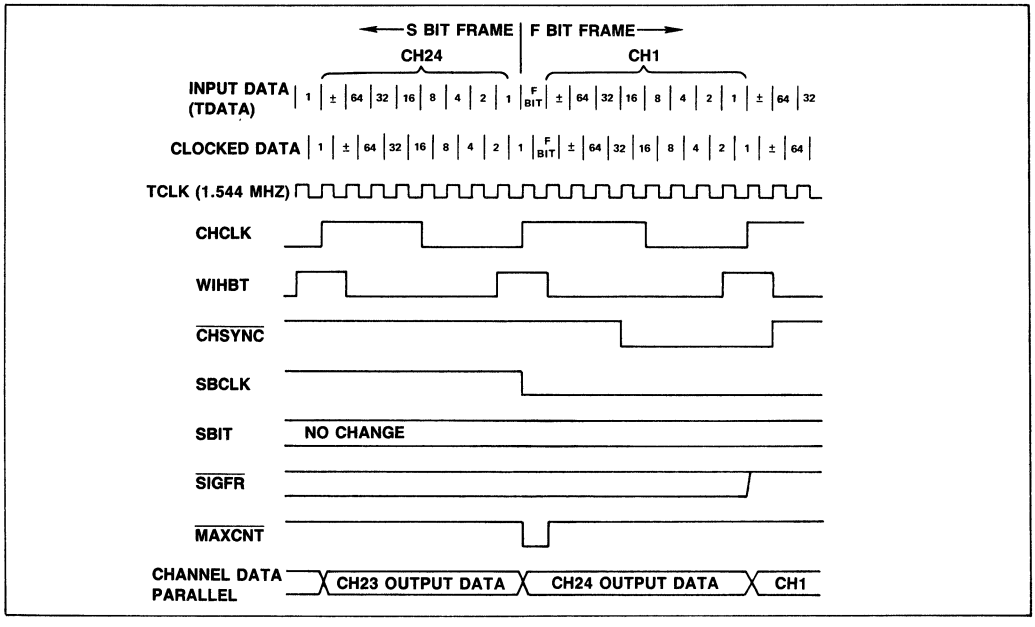
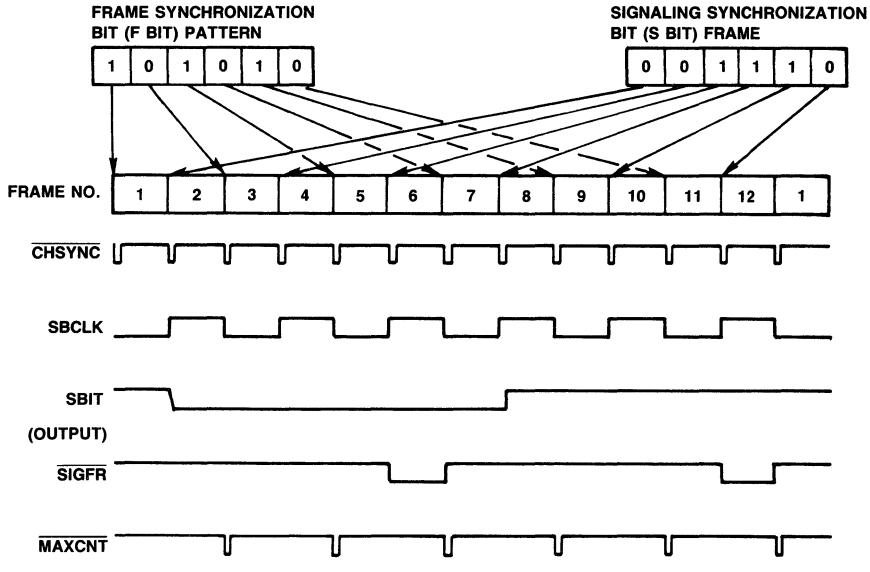


Figure 4. Signal Relationship at Beginning of F_T Frame (F-BIT)



FRAME = 24 TIME SLOTS = 193 BITS = 125 μS
TIME SLOT = 5.18 μS ONE BIT = 648 NS
MULTIFRAME = 12 FRAMES = 1.5 MS.

F BIT (F_T) ALIGNMENT SIGNAL
(ODD-NUMBERED FRAMES)

FRAME	FIRST BIT
1	1
3	0
5	1
7	0
9	1
11	0

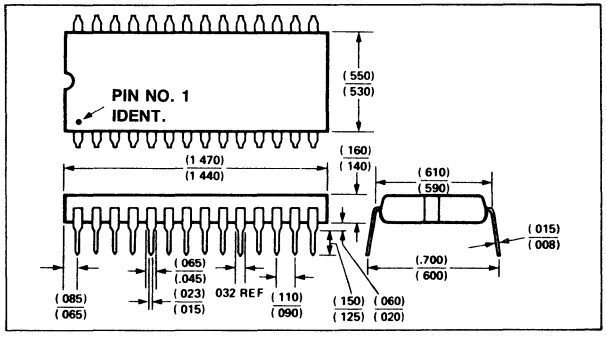
S BIT (F_S) MULTIFRAME ALIGNMENT SIGNAL
(EVEN-NUMBERED FRAMES)

FRAME	FIRST BIT
2	0
4	0
6	1
8	1
10	1
12	0

Figure 5. Multiframe Signal Relationships

Table 1. Output Propagation Delay Worst Case, From Rising Edge of TCLK

OUTPUT	MAX DELAY (NS)
CHCLK	300
$\overline{\text{CHSYNC}}$	300
WIHBT	300
$\overline{\text{MAXCNT}}$	300
SBCLK	400
SBIT	400
$\overline{\text{SIGFR}}$	475
SBALRM	475
B2ALRM	450
CALRM	300
FRALRM	900
CDB (1–8)	400



Packaging Diagram

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Logic "0" Voltage	V_{IL}	−0 3	0.8	V
Output Logic "1" Voltage	V_{OH}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	−100		μA
Output Sink Current	I_{OL}	400		μA
Clock Frequency	T_{CLK}		1 85	MHz
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation	P_{DSS}		550	mW

Rockwell

R8069
Line Interface Unit (LIU)

INTRODUCTION

The Rockwell R8069 Line Interface Unit (LIU) is a single chip CMOS device that interfaces the Rockwell R8070 T1/CEPT PCM Transceiver to the physical T-1/CEPT PCM30 transmission medium.

The R8069 LIU device contains analog and digital circuits which are based on CMOS technology to implement the line interface function required in ISDN primary rate transmission. The R8069 provides capabilities for 4-wire transmission of image, voice, or data signals; clock extraction; line equalization; bipolar violation detection; jitter accommodation; and AIS (Blue Alarm) generation and detection. In addition, the device operates at 1.544 or 2.048 Mbit/s and meets pulse shape and jitter specifications which are in accordance with T-1 and PCM30 standards.

The R8069 is ideally suited for image, voice, or data transmission required in ISDN primary rate applications. The device is highly integrated and requires virtually no external components.

Internal LIU functions allow system designers to minimize their development cost and easily implement a T-1/PCM30 physical interface to primary rate lines without concern about most of the complex details normally associated with such a design. The R8069 also provides a high level of integration which increases system reliability, reduces space and achieves higher levels of performance and quality.

FEATURES

- Compatible with T-1 and PCM30 (1.544 Mbit/s and 2.048 Mbit/s)
- Selectable T-1 and PCM30 clock rates
- Implements ISDN primary rate interface
- Directly compatible with Rockwell R8070 T-1/CEPT PCM Transceiver and R8071 ISDN/DMI Link Layer Controller devices
- Independent transmit and receive sections
- Phase locked loop for loop timing applications
- Satisfies T-1 (AT&T Technical Advisory No. 34) and PCM30 (CCITT G.703)
- Provides line equalization for up to 655 feet of 22-gauge plastic insulated (ABAM) cable for T-1 applications
- Transmission/reception of data for up to 1600 feet of cable
- Accomodates pulse shape requirements for 75 Ω and 120 Ω lines in PCM30 application
- Meets or surpasses jitter requirements specified by T-1 (AT&T Publication 62411, October 1985) and PCM30 (CCITT G.823)
- Intrinsic jitter under 0.05 UI
- Jitter attenuation starts at 2 Hz
- Jitter tolerance above 0.4 UI for jitter frequency up to 100 kHz
- 32-bit elastic store for jitter control and attenuation
- Elastic store bypass provisions
- Master/slave timing option
- Local and remote loop operation
- AIS (Blue Alarm) generation and detection
- On-chip line drivers
- Bipolar violation detector
- Analog CMOS technology
- Operates from a single +5V supply
- 28-pin plastic dual in-line package (DIP)
- TTL/CMOS I/O compatible

ORDERING INFORMATION

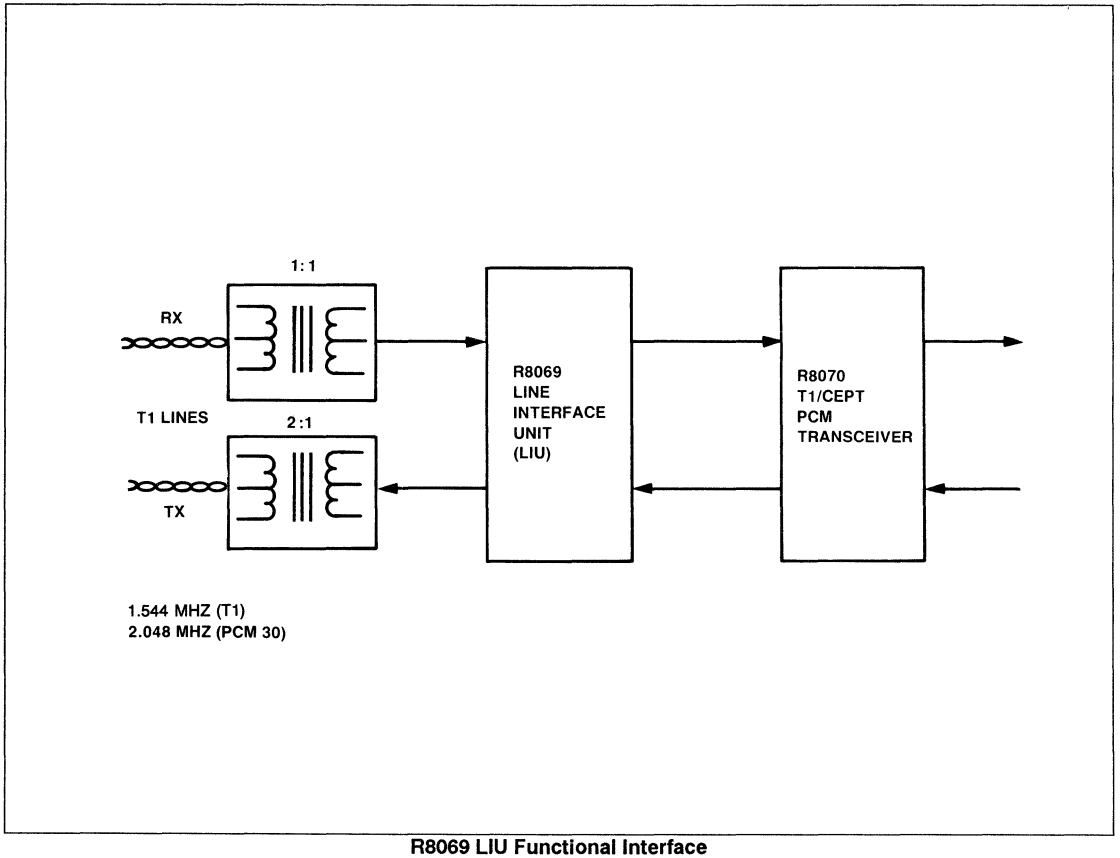
Part Number:
R8069_

Temperature
Blank = 0°C to + 70°C

Package
P = 28-Pin Plastic DIP

INTERFACE SIGNAL DESCRIPTION

The R8069 interfaces directly to the R8070 and R8071 on one side and the DSX-1 or PCM30 demarcation point on the other, through transmit and receive transformers located external to the LIU device. The R8069 LIU interface signals are functionally grouped in Figure 1. Figure 2 shows the R8069 pin assignments. The R8069 interface signals are described in Table 1.



R8069 LIU Functional Interface

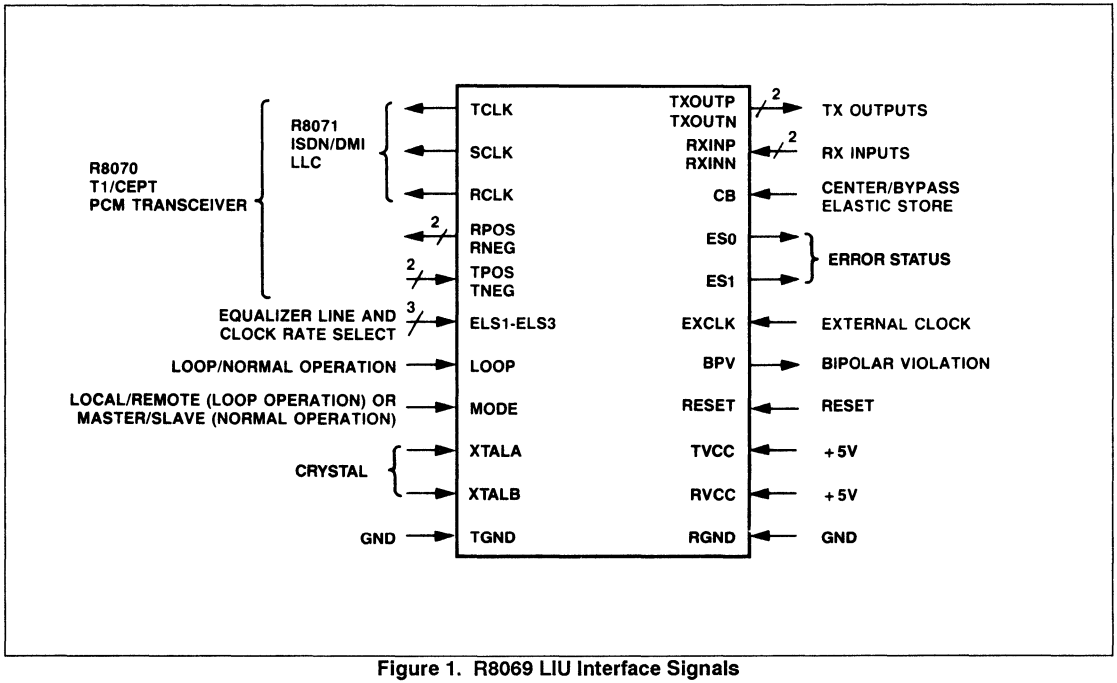


Figure 1. R8069 LIU Interface Signals

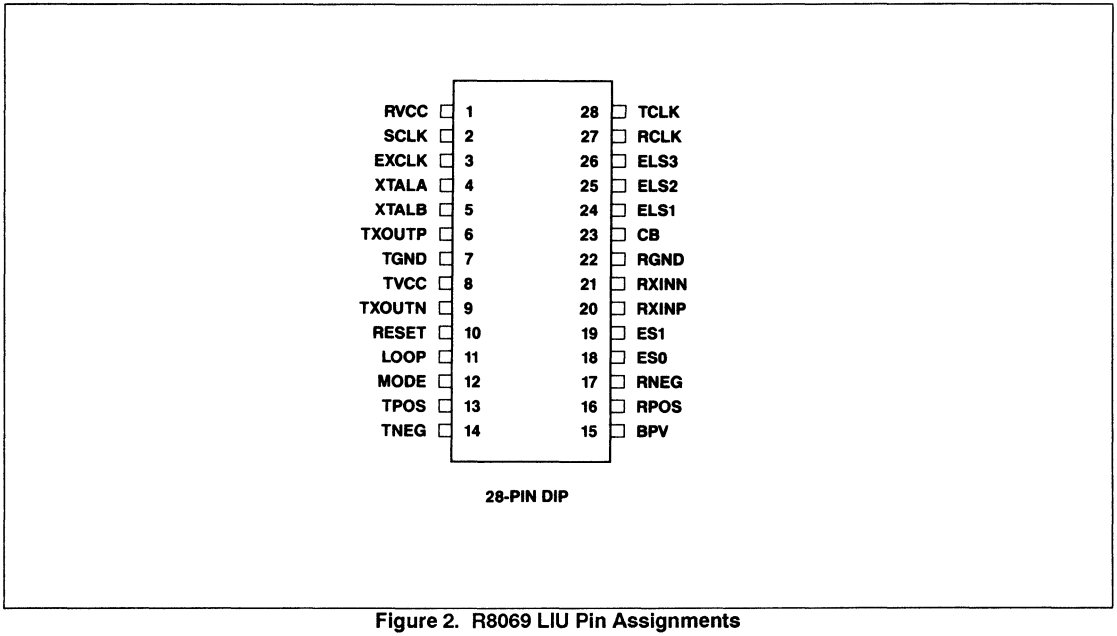


Figure 2. R8069 LIU Pin Assignments

Table 1. R8069 Interface Signal Descriptions

Symbol	Pin	I/O	Name/Function
RXINP, RXINN	20, 21	I	**Receive Data Input P, Receive Data Input N.** Receive bipolar data from transmission line. A 1:1 transformer is required on these input lines.
RPOS, RNEG	16, 17	O	**Receive Unipolar Positive, Receive Unipolar Negative.** RPOS and RNEG are the outputs of the received data recovered from RXINP and RXINN AMI line pulses. RPOS and RNEG have TTL levels and are in NRZ format. (These lines can be directly connected to R8070's RPOS and RNEG inputs.) RPOS and RNEG are clocked out at the falling edge of TCLK (when elastic store bypass is enabled) or RCLK (when elastic store bypass is disabled).
RCLK	27	O	**Recovered Clock.** RCLK is the recovered clock output which is locked to the carrier frequency and phase of the incoming data.
EXCLK	3	I	**External Clock.** EXCLK is a TTL level input. The clock frequency should be 1.544 MHz ±32 ppm for T-1 applications and 2.048 MHz ±50 ppm for PCM30 applications.
CB	23	I	**Center/Bypass Elastic Store.** Elastic store is centered on the rising edge of CB. Elastic store is bypassed when CB is high. (Minimum pulse width is one clock cycle.)
BPV	15	O	**Bipolar Violation Detection.** Whenever a bipolar violation on the input bus is detected, the BPV generates a positive pulse of one unit interval at the falling edge of TCLK (CB low) or RCLK (CB high).
ES0, ES1	18, 19	O	**Error Status.** The Error Status is continuously updated on the rising edge of TCLK. **ES0 ES1** 0 0 **AIS Detected.** AIS is activated by detection of a string of 2316 ones with no more than two zeros. AIS is deactivated when three or more zeros are found after the AIS detection. 0 1 **Loss of Signal.** Activated when the input signal level drops below 0.5 volts; deactivated when the input signal level rises above 1.0 volts. 1 0 **Elastic Buffer Limit**. Indicates an overrun/underrun on the elastic store. It will be negated when CB or RESET is activated. 1 1 **Normal Operation.**
TPOS, TNEG	13, 14	I	**Transmit Unipolar Positive, Transmit Unipolar Negative.** TPOS and TNEG are the "unipolar paired" input for transmitted data. TPOS and TNEG must have TTL levels and must be in NRZ format. (These lines can be directly connected to R8070 TPOS and TNEG outputs.) They are clocked in at the falling edge of TCLK. There are only three valid states for TPOS/TNEG (10, 01, 00); **state 11 is not allowed**.
TXOUTP, TXOUTN	6, 9	O	**Transmit Data Output P, Transmit Data Output N.** Transmit bipolar data to transmission line. A 1:2 step up transformer is needed at the output.
TCLK	28	O	**Transmit Clock.** TCLK is the transmitter clock output which is either the smoothed clock provided through EXCLK, or the smoothed clock extracted from the input data when in the slave mode. TPOS and TNEG are clocked in on the falling edge of TCLK. The receive data is also clocked out on the falling edge of TCLK, except when in the elastic store bypass mode (CB high). (TCLK output provides the proper clock signal to the R8070's and R8071's TCLK and/or RCLK.)
SCLK	2	O	**System Clock.** SCLK runs at two times the clock rate of TCLK, which is required by the R8071.
ELS1-ELS3	24, 25, 26	I	**Equalizer Line and Clock Rate Select.** Selectable strap inputs that allow selection of T-1 cable length equalization or the PCM30 line load impedance selection.

Table 1. R8069 Interface Signal Descriptions (Cont'd)

Symbol	Pin	I/O	Name/Function
LOOP	11	I	**Loop Operation Select.** LOOP low selects normal operation (MODE selects master or slave timing). LOOP high selects loop operation (MODE selects local or remote loop).
MODE	12	I	**Mode Select.** In **normal operation** (LOOP low), MODE low selects master timing and MODE high selects slave timing. In **loop operation** (LOOP high), MODE low selects local loop and MODE high selects remote loop.
RESET	10	I	**Reset.** Recenters the elastic store and trains the VCO to lock to EXCLK when RESET is high.
XTALA, XTALB	4, 5	I	**XTAL Input pins.** An external parallel resonant 6.176 MHz or 8.192 MHz crystal is needed for T-1 or PCM30, respectively.
RVCC	1	I	**Receive Power.** +5V power supply for the receive section.
RGND	22	I	**Receive Ground.** Ground for the receive section.
TVCC	8	I	**Transmit Power.** +5V power supply for the transmit section.
TGND	7	I	**Transmit Ground.** Ground for the transmit section.

FUNCTIONAL DESCRIPTION

The R8069 LIU contains both analog and digital circuitry to independently process transmit and receive primary rate voice or data information. Circuitry to provide local loop, remote loop and master/slave timing is also included. A simplified block diagram of the Rockwell R8069 Line Interface Unit (LIU) is depicted in Figure 3.

TRANSMIT SECTION

Transmit data (TPOS and TNEG) are provided to the R8069 from the R8070 for the generation of Alternate Mark Inversion (AMI) data on output pins TXOUTP and TXOUTN. The input data are provided to a transmit compromise line equalizer for pulse shaping and conditioning. The equalizer is capable of equalizing for up to 655 feet of ABAM cable (22-gauge plastic insulated cable with characteristics specified in Appendix B of the AT&T Technical Reference Number 34, Sept 1983). The recommended cable is AT&T part no. 606-6/22 R6900.

Three encoded inputs, ELS1-ELS3, allow selection of cable length equalization and clock rates (Table 2). Equalization for cable lengths of 0-660 feet in increments of 110 feet are selectable for a T-1 line. Loading impedance of 75 Ω (for coaxial cable) or 120 Ω (for twisted-pair cable) is selectable for a PCM30 line.

The equalized data are then provided to a line driver. In T-1 environment with a modulation rate of 1.544 Mbps, this driver can drive a twisted pair cable up to 655 feet in length, and still meet the Isolated Pulse Template at the end of the cable (at DSX-1) as specified by AT&T Technical Advisory No. 34. In PCM30 mode, the LIU provides a pulse shape which, when measured at the output of the transmit transformer, meets the requirements of CCITT Recommendation G.703. The typical output pulse shape conforms to the DSX-1 pulse template for T-1 (Figure 4 and Table 3) and PCM30 (Figure 5).

RECEIVE SECTION

On the receive side, bipolar input data (RXINN and RXINP) is converted to a unipolar signal from which a clock can be extracted. A phase locked loop circuit (PLL1), which is based on an internal oscillator circuit, extracts the clock from the incoming data. The PLL1 clock recovery circuit derives the Recovered Clock (RCLK) from this unipolar signal, unless Loss of Signal occurs. Should Loss of Signal occur, PLL1 derives RCLK from the External Clock (EXCLK) input.

Depending on the loop and timing mode selection, phase locked loop circuit PLL2 smooths the clock signal (1.544 MHz or 2.048 MHz) provided by the EXCLK input or the RCLK output of PLL1. Jitter-free TCLK and SCLK clocks are then generated by PLL2. PLL2 is based on the crystal oscillator input at XTALA and XTALB. TCLK represents the base clock frequency (1.544 MHz or 2.048 MHz) and SCLK is twice the base frequency. TCLK and SCLK are used as transmit clocks by the R8070 and R8071, respectively.

Table 2. ELS1 - ELS3 Encoding

ELS3	ELS2	ELS1	Cable Length/ Line Impedance	Clock Rate*
L	L	L	0 - 110 ft	T-1
L	L	H	110 - 220 ft	T-1
L	H	L	220 - 330 ft	T-1
L	H	H	330 - 440 ft	T-1
H	L	L	440 - 550 ft	T-1
H	L	H	550 - 660 ft	T-1
H	H	L	120 Ω	PCM30
H	H	H	75 Ω	PCM30

* T-1 = 1.544 MHz; PCM30 = 2.048 MHz

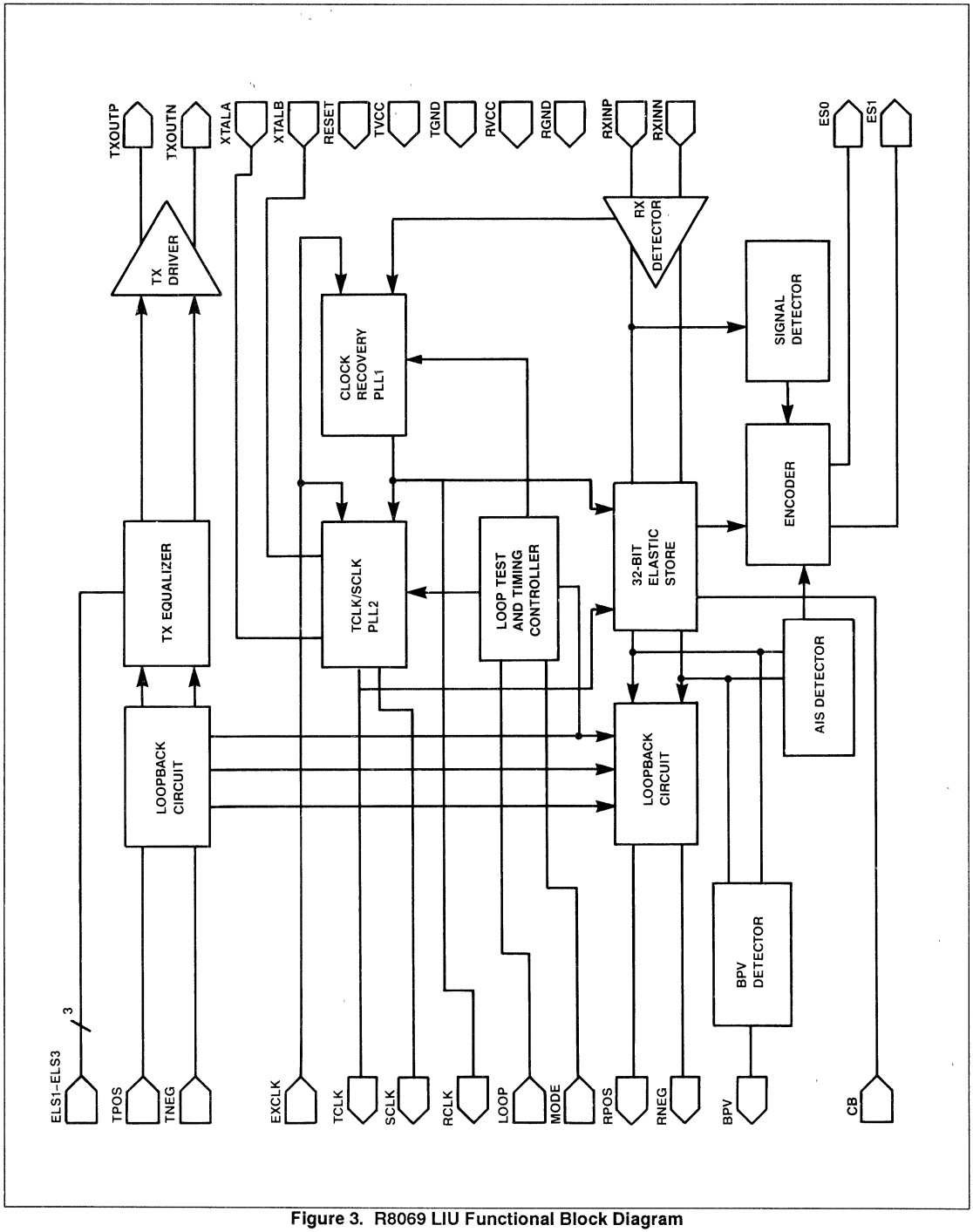


Figure 3. R8069 LIU Functional Block Diagram

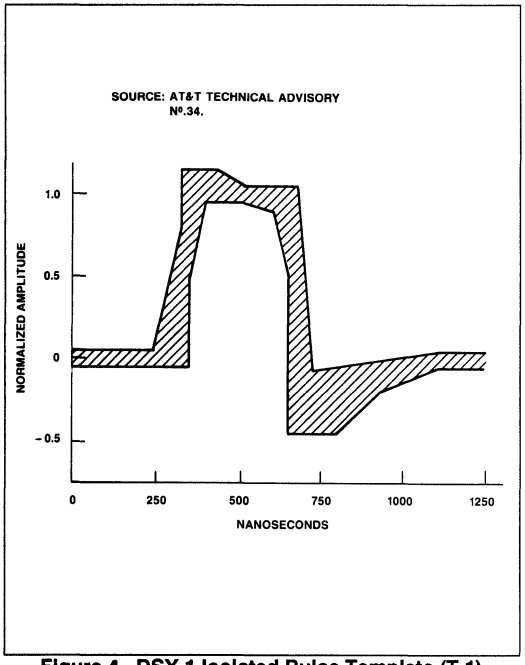
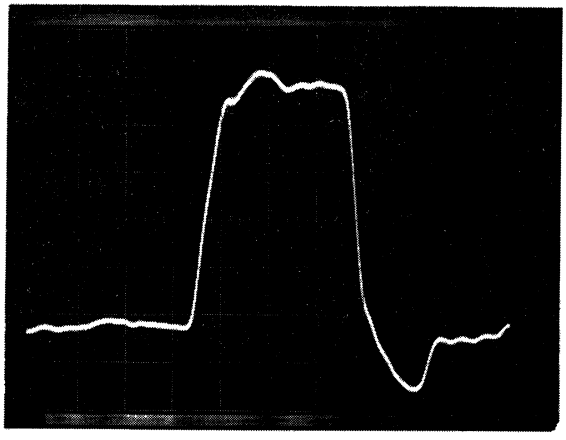


Figure 4. DSX-1 Isolated Pulse Template (T-1)

Table 3. DSX-1 Pulse Template Corner Points (T-1)

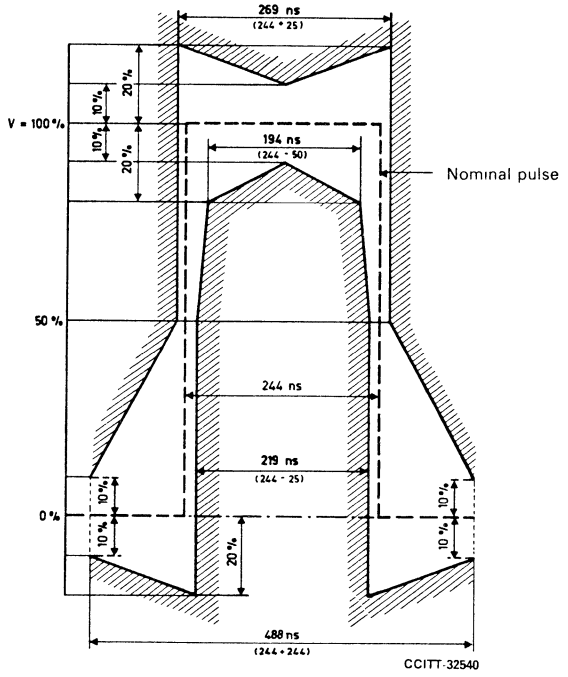
Maximum Curve		Minimum Curve	
ns	Normalized Voltage	ns	Normalized Voltage
0,	0.05	0,	–0.05
250,	0.05	350,	–0.05
325,	0.80	350,	0.50
325,	1.15	400,	0.95
425,	1.15	500,	0.95
500,	1.05	600,	0.90
675,	1.05	650,	0.50
725,	–0.07	650,	–0.45
875,	0.05	800,	–0.45
1250,	0.05	925,	–0.20
		1100,	–0.05
		1250,	–0.05

Note: Successive corner points are joined by straight lines to form the template shown in Figure 4.



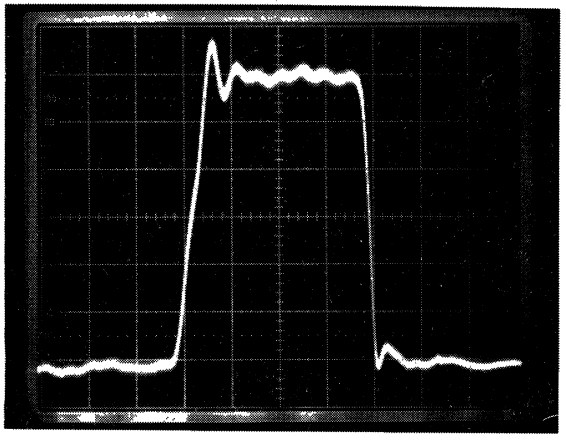
Actual T-1 Pulse Waveform at 330 Feet

6



FOR
75 Ω LOAD IMPEDANCE: V = 2.37V
120 Ω LOAD IMPEDANCE: V = 3.00V
OPERATING FREQUENCY 2.048 MBPS
SOURCE: CCITT REC G.703

Figure 5. DSX-1 Isolated Pulse Template (PCM30)



Actual PCM30 Pulse Waveform with Load Impedance = 75 Ohms

R8069 Jitter Conformance

Input jitter tolerance, intrinsic output jitter and jitter transfer function of the R8069 surpasses the requirements set forth in AT&T Pub 62411 and CCITT Recommendation G.823.

Jitter is defined as a short term phase shift of a digital signal from its ideal position in time. Wander (jitter below 10 Hz) is a long term phase shift of a digital signal, which may result due to change in the propagation delay of the transmission media being used.

Input jitter tolerance is the amount of jitter that the Data Terminal Equipment (DTE) can accept in its input signal and still be able to operate with specified bit error rate (BER $<10^{-8}$). The input jitter tolerance of the R8069 is shown in Figure 6a. The jitter tolerance of the R8069 PLL clock recovery circuit is shown in Figure 6b.

Intrinsic output jitter is the inherent jitter generated within the individual equipment when the input signal is jitter free. The R8069's advanced PLL utilizes a parallel resonant crystal in its circuitry in order to achieve an extremely low intrinsic output jitter. The maximum output jitter is shown in Figure 7.

Jitter transfer function represents the amount of jitter that is carried over from the input signal to the output signal. The R8069 advanced design minimizes this transference of jitter from the input signal to the output signal as depicted be seen in Figure 8.

Elastic Buffer

In order to avoid data loss due to jitter, a 32-bit elastic store is provided in the receive data path. Its function is to eliminate the effect of short term jitter resulting from transmission line impairments. The receive data is written into the elastic buffer by the Recovered Clock (RCLK) and read out from the elastic buffer by TCLK. The output of the elastic buffer drives the unipolar output signal (RPOS and RNEG).

Input signal CB is used in conjunction with the elastic store to center/bypass the 32-bit buffer should an overflow or underflow of the data be detected. When CB is high, the elastic buffer is bypassed and receive data drives the unipolar output signal (RPOS and RNEG) directly. An overflow or underflow of the data is reported by the error status outputs (ES0=H and ES1=L). The overflow or underflow status can be negated by asserting CB or RESET. Figures 9 and 10 show the relative timing of the receiver channel signals for the Elastic Store Enable and Elastic Store Bypass modes, respectively.

Loss of Signal

Loss of signal indicates detection of a low level signal and is represented in the error status by outputs ES0=L and ES1=H. When loss of signal occurs, PLL2 always switches to using the EXCLK as the reference clock to generate TCLK and SCLK.

Alarm Indicator Signal

Alarm Indicator Signal (AIS) is asserted when a long string of ones (2316) and less than 3 zeros are detected in a row. This condition indicates that a possible local loop back test may be taking place at the other end of the line. This condition is represented in the error status by ES0=L and ES1=L.

When multiple error status occurs, only the status that has the higher priority is reported. Both loss of signal and AIS share the highest priority but are mutually exclusive, thus preventing a conflict of priority. Elastic buffer limit exceeded has a lower priority than either AIS and loss of signal.

Bipolar Violation

Bipolar violation is reported on output pin BPV whenever bipolar violations occur on RPOS and RNEG. Output pin BPV generates a positive pulse of one unit interval (T-1: 1 UI = 648 ns; PCM30: 1 UI = 488 ns) at the falling edge of TCLK (when CB=low) or RCLK (when CB=high).

LOOP AND TIMING MODE SELECTION

Input pins LOOP and MODE select different loopback and timing configurations. The LOOP input determines either normal (no loop) or loop operation. The MODE input selects master/slave timing in normal operation, or local/remote loop in loop operation:

LOOP	MODE	Operation/mode
L	L	Normal operation - Master timing
L	H	Normal operation - Slave timing
H	L	Loop operation - Local loop
H	H	Loop operation - Remote loop

NORMAL OPERATION

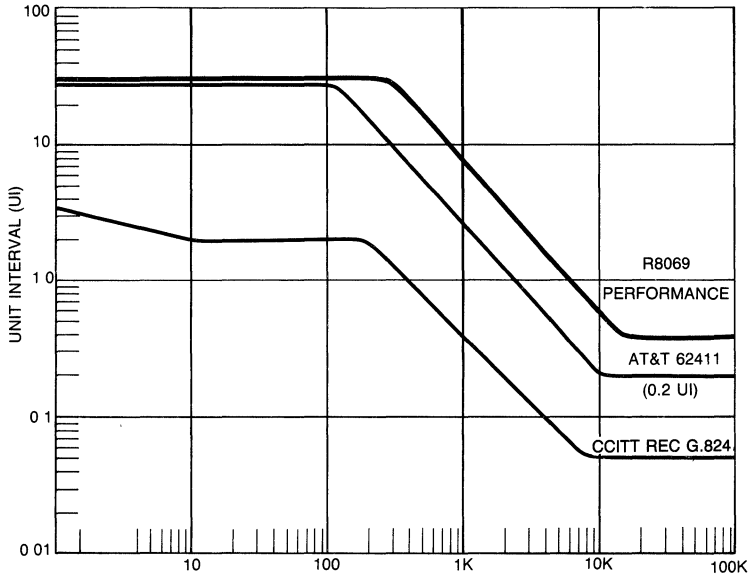
When the LOOP input is low, normal operation (no loopback) is selected. The separate transmit and receive sections of the LIU process data independently. In normal operation the LIU offers the flexibility of operating in either a master (MODE=L) or a slave (MODE=H) timing configuration. Figures 11 and 12 show the relative timing of the transmit channels for master and slave modes, respectively.

Normal Operation - Slave Timing

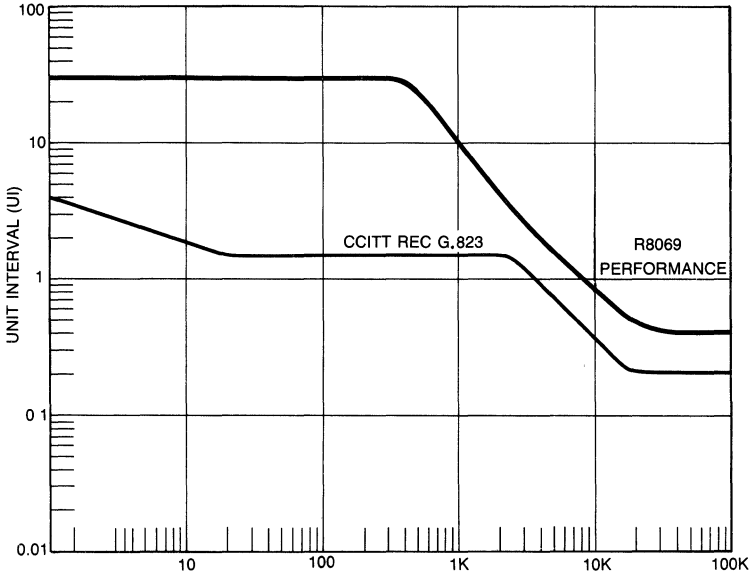
In slave timing mode, the recovered clock (RCLK) is extracted from the incoming receive data. TCLK and SCLK are also derived from the recovered clock. This configuration support DMI type applications where the PBX acts as a master and the host as a slave.

Normal Operation - Master Timing

In master timing mode, RCLK is still extracted from the incoming received data while TCLK and SCLK are extracted from the external input clock (EXCLK).



1.544 MHz Operation



2.048 MHz Operation

Figure 6a. R8069 Input Data Jitter Tolerance

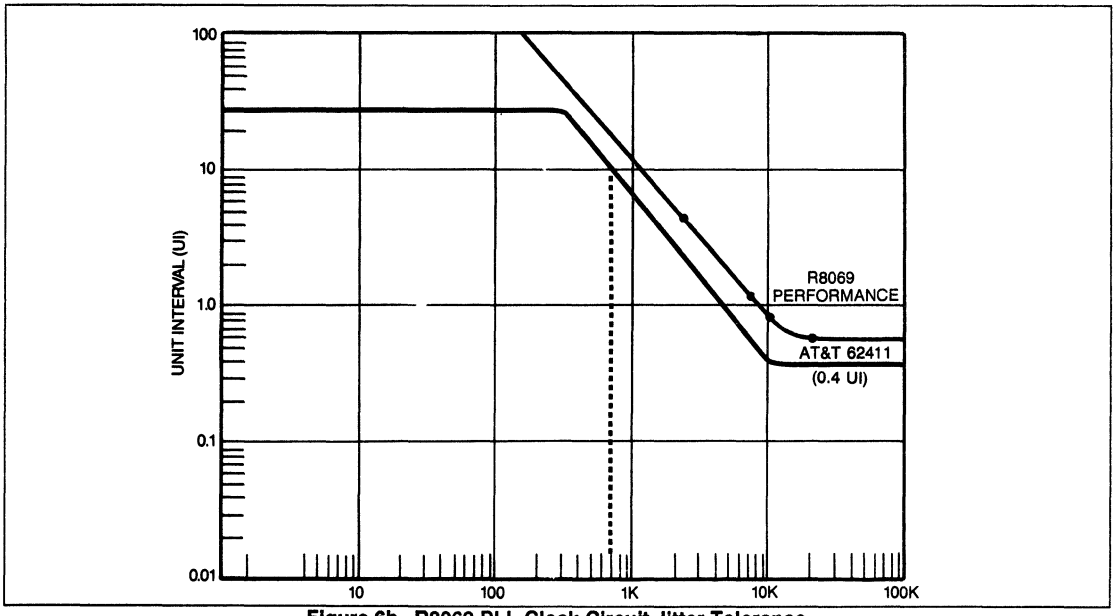


Figure 6b. R8069 PLL Clock Circuit Jitter Tolerance

6

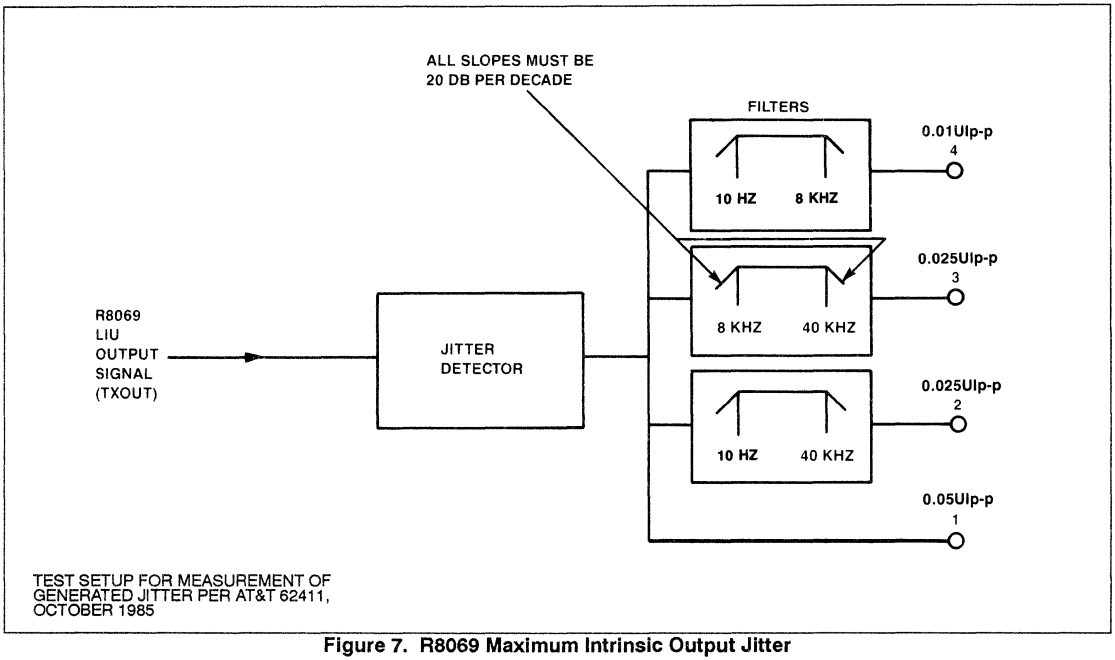


Figure 7. R8069 Maximum Intrinsic Output Jitter

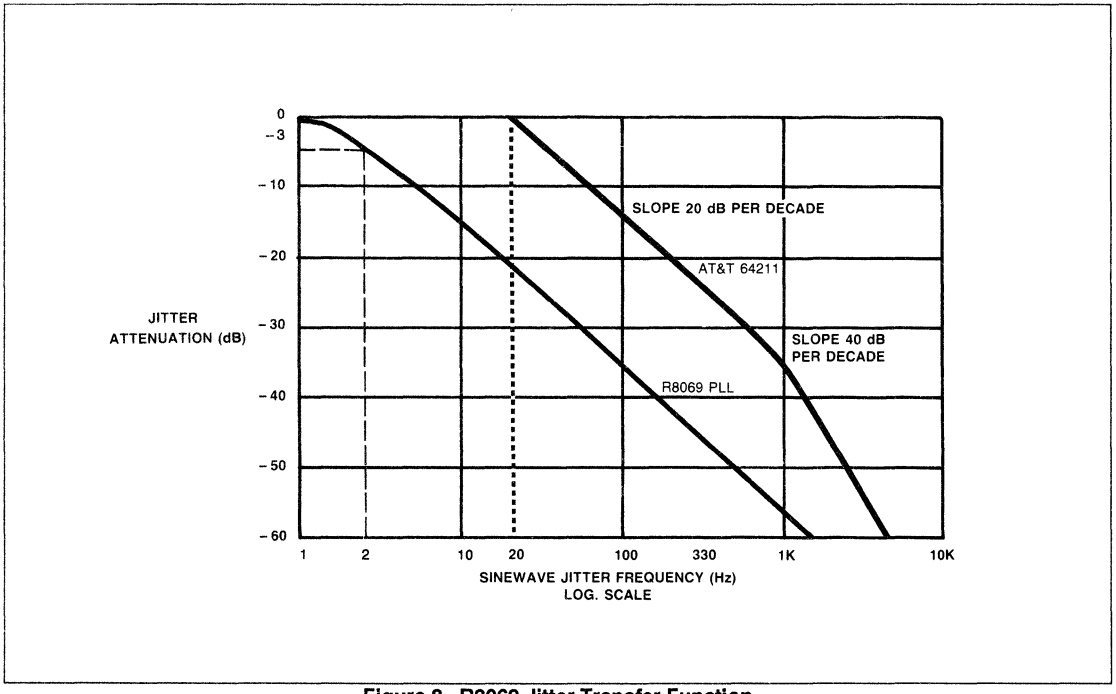


Figure 8. R8069 Jitter Transfer Function

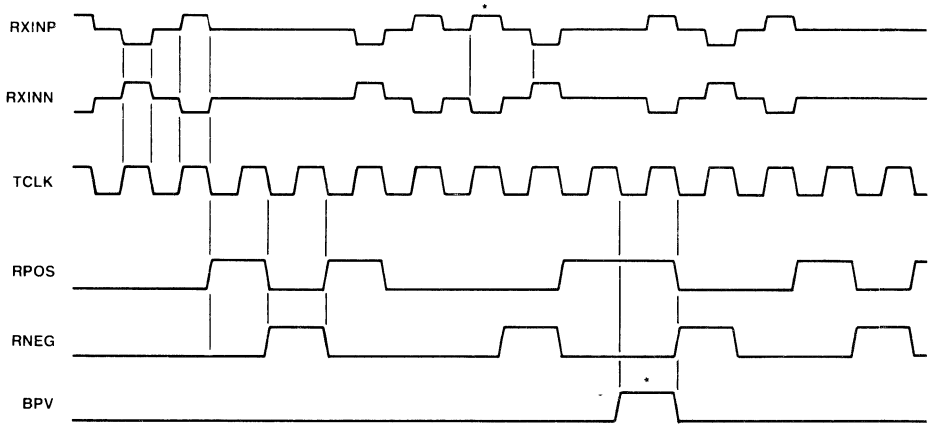


Figure 9. R8069 Receiver Waveforms - Elastic Store Enable

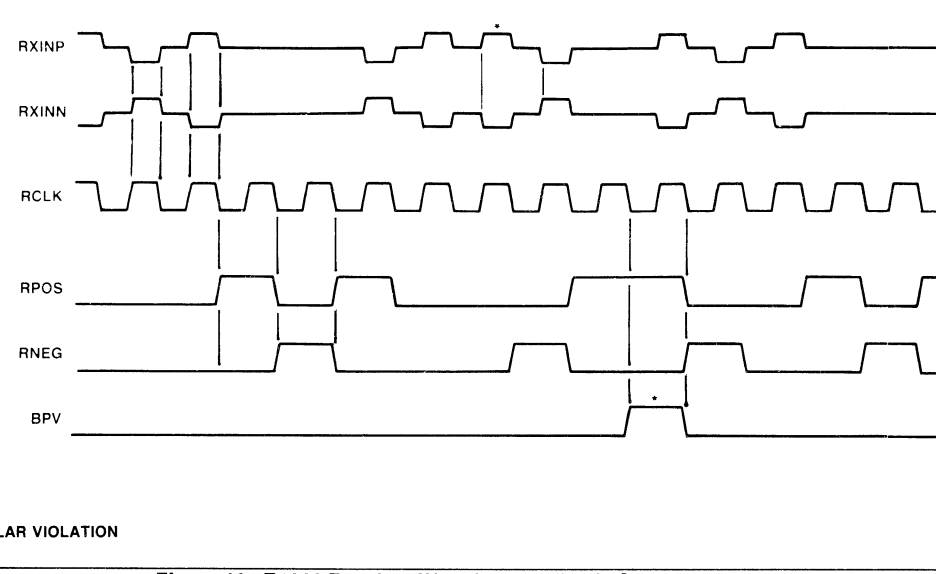


Figure 10. R8069 Receiver Waveforms - Elastic Store Bypass

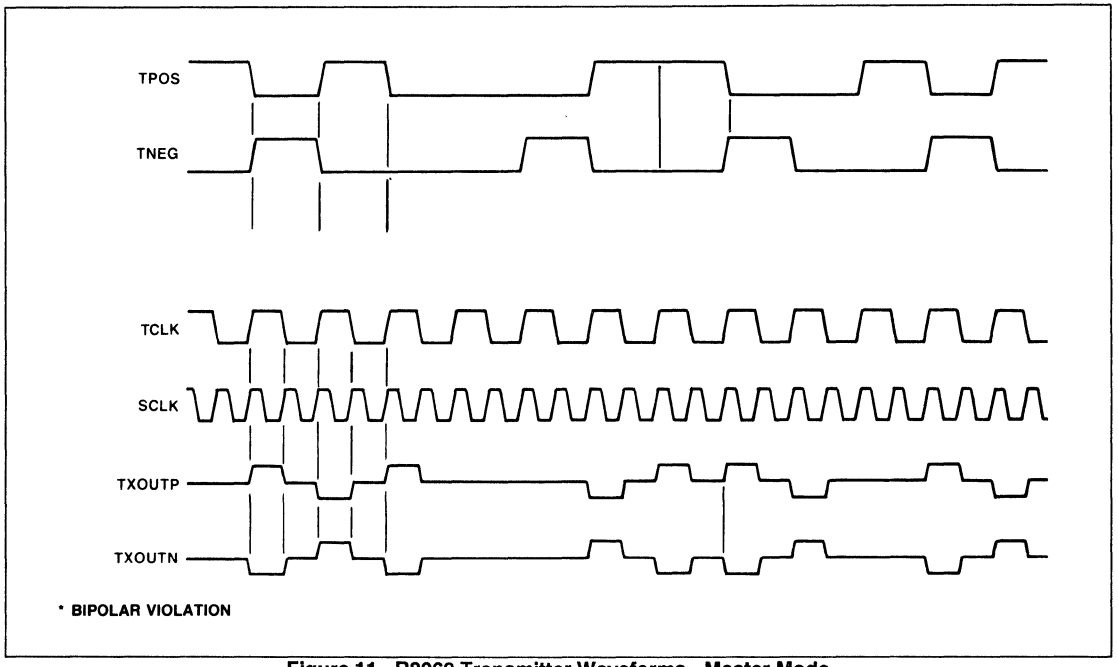


Figure 11. R8069 Transmitter Waveforms - Master Mode

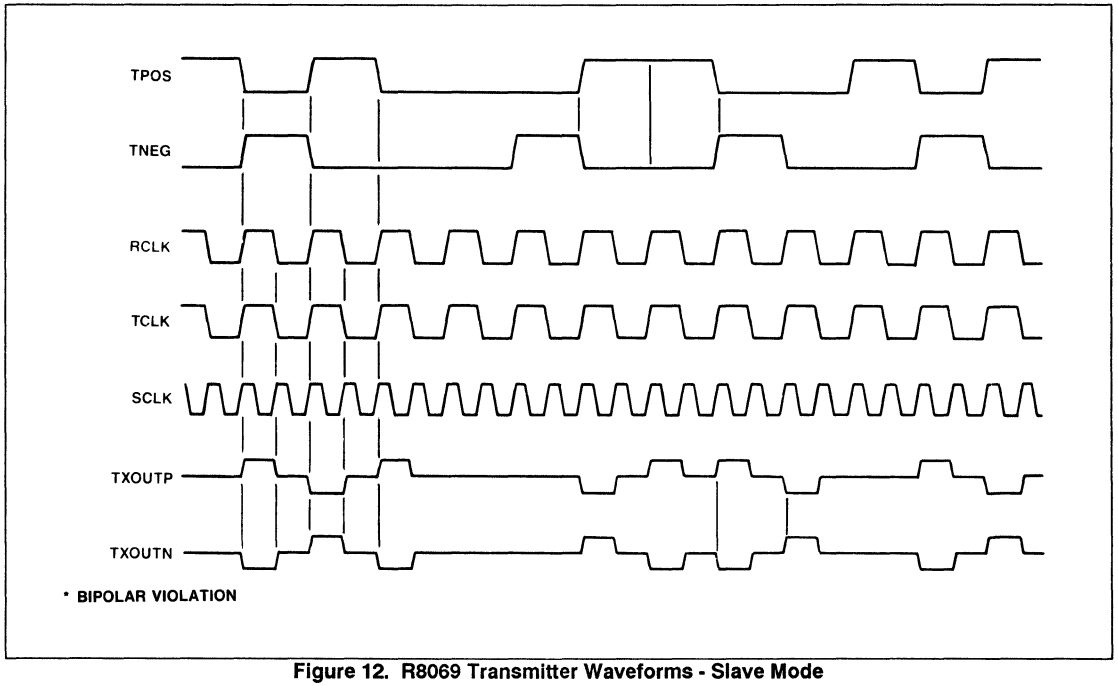


Figure 12. R8069 Transmitter Waveforms - Slave Mode

LOOP OPERATION

When the LOOP input is high, loopback operation is selected. Loopback modes allow testing of LIU operation and signal routing in local (MODE=low) or remote (MODE=high) configuration.

Local Loop

In local loop operation, the transmit input data (TPOS and TNEG) is looped internally to the receive data outputs (RPOS and RNEG). Data provided to the T-1/CEPT line on the TXOUTP and TXOUTN consists of a string of ones transmitted to the remote end (Blue Alarm). The received data on RXINP and RXINN is ignored. In this mode, RCLK is normally not used for clocking data into the R8070. RCLK is, however, still extracted from the received data on RXINP and RXINN, while TCLK and SCLK are extracted from EXCLK.

Remote Loop

In remote loop operation, the receive input data (RXINP and RXINN) is looped back onto the transmit data outputs (TXOUTP and TXOUTN) and is transmitted back to the remote end. The processing of the input data by the LIU receive side continues uninterrupted. The input transmit data made available to the LIU on TPOS and TNEG are ignored, and hence, do not appear on TXOUTP and TXOUTN outputs. In this mode all output clocks (RCLK, TCLK and SCLK) are derived from the received data on RXINP and RXINN.

APPLICATION

Typical R8069 LIU connections are shown in Figure 13, 14 and 15.

Note that a 430 ohms ± 5% (power dissipation < 1/8 W) external resistor in shunt with the secondary output of the transmit transformer (Falcon 27.1) is required in order to meet the 120 ohm CEPT pulse template (Figure 15).

Listed below are critical criterias in which the R8069 LIU will meet applicable pulse templates:

- For CEPT using twisted pair wire (120 ohms), a 430 ohm shunt resistor is required as stated above.
- For CEPT using coaxial cable (75 ohms), the 430 ohm resistor is not to be used.
- For T-1 (100 ohms), the R8069 will work with or without the 430 ohm resistor, i.e., its use is optional in T-1 mode.

Application Note, "R8069 Interface Transformer Specifications and Connections", Order No. 340, is also available.

Table 4. Load Impedance and Shunt Resistor

Mode	Load Impedance	430 ohm Resistor
CEPT 1	120 Ohms	Required
CEPT 2	75 Ohms	Not to be used
T-1	100 Ohms	Optional

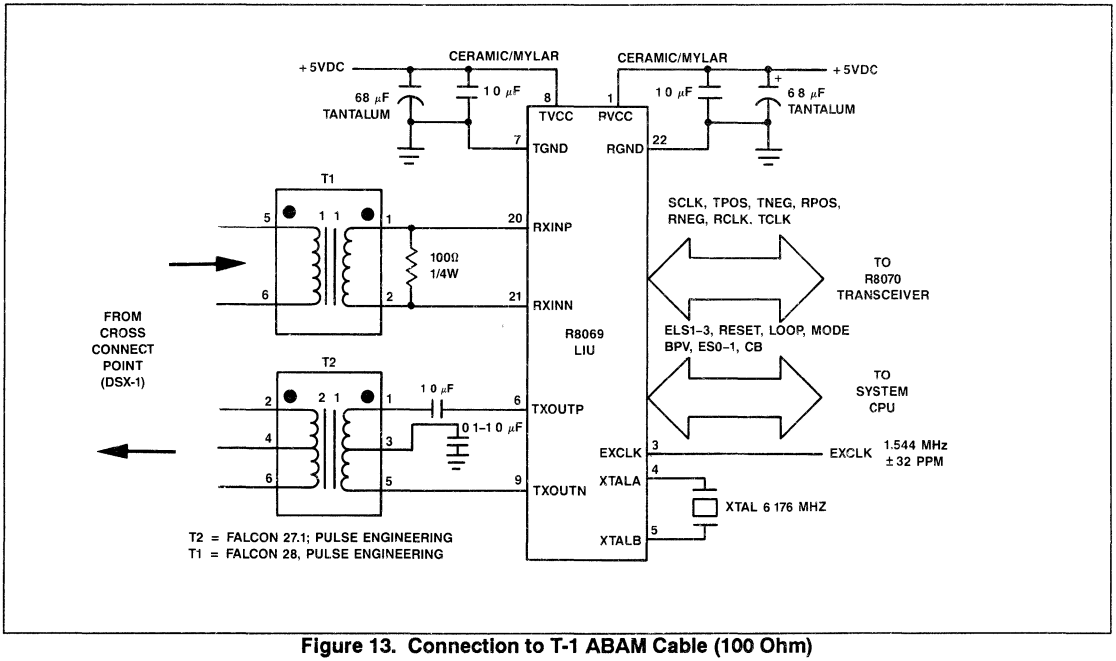


Figure 13. Connection to T-1 ABAM Cable (100 Ohm)

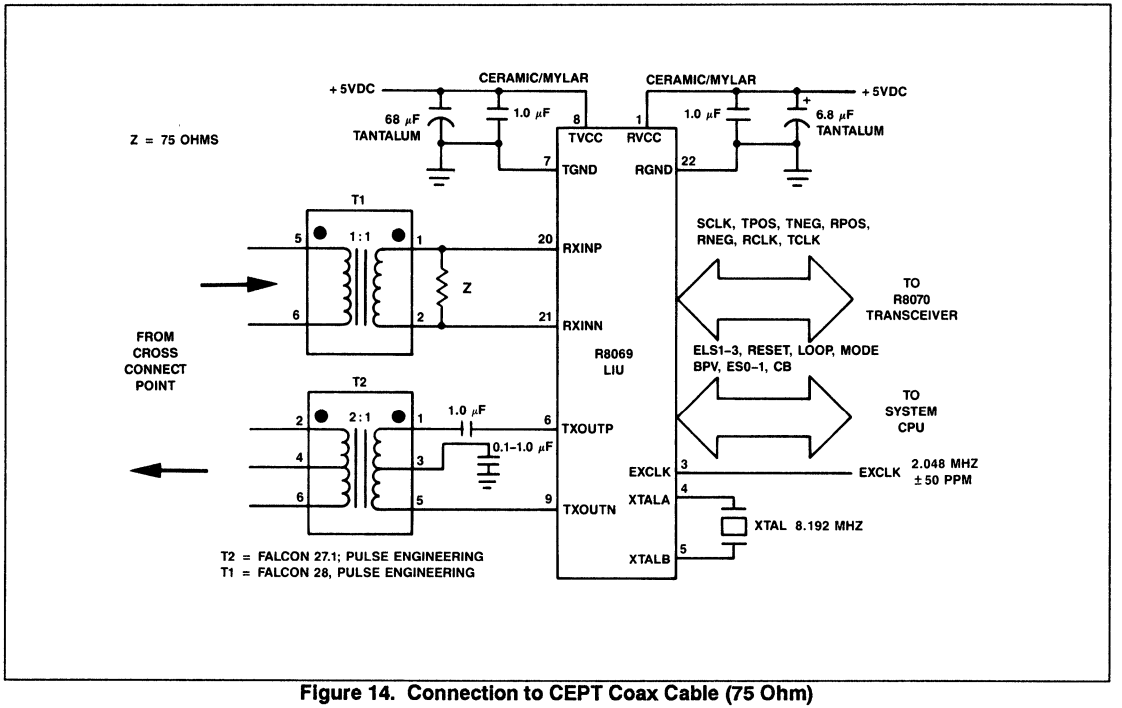


Figure 14. Connection to CEPT Coax Cable (75 Ohm)

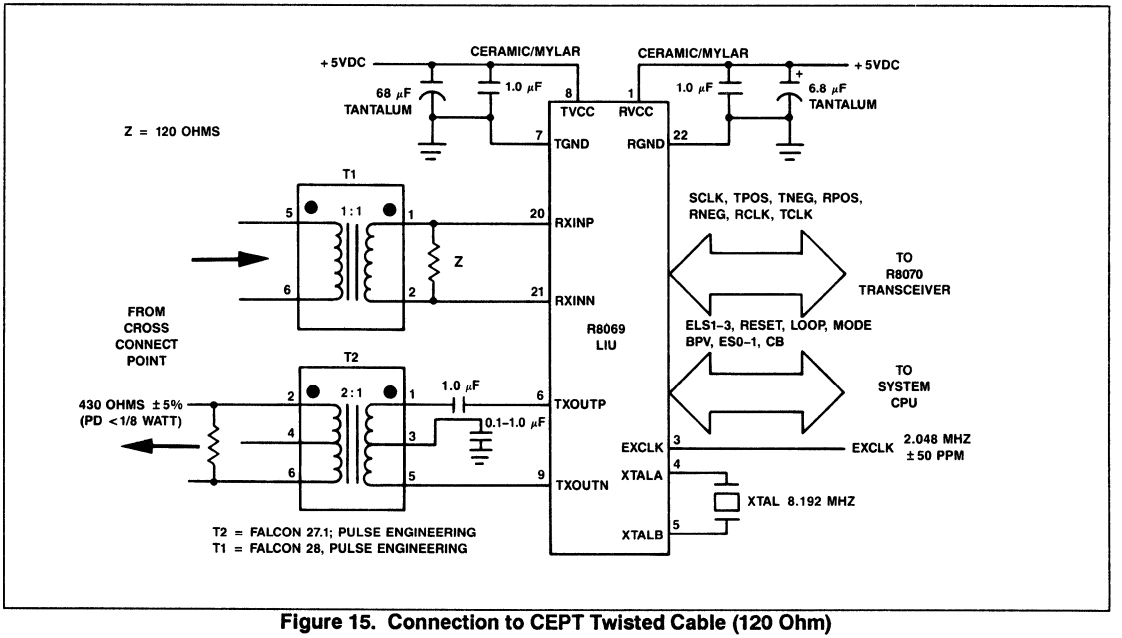


Figure 15. Connection to CEPT Twisted Cable (120 Ohm)

LIU SYSTEM APPLICATIONS

Two typical R8069 applications are shown on Figures 13 and 14.

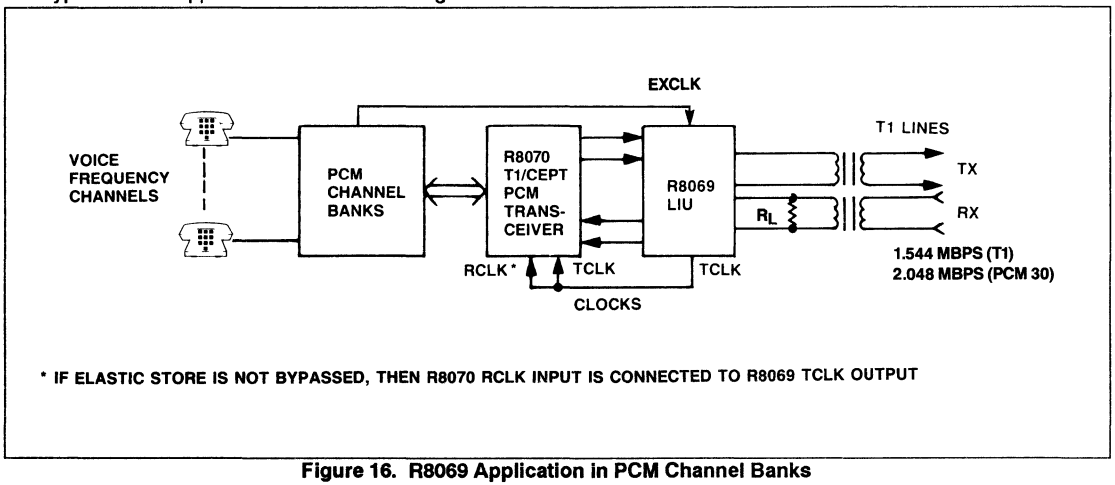


Figure 16. R8069 Application in PCM Channel Banks

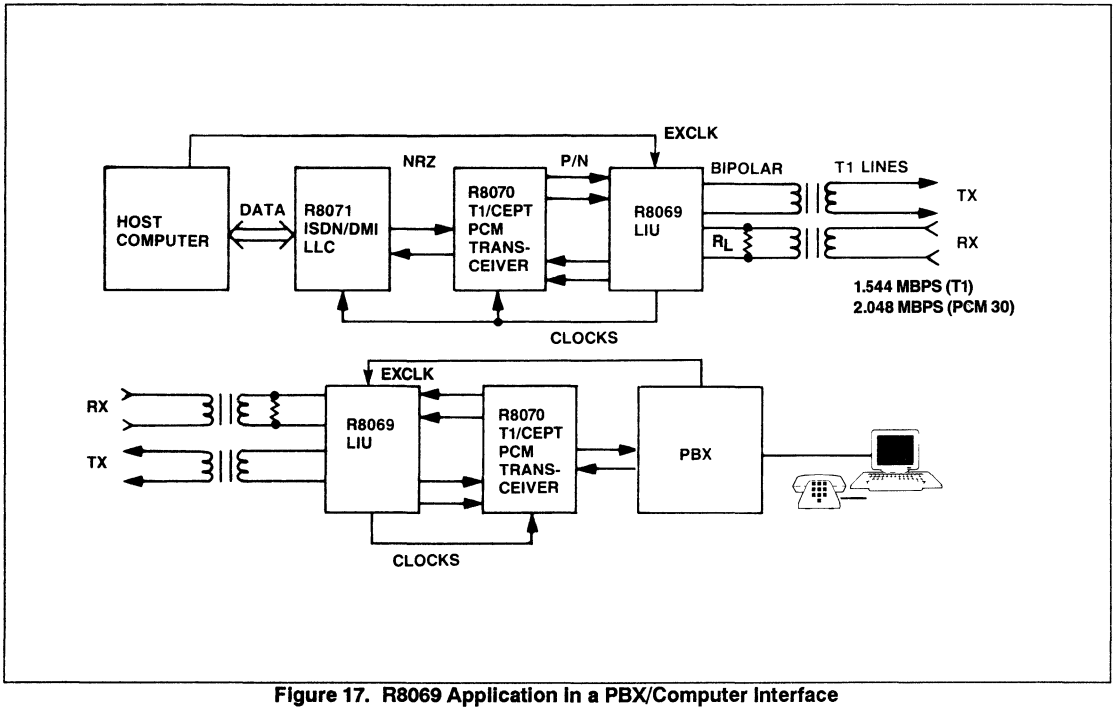
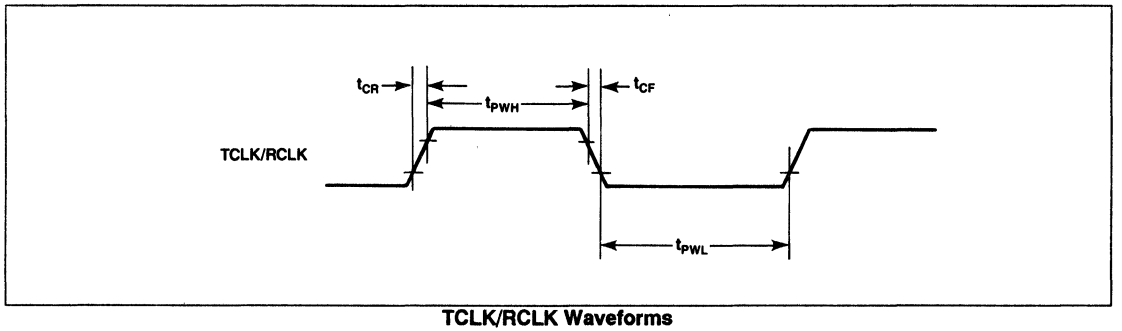
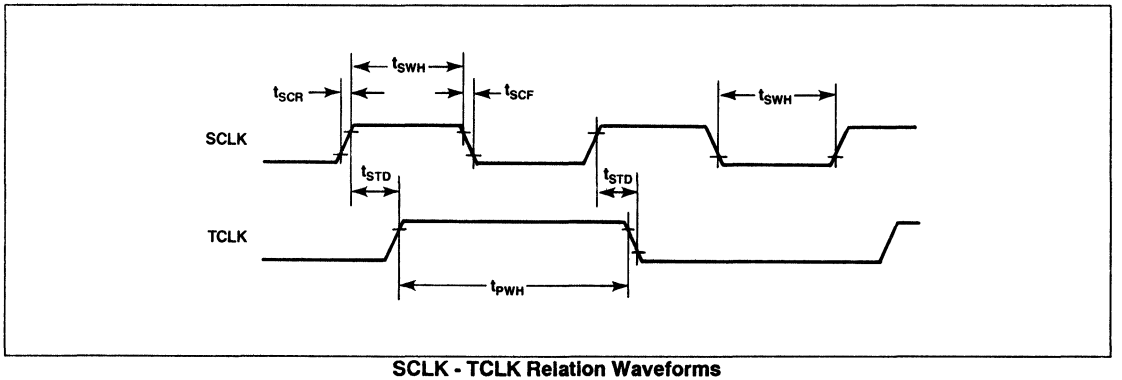


Figure 17. R8069 Application in a PBX/Computer Interface

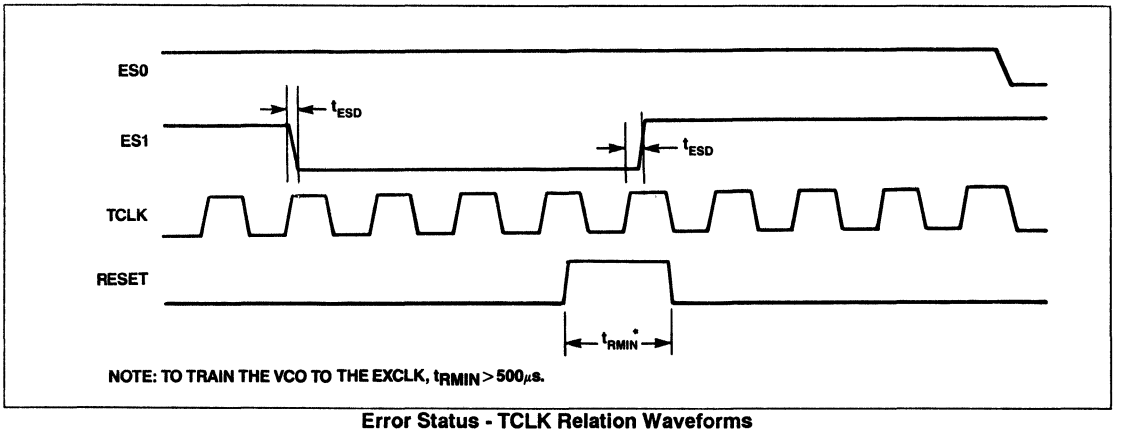
SWITCHING CHARACTERISTICS - WAVEFORMS



TCLK/RCLK Waveforms

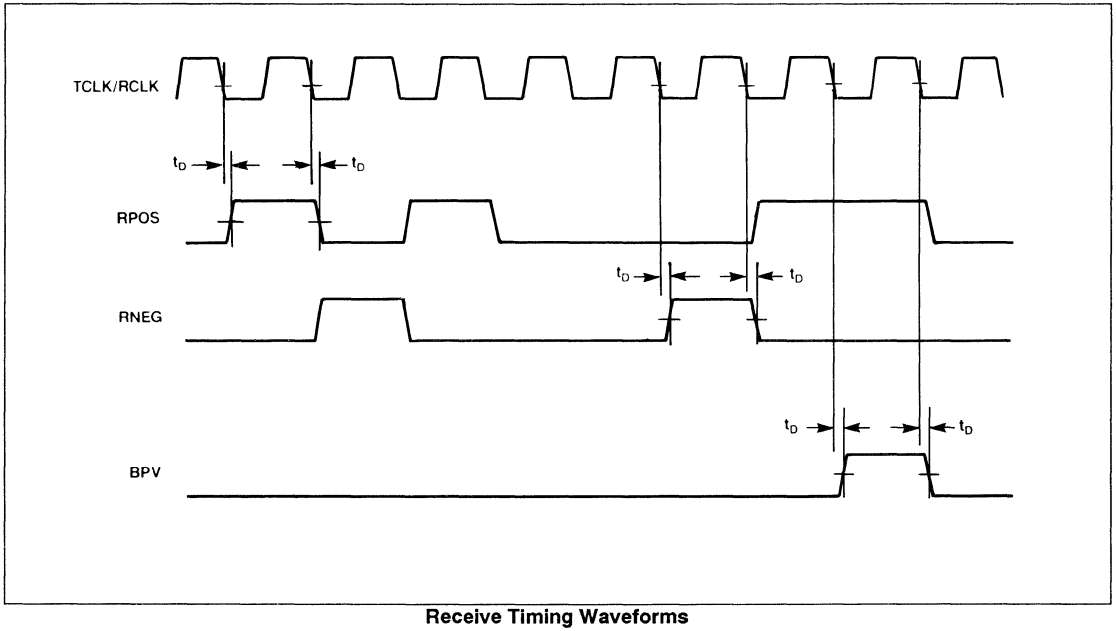


SCLK - TCLK Relation Waveforms

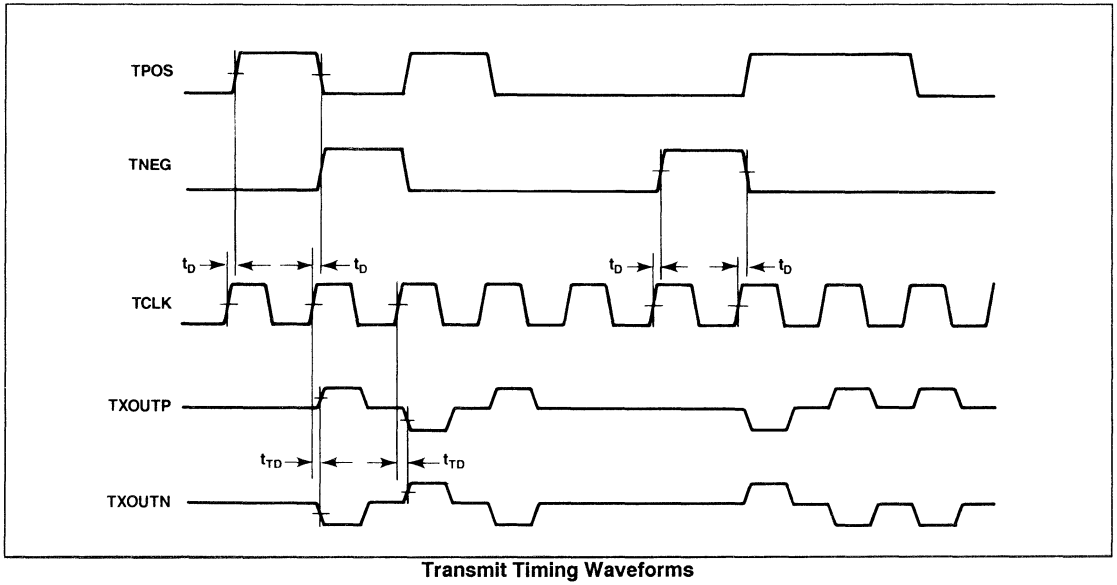


Error Status - TCLK Relation Waveforms

SWITCHING CHARACTERISTICS - WAVEFORMS (CONT'D)



Receive Timing Waveforms



Transmit Timing Waveforms

SWITCHING CHARACTERISTICS – TIMING

(V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, Vdc T_A= 0°C to 70°C, unless otherwise specified)

Parameter	Symbol	Min.	Max.	Units	Notes
Rise and Fall time					
RCLK, TCLK	t_{CR}, t_{CF}	–	20	ns	1
SCLK	t_{SCR}, t_{SCF}	–	10	ns	2
Rise and Fall time,					
TPOS, TNEG, RPOS, RNEG, BPV, ES0, ES1	t_{PR}, t_{PF}	–	60	ns	
Delay Time					
TCLK (or RCLK) to RPOS, RNEG, BPV	t_D	0	80	ns	
SCLK to TCLK	t_{STD}	0	50	ns	
TCLK to Error Status VALID	t_{ESD}	0	80	ns	
RESET Pulse Width	t_{RMIN}	244	–	ns	
T-1					
Pulse Width, TCLK or RCLK Low	t_{PWL}	315	335	ns	3
Pulse Width, TCLK or RCLK High	t_{PWH}	315	335	ns	3
Pulse Width, SCLK Low	t_{SWL}	155	165	ns	4
Pulse Width, SCLK High	t_{SWH}	155	165	ns	4
PCM30					
Pulse Width, TCLK or RCLK Low	t_{PWL}	235	255	ns	3
Pulse Width, TCLK or RCLK High	t_{PWH}	235	255	ns	3
Pulse Width, SCLK or SCLK Low	t_{SWL}	115	135	ns	4
Pulse Width, SCLK or SCLK High	t_{SWH}	115	135	ns	4

Notes:

1. TCLK and RCLK rise and fall times are defined as TTL levels from 0.4 Vdc to 2.4 Vdc at I_{LOAD} = 1.6 mA and C_L = 50 pF.
2. SCLK rise and fall times are defined as TTL levels from 0.4 Vdc to 2.4 Vdc at I_{LOAD} = 1.6 mA and C_L = 30 pF.
3. The summation of t_{PWL} and t_{PWH} must meet the frequency specifications listed in the Interface Requirements table.
4. The summation of t_{SWL} and t_{SWH} must be exactly one-half the summation of t_{PWL} and t_{PWH}.

INTERFACE REQUIREMENTS

Characteristic	Value
Operation	4-wire full-duplex on primary rate lines (T-1 or PCM30)
Transmit Pulse Requirements	
Transmit Level	
1.544 Mbps (T-1)	3V (nominal). Fits the pulse shape templates in DSX-1 Interconnection Specification (T-1) and CCITT Recommendation G.703
2.048 Mbps (PCM30)	3V (nominal). Fits the pulse shape templates in CCITT Recommendation G.703
Transmit Pulse width	
1.544 Mbps (AT&T & CCITT)	324 ns (nominal)
2.048 Mbps (CCITT)	244 ns (nominal)
Transmit Clock Accuracy	
AT&T	1.544 Mbps ±32 ppm
CCITT	1.544 Mbps ±50 ppm
CCITT	2.048 Mbps ±50 ppm
Receive Clock Accuracy	
AT&T	1.544 Mbps ±130 ppm
CCITT	1.544 Mbps ±50 ppm
CCITT	2.048 Mbps ±50 ppm
Input Jitter Tolerance	28 UIpp
Receiver Sensitivity	10 db below DSX-1 or G.703 specification
Diagnostics	On-chip loop test circuit (local and remote)
Transmitter Transformer Test Load Impedance	
1.544 Mbps (AT&T & CCITT)	100 Ω resistive
2.048 Mbps (CCITT)	120 Ω /75 Ω resistive
Interface to R8070/R8071	
Level	CMOS/TTL compatible
Clock timing	Meets R8070/R8071 timing specifications
Data from R8070	Unipolar data to be transmitted on primary rate lines (TPOS and TNEG)
Data to R8070	Unipolar data received from primary rate lines (RPOS and RNEG)
Clocks to R8070/R8071	
Recovered Clock	RCLK
Transmit clock	TCLK
System Clock	SCLK (= 2 x TCLK)

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	–0.3 to +7.0	Vdc
Input Voltage	V_{IN}	–0.3 to V_{CC} + 0.3	Vdc
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{STG}	–55 to + 150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device r eliability.

ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, TA = 0°C to 70°C unless otherwise specified)

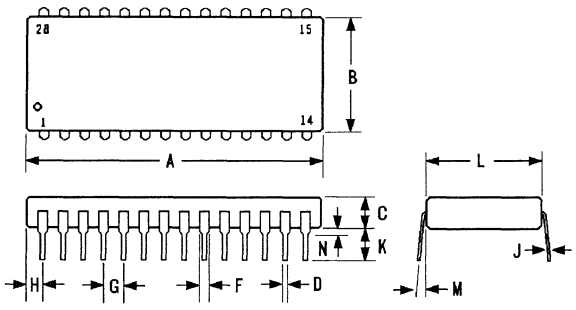
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Input Low Voltage	V_{IL}	–0.3	–	+0.8	V	
Input High Voltage	V_{IH}	+2.0	–	VCC +0.3	V	
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{LOAD} = 1.6 mA
Output High Voltage						
TTL	V_{OH}	2.4	–	–	–	I_{LOAD} = –100 µA
CMOS	–	3.5	–	–	–	I_{LOAD} = –100 µA
Output Low Current	I_{OL}	+1.6	–	–	mA	V_{OL} = 0.4V
Output High Current	I_{OH}	–100	–	–	µA	V_{OH} = 3.5V
Input Capacitance	C_{IN}	–	–	5	pF	
Power Dissipation[2]	P_D				mW	
T-1 Mode						
Random Data						
330 ft.		–	270	305		
655 ft.		–	280	360		
All Ones						
330 ft.		–	350	430		
655 ft.		–	410	480		
PCM30 Mode						
Random Data		–	240	280		
All Ones		–	310	360		
Power Consumption[2]	P_C				mW	
T-1 Mode						
Random Data						
330 ft.		–	300	375		
655 ft.		–	340	410		
All Ones						
330 ft.		–	420	500		
655 ft.		–	500	570		
PCM30 Mode						
Random Data		–	260	300		
All Ones		–	350	400		

Notes: 1. Applies to all signals except TXOUTP, TXOUTN, RXINP and RXINN.
2. Power Consumption = Power dissipated as heat and power used to drive cable.

RECOMMENDED CRYSTAL SPECIFICATION

Parameter	Value
Frequency @ 25°C ±2°C T-1 PCM30	 6.176 MHz 8.192 MHz
Frequency Tolerance @ 25°C	±0.001%
Temperature Stability (0°C - 70°C)	±0.003%
Load Capacitance	13.5 pF
Equivalent Series resistance (Max.)	50 Ω
Motional Capacitance (Min.) T-1 (@ 6.176 MHz) PCM30 (@ 8.192 MHz)	 0.022 pF 0.025 pF
Recommended Aging	2 ppm/year
Shunt Capacitance (Max.) T-1 (@ 6.176 MHz) PCM30 (@ 8.192 MHz)	 6 pF 6 pF
Mode of Operation	Fundamental
Drive Level (Max.)	2.5 mW
Resonance Mode	Parallel

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	36.32	37.34	1.430	1.470
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

6

Rockwell

R8069A
Enhanced T-1/PCM-30 Line Interface Unit (LIU)

INTRODUCTION

The Rockwell R8069A Line Interface Unit (LIU) is a single chip CMOS device that interfaces the Rockwell R8070 T1/CEPT PCM Transceiver to the physical T-1/CEPT PCM30 transmission medium.

The R8069A LIU device contains analog and digital circuits which are based on CMOS technology to implement the line interface function required in ISDN primary rate transmission. The R8069A provides capabilities for 4-wire transmission of image, voice, or data signals; clock extraction; line equalization; bipolar violation detection; jitter accommodation; and AIS (Blue Alarm) generation and detection. In addition, the device operates at 1.544 or 2.048 Mbit/s and meets pulse shape and jitter requirements specified by T-1 or PCM30 standards, respectively.

The R8069A is ideally suited for image, voice, or data transmission required in ISDN primary rate applications. The device is highly integrated and requires virtually no external components.

Internal LIU functions allow system designers to minimize their development cost and easily implement a T-1/PCM30 physical interface to primary rate lines without concern about most of the complex details normally associated with such a design. The R8069A also provides a high level of integration which increases system reliability, reduces space and achieves higher levels of performance and quality.

NEW FEATURES INCLUDE:

- 44-Bit Receive Elastic Store for Up to 40 UI Jitter Accommodation
- Exceeds Latest CEPT Requirement
- Transmit Elastic Store for Alignment of Transmit Data with System Clock
- Standby Mode for Transmitter
- Mode Independent Loopbacks
- Self Generation of Line Rate Clock for Elimination of External Clock Generator or Fall Back if External Clock Lost
- Automatic RCLK Source Selection
- Improved Pulse Shape for Added Margin from Template

FEATURES

- Compatible with T-1 (1.544 Mbit/s) and PCM30 (2.048 Mbit/s)
- Selectable T-1 and PCM30 clock rates
- Implements ISDN primary rate interface
- Directly compatible with Rockwell R8070 T-1/CEPT PCM Transceiver and R8071 ISDN/DMI Link Layer Controller devices
- Independent transmit and receive sections
- Phase locked loop for loop timing applications
- Satisfies T-1 (AT&T Technical Advisory No. 34) and PCM30 (CCITT G.703)
- Provides line equalization for up to 655 feet of 22-gauge plastic insulated (ABAM) cable for T-1
- Transmission/reception of data for up to 1600 feet of cable
- Accommodates pulse shape requirements for 75 Ω and 120 Ω lines in PCM30 application
- Meets jitter requirements specified by T-1 (AT&T Publication 62411, Oct. 1985) and PCM30 (CCITT G.823)
- Intrinsic jitter under 0.05 UI
- Jitter attenuation starts at 2 Hz
- Jitter tolerance above 0.4 UI for jitter frequency from 20 kHz to 100 kHz
- 8-bit TX elastic store for jitter control and attenuation
- 44-bit RX elastic store for jitter control and attenuation
- Provision to bypass RX elastic store
- Master/slave timing option
- Local and remote loop operation
- AIS (Blue Alarm) generation and detection
- Bipolar violation detector
- EXCLK activity detector
- On-chip line drivers
- Analog CMOS technology
- CMOS/TTL compatible inputs and outputs
- Operates from a single +5V supply
- 28-pin plastic dual in-line package (DIP)

Document No. 29300N52 **Product Preview** **Order No. 352**
January 1989

Rockwell

R8070
T1/CEPT PCM Transceiver

INTRODUCTION

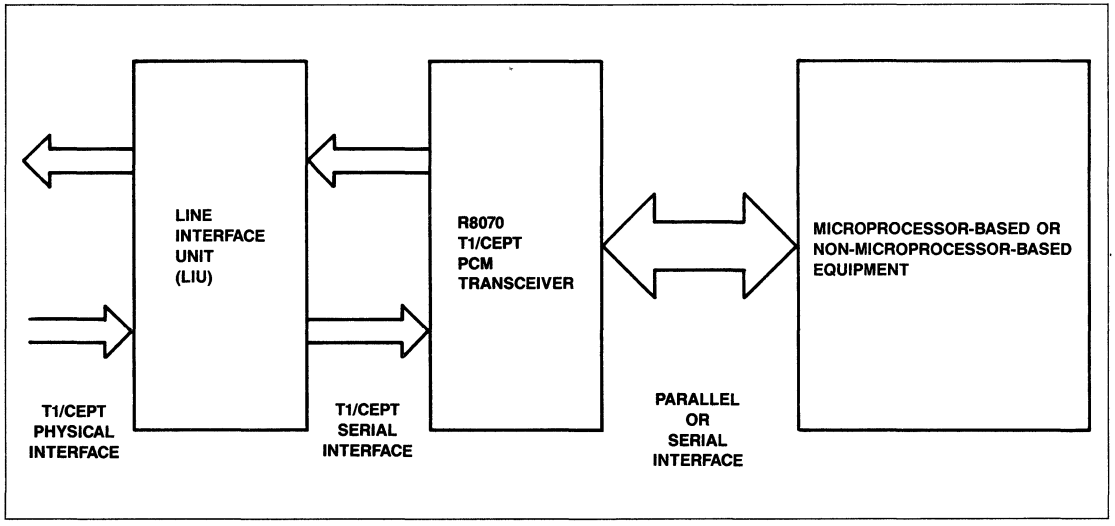
The Rockwell R8070 T1/CEPT PCM Transceiver is a monolithic silicon gate CMOS device designed to implement PCM transmitter and receiver functions applied in primary-rate digital carrier systems worldwide. Both the transmitter and receiver contain appropriate circuitry for synchronization, channel monitoring and signaling extraction.

The R8070 supports CCITT recommendations G.732, G.733 and applicable sections of G.703, as well as AT&T technical advisories on clear channel capability and Extended Superframe Format (ESF). This device provides the interfaces between the multiplexed digital signals of the subscriber loop and the PCM highway in a digital telephone switching system. The device operates from a single power supply of 5 volts and a sampling clock of 1.544 to 2.048 MHz, depending on the mode of operation.

Packaged in a 64-pin QUIP (quad in-line package) or a 68-pin PLCC (plastic leaded chip carrier), the R8070 requires less real-estate and provides added flexibility in system integration and manufacturing. With eleven modes of operation and a serial or parallel data interface, the R8070 finds worldwide application in diverse areas of voice/data communications.

FEATURES

- Implements primary-rate PCM formats:
  — T-carrier T1 (D4), T1 (ESF) and 1/2 T1C synchronous
  — CEPT PCM-30
- Meets CCITT G.732 (2.048 Mbps), G.733 (1.544 Mbps) and applicable sections of G.703
- Supports AT&T technical advisories on Extended Superframe Format and Clear Channel operation with B8ZS coding
- Supports SLC-96 applications
- Single chip receiver and transmitter
- Selectable serial or parallel data interface
- Reframe time less than 10 ms
- Interfaces directly with Rockwell R8071 ISDN/DMI Link Controller
- Available in 64-pin quad in-line (QUIP) and 68-pin plastic leaded chip carrier (PLCC) packages
- Operates from a single +5 Vdc supply
- CMOS/TTL compatible inputs and outputs
- Low power CMOS technology



R8070 Functional Interface

ORDERING INFORMATION

Part Number:
R8070

Temperature
Blank = 0°C to +70°C
E = −40°C to +85°C

Package
P = 64-Pin Plastic QUIP
S = 64-Pin Cerpac QUIP
J = 68-Pin Plastic Leaded Chip Carrier (PLCC)
JC = 68-Pin Ceramic Leaded Chip Carrier (CLCC)

R8070 OPERATING MODE AND INTERFACE SELECTION

The R8070 has eleven modes of operation covering T1 (D1D, D2, D3 and D4), T1 (Extended Superframe Format), T1C, and CEPT PCM-30 formats. Nine modes support T1 formats and two modes support CEPT formats. The mode is selected using M1–M4 to match the required PCM format. Modes may be chosen with or without signaling, and with a choice of zero suppression technique.

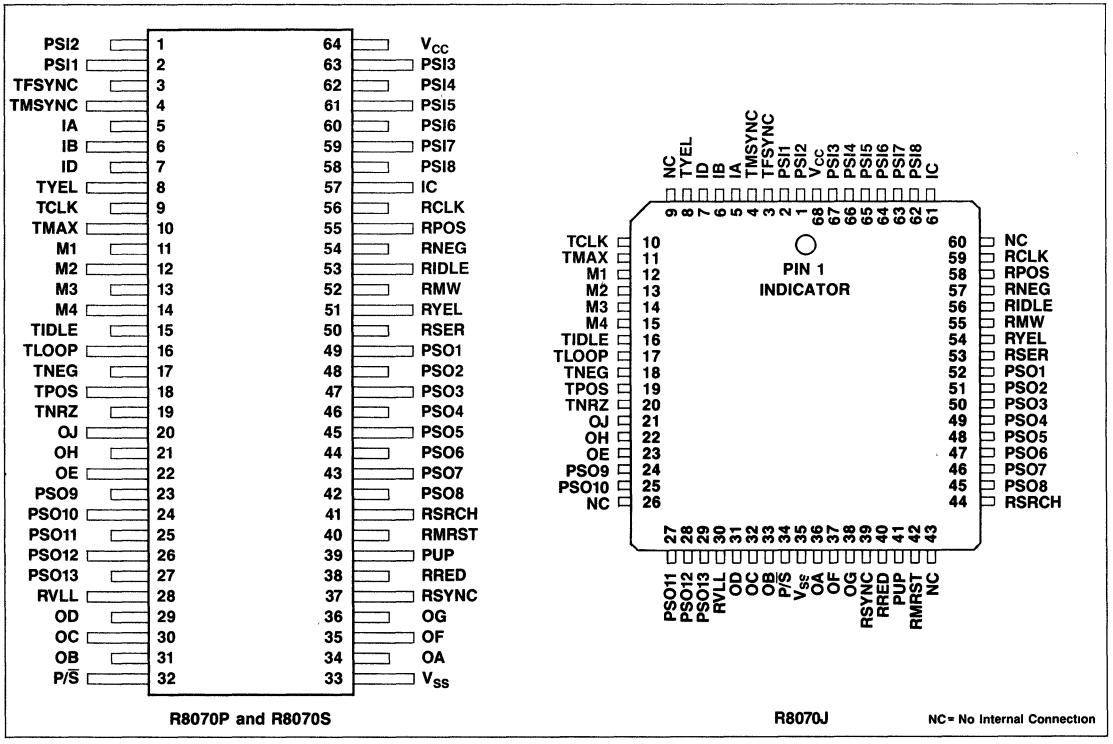
For increased flexibility and lower external part count (no parallel/serial conversion required), a parallel (P/$\overline{S}$ high) or serial (P/$\overline{S}$ low) interface may be selected. The parallel interface may be chosen to match a byte-wide microprocessor bus; the serial interface may be preferred to match an existing interface.

DATA SHEET STRUCTURE

The R8070 pin assignment, general interface and functional block diagrams that apply to both T1 and CEPT formats are shown in the front of the data sheet. The electrical and switching characteristics and packaging information are included in a short common section at the end of this document.

The PCM formats, the R8070 interface signals and R8070 operation in T1 and CEPT environments are described separately to simplify the use of this data sheet. These two major sections are structured similarly and include four subsections:

- The Overview provides an introduction to PCM formats and terminology, and a guide to mode selection.
- The Functional Description gives an overview of the R8070 operation and groups the signals associated with each aspect of PCM transceiver design: channel data, signaling, alarm indication, error reporting, timing and synchronization.



R8070 Pin Assignments

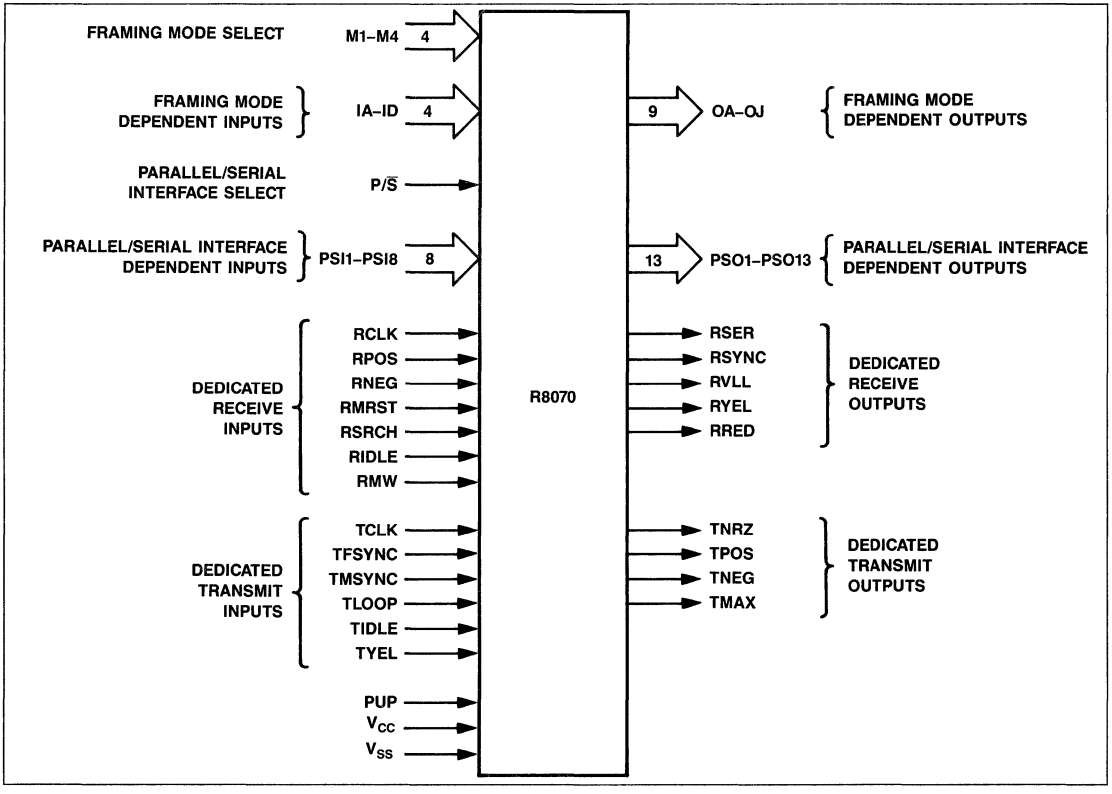
- The Interface Description is arranged so that, having chosen an operating mode (PCM format) and data interface (parallel or serial), the designer can clearly identify the signals available in that configuration. Pin assignments and pin definitions are separately listed with applicable interface and mode. Within each table, the R8070 signals are arranged in three groups:
  1. Dedicated signals whose function is fixed.
  2. Parallel/serial interface dependent signals.
  3. Framing mode dependent signals.
- The Waveforms show major signaling or frame level signals followed by channel/bit level signals.

For more detailed information, see the R8070 T1/CEPT PCM Transceiver Designer's Guide (Order No. 313).

R8070 Operating Mode Selection and Characteristics

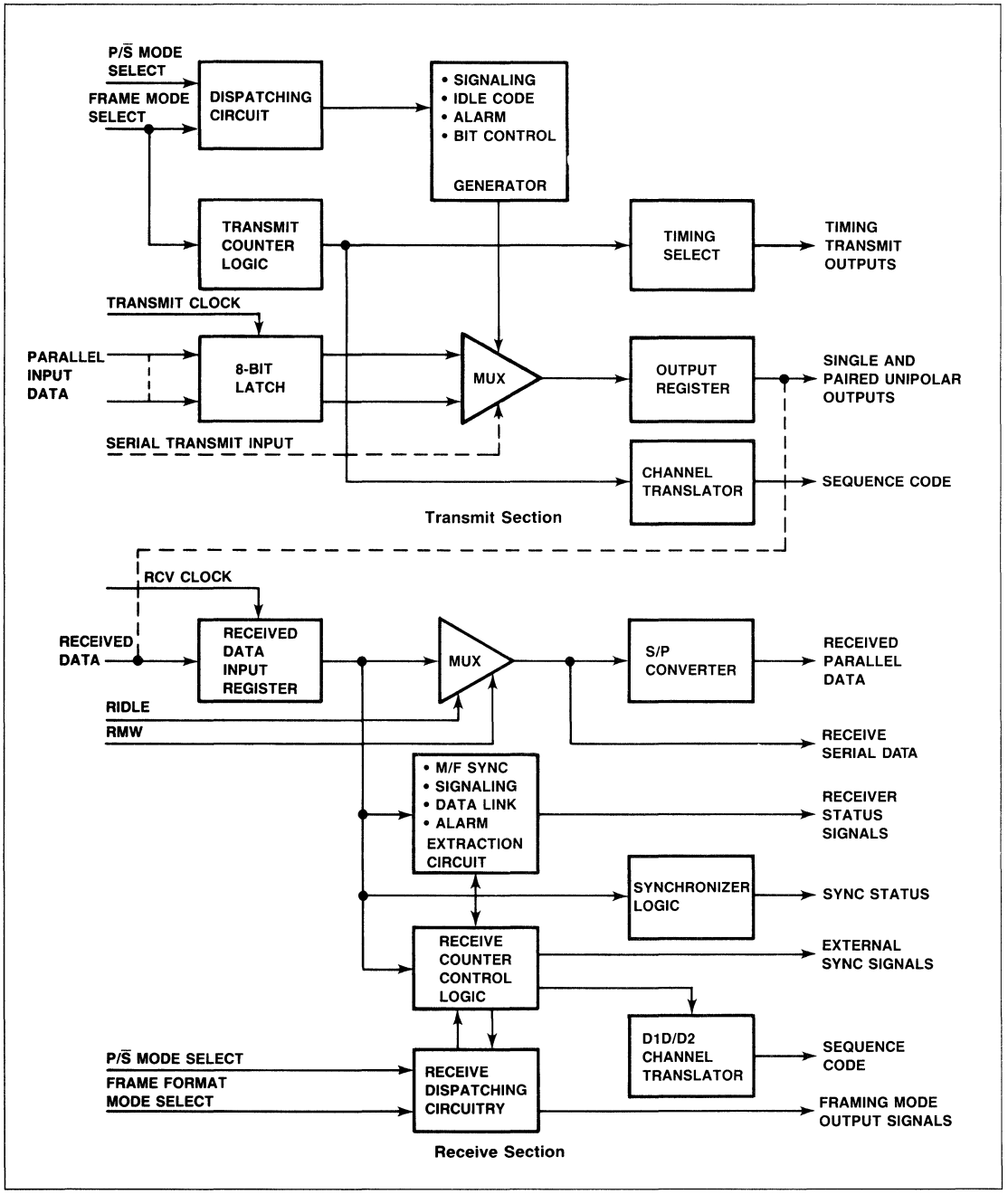
Mode	Data Rate (Mbps)	Bits/Frame	Frames/Multiframe	Signaling	Zero Suppression	Mode Select Lines M1	M2	M3	M4	PCM Format
193S	1.544	193	12	Yes	B8ZS	1	0	1	0	T1 (D4)
193S			12	Yes	B7	0	0	1	0	
193N			4	No	B8ZS	1	1	1	0	
193N			4	No	B7	0	1	1	0	
193E	1.544	193	24	Yes	B8ZS	1	1	1	1	Extended Superframe Format (ESF)
193E			24	Yes	B7	0	1	1	1	
193F			24	Special	B8ZS	1	0	1	1	
197S	1.576	197	12	Yes	Transparent	1	0	0	0	T1C
197N			4	No	Transparent	1	1	0	0	
256S	2.048	256	16	Yes	HDB3	0	0	0	0	CEPT PCM-30
256N			2	No	HDB3	0	1	0	0	

Notes: B7: Bit 7 is forced to a 1 (stuffed) on an otherwise all zero channel. HDB3: High Density Bipolar 3-zero maximum.
B8ZS: Bipolar 8-zero substitution. Transparent: No zero suppression or substitution.



R8070 Interface Signals — General

R8070 OVERVIEW (Cont'd)



R8070 Functional Block Diagram

T1 OVERVIEW

T1 is a PCM format for time-division multiplexing 24 voice (telephone) or data circuits onto a single transmission path. This path is normally a dual twisted-pair cable with digital repeaters at intervals of 6000 feet.

T1 presently has two major formats; the older D4 format and the emerging Extended Superframe Format (ESF). The major differences between them are in the signaling format and the definition of the F-bit pattern. Both formats, as well as their derivatives, are supported by the R8070.

In addition, there is a hierarchy of PCM formats within the T-carrier system that defines further time-division multiplexing of multiple T1 lines, to produce T1C (two T1 lines), T2 (four T1 lines), and so on. These higher level formats are used for long-haul transmission via satellite or microwave links. The R8070 provides specific support of the T1C format, in addition to T1.

T1 FORMATS

Basic T1 (D4)

Prior to transmission, each voice circuit is sampled at 8 kHz using an 8-bit μ-law companding analog-to-digital converter. The resulting 64 kbps (8 bits x 8 kHz) signal is time-division multiplexed with 23 other sampled channels to produce a frame of 192 bits (24 channels x 8 bits). An extra bit (193rd bit or F-bit) is inserted at the beginning of each frame to define the frame boundaries. Since each voice circuit is sampled at 8 kHz, the frame rate is 125 μs. To transmit 193 bits in 125 μs requires a bit rate of 1.544 Mbps, hence the standard T1 clock frequency of 1.544 MHz.

Signaling Data. Signaling data, such as on-hook and off-hook conditions, dialing digits, call progress, etc., associated with each voice circuit is transmitted within the voice channel itself. This is known as associative signaling, as opposed to common channel signaling, where a single (common) channel is dedicated to carry the signaling data for all the voice circuits within a T1 link, for example.

The signaling data, known as A- and B-bits, is conveyed in the 8th bit position (least significant bit) of each channel within frames 6 (A-bit) and 12 (B-bit). This signaling method is also known as "robbed-bit" signaling since the A- and B-bits actually displace the original LSB of the voice signal, causing a slight, but insignificant, error in the received signal.

The requirement for associated signaling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames.

To recap, the PCM structure consists of: a multiframe of 12 frames; a frame of 24 channels, plus an F-bit; and 8 bits to per channel, where a channel is equivalent to one voice circuit or one 64 kbps data circuit.

This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or Fs bit (signaling framing bit). The Ft bit carries a pattern of alternating 0s and 1s (101010) that defines the frame boundaries so that one channel may be distinguished from another. The Fs bit carries a pattern of 001110 and defines the multiframe boundaries so that one frame may be distinguished from another, in particular, frame 6 and frame 12 may be identified for the recovery of signaling bits.

Alarms and Error Conditions. In addition to voice and signaling data, T1 defines several alarm and error conditions that must be monitored and reported. The principal alarms are:

1. Red Alarm
2. Yellow Alarm

A Red Alarm is produced by a receiver to indicate that it has lost frame alignment. A Yellow Alarm is returned to the transmitting terminal to report a loss of frame alignment at the receiving terminal. Normally, a T1 terminal will use the receiver's Red Alarm to request that a Yellow Alarm be transmitted.

The principal error conditions are:

1. Loss of carrier
2. Bipolar violation
3. Fs bit error
4. Ft bit error

A loss of carrier means that received data was zero for 31 consecutive bits. A bipolar violation is a failure to meet the Alternate Mark Inversion (AMI) line code of T1. AMI dictates that 1s (marks) are transmitted alternately as positive or negative pulses; zeros are transmitted as zero volts.

Clock Recovery. In order to guarantee adequate clock recovery from the received data, a minimum "ones density" must be observed. One of two methods may be used; B8ZS or bit-7 stuffing. B8ZS represents a group of 8 zeros by a predefined code that includes intentional bipolar violations. At the receiver, the code is recognized and the original 8 zeros are restored. The older method of bit-7 stuffing forces bit 7 to a 1 in an otherwise all zero channel. This forced 1 is not coded as a bipolar violation and the original data cannot be recovered by the receiver.

The R8070 supports all major requirements of the T1 system, including channel data recovery, signaling, alarm indication, error reporting and both methods of zero suppression to satisfy the ones density requirement.

Extended Superframe Format (ESF)

In Extended Superframe Format, the multiframe structure is extended to 24 frames from the 12 frames used in D4. The frame and channel structure is the same in both formats. Robbed-bit signaling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit), and frame 24 (D-bit).

T1 OVERVIEW (Cont'd)

The F-bit pattern of ESF contains three functions:

1. Framing Pattern Sequence (FPS) which defines the frame and multiframe boundaries.
2. Facility Data Link (FDL) which allows data such as error performance to be passed within the T1 link
3. Cyclic Redundancy Check (CRC) which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm

The R8070 supports all major requirements of ESF, including channel data recovery, signaling, alarm indication, error reporting and both methods of zero suppression to satisfy the ones density requirement.

T1C Mode 1 Synchronous

The frame structure of T1C is the same as basic T1 but 4 extra (link) bits are included in each of the two multiplexed T1 lines at the end of channel 6, 12, 18 and 24 (where the link bit follows the F-bit). The bit rate of T1C is 3.152 Mbps. Two R8070s can be used, each clocked at 1.576 MHz, to configure a T1C multiplexer/demultiplexer.

Summary

The three major T1 formats supported by R8070 are:

Format	Modes
1. Basic T1 (D4)	193S, 193N
2. Extended Superframe Format (ESF)	193E, 193F
3. T1C Mode 1 Synchronous	197S, 197N

T1 MODES DESCRIPTION

The R8070 T1 operating mode is selected by configuring the four encoded Mode Select input lines (M1–M4) to one of nine T1 modes (see T1 Mode Selection Table).

Standard T1 (D4) Modes

193S Mode. The 193S mode implements the standard T1 PCM format at 1.544 Mbps with 12 frames per multiframe, sometimes referred to as D4 (channel bank designation). A and B robbed-bit signaling is included. The pseudo-random channel numbering of D1D and D2 is supported, as well as the sequential numbering of D3 and D4. There are 193 bits per frame.

The Ft and Fs bit patterns are generated by the R8070 transmitter and recovered by the receiver. The Fs pattern is included in the receiver synchronization algorithm for improved immunity against Ft-imitating signals such as digital milliwatt. Robbed-bit signaling can be disabled to allow the use of the 193S mode in nonsignaling applications and thus retain its superior framing properties.

To satisfy the "ones density" requirement, either B8ZS or bit-7 stuffing techniques can be selected. Zero suppression may be disabled to allow transparent operation.

193N Mode. The 193N mode implements standard T1 PCM format at 1.544 Mbps with 4 frames per multiframe. Robbed-bit signaling is omitted. There are 193 bits per frame.

The transmitter generates the Ft pattern but not the Fs pattern, which may be externally supplied. The receiver does not use the Fs pattern for synchronization but reports the Fs data

This mode may be used in point-to-point communications where no robbed-bit signaling is required and the standard Fs pattern cannot be used If the standard Fs pattern can be used, then 193S mode provides more reliable synchronization.

To satisfy the "ones density" requirement, either B8ZS or bit-7 stuffing techniques can be selected. Zero suppression may be disabled to allow transparent operation.

Extended Superframe Format T1 Modes

193E Mode. The 193E mode implements the Extended Superframe Format of T1 at 1.544 Mbps with 24 frames per multiframe, sometimes referred to as ESF or Fe. A, B, C and D robbed-bit signaling is implemented. There are 193 bits per frame.

The transmitter generates the Framing Pattern Sequence (FPS), computes the Cyclic Redundancy Check (CRC) checksum, and accepts the Facility Data Link (FDL) bits, then combines them into the F-bit stream. The receiver recovers the FPS to establish framing, checks the CRC against the data (reporting any errors), and presents the FDL data bits.

To satisfy the "ones density" requirement, either B8ZS or bit-7 stuffing techniques can be selected. Zero suppression may be disabled to allow transparent operation.

193F Mode. The 193F mode is identical to 193E mode, but robbed-bit signaling is omitted. This mode is convenient for common channel signaling, and some additional timing signals are provided for this purpose. There are 193 bits per frame.

The zero suppression technique is pre-selected as B8ZS but may be disabled to allow transparent operation.

T1C Modes

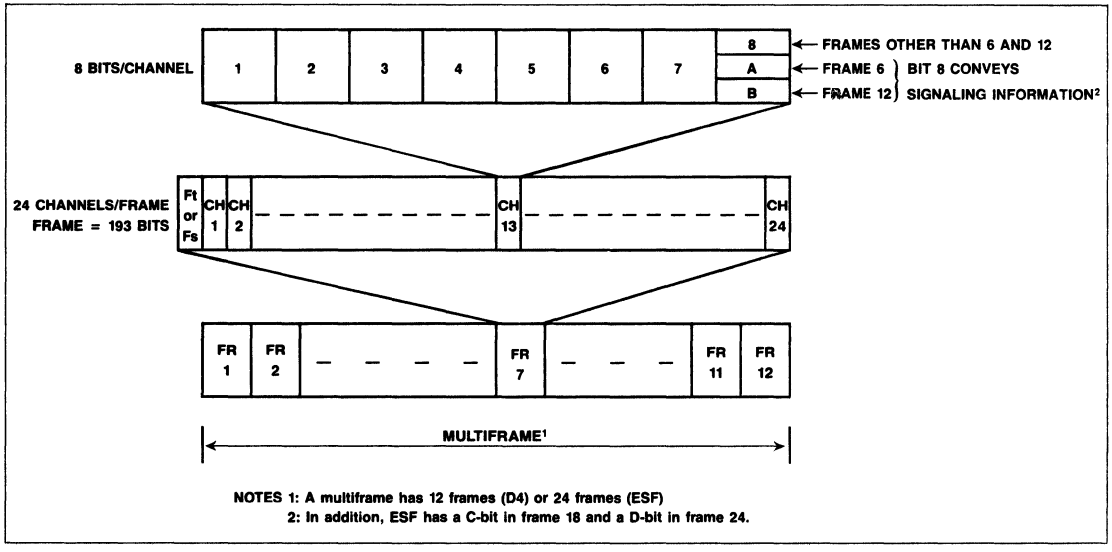
197S Mode. The 197S mode implements one-half of the T1C PCM format at 1.576 Mbps with 12 frames per multiframe. Two R8070s can be used with additional logic to provide T1C, mode 1 synchronous, multiplex and demultiplex functions. A and B robbed-bit signaling is supported. 197S framing is identical to that of 193S, but 4 link bits per frame are added. There are 197 bits per frame

No zero suppression is used in 197S (transparent).

197N Mode. The 197N mode implements one-half of the T1C PCM format at 1.576 Mbps with 4 frames per multiframe. Two R8070s can be used with additional logic to provide T1C, mode 1 synchronous, multiplex and demultiplex functions. Robbed-bit signaling is omitted. 197N framing is identical to that of 193N, but 4 link bits per frame are added. There are 197 bits per frame.

No zero suppression is used in 197N (transparent).

T1 OVERVIEW (Cont'd)



NOTES 1: A multiframe has 12 frames (D4) or 24 frames (ESF)
2: In addition, ESF has a C-bit in frame 18 and a D-bit in frame 24.

T1 PCM Format

T-Carrier Hierarchy

Digital Signal Number	Number of Voice Circuits	Bit Rate (Mbps)
DS-1	24	1.544
DS-1C	48	3.152
DS-2	96	6.312
DS-3	672	44.736
DS-4	4032	274.176

F-bit Assignment—D4 Format

Frame Number	Bit Number	F-Bit	
		F_s	F_t
1	0	—	1
2	193	0	—
3	386	—	0
4	579	0	—
5	772	—	1
6	965	1	—
7	1158	—	0
8	1351	1	—
9	1544	—	1
10	1737	1	—
11	1930	—	0
12	2123	0	—

F_s = Signaling Framing (Sequence ...001110...)
F_t = Terminal Framing (Sequence ...101010...)

F-bit Assignment—Extended Superframe Format

ESF Frame Number	ESF Bit Number	F-Bit Assignment		
		FPS	FDL	CRC
1	0	—	m	—
2	193	—	—	CB1
3	386	—	m	—
4	579	0	—	—
5	772	—	m	—
6	965	—	—	CB2
7	1158	—	m	—
8	1351	0	—	—
9	1544	—	m	—
10	1737	—	—	CB3
11	1930	—	m	—
12	2123	1	—	—
13	2316	—	m	—
14	2509	—	—	CB4
15	2702	—	m	—
16	2895	0	—	—
17	3088	—	m	—
18	3281	—	—	CB5
19	3474	—	m	—
20	3667	1	—	—
21	3860	—	m	—
22	4053	—	—	CB6
23	4246	—	m	—
24	4439	1	—	—

FPS—Framing Pattern Sequence (...001011...)
FDL—4 kbps Facility Data Link (message bits m)
CRC—CRC-6 Cyclic Redundancy Check (check bits CB1–CB6)

6

T1 FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

The transmit section of the R8070 provides the data formatting, signaling and alarm indication functions required for PCM transmission according to CCITT G.733 and applicable sections of G.703. The AT&T technical advisories on Clear Channel and Extended Superframe Format are also supported.

PCM Channel Data

Data Input. Data is clocked into the transmitter either serially (via TSER) or in parallel form (via T1-T8), on the rising edge of the transmitter clock (TCLK). The externally provided TCLK normally has a rate of 1.544 MHz for T1 and 1.576 MHz for T1C.

For a serial data interface, Transmit Sequence signals (TSQ1-TSQ5) specify the binary value of the next channel to be sampled. These signals, which can be used for control of channel banks, may be advanced by one bit time using Transmit Sequence Advance (TSA). The sequence of channel codes may be selected to meet D1D (1, 13, 2, 14, 3, etc.), D2 (12, 13, 1, 17, 5, etc.) or D3 and D4 (1, 2, 3, 4, 5, etc.), using D1D and D2 inputs.

For a parallel data interface, timing signals are output at the channel rate (TCHCLK) and at the frame rate (TCHSYNC) for clocking data interface circuits.

Data Output. The serial PCM data is clocked out of the transmitter on the rising edge of TCLK and is available on two outputs simultaneously (TNRZ, TPOS and TNEG). TNRZ provides a standard, nonreturn-to-zero (NRZ) TTL level version of the data. TPOS and TNEG carry the same NRZ TTL level data as TNRZ except that the 1s are routed alternately to TPOS and TNEG. This facilitates the translation into the Alternate Mark Inversion (AMI) line code, where 1s are represented alternately as positive and negative pulses.

Loopback. The outputs TPOS and TNEG may be internally connected to RPOS and RNEG (TLOOP high) for loopback testing. During loopback, the external TPOS and TNEG carry a continuous stream of 1s; TNRZ is unaffected.

Idle Code. Idle code (01111111) may be substituted in place of the normal channel data, on a channel-by-channel basis, using TIDLE.

B8ZS Encoding and B7 Stuffing. B8ZS encoding is handled automatically by the R8070. The entire data stream, including F (and L) bits, is scanned for an occurrence of 8 consecutive zeros. Any such occurrence is replaced by the appropriate B8ZS code. The B8ZS encoder may be disabled by connecting RPOS to RNEG (and using an NRZ form of input data). This invokes the transparent mode where zeros are transmitted as zeros, regardless of the 1s density. This may be used for testing or for systems that guarantee 1s density by other means. B8ZS encoding applies only to the TPOS and TNEG outputs; TNRZ is unaffected.

In B7 stuffing, bit 7, the next least significant bit, is forced to a 1 if the channel data would otherwise be all 0s. No extra bit is "stuffed". The F and L bits are unaffected. B7 stuffing is applied to outputs TPOS/TNEG and TNRZ.

Frame and Multiframe Formatting

The transmitter contains frame and multiframe counters which maintain the correct PCM format by inserting Ft and Fs bits (T1 modes with signaling; 193S, 197S), Ft (T1 nonsignaling modes; 193N, 197N) and Framing Pattern Sequence (FPS), Facility Data Link (FDL) bits and Cyclic Redundancy Check (CRC) bits (Extended Superframe Format).

The required F-bit is generated by the R8070 and output on TFGEN. The input TFSIG is sampled to obtain the F-bit. Normally, TFGEN would be connected directly to TFSIG, but externally supplied F-bit patterns may be multiplexed into TFSIG, if required.

The frame counter may be reset to bit 1, channel 1 (TFSYNC high), and the multiframe counter may be reset to frame 1 (TMSYNC high).

T1 Operating Mode Selection and Characteristics

Mode	Data Rate (Mbps)	Bits/Frame	Frames/Multiframe	Signaling	Zero Suppression	Mode Select Lines M1	M2	M3	M4	PCM Format
193S	1.544	193	12	Yes	B8ZS	1	0	1	0	T1 (D4)
193S			12	Yes	B7	0	0	1	0	
193N			4	No	B8ZS	1	1	1	0	
193N			4	No	B7	0	1	1	0	
193E	1.544	193	24	Yes	B8ZS	1	1	1	1	Extended
193E			24	Yes	B7	0	1	1	1	Superframe
193F			24	Special	B8ZS	1	0	1	1	Format (ESF)
197S	1 576	197	12	Yes	Transparent	1	0	0	0	T1C
197N			4	No	Transparent	1	1	0	0	

Notes: B7. Bit 7 is forced to a 1 (stuffed) on an otherwise all zero channel.
B8ZS· Bipolar 8-zero substitution.
Transparent. No zero suppression or substitution.

T1 FUNCTIONAL DESCRIPTION (Cont'd)

Signaling and Link Data

Robbed-bit Signaling

193S and 197S Modes. The R8070 implements robbed bit signaling by inserting an A signaling bit into bit 8 of each channel in frame 6, and a B signaling bit into bit 8 of each channel in frame 12. These bits replace the original LSB of the channel data. The A and B signaling bits are input via TA and TB or via TSER (selected by TSIGMD). Robbed-bit signaling may be defeated, if not required, by connecting TA and TB to T8 for the Parallel Interface, or by selecting TSER as the source (and not inserting signaling bits) for the Serial Interface.

193N and 197N Modes. No signaling is used in this mode. The standard Fs bit pattern is not generated, but an external Fs pattern may be used, e.g., for SLC-96 applications. See S-bit signaling.

193E Mode. The R8070 implements robbed-bit signaling by inserting an A signaling bit into bit 8 of every channel in frame 6, B-bits in frame 12, C-bits in frame 18 and D-bits in frame 24. These bits replace the original LSB of the channel data. The A- and C-bits are input via TA(C); the B- and D-bits are input via TB(D). TSIGSEL or TSIGSQ may be used to gate the appropriate bits to the signaling inputs.

193F Mode. ABCD signaling is not used. Instead, this mode is suitable for common channel signaling schemes where one channel (e.g., channel 24) is dedicated for interoffice signaling.

Link Data

193E and 193F Modes. In Extended Superframe Format, half of the F-bits are allocated for a Facility Data Link at 4 kbps. TLINK is the input for link data, which may be clocked externally by TLCLK.

197N and 197S Modes. In the T1C modes there are 4 link bits (L-bits) in addition to the normal 193 bits in a T1 frame, making a total of 197 bits. These L-bits follow channels 6, 12, 18 and 24 (the L-bit follows the F-bit). The L-bits are input via TLINK, using TLCLK to clock external circuitry. The input data rate is 32 kbps. The link data reappears on TFGEN after being sampled at TLINK, and is then input to TFSIG. If TFGEN is not connected directly to TFSIG, then the link data must be multiplexed into TFSIG by the user, rather than input via TLINK.

S-Bit Signaling

193N and 197N Modes. In 193N and 197N modes, the R8070 does not provide the standard Fs bit pattern. Instead, Fs (S-bit) may be externally supplied via TSBIT using TSBCLK to clock external circuits. The Fs bit will be inserted into the data stream at the appropriate time, but does not appear on TFGEN.

Alarms

A Yellow Alarm is transmitted, with a format appropriate to the selected mode, when requested by TYEL. In 193S mode, two formats are supported (bit 2 = 0 or S-bit of frame 12 = 1). These are selected by YELMD for both the transmitter and receiver.

Clocks

The R8070 provides clock signals at the bit, channel, frame and multiframe rate to facilitate data clocking and timing of external circuitry.

Rate	Clock	Description
Bit	TCLK	Same period as bit time. Rising edge clocks all inputs and outputs.
Channel	TCHCLK	T1-T8 sampled at the rising edge.
Frame	TCHSYNC	High for sampling of channel 24.
	TLCLK	Indicates TLINK sampling.
	TSBCLK	Indicates TSBIT sampling.
Multiframe	TMAX	High for sampling of the next to last bit in multiframe.
	TFR24	High for sampling of frame 24 (193F).

RECEIVE SECTION

The receive section of the R8070 provides the synchronization, signaling and alarm indication functions required for reception of PCM data formatted according to CCITT G.733 and applicable sections of G.703. The AT&T technical advisories on Clear Channel and Extended Superframe Format are also supported.

PCM Channel Data

Data Input. Received unipolar data on RPOS, derived from the received positive pulses, and RNEG, derived from the received negative pulses, is clocked into the receiver on the rising edge of RCLK.

Data Output. The received data is clocked out on the rising edge of RCLK and is available in serial form on RSER and also, if a Parallel Interface is selected, in parallel (8-bit channel) form on R1-R8. The parallel output R8 is also available for the Serial Interface, so that robbed signaling bits may be recovered.

For a serial data interface, Receive Sequence signals (RSQ1-RSQ5) specify the binary value of the current channel. The sequence may be retarded by one bit-time using Receive Sequence Retard (RSR). If RSHIFT is high, the sequence is "shifted" (upper bank and lower bank channel numbers are interchanged), so that channel 1 becomes 13, 2 becomes 14, and so on. F-bit and L-bit codes remain the same.

For a parallel data interface, timing signals are provided at the channel rate (RCHCLK) and the frame rate (RCHSYNC) for clocking data interface circuits. RWIHBT is high for 2 bit times to "cover" the change of data on R1-R8. This may be used to inhibit the write signal for external memory.

Loopback. Under control of TLOOP, the normal external inputs on RPOS and RNEG may be replaced with an internal loopback to the internal TPOS and TNEG. When switching in and out of loopback, resynchronization will usually take place because the two signals will not normally have identical framing.

T1 FUNCTIONAL DESCRIPTION (Cont'd)

Idle and Digital Milliwatt Codes. The normal received data may be replaced, on a channel-by-channel basis, either with Idle code (using RIDLE) or with digital milliwatt (using RMW).

B8ZS Decoding and B7 Stuffing. B8ZS decoding is handled automatically by the R8070. The incoming data stream is scanned for occurrences of the B8ZS code. These are replaced with 8 zeros, thus restoring the original data. Both serial (RSER) and parallel (R1-R8) data outputs include B8ZS corrections.

Bit 7 stuffing produces a forced error (which is acceptable for a voice channel, but not data), so the receiver cannot recover the original data.

Synchronization

The serial bit stream at RPOS and RNEG is examined by the synchronizer, and the framing pattern is located through a five-stage process that eliminates erroneous bit candidates. Synchronization is achieved in less than 10 ms.

A generalized form of the synchronization algorithm is described in the R8070 Designer's Guide (Order No. 313). After a power-up reset (PUP low for at least 16 cycles), the receiver begins to search for frame and multiframe alignment. When synchronization is achieved, the receiver monitors the frame and multiframe alignment signals for errors. A Red Alarm is generated (RRED high) if frame alignment is lost. The criterion for loss of frame alignment in all T-carrier modes is "2 out of 5" errors in the Ft pattern.

The receiver can be forced to restart a synchronization search (RMRST high) or to skip a bit while synchronized (RSRCH low).

D1D and D2 high prevents resynchronization after loss of frame alignment. The sequential channel assignment of D4 is assumed for RSQ1-RSQ5 and TSQ1-TSQ5. This mode of operation may be used during testing.

Signaling and Link Data

Robbed-bit Signaling

193S and 197S Modes. The A and B signaling bits may be recovered from the parallel output R8, which is always available regardless of whether a Serial or Parallel Interface is selected. RSIG is high for the duration of frame 6 and frame 12, which contain the A- and B-bits, respectively. In addition, RSIGSQ rising edge indicates the start of frame 6, and the falling edge indicates the start of frame 12. These two timing signals allow the external circuitry to recover the A and B signaling bits. RSBIT takes the value of the last received Fs (S-bit). RSBCLK rising edge provides a convenient clock for RSBIT and RSIGSQ, as it succeeds them by one bit time.

193N and 197N Modes. No robbed-bit signaling is used in these modes. See S-bit signaling.

193E Mode. The A, B, C and D signaling bits may be recovered from the parallel output R8, which is always available, regardless of whether a Serial or Parallel Interface is selected. RSIG is high for the duration of frames 6, 12, 18 and 24, which contain the A-, B-, C- and D-bits, respectively. These bits may be distinguished by examining RSIGBD and RSIGCD. RSBCLK occurs one bit time after these signals and thus provides a convenient clock.

193F Mode. Robbed-bit signaling is not used in this mode. If common channel signaling is employed, the signaling information is contained in a data channel and is recovered in the same way as the channel data.

Link Data

193E and 193F Modes. The 4 kbps Facility Data Link bits, contained within the F-bit structure of the Extended Superframe Format, are recovered at RLINK using RLCLK as a clock.

197N and 197S Modes. The four link bits per frame of the T1C mode are recovered at RLINK with RLCLK as a clock.

S-bit Signaling

193N and 197N Modes. In 193N and 197N modes, the user-supplied S-bits (Fs) are recovered at RSBIT with RSBCLK as a clock. In SLC-96 applications, which use the Fs bit for signaling, an input RS96E is provided which locks the currently received Fs pattern, thus maintaining Fs dependent signals such as RSIG, RSIGSQ and RSBCLK.

Alarms

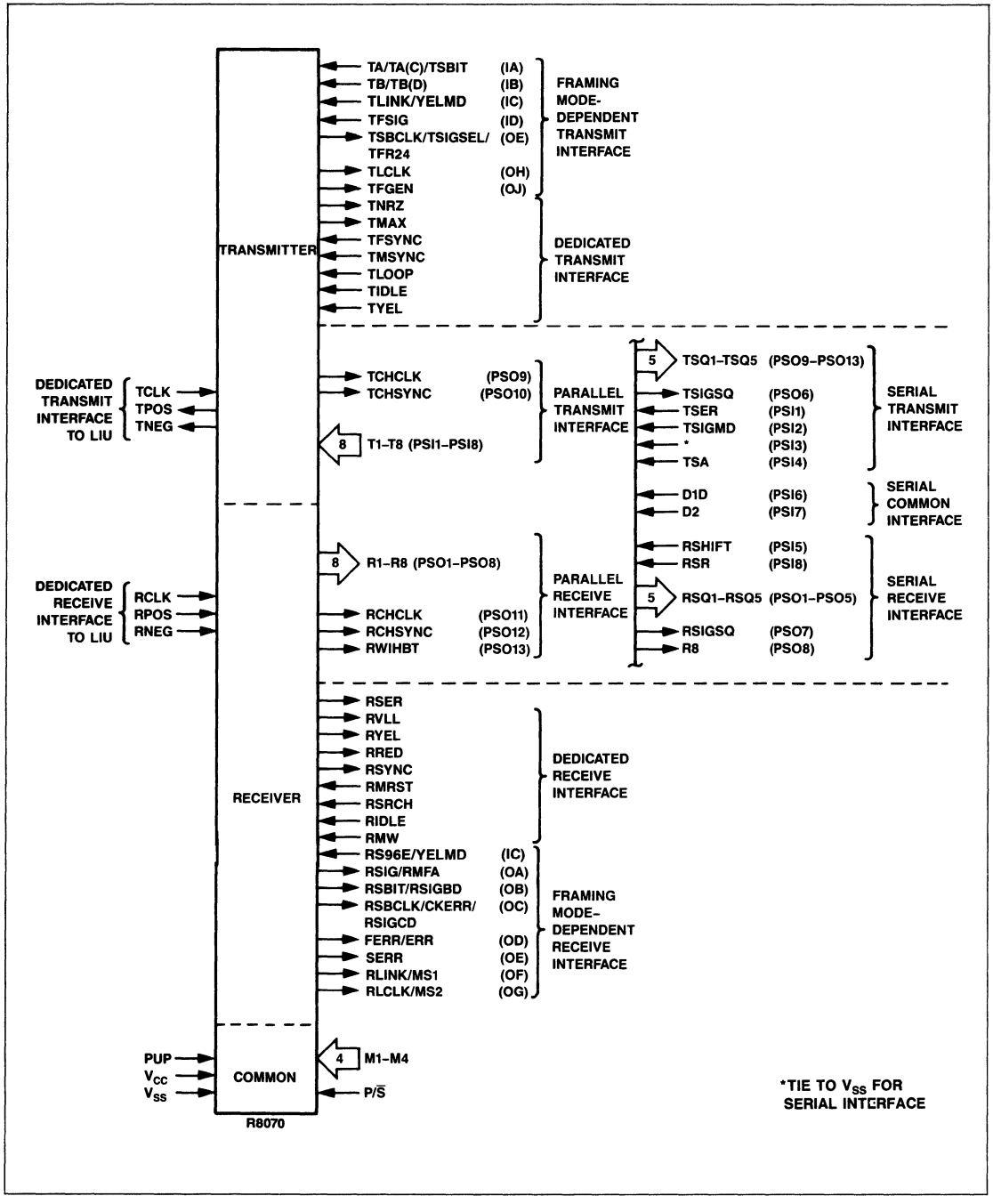
Name	Mode	Alarm Indication
RRED	All	Loss of frame alignment.
RYEL	All	Yellow Alarm.
ERR	193E	FPS (Framing) or CRC error.
FERR	All but 193E	Frame alignment error.
CKERR	193F	CRC error.
SERR	193S, 197S	S-bit error.
RVLL	All	Bipolar violation, Loss of carrier.

Clocks

The R8070 provides clock signals at the bit, channel, frame and multiframe rate to facilitate data clocking and timing of external circuitry.

Rate	Clock	Description
Bit	RCLK	Same period as bit time. Rising edge clocks all inputs and outputs.
Channel	RCHCLK RWIHBT	R1-R8 changes at the rising edge. Memory-write inhibit at R1-R8 change.
Frame	RCHSYNC RLCLK	High for output of channel 24. Indicates RLINK data bit ready.
Multiframe	RSYNC RMFA	High for first F-bit of multiframe. High during frame 24 (193F).

T1 INTERFACE DESCRIPTION



R8070 Input/Output Signals — T1 Modes

T1 INTERFACE DESCRIPTION (Cont'd)

Pin Assignments—Dedicated Signals

Pin Name/Symbol	I/O	Pin No. QUIP	Pin No. PLCC	Signal Name
TCLK	I	9	10	Transmit Clock
TFSYNC	I	3	3	Transmit Frame Sync
TMSYNC	I	4	4	Transmit Multiframe Sync
TLOOP	I	16	17	Transmit Loop
TIDLE	I	15	16	Transmit Idle
TYEL	I	8	8	Transmit Yellow Alarm
TPOS	O	18	19	Transmit Unipolar Positive
TNEG	O	17	18	Transmit Unipolar Negative
TNRZ	O	19	20	Transmit Non-Return-to-Zero
TMAX	O	10	11	Transmit Maximum
RCLK	I	56	59	Receive Clock
RPOS	I	55	58	Receive Unipolar Positive
RNEG	I	54	57	Receive Unipolar Negative
RIDLE	I	53	56	Receive Idle
RMW	I	52	55	Receive Milliwatt
RMRST	I	40	42	Receive Master Reset
RSRCH	I	41	44	Receive Search
RSER	O	50	53	Receive Serial Data
RSYNC	O	37	39	Receive Sync
RVLL	O	28	30	Receive Bipolar Violation, Loss of Carrier
RYEL	O	51	54	Receive Yellow Alarm
RRED	O	38	40	Receive Red Alarm
M1	I	11	12	Framing Mode Select 1
M2	I	12	13	Framing Mode Select 2
M3	I	13	14	Framing Mode Select 3
M4	I	14	15	Framing Mode Select 4
P/$\overline{S}$	I	32	34	Parallel/Serial Interface Select
PUP	I	39	41	Power-Up
V_{CC}	I	64	68	+5V Power
V_{SS}	I	33	35	Ground

Pin Assignments—Parallel/Serial Interface-Dependent Signals

Pin Name	I/O	Pin No. QUIP	Pin No. PLCC	Parallel Interface (P/$\overline{S}$ = High) Symbol	Parallel Interface (P/$\overline{S}$ = High) Signal Name	Serial Interface (P/$\overline{S}$ = Low) Symbol	Serial Interface (P/$\overline{S}$ = Low) Signal Name
PSI1	I	2	2	T1	Transmit Channel Data Bits 1–8	TSER	Transmit Serial
PSI2	I	1	1	T2		TSIGMD	Transmit Signaling Mode
PSI3	I	63	67	T3		—	See Note 1
PSI4	I	62	66	T4		TSA	Transmit Sequence Advance
PSI5	I	61	65	T5		RSHIFT	Receive Shift
PSI6	I	60	64	T6		D1D	D1D Channel Sequence Select
PSI7	I	59	63	T7		D2	D2 Channel Sequence Select
PSI8	I	58	62	T8		RSR	Receiver Sequence Retard
PSO1	O	49	52	R1	Receive Channel Data Bits 1–8	RSQ1	Receive Sequence Code Bits 1–5
PSO2	O	48	51	R2		RSQ2	
PSO3	O	47	50	R3		RSQ3	
PSO4	O	46	49	R4		RSQ4	
PSO5	O	45	48	R5		RSQ5	
PSO6	O	44	47	R6		TSIGSQ[2]	Transmit Signaling Square Wave
PSO7	O	43	46	R7		RSIGSQ[2]	Receive Signaling Square Wave
PSO8	O	42	45	R8		R8[2]	Receive Data Bit 8
PSO9	O	23	24	TCHCLK	Transmit Channel Clock	TSQ1	Transmit Sequence Code Bits 1–5
PSO10	O	24	25	TCHSYNC	Transmit Channel Sync	TSQ2	
PSO11	O	25	27	RCHCLK	Receive Channel Clock	TSQ3	
PSO12	O	26	28	RCHSYNC	Receive Channel Sync	TSQ4	
PSO13	O	27	29	RWIHBT	Receive Write Inhibit	TSQ5	

Notes:
1. Not applicable to T1 modes; tie to GND
2. Different signal than CEPT modes

T1 INTERFACE DESCRIPTION (Cont'd)

Pin Assignments—Framing Mode-Dependent Signals

Pin Name	I/O	Pin No.		193N Mode		193S Mode	
		QUIP	PLCC	Symbol	Signal Name	Symbol	Signal Name
IA	I	5	5	TSBIT	Transmit S-Bit	TA	Transmit A Signaling
IB	I	6	6	—	See Note 1	TB	Transmit B Signaling
IC	I	57	61	RS96E	Receive SLC-96 Enable	YELMD	Yellow Alarm Mode
ID	I	7	7	TFSIG	Framing-Bit Signal	TFSIG	Framing-Bit Signal
OA	O	34	36	RSIG	Receive Signaling Frame	RSIG	Receive Signaling Frame
OB	O	31	33	RSBIT	Receive S-Bit	RSBIT	Receive S-Bit
OC	O	30	32	RSBCLK	Receive S-Bit Clock	RSBCLK	Receive S-Bit Clock
OD	O	29	31	FERR	Framing Error	FERR	Framing Error
OE	O	22	23	TSBCLK	Transmit S-Bit Clock	SERR	S-Bit Errors
OF	O	35	37	MS1	Master State Sequence Code, Bit 1	MS1	Master State Sequence Code, Bit 1
OG	O	36	38	MS2	Master State Sequence Code, Bit 2	MS2	Master State Sequence Code, Bit 2
OH	O	21	22	—	See Note 2	—	See Note 2
OJ	O	20	21	TFGEN	Framing-Bit Generator	TFGEN	Framing-Bit Generator

Pin Name	I/O	Pin No.		193F Mode		193E Mode	
		QUIP	PLCC	Symbol	Signal Name	Symbol	Signal Name
IA	I	5	5	—	See Note 1	TA(C)	Transmit A(C) Signaling
IB	I	6	6	—	See Note 1	TB(D)	Transmit B(D) Signaling
IC	I	57	61	TLINK	Transmit Link	TLINK	Transmit Link
ID	I	7	7	TFSIG	Framing-Bit Signal	TFSIG	Framing-Bit Signal
OA	O	34	36	RMFA	Receive Multiframe Alignment	RSIG	Receive Signaling Frame
OB	O	31	33	—	See Note 2	RSIGBD	Receive Signaling B or D
OC	O	30	32	CKERR	Cyclic Redundancy Check Bit Error	RSIGCD	Receive Signaling C or D
OD	O	29	31	FERR	Framing Error	ERR	Framing or CRC Error
OE	O	22	23	TFR24	Transmit Frame 24	TSIGSEL	Transmit Signaling Select
OF	O	35	37	RLINK	Receive Data Link	RLINK	Receive Data Link
OG	O	36	38	RLCLK	Receive Link Clock	RLCLK	Receive Link Clock
OH	O	21	22	TLCLK	Transmit Link Clock	TLCLK	Transmit Link Clock
OJ	O	20	21	TFGEN	Framing-Bit Generator	TFGEN	Framing-Bit Generator

Pin Name	I/O	Pin No.		197N Mode		197S Mode	
		QUIP	PLCC	Symbol	Signal Name	Symbol	Signal Name
IA	I	5	5	TSBIT	Transmit S-Bit	TA	Transmit A Signaling
IB	I	6	6	—	See Note 1	TB	Transmit B Signaling
IC	I	57	61	TLINK	Transmit Link	TLINK	Transmit Link
ID	I	7	7	TFSIG	Framing-Bit Signal	TFSIG	Framing-Bit Signal
OA	O	34	36	RSIG	Receive Signaling Frame	RSIG	Receive Signaling Frame
OB	O	31	33	RSBIT	Receive S-Bit	RSBIT	Receive S-Bit
OC	O	30	32	RSBCLK	Receive S-Bit Clock	RSBCLK	Receive S-Bit Clock
OD	O	29	31	FERR	Framing Error	FERR	Framing Error
OE	O	22	23	TSBCLK	Transmit S-Bit Clock	SERR	S-Bit Errors
OF	O	35	37	RLINK	Receive Data Link	RLINK	Receive Data Link
OG	O	36	38	RLCLK	Receive Link Clock	RLCLK	Receive Link Clock
OH	O	21	22	TLCLK	Transmit Link Clock	TLCLK	Transmit Link Clock
OJ	O	20	21	TFGEN	Framing-Bit Generator	TFGEN	Framing-Bit Generator

Notes:
1 Test input, tie to a high level
2. Test output, leave open (unconnected)

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T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Dedicated Signals

Pin Name/ Symbol	I/O	Signal Name/Description
TCLK	I	**Transmit Clock.** TCLK is the transmitter clock input and **must be present for normal transceiver (transmitter or receiver) operation.** TCLK must be in the range 100 kHz – 3.1 MHz and will normally be 1.544 MHz for T1 and 1.576 MHz for 1/2 T1C. All inputs and outputs are clocked on the rising edge of TCLK.
TFSYNC	I	**Transmit Frame Sync.** TFSYNC high resets the bit counter to the beginning of a frame. The counter restarts on the first rising edge of TCLK after TFSYNC goes low TFSYNC should be synchronous with TCLK to ensure setup and hold times. TFSYNC need only be applied to change the transmitter frame alignment.
TMSYNC	I	**Transmit Multiframe Sync.** TMSYNC high resets the frame counter to frame 1. TMSYNC low enables the frame counter. TMSYNC need only be applied to change the transmitter multiframe alignment. TFSYNC is normally applied with TMSYNC to align to the first bit of the multiframe.
TLOOP	I	**Transmit Loop.** TLOOP high invokes loopback mode, where TPOS and TNEG are internally routed to RPOS and RNEG, respectively. TPOS and TNEG external signals carry alternate 1s representing a continuous stream of 1s. TLOOP does not affect TNRZ. This internal looping has one bit time less delay than an equivalent external looping.
TIDLE	I	**Transmit Idle.** TIDLE high causes the idle code (01111111) to be transmitted in the next channel, in place of the normal data. This substitution continues for each channel in which TIDLE is high.
TYEL	I	**Transmit Yellow Alarm.** TYEL high causes transmission of a Yellow Alarm in the following formats: **Mode** — **Format** 193N, 193S (YELMD = 0), 197N, 197S — Bit 2 = 0 in all data channels 193S (YELMD = 1) — S-bit high in frame 12 193F, 193E — 8 0s, 8 1s pattern on data link
TPOS, TNEG	O	**Transmit Unipolar Positive, Unipolar Negative.** TPOS and TNEG are the "unipolar-paired" TTL, NRZ outputs for transmitted data Binary 0 is coded as a low (0) level on both outputs Binary 1 is coded as a high (1) level on TPOS or TNEG, alternately. TPOS and TNEG allow the direct generation of AMI line code in which a 1 (mark) is alternately represented as a positive or negative pulse. There is an 8-bit throughput delay between the TSER input and the TPOS/TNEG outputs.
TNRZ	O	**Transmit Non-Return-to-Zero.** TNRZ is the TTL, NRZ output for transmitted data. This output is unaffected by TLOOP or by B8ZS zero suppression coding. There is an 8-bit throughput delay between the TSER input and the TNRZ output.
TMAX	O	**Transmit Maximum.** TMAX is high for one bit time per multiframe coincident with the sampling of bit 7 of channel 24 of the last frame (2 bit times before sampling the first F-bit of a multiframe).
RCLK	I	**Receive Clock.** RCLK is the receiver clock input and must be present for normal transceiver operation. All inputs and outputs are clocked on the rising edge of RCLK. RCLK must be in the range 100 kHz – 3.1 MHz and will normally be 1.544 MHz for T1 and 1.576 MHz for 1/2 T1C.
RPOS, RNEG	I	**Receive Unipolar Positive, Unipolar Negative.** RPOS and RNEG are the inputs for received data recovered from the positive and negative AMI line pulses. RPOS and RNEG should have TTL levels and may be of either NRZ or RZ form. If RPOS is strapped to RNEG (and given composite RPOS/RNEG data) the first occurrence of a 1 will invoke the transparent mode in which B8ZS zero suppression is disabled in both the receiver and the transmitter.
RIDLE	I	**Receive Idle.** RIDLE high causes data in the next received channel to be substituted with the idle code (01111111). The substitution continues for each channel in which RIDLE is high. RIDLE and RMW should not be high simultaneously.
RMW	I	**Receive Milliwatt.** RMW high causes data in the next received channel to be substituted with the digital milliwatt code; a repeating pattern of eight 8-bit bytes that translate into a 1 kHz signal at a level of 1 mW. The substitution is performed for each channel in which RMW is high. RMW and RIDLE should not be high simultaneously.
RMRST	I	**Receive Master Reset.** RMRST high resets the master state sequencer in the synchronizer to its initial (WAIT) state. RMRST low allows synchronization to proceed.
RSRCH	I	**Receive Search.** RSRCH low prevents the master state sequencer in the synchronizer from proceeding out of the WAIT state. It does not force the synchronizer to the WAIT state (see RMRST). If RSRCH is low while the receiver is in frame alignment (RRED low), bit 5 of channel 1, frame 1 is skipped. This allows recentering of elastic stores.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Dedicated Signals (Cont'd)

Pin Name/ Symbol	I/O	Signal Name/Description
RSER	O	**Receive Serial Data.** RSER is the serial data output including F-bits and L-bits and after B8ZS decoding, if applicable. The throughput delay from RPOS/RNEG to RSER is 14 cycles of RCLK. RSER is always valid, regardless of the synchronizer state.
RSYNC	O	**Receive Sync.** RSYNC is high during the first F-bit of each multiframe while the receiver is synchronized.
RVLL	O	**Receive Bipolar Violation, Loss of Carrier.** RVLL high indicates that the 1 currently at RSER resulted from a bipolar violation. RVLL also goes high after 31 consecutive 0s at RSER, to indicate "loss of carrier". The first received 1 (if non-bipolar violation) resets RVLL. These two signals are distinguished by the level on RSER.
RYEL	O	**Receive Yellow Alarm.** RYEL high indicates a received Yellow Alarm for the following conditions: **Mode** — **Condition** 193N, 193S (YELMD = 0), 197N, 197S — Bit 2 = 0 for 255 consecutive channels 193S (YELMD = 1) — S-bit high in frame 12 193F, 193E — 16 ±1 sets of 8 0s, 8 1s on data link
RRED	O	**Receive Red Alarm.** RRED high indicates loss of frame alignment. RRED low indicates correct frame alignment. Multiframe alignment is separately indicated.
M1–M4	I	**Framing Mode Select.** M1–M4 select the framing mode as follows (See the T1 Mode Selection Table for additional mode information): **M1 M2 M3 M4 — T1 Mode — Zero Suppression** 1 0 1 0 — 193S — B8ZS 0 0 1 0 — 193S — B7 1 1 1 0 — 193N — B8ZS 0 1 1 0 — 193N — B7 1 1 1 1 — 193E — B8ZS 0 1 1 1 — 193E — B7 1 0 1 1 — 193F — B8ZS 1 0 0 0 — 197S — Transparent 1 1 0 0 — 197N — Transparent
P/$\overline{S}$	I	**Parallel/Serial Interface Select.** P/$\overline{S}$ selects parallel (P/$\overline{S}$ high) or serial (P/$\overline{S}$ low) operation of the PSI1–PSI8 and PSO1–PSO13 pins
PUP	I	**Power-up.** PUP initializes the R8070 transmitter and receiver It includes TFSYNC, TMSYNC and RMRST reset functions. PUP sets all outputs, except OJ, to a high-impedance state, to facilitate testing of peripheral circuitry.
V_{CC}	I	**+5V Power.** +5 VDC power
V_{SS}	I	**Ground.** Power and signal ground

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T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Parallel/Serial Interface-Dependent Signals

a. Parallel Interface (P/$\overline{S}$ = High)

Pin Name/ Symbol	I/O	Symbol	Signal Name/Description
PSI1–PSI8	I	T1–T8	**Transmit Channel Data Bits 1–8.** T1–T8 are the parallel inputs for channel data. They are clocked into the transmitter at the rising edge of TCHCLK, by the rising edge of TCLK. The falling edge of TCHCLK may be used to present the next channel data at T1–T8.
PSO1–PSO8	O	R1–R8	**Receive Channel Data Bits 1–8.** R1–R8 are the parallel outputs for channel data. F-bits and L-bits are excluded; "robbed" signaling bits are included on R8. The channel data is available for a complete channel time and is updated at the rising edge of RCHCLK. The falling edge of RCHCLK may be used to clock this data into external buffers. R1–R8 are only valid while the receiver is synchronized; RSER, the serial data output, is always available and always valid.
PSO9	O	TCHCLK	**Transmit Channel Clock.** TCHCLK is a channel-rate clock whose rising edge indicates that parallel data on T1–T8 is being sampled The falling edge is used to present the next channel's data on T1–T8. TCHCLK is low for 4 bit times.
PSO10	O	TCHSYNC	**Transmit Channel Sync.** TCHSYNC is a frame-rate signal which is high for 8 bit times, prior to the sampling of channel 1. The rising edge precedes channel 24 sampling by one bit time; the falling edge precedes channel 1 sampling by one bit time.
PSO11	O	RCHCLK	**Receive Channel Clock.** RCHCLK is a channel-rate clock whose rising edge indicates that new channel data has been output to R1–R8. The falling edge may be used to clock this data into external buffers. RCHCLK is high for 4 bit times.
PSO12	O	RCHSYNC	**Receive Channel Sync.** RCHSYNC is a frame-rate signal which is high for 9 (193) or 10 (197) bit times. The rising edge occurs one bit time after the output of channel 24 data on R1–R8. The falling edge occurs one bit time after the output of channel 1 data on R1–R8.
PSO13	O	RWIHBT	**Receive Write Inhibit.** RWIHBT is a channel-rate signal, 2 bit times high, which "covers" the change of parallel data on R1–R8. RWIHBT is high for one bit time before and after the rising edge of RCHCLK.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Parallel/Serial Interface-Dependent Signals

b. Serial Interface ($P/\overline{S}$ = Low)

Pin Name/ Symbol	I/O	Symbol	Signal Name/Description
PSI1	I	TSER	**Transmit Serial.** TSER is the serial input for the channel data and, optionally, signaling data
PSI2	I	TSIGMD	**Transmit Signaling Mode.** TSIGMD selects the source for "robbed" signaling bits. If low, TA and TB (193S and 197S) or TA(C) and TB(D) (193E) are the source. If high, TSER is the source.
PSI3	I		**PSI3.** Not applicable to T1 modes, tie to ground
PSI4	I	TSA	**Transmit Sequence Advance.** TSA high advances the standard timing of TSQ1–TSQ5 and TSIGSQ by one bit time
PSI5	I	RSHIFT	**Receive Shift.** RSHIFT high shifts the RSQ1–RSQ5 sequence of channel numbers from 1 to 13, 2 to 14, . 12 to 24 The F-bit and L-bit codes are unaffected
PSI6, PSI7	I	D1D, D2	**Channel Sequence Select.** D1D and D2 select the sequence of channel numbers according to D1D, D2, D3 or D4 channel assignments. **D2** **D1D** **Channel Assignment** 0 0 D3, D4 0 1 D1D 1 0 D2 1 1 D3, D4 plus synchronization lock (inhibits resync after loss of frame alignment)
PSI8	I	RSR	**Receive Sequence Retard.** RSR high delays the standard timing of RSQ1–RSQ5 and RSIGSQ by one bit time
PSO1–PSO5	O	RSQ1–RSQ5	**Receive Sequence Code Bits 1–5.** RSQ1–RSQ5 is the binary value of the channel number (1–24) currently emerging from RSER. The sequence is selected by D1D and D2 to match D1D, D2, D3 or D4 channel assignments The code for F-bit is 00000 The codes for L-bit (197 modes) are· 11100 (following channel 24), 11101 (channel 6), 11110 (channel 12) and 11111 (channel 18).
PSO6	O	TSIGSQ	**Transmit Signaling Square Wave.** TSIGSQ is a 2/3 kHz square wave which is high for frames 6–11 (193S) or frames 6–11, 18–23 (193E) and low for other frames. TSIGSQ allows certain per-channel codecs to insert A and B signaling bits into TSER.
PSO7	O	RSIGSQ	**Receive Signaling Square Wave.** RSIGSQ is identical in form to TSIGSQ The rising edge precedes frames carrying A(C) signaling bits, the falling edge precedes frames carrying B(D) signaling bits
PSO8	O	R8	**Receive Data Bit 8.** R8 carries bit 8 parallel channel data and is available for the complete channel time. R8 allows extraction of the "robbed" signaling bits, which are located in bit 8
PSO9–PSO13	O	TSQ1–TSQ5	**Transmit Sequence Code Bits 1–5.** TSQ1–TSQ5 is the binary value of the channel number (1–24) currently being sampled at TSER. The channel assignment and codes for F-bit and L-bit are identical to those in RSQ1–RSQ5.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Framing Mode-Dependent Signals

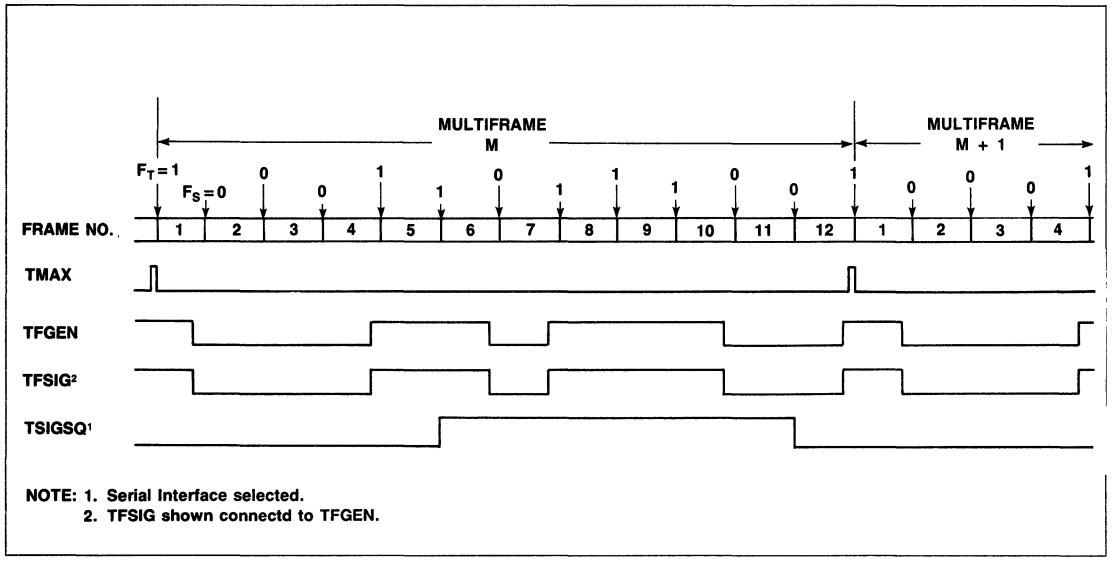
Pin Name	I/O	Signal Symbol	Mode						Signal Name/Description
			193N	193S	193F	193E	197N	197S	
IA	I	TSBIT	•	—	—	—	•	—	**Transmit S-Bit.** TSBIT is the S-bit (Fs) input.
		TA	—	•	—	—	—	•	**Transmit A Signaling.** TA is the A-bit input for robbed-bit signaling.
		TA(C)	—	—	—	•	—	—	**Transmit A(C) Signaling.** TA(C) is the A-bit (TSIGSEL low) or C-bit (TSIGSEL high) input for robbed-bit signaling.
IB	I	TB	—	•	—	—	—	•	**Transmit B Signaling.** TB is the B-bit input for robbed-bit signaling.
		TB(D)	—	—	—	•	—	—	**Transmit B(D) Signaling.** TB(D) is the B-bit (TSIGSEL low) or D-bit (TSIGSEL high) input for robbed-bit signaling.
IC	I	RS96E	•	—	—	—	—	—	**Receive SLC-96 Enable.** RS96E selects the method for Fs recovery. If low, Fs is extracted from the incoming data. If high, the current Fs pattern is recirculated.
		YELMD	—	•	—	—	—	—	**Yellow Alarm Mode.** YELMD selects the method for transmission and detection of Yellow Alarm. If low, Yellow Alarm is transmitted as bit 2 = 0 in all data channels. If high, Yellow Alarm is transmitted as a 1 in the S-bit of frame 12.
		TLINK	—	—	•	•	•	•	**Transmit Link.** TLINK is the serial data link input. The data rate is 4 kbps (193E, 193F) or 32 kbps (197N, 197S).
ID	I	TFSIG	•	•	•	•	•	•	**Framing-Bit Signal.** TFSIG is the input for Ft and Fs bits and is sampled coincident with channel 1 parallel data. Connect to TFGEN for internally generated framing bits.
OA	O	RSIG	•	•	—	•	•	•	**Receive Signaling Frame.** RSIG is high during the receipt of signaling frames, low for non-signaling frames. RSIG is held low for recent Ft or Fs errors.
		RMFA	—	—	•	—	—	—	**Receive Multiframe Alignment.** RMFA is high during frame 24. Transitions coincide with the emergence of the F-bit at RSER.
OB	O	RSBIT	•	•	—	—	•	•	**Receive S-Bit.** RSBIT is the output of the last received S-bit.
		RSIGBD	—	—	—	•	—	—	**Receive Signaling B or D.** RSIGBD is a 2 kHz square wave which is low for A- and C-bit signaling frames, and high for B- and D-bit signaling frames. RSIGBD, RSIGCD and RSIG are used to decode A, B, C and D signaling bits. (See RSIGCD.)
OC	O	RSBCLK	•	•	—	—	•	•	**Receive S-Bit Clock.** RSBCLK is a 4 kHz square wave with a rising edge 1 bit time after the emergence of an S-bit (Fs) at RSER.
		CKERR	—	—	•	—	—	—	**Cyclic Redundancy Check Bit Error.** CKERR high indicates an error in the current CRC bit at RSER.
		RSIGCD	—	—	—	•	—	—	**Receive Signaling C or D.** RSIGCD is a 1/3 kHz square wave which is low for A- and B-bit signaling frames, and high for C- and D-bit signaling frames. (See RSIGBD.)
OD	O	FERR	•	•	•	—	•	•	**Framing Error.** FERR high indicates an error in the current framing bit at RSER.
		ERR	—	—	—	•	—	—	**Framing or CRC Error.** ERR high indicates an error in the current framing bit (RSIGBD high) or checksum bit (RSIGBD low) at RSER.
OE	O	TSBCLK	•	—	—	—	•	—	**Transmit S-Bit Clock.** TSBCLK is a 4 kHz square wave whose rising edge occurs 2 bit times after the sampling of TSBIT.
		SERR	—	•	—	—	—	•	**S-Bit Errors.** SERR high indicates one or more errors in the last five S-bits. SERR will remain high until the last five S-bits are correct.
		TFR24	—	—	•	—	—	—	**Transmit Frame 24.** TFR24 is high during frame 24.
		TSIGSEL	—	—	—	•	—	—	**Transmit Signaling Select.** TSIGSEL is low for frames 2–13 (A- and B-bit sampling), and high for frames 14–24 and 1 (C- and D-bit sampling). Transitions coincide with F-bit sampling.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Framing Mode-Dependent Signals (Cont'd)

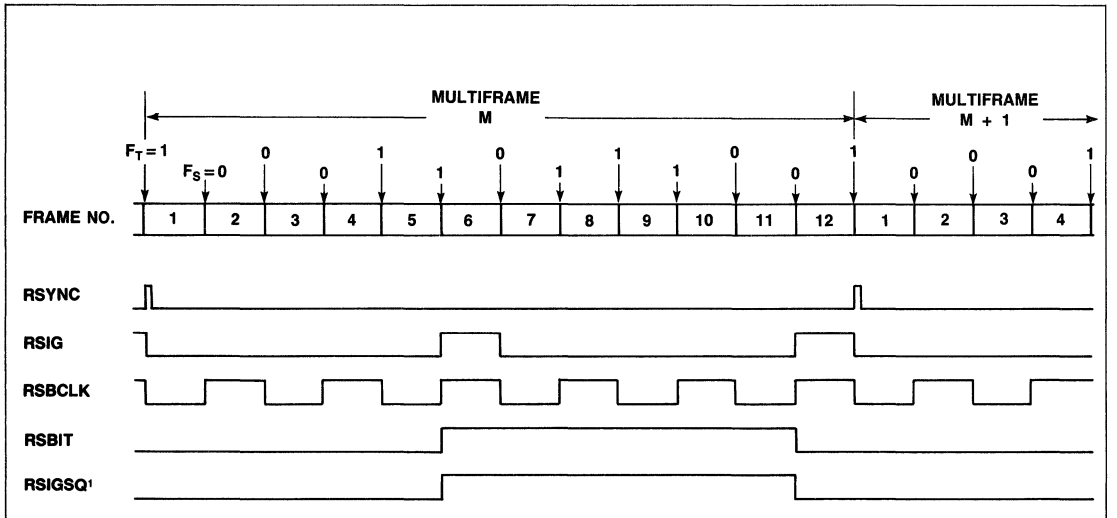
Pin Name	I/O	Signal Symbol	Mode						Signal Name/Description
			193N	193S	193F	193E	197N	197S	
OF	O	MS1	•	•	—	—	—	—	**Master State Sequence Code, Bit 1.** MS1 is the least significant bit (bit 1) of master state sequence code MS1, MS2 and MS3 indicate the binary value of the current state of the receiver's synchronizer MS3 is the inverse of RRED ($\overline{\text{RRED}}$) MS3 / MS2 / MS1 / Master State 0 0 0 Wait 0 0 1 Initialize 0 1 0 Search 0 1 1 Demons 1 0 0 Proving State 1 (P1) 1 0 1 Proving State 2 (P2) 1 1 0 Proving State 3 (P3) 1 1 1 Multiframe Synchronization
		RLINK	—	—	•	•	•	•	**Receive Data Link.** RLINK is the serial data link output The data rate matches that of TLINK 4 kbps (193E, 193F) or 32 kbps (197N, 197S)
OG	O	MS2	•	•	—	—	—	—	**Master State Sequence Code, Bit 2.** MS2 is bit 2 of the master state sequence code (See MS1)
		RLCLK	—	—	•	•	•	•	**Receive Link Clock.** RLCLK is a square wave whose rising edge occurs 2 bit times (193E, 193F) or 1 bit time (197N, 197S) after the received data on RLINK
OH	O	TLCLK	—	—	•	•	•	•	**Transmit Link Clock.** TLCLK is a square wave whose rising edge occurs 4 bit times after the sampling of TLINK
OJ	O	TFGEN	•	•	•	•	•	•	**Framing-Bit Generator.** TFGEN is the output of the framing pattern generator It includes the Ft and Fs bit (193S, 197S), Ft bit (193N, 197N) and framing, data link and CRC check bits (193E, 193F)

T1 WAVEFORMS



NOTE: 1. Serial Interface selected.
2. TFSIG shown connectd to TFGEN.

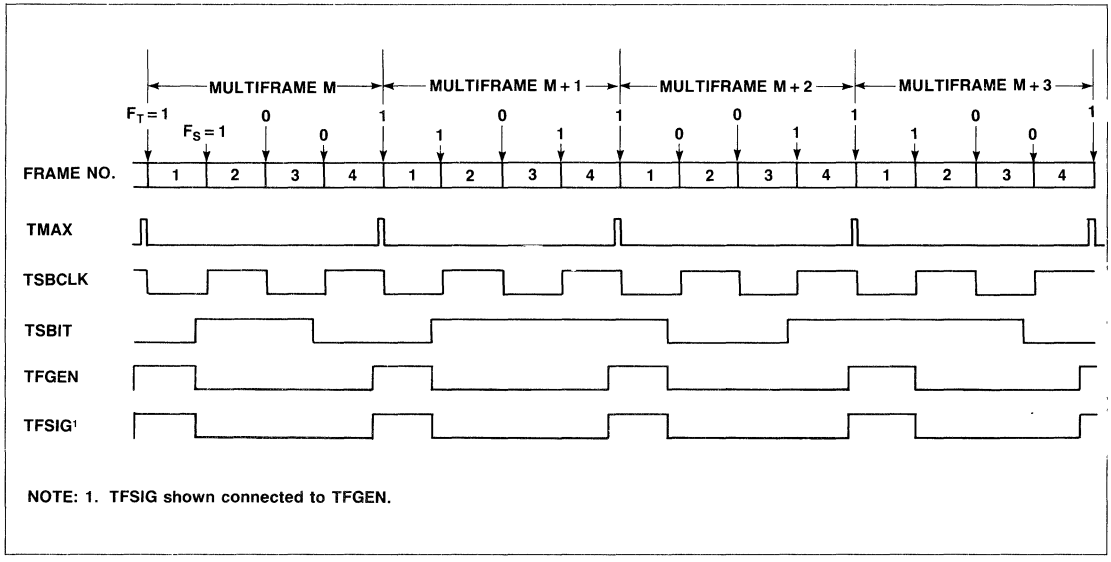
Transmit Signaling—Mode 193S and 197S



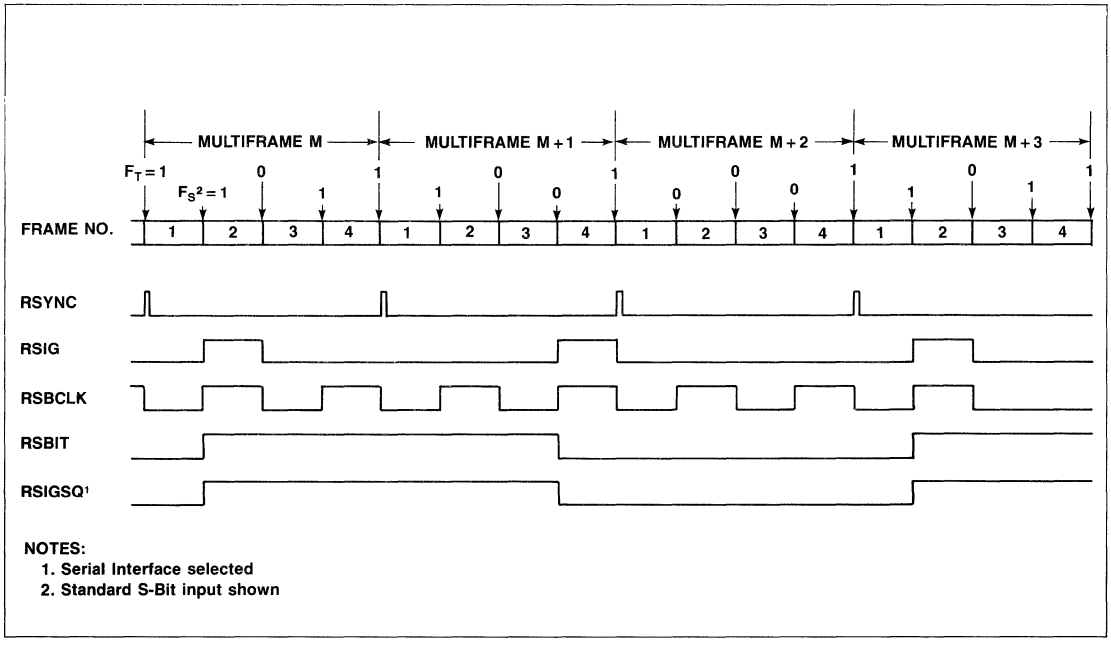
NOTE: 1. Serial Interface selected

Receive Signaling—Modes 193S and 197S

T1 WAVEFORMS (Cont'd)

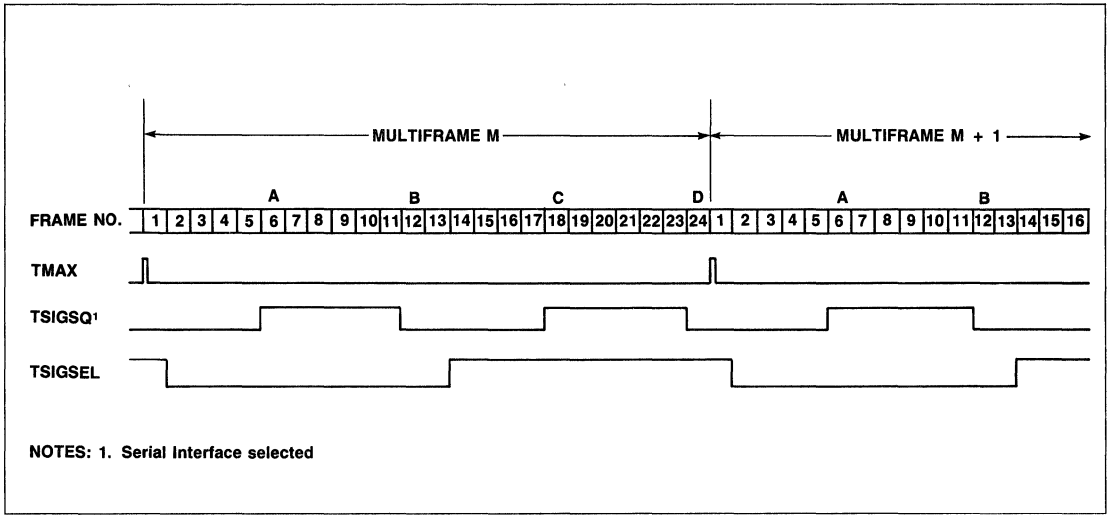


Transmit Signaling—Mode 193N and 197N

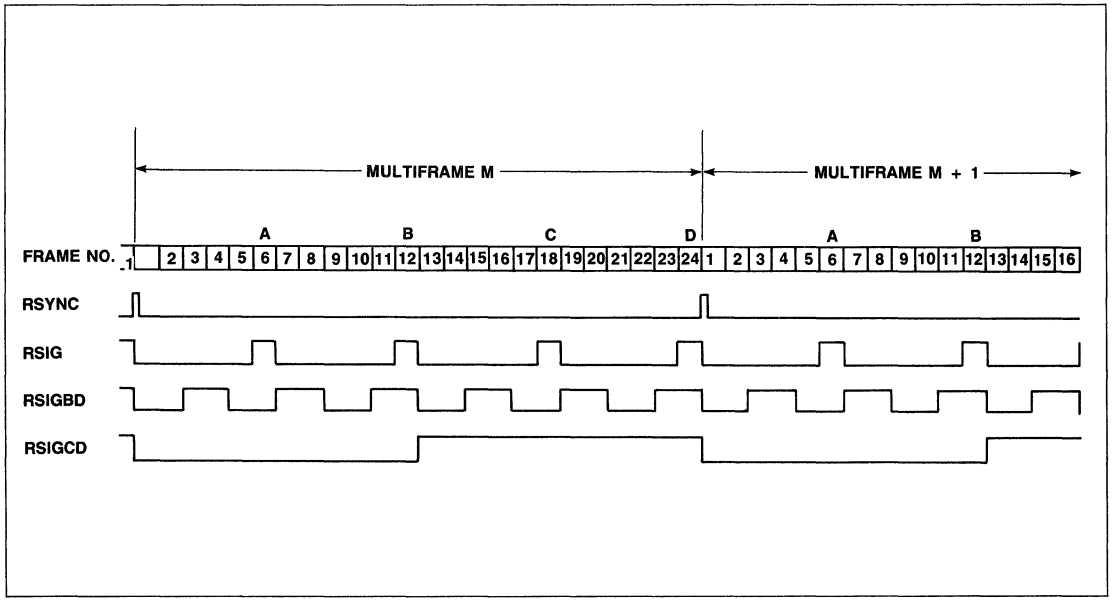


Receive Signaling—Mode 193N and 197N

T1 WAVEFORMS (Cont'd)

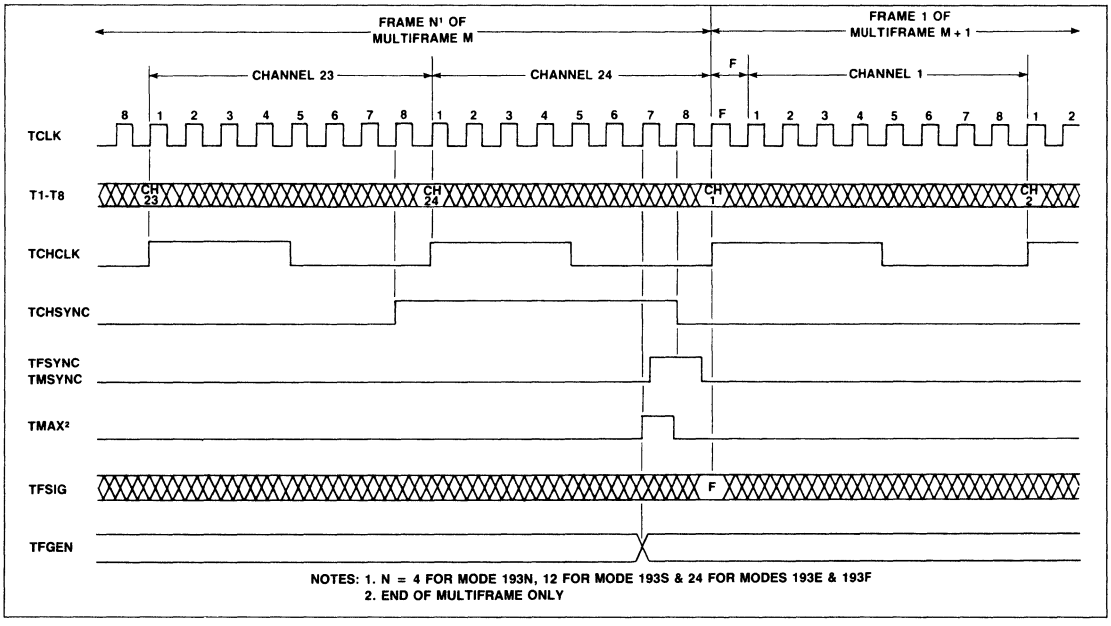


Transmit Signaling—Mode 193E

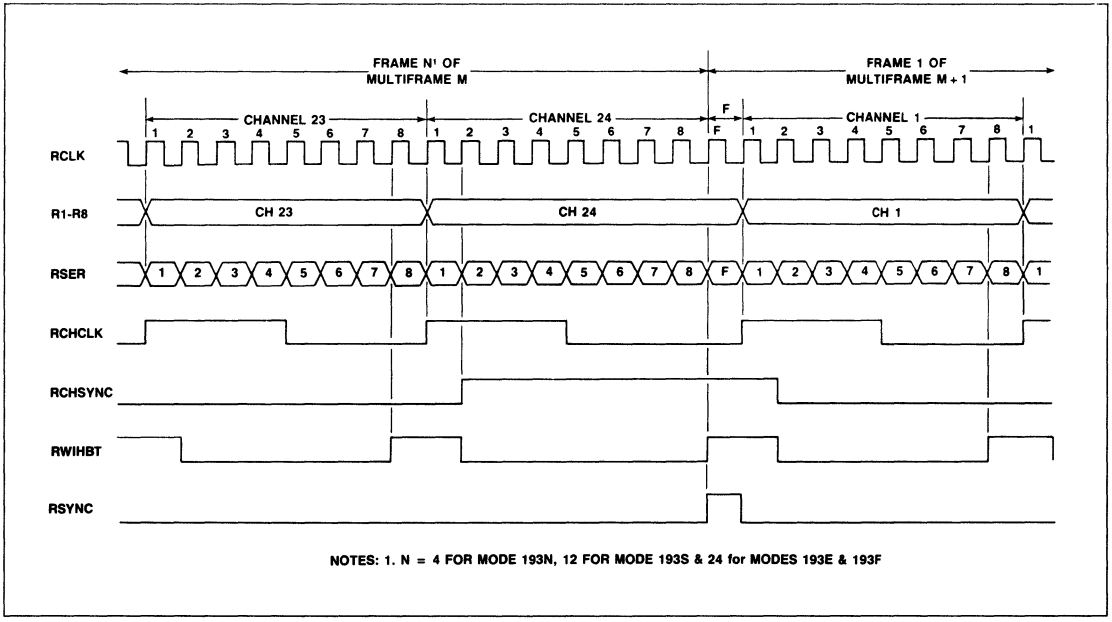


Receive Signaling—Mode 193E

T1 WAVEFORMS (Cont'd)

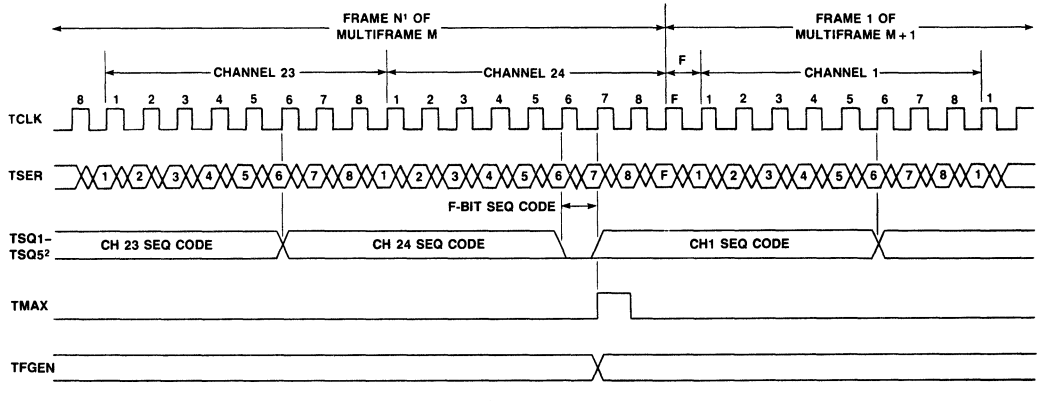


Parallel Interface—Transmit Signals—Modes 193N, S, E & F



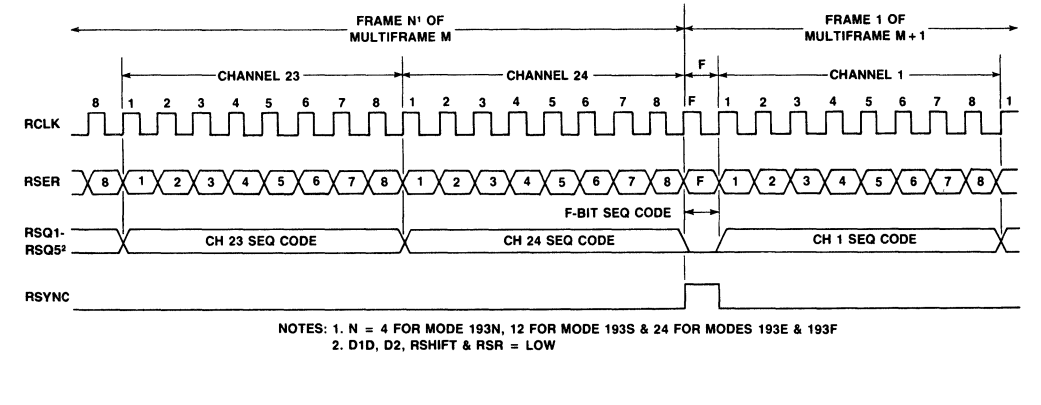
Parallel Interface—Receive Signals—Modes 193N, S, E & F

T1 WAVEFORMS (Cont'd)



NOTES: 1. N = 4 FOR MODE 193N, 12 FOR MODE 193S & 24 FOR MODES 193E & 193F
2. D1D, D2 & TSA = LOW

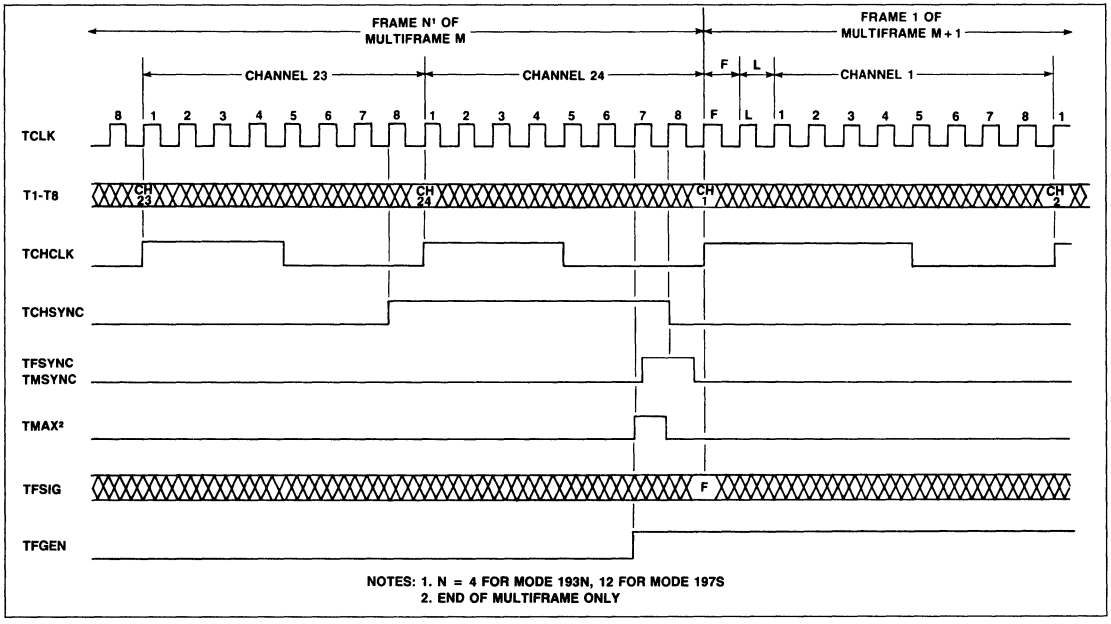
Serial Interface—Transmit Signals—Modes 193N, S, E & F



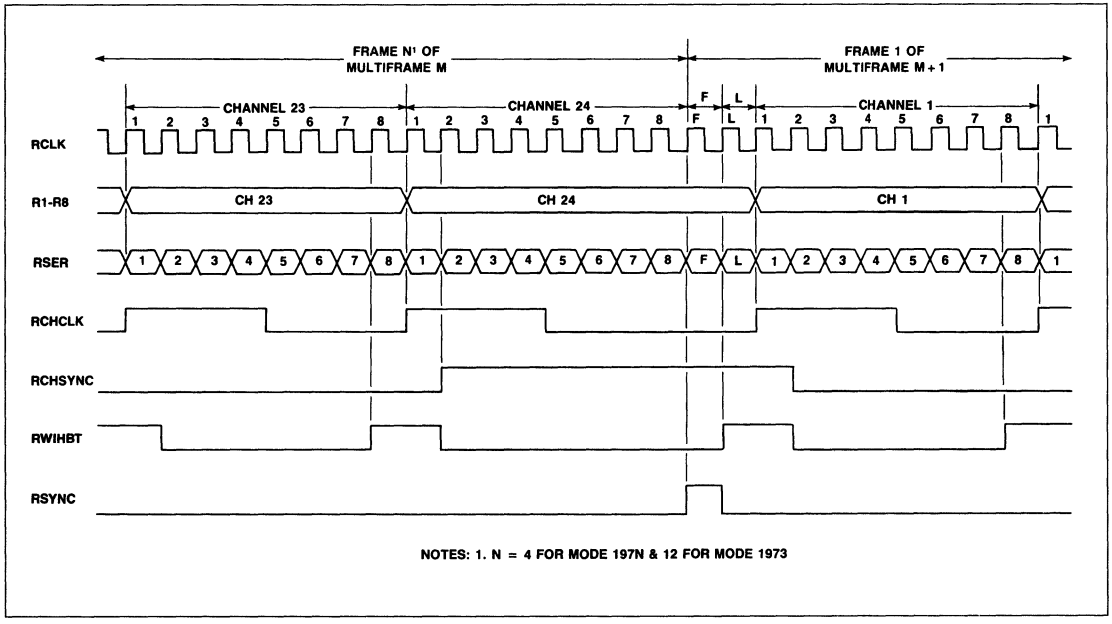
NOTES: 1. N = 4 FOR MODE 193N, 12 FOR MODE 193S & 24 FOR MODES 193E & 193F
2. D1D, D2, RSHIFT & RSR = LOW

Serial Interface—Receive Signals—Modes 193N, S, E & F

T1 WAVEFORMS (Cont'd)

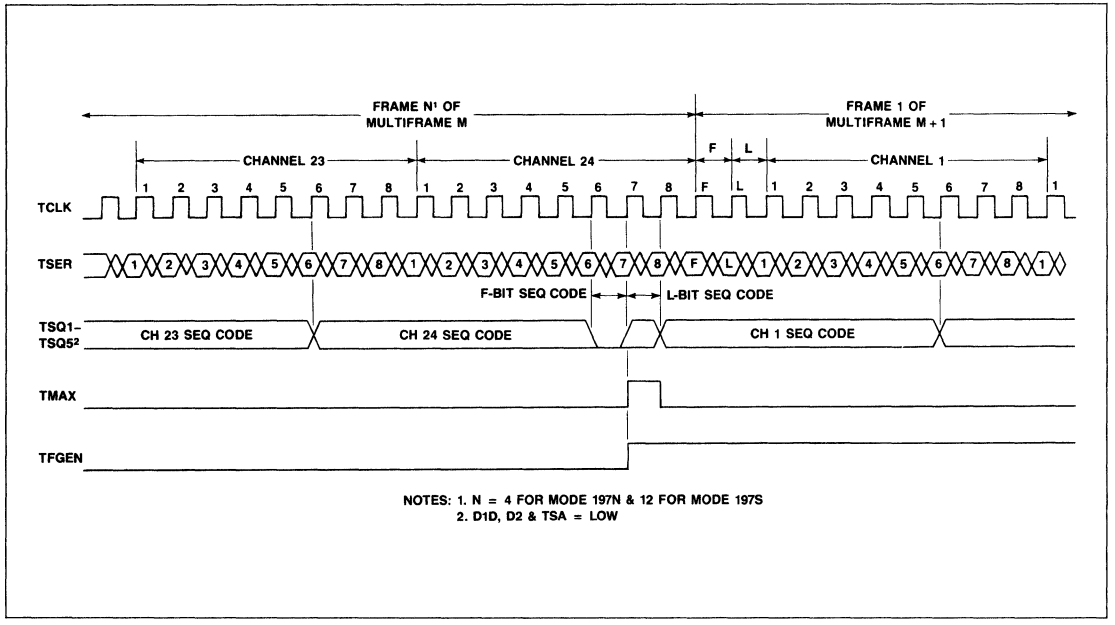


Parallel Interface—Transmit Signals—Modes 197N & S

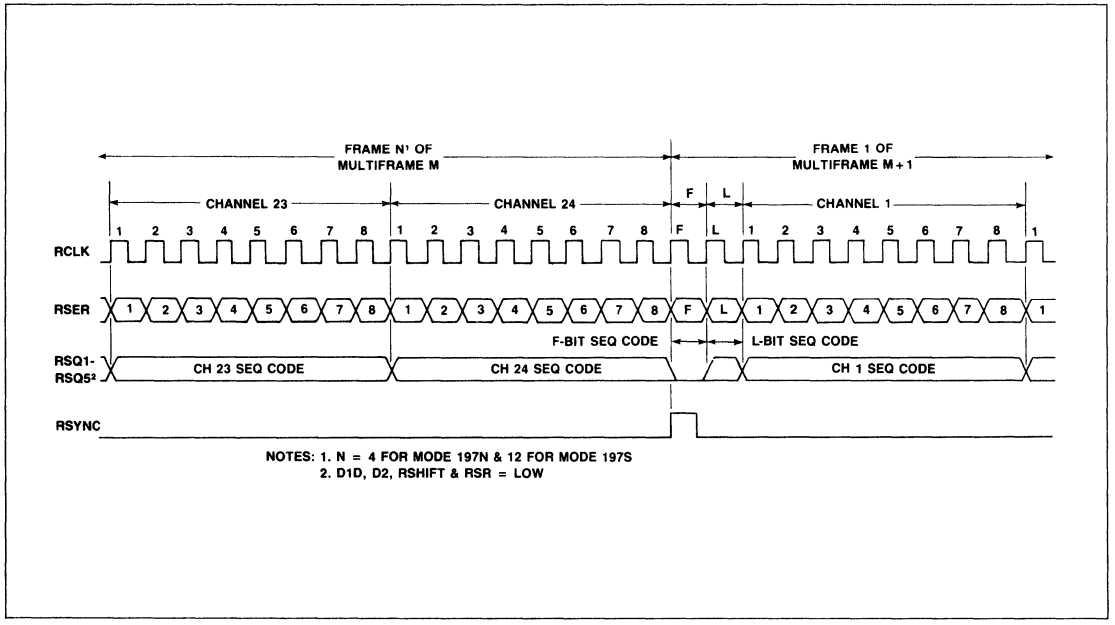


Parallel Interface—Receive Signals—Modes 197N & S

T1 WAVEFORMS (Cont'd)



Serial Interface—Transmit Signals—Modes 197N & S



Serial Interface—Receive Signals—Modes 197N & S

CEPT PCM-30 OVERVIEW

CEPT PCM-30 FORMAT

CEPT PCM-30 is a PCM format for time-division multiplexing 30 voice (telephone) or data circuits onto a single transmission path. This path is normally a dual twisted-pair cable with digital repeaters. There is a hierarchy of PCM formats within the CEPT PCM system that defines further time-division multiplexing of multiple PCM-30 lines.

Prior to transmission, each voice circuit is sampled at 8 kHz using an 8-bit A-law companding analog-to-digital converter. The resulting 64 kbps (8 bits × 8 kHz) signal is time-division multiplexed with 29 other sampled channels, plus 2 channels of alignment and signaling bits, to produce a frame of 256 bits (32 channels × 8 bits). Since each voice circuit is sampled at 8 kHz, the frame rate is 125 μs. To transmit 256 bits in 125 μs requires a bit rate of 2.048 Mbps, hence the standard CEPT PCM-30 clock frequency of 2.048 MHz.

Signaling Data. Signaling data, such as on-hook and off-hook conditions, dialing digits, call progress, etc., associated with each voice circuit is transmitted within time slot 16. This is known as common channel signaling since a single (common) channel is dedicated for the signaling data of all voice circuits within the PCM link.

In order for each channel to be distinguished at the receiver, a frame alignment signal (0011011) is transmitted in bits 2–8 of time slot 0 in alternating frames. The remaining bit 1 of time slot 0 carries the International bit. In frames not containing the frame alignment signal, bit 2 is fixed at 1 to avoid imitation of that signal. The remaining bits carry National and International signaling and alarm indication for loss of frame alignment.

In order for each frame to be distinguished at the receiver (for recovery of ABCD signaling data), a multiframe alignment signal is transmitted in bits 1–4 of time slot 16 of frame 0. Bit 6 of the same time slot indicates loss of multiframe alignment. Bits 5, 7 and 8 carry Extra-bit signaling.

To recap, the PCM structure consists of: a multiframe of 16 frames; a frame of 32 time slots (30 voice channels plus 2 alignment and signaling time slots); and 8 bits per time slot.

Alarms and Error Conditions. In addition to channel and signaling data, CEPT defines several alarm and error conditions that must be monitored and reported. The principal alarms are:

1. Red Alarm
2. Yellow Alarm
3. Multiframe Red Alarm
4. Multiframe Yellow Alarm

A Red Alarm is produced by a receiver to indicate that it has lost frame alignment. A Yellow Alarm is returned to the transmitting terminal to report a loss of frame alignment at the receiving terminal. Normally, a CEPT terminal will use the receiver's Red Alarm to request that a Yellow Alarm be transmitted. The multiframe alarms refer to loss of multiframe alignment.

The principal error conditions are:

1. Bipolar violation
2. Frame alignment error
3. Multiframe alignment error

A bipolar violation is a failure to meet the Alternate Mark Inversion (AMI) line code of CEPT PCM-30. AMI dictates that 1s (marks) are transmitted alternately as positive or negative pulses; zeros are transmitted as zero volts.

Clock Recovery. In order to guarantee adequate clock recovery from the received data, a minimum "ones density" must be observed. HDB3 represents a group of 4 zeros by a predefined code that includes an intentional bipolar violation. At the receiver, the code is recognized and the original 4 zeros are restored.

The R8070 supports all major requirements of the CEPT PCM-30 system, including channel data recovery, signaling, alarm indication, error reporting, and zero suppression to satisfy the ones density requirement.

CEPT MODES DESCRIPTION

One of the two CEPT modes can be selected by configuring the M1–M4 lines as shown in the CEPT Mode Selection Table.

256S Mode. The 256S mode implements CEPT PCM-30 format at 2.048 Mbps with 16 frames per multiframe and 32 time slots per frame. ABCD common channel signaling is supported in time slot 16. There are 256 bits per frame.

The frame alignment signal (in time slot 0) and the multiframe alignment signal (in time slot 16) are generated by the R8070 transmitter and recovered by the receiver.

National-bit (time slot 0), International-bit (time slot 0) and Extra-bit (time slot 16) signaling is provided.

HDB3 zero suppression is standard but may be disabled for transparent operation.

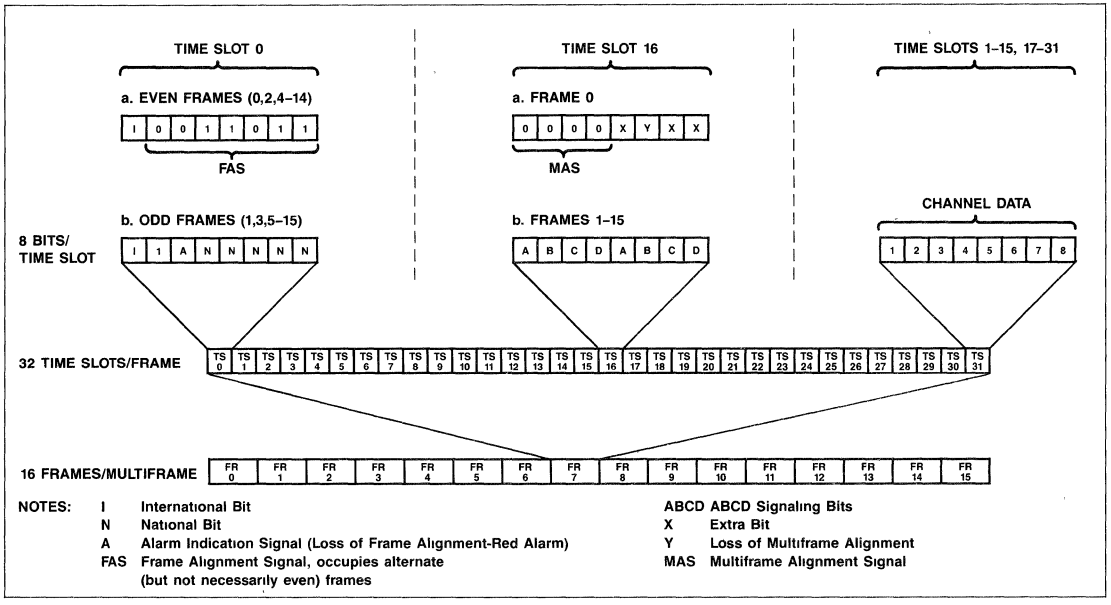
256N Mode. The 256N mode also implements CEPT PCM-30 format at 2.048 Mbps but without ABCD common channel signaling. There are 2 frames per multiframe and 32 time slots per frame. A data link channel is implemented via time slot 16, in place of ABCD signaling. There are 256 bits per frame.

The frame alignment signal in time slot 0 is generated by the transmitter and recovered by the receiver. There is no multiframe alignment signal and so the multiframe structure degenerates to 2 frames, which are distinguished by time slot 0 content.

National-bit and International-bit signaling is provided in time slot 0. There is no Extra-bit signaling as time slot 16 is dedicated to the data link.

HDB3 zero suppression is standard but may be disabled for transparent operation.

CEPT PCM-30 OVERVIEW (Cont'd)



CEPT PCM-30 Format

CEPT PCM-30 Hierarchy

Level Number	Number of Voice Circuits	Bit Rate (Mbps)
1	30	2 048
2	120	8 448
3	480	34 368
4	1920	139 264
5	7680	565 148

CEPT PCM-30 Time Slot and Channel Numbering

Time Slot	Channel	Time Slot	Channel
0	FAS	16	MAS
1	1	17	16
2	2	18	17
3	3	19	18
4	4	20	19
5	5	21	20
6	6	22	21
7	7	23	22
8	8	24	23
9	9	25	24
10	10	26	25
11	11	27	26
12	12	28	27
13	13	29	28
14	14	30	29
15	15	31	30

NOTES: FAS Frame Alignment Signal, International and National Bits, and Alarm Indication Signal (loss of frame alignment)

MAS Multiframe Alignment Signal, ABCD Signaling, Extra Bits, and Loss of Multiframe Alignment

CEPT FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

The transmit section of the R8070 provides the data formatting, signaling and alarm indication functions required for PCM transmission according to CCITT G.732 and applicable sections of G.703.

PCM Channel Data

Data Input. Data is clocked into the transmitter either serially (via TSER) or in parallel form (via T1–T8), on the rising edge of the transmitter clock (TCLK). The externally provided TCLK normally has a rate of 2.048 MHz.

For a serial data interface, Transmit Sequence signals (TSQ1–TSQ5) specify the binary value of the next channel to be sampled. These signals, which can be used for control of channel banks, may be advanced by one bit time using Transmit Sequence Advance (TSA).

For a parallel data interface, timing signals are provided at the channel rate (TCHCLK) and at the frame rate (TCHSYNC) for clocking data interface circuits.

Data Output. The serial PCM data is clocked out of the transmitter on the rising edge of TCLK and is available on two outputs simultaneously (TNRZ, TPOS and TNEG). TNRZ provides a standard, nonreturn-to-zero (NRZ) TTL level version of the data. TPOS and TNEG carry the same NRZ TTL level data as TNRZ except that the 1s are routed alternately to TPOS and TNEG. This facilitates the translation into the Alternate Mark Inversion (AMI) line code, where 1s are represented alternately as positive and negative pulses.

Loopback. The outputs TPOS and TNEG may be internally connected to RPOS and RNEG (TLOOP high) for loopback testing. During loopback, the external TPOS and TNEG carry a continuous stream of 1s; TNRZ is unaffected.

Idle Code. Idle code (01010100) may be substituted in place of the normal channel data, on a channel-by-channel basis, using TIDLE.

HDB3 Encoding. HDB3 encoding is handled automatically by the R8070. The entire data stream, including time slots 0 and 16, is scanned for an occurrence of four consecutive zeros. Any such occurrence is replaced by the appropriate HDB3 code. The HDB3 encoder may be disabled by connecting RPOS to RNEG (and using an NRZ form of input data). This invokes the transparent mode where zeros are transmitted as zeros, regardless of the 1s density. This may be used for testing or for systems that guarantee 1s density by other means. HDB3 encoding applies only to the TPOS and TNEG outputs; TNRZ is unaffected.

Frame and Multiframe Formatting

The transmitter contains frame and multiframe counters which maintain the correct PCM format by inserting the frame alignment signal into time slot 0, and the multiframe alignment signal into time slot 16. The frame counter may be reset to bit 1, time slot 0 (TFSYNC high), and the multiframe counter may be reset to frame 0 (TMSYNC high).

Signaling

ABCD/Link Signaling. In 256S mode, the 8 bits of time slot 16 of frames 1-15 contain two sets of ABCD signaling bits for channels 1-30. The ABCD signaling bits for transmission in time slot 16 are input via TABCD or TSER—selected by TSIGMD—(Serial Interface) or T1–T8 (Parallel Interface). TTS16 may be used to gate or clock in ABCD bits from external circuits. "All 1s" may be transmitted in time slot 16 (TDAT1S high).

In 256N mode, there are 2 frames per multiframe and no multiframe alignment signal. Both time slots 16 carry data link information. If TSIGMD low, link bits are input via TSER (TLNKMD high, Serial Interface), T1–T8 (TLNKMD high, Parallel Interface) or TLINK (TLNKMD low). If TSIGMD high, the data link bits are set to 1. TTS16 may be used to clock link data to the TSER or T1–T8 inputs. TLCLK may be used to clock link data to the TLINK input.

National-, International- and Extra-Bit Signaling. The National bits are located in bits 4–8 of time slot 0 of nonframe-alignment frames. The International bit is located in bit 1 of time slot 0. The Extra bits are located in bits 5, 7 and 8 of time slot 16, frame 0.

These bits are input to the transmitter via TNBITS, TIBITS and TXBITS. For the Serial Interface, these inputs are sampled instead of TSER at the appropriate bit sampling time. TNSYNC may be used to gate the National bits to either TNBITS or TSER. For the Parallel Interface, these inputs are sampled and OR'd with the equivalent bit on the parallel inputs T1–T8. This allows either T1–T8 or TNBITS/TIBITS/TXBITS to be the source.

In 256N mode, the Extra bits are not available, as both time slots 16 carry link data.

Alarms

A Yellow Alarm is transmitted (bit 3 = 1 in time slot 0 of nonframe-alignment frames) when requested by TYEL.

CEPT Operating Mode Selection and Characteristics

Mode	Data Rate (Mbps)	Bits/Frame	Frames/Multiframe	Signaling	Zero Suppression	Mode Select Lines M1	M2	M3	M4	PCM Format
256S	2.048	256	16	Yes	HDB3	0	0	0	0	CEPT
256N			2	No	HDB3	0	1	0	0	PCM-30

Notes: HDB3: High Density Bipolar 3-zero maximum

CEPT FUNCTIONAL DESCRIPTION (Cont'd)

A Multiframe Yellow Alarm (bit 6 = 1 in time slot 16, frame 0) is automatically transmitted if an error occurs in two consecutive multiframe alignment signals, or all time slot 16 bits are 0 for at least one multiframe.

Clocks

The R8070 provides clock signals at the bit, channel, frame and multiframe rate to facilitate data clocking and timing of external circuitry.

Rate	Clock	Description
Bit	TCLK	Same period as bit time. Rising edge clocks all inputs and outputs.
Channel	TCHCLK	T1–T8 sampled at the rising edge.
Frame	TCHSYNC	High for sampling of time slot 0
	TTS16	High for sampling of time slot 16.
	TLCLK	Indicates TLINK sampling.
	TNSYNC	High for sampling of TNBITS.
Multiframe	TMAX	High for sampling of the next to last bit in multiframe.
	TMFA	High for sampling of frame 0.

RECEIVE SECTION

The receive section of the R8070 provides the synchronization, signaling and alarm indication functions required for reception of PCM data formatted according to CCITT G.732 and applicable sections of G.703.

PCM Channel Data

Data Input. Received unipolar data on RPOS, derived from the received positive pulses, and RNEG, derived from the received negative pulses, is clocked into the receiver on the rising edge of RCLK.

Data Output. The received data is clocked out on the rising edge of RCLK and is available in serial form on RSER and, if a Parallel Interface is selected, in parallel (8-bit channel) form on R1–R8.

For a serial data interface, Receive Sequence signals (RSQ1–RSQ5) specify the binary value of the current channel The sequence may be retarded by one bit-time using Receive Sequence Retard (RSR). If RSHIFT is high, the sequence is "shifted" (upper bank and lower bank channel numbers are interchanged), so that channel time slot 1 becomes 16, 2 becomes 17, and so on. Time slot 0 and time slot 16 codes remain the same.

For a parallel data interface, timing signals are provided at the channel rate (RCHCLK) and the frame rate (RCHSYNC) for clocking data interface circuits. RWIHBT is high for 2 bit times to "cover" the change of data on R1–R8. This may be used to inhibit the write signal for external memory

Loopback. Under control of TLOOP, the normal external inputs on RPOS and RNEG may be replaced with an internal loopback to the internal TPOS and TNEG. When switching in and out of loopback, resynchronization will usually take place because the two signals will not normally have identical framing.

Idle and Digital Milliwatt Codes. The normal received data may be replaced, on a channel-by-channel basis, either with Idle code (using RIDLE) or with digital milliwatt (using RMW).

HDB3 Decoding. HDB3 decoding is handled automatically by the R8070. The incoming data stream is scanned for occurrences of the HDB3 code. These are replaced with four zeros, thus restoring the original data. Both serial (RSER) and parallel (R1–R8) data outputs include HDB3 corrections.

Synchronization

The serial bit stream at RPOS and RNEG is examined by the synchronizer, and the framing pattern is located through a five-stage process that eliminates erroneous bit candidates. Synchronization is achieved in less than 10 ms.

A generalized form of the synchronization algorithm is described in the R8070 Designer's Guide (Order No. 313). After a power-up reset (PUP low for at least 16 cycles), the receiver begins to search for frame and multiframe alignment. When synchronization is achieved, the receiver monitors the frame and multiframe alignment signals for errors. A Red Alarm is generated (RRED high) if frame alignment is lost; a Multiframe Red Alarm is generated (RMRED high) if multiframe alignment is lost. The criterion for loss of frame alignment is "4 out of 5" errors in the frame alignment signal or "3 out of 5" errors plus a multiframe alignment signal error. The criterion for loss of multiframe alignment is 2 consecutive errors in the multiframe alignment signal.

The receiver can be forced to restart a synchronization search (RMRST high) or to skip a bit while synchronized (RSRCH low).

D1D and D2 high prevents resynchronization after loss of frame alignment. This mode of operation may be used during testing.

Signaling

ABCD/Link Signaling. In 256S mode, with a Serial Interface, the ABCD signaling bits, contained within time slot 16 of frames 1–15 are output on RABCD. The 8-bit serial data on RABCD contains the ABCD bits in bit positions 1–4 and repeated in bit positions 5–8, aligned with the corresponding channel currently emerging from RSER. During time slot 0, RABCD contains the multiframe alignment signal (0000) in bit positions 1–4, repeated in bit positions 5–8. During time slot 16, RABCD is not defined and should not be used.

In 256S mode, with a Parallel Interface, time slot 16 data is available in parallel on R1–R8 with the normal channel timing. External circuitry is normally used to recover the ABCD bits for each channel. Each time slot 16 (of frames 1–15) contains four signaling bits (ABCD) for each of a pair of channels. The 30 PCM channels are grouped into 15 pairs as follows: Channel 1 of the current frame with channel 16 of the previous frame; channel 2 of the current frame with channel 17 of the previous frame, etc.

CEPT FUNCTIONAL DESCRIPTION (Cont'd)

Note

The CCITT numbering scheme for the 32 time slots per frame is time slot 0 through time slot 31; 30 of these time slots (1–15 and 17–31) are occupied by 30 PCM channels, referred to as channel time slots 1–15 and 16–30.

RTS16 high indicates time slot 16 is currently available at R1–R8 or RSER.

In 256N mode, there is no multiframe alignment signal or ABCD signaling bits. Time slot 16 provides a 64 kbps data link. Link data is output in serial form on RLINK in association with the clock, RLCLK at the same continuous 64 kbps rate as the input TLINK.

RLINK1 high indicates reception of 255 consecutive 1s in the data link channel (time slot 16).

National-, International- and Extra-Bit Signaling. RNBITS, RIBITS AND RXBITS are timing signals which indicate when the respective N-, I- and X-bits are available on RSER. See the CEPT Transmit Section for bit locations.

In 256N mode, the Extra bits are not available, as both time slots 16 carry link data.

Alarms

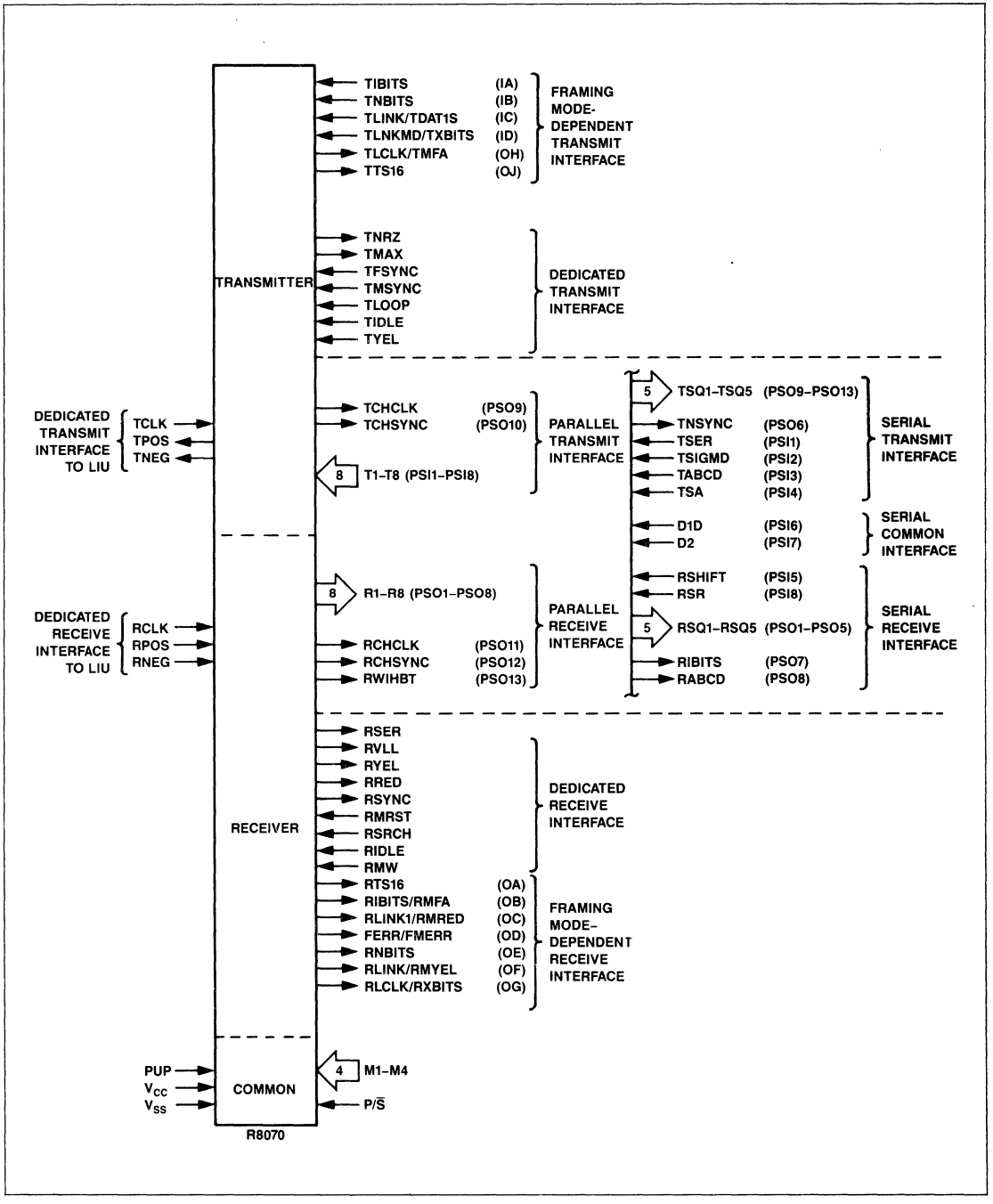
Name	Mode (N or S)	Alarm Indication
RRED	N, S	Loss of frame alignment.
RMRED	S	Loss of multiframe alignment.
RYEL	N, S	Yellow Alarm.
RMYEL	S	Multiframe Yellow Alarm.
FERR	N	Frame alignment error.
FMERR	S	Frame, multiframe alignment error.
RVLL	N, S	Bipolar violation.

Clocks

The R8070 provides clock signals at the bit, channel, frame and multiframe rate to facilitate data clocking and timing of external circuitry.

Rate	Clock	Description
Bit	RCLK	Same period as bit time. Rising edge clocks all inputs and outputs.
Channel	RCHCLK	R1–R8 changes at the rising edge.
	RWIHBT	Memory-write inhibit at R1–R8 change.
Frame	RCHSYNC	High for output of time slot 0.
	RTS16	High for output of time slot 16.
	RLCLK	Indicates RLINK data bit ready.
	RNBITS	High for output of National bits.
	RIBITS	High for output of International bits.
	RXBITS	High for output of Extra bits.
Multiframe	RSYNC	High for first bit of multiframe.
	RMFA	High during frame 0.

CEPT INTERFACE DESCRIPTION



R8070 Input/Output Signals — CEPT Modes

CEPT INTERFACE DESCRIPTION (Cont'd)

Pin Assignments—Dedicated Signals

Pin Name/Symbol	I/O	Pin No. QUIP	Pin No. PLCC	Signal Name
TCLK	I	9	10	Transmit Clock
TFSYNC	I	3	3	Transmit Frame Sync
TMSYNC	I	4	4	Transmit Multiframe Sync
TLOOP	I	16	17	Transmit Loop
TIDLE	I	15	16	Transmit Idle
TYEL	I	8	8	Transmit Yellow Alarm
TPOS	O	18	19	Transmit Unipolar Positive
TNEG	O	17	18	Transmit Unipolar Negative
TNRZ	O	19	20	Transmit Non-Return-to-Zero
TMAX	O	10	11	Transmit Maximum
RCLK	I	56	59	Receive Clock
RPOS	I	55	58	Receive Unipolar Positive
RNEG	I	54	57	Receive Unipolar Negative
RIDLE	I	53	56	Receive Idle
RMW	I	52	55	Receive Milliwatt
RMRST	I	40	42	Receive Master Reset
RSRCH	I	41	44	Receive Search
RSER	O	50	53	Receive Serial Data
RSYNC	O	37	39	Receive Sync
RVLL	O	28	30	Receive Bipolar Violation
RYEL	O	51	54	Receive Yellow Alarm
RRED	O	38	40	Receive Red Alarm
M1	I	11	12	Framing Mode Select 1
M2	I	12	13	Framing Mode Select 2
M3	I	13	14	Framing Mode Select 3
M4	I	14	15	Framing Mode Select 4
P/$\overline{S}$	I	32	34	Parallel/Serial Interface Select
PUP	I	39	41	Power-Up
V_{CC}	I	64	68	+5V Power
V_{SS}	I	33	35	Ground

Pin Assignments—Parallel/Serial Interface-Dependent Signals

Pin Name	I/O	Pin No. QUIP	Pin No. PLCC	Parallel Interface (P/$\overline{S}$ = High) Symbol	Parallel Interface (P/$\overline{S}$ = High) Signal Name	Serial Interface (P/$\overline{S}$ = Low) Symbol	Serial Interface (P/$\overline{S}$ = Low) Signal Name
PSI1	I	2	2	T1	Transmit Channel Data Bits 1–8	TSER	Transmit Serial
PSI2	I	1	1	T2		TSIGMD	Transmit Signaling Mode
PSI3	I	63	67	T3		TABCD	Transmit Signaling Input
PSI4	I	62	66	T4		TSA	Transmit Sequence Advance
PSI5	I	61	65	T5		RSHIFT	Receive Shift
PSI6	I	60	64	T6		D1D	D1D Channel Sequence Select
PSI7	I	59	63	T7		D2	D2 Channel Sequence Select
PSI8	I	58	62	T8		RSR	Receiver Sequence Retard
PSO1	O	49	52	R1	Receive Channel Data Bits 1–8	RSQ1	Receive Sequence Code Bits 1–5
PSO2	O	48	51	R2		RSQ2	
PSO3	O	47	50	R3		RSQ3	
PSO4	O	46	49	R4		RSQ4	
PSO5	O	45	48	R5		RSQ5	
PSO6	O	44	47	R6		TNSYNC[1]	Transmit National Bit Sync
PSO7	O	43	46	R7		RIBITS[1]	Receive International Bits
PSO8	O	42	45	R8		RABCD[1]	Receive Signaling Output
PSO9	O	23	24	TCHCLK	Transmit Channel Clock	TSQ1	Transmit Sequence Code Bits 1–5
PSO10	O	24	25	TCHSYNC	Transmit Channel Sync	TSQ2	
PSO11	O	25	27	RCHCLK	Receive Channel Clock	TSQ3	
PSO12	O	26	28	RCHSYNC	Receive Channel Sync	TSQ4	
PSO13	O	27	29	RWIHBT	Receive Write Inhibit	TSQ5	

Notes:
1. Different signal than T1 modes.

CEPT INTERFACE DESCRIPTION (Cont'd)

Framing Mode—Dependent Signals

Pin Name	I/O	Pin No.		256N Mode		256S Mode	
		QUIP	PLCC	Symbol	Signal Name	Symbol	Signal Name
IA	I	5	5	TIBITS	Transmit International Bits	TIBITS	Transmit International Bits
IB	I	6	6	TNBITS	Transmit National Bits	TNBITS	Transmit National Bits
IC	I	57	61	TLINK	Transmit Link	TDAT1S	Transmit Data Ones
ID	I	7	7	TLNKMD	Transmit Link Mode	TXBITS	Transmit Extra Bits
OA	O	34	36	RTS16	Receive Time Slot 16	RTS16	Receive Time Slot 16
OB	O	31	33	RIBITS	Receive International Bits	RMFA	Receive Multiframe Alignment
OC	O	30	32	RLINK1	Receive Link 1	RMRED	Receive Multiframe Red
OD	O	29	31	FERR	Framing Error	FMERR	Frame or Multiframe Error
OE	O	22	23	RNBITS	Receive National Bits	RNBITS	Receive National Bits
OF	O	35	37	RLINK	Receive Data Link	RMYEL	Receive Multiframe Yellow
OG	O	36	38	RLCLK	Receive Link Clock	RXBITS	Receive Extra Bits
OH	O	21	22	TLCLK	Transmit Link Clock	TMFA	Transmit Multiframe Alignment
OJ	O	20	21	TTS16	Transmit Time Slot 16	TTS16	Transmit Time Slot 16

CEPT INTERFACE DESCRIPTION (Cont'd)

Signal Definition — Dedicated Signals

Pin Name/ Symbol	I/O	Signal Name/Description
TCLK	I	**Transmit Clock.** TCLK is the transmitter clock input and **must be present for normal transceiver (transmitter or receiver) operation.** TCLK must be in the range 100 kHz – 3.1 MHz and will normally be 2.048 MHz for CEPT format. All inputs and outputs are clocked on the rising edge of TCLK.
TFSYNC	I	**Transmit Frame Sync.** TFSYNC high resets the bit counter to the beginning of a frame. The counter restarts on the first rising edge of TCLK after TFSYNC goes low. TFSYNC should be synchronous with TCLK to ensure setup and hold times. TFSYNC need only be applied to change the transmitter frame alignment.
TMSYNC	I	**Transmit Multiframe Sync.** TMSYNC high resets the frame counter to frame 0. TMSYNC low enables the frame counter. TMSYNC need only be applied to change the transmitter multiframe alignment. TFSYNC is normally applied with TMSYNC to align to the first bit of the multiframe.
TLOOP	I	**Transmit Loop.** TLOOP high invokes loopback mode, where TPOS and TNEG are internally routed to RPOS and RNEG, respectively. TPOS and TNEG external signals carry alternate 1s representing a continuous stream of 1s. TLOOP does not affect TNRZ. This internal looping has one bit time less delay than an equivalent external looping.
TIDLE	I	**Transmit Idle.** TIDLE high causes the idle code (01010100) to be transmitted in the next channel, in place of the normal data. This substitution continues for each channel in which TIDLE is high.
TYEL	I	**Transmit Yellow Alarm.** TYEL high causes transmission of a Yellow Alarm· Bit 3=1 in time slot 0 of nonframe-alignment frames.
TPOS, TNEG	O	**Transmit Unipolar Positive, Unipolar Negative.** TPOS and TNEG are the "unipolar-paired" TTL, NRZ outputs for transmitted data. Binary 0 is coded as a low (0) level on both outputs Binary 1 is coded as a high (1) level on TPOS or TNEG, alternately. TPOS and TNEG allow the direct generation of AMI line code in which a 1 (mark) is alternately represented as a positive or negative pulse. There is an 8-bit throughput delay between the TSER input and the TPOS/TNEG outputs.
TNRZ	O	**Transmit Non-Return-to-Zero.** TNRZ is the TTL, NRZ output for transmitted data. This output is unaffected by TLOOP or by HDB3 zero suppression coding. There is an 8-bit throughput delay between the TSER input and the TNRZ output.
TMAX	O	**Transmit Maximum.** TMAX is high for one bit time per multiframe coincident with the sampling of the next to last serial bit of a multiframe.
RCLK	I	**Receive Clock.** RCLK is the receiver clock input and must be present for normal transceiver operation. All inputs and outputs are clocked on the rising edge of RCLK RCLK must be in the range 100 kHz – 3.1 MHz and will normally be 2.048 MHz for CEPT format
RPOS, RNEG	I	**Receive Unipolar Positive, Unipolar Negative.** RPOS and RNEG are the inputs for received data recovered from the positive and negative AMI line pulses. RPOS and RNEG should have TTL levels and may be of either NRZ or RZ form. If RPOS is strapped to RNEG (and given composite RPOS/RNEG data) the first occurrence of a 1 will invoke the transparent mode in which HDB3 zero suppression is disabled in both the receiver and the transmitter.
RIDLE	I	**Receive Idle.** RIDLE high causes data in the next received channel to be substituted with the idle code (01010100). The substitution continues for each channel in which RIDLE is high RIDLE and RMW should not be high simultaneously.
RMW	I	**Receive Milliwatt.** RMW high causes data in the next received channel to be substituted with the digital milliwatt code; a repeating pattern of eight 8-bit bytes that translate into a 1 kHz signal at a level of 1 mW The substitution is performed for each channel in which RMW is high. RMW and RIDLE should not be high simultaneously
RMRST	I	**Receive Master Reset.** RMRST high resets the master state sequencer in the synchronizer to its initial (WAIT) state. RMRST low allows synchronization to proceed.
RSRCH	I	**Receive Search.** RSRCH low prevents the master state sequencer in the synchronizer from proceeding out of the WAIT state. It does not force the synchronizer to the WAIT state (see RMRST). If RSRCH is low while the receiver is in frame alignment (RRED low), bit 5 of time slot 0, frame 0 is skipped This allows recentering of elastic stores.

CEPT INTERFACE DESCRIPTION (Cont'd)

Signal Definition — Dedicated Signals (Cont'd)

Pin Name/ Symbol	I/O	Signal Name/Description
RSER	O	**Receive Serial Data.** RSER is the serial data output including HDB3 decoding. The throughput delay from RPOS/RNEG to RSER is 14 cycles of RCLK. RSER is always valid, regardless of the synchronizer state.
RSYNC	O	**Receive Sync.** RSYNC is high during the first bit of each multiframe while the receiver is synchronized
RVLL	O	**Bipolar Violation.** RVLL high indicates that the 1 currently at RSER resulted from a bipolar violation.
RYEL	O	**Receive Yellow Alarm.** RYEL high indicates a received Yellow Alarm. Bit 3 = 1 in time slot 0 of nonframe-alignment frames.
RRED	O	**Receive Red Alarm.** RRED high indicates loss of frame alignment. RRED low indicates correct frame alignment. Multiframe alignment is separately indicated by RMRED.
M1–M4	I	**Framing Mode Select.** M1–M4 select the framing mode as follows (See CEPT Mode Selection Table for additional mode information)· **M1 M2 M3 M4 CEPT Mode** 0 0 0 0 256S; 0 1 0 0 256N
P/$\overline{S}$	I	**Parallel/Serial Interface Select.** P/$\overline{S}$ selects parallel (P/$\overline{S}$ high) or serial (P/$\overline{S}$ low) operation of the PSI1–PSI8 and PSO1–PSO13 pins.
PUP	I	**Power-up.** PUP initializes the R8070 transmitter and receiver. It includes TFSYNC, TMSYNC and RMRST reset functions. PUP sets all outputs, except OJ, to a high-impedance state, to facilitate testing of peripheral circuitry.
V_{CC}	I	**+5V Power.** +5 VDC power
V_{SS}	I	**Ground.** Power and signal ground.

CEPT INTERFACE DESCRIPTION (Cont'd)

Signal Definition — Parallel/Serial Interface-Dependent Signals

a. Parallel Interface (P/$\overline{S}$ = High)

Pin Name/ Symbol	I/O	Symbol	Signal Name/Description
PSI1–PSI8	I	T1–T8	**Transmit Channel Data Bits 1–8.** T1–T8 are the parallel inputs for channel data and, optionally, link data They are clocked into the transmitter at the rising edge of TCHCLK, by the rising edge of TCLK. The falling edge of TCHCLK may be used to present the next channel data at T1–T8
PSO1–PSO8	O	R1–R8	**Receive Channel Data Bits 1–8.** R1–R8 are the parallel outputs for channel data. The channel data is available for a complete channel time and is updated at the rising edge of RCHCLK The falling edge of RCHCLK may be used to clock this data into external buffers R1–R8 are only valid while the receiver is synchronized; RSER, the serial data output, is always available and always valid
PSO9	O	TCHCLK	**Transmit Channel Clock.** TCHCLK is a channel-rate clock whose rising edge indicates that parallel data on T1–T8 is being sampled The falling edge is used to present the next channel's data on T1–T8. TCHCLK is low for 4 bit times
PSO10	O	TCHSYNC	**Transmit Channel Sync.** TCHSYNC is a frame-rate signal which is high for 8 bit times The rising edge precedes the sampling of time slot 0 by one bit time. The falling edge precedes time slot 1 sampling by one bit time
PSO11	O	RCHCLK	**Receive Channel Clock.** RCHCLK is a channel-rate clock where rising edge indicates that new channel data has been output to R1–R8. The falling edge may be used to clock this data into external buffers. RCHCLK is low for 4 bit times
PSO12	O	RCHSYNC	**Receive Channel Sync.** RCHSYNC is a frame-rate signal which is high for 8 bit times The rising edge occurs one bit time after the output time slot 0 of data on R1–R8 The falling edge occurs one bit time after the output time slot 1 of data on R1–R8
PSO13	O	RWIHBT	**Receive Write Inhibit.** RWIHBT is a channel-rate signal, 2 bit times high, which "covers" the change of parallel data on R1–R8 RWIHBT is high for one bit time before and after the rising edge of RCHCLK

CEPT INTERFACE DESCRIPTION (Cont'd)

Signal Definition — Parallel/Serial Interface-Dependent Signals (Cont'd)

b. Serial Interface ($P/\overline{S}$ = Low)

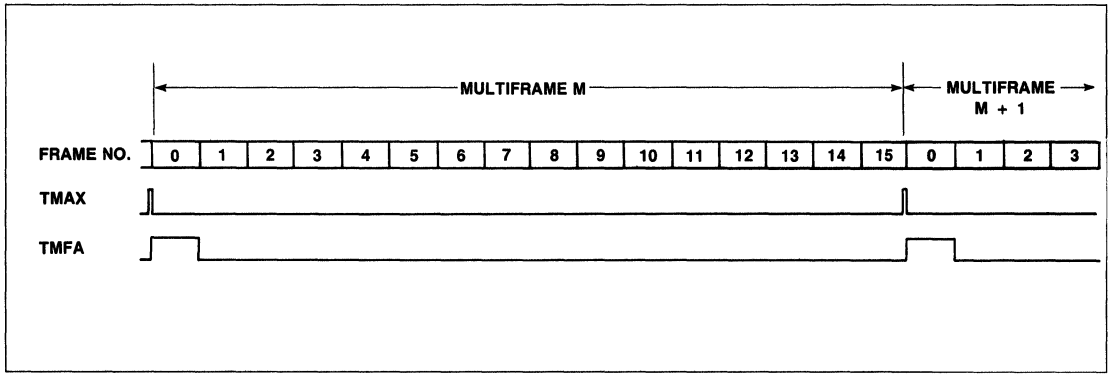
Pin Name/ Symbol	I/O	Symbol	Signal Name/Description
PSI1	I	TSER	**Transmit Serial.** TSER is the serial input for the channel data and, optionally, signaling data.
PSI2	I	TSIGMD	**Transmit Signaling Mode.** In mode 256S: TSIGMD low selects TABCD as the source for ABCD signaling bits of time slot 16, TSIGMD high selects TSER as the source. In mode 256N: TSIGMD low specifies TLNKMD as the selector for the source of time slot 16 data link signaling, TSIGMD high causes all 1s to be transmitted in time slot 16.
PSI3	I	TABCD	**Transmit Signaling Input.** TABCD is the input for ABCD signaling in time slot 16.
PSI4	I	TSA	**Transmit Sequence Advance.** TSA high advances the standard timing of TSQ1–TSQ5 and TSIGSQ by one bit time.
PSI5	I	RSHIFT	**Receive Shift.** RSHIFT high shifts the RSQ1–RSQ5 sequence of channel numbers from 1 to 16, 2 to 17, ... 15 to 30. Time slot 0 remains as 00000, time slot 16 remains as 11111.
PSI6, PSI7	I	D1D, D2	**Channel Sequence Select.** D1D and D2 channel assignments are not required for CEPT; set to 0,0 for normal operation; set to 1,1 for synchronization lock which inhibits resynchronization after loss of frame alignment.
PSI8	I	RSR	**Receive Sequence Retard.** RSR high delays the standard timing of RSQ1–RSQ5 and RSIGSQ by one bit time.
PSO1–PSO5	O	RSQ1–RSQ5	**Receive Sequence Code Bits 1-5.** RSQ1–RSQ5 is the binary value of the currently received channel (1–30), plus time slot 0 (00000) and time slot 16 (11111).
PSO6	O	TNSYNC	**Transmit National Bit Sync.** TNSYNC goes high to indicate sampling of the National bits (bits 4–8 of time slot 0 of nonframe-alignment frames). TNSYNC rising edge coincides with the sampling of bit 3; the falling edge coincides with the sampling of bit 8, of the above time slot.
PSO7	O	RIBITS	**Receive International Bits.** RIBITS high indicates that the International bit (bit 1, time slot 0) is present at RSER.
PSO8	O	RABCD	**Receive Signaling Output.** RABCD is the output of the received ABCD signaling bits for the channel currently emerging from RSER.
PSO9–PSO13	O	TSQ1–TSQ5	**Transmit Sequence Code Bits 1-5.** TSQ1–TSQ5 is the binary value of the currently sampled channel (1–30), plus time slot 0 (00000) and time slot 16 (11111).

CEPT INTERFACE DESCRIPTION (Cont'd)

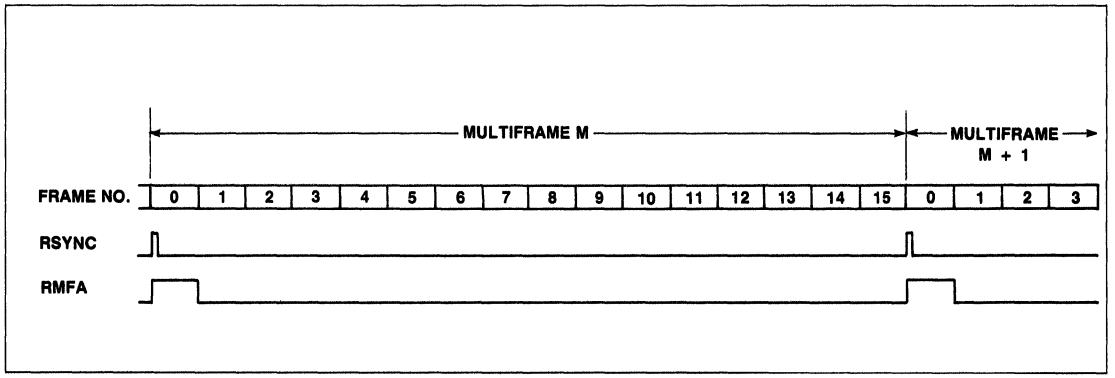
Signal Definitions — Framing Mode-Dependent Signals

Pin Name	I/O	Signal Symbol	Mode 256N	Mode 256S	Signal Name/Description
IA	I	TIBITS	•	•	**Transmit International Bits.** TIBITS is the I-bit input for International-bit signaling
IB	I	TNBITS	•	•	**Transmit National Bits.** TNBITS is the N-bit input for National-bit signaling
IC	I	TLINK	•	—	**Transmit Link.** TLINK is the serial data link input The data rate is 64 kbps.
		TDAT1S	—	•	**Transmit Data Ones.** TDAT1S high selects "all 1s" transmission in time slot 16
ID	I	TLNKMD	•	—	**Transmit Link Mode.** TLNKMD selects the source for time slot 16 signaling If low, TLINK is the input for time slot 16 signaling. If high, T1–T8 (parallel interface) or TSER (serial interface) is the input for time slot 16 signaling
		TXBITS	—	•	**Transmit Extra Bits.** TXBITS is the X-bit input for Extra-bit signaling in time slot 16
OA	O	RTS16	•	•	**Receive Time Slot 16.** RTS16 is high during time slot 16
OB	O	RIBITS	•	—	**Receive International Bits.** RIBITS high indicates that the International bit (bit 1, time slot 0) is present at RSER
		RMFA	—	•	**Receive Multiframe Alignment.** RMFA is high during frame 0, which contains the multiframe alignment signal
OC	O	RLINK1	•	—	**Receive Link 1.** RLINK1 high indicates the reception of 255 consecutive 1s in time slot 16
		RMRED	—	•	**Receive Multiframe Red.** RMRED high indicates 2 consecutive multiframe alignment errors or "all time slot 16 bits low" for at least one multiframe. When RMRED is high, a Multiframe Yellow Alarm is automatically transmitted as bit 6 = 1 in time slot 16, frame 0
OD	O	FERR	•	—	**Framing Error.** FERR high indicates an error in the current framing bit at RSER
		FMERR	—	•	**Frame or Multiframe Error.** FMERR high in bit 1, time slot 0 indicates a frame error, high in bit 1, time slot 16 indicates a multiframe error
OE	O	RNBITS	•	•	**Receive National Bits.** RNBITS high indicates that a National bit is present at RSER (bits 4–8 of a nonframe-alignment time slot 0)
OF	O	RLINK	•	—	**Receive Data Link.** RLINK is the serial data link output The data rate matches that of TLINK (64 kbps).
		RMYEL	—	•	**Receive Multiframe Yellow.** RMYEL is the received Multiframe Yellow Alarm signal, bit 6 of time slot 16, frame 0 RMYEL high indicates a Multiframe Yellow Alarm
OG	O	RLCLK	•	—	**Receive Link Clock.** RLCLK is a square wave whose rising edge occurs 2 bit times after the received data on RLINK
		RXBITS	—	•	**Receive Extra Bits.** RXBITS high indicates an Extra bit is present at RSER (bits 5, 7 and 8 of time slot 16, frame 0)
OH	O	TLCLK	•	—	**Transmit Link Clock.** TLCLK is a square wave whose rising edge occurs 4 bit times after the sampling of TLINK.
		TMFA	—	•	**Transmit Multiframe Alignment.** TMFA is high during the data sampling of frame 0, which contains the multiframe alignment signal.
OJ	O	TTS16	•	•	**Transmit Time Slot 16.** TTS16 is high during the sampling of time slot 16.

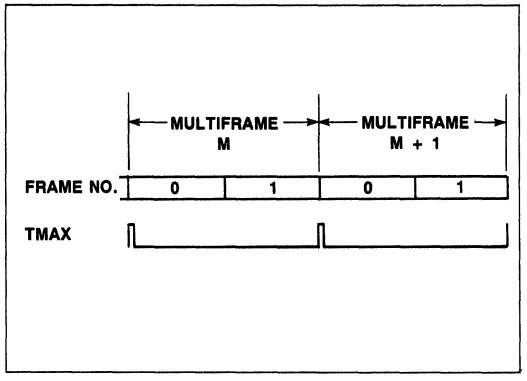
CEPT WAVEFORMS



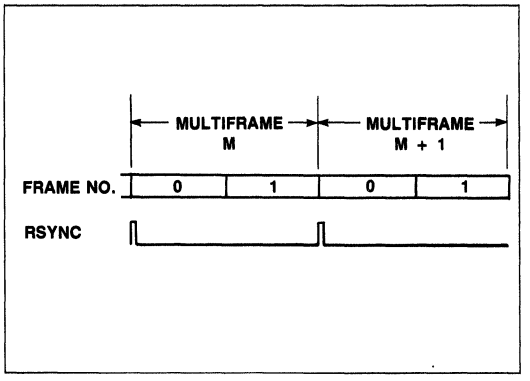
Transmit-Multiframe—Mode 256S



Receive-Multiframe—Mode 256S

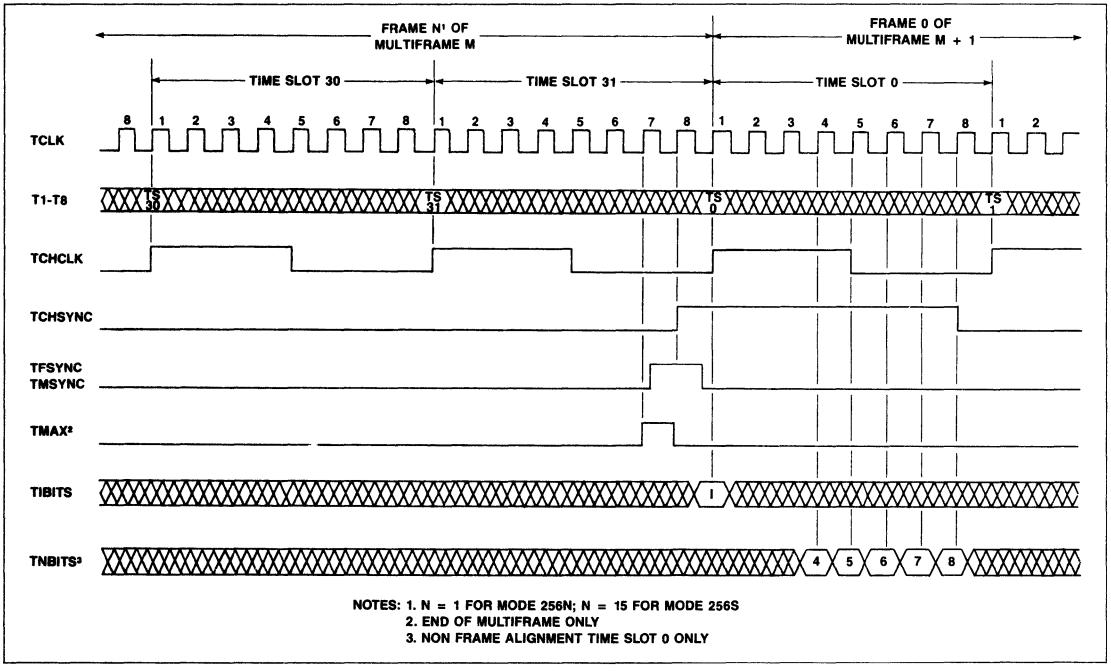


Transmit-Multiframe—Mode 256N

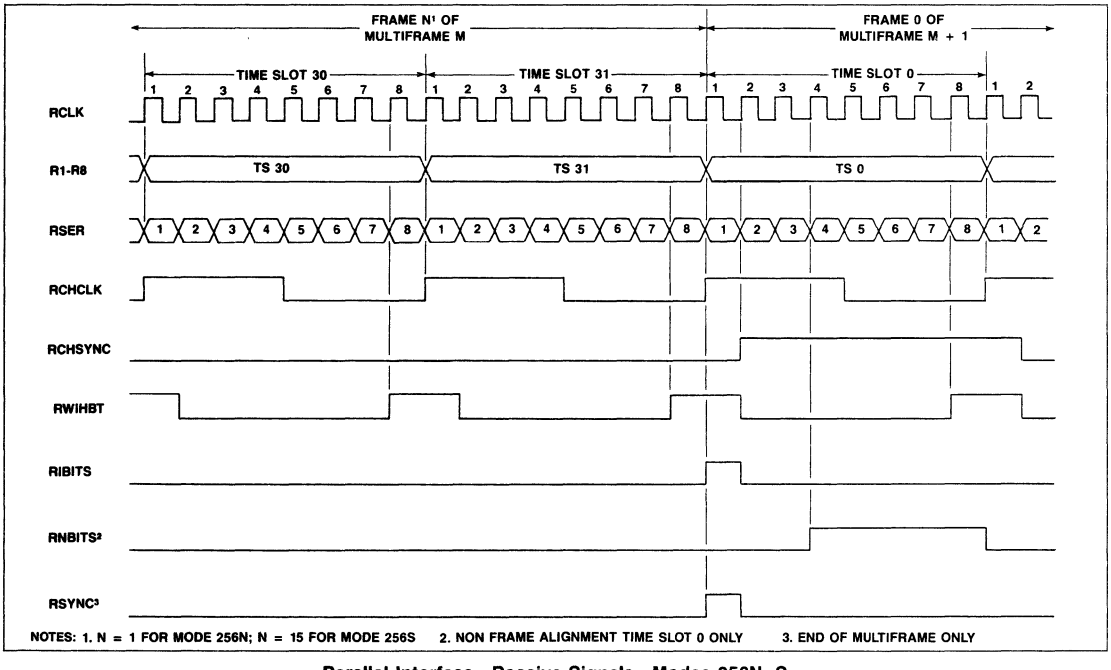


Receive-Multiframe—Mode 256N

CEPT WAVEFORMS (Cont'd)

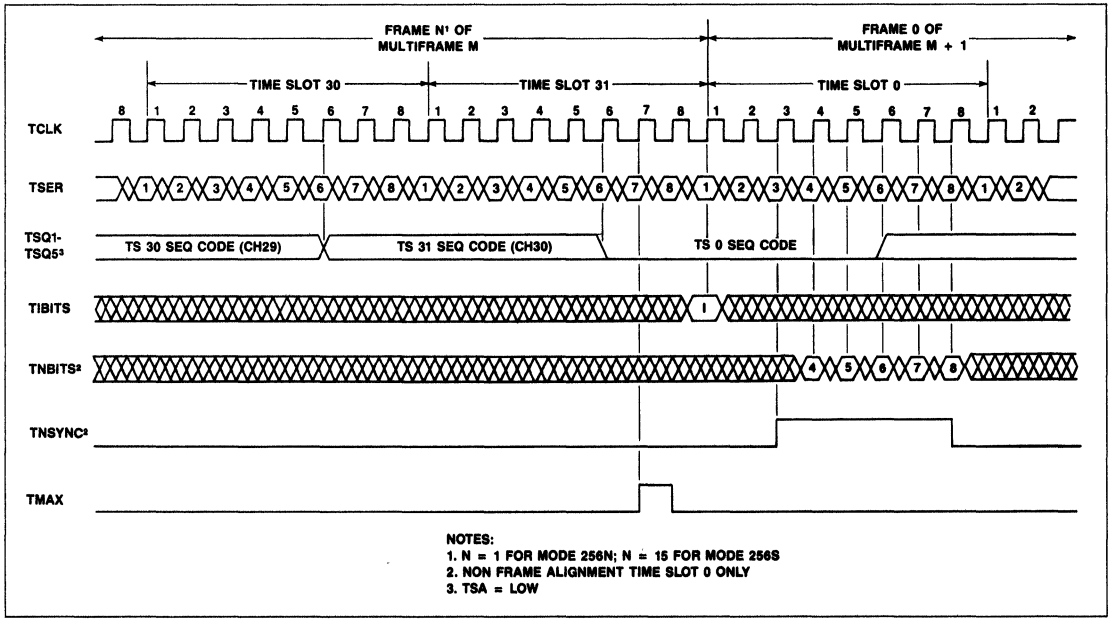


Parallel Interface—Transmit Signals—Modes 256N, S

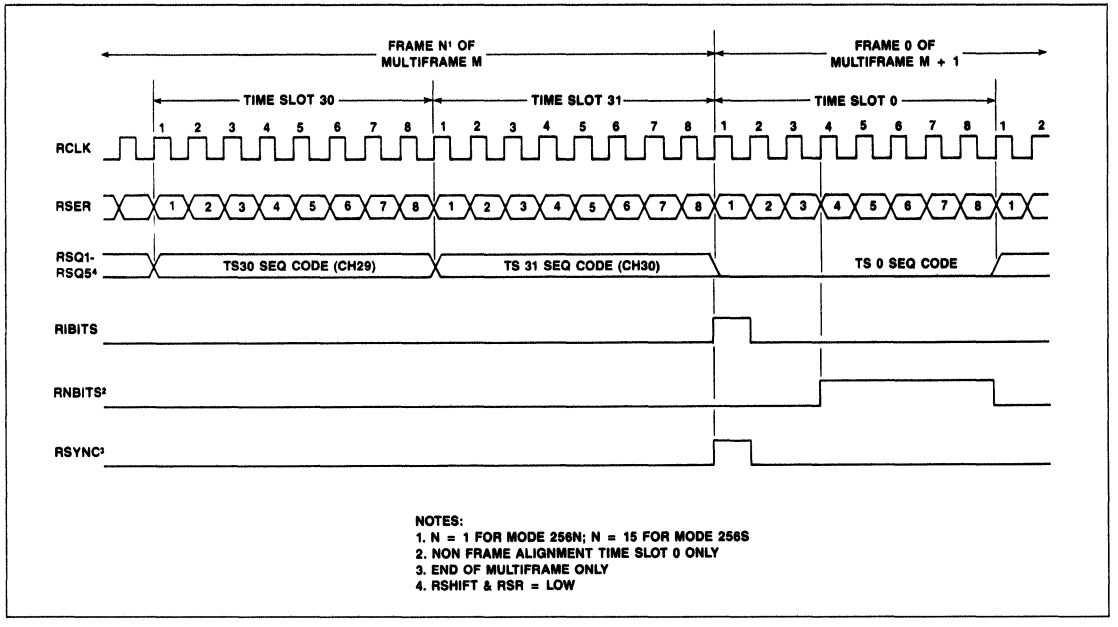


Parallel Interface—Receive Signals—Modes 256N, S

CEPT WAVEFORMS (Cont'd)



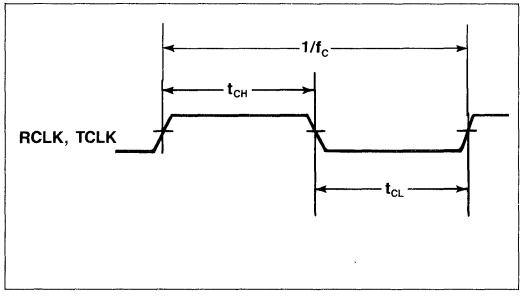
Serial Interface—Transmit Signals—Modes 256N, S



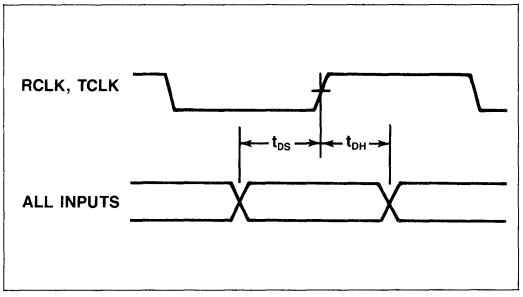
Serial Interface—Receive Signals—Modes 256N, S

SWITCHING CHARACTERISTICS

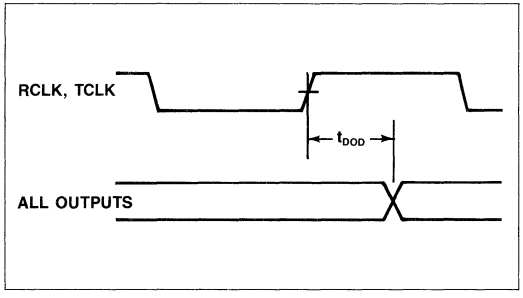
Parameters	Symbol	Min	Typ	Max	Units
Clock Frequency	f_C	0 1	—	3 1	MHz
Clock Pulse Width High	t_{CH}	160	—	—	ns
Clock Pulse Width Low	t_{CL}	160	—	—	ns
Input Data Setup Time	t_{DS}	60	—	—	ns
Input Data Hold Time	t_{DH}	60	—	—	ns
Output Data Delay Time	t_{DOD}	—	—	125	ns



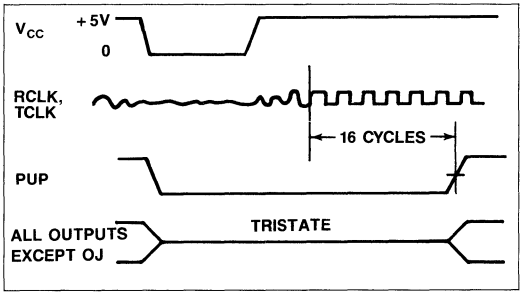
Minimum Clock Pulse Widths



Input Data Setup and Hold Times



Output Data Delay Time



Minimum Reset Time

REFRAME TIMING

Mode	Minimum	Average	Maximum	Unit
193N	1 5	2 7	3 8	ms
197N	1 5	2 7	3 8	ms
193S	1 0	1 6	2 2	ms
197S	1 0	1 6	2 2	ms
193E	4 5	6 7	8 5	ms
193F	4 5	6 7	8 5	ms
256N	3	60	1 3	ms
256S	3	60	1 3	ms

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+4.75 to 5.25	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+4.75 to 5 25	Vdc
Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C

ELECTRICAL CHARACTERISTICS

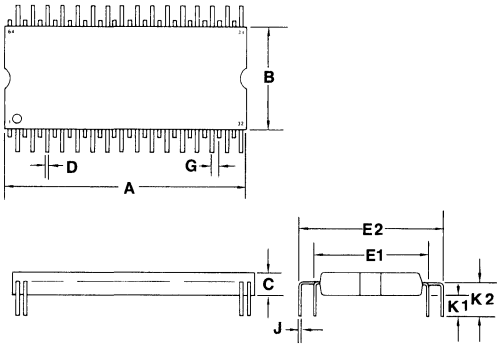
Parameter	Symbol	Min	Max	Unit	Test Condition
Input Low Voltage	V_{IL}	−0 3	0.8	V	
Input High Voltage	V_{IH}	2 0	V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}	—	0 4	V	I_{LOAD} = +1.6 mA
Output High Voltage TTL CMOS	V_{OH}	 2.4 3.5	 — —	V	 I_{LOAD} = −100μA I_{LOAD} = −100μA
Output Low Current	I_{OL}	+1 6	—	mA	V_{OL} = 0.4V
Output High Current	I_{OH}	−100	—	μA	V_{OH} = 3.5V
Input Capacitance	C_{IN}	—	5	pF	
Output Capacitance	C_{OUT}	—	50	pF	
Power Dissipation	P_{WD}	—	100	mW	

REFERENCE DATA

For detail information refer to the R8070 T1/CEPT PCM Transceiver Designer's Guide (Order Number 313).

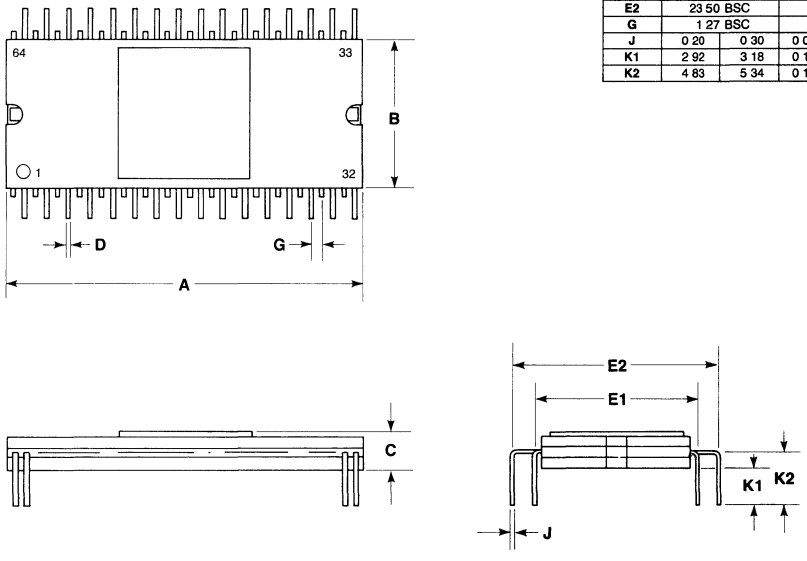
PACKAGE DIMENSIONS

64-PIN PLASTIC QUAD IN-LINE PACKAGE (QUIP)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41 10	41 61	1 618	1 638
B	17 02	17 23	0 670	0 690
C	3 56	4 58	0 140	0 180
D	0 48	0 56	0 018	0 022
E1	19 05 BSC		0 750 BSC	
E2	23 50 BSC		0 925 BSC	
G	1 27 BSC		0 050 BSC	
J	0 18	0 33	0 007	0 013
K1	2 92	3 18	0 115	0 125
K2	4 83	5 34	0 190	0 210

64-PIN CERPAC QUAD IN-LINE PACKAGE (QUIP)

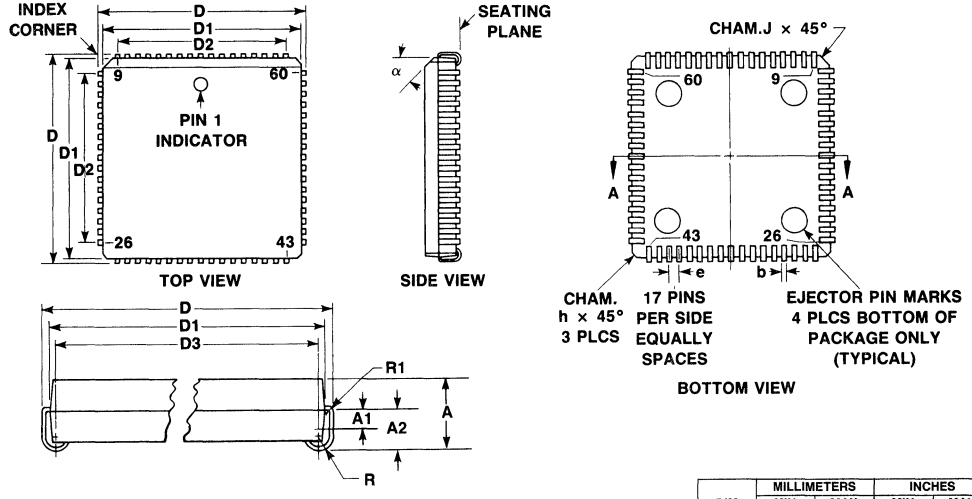


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	40 77	41 28	1 605	1 625
B	16 76	17 27	0 660	0 680
C	3 56	4 58	0 140	0 180
D	0 48	0 56	0 018	0 022
E1	19 05 BSC		0 750 BSC	
E2	23 50 BSC		0 925 BSC	
G	1 27 BSC		0 050 BSC	
J	0 20	0 30	0 008	0 012
K1	2 92	3 18	0 115	0 125
K2	4 83	5 34	0 190	0 210

6

PACKAGE DIMENSIONS (Cont'd)

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4 14	4 39	0 163	0 173
A1	1 37	1 47	0 054	0 058
A2	2 31	2 46	0 091	0 097
b	0 457 TYP		018 TYP	
D	25 02	25 27	985	995
D1	24 00	24 26	945	955
D2	20 19	20 45	795	805
D3	23 24	23 50	915	925
e	1 27 BSC		050 BSC	
h	0 25 TYP		010 TYP	
J	1 15 TYP		045 TYP	
α	45° TYP		45° TYP	
R	0 89 TYP		035 TYP	
R1	0 25 TYP		010 TYP	

R8070A
T1/CEPT PCM Transceiver

INTRODUCTION

This data sheet addendum describes the enhanced framing procedure implemented in the R8070A version of the R8070 T-1/PCM-30 Transceiver device. This enhancement is only applicable to the 193E and 193F modes associated with the North American Extended Superframe (ESF) standard.

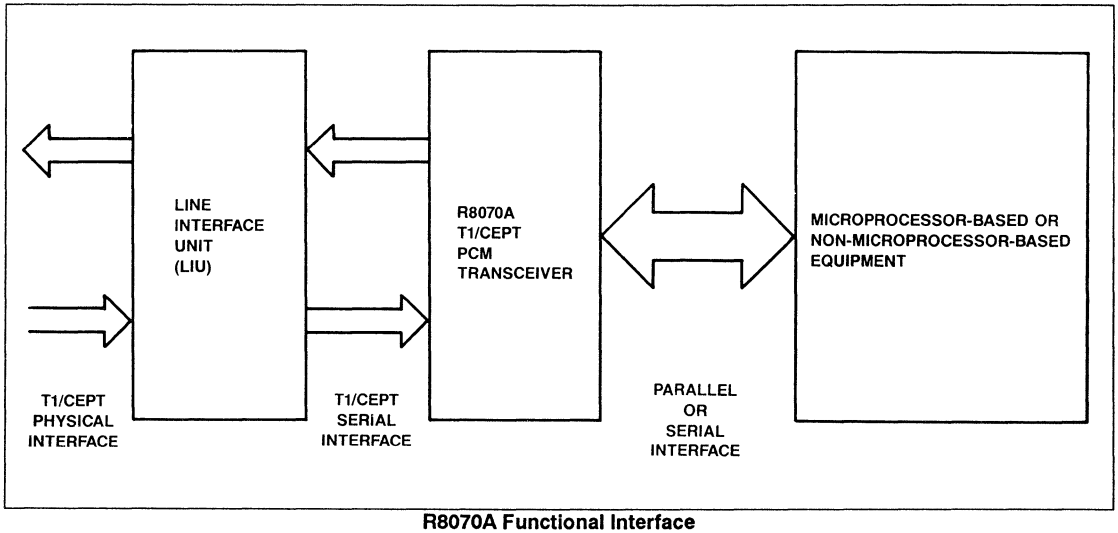
The improvements incorporated in the R8070A are transparent to the user, as well as interfacing hardware and software. All designs using the R8070 can use the R8070A to improve reliability.

FUNCTIONAL DESCRIPTION

The R8070A is functionally and electrically identical to the R8070 except for the frame synchronization procedure when the device is configured in an Extended Superframe mode (193E or 193F). An extended CRC-6 check interval on the order of 8 - 12 multiframes has been added to the master state sequence. This extended period starts at the beginning of the "SYNC" state.

The extended CRC-6 check interval causes the R8070A to reframe if two consecutive CRC-6 block errors are detected.

These enhancements ensure extremely robust framing operation against false framing on data patterns that constantly mimic the ESF frame pattern.



R8070A Functional Interface

Rockwell

R8071
ISDN/DMI Link Layer Controller

APPLICATIONS

ISDN
- PRIMARY RATE INTERFACES
- BASIC RATE D-CHANNEL CONTROLLER

DMI
- HOST INTERFACE
- PBX TRUNKSIDE ADAPTERS

INTRODUCTION

The Rockwell R8071 ISDN/DMI Link Layer Controller device multiplexes/demultiplexes up to 32 high speed data channels to support implementation of the Digital Multiplexed interface (DMI) between a digital PBX and a host computer (Figure 1). The R8071 operates at layer 2 (data link protocol level) of the Open Systems Interconnection (OSI) reference model recommended by the International Organization for Standardization (ISO) and resides between the R8070 T1/CEPT PCM Transceiver and a buffer memory shared with one or more host processors.

The R8071 processes transmit and receive data on a T1 communications medium with DS1 signaling at 1.544 Mbps in the D4 framing format or the F_e extended framing format, or at 2.048 Mbps in the CEPT PCM 30 carrier format. The device provides HDLC formatting functions for synchronous data and manages buffer memory for each of the active data channels, including the common signaling channel, using simple linked-list structures.

The R8071 is compatible with the Integrated Services Digital Network (ISDN) specified by the International Telegraph and Telephone Consultative Committee (CCITT) and supports connections of computers to the ISDN at the primary rate. It also supports modes 0, 1, 2 and 3 of the DMI protocol for clear channel transmission of data at 64 kbps, 56 kbps synchronous, standard data rates up to 19.2 kbps, and 64 kbps virtual circuit protocol using LAPD, respectively.

The R8071 device provides additional functions which support X.30 and X.31 rate adaption as well as ISDN hyperchannels. The device is also compatible with HDLC, SNA SDLC, X.25, X.75, LAPB and LAPD protocols. These features allow the use of the R8071 in applications that go beyond the host-end DMI interface.

The R8071 complements the Rockwell R8070 T1/CEPT PCM Transceiver, which operates at layer 1 (physical interface level) of the OSI reference model, and provides basic T1 framing and maintenance functions of the DMI link.

The R8071 finds applications in widely diverse areas of telecommunications (including TDM machines, Central Office switches, and PBX), as well as the basic host computer-PBX DMI links. In ISDN switching applications, the R8071 can function as a multiplexed controller for as many as 32 ISDN basic access "D" channels, and can substantially off-load LAPD processing from the Switch Central Control.

FEATURES

- DMI implementation, solidly based on T1 and CEPT primary rate carrier with designed-in compatibility with ISDN, is the key to world-wide networking
  - — T1/CEPT provides the link beyond the central office or PBX
  - — ISDN provides the phone/terminal to the central office or PBX basic access link
  - — DMI provides the computer to computer, and computer to PBX, link
- R8071 single chip CMOS monolithic device simplifies ISDN/DMI implementation
- Provides up to 32 full duplex channels with HDLC/SDLC protocol formatting
- Supports all four DMI B channel data options:
  - — Mode 0 (clear channel 64 kbps synchronous)
  - — Mode 1 (56 kbps synchronous data without or with HDLC protocol)
  - — Mode 2 (up to 19.2 kbps synchronous or asynchronous)
  - — Mode 3 (64 kbps virtual circuit service)
- Supports both DMI D channel signaling options
  - — Bit-oriented signaling (BOS)
  - — Message-oriented signaling (MOS)
- Compatible with 1.544 Mbps T1 D4 and extended framing format as well as 2.048 Mbps CEPT PCM 30 carrier format
- Supports both flag stuffing (I.462, DMI mode 2) and RA2 intermediate rate adaption (I.460, X.30, V.110 or ECMA-102)
- Provides ISDN standard hyperchannel options (CCITT I.412):
  - — In T1: H0 (384 kbps)
    H11 (1.536 Mbps)
  - — In CEPT PCM 30: H12 (1.920 Mbps)
- Compatible with HDLC, SNA SDLC, X.25, X.75, LAPB and LAPD protocols
- On-board buffer memory management function
- On-board CRC-16 generation and checking, automatic flag detection and transmission, and zero-bit insertion and deletion
- Simple interface to Rockwell R8070 T1/CEPT PCM Transceiver
- Available in 64-pin quad in-line (QUIP) and 68-pin plastic leaded chip carrier (PLCC) packages
- Operates from a single +5 Vdc supply

Document No. 29300N18 **Data Sheet** **Order No. 318**
Rev. 2, December 1988

ORDERING INFORMATION

Part Number:
R8071

Temperature
Blank = 0°C to +70°C

Package
P = 64-Pin Plastic QUIP
S = 64-Pin Cerpac QUIP
J = 68-Pin Plastic Leaded Chip Carrier (PLCC)
JC = 68-Pin Ceramic Leaded Chip Carrier (CLCC)
G = 68-Pin Pin Grid Array (PGA)

INTERFACE

The R8071 ISDN/DMI Link Layer Controller transmits data to, and receives data from, an R8070 T1/CEPT PMC Transceiver (or compatible framer device) in ISDN/DMI rate and formats as illustrated in Figure 1. It transfers the data in 8-bit parallel form to and from an external buffer memory shared by a host computer system. (The external buffer memory is referred to as shared memory and the host computer system is referred to as the host.) The R8071 interface signals are functionally grouped in Figure 2. The R8071 pin assignments are shown in Figure 3 and the R8071 interface signals are defined in Table 1.

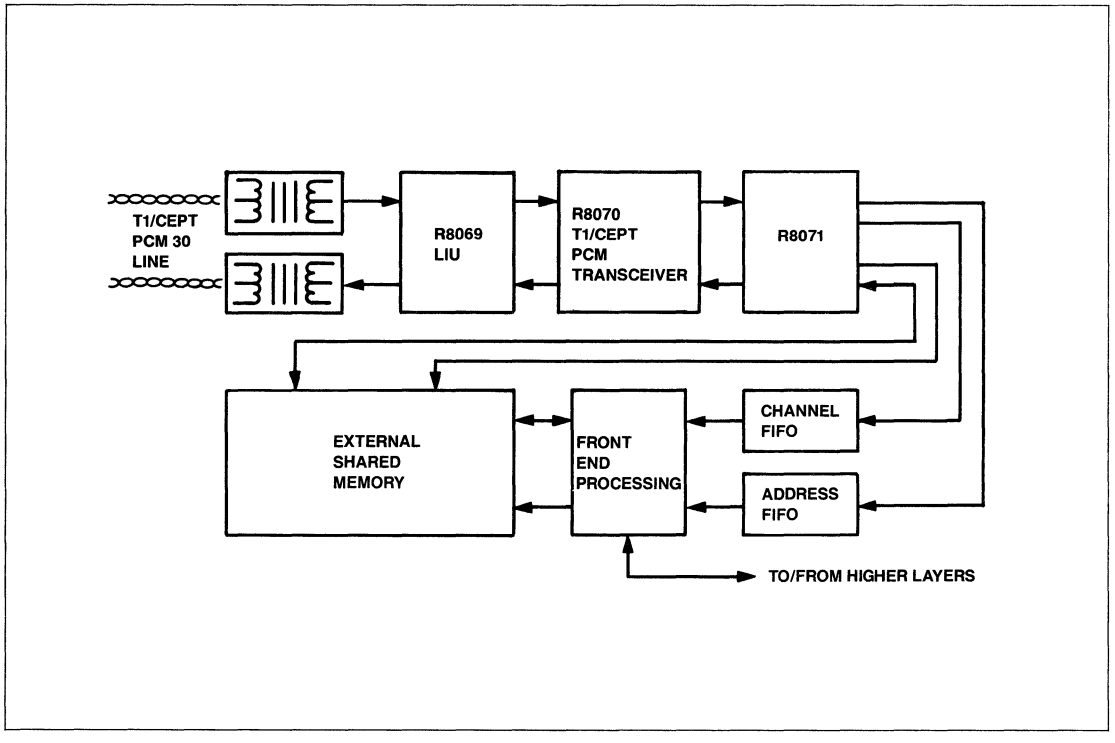


Figure 1. Functional Architecture for Host ISDN/DMI Primary Rate Access, PBX ISDN/DMI Trunkside Adapter

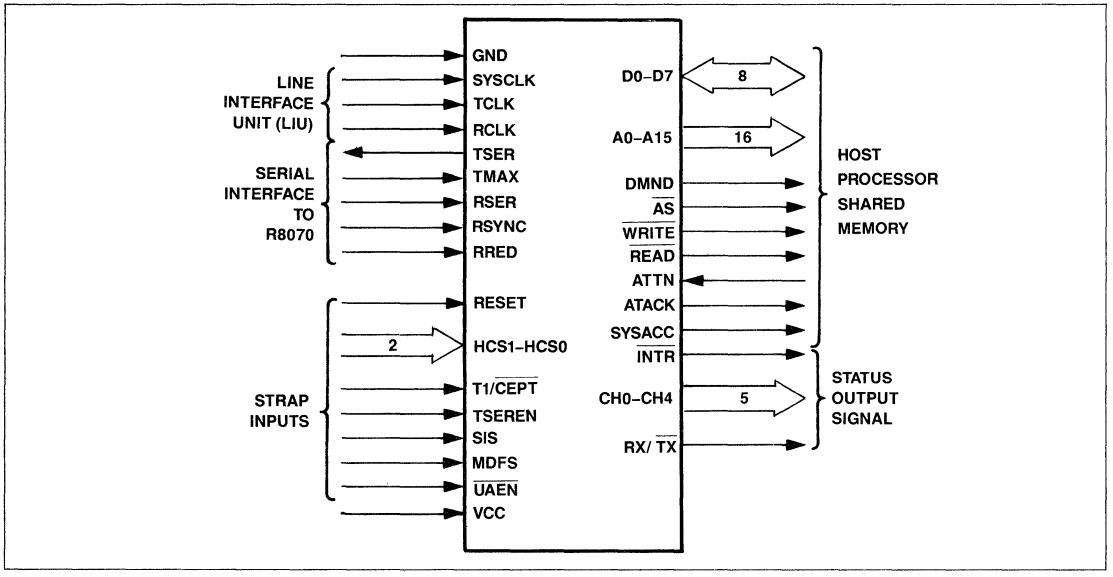
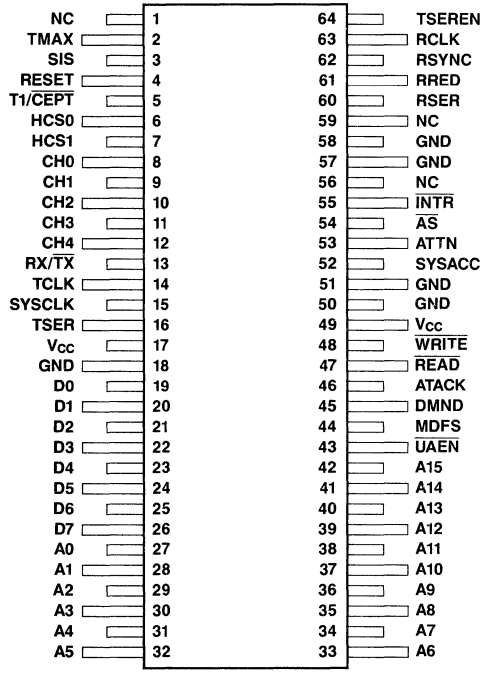
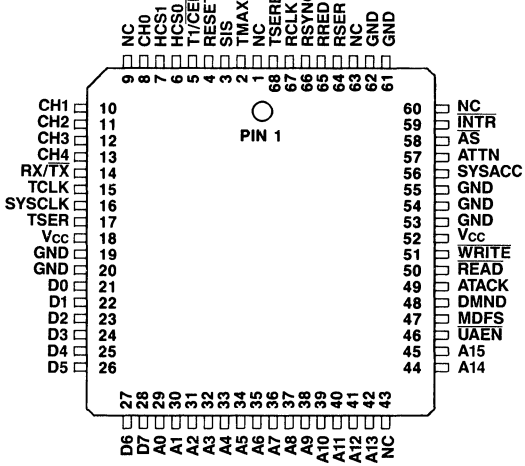


Figure 2. R8071 Interface Signals

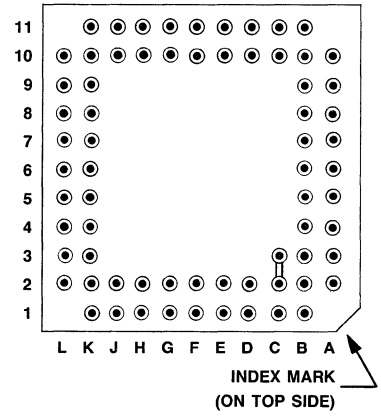


64-Pin QUIP



68-Pin PLCC

Back View of Pin Grid Array



PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A2	NC	B9	MDFS	F10	A6	K4	TCLK
A3	INTR	B10	A15	F11	A7	K5	TSER
A4	ATTN	B11	A14	G1	RESET	K6	VCC
A5	BMRT	C1	RSER	G2	SIS	K7	GND
A6	GND	C2	NC	G10	A4	K8	D1
A7	VCC	C10	A12	G11	A5	K9	D3
A8	READ	C11	A13	H1	HCS0	K10	D6
A9	DMND	D1	RSYNC	H2	T1/CEPT	K11	D7
A10	UAEN	D2	RRED	H10	A2	L2	CH3
B1	GND	D10	A10	H11	A3	L3	RX/TX
B2	GND	D11	A11	J1	CH0	L4	SYSCLK
B3	AS	E1	TSEREN	J2	HCS1	L5	VCC
B4	SYSACC	E2	RCLK	J10	A0	L6	GND
B5	GND	E10	A8	J11	A1	L7	D0
B6	VCC	E11	A9	K1	CH1	L8	D2
B7	WRITE	F1	TMAX	K2	CH2	L9	D4
B8	ATACK	F2	NC	K3	CH4	L10	D5

68-Pin PGA

NC = NO CONNECTION TO BE MADE TO THIS PIN.

Figure 3. R8071 Pin Assignments

Table 1. R8071 Interface Signal Definitions

Symbol	I/O	Signal Name/Description
Memory Interface		
D0–D7	I/O	**Memory Data Lines.** Bidirectional 8-bit memory data bus between the R8071 and the shared memory D0 is the LSB and D7 is the MSB
A0–A15	O	**Memory Address Lines.** Output lines to the shared memory A0 is the LSB and A15 is the MSB
DMND	O	**Memory Demand.** Active high output to shared memory The R8071 accesses shared memory within one TCLK period after assertion (rising edge) of DMND DMND is negated at completion of the memory access cycle
$\overline{AS}$	O	**Memory Address Strobe.** A valid memory address is present on the memory address lines at the falling edge of the active low $\overline{AS}$
$\overline{WRITE}$	O	**Memory Write.** Active low output to the shared memory to perform a write cycle
$\overline{READ}$	O	**Memory Read.** Active low output to the shared memory to perform a read cycle Data from memory is latched in the R8071 prior to the negation of $\overline{READ}$
ATTN	I	**Attention.** Active high input that commands attention from the R8071 to shared memory locations which contain updates to status, modes, and/or buffer start address of a specified channel A sequence of memory accesses are performed soon after ATTN is asserted ATTN is negated in response to ATACK
ATACK	O	**Attention Acknowledge.** Active high output asserted when the sequence of memory accesses (in response to ATTN) is complete ATACK is negated in response to negation of ATTN
SYSACC	O	**System Access.** Active high output asserted to indicate the R8071 is accessing one of the 129 system memory locations (Channel Activation Byte or Channel Buffer Pointers)
LIU Interface		
SYSCLK	I	**System Clock.** Square wave input from the LIU clock generator for internal use in the R8071 Nominally, 3 088 MHz for T1 and 4 096 MHz for CEPT PCM 30
TCLK	I	**Transmit Clock.** Square wave input from the LIU clock generator providing the master timing source for the transmit function The frequency is one-half that of the SYSCLK
RCLK	I	**Received Clock.** Input from the external LIU/Clock recovery for the R8071 to sample RSER, the received serial data Nominally, 1 544 MHz for T1 and 2 048 MHz for CEPT PCM 30
Serial Interface		
TSER	O	**Transmitter Serial Data.** Output from the R8071 to the R8070 T1/CEPT PCM Transceiver representing the transmit serial data bit stream
TMAX	I	**Transmit Multiframe Sync.** Active high input pulse from the R8070 T1/CEPT PCM Transceiver indicating the beginning of a multiframe
RSER	I	**Received Serial Data.** Input from the R8070 T1/CEPT PCM Transceiver representing the received serial data bit stream
RSYNC	I	**Receive Synchronization.** Active high input level or pulse from the R8070 T1/CEPT PCM Transceiver for frame synchronization reference
RRED	I	**Receive Red Alarm.** Active high input from the R8070 T1/CEPT PCM Transceiver indicating a failure to frame on the T1 or CEPT PCM 30 time-division multiplexed (TDM) signals Low indicates that frame alignment has been found

Table 1. R8071 Interface Signal Definitions (Continued)

Symbol	I/O	Signal Name/Description
Strap Option Inputs		
T1/$\overline{\text{CEPT}}$	I	**T1 or CEPT Framing Select.** High selects the T1 framing mode Low selects the CEPT PCM 30 framing mode
HCS1, HCS0	I	**Hyperchannel Select.** Encoded inputs select the T1/CEPT PCM 30 hyperchannels (See Figure 5.)

T1/$\overline{\text{CEPT}}$	HCS1	HCS0	Channel Selection
X	Low	Low	All channels are 64 Kbps
High	High	Low	Four channels of 384 Kbps (H0)[1]
High	Low	High	Single channel of 1.536 Mbps (H11)[1]
Low	High	Low	Single channel of 1 92 Mbps (H12)[2], time slots 0 and 16 are 64 kbps
X	High	High	Reserved
Low	Low	High	Reserved

Notes: "X" denotes "Don't Care"
1. Valid for T1 only.
2. Valid for CEPT only

TSEREN	I	**TSER Enable.** Active high input that works in conjunction with the FILL/MASK bit as follows:

	FILL/MASK Bit	
TSEREN	0*	1
High	Send a 1 on TSER	Send data on TSER
Low	High impedance output on TSER	Send data on TSER

* or any F bit, or any bit during RESET, R8071 initialization, and until a channel is activated.

SIS	I	**Serial Interface Select.** High level identifies an R8070 compatible serial interface. Low level identifies AT&T compatible interface.
MDFS	I	**Memory Data Format Select.** High indicates that the most and least significant bytes of next buffer start address, buffer size and data length in shared memory reside at even and odd addresses, respectively (68000 MPU word addressing compatible). Low indicates that the least and most significant bytes of next buffer start address, buffer size and data length reside at even and odd addresses, respectively (8086 MPU word addressing compatible).
$\overline{\text{UAEN}}$	I	**Upper Address Enable.** High level input causes the upper address bus lines (A8–A15) to be in the high impedance state during system shared memory access (when SYACC is asserted). Low input causes the upper address outputs to be forced low by the R8071 when SYACC is asserted
Status Outputs		
$\overline{\text{INTR}}$	O	**Interrupt.** Active low output pulse of one SYSCLK period to the host system to indicate that the buffer status is being updated.
CH0–CH4	O	**Channel Number (0–4).** Encoded output indicating the channel number being served. CH0 is LSB and CH4 is MSB.
RX/$\overline{\text{TX}}$	O	**Receive/Transmit Channel.** Output used in conjunction with the channel number (CH0–CH4). High indicates a receive channel and low indicates a transmit channel.
Reset and Power		
RESET	I	**Reset.** Active high input that initializes all R8071 functions. Reset causes the R8071 to default to HDLC mode, causes all 0s in the FILL/MASK, and deactivates all channels Inactive transmit channels output all 1s. R8071 initialization is complete within 90 SYSCLK periods after RESET returns low.
VCC		**Power Supply Voltage.** +5 Vdc with respect to VSS
VSS		**Ground.** Ground reference voltage

FUNCTIONAL DESCRIPTION

The R8071 fetches the data to be transmitted from the shared memory, processes the data for up to 32 channels, channel-by-channel, by performing protocol formatting and rate adaption, and transmits it to the transceiver in serial form. Similarly, the R8071 processes, on a channel-by-channel basis, the received serial data on up to 32 channels by performing protocol deformatting and rate adaption, and stores the data into the shared memory.

Each channel is processed depending on the operational mode specified by the host as set up in the shared memory For any channel, the transmitter and the receiver operating modes may be specified independently of each other.

The internal functions of the R8071 are partitioned logically in to five major blocks (Figure 4):

- Transmit Bit-Level Processor
- Receive Bit-Level Processor
- Buffer Memory Manager
- Device Mode Controller
- System Monitor

TRANSMIT BIT-LEVEL PROCESSOR

HDLC and Non-HDLC Modes

The Transmit Bit-Level Processor performs basic HDLC* protocol formatting (DMI data modes 2 and 3, ISDN LAPD and IBM SNA) or other non-protocol transmit functions (DMI data modes 0 and 1, and bit-oriented signaling mode) for each channel independently of any another channel

In the HDLC mode, it generates flags, abort and idle codes, inserts zeroes for bit transparency, computes the HDLC frame check sequence (FCS) and composes HDLC frames from the data provided in the shared memory.

In the non-HDLC data mode, the data from the shared memory is not framed

In either mode, the R8071 performs rate adaption of sub-64 kbps data rates of the form

$$n \times 8 \text{ kbps } (n = 1 \text{ through } 8)$$

to the standard 64 kbps bearer rate (I.460, second stage RA2). An 8-bit FILL/MASK sequence (specified in in shared memory) is applied to the HDLC-formatted or non-HDLC data on a bit-by-bit basis (see FILL/MASK description on page 26). The resulting 8-bit sequence, consisting of the actual data bits and any 'time fill' bits (always a one) based on the FILL/MASK sequence, is then transmitted over the channel Figure 5a illustrates this process.

In the HDLC mode, the R8071 adapts the standard sub-64 kbps data rates (CCITT X 1 or DMI mode 2, but not necessarily n x 8 kbps) directly to the 64 kbps bearer rate (I.462 and DMI).

*The R8071 does not distinguish between the the High Level Data Link Control (HDLC) and the Synchronous Data Link Control (SDLC) protocols but implements the common link-layer functions for both Reference to HDLC in this document also implies SDLC unless otherwise stated.

A number (specified in the shared memory) of HDLC flags are appended to the end of an HDLC frame as time fill sequences. The R8071 monitors the number of intentionally inserted zeroes (which may be viewed as non-data intra-frame time fill bits). The programmed number of flags are adjusted based on the number of zeroes inserted. Reset activates the HDLC mode for all channels.

Logical Inversion

Logical inversion of data, as well as abort, flag and FCS bits, before transmission is programmable. Reset activates inversion for all channels

Loop Mode

Loop mode for both the transmit and receive channels is also programmable in shared memory. For a channel in the near-end loop mode, the R8071 stores the data transmitted during the channel period in an intermediate buffer. Such data is to be taken by the receive data channel programmed in the loop mode and eventually sent back to the shared memory. Only a single transmit channel and a single receive channel may be placed in the loop mode at one time for proper operation. Note that loop mode does not support H0 hyperchannel operation Reset deactivates the loop mode for all channels.

Signaling

Bit-oriented signaling and LAPD-based message-oriented signaling channels are directed to the non-HDLC processing elements, without any special consideration.

ISDN Hyperchannels

The 64 kbps channels (or time slots) are grouped into the ISDN standard hyperchannels (Figure 6). The actual hyperchannel grouping is specified by the HCS1 and HCS0 inputs (see Table 1, Strap Input Options). Reset deactivates signaling mode for all channels

Transmit Interface

The Transmit Bit-Level Processor interfaces directly to an R8070 T1/CEPT PCM Transceiver without any external circuitry. All the channel counter functions are built-in The Transmit Serial Data (TSER) output is driven with the transmit serial data bit stream acquired from the shared memory The Transmit Clock (TCLK) input is the timing reference for TSER The Transmit Multiframe Sync (TMAX) input is the starting reference for the TDM frame.

TSER is placed in the high impedance (tri-state) mode whenever the TSEREN input is low and the FILL/MASK bit is zero (see Table 1, Strap Input Options) This enables the TSER outputs of up to eight R8071s to be connected together and allows the R8071s to be programmed with mutually exclusive FILL/MASK sequences in order to accomplish subrate time-division multiplexing over a 64 kbps channel

In summary, each channel may be programmed by the host system independently of any other channel by specifying HDLC mode, FILL/MASK, data inversion, and loop mode options. Both the rate adaption recommendation, namely HDLC flag insertion and the second stage intermediate rate adaption, are implemented. In addition, various other HDLC formatted rates of the form n x 8 kbps (n = 1 through 8) are also adapted to the 64 kbps bearer rate.

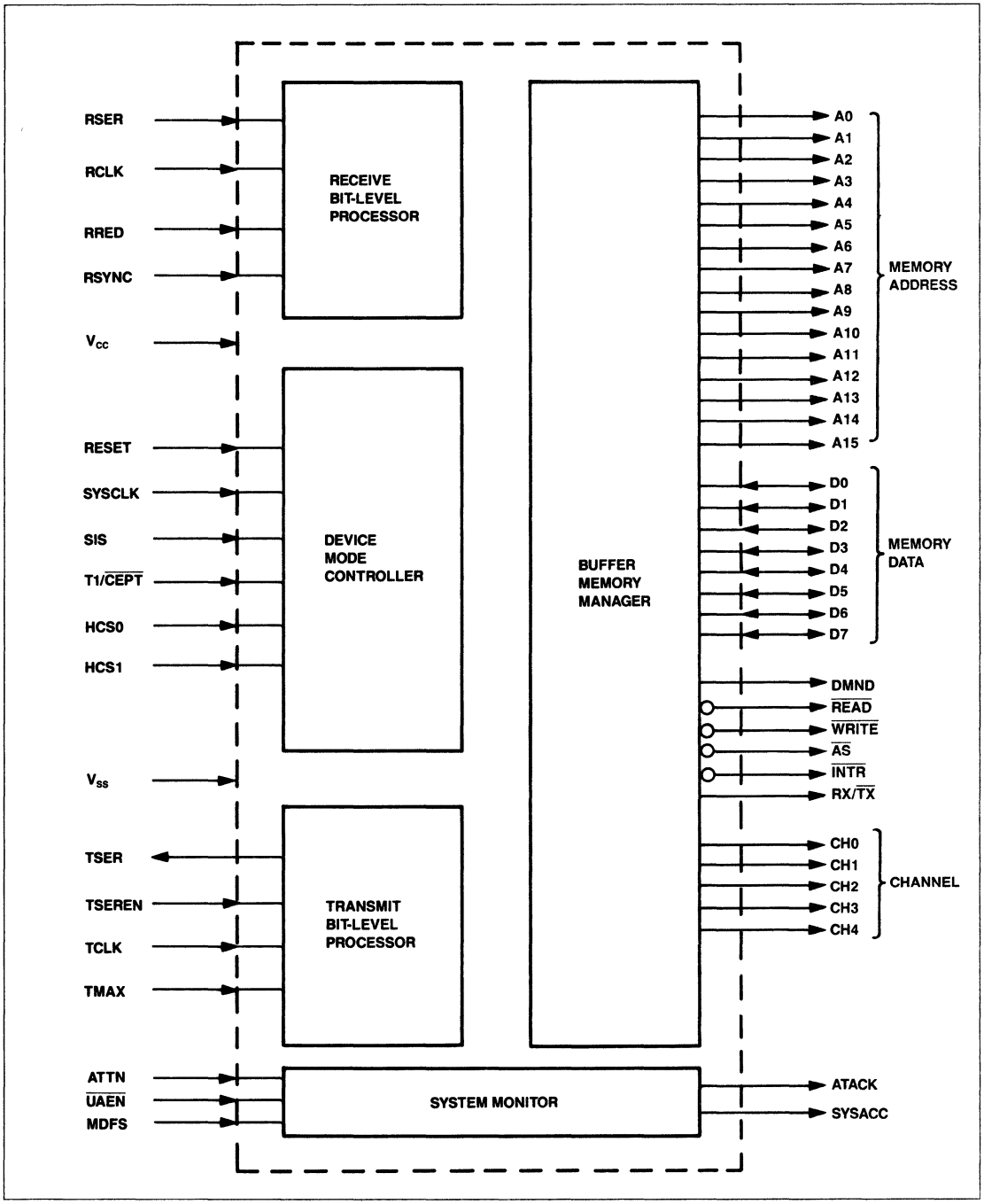


Figure 4. R8071 ISDN/DMI Link Layer Controller Functional Block Diagram

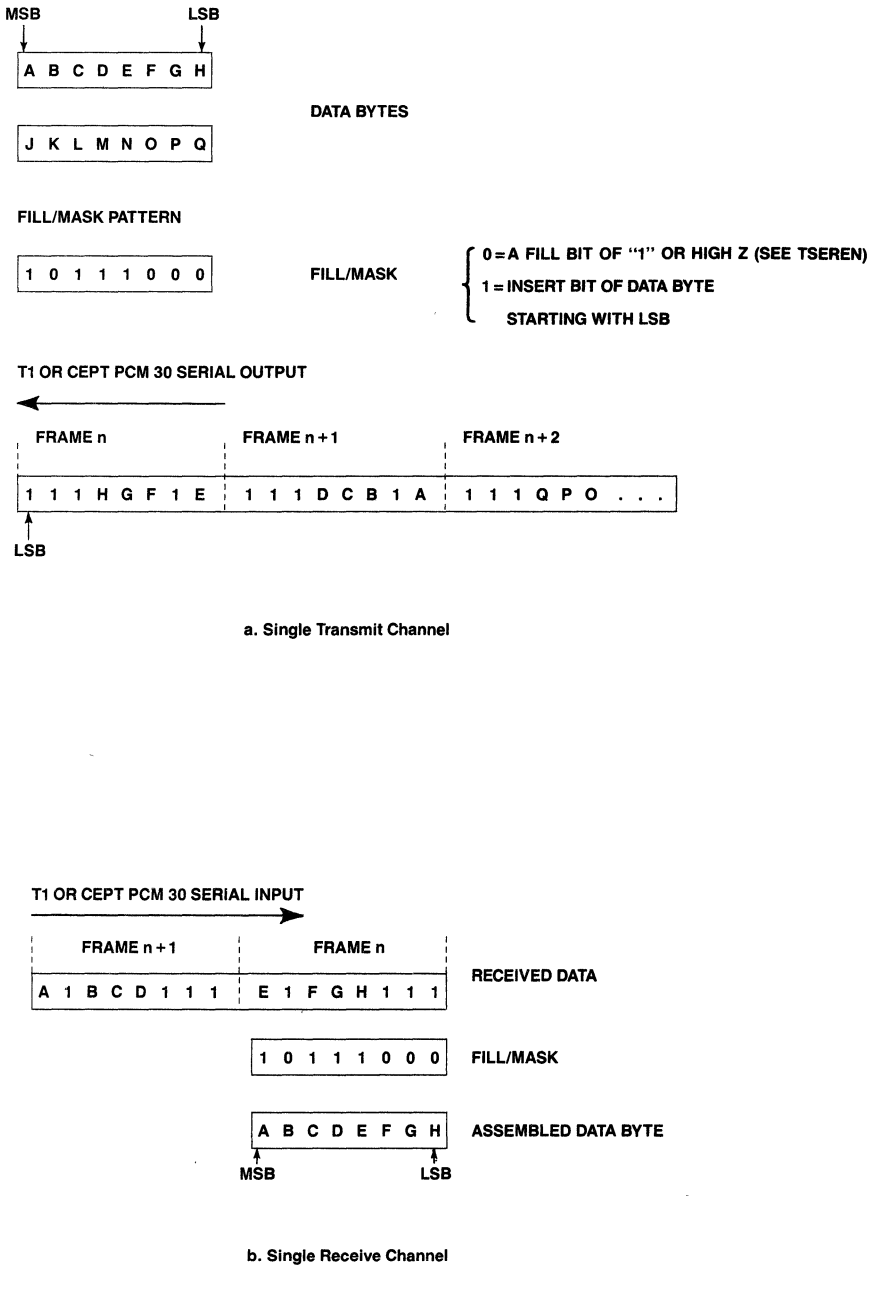
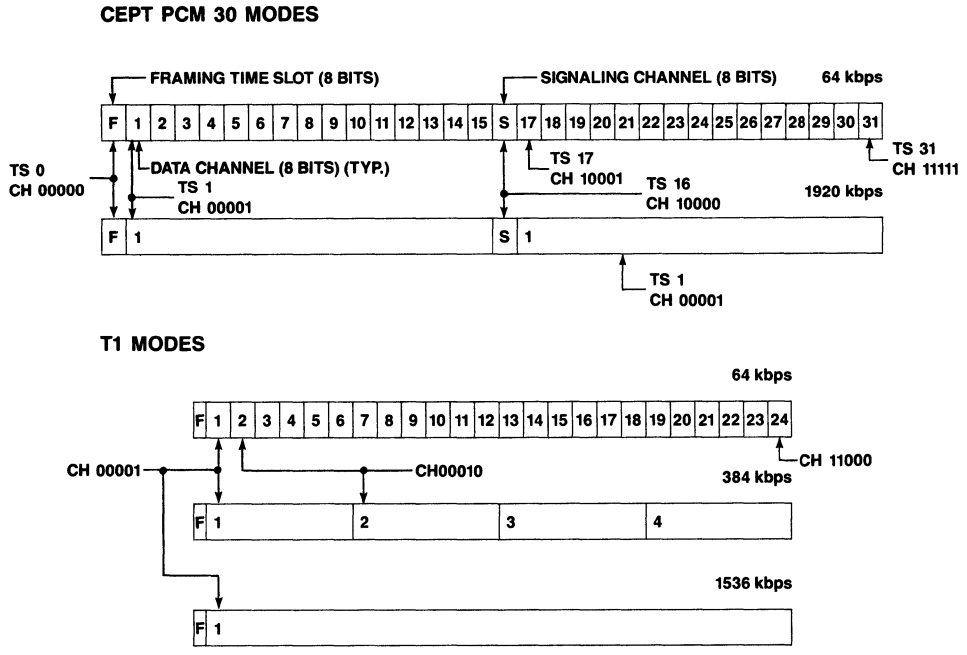


Figure 5. 32 kbps Subrate Operation



NOTE: GROUPING OF 64 KBPS CHANNELS INTO HYPER CHANNELS IS FIXED AS SHOWN. CHANNEL ASSIGNMENTS CANNOT BE CHANGED.

Figure 6. R8071 Hyperchannel Provisions

6

RECEIVE BIT-LEVEL PROCESSOR

HDLC and Non-HDLC Modes

The Receive Bit-Level Processor performs basic HDLC/SDLC protocol deformatting (DMI data modes 2 and 3, ISDN LAPD, and IBM SNA) or other non-protocol receive functions (DMI data modes 0 and 1, and bit-oriented signaling channels) for each channel independently of any other channel.

In the HDLC mode, the R8071 detects flags, aborts and inserted zeroes, and also checks the Frame Check Sequence (FCS). It also filters out any time fill patterns received by applying the 8-bit FILL/MASK sequence specified in the shared memory. The resulting serial data, including the HDLC header (i.e., address and control fields), is then assembled into bytes for storage in the shared memory (Figure 5b). The validity of every HDLC frame is checked and reported to the shared memory appropriately. Reset activates HDLC mode for all channels.

In the non-HDLC data mode, any time fill patterns received are also filtered out based on the 8-bit FILL/MASK sequence. The resulting serial data is simply grouped into bytes for transfer to the shared memory.

Logical Inversion

Logical inversion of all the received serial data is programmable in the external shared memory. Reset activates inversion for all channels.

Loop Mode

Loop mode for receive channels is also programmable in shared memory. For a channel in the near-end loop mode, the input data is taken from an internal buffer rather than from the external data. The internal buffer presumably has been filled with data from a transmit channel in the loop mode. Thereafter, the looped data is processed according to the specified mode of operation. Reset deactivates loop mode for all channels.

Non-HDLC Signaling Mode

In the non-HDLC signaling channel mode, the R8071 detects the multiframe (or extended superframe) alignment sequence for DMI bit-oriented signaling (G.732 and DMI). If a valid multiframe alignment is found, the received data is transferred to shared memory. If the multiframe alignment sequence is found to be in error, transfer of signaling data to the shared memory is suspended until a valid multiframe is detected (G.732 and DMI). Loss of multiframe is reported to the shared memory. Note that any channel(s) can be specified to receive bit-oriented signaling. This feature is very useful in central office switching applications. Reset deactivates signaling for all channels.

ISDN Hyperchannels

The 64 kbps channels are grouped into the ISDN standard hyperchannels (Figure 6) based on the input strap pins HCS0 and HCS1 (see Table 1, Strap Input Options).

Elastic Buffer

The received serial data from a T1 or CEPT PCM 30 multiframe, in general, has no relationship to the transmit data multiframe in terms of frame beginning. Both the Receive Bit-Level Processor and the Transmit Bit-Level Processor exchange data with the shared memory over a single data bus. In order to handle contention for the data bus, an elastic buffer is used in the Receive Bit-Level Processor.

The elastic buffer input is clocked by the Receive Data Clock (RCLK) and the output is re-timed using the Transmit Data Clock (TCLK). Thus the TCLK is used as a reference for both the transmit and the re-timed receive data. As a result, the shared memory access is simple and predictable. Note that the looped data bypasses the elastic buffer. Also, any overflow or underflow of the elastic buffer is reported to the shared memory for all the channels. The elastic buffer also protects the shared memory against underflow or overflow in the remote loopback (i.e., echo) mode.

Receive Interface

The Receive Bit-Level Processor interfaces directly to the R8070 without any need for additional logic. All the needed channel counters are supplied internally. Received serial data is extracted from the Received Serial Data (RSER) input bit stream on the falling edge of the Receive Clock (RCLK) input. (R8070 mode, see SIS input.)

The Receive Synchronization (RSYNC) input provides a frame synchronization reference. The RRED input is monitored for loss of T1 or CEPT PCM 30 frame synchronization and reported to the shared memory.

BUFFER MEMORY MANAGER

The Buffer Memory Manager controls the flow of data between the Transmit Bit-Level Processor/Receive Bit-Level Processor and the data buffers in external shared memory. Shared memory is allocated for each transmit or receive channel as a linked list of buffers which are set up by the host. The shared memory is managed with minimal intervention from the host. The host simply has to allocate enough memory in the buffers such that the real-time operation of transmission and reception can take place without any data underrun or overrun, respectively.

The buffers contain information such as operational modes, buffer or HDLC frame completion status, size of the buffer, number of transmit or receive data bytes, link to the next buffer, and the transmit or receive data bytes.

The R8071 updates the status of each channel buffer as each individual buffer or HDLC frames are completed and simultaneously asserts the Interrupt Indication ($\overline{INTR}$) output to the host.

During transmission, the Empty (MPTY), Command (CMND), and Complete Frame/Partial Data Buffer (CF/$\overline{P}$) bits are monitored in the transmit status byte (see External Shared Memory Organization and Definition). The MPTY, Invalid Buffer Address (IVBA), and Underrun (UNDR) bits in the transmit status byte in shared memory are updated.

During reception, the Empty (MPTY), Command,(CMND), and Complete Frame/Partial Data Buffer (CF/$\overline{P}$) bits are monitored in the receive status byte. The MPTY, Invalid Buffer Address (IVBA), and CF/$\overline{P}$ bits in the receive status byte in shared memory are updated. Three encoded error reporting bits in the receive status byte, Abort (ABRT), Frame Check Error (FCER) and Short HDLC Frame Error (SHER), are also updated to report conditions such as invalid HDLC frame, frame check error, abort code received, loss of T1 or CEPT PCM 30 frame synchronization, loss of T1 or CEPT PCM 30 signaling channel multiframe alignment, and elastic buffer underrun or overrun.

Operational modes, loop, and invert commands as well as the FILL/MASK patterns are extracted from the transmit and receive command buffers and passed to the Transmit Bit-Level Processor and the Receive Bit-Level Processor, respectively. The modes are decoded from the HDLC Mode Select (HDLC) and Signaling Mode Select (SIG) bits. Loop and invert commands are pulled from the LOOP and INV bits, respectively.

The Buffer Memory Manager responds to host processor-initiated changes in the operational modes of a channel or relocation of the allocated buffers without affecting the operation of the other channels.

The Channel Number (CH0-CH4) and Receive/Transmit Channel (RX/$\overline{TX}$) outputs are updated to reflect to the channel being served.

The Buffer Memory Manager also causes mode changes in the Transmit Bit-Level Processor and the Receive Bit-Level Processor in response to the host processor-initiated mode changes.

DEVICE MODE CONTROLLER

The Device Mode Controller provides the central device timing and control for the other device functions. General and memory interface internal timing is derived from the System Clock (SYSCLK) input. Device reset to the other functions is distributed based on the Reset (RESET) input.

The selected carrier and framing format based on the T1/CEPT PCM 30 Carrier Select (T1/$\overline{CEPT}$) input and the encoded Hyperchannel Select inputs (HCS0 and HCS1), are passed to the Transmit Bit-Level Processor and the Receive Bit-Level Processor. The transceiver interface specified by the Serial Interface Select (SIS) input is also routed to those functions. (See Table 1, Strap Input Options.)

SYSTEM MONITOR

The System Monitor informs the Buffer Memory Manager of a host-initiated Attention (ATTN) command. Prior to asserting ATTN, the host will have set up, in shared memory, the actual channel number that needs the R8071's attention, its mode of operation and the start address of the linked list of buffers.

Whenever the R8071 accesses the Channel Activation Byte or Channel Buffer Pointers in shared memory, the System Access (SYSACC) output is asserted indicating that system memory is being accessed. At that time, the upper order address lines (A8-A15) are placed in the high impedance state or driven low depending on whether the Upper Address Enable (UAEN) input is high or low, respectively. In the high impedance state, the host can drive the A8-A15 lines to any logic level. As soon as the R8071 completes the ATTN command processing, the Attention Acknowledgement (ATACK) output is asserted. The falling edge of ATTN causes ATACK to return low.

In addition, the relative locations of the upper (most significant) and the lower (least significant) bytes of certain 16-bit words (i.e., next buffer address, buffer size and data length) in the shared memory are determined based on the Memory Data Format Select (MDFS) input (see Table 1, Strap Input Options).

SERIAL INTERFACE TO R8070 T1/CEPT PCM TRANSCEIVER (SIS = HIGH)

TRANSMIT

T1 Mode (T1/$\overline{CEPT}$ input high). The serial data output (TSER) from the R8071 changes in response to the falling edge of the TCLK as shown in Figure 7. Setup and hold time periods for TSER are such that TSER can be sampled reliably at the next rising edge of the TCLK inside the R8070 T1/CEPT PCM Transceiver device. TSER is a tri-state output. Its actual logic level and impedance level over any bit period are determined by the combination of the corresponding FILL/MASK bit and the TSEREN input.

Transmit synchronous operation between the R8070 and the R8071 is attained by TMAX application.

When TMAX is synchronously asserted, the R8071 will be transmitting the last bit of a frame. TMAX may be applied synchronously as frequently as a frame rate, or as seldom as when a system needs to reinitiate synchronism.

When TMAX is applied to initiate synchronism, the transmitter completes the processing of the current channel, fills the interim time with 1s (or goes high impedance — see TSEREN) and begins transmitting the first bit of time slot 1 which will occur nine or ten (CEPT/T1) bit times after TMAX.

CEPT PCM 30 Mode (T1/$\overline{CEPT}$ input low). TSER from the R8071 changes in response to the falling edge of the TCLK as shown in Figure 8. Setup and hold time periods for TSER are such that TSER can be sampled reliably at the next rising edge of the TCLK by the R8070. TSER is a tri-state output. Its actual logic level and impedance level over any bit period are determined by the combination of the corresponding FILL/MASK bit and the TSEREN input.

RECEIVE

T1 Mode (T1/$\overline{CEPT}$ input high). The receive data (RSER) is processed serially and sampled at the negative edge of RCLK at a rate of 1.544 MHz. The R8070 accomplishes multiframe synchronization at the third assertion of RSYNC after RRED (internally delayed) goes low. RSYNC is synchronous with the rising edge of RCLK and the first "F" bit of a multiframe. Figure 9 illustrates the timing.

CEPT PCM 30 Mode (T1/$\overline{CEPT}$ input low). RSER is processed serially and sampled by the negative edge of RCLK at a rate of 2.048 MHz. RSYNC is synchronous with the rising edge of RCLK 'and bit 1' in time slot zero of the first frame of a multiframe. Figure 10 illustrates the timing.

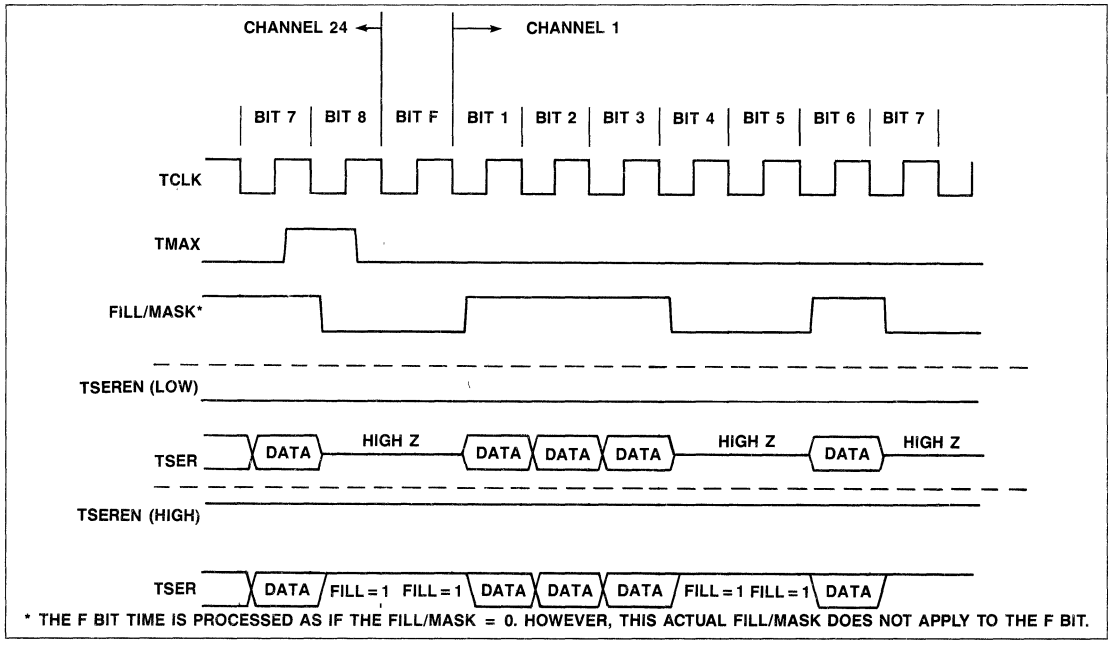


Figure 7. Transmit Frame Synchronization Timing—T1 Mode (R8070 Interface)

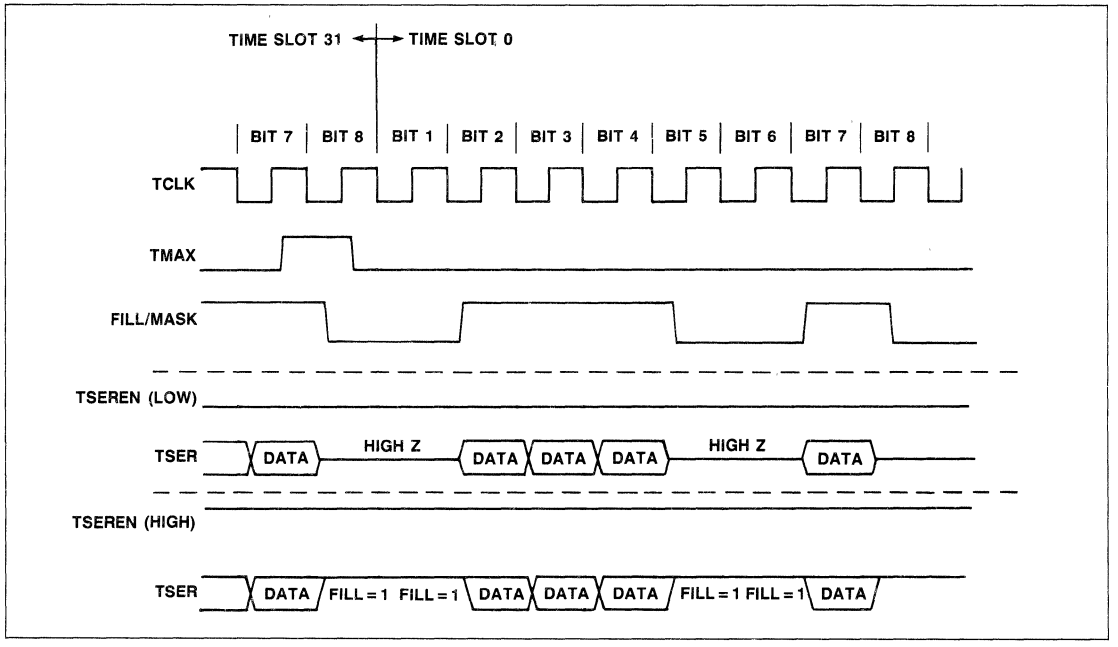


Figure 8. Transmit Frame Synchronization Timing—CEPT PCM 30 Mode (R8070 Interface)

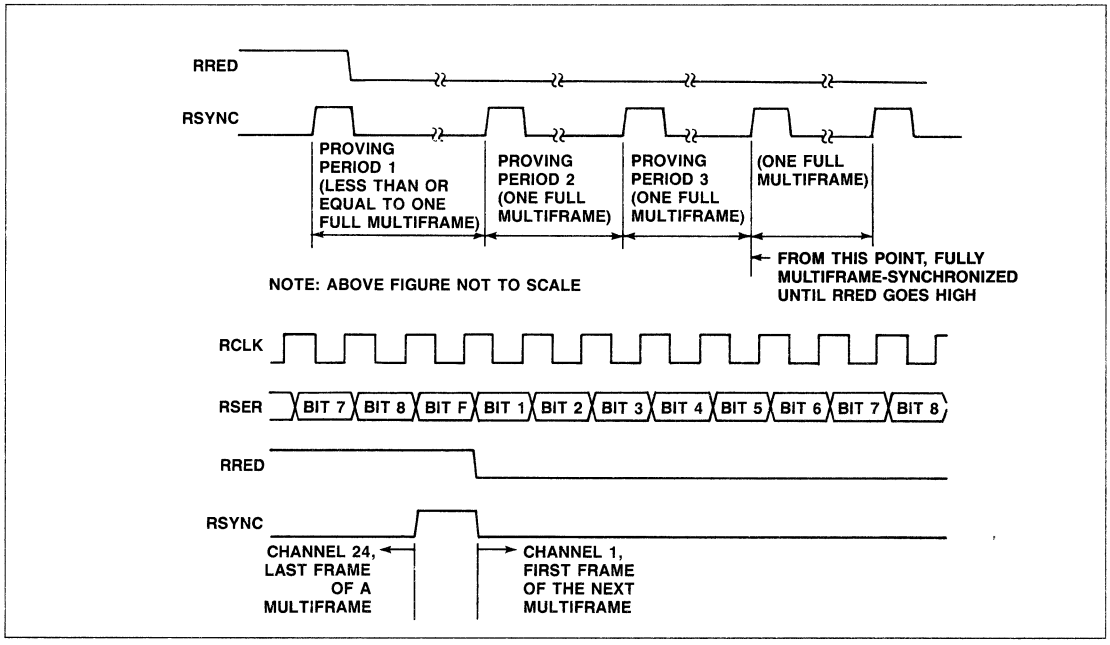


Figure 9. Receive Frame Synchronization Timing—T1 Mode (R8070 Interface)

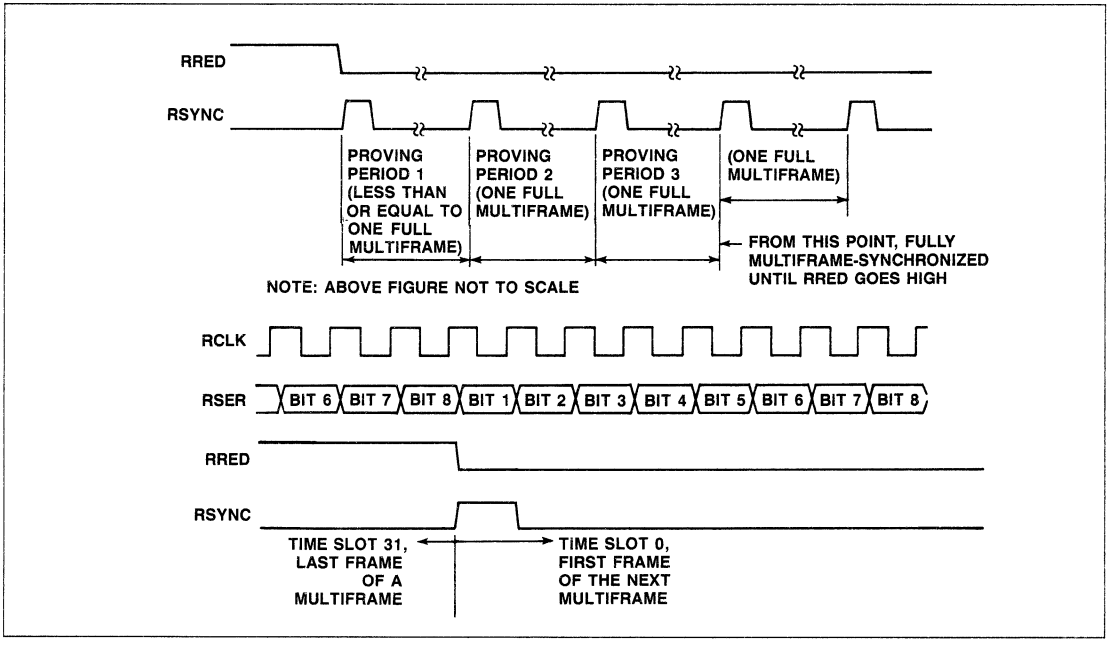


Figure 10. Receive Frame Synchronization—CEPT PCM 30 Mode (R8070 Interface)

EXTERNAL SHARED MEMORY ORGANIZATION AND DEFINITION

GENERAL STRUCTURE

Transmit data, received data, channel commands and channel pointers are organized in the external memory shared by the host and R8071.

For each transmit and receive channel, the host must allocate shared memory for a channel activation byte, channel buffer pointers, and a set of channel data buffers. Figure 11 illustrates an arrangement of shared buffer memory within the host computer main memory.

The Channel Activation Byte and the Channel Buffer Pointers are located in a 256-byte address space referred to as system memory (Figure 12). The Channel Activation Byte is located at address j followed by 127 unassigned bytes. The Channel Buffer Pointers are located at addresses j + 128 through j + 255. The Channel Data Buffers are located at starting addresses specified by the channel pointers. The length of the data buffers is specified in data descriptors included within the data buffer.

CHANNEL ACTIVATION BYTE

The Channel Activation Byte (Figure 12) contains a command to activate or deactivate the channel number identified within the byte. The direction of data travel is also specified. The individual bits are defined as follows:

ACTIVE—Activate Channel. When set by the host, the indicated channel (CHANNEL number) is activated. When reset by the host, the channel is deactivated.

RX/$\overline{TX}$—Receive/Transmit. When set by the host, the indicated channel is a receive channel. When reset by the host, the channel is a transmit channel.

CHANNEL—Channel Number. Set by the host to select the number of the channel:

Bit					
4	3	2	1	0	Channel Number
0	0	0	0	0	0
	.				
	.				
	.				
1	1	1	1	1	31

CHANNEL BUFFER POINTERS

The Channel Buffer Pointers specify the start addresses for the Channel Data Buffers. The pointers must be stored by the host in 128 contiguous bytes beginning at j + 128. For each channel, the buffer start address is to be specified as a 16-bit (2-byte) word. The relative location of the upper and lower bytes of the 16-bit word is determined by the MDFS input (Figure 12). Pointers for up to 32 transmit and 32 receive channels can be specified.

The upper address lines (A8-A15) are placed in the high impedance state by the R8071 during the System memory accesses (i. e., while the Channel Activation Byte or Channel Buffer Pointers are being accessed) when the UAEN input is high.

CHANNEL DATA BUFFERS

A buffer is a group of contiguous memory locations for each meaningful group of ordered data. The number of memory locations in a buffer depends on memory availability and user data frame size, if any. For example, a group of contiguous memory locations may be assigned to the data that has to be framed according to HDLC protocol. The data has to be grouped into an 8-bit entity, also referred to as octet or byte. If necessary, one octet is read from or written to the data buffer by the R8071 during a single memory access.

The Channel Data Buffers (also referred to as the data buffers) may reside anywhere in the memory within the addressing range of the Channel Buffer Pointers. Any number of data buffers may be assigned for any channel and their starting addresses may be changed at any time. A set of data buffers are usually assigned for each active channel for storing the data to be transmitted and another set for the received data.

TRANSMIT DATA/COMMAND BUFFER ORGANIZATION

A general organization of data within a buffer and the linking of buffers are illustrated in Figure 13. The detail contents of a Transmit Data Buffer are shown in Figure 14. The contents of a Transmit Command Buffer are shown in Figure 15. Information within the buffer is organized into two groups: descriptors and data.

The first group of seven bytes contains the buffer descriptors, i.e., information such as the link (pointer) to the next transmit data buffer, buffer size, the number of data bytes in the buffer and buffer status. This group of information is mandatory for each buffer.

The second group contains k-bytes of information, k being a variable number. This group contains user data (including any header) that has to be framed according to HDLC, data to be transmitted unframed, or channel mode and fill/mask information.

TRANSMIT CHANNEL DESCRIPTORS

The breakdown and the ordering of the seven bytes of descriptors appears in Figure 14. The first six bytes contain the next buffer address, the buffer size and the data length—each consisting of two bytes. The relative locations of the upper and the lower bytes are interchangeable by the use of the input strap pin MDFS. The seventh byte contains the status of the current transmit buffer as well as the status of the transmit channel. A byte not used by the R8071, and free to be used by the host, will proceed or follow the status byte as determined by MDFS (Figure 14).

Next Buffer Start Address

Bytes 0 and 1 contain the 16-bit start address of the next buffer. The next buffer start address can be the same as that of the current buffer. Such a buffer is referred to as a recirculating buffer.

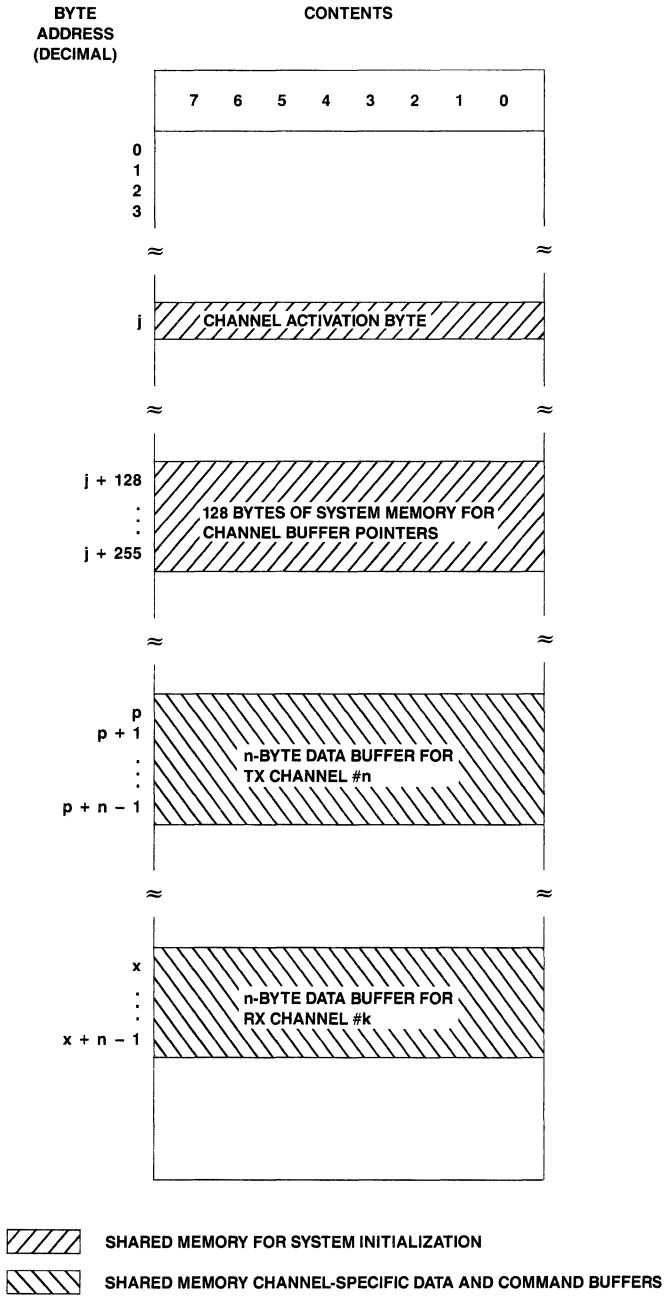


Figure 11. External Shared Memory Map—Top Level

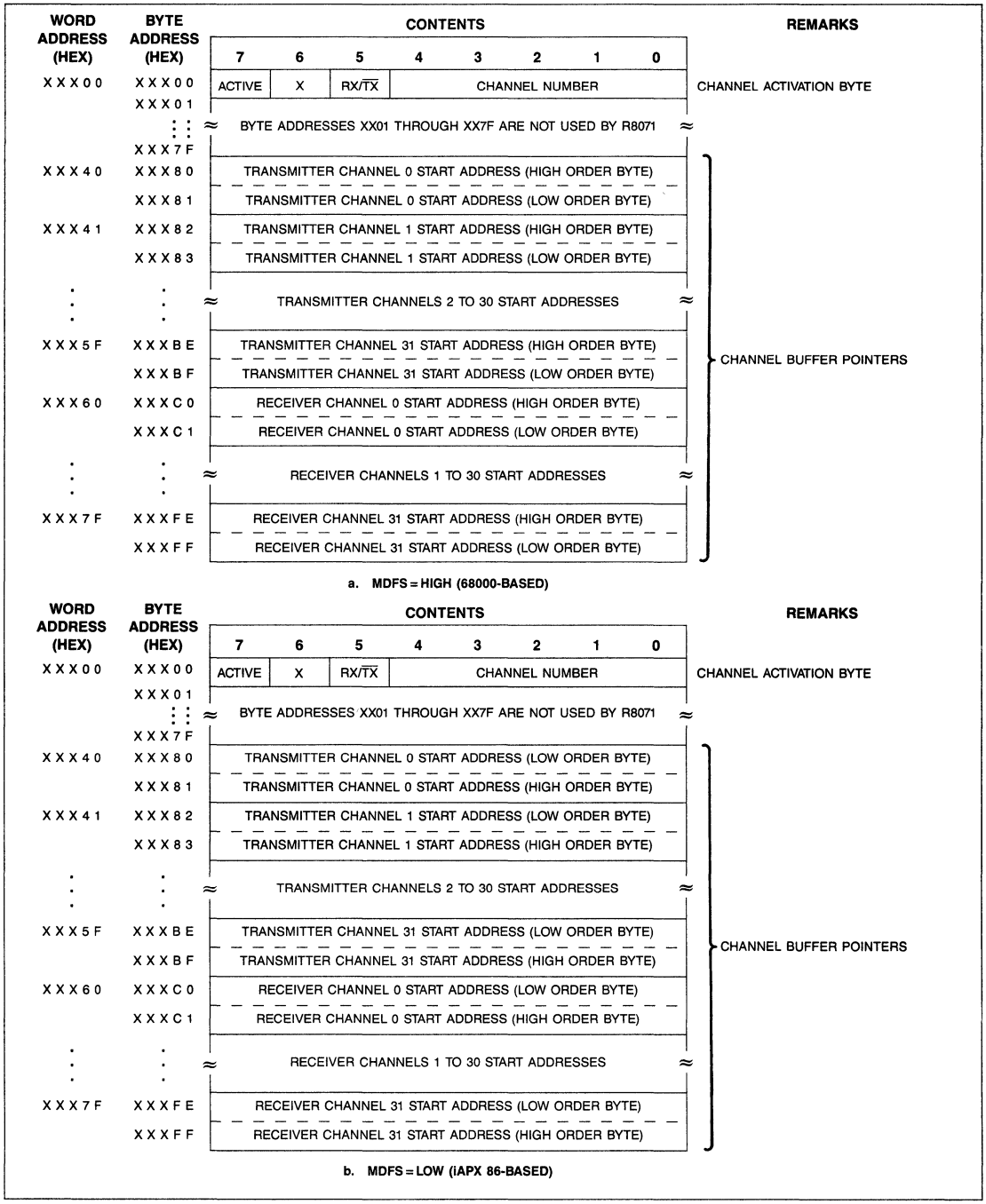


Figure 12. System Memory Map Locations

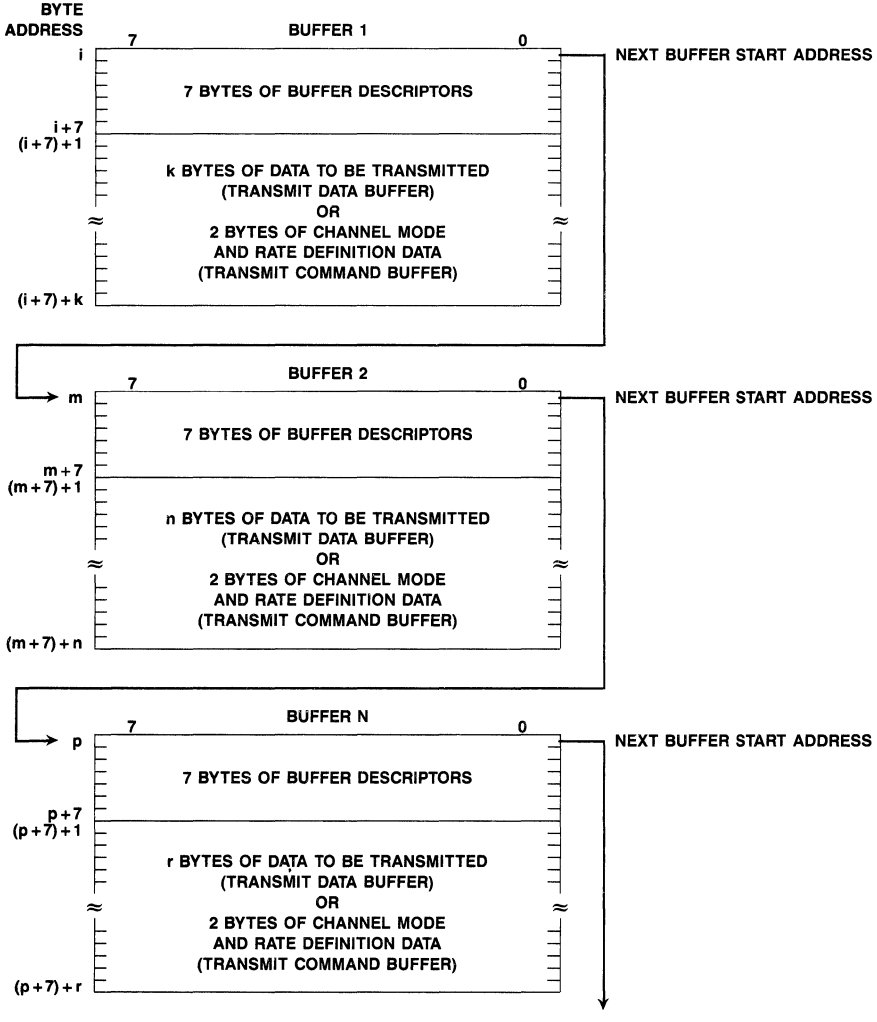


Figure 13. Organization and Linking of Transmit Buffers.

BYTE ADDRESS	CONTENTS 7	6	5	4	3	2	1	0
i	msb NEXT BUFFER ADDRESS							
i+1								lsb
i+2	X	X	X	X	msb BUFFER SIZE (k)			
i+3								lsb
i+4	FC	FO	X	X	msb DATA LENGTH (j)			
i+5								lsb
i+6	NOT USED BY R8071							
i+7	STATUS UNDR	IVBA	X	X	X	CF/$\overline{P}$	(0) CMND	MPTY
(i+7)+1	FIRST DATA BYTE							
(i+7)+2	SECOND DATA BYTE							
(i+7)+j	LAST DATA BYTE							
(i+7)+j+1	FLAG COUNT (OPTIONAL)							
(i+7)+k	LAST LOCATION IN BUFFER							

a. MDFS = High

BYTE ADDRESS	CONTENTS 7	6	5	4	3	2	1	0
i	NEXT BUFFER ADDRESS							lsb
i+1	msb							
i+2					BUFFER SIZE (k)			lsb
i+3	X	X	X	X	msb			
i+4					DATA LENGTH (j)			lsb
i+5	FC	FO	X	X	msb			
i+6	STATUS UNDR	IVBA	X	X	X	CF/$\overline{P}$	(0) CMND	MPTY
i+7	NOT USED BY R8071							
(i+7)+1	FIRST DATA BYTE							
(i+7)+2	SECOND DATA BYTE							
(i+7)+j	LAST DATA BYTE							
(i+7)+j+1	FLAG COUNT (OPTIONAL)							
(i+7)+k	LAST LOCATION IN BUFFER							

b. MDFS = Low

Figure 14. Transmit Data Buffer Contents

BYTE ADDRESS	CONTENTS 7	6	5	4	3	2	1	0
i	msb NEXT BUFFER ADDRESS (i)							
i+1								lsb
i+2	NOT USED BY R8071							
i+3								
i+4	NOT USED BY R8071							
i+5								
i+6	NOT USED BY R8071							
i+7	STATUS UNDR	IVBA	x	x	x	CF/$\overline{P}$	(1) CMND	MPTY
(i+7)+1	MODES 0	0	0	0	INV	LOOP	SIG	HDLC
(i+7)+2	FILL/MASK							

a. MDFS = High

BYTE ADDRESS	CONTENTS 7	6	5	4	3	2	1	0
i	NEXT BUFFER ADDRESS (i)							lsb
i+1	msb							
i+2	NOT USED BY R8071							
i+3								
i+4	NOT USED BY R8071							
i+								
i+6	STATUS UNDR	IVBA	x	x	x	CF/$\overline{P}$	(1) CMND	MPTY
i+7	NOT USED BY R8071							
(i+7)+1	MODES 0	0	0	0	INV	LOOP	SIG	HDLC
(i+7)+2	FILL/MASK							

b. MDFS = Low

Figure 15. Transmit Command Buffer Contents

Buffer Size

Bytes 2 and 3 contain the 12-bit BUFFER SIZE, k The BUFFER SIZE specifies the total number of memory bytes allocated by the host processor for storing the data to be transmitted The four most significant bits are not used by the R8071

The R8071 reads the buffer size only if the status indicates that the data buffer contains partial data and then interprets the buffer size to be the actual number of data bytes in this buffer The R8071 does not read this word when the data buffer is a command buffer

Data Length

Bytes 4 and 5 contain the 12-bit DATA LENGTH field and a 2-bit field containing host processor options for rate adaptation and timer functions The remaining 2-bit field is not used by the R8071

Data Length—DATA LENGTH, j, specifies the actual number of data bytes in the buffer to be transmitted. The R8071 reads DATA LENGTH only if the status indicates that the buffer contains the last byte of an HDLC frame or non-HDLC data (CF/$\overline{P}$ = 1).

FO—Flag Offset Control. This bit is meaningful only when FC is set. When FO is set by the host, the transmitter of the specific channel counts the total number of HDLC zeroes intentionally inserted over the data and the CRC fields for the entire duration of transmission. At the end of each HDLC frame, it divides the accumulated number by eight and retains the remainder. The quotient is known as the flag count offset. The quotient represents the number of bytes of non-data entities transmitted and can be viewed as the HDLC intra-frame fill. The R8071 subtracts the flag count offset from the FLAG COUNT which was specified without the knowledge of the inserted zeroes The resultant count equals the actual number of additional flags that are transmitted by the R8071. This is extremely useful in synchronous data rate-adaption applications.

The flag count offset can be any number from zero through three, implying that HDLC frames long enough to cause up to 24 zero insertions can be monitored by the transmitter without any overflow of the internal 2-bit flag count offset If the resultant flag count after subtracting the offset is zero or negative, no additional flags are transmitted

When FC is a 0, the FLAG COUNT is not adjusted. For applications such as LAPD which require an opening flag and a separate closing flag, FC should be set, FO reset, and FLAG COUNT set to 1

In a non-HDLC mode, the flag count offset will always be zero. The state of FO does not matter.

FC—Flag Control. When set by the host, this bit specifies that the corresponding HDLC channel transmitter contains a certain number of HDLC flags after the CRC. A minimum of one FLAG that plays the dual role of the closing FLAG of the current frame and the opening FLAG of the next frame is sent regardless of FC The actual number of additional flags to be transmitted when FC is a 1 is dependent on the optional FLAG COUNT byte shown in Figure 14

This flag control feature is very useful in rate adaption of sub-64 kbps data rates to the 64 kbps bearer channel rate and also as a timer The R8071 automatically goes to the next buffer after sending the specified number of flags.

In the non-HDLC data mode, the R8071 sends the specified number of all ones octets after the last data byte.

For the non-HDLC signaling channel, buffers need to be specified to be partial data buffers for meaningful operation. In such a case, FC will not be read

When FC is reset, no additional flags are transmitted The R8071 does not process the FC bit in a command buffer.

Transmit Buffer Status

The Transmit Buffer STATUS byte contains the status of the current transmit buffer as well as the status of the transmit channel (Figure 14) The individual bits are defined as follows

MPTY—Empty. This bit is set by the host to inform the R8071 that the data buffer is empty, i e., data is not ready for transmission The host resets this bit when the buffer contains valid data ready for transmission. When the buffer is empty, the R8071 keeps polling this bit until it is non-empty

This bit is set by the R8071 to inform the host that the R8071 has completed transmission of all the data in this buffer or completed processing a command buffer

CMND—Command. This bit is set by the host to inform the R8071 that this buffer is a command buffer. A command buffer contains channel-specific mode definition and FILL/MASK information This bit is reset by the host to indicate that the buffer is a data buffer which contains transmit data Upon writing status, the R8071 will update the CMND bit according to the buffer type just processed

CF/$\overline{P}$—Complete Frame/Partial Data Buffer. This bit is set by the host to indicate that this buffer contains the last byte of a sequence of bytes to be formatted according to HDLC The R8071 automatically appends CRC and flag to the data before looking for more data in the next buffer The actual number of data bytes is specified by the 12 bit DATA LENGTH words

In non-HDLC applications, this bit must be reset to indicate continuous data transmission, otherwise the all ones octet pattern will be transmitted after the last byte of data in a buffer.

This bit is reset by the host to indicate that this buffer contains only a part of the data to be transmitted; the rest perhaps is in one or more succeeding buffers. Such a buffer is referred to as a partial data buffer In this case, the R8071 transmits all the data in this buffer and then automatically transmits any data in the next buffer. The actual number of data bytes is specified by the 12-bit BUFFER SIZE word.

The R8071 does not read the CF/$\overline{P}$ bit in a command buffer It will, however, set the CF/$\overline{P}$ bit when reporting status for a processed command buffer The CF/$\overline{P}$ bit will also be set upon completion of the first signaling (partial) buffers

IVBA—Invalid Buffer Address. This bit is set by the R8071 if it encounters an invalid next buffer address, i.e., a next buffer address with a starting address of 16 zeroes or hexadecimal FFFX (X = don't care). In this case, the specific transmit channel of the R8071 enters the inactive state and continuously transmits octets of all ones until a channel is reactivated by the host.

UNDR—Underrun. This bit is set by the R8071 when its transmit channel runs out of data. Such is the case when the R8071 encounters either an invalid buffer address, an empty data buffer, or a command buffer following a partial data buffer. In HDLC mode, the transmitter of the specific channel automatically transmits an ABORT code, followed by FLAGs until the condition is cleared. In all cases of underrun, the non-HDLC transmit channel sends the all ones octet pattern repeatedly until a valid non-empty data buffer is set up by the host. The remaining bits in the status byte will not be read by the R8071, however, they will be reset upon a status update.

TRANSMIT DATA BUFFER

A transmit data buffer contains actual data to be transmitted and optional FLAG COUNT byte for rate adaption (Figure 14).

TRANSMIT COMMAND BUFFER

A transmit command buffer contains exactly two bytes of data following the seven bytes of descriptors (Figure 15).

The first byte (MODE) defines the channel modes of operation—specifically HDLC, signaling, data inversion and loop back. The second byte (FILL/MASK) defines the data rate. The breakdown and the ordering of bytes within the command buffer are illustrated in Figure 15.

For a command buffer, the R8071 will not process the bytes at addresses [i + 2, i + 3] and [i + 4, i + 5] as the data length is presumed to be exactly 2 bytes. However, the R8071 will read the next buffer address at locations i and i + 1 as part of processing the command buffer. As mentioned before, the relative locations of the upper and the lower bytes of the next buffer address are interchangeable by means of MDFS. The mode and FILL/MASK bytes locations are not interchangeable by MFDS.

MODES

The MODES byte specifies the operational modes of the given channel—specifically, HDLC or non-HDLC, signaling channel or not, data to be inverted bit-by-bit prior to transmission or not and channel transmit data to be looped back via the receiver to the host shared memory or not (Figure 14).

SIG and HDLC— Mode Select. These two bits select the R8071 framing mode.

SIG	HDLC	Mode Selected
1	0	Non-HDLC Signaling Channel Mode
0	0	Non-HDLC Data Channel Mode
0	1	HDLC Data Channel Mode
1	1	Reserved

Non-HDLC Signaling Channel Mode. The channel carries bit-oriented signaling data without an HDLC format. The R8071 treats this channel without any special consideration to signaling. However, the R8071 assumes that only one, or at the most two, linked data buffers are assigned to the signaling channel by the host. Additionally, the last data buffer (even if it is the only buffer) is assumed to be a recirculating buffer.

Non-HDLC Data Channel Mode. The channel is a non-HDLC data channel. In DMI applications, data modes 0 and 1 may be specified by this combination. The CF/$\overline{P}$ bit of the status byte of the allocated data buffers must be reset for uninterrupted data transmission, otherwise, the R8071 will transmit the all ones octet pattern repeatedly after the last byte as many times as is dictated by FC, FLAG COUNT and the availability of the data in the next buffer. The channel time fill and the idle codes are one and the same.

HDLC Data Channel Mode. The channel is an HDLC data channel or a LAPD message-oriented HDLC signaling channel. No distinction is made between an HDLC data channel and a LAPD channel. No special handling is done on the header, i.e., address and control fields of the HDLC frame. The information field is assumed to be an integer number of octets or bytes. The 16-bit CRC-CCITT generator polynomial, $X^{16} + X^{12} + X^5 + 1$ is used for calculating the FCS. The transmitted ABORT sequence has 14 consecutive ones to satisfy SDLC and HDLC requirements.

INV—Invert Data. When set by the host, the R8071 inverts the data prior to transmission whenever the channel is active. When reset by the host, the R8071 sends the data non-inverted, i.e., as it is read from the transmit buffer. With INV bit set by the host (when the channel is idle), an octet of eight zeroes (0s) is sent for HDLC or non-HDLC channels. However, when INV is not set, an octet of eight ones (1s) is sent for idle code. All other data including HDLC flag and ABORT is conditioned by the INV bit.

Note that the combination of the HDLC procedure and data inversion guarantee that there will not be more than five consecutive zero bits in any primary rate channel during data transmission or seven consecutive zero bits during ABORT transmission.

LOOP—Loop Mode. When set by the host, the associated transmit channel data is stored internally in R8071 in addition to being transmitted. If the LOOP bit for the corresponding receive channel is also set, the previously stored transmit channel data can be looped back to the shared memory through the receive channel.

Only one channel can be placed in LOOP mode at any time for reliable loop operation. But the loop channel number, the FILL/MASK and its mode can be specified independently for any transmit and receive channel and need not be identical. Such a provision makes possible powerful software-based diagnostics routines.

Note that the loop mode operation will fail without the host being informed if the host programs only a transmit channel in the loop mode without programming a receive channel. However, the host shared memory will still be filled with the external serial data of the channel, if the channel is active.

FILL/MASK

The second byte of a command buffer contains the FILL/MASK pattern. It is used as a masking pattern on the HDLC-formatted (including FLAG, header, data, CRC and ABORT code) or non-HDLC data to adapt subrates that are multiples of 8 kbps to the 64 kbps rate

TRANSMIT CONSIDERATIONS

Minimum Number of Data Bytes in a Buffer

There is a minimum number of data bytes required in each buffer in order for the R8071 to perform the buffer maintenance and still effect a smooth transition to the next buffer. The minimum number of bytes depends on the type of the buffer and that of the following buffer. Table 2 gives a summary.

Maximum Number of Data Bytes in a Buffer

The number of data bytes in a complete frame buffer, as specified by the DATA LENGTH word, should not exceed 4095 (2^{12}-1) This does not include the optional one-byte FLAG COUNT The number of data bytes in a partial data buffer, as specified by the BUFFER SIZE word, should not exceed 4095 (2^{12}-1)

RECEIVE DATA BUFFER/COMMAND ORGANIZATION

A general organization of data within a buffer and the linking of receive buffers is illustrated in Figure 16 The detail content of a Receive Data Buffer is shown in Figure 17 The content of a Receive Command Buffer is shown in Figure 18. Information within the buffer is organized in to two groups· descriptors and data.

The first group of bytes contains the buffer descriptors, i.e , information such as the link to the next buffer, buffer size, the number of data bytes in the buffer and buffer status. This group of information is mandatory for each buffer.

The second group contains k-bytes of information, k being a variable number They may be the received data (including any header) after processing by R8071 (if necessary), or channel mode and data rate definition information as specified by the host processor.

RECEIVE CHANNEL DESCRIPTORS

The breakdown and the ordering of the seven bytes of descriptors is shown in in Figure 17 The first six bytes contain the next buffer address, the buffer size and the data length—each consisting of two bytes. The relative locations of the upper and the lower bytes are interchangeable by the use of the input strap pin MDFS The seventh byte contains the status of the current receive buffer as well as the status of the receive transmit channel A byte not used by the R8071, and free to be used by the host, will proceed or follow the status byte as determined by MDFS (Figure 14)

Next Buffer Start Address

Bytes 0 and 1 contain the 16-bit NEXT BUFFER ADDRESS written by the host The meaning of invalid and recirculating buffers are the same as those for the transmit buffer.

Buffer Size

Bytes 2 and 3 contain the 12-bit BUFFER SIZE, k, written by the host The BUFFER SIZE specifies the total number of memory bytes allocated by the host for storing the data to be received The four most significant bits are not used by the R8071

The R8071 reads it and stores it for all except command buffers If the last byte of a receive HDLC frame is not received before the buffer is completely filled, the R8071 automatically searches for the availability of the next buffer specified.

Data Length

Bytes 4 and 5 contain the 12-bit DATA LENGTH field, j, written by the R8071. DATA LENGTH specifies the actual number of received data bytes transferred to the receive data buffer by the R8071 The four most significant bits are not used. (The R8071 clears these bits to zeroes.)

DATA LENGTH is written by the R8071 after it receives the last byte of an HDLC frame, receives the HDLC ABORT code, or upon the loss of multiframe alignment error from a non-HDLC signaling channel. DATA LENGTH is not written if the end of the allocated buffer is reached before the last byte is received (data frame length greater than buffer size) In such a case, the data length is equal to the given buffer size. Also, data length may not be written if the ATTN input is asserted, resulting in the deactivation or reactivation of an active channel. DATA LENGTH will not exceed the programmed buffer size DATA LENGTH is not meaningful in a command buffer.

Table 2. Minimum Number of Data Bytes

Current Buffer Status as Set Up by Host			Next Buffer Status as Set Up by Host			Min. No. of Data Bytes in Next Buffer*	Remarks
CMND	MPTY	CF/$\overline{P}$	CMND	MPTY	CF/$\overline{P}$		
1	0	X	0	0	1	2	Complete frame buffer following a command buffer
1	0	X	0	0	0	5	Partial data bufffer following a command buffer
X	X	X	1	0	X	2	Command buffer following any buffer
0	0	1	0	0	0	5	Partial data buffer following a complete frame buffer
0	0	1	0	0	1	2	Complete frame buffer following a complete frame buffer
0	0	0	0	0	1	3	Complete frame buffer following a partial data buffer
0	0	0	0	0	0	6	Partial data buffer following a partial data buffer

*Data byte refers only to the actual header data or information or mode but not the buffer descriptors or the optional flag count

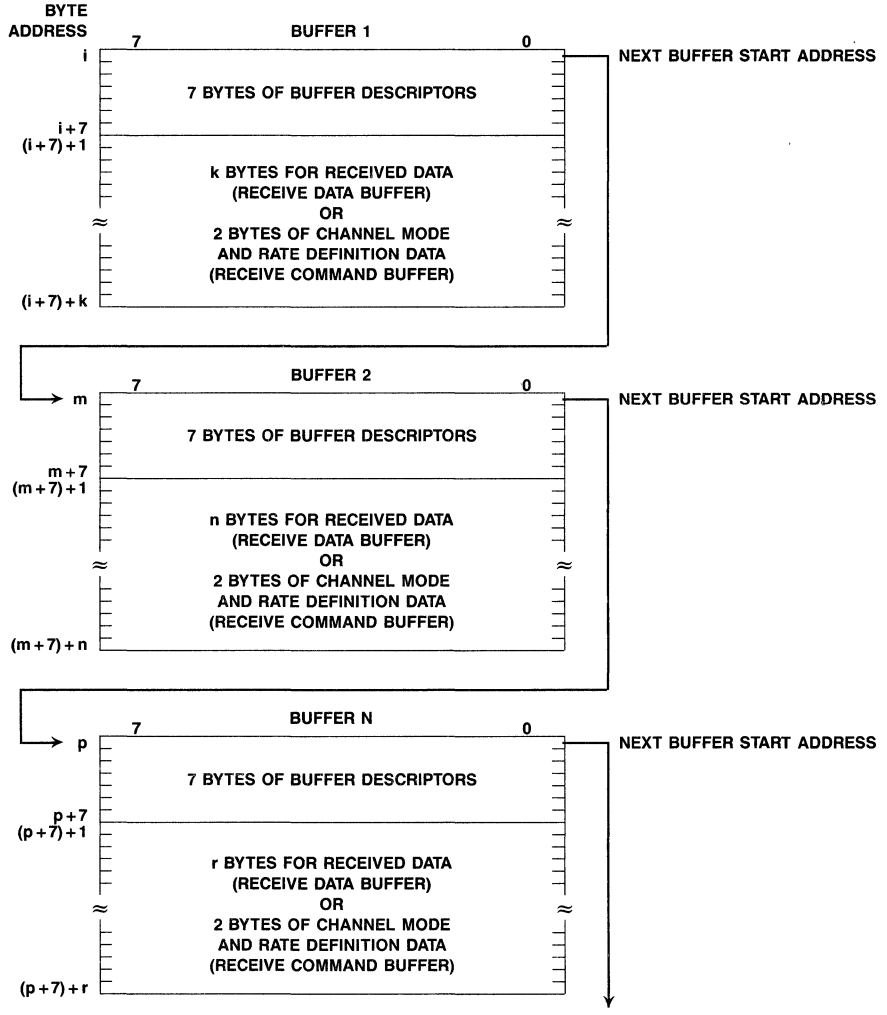


Figure 16. Organization and Linking of Receive Data Buffers

BYTE ADDRESS	CONTENTS 7	6	5	4	3	2	1	0
I	msb NEXT BUFFER ADDRESS							
I+1								lsb
I+2					msb BUFFER SIZE (k)			
I+3								lsb
I+4	X	X	X	X	msb DATA LENGTH (j)			
I+5								lsb
I+6	NOT USED BY R8071							
I+7	STATUS OVER	IVBA	ABRT	FCER	SHER	CF/$\overline{P}$	(0) CMND	MPTY
(I+7)+1	FIRST DATA BYTE							
(I+7)+2	SECOND DATA BYTE							
⋮	⋮							
(I+7)+J	LAST DATA BYTE							
⋮	⋮							
(I+7)+k	LAST LOCATION IN BUFFER							

a. MDFS = High

BYTE ADDRESS	CONTENTS 7	6	5	4	3	2	1	0
I								lsb
I+1	msb NEXT BUFFER ADDRESS							
I+2								lsb
I+3					msb BUFFER SIZE (k)			
I+4								lsb
I+5	X	X	X	X	msb DATA LENGTH (j)			
I+6	STATUS OVER	IVBA	ABRT	FCER	SHER	CF/$\overline{P}$	(0) CMND	MPTY
I+7	NOT USED BY R8071							
(I+7)+1	FIRST DATA BYTE							
(I+7)+2	SECOND DATA BYTE							
⋮	⋮							
(I+7)+J	LAST DATA BYTE							
⋮	⋮							
(I+7)+k	LAST LOCATION IN BUFFER							

b. MDFS = Low

Figure 17. Receive Data Buffer Contents

BYTE ADDRESS	CONTENTS 7	6	5	4	3	2	1	0
I	msb NEXT BUFFER ADDRESS (i)							
I+1								lsb
I+2	NOT USED BY R8071							
I+3								
I+4	NOT USED BY R8071							
I+5								
I+7	NOT USED BY R8071							
I+6	STATUS OVER	IVBA	X	X	X	CF/$\overline{P}$	(1) CMND	MPTY
(I+7)+1	MODES X	X	X	X	INV	LOOP	SIG	HDLC
(I+7)+2	FILL/MASK							

a. MDFS = High

BYTE ADDRESS	CONTENTS 7	6	5	4	3	2	1	0
I								lsb
I+1	msb NEXT BUFFER ADDRESS (i)							
I+2	NOT USED BY R8071							
I+3								
I+4	NOT USED BY R8071							
I+5								
I+6	STATUS OVER	IVBA	X	X	X	CF/$\overline{P}$	(1) CMND	MPTY
I+7	NOT USED BY R8071							
(I+7)+1	MODES X	X	X	X	INV	LOOP	SIG	HDLC
(I+7)+2	FILL/MASK							

b. MDFS = Low

Figure 18. Receive Command Buffer Contents

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Receive Buffer Status

The Receive Buffer STATUS byte specifies the status of the current receive buffer as well as the status of the receive channel. The individual bits are defined as follows.

MPTY—Empty. This bit is set by the host to inform the R8071 that the buffer is empty, i.e., available for storing the received data. When the bit is reset, the buffer is not empty , i. e., not available to store the received data. The R8071 polls this bit until it is empty before it writes the received data.

This bit is reset by the R8071 whenever it updates the buffer status. This is the case even if the R8071 writes only a single byte and then is forced to update the buffer status because of abnormal conditions.

CMND—Command. This bit is set by the host to inform the R8071 that this buffer is a command buffer. The command buffer contains channel-specific mode definition and FILL/MASK information at the next two bytes following the STATUS byte. This bit is reset by the host to indicate that this buffer is a data buffer meant to store received data.

CF/$\overline{P}$—Complete Frame/Partial Data Buffer. This bit may be reset by the host at buffer initialization. This bit is set by the R8071 to indicate that this buffer contains the last byte of an HDLC frame. The R8071 automatically verifies the CRC and the starts the next HDLC frame before writing the data of the next HDLC frame in the next available buffer. In HDLC and Non-HDLC modes, if the reception of data is truncated by a resync condition asserted by an ABORT, RSYNC, TMAX or RRED, the R8071 sets the CF/$\overline{P}$ bit and writes the DATA LENGTH of the truncated buffer. In signalling Channel Mode, when two consecutive signalling synchronization errors are encountered, the R8071 will also set the CF/$\overline{P}$ bit.

This bit is reset by the R8071 to indicate that this buffer contains only a part of the received data and that more data is expected to be placed in one or more succeeding buffers. In HDLC mode, it implies that the last byte of the HDLC frame is not in this buffer. For non-HDLC data and signaling channels, this bit will be invariably reset after the buffer is filled. The R8071 does not read the CF/$\overline{P}$ bit in a command buffer. Note that the host can detect whether a received HDLC frame size exceeded the maximum anticipated buffer size by simply checking for CF/$\overline{P}$ to be set in the starting buffer of the HDLC frame.

ABRT—Abort. This bit is written by the R8071 and, in conjunction within the FCER and SHER bits, reports abnormal conditions detected by the R8071 (see Table 3).

FCER—Frame Check Error. This bit is written by the R8071 and, in conjunction within the ABRT and SHER bits, reports abnormal conditions detected by the R8071 (see Table 3).

SHER—Short HDLC Frame Error. This bit is written by the R8071 and, in conjunction within the ABRT and FCER bits, reports abnormal conditions detected by the R8071 (see Table 3).

IVBA—Invalid Buffer Address. This bit is set by the R8071 if it encounters an invalid next buffer address. In this case, the specific receive channel enters the idle state and will not receive more data until re-activated by the host.

OVER—Overrun. This bit is set by the R8071 after its receive channel has no next data buffer available for received data. Note that a command buffer is not available for data. The OVER bit is written as part of the status of the just completed buffer. Also note that no overrun will be reported for non-HDLC signaling channel data buffers. New data will be written in place of any earlier received signaling data.

Table 3. Receive Buffer Status—Error Table

ABRT	FCER	SHER	Description
0	0	0	No errors detected
0	0	1	Short or Non-integer HDLC Frame Error
0	1	0	CRC Error
0	1	1	CRC Error & Non-integer Error
1	0	0	HDLC ABORT Code Received
1	0	1	Non-HDLC Multiframe Alignment Lost
1	1	0	Elastic Buffer Error & RSYNC Error
1	1	1	RRED Alarm

RECEIVE COMMAND BUFFER

A receive command buffer is identical to the transmit command buffer in that it contains exactly two-bytes of data following the STATUS byte for defining the channel modes and data rate.

The first byte (MODE) defines the channel modes of operation—specifically HDLC, signaling, data inversion and loop back. The second byte (FILL/MASK) defines the data rate. A data buffer contains the actual data received after processing by the R8071.

The breakdown and the ordering of bytes within the command buffer are illustrated in Figure 18.

For a command buffer, the R8071 does not process the bytes at addresses [i+2, i+3] and [i+4, i+5] as the data length is presumed to be exactly two bytes. However, the R8071 reads the next buffer address at locations i and i+1 as part of processing the command buffer. As mentioned before, the relative locations of the upper and the lower bytes of the next buffer address are interchangeable by means of the MDFS input. The mode and FILL/MASK bytes locations are not interchangeable by MDFS.

MODES

The MODES byte is the first byte following the status byte and specifies the operational modes of the given channel—specifically, HDLC or non-HDLC, signaling channel or not, data to be inverted bit-by-bit prior to receiver processing or not and channel receive data source to be the loop register or not.

SIG	HDLC	Mode
1	0	Non-HDLC Signaling Channel Mode
0	0	Non-HDLC Data Channel Mode
0	1	HDLC Data Channel Mode
1	1	Reserved

Non-HDLC Signaling Channel Mode. The R8071 processes the received bit-oriented signaling data without the HDLC format (G.732 or DMI). The R8071 arranges the received signaling data as in Figure 19 for easy association of the channel number and its signaling bits. In addition, errors in multiframe alignment sequence will be detected and any resulting loss of multiframe alignment will be reported in the STATUS byte.

BYTE ADDRESS	CONTENTS							
	7	6	5	4	3	2	1	0
i	NEXT BUFFER ADDRESS = i or j							
i+1								
i+2 ≈ i+7	REST OF THE DESCRIPTORS							
(i+7)+1	X	1	X	X	X	B1	A1	A13
(i+7)+2	X	1	X	X	X	B2	A2	A14
(i+7)+3	X	1	X	X	X	B3	A3	A15
⋮				⋮				
(i+7)+11	X	1	X	X	X	B11	A11	A23
(i+7)+12	X	1	X	X	X	B12	A12	A1
(i+7)+13	X	1	X	X	X	B13	A13	A1
(i+7)+14	X	1	X	X	X	B14	A14	A2
(i+7)+15	X	1	X	X	X	B15	A15	A3
(i+7)+16	X	1	X	X	X	B16	A16	A4
(i+7)+17	X	1	X	X	X	B17	A17	A5
⋮				⋮				
(i+7)+23	X	1	X	X	X	B23	A23	A11
(i+7)+24	1	0	Ys	0	1	1	1	A12

a. T1 Mode

BYTE ADDRESS	CONTENTS							
	7	6	5	4	3	2	1	0
i	NEXT BUFFER ADDRESS = i or j							
i+1								
i+2 ≈ i+7	REST OF THE DESCRIPTORS							
(i+7)+1	D17	C17	B17	A17	D1	C1	B1	A1
(i+7)+2	D18	C18	B18	A18	D2	C2	B2	A2
(i+7)+3	D19	C19	B19	A19	D3	C3	B3	A3
⋮				⋮				
(i+7)+11	D27	C27	B27	A27	D11	C11	B11	A11
(i+7)+12	D28	C28	B28	A28	D12	C12	B12	A12
(i+7)+13	D29	C29	B29	A29	D13	C13	B13	A13
(i+7)+14	D30	C30	B30	A30	D14	C14	B14	A14
(i+7)+15	D31	C31	B31	A31	D15	C15	B15	A15
(i+7)+16	1	1	Ys	1	0	0	0	0

b. CEPT PCM 30 Mode

Figure 19. Receive Buffer Data Arrangement for Non-HDLC Bit-Oriented Signaling Channel

Non-HDLC Data Channel Mode. The channel is a non-HDLC data channel that can support DMI data modes 0 or 1.

As soon as a channel receiver is activated with mode, the R8071 checks the availability of the allocated buffer and starts placing the received data in the buffer. After filling a buffer, it updates the status of the just completed buffer, simultaneously asserting $\overline{INTR}$. It then moves on to the next allocated buffer. Since non-HDLC data has no frame boundary, this process will continue forever unless the host interrupts by an ATTN or the system runs out of allocated buffers.

HDLC Data Channel Mode. The channel is to receive HDLC-formatted data. It can imply an HDLC-formatted data channel, such as the ones in DMI mode 2 or 3 or X.25 LAPB, or a message-oriented signaling channel as in LAPB. The R8071 treats each one of them the same way and deformats the data. No special handling is performed on the header, i.e., the address and control fields of the HDLC frame. The information field is assumed to be an integer number of octets or bytes. The 16-bit CRC-CCITT generator polynomial, $X^{16} + X^{12} + X^5 + 1$ is used for recomputing the FCS. Abort and flag characters are recognized as are intentionally inserted zeroes.

INV—Invert Data. When set by the host, the R8071 inverts the received data prior to processing. When INV is reset by the host, the R8071 does not invert the received data. The INV bit is applied to every received bit.

LOOP—Loop Mode. When set by the host, the R8071 selects as its input the serial output data from the internal loop data buffer, as opposed to the externally supplied serial data. If an identically numbered transmit channel was also programmed to be in the loop mode earlier, data from that channel is looped back to the shared memory through the receive channel. The loop channel number, FILL/MASK, and its mode can be specified independently for any transmit and receive channel and need not be identical. If no transmit channel has loop activated, the R8071 processes the channel as if a receiver RRED condition were active for that channel duration.

FILL/MASK

The second byte of a command buffer contains the FILL/MASK pattern. It is used as a masking pattern on the HDLC-formatted (including flag, header, data, CRC, and ABORT code) or non-HDLC data to adapt subrates that are multiples of 8 kbps to the 64 kbps rate.

Table 4 shows the data rates of the form n × 8 kbps (n = 1, 2, . . . , 8) and several examples of codes for the FILL/MASK to adapt the subrates to the 64 kbps rate. The actual data bit is transmitted on TSER output as long as the FILL/MASK is a 1 at the corresponding bit position. If the FILL/MASK = 0, a FILL bit of 1 is transmitted in place of the data bit on TSER as long as TSEREN = 1. The data bit that is held in favor of the FILL bit is buffered internally until all the FILL bits have been transmitted corresponding to the FILL/MASK bits equalling 0.

Table 4. Examples of FILL/MASK Options

Option No.	Data Rate	Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Remarks
0*	0 Kbps	0	0	0	0	0	0	0	0	No data will be sent. A time FILL of eight 1s will be sent provided TSEREN = 1.
1	8 Kbps	0	0	0	0	0	0	0	1	
		0	0	1	0	0	0	0	0	Arbitrary-user defined. A 1 in any one bit position but only one 1.
2	16 Kbps	0	0	0	0	0	0	1	1	
		0	0	0	0	1	1	0	0	User defined patterns, a 1 in any 2 bit positions but only two 1s
		0	0	1	1	0	0	0	0	
		1	1	0	0	0	0	0	0	
3	24 Kbps	0	0	0	0	0	1	1	1	A total of three 1s anywhere as defined by user
		0	1	0	1	0	1	0	0	
4	32 Kbps	0	0	0	0	1	1	1	1	A total of four 1s anywhere as defined by user
		1	1	1	1	0	0	0	0	
		1	0	1	0	1	0	1	0	
5	40 Kbps	0	0	0	1	1	1	1	1	A total of five 1s anywhere as defined by user.
6	48 Kbps	0	0	1	1	1	1	1	1	A total of six 1s anywhere as defined by user.
7	56 Kbps	0	1	1	1	1	1	1	1	Standard rate in Digital Data Service, restricted version of 64 Kbps.
		1	1	1	1	1	1	1	0	A total of seven 1s anywhere as defined by user.
8	64 Kbps	1	1	1	1	1	1	1	1	

*Special purpose mode, transmitter operates as if at 64 Kbps including fetching data from shared memory, even though no data is transmitted

When the FILL/MASK bit becomes a 1 again, the buffered data bit is transmitted on a first in-first out basis (Figure 7.)

Thus, there is a one-to-one correspondence between the FILL/MASK bit and the T1 or CEPT PCM 30 channel serial data associated with the FILL/MASK bit position.

When the FILL/MASK bit is 0, TSEREN determines what is to be transmitted on TSER:

Data Bit	FILL/MASK Bit	TSEREN	TSER (Output)
1	1	X	1
0	1	X	0
X	0	1	1
X	0	0	High Z

The data bit may be the same as, or logical complement (inverted version), of the actual data.

A bit-oriented 64 kbps signaling channel should be programmed with 1111 1111 as the FILL/MASK. The R8071 will not override any other user-supplied FILL/MASK pattern even if it is erroneous, i.e., not equal to 1111 1111. An IDLE bit-oriented signaling channel will carry 1111 1111 as long as the channel is IDLE. Any remote receiver will not be able to achieve signaling channel multiframe alignment if 1111 1111 is received continuously.

RECEIVE CONSIDERATIONS

Minimum Buffer Size

There is a minimum number of memory locations that have to be allocated in each buffer for the R8071 to perform the buffer maintenance and still effect a smooth transition to the next buffer without losing data. The minimum buffer allocations for data must allow six data bytes in addition to the seven bytes of descriptors. Command buffers have exactly two bytes and are processed without regard for the BUFFER SIZE word.

Note: The minimum HDLC frame received can have as few as two bytes of data and the R8071 will still function properly; however, it is essential that a buffer size of six must be allocated as a minimum since the received frame size is not known apriori.

SHARED MEMORY ACCESS

The R8071 accesses shared memory for buffer maintenance, command data, information and also for channel activation. It manages the buffer memory for up to 64 channels (32 transmit and 32 receive).

The T1 or CEPT PCM 30 data throughput requirements demand that one octet of data be supplied to the transmitter and one octet of data be taken from the receiver in a single channel period (8 TCLK periods). The host and the R8071 must work cooperatively to meet the data throughput requirements. The R8071 uses a memory access scheme that simplifies the system design in achieving the required data throughput.

The R8071 processes the memory requirements of up to 32 channels in the same order in which they are multiplexed in a T1 or CEPT PCM 30 carrier system. Typically, during TX channel m (for example), the R8071 fetches a single data byte from memory for the transmitter so that it can transmit it over channel m at the next appropriate T1 or CEPT PCM 30 frame. Similarly, the last data byte received by channel j is written to the memory by the R8071 during the next appropriate receive channel j. Then it services TX channel (m + 1) and RX channel (j + 1) and so on.

The R8071 divides a channel period in to two halves, each for a duration of 4 TCLK periods. During the first half-channel period, it accesses the shared memory for channel command information, buffer descriptors, and/or transmit buffer data (including mode definition data) for a transmit channel. During the second half-channel period, it accesses the shared memory for channel command information, buffer descriptors (including mode definition data), and/or received data for a receive channel. Since the transmit and the receive channel boundaries are generally unrelated, an elastic buffer is used to synchronize the receive channel boundary to that of the transmit channel. Hence, no contention exists between a transmit channel and receive channel for the shared memory.

In each half-channel period, under normal circumstances, the R8071 accesses shared memory once for data. If descriptor information is also to be updated, it accesses shared memory a second time. Additionally, if system memory access is also required (as determined by assertion of the ATTN input), it accesses shared memory a third time. In summary, different states of buffer processing will cause anywhere from zero to three accesses to shared memory for an active channel during a half-channel period.

At the start of every half-channel period, the R8071 outputs the binary code for the 5-bit channel number (CH0–CH4) being served. It also specifies whether it is the receive or transmit channel via the RX/$\overline{TX}$ output. About one-half TCLK period later, the R8071 asserts the Memory Demand (DMND) output. DMND rising edge informs any external shared memory arbitration logic that the R8071 needs unconditional access to the shared memory within one TCLK period from DMND rising edge. Note that the R8071 will not wait for a memory acknowledge to start memory access. Thus there is an implied memory acknowledge after one TCLK. See Figure 20 for timing. Prior to asserting $\overline{READ}$ or $\overline{WRITE}$ strobes, the R8071 asserts Memory Address Strobe ($\overline{AS}$).

At $\overline{AS}$ falling edge, the memory address on the A0–A15 lines is valid. Simultaneously, when the memory address changes, the output SYSACC is asserted provided the system memory is being addressed. Moreover, the R8071 will selectively tri-state the high order memory address lines (A8–A15) during the system memory accesses when specified so by UAEN.

Following $\overline{AS}$, the R8071 asserts the $\overline{READ}$ or $\overline{WRITE}$ output strobe for read or write operation, respectively. The data on the data bus (D0–D7) is latched by R8071 just prior to the rising edge of $\overline{READ}$ during a read operation. Data placed on the data bus is written to the memory during the period that $\overline{WRITE}$ is low.

Address setup time, address hold time, data setup time, and data hold time are specified such that a wide variety of off-the-shelf RAM devices may be used. The $\overline{READ}$ output from R8071 may be used as an Output Enable ($\overline{OE}$) input to the RAM devices. Since the R8071 uses its SYSCLK input to generate the various strobes for memory access, the access time requirements are automatically scaled depending on the T1 or CEPT PCM 30 application.

Once the R8071 makes the first memory access, it assumes that continued access to the memory is guaranteed as long as DMND is active. It no longer waits for one TCLK period before the actual memory access. At the most, there may be two more memory accesses. Such a case is illustrated in Figure 20. After completing the needed memory accesses, the R8071 negates the DMND output indicating that it no longer needs access to memory. It also negates the SYSACC output as long as it does not access system memory locations.

The minimum one TCLK latency (two TCLK periods with ATTN inactivity) between DMND and the actual memory access is considered to be sufficient for an external arbitration logic to release the memory bus to the R8071. Failure to do so may cause loss of data and unpredictable operation. The time between DMND going low and the start of the first memory access by R8071 is considered to be sufficiently long either for a single complete memory bus cycle by the host or for the completion of a pending host memory bus cycle. Since the R8071 does not wait for a memory acknowledgement, DMA-like operation using a single external shared address and a data bus cannot be guaranteed.

Examples of the R8071 to shared memory interface waveforms are shown in Figure 20.

MEMORY ADDRESS EXTENSION

The 16-bit memory address output by the R8071 may be extended to more than 16 bits by the use of the channel number (CH0–CH4) and RX/$\overline{TX}$ bits. These six bits may be used directly as higher order address bits for a 22-bit address, or they can be mapped by an external look-up table to another set of n bits (where n is specified by the host). Since the channel number and RX/$\overline{TX}$ are output by the R8071 well in advance of the 16-bit address, address translation time is not of any concern.

Address selection for the system memory locations can be achieved by the host by using the SYSACC output and the UAEN input. External hardware can jam any address on the upper eight bits of the R8071 memory address, i.e., A8–A15, since the R8071 tri-states them (if UAEN is active during SYSACC.)

MEMORY ADDRESS RESTRICTIONS

System Memory Address

The R8071 checks the start address of the first buffer of any channel for an invalid address. It does the above check immediately after it reads the 2-byte start address from the system memory, as part of servicing the ATTN interrupt from the host If an invalid start address is detected for any channel, that channel is forced inactive automatically.

Data Buffer Memory Addresses

The R8071 checks the next buffer address for an invalid address for all the channels. If it is an invalid address, it forces the corresponding channel to an inactive state and also sets the IVBA status bit. Recovery from an idle state to an active state is possible only if the host system asserts the ATTN input to the R8071 In host systems using more than 16 bits for shared memory address, an invalid address, as interpreted by the R8071, refers to all addresses divisible exactly by 65,536 or an address of the form $n \times 2^{16} \times (1111\ 1111\ 1111\ XXXX)$, where n is a power of 2 Within each 64 kbyte address block, only addresses 0001–FFEF (hex) are valid

The R8071 BMM internal adder calculates the absolute memory address from the given buffer start address and any offset needed to locate either the bookkeeping information or the data byte. The maximum address within a buffer for a given channel is the address of the last byte of the buffer Since it is always represented by a 16-bit binary number, it is restricted to 65,535 (decimal) In other words, it is reduced to modulo 65,536. Hence, the following bound,

16-bit address of the last byte = 16-bit buffer start address
+ 610 (for bookkeeping)
− 12-bit data length or buffer size

≤ 65,535 (decimal) or FFFF (hexadecimal)

should be strictly adhered to when programming the **buffer start address** and the **Data Length/Buffer Size**; otherwise, the R8071 will access memory locations not intended for that channel

It is to be emphasized that the R8071 **does check** for buffer start addresses in the range FFF0 through FFFF and declares them as invalid addresses. For systems using more than 65,535 byte addresses, all shared memory addresses must be within one 64 kbyte page or bank.

INTERRUPT INDICATION

The R8071 asserts the Interrupt Indication ($\overline{INTR}$) output anytime the status of any buffer is updated (written) by the R8071. See Figure 20 for timing illustration. The active period of $\overline{INTR}$ is one-half TCLK period At the rising edge of $\overline{INTR}$, the channel number (including RX/$\overline{TX}$) and its current buffer status placed on the data bus are guaranteed to be valid so that they can be captured in an external FIFO queue. The R8071 does not queue the interrupts and their causes internally nor does it wait for an interrupt acknowledge from the host before removing the interrupting channel number and its buffer status. The R8071 processes a channel only for a half-channel period and then moves on to the next channel

In addition to capturing the channel number and buffer status, external hardware can also capture the actual memory address of the status byte in another FIFO queue. By reading such a queue, the host system can reallocate the completed buffers in any way it sees fit and also cross-check against its own list of linked buffer addresses If all the buffer start addresses are divisible exactly by eight, they can be derived from the STATUS byte addresses in the FIFO queue by simply setting the three LSB addresses to zero

DEVICE INITIALIZATION

Upon reset, all the transmit channels are forced to the inactive state All the transmit channels are initialized to the HDLC INV, NON-SIG data mode with a FILL/ MASK byte of eight 0s. No data is transferred from memory. All the receive channels are forced to the idle state They are initialized to the HDLC data mode with a FILL/MASK byte of eight 0s No data is written to the shared memory. The input strap pins define the TDM format, i e., T1 or CEPT PCM 30, and also the hyperchannel grouping. The modes bits are assumed to be (INV = 1, LOOP = 0, SIG = 0) in addition to HDLC = 1 for each channel.

The Transmit Multiframe Sync (TMAX) pulse is assumed to be valid for the purpose of generating an internal channel number. The Receive Multiframe Sync (RSYNC) pulse and the RRED input are monitored by the R8071 to ascertain the receiver framing synchronization

CHANNEL INITIALIZATION

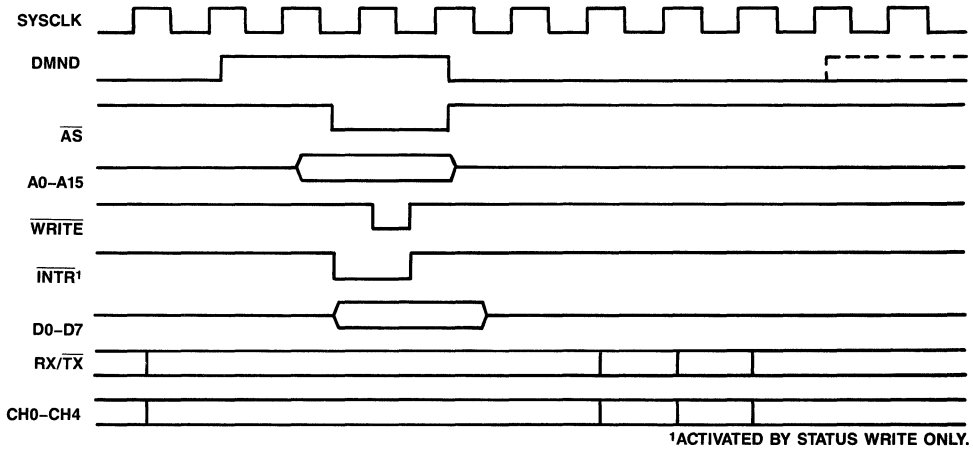
The host may activate any transmit or receive channel to any mode, by pointing it to a command buffer. It does so in a simple and systematic manner as illustrated in Figure 21.

It chooses a starting address for a command buffer and writes the 2-byte starting address as the data at the system memory location dedicated to the channel to be initialized It then prepares a command buffer at the above starting address by specifying the descriptor information and the mode of operation. A linked list of data buffers is set up by the host following the command buffer. This completes the preparation for activating a channel.

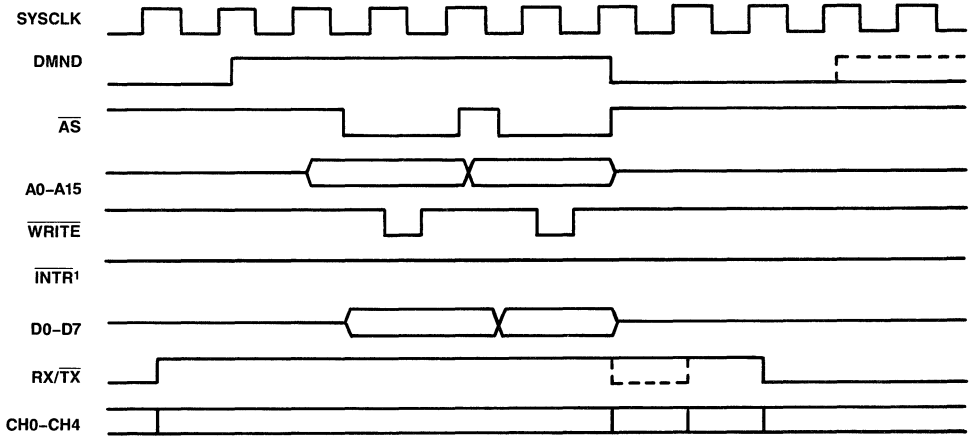
As the last step, the host writes to Channel Activation Byte containing the the channel number, channel direction and the activation command then asserts the ATTN input to the R8071

If ATTN is asserted, the R8071 first reads the Channel Activation Byte. Based on the channel number, it then reads the starting address of the first buffer from the Channel Buffers Pointers, one byte at a time It stores the starting buffer address internally and acknowledges the task completion by asserting ATACK The host system must respond to ATACK negating ATTN.

The negation of ATTN causes ATACK output to be negated. Thus the channel initialization process is complete. This process can be repeated for each channel that needs to be initialized. During each system memory access the R8071 asserts the SYSACC output. It needs to make three system memory accesses to complete the channel ATTN processing The worst case time delay from ATTN assertion to ATACK assertion is three T1 or CEPT PCM 30 channel periods The earliest is $1\frac{1}{2}$ channel periods Since this is guaranteed, the host need not be polling the ATACK output blindly nor need it service the ATACK as an interrupt. Sample channel initialization sequences are shown in Figures 22 and 23.

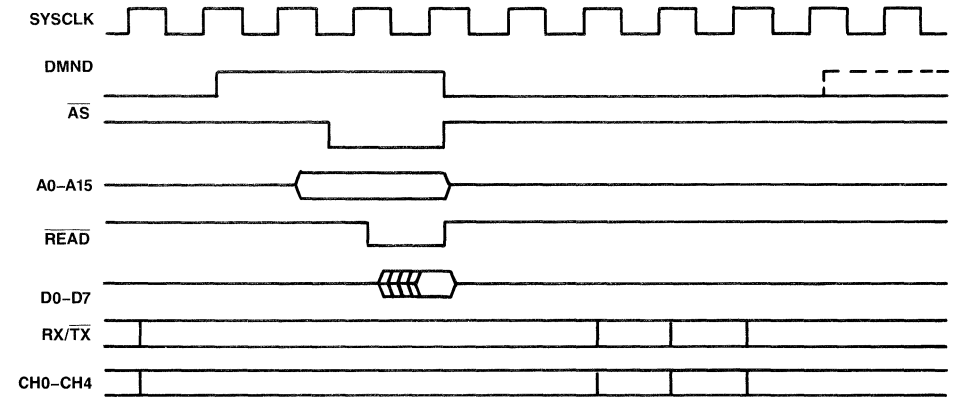


a. Single Write Memory Access

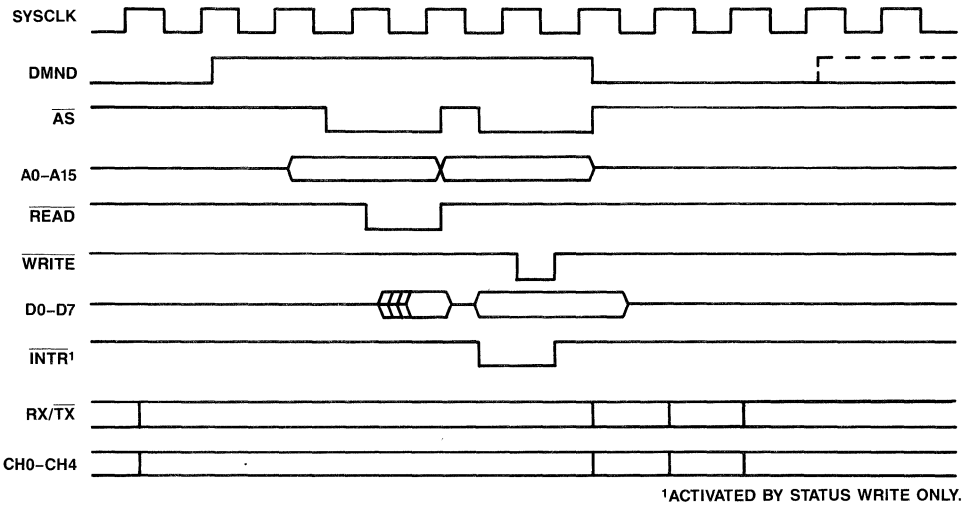


b. Double Write Memory Access

Figure 20. R8071 Shared Memory Example Interface Waveforms

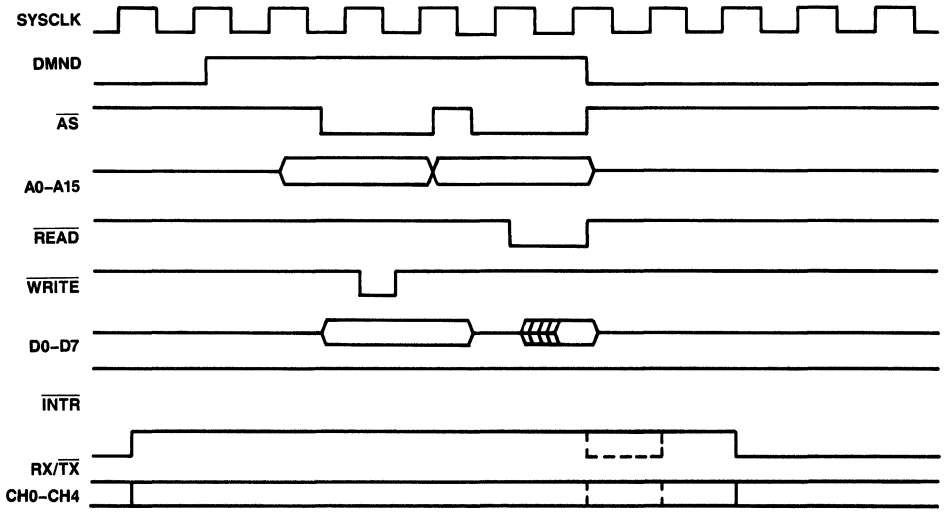


c. Single Read Memory Access

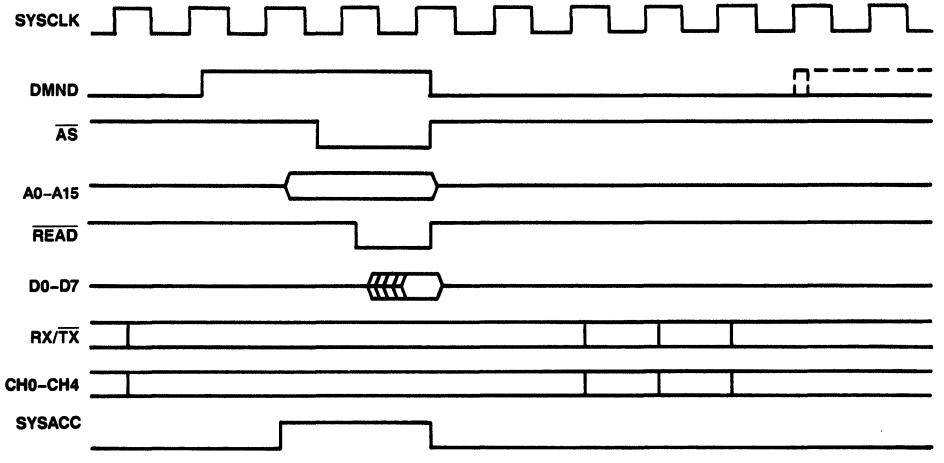


d. Read/Write Double Memory Access

Figure 20. R8071 Shared Memory Example Interface Waveforms (Continued)

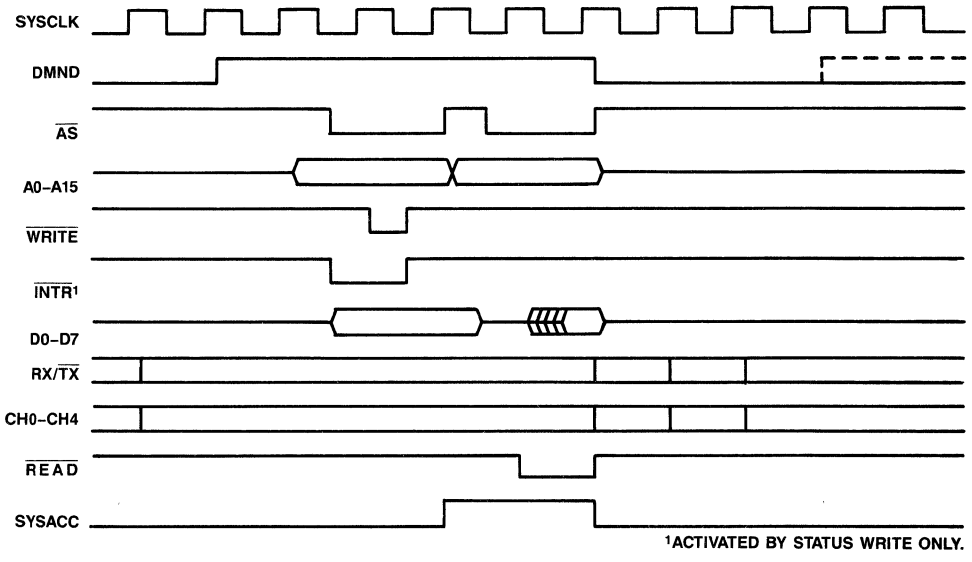


e. Write/Read Double Memory Access

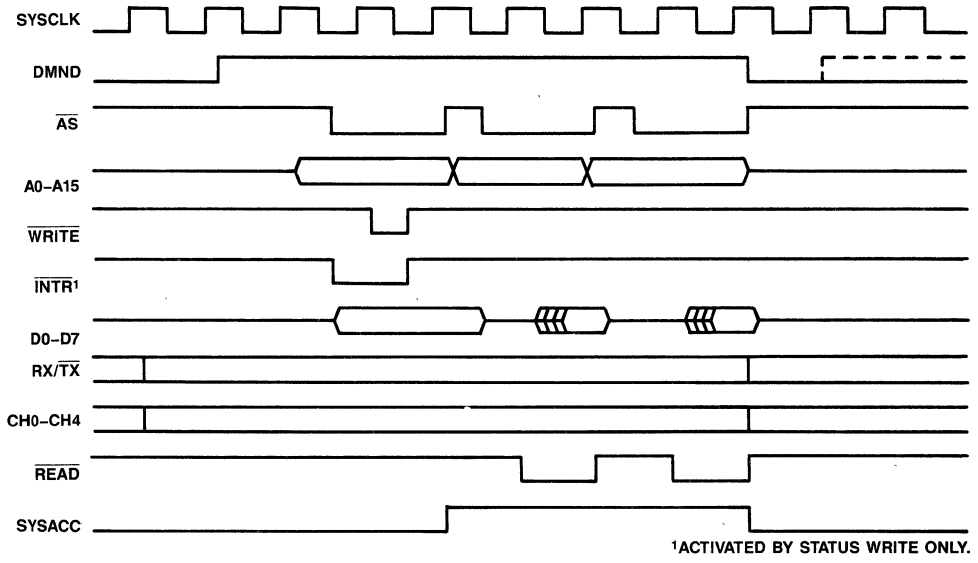


f. Single System Read Memory Access

Figure 20. R8071 Shared Memory Example Interface Waveforms (Continued)

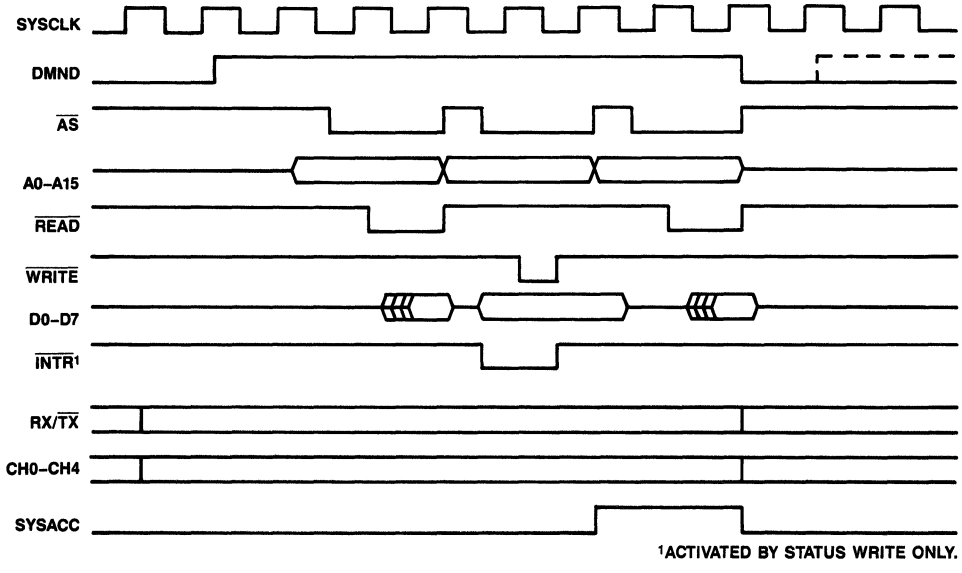


g. Single Write Memory Access Plus a Single System Read Access



h. Single Write Memory Access Plus a Double System Read Access

Figure 20. R8071 Shared Memory Example Interface Waveforms (Continued)



i. Write/Read Double Memory Access Plus Single System Read Access

Figure 20. R8071 Shared Memory Example Interface Waveforms (Continued)

ORDER OF DATA

Transmission

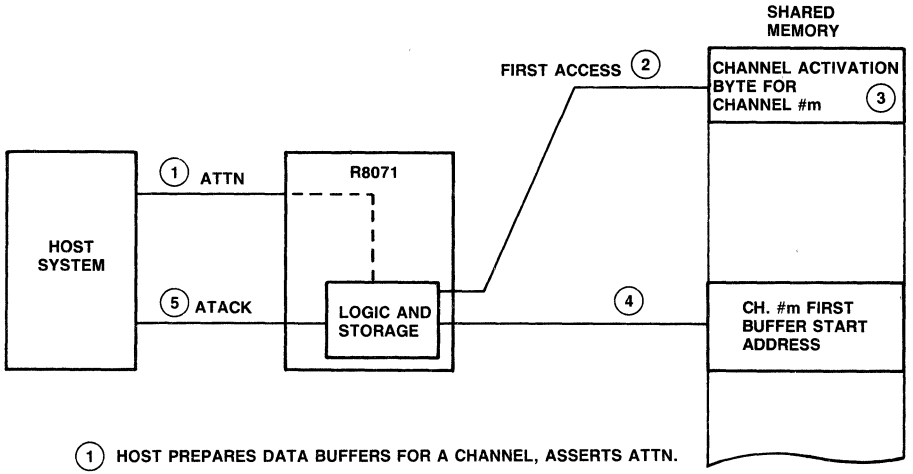
The R8071 transmits data bytes in the same time sequence as they are arranged in ascending addresses in the external buffers. The data at byte address m is transmitted first, the one at address m + 1 is transmitted next, and so on as long as the data bytes are in the same buffer. After the data in a single buffer is exhausted, the R8071 starts to transmit the next byte from the next buffer whose address is specified in the current buffer. The transition to the next buffer is transparent to the host while maintaining the flow of actual data.

The R8071 transmits the LSB (D0) of a data byte first; the next LSB is transmitted second; the MSB (D7) is transmitted last. The only exception is that the MSB of the HDLC FCS (CRC-CCITT) is transmitted first; the LSB is transmitted last.

Reception

The R8071 writes received data bytes in the external shared memory in the same order in which they are received in time. The first received byte is written at byte m, the second received at byte address m + 1, and so on as long as the buffer is not completely filled or an end-of-frame is not reached. After the end of the frame or the end of the buffer (whichever occurs first) is detected, the R8071 writes the next received data byte at the first allocated address of the next available buffer. The transition to the next buffer is transparent to the host and maintains the flow of the actual data.

The R8071 writes the first received data bit of an octet at the LSB (D0) position of the external buffer byte; the second received data bit at the next to LSB position and so on. The last (eighth) received data bit of an octet is written at the MSB (D7) position of the data byte.



1. HOST PREPARES DATA BUFFERS FOR A CHANNEL, ASSERTS ATTN.
2. R8071 SENSES ATTN, READS CHANNEL NO. IN CHANNEL ACTIVATION BYTE.
3. R8071 ADDRESSES THE MEMORY LOCATION DEDICATED FOR THE SPECIFIC CHANNEL.
4. R8071 READS AND STORES THE START ADDRESS OF THE FIRST BUFFER ALLOCATED FOR THE CHANNEL.
5. R8071 ACKNOWLEDGES TASK COMPLETION BY ASSERTING ATACK.

Figure 21. Channel Initialization

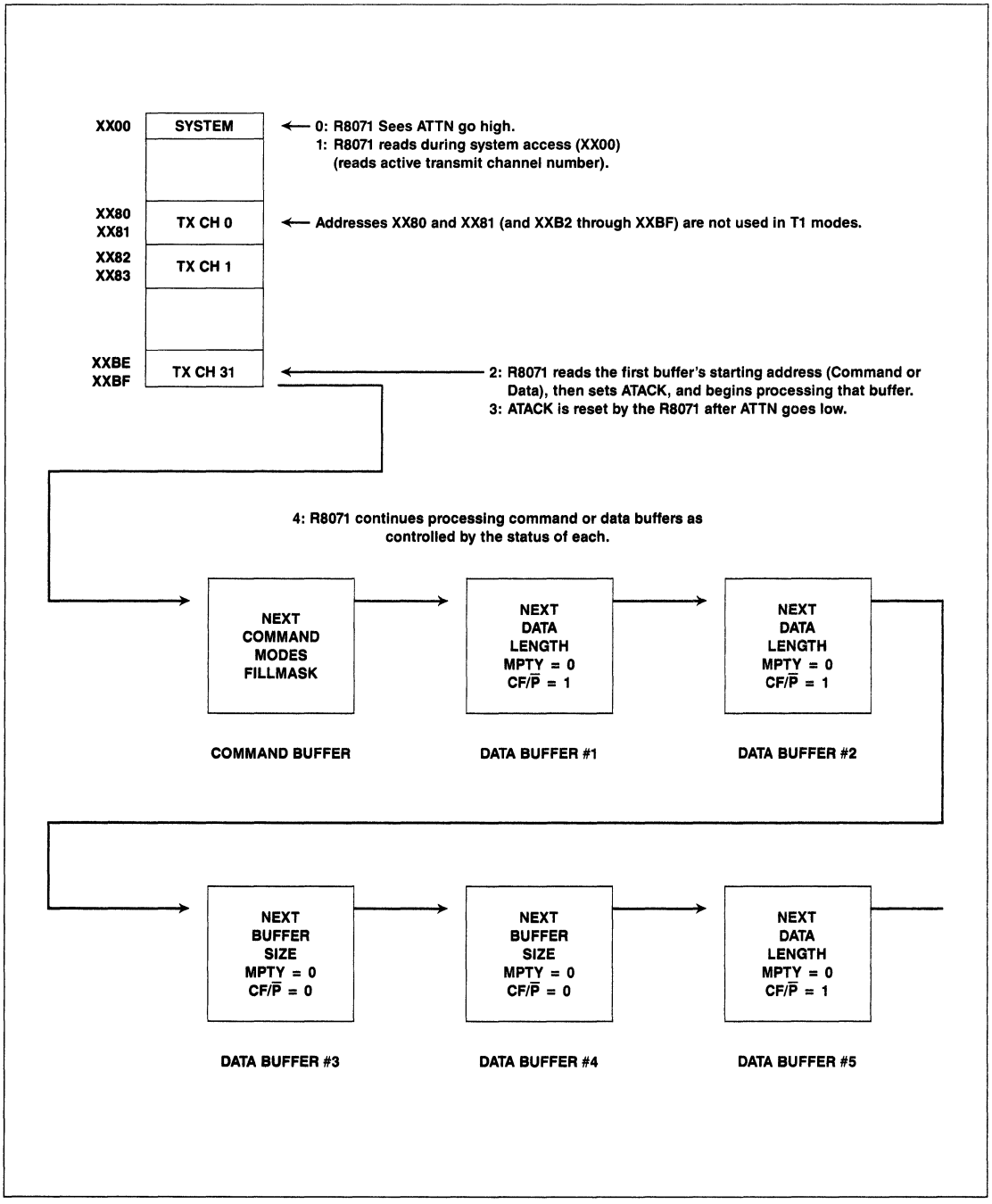


Figure 22. A Typical Linked Buffer Transmit Sequence

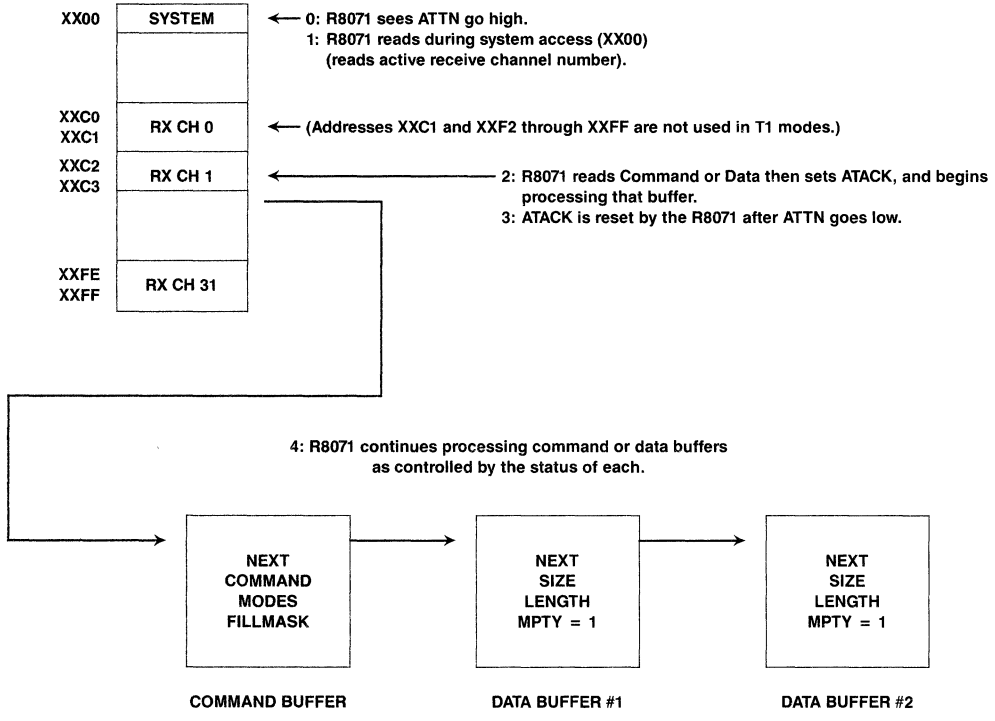
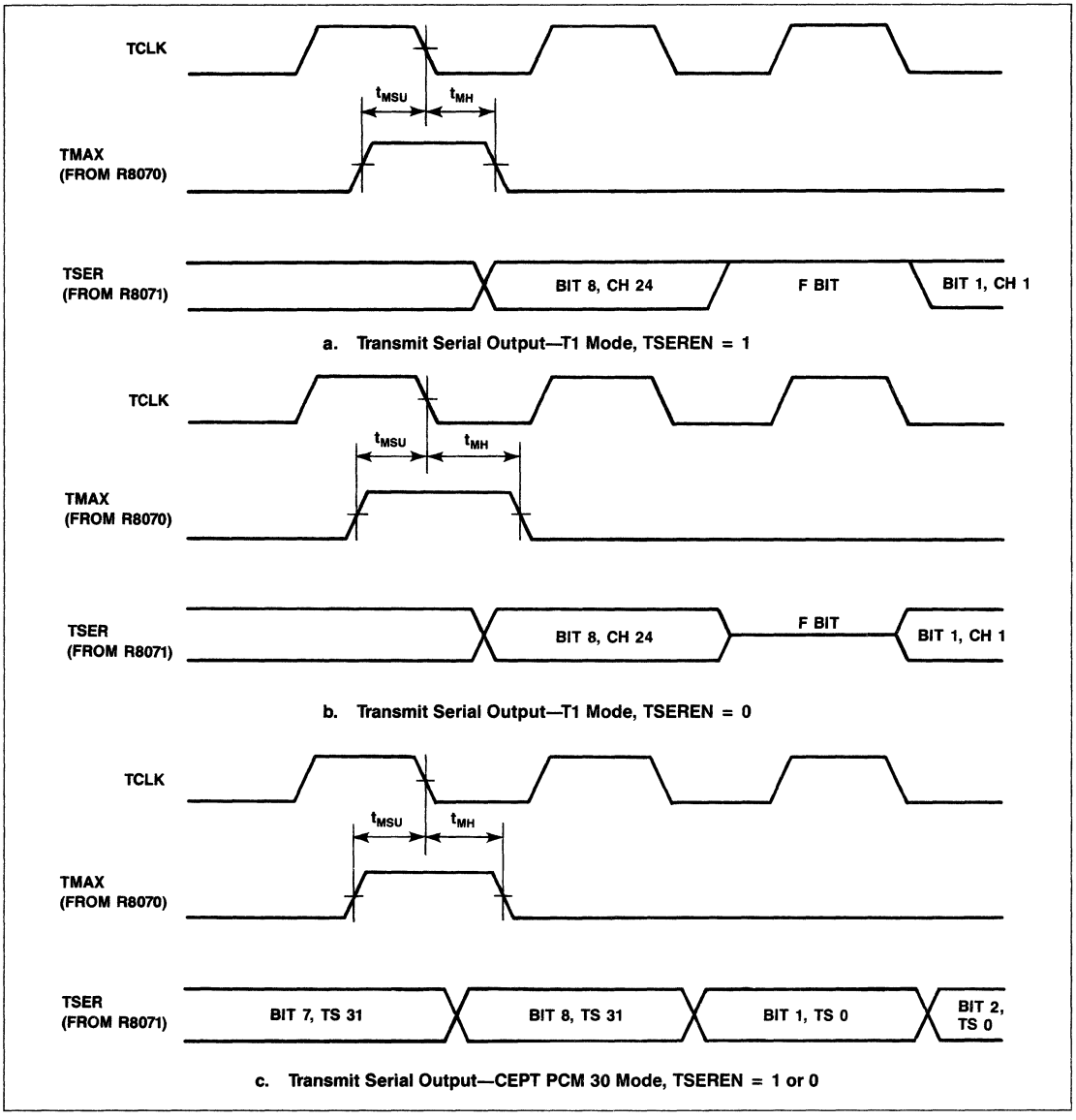


Figure 23. A Typical Linked Buffer Receiver Activity

SWITCHING CHARACTERISTICS

R8070 INTERFACE—R8071 TRANSMIT FRAME SYNCHRONIZATION TIMING



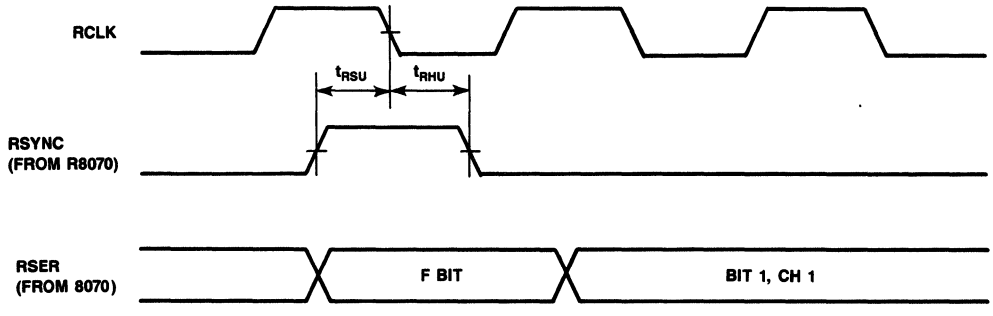
R8071 Transmit Frame Snchronization Waveforms

R8071 Transmit Frame Synchronization Timing

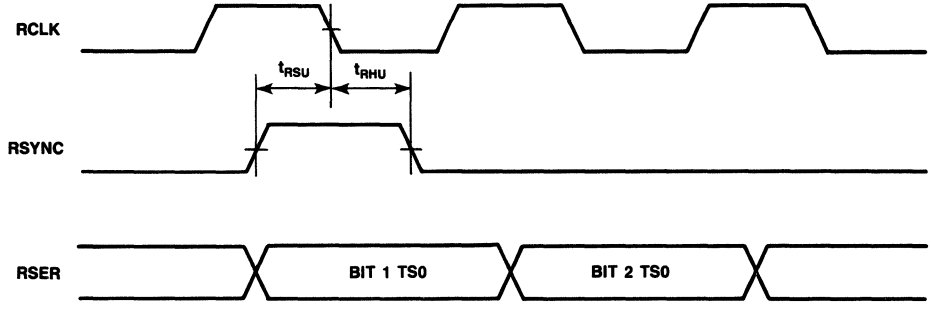
Symbol	Parameter	Min.	Max.	Units
t_{MSU}	TMAX Setup time	60	—	ns
t_{MH}	TMAX Hold time	60	—	ns

SWITCHING CHARACTERISTICS (Cont'd.)

R8070 INTERFACE



a. Receiver Serial Input—T1 Mode



b. Receiver Serial Input—CEPT PCM 30 Mode

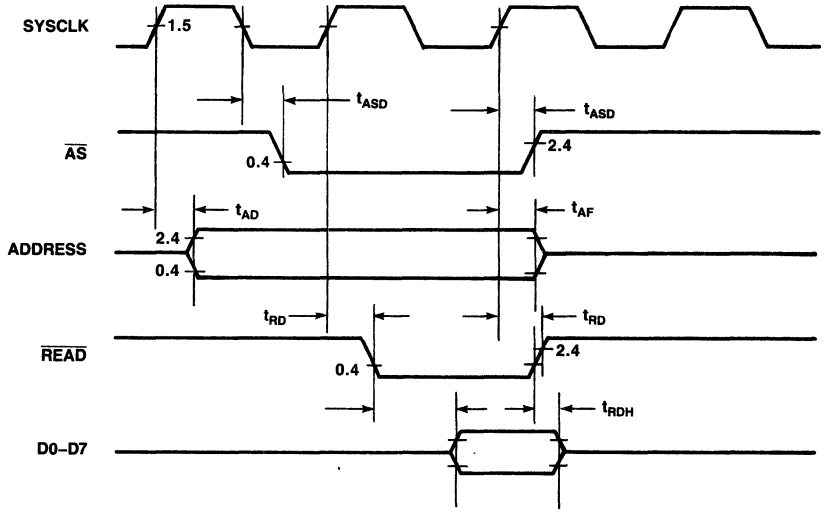
R8071 Receive Frame Synchronization Waveforms

R8071 Rescue Frame Synchronization Timing

Symbol	Parameter	Min.	Max.	Units
t_{RSU}	RSYNC Setup time	50	—	ns
t_{RHU}	RSYNC Hold time	50	—	ns

SWITCHING CHARACTERISTICS (Cont'd.)

SHARED MEMORY INTERFACE



Read Cycle Waveforms

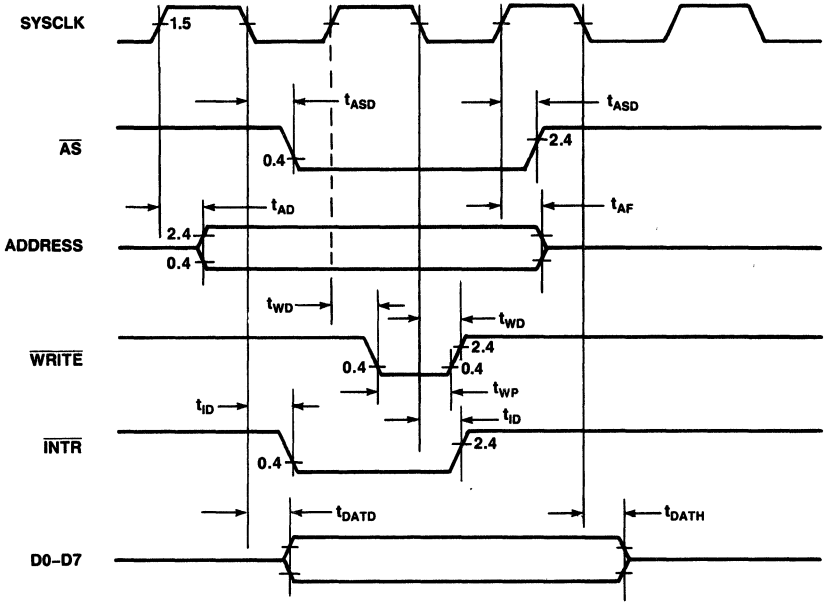
Read Cycle Timing

Parameter	Symbol	Min.	Max.	Units
Address Strobe Delay	t_{ASD}	10	75	ns
Address Delay	t_{AD}	10	90	ns
Address Float Delay	t_{AF}	10	90	ns
Read Enable Delay	t_{RD}	10	75	ns
Read Data Access Time	t_{RDA}	—	Note 1	ns
Read Data Hold Time	t_{RDH}	0	Note 2	ns

Notes:
1. Read Data Access time for shared memory = t_{SCP} – 125 ns.
2. Data Drive to Data Bus Float = t_{SCPW} – 65 ns

SWITCHING CHARACTERISTICS (Cont'd.)

SHARED MEMORY INTERFACE (Cont'd.)



Write Cycle Waveforms

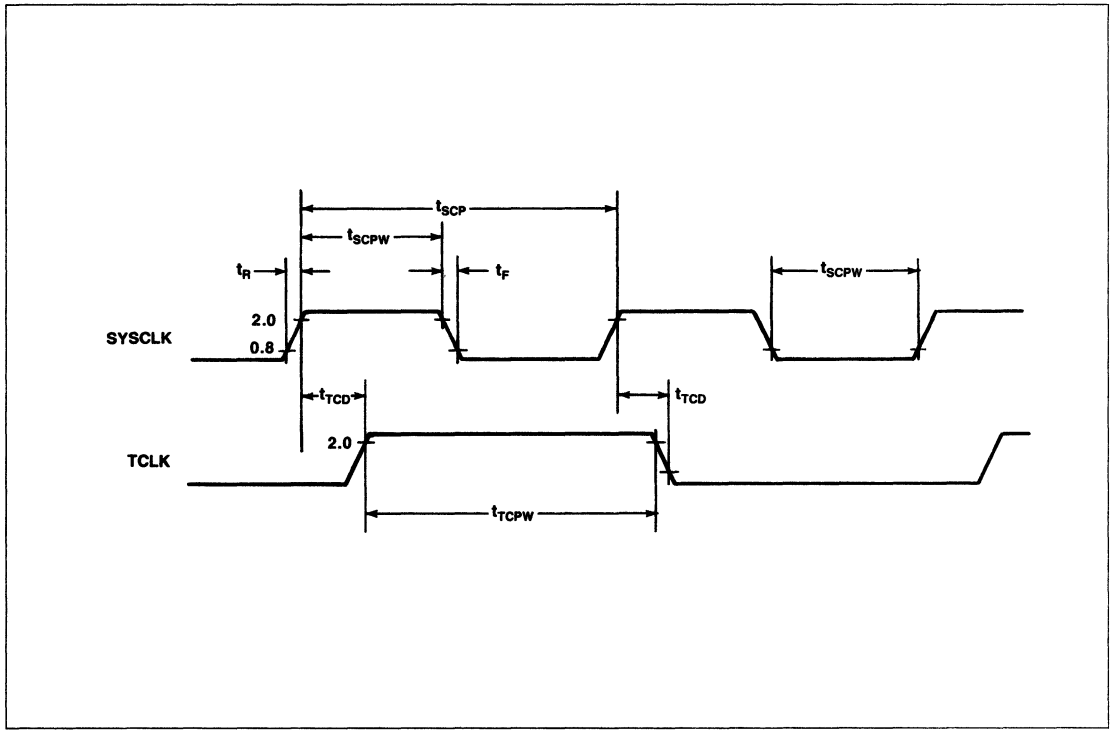
Write Cycle Timing

Parameter	Symbol	Min.	Max.	Units
Address Strobe Delay	t_{ASD}	10	75	ns
Address Delay	t_{AD}	10	90	ns
Address Float Delay	t_{AF}	10	90	ns
Write Delay	t_{WD}	10	75	ns
Write Pulse Width	t_{WP}	80	—	ns
Interrupt Delay	t_{ID}	10	75	ns
Write Data Delay	t_{DATD}	10	90	ns
Write Data Hold Time[1]	t_{DATH}	10	90	ns

Note:
1 Data Drive to Data Bus Float time

SWITCHING CHARACTERISTICS (Cont'd.)

LIU INTERFACE



R8071 Clock Waveforms

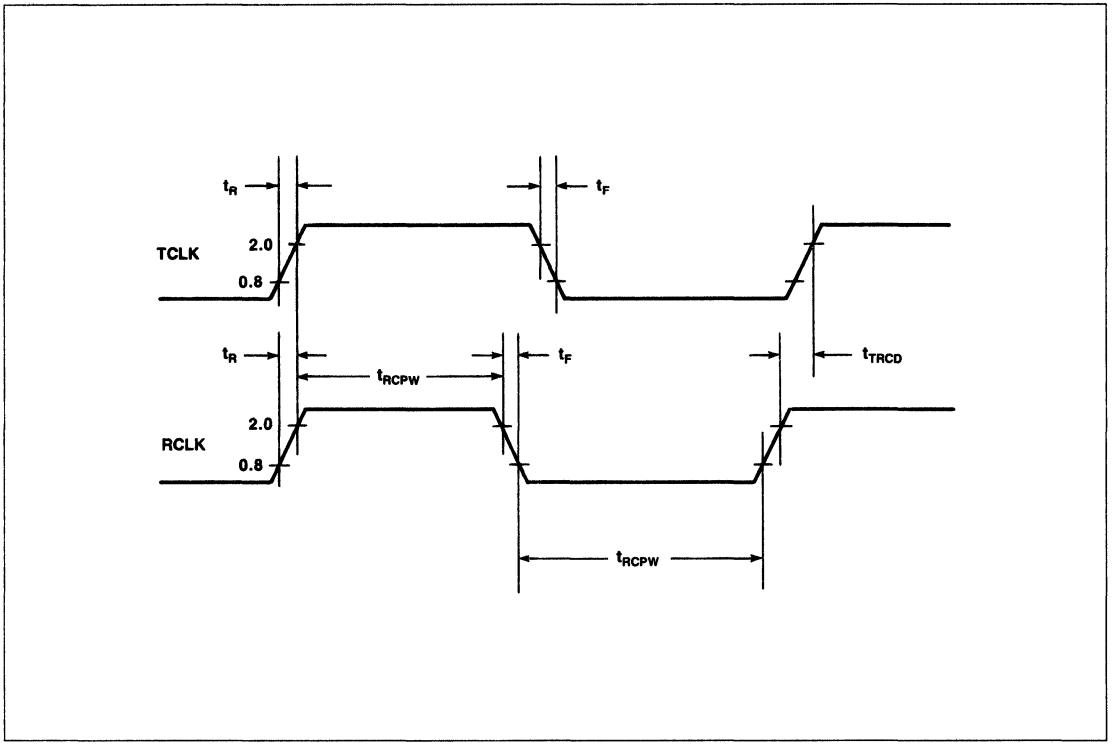
R8071 Clock Timing

Parameter	Symbol	Min.	Max.	Units
TCLK Delay	t_{TCD}	0	50	ns
SYSCLK Pulse Width	t_{SCPW}	110	—	ns
TCLK Pulse Width	t_{TCPW}	200	—	ns
SYSCLK Period	t_{SCP}	240	10,000	ns
Rise, Fall Time	t_r, t_f	—	5	ns

6

SWITCHING CHARACTERISTICS (Cont'd.)

LIU INTERFACE (Cont'd.)



R8071 TCLK — RCLK Relationship Waveforms

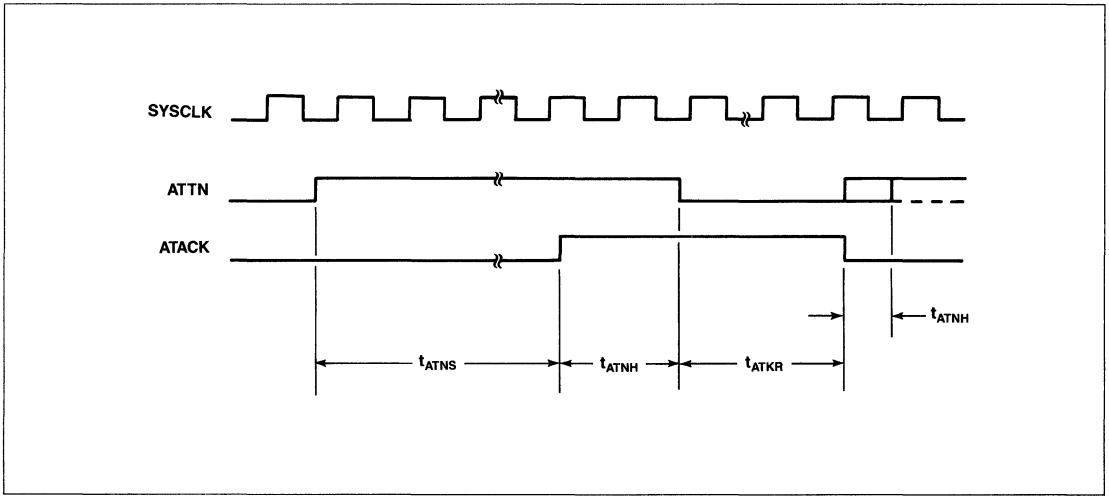
R8071 TCLK — RCLK Relationship Timing

Parameter	Symbol	Min.	Max.	Units
Rise, Fall Time	t_r, t_f	—	10	ns
RCLK Pulse Width	t_{RCPW}	190	—	ns
TCLK, RCLK Difference	t_{TRCD}	—	Note 1	ns

Note:
1. RCLK is to be centered around TCLK. The summation of RCLK and TCLK periodic differences over any duration of time must never exceed 14 TCLK periods.

SWITCHING CHARACTERISTICS (Cont'd.)

CHANNEL ACTIVATION/DEACTIVATION



Channel Activation/Deactivation Waveforms

Channel Activation/Deactivation Timing

Parameter	Symbol	Min.	Max.	Units
ATTN to ATACK Response Time	t_{ATNS}	20	48	SYSCLKS
ATTN Hold time	t_{ATNH}	0	—	ns
ATACK Reset Delay	t_{ATKR}	2	4	SYSCLKS

6

R8071 INPUT AC ELECTRICAL CHARACTERISTICS

Signal Name	Reference Signal	Edge[1]	Setup (Min.)	Hold (Min.)	Units
ATTN	SYSCLK	PE	50	50	ns
RESET	TCLK	NE	60	60	ns
D0–D7	$\overline{READ}$	NE/PE	50	0	ns
TMAX (SIS = I)	TCLK	NE	60	60	ns
TMAX (SIS = O)	TCLK	PE	60	60	ns
RSER (SIS = I)	RCLK	NE	50	50	ns
RSER (SIS = O)	RCLK	PE	50	50	ns
RRED (SIS = I)	RCLK	NE	50	50	ns
RRED (SIS = O)	RCLK	PE	50	50	ns
RSYNC (SIS = I)	RCLK	NE	50	50	ns
RSYNC (SIS = O)	RCLK	PE	50	50	ns

Notes:
1. PE = positive edge; NE = negative edge.
2. All input AC Timing measurements are referenced to the 0.8 and 2.0 Vdc logic levels

R8071 OUTPUT AC ELECTRICAL CHARACTERISTICS

Signal Name	Reference Signal	Edge[1]	Max. DELAY	Min. HOLD	Units
DMND	SYSCLK	PE	75	10	ns
$\overline{AS}$	SYSCLK	PE/NE	75	10	ns
A0–A15	SYSCLK	PE	90	10	ns
SYSACC	SYSCLK	PE	75	10	ns
$\overline{READ}$	SYSCLK	PE	75	10	ns
$\overline{WRITE}$	SYSCLK	PE/NE	75	10	ns
D0–D7	SYSCLK	NE	90	10	ns
$\overline{INTR}$	SYSCLK	NE	75	10	ns
CH0–CH4	SYSCLK	PE	140	10	ns
RX/$\overline{TX}$	SYSCLK	PE	140	10	ns
ATACK	SYSCLK	PE	75	10	ns
TSER	TCLK	NE	75	10	ns

Notes:
1. PE = positive edge; NE = negative edge.
2. All output AC Timing measurements are referenced to the 0 4 and 2 4 Vdc logic levels.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

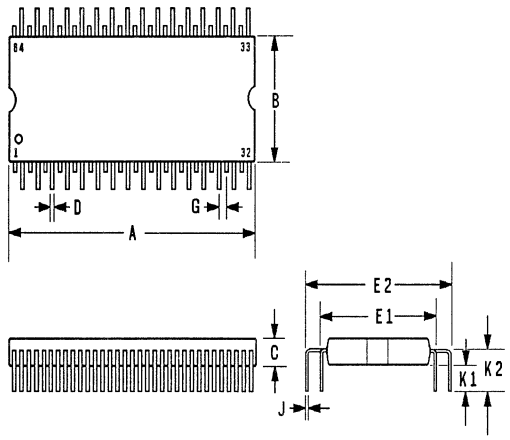
DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0 to +70°C, unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Low Voltage	V_{IL}	−0.3	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}	—	0.4	V	I_{LOAD} = +1.6 mA
Output High Voltage CMOS	V_{OH}	 3.5	 —	V	 I_{LOAD} = +100 μA
Output Low Current CH0–CH4, RX/$\overline{TX}$, TSER Others	I_{OL}	 +3.2 +1.6	 — —	mA	V_{OL} = 0.4V
Output High Current CH0–CH4, RX/$\overline{TX}$, TSER Others	I_{OH}	 −200 −100	 — —	μA	V_{OH} = 3.5V
Input Capacitance	C_{IN}	—	5	pF	
Output Capacitance (Load) TSER All Others	C_{OUT}	 — —	 100 50	 pF pF	
Power Dissipation	P_{WD}	—	250	mW	

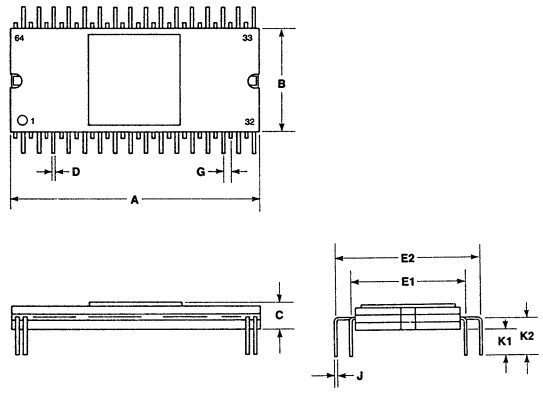
6

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	41.10	41 61	1.618	1.638
B	17.02	17.23	0.670	0.690
C	3.56	4.58	0.140	0.180
D	0.48	0.56	0 018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23 50 BSC		0.925 BSC	
G	1 27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	2 92	3.18	0.115	0.125
K2	4.83	5.34	0.190	0 210

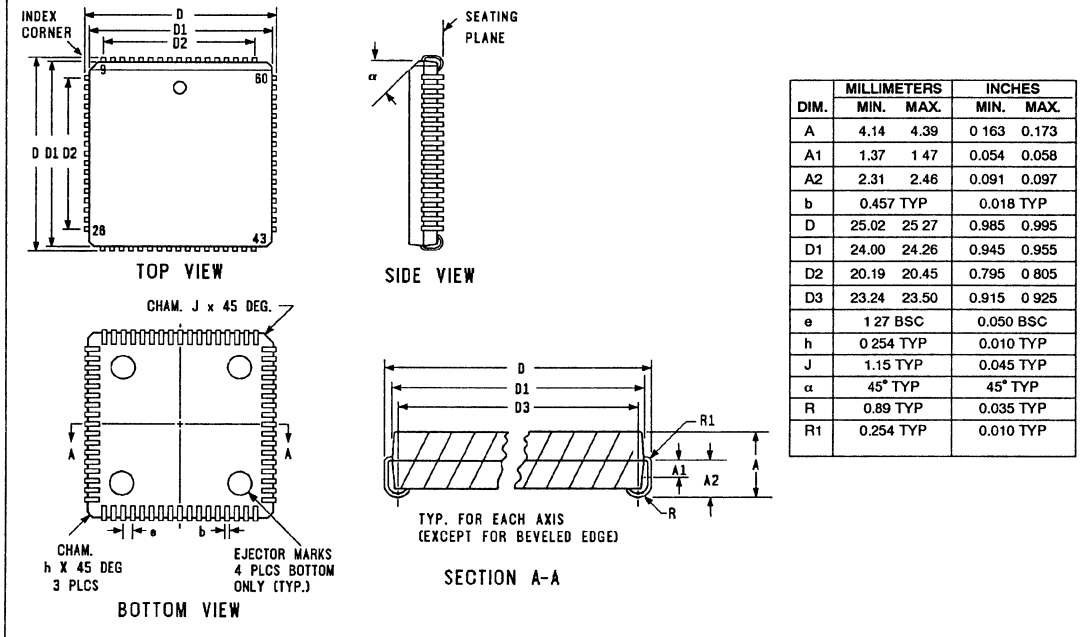
64-Pin Plastic Quad In-Line Package (QUIP)



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	40 77	41 28	1 605	1 625
B	16 76	17 27	0.660	0.680
C	3.56	4.58	0.140	0.180
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1 27 BSC		0.050 BSC	
J	0 20	0 30	0.008	0 012
K1	2 92	3.18	0.115	0.125
K2	4.83	5 34	0.190	0 210

64-Pin Cerpac Quad In-Line Package (QUIP)

PACKAGE DIMENSIONS

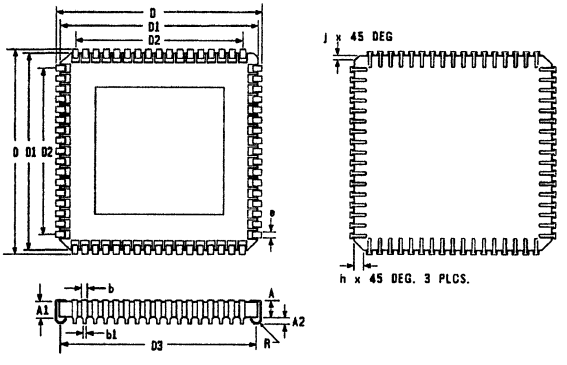


DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.14	4.39	0 163	0.173
A1	1.37	1 47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25 27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0 805
D3	23.24	23.50	0.915	0 925
e	1 27 BSC		0.050 BSC	
h	0 254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	

68-Pin Plastic Leaded Chip Carrier (PLCC)

6

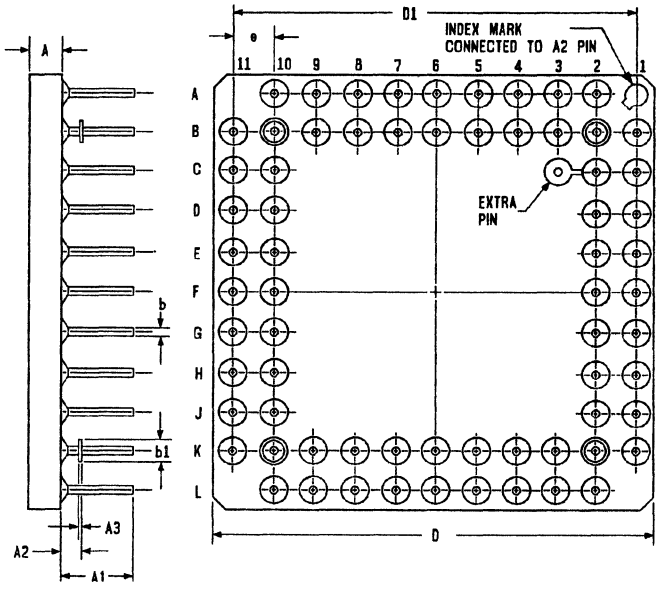
PACKAGE DIMENSIONS



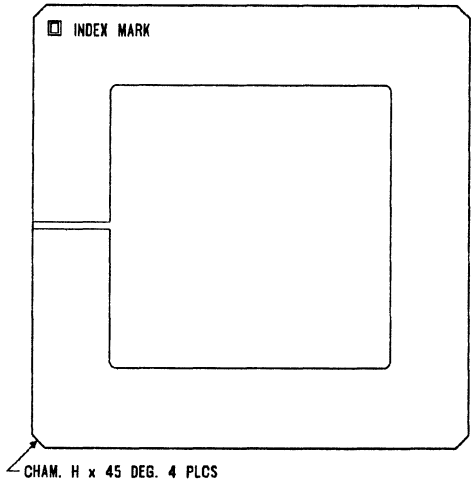
DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	1.83	2.24	0.072	0.088
A1	2.41 REF		0.095 REF	
A2	0.89 REF		0.035 REF	
D	24.64	25.65	0.970	1.010
D1	23.88	24.51	0.940	0.965
D2	23.11	24.13	0.910	0.950
D3	20.20	20.45	0.795	0.805
e	1.27 TYP		0.050 TYP	
h	1.02 REF		0.010 TYP	
J	0.51 REF		0.020 REF	

68-Pin Ceramic Leaded Chip Carrier (CLCC)

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	1.70	2.11	0.067	0.083
A1	4.45	4.70	0.175	0.185
A2	1.19	1.35	0.047	0.053
A3	0.20 REF		0.008 REF	
b	0.41	0.51	0.016	0.020
b1	1.19	1.35	0.047	0.053
D	27.58	28.19	1.086	1.110
D1	25.15	25.65	0.990	1.010
e	2.41	2.67	0.095	0.105
h	0.51 REF		0.020 REF	



68-Pin Grid Array (PGA)

Rockwell

R8075 CRC-4 Encoder/Decoder

INTRODUCTION

The Rockwell R8075 CRC-4 Encoder/Decoder is a support device to the R8070/R8070A T-1/CEPT PCM Transceiver and the R8069 Line Interface Unit. Used with the R8070 and the R8069, the R8075 implements transmit and receive functions in accordance with CCITT Recommendation G.704 for PCM30 using CRC-4. Operation of the R8075 is entirely transparent other than error detection/reporting and handling of the Spare Bits. The R8075 can be set in either enable or disable mode, for systems which handle both data encoded with CRC-4 and without CRC-4.

Transmit functions compute the CRC-4 polynomial and insert the proper alignment timing and Spare Bits (SP1, SP2) into the transmit data stream. HDB3 encoding is also handled by the R8075.

Receive functions are independent error detection of CRC-4 and multiframe alignment, extraction of the spare bits, and HDB3 decoding (including reporting of bipolar violations).

The Bit, Channel and Frame timing signals are available to the system for both the transmit and receive sections. The R8075 can support ISDN applications using the R8070 256N mode and PCM30 signalling modes using the 256S mode.

FEATURES

- CRC-4 transmit and receive as per CCITT Recommendation G.704
- Insertion and extraction of Spare Bits (SP1 and SP2)
- Independent error detection and reporting of CRC-4 and multiframe alignment errors
- CRC-4 enable/disable capability
- Enhanced HDB3 encode/decode section, includes reporting of bipolar violations
- Read/Write access to International Bits in CRC-4 disable mode (through R8070)
- Supports 256N and 256S modes
- Bit, Channel and Frame timing available to system
- Low power CMOS technology
- Operates from single +5V supply
- Package Options
  - 24-pin plastic DIP
  - 24-pin CERDIP
  - 28-pin PLCC

ORDERING INFORMATION

Part Number:
R8075

- Temperature
  - Blank = 0°C to 70°C
  - E = –40°C to +85°C
- Package
  - P = 24-pin DIP
  - S = 24-pin CERDIP
  - J = 28-pin PLCC

INTERFACE SIGNALS DESCRIPTION

The R8075 interfaces to the R8070 T1/CEPT PCM Transceiver, the R8069 Line Interface Unit, and to the system. The functional interface is shown in Figure 1. Figure 2 shows the signals grouped by interface. The R8075 interface signals are listed by pin number in Figure 3 and shown graphically in Figure 4.

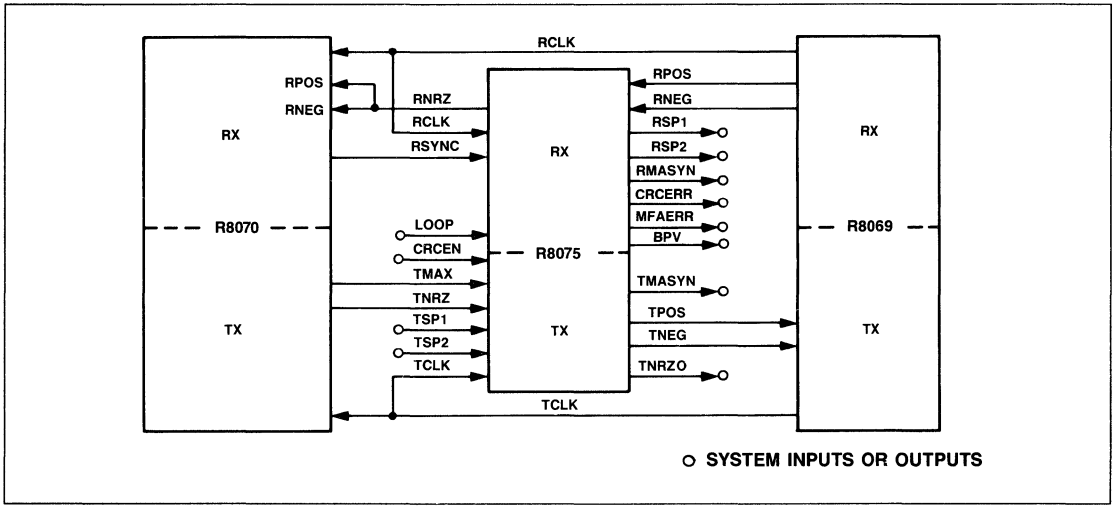


Figure 1. R8075 Functional Interface

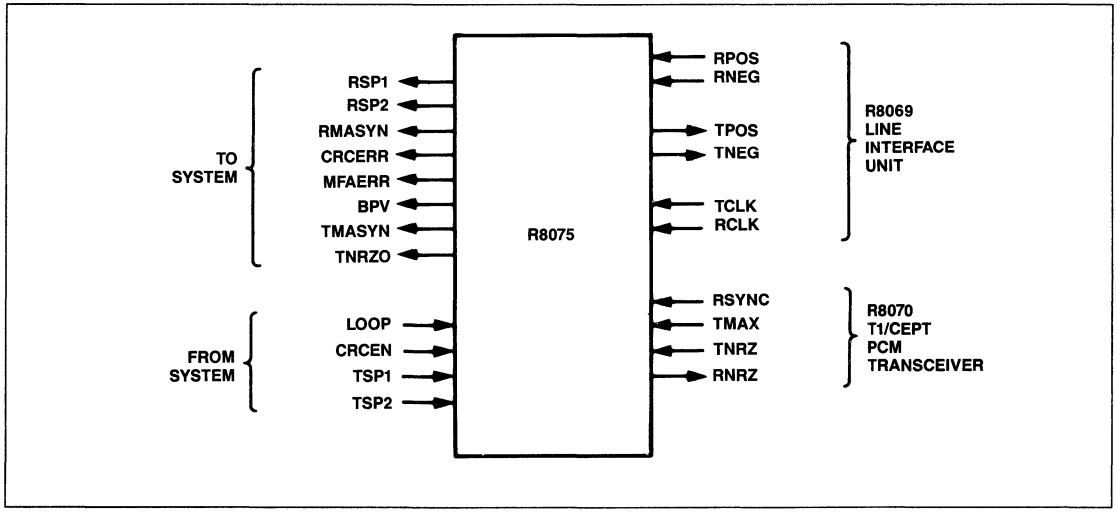


Figure 2. R8075 Interface Signals

Table 1. R8075 Pin Assignments

Symbol	24-Pin DIP	28-Pin PLCC	Signal Name	I/O	Source/ Destination
LOOP	1	1	Loopback Mode	I	System
TNEG	2	2	Transmit Unipolar Negative	O	R8069
TPOS	3	3	Transmit Unipolar Positive	O	R8069
N.C.	–	4	No Connect		
TNRZ	4	5	Transmit NRZ Data (IN)	I	R8070
TNRZO	5	6	Transmit NRZ Data (OUT)	O	System
BPV	6	7	Bipolar Violation	O	System
VDD	7	8	+5 VDC Power	–	Power Supply
CRCERR	8	9	CRC-4 Error	O	System
RSP2	9	10	Receive Spare Bit 2	O	System
N.C.	–	11	No Connect		
RSYNC	10	12	Receive Sync	I	R8070
CRCEN	11	13	CRC-4 Enable	I	System
RNRZ	12	14	Receive NRZ Data	O	R8070
RCLK	13	15	Recovered (Receive) Clock	I	R8069
RPOS	14	16	Receive Unipolar Positive	I	R8069
RNEG	15	17	Receive Unipolar Negative	I	R8069
N.C.	–	18	No Connect		
MFAERR	16	19	Multiframe Alignment Error	O	System
TSP1	17	20	Transmit Spare Bit 1	I	System
TSP2	18	21	Transmit Spare Bit 2	I	System
VSS	19	22	Ground	–	Ground
TCLK	20	23	Transmit Clock	I	R8069
TMAX	21	24	Transmit Maximum	I	R8070
N.C.	–	25	No Connect		
RSP1	22	26	Receive Spare Bit 2	O	System
RMASYN	23	27	Receive MF Alignment Sync	O	System
TMASYN	24	28	Transmit MF Alignment Sync	O	System

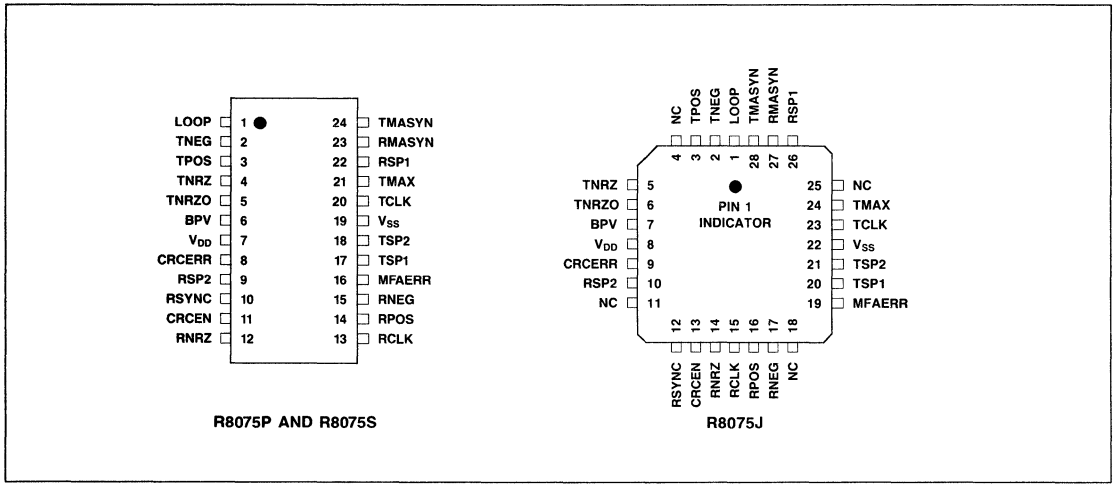


Figure 3. R8075 Pin Assignments

Table 2. R8075 Interface Signal Definitions

Mnemonic	DIP Pin No.	PLCC Pin No.	Name/Description
INPUTS FROM R8069 (LINE INTERFACE UNIT)			
RCLK	13	15	**Recovered (Receive) Clock.** From R8069 Output Pin 27. RCLK is the recovered clock output which is locked to the frequency and phase of the incoming data. RPOS and RNEG are clocked out of the R8069 at the falling edge of RCLK in the elastic store bypass mode (CB high). This signal is also input to the R8070 as the receiver clock input, pin 56 of the QUIP (pin 59 of the PLCC).
TCLK	20	23	**Transmit Clock.** From R8069 Output Pin 28. Transmitter clock output which is either the smoothed clock provided through EXCLK (EXternal CLocK Reference, R8069 pin 3) or the smoothed clock extracted from the input data. The receive data is also clocked out on the falling edge of TCLK, except in elastic store bypass mode (CB high). This signal is also input to the R8070 as the transmitter clock input, pin 9 (QUIP) / pin 10 (PLCC).
RPOS RNEG	14 15	16 17	**Receive Unipolar Positive, Negative.** From R8069 Output Pins 16, 17. RPOS and RNEG are the outputs of the received data recovered from RXINP and RXINN AMI line pulses. RPOS and RNEG have TTL levels and are in NRZ format. These are directly connected to the R8075. RPOS and RNEG are clocked out of the R8069 at the falling edge of RCLK (elastic store bypass mode or TCLK in (elastic store enable mode), and clocked into the R8075 at the rising edge of RCLK.
INPUTS FROM R8070 (PCM30 TRANCEIVER)			
RSYNC	10	12	**Receive Sync.** From R8070 Output Pin 37 (QUIP)/Pin 39 (PLCC). While the receiver is synchronized, RSYNC is high during the first bit of each multiframe.
TMAX	21	24	**Transmit Maximum.** From R8070 Output Pin 10 (QUIP)/Pin 11 (PLCC). TMAX is high for one bit time per multiframe coincident with the sampling of the next to last serial bit of a multiframe.
TNRZ	4	5	**Transmit NRZ Data.** From R8070 Output Pin 19 (QUIP)/Pin 20 (PLCC). NRZ (Non-Return-to-Zero) output for transmitted data. This output is unaffected by LOOP or by HDB3 zero-suppression coding. There is an 8-bit throughput delay between the TSER input and the TNRZ output.
INPUTS FROM THE SYSTEM			
CRCEN	11	13	**CRC-4 Enable.** Control input which enables the R8075 when CRCEN is high. When CRCEN is low, the R8075 is disabled, providing full transparent operation; in this mode, the user has control of the international bits through the TIBITS. The R8075 receiver functions always operate; only the transmit functions are disabled when CRCEN is low.
LOOP	1	1	**Loopback Mode.** Control input placing the R8070 plus R8075 in loopback mode. In this mode, TPOS and TNEG are routed internally to RPOS, RNEG (respectively). This function is identical to the equivalent function of the R8070. It replaces the R8070 loopback function. CRCEN does not affect this function.
TSP1 TSP2	17 18	20 21	**Transmit Spare Bits 1, 2.** Input to R8075 which allows insertion of the spare international bits. When the R8075 is enabled, the user may update the TSP1, TSP2 inputs at the occurrence of TMASYN (R8075 output). These bits are reserved for future international applications, and for now, they should be fixed at 1 on digital paths crossing international borders. If CRCEN is low (R8075 disabled), the user may access the international bit through the IA pin (TIBIT) on the R8070, pin 5 (QUIP and PLCC).
OUTPUTS TO R8069 (LINE INTERFACE UNIT)			
TPOS TNEG	3 2	3 2	**Transmit Unipolar Positive, Unipolar Negative R8069 Input Pins 13,14.** TPOS and TNEG are the "unipolar paired" input for transmitted data. They must have TTL levels and be in NRZ format. These outputs from the R8075 replace those which would ordinarily come from the R8070. They are clocked in at the falling edge of TCLK. The state TPOS, TNEG = 1 is not valid, all other combinations are valid. The R8075 never generates the invalid combination.

Table 2. R8075 Interface Signal Definitions (Cont'd)

Mnemonic	DIP Pin No.	PLCC Pin No.	Name/Description
OUTPUTS TO R8070 (PCM30 TRANSCEIVER)			
RNRZ	12	14	**Receive NRZ Data.** R8070 Input Pins 54, 55 (QUIP) / pins 57, 58 (PLCC) This lead is connected to both the RNEG and RPOS pins of the R8070. It must remain stable for 60 ns before and after the rising edge of RCLK. When connected in this manner, the HDB3 encoder and decoder along with the Bipolar Violation Detector in the R8070 are disabled. These functions are supplied by the R8075.
OUTPUTS TO THE SYSTEM			
CRCERR	8	9	**CRC-4 Error.** At the end of every SMF (sub-multiframe, 8 frames each), the current frame CRC result is clocked into a temporary holding register. During the following SMF, the incoming CRC bits on RSER are compared with the contents of the holding register. If a mismatch occurs, the CRC-4 error signal, CRCERR, is generated. This condition can result from a loss of frame alignment or by an incidental data error. This signal is valid after the falling edge of the second RCLK in the SMF and remains valid for the entire SMF, resetting at the end of the SMF.
MFAERR	16	19	**Multiframe Alignment Error.** The Multiframe Alignment Error signal is generated when there is a miss in the CRC-4 alignment bits (sequence of ...001011...). It indicates each instance of multiframe alignment and is valid during each MF. It is reset when the CRC-4 alignment is regained. This signal can be used by the system to improve the frame alarm handling.
TNRZO	5	6	**Transmit NRZ Data.** Serial transmit NRZ data. Derived by the R8075 (from the TNRZ input to the R8075 from the R8070, it is regenerated, aligned with the timebase of the TPOS/TNEG outputs of the R8075.
RMASYN	23	27	**CRC-4 Receive Multiframe Alignment Sync.** Derived signal generated by the R8075 indicating the beginning of the received CRC-4 multiframe. It is a positive pulse of one RCLK in duration.
TMASYN	24	28	**CRC-4 Transmit Multiframe Alignment Sync.** This signal indicates the beginning of the transmitted CRC-4 multiframe. It is a positive pulse of one TCLK period in duration.
BPV	6	7	**Bipolar Violation.** This signal indicates that a Bipolar Violation has occurred. It replaces the equivalent signal RVLL from the R8070, which indicates a Bipolar Violation.
RSP1 RSP2	22 9	26 10	**Receive Spare International Bits.** The receive logic extracts these spare international bits and makes them available to the system at the beginning of each multiframe (RMASYN).
POWER AND GROUND			
V_{DD}	7	8	**Power.** + 5V DC power.
V_{SS}	19	22	**Ground.** Power and signal ground.
NC		4, 11 18, 25	**No Connect.** These are pins on the PLCC which are not to be connected.

FUNCTIONAL DESCRIPTION

The R8075 is used with the R8070 Transceiver and the R8069 Line Interface Unit to provide CRC-4 capability for PCM30 systems. There are two basic sections to the R8075: the Transmit section and the Receive section.

Signals connected to either the R8069 or R8070 are described in the pin definitions (Table 2). For more information, please refer to the functional and interface descriptions of the data sheets for the R8069 and R8070.

TRANSMIT SECTION

The transmit section computes the CRC-4 polynomial, inserts alignment timing signals and spare bits into the transmit data stream, and encodes the bipolar transmit data using HDB3.

The six R8075 transmit section inputs are from the system (TSP1, TSP2, CRCEN), from the R8069 (TCLK), and from the R8070 (TNRZ). The four R8075 transmit section outputs go to the system (TNRZO and TMASYN) and to the R8069 (TPOS and TNEG).

The R8075 transmit section is divided into four blocks:

1. Transmit Logic
2. CRC-4 Encoder
3. HDB3 Encoder
4. Transmit Bit/Frame/Multiframe Control (Transmit Timing Control)

TRANSMIT LOGIC

The Transmit Logic section provides the TNRZO (Transmit NRZ Data) output to the system. This signal has the CRC-4 bits and the Spare Bits inserted at the proper time, as appropriate.

Data inputs to the Transmit Logic section are the NRZ (Non Return-to-Zero) output for transmitted data from the R8070 (TNRZ) and the Transmit Spare Bits from the system (TSP1, TSP2). When the CRC-4 encoder is enabled (CRCEN = HIGH) the CRC-4 Encoder section provides CRC-4 data to the Transmit Logic section for insertion into the transmitted bit stream. When CRCEN = LOW, CRC-4 is not being implemented, and access to the international bit for each frame is provided through the R8070/70A. In this case, the R8075 passes the international bit transparently.

Control and timing inputs to the Transmit Logic are provided by the Transmit Bit/ Frame/Multiframe Control (Transmit Timing Control) to determine the proper insertion points for the CRC-4 bits if CRCEN is HIGH. The Transmit Timing Control also properly times insertion of the Spare Bits. If CRCEN is LOW, there will be no insertion of CRC-4 bits into the transmitted bit stream, and the Spare Bits are accessed through the R8070 instead of through the R8075. In this condition, the CRC-4 is not implemented.

The output of the Transmit Logic section to the system is TNRZO, the Transmit NRZ Data which has been CRC-4 encoded and has Spare Bits inserted at the proper time (if CRCEN is HIGH). This is a regenerated signal derived from the TNRZ signal from the R8070, which is unchanged if CRCEN is LOW. This signal, regardless of whether the R8075 is enabled or disabled is used to replace the R8070 TNRZ signal as an output to the system. TNRZO also is an input to the HDB3 Encoder, which generates the Transmit Bipolar Data, TPOS and TNEG.

CRC-4 ENCODER

This section calculates the CRC-4 polynomial and provides the CRC-4 bits for insertion into the transmitted bit stream. This insertion is performed at the proper time by the Transmit Logic (see above). The CRC-4 Encoder may be disabled for transparent operation without CRC-4 computation by CRCEN set LOW.

The data inputs to the CRC-4 Encoder section is the TNRZ (Non Return-to-Zero) output for transmitted data from the R8070. The R8069 provides TCLK (Transmit Clock) to the CRC-4 Encoder section as a timing input. Control and timing inputs to the CRC-4 Encoder are also provided by the Transmit Bit/Frame/ Multiframe Control (Transmit Timing Control) to determine the proper insertion points for the CRC-4 bits if CRCEN is HIGH. This information is generated using TMAX (from R8070) to derive multiframe timing and CRCEN (from system) to decide whether to compute CRC-4.

The output of the CRC-4 Encoder section goes through a holding register into the Transmit Logic for insertion of the CRC-4 bits (if CRCEN is HIGH) into the Transmit bit stream.

HDB3 ENCODER

This section takes the Transmit NRZ data provided by the Transmit Logic and provides HDB3 encoding. The resulting output is the two unipolar signals TPOS and TNEG which go to the R8069 for transmission onto the PCM-30 line.

Data input to the HDB3 Encoder is the TNRZO output of the Transmit Logic section of the R8075. This signal already has CRC-4 and Spare Bits inserted as appropriate. The TNRZO data is converted to a set of bipolar signals (TPOS, TNEG) using HDB3 encoding for bipolar PCM-30 data. The TCLK input to the HDB3 Encoder comes directly from the R8069.

The output of the HDB3 Encoder section is the set of Unipolar Transmit signals, TPOS and TNEG. These signals go directly to the R8069 for transmission onto the

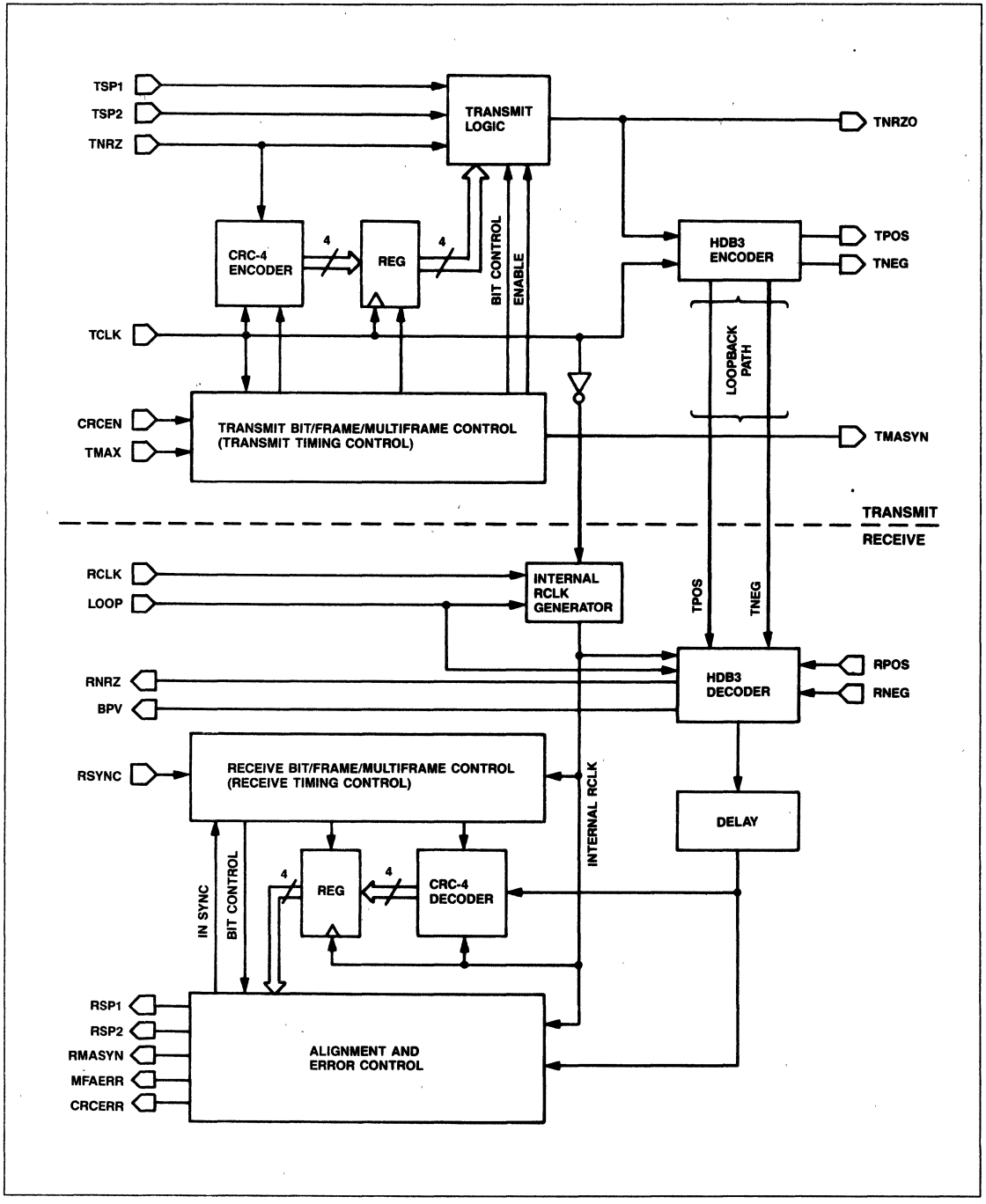


Figure 4. R8075 Functional Block Diagram

PCM-30 line. These signals also are provided to the HDB3 decoder section.

Transmit Bit/Frame/Multiframe Control (Transmit Timing Control)

Transmit timing is provided by this section to properly handle insertion of the CRC-4 bits and the Spare Bits into the outgoing transmit bit stream. This section provides timing and control to the CRC-4 Encoder and Transmit Logic sections. It also provides the Transmit Multiframe Alignment Sync signal to the system, so the system can align properly on multiframe boundaries.

Inputs to this section are TCLK (from R8069), TMAX (from R8070) and CRCEN (from system). If CRCEN is high, the control is provided to the Transmit Logic to implant the CRC-4 and Spare Bits into the transmit bit stream. TCLK is used to derive the bit timing; TMAX is used to derive the frame and multiframe timing.

The CRC-4 bits are inserted in the even frames, in the bit 1 position of these frames. There are four CRC-4 bits in each 8-frame Sub-MultiFrame (SMF). In odd frames, bit 1 of the first six frames of each 16-frame MultiFrame (MF) contains the CRC multiframe alignment signal (001011). Bit 1 of the last two odd frames of the multiframe (frame 13, 15) contain the Spare Bits. Access to the International Bit (bit 1 of each frame) is provided through the R8070 when the R8075 is in CRC-4 disable mode.

Outputs from this section are the timing and controls described above, and the Transmit Multiframe Alignment Sync (TMASYN) signal. TMASYN is an output to the system which indicates the beginning of the transmitted CRC-4 multiframe. It is a positive pulse of one TCLK period in duration.

RECEIVE SECTION

The receive section provides independent error detection/reporting of the CRC-4 and Multiframe Alignment errors, extraction of the Spare Bits, and HDB3 decoding with reporting of bipolar violations. The R8075 receive section also provides RNRZ (Receive NRZ Data) to the R8070, connected to the R8070 RPOS, RNEG inputs. This connection will bypass the HDB3 encoder and decoder sections of the R8070, along with the R8070 bipolar violations detector. These functions are supplied by the Transmit and Receive sections of the R8075.

The four inputs to the R8075 receive section are: RPOS and RNEG (unipolar receive data) from the R8069, RSYNC (receive sync) from the R8070, and LOOP (Loopback Mode) from the system.

The seven outputs from the R8075 receive section are: RNRZ (receive NRZ data) to the R8070, and the R8075 outputs to the system. These are: CRCERR (CRC-4 Error), MFAERR (Multiframe Alignment Error), RMASYN (Receive Multiframe Alignment Sync), BPV (Bipolar Violation), RSP1 and RSP2 (Receive Spare Bits).

The receive section has the following functional blocks:

1. Internal RCLK Regenerator
2. HDB3 Decoder
3. CRC-4 Decoder
4. Alignment and Error Control
5. Receive Bit/Frame/Multiframe Control (Receive Timing Control)

Internal RCLK Generator

This section takes the RLCK and TCLK from the R8069, along with the LOOP control from the system and produces the internal RCLK timing. This RCLK provides master bit timing for the other blocks of the receive section of the R8075.

HDB3 Decoder

This section takes the RPOS and RNEG from the R8069 and generates the RNRZ output to the R8070 and identifies bipolar violations (BPV) for output to the system.

Inputs to this section are the RPOS and RNEG (from R8069), TPOS and TNEG (from R8075 HDB3 encoder block), the LOOP control (from system), and the internal RCLK (from internal RCLK). Using the LOOP and TPOS/TNEG signals, if the loopback mode is enabled (LOOP = HIGH), the TPOS and TNEG signals generated in the R8075 HDB3 encoder are routed to the RPOS/RNEG inputs of the HDB3 decoder. This function is identical to and replaces the equivalent R8070 function.

HDB3 Decoder (continued)

Outputs from this section are RNRZ (to the R8070) and BPV (to system). The RNRZ is generated according to the HDB3 format, and sent to the R8070 RPOS/RNEG inputs, bypassing the R8070's HDB3 encode and decode functions. According to the HDB3 algorithm, bipolar violations are detected and reported through the BPV (system output). After HDB3 decoding of the receive data, it is also passed to the CRC-4 Decoder and the Alignment/Error Control blocks. Note that tying RPOS and RNEG together will bypass the HDB3 decode section. This function is identical in the R8070 and R8075, bypassing the respective HDB3 decode logic in each device used in this manner.

CRC-4 Decoder

The RNRZ output of the HDB3 decoder section, the internal RCLK, and the RSYNC timing are inputs to the CRC-4 decoder. At the end of every SMF, the current frame CRC-4 result computed by the CRC-4 decoder block is clocked into a temporary holding register. During the following SMF, the incoming CRC-4 bits on RSER are compared with the contents of the holding register. If a mismatch occurs, the CRC-4 error signal (CRCERR) is generated in the Alignment/Error control block. Timing is generated by the receive bit/frame/MF control block.

Alignment/Error Control

This block generates the receive multiframe alignment sync signal output to the system (RMASYN), outputs the Receive Spare Bits (RSP1, RSP2), and generates the error signals MFAERR (Multiframe Alignment Error) and CRCERR (CRC-4 error) output to the system.

Handling of the errors is a system function to be done in accordance with CCITT Standard G70X and Recommendation I.431.

Inputs to the Alignment/Error Control block are the internally generated RCLK, the RNRZ data from the HDB3 decoder block, the contents of the CRC-4 holding register, and timing signals from the Receive Bit/Frame/MF control block.

While the CRCERR and MFAERR are closely related, they are independently generated. CRCERR is generated upon a mismatch between the incoming CRC bits from RSER and the previous SMF's CRC result from the previous SMF, found in the holding register. This can occur due to an incidental data error or by a loss of frame alignment. This signal is valid for the entire SMF, resetting at the end of each SMF. MFAERR is generated when there is a miss in the CRC-4 alignment bits, indicating each instance of multiframe alignment error. It is valid during each MF, and is reset when the CRC-4 alignment is regained. This signal is useful to the system for implementing alarm handling.

Alignment/Error Control (continued)

RMASYN is derived from the RCLK. It is a positive pulse of one RCLK period in length, and indicates the beginning of the received CRC-4 multiframe. This section also extracts the Spare Bits (RSP1 and RSP2), making them available to the system at the beginning of each multiframe (at RMASYN).

Receive Bit/Frame/MF Control (Receive Timing Control)

This section takes RSYNC from the R8070, the internally generated RCLK, and a sync valid signal generated by the Alignment/Error control block to generate timing for the CRC-4 Decoder and the bit timing for the Alignment/Error control blocks. This block generates internal timing. It has no off-chip outputs.

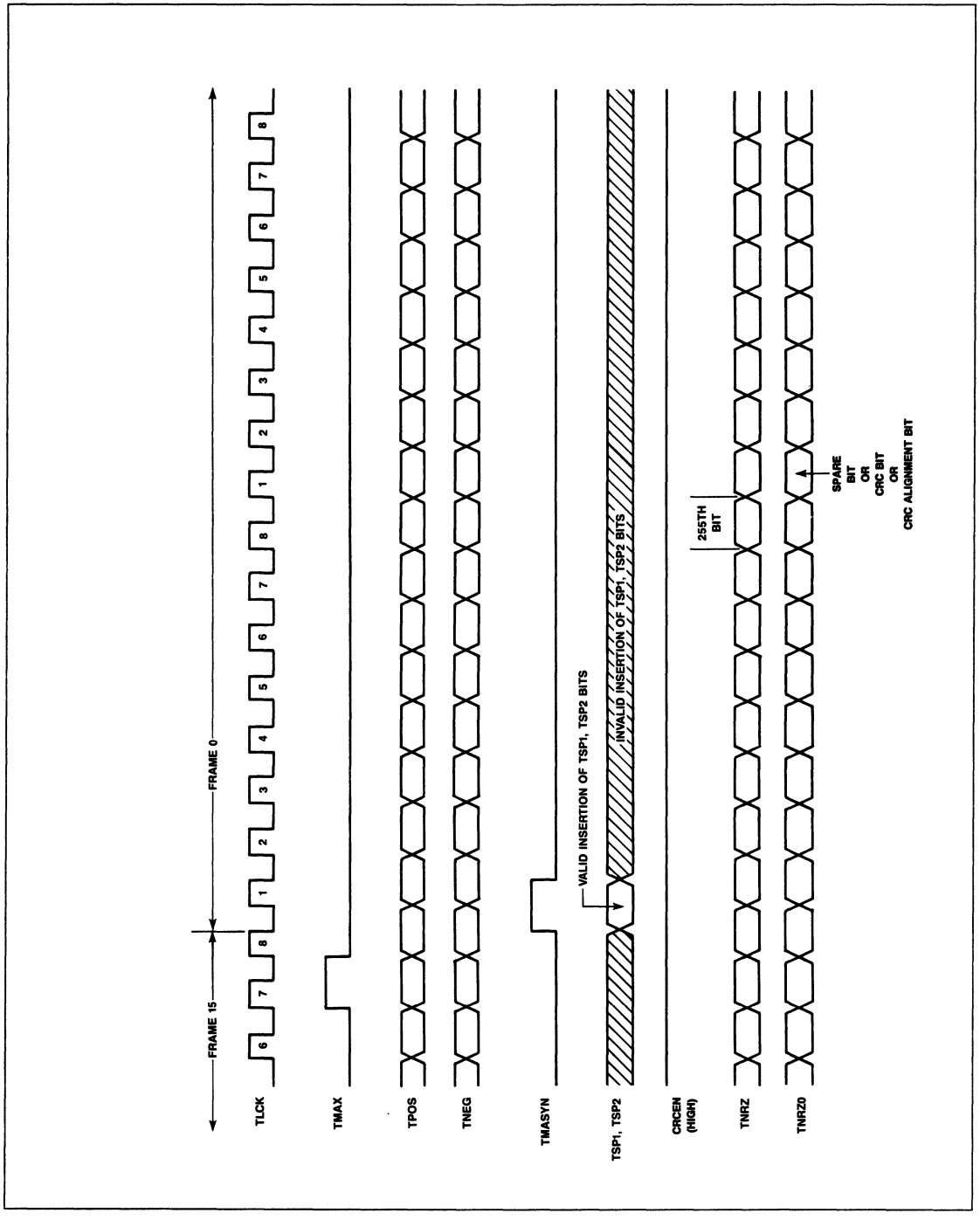


Figure 5. R8075 Transmit Timing

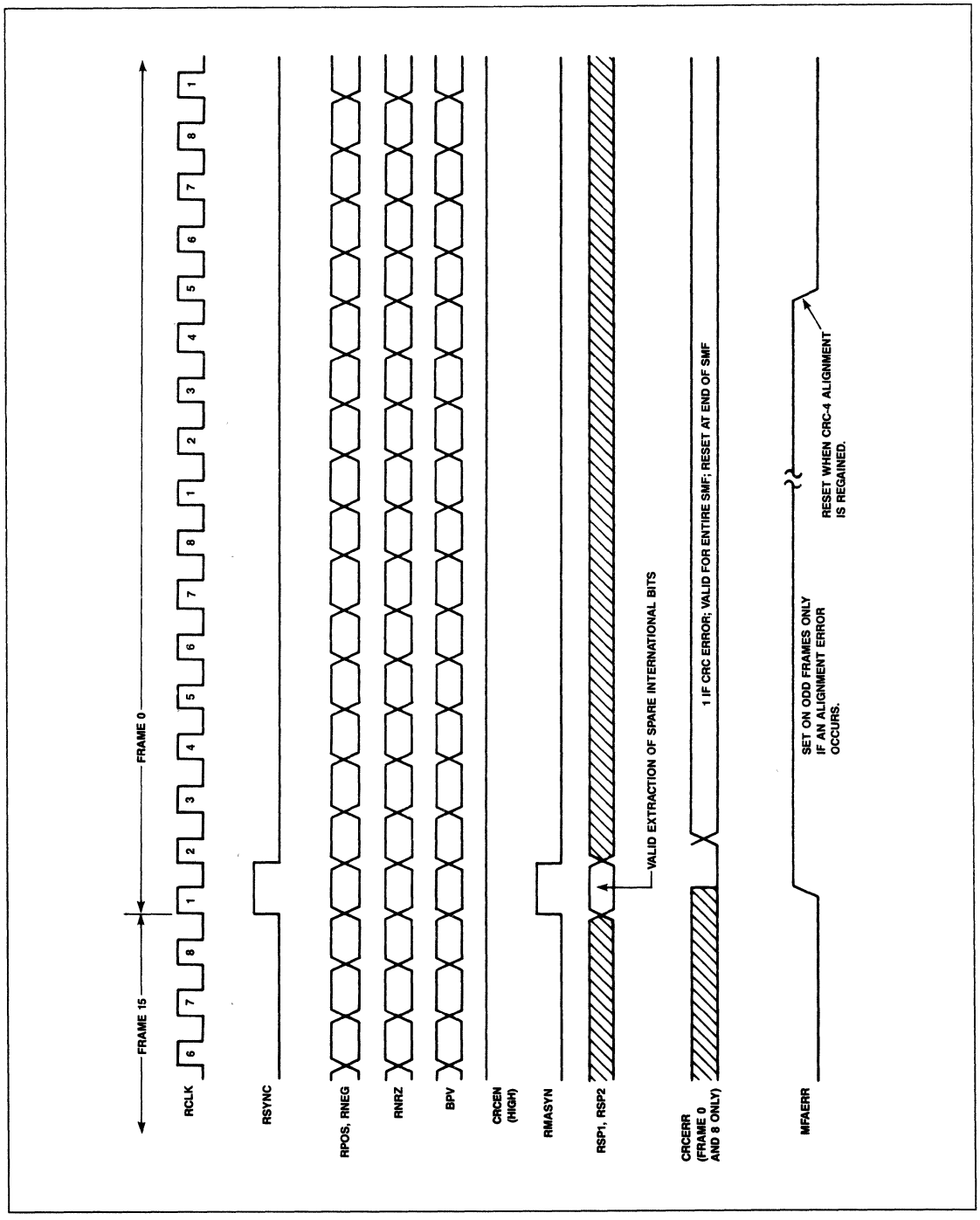


Figure 6. R8075 Receive Timing

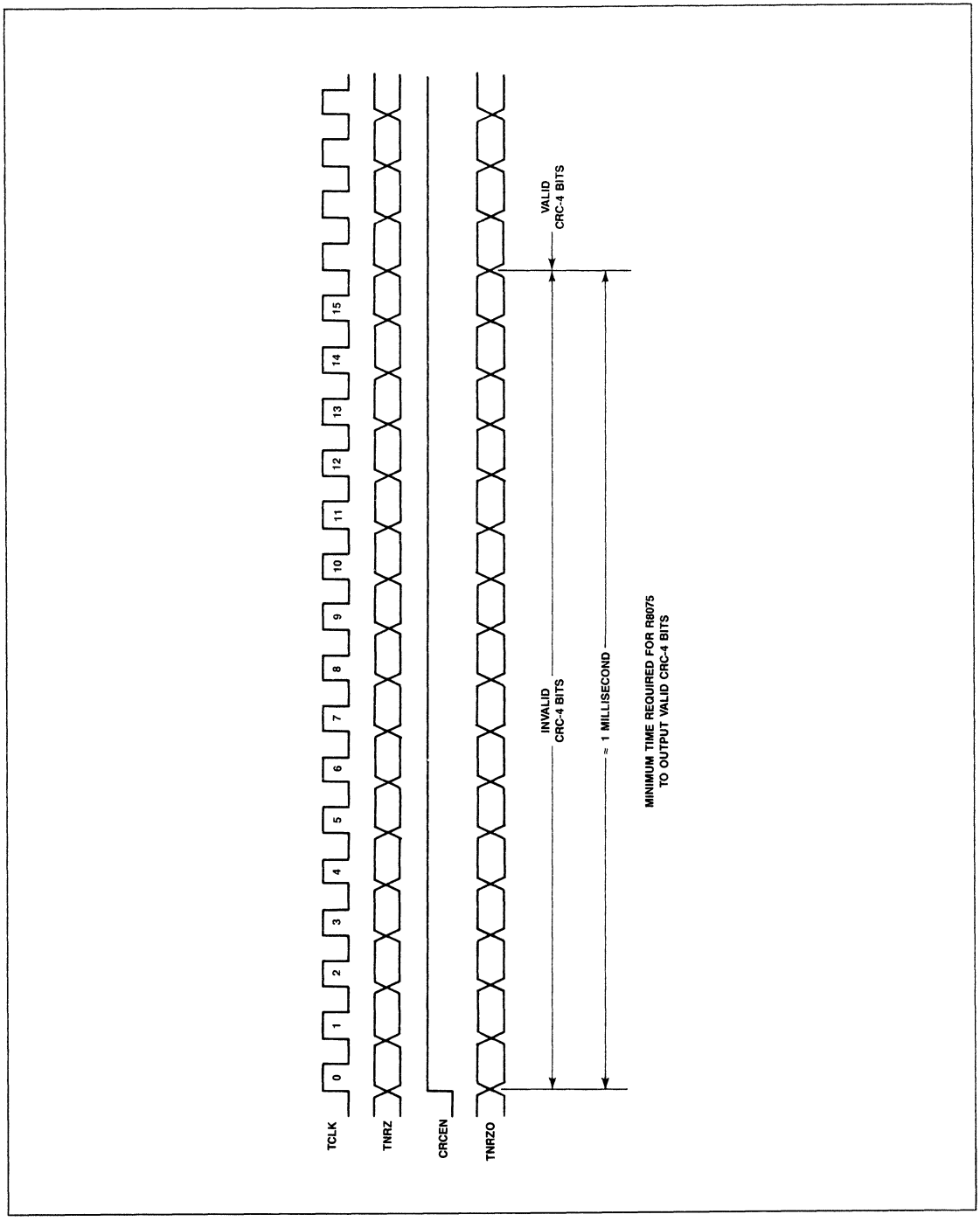


Figure 7. CRC-4 Output Timing

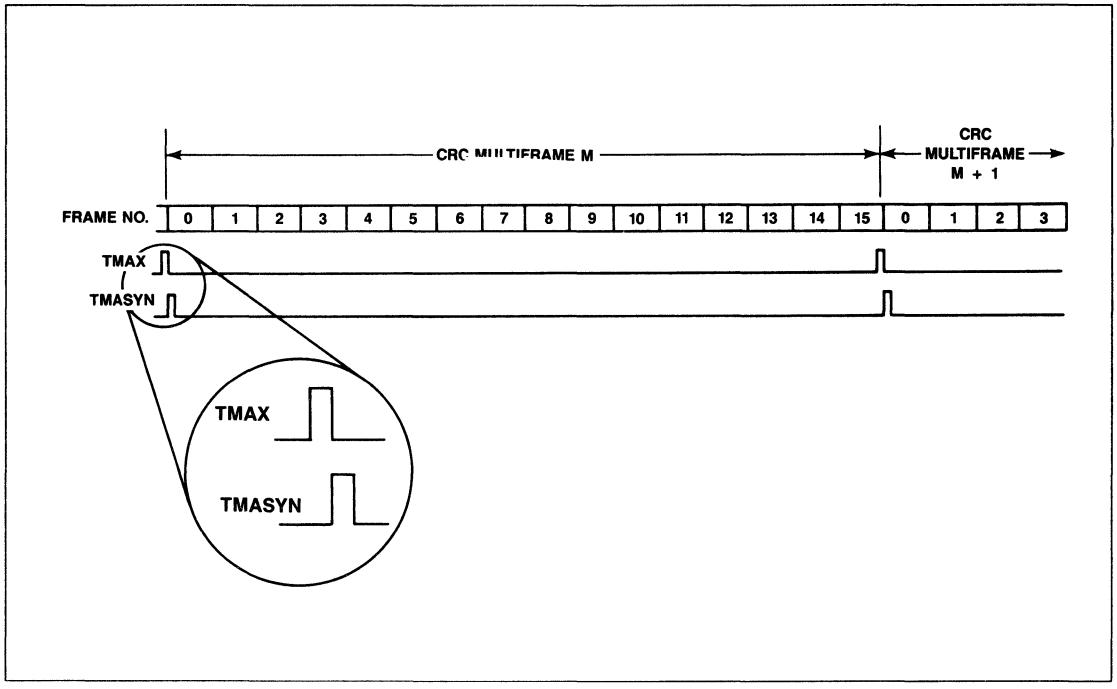


Figure 8. Transmit CRC Multiframe - R8070 Mode 256S

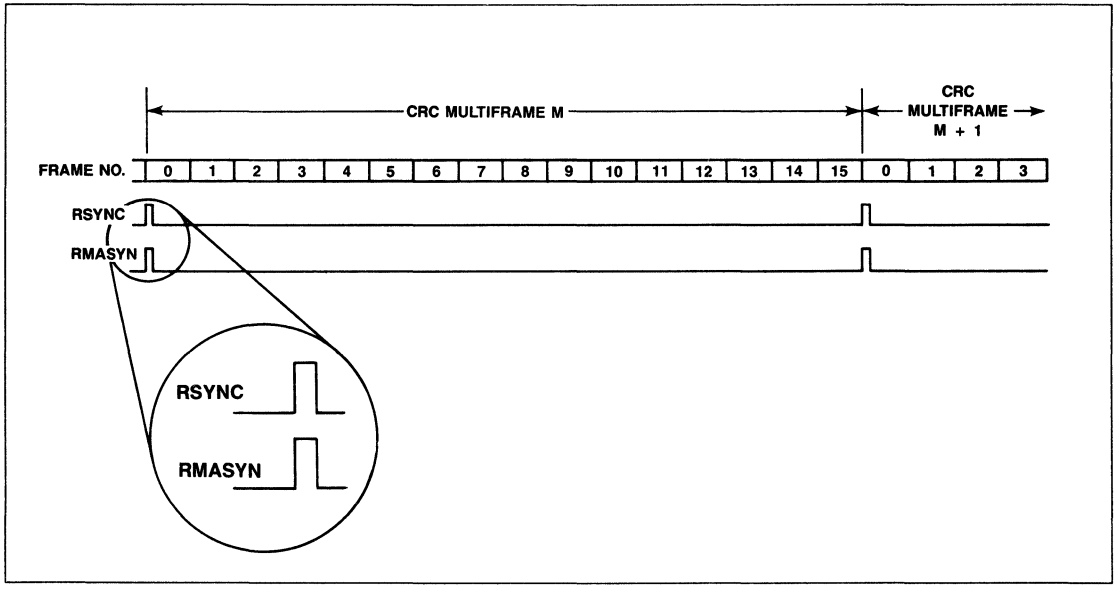


Figure 9. Receive CRC Multiframe - R8070 Mode 256S

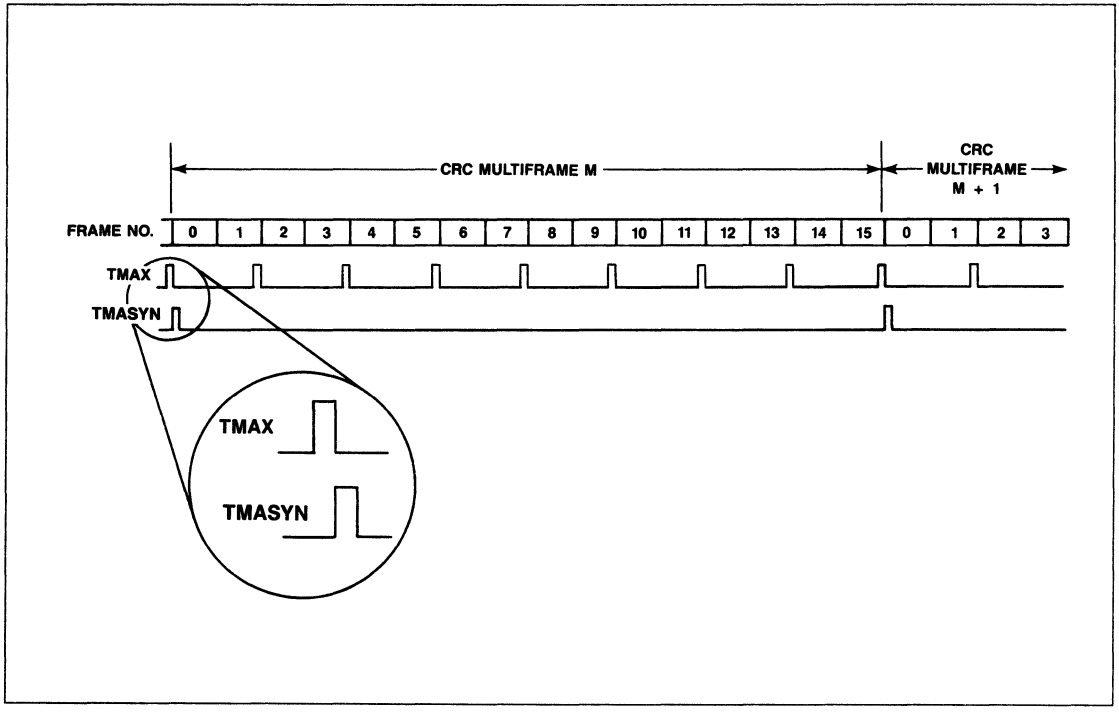


Figure 10. Transmit CRC Multiframe - R8070 Mode 256N

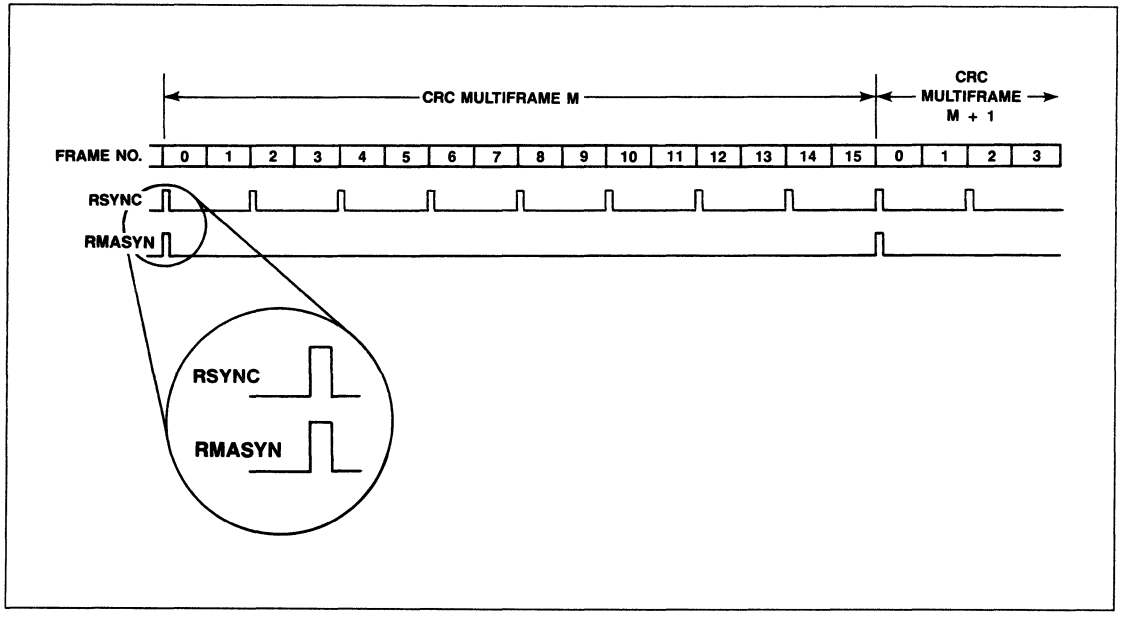


Figure 11. Receive CRC Multiframe - R8070 Mode 256N

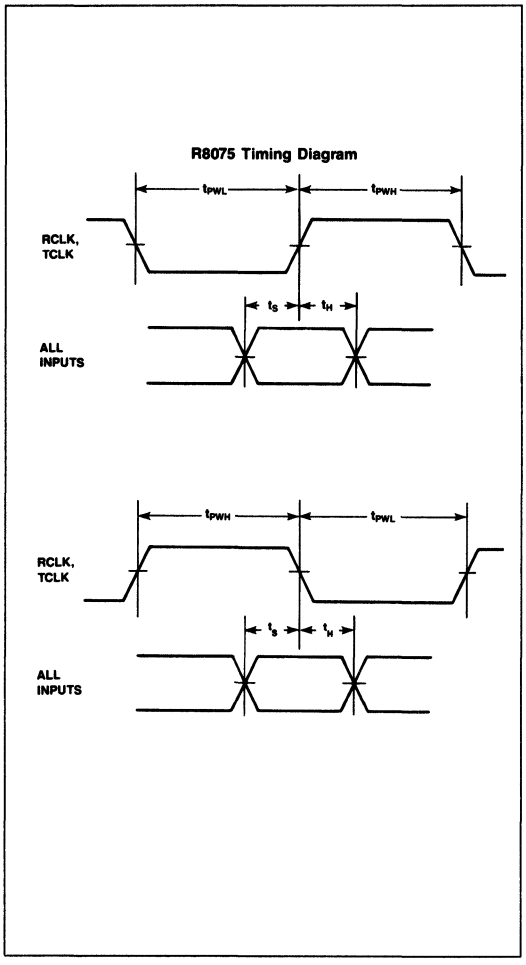


Figure 12. Input Timing

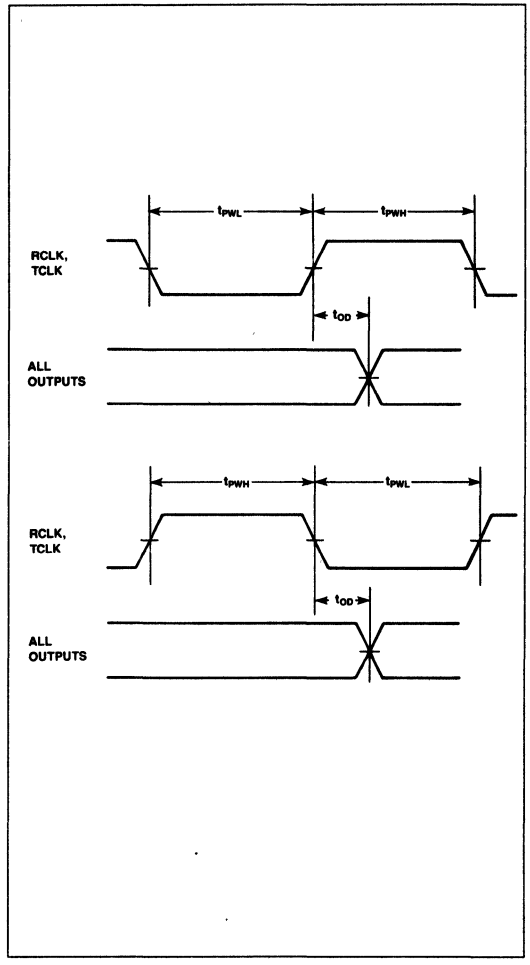


Figure 13. Output Timing

Table 3. Input and Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock Pulse Width High, Low	t_{PWH}, t_{PWL}	244	–	–	ns
Input Setup Time	t_S	60	–	–	ns
Input Hold Time	t_H	60	–	–	ns
Output Delay Time	t_{OD}	–	–	60	ns

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	–0.3 to +7.0	Vdc
Input Voltage	V_{IN}	–0.3 to V_{CC} + 0.3	Vdc
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{STG}	–55 to + 150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

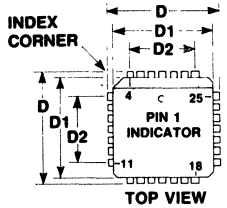
ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise specified)

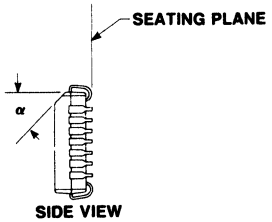
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Input Low Voltage	V_{IL}	–0.3	–	+0.8	V	
Input High Voltage	V_{IH}	+2.0	–	VCC +0.3	V	
Output Low Voltage	V_{OL}	–	–	+0.4	V	I_{LOAD} = 1.6 mA
Output High Voltage TTL	V_{OH}	+2.4	–	–	V	I_{LOAD} = –100 µA
CMOS	V_{OH}	+3.5	–	–	V	I_{LOAD} = 0
Output Low Current	I_{OL}	–1.6	–	–	mA	V_{OL} = 0.4V
Output High Current	I_{OH}	–100	–	–	µA	V_{OH} = 2.4V
Input Capacitance	C_{IN}	–	–	5	pF	
Power Dissipation	P_D	–	–	100	mW	

PACKAGE DIMENSIONS

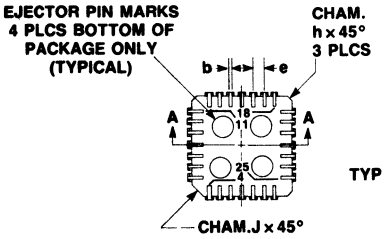
28-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



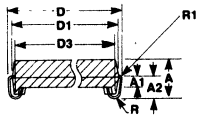
TOP VIEW



SIDE VIEW



BOTTOM VIEW

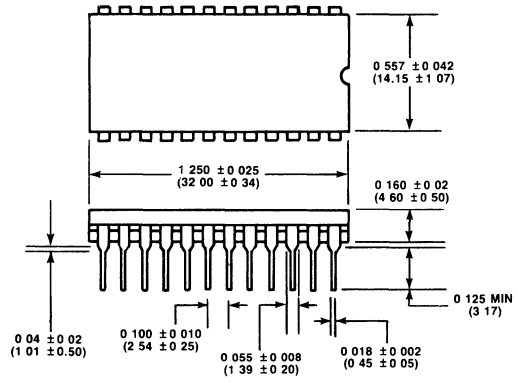


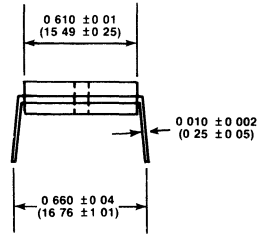
SECTION A-A
TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4 14	4 39	0 163	0 173
A1	1 37	1 47	0 054	0 058
A2	2 31	2 46	0 091	0 097
b	0 457 TYP		0 018 TYP	
D	12 37	12 52	0 487	0 493
D1	11 43	11 53	0 450	0 454
D2	7 54	7 70	0 297	0 303
D3	10 67 REF		0 420 REF	
e	1 27 BSC		0 050 BSC	
h	1 15 TYP		0 045 TYP	
J	0 25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0 89 TYP		0 035 TYP	
R1	0 25 TYP		0 010 TYP	

PACKAGE DIMENSIONS (CONT'D)

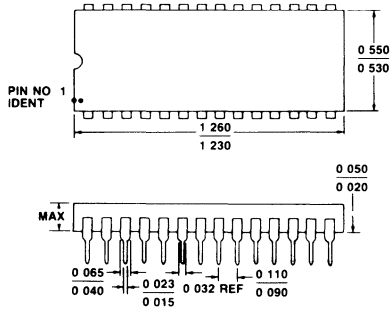
24-PIN CERDIP

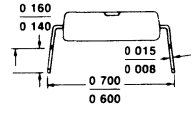




DIMENSIONS IN INCHES AND (MILLIMETERS)

24-PIN PLASTIC DIP





6

Rockwell

RT9170 Intelligent T-1 Controller

INTRODUCTION

The Rockwell RT9170 Intelligent T-1 Controller is a microprocessor (MPU) controlled device which implements T-1 interface between the multiplexed digital signal of the subscriber loop and the PCM highway of digital voice and data system equipment. The RT9170 handles both the D4 and the ESF standard with Facility Data Link (FDL) used in T-1 and ISDN Primary Rate digital carrier systems.

Users are provided a cost effective solution for T-1/ISDN Primary Rate interface which integrates complex functions to minimize system development time, component count, cost, and board space. Combining dedicated control pins with host addressable on-chip registers, maximum functional control is achieved with minimal microprocessor intervention. Direct control over the R8069 Line Interface Unit is provided by the RT9170 Intelligent T-1 Controller.

The RT9170 functional interface is illustrated in Figure 1.

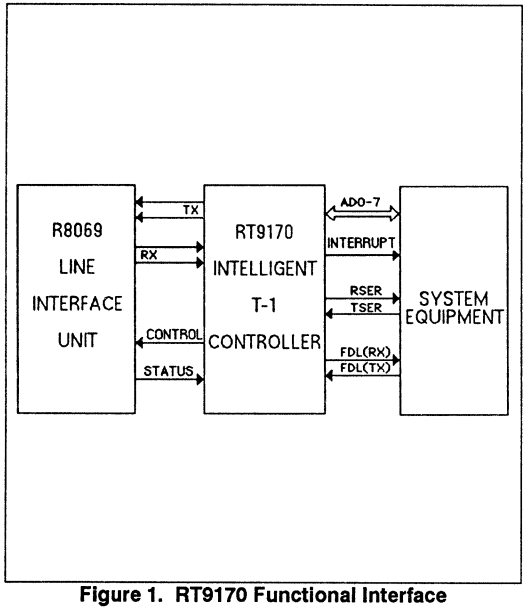


Figure 1. RT9170 Functional Interface

FEATURES

- Intelligent single chip DS1 T-carrier transceiver (1.544 MHz)
- Compatible with ANSI standards T1C1.2 covering Facility Data Link operations:
  - —Priority codeword handling
  - —Near-end and far-end performance monitoring
  - —Extracted link data handling
- Intel-compatible Microprocessor bus interface:
  - —8 bits address/data bus for programming control information.
- Separate serial interface for DS1 data
- Microprocessor-controlled registers: 16 Control, 14 Facility Data Link, 24 Per-channel Control, and 12 Receiver Signalling registers
- Maskable interrupts
- Independent transmit and receive function
- Off-line framer (External Transmit Sync) option
- T-1 formats with and without signalling
  - —T-1 (D4), 12 frames/superframe
  - —T-1 (ESF), 24 frames/superframe
- Comprehensive zero suppression modes
  - —B7 stuffing
  - —B8ZS
  - —Transparent
- Meets CCITT G.733 (1.544 MHz) and applicable sections of G.703
- Compatible with AT&T technical advisories on ESF and clear channel operation with B8ZS
- Alarm generation and detection
- Reframe time less than 10 ms
- Remote and locally controlled payload loopback
- Directly interfaces with the R8069 Line Interface Unit (LIU) and R8071 ISDN/DMI Link Layer Controller
- Available in 40-pin plastic or ceramic dual in-line (DIP) and 44-pin plastic leaded chip carrier (PLCC) packages
- Operates from a single +5 Vdc ± 5% power supply
- CMOS/TTL compatible inputs and outputs
- Low power CMOS technology

ORDERING INFORMATION

Part Number:
RT9170

- Temperature
  - Blank = 0°C to 70°C
- Package
  - P = 40–Pin Plastic Dip
  - J = 44–Plastic Leaded Chip Carrier (PLCC)

GENERAL DESCRIPTION

Microprocessor Interface

The RT9170 provides the intelligent functions of T-1 mode control, signalling control, error and alarm reporting, and handling of the Facility Data Link through internal registers accessible using the microprocessor interface. These registers are programmed via an 8-bit parallel Microprocessor Unit (MPU) control interface. The RT9170 has 16 Control Registers; 14 Facility Data Link Registers; 24 Per-Channel Control Registers, and 12 Receiver Signalling Registers. The RT9170 also provides maskable interrupts for exception condition handling. The RT9170 interface signals are shown in Figure 2.

Facility Data Link

Control over the ESF Facility Data Link (4 kbps channel) is managed by the RT9170, which adheres to ANSI standard T1C1.2. The RT9170 supports Priority Code Word formatting, user-supplied HDLC protocol, and performance monitoring and reporting. Near-end and Far-End Performance message reporting is handled in the FDL registers. The ESF data link may be used for user-supplied Extracted Link Protocol transmission when it is not being used for Yellow Alarms, codeword messages, or performance messages. Two pins, EXDATA and TLCLK, are provided for this purpose.

Per-Channel Control

Users are provided control over Signal and Trunk Conditioning on a per-channel basis. There are 24 internal registers provided, one for each T-1 channel. Robbed-bit signalling (2, 4, or 16 code "ABCD" signalling), or no-signalling, can be implemented on a per-channel basis. Trunk and Signal Conditioning substitutions may be made on a per-channel basis to include IDLE (both user specific and standard IDLE), BUSY, VACANT, and Digital Milliwatt codes.

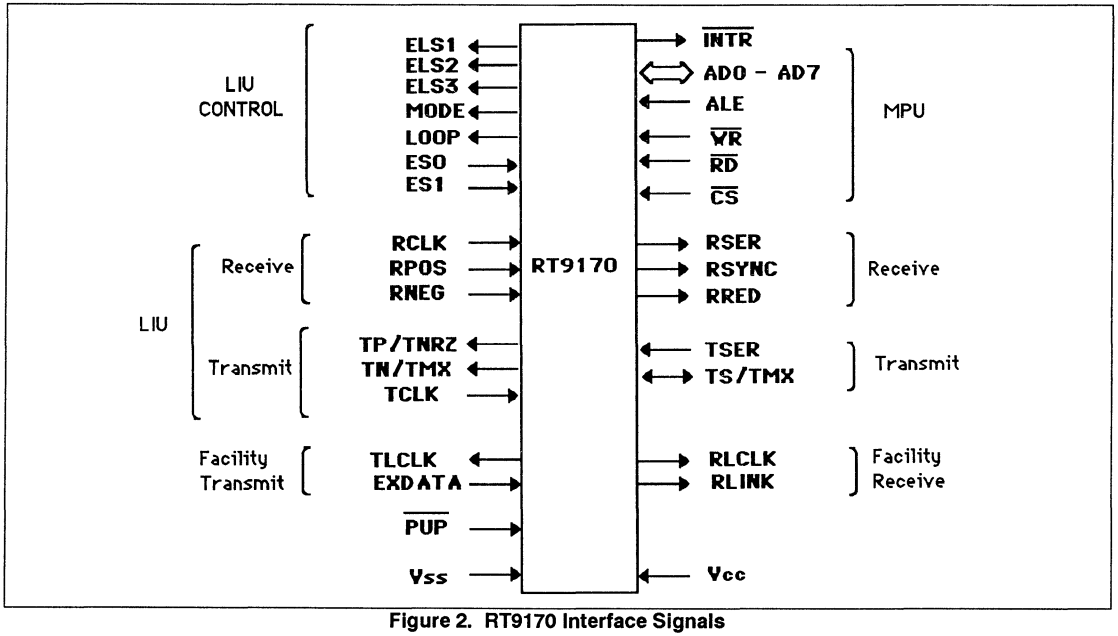


Figure 2. RT9170 Interface Signals

Transceiver and Off-Line Framer Functions

The RT9170 has fully independent transmit and receive sections. A robust framing algorithm which prevents synchronization on patterns which mimic the framing bits is implemented for ESF mode. An Off-Line Framer mode is provided. In this mode, the Receiver Sync signals are derived from the Off-Line Framer timing, which also provides bit, frame, and multiframe timing for receiving Trunk and Signal Conditioning. Transceiver functions also include zero suppression, alarm generation and detection, and loopback modes.

General

The RT9170 supports the T1C1.2 technical subcommittee draft, CCITT Recommendation G.733, applicable sections of G.703, and AT&T technical advisories on clear-channel capability and Extended SuperFrame format (ESF). The following modes of T-1 PCM operation are supported: 193S, 193E, 193N, 193F.

The RT9170 is a low power CMOS device which operates from a single +5 volt power supply and a sampling clock of 1.544 MHz. Packaged in a 40-pin plastic DIP or a 44-pin PLCC, the RT9170 requires less real-estate and offers increased functionality than previous devices. The flexibility and power of the RT9170 supports use in diverse areas of voice and data communications.

R6551
Asynchronous Communications Interface Adapter (ACIA)

DESCRIPTION

The Rockwell R6551 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at $^1/_{16}$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $^1/_{16}$ times an external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R6551's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receiver circuits.

ORDERING INFORMATION

Part No.: R6551

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range:
  - 1 = 1 MHz
  - 2 = 2 MHz
- Frequency Range.
  - No Letter = 1 MHz
  - A = 2 MHz

FEATURES

- Compatible with 8-bit microprocessors
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 2 or 1 MHz operation
- 5.0 Vdc ± 5% supply requirements
- 28-pin plastic or ceramic DIP
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 microprocessors

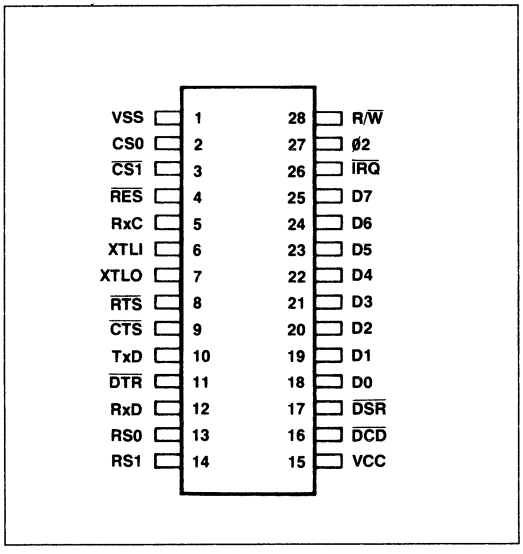


Figure 1. R6551 ACIA Pin Configuration

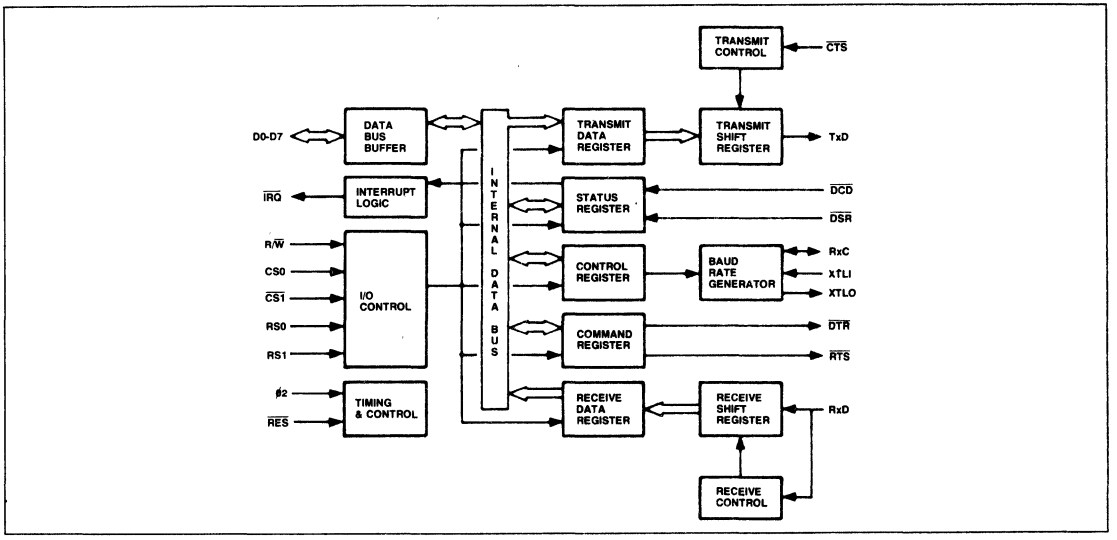


Figure 2. ACIA Internal Organization

FUNCTIONAL DESCRIPTION

A block diagram of the ACIA is presented in Figure 2. A description of each functional element of the device follows.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data lines to the ACIA internal data bus. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer drives the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select (RS1, RS0) and Read/Write (R/$\overline{W}$) lines as described later in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus, the registers, the Data Bus Buffer, the microprocessor data bus, and the hardware reset.

Timing is controlled by the system Ø2 clock input. The chip will perform data transfers to or from the microcomputer data bus during the Ø2 high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmit and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (R/$\overline{W}$) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status information. The interrupt conditions are Data Set Ready and Data Carrier Detect transitions, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	$\overline{DSR}$	$\overline{DCD}$	TDRE	RDRF	OVRN	FE	PE

Bit 7 **Interrupt (IRQ)**
0 No interrupt
1 Interrupt has occurred

Bit 6 **Data Set Ready ($\overline{DSR}$)**
0 $\overline{DSR}$ low (ready)
1 $\overline{DSR}$ high (not ready)

Bit 5 **Data Carrier Detect ($\overline{DCD}$)**
0 $\overline{DCD}$ low (detected)
1 $\overline{DCD}$ high (not detected)

Bit 4 **Transmitter Data Register Empty**
0 Not empty
1 Empty

Bit 3 **Receiver Data Register Full**
0 Not full
1 Full

Bit 2 **Overrun***
0 No overrun
1 Overrun has occurred

Bit 1 **Framing Error***
0 No framing error
1 Framing error detected

Bit 0 **Parity Error***
0 No parity error
1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	**Hardware reset**
—	—	—	—	—	0	—	—	**Program reset**

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (Bit 2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register).

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

NOTE: There is a delay of approximately $\frac{1}{16}$ of a bit time after TDR becomes empty/full before this flag is updated.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until after the Status Register has been interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 — Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits For WL = 5 and no parity
1	1 Stop bit For WL = 8 and parity

Bits 6-5 — Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 — Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 — Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	16x External Clock
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
–	–	–	–	–	–	–	–	Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at $^1/_{16}$ an external clock rate or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the ACIA. Figure 3 shows the Transmitter and Receiver layout.

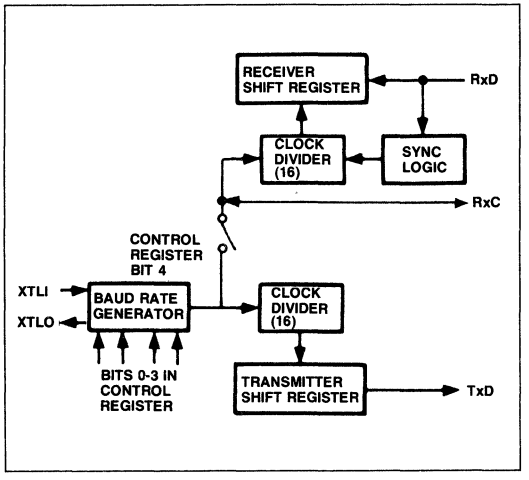


Figure 3. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of $^1/_{16}$ an external clock. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, or 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PMC1	PMC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode Bits 2 and 3 must also be zero for receiver echo mode, $\overline{RTS}$ will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	$\overline{RTS}$ = High, transmitter disabled*
0	1	$\overline{RTS}$ = Low, transmit interrupt enabled
1	0	$\overline{RTS}$ = Low, tansmit interrupt disabled
1	1	$\overline{RTS}$ = Low, transmit interrupt disabled, transmit break on TxD**

Bit 1 Receiver Interrupt Request Disabled (IRD)

0	$\overline{IRQ}$ enabled (receiver)
1	$\overline{IRQ}$ disabled (receiver)

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{DTR}$ high)*
1	Data terminal ready ($\overline{DTR}$ low)

NOTES

*The transmitter is disabled immediately. The receiver is disabled but will first complete receiving a byte in process of being received.

**A break is transmitted only after the end of a character stream. If the Transmit Data Register contains a character, the break is not transmitted.

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. $\overline{DTR}$ also enables and disables the transmitter and receiver.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 disables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
–	–	–	0	0	0	0	0	Program reset

INTERFACE SIGNALS

Figure 4 shows the ACIA interface signals associated with the microprocessor and the modem.

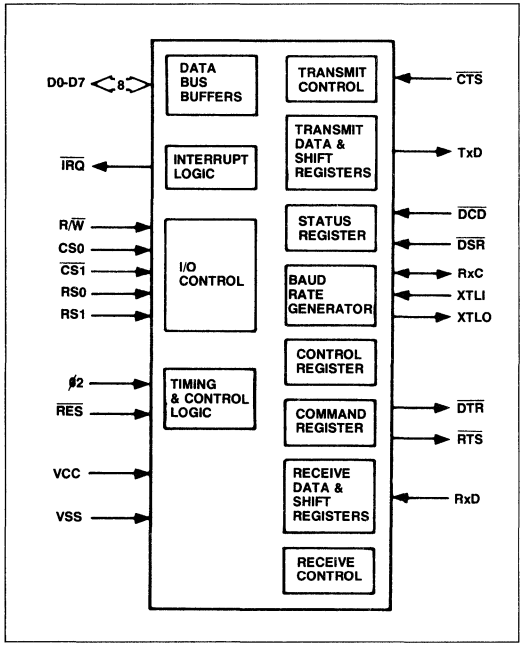


Figure 4. ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset ($\overline{RES}$)

During system initialization a low on the $\overline{RES}$ input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{DSR}$ and $\overline{DCD}$ lines, and the transmitter Empty bit, which is set. $\overline{RES}$ must be held low for one Ø2 clock cycle for a reset to occur.

Input Clock (Ø2)

The input clock is the system Ø2 clock and clocks all data transfers between the system microprocessor and the ACIA.

NOTE: The specified maximum cycle time for the signal on this input is 40 μs. This specification must be observed to prevent loss of data.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the commmon $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, $\overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select decoding.

Table 1. ACIA Register Selection

RS1	RS0	Register Operation	
		R/$\overline{W}$ = Low	R/$\overline{W}$ = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Only the Command and Control registers can be both read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset ($\overline{RES}$); refer to the register description.

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to a series mode external crystal (1.8432 MHz) to derive the various baud rates. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

Transmit Data (TxD)

The TxD output line transfers serial nonreturn-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or by an external clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is determined by the programmed baud rate or by an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

RxC is a bi-directional pin which is either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ output pin controls the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

Clear to Send ($\overline{CTS}$)

The $\overline{CTS}$ input pin controls the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

Data Terminal Ready ($\overline{DTR}$)

This output pin indicates the status of the ACIA to the modem. A low on $\overline{DTR}$ indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect ($\overline{DCD}$)

The $\overline{DCD}$ input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output ($\overline{IRQ}$) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

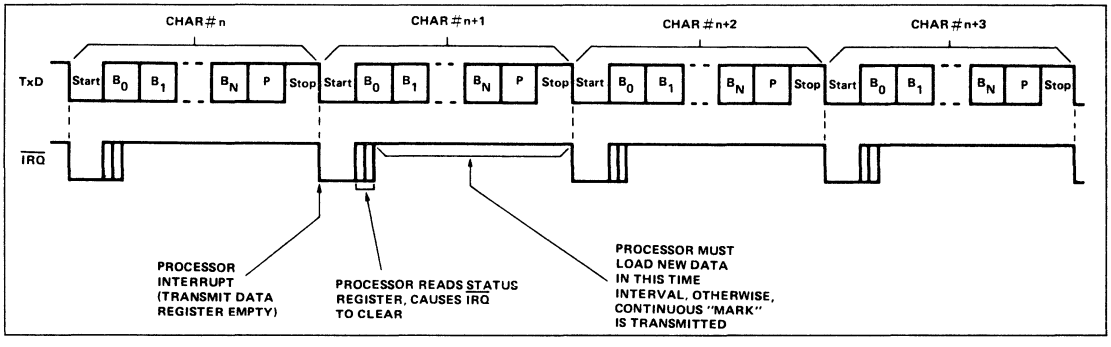


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{IRQ}$ when the ACIA has received a full data word. This occurs at about $^{9}/_{16}$ point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

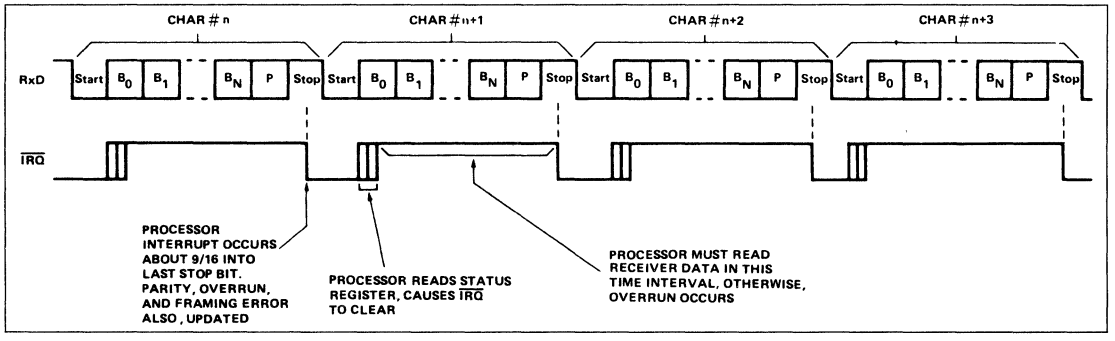


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{IRQ}$ interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

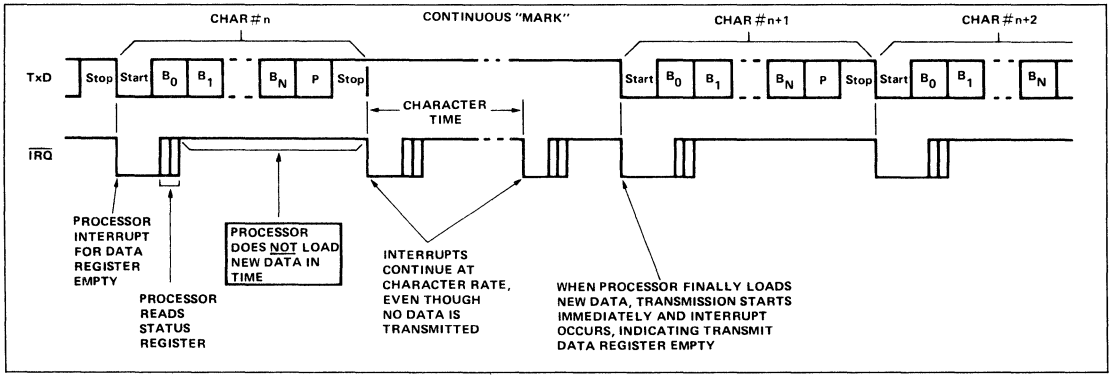


Figure 7. Transmit Data Register Not Loaded by Processor

$\overline{CTS}$ is the Clear-to-Send Signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "MARK" condition. Interrupts continue at the same rate, but the Status Register does not indicate that the Transmit Data Register is empty. Since there is no status bit for $\overline{CTS}$, the processor must deduce that $\overline{CTS}$ has gone to the FALSE (high) state. $\overline{CTS}$ is a transmit control line only, and has no effect on the R6551 Receiver Operation. Figure 8 shows the timing relationship for this operation.

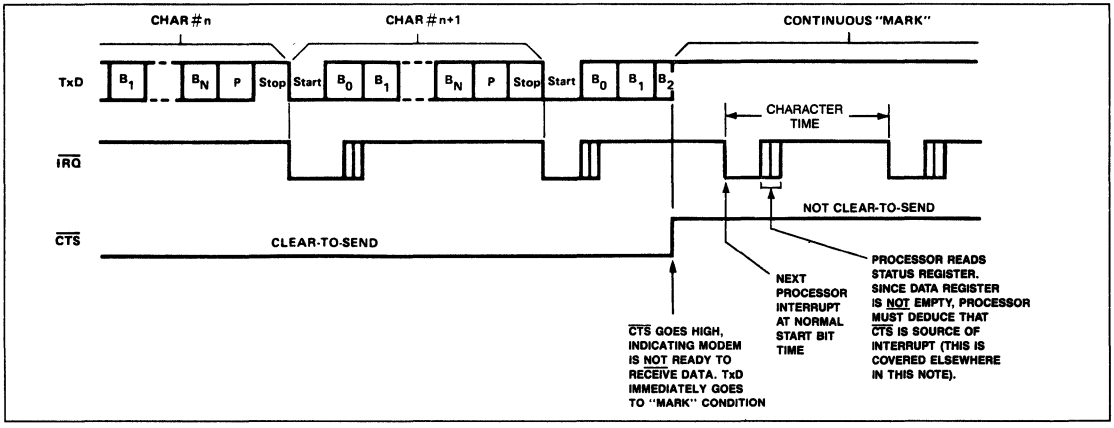


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver data Register in the allocated time, then, when the next interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost. Figure 9 shows the timing relationship for this mode.

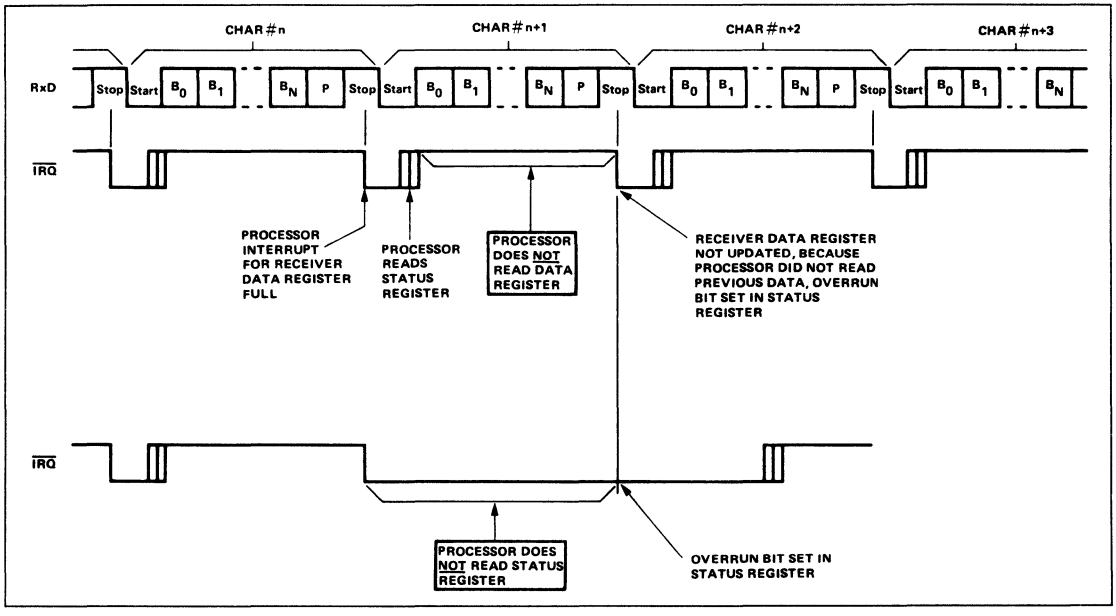


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time, as shown in Figure 10.

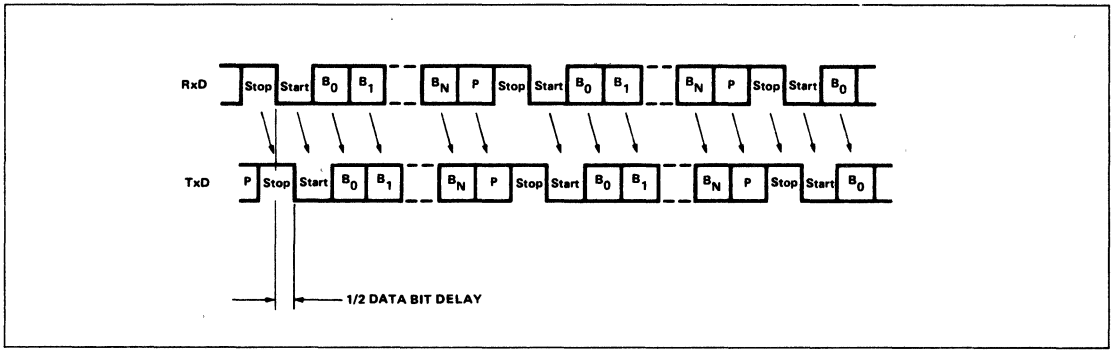


Figure 10. Echo Mode Timing

Effect of $\overline{CTS}$ on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by $\overline{CTS}$, however, the Transmitter is affected when $\overline{CTS}$ goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that the Receiver Data Register is full in response to an $\overline{IRQ}$, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

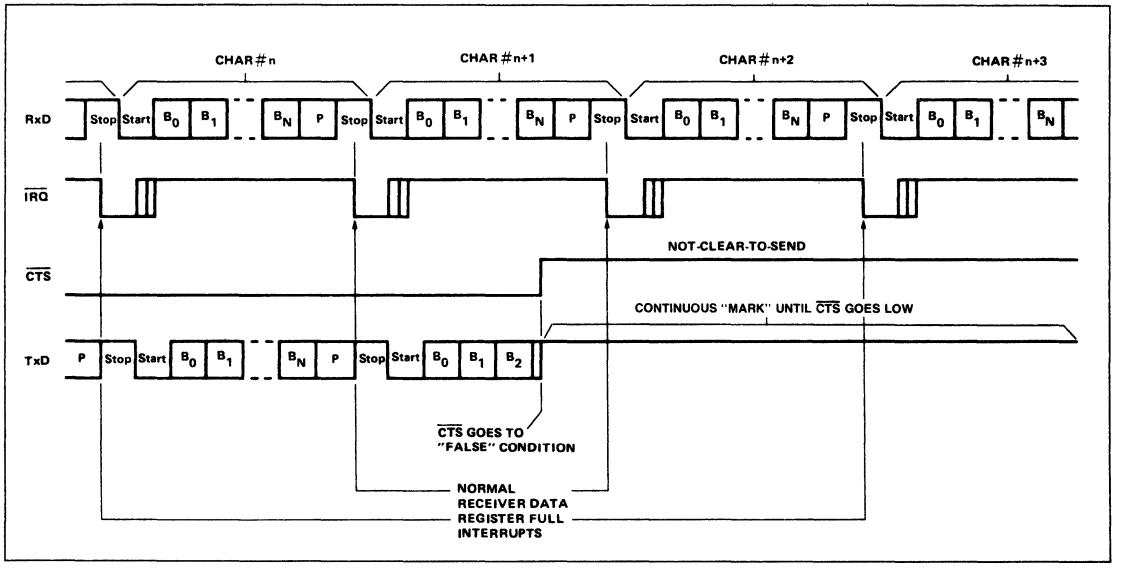


Figure 11. Effect of $\overline{CTS}$ on Echo Mode

Overrun in Echo Mode

If Overrun occurs in Echo Mode, the Receiver is affected the same way as a normal overrun in Receive Mode. For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

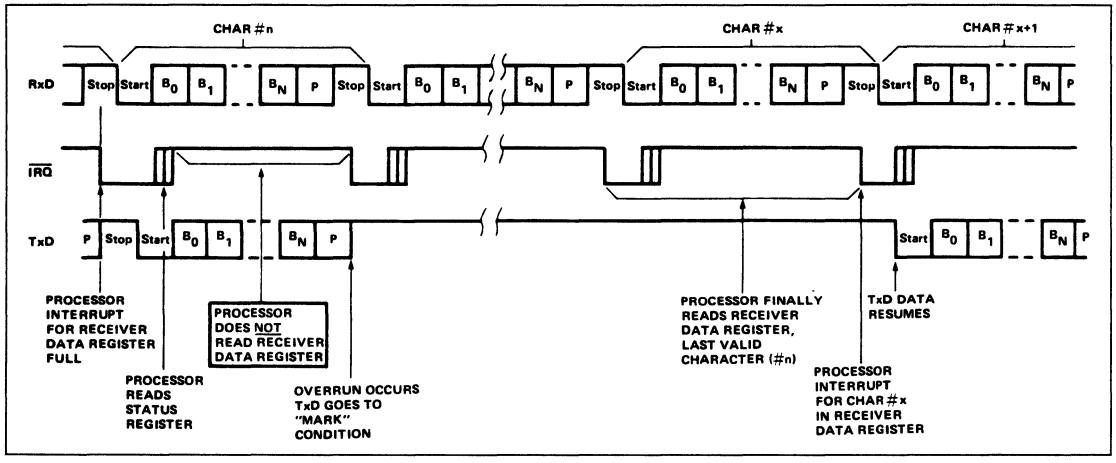


Figure 12. Overrun in Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 1 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to $\overline{IRQ}$, generated by RDRF, the Status Register can also be checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

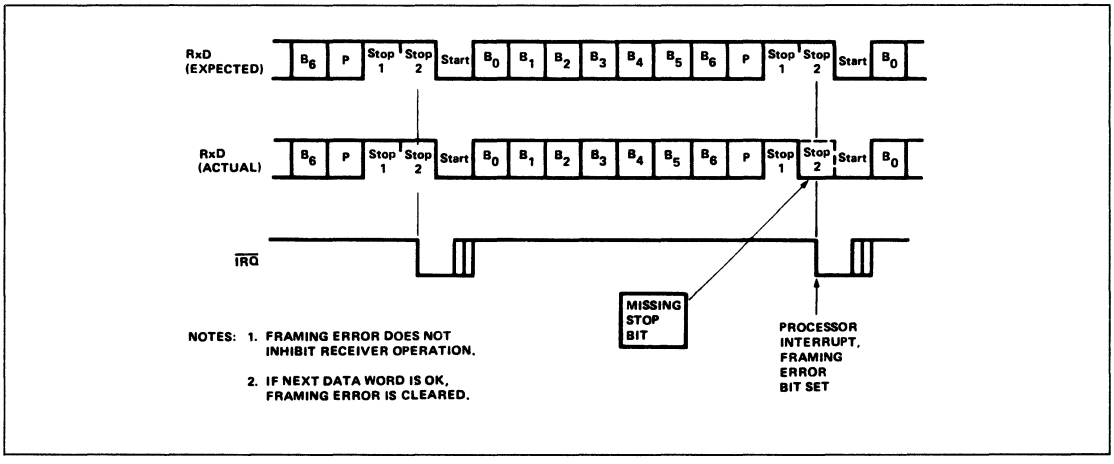


Figure 13. Framing Error

Effect of $\overline{DCD}$ on Receiver

$\overline{DCD}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts $\overline{IRQ}$ whenever $\overline{DCD}$ changes state and indicates this condition via bit 5 in the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the ACIA automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another $\overline{IRQ}$ occurs (see Figure 14).

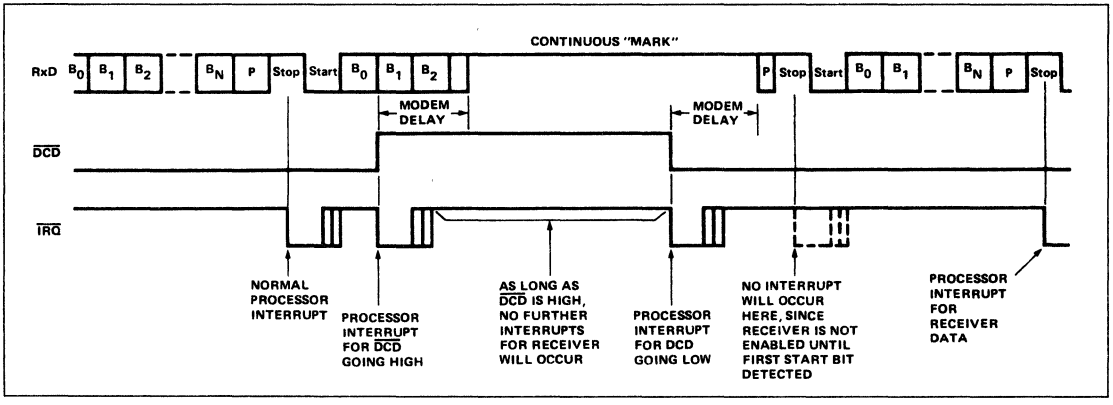


Figure 14. Effect of DCD on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{IRQ}$ asserted for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode.

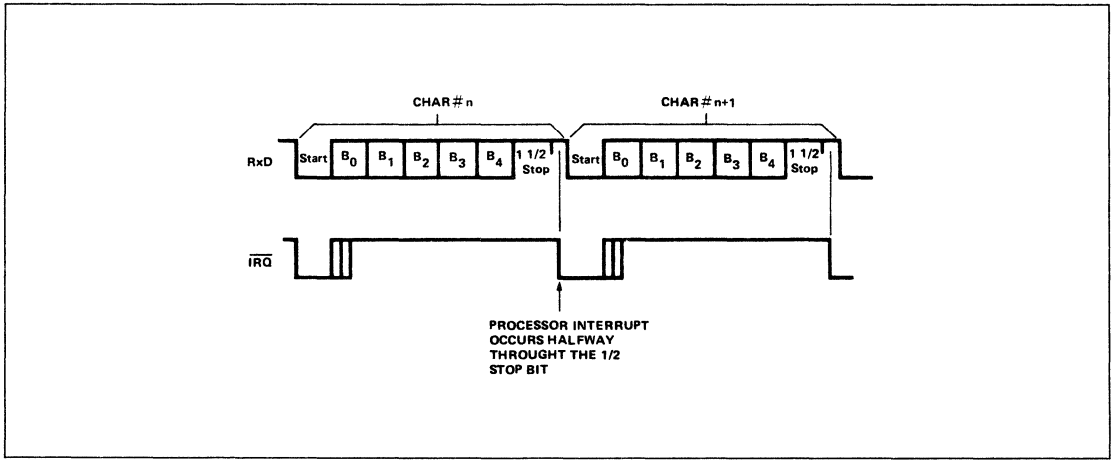


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

Note

If, while operating in the Transmit Continuous "BREAK" mode, the $\overline{CTS}$ should go to a high, the TxD will be overridden by the $\overline{CTS}$ and will go to continuous "MARK" at the beginning of the next character transmitted after the $\overline{CTS}$ goes high.

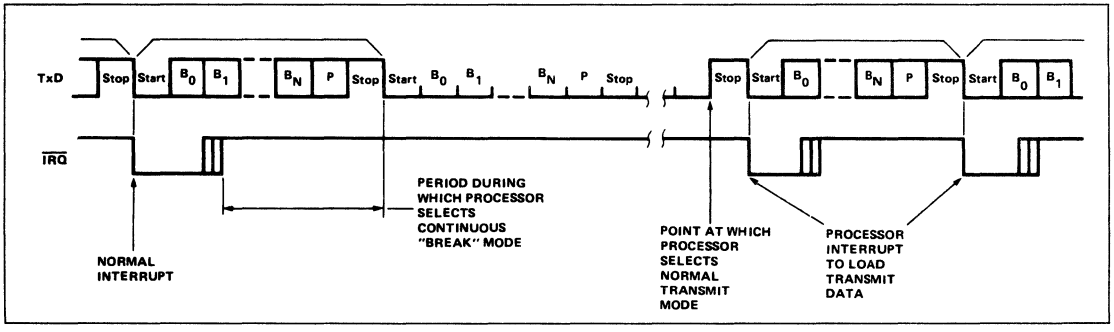


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17 shows the timing relationship for continuous "BREAK" characters.

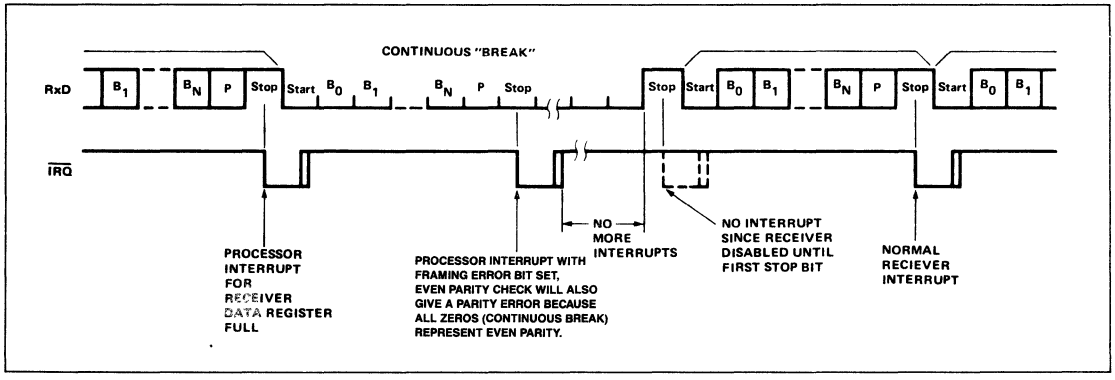


Figure 17. Receive Continuous "BREAK"

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check IRQ (Bit 7) in the data read from the Status Register

   If not set, the interrupt source is not the ACIA.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2) if the Receiver Data Register is full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above conditions exist, then $\overline{CTS}$ must have gone to the false (high) state.

PROGRAM RESET OPERATION

A program reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program reset on internal registers.

2. The $\overline{DTR}$ line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.

4. $\overline{DCD}$ and $\overline{DSR}$ interrupts are disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.

5. Overrun cleared, if set.

MISCELLANEOUS

1. If Echo Mode is selected, $\overline{RTS}$ goes low.

2. If Bit 0 of Command Register ($\overline{DTR}$) is 0 (disabled), then:

   a) All interrupts are disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter is disabled immediately.
   c) Receiver is disabled, but a character currently being received will be completed first.

3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.

4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.

5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.

6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit time to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. $\overline{DCD}$ andd $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no affect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated to GND.

CRYSTAL/CLOCK CONSIDERATIONS

CLOCK OSCILLATOR

The on-chip oscillator is designed for a series resonant crystal connected between XTLI and XTLO pins (Figure 18).

A series resonant crystal is specified by the series resistance (R_S) at its series resonant frequency. For proper oscillator operation, the selected series resonant crystal should have a series resistance less than 400 ohms.

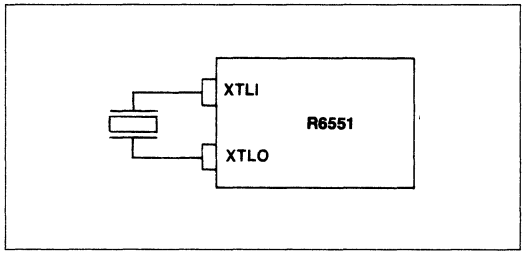


Figure 18. Internal Clock Connection

EXTERNAL CLOCK

The XTLI input may be used as an external clock input (Figure 19). For this implementation, a times 16 clock is input on XTLI and XTLO is left open.

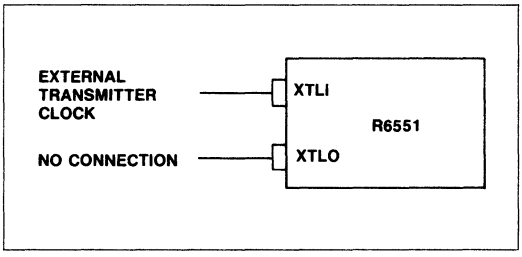


Figure 19. External Clock Connection

BAUD RATE GENERATION

DIVISORS

The internal counter/divider circuit generates appropriate divisors to produce standard baud rates when a 1.8432 MHz crystal is connected between XTLI and XTLO. Control Register bits 0-3 select the divisor for a particular bit rate as shown in Table 2.

GENERATING NON-STANDARD BAUD RATES

By using a different crystal, non-standard baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits 3 2 1 0	Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (F)
0 0 0 0	No Divisor Selected	16 × External Clock at Pin RxC	16 × External Clock at Pin RxC
0 0 0 1	36,864	1 8432 × 10^6 / 36,864 = 50	F / 36,864
0 0 1 0	24,576	1 8432 × 10^6 / 24,576 = 75	F / 24,576
0 0 1 1	16,769	1 8432 × 10^6 / 16,769 = 109.92	F / 16,769
0 1 0 0	13,704	1.8432 × 10^6 / 13,704 = 134 51	F / 13,704
0 1 0 1	12,288	1.8432 × 10^6 / 12,288 = 150	F / 12,288
0 1 1 0	6,144	1.8432 × 10^6 / 6,144 = 300	F / 6,144
0 1 1 1	3,072	1 8432 × 10^6 / 3,072 = 600	F / 3,072
1 0 0 0	1,536	1.8432 × 10^6 / 1,536 = 1,200	F / 1,536
1 0 0 1	1,024	1.8432 × 10^6 / 1,024 = 1,800	F / 1,024
1 0 1 0	768	1.8432 × 10^6 / 768 = 2,400	F / 768
1 0 1 1	512	1.8432 × 10^6 / 512 = 3,600	F / 512
1 1 0 0	384	1 8432 × 10^6 / 384 = 4,800	F / 384
1 1 0 1	256	1.8432 × 10^6 / 256 = 7,200	F / 256
1 1 1 0	192	1.8432 × 10^6 / 192 = 9,600	F / 192
1 1 1 1	96	1 8432 × 10^6 / 96 = 19,200	F / 96

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating an ACIA is shown in Figure 20.

It may be desirable to include in the system a facility for local loop-back testing.

In loop-back testing from the point of view of the processor, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry. Figure 21 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables outputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs (i.e. TxD to RxD, $\overline{DTR}$ to $\overline{DCD}$, $\overline{RTS}$ to $\overline{CTS}$).

LLB may be tied to a peripheral control pin (from an R6520 or R6522, for example) to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

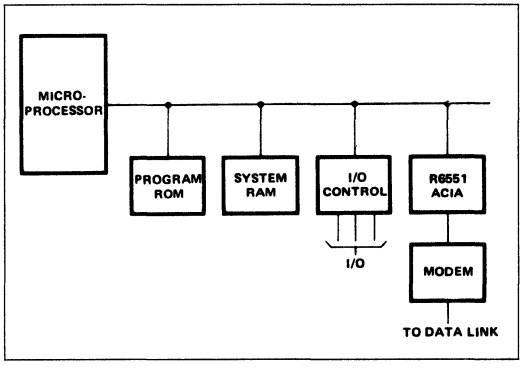


Figure 20. Simplified System Diagram

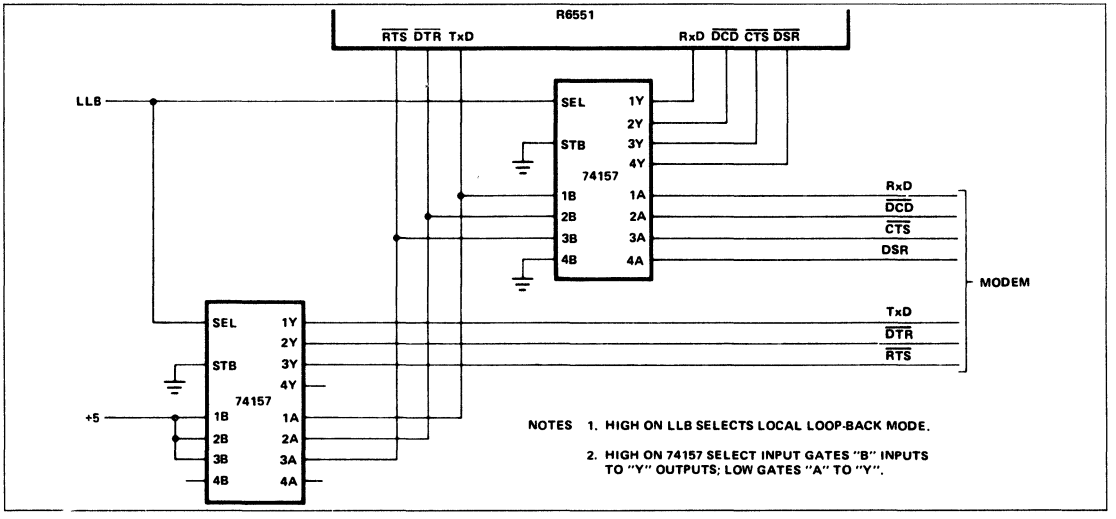


Figure 21. Loop-Back Circuit Schematic

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{IRQ}$ generation are shown in Figures 22, 23 and 24, respectively. The corresponding timing characteristics are listed in the Table 3.

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
RTS Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns
Load Capacitance $\overline{DTR}$, RTS	C_L	—	130	—	130	pF
TxD		—	30	—	30	pF

Notes:
(t_R, t_F = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

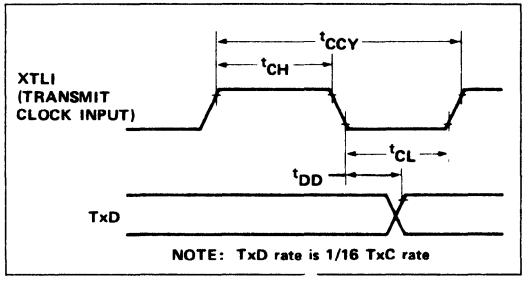


Figure 22. Transmit Timing with External Clock

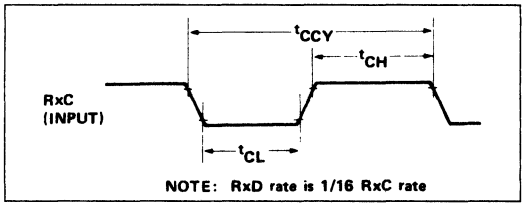


Figure 23. Receive External Clock Timing

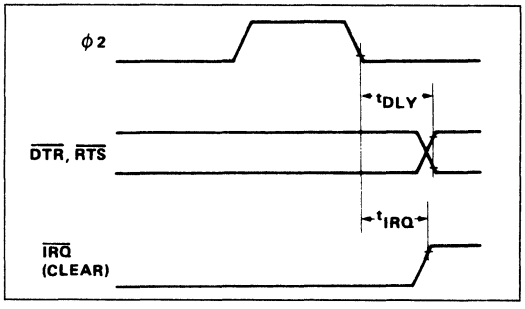


Figure 24. Interrupt and Output Timing

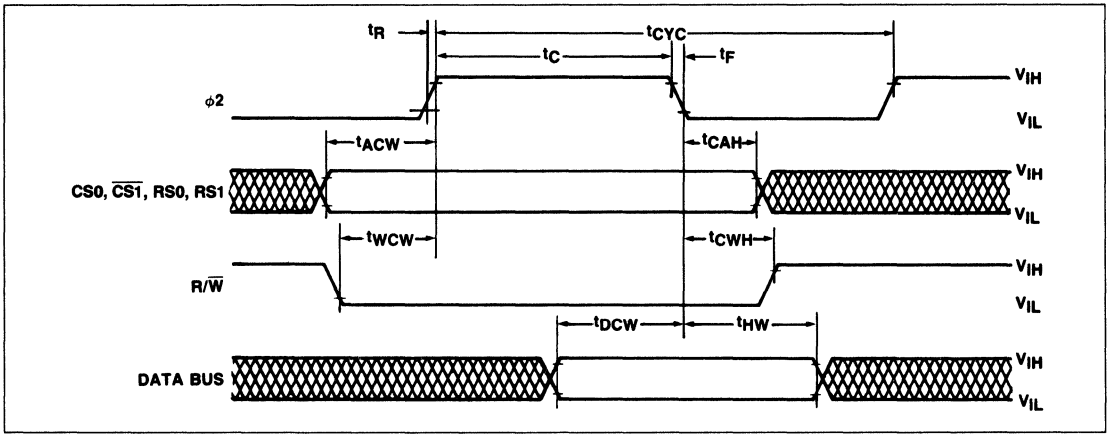
6

AC CHARACTERISTICS

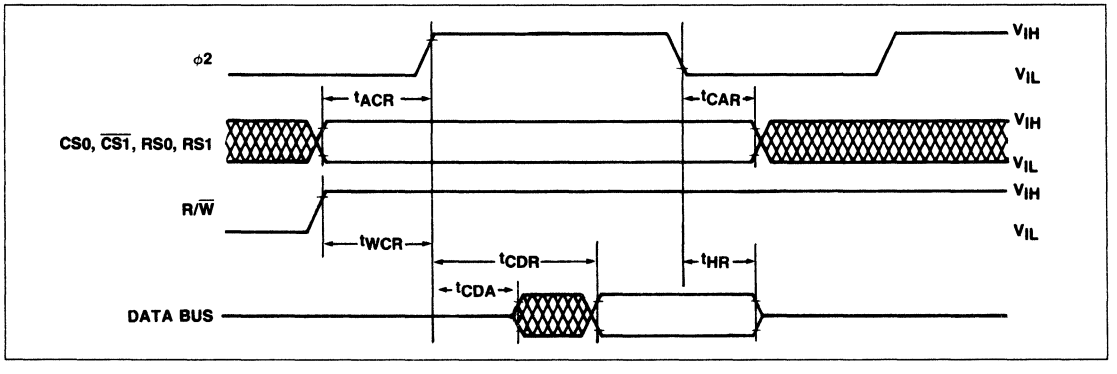
(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
ø2 Pulse Width	t_C	400	—	200	—	ns
Address Set-Up Time	t_{ACW}, t_{ACR}	120	—	70	—	ns
Address Hold Time	t_{CAH}, t_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}, t_{WCR}	120	—	70	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	150	—	60	—	ns
Data Bus Hold Time	t_{HW}	20	—	20	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	150	ns
Read Hold Time	t_{HR}	20	—	20	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	40	—	ns

Notes: 1. t_R and t_F = 10 to 30 ns.
2. D0-D7 load capacitance = 130 pF.
3. Timing measurements are referenced to/from a low of 0.8 volts and a high of 2.0 volts.



Write Timing Diagram



Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC}	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC}	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40°C to +85°C

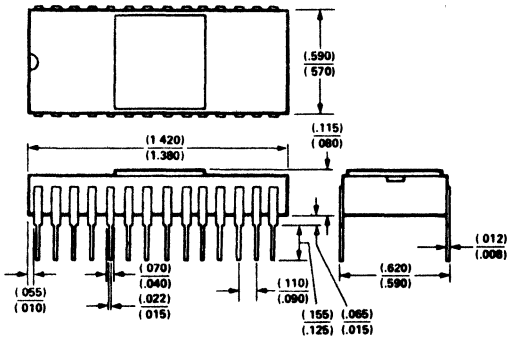
DC CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

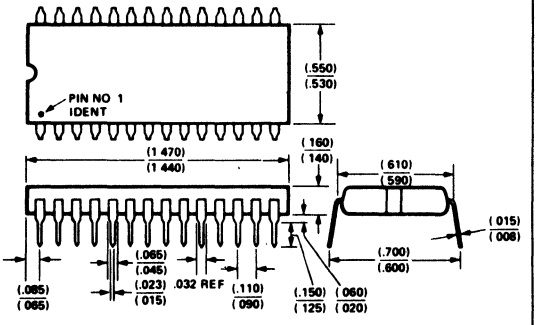
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTLI and XTLO XTLI and XTLO	V_{IH}	 2.0 2.4	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage Except XTLI and XTLO XTLI and XTLO	V_{IL}	 V_{SS} V_{SS}	 — —	 0.8 0.4	V	
Input Leakage Current Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, CS1, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$	I_{IN}	—	—	2.5	μA	V_{IN} = 0V to 5V V_{CC} = 0V
Input Leakage Current for High Impedance (Three State Off) D0–D7	I_{TSI}	—	—	±10.0	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	V_{OH}	2.4	—	—	V	I_{LOAD} = −100 μA V_{CC} = 4 75V
Output Low Voltage D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	I_{OH}	−100	—	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking) D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (off state) $\overline{IRQ}$	I_{OFF}	—	—	10.0	μA	V_{OUT} = 5V
Clock Capacitance (Ø2)	C_{CLK}	—	—	20	pF	V_{CC} = 5V V_{IN} = 0V f = 1 MHz T_A = 25°C
Input Capacitance except Ø2, XTLI, XTLO	C_{IN}	—	—	10	pF	
Output Capacitance	C_{OUT}	—	—	10	pF	
Power Dissipation	P_D	—	170	300	mW	T_A = 0°C

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



R65C51
Asynchronous Communications Interface Adapter (ACIA)

DESCRIPTION

The Rockwell CMOS R65C51 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be any one of 15 different rates from 50 to 19,200 baud, or $^1/_{16}$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $^1/_{16}$ times an external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, $1^1/_2$, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R65C51's operating modes and data checking parameters and determine operational status.

FEATURES

- Low power CMOS N-well silicon gate technology
- Replacement for NMOS R6551 ACIA
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 1 or 2 MHz operation
- 5.0 Vdc ±5% supply requirements
- Wide range of packages available
  - — 28-pin ceramic or plastic DIP
  - — 28-pin plastic leaded chip carrier (PLCC)
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 microprocessors

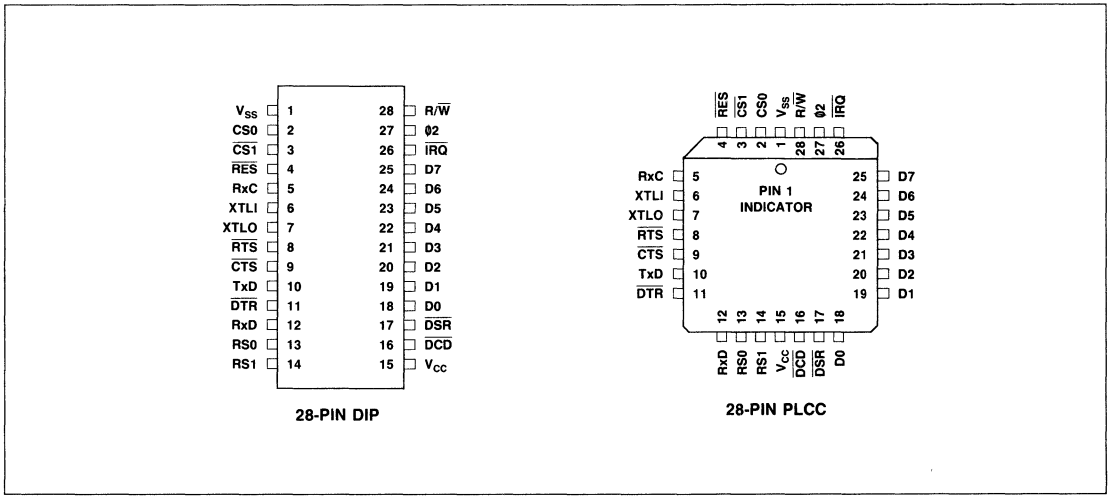
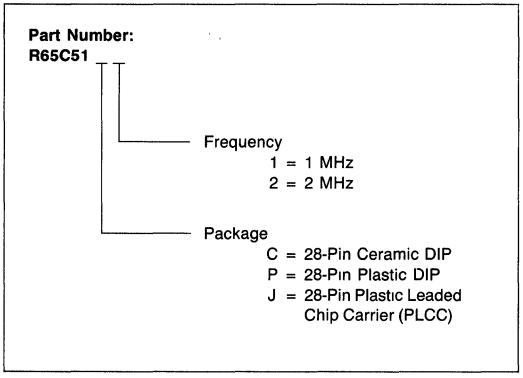


Figure 1. R65C51 ACIA Pin Assignments

ORDERING INFORMATION



INTERFACE SIGNALS

Figure 1 (front page) shows the R65C51 ACIA pin assignments and Figure 2 groups the signals by functional interface.

MICROPROCESSOR INTERFACE

Reset ($\overline{RES}$)

During system initialization, a low on the $\overline{RES}$ input causes a hardware Reset to occur. Upon Reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{DSR}$ and $\overline{DCD}$ lines, and the Transmitter Empty bit, which is set. $\overline{RES}$ must be held low for one Ø2 clock cycle for a reset to occur.

Input Clock (Ø2)

The input clock is the system Ø2 clock and clocks all data transfers between the system microprocessor and the ACIA.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

Data Bus (D0–D7)

The eight data line (D0–D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, $\overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select decoding.

Table 1. ACIA Register Selection

		Register Operation	
RS1	RS0	R/$\overline{W}$ = Low	R/$\overline{W}$ = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receive circuits.

Only the Command and Control registers can be both read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset ($\overline{RES}$); refer to the register description.

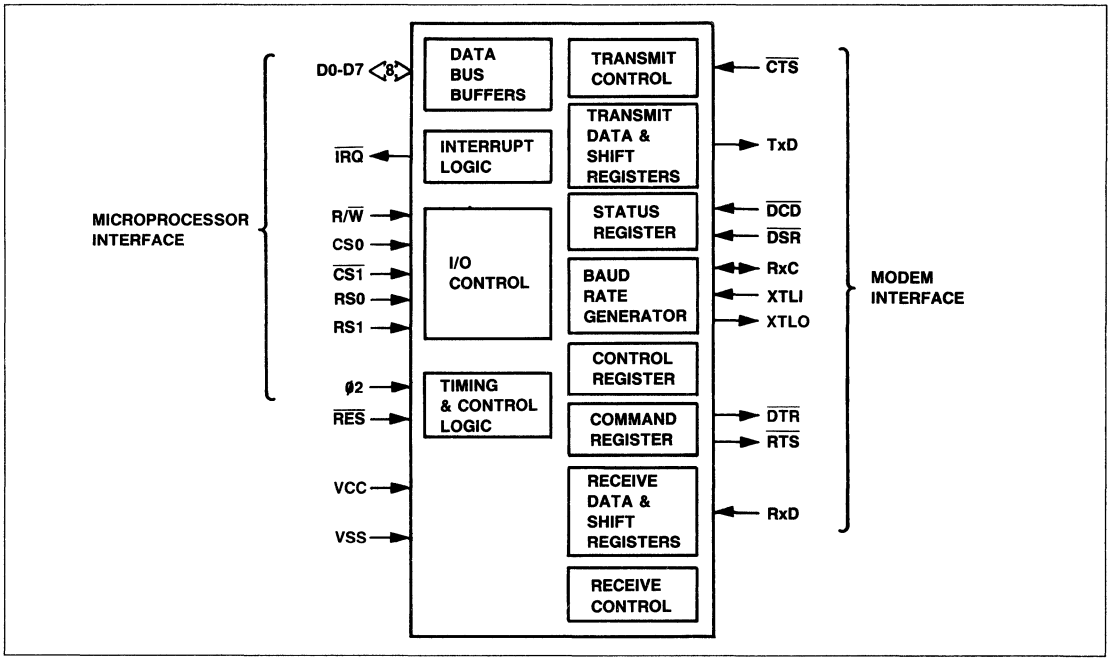


Figure 2. ACIA Interface Diagram

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to a parallel mode external crystal (1.8432 MHz) to derive the various baud rates. Note that capacitors are required from XTLI to ground and from XTLO to ground. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float.

Transmit Data (TxD)

The TxD output line transfers serial non-return-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or by an external transmitter clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is determined by the programmed baud rate or by an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

RxC is a bi-directional pin which is either the external receiver clock input or a clock output of 16x the baud rate. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ output pin controls the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

Clear to Send ($\overline{CTS}$)

The $\overline{CTS}$ input pin controls the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

Data Terminal Ready ($\overline{DTR}$)

This output pin indicates the status of the ACIA to the modem. A low on $\overline{DTR}$ indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect ($\overline{DCD}$)

The $\overline{DCD}$ input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

FUNCTIONAL DESCRIPTION

A block diagram of the R65C51 ACIA is presented in Figure 3. A description of each functional element of the device follows.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data lines to the ACIA internal data bus. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer drives the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receive Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select (RS1, RS0) and Read/Write (R/$\overline{W}$) lines as shown in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus, the registers, the Data Bus Buffer, the microprocessor data bus, and the hardware reset.

Timing is controlled by the system ϕ2 clock input. The chip will perform data transfers to or from the microcomputer data bus during the ϕ2 high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmit and Receive circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (R/$\overline{W}$) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care" bits.

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

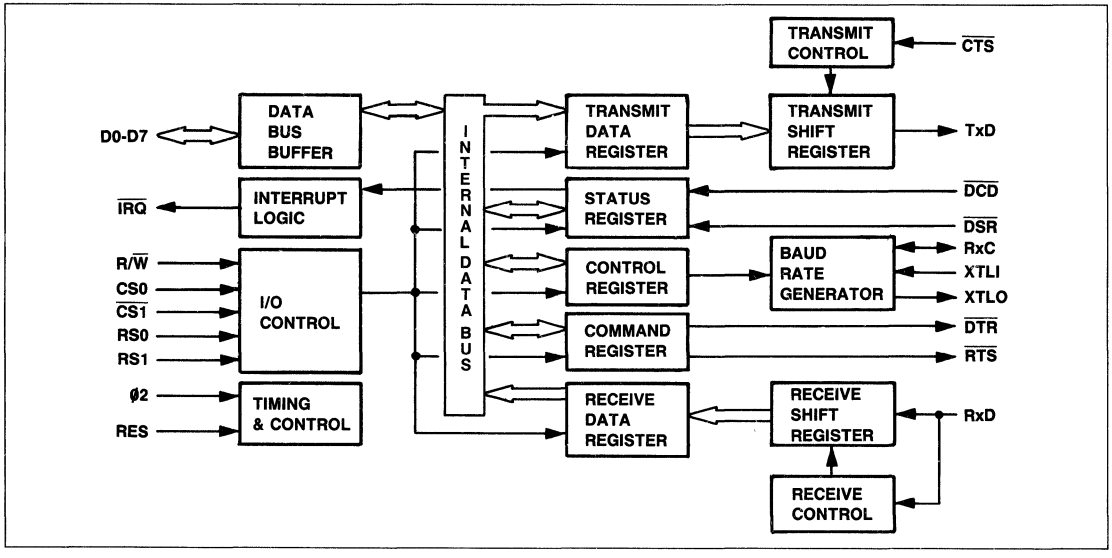


Figure 3. R65C51 ACIA Block Diagram

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status information. The interrupt conditions are Data Set Ready and Data Carrier Detect transitions, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0, respectively).

7	6	5	4	3	2	1	0
IRQ	$\overline{DSR}$	$\overline{DCD}$	TDRE	RDRF	OVRN	FE	PE

Bit 7 Interrupt (IRQ)
0 No interrupt
1 Interrupt has occurred

Bit 6 Data Set Ready (DSR)
0 DSR low (ready)
1 DSR high (not ready)

Bit 5 Data Carrier Detect (DCD)
0 DCD low (detected)
1 DCD high (not detected)

Bit 4 Transmitter Data Register Empty
0 Not empty
1 Empty

Bit 3 Receiver Data Register Full
0 Not full
1 Full

Bit 2 Overrun*
0 No overrun
1 Overrun has occurred

Bit 1 Framing Error*
0 No framing error
1 Framing error detected

Bit 0 Parity Error*
0 No parity error
1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	Hardware reset
_	—	—	—	—	0	—	—	Program reset

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (Bit 2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register.)

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

NOTE: There is a delay of approximately $\frac{1}{16}$ of a bit time after the TDR becomes empty/full before this flag is updated.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs, unless bit 1 of the Command Register (IRD) is set to a 1 to disable $\overline{IRQ}$. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until after the Status Register has been interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new state. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits For WL = 5 and no parity
1	1 Stop bit For WL = 8 and parity

Bits 6-5 Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	TxC rate ÷ 16*
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

*XTLI is the input for the External Transmitter Clock (TxC)

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
—	—	—	—	—	—	—	—	Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at 1/16 an external transmitter clock rate or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate as the transmitter (bit 4 = 1), then RxC becomes an output (at 16x the baud rate) and can be used to slave other circuits to the ACIA. Figure 4 shows the Transmitter and Receiver layout.

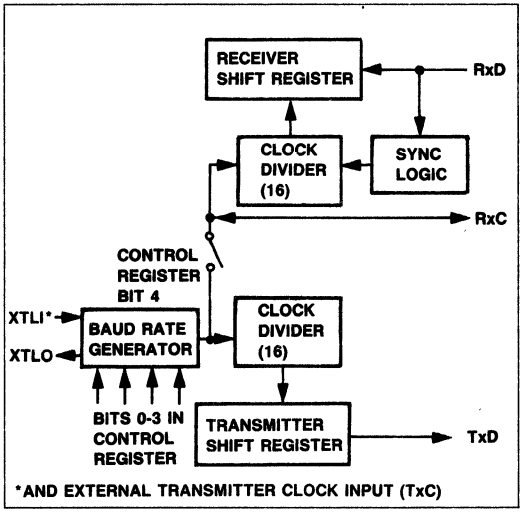


Figure 4. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of 1/16 the external receiver clock on pin RxC. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PNC1	PNC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode Bits 2 and 3 must also be zero for receiver echo mode, $\overline{RTS}$ will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	$\overline{RTS}$ = High, transmitter disabled*
0	1	$\overline{RTS}$ = Low, transmit interrupt enabled
1	0	$\overline{RTS}$ = Low, transmit interrupt disabled
1	1	$\overline{RTS}$ = Low, transmit interrupt disabled, transmit break on TxD**

Bit 1 Receiver Interrupt Request Disabled (IRD)

0	$\overline{IRQ}$ enabled (receiver)
1	$\overline{IRQ}$ disabled (receiver)

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{DTR}$ high)*
1	Data terminal ready ($\overline{DTR}$ low)

NOTE

*The transmitter is disabled immediately. The receiver is disabled but will first complete receiving a byte in process of being received.

**A "BREAK" is transmitted only after the end of a character stream. If the Transmitter Data Register contains a character, the "BREAK" is not transmitted.

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. $\overline{DTR}$ also enables and disables the transmitter and receiver.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver $\overline{DCD}$ and $\overline{DSR}$ from generating an interrupt when set to a 1. The Receiver $\overline{DCD}$ and $\overline{DSR}$ interrupts are enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 disables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
—	—	—	0	0	0	0	0	Program reset

6

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check $\overline{IRQ}$ (Bit 7) in the data read from the Status Register

   If not set, the interrupt source is not the ACIA.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modem "on-line") and they are unchanged, then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0–2) if the Receiver Data Register is full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

PROGRAM RESET OPERATION

A program Reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program Reset operates somewhat differently from the hardware Reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program Reset on internal registers.

2. The $\overline{DTR}$ line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.

4. $\overline{DCD}$ and $\overline{DSR}$ interrupts are disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.

5. Overrun cleared, if set.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output ($\overline{IRQ}$) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

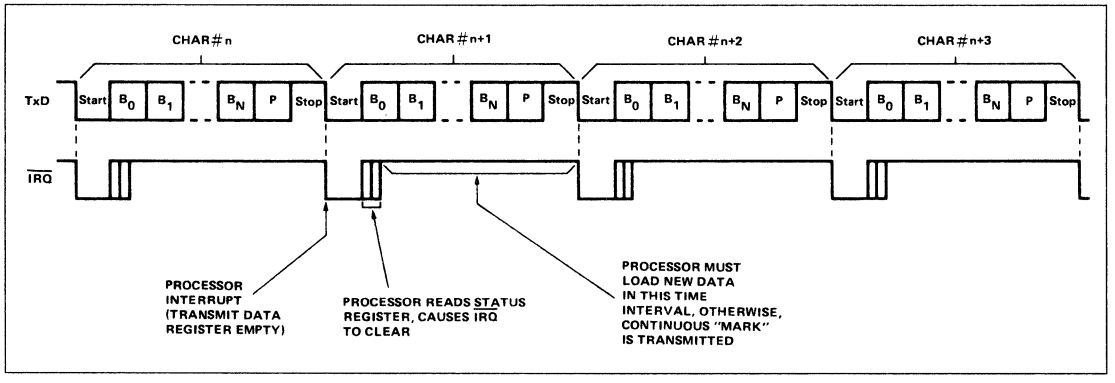


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{IRQ}$ when the ACIA has received a full data word. This occurs at about $^{9}/_{16}$ point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

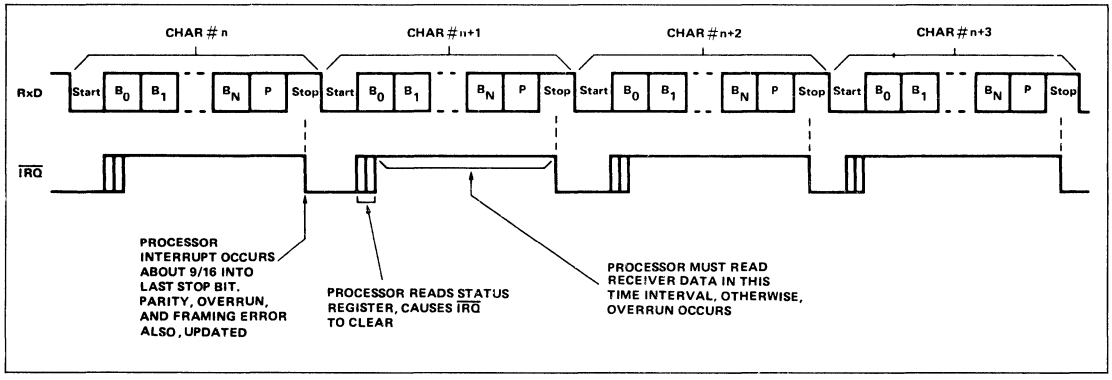


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{IRQ}$ interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

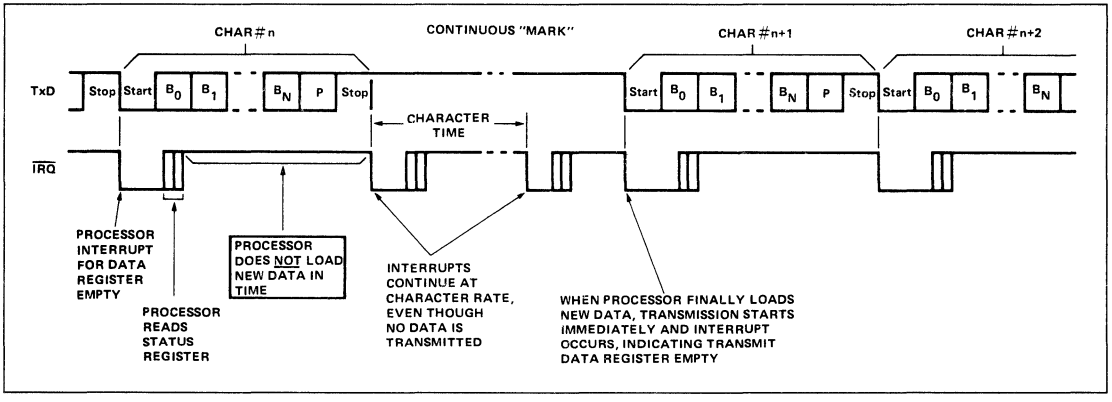


Figure 7. Transmit Data Register Not Loaded by Processor

Effect of $\overline{CTS}$ on Transmitter

$\overline{CTS}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line goes to the "MARK" condition after the entire last character (including parity and stop bit) has been transmitted, unless $\overline{CTS}$ goes high during the start bit. Then TxD goes immediately to a "MARK" condition. Bit 4 in the Status Register indicates that the Transmitter Data Register is not empty and $\overline{IRQ}$ is *not* asserted. $\overline{CTS}$ is a transmit control line only, and has no effect on the ACIA Receiver Operation. Figure 8 shows the timing relationship for this mode of operation.

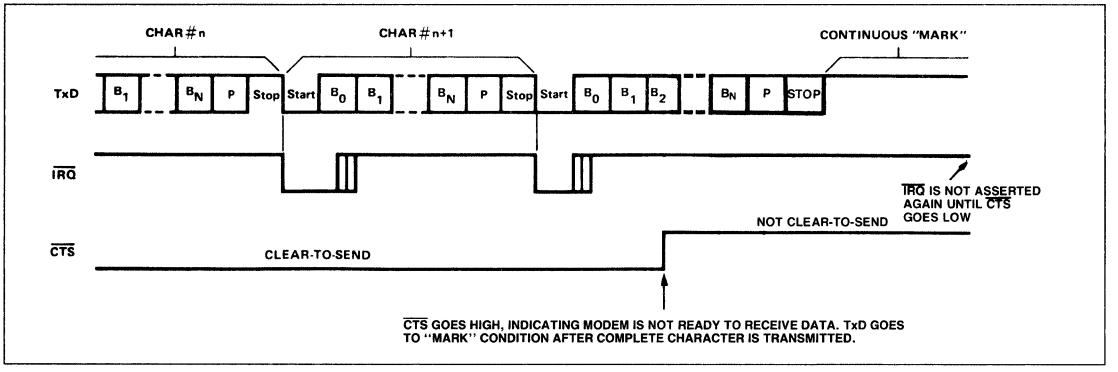


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver Data Register in the allocated time, when the next interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost. Figure 9 shows the timing relationship for this mode.

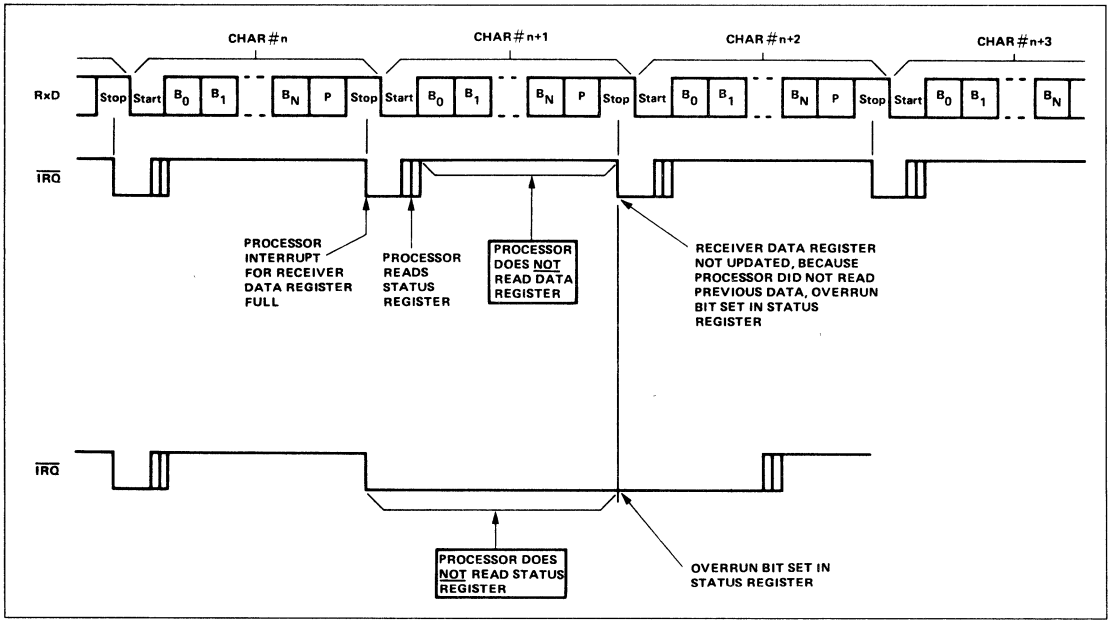


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time, as shown in Figure 10.

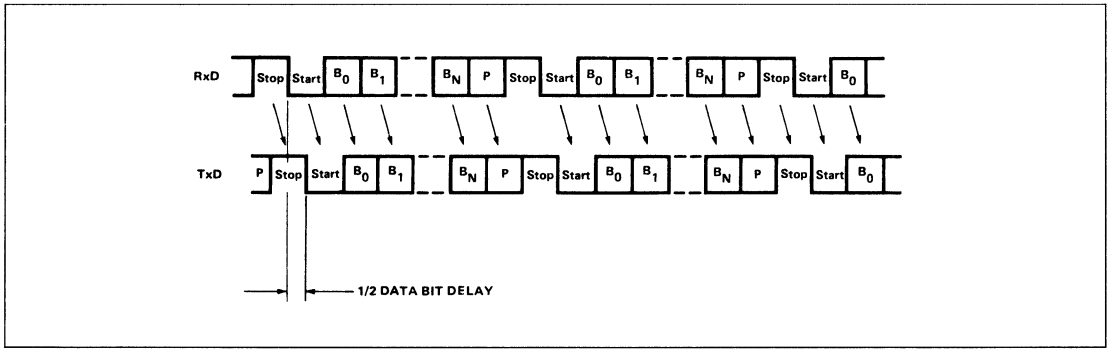


Figure 10. Echo Mode Timing

Effect of $\overline{CTS}$ on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by $\overline{CTS}$, however, the Transmitter is affected when $\overline{CTS}$ goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that the Receiver Data Register is full in response to an $\overline{IRQ}$, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

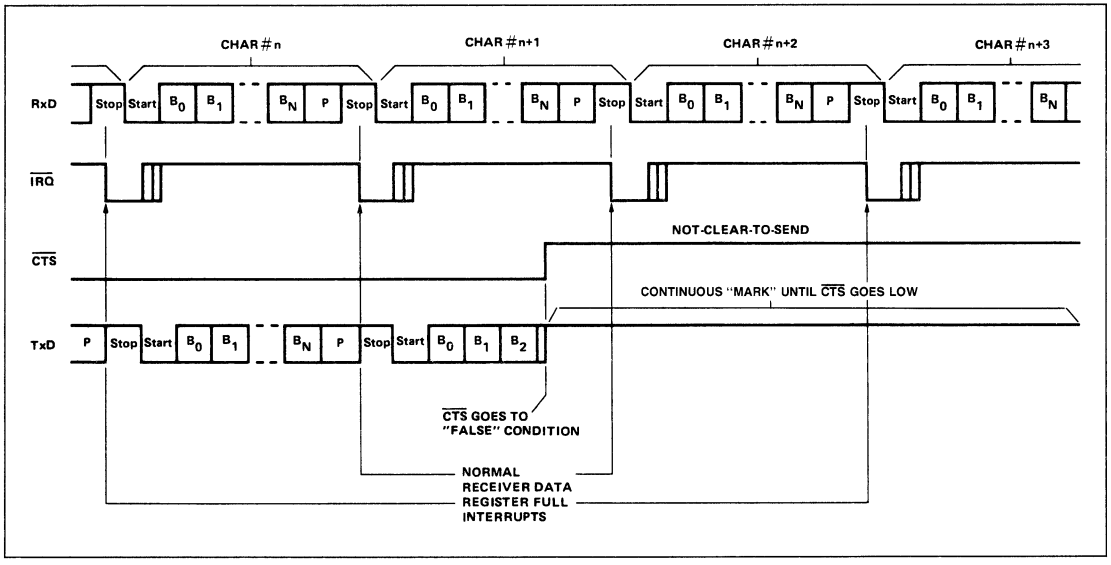


Figure 11. Effect of $\overline{CTS}$ on Echo Mode

Overrun in Echo Mode

If Overrun occurs in Echo Mode, the Receiver is affected the same way as a normal overrun in Receive Mode. For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

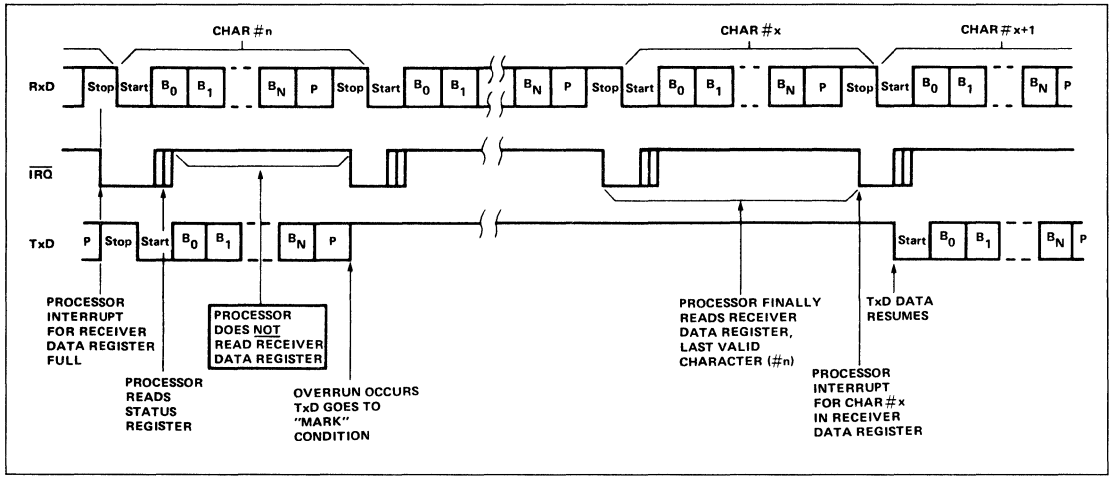


Figure 12. Overrun in Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 1 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to IRQ, generated by RDRF, the Status Register can also be checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

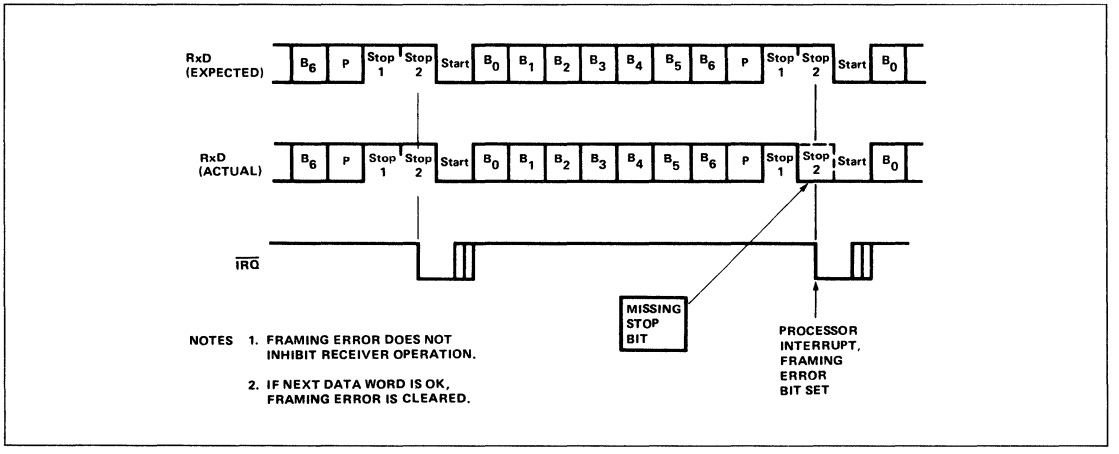


Figure 13. Framing Error

Effect of $\overline{DCD}$ on Receiver

$\overline{DCD}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts $\overline{IRQ}$ whenever $\overline{DCD}$ changes state and indicates this condition via bit 5 in the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the $\overline{DCD}$ input is high, the receiver is disabled (see Figure 14).

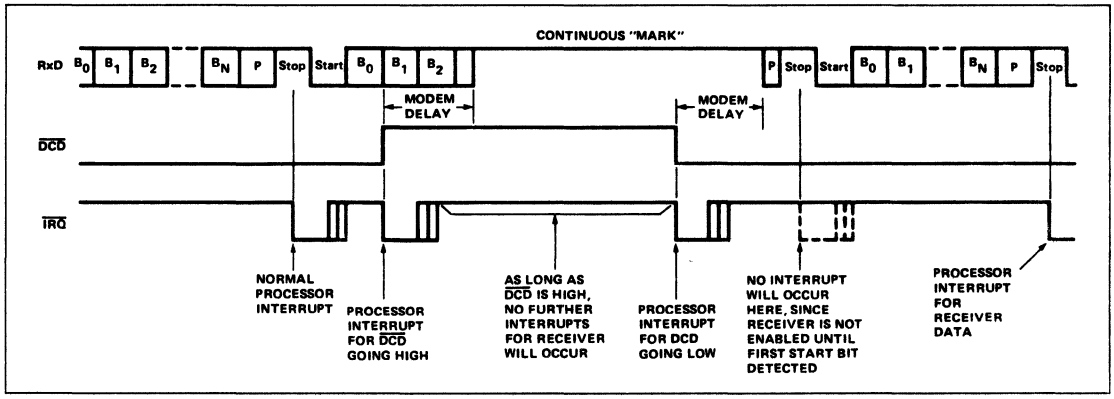


Figure 14. Effect of $\overline{DCD}$ on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{IRQ}$ asserted for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode.

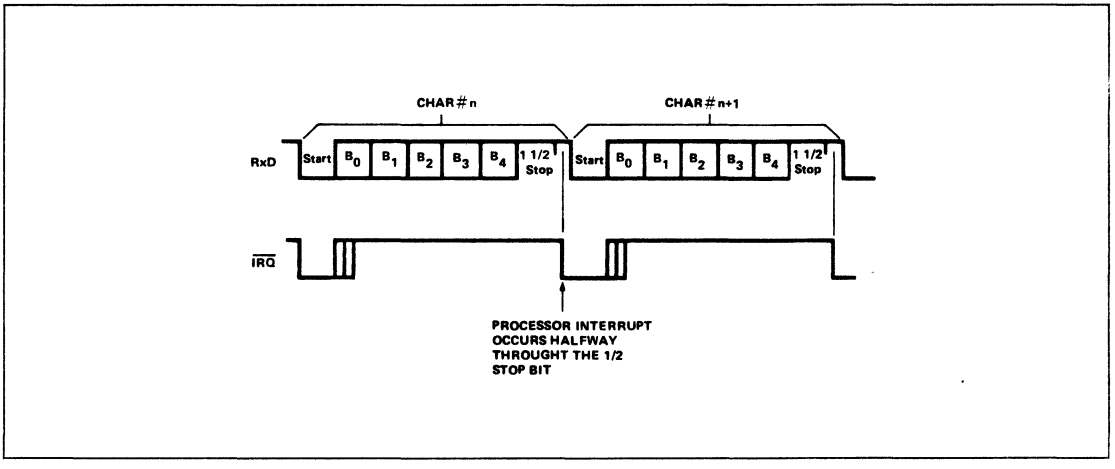


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

NOTE

If, while operating in the Transmit Continuous "BREAK" mode, the $\overline{CTS}$ should go to a high, the TxD will be overridden by the $\overline{CTS}$ and will go to continuous "MARK" at the beginning of the next character transmitted after the $\overline{CTS}$ goes high.

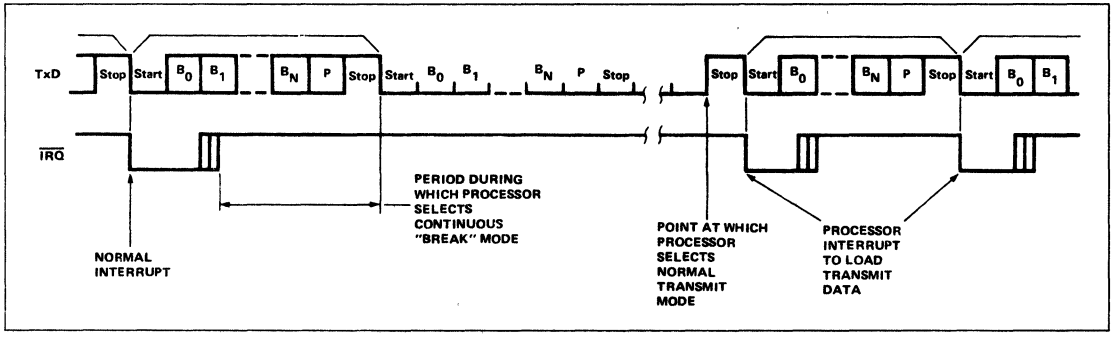


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17 shows the timing relationship for continuous "BREAK" characters.

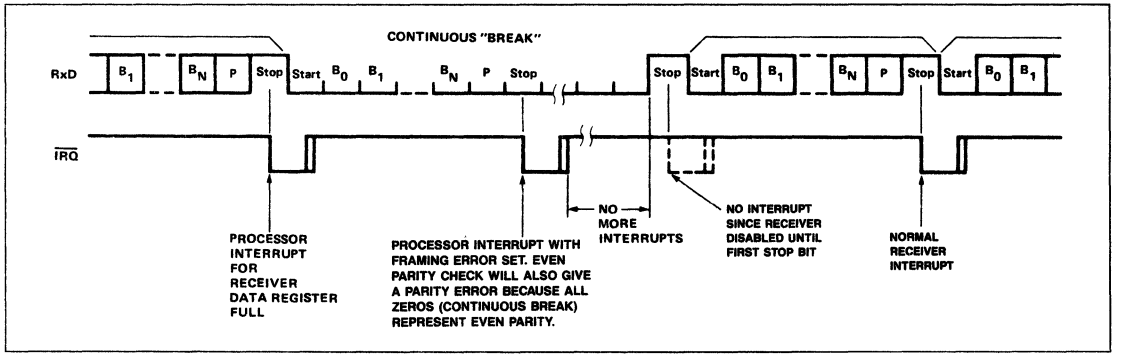


Figure 17. Receive Continuous "BREAK"

CRYSTAL/CLOCK CONSIDERATIONS

CLOCK OSCILLATOR

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 18.

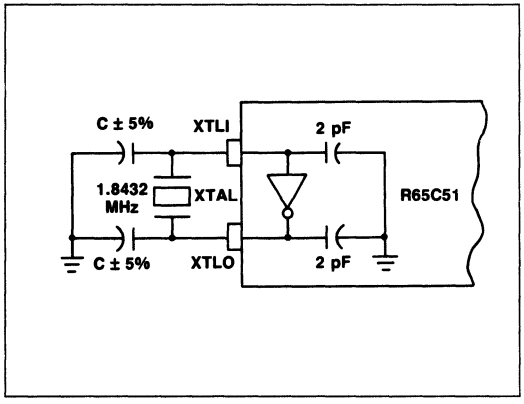


Figure 18. Internal Clock

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 2) = 2C_L \quad \text{or} \quad C = 2C_L - 2$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 13 pF for a 1.8432 MHz parallel resonant crystal, then

$$C = (2 \times 13) - 2 = 18 \text{ pF}$$

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(1.8432 \times 13)^2} \cong 3.3\text{K ohms}$$

EXTERNAL CLOCK MODES

The XTLI input may be used as an external clock input (Figure 19). For this implementation, a times 16 clock is input on XTLI and XTLO is left open.

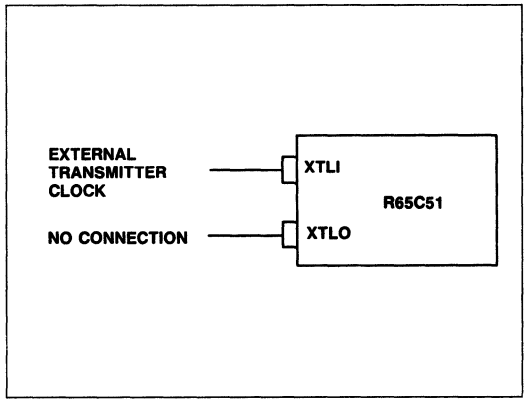


Figure 19. External Clock

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit generates appropriate divisors to produce standard baud rates when a 1.8432 MHz crystal is connected between XTLI and XTLO. Control Register bits 0–3 select the divisor for a particular baud rate as shown in Table 2.

Generating Non-Standard Baud Rates

By using a different crystal, non-standard baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (F)
3	2	1	0			
0	0	0	0	16	External Transmitter Clock Rate ÷ 16	External Transmitter Clock Rate ÷ 16
0	0	0	1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0	0	1	0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0	0	1	1	16,769	$\frac{1.8432 \times 10^6}{16,769} = 109.92$	$\frac{F}{16,769}$
0	1	0	0	13,704	$\frac{1.8432 \times 10^6}{13,704} = 134.51$	$\frac{F}{13,704}$
0	1	0	1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0	1	1	0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0	1	1	1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1	0	0	0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1,200$	$\frac{F}{1,536}$
1	0	0	1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1,800$	$\frac{F}{1,024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2,400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3,600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4,800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7,200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9,600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19,200$	$\frac{F}{96}$

DIAGNOSTIC LOOP-BACK OPERATING MODES

It may be desirable to include in the system a facility for local loop-back testing.

In local loop-back testing, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry. Figure 20 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables inputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective received inputs (i.e., TxD to RxD, $\overline{DTR}$ to $\overline{DCD}$, $\overline{RTS}$ to $\overline{CTS}$).

LLB may be tied to a peripheral control pin (from an R65C21 or R65C24, for example) to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

MISCELLANEOUS

1. If Echo Mode is selected, $\overline{RTS}$ goes low.
2. If Bit 0 of Command Register ($\overline{DTR}$) is 0 (disabled), then:
   a) All interrupts are disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter is disabled immediately.
   c) Receiver is disabled, but a character currently being received will be completed first.
3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.
4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.

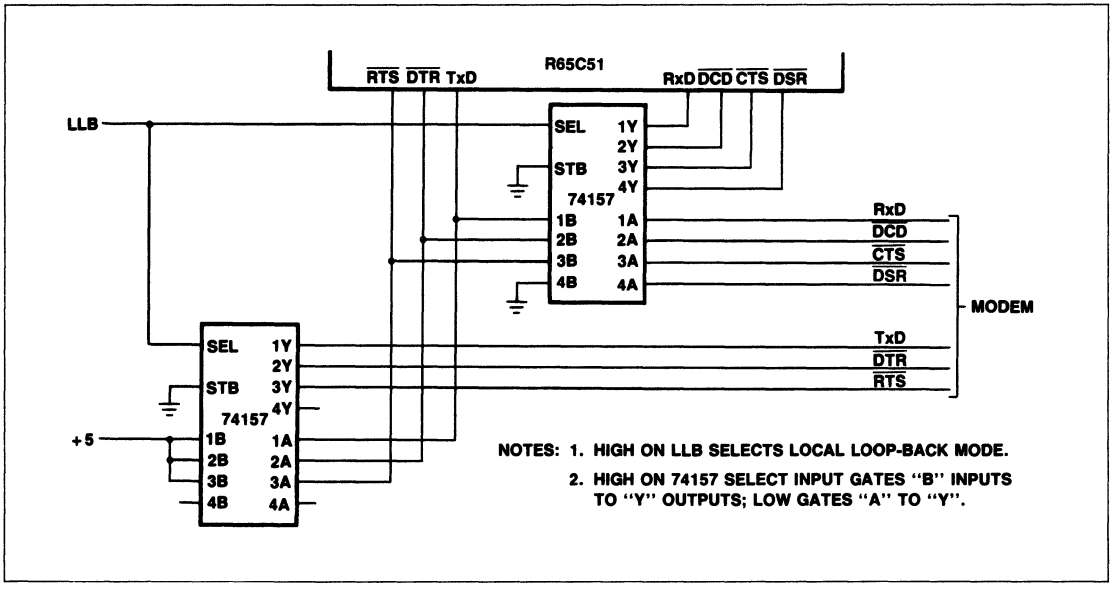


Figure 20. Loop-Back Circuit Schematic

6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit time to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no affect on transmitter operation. Data will continue to be sent, unless the processor forces the transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be tied to GND.

8. If TDRE is checked by polling (rather than by interrupt), a period of at least $\frac{1}{16}$ Baud clock should be allowed after loading Tx Data Buffer to ensure that TDRE is valid.

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{IRQ}$ generation are shown in Figures 21, 22 and 23, respectively. The corresponding timing characteristics are listed in Table 3.

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
$\overline{RTS}$, $\overline{DTR}$ Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns

Notes:
(t_R, t_F = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

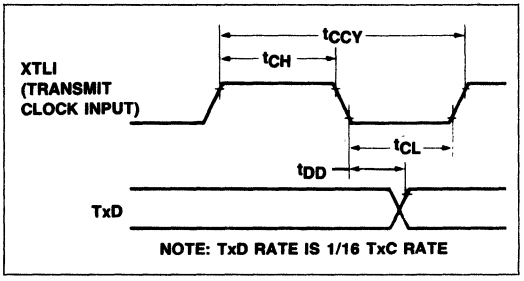


Figure 21. Transmit Timing with External Clock

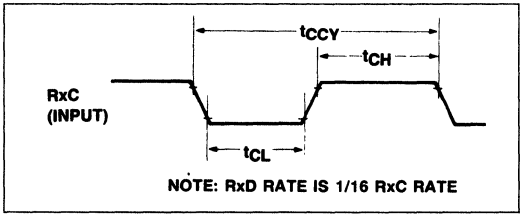


Figure 22. Receive External Clock Timing

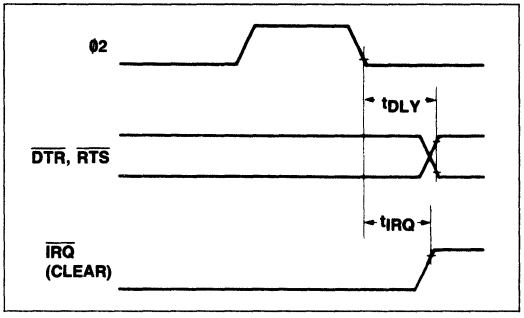


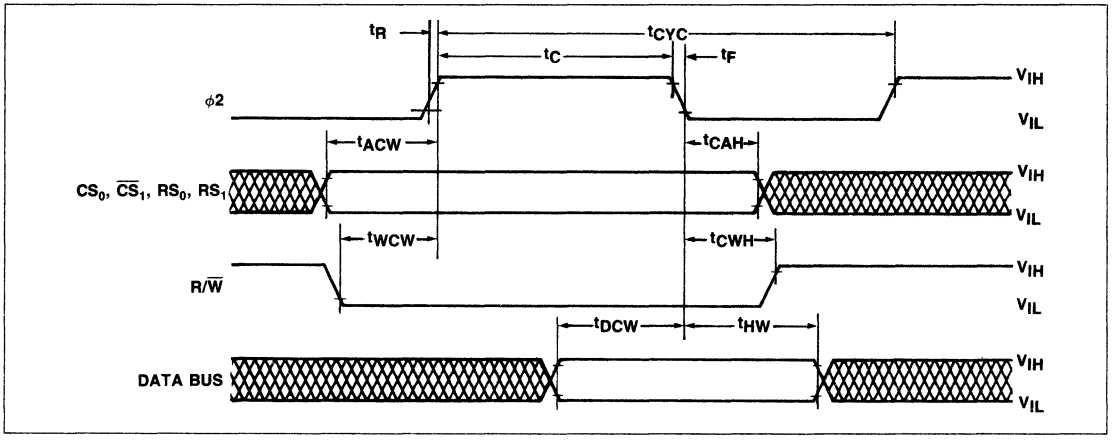
Figure 23. Interrupt and Output Timing

SWITCHING CHARACTERISTICS

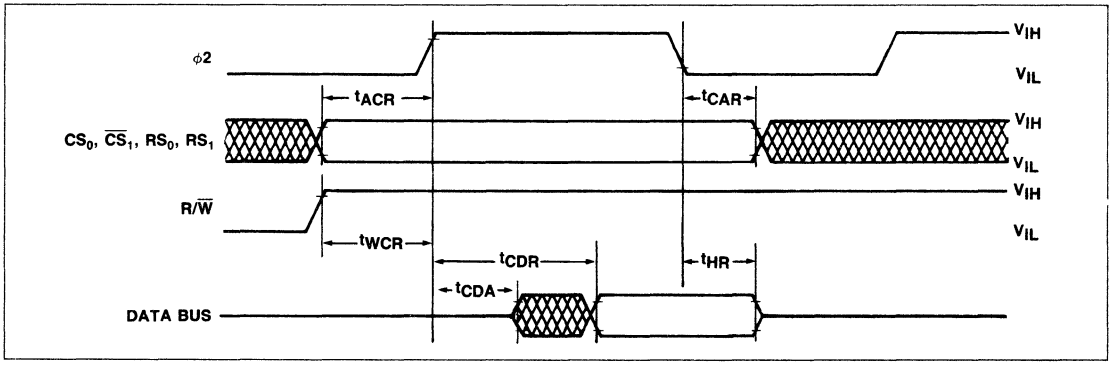
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Ø2 Cycle Time	t_{CYC}	1000	—	500	—	ns
Ø2 Pulse Width	t_C	400	—	200	—	ns
Address Set-Up Time	t_{ACW}, t_{ACR}	120	—	60	—	ns
Address Hold Time	t_{CAH}, t_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}, t_{WCR}	120	—	60	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	150	—	60	—	ns
Data Bus Hold Time	t_{HW}	20	—	10	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	170	ns
Read Hold Time	t_{HR}	20	—	10	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	20	—	ns

Notes:
1. t_R and t_F = 10 to 30 ns.
2. Timing measurements are referenced to/from a low of 0.8 volts and a high of 2.0 volts.



Write Timing Diagram



Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5Vdc ±5%
Temperature Range Commercial	T_A	T_L to T_H 0° to 70°C

ELECTRICAL CHARACTERISTICS

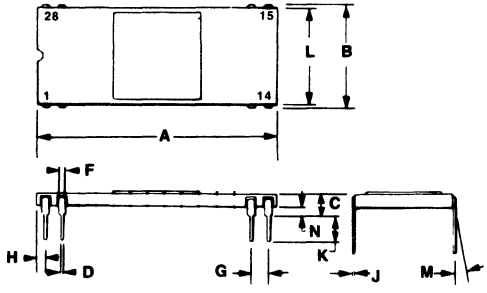
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTLI XTLI	V_{IH}	 2.0 2.8	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage Except XTLI XTLI	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current: Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current (Three State Off) D0–D7	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage: D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	V_{OH}	2.4	—	—	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage: D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing): D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	I_{OH}	−100	−400	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking): D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (off state): $\overline{IRQ}$	I_{OFF}	—	—	10	μA	V_{OUT} = 5.0V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance Ø2 All except Ø2	 C_{CLK} C_{IN}	 — —	 — —	 20 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and TA = 25°C.

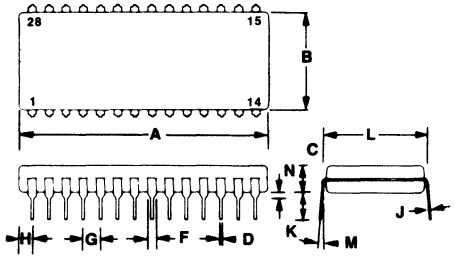
PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



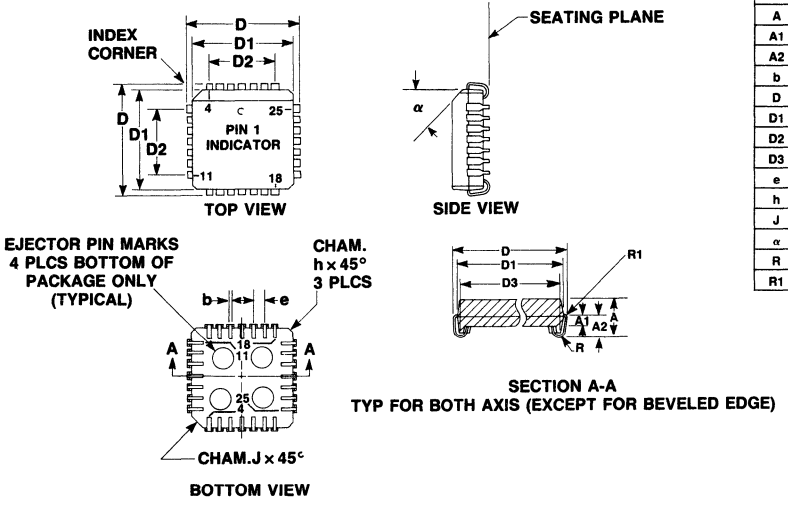
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35 05	36 07	1 380	1 420
B	15 11	15 88	0 595	0 625
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 27	0 030	0 050
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

28-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36 32	37 34	1 430	1 470
B	13 46	13 97	0 530	0 550
C	3 56	5 08	0 140	0 200
D	0 38	0 53	0 015	0 021
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 30	4 32	0 130	0 170
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

28-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4 14	4 39	0 163	0 173
A1	1 37	1 47	0 054	0 058
A2	2 31	2 46	0 091	0 097
b	0 457 TYP		0 018 TYP	
D	12 37	12 52	0 487	0 493
D1	11 43	11 53	0 450	0 454
D2	7 54	7 70	0 297	0 303
D3	10 67 REF		0 420 REF	
e	1 27 BSC		0 050 BSC	
h	1 15 TYP		0 045 TYP	
J	0 25 TYP		0 010 TYP	
α	45° TYP		45° TYP	
R	0 89 TYP		0 035 TYP	
R1	0 25 TYP		0 010 TYP	

6

Rockwell

R65C52
Dual Asynchronous Communications Interface Adapter (DACIA)

DESCRIPTION

The Rockwell CMOS R65C52 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled two-channel interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel.

Transmitter and Receiver bit rates may be controlled by an internal baud rate generator or external times 16 clocks. The baud rate generator accepts either a crystal or a clock input, and provides 15 programmable baud rates. When a 3.6864 MHz crystal is used, the baud rates range from 50 bps to 38,400 bps.

The DACIA may be programmed to transmit and receive frames having word lengths of 5, 6, 7 or 8 bits; even, odd, space, mark or no parity; and 1 or 2 stop bits.

A Compare Register, and the ability to detect address frames, facilitate address recognition in a multidrop mode.

FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 bps to 38,400 bps)
- Program-selectable internally or externally controlled receiver and transmitter bit rates
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Edge detect for $\overline{DCD}$, $\overline{DSR}$, and $\overline{CTS}$
- Program-selectable echo mode for each channel
- Compare Register
- Address/Data frame recognition
- 5.0 Vdc ±5% supply requirements
- 40-pin plastic or ceramic DIP or 44-pin PLCC
- Full TTL or CMOS input/output compatibility
- Compatible with R6500 and R65C00 microprocessors and R6500/* microcomputers

ORDERING INFORMATION

Part Number:
R65C52 ___

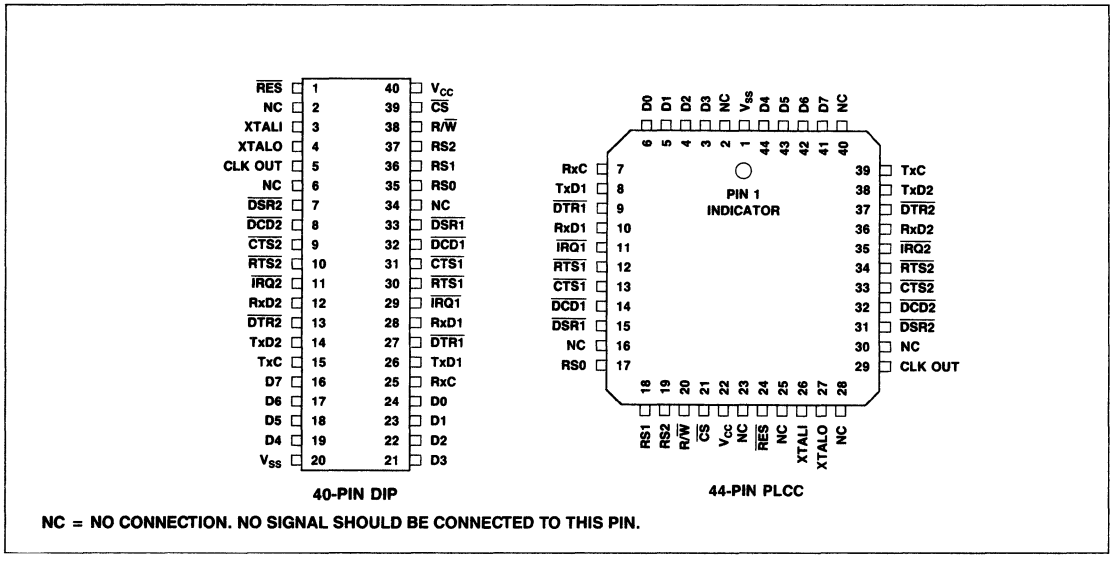
Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

Frequency Range:
1 = 1 MHz
2 = 2 MHz
3 = 3 MHz

Package
C = 40-Pin Ceramic DIP
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

The DACIA is available in a 40-pin DIP or a 44-pin PLCC. Figure 1 shows the pin assignments for each package. The DACIA interface signals are shown in Figure 2. Table 1 contains a description of each signal.



NC = NO CONNECTION. NO SIGNAL SHOULD BE CONNECTED TO THIS PIN.

Figure 1. R65C52 Pin Assignments

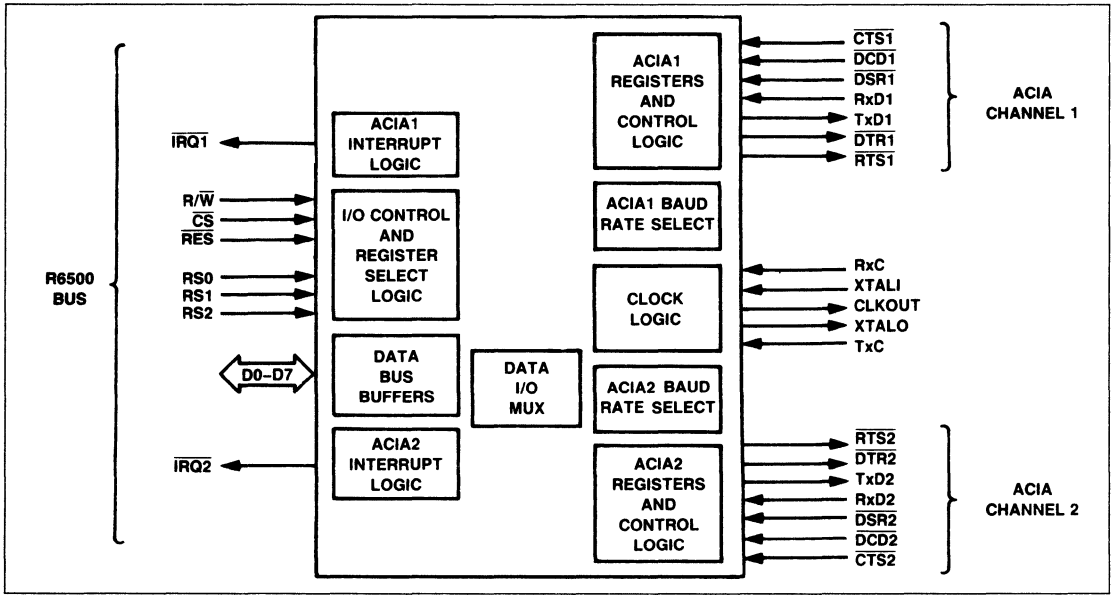


Figure 2. R65C52 DACIA Interface Signals

Table 1. DACIA Interface Signal Definitions

Signal	Pin No. DIP	Pin No. PLCC	I/O	Name/Description
Host Interface				
$\overline{RES}$	1	24	I	**Reset.** Active low input controlling the reset function. This signal must be driven low for a minimum of 4 μs for a valid reset to occur. It is driven high during normal operation.
R/$\overline{W}$	38	20	I	**Read/Write.** Input controlling the direction of data transfer. It is driven low during write cycles, and is driven high at all other times.
$\overline{CS}$	39	21	I	**Chip Select.** Active low input enabling data transfers between the host CPU and the DACIA. The DACIA latches register selects and the R/$\overline{W}$ input on the falling edge of $\overline{CS}$. It latches input data on the rising edge of $\overline{CS}$.
RS0–RS3	35–37	17–19	I	**Register Select.** Three inputs controlling access to the DACIA internal registers. Table 3 lists the coding for each register.
D0–D3 D4–D7	24–21 19–16	6–3 44–41	I/O	**Data Bus.** Eight bidirectional lines used to transfer data between the host and the DACIA. These lines output data during READ cycles when $\overline{CS}$ is low. At all other times, they are in the high impedance state.
$\overline{IRQ1}$ $\overline{IRQ2}$	29 11	11 35	O	**Interrupt Request.** Two active low, open-drain outputs from the interrupt control logic. These outputs are normally high. An $\overline{IRQ}$ line goes low when one of the flags of the associated ISR is set if the corresponding enable bit is set in the IER.
Clock Interface				
XTALI XTALO	3 4	26 27	I O	**Crystal Input/Output.** One input and one output through which the reference signal for the internal clock oscillator is supplied. A parallel resonant crystal may be connected across the pins or a clock may be input at XTALI. When a clock is used, XTALO must be left open.
CLK OUT	5	29	O	**Clock Out.** A buffered output from the internal clock oscillator which is in phase with XTALI. This output may be used to drive the XTALI input of another DACIA. Therefore, several DACIA chips may be driven with one crystal.
RxC	25	7	I	**Receiver Clock.** Input for external 16x receiver clock.
TxC	15	39	I	**Transmitter Clock.** Input for external 16x transmitter clock.
Serial Channel Interface				
$\overline{DTR1}$ $\overline{DTR2}$	27 13	9 37	O	**Data Terminal Ready.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated Format Register (FR) high or low. The state of each $\overline{DTR}$ line is reflected by the $\overline{DTR}$ LVL bit in the associated Control Status Register (CSR).
$\overline{DSR1}$ $\overline{DSR2}$	33 7	15 31	I	**Data Set Ready.** Two general purpose inputs. An active transition sets the $\overline{DSR}$T bit in the Interrupt Status Register (ISR). The $\overline{DSR}$ LVL bit in the associated CSR reflects the current state of a $\overline{DSR}$ line.
$\overline{RTS1}$ $\overline{RTS2}$	30 10	12 34	O	**Request To Send.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated FR high or low. The state of an $\overline{RTS}$ line is reflected by the $\overline{RTS}$ LVL bit in the associated CSR.
$\overline{CTS1}$ $\overline{CTS2}$	31 9	13 33	I	**Clear To Send.** The $\overline{CTS}$ control line inputs allow handshaking by the transmitters. When $\overline{CTS}$ is low, the data is transmitted continuously. When $\overline{CTS}$ is high, the Transmit Data Register Empty bit (TDRE) in the associated ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on a $\overline{CTS}$ line sets the $\overline{CTS}$T bit in the appropriate ISR. The $\overline{CTS}$ LVL bit in the associated CSR reflects the current state of $\overline{CTS}$.
TxD1 TxD2	26 14	8 38	O	**Transmit Data.** The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator or external clock.
$\overline{DCD1}$ $\overline{DCD2}$	32 8	14 32	I	**Data Carrier Detect.** Two general purpose inputs. An active transition sets the $\overline{DCD}$T bit in the appropriate ISR. The $\overline{DCD}$ LVL bit in the associated CSR reflects the current state of a $\overline{DCD}$ line.
RxD1 RxD2	28 12	10 36	I	**Receive Data.** The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator or external clock.
Power				
VCC	40	22	I	**DC Power Input.** 5.0V ± 5%.
VSS	20	1	I	**Power and Signal Reference.**

FUNCTIONAL DESCRIPTION

Figure 3 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

RESET LOGIC

The Reset Logic sets various internal registers, status bits and control lines to a known state. The $\overline{RES}$ input must be driven low for a minimum of 4 μs for a valid reset to occur. At this time, the IERs are set to $80, the RDRs and ACRs are cleared, and the compare mode is disabled. Also, the $\overline{DTR}$ and $\overline{RTS}$ outputs are driven high and the $\overline{CTS}$, $\overline{DCD}$ and $\overline{DSR}$ transition detect flags are cleared. No other bits are affected.

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the data lines and the internal data bus. The state of the Data Bus Buffer is controlled by the I/O Control Logic and the Interrupt Logic. Table 2 summarizes the Data Bus Buffer states.

I/O CONTROL LOGIC

The I/O Control Logic controls data transfers between the Internal Registers and the Data Bus Buffer. Internal Register selection is determined by the Register Select inputs as shown in Table 3. When R/$\overline{W}$ is high and $\overline{CS}$ is low, data from the selected register is transferred from the internal data bus to the data lines. When $\overline{CS}$ is high, the DACIA is deselected and the data lines are tri-stated.

INTERRUPT LOGIC

The interrupt logic causes the $\overline{IRQ}$ lines ($\overline{IRQ1}$ or $\overline{IRQ2}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. An $\overline{IRQ}$ will be asserted *on the transition* of one of the flags in an ISR from 0 to 1 if the corresponding bit in the associated IER is set. The $\overline{IRQ}$ line is negated when the ISR is read or when the interrupting condition is cleared. CAUTION: When the interrupt is generated by TDRE, 1/16 of a bit time must elapse before $\overline{IRQ}$ can be cleared by reading the ISR.

CLOCK OSCILLATOR LOGIC

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock.

The baud rate generator may be disabled by connecting XTALI to ground and leaving XTALO open. When this is done, a transmitter times 16 clock must be input at TxC, a receiver times 16 clock must be input at RxC and the Control Registers must be programmed to select TxC and RxC clocks.

Table 2. Data Bus Buffer Summary

Control Signals R/$\overline{W}$	Control Signals $\overline{CS}$	Data Bus Buffer State
L	L	Write Mode — Tri-State
H	L	Read Mode — Output Data
X	H	Deselected — Tri State

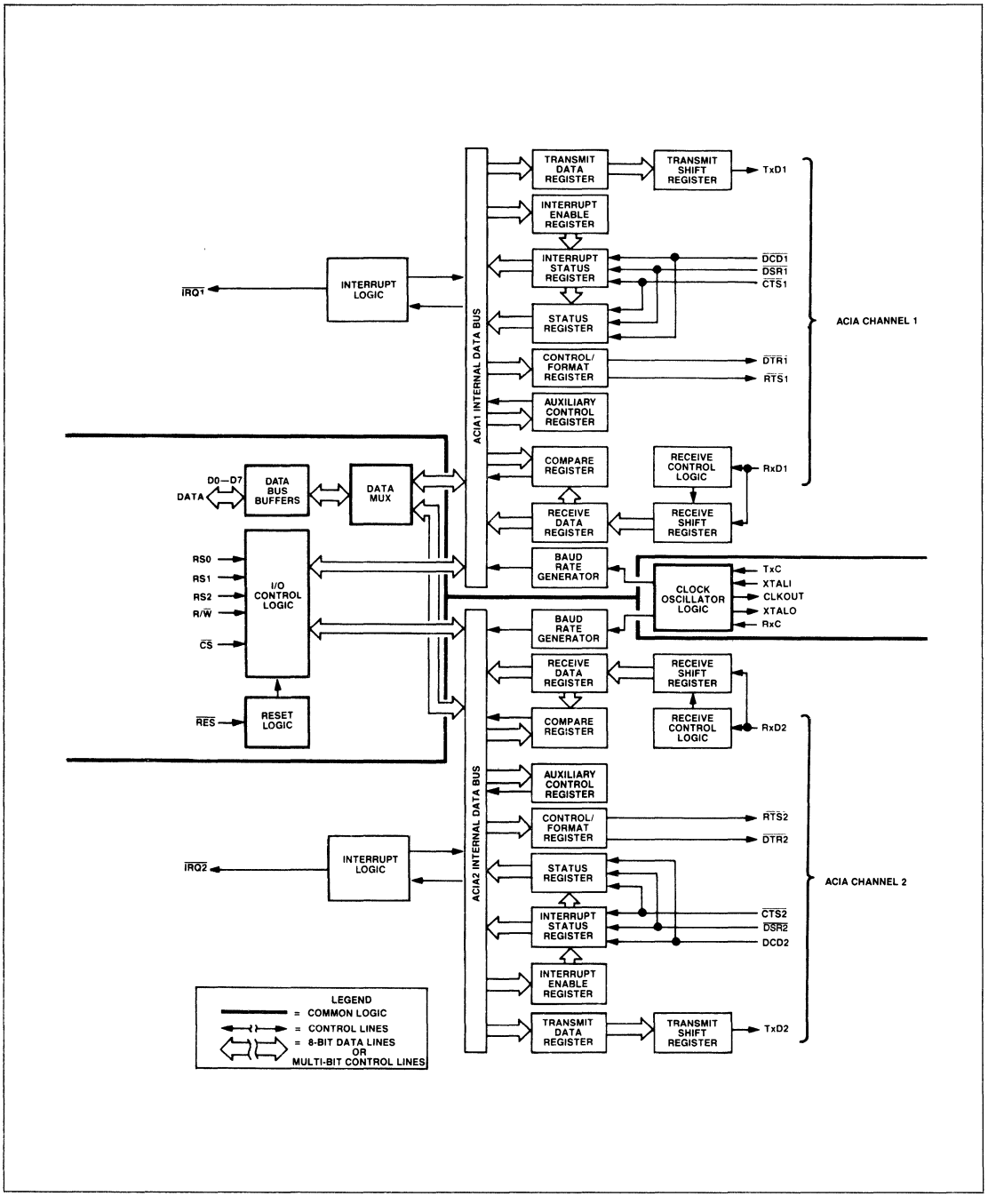


Figure 3. DACIA Block Diagram

Table 3. DACIA Register Selection

Register Select Lines				Register Accessed			
				Write		Read	
HEX	RS2	RS1	RS0	Symbol	Name	Symbol	Name
0	L	L	L	IER1	Interrupt Enable Register 1	ISR1	Interrupt Status Register 1
1	L	L	H	CR1	Control Register 1[1]	CSR1	Control Status Register 1
				FR1	Format Register 1[2]		
2	L	H	L	CDR1	Compare Data Register 1[3]		Not Used
				ACR1	Auxiliary Control Register 1[4]		
3	L	H	H	TDR1	Transmit Data Register 1	RDR1	Receive Data Register 1
4	H	L	L	IER2	Interrupt Enable Register 2	ISR2	Interrupt Status Register 2
5	H	L	H	CR2	Control Register 2[1]	CSR2	Control Status Register 2
				FR2	Format Register 2[2]		
6	H	H	L	CDR2	Compare Data Register 2[3]		Not Used
				ACR2	Auxiliary Control Register 2[4]		
7	H	H	H	TDR2	Transmit Data Register 2	RDR2	Receive Data Register 2

Notes:
1. D7 must be set low to write to the Control Registers.
2. D7 must be set high to write to the Format Registers.
3 Control Register bit 6 must be set to 0 to access the Compare Register.
4. Control Register bit 6 must be set to 1 to access the Auxiliary Control Register

SERIAL DATA CHANNELS

Two independent serial data channels are available for the full duplex (simultaneous transmit and receive) transfer of asynchronous frames. Separate internal registers are provided for each channel for the selection of frame parameters (number of bits per character, parity options, etc.), status flags, interrupt control and handshake. The asynchronous frame format is shown in Figure 4.

Transmit data from the host system is loaded into the Transmit Data Register. From there, it is transferred to the Transmit Shift Register where it is shifted, LSB first, onto the TxD line. All transmissions begin with a start bit and end with the user selected number of stop bits. A parity bit is transmitted before the stop bit(s) if parity is enabled.

Receive data is shifted into the Receive Shift Register from the associated RxD line. Start and stop bits are stripped from the frame and the data is transferred to the Receive Data Register. Parity bits may be discarded or stored in the ISR.

Five I/O lines are provided for each channel for handshake with the data communications equipment (DCE). Four of these signals ($\overline{RTS}$, $\overline{DTR}$, $\overline{DSR}$ and $\overline{DCD}$) are general purpose inputs or outputs. The fifth signal, $\overline{CTS}$, enables/disables the transmitter. When $\overline{CTS}$ is high and the Transmit Shift Register is empty, the transmitter (except for Echo Mode) is inhibited. When $\overline{CTS}$ is low, the transmitter is enabled.

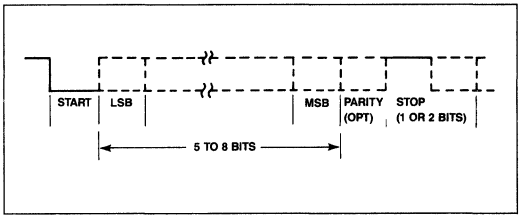


Figure 4. Asynchronous Frame Format

INTERNAL REGISTERS

The DACIA contains ten control registers and four status registers in addition to the transmit and receive registers. The Control Registers provide for control of frame parameters, baud rate, interrupt generation, handshake lines, transmission and reception. The status registers provide status information on transmit and receive registers, error conditions and interrupt sources. Table 4 summarizes the bit definitions of these registers. A detailed description follows.

Table 4. Register Formats

Register Select (Hex)	Register	R/$\overline{W}$	Bit 7	6	5	4	3	2	1	0	Reset Value 76543210
0 4	ISR1 ISR2	R	ANY BIT SET	TDRE	$\overline{CTS}$T	$\overline{DCD}$T	$\overline{DSR}$T	PAR	F/O/B	RDRF	1 - 00000 -
0 4	IER1 IER2	W	CLR/SET BITS	TDRE IE	$\overline{CTS}$T IE	$\overline{DCD}$T IE	$\overline{DSR}$T IE	PAR IE	F/O/B IE	RDRF IE	- 0000000
1 5	CSR1 CSR2	R	FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL	1 - - - - 011
1 5	CR1 CR2	W	0	CDR/ ACR	STOP BITS	ECHO	BIT RATE SEL				0 - - - - - - -
1 5	FR1 FR2	W	1	DATA BITS		PAR SEL		PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL	1 - - - - - - -
2 6	CDR1 CDR2	W (CR6 = 0)	COMPARE DATA								- - - - - - - -
2 6	ACR1 ACR2	W (CR6 = 1)	UNUSED						TRNS BRK	PAR ERR/ST	- - - - - - 00
3 7	RDR1 RDR2	R	RECEIVE DATA REGISTER								00000000
3 7	TDR1 TDR2	W	TRANSMIT DATA REGISTER								- - - - - - - -

INTERRUPT STATUS REGISTERS (ISR1, ISR2)

The Interrupt Status Registers are read-only registers indicating the status of each interrupt source. Bits 6 through 0 are set when the indicated $\overline{IRQ}$ condition has occurred. Bit 7 is set to a 1 when any $\overline{IRQ}$ source bit is set, or if Echo Mode is disabled, when $\overline{CTS}$ is high.

7	6	5	4	3	2	1	0
ANY BIT SET	TDRE	$\overline{CTST}$	$\overline{DCDT}$	$\overline{DSRT}$	PAR	F/O/B	RDRF

Address = 0,4 Reset Value = 1 - 00000 -

Bit 7 **Any Bit Set**
- 1 Any bit (6 through 0) has been set to a 1 or $\overline{CTS}$ is high with echo disabled
- 0 No bits have been set to a 1 or echo is enabled

Bit 6 **Transmit Data Register Empty (TDRE)**
- 1 Transmit Data Register is empty and $\overline{CTS}$ is low
- 0 Transmit Data Register is full or $\overline{CTS}$ is high

Bit 5 **Transition On $\overline{CTS}$ Line ($\overline{CTST}$)**
- 1 A positive or negative transition has occurred on $\overline{CTS}$
- 0 No transition has occurred on $\overline{CTS}$, or ISR has been Read

Bit 4 **Transition On $\overline{DCD}$ Line ($\overline{DCDT}$)**
- 1 A positive or negative transition has occurred on $\overline{DCD}$
- 0 No transition has occurred on $\overline{DCD}$, or ISR has been Read

Bit 3 **Transition On $\overline{DSR}$ Line ($\overline{DSRT}$)**
- 1 A positive or negative transition has occurred on $\overline{DSR}$
- 0 No transition has occurred on $\overline{DSR}$, or ISR has been Read

Bit 2 **Parity Status (PAR)**

ACR bit 0 = 0
- 1 A parity error has occurred in received data
- 0 No parity error has occurred, or the Receive Data Register (RDR) has been Read

ACR bit 0 = 1
- 1 Parity bit = 1
- 0 Parity bit = 0

Bit 1 **Frame Error, Overrun, Break**
- 1 A framing error, receive overrun, or receive break has occurred or has been detected
- 0 No error, overrun, break has occurred or RDR has been Read

Bit 0 **Receive Data Register Full (RDRF)**
- 1 Receive Data Register is full
- 0 Receive Data Register is empty

INTERRUPT ENABLE REGISTERS (IER1, IER2)

The Interrupt Enable Registers are write-only registers that enable/disable the $\overline{IRQ}$ sources. $\overline{IRQ}$ sources are enabled by writing to an IER with bit 7 set to a 1 and the bit for every $\overline{IRQ}$ source to be enabled set to a 1. $\overline{IRQ}$ sources are disabled by writing to an IER with bit 7 reset to a 0 and the bit for every source to be disabled set to a 1. Any source bit reset to 0 is unaffected and remains in its original state. Thus, writing $7F to an IER disables all of that channel's interrupts and writing an $FF to an IER enables all of that channel's interrupts.

7	6	5	4	3	2	1	0
SET BITS	TDRE IE	$\overline{CTST}$ IE	$\overline{DCDT}$ IE	$\overline{DSRT}$ IE	PAR IE	F/O/B IE	RDRF IE

Address = 0,4 Reset Value = - 0000000

Bit 7 **Enable/Disable**
- 1 Enable selected IRQ source
- 0 Disable selected IRQ source

Bits 0-6
- 1 Select for enable/disable
- 0 No change

CONTROL STATUS REGISTERS (CSR1, CSR2)

The Control Status Registers are read-only registers that provide I/O status and error condition information. A CSR is normally read after an $\overline{IRQ}$ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL

Address = 1,5 Reset Value = 1 - - - - 011

Bit 7 **Framing Error (FE)**
- 1 A framing error occurred in receive data
- 0 No framing error occurred, or the RDR was read

Bit 6 **Transmitter Underrun (TUR)**
- 1 Transmit Shift Register is empty and TDRE is set
- 0 Transmitter Shift Register is not empty

Bit 5 **$\overline{CTS}$ Level ($\overline{CTS}$ LVL)**
- 1 $\overline{CTS}$ line is high
- 0 $\overline{CTS}$ line is low

Bit 4 **$\overline{DCD}$ Level ($\overline{DCD}$ LVL)**
- 1 $\overline{DCD}$ line is high
- 0 $\overline{DCD}$ line is low

Bit 3 **$\overline{DSR}$ Level ($\overline{DSR}$ LVL)**
- 1 $\overline{DSR}$ line is high
- 0 $\overline{DSR}$ line is low

Bit 2 **Receive Break (BRK)**
- 1 A Receive Break has occurred
- 0 No Receive Break occurred, or RDR was read

Bit 1 **$\overline{DTR}$ Level ($\overline{DTR}$ LVL)**
- 1 $\overline{DTR}$ line is high
- 0 $\overline{DTR}$ line is low

Bit 0 **$\overline{RTS}$ Level ($\overline{RTS}$ LVL)**
- 1 $\overline{RTS}$ line is high
- 0 $\overline{RTS}$ line is low

CONTROL REGISTERS (CR1, CR2)

The Control Registers are write-only registers. They control access to the Auxiliary Control Register and the Compare Data Register. They select the number of stop bits, control Echo Mode, and select the data rate.

(Accessed when Bit 7 = 0)

7	6	5	4	3 2 1 0
0	CDR/ACR	STOP BITS	ECHO	BAUD RATE SEL

Address = 1,5 Reset Value = 0 - - - - - - -

Bit 7 **Control or Format Register**
0 Access Control Register

Bit 6 **CDR/ACR**
1 Access the Auxiliary Control Register (ACR)
0 Access the Compare Data Register (CDR)

Bit 5 **Number of Stop Bits Per Character**
1 Two stop bits
0 One stop bit

Bit 4 **Echo Mode Selection**
1 Echo Mode enabled
0 Echo Mode disabled

Bits 3-0				Baud Rate Selection
3	2	1	0	(bits per second with 3.6864 MHz crystal)
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External TxC and RxC X16 Clocks

FORMAT REGISTERS (FR1, FR2)

The Format Registers are write-only registers. They select the number of data bits per character and parity generation/checking options. They also control $\overline{RTS}$ and $\overline{DTR}$.

(Accessed when Bit 7 = 1)

7	6 5	4 3	2	1	0
1	DATA BITS	PAR SEL	PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL

Address = 1,5 Reset Value = 1 - - - - - - -

Bit 7 **Control or Format Register**
1 Access Format Register

Bits 6-5		Number of Data Bits Per Character
6	5	
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3		Parity Mode Selection
4	3	
0	0	Odd Parity
0	1	Even Parity
1	0	Mark in Parity bit
1	1	Space in Parity bit

Bit 2 **Parity Enable**
1 Parity as specified by bits 4-3
0 No Parity

Bit 1 **$\overline{DTR}$ Control**
1 Set $\overline{DTR}$ high
0 Set $\overline{DTR}$ low

Bit 0 **$\overline{RTS}$ Control**
1 Set $\overline{RTS}$ high
0 Set $\overline{RTS}$ low

COMPARE DATA REGISTERS (CDR1, CDR2)

The Compare Data Registers are write-only registers which can be accessed when CR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

(Control Register bit 6 = 0)

7	6	5	4	3	2	1	0
COMPARE DATA							

Address = 2,6 Reset Value = --------

AUXILIARY CONTROL REGISTERS (ACR1, ACR2)

The Auxiliary Control Registers are write-only registers. Bits 7-2 are unused. Bit 1 causes the transmitter to transmit a BREAK. Bit 0 determines whether parity error or the parity bit is displayed in ISR bit 2.

(Control Register bit 6 = 1)

7	6	5	4	3	2	1	0
NOT USED						TRNS BRK	PAR ERR/ST

Address = 2,6 Reset Value = ------00

Bits 7-2 **Not Used**

Bit 1 **Transmit Break (TRNS BRK)**
1 Transmit continuous Break
0 Normal transmission

Bit 0 **Parity Error/State (PAR ERR/ST)**
1 Send value of parity bit to ISR bit 2 (Address Recognition mode)
0 Send Parity Error status to ISR bit 2

RECEIVE DATA REGISTERS (RDR1, RDR2)

The Receive Data Registers are read-only registers which are loaded with the received data character of each frame. Start bits, stop bits and parity bits are stripped off of incoming frames before the data is transferred from the Receive Shift Register to the Receive Data Register. For characters of less than eight bits, the unused bits are the high order bits which are set to 0.

MSB **LSB**

7	6	5	4	3	2	1	0
RECEIVE DATA							

Address = 3,7 Reset Value = 00000000

TRANSMIT DATA REGISTERS (TDR1, TDR2)

The Transmit Data Registers are write-only registers which are loaded from the CPU with data to be transmitted. For data characters of less than eight bits, the unused bits are the high order bits which are "don't care".

MSB **LSB**

7	6	5	4	3	2	1	0
TRANSMIT DATA							

Address = 3,7 Reset Value = --------

OPERATION

TERMINATION OF UNUSED INPUTS

Noise on floating inputs can affect chip operation. All unused inputs must be terminated. If the baud rate generator is bypassed, XTALI must be connected to ground (XTALO is an output and must be left open). If the external clock mode is not used, RxC and TxC may be tied either to +5V or to ground. If the handshake inputs are not needed, the $\overline{CTS}$ inputs should be tied low to enable the transmitters. The $\overline{DCD}$ and $\overline{DSR}$ inputs may either be tied high or low.

RESET INITIALIZATION

During power on initialization, all readable registers should be read to assure that the status registers are initialized. Specifically, the RDRF bit of the Interrupt Status Registers is not initialized by reset. The Receiver Data Registers must be read to clear this bit.

TDRE $\overline{IRQ}$ is generated only on the transition of the corresponding TDR from full to empty. Initialization software must account for this occurrence.

BAUD RATE CLOCK OPTIONS

The receiver and transmitter clocks may be supplied either by the internal Baud Rate Generator or by user supplied external clocks. Both channels may use the same clock source or one may use the Baud Rate Generator and the other channel external clocks. If both channels use the Baud Rate Generator, each channel may have a different bit rate. The options are shown in Figure 5.

An internal clock oscillator supplies the time base for the Baud Rate Generator. The oscillator can be driven by a crystal or an external clock.

If the on-chip oscillator is driven by a crystal, a parallel resonant crystal is connected between the XTALI and XTALO pins. The equivalent oscillator circuit is shown in Figure 6.

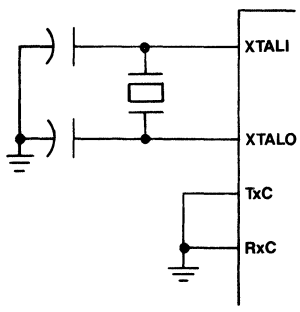
A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

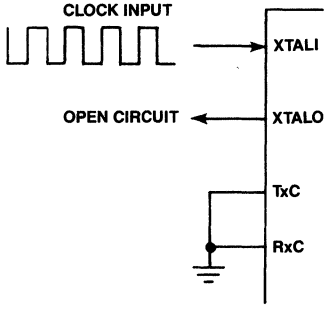
$$(C + 2) = 2C_L \quad \text{or} \quad C = 2C_L - 2$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

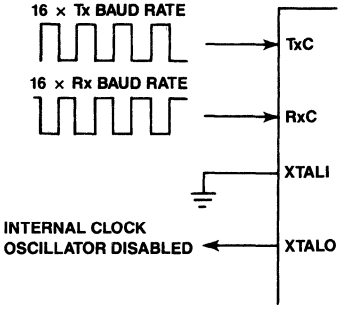
To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.





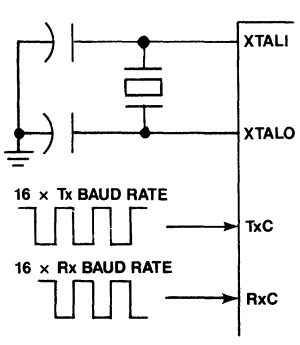
- Baud rate determined by XTALI frequency and 1 of 15 divisors selected in CR1 and CR2. CR1 and CR2 must not be set to all ones.
- Channel 1 baud rate may be different from channel 2 baud rate.
- Receiver baud rate must be the same as transmitter baud rate.

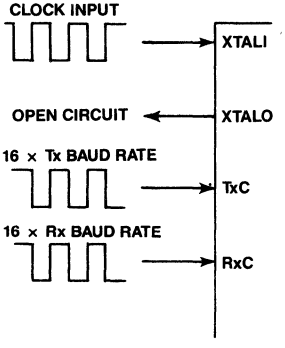
A. Both Channels Use Internal Baud Rate Generator



- Transmitter baud rate 1/16 TxC input frequency.
- Receiver baud rate 1/16 RxC input frequency.
- Channel 1 baud rate is the same as channel 2 baud rate.
- Receiver baud rate may be different from transmitter baud rate.
- Bits 3-0 of CR1 and CR2 must be set to all ones.

B. Both Channels Use External Clocks





- Channel 1 baud rate may be different from channel 2 baud rate.
- Transmitter baud rate may be different from receiver baud rate on channel using external clock.

C. One Channel Uses Internal Baud Rate Generator;
One Channel Uses External Clocks

Figure 5. Baud Rate Clock Options

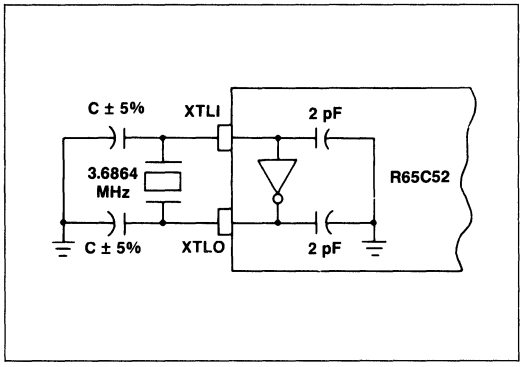


Figure 6.

For example, if C_L = 22 pF for a 3.6864 MHz parallel resonant crystal, then

$C = (2 \times 22) - 2 = 42$ pF (use standard value of 43 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(3.6864 \times 22)^2} = 304 \text{ ohms}$$

If the on-chip oscillator is driven by an external clock, the clock is input at XTALI and XTALO is left open.

An internal counter/divider circuit divides the frequency input at XTALI by the divisor selected in bits 3 through 0 of the Control Registers. Table 5 lists the divisors that may be selected and shows the bit rates generated with a 3.6864 MHz crystal or clock input. Other bit rates may be generated by changing the clock or crystal frequency. However, the input frequency must not exceed 4 MHz.

For external clock operation, a transmitter times 16 clock must be supplied at TxC and a receiver times 16 clock must be input at RxC. Since there are separate receiver and transmitter clock inputs, the receiver data rate may be different from the transmitter data rate.

Table 5. Baud Rate Generator Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal or Clock	Baud Rate Generated* With a Crystal or Clock of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73,728 = 50$	f/73,728
0	0	0	1	33,538	$(3.6864 \times 10^6)/33,538 = 109.92$	f/33,538
0	0	1	0	27,408	$(3\ 6864 \times 10^6)/27,408 = 134\ 58$	f/27,408
0	0	1	1	24,576	$(3.6864 \times 10^6)/24,576 = 150$	f/24,576
0	1	0	0	12,288	$(3.6864 \times 10^6)/12,288 = 300$	f/12,288
0	1	0	1	6,144	$(3.6864 \times 10^6)/6,144 = 600$	f/6,144
0	1	1	0	3,072	$(3.6864 \times 10^6)/3,072 = 1,200$	f/3,072
0	1	1	1	2,048	$(3.6864 \times 10^6)/2,048 = 1,800$	f/2,048
1	0	0	0	1,536	$(3.6864 \times 10^6)/1,536 = 2,400$	f/1,536
1	0	0	1	1,024	$(3.6864 \times 10^6)/1,024 = 3,600$	f/1,024
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4,800$	f/768
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7,200$	f/512
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9,600$	f/384
1	1	0	1	192	$(3\ 6864 \times 10^6)/192 = 19,200$	f/192
1	1	1	0	96	$(3\ 6864 \times 10^6)/96 = 38,400$	f/96
1	1	1	1	16	Transmitter Baud Rate = TxC/16	Receiver Baud Rate = RxC/16

*Baud Rate = $\frac{\text{Frequency}}{\text{Divisor}}$

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An $\overline{IRQ}$ occurs on the transition of the TDR from full to empty if the corresponding TDRE $\overline{IRQ}$ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. 1/16 of a bit time after $\overline{IRQ}$ goes low, the $\overline{IRQ}$ line may be reset by reading the ISR. $\overline{IRQ}$ will always reset when data is written to the TDR. Figure 7 shows the relationship between $\overline{IRQ}$ and TxD for the Continuous Data Transmit mode.

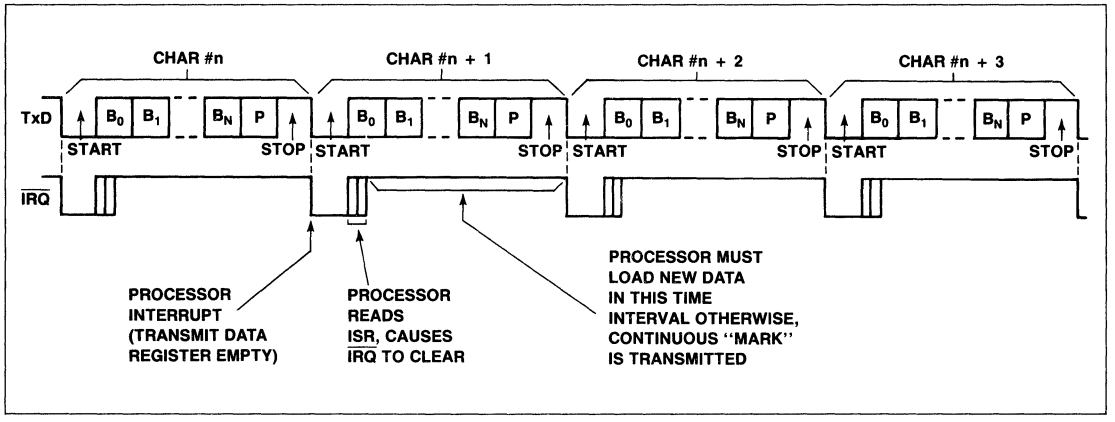


Figure 7. Continuous Data Transmit

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun flag (TUR) is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{IRQ}$ and TxD for the Transmit Underrun Condition.

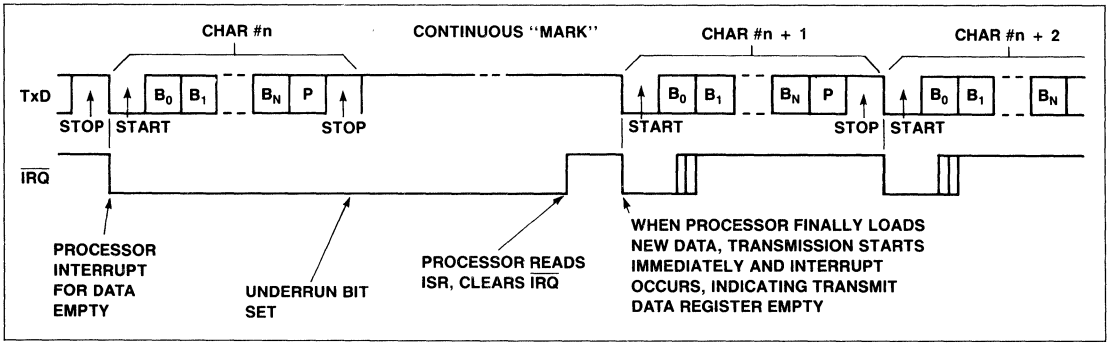


Figure 8. Transmit Underrun Condition Relationship

TRANSMIT BREAK CHARACTER

A BREAK may be transmitted by setting bit 1 of the ACR (Transmit Break bit) to a 1. The BREAK is transmitted after the character in the Transmit Shift Register is sent. If there is a character in the Transmit Data Register, it will be transmitted after the BREAK is terminated. The Transmit Break bit must remain set for at least one character time to assure that a proper BREAK is transmitted. If the Transmit Break bit is cleared before one character time of BREAK has been transmitted, the BREAK will be terminated after one character time has elapsed. If the Transmit Break bit is cleared after one character time of BREAK has been transmitted, the BREAK will be terminated immediately. Figure 9 shows the relationship of TxD, $\overline{IRQ}$ and ACR bit 1 for various BREAK options.

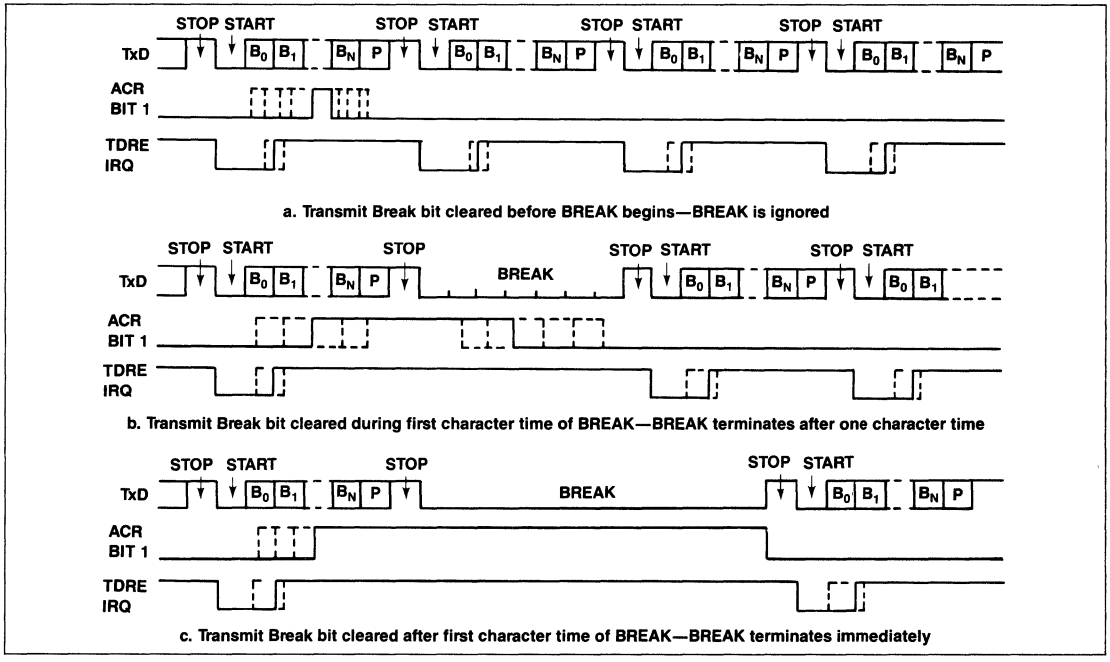


Figure 9. Transmit BREAK

EFFECTS OF $\overline{CTS}$ ON TRANSMITTER

The $\overline{CTS}$ control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the $\overline{CTS}$ line is low, the transmitter operates normally. A high condition inhibits the TDRE bit in the ISR from becoming set. Transmission of the word currently in the shift register is completed but any word in the TDR is held until $\overline{CTS}$ goes low.

Any transition on $\overline{CTS}$ sets bit 5 ($\overline{CTST}$) of the ISR. A high on $\overline{CTS}$ forces bit 6 (TDRE) of the ISR to a 0. Bit 7 of the ISR also goes to a 1 when $\overline{CTS}$ is high, if Echo Mode is disabled. Thus, when the ISR is $80, it means that $\overline{CTS}$ is high and no interrupt source requires service. A processor interrupt will not be generated under these circumstances, but an ISR polling routine should accommodate this.

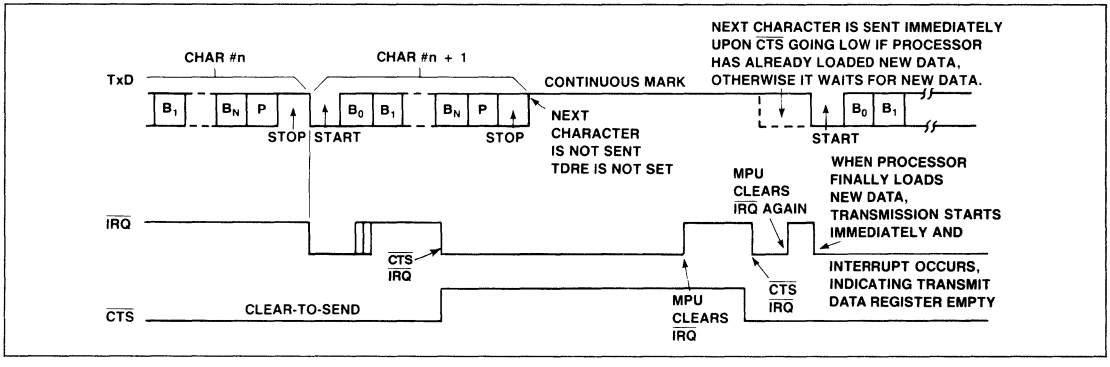


Figure 10. Effects of $\overline{CTS}$ on Transmitter

ECHO MODE TIMING

In the Echo Mode, the TxD line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and TxD for Echo Mode.

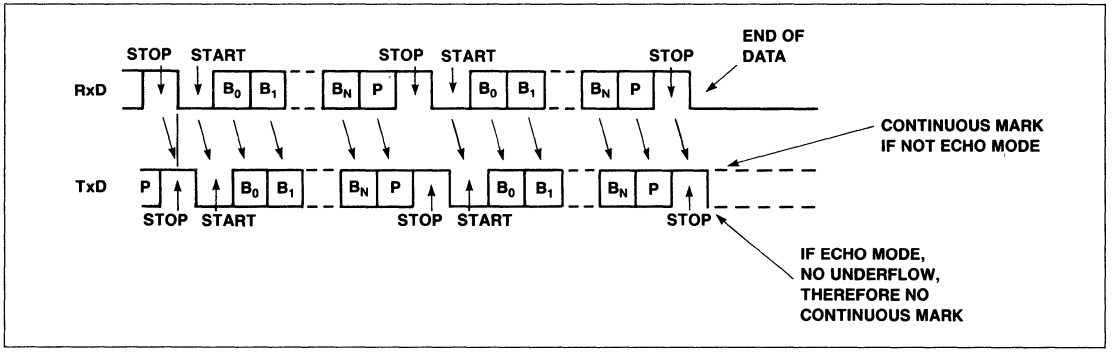


Figure 11. Echo Mode Timing

CONTINUOUS DATA RECEIVE

The normal receive mode sets the RDRF bit in the ISR when the DACIA channel has received a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 12 shows the relationship between $\overline{IRQ}$ and RxD for the continuous Data Receive mode.

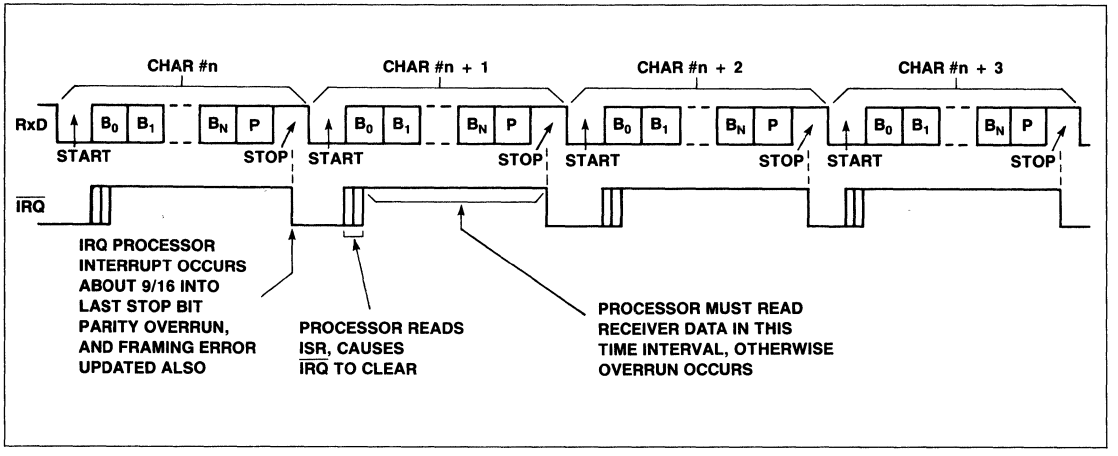


Figure 12. Continuous Data Receive

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 13 shows the relationship of $\overline{IRQ}$ and RxD when overrun occurs.

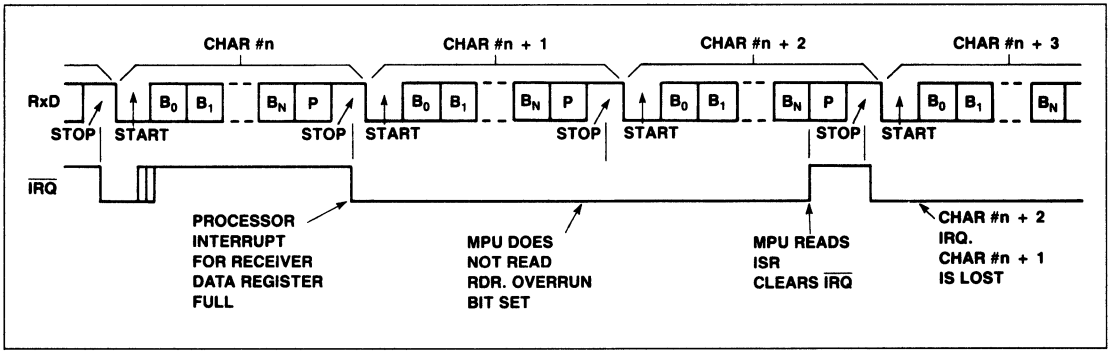


Figure 13. Effects of Overrun on Receiver

RECEIVE BREAK CHARACTER

When a Break character is received, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the next character is received normally. Figure 14 shows the relationship of $\overline{IRQ}$ and RxD for a Receive Break Character.

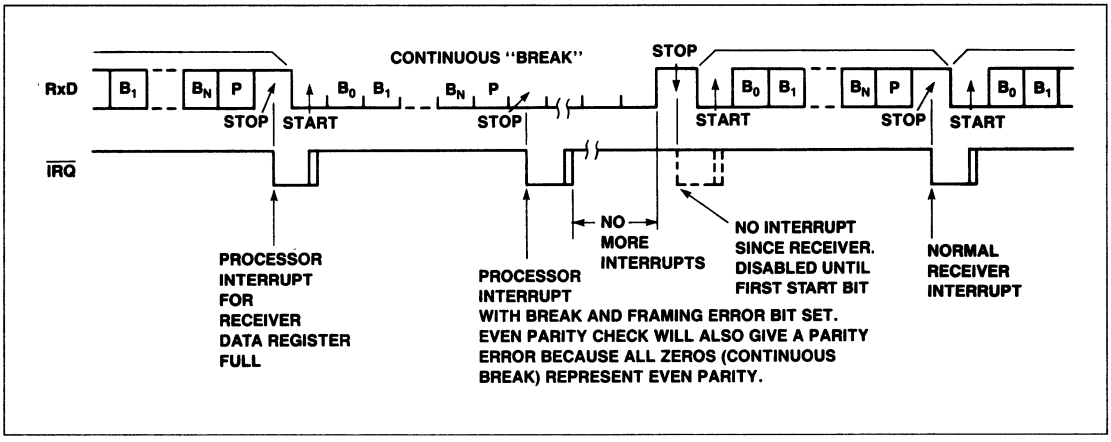


Figure 14. Receive Break Character

FRAMING ERROR

Framing error is caused by the absence of stop bit(s) on received data. The framing error bit is set when the RDRF bit is set. Subsequent data words are tested separately, so the status bit always reflects the last data word received. Figure 15 shows the relationship of $\overline{IRQ}$ and RxD when a framing error occurs.

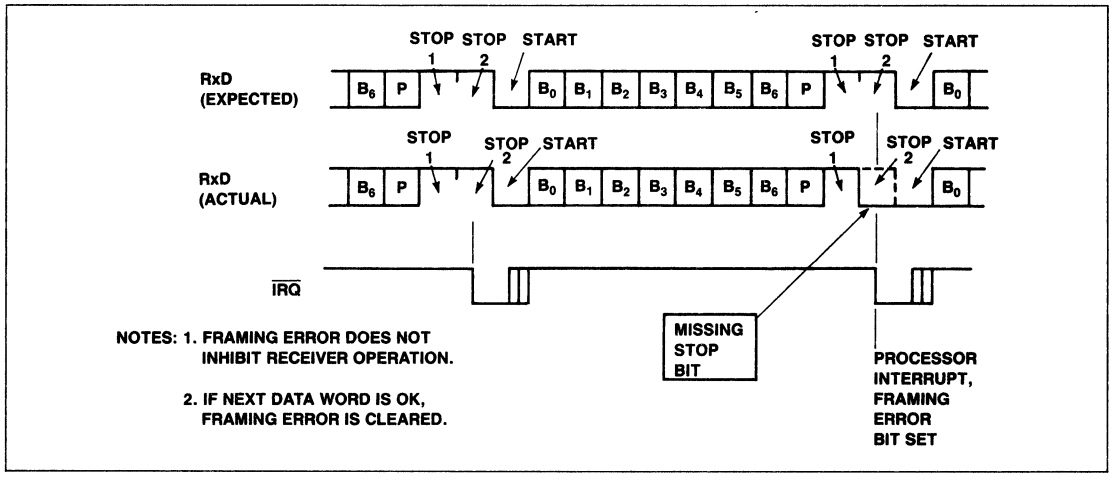


Figure 15. Framing Error

PARITY ERROR DETECT/ADDRESS FRAME RECOGNITION

The Parity Status bit (ISR bit 2) may be programmed to indicate parity errors (ACR bit 0 = 0) or to display the parity bit received (ACR bit 0 = 1).

In applications where parity checking is used, one of the parity checking modes is enabled by setting bits 2, 3 and 4 of the Format Register to the desired option and bit 0 of the Auxiliary Control Register is reset to 0. Then, when the RDRF bit (bit 0) is set in the ISR, the PAR bit (bit 2) will be set when a parity error is detected.

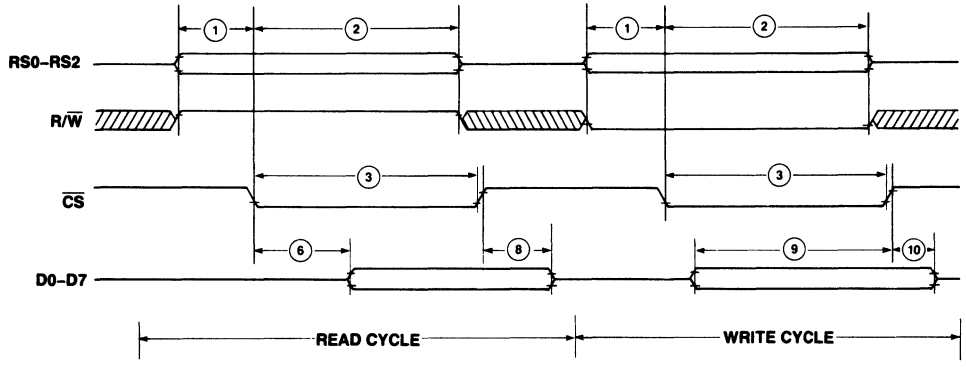
In multi-drop applications, the parity bit is used as an address/data flag. It is set to 1 for address frames and is 0 on data frames. For this type of operation, bit 0 of the ACR is set to a 1 and bits 2, 3 and 4 of the FR select a parity checking mode. Then, ISR bit 2 will be set to a 1 by incoming address frames and it will be a 0 on data frames.

COMPARE MODE

The Compare Mode is automatically enabled, i.e., the channel is put to sleep, whenever data is written to the Compare Data Register. NOTE: Bit 6 of the Control Register must be set to 0 to enable access to the Compare Data Register. When the channel is in the compare mode, the RDRF bit (bit 0 of the ISR) is forced to a 0. Upon receipt of a matching character, normal receiver operation resumes and the RDRF bit (bit 0 of the ISR) will be set upon receipt of the *next* character.

SPECIFICATIONS

DACIA READ/WRITE WAVEFORMS



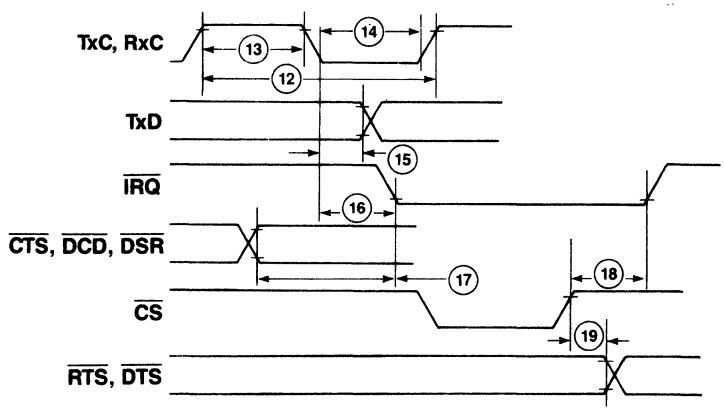
NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8V AND A HIGH VOLTAGE OF 2.0V, UNLESS OTHERWISE NOTED.

DACIA READ/WRITE CYCLE TIMING

(V_{CC} = 5 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	1 MHz		2 MHz		3 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	R/$\overline{W}$, RS0–RS2 Valid to $\overline{CS}$ Low (Setup)	T_{RSU}	5	—	5	—	5	—	ns
2	$\overline{CS}$ Low to R/$\overline{W}$, RS0–RS2 Invalid (Hold)	T_{RH}	45	—	45	—	45	—	ns
3	$\overline{CS}$ Pulse Width	T_{CP}	410	—	340	—	210	—	ns
6	$\overline{CS}$ Low to Data Valid (Read)	T_{CDV}	—	360	—	290	—	170	ns
8	$\overline{CS}$ High to Data Invalid (Read)	T_{CDR}	10	50	10	50	10	50	ns
9	Data Valid to $\overline{CS}$ High (Write, Setup)	T_{DSU}	30	—	30	—	30	—	ns
10	$\overline{CS}$ High to Data Invalid (Write Hold)	T_{CDW}	10	—	10	—	10	—	ns

DACIA TRANSMIT/RECEIVER WAVEFORMS



NOTE: IRQ WILL NOT CHANGE STATE WHEN CS IS LOW.

NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8V AND A HIGH VOLTAGE OF 2.0V, UNLESS OTHERWISE NOTED.

TRANSMIT/RECEIVE AND INTERRUPT ACKNOWLEDGE TIMING

(V_{CC} = 5 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	Min.	Max.	Unit
TRANSMIT/RECEIVE TIMING					
12	Transmit/Receive Clock Rate	t_{CY}	300	—	ns
13	Transmit/Receive Clock High	t_{CH}	125	—	ns
14	Transmit/Receive Clock Low	t_{CL}	125	—	ns
15	TxC, RxC to TxD Propagation Delay	t_{DD}	—	285	ns
16	TxC, RxC to IRQ Propagation Delay	t_{DI}	—	285	ns
17	CTS, DCD, DSR Valid to IRQ Low	t_{CTI}	—	150	ns
18	IRQ Propagation Delay (Clear)	t_{IRQ}	—	150	ns
19	RTS, DTR Propagation Delay	t_{DLY}	—	150	ns

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ± 5%
Temperature Range Commercial Industrial	T_A	 0 to 70°C −40°C to +85°C

DC CHARACTERISTICS

(V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

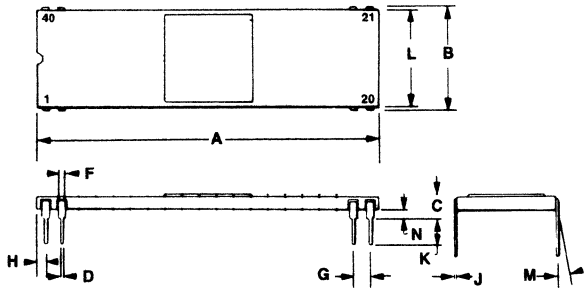
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI XTALI	V_{IH}	 +2.0 +3.0	 — —	 V_{CC} + 0.3 V_{CC} + 0.3	V	
Input Low Voltage Except XTALI XTALI	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current R/W, RES, RS0, RS1, RS2, RxD, CTS, DCD, DSR, RxC, TxC, CS	I_{IN}	—	10	50	μA	V_{IN} = 0V to 5.0V V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	—	±2	10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OH}	+2.4	—	—	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output Leakage Current (Off State) IRQ	I_{OFF}	—	±2	±10	μA	V_{CC} = 5.25V V_{OUT} = 0 to 2.4V
Power Dissipation	P_D	—	—	10	mW/MHz	
Input Capacitance Except XTALI XTALI	C_{IN}	 — —	 — —	 5 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—		10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

6

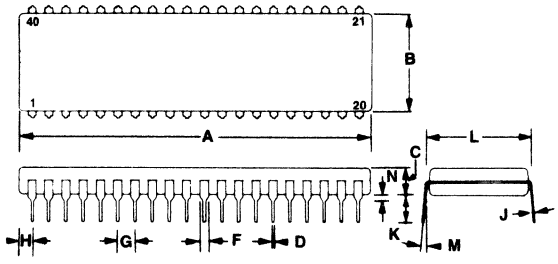
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



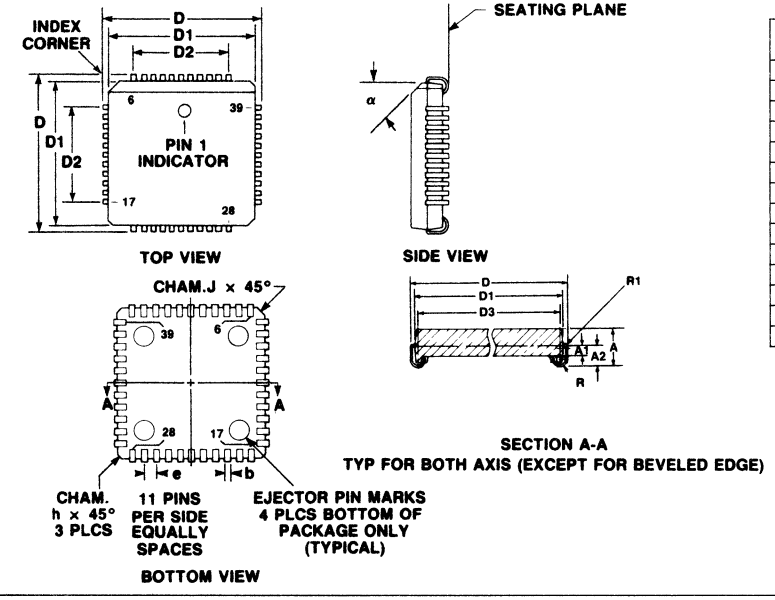
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50 29	51 31	1 980	2 020
B	15 11	15 88	0 595	0 625
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 27	0 030	0 050
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 82	52 32	2 040	2 060
B	13 46	13 97	0 530	0 550
C	3 56	5 08	0 140	0 200
D	0 38	0 53	0 015	0 021
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 30	4 32	0 130	0 170
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4 14	4 39	0 163	0 173
A1	1 37	1 47	0 054	0 058
A2	2 31	2 46	0 091	0 097
b	0 457 TYP		0 018 TYP	
D	17 45	17 60	0 687	0 693
D1	16 46	16 56	0 648	0 652
D2	12 62	12 78	0 497	0 503
D3	15 75 REF		0 620 REF	
e	1 27 BSC		0 050 BSC	
h	1 15 TYP		0 045 TYP	
J	0 25 TYP		0 010 TYP	
α	45° TYP		45° TYP	
R	0 89 TYP		0 035 TYP	
R1	0 25 TYP		0 010 TYP	

Rockwell

R68C552
Dual Asynchronous Communications Interface Adapter (DACIA)

DESCRIPTION

The Rockwell CMOS R68C552 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled two-channel interface between 16-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel.

Transmitter and Receiver bit rates may be controlled by an internal baud rate generator or external times 16 clocks. The baud rate generator accepts either a crystal or a clock input, and provides 15 programmable baud rates. When a 3.6864 MHz crystal is used, the baud rates range from 50 bps to 38,400 bps.

The DACIA may be programmed to transmit and receive frames having word lengths of 5, 6, 7 or 8 bits; even, odd, space, mark or no parity; and 1 or 2 stop bits.

A Compare Register, and the ability to detect address frames, facilitate address recognition in a multidrop mode.

FEATURES

- Low power CMOS N-well silicon gate technoiogy
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 bps to 38,400 bps)
- Program-selectable internally or externally controlled receiver and transmitter bit rates
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Edge detect for $\overline{DCD}$, $\overline{DSR}$, and $\overline{CTS}$
- Program-selectable echo mode for each channel
- Compare Register
- Address/Data frame recognition
- 5.0 Vdc ±5% supply requirements
- 40-pin plastic or ceramic DIP or 44-pin PLCC
- Full TTL or CMOS input/output compatibility
- Compatible with R68000 microprocessors

ORDERING INFORMATION

Part Number:
R68C552 — — —

— Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

— Package:
C = 40-Pin Ceramic DIP
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

6

INTERFACE SIGNALS

The DACIA is available in a 40-pin DIP or a 44-pin PLCC. Figure 1 shows the pin assignments for each package. The DACIA interface signals are shown in Figure 2. Table 1 contains a description of each signal.

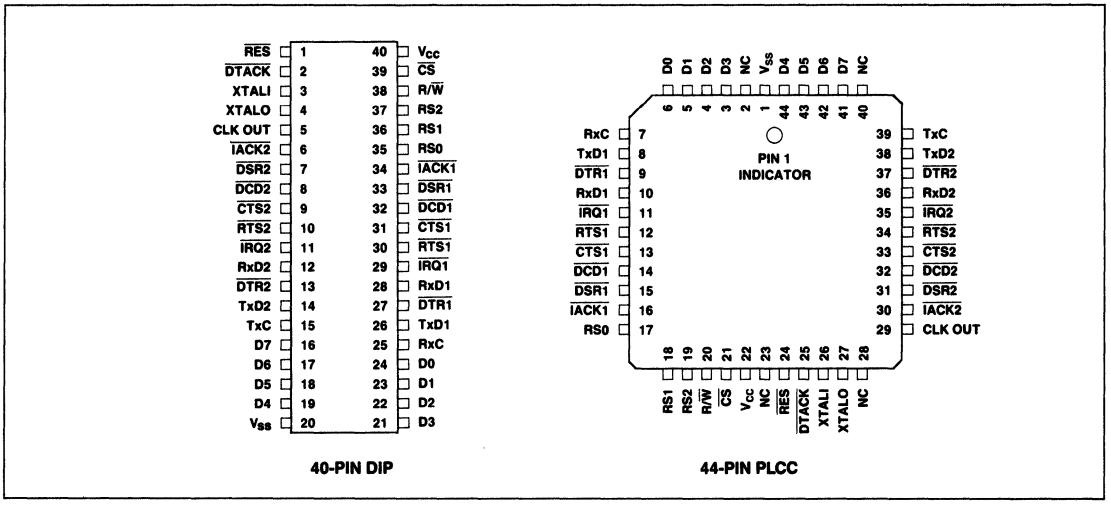


Figure 1. R68C552 Pin Assignments

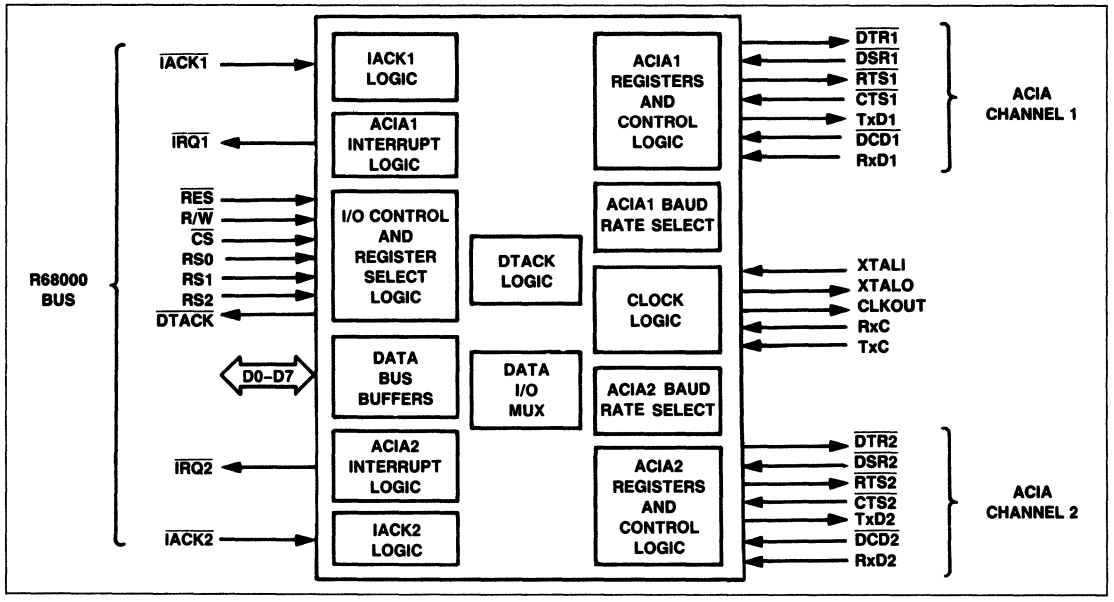


Figure 2. R68C552 DACIA Interface Signals

Table 1. DACIA Interface Signal Definitions

Signal	Pin No. DIP	Pin No. PLCC	I/O	Name/Description
Host Interface				
$\overline{RES}$	1	24	I	**Reset.** Active low input controlling the reset function. This signal must be driven low for a minimum of 4 μs for a valid reset to occur. It is driven high during normal operation.
R/$\overline{W}$	38	20	I	**Read/Write.** Input controlling the direction of data transfer. It is driven low during write cycles, and is driven high at all other times.
$\overline{CS}$	39	21	I	**Chip Select.** Active low input enabling data transfers between the host CPU and the DACIA. The DACIA latches register selects and the R/$\overline{W}$ input on the falling edge of $\overline{CS}$. It latches input data on the rising edge of $\overline{CS}$.
RS0-RS3	35-37	17-19	I	**Register Select.** Three inputs controlling access to the DACIA internal registers. Table 3 lists the coding for each register.
D0-D3 D4-D7	24-21 19-16	6-3 44-41	I/O	**Data Bus.** Eight bidirectional lines used to transfer data between the host and the DACIA. These lines output data during READ cycles when $\overline{CS}$ is low and they output the interrupt vector during INTERRUPT ACKNOWLEDGE cycles when $\overline{IACK1}$ or $\overline{IACK2}$ is low. At all other times, they are in the high impedence state.
$\overline{DTACK}$	2	25	O	**Data Transfer Acknowledge.** Active low open drain output generated in response to $\overline{CS}$, $\overline{IACK1}$ and $\overline{IACK2}$ during asynchronous data transfers. $\overline{DTACK}$ goes to the high impedence state when $\overline{CS}$, $\overline{IACK1}$ and $\overline{IACK2}$ are high.
$\overline{IRQ1}$ $\overline{IRQ2}$	29 11	11 35	O	**Interrupt Request.** Two active low, open-drain outputs from the interrupt control logic. These outputs are normally high. An $\overline{IRQ}$ line goes low when one of the flags of the associated ISR is set if the corresponding enable bit is set in the IER.
$\overline{IACK1}$ $\overline{IACK2}$	34 6	16 30	I	**Interrupt Acknowledge.** Two active low inputs indicating that an INTERRUPT ACKNOWLEDGE cycle is in progress. When an $\overline{IACK}$ goes low, the DACIA places the interrupt vector for the associated channel on the data bus and issues $\overline{DTACK}$.
Clock Interface				
XTALI XTALO	3 4	26 27	I O	**Crystal Input/Output.** One input and one output through which the reference signal for the internal clock oscillator is supplied. A parallel resonant crystal may be connected across the pins or a clock may be input at XTALI. When a clock is used, XTALO must be left open.
CLK OUT	5	29	O	**Clock Out.** A buffered output from the internal clock oscillator which is in phase with XTALI. This output may be used to drive the XTALI input of another DACIA. Therefore, several DACIA chips may be driven with one crystal.
RxC	25	7	I	**Receiver Clock.** Input for external 16x receiver clock
TxC	15	39	I	**Transmitter Clock.** Input for external 16x transmitter clock.
Serial Channel Interface				
$\overline{DTR1}$ $\overline{DTR2}$	27 13	9 37	O	**Data Terminal Ready.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated Format Register (FR) high or low. The state of each $\overline{DTR}$ line is reflected by the $\overline{DTR}$ LVL bit in the associated Control Status Register (CSR).
$\overline{DSR1}$ $\overline{DSR2}$	33 7	15 31	I	**Data Set Ready.** Two general purpose inputs. An active transition sets the $\overline{DSRT}$ bit in the Interrupt Status Register (ISR). The $\overline{DSR}$ LVL bit in the associated CSR reflects the current state of a $\overline{DSR}$ line.
$\overline{RTS1}$ $\overline{RTS2}$	30 10	12 34	O	**Request To Send.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated FR high or low. The state of an $\overline{RTS}$ line is reflected by the $\overline{RTS}$ LVL bit in the associated CSR.
$\overline{CTS1}$ $\overline{CTS2}$	31 9	13 33	I	**Clear To Send.** The $\overline{CTS}$ control line inputs allow handshaking by the transmitters. When $\overline{CTS}$ is low, the data is transmitted continuously. When $\overline{CTS}$ is high, the Transmit Data Register Empty bit (TDRE) in the associated ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on a $\overline{CTS}$ line sets the $\overline{CTST}$ bit in the appropriate ISR. The $\overline{CTS}$ LVL bit in the associated CSR reflects the current state of $\overline{CTS}$.
TxD1 TxD2	26 14	8 38	O	**Transmit Data.** The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator or external clock.
$\overline{DCD1}$ $\overline{DCD2}$	32 8	14 32	I	**Data Carrier Detect.** Two general purpose inputs. An active transition sets the $\overline{DCDT}$ bit in the appropriate ISR. The $\overline{DCD}$ LVL bit in the associated CSR reflects the current state of a $\overline{DCD}$ line.
RxD1 RxD2	28 12	10 36	I	**Receive Data.** The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator or external clock.
Power				
VCC	40	22	I	**DC Power Input.** 5.0V ± 5%.
VSS	20	1	I	**Power and Signal Reference.**

FUNCTIONAL DESCRIPTION

Figure 3 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

RESET LOGIC

The Reset Logic sets various internal registers, status bits and control lines to a known state. The $\overline{RES}$ input must be driven low for a minimum of 4 μs for a valid reset to occur. At this time, the IERs are set to $80, the RDRs and ACRs are cleared, and the compare mode is disabled. Also, the $\overline{DTR}$ and $\overline{RTS}$ outputs are driven high and the $\overline{CTS}$, $\overline{DCD}$ and $\overline{DSR}$ transition detect flags are cleared. No other bits are affected.

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the data lines and the internal data bus. The state of the Data Bus Buffer is controlled by the I/O Control Logic and the Interrupt Logic. Table 2 summarizes the Data Bus Buffer states.

I/O CONTROL LOGIC

The I/O Control Logic controls data transfers between the Internal Registers and the Data Bus Buffer. Internal Register selection is determined by the Register Select inputs as shown in Table 3. When R/$\overline{W}$ is high and $\overline{CS}$ is low, data from the selected register is transferred from the internal data bus to the data lines and $\overline{DTACK}$ is asserted. When $\overline{CS}$ is high, the DACIA is deselected if the $\overline{IACK}$ inputs are high and the data lines are tri-stated.

INTERRUPT LOGIC

The interrupt logic causes the $\overline{IRQ}$ lines ($\overline{IRQ1}$ or $\overline{IRQ2}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. An $\overline{IRQ}$ will be asserted *on the transition* of one of the flags in an ISR from 0 to 1 if the corresponding bit in the associated IER is set. The $\overline{IRQ}$ line is negated when the ISR is read or when the interrupting condition is cleared. CAUTION: When the interrupt is generated by TDRE, 1/16 of a bit time must elapse before $\overline{IRQ}$ can be cleared by reading the ISR.

When an $\overline{IACK}$ input goes low in response to an $\overline{IRQ}$, the following occurs if $\overline{CS}$ and R/$\overline{W}$ are high: D0 goes low if the $\overline{IRQ}$ is generated by TDR empty or RDR full. D0 goes high for all other interrupt sources. TDRE and RDRF interrupts have priority over all other interrupt sources. D1 goes low when the interrupt request is from Channel 1. It goes high if the $\overline{IRQ}$ is from Channel 2. D2 through D7 outputs the Interrupt Vector Number stored in bits 2 through 7 of the Auxiliary Control Register. $\overline{DTACK}$ is asserted.

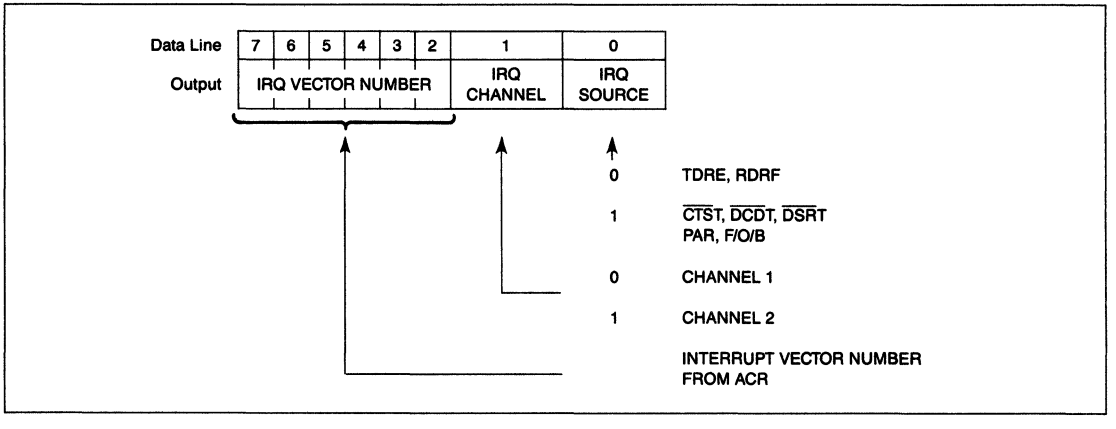
CLOCK OSCILLATOR LOGIC

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock.

The baud rate generator may be disabled by connecting XTALI to ground and leaving XTALO open. When this is done, a transmitter times 16 clock must be input at TxC, a receiver times 16 clock must be input at RxC and the Control Registers must be programmed to select TxC and RxC clocks.

Table 2. Data Bus Buffer Summary

Control Signals				Data Bus Buffer State
R/$\overline{W}$	$\overline{CS}$	$\overline{IACK1}$	$\overline{IACK2}$	
L	L	L	L	Illegal Mode — Tri-State
L	L	L	H	Illegal Mode — Tri-State
L	L	H	L	Illegal Mode — Tri-State
L	L	H	H	Write Mode — Tri-State
L	H	L	L	Illegal Mode — Tri-State
L	H	L	H	Illegal Mode — Tri-State
L	H	H	L	Illegal Mode — Tri-State
L	H	H	H	Tri-State
H	L	L	L	Illegal Mode — Output $0F
H	L	L	H	Illegal Mode — Output $0F
H	L	H	L	Illegal Mode — Output $0F
H	L	H	H	Read Mode — Output Data
H	H	L	L	Illegal Mode — Output $0F
H	H	L	H	Output IRQ Vector 1
H	H	H	L	Output IRQ Vector 2
H	H	H	H	Tri-State



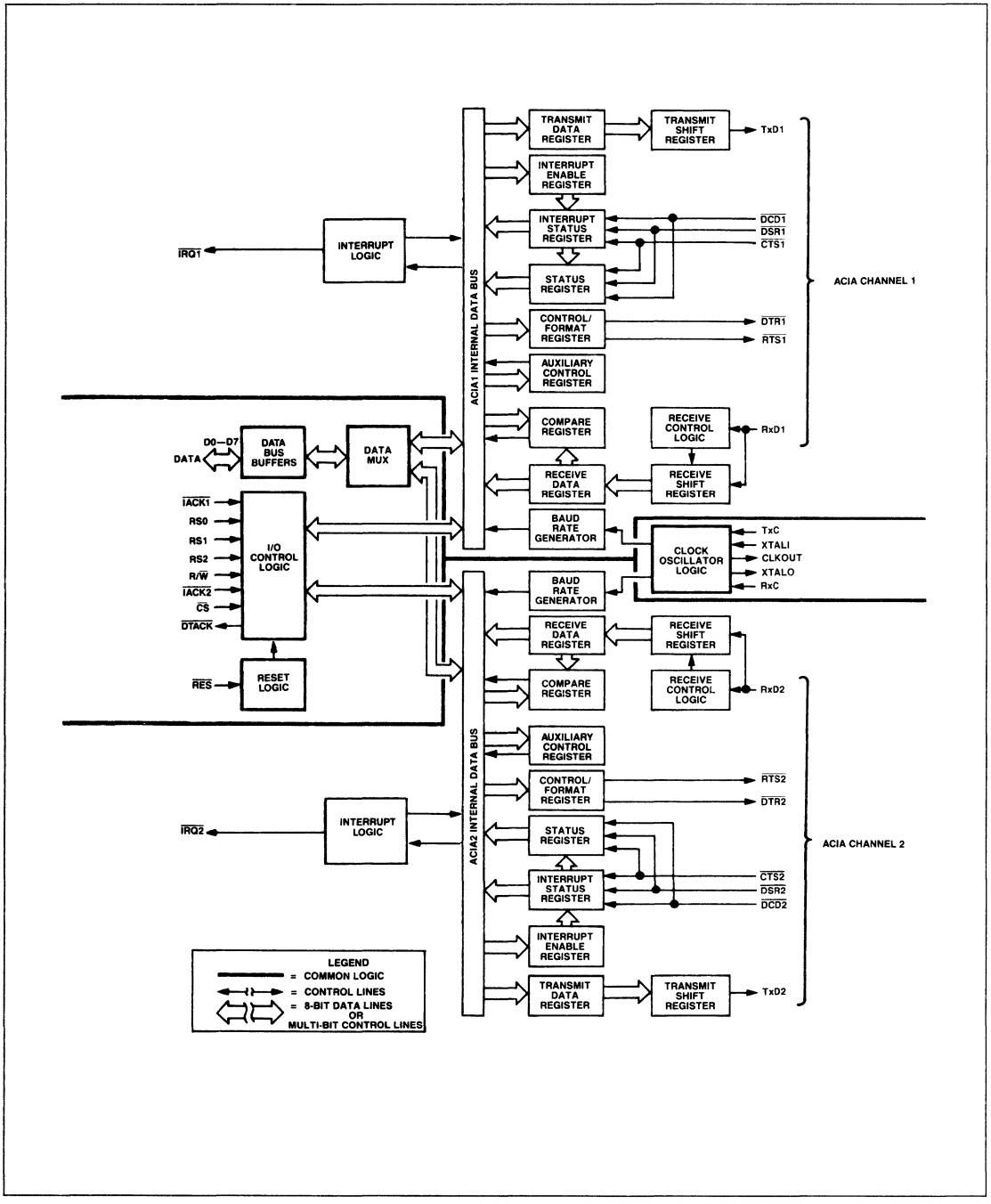


Figure 3. DACIA Block Diagram

Table 3. DACIA Register Selection

Register Select Lines				Register Accessed			
				Write		Read	
HEX	RS2	RS1	RS0	Symbol	Name	Symbol	Name
0	L	L	L	IER1	Interrupt Enable Register 1	ISR1	Interrupt Status Register 1
1	L	L	H	CR1	Control Register 1[1]	CSR1	Control Status Register 1
				FR1	Format Register 1[2]		
2	L	H	L	CDR1	Compare Data Register 1[3]		Not Used
				ACR1	Auxiliary Control Register 1[4]		
3	L	H	H	TDR1	Transmit Data Register 1	RDR1	Receive Data Register 1
4	H	L	L	IER2	Interrupt Enable Register 2	ISR2	Interrupt Status Register 2
5	H	L	H	CR2	Control Register 2[1]	CSR2	Control Status Register 2
				FR2	Format Register 2[2]		
6	H	H	L	CDR2	Compare Data Register 2[3]		Not Used
				ACR2	Auxiliary Control Register 2[4]		
7	H	H	H	TDR2	Transmit Data Register 2	RDR2	Receive Data Register 2

Notes:
1. D7 must be set low to write to the Control Registers.
2. D7 must be set high to write to the Format Registers.
3. Control Register bit 6 must be set to 0 to access the Compare Register.
4. Control Register bit 6 must be set to 1 to access the Auxiliary Control Register.

SERIAL DATA CHANNELS

Two independent serial data channels are available for the full duplex (simultaneous transmit and receive) transfer of asynchronous frames. Separate internal registers are provided for each channel for the selection of frame parameters (number of bits per character, parity options, etc.), status flags, interrupt control and handshake. The asynchronous frame format is shown in Figure 4.

Transmit data from the host system is loaded into the Transmit Data Register. From there, it is transferred to the Transmit Shift Register where it is shifted, LSB first, onto the TxD line. All transmissions begin with a start bit and end with the user selected number of stop bits. A parity bit is transmitted before the stop bit(s) if parity is enabled.

Receive data is shifted into the Receive Shift Register from the associated RxD line. Start and stop bits are stripped from the frame and the data is transferred to the Receive Data Register. Parity bits may be discarded or stored in the ISR.

Five I/O lines are provided for each channel for handshake with the data communications equipment (DCE). Four of these signals ($\overline{RTS}$, $\overline{DTR}$, $\overline{DSR}$ and $\overline{DCD}$) are general purpose inputs or outputs. The fifth signal, $\overline{CTS}$, enables/disables the transmitter. When $\overline{CTS}$ is high and the Transmit Shift Register is empty, the transmitter (except for Echo Mode) is inhibited. When $\overline{CTS}$ is low, the transmitter is enabled.

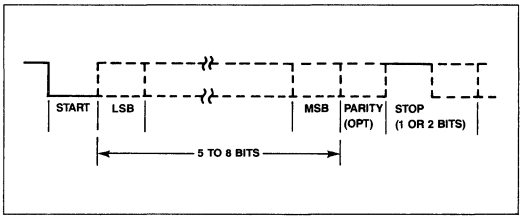


Figure 4. Asynchronous Frame Format

INTERNAL REGISTERS

The DACIA contains ten control registers and four status registers in addition to the transmit and receive registers. The Control Registers provide for control of frame parameters, baud rate, interrupt generation, handshake lines, transmission and reception. The status registers provide status information on transmit and receive registers, error conditions and interrupt sources. Table 4 summarizes the bit definitions of these registers. A detailed description follows.

Table 4. Register Formats

Register Select (Hex)	Register	R/$\overline{W}$	Bit 7	6	5	4	3	2	1	0	Reset Value 76543210
0 4	ISR1 ISR2	R	ANY BIT SET	TDRE	$\overline{CTS}$T	$\overline{DCD}$T	$\overline{DSR}$T	PAR	F/O/B	RDRF	1 - 00000 -
0 4	IER1 IER2	W	CLR/SET BITS	TDRE IE	$\overline{CTS}$T IE	$\overline{DCD}$T IE	$\overline{DSR}$T IE	PAR IE	F/O/B IE	RDRF IE	- 0000000
1 5	CSR1 CSR2	R	FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL	1 - - - - 011
1 5	CR1 CR2	W	0	CDR/ ACR	STOP BITS	ECHO	BIT RATE SEL				0 - - - - - - -
1 5	FR1 FR2	W	1	DATA BITS		PAR SEL		PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL	1 - - - - - - -
2 6	CDR1 CDR2	W (CR6 = 0)	COMPARE DATA								- - - - - - - -
2 6	ACR1 ACR2	W (CR6 = 1)	IRQ VECTOR NUMBER						TRNS BRK	PAR ERR/ST	- - - - - - 00
3 7	RDR1 RDR2	R	RECEIVE DATA REGISTER								00000000
3 7	TDR1 TDR2	W	TRANSMIT DATA REGISTER								- - - - - - - -

INTERRUPT STATUS REGISTERS (ISR1, ISR2)

The Interrupt Status Registers are read-only registers indicating the status of each interrupt source. Bits 6 through 0 are set when the indicated $\overline{IRQ}$ condition has occurred. Bit 7 is set to a 1 when any $\overline{IRQ}$ source bit is set, or if Echo Mode is disabled, when $\overline{CTS}$ is high.

7	6	5	4	3	2	1	0
ANY BIT SET	TDRE	$\overline{CTS}$T	$\overline{DCD}$T	$\overline{DSR}$T	PAR	F/O/B	RDRF

Address = 0,4 Reset Value = 1 - 00000 -

Bit 7 **Any Bit Set**
- 1 Any bit (6 through 0) has been set to a 1 or $\overline{CTS}$ is high with echo disabled
- 0 No bits have been set to a 1 or echo is enabled

Bit 6 **Transmit Data Register Empty (TDRE)**
- 1 Transmit Data Register is empty and $\overline{CTS}$ is low
- 0 Transmit Data Register is full or $\overline{CTS}$ is high

Bit 5 **Transition On $\overline{CTS}$ Line ($\overline{CTS}$T)**
- 1 A positive or negative transition has occurred on $\overline{CTS}$
- 0 No transition has occurred on $\overline{CTS}$, or ISR has been Read

Bit 4 **Transition On $\overline{DCD}$ Line ($\overline{DCD}$T)**
- 1 A positive or negative transition has occurred on $\overline{DCD}$
- 0 No transition has occurred on $\overline{DCD}$, or ISR has been Read

Bit 3 **Transition On $\overline{DSR}$ Line ($\overline{DSR}$T)**
- 1 A positive or negative transition has occurred on $\overline{DSR}$
- 0 No transition has occurred on $\overline{DSR}$, or ISR has been Read

Bit 2 **Parity Status (PAR)**
ACR bit 0 = 0
- 1 A parity error has occurred in received data
- 0 No parity error has occurred, or the Receive Data Register (RDR) has been Read

ACR bit 0 = 1
- 1 Parity bit = 1
- 0 Parity bit = 0

Bit 1 **Frame Error, Overrun, Break**
- 1 A framing error, receive overrun, or receive break has occurred or has been detected
- 0 No error, overrun, break has occurred or RDR has been Read

Bit 0 **Receive Data Register Full (RDRF)**
- 1 Receive Data Register is full
- 0 Receive Data Register is empty

INTERRUPT ENABLE REGISTERS (IER1, IER2)

The Interrupt Enable Registers are write-only registers that enable/disable the $\overline{IRQ}$ sources. $\overline{IRQ}$ sources are enabled by writing to an IER with bit 7 set to a 1 and the bit for every $\overline{IRQ}$ source to be enabled set to a 1. $\overline{IRQ}$ sources are disabled by writing to an IER with bit 7 reset to a 0 and the bit for every source to be disabled set to a 1. Any source bit reset to 0 is unaffected and remains in its original state. Thus, writing $7F to an IER disables all of that channel's interrupts and writing an $FF to an IER enables all of that channel's interrupts.

7	6	5	4	3	2	1	0
SET BITS	TDRE IE	$\overline{CTS}$T IE	$\overline{DCD}$T IE	$\overline{DSR}$T IE	PAR IE	F/O/B IE	RDRF IE

Address = 0,4 Reset Value = - 0000000

Bit 7 **Enable/Disable**
- 1 Enable selected IRQ source
- 0 Disable selected IRQ source

Bits 0-6
- 1 Select for enable/disable
- 0 No change

CONTROL STATUS REGISTERS (CSR1, CSR2)

The Control Status Registers are read-only registers that provide I/O status and error condition information. A CSR is normally read after an $\overline{IRQ}$ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL

Address = 1,5 Reset Value = 1 - - - - 011

Bit 7 **Framing Error (FE)**
- 1 A framing error occurred in receive data
- 0 No framing error occurred, or the RDR was read

Bit 6 **Transmitter Underrun (TUR)**
- 1 Transmit Shift Register is empty and TDRE is set
- 0 Transmitter Shift Register is not empty

Bit 5 **$\overline{CTS}$ Level ($\overline{CTS}$ LVL)**
- 1 $\overline{CTS}$ line is high
- 0 $\overline{CTS}$ line is low

Bit 4 **$\overline{DCD}$ Level ($\overline{DCD}$ LVL)**
- 1 $\overline{DCD}$ line is high
- 0 $\overline{DCD}$ line is low

Bit 3 **$\overline{DSR}$ Level ($\overline{DSR}$ LVL)**
- 1 $\overline{DSR}$ line is high
- 0 $\overline{DSR}$ line is low

Bit 2 **Receive Break (BRK)**
- 1 A Receive Break has occurred
- 0 No Receive Break occurred, or RDR was read

Bit 1 **$\overline{DTR}$ Level ($\overline{DTR}$ LVL)**
- 1 $\overline{DTR}$ line is high
- 0 $\overline{DTR}$ line is low

Bit 0 **$\overline{RTS}$ Level ($\overline{RTS}$ LVL)**
- 1 $\overline{RTS}$ line is high
- 0 $\overline{RTS}$ line is low

CONTROL REGISTERS (CR1, CR2)

The Control Registers are write-only registers. They control access to the Auxiliary Control Register and the Compare Data Register. They select the number of stop bits, control Echo Mode, and select the data rate.

(Accessed when Bit 7 = 0)

7	6	5	4	3 2 1 0
0	CDR/ACR	STOP BITS	ECHO	BAUD RATE SEL

Address = 1,5 Reset Value = 0-------

Bit 7 **Control or Format Register**
0 Access Control Register

Bit 6 **CDR/ACR**
1 Access the Auxiliary Control Register (ACR)
0 Access the Compare Data Register (CDR)

Bit 5 **Number of Stop Bits Per Character**
1 Two stop bits
0 One stop bit

Bit 4 **Echo Mode Selection**
1 Echo Mode enabled
0 Echo Mode disabled

Bits 3-0 **Baud Rate Selection**

3	2	1	0	(bits per second with 3.6864 MHz crystal)
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External TxC and RxC X16 Clocks

FORMAT REGISTERS (FR1, FR2)

The Format Registers are write-only registers. They select the number of data bits per character and parity generation/checking options. They also control $\overline{RTS}$ and $\overline{DTR}$.

(Accessed when Bit 7 = 1)

7	6 5	4 3	2	1	0
1	DATA BITS	PAR SEL	PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL

Address = 1,5 Reset Value = 1-------

Bit 7 **Control or Format Register**
1 Access Format Register

Bits 6-5 **Number of Data Bits Per Character**

6	5	
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3 **Parity Mode Selection**

4	3	
0	0	Odd Parity
0	1	Even Parity
1	0	Mark in Parity bit
1	1	Space in Parity bit

Bit 2 **Parity Enable**
1 Parity as specified by bits 4-3
0 No Parity

Bit 1 **$\overline{DTR}$ Control**
1 Set $\overline{DTR}$ high
0 Set $\overline{DTR}$ low

Bit 0 **$\overline{RTS}$ Control**
1 Set $\overline{RTS}$ high
0 Set $\overline{RTS}$ low

COMPARE DATA REGISTERS (CDR1, CDR2)

The Compare Data Registers are write-only registers which can be accessed when CR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

(Control Register bit 6 = 0)

7	6	5	4	3	2	1	0
COMPARE DATA							

Address = 2,6 Reset Value = --------

AUXILIARY CONTROL REGISTERS (ACR1, ACR2)

The Auxiliary Control Registers are write-only registers. Bits 7-2 hold the user selected interrupt vector number to be output on data lines 7-2 during interrupt acknowledge. Bit 1 causes the transmitter to transmit a BREAK. Bit 0 determines whether parity error or the parity bit is displayed in ISR bit 2.

(Control Register bit 6 = 1)

7	6	5	4	3	2	1	0
IRQ VECTOR ADDRESS						TRNS BRK	PAR ERR/ST

Address = 2,6 Reset Value = ------00

Bits 7-2	IRQ Vector Address
Bit 1	**Transmit Break (TRNS BRK)**
1	Transmit continuous Break
0	Normal transmission
Bit 0	**Parity Error/State (PAR ERR/ST)**
1	Send value of parity bit to ISR bit 2 (Address Recognition mode)
0	Send Parity Error status to ISR bit 2

RECEIVE DATA REGISTERS (RDR1, RDR2)

The Receive Data Registers are read-only registers which are loaded with the received data character of each frame. Start bits, stop bits and parity bits are stripped off of incoming frames before the data is transferred from the Receive Shift Register to the Receive Data Register. For characters of less than eight bits, the unused bits are the high order bits which are set to 0.

MSB **LSB**

7	6	5	4	3	2	1	0
RECEIVE DATA							

Address = 3,7 Reset Value = 00000000

TRANSMIT DATA REGISTERS (TDR1, TDR2)

The Transmit Data Registers are write-only registers which are loaded from the CPU with data to be transmitted. For data characters of less than eight bits, the unused bits are the high order bits which are "don't care".

MSB **LSB**

7	6	5	4	3	2	1	0
TRANSMIT DATA							

Address = 3,7 Reset Value = --------

OPERATION

TERMINATION OF UNUSED INPUTS

Noise on floating inputs can affect chip operation. All unused inputs must be terminated. If unused, $\overline{IACK1}$ and $\overline{IACK2}$ must be tied high. If the baud rate generator is bypassed, XTALI must be connected to ground (XTALO is an output and must be left open). If the external clock mode is not used, RxC and TxC may be tied either to +5V or to ground. If the handshake inputs are not needed, the $\overline{CTS}$ inputs should be tied low to enable the transmitters. The $\overline{DCD}$ and $\overline{DSR}$ inputs may either be tied high or low.

TERMINATION OF $\overline{DTACK}$

A current limiting resistor with a minimum value of 3.6 KΩ should be connected between $\overline{DTACK}$ and +5V.

RESET INITIALIZATION

During power on initialization, all readable registers should be read to assure that the status registers are initialized. Specifically, the RDRF bit of the Interrupt Status Registers is not initialized by reset. The Receiver Data Registers must be read to clear this bit.

TDRE $\overline{IRQ}$ is generated only on the transition of the corresponding TDR from full to empty. Initialization software must account for this occurrence.

BAUD RATE CLOCK OPTIONS

The receiver and transmitter clocks may be supplied either by the internal Baud Rate Generator or by user supplied external clocks. Both channels may use the same clock source or one may use the Baud Rate Generator and the other channel external clocks. If both channels use the Baud Rate Generator, each channel may have a different bit rate. The options are shown in Figure 5.

An internal clock oscillator supplies the time base for the Baud Rate Generator. The oscillator can be driven by a crystal or an external clock.

If the on-chip oscillator is driven by a crystal, a parallel resonant crystal is connected between the XTALI and XTALO pins. The equivalent oscillator circuit is shown in Figure 6.

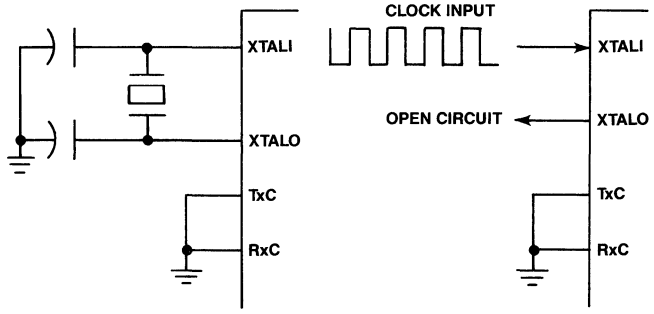
A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 2) = 2C_L \quad \text{or} \quad C = 2C_L - 2$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

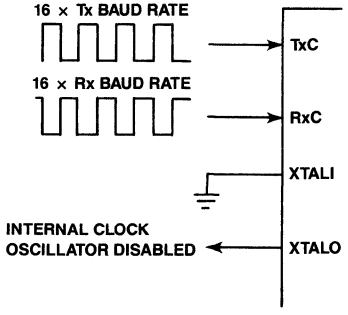
where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.



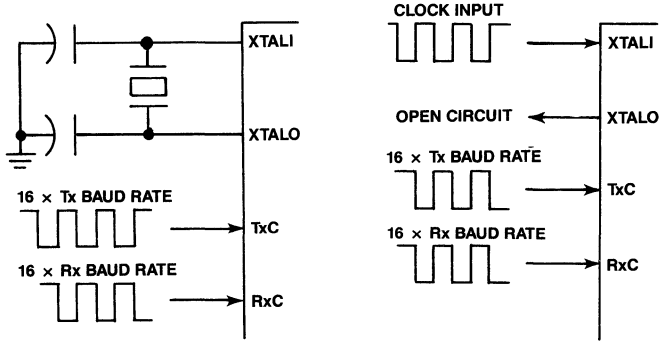
- Baud rate determined by XTALI frequency and 1 of 15 divisors selected in CR1 and CR2. CR1 and CR2 must not be set to all ones.
- Channel 1 baud rate may be different from channel 2 baud rate.
- Receiver baud rate must be the same as transmitter baud rate.

A. Both Channels Use Internal Baud Rate Generator



- Transmitter baud rate 1/16 TxC input frequency.
- Receiver baud rate 1/16 RxC input frequency.
- Channel 1 baud rate is the same as channel 2 baud rate.
- Receiver baud rate may be different from transmitter baud rate.
- Bits 3-0 of CR1 and CR2 must be set to all ones.

B. Both Channels Use External Clocks



- Channel 1 baud rate may be different from channel 2 baud rate.
- Transmitter baud rate may be different from receiver baud rate on channel using external clock.

C. One Channel Uses Internal Baud Rate Generator; One Channel Uses External Clocks

Figure 5. Baud Rate Clock Options

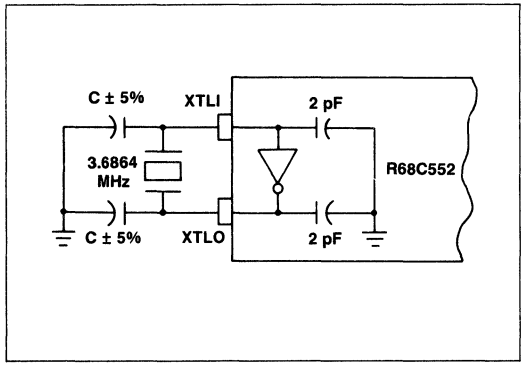


Figure 6.

For example, if C_L = 22 pF for a 3.6864 MHz parallel resonant crystal, then

$C = (2 \times 22) - 2 = 42$ pF (use standard value of 43 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(3.6864 \times 22)^2} = 304 \text{ ohms}$$

If the on-chip oscillator is driven by an external clock, the clock is input at XTALI and XTALO is left open.

An internal counter/divider circuit divides the frequency input at XTALI by the divisor selected in bits 3 through 0 of the Control Registers. Table 5 lists the divisors that may be selected and shows the bit rates generated with a 3.6864 MHz crystal or clock input. Other bit rates may be generated by changing the clock or crystal frequency. However, the input frequency must not exceed 4 MHz.

For external clock operation, a transmitter times 16 clock must be supplied at TxC and a receiver times 16 clock must be input at RxC. Since there are separate receiver and transmitter clock inputs, the receiver data rate may be different from the transmitter data rate.

Table 5. Baud Rate Generator Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal or Clock	Baud Rate Generated* With a Crystal or Clock of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73,728 = 50$	f/73,728
0	0	0	1	33,538	$(3.6864 \times 10^6)/33,538 = 109.92$	f/33,538
0	0	1	0	27,408	$(3.6864 \times 10^6)/27,408 = 134.58$	f/27,408
0	0	1	1	24,576	$(3.6864 \times 10^6)/24,576 = 150$	f/24,576
0	1	0	0	12,288	$(3.6864 \times 10^6)/12,288 = 300$	f/12,288
0	1	0	1	6,144	$(3.6864 \times 10^6)/6,144 = 600$	f/6,144
0	1	1	0	3,072	$(3.6864 \times 10^6)/3,072 = 1,200$	f/3,072
0	1	1	1	2,048	$(3.6864 \times 10^6)/2,048 = 1,800$	f/2,048
1	0	0	0	1,536	$(3.6864 \times 10^6)/1,536 = 2,400$	f/1,536
1	0	0	1	1,024	$(3.6864 \times 10^6)/1,024 = 3,600$	f/1,024
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4,800$	f/768
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7,200$	f/512
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9,600$	f/384
1	1	0	1	192	$(3.6864 \times 10^6)/192 = 19,200$	f/192
1	1	1	0	96	$(3.6864 \times 10^6)/96 = 38,400$	f/96
1	1	1	1	16	Transmitter Baud Rate = TxC/16	Receiver Baud Rate = RxC/16

*Baud Rate = $\frac{\text{Frequency}}{\text{Divisor}}$

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An $\overline{IRQ}$ occurs on the transition of the TDR from full to empty if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. 1/16 of a bit time after $\overline{IRQ}$ goes low, the $\overline{IRQ}$ line may be reset by reading the IRS. $\overline{IRQ}$ will always reset when data is written to the TDR. Figure 7 shows the relationship between $\overline{IRQ}$ and TxD for the Continuous Data Transmit mode.

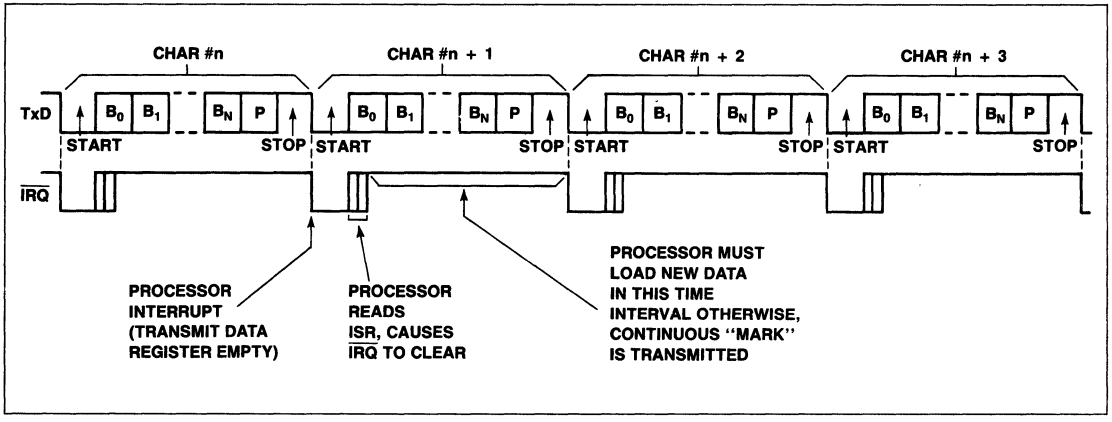


Figure 7. Continuous Data Transmit

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun flag (TUR) is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{IRQ}$ and TxD for the Transmit Underrun Condition.

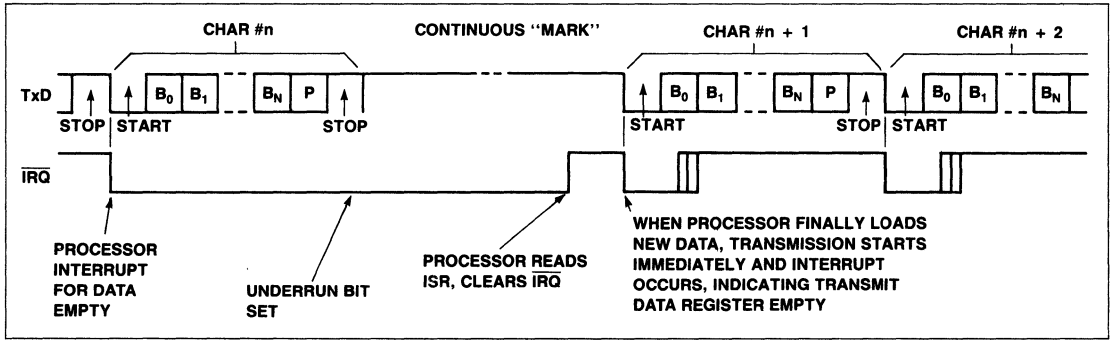


Figure 8. Transmit Underrun Condition Relationship

TRANSMIT BREAK CHARACTER

A BREAK may be transmitted by setting bit 1 of the ACR (Transmit Break bit) to a 1. The BREAK is transmitted after the character in the Transmit Shift Register is sent. If there is a character in the Transmit Data Register, it will be transmitted after the BREAK is terminated. The Transmit Break bit must remain set for at least one character time to assure that a proper BREAK is transmitted. If the Transmit Break bit is cleared before one character time of BREAK has been transmitted, the BREAK will be terminated after one character time has elapsed. If the Transmit Break bit is cleared after one character time of BREAK has been transmitted, the BREAK will be terminated immediately. Figure 9 shows the relationship of TxD, $\overline{IRQ}$ and ACR bit 1 for various BREAK options.

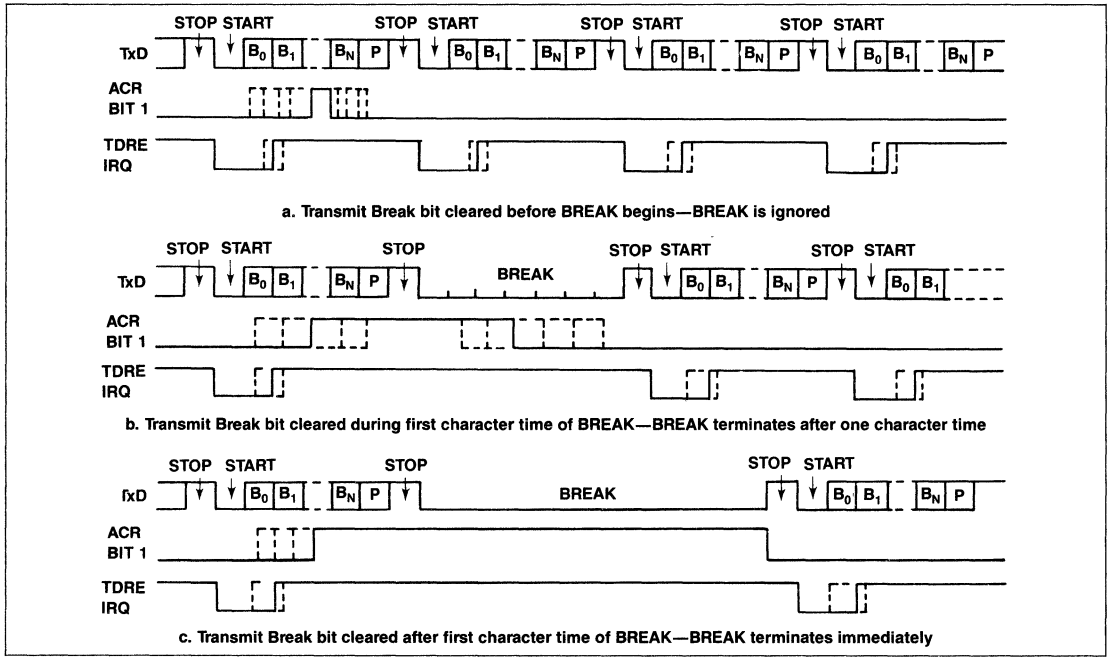


Figure 9. Transmit BREAK

EFFECTS OF $\overline{CTS}$ ON TRANSMITTER

The $\overline{CTS}$ control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the $\overline{CTS}$ line is low, the transmitter operates normally. A high condition inhibits the TDRE bit in the ISR from becoming set. Transmission of the word currently in the shift register is completed but any word in the TDR is held until $\overline{CTS}$ goes low.

Any transition on $\overline{CTS}$ sets bit 5 ($\overline{CTST}$) of the ISR. A high on $\overline{CTS}$ forces bit 6 (TDRE) of the ISR to a 0. Bit 7 of the ISR also goes to a 1 when $\overline{CTS}$ is high, if Echo Mode is disabled. Thus, when the ISR is $80, it means that $\overline{CTS}$ is high and no interrupt source requires service. A processor interrupt will not be generated under these circumstances, but an ISR polling routine should accommodate this.

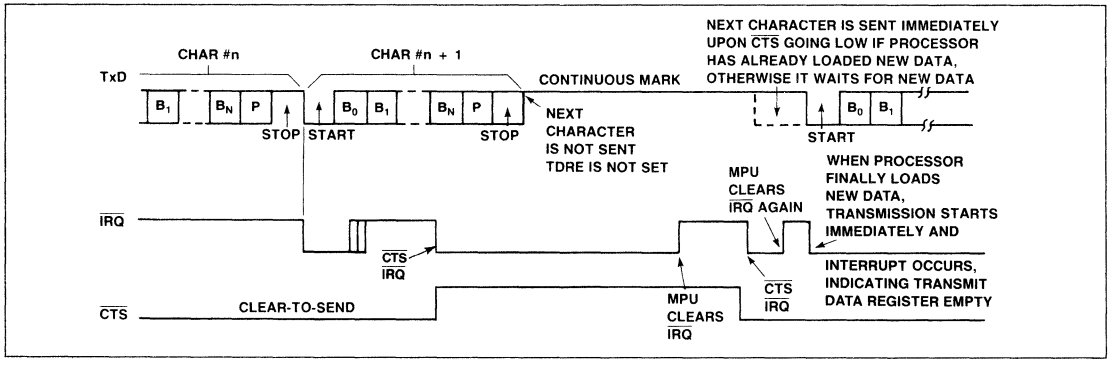


Figure 10. Effects of $\overline{CTS}$ on Transmitter

ECHO MODE TIMING

In the Echo Mode, the TxD line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and TxD for Echo Mode.

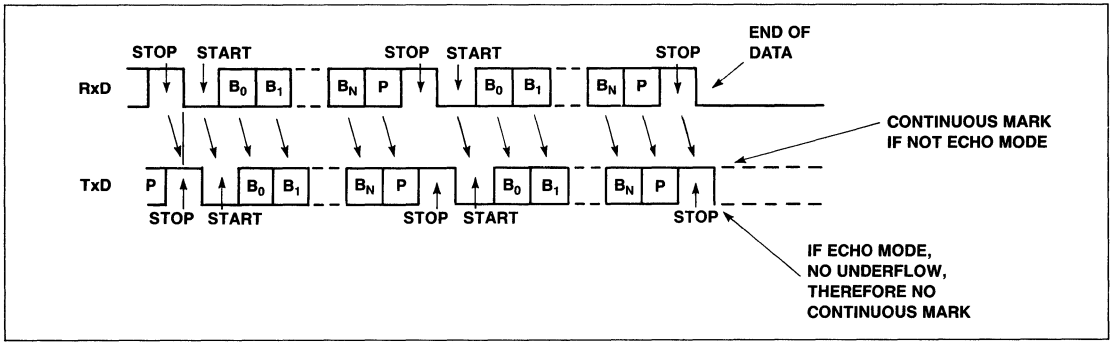


Figure 11. Echo Mode Timing

CONTINUOUS DATA RECEIVE

The normal receive mode sets the RDRF bit in the ISR when the DACIA channel has received a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 12 shows the relationship between $\overline{IRQ}$ and RxD for the continuous Data Receive mode.

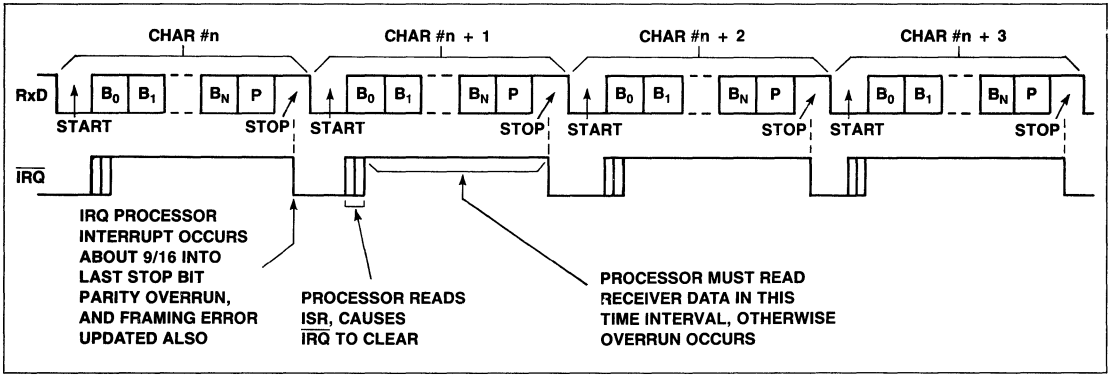


Figure 12. Continuous Data Receive

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 13 shows the relationship of $\overline{IRQ}$ and RxD when overrun occurs.

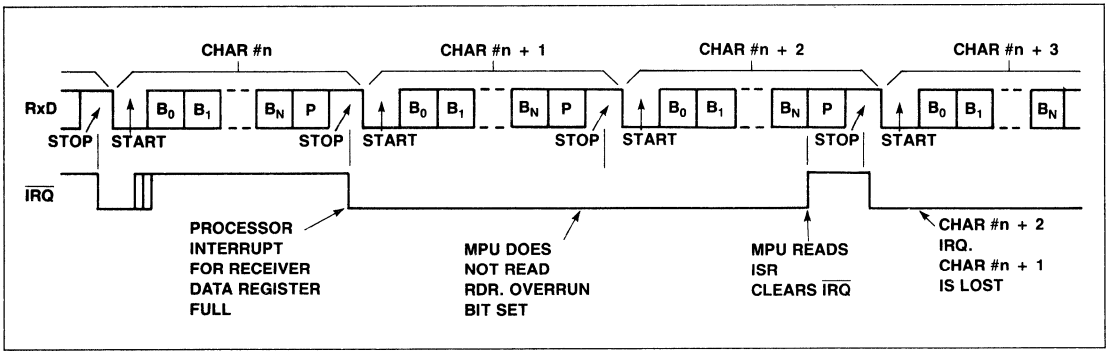


Figure 13. Effects of Overrun on Receiver

RECEIVE BREAK CHARACTER

When a Break character is received, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the next character is received normally. Figure 14 shows the relationship of $\overline{IRQ}$ and RxD for a Receive Break Character.

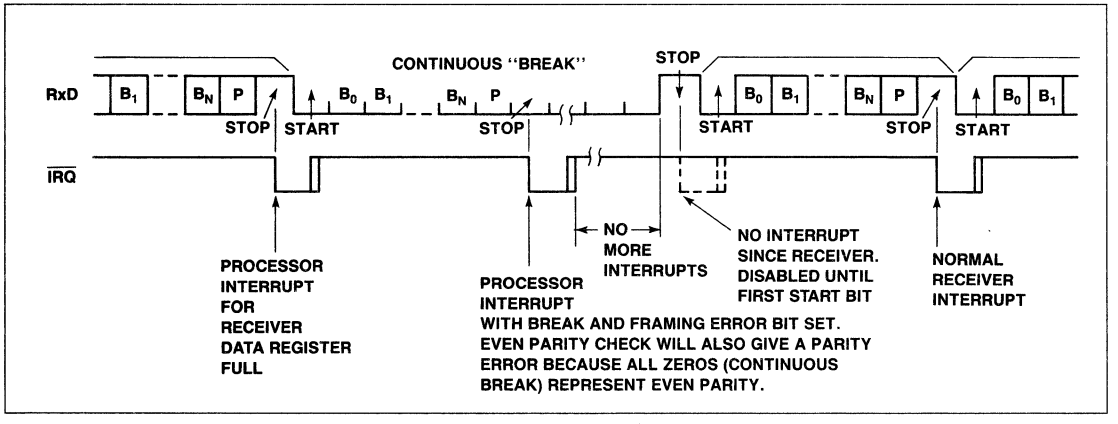


Figure 14. Receive Break Character

FRAMING ERROR

Framing error is caused by the absence of stop bit(s) on received data. The framing error bit is set when the RDRF bit is set. Subsequent data words are tested separately, so the status bit always reflects the last data word received. Figure 15 shows the relationship of $\overline{IRQ}$ and RxD when a framing error occurs.

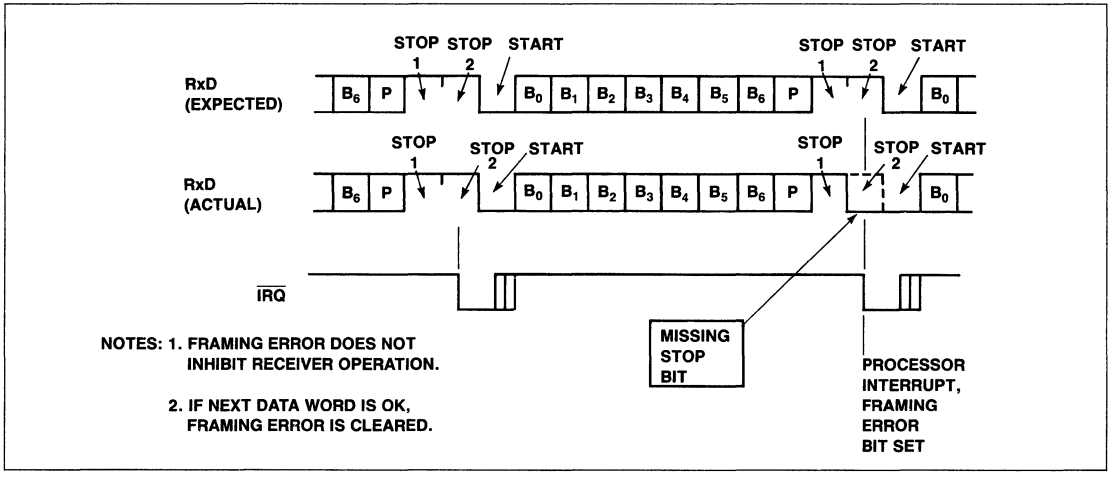


Figure 15. Framing Error

PARITY ERROR DETECT/ADDRESS FRAME RECOGNITION

The Parity Status bit (ISR bit 2) may be programmed to indicate parity errors (ACR bit 0 = 0) or to display the parity bit received (ACR bit 0 = 1).

In applications where parity checking is used, one of the parity checking modes is enabled by setting bits 2, 3 and 4 of the Format Register to the desired option and bit 0 of the Auxiliary Control Register is reset to 0. Then, when the RDRF bit (bit 0) is set in the ISR, the PAR bit (bit 2) will be set when a parity error is detected.

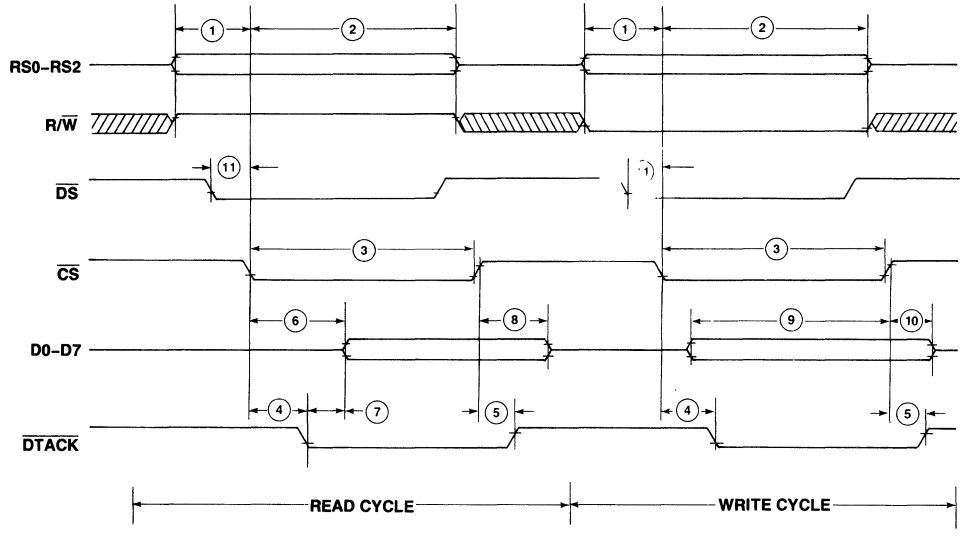
In multi-drop applications, the parity bit is used as an address/data flag. It is set to 1 for address frames and is 0 on data frames. For this type of operation, bit 0 of the ACR is set to a 1 and bits 2, 3 and 4 of the FR select a parity checking mode. Then, ISR bit 2 will be set to a 1 by incoming address frames and it will be a 0 on data frames.

COMPARE MODE

The Compare Mode is automatically enabled, i.e., the channel is put to sleep, whenever data is written to the Compare Data Register. NOTE: Bit 6 of the Control Register must be set to 0 to enable access to the Compare Data Register. When the channel is in the compare mode, the RDRF bit (bit 0 of the ISR) is forced to a 0. Upon receipt of a matching character, normal receiver operation resumes and the RDRF bit (bit 0 of the ISR) will be set upon receipt of the *next* character.

SPECIFICATIONS

DACIA READ/WRITE WAVEFORMS



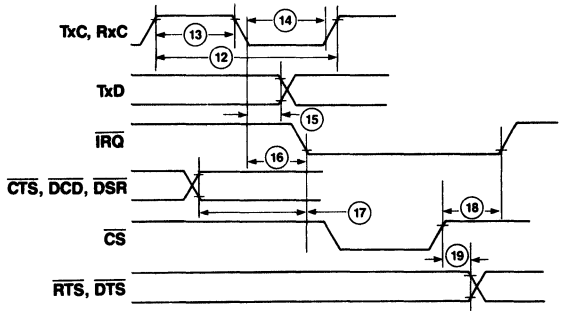
NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8V AND A HIGH VOLTAGE OF 2.0V, UNLESS OTHERWISE NOTED.

DACIA READ/WRITE CYCLE TIMING

(V_{CC} = 5 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

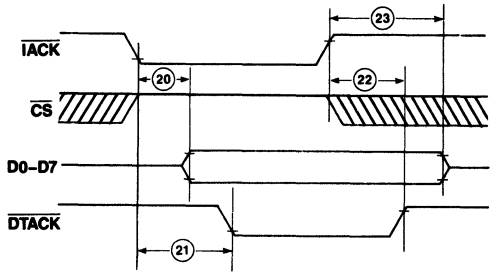
Number	Characteristic	Symbol	Min.	Typ.	Max.	Unit
1	R/$\overline{W}$, RS0-RS2 Valid to $\overline{CS}$ Low (Setup)	T_{RSU}	5		—	ns
2	$\overline{CS}$ Low to R/$\overline{W}$, RS0-RS2 Invalid (Hold)	T_{RH}	45		—	ns
3	$\overline{CS}$ Pulse Width	T_{CP}	210		—	ns
4	$\overline{CS}$ Low to $\overline{DTACK}$ Low	T_{CTL}	—		55	ns
5	$\overline{CS}$ High to $\overline{DTACK}$ High	T_{CTH}	0		170	ns
6	$\overline{CS}$ Low to Data Valid (Read)	T_{CDV}	—		170	ns
7	$\overline{DTACK}$ Low to Data Valid (Read)	T_{TDV}	—		110	ns
8	$\overline{CS}$ High to Data Invalid (Read)	T_{CDR}	10		50	ns
9	Data Valid to $\overline{CS}$ High (Write, Setup)	T_{DSU}	30		—	ns
10	$\overline{CS}$ High to Data Invalid (Write Hold)	T_{CDW}	10		—	ns
11	$\overline{DS}$ Low to $\overline{CS}$ Low (Delay for $\overline{CS}$ derived from Data Strobe)	T_{DSC}		20		ns

DACIA TRANSMIT/RECEIVER WAVEFORMS



NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8V AND A HIGH VOLTAGE OF 2.0V, UNLESS OTHERWISE NOTED.

DACIA INTERRUPT ACKNOWLEDGE WAVEFORMS



NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8V AND A HIGH VOLTAGE OF 2.0V, UNLESS OTHERWISE NOTED.

NOTE: $\overline{CS}$ MUST BE HIGH DURING $\overline{IACK}$ CYCLE.

TRANSMIT/RECEIVE AND INTERRUPT ACKNOWLEDGE TIMING

(V_{CC} = 5 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	Min.	Max.	Unit
TRANSMIT/RECEIVE TIMING					
12	Transmit/Receive Clock Rate	t_{CY}	300	—	ns
13	Transmit/Receive Clock High	t_{CH}	125	—	ns
14	Transmit/Receive Clock Low	t_{CL}	125	—	ns
15	TxC, RxC to TxD Propagation Delay	t_{DD}	—	285	ns
16	TxC, RxC to $\overline{IRQ}$ Propagation Delay	t_{DI}	—	285	ns
17	$\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ Valid to $\overline{IRQ}$ Low	t_{CTI}	—	150	ns
18	$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	150	ns
19	$\overline{RTS}$, $\overline{DTR}$ Propagation Delay	t_{DLY}	—	150	ns
INTERRUPT ACKNOWLEDGE TIMING					
20	$\overline{IACK}$ Low to Data Valid	t_{IDV}	—	170	ns
21	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{ITL}	—	62	ns
22	$\overline{IACK}$ High to $\overline{DTACK}$ High	t_{ITH}	—	170	ns
23	$\overline{IACK}$ High to Data Invalid	t_{IDZ}	10	40	ns

6

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ± 5%
Temperature Range Commercial Industrial	T_A	 0 to 70°C −40°C to +85°C

DC CHARACTERISTICS

(V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

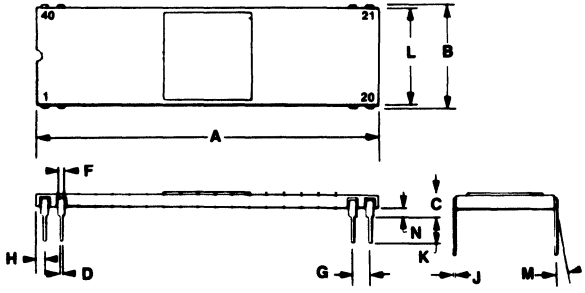
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI XTALI	V_{IH}	 +2.0 +3.0	 — —	 V_{CC} + 0.3 V_{CC} + 0.3	V	
Input Low Voltage Except XTALI XTALI	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RxD, $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$, RxC, TxC, $\overline{CS}$, $\overline{IACK}$	I_{IN}	—	10	50	μA	V_{IN} = 0V to 5.0V V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	—	±2	10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0–D7, TxD, CLK OUT, $\overline{RTS}$, $\overline{DTR}$	V_{OH}	+2.4	—	—	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage D0–D7, TxD, CLK OUT, $\overline{RTS}$, $\overline{DTR}$	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output Leakage Current (Off State) $\overline{IRQ}$, $\overline{DTACK}$	I_{OFF}	—	±2	±10	μA	V_{CC} = 5.25V V_{OUT} = 0 to 2.4V
Power Dissipation	P_D	—	—	10	mW/MHz	
Input Capacitance Except XTALI XTALI	C_{IN}	 — —	 — —	 5 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—		10	pF	

Notes

1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

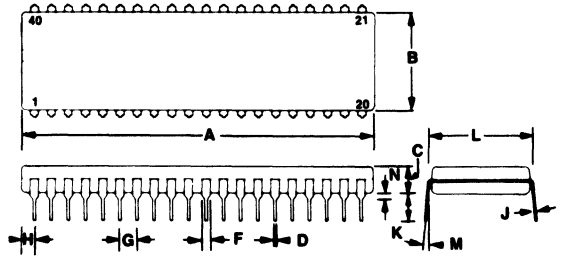
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



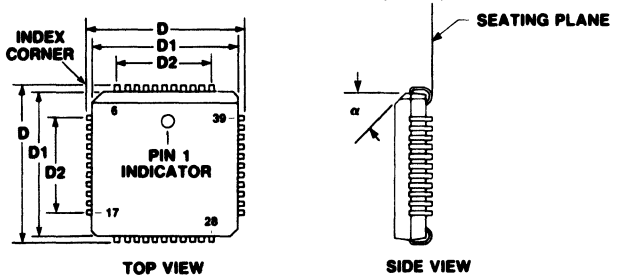
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51 31	1 980	2.020
B	15.11	15.88	0.595	0.625
C	2.54	4.19	0.100	0.165
D	0.38	0 53	0.015	0.021
F	0.76	1.27	0 030	0 050
G	2 54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0 070
J	0 20	0.33	0.008	0 013
K	2 54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1 52	0 020	0 060

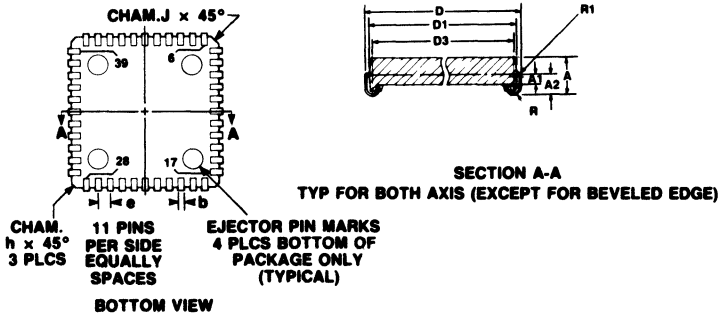
40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3 56	5 08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0 100 BSC	
H	1.65	2 16	0 065	0 085
J	0.20	0.30	0.008	0.012
K	3 30	4.32	0.130	0 170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0 020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4 14	4.39	0.163	0.173
A1	1.37	1 47	0.054	0.058
A2	2.31	2 46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17 45	17.60	0 687	0 693
D1	16.46	16 56	0 648	0.652
D2	12.62	12 78	0 497	0.503
D3	15.75 REF		0 620 REF	
e	1.27 BSC		0.050 BSC	
h	1 15 TYP		0 045 TYP	
J	0.25 TYP		0 010 TYP	
α	45° TYP		45° TYP	
R	0 89 TYP		0 035 TYP	
R1	0 25 TYP		0.010 TYP	

6

Rockwell

R68560, R68561 Multi-Protocol Communications Controller (MPCC)

DESCRIPTION

The R68560, R68561 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 68008/68000 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, two channel DMA interface and three separate interrupt vector numbers optimize MPCC performance to take full advantage of the 68008/68000 processing capabilities and asynchronous bus structure.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYNC) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 22 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC68440/MC68450 DMA Controllers. Three prioritized interrupt vector numbers separately support receiver, transmitter and modem interface operation.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

The 48-pin R68561 supports word-length (16-bit) operation when connected to the 68000 16-bit asynchronous bus, as well as byte-length (8-bit) operation when connected to the 68008 8-bit bus. The 40-pin R68560 supports byte-length operation on the 68008 bus.

FEATURES

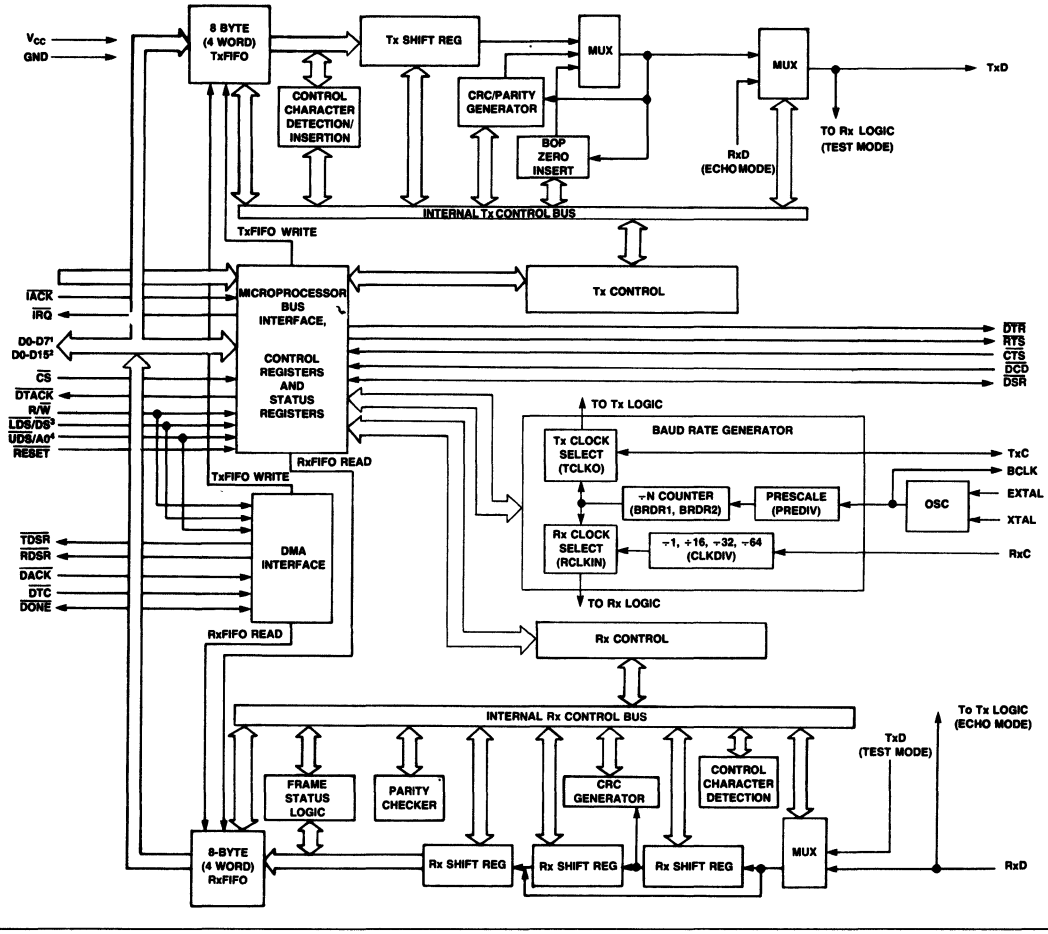
- Full duplex synchronous/asynchronous receiver and transmitter
- Implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, X3.28k, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit oriented protocols (BOP), such as SDLC, HDLC, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and baud rate generator with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 68008/68000 asynchronous bus
- Eight-character receiver and transmitter buffer registers
- 22 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Three separate programmable interrupt vector numbers for receiver, transmitter and serial interface
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer; polled, interrupt and two-channel DMA transfer compatible with MC68440/MC68450
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R6856 —	4 MHz	0°C to 70°C

— Package: C = Ceramic
P = Plastic

— Number of pins: 0 = 40
1 = 48



NOTES:
1. R68560 ONLY.
2. R68561 ONLY.
3. $\overline{UDS}$ ON R68561 A0 ON R68560
4. $\overline{LDS}$ ON R68561 $\overline{DS}$ ON R68560

Figure 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independently of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. For example, R/$\overline{W}$ indicates write is active low and read is active high.

Note: The R68561 interface is described for word mode operation only and the R68560 interface is described for byte mode operation only.

A1–A4—Address Lines. A1–A4 are active high inputs used in conjunction with the $\overline{CS}$ input to access the internal registers. The address map for these registers is shown in Table 1.

D0–D15—Data Lines. The bidirectional data lines transfer data between the MPCC and the MPU, memory or other peripheral device. D0–D15 are used when connected to the 16-bit 68000 bus and operating in the MPCC word mode. D0–D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the MPCC byte mode. The data bus is three-stated when $\overline{CS}$ is inactive. (See exceptions in DMA mode.)

$\overline{CS}$—Chip Select. $\overline{CS}$ low selects the MPCC for programmed transfers with the host. The MPCC is deselected when the $\overline{CS}$ input is inactive in non-DMA mode. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

R/$\overline{W}$—Read/Write. R/$\overline{W}$ controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

$\overline{DTACK}$—Data Transfer Acknowledge. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MPCC after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. $\overline{DTACK}$ is driven high after assertion prior to being tri-stated. A holding resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{DS}$—Data Strobe (R68560). During a write (R/$\overline{W}$ low), the $\overline{DS}$ positive transition latches data on data bus lines D0–D7 into the MPCC. During a read (R/$\overline{W}$ high), $\overline{DS}$ low enables data from the MPCC to data bus lines D0–D7.

$\overline{LDS}$—Lower Data Strobe (R68561). During a write (R/$\overline{W}$ low), the positive transition latches data on the data bus lines D0–D7 (and on D8–D15 if $\overline{UDS}$ is low) into the MPCC. During a read (R/$\overline{W}$ high), $\overline{LDS}$ low enables data from the MPCC to D0–D7 (and to D8–D15 if $\overline{UDS}$ is low).

A0—Address Line A0 (R68560). When interfacing to an 8-bit data bus system such as the 68008, address line A0 is used to access an internal register. A0 = 0 defines an even register and A0 = 1 defines an odd register. See Table 1b.

$\overline{UDS}$—Upper Data Strobe (R68561). When interfacing to a 16-bit data bus system such as the 68000, a low on control bus signal $\overline{UDS}$ enables access to the upper data byte on D8–D15. A high on $\overline{UDS}$ disables access to D8–D15. Data is latched and enabled in conjunction with $\overline{LDS}$.

$\overline{IRQ}$—Interrupt Request. The active low $\overline{IRQ}$ output requests interrupt service by the MPU. $\overline{IRQ}$ is driven high after assertion prior to being tri-stated.

$\overline{IACK}$—Interrupt Acknowledge. The active low $\overline{IACK}$ input indicates that the current bus cycle is an interrupt acknowledge cycle. When $\overline{IACK}$ is asserted the MPCC places an interrupt vector on the lower byte (D0–D7) of the data bus.

$\overline{TDSR}$—Transmitter Data Service Request. When Transmitter DMA mode is active, the low $\overline{TDSR}$ output requests DMA service.

$\overline{RDSR}$—Receiver Data Service Request. When receiver DMA mode is active, the low $\overline{RDSR}$ output requests DMA service.

$\overline{DACK}$—DMA Acknowledge. The $\overline{DACK}$ low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

$\overline{DTC}$—Data Transfer Complete. On a 68000 bus, the $\overline{DTC}$ low input indicates that a DMA data transfer was completed with no bus conflicts. $\overline{DTC}$ in response to a $\overline{RDSR}$ indicates that the data has been successfully stored in memory. $\overline{DTC}$ in response to a $\overline{TDSR}$ indicates that the data is present on the data bus for strobing into the MPCC. If not used, this input should be connected to ground.

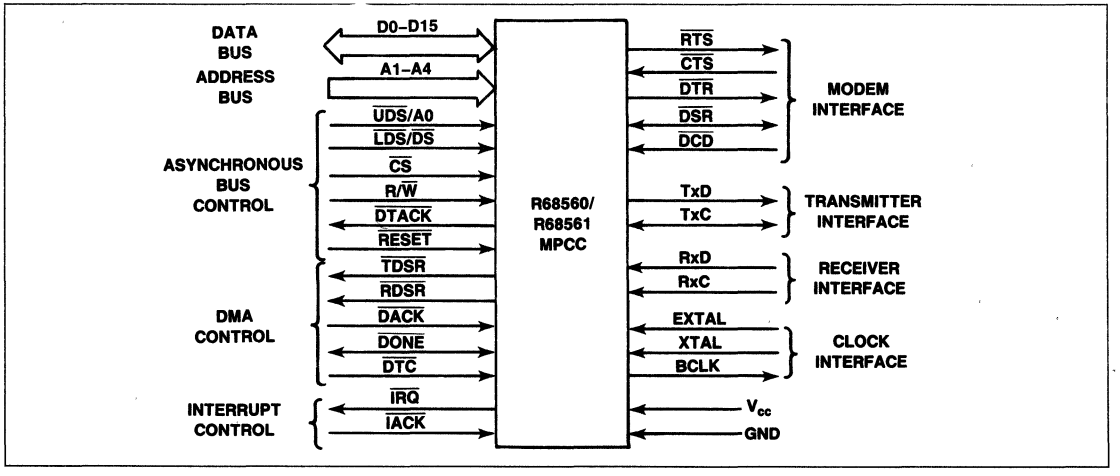


Figure 2. MPCC Input and Output Signals

DONE—Done. DONE is a bidirectional active low signal. The DONE signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or asserted by the MPCC when the status byte following the last character of a frame (block) is being transferred in response to a RDSR. The DONE signal asserted by the DMAC in response to a TDSR will be stored to track with the data byte (lower byte for word transfer) through the TxFIFO.

RESET—Reset. RESET is an active low, high impedance input that initializes all MPCC functions. RESET must be asserted for at least 500 ns to initialize the MPCC.

DTR—Data Terminal Ready. The DTR active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR).

RTS—Request to Send. The RTS active low output is general purpose in nature, and is controlled by the RTSLVL bit in the SICR.

CTS—Clear to Send. The CTS active low input positive transition and level are reported in the CTST and CTSLVL bits in the Serial Interface Status Register (SISR), respectively.

DSR—Data Set Ready. The DSR active low input negative transition and level are reported in the DSRT and DSRLVL bits in the SISR, respectively. DSR is also an output for RSYN.

DCD—Data Carrier Detect. The DCD active low input positive transition and level are reported in the DCDT and DCDLVL bits in the the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of TxC.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the negative going edge of RxC.

TxC—Transmitter Clock. TxC can be programmed to be an input or an output. When TxC is selected to be an input, the transmitter clock must be provided externally. When TxC is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator.

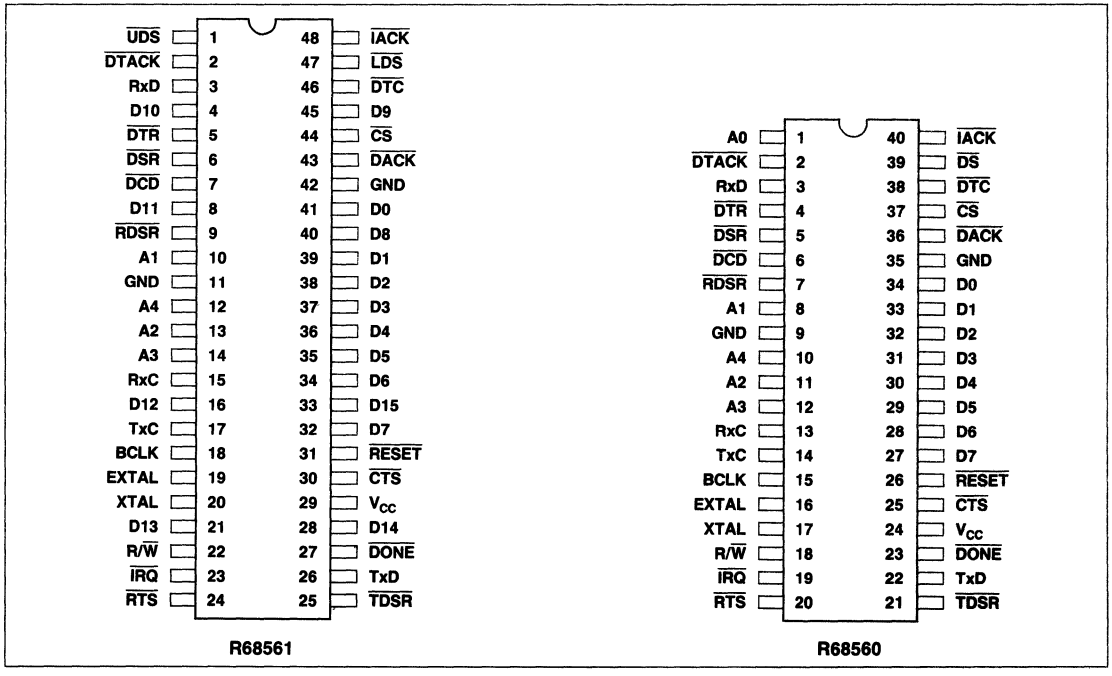
RxC—Receiver Clock. RxC provides the MPCC receiver with received data timing information.

EXTAL—Crystal/External Clock Input.
XTAL Crystal Return. EXTAL and XTAL connect a 20 kHz to 8.064 MHz parallel resonant external crystal to the MPCC internal oscillator (see CLOCK OSCILLATOR). The pin EXTAL may also be used as a TTL level input to supply DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

V_{CC}—Power. 5V ±5%.

GND—Ground. Ground (V_{SS}).



Pin Configuration

MPCC REGISTERS

Twenty-two registers control and monitor the MPCC operation. The registers and their addresses are identified in Table 1a (R68561 operation in word mode) and in Table 1b (R68560 operation in byte mode). When the R68561 is operated in the word mode, two registers are read or written at a time starting at an even boundary. When the R68560 is operated in the byte mode, each register is explicitly addressed based on A0.

Table 2 summarizes the MPCC register bit assignments and their access. A read from an unassigned location results in a read from a "null register." A null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.

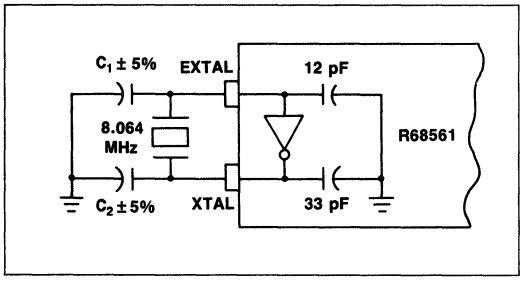
Table 1a. R68561 Accessible Registers (Word Mode)

Register(s)		R/W	Addr (Hex.)	Address Lines A4 A3 A2 A1
15 ——— (Odd Registers) ——— 8	7 ——— (Even Registers) ——— 0			
Receiver Control Register (RCR)	Receiver Status Register (RSR)	R/W	00	0 0 0 0
Receiver Data Register (RDR)—16 bits[1]		R	02	0 0 0 1
Receiver Interrupt Enable Register (RIER)	Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0 0 1 0
Transmitter Control Register (TCR)	Transmitter Status Register (TSR)	R/W	08	0 1 0 0
Transmitter Data Register (TDR)—16 bits[2]		W	0A	0 1 0 1
Transmitter Interrupt Enable Register (TIER)	Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0 1 1 0
Serial Interface Control Register (SICR)	Serial Interface Status Register (SISR)	R/W	10	1 0 0 0
Reserved[3]	Reserved[3]	R/W	12	1 0 0 1
Serial Interrupt Enable Register (SIER)	Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1 0 1 0
Protocol Select Register 2 (PSR2)	Protocol Select Register (PSR1)	R/W	18	1 1 0 0
Address Register 2 (AR2)	Address Register 1 (AR1)	R/W	1A	1 1 0 1
Baud Rate Divider Register 2 (BRDR2)	Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1 1 1 0
Error Control Register (ECR)	Clock Control Register (CCR)	R/W	1E	1 1 1 1

Notes:
1. Accessible register of the four word RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first word.
2. Accessible register of the four word TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first word.
3. Reserved registers may contain random bit values.

CLOCK OSCILLATOR

An on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in the figure below.



A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$C_1 = 2C_L - 12 \text{ pF}$$

$$C_2 = 2C_L - 33 \text{ pF}$$

$$R_s \; / \; R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 20 pF for an 8.064 MHz parallel resonant crystal, then

C_1 = 40 − 12 = 28 pF (Use standard value of 27 pF.)

C_2 = 40 − 33 = 7 pF (Use standard value of 6.8 pF.)

Note: C_X = Total Shunt Capacitance including that due to board layout.

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(8.064 \times 20)^2} = 77 \text{ ohms}$$

Table 1b. R68560 Accessible Registers (Byte Mode)

Register(s)	R/W	Addr (Hex.)	Address Lines A4	A3	A2	A1	A0
7 0							
Receiver Status Register (RSR)	R/W	00	0	0	0	0	0
Receiver Control Register (RCR)	R/W	01	0	0	0	0	1
Receiver Data Register (RDR)—8 bits[1]	R	02	0	0	0	1	0
Reserved[3]		03	0	0	0	1	1
Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0	0	1	0	0
Receiver Interrupt Enable Register (RIER)	R/W	05	0	0	1	0	1
Transmitter Status Register (TSR)	R/W	08	0	1	0	0	0
Transmitter Control Register (TCR)	R/W	09	0	1	0	0	1
Transmitter Data Register (TDR)[2]—8 bits	W	0A	0	1	0	1	0
Reserved[3]		0B	0	1	0	1	1
Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0	1	1	0	0
Transmitter Interrupt Enable Register (TIER)	R/W	0D	0	1	1	0	1
Serial Interface Status Register (SISR)	R/W	10	1	0	0	0	0
Serial Interface Control Register (SICR)	R/W	11	1	0	0	0	1
Reserved[3]		12	1	0	0	1	0
Reserved[3]		13	1	0	0	1	1
Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1	0	1	0	0
Serial Interrupt Enable Register (SIER)	R/W	15	1	0	1	0	1
Protocol Select Register 1 (PSR1)	R/W	18	1	1	0	0	0
Protocol Select Register 2 (PSR2)	R/W	19	1	1	0	0	1
Address Register 1 (AR1)	R/W	1A	1	1	0	1	0
Address Register 2 (AR2)	R/W	1B	1	1	0	1	1
Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0	0
Baud Rate Divider Register 2 (BRDR2)	R/W	1D	1	1	1	0	1
Clock Control Register (CCR)	R/W	1E	1	1	1	1	0
Error Control Register (ECR)	R/W	1F	1	1	1	1	1

Notes:
1. Accessible register of the eight byte RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first byte.
2. Accessible register of the eight byte TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first byte.
3. Reserved registers may contain random bit values.

Table 2. MPCC Register Bit Assignments

R/W Access	Bit Number 7	6	5	4	3	2	1	0	Reset[1] Value	
R/W	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
R/W	0	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABTEN	RRES	01	Receiver Control Register (RCR)
R	RECEIVER DATA (RxFIFO)[2]								— —	Receiver Data Register (RDR)
R/W	RECEIVER INTERRUPT VECTOR NUMBER (RIVN)								0F	Receiver Interrupt Vector Number Register (RIVNR)
R/W	RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0	00	Receiver Interrupt Enable Register (RIER)
R/W	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
R/W	TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
W	TRANSMITTER DATA (TxFIFO)[2]								— —	Transmitter Data Register (TDR)
R/W	TRANSMITTER INTERRUPT VECTOR NUMBER (TIVN)								0F	Transmitter Interrupt Vector Number Register (TIVNR)
R/W	TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	0	00	Transmitter Interrupt Enable Register (TIER)
R/W	CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
R/W	RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0	00	Serial Interface Control Register (SICR)
	RANDOM BIT VALUES									(reserved)
	RANDOM BIT VALUES									(reserved)
R/W	SERIAL INTERRUPT VECTOR NUMBER (SIVN)								0F	Serial Interrupt Vector Number Register (SIVNR)
R/W	CTS IE	DSR IE	DCD IE	0	0	0	0	0	00	Serial Interrupt Enable Register (SIER)
R/W	0	0	0	0	0	0	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
R/W	WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL			00	Protocol Select Register 2 (PSR2)
		SB2	SB1	CL2	CL1	PS3	PS2	PS1		
R/W	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
R/W	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
R/W	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
R/W	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
R/W	0	0	0	PSCDIV	TCLKO	RCLKIN	CLK DIV		00	Clock Control Register (CCR)
							CK2	CK1		
R/W	PAREN	ODDPAR	0	0	CFCRC	CRCPRE	CRC SEL		04	Error Control Register (ECR)
							CR2	CR1		

Notes:
1. RESET = Register contents upon power up or $\overline{\text{RESET}}$.
2. 16-bits for R68561 (word mode); 8-bits for R68560 (byte mode).

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

Address = 00 Reset Value = $00

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by $\overline{\text{RESET}}$. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the next byte or word in the RxFIFO) must be read prior to resetting the corresponding status bit in the RSR. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR
7 RDA —Receiver Data Available. (RSR only).
0 The FxFIFO is empty (i.e., no received data is available).
1 RDA is set and an interrupt issued (if enabled) when the RxFIFO has 1 to 8 bytes, or 1 to 4 words, of data in it.

RDA Reset — RDA cannot be cleared or reset in software. It is initialized to 0 upon hardware reset and remains 0 if no data has been received. It is set to a 1 and an interrupt issued when a data byte/word is loaded to the RxFIFO with the negative edge of RxC coincident with the first bit of the next byte transmitted. It is automatically reset to 0 when the last byte/word is read from the RxFIFO by the host through RDR.

RSR
6 EOF —End of Frame. (BOP and BSC)
0 No end of frame has been detected.
1 The closing flag (BOP) or pad (BSC) has been detected. EOF is loaded in the RxFIFO along with the FSB with which it is associated. The EOF is loaded into the RSR and the interrupt issued, if enabled, (when the RxFIFO read pointer is positioned at the FSB) with the trailing edge of $\overline{\text{LDS}}$.

EOF Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the EOF bit. Then EOF may be reset by writing a 1 to RSR6.

RSR
5 RHW —Receive Half Word. (Frame Status only)*
0 The last word of the frame contains data on the upper half (D8–D15) and frame status on the lower half (D0–D7) of the data bus.
1 The lower half of the data bus (D0–D7) contains the frame status but the upper half (D8–D15) is blank or invalid.

*See Frame Status (RSR) on next page.

RSR
4 C/PERR —CRC/Parity Error.
0 No CRC or parity error detected.
1 CRC error detected (BOP, BSC) or parity error detected (ASYNC, ISOC and COP). The C/PERR bit is loaded into the RxFIFO with the negative-going RxC edge, along with the byte or word with which it is associated. For ASYNC, ISOCH or COP protocols, this is with the byte/word containing a parity error. For BOP or BSC, it is loaded to RxFIFO (after the CRC check) with the FSB. C/PERR is loaded into the RSR and the interrupt issued (when the read pointer is positioned at the FSB) with the trailing edge of $\overline{\text{LDS}}$.

C/PERR Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the C/PERR bit. Then it may be reset by writing a 1 to RSR4.

RSR
3 FRERR —Frame Error.
0 No frame error detected.
1 FRERR is set for receiver overrun, flag detected off boundary (BOP), or frame error (ASYNC, ISOCH). For receiver overrun, the FRERR bit is set in the RxFIFO with the last byte when the overrun is detected.

For BOP, a minimum message size is an opening flag, one address byte and one control byte. If the closing flag is detected before the control byte is sent, a short frame is indicated and a frame error results. For address extension, multi-address bytes may be received before the control byte is expected. The FRERR bit is latched in RxFIFO with the negative-going edge of RxC with the last address byte received upon detection of the flag off boundary. FRERR is loaded into the RSR and the interrupt issued when the read pointer is positioned at the FSB with the trailing edge of $\overline{\text{LDS}}$.

In ASYNC or ISOCH, a FRERR bit set indicates that the stop bit was detected off boundary (too early or too late for the number of bits expected by the setting of PSR2-3 and PSR2-4) or it was not the correct width (as expected by the setting of PSR2-6 and PSR2-5).

FRERR Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the C/PERR bit. The C/PERR bit may then be reset by writing a 1 to RSR3.

RSR
2 ROVRN —Receiver Overrun.
0 No receiver overrun detected.
1 Receiver overrun detected. Data is loaded into the RxFIFO on byte boundaries with the negative-going edge of RxC coincident with the first bit of the subsequent data being received. When the eighth byte, or fourth word, of data has been written into RxFIFO without any data being read out, the RxFIFO is full and the incremented write pointer "catches up" with the read pointer. The next attempt to write data to RxFIFO causes ROVRN bit to be loaded to the RSR and the interrupt issued (if enabled). The data in the RxFIFO is not affected, but new received data is lost.

ROVRN Reset — The ROVRN bit is not self-clearing when data is read from the RxFIFO, but may be reset by writing a 1 to RSR2.

RSR

1 RA/B —Receiver Abort/Break.

0 Normal Operation.

1 (BOP) When an ABORT (seven 1s) is detected after the opening flag, the RA/B bit is set in the RSR and an interrupt issued (if enabled). This bit is latched with the negative edge of RxC after the seventh 1 bit is detected. (NOTE: Because the previous byte can end in zero to five 1 bits, the abort could be recognized in the next byte as early as two to seven 1 bits.)

(BSC) When ENQ is detected in a block of text data, the RA/B bit is set in the RSR and the interrupt issued (if enabled) with the next negative edge of the RxC clock.

RA/B Reset — The RA/B bit is reset by writing a 1 to RSR1.

RSR

0 RIDLE —Receiver Idle. (BOP only).

0 Receiver is not idle.

1 15 or more 1s have been detected. The RIDLE bit is set in RSR with the negative edge of the next RxC after 15 consecutive 1s have been detected.

RIDLE Reset — The RIDLE is reset by writing a 1 to RSR0. (NOTE: The RIDLE bit will set again in 15 clock cycles if RxD is still in the idle condition.)

*Frame Status (RSR)

7	6	5	4	3	2	1	0
0	EOF	RHW	C/PERR	FRERR	ROVRN	RA/B	0

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the RxFIFO following the last data byte of each block. The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE. But, in addition to the RSR contents, the frame status byte has a RHW status in bit 5 which indicates either an even or odd boundary (applicable to word mode only).

If the MPCC is in word mode and the last data byte was on an even byte boundary (i.e., there was an even number of bytes in the message), a blank byte will be loaded into the RxFIFO prior to loading the frame status byte in order to force the "frame status" byte and the next frame to be on an even boundary. When RHW = 0, the last word of the frame contains data on the upper half and status on the lower half of the data bus. If RHW = 1, the lower half of the bus contains status but the upper half is a blank or invalid byte.

In the byte mode, the status byte will always immediately follow the last data byte of the block/frame (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the RxFIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
—	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABEN	RRES

Address = 01 Reset value = $01

The Receiver Control Register (RCR) selects receiver control options.

RCR

7 —Not used.

RCR

6 RDSREN —Receiver Data Service Request Enable.

0 Disable receiver DMA mode.

1 Enable receiver DMA mode.

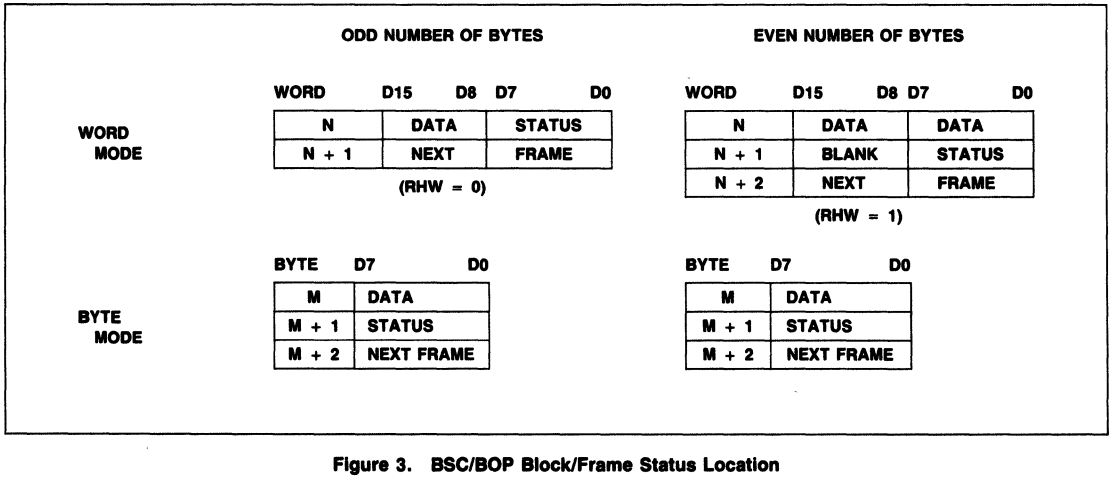


Figure 3. BSC/BOP Block/Frame Status Location

RCR
5 DONEEN —$\overline{\text{DONE}}$ Output Enable.
0 Disable $\overline{\text{DONE}}$ output.
1 Enable $\overline{\text{DONE}}$ output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR
4 RSYNEN —RSYNEN Output Enable. Selects the DSR signal input or the RSYN SYNC signal output on the $\overline{\text{DSR}}$ pin.
0 Input DSR on $\overline{\text{DSR}}$.
1 Output RSYN on $\overline{\text{DSR}}$.

RCR
3 STRSYN —Strip SYN Character (COP only).
0 Do not strip SYN character.
1 Strip SYN character.

RCR
2 MUST BE ZERO
0

RCR
1 RABTEN —Receiver Abort Enable (BOP only).
0 Do not abort frame upon error detection.
1 Abort frame upon RxFIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame. (EOF is set upon abort).

RCR
0 RRES —Receiver Reset Command.
0 Enable normal receiver operation.
1 Reset receiver. Resets the receiver section including the RxFIFO and the RSR (but not the RCR). RRES is set by $\overline{\text{RESET}}$ or by writing a 1 into this bit and must be cleared by writing a 0 into this bit. RRES requires clearing after $\overline{\text{RESET}}$.

Receiver Data Register (RDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1			LSB		MSB			Byte 0			LSB	

Address = 02

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0			LSB	

Address = 02

The receiver has an 8-byte (or 4-word) First In First Out (FIFO) register file (RxFIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the RxFIFO via the RDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. When the RxFIFO has a data byte/word ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Vector Number Register (RIVNR)

7	6	5	4	3	2	1	0
Receiver Interrupt Vector Number (RIVN)							

Address = 04 Reset value = $0F

If a receiver interrupt condition occurs (as reported by status bits in the RSR that correspond to interrupt enable bits in the RIER) and the corresponding bit is set in the RIER, $\overline{\text{IRQ}}$ output is asserted to request MPU receiver interrupt service. When the $\overline{\text{IACK}}$ input is asserted from the bus, the Receiver Interrupt Vector Number (RIVN) from the Receiver Interrupt Vector Number Register (RIVNR) is placed on the data bus.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0

Address = 05 Reset value = $00

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the $\overline{\text{IRQ}}$ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER
7 RDA IE —Receiver Data Available Interrupt Enable.
0 Disable RDA Interrupt.
1 Enable RDA Interrupt.

RIER
6 EOF IE —End of Frame Interrupt Enable.
0 Disable EOF Interrupt.
1 Enable EOF Interrupt.

RIER
5 —Not used.

RIER
4 C/PERR IE —CRC/Parity Error Interrupt Enable.
0 Disable C/PERR Interrupt.
1 Enable C/PERR Interrupt.

RIER
3 FRERR IE —Frame Error Interrupt Enable.
0 Disable FRERR Interrupt.
1 Enable FRERR Interrupt.

RIER
2 ROVRN IE —Receiver Overrun Interrupt Enable.
0 Disable ROVRN Interrupt.
1 Enable ROVRN Interrupt.

RIER
1 RA/B IE —Receiver Abort/Break Interrupt Enable.
0 Disable RA/B Interrupt.
1 Enable RA/B Interrupt.

RIER
0 —Not used.

TRANSMITTER REGISTERS

Transmitter Status Register (TSR)

7	6	5	4	3	2	1	0
TDRA	TFC	0	0	0	TUNRN	TFERR	0

Address = 08 Reset value = $80

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by RESET. The IRQ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR
7 TDRA —Transmitter Data Register Available.
0 The TxFIFO is full.
1 The TxFIFO is available to be loaded via the TDR (1 to 8 bytes, or 1 to 4 words).

TDRA Reset — TDRA cannot be reset by the host in normal operation. It initializes to a 1 upon hardware or software reset of the MPCC. TDRA is not dependent on the serial clock.

TSR
6 TFC —Transmitted Frame Complete. (BOP, BSC and COP only).
0 (All) Frame not complete.
1 (BOP) Closing flag or ABORT has been transmitted. The TFC bit is set and the interrupt issued (if enabled) with the negative edge of TxC coincident with the end of the last bit of the flag. When TABT is set in TCR1, an ABORT is transmitted immediately but TFC is not issued until after the closing flag or 8 bits of the MARK idle condition after the TxFIFO is flushed of all current data bytes.

(BSC) Trailing pad has been transmitted. TFC bit set and/or interrupt issued with negative edge of TxC coincident with the end of the last bit of the trailing pad.

(COP) Last byte has been transmitted (TLAST set in TCR3). TFC bit set and/or interrupt issued with negative edge of the TxC coincident with the end of the last bit of the last byte.

TFC Reset — One full cycle of the serial clock (TxC) must elapse before the TFC bit can be reset by writing a 1 to TSR6.

TSR
5-3 —Not used.

TSR
2 TUNRN —Transmitter Underrun (BOP, BSC and COP only).
0 No TxFIFO underrun has occurred.
1 An empty TxFIFO was accessed for data.
(BOP) Underrun is treated as an ABORT in that eight consecutive 1s are transmitted followed by the idle condition of MARK or FLAG.

(BSC, COP) Underrun causes SYN characters to be transmitted until new data is available in the TxFIFO.

The TUNRN bit is set in TSR2 and the interrupt issued with the positive edge of the TxC coincident with the eighth bit of data prior to the ABORT in BOP or to SYN in BSC or COP.

TUNRN Reset — One full cycle of the serial clock (TxC) must elapse before the TUNRN bit can be reset by writing a 1 to TSR2.

TSR
1 TFERR —Transmit Frame Error (BOP only).
0 No frame error has occurred.
1 A short frame condition exists in that no control field is transmitted. (TLAST was issued early with an address byte.) TFERR bit is set and the interrupt issued with the positive edge of TxC coincident with the end of the last bit of the byte causing the error.

TFERR Reset — One full cycle of the serial clock (TxC) must elapse before TFERR bit can be reset by writing a 1 to TSR1.

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES

Address = 09 Reset value = $01

The Transmitter Control Register (TCR) selects transmitter control function.

TCR
7 TEN —Transmitter Enable.
0 Disable transmitter. TxD output is idled. The TxFIFO may be loaded while the transmitter is disabled.
1 Enable transmitter.

TCR
6 TDSREN —Transmitter Data Service Request Enable.
0 Disable transmitter DMA mode.
1 Enable transmitter DMA mode.

TCR
5 TICS —Transmitter Idle Character Select. Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).
0 Mark Idle (TxD output is held high).
1 Content of AR2 (BSC and COP), BREAK condition (ASYNC and ISOC), or FLAG character (BOP).

TCR
4 THW —Transmit Half Word. (R68561, word mode only). This bit is used when the frame or block ends on an odd boundary in conjunction with the TLAST bit and indicates that the last word in the TxFIFO contains valid data in the upper byte only. This bit must always be 0 in byte mode (R68560).
0 Transmit full word (16 bits) from the TxFIFO.
1 Transmit upper byte (8 bits) from the TxFIFO.

TCR

3 TLAST —Transmit Last Character (BOP, BSC and COP only).

0 The next character is not the last character in a frame or block.

1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the TxFIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by DONE from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR

2 TSYN —Transmit SYN (BSC and COP only)

0 Do not transmit SYN characters.

1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR

1 TABT —Transmit ABORT (BOP only).

0 Enable normal transmitter operation.

1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the TxFIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the TxFIFO.

TCR

0 TRES —Transmitter Reset Command.

0 Enable normal transmitter operation.

1 Reset transmitter. Clears the transmitter section including the TxFIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by RESET or by writing a 1 into this bit and is cleared by writing a 0 into this bit. TRES requires clearing after RESET.

Transmit Data Register (TDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1			LSB		MSB			Byte 0			LSB	

Address = 0A

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0			LSB	

Address = 0A

The transmitter has an 8-byte (or 4-word) FIFO register file (TxFIFO). Data to be transmitted is transferred from the bus into the TxFIFO via the TDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. The TDRA status bit in the TSR is set to 1 when the TxFIFO is ready to accept another data word/byte.

Transmitter Interrupt Vector Number Register (TIVNR)

7	6	5	4	3	2	1	0
Transmitter Interrupt Vector Number (TIVN)							

Address = 0C Reset value = $0F

If a transmitter interrupt condition occurs (as reported by status bits in the TSR that correspond to interrupt enable bits in the TIER) and the corresponding bit in the TIER is set, the IRQ output is asserted to request MPU transmitter interrupt service. When the IACK input is asserted from the bus, the Transmitter Interrupt Vector Number (TIVN) from the Transmitter Interrupt Vector Number Register (TIVNR) is placed on the data bus.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	—

Address = 0D Reset value = $00

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the IRQ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER

7 TDRA IE —Transmitter Data Register (TDR) Available Interrupt Enable.

0 Disable TDRA Interrupt.

1 Enable TDRA Interrupt.

TIER

6 TFC IE —Transmit Frame Complete (TFC) Interrupt Enable.

0 Disable TFC Interrupt.

1 Enable TFC Interrupt.

TIER

5-3 —Not used.

TIER

2 TUNRN IE —Transmitter Underrun (TUNRN) Interrupt Enable.

0 Disable TUNRN Interrupt.

1 Enable TUNRN Interrupt.

TIER

1 TFERR IE —Transmit Frame Error (TFERR) Interrupt Enable.

0 Disable TFERR Interrupt.

1 Enable TFERR Interrupt.

TIER

0 —Not used.

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0

Address = 10 Reset value = $00

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTST, DSRT and DCDT) are cleared by writing a 1 into their respective positions, or by RESET. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The IRQ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR
7 CTST —Clear to Send Transition Status.
0 The input on CTS has not transitioned positive.
1 The input on CTS has transitioned positive from active to inactive. To detect this transition, RTS must be active (low) and the transmitter must be enabled (TRES in TCR0 = 0). The CTST bit is set in SISR7 and an interrupt issued (if enabled) with the negative edge of TxC.

CTST Reset — A negative transition of the serial clock (TxC) must occur after the CTS input goes high before the CTST bit can be reset by writing a 1 to SISR7.

SISR
6 DSRT —Data Set Ready Transition Status.
0 The input on DSR has not transitioned negative.
1 The input on DSR has transitioned negative from inactive to active. The DSRT bit is set in SISR7 and an interrupt issued (if enabled) with the negative edge of RxC. The receiver must be enabled (RRES in RCR0 = 0).

DSRT Reset — A negative transition of the serial clock (RxC) must occur after the DSR input goes high before the DSRT bit can be reset by writing a 1 to SISR6.

SISR
5 DCDT —Data Carrier Detect Transition Status.
0 The input on DCD has not transitioned positive.
1 The input on DCD has transitioned positive from active to inactive. The DCDT bit is set in SISR5 and an interrupt issued (if enabled) with the negative edge of RxC. The receiver must be enabled (RRES in RCR0 = 0).

DCDT Reset — A negative transition of the serial clock (RxC) must occur after the DCD input goes high before the DCDT bit can be reset by writing a 1 to SISR5.

SISR
4 CTSLVL —Clear to Send Level.
0 The input on CTS is negated (high, inactive).
1 The input on CTS is asserted (low, active).

CRSLVL Reset — The CTSLVL bit in SISR4 follows the state of the input to CTS and cannot be reset internally.

SISR
3 DSRLVL —Data Set Ready Level.
0 The input on DSR is negated (high, inactive).
1 The input on DSR is asserted (low, active).

DSRLVL Reset — The DSRLVL bit in SISR3 follows the state of the input to DSR and cannot be reset internally.

SISR
2 DCDLVL —Data Carrier Detect Level.
0 The input on DCD is negated (high, inactive).
1 The input on DCD is asserted (low, active).

DCDLVL Reset — The DCDLVL bit in SISR2 follows the state of the input to DCD and cannot be reset internally.

SISR
1-0 —Not used.

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0

Address = 11 Reset value = $00

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR
7 RTSLVL —Request to Send Level.
0 Negate RTS output (high).
1 Assert RTS output (low).

NOTE

In BOP, BSC, or COP, when the RTSLVL bit is cleared in the middle of data transmission, the RTS output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the RTS output is negated when the TxFIFO is empty. If the transmitter is idling when the RTSLVL bit is reset, the RTS output is negated within two bit times.

SICR
6 DTRLVL —Data Terminal Ready Level.
0 Negate DTR output (high).
1 Assert DTR output (low).

SICR
5-3 —Not used. These bits are initialized to 0 by RESET and must not be set to 1.

SICR
2 ECHO —Echo Mode Enable.
0 Disable Echo mode (enable normal operation).
1 Enable Echo mode. Received data (RxD) is routed back through the transmitter to TxD. The contents of the TxFIFO is undisturbed. This mode may be used for remote test purposes.

SICR
1 TEST —Self-test Enable.
0 Disable self-test (enable normal operation).
1 Enable self-test. The transmitted data (TxD) and clock (TxC) are routed back through to the receiver through RxD and RxC, respectively (DCD and CTS are ignored). This "loopback" self-test may be used for all protocols. RxC is external and CCR bits 2 and 3 must be a 1.

SICR
0 MUST BE ZERO
0

Serial Interrupt Vector Number Register (SIVNR)

7	6	5	4	3	2	1	0
Serial Interrupt Vector Number (SIVN)							

Address = 14 Reset value = $0F

If a serial interface interrupt condition occurs (as reported by status bits in the SISR that correspond to interrupt enable bits in the SIER) and the corresponding bit in the SIER is set, the $\overline{IRQ}$ output is asserted to request MPU serial interface interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Serial Interrupt Vector Number (SIVN) from the Serial Interrupt Vector Number Register (SIVNR) is placed on the data bus.

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	0	0	0	0	0

Address = 15 Reset value = $00

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the $\overline{IRQ}$ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER
7 CTS IE —Clear to Send (CTS) Interrupt Enable.
0 Disable CTS Interrupt.
1 Enable CTS Interrupt.

SIER
6 DSR IE —Data Set Ready (DSR) Interrupt Enable.
0 Disable DSR Interrupt.
1 Enable DSR Interrupt.

SIER
5 DCD IE —Data Carrier Detect (DCD) Interrupt Enable.
0 Disable DCD Interrupt.
1 Enable DCD Interrupt.

SIER
4-0 —Not used.

GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES in the TCR and RRES in the RCR should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTLEX	ADDEX

Address = 18 Reset value = $00

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1
7-2 —Not used.

PSR1
1 CTLEX —Control Field Extend (BOP only).
0 Select 8-bit control field.
1 Select 16-bit control field.

PSR1
0 ADDEX —Address Extend (BOP only).
0 Disable address extension. All eight bits of the address byte are utilized for addressing.
1 Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL		
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Address = 19 Reset value = $00

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2
7 WD/BYT —Data Bus Word/Byte Mode.
0 Select byte mode. Selects the number of data bits to be transferred from the RxFIFO and the registers to the data bus and to be transferred from the data bus to the TxFIFO and the registers. The MPCC is initialized by $\overline{RESET}$ to the byte mode.
1 Select word mode. For operation with the 16-bit bus, select the word mode by sending $80 on D7–D0 to address $19 prior to transferring subsequent data between the MPCC and the data bus.

PSR2
6-5 STOP BIT SEL —Number of Stop Bits Select. Selects the number of stop bits transmitted at the end of the data bits in ASYNC and ISOC modes.

6 SB2	5 SB1	No. of Stop Bits ASYNC	No. of Stop Bits ISOC
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2

4-3 CHAR LEN SEL —Character Length Select. Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.

4 CL2	3 CL1	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2

2-0 PROTOCOL SEL—Protocol Select. Selects protocol and defines the protocol dependent control bits.

2 PS3	1 PS2	0 PS1	Protocol
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYNC
1	1	1	ISOC

Address Register 1 (AR1) Address

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Address = 1A Reset value = $00

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BSC & COP SYN							

Address = 1B Reset value = $00

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of AR1 is used for address matching. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	AR1	AR2
BOP (Primary)	X	X
BOP (Secondary)	Address	X
BSC EBCDIC	Leading PAD	SYN
BSC ASCII	Leading PAD	SYN
COP	Leading PAD	SYN
*X = Not used		

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Address = 1C Reset value = $01

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

Address = 1D Reset value = $00

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH), With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{\text{(Prescaler Divider) (Baud Rate) (K)}}$$

where: K = 1 for isochronous or synchronous
2 for asynchronous

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
0	0	0	PSCDIV	TCLKO	RCLKIN	CLK DIV	
						CK2	CK1

Address = 1E Reset value = $00

The CCR selects various clock options.

CCR

7-5 —Not used.

CCR

4 PSCDIV —Prescaler Divider. The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.

0 Divide by 2.
1 Divide by 3.

CCR

3 TCLKO —Transmitter Clock Output Select.

0 Select TxC to be an input.
1 Select TxC to be an output. (1X clock)

Table 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bit Rate)	Prescaler Divider		Baud Rate Divider					
			Asynchronous			Isochronous and Synchronous		
				Hexadecimal Value			Hexadecimal Value	
	Decimal Value	PSCDIV (0 to 1)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	8C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

CCR

2 RCLKIN —Receiver Clock Internal Select (ASYNC only).

0 Select External RxC.
1 Select Internal RxC.

CCR

1-0 CLK DIV —External Receiver Clock Divider. Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider
0	0	1 (ISOC)
0	1	16
1	0	32 (ASYNC) only
1	1	64

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CFCRC	CRCPRE	CRCSEL	
						CR2	CR1

Address = 1F Reset value = $04

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR

7 PAREN —Parity Enable. (ASYNC, ISOC and COP only).

0 Disable parity generation/checking.
1 Enable parity generation/checking.

ECR

6 ODDPAR —Odd/Even Parity Select (Effective only when PAREN = 1).

0 Generate/check even parity.
1 Generate/check odd parity.

ECR

5-4 —Not used.

ECR

3 CFCRC —Control Field CRC Enable. (BOP Only)

0 Disable control field CRC.
1 Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR

2 CRCPRE —CRC Generator Preset Select. (BOP, BSC Only)

0 Preset CRC Generator to 0. (For BSC)
1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder. (For BOP)

ECR

1-0 CRCSEL —CRC Polynomial Select. Selects one of the RC polynominals.

1 CR2	0 CR1	Polynominal
0	0	$x^{16}+x^{12}+x^5+1$ (CCITT V.41) (BOP)
0	1	$x^{16}+x^{15}+x^2+1$ (CRC-16) (BSC)
1	0	x^8+1 (VRC/LRC)* (BSC, ASCII, non-transparent)
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals:

	R68561	R68560
Address Lines	A1–A4	A0–A4
Data Lines	D0–D15	D0–D7
Read/Write	R/$\overline{W}$	R/$\overline{W}$
Data Transfer Acknowledge	$\overline{DTACK}$	$\overline{DTACK}$
Chip Select	$\overline{CS}$	$\overline{CS}$
Data Strobes	$\overline{UDS}$ and $\overline{LDS}$	$\overline{DS}$

Figures 10 and 11 show typical interface connections.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the MPCC for access to the internal registers and other operations. When $\overline{CS}$ is asserted, the data I/O buffer acts as an output driver during a read operation and as an input buffer during a write operation. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

When the R68561 is connected to the 16-bit bus for operation in the word mode (WD/BYT = 1 in the PSR2), address lines A1–A4 select the internal register(s) (the 8-bit control/status registers are accesed two at a time and the 16-bit data registers are accessed on even address boundaries). When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), 16 bits of register data are placed on the data bus when the data strobes ($\overline{LDS}$ and $\overline{UDS}$) are asserted. $\overline{LDS}$ strobes the eight data bits from the even numbered registers to the lower data bus lines (D0–D7) and $\overline{UDS}$ strobes the eight data bits from the odd numbered registers to the upper data bus lines (D8–D15). The MPCC asserts Data Transfer Acknowledge ($\overline{DTACK}$) prior to placing data on the data bus. Conversely, when the MPCC is selected ($\overline{CS}$ low) during a write (R/$\overline{W}$ low) $\overline{LDS}$ and $\overline{UDS}$ strobe data from the D0–D7 and D8–D15 data bus lines into the addressed even and odd numbered registers, respectively, and the MPCC asserts $\overline{DTACK}$. $\overline{DTACK}$ is negated when $\overline{CS}$ is negated. Figures 12 and 13 show the read and write timing relationships.

When the R68560 is connected to the 8-bit bus for operation in the byte mode (WD/BYT = 0 in the PSR2), address lines A0–A4 select one internal 8-bit register. When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), eight bits of register data are placed on data bus lines D0–D7 when the data strobe ($\overline{DS}$) is asserted. When the MPCC is selected ($\overline{CS}$ low) for a write (R/$\overline{W}$ low), $\overline{DS}$ strobes data from the D0–D7 data lines into the selected register.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers at up to 2 Mbytes per second when used with the MC68440 or MC68450 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which requires a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input ($\overline{DACK}$) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/$\overline{W}$ input to distinguish between the Transmitter Data Service Request ($\overline{TDSR}$ acknowledge and the Receiver Data Service Request ($\overline{RDSR}$) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the RxFIFO, Receiver Data Service Request ($\overline{RDSR}$) is asserted for one receiver clock period (BOP and BSC) to initiate the MPCC to memory DMA transfer. For asynchronous operation, $\overline{RDSR}$ is asserted for 2–3 periods of the system clock depending on prescale factor. The next $\overline{RDSR}$ cycle may be initiated as soon as the current $\overline{RDSR}$ cycle is completed (i.e., a full sequence of $\overline{DACK}$, $\overline{DS}$, and $\overline{DTC}$).

In response to $\overline{RDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to write, asserts the memory address, address strobe, and DMA acknowledge. The MPCC outputs data from the RxFIFO to the data bus and the DMAC asserts the data strobes. The memory latches the data and asserts $\overline{DTACK}$ to complete the data transfer. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data transfer is complete. Figure 14 shows the timing relationships for the receiver DMA mode.

$\overline{RDSR}$ is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when $\overline{RESET}$ is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the TxFIFO is available, Transmitter Data Service Request ($\overline{TDSR}$) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. For asynchronous operation, $\overline{TDSR}$ is asserted for a period of one-half the transmitter baud rate. The next $\overline{TDSR}$ cycle may be initiated as soon as the current $\overline{TDSR}$ cycle is completed.

In the transmitter DMA mode, the TxFIFO Is implicitly addressed. That is, when the transfer is from memory to the TxFIFO, only the memory is addressed. In response to $\overline{TDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to read, asserts the memory address, the address strobe, the data strobes and DMA acknowledge. The memory places data on the data bus and asserts $\overline{DTACK}$. Data is valid at this time and will remain valid until the data strobes are negated. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data is available. The MPCC loads the data into the TxFIFO on the negation (rising edge) of $\overline{DS}$ and the transfer is complete. When a TxFIFO underrun occurs, the TUNRN bit is set in TSR2, the interrupt is issued, and the ABORT sequence is entered (eight consecutive 1s are transmitted). The next word/byte in TxFIFO clears the ABORT bit and the idle mode is entered. When a transmission is aborted, it is expected that the interrupt will allow the host system to decide the next course of action; probably to reset the DMAC and retransmit the message. A timing diagram for the transmitter DMA Mode is shown in Figure 15.

$\overline{TDSR}$ is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when $\overline{RESET}$ is asserted.

DONE Signal

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts DONE which sets the TLAST bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode of operation, DONE is issued by the MPCC on an MPCC-to-memory transfer when the last byte/word is being transferred from the RxFIFO to the data bus (if DONEEN bit is set in RCR5). In the byte mode, this is the Frame Status Byte (FSB). In the word mode, this is the last data byte and FSB (for an odd number of data byte transfers) or FSB and blank (for an even number of data byte transfers).

DONE is asserted as a result of the FSB being transferred and not as a result of the error conditions. The EOF, C/PERR and FRERR are addendum bits in the RxFIFO which are written to FIFO when they occur and follow the data through the FIFO. The frame is aborted upon overrun or error detection if RCR1 = 1.

CAUTION

DONE is reasserted with each occurrence of DACK until EOF is cleared in the RSR.

INTERRUPTS

If an interrupt generating status occurs and the interrupt is enabled, the MPCC asserts the IRQ output. Upon receiving IACK for the pending interrupt request, the MPCC places an interrupt vector on D0-D7 data bus and asserts DTACK.

The MPCC has three vector registers: Receiver Interrupt Vector Number Register (RIVNR), Transmitter Interrupt Vector Number Register (TIVN), and Serial Interrupt Vector Number Register (SIVNR). The receiver interrupt has priority over the transmitter interrupt, and the transmitter interrupt has priority over the serial interface interrupt. For example, if a pending interrupt request has been generated simultaneously by the receiver and the transmitter, the Receiver Interrupt Vector Number (RIVN) is placed on D0-D7 when acknowledged by the MPU. Upon completion of the first interrupt request cycle (which clears the receiver interrupt), IRQ will remain low to start the transmitter interrupt cycle. IRQ is negated by clearing all bits set in a status register that could have caused the interrupt.

CAUTION

A higher priority interrupt occuring while IACK is low during transfer of a lower priority interrupt vector to the MPU will cause the lower priority interrupt vector on the data bus to be invalid if there are any 1's in the higher priority interrupt vector in the same bit poositions as any 0's in the lower priority interrupt vector. To prevent this problem from occuring, ensure that the higher priority interrupt vectors contain 1's only in bit positions where there are 1's in the lower priority interrupt vectors, e.g.:

Vector	Vector Value (Hex)	Vector Value (Binary)
Receiver Interrupt Vector Number (RIVN)	44	01000100
Transmitter Interrupt Vector Number (TIVN)	4C	01001100
Serial Interrupt Vector Number (SIVN)	5C	01011100

A timing diagram for the interrupt acknowledge sequence is shown in Figure 16.

SERIAL INTERFACE

The MPCC is a high speed, high performance device supporting the more popular bit and character oriented data protocols. The lower speed asynchronous (ASYNC) and isochronous (ISOCH) modes are also supported. An on-chip clock oscillator and baud rate generator provide an output data clock at a frequency of DC to a 4 MHz.. The clock can also be used in the ASYNC mode to provide a receive clock for the incoming data. The serial interface consists of the following signals:

RTS (Request to Send) Output

The RTS output to the DCE is controlled by the RTSLVL bit in the SICR inn conjunction with the state of the transmitter section. When the RTSLVL bit is set to 1, the RTS output is asserted. When the RTSLVL bit is reset to 0 (no sooner than one full cycle of TxC after transmission has started), the RTS output remains asserted until the TxFIFO becomes empty, or the end of the message (or frame), complete with CRC code (if any), closing flag, and one full cycle of idle has been transmitted. RTS also is negated when the RTSLVL bit is reset during transmitter idle, or when the RESET input is asserted.

CTS (Clear to Send) Input

The CTS input signal is normally generated by the DCE to indicate whether or not the data set is ready to receive data. The CTST bit in the SISR reflects the transition status of the CTS input while the CTSLVL bit in the SISR reflects the current level. A positive transition on the CTS pin asserts IRQ if the CTS IE bit in the SIER is set. The CTS input in an inactive state disables the start of transmission of each frame.

DCD (Data Carrier Detect) Input

The DCD input signal is normally gnerated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The DCDT bit in the SISR reports the transition status of the DCD input while the DCDLVL bit in the SISR contains the current level. A positive transition on the DCD pin asserts the IRQ output if the DCD IE bit in the SIER is set. A negated DCD input disables the start of the receiver but does not stop the operation of an incoming message already in progress.

$\overline{DSR}$ (Data Set Ready) Input/RSYN Output

The DSRT input from the DCE indicates the status of the local set. The DSRT bit in the SISR contains the transition status of the $\overline{DSR}$ input while the DSRLVL bit in the SISR reports the current level. A negative transition on the $\overline{DSR}$ pin asserts the $\overline{IRQ}$ output if the DSR IE bit in the SIER is set.

The $\overline{DSR}$ pin is used as an output for RSYN when enabled by a 1 in RSR4 (RSYNEN = 1). DSR output low indicates detection of a SYN (non-transparent) in BSC or COP protocols or DLE-SYN pair (transparent) in BSC protocol. It is asserted as a negative-going pulse one-bit time after the end of the SYN byte and lasts for one full serial clock cycle before being reset.

In BOP protocol, RSYN is asserted as a result of address match at the beginning of a frame. It is asserted one bit time after the end of the address byte(s) if an address match is made, and lasts for one full serial clock cycle.

$\overline{DTR}$ (Data Terminal Ready) Output

The $\overline{DTR}$ output is general purpose in nature and can be used to control switching of the DCE. The $\overline{DTR}$ output is controlled by the DTRLVL bit in the SICR.

TxC (Transmitter Clock) Input/Output

The transmitter clock (TxC) may be programmed to be input or an output. When the TCLKO control bit in the CCR is set to a 1, the TxC pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the TCKLO control bit is reset, TxC is an input and the transmitter shift timing must be provided exernally. The TxD output changes state on the negative-going edge of the transmitter clock. In the asynchronous mode when TCLKO = 0 in the CCR, the TxC input frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in NRZ data format. The first byte of a message transmitted out of the R68561 MPCC is the even byte of the 68000 bus (D8–D15). It is transmitted least significant bit (LSB) first.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the RxC.

RxD (Received Data) Input

The serial data received by the MPCC is in NRZ data format. The first byte received in the MPCC RXFIFO is output to the 68000 bus on (D8–D15).

Serial Interface Timing

The timing for the serial interface clock and data lines is shown in Figure 18. The MPCC supports high speed synchronous operation. As shown, the TxD output changes with the negative-going edge of TxC and the received data on RxD is latched on the negative edge of RxC. This assures high speed two-way operation between two MPCCs connected as shown in Figure 17.

For low speed operation between the MPCC and a modem or RS-232C Data Communications Equipment (DCE), an inverter can be used in the TxC output lines as shown in Figure 17. RS-232 and RS-423 (covering serial data interface up to 100K baud) require that data be centered ±25% about the negative-going edge of the RxC. This criteria is met for frequencies up to 1.25 MHz using the inverter. Use of the inverter also allows MPCC to MPCC operation up to 2.17 MHz.

SERIAL COMMUNICATION MODES AND PROTOCOLS

ASYNCHRONOUS AND ISOCHRONOUS MODES

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (LSB) first. The data line is normally held high (MARK) between frames, however, a BREAK (minimum of one frame length for which the line is held low) is used for control purposes. Figure 4 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (ASYNC) mode, data reception on RxD occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on RxC. When RCLKIN in the CCR is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchronization. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the RxFIFO and set appropriate status bits in the RSR when the character with an error reaches the last RxFIFO register where it is ready to be transferred onto the data bus via the RDR.

Isochronous Receive

In the isochronous (ISOC) mode, a times 1 clock on RxC is required with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data transmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character. Each frame is terminated with 1, 1½ or 2 stop bits as selected by PSR2 bits 5 and 6.

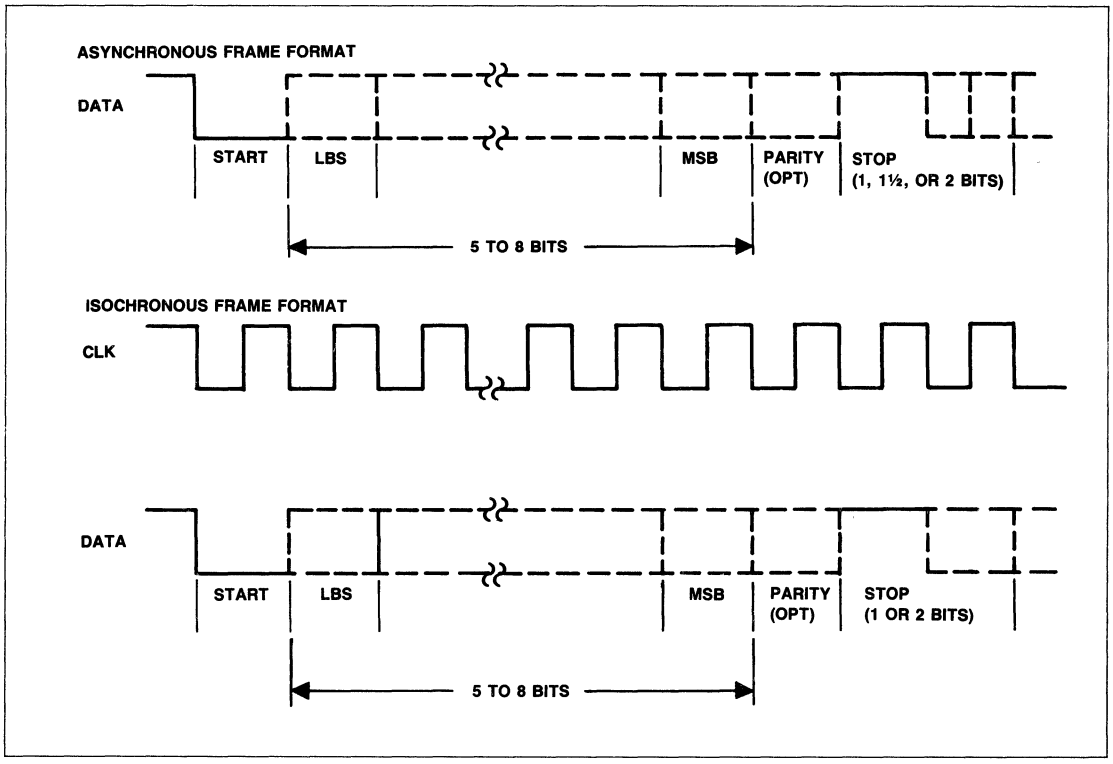


Figure 4. Asynchronous and Isochronous Frame Format

SYNCHRONOUS MODES

In synchronous modes, a times one clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 5).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. The first byte of the address field is automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made. The control field of one or two bytes is transparent to the MPCC and sent directly to the host without interpretation.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1s, and the 1s complement of the resulting remainder is transmitted. (See X.25 Recommendation.)

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110

Figure 5. Bit Oriented Protocol (BOP) Frame Format

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

The end of the frame is determined by the detection of the closing Flag special character which is the same is the opening Flag.

With the control options offered by the MPCC, commonly used bit oriented protocols such as SDLC, HDLC and X.25 standards can be supported. Figure 6 compares the requirements of these options.

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a Flag. The receiver also continues to search for additional Flag, or Abort, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the Flag detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "011111101111110."

Character assembly and CRC accumulation are stopped when a closing Flag or Abort is detected. The CRC accumulation includes all the characters between the opening Flag and the closing Flag. The contents of the CRC register are checked at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the Flag are not passed on to the RxFIFO.

If the Flag is a closing flag, checks for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an Abort (seven 1s) is detected, the remaining frame is discarded and the RA/B bit is set in the RSR. When a link idle (15 or more consecutive 1s) is detected, the RIDLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of the first byte. If there is no address match, or if null address is received, the receiver ignores the remainder of the frame by searching for the Flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

For the control field, one or two bytes are assembled and passed on to the RxFIFO depending on the state of the extended control field bit.

If the CFCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the TxFIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading Flag is automatically sent prior to transmitting data from the TxFIFO. The TDRA bit is set to 1 in the TSR as long as TxFIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an Abort (11111111) is transmitted followed by continuous Flags or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the $\overline{\text{DONE}}$ signal from the DMAC.

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an Abort character followed by the remainder of the current frame data in the TxFIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1s, and a 0 is inserted in the data stream each time this condition occurs (excluding Flag and Abort characters).

CRC accumulation begins with the first non-Flag character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTLCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control field. The final Frame Check Sequence is calculated over the balance of the frame.

IBM SDLC FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

Figure 6. Bit Oriented Protocols

LEADING PAD 1 BYTE (AR1)	SYN 1 BYTE (AR2)	SYN 1 BYTE (AR2)	BODY	BCC	TRAILING PAD 11111111

Figure 7. BSC Block Format

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 7. The MPCC can process both transparent and nontransparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 4.

Table 4. BSC Control Sequences—Inclusion in CRC Accumulation

ASCII			EBCDIC		
Command	Byte 1	Byte 2	Command	Byte 1	Byte 2
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

Note: *Programmable

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 5 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 8 shows various formats for Control/Response Blocks and Heading and Text Blocks.

Table 5. Transparent Mode BSC Control Sequences — Inclusion in CRC Accumulation

Character of Sequence	Included in CRC Accumulation	
	Yes	No
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

*If not preceded within the same block by transparent heading information.

6

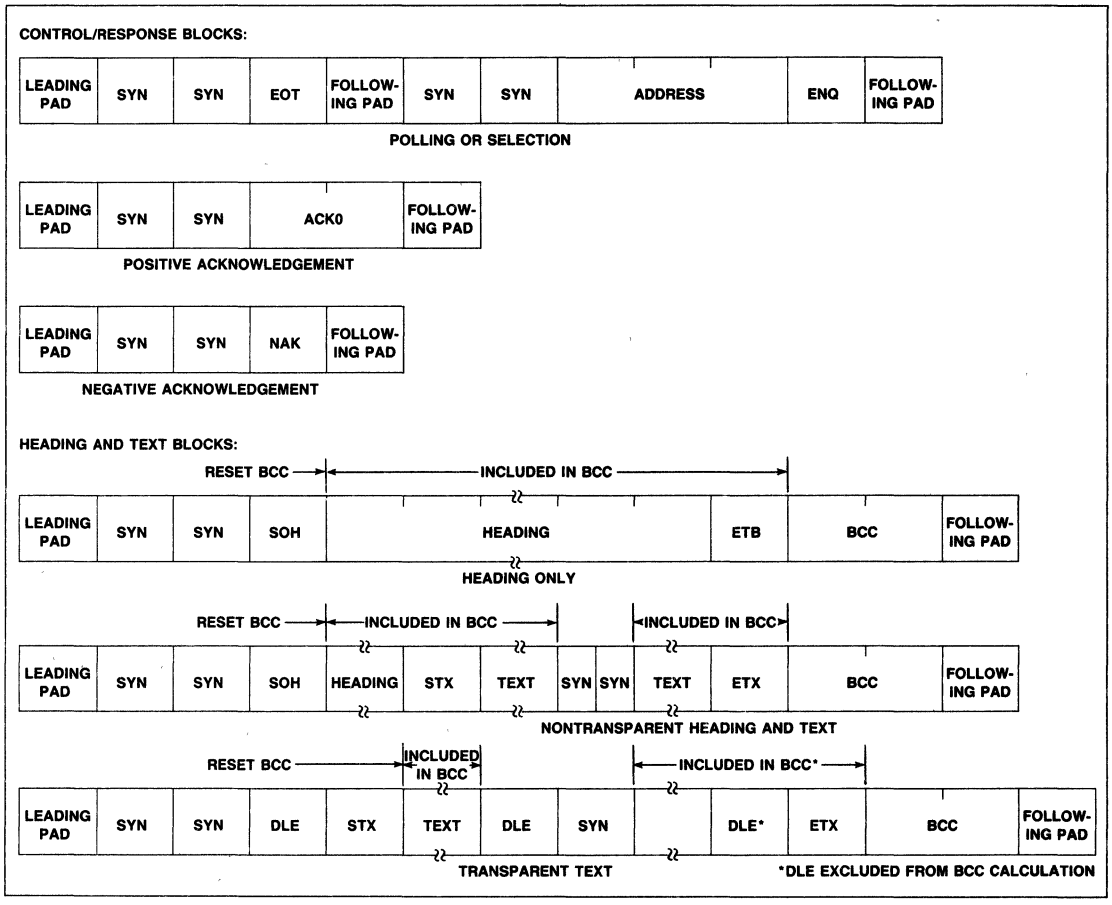


Figure 8. BSC Message Format Examples

BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided that VRC/LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the RxFIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the RxFIFO. The SYN character pairs in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation and is discarded. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). The first SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available. The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the TxFIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 5 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the TxFIFO. ETB, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters. DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the TxFIFO.

CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 9. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the RxFIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.

DMA CONSIDERATIONS

When the R68561, in the word mode, is used with a DMAC, high throughput of bit-oriented protocols is achieved. However, problems can arise when trying to DMA byte-oriented data in the word mode.

BOP and BSC have well-defined message boundaries and the MPCC can detect the end of message, determine if there is an odd (single) byte at the end of a message, and so inform the host MPU by setting the Received Half Word (RHW) bit in the Frame Status byte.

In byte-oriented protocols (such as ASYNC and COP) there is no defined message length. In the word mode, received bytes are grouped in pairs. In the byte mode, each byte is available through the RxFIFO as it is received. Thus, the MPCC in the word mode has no way of knowing when an odd (single) byte has been received at an end of a transmission to be passed onto the host MPU. In the word mode received bytes are grouped in pairs. In the byte mode each byte is available through the FIFO as it is received.

For transmission of data by the MPCC in the word mode, the MPCC provides a Transmit Half Word (THW) bit in the Transmit Control Register. When set, this bit informs the MPCC that the last word in the TxFIFO (marked by setting the TLAST bit with $\overline{\text{DONE}}$) contains only the upper byte as valid data. However, the currently available DMACs have no method to inform the MPCC that the last word of the message contains a single byte and MPU intervention is necessary.

To handle byte-oriented protocols with DMAC, an R68561 in the byte mode or the R68560 (byte mode only) should be used.

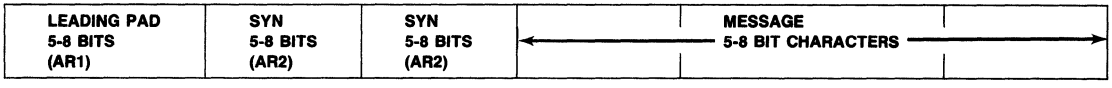


Figure 9. Character Oriented Protocol Format

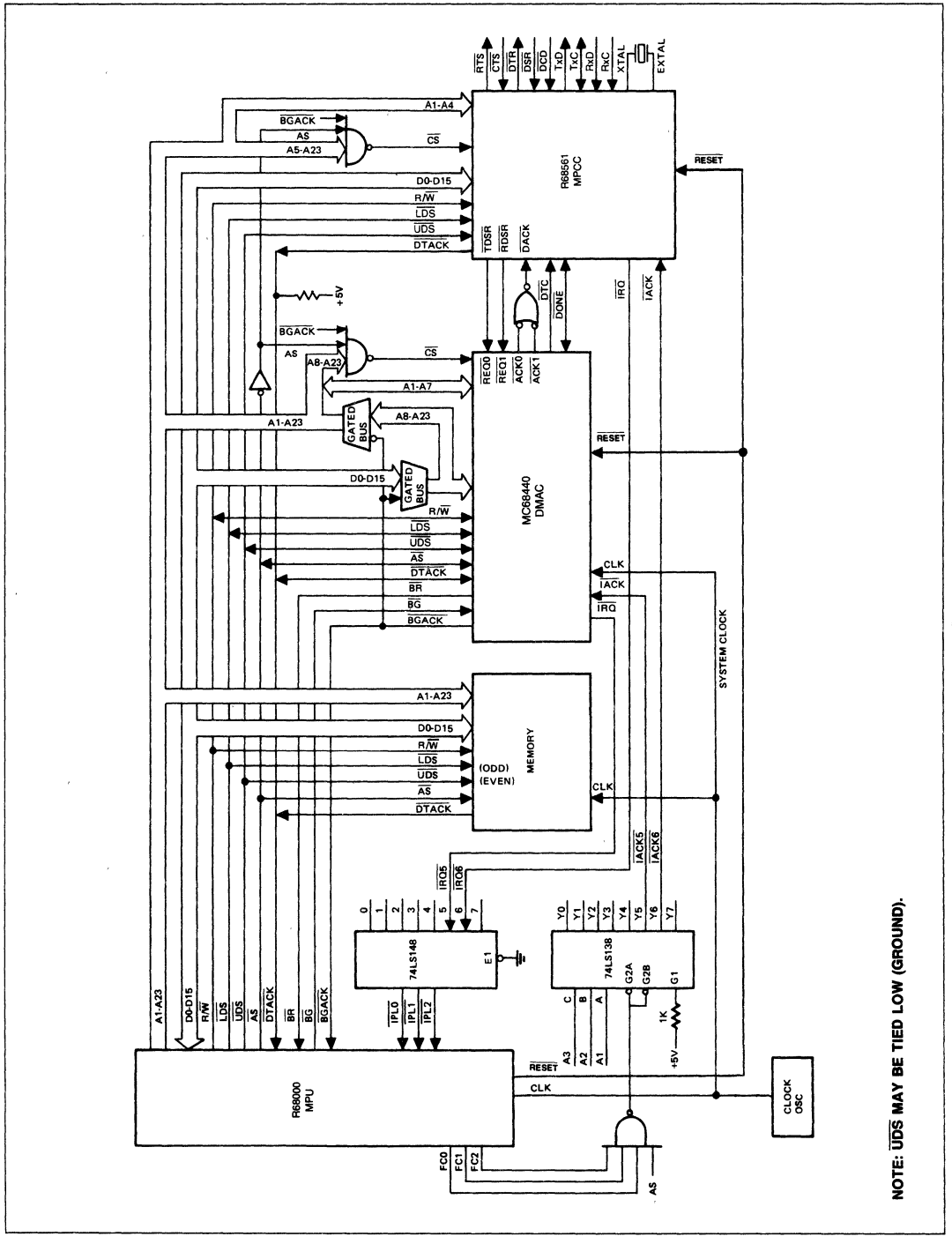


Figure 10. Typical Interface to 68000-Based System

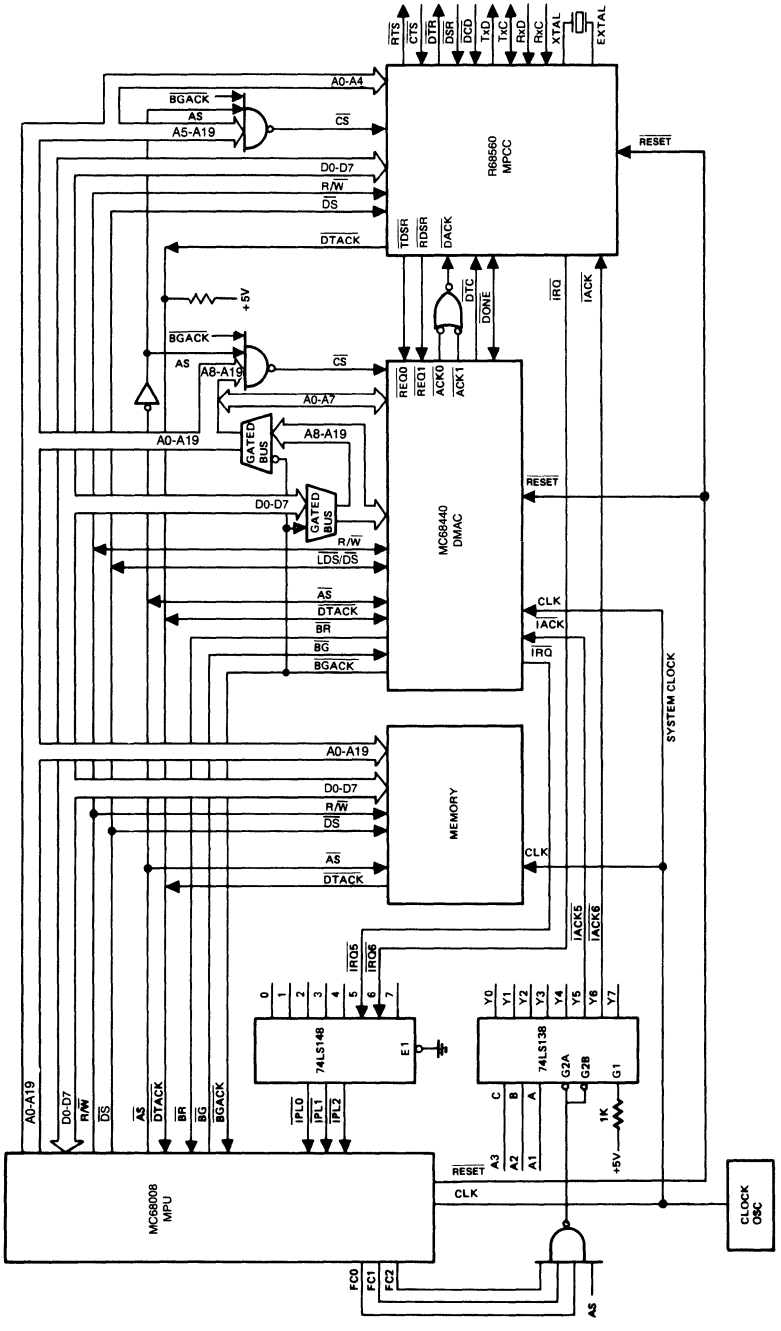


Figure 11. Typical Interface to 68008-Based System

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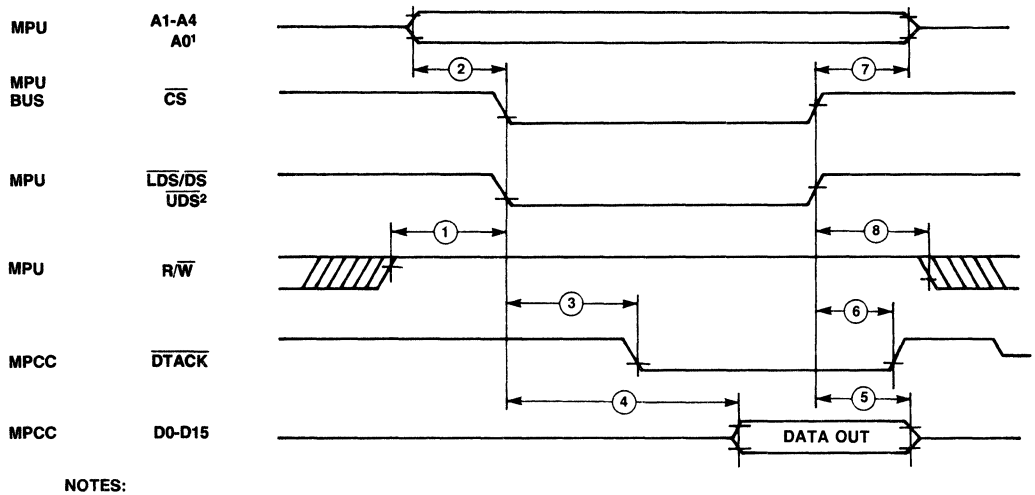
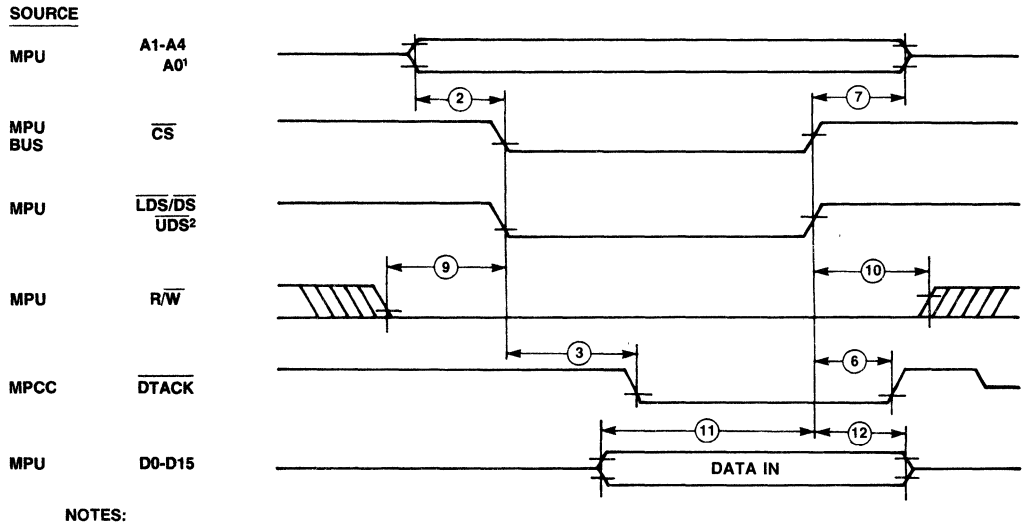


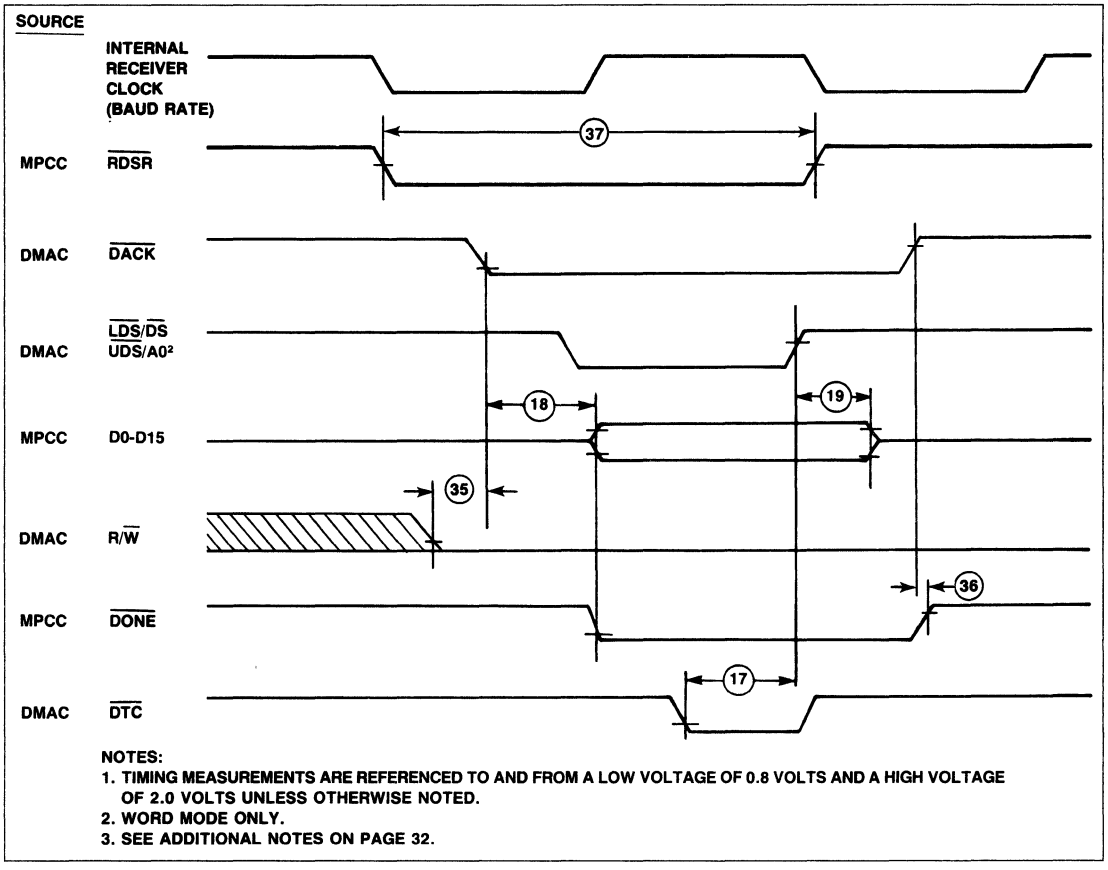
NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO $\overline{UDS}$ ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
4. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 12. MPCC Read Cycle Timing



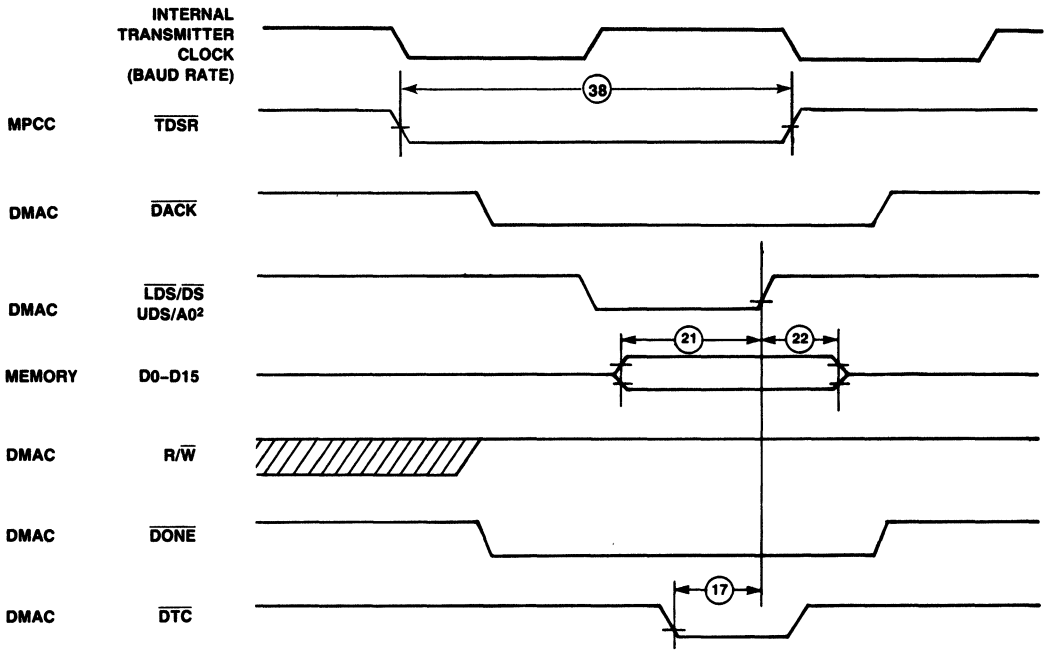
NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO $\overline{UDS}$ ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
4. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 13. MPCC Write Cycle Timing



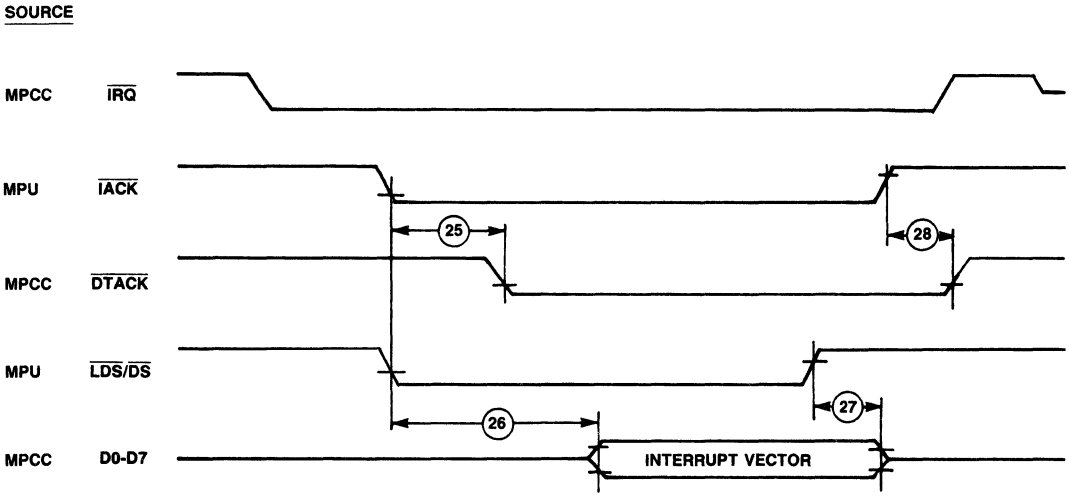
NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.
3. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 14. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.
3. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 15. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. IRQ IS NEGATED WHEN ALL BITS IN STATUS REGISTERS THAT COULD HAVE CAUSED THE INTERRUPT ARE CLEARED.
3. SEE ADDITIONIONAL NOTES ON PAGE 32.

Figure 16. Interrupt Request Cycle Timing

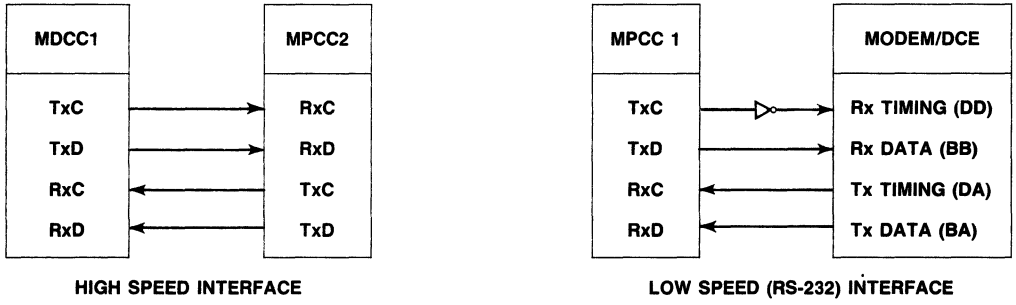


Figure 17. Serial Interface

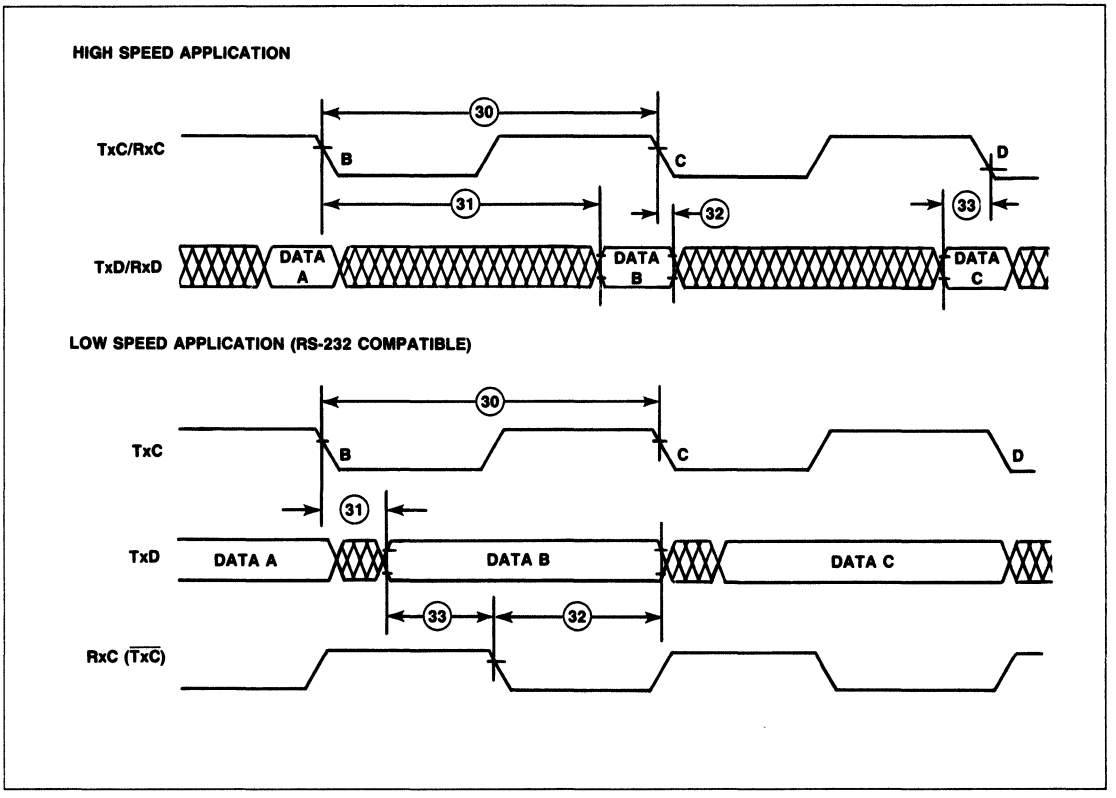


Figure 18. Serial Interface Timing

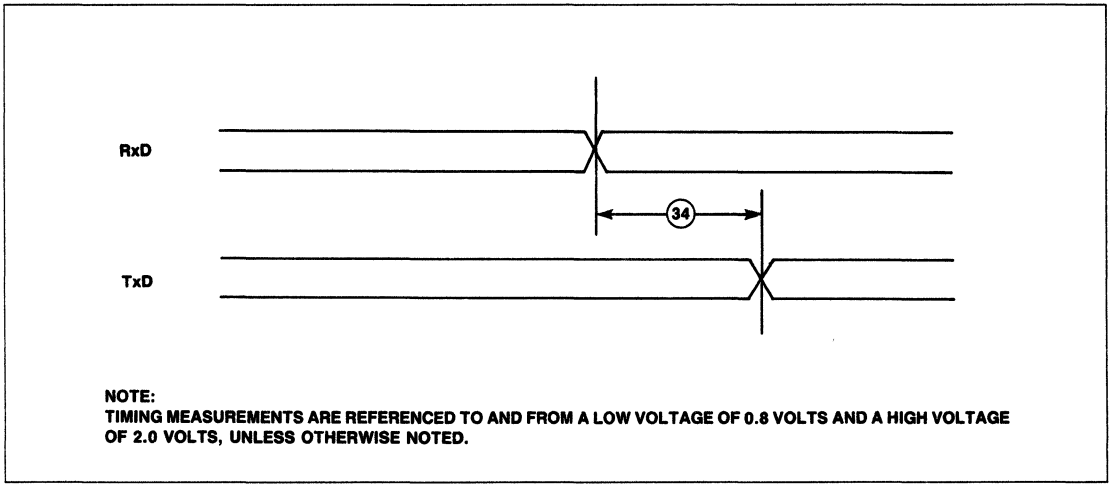


Figure 19. Serial Interface Echo Mode Timing

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Number	Parameter	Symbol	Min	Max	Unit
1	R/$\overline{W}$ High to $\overline{CS}$, $\overline{DS}$ Low	t_{RHSL}	0	—	ns
2	Address Valid to CS, $\overline{DS}$ Low	t_{AVSL}	30	—	ns
3[1]	$\overline{CS}$ Low to $\overline{DTACK}$ Low	t_{CLDAL}	0	60	ns
4[1]	$\overline{CS}$, $\overline{DS}$ Low to Data Valid	t_{SLDV}	0	140	ns
5	$\overline{DS}$ High to Data Invalid	t_{SHDXR}	10	150	ns
6	$\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAT}	0	40	ns
7	$\overline{DS}$ High to Address Invalid	t_{SHAI}	20	—	ns
8	$\overline{CS}$, $\overline{DS}$ High to R/$\overline{W}$ Low	t_{SHRL}	20	—	ns
9	R/$\overline{W}$ Low to $\overline{CS}$, $\overline{DS}$ Low	t_{RLSL}	0	—	ns
10	$\overline{CS}$ High, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	20	—	ns
11	Data Valid to $\overline{CS}$, $\overline{DS}$ High	t_{DVSH}	60	—	ns
12	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDXW}	0	—	ns
17	$\overline{DTC}$ Low to $\overline{DS}$ High	t_{CLSH}	60	—	ns
18	$\overline{DACK}$ Low to Data Valid, $\overline{DONE}$ Low	t_{ALDV}	0	140	ns
19	$\overline{DS}$ High to Data Invalid	t_{SHDXDR}	10	150	ns
21	Data Valid to $\overline{DS}$ High	t_{DVSH}	60	—	ns
22	$\overline{DS}$ High to Data Invalid	t_{SHDXDW}	0	—	ns
25	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{IALAL}	0	40	ns
26	$\overline{IACK}$, $\overline{DS}$ Low to Data Valid	t_{IALDV}	0	140	ns
27	$\overline{DS}$ High to Data Invalid	t_{ISHDI}	10	150	ns
28	$\overline{IACK}$ High to $\overline{DTACK}$ High	t_{IAHDAT}	0	40	ns
30	RxC and TxC Period	t_{CP}	248	—	ns
31	TxC Low to TxD Delay	t_{TCLTD}	0	200	ns
32	RxC Low to RxD Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to RxC Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to TxD Delay (Echo Mode)	t_{RDTD}	—	200	ns
35	R/$\overline{W}$ Low to $\overline{DACK}$ Low (Setup)	t_{RLAL}	0	—	ns
36	$\overline{DACK}$ High to $\overline{DONE}$ High	t_{AHDH}	0	—	ns
37[2, 3]	$\overline{RDSR}$ Pulse Width	t_{RPW}	1	—	clock period
38[2, 4]	$\overline{TDSR}$ Pulse Width	t_{TPW}	1	—	clock period

Notes:
1. For read cycle timing, the MPCC asserts $\overline{DTACK}$ within the MPU S4 clock low setup time requirement and establishes valid data (Data In) within the MPU S6 clock low setup time requirement.
2. For synchronous protocols, this is one full serial clock period of RxC for $\overline{RDSR}$ and TxC for $\overline{TDSR}$.
3. For asynchronous protocols, $\overline{RDSR}$ is asserted for two system clock periods for a prescale factor of 2 and for three system clock periods for a prescale factor of 3.
4. For asynchronous protocols, $\overline{TDSR}$ is asserted for a period of one-half the baud rate.

*NOTES TO FIGURES 12–16.

Address, $\overline{LDS}$, $\overline{UDS}$ and R/$\overline{W}$ are signals generated by the 68000 MPU and its bus timing prevails. $\overline{CS}$ is derived with external logic from the address bus and generally an Address Strobe ($\overline{AS}$) signal from the MPU. It will naturally be delayed somewhat from the $\overline{AS}$ signal. The active read or write cycle timing in the MPCC is during the summation of the active signal time, i.e., the last active signal starts the timing sequence. For an MPCC read cycle, for example, the data out parameter (t_{SLDV}, item 4) will be available 0 to 140 ns from the falling edge of $\overline{CS}$ or $\overline{LDS}$ whichever is active last. The data out parameter (t_{SHDXR}, item 5) will remain valid for 0–150 ns after the negation of $\overline{CS}$ or $\overline{LDS}$, whichever is negated first.

The minimum pulse widths for $\overline{CS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{DACK}$, $\overline{IACK}$ and $\overline{DTC}$ are not specified since they are system dependent and relate to system clock timing. For example, it is apparent that the minimum active time for "AND" condition of $\overline{CS}$ and $\overline{LDS}$ is 140 ns (t_{SLDV}, item 4) plus the setup time of the Data In to the receiving device if $\overline{LDS}$ high is used to strobe the data in. These same factors hold true for $\overline{UDS}$, $\overline{DACK}$ and $\overline{IACK}$. If $\overline{DTC}$ is used it must be true a minimum of 60 ns before the rising edge of $\overline{LDS}$ and thus this is the minimum pulse width. It may be connected to ground.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		68	

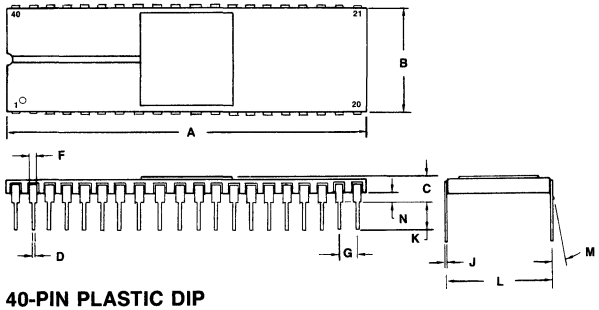
DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage All Inputs	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage All Inputs	V_{IL}	−0.3	+0.8	V	
Input Leakage Current R/$\overline{W}$, $\overline{RESET}$, $\overline{CS}$, A1-A4	I_{IN}	—	10.0	μA	V_{IN} = 0 to 5.25V V_{CC} = 5.25V
Three-State (Off State) Input Current $\overline{IRQ}$, $\overline{DTACK}$, D0-D15	T_{TSI}	—	10.0	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.25V
Output High Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$, D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = −400 μA C_{LOAD} = 130 pF
BCLK	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = 0 C_{LOAD} = 30 pF
Output Low Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$ D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC, BCLK,	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA
$\overline{DONE}$	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 8.8 mA
Internal Power Dissipation	P_{INT}	—	1	W	T_A = 25°C
Input Capacitance	C_{IN}	—	13	pF	V_{IN} = 0V T_A = 25°C f = 1 MHz

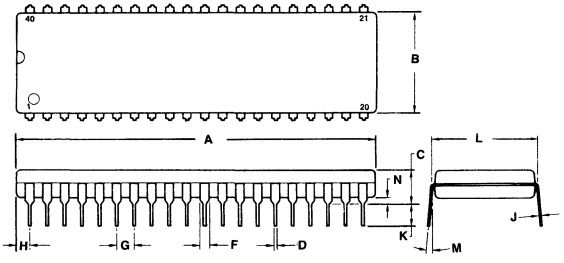
PACKAGE DIMENSIONS — 40-PIN DIP

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50 29	51 31	1 980	2 020
B	14 73	15 24	0 580	0 600
C	3 30	4 32	0 130	0 170
D	0 38	0 53	0 015	0 021
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
J	0 20	0 30	0 008	0 012
K	2 54	4 06	0 100	0 160
L	14 99	15 49	0 590	0 610
M	0°	10°	0°	10°
N	1 02	1 52	0 040	0 060

40-PIN PLASTIC DIP

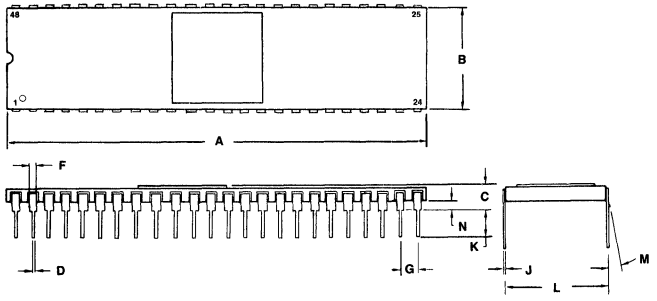


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 82	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	4 06	5 08	0 160	0 200
D	0 38	0 53	0 015	0 021
F	1 14	1 40	0 045	0 055
G	2 54 BSC		0 100 BSC	
H	1 40	1 91	0 055	0 075
J	0 20	0 30	0 008	0 012
K	3 30	4 32	0 130	0 170
L	14 48	16 00	0 570	0 630
M	0°	10°	0°	10°
N	0 51	1 02	0 020	0 040

6

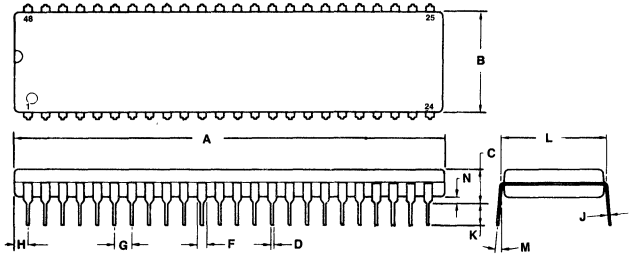
PACKAGE DIMENSIONS — 48-PIN DIP

48-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	60 35	61 57	2.376	2 424
B	14 73	15 24	0 580	0 600
C	3 30	4 32	0 130	0 170
D	0 38	0 53	0 015	0 021
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
J	0 20	0 30	0 008	0 012
K	2 54	4 06	0 100	0 160
L	14 99	15 49	0 590	0 610
M	0°	10°	0°	10°
N	1 02	1 52	0 040	0 060

48-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	60 83	61 85	2 395	2 435
B	13 72	14 22	0 540	0 560
C	4 06	5 08	0 160	0 200
D	0 38	0 53	0 015	0 021
F	1 14	1 40	0 045	0 055
G	2 54 BSC		0 100 BSC	
H	1 40	1 91	0 055	0 075
J	0 20	0 30	0 008	0 012
K	3 30	4 32	0 130	0 170
L	14 48	16 00	0 570	0 630
M	0°	10°	0°	10°
N	0 51	1 02	0 020	0 040

R68802
LOCAL NETWORK CONTROLLER (LNET)

DESCRIPTION

The R68802 Local Network Controller (LNET) implements the IEEE 802.3 CSMA/CD Access Method local network standard. This device supports Ethernet* (10BASE5), Cheapernet (10BASE2) and StarLAN (1BASE5) implementations of this standard.

The basic function of the LNET is to execute the CSMA/CD algorithm, perform parallel-to-serial and serial-to-parallel conversions for data streams up to 10 Mbps, and assemble and disassemble the packet format. In addition, the LNET provides an 8-bit or 16-bit processor interface, the required DMA interfaces, and the proper interface to the Manchester Code Converter (MCC) used to connect the LNET to an IEEE 802.3 defined Media Attachment Unit (MAU).

The controller can interface data terminal equipment to local networks with differing performance requirements. At the high end, the R68802 meets the IEEE 802.3 10 Mbps specification and supports the implementation of ISO reference model layers one and two. For low cost networks, the controller can be run at greatly reduced data rates and inexpensive system components (drivers, cables, etc.) may be selected (e.g., Cheapernet and StarLAN).

The LNET controller implements a protocol known as Carrier Sense Multiple Access with Collision Detection (CSMA/CD), which allows multiple Data Terminal Equipment to share the same communication medium without the need for a central arbiter of medium utilization.

IEEE 802.3 nodes needing to transmit wait a specific multiple of transmit clock periods before transmitting data to provide recovery time for other controllers and the cable itself. If a collision with another station is detected, the transmission is aborted and a jam signal transmitted to alert other nodes. Following a jam, the station waits a random amount of time based on a Binary Exponential Back-off algorithm before retransmitting. Repeated collisions result in repeated retries and an increase in the randomly selected time interval to improve trafficking

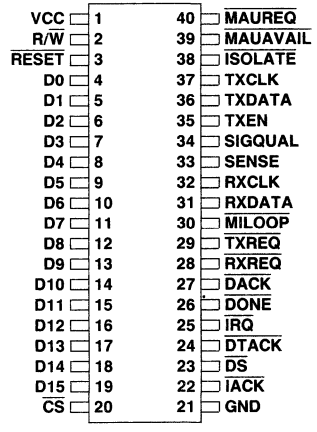
ORDERING INFORMATION

Part Number
R68802 —
— Package
C = Ceramic
P = Plastic

FEATURES

- Meets the IEEE 802.3 specifications for local networks (e.g., Ethernet*, Cheapernet and StarLAN)
- Serial data rates as high as 10 Mbps
- Compatible with a variety of 8- or 16-bit processors and DMA controllers
- Interfaces to a variety of manchester code converters
- Programmable interframe wait times for smaller topologies and lower data rates
- CSMA/CD algorithm:
  —Wait before transmit
  —Jam on collision
  —Binary exponential backoff
- Programmable 2- or 6-byte address recognition
- Supports loopback self-test
- Extensive network management capabilities
- Programmable disable on reception
- Programmable collision handling minimizes CPU intervention
- 32-bit CRC generation and reception
- Broadband applications
- 32-byte FIFO on both transmitter and receiver
- TTL compatible I/O
- 40-pin DIP
- Single 5V power supply

Ethernet is a trademark of the Xerox Corporation



R68802 Pin Assignments

6

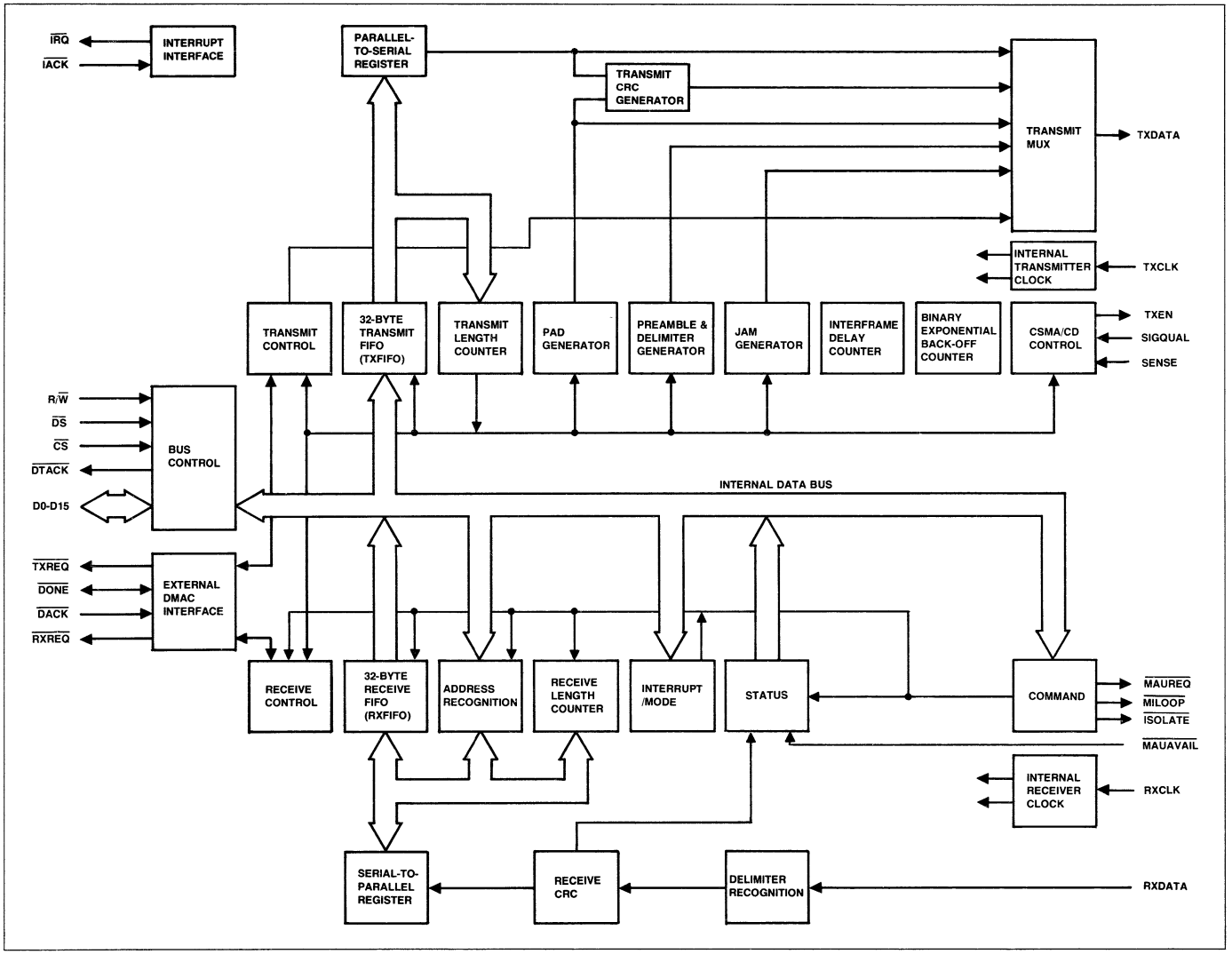


Figure 1. LNET Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar, R/$\overline{W}$ indicates a write is active low and a read active high.

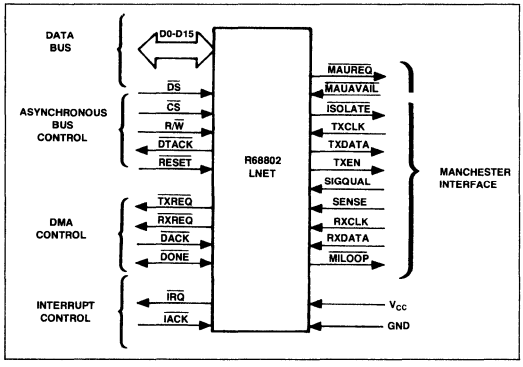


Figure 2. LNET Input and Output Signals

D0–D15—Data Lines. The bidirectional data lines transfer data between the LNET and the MPU, memory or other peripheral device. D0–D15 are used when connected to a 16-bit bus and operating in the word mode. D0–D7 are used when operating in the byte mode. The data bus is tri-stated when $\overline{CS}$ is inactive. (See exceptions in DMA mode.)

$\overline{CS}$—Chip Select. $\overline{CS}$ low input selects the LNET for programmed transfers with the host. The LNET is deselected when the $\overline{CS}$ input is inactive in non-DMA mode. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

R/$\overline{W}$—Read/Write. R/$\overline{W}$ input controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

$\overline{DTACK}$—Data Transfer Acknowledge. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the LNET after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. A pull up resistor is required to maintain $\overline{DTACK}$ high between bus cycles. This line is an open drain output.

$\overline{DS}$—Data Strobe. During a write (R/$\overline{W}$ low), the $\overline{DS}$ input positive transition latches data from the external data bus lines into the LNET. During a read (R/$\overline{W}$ high), $\overline{DS}$ low enables data from the LNET onto data bus lines.

$\overline{IRQ}$—Interrupt Request. The active low $\overline{IRQ}$ output requests interrupt service by the MPU. This line is open drain and should be tied high with a pull-up resistor.

$\overline{IACK}$—Interrupt Acknowledge. The active low $\overline{IACK}$ input indicates that the current bus cycle is an interrupt acknowledge cycle. When $\overline{IACK}$ is asserted the LNET places an interrupt vector on the lower byte (D0–D7) of the data bus.

$\overline{DACK}$—DMA Acknowledge. The $\overline{DACK}$ low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

$\overline{DONE}$—Done. $\overline{DONE}$ is a bidirectional active low signal. The $\overline{DONE}$ signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or is asserted by the LNET when either the last byte of receive data is transferred or a collision is detected during a transmission or reception. This line is open drain and should be tied high with a pull-up resistor.

$\overline{RESET}$—Reset. The active low, high impedance $\overline{RESET}$ input initializes all LNET functions. $\overline{RESET}$ must be asserted for at least 10 TXCLKs to initialize the LNET.

$\overline{RXREQ}$—Receive DMA Request. When receive data becomes available in the RXFIFO, $\overline{RXREQ}$ output is asserted and held low for 8 or 16 (single address burst mode) DMAC cycles (8 or 16 sequential $\overline{DACK}$ pulses) or until the end of the receive block. When the last data byte of the receive block is transferred, $\overline{DONE}$ is asserted by the LNET with the last $\overline{DACK}$ strobe and the negation of $\overline{RXREQ}$.

$\overline{TXREQ}$—Transmit DMA Request. When the Transmitter Enable bit is set in the Command Register, $\overline{TXREQ}$ output is asserted and held low for 8 or 16 (single address burst mode) DMAC cycles (8 or 16 sequential $\overline{DACK}$ pulses) or until the end of the transmit data block as signaled by the DMAC's assertion of $\overline{DONE}$.

$\overline{MILOOP}$—MI Loopback. With an active $\overline{MILOOP}$ output, the MCC shunts its LNET data-in path to its LNET data-out path, effectively routing the LNET TXDATA output into the LNET RXDATA input.

RXDATA—Receive Data. The LNET receives serial data via the RXDATA input. The RXDATA input is shifted into the receiver on the positive going edge of RXCLK.

RXCLK—Receive Clock. The free-running Receive Clock input provides the LNET with receive data timing information.

SENSE—Carrier Sense. The active high SENSE input indicates the presence of data on the RXDATA serial input line.

SIGQUAL—Signal Quality. The assertion of the active high SIGQUAL input by the MCC indicates an error condition on the medium. During the transmission mode the LNET interprets this as a collision.

TXEN—Transmit Enable. The active high TXEN output indicates to the MCC that data is present on the TXDATA output.

TXDATA—Transmit Data. The LNET transmits serial data on the TXDATA line. The TXDATA output changes on the negative going edge of TXCLK.

TXCLK—Transmit Clock. The Transmit Clock input is a free-running clock supplied by the MCC that provides both a system clock and a means of shifting out serial data bit on the TXDATA output line.

$\overline{\text{ISOLATE}}$—Isolate MAU. The active low $\overline{\text{ISOLATE}}$ output is asserted when the Isolate bit in the Command Register is set to 1. This pin can be used to isolate the MAU from the media. As long as $\overline{\text{ISOLATE}}$ is low, the MAU is unable to transmit or receive on the medium.

$\overline{\text{MAUAVAIL}}$—MAU Available. When the active low $\overline{\text{MAUAVAIL}}$ input is asserted, the transmission algorithm can proceed.

$\overline{\text{MAUREQ}}$—MAU Request. The active low $\overline{\text{MAUREQ}}$ output is asserted prior to transmission if $\overline{\text{MAUAVAIL}}$ is not asserted.

V_{CC}—Power. 5V ±5%.

GND—Ground. Ground.

LNET REGISTERS

The LNET contains three groups of registers accessible from the MPU bus which initialize the LNET, control and monitor LNET operation, and transfer data between the LNET and the MPU bus. These register groups, specific registers within each group, and the size, access and mode of each register are listed in Table 1.

All registers, except the Mode Register, may be accessed either in the word or byte mode, depending on the MPU data bus length (8-bit or 16-bit) and the Word/Byte mode selected in bit 4 of the Mode Register during initialization.

INITIALIZATION REGISTERS

The initialization registers contain command information to configure the LNET for normal operation. The registers are the one-byte Mode Register (MR), the one-byte Interrupt Vector Number Register (IVNR) and the two- or six-byte Station Address Register (SAR). These registers must be loaded upon RESET (either caused by power up or initiated during normal operation) or upon setting of the RESET bit in the Command Register. Any of these conditions reset the LNET by clearing the Mode Register, Station Address Register, Command Registers and Status Registers.

All initialization registers must be written to by the MPU instruction sequence immediately after a reset in the manner described below even if no data is changed in a register. The number of bytes written depends upon the number of bytes in the Station Address as selected in bit 4 of the Mode Register.

After the proper number of write cycles have been completed, the LNET is initialized and further MPU writes to the LNET will address only the Command Register. All MPU reads of the LNET after initialization is complete will access only Status Register 1 or 2.

Initialization Procedure for 16-Bit MPU Bus

Write cycle 1—write the Mode byte on the lower byte of the data bus D0–D7. The upper byte is not used and can contain any data.

Write cycle 2—write the Interrupt Vector Number on the lower byte of the data bus D0–D7. The upper byte is not used and can contain any data.

Write cycle 3 or write cycles 3 through 5—write the one- or three-word Station Address (depending on the Station Address Size loaded into the Mode Register) on the data bus (D0–D15). The first word of the Station Address Register will be compared to the first word in the destination address field of an incoming packet.

Table 1. LNET MPU Bus Accessible Registers

Register Group	Register Name	Size (No. Bytes)	Access	Mode
Initialization Registers	Mode Register (MR)	1	$\overline{DS}$ = L, $\overline{CS}$ = L, R/$\overline{W}$ = L (write one byte[1])	MPU Write
	Interrupt Vector Number Register (IVNR)	1	$\overline{DS}$ = L, $\overline{CS}$ = L, R/$\overline{W}$ = L (write one byte[1])	
	Station Address Register (SAR)	2 or 6	$\overline{DS}$ = L, $\overline{CS}$ = L, R/$\overline{W}$ = L (write 1 or 3 sequential words or 2 or 6 sequential bytes)	
Operating Registers	Command Register (CR)	1	$\overline{DS}$ = L, $\overline{CS}$ = L, R/$\overline{W}$ = L	MPU Write
	Status Register 1 (SR1) Status Register 2 (SR2)	1 1	$\overline{DS}$ = L, $\overline{CS}$ = L, R/$\overline{W}$ = H	MPU Read
Data Buffers	Transmit FIFO Register File (TXFIFO)	32	$\overline{TXREQ}$ = L, $\overline{DS}$ = L, $\overline{DACK}$ = L	DMA Write
	Receive FIFO Register File (RXFIFO)	32	$\overline{RXREQ}$ = L, $\overline{DS}$ = L, $\overline{DACK}$ = L	DMA Read

Note:
1. Upper byte in word mode ignored.

Initialization Procedure for 8-Bit MPU Bus

Write cycle 1—write the Mode byte on the data bus (D0–D7).

Write cycle 2—write the Interrupt Vector Number of the data bus (D0–D7).

Write cycles 3 through 4 or 3 through 8—write the two- or six-byte Station Address (depending on the Station Address Size loaded into the Mode Register). The first byte of the Station Address Register will be compared to the first byte in the destination field of an incoming packet.

Mode Register (MR)

7	6	5	4	3	2	1	0
IFWT			BYTE	INTCOL	DISRX	NOLC	SAS

The Mode Register sets conditions during initialization for use during normal operations. It must be the first byte written during initialization. All mode bits are active high, i.e., = 1.

MR 7-5 IFWT —Interframe Wait Time

No. of TXCLKs (Wait Time)
000 16
001 32
010 48
011 64
100 80
101 96
110 112
111 128

MR 4 BYTE —Data Bus Byte Mode

0 Select word mode (for use with 16-bit MPU bus).
1 Select byte mode (for use with 8-bit MPU bus).

MR 3 INTCOL—Interrupt on Collision

0 Assert only $\overline{\text{DONE}}$ on collision.
1 Assert $\overline{\text{IRQ}}$ on collision.

MR 2 DISRX —Disable Receiver

0 Enable receiver after each packet reception.
1 Disable receiver after each addressed packet reception if CR-6 is not set.

Note: See Table 2.

MR 1 NOLC —No Length Count

0 Use length count in packet format.
1 Do not use length count in packet format.

MR 0 SAS —Station Address Size

0 6-byte station address.
1 2-byte station address.

Interrupt Vector Number Register (IVNR)

7	6	5	4	3	2	1	0
Interrupt Vector Number (IVN)							

If an interrupt condition occurs (as reported by bits in Status Register 1 and Status Register 2), $\overline{\text{IRQ}}$ is asserted to request MPU interrupt service. Upon $\overline{\text{IACK}}$ input assertion, the Interrupt Vector Number (IVN) from the Interrupt Vector Number Register (IVNR) is placed on the data bus (D0–D7). The IVN must be the second byte initialized during LNET initialization.

Station Address Register (SAR)

7	6	5	4	3	2	1	0
Station Address							

The Station Address Register holds the Station Address for the Receiver Address Recognition circuitry. The Station Address bytes must be written to the LNET following the Interrupt Vector Number during the initialization sequence. Either two or six bytes must be written, least significant bytes first, depending on the Station Address Size loaded into the Mode Register.

OPERATING REGISTERS

The command or status registers are addressed during an MPU write or read, respectively, after initialization is complete. In word mode, the Command Register is written during one write cycle. The Command Register receives the lower byte of the word. Likewise, while reading the status registers in word mode, Status Register 1 occupies the lower byte of the word.

COMMAND REGISTER

Command Register (CR)

The Command Register controls the operation of the LNET. All command bits are active high (i.e., = 1).

7	6	5	4	3	2	1	0
RESET	RXEN	RXALL	NOISOL	MILOOP	—	ODDNO	TXCMD

CR 7 RESET —Reset

0 Enable LNET operation.
1 Reset LNET.

Note: The RESET bit is automatically cleared to 0 upon the completion of the reset sequence. This bit is unaffected by the $\overline{\text{RESET}}$ pin level.

CR
6 RXEN —Receiver Enable
0 Disable receiver.
1 Enable receiver. This bit must be set after each packet is received to enable reception of the next packet only if bit 2 in the Mode Register is set at initialization. Reception of the packet clears this bit if CR-5 is not set.

Note: This bit is not used if bit MR2 is not set at initialization. See Table 2.

CR
5 RXALL —Receive All Packets
0 Receive only addressed packets. The address must correspond to the Station Address loaded into the Station Address Register upon initialization.
1 Receive all packets (regardless of address), only if bit 2 in the mode Register is not set at initialization.

Note: See Table 2.

CR
4 NOISOL—No Isolate
0 Assert $\overline{\text{ISOLATE}}$ to request that the MAU isolate itself from the medium.
1 Negate $\overline{\text{ISOLATE}}$ to request that the MAU connect itself to the medium.

CR
3 MILOOP—Manchester Interface Loopback Test
0 Negate $\overline{\text{MILOOP}}$ to command MI normal operation.
1 Assert $\overline{\text{MILOOP}}$ to command MI loopback operation.

CR
2 Reserved
Bit must be set to zero.

CR
1 ODDNO—Odd Number of Bytes
0 Transmit even number of bytes in a block.
1 Transmit odd number of bytes on block.

CR
0 TXCMD —Transmit Command
0 Disable transmission.
1 Start transmission. Asserts $\overline{\text{TXREQ}}$ and $\overline{\text{MAUREQ}}$. Clears automatically after packet transmission.

Table 2. Receive Operation

Bit			
MR2	CR-5	CR-6	Operation
0	0	X	Receive addressed packets continuously
0	1	X	Receive all packets (regardless of address) continuously
1	0	0	Disable receiver
1	0	1	Receive only one addressed packet
1	1	0	Disable receiver
1	1	1	Receive addressed packets continuously

STATUS REGISTERS

The two interrupt driven status registers report the status of the LNET receiver and transmitter operations. Status registers can be read upon interrupt service by the MPU. Status is reported in either discrete or encoded bits. All discrete (or non-encoded) status bits are active high (i.e. = 1).

A change in any of these status bits causes IRQ to be asserted (except as noted). In the byte mode, both status registers must be read in consecutive read cycles.

Status Register 1 (SR1)

7	6 5 4	3	2 1 0
—	TXSTAT	ODD	RXSTAT

SR1
7 Not Used

SR1
6-4 TXSTAT—Transmitter Status
000 Transmitter idle.
001 Transmit successful.
010 Collision (Assertion of SIGQUAL within the first 512 bit times causes $\overline{\text{DONE}}$, or $\overline{\text{DONE}}$ and $\overline{\text{IRQ}}$, to be asserted depending on the state of MR bit 3).
011 Signal Quality error (SIGQUAL asserted after the first 512 bit times).
100 Transmit retry count exceeded.
101 Transmit buffer underflow during transmission (indicates the TXFIFO emptied between the 16th data byte delivered for transmission and the assertion of $\overline{\text{DONE}}$).
110 Transmit in progress (indicates the real time activity of TXDATA pin. This state does not set the $\overline{\text{IRQ}}$ bit in SR2 nor cause $\overline{\text{IRQ}}$ to be asserted. This bit pattern is not reset to the transmitter idle pattern upon reading SR1.
111 $\overline{\text{MAUAVAIL}}$ changed state during transmission.

SR1
3 ODD —Odd Number of Receive Bytes
0 Even number of bytes in the receive packet.
1 Odd number of bytes in the receive packet.

SR1
2-0 RXSTAT—Receiver Status
000 Reserved.
001 Receive successful.
010 Minimum packet size error.
011 Receive buffer overflow.
100 Frame terminated on a non-byte boundary error.
101 Frame Check Sequence (FCS) error.
110 Reserved.
111 Reserved.

Status Register 2 (SR2)

7	6	5	4	3	2	1	0
IRQ	—	—	MAUAVAIL	COLCNT			

SR2
7 **IRQ —Interrupt Request**
0 An interrupt condition has not occurred and $\overline{IRQ}$ has not been asserted.
1 An interrupt condition has occurred and $\overline{IRQ}$ has been asserted.

Note: This bit is cleared when SR2 is read and there is no pending interrupt condition.

SR2
6 **—Not Used**

SR2
5 **—Not Used**

SR2
4 **MAUAVAIL—MAU Available**
0 MAU is not available.
1 MAU is available.

Note: This bit is not cleared when SR2 is read.

SR2
3-0 **COLCNT —Collision Count**
0000 Zero
. .
. .
. .
1111 Fifteen

Note: Reset to zero when the TXCMD bit (CR-0) is set. If Mode Register bit 3 is negated the changing count does not generate IRQ interrupts. $\overline{IRQ}$ is asserted when maximum collision count is reached.

TRANSMIT DATA BUFFER (TXFIFO)

The Transmit data buffer is a 32-byte FIFO register file (TXFIFO) which can be loaded only by DMA service. One half of the TXFIFO loads data for transmission via the DMAC; the other half holds data currently being transmitted out serially on TXDATA. When the transmitting half is empty it becomes the loading half and the current loading buffer becomes the transmitting half. If the transmitting buffer empties before the loading buffer is fully loaded, $\overline{IRQ}$ is asserted and the transmitter buffer underflow bit pattern (101) is set in Status Register 1.

The time required to load half the transmitter buffer under DMAC control must be less than the time it takes to serialize out the transmitting half on TXDATA. From the assertion of $\overline{TXREQ}$ to the end of the 16th DMAC bus cycle (byte mode) or the 8th DMAC bus cycle (word mode), no more than 128 TXCLKs can elapse.

RECEIVE DATA BUFFER (RXFIFO)

The Receive data buffer is a 32-byte FIFO register file (RXFIFO) which can be read only during DMA service. One half of the RXFIFO is a receiving buffer for the data from the Serial-to-Parallel Register; the other half is a reading buffer for the data ready to be transferred to the MPU bus. As soon as the receiving buffer is full, these two halves switch roles. If the receiving buffer is fully loaded before the reading buffer is empty, $\overline{IRQ}$ is asserted and the receive buffer overflow bit pattern (011) is set in Status Register 1.

The time it takes to unload the reading buffer under DMAC control must be less than the time it takes to load the receiving buffer from RXDATA. The loading time is 128 RXCLKs.

INPUT/OUTPUT FUNCTIONS

Typical LNET interface connections to a 16-bit data bus or an 8-bit data bus are shown in Figure 4 and Figure 5, respectively.

MPU INTERFACE

Transfer of data between the LNET and the system bus involves the following signals: Data Bus D0 through D15 and control signals consisting of R/$\overline{W}$, $\overline{DTACK}$, $\overline{CS}$, $\overline{IACK}$, and $\overline{DS}$.

16-Bit MPU Interface

Bit 4 in the Mode Register, left at its default value of 0 during initialization, selects the word mode. In the word mode, a read of both status registers performed with one word read cycle transfers Status Register 1 on D0–D7 and Status Register 2 on D8–D15. A write to the 8-bit Command Register is also accomplished in one cycle on D0–D7.

8-Bit MPU Interface

Bit 4 of the Mode Register, set to 1 during initialization, selects the byte mode. In the byte mode, reading of the status registers is performed with two consecutive byte read cycles to enable first Status Register 1 and then Status Register 2 onto D0–D7. Writing to the Command Register requires one cycle.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the LNET for access to the internal registers and other operations. When $\overline{CS}$ is asserted the data I/O buffer acts as an output driver during a read operation, and as an input buffer during a write operation.

If the LNET is selected ($\overline{CS}$ = low) for a read (R/$\overline{W}$ = high), data is placed on the data bus from the status register when $\overline{DS}$ is asserted. The LNET asserts Data Transfer Acknowledge ($\overline{DTACK}$) concurrent with the output data.

If the LNET is selected ($\overline{CS}$ = low) for a write (R/$\overline{W}$ = low), $\overline{DS}$ strobes data into the selected register and the LNET asserts $\overline{DTACK}$ immediately after $\overline{DS}$ is asserted.

DMA INTERFACE

During receiving or transmitting data from the MPU bus, the LNET asserts a receive or transmit request ($\overline{RXREQ}$ or $\overline{TXREQ}$) to the DMAC. A DMA acknowledge ($\overline{DACK}$) signal is asserted in response to $\overline{RXREQ}$ or $\overline{TXREQ}$ when the DMAC is ready to service the request. Both receive request and transmit request share the same $\overline{DACK}$ pin; therefore, in the case of DMAC devices with a $\overline{DACK}$ for each channel, they must be ORed together externally.

Transmit DMA Request

In servicing the $\overline{TXREQ}$, the DMAC writes to the TXFIFO a byte or a word at a time. The TXFIFO input pointer (TIP) is advanced and data latches on the rising edge of $\overline{DS}$.

Receive DMA Request

In servicing the $\overline{RXREQ}$, the DMAC reads from the RXFIFO a byte or word at a time. Data is enabled out on the falling edge of $\overline{DACK}$ and the RXFIFO output pointer (ROP) is advanced on the rising edge of $\overline{DACK}$. The data lines are tri-stated following the rising edge of $\overline{DACK}$.

$\overline{DONE}$

$\overline{DONE}$ is a bidirectional signal line to or from the DMAC and indicates one of three conditions:

1. As an input to the R68802, $\overline{DONE}$ tells the LNET that no more data bytes will be transmitted.
2. As an output from the R68802, $\overline{DONE}$ indicates the last byte of received data is being loaded onto the data bus.
3. As an output from the R68802, $\overline{DONE}$ also indicates premature end of transmission or reception resulting from a collision. Examine SR2-3 to SR2-0 (Collision Count) to determine valid or invalid data transfer.

INTERRUPTS

The $\overline{IRQ}$ output asserts when there is status information available after the completion of a transmit or receive transaction, or an error condition exists. The MPU grants the interrupt by asserting an interrupt acknowledge ($\overline{IACK}$) signal and reads the interrupt vector when the LNET asserts data transfer acknowledge ($\overline{DTACK}$). The subsequent negation of $\overline{IACK}$ and $\overline{IRQ}$ precede MPU interrupt processing.

MANCHESTER INTERFACE SIGNALS

The abbreviation MCC refers to the Manchester Code Converter necessary to interface the LNET to an IEEE 802.3 specified Media Access Unit (MAU).

SENSE (Sense Carrier) Input

The MCC asserts SENSE when it has detected a change in Carrier Sense from no carrier present to carrier present. SENSE stays active as long as carrier is present and is negated when the carrier disappears.

$\overline{ISOLATE}$ (Isolate Message Request) Output

The LNET asserts $\overline{ISOLATE}$ to direct the MCC to send an Isolate message to the MAU. When $\overline{ISOLATE}$ is negated, the MCC sends a Normal message to the MAU unless the LNET requires that the MAU request message be sent to permit data output.

$\overline{MAUREQ}$ (MAU Request) Output

The LNET asserts MAUREQ when CR bit 0 is active. $\overline{MAUREQ}$ stays active and a MAU request message is sent until the end of a packet transmission.

$\overline{MAUAVAIL}$ (MAU Available) Input

The MCC asserts $\overline{MAUAVAIL}$ when an MAU available message from the MAU is received. $\overline{MAUAVAIL}$ is negated when an MAU not available message is received from the MAU.

SIGQUAL (Signal Quality) Input

SIGQUAL is asserted by the MCC when a Signal Quality Error Message is received from the MAU.

TXEN (Transmission Enable) Output

The LNET starts a transmission by asserting TXEN and outputs serial data on TXDATA which is Manchester encoded by the MCC. TXEN is active until the end of the transmission.

RXCLK (Receive Clock) Input

RXCLK shifts receive data into the LNET and is free running at 10 MHz, or slower.

TXCLK (Transmitter Clock) Input

The TXCLK is a free running 10 MHz, or slower, clock used to clock data into the MCC and perform operations in the transmitter.

$\overline{MILOOP}$ (MI Loopback) Output

The $\overline{MILOOP}$ output signals the MCC that the current data is a test frame and it is to be "looped back" to the LNET instead of being sent to the MAU.

LNET FUNCTIONAL DESCRIPTION

The LNET transmits and receives serial data on an IEEE 802.3 CSMA/CD Access Method defined communications medium and transfers parallel data to and from a host system under program or DMA control according to the IEEE 802.3 data link specification.

Frame Format

Serial data transfers synchronously between the LNET and the MCC within the frame structure for data communications using local area network media access control (MAC) procedures. Each MAC frame, or packet, consists of eight fields: Preamble, Start Field Delimiter (SFD), Destination Address, Source Address, Length Count, Data, Pad and Frame Check Sequence (FSC). Figure 3 illustrates the frame format.

The Preamble consists of seven bytes of alternating 1's and 0's, i.e., 1010...1010.

The Start Field Delimiter (SFD) consists of one byte of bit pattern 10101011 immediately following the Preamble pattern which indicates the start of a valid frame.

The Destination and Source Addresses are either two or six bytes in length. Addresses may be any one of the following three types: Station Address, Logical Group, or Broadcast. Logical Group and Broadcast Addresses are identified by a 1 in the first bit position received. The first bit of a Station Address is 0.

The Length Count field is two bytes in length and specifies the Data field length (in an Ethernet application this field is the Type field and the Length Count field in the Mode Register must be initialized appropriately).

The Data field can have a variable number of bytes. If the Data field is less than 46 bytes (in a six-byte address mode), or less than 54 bytes (in a two-byte address mode), pad bytes are added to the frame on transmission to bring the overall packet size up to the minimum size of 72 bytes. The maximum Data field length must be programmed into the DMAC operating with the LNET.

The Frame Check Sequence (FCS) field is four bytes in length.

Frame Reception

The Receiver consists of the following sections: Delimiter Recognition, Receive CRC, Serial-to-Parallel Register, Receive Length Counter, Address Recognition, and a 32-byte FIFO register file (RXFIFO). These registers are all driven or loaded by RXCLK or a derivative.

In the absence of serial input data from the network bus, the SENSE input from the MCC is inactive. The Receive Clock (RXCLK) is free running and the Receiver front end is idling.

The assertion of SENSE defines the beginning of a frame. The rising edge of RXCLK enables SENSE and, concurrently, the first Preamble bit on RXDATA to the LNET. The falling edge of RXCLK shifts the first bit of the Preamble into the Delimiter Recognition logic and SENSE into the SENSE Detection logic. Delimiter Recognition is deferred for eight RXCLKS after the assertion of SENSE, to give the MCC unit time to synchronize on the Preamble.

If sequential zeros are detected during the time the LNET is searching for the double ones delimiter, the packet's reception is aborted.

The Preamble bits are shifted through the Delimiter Recognition logic without result. As the last bit of the Delimiter is shifted in, an internal signal is asserted.

The data is then routed to the Receive CRC and the Serial-to-Parallel Register. The Byte Alignment and Odd/Even byte monitor is initialized, and a Byte Counter is started.

At the appropriate byte count, the first byte of Destination Address is converted to parallel data, compared with the first byte of Station Address, and loaded into the RXFIFO.

The RXFIFO Input Pointer (RIP) is then advanced by one. The next byte(s) of destination and source addresses are loaded in the same manner. As the two length count bytes are sent to the RXFIFO they are also loaded into the Length Counter. If this field is non-zero it is decremented on each succeeding byte of the packet.

The remainder of the first 16 bytes of the packet are loaded into the RXFIFO (unless the Length Counter reaches its terminal count or the packet terminates).

With 16 bytes buffered, the RXFIFO is half full. $\overline{\text{RXREQ}}$ is now asserted. The receiving half of the buffer becomes the reading half, and the first 16 bytes of receive data are unloaded by advancing the RXFIFO Output Pointer (ROP) as a function of the DMAC's $\overline{\text{DACK}}$ and $\overline{\text{DS}}$ signals. The first and second bytes of the received packet are read out of the RXFIFO on D0–D7 and D8–D15, respectively, in word mode. The first byte out of the RXFIFO is the destination address. Meanwhile the empty, receiving half of the RXFIFO continues to fill.

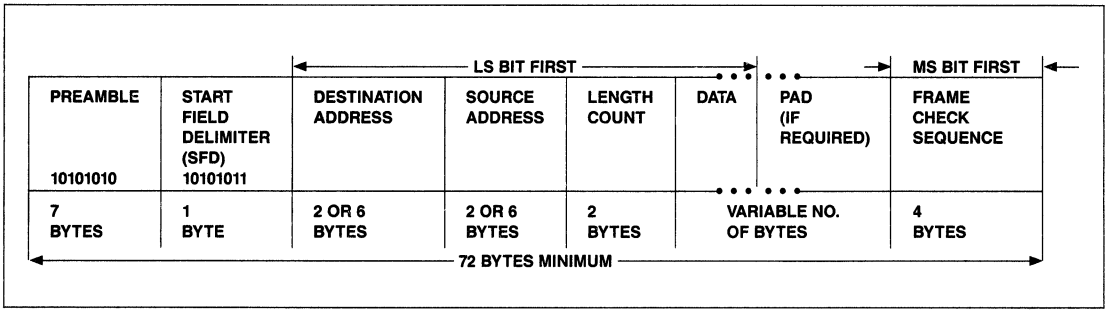


Figure 3. MAC Frame Format

As the 32nd byte of received data is loaded, $\overline{RXREQ}$ is asserted again and RIP proceeds to the just emptied reading buffer while DMA bus cycles unload the new reading buffer.

The RXFIFO continues to load and unload in this manner throughout the duration of the packet's Data field.

The position of RIP indicates when the load the Length Counter from the data stream, when to check for a valid address, and when to assert or negate $\overline{RXREQ}$ and to flag an overrun of the receive DMA service.

The two-byte Length Counter is located either four or twelve bytes (depending on the address mode) after Valid Delimiter. The Length Counter is decremented every eight RXCLKs. When the Length Counter equals zero, indicating the end of the Data field, RIP is disabled and $\overline{RXREQ}$ asserts long enough to unload the last bytes.

In the case of a normal termination of the packet, after the last bytes are unloaded, the LNET asserts $\overline{DONE}$ concurrently with the last $\overline{DACK}$ strobe and negates $\overline{RXREQ}$. The CRC Register continues to calculate over the Pad and Frame Check Sequence fields and the Byte Alignment Checker continues to run until packet end. The state of the Odd/Even byte checker is latched at the time of the Length Counter's terminal count.

The end of the packet is recognized as follows. The last FCS bit is latched into the LNET when RXCLK goes high in the normal manner. Two RXCLKs later the negated value of SENSE is detected. At the next rising edge of RXCLK, the CRC syndrome is compared and the result is posted to Status Register 1 and $\overline{IRQ}$ is asserted.

Frame Transmission

The Transmitter consists of the following: Parallel-to-Serial Register, Transmit Length Counter, 32-byte Transmitter FIFO register file (TXFIFO), Transmit CRC Generator, Preamble and Delimiter Generator, Jam Generator, Interframe Delay Counter, and the Binary Exponential Back-Off Counter. These sections are all driven by TXCLK or a derivation.

Frame transmission commences with a MPU write to Command Register 1 setting the Enable Transmission bit (CR–0). The LNET responds by asserting Transmit DMA Request ($\overline{TXREQ}$). Under DMA control, 16 bytes are loaded from the MPU bus into the TXFIFO by advancing the TXFIFO Input Pointer (TIP) as a function of $\overline{DACK}$ and $\overline{DS}$. The LNET then negates $\overline{TXREQ}$ until the first byte of this data has been serialized out. In word mode this corresponds to data loaded into the TXFIFO on data bus D0–D7.

While the first 16 bytes are being loaded into the TXFIFO, the LNET is monitoring the SENSE input. Upon SENSE negation, the Transmitter waits 96 TXCLKs (strict IEEE 802.3 or Ethernet application, otherwise the delay follows whatever is programmed into Mode Register bits 5–7) and then serializes out the first byte of data on TXDATA if the TXFIFO is half full (if it is not half full yet, the LNET returns to monitoring SENSE). If SENSE is active the LNET waits until it is negated and then starts the Interframe Delay Counter.

At the terminal count of the Interframe Delay Counter, the first preamble bits are shifted out under TXCLK control and the transmitter begins to monitor the SIGQUAL input. At the same time, $\overline{TXREQ}$ is asserted again and another 16-byte data burst is transferred into the empty half of the TXFIFO.

As the TXFIFO Output Pointer (TOP) advances to the first byte of the most recently filled half of the buffer, $\overline{TXREQ}$ is again asserted to reload the half just emptied.

Upon the assertion of the $\overline{DONE}$ input by the DMAC (at the time of the last byte or word transfer), the transmitter finishes serializing the last bytes out, zeros the TXFIFO Input Pointer (TIP) and serializes the contents of the CRC Register out on TXDATA.

If SIGQUAL is asserted by the MCC *during* the first 512 TXCLKs, the LNET assumes there has been a collision between its own transmission and that of another node in the network. The response of the LNET at its MCC interface is to abort the frame transmission after appending a Jam signal consisting of alternating zeros and ones to it. Internally the LNET enters the Binary Exponential Backoff Algorithm. The Jam signal is sent whenever the LNET has successfully contended for the medium and then has been interrupted in its transmission during the collision window.

DMA TRANSFER MODES

The response of the LNET at its MPU/DMAC interface to a collision is programmable to one of two modes in the Mode Register at initialization.

This allows for the LNET to be used with DMACs of differing capabilities. Specifically, some DMACs need to be reinitialized by the MPU if they are to restart a block transfer that has been aborted by a peripheral's assertion of a $\overline{DONE}$ and an $\overline{IRQ}$. Others are capable of automatically re-starting a block by themselves if a $\overline{DONE}$ is detected during a transfer.

Mode One: Assert $\overline{IRQ}$ On Collision.

Assertion of SIGQUAL *during* the first 512 TXCLKs after transmission begins sets the collison code (010) in the encoded Transmitter Status field in Status Register 1 and increments the Collision Count field in Status Register 2 by one. Next, $\overline{IRQ}$ is asserted, and the Interrupt Vector Number from the Interrupt Vector Number Register is output on the data bus when $\overline{IACK}$ is asserted.

The MPU processes the interrupt by reading the status registers to determine the cause of the interrupt and to clear the interrupt. The MPU then reinitializes the DMAC and gives the transmit command to the LNET to reload the first 16 bytes of the aborted data packet into the TXFIFO. Meanwhile the LNET is sending the Jam signal followed by a delay interval determined by the Binary Exponential Back-off Counter. At the end of this time interval the LNET begins to transmit the preamble and delimiter again if the TXFIFO has been reloaded with the first 16 bytes of the packet. If the TXFIFO has not been reloaded by the time the Jam signal and the back-off delay interval are over, the LNET will wait for data.

Mode Two: Assert $\overline{DONE}$ On Collision.

Upon the assertion of SIGQUAL *during* the first 512 TXCLKs, the LNET zeros the TXFIFO Input Pointer (TIP), asserts $\overline{DONE}$ to the DMAC concurrently with the next $\overline{DACK}$ signal, increments the retry count and remains in the transmit mode ($\overline{TXREQ}$ asserted, etc.), the JAM is sent, and the Back-off delay is observed. In the meantime, 16 bytes of data are loaded into the TXFIFO by the DMAC. The packet is then transmitted as before.

If the MCC asserts SIGQUAL *after* the first 512 TXCLKs, $\overline{IRQ}$ is asserted and the Transmitter Status field in Status Register 2 is set to 011

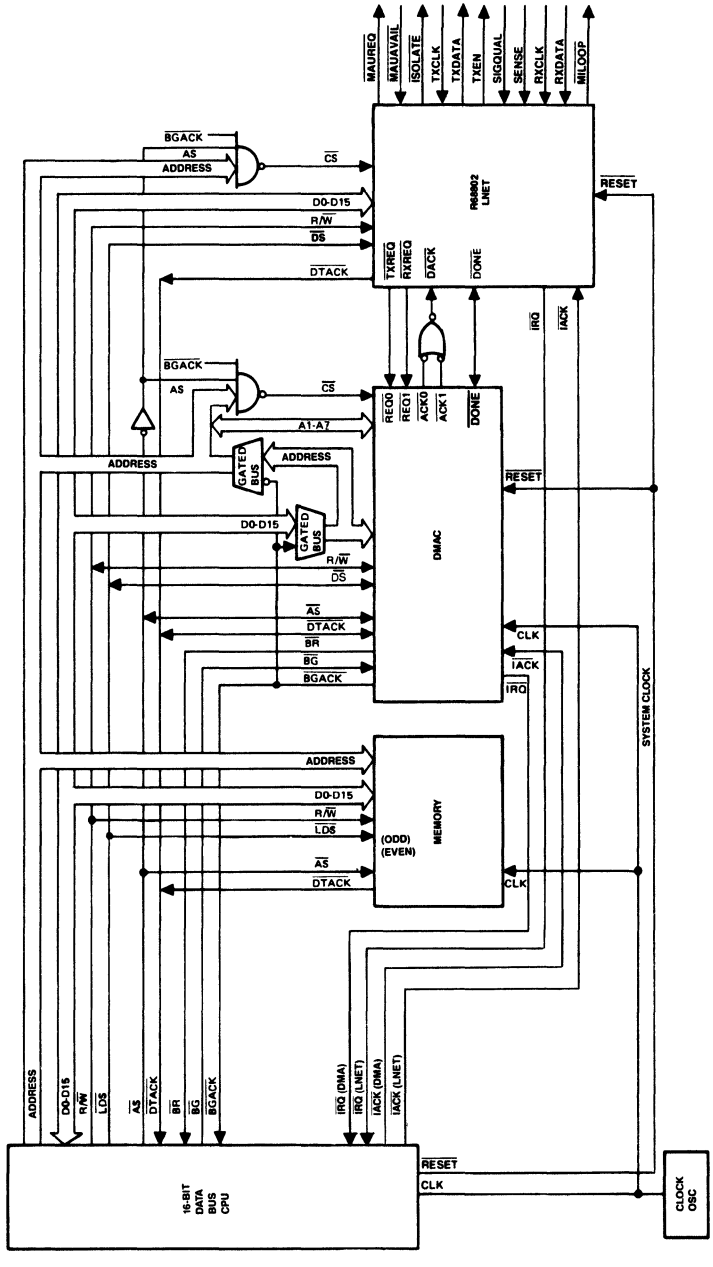


Figure 4. Typical Interface to a 16-Bit Data Bus CPU

6

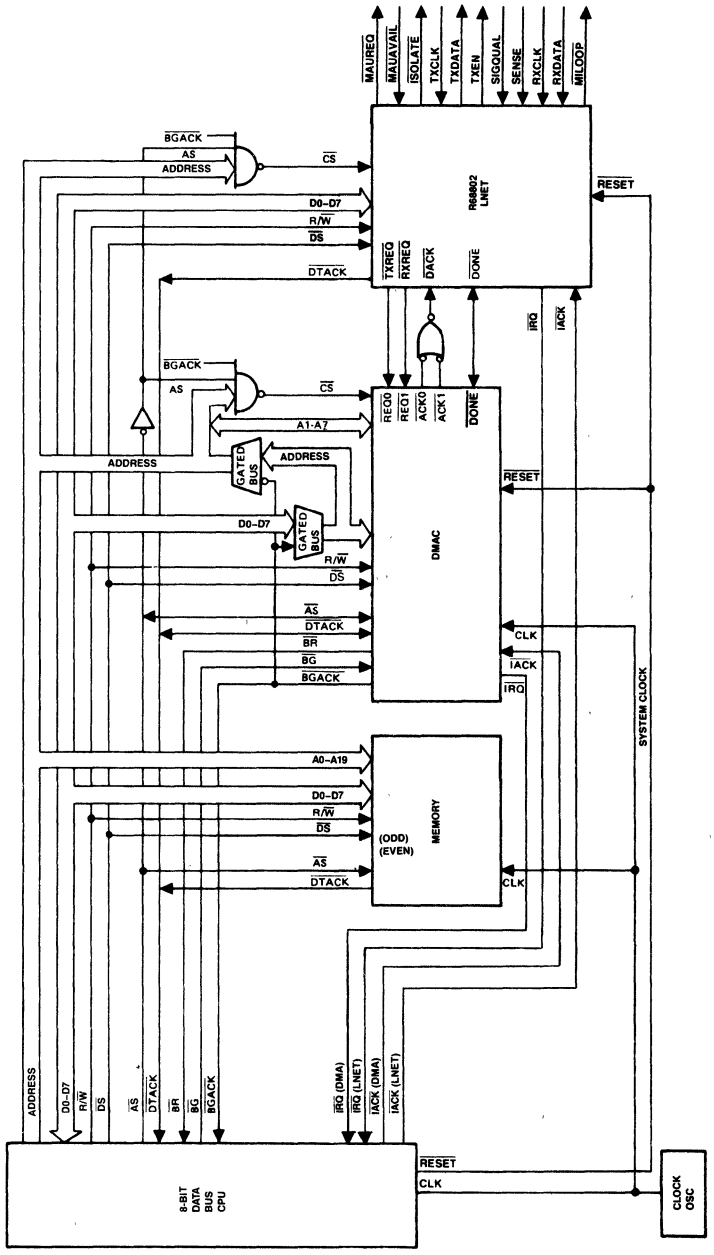
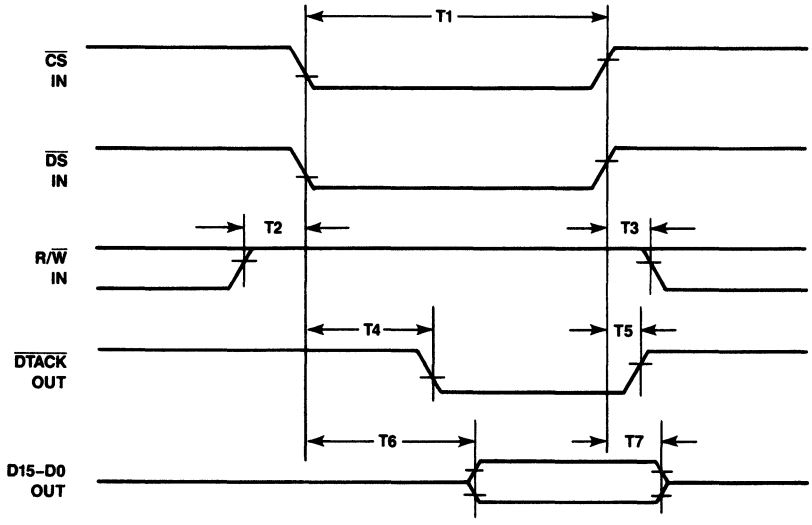


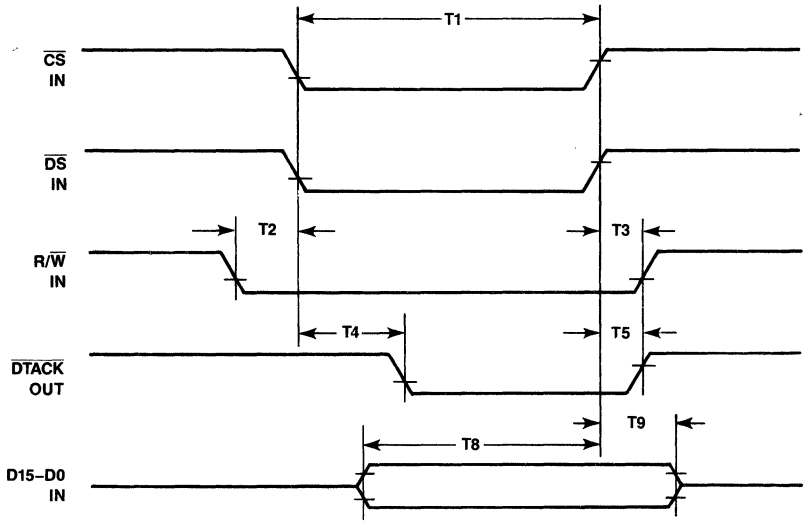
Figure 5. Typical Interface to an 8-Bit Data Bus CPU



NOTES: CS AND DS LOW STARTS THE TIMING FOR T2, T4 AND T6.
CS OR DS HIGH STARTS THE TIMING FOR T3, T5 AND T7.

TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

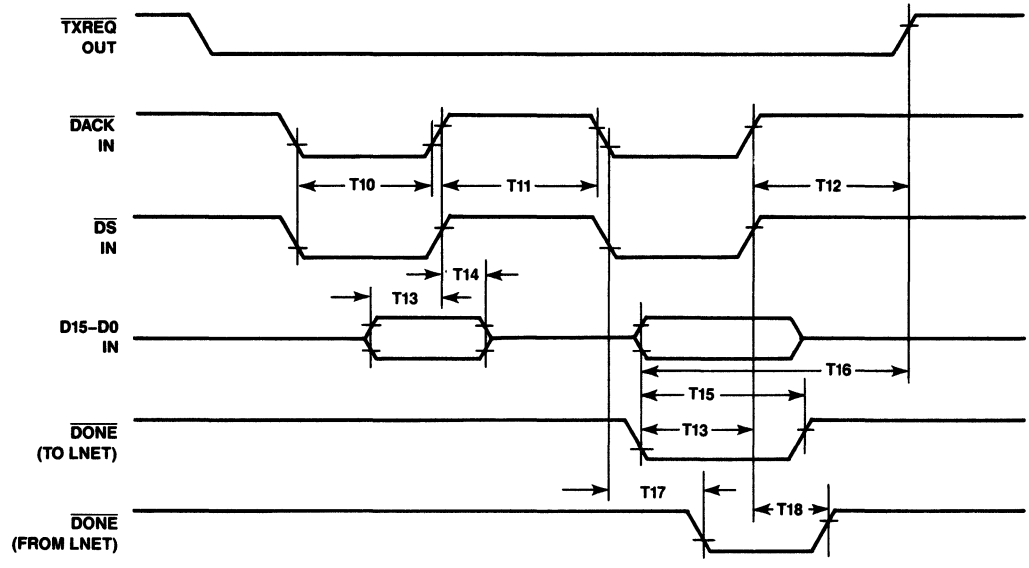
Figure 6. LNET Read Timing



NOTES: CS AND DS LOW STARTS THE TIMING FOR T2 AND T4.
CS OR DS HIGH STARTS THE TIMING FOR T3, T5, T8 AND T9.

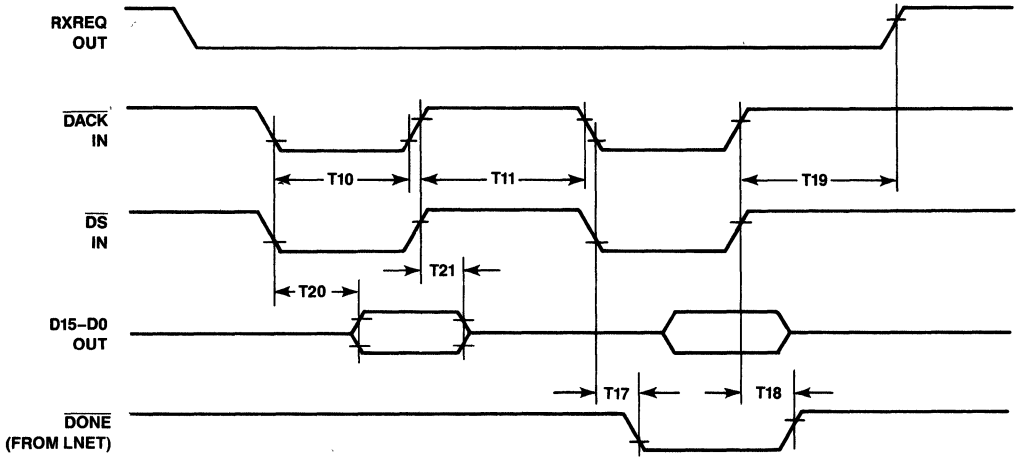
TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 7. LNET Write Timing



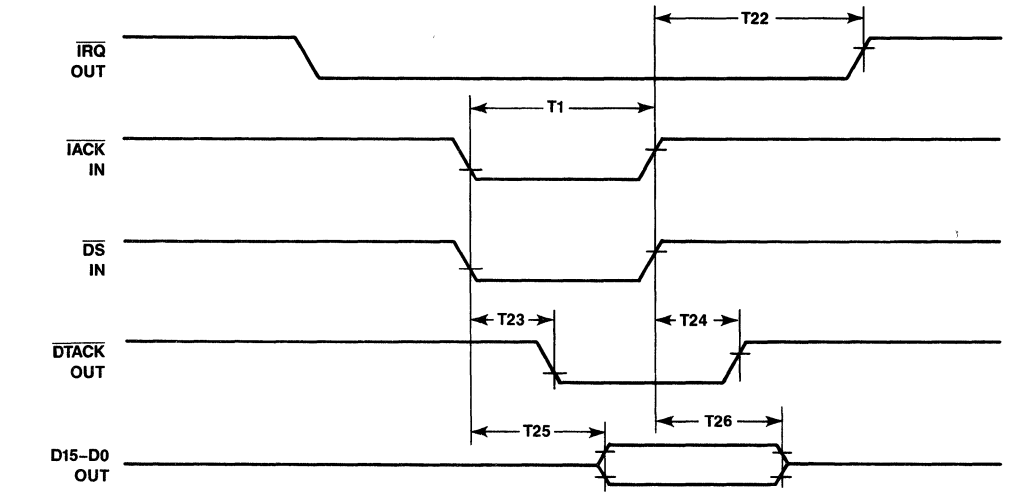
NOTES: 1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.

Figure 8. DMA Timing: Memory to LNET



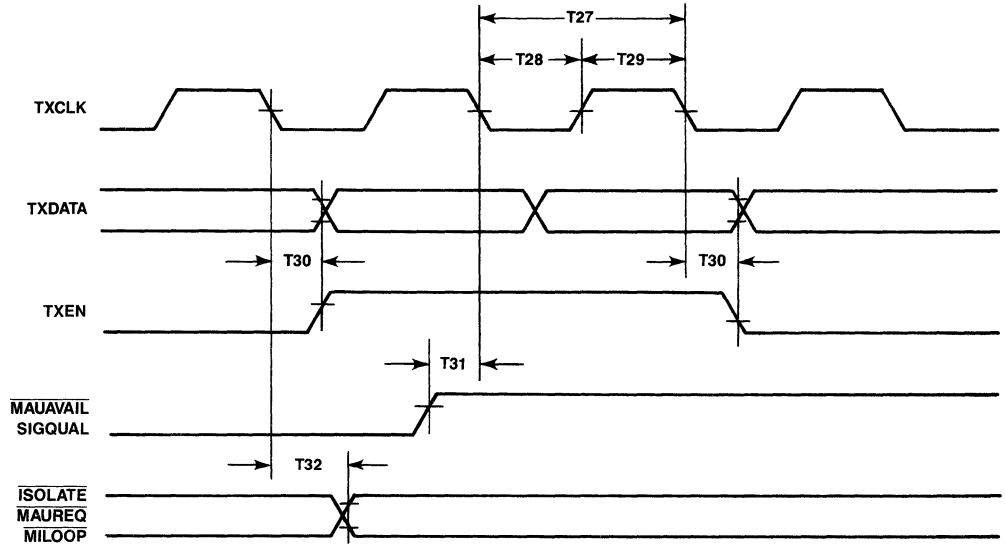
NOTES: 1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.

Figure 9. DMA Timing: LNET to Memory



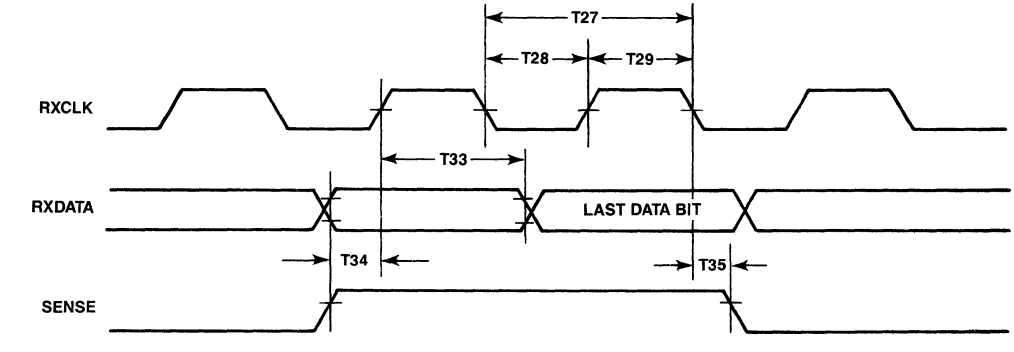
NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 10. Interrupt Timing



NOTES: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 11. Serial Interface Timing: Transmitter



NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 12. Serial Interface Timing: Receiver

SPECIFICATIONS

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T1	$\overline{CS}$ or $\overline{DS}$ Pulse Width	80	—	—	ns	1
T2	R/$\overline{W}$ Setup to $\overline{CS}$ or $\overline{DS}$ Low	25	—	—	ns	1
T3	R/$\overline{W}$ Hold After $\overline{CS}$ or $\overline{DS}$ High	20	—	—	ns	1
T4	$\overline{CS}$ or $\overline{DS}$ Low to DTACK Low	20	40	80	ns	1
T5	$\overline{CS}$ or $\overline{DS}$ High to DTACK High	20	40	100	ns	1
T6	$\overline{CS}$ or $\overline{DS}$ Low to DATA Valid	0	—	320	ns	1
T7	DATA Float After $\overline{CS}$ or $\overline{DS}$ High	0	—	40	ns	1
T8	DATA Setup to $\overline{CS}$ or $\overline{DS}$ High	240	—	—	ns	1
T9	DATA Hold to $\overline{CS}$ or $\overline{DS}$ High	30	—	—	ns	1
T10	$\overline{DS}$ or $\overline{DACK}$ Low Pulse Width	80	—	—	ns	1
T11	$\overline{DS}$ or $\overline{DACK}$ High Pulse Width	210	—	—	ns	1
T12	$\overline{DS}$ or $\overline{DACK}$ High to TXREQ High	—	—	230	ns	1
T13	DATA or $\overline{DONE}$ Setup to $\overline{DS}$ or $\overline{DACK}$ High	65	—	—	ns	1
T14	DATA Hold to $\overline{CS}$ or $\overline{DACK}$ High	35	—	—	ns	1
T15	$\overline{DONE}$ Low Pulse Width	70	—	—	ns	1
T16	$\overline{DONE}$ Low to $\overline{TXREQ}$ High	—	—	3(T27) + 300	ns	1
T17	$\overline{DACK}$ or $\overline{DS}$ Low to $\overline{DONE}$ Low	—	—	100	ns	1
T18	$\overline{DACK}$ or $\overline{DS}$ High to $\overline{DONE}$ High	—	—	80	ns	1
T19	$\overline{DS}$ or $\overline{DACK}$ High to $\overline{RXREQ}$ High	—	—	370	ns	1
T20	$\overline{DS}$ or $\overline{DACK}$ Low to DATA Valid	—	—	70	ns	1
T21	DATA Float After $\overline{DS}$ or $\overline{DACK}$ High	0	—	40	ns	1
T22	$\overline{IACK}$ or $\overline{DS}$ High to $\overline{IRQ}$ High	—	—	3(T27) + 380	ns	1
T23	$\overline{IACK}$ or $\overline{DS}$ Low to $\overline{DTACK}$ Low	20	40	80	ns	1
T24	$\overline{IACK}$ or $\overline{DS}$ High to $\overline{DTACK}$ High	20	40	100	ns	1
T25	$\overline{IACK}$ or $\overline{DS}$ Low to DATA Valid	0	—	320	ns	1
T26	DATA Float After $\overline{IACK}$ or $\overline{DS}$ High	—	—	50	ns	1
T27	TXCLK or RXCLK Period	100	—	2000	ns	2
T28	TXCLK or RXCLK Low Time	50	—	—	ns	2
T29	TXCLK or RXCLK High Time	50	—	—	ns	2
T30	TXCLK Low to TXDATA or TXEN Valid	—	—	70	ns	1
T31	$\overline{MAUAVAIL}$ or SIGQUAL Setup to TXCLK	100	—	—	ns	1
T32	TXCLK Low to $\overline{MAUREQ}$, $\overline{MILOOP}$, $\overline{ISOLATE}$ Active	—	—	90	ns	1
T33	RXDATA Hold to RXCLK High	20	—	—	ns	1
T34	RXDATA, SENSE, Setup to RXCLK High	30	—	—	ns	1
T35	SENSE Hold to RXCLK Low	30			ns	1

Notes:
1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted
2. Measured at 1.5V.

MAXIMUM RATINGS

Characteristics	Symbol	Value
Supply Voltage	V_{CC}	−0.3 to +7.0V
Input Voltage	V_{IN}	−0.3 to +7.0V
Operating Temperatures	T_A	0 to 70°C
Storage Temperature	T_{STG}	−55 to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, normal precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		
Ceramic		50	°C/W
Plastic		68	°C/W

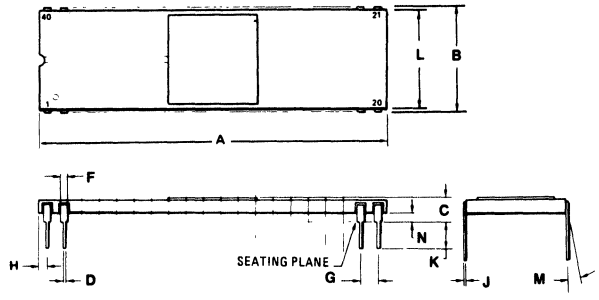
DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0 to 70°C unless otherwise noted)

Characteristics	Symbol	Min.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	+0.8	V	
Input Leakage Current SIGQUAL, TXCLK, MAUAVAIL, R/W, RESET, CS, IACK, DS, DACK, RXCLK, SENSE, RXDATA	I_{IN}	—	10	μA	V_{IN} = 0 to 5.25V
Input Leakage Current for Three State (Off) D0–D15	I_{TSI}	—	10	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 0V
Output High Voltage RXREQ, TXREQ, DTACK, D0–D15, MILOOP, MAUREQ, ISOLATE TXEN, TXDATA	V_{OH}	 +2.4 +2.4 +2.4	— — — —	 V V V	V_{CC} = 4.75 V I_{LOAD} = −400 μA, C_{LOAD} = 130 pF I_{LOAD} = −400 μA, C_{LOAD} = 32 pF I_{LOAD} = 0, C_{LOAD} = 30 pF
Output Low Voltage RXREQ, TXREQ, TXEN, TXDATA, DTACK, D0–D15 MILOOP, MAUREQ, ISOLATE IRQ, DONE	V_{OL}	 — —	 0.5 0.5	 V V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 8.8 mA
Power Dissipation	P_{INT}	—	1.0	W	T_A = 25°C
Input Capacitance	C_{IN}	—	13	pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C

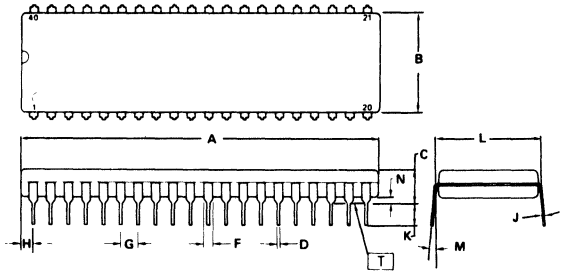
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50 29	51 31	1 980	2 020
B	15 11	15 88	0 595	0 625
C	2 54	4 19	0 100	0.165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0.605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1.52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0.008	0 012
K	3 30	4 32	0 130	0 170
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0.040

SECTION 7
Digital Network Products Evaluation Tools

R8069 Evaluation Board 7-3
R8070 Evaluation Board 7-4
R8071 Evaluation Board 7-5

R8069EB
R8069 Evaluation Board

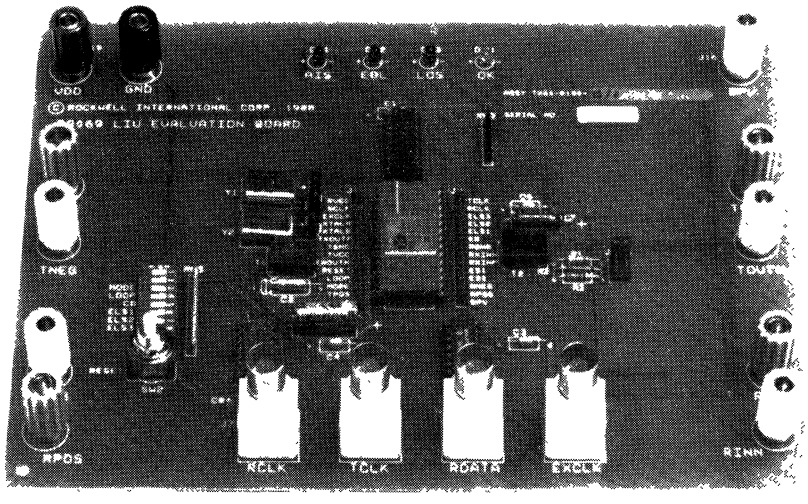
SUMMARY

To aid you in understanding how the R8069 Line Interface Unit (LIU) connects to the physical T-1/CEPT PCM 30 transmission medium, Rockwell offers the R8069 Evaluation Board (R8069EB). The R8069EB exercises all the modes of operation of the R8069. You can also interface the Rockwell R8070 T-1/PCM 30 transceiver to this board to perform various system tests.

The R8069EB comes complete with a kit containing one R8069 LIU, two crystals, two transformers, status LEDs, selection switches, peripherial logic, unipolar and bipolar input/output banana plugs, and a comprehensive, easy-to-follow user's manual.

FEATURES

- 6" x 8" card on stand-offs for easy access to all pins
- Requires only a single +5 Vdc power supply
- On-board receive/transmit transformer alows direct connection to T-1/PCM 30 lines
- Provides test access to R8069 device
- Four LED indicate error status



R8069EB Evaluation Board

R8070EB
R8070 Test/Evaluation Board

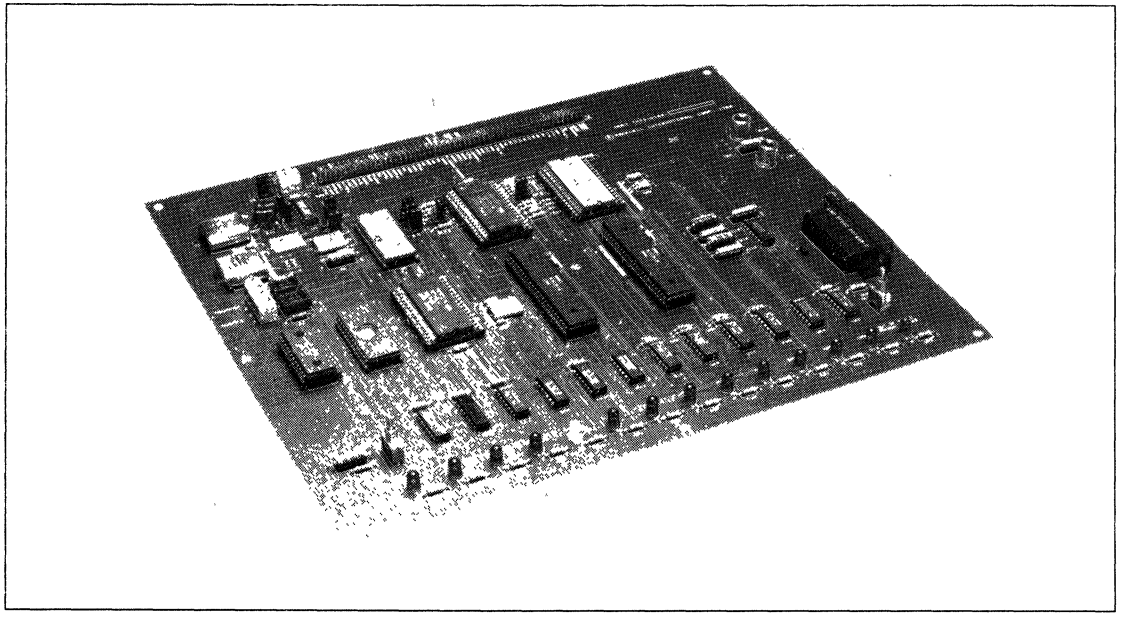
SUMMARY

To aid you in understanding the T-1 carrier and the R8070 PCM30 formats, an R8070 Test/Evaluation Board (R8070EB) has been developed by Rockwell. This useful board also clarifies the operational differences between modes, allows R8070 check-out against a known good device and allows interface to the R8071 ISDN/DMI Link Layer Controller and the R8069 Line Interface Unit with additional hardware.

The R8070 Test/Evaluation Board comes complete with a kit containing one R8070, peripheral logic, selection switches, status LEDS that allow the user to view most functions of the R8070 T-1/CEPT PCM30 Transceiver within each mode of operation. Also included is a comprehensive, easy-to-follow user's manual.

FEATURES

- 8" x 12" card on stand-offs for easy access to all pins
- Uses single +5 Vdc supply at 400 to 650 mA
- Zero insertion force quad in-line socket for the R8070
- Plated-through holes interconnected for 68-pin chip carrier "J" socket
- Plated-through holes for R6500/12 CPU
- Two working spaces to add user-defined circuitry



R8070EB Evaluation Board

R8071EB
R8071 Evaluation Board

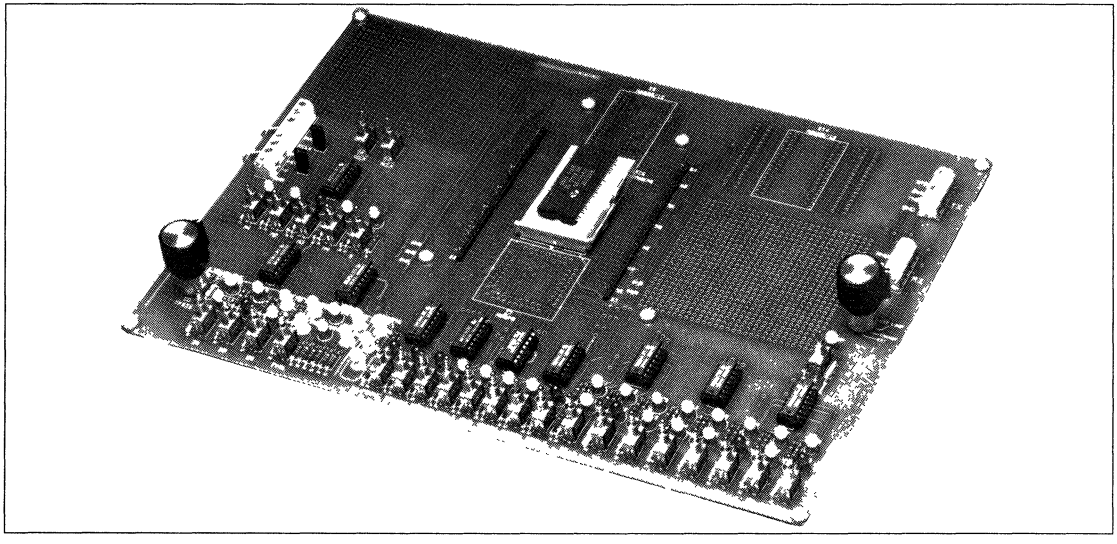
SUMMARY

To aid you in the design of ISDN Primary Rate (T-1/PCM-30) communications systems, Rockwell offers the R8071 Evaluation Board (R8071EB). This board allows you to increase your understanding of the Physical Layer and the Link Layer of the ISDN protocol. The R8071EB provides a menu-driven, user-friendly interface program accessible from a terminal or personal computer equipped with an RS-232-C interface. The software allows for easy system configuration, acceptance of input data from the keyboard, and display of transmitted data and data link condition on the terminal/PC monitor. The transmit and receive data is automatically formatted and unformatted, respectively, according to ISDN, DMI, T-1, and PCM30 standards with minimal user effort. The board also allows functional check-out of the R8071, and provides test access to the R8069 and R8070 devices.

The R8071 Evaluation Board comes assembled and includes three communication devices (R8069 Line Interface Unit, R8070 T1/CEPT PCM Transceiver, and R8071 ISDN/DMI Link Layer Controller), RS-232-C and peripheral logic, Status LEDs, and a Reset switch. A comprehensive, easy-to-follow user's manual guides you through a series of tests and procedures to familiarize you with complete board operation.

FEATURES

- 10" x 12" multi-layer printed circuit board (PCB) on stand-offs for easy access to all pins
- Allows R8071 to be evaluated in all possible configurations
- Provides test access to R8069 and R8070
- Uses single +5 Vdc power supply
- Accessible via terminal/or personal computer with the use of RS-232-C interface
- On-board coupling transformers allow direct connection to T-1 or PCM30 links (jumper selectable)
- User-friendly menu-driven program



R8071EB Evaluation Board

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R8069/R8069A Interface Transformer Specifications and Connections

INTRODUCTION

The R8069 Line Interface Unit (LIU) and R8069A LIU interface to a T-1/PCM-30 carrier line through transmit and receive coupling transformers. This application note specifies the electrical characteristics of these coupling (or interface) transformers. In addition, R8069/R8069A connections to typical transformers are shown.

TRANSFORMER SPECIFICATIONS

The transformers must meet the following specifications:

Transmit Transformer:

Turn Ratio:	1CT:2CT
Rise/Fall Time:	22 ns maximum
Serial Resistance:	0.7 Ω maximum
Primary Inductance:	1.0 mH minimum
Isolation Voltage:	1500 Vrms
Insulation Resistance:	10,000 MΩ minimum
Average Power Rating:	500 mW
Leakage Inductance:	0.30 μH minimum 0.55 μH maximum

Receive Transformer:

Turn Ratio:	1:1
Rise/Fall Time:	22 ns maximum
Serial Resistance:	0.7 Ω maximum
Primary Inductance:	1.0 mH minimum
Isolation Voltage:	1500 Vrms
Insulation Resistance:	10,000 MΩ minimum
Average Power Rating:	500 mW
Leakage Inductance:	0.55 μH maximum

TYPICAL CONNECTIONS

Transformers are available from numerous manufacturers that meet the required transmit and receive transformer's specifications.

As an example, this application note uses the following Pulse Engineering's FALCON series transformers:

Part Number	Name
PE-64943	FALCON 27.1
PE-64934	FALCON 28.0
PE-64954	FALCON 31.1

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CASE 1 - Interface to T-1 Lines Using Separately Packaged Transmit and Receive Transformers

Figure 1 illustrates how to interface the R8069 to T-1 lines through separately packaged transmit and receive transformers. The transmit transformer is a FALCON 27.1 and the receive transformer is a FALCON 28.0.

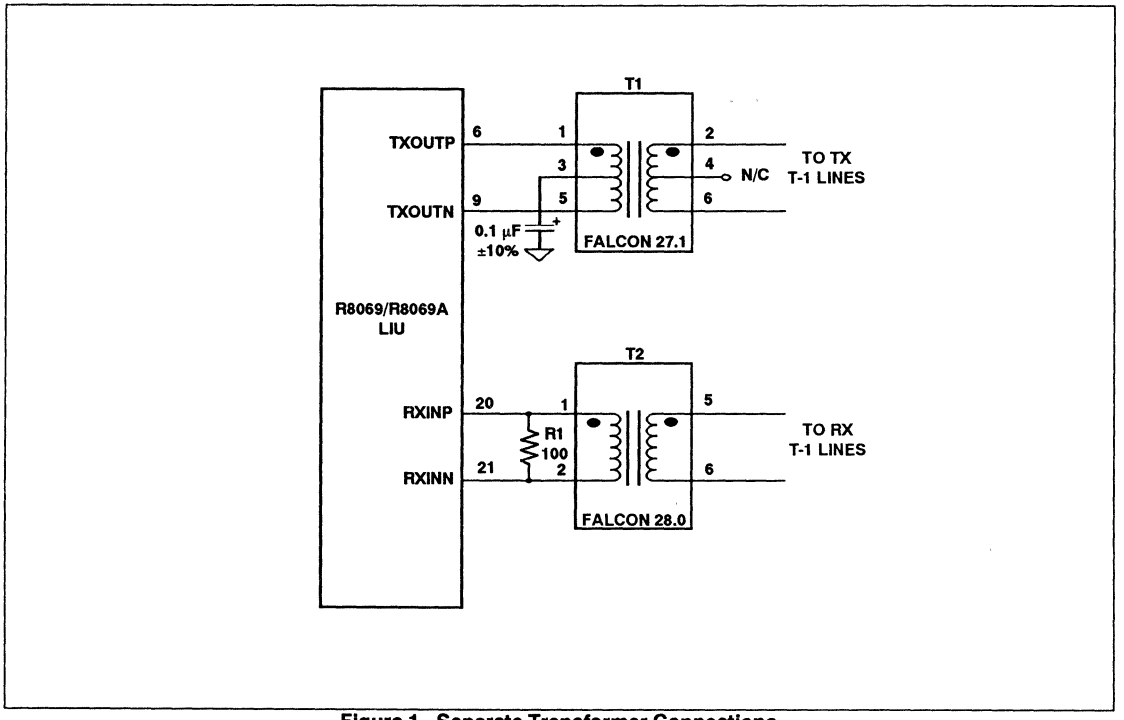

Figure 1. Separate Transformer Connections

CASE 2 - Interface to T-1 Lines Using an Integrated Transmit and Receive Transformer

Figure 2 illustrates how to interface the R8069 to T-1 lines through a FALCON 31.1, which contains both the transmit transformer and the receive transformer in a single package.

CASE 3 - Interface to CEPT PCM 30 Lines

The interface configurations that are illustrated in Case 1 and Case 2 can be applied to a CEPT PCM 30 line simply by installing a 75 Ω or 120 Ω resistor for R1 depending on the application.

For driving a twisted-pair cable to a digital cross connect, the terminating resistor should be 120 Ω. In this case, the R8069 line equalization should be set to select 120 Ω (ELS3 = 1, ELS2 = 1, ELS1 = 0).

The terminating resistor should be 75 Ω and R8069 line equalization set to 75 Ω (ELS3 = 1, ELS2 = 1, ELS1 = 1) for driving a coaxial cable.

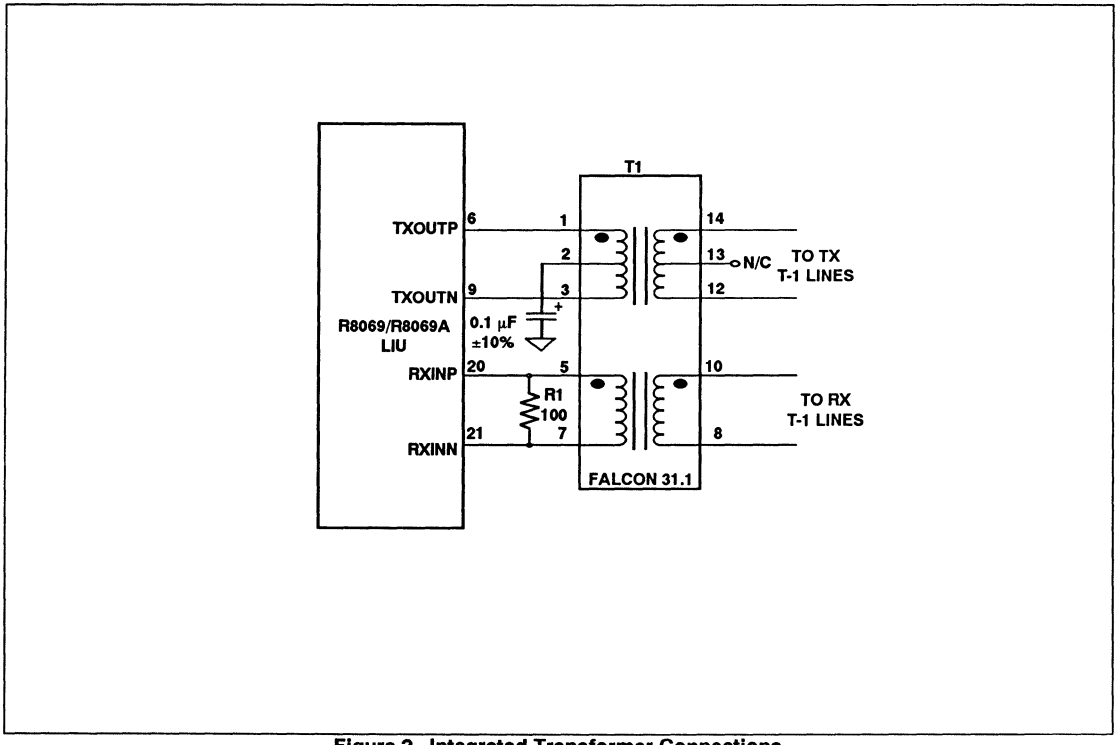

Figure 2. Integrated Transformer Connections

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Which Mode For Data Transmission?

INTRODUCTION

The T1 digital transmission system was developed as a means for increasing cable capacity, originally for voice transmission. Twenty four multiplexed, PCM encoded voice channels plus associated signaling can be simultaneously transmitted over a single twisted-pair cable at 1.544 Mbps.

The T1 system may, however, also be used for the direct transmission of digital information. When selecting a suitable mode for data transmission, the following subjects should be considered.

- R8070 Mode
- Zero Suppression
- Signaling
- Synchronization

R8070 MODE

The R8070 T1/CEPT PCM Transceiver has eleven operating modes covering the standard data formats, with or without signaling, of both the North American T1 and European CEPT PCM 30 transmission standards. These modes are summarized in Table 1.

Each mode is characterized by the number of bits per frame (193, 197, or 256), the availability of signaling (N, S, E or F) and the method of zero-suppression (B8ZS, B7 or HDB3).

ZERO SUPPRESSION

To maintain the D.C. line voltage near zero and to facilitate clock recovery, the transmitted T1 signal must contain no more than 15 consecutive zeros. The R8070 implements several forms of zero suppression to accommodate the requirements of each transmission standard.

B7 BIT-7 STUFFING

If the eight data bits in a channel would otherwise be all zeros, bit 7 is forced to a "1". Do not confuse this term with the method of adjusting clock timing—no extra bits are "stuffed" in zero suppression.

Since a bit which is forced to "1" looks like a valid "1", it is not possible for the receiver to recover the original data. This technique is therefore not suitable for data transmission. (The error is insignificant in voice transmission.)

B8ZS BIPOLAR 8-ZERO SUBSTITUTION

This method uses a special code to represent the occurrence of eight consecutive zeros. Note that these eight zeros may include the Terminal Framing (Ft) bits, Signaling Framing (Fs) bits, or Link bits; they are not restricted to the eight channel-bits as they are in the B7 method.

Since the special 8-zero code includes intentional bipolar violations in a predetermined sequence, the receiver can recover the original data pattern. This technique is therefore suitable for data transmission.

HDB3 HIGH DENSITY BIPOLAR 3-ZERO

This method is similar to B8ZS but allows only three consecutive zeros before applying zero suppression. This is required by the European CEPT PCM 30 standard. Intentional bipolar violations are used to allow recovery of the original data. This technique is suitable for data transmission.

R8070 Operating Mode Selection and Characteristics

Mode	Data Rate (Mbps)	Bits/Frame	Frames/Multiframe	Signaling	Zero Suppression	Mode Select Lines M1	M2	M3	M4	PCM Format
193S	1.544	193	12	Yes	B8ZS	1	0	1	0	T1 (D4)
193S			12	Yes	B7	0	0	1	0	
193N			4	No	B8ZS	1	1	1	0	
193N			4	No	B7	0	1	1	0	
193E	1.544	193	24	Yes	B8ZS	1	1	1	1	Extended Superframe Format (ESF)
193E			24	Yes	B7	0	1	1	1	
193F			24	Special	B8ZS	1	0	1	1	
197S	1.576	197	12	Yes	Transparent	1	0	0	0	T1C
197N			4	No	Transparent	1	1	0	0	
256S	2.048	256	16	Yes	HDB3	0	0	0	0	CEPT PCM 30
256N			2	No	HDB3	0	1	0	0	

Notes: B7: Bit 7 is forced to a 1 (stuffed) on an otherwise all zero channel. HDB3: High Density Bipolar 3-zero maximum.
B8ZS. Bipolar 8-zero substitution. Transparent: No zero suppression or substitution.

TRANSPARENT

No zero suppression takes place, the zeros are transmitted intact. The transparent mode is used in the 197 modes which are intended for T1C applications. It may also be invoked at any time, by connecting RPOS to RNEG, to facilitate testing.

When connecting RPOS to RNEG, do not leave them connected to TPOS and TNEG as this would short circuit the transmitter outputs. In a local test of the transmitter and receiver of an R8070, it is convenient to connect TNRZ to RPOS and RNEG. If TPOS and TNEG are from a remote source, they should be OR'd and connected to RPOS/RNEG to invoke the transparent mode. If it is desired not to have the receiver operate, connect RPOS to RNEG to logic 0. This avoids RPOS = RNEG = 1 which would invoke the transparent mode thus disabling the B8ZS or HDB3 zero suppression. Under no circumstances should RPOS and RNEG be left floating.

SIGNALING

In the European CEPT PCM 30 standard, a separate channel (time slot 16) is allocated for signaling so there is no interference with the data channels, which may convey data or voice information without restriction.

In the North American T1 standard, the signaling information is conveyed within the data channel by replacing data bit 8 with a signaling bit A (for each channel in frame 6) and a signaling bit B (for each channel in frame 12). For voice communication this loss of information is not important, but in data communication it produces unacceptable errors and should be avoided.

In the non-signaling modes, the A and B signaling bits are not inserted. At first this appears to be satisfactory for data transmission, but see the notes on synchronization below.

In the signaling modes it is possible to avoid the insertion of the signaling bits:

SERIAL DATA INTERFACE TO THE TRANSMITTER — TSER

If TSIGMD = 0, the signaling bits are input via IA and IB.
If TSIGMD = 1, the signaling bits are input via TSER.

If TSIGMD is set to "1" the serial data input is correctly transmitted because the signaling bits are assumed to be contained within the data stream.

PARALLEL DATA INTERFACE TO THE TRANSMITTER — T1-T8

In this case, A and B signaling bits must be supplied via IA and IB. To preserve correct data transmission, IA and IB may be tied together and connected to T8. Thus the signaling bits take the same value as the data bits they replaced.

SYNCHRONIZATION

The R8070 uses the received Ft and the Fs pattern to establish and maintain synchronization with the frame and multiframe structure. Ft is simply an alternating sequence of "0"s and "1"s which can usually be distinguished from the random pattern of digitalized voice contained in the channels. However, this simple pattern is more readily imitated by data signals, which may be less random in nature. Thus it may be more difficult to preserve synchronization when data is transmitted.

Those modes which include signaling usually have more frames per multiframe and carry a longer, more easily identified framing pattern. This facilitates synchronization in the presence of data signals.

The longer F bit sequences in the Extended Framing modes (193E and 193F) provide even greater assurance of correct synchronization. In addition, they include a 6-bit cyclic redundancy checksum (CRC bits) that allows detection of 98.4 percent of error-containing frames.

SUMMARY

When considering a suitable mode for data transmission:

1. Don't use B7 zero suppression—it forces data errors; use B8ZS or HDB3.
2. Avoid "robbed" signaling bits that overwrite data bit 8. For parallel data input, tie IA to IB to T8. For serial data input, select TSIGMD = 1.
3. Signaling modes may facilitate synchronization in the presence of "Ft imitating" data.
4. The Extended Framing modes provide a cyclic redundancy check for detection of 98.4% of error-containing frames.

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Monitoring and Controlling the Synchronization State

INTRODUCTION

This note describes the signals that allow the R8070 synchronizer state to be monitored and controlled.

Figure 4-1 on page 4-3 of the R8070 Designer's Guide (Order No. 313, Rev 1) shows the various states through which the Master State Controller passes as it gains or loses synchronization Each of the eight states is represented by a three-bit number MS3, MS2 and MS1, where MS3 is the most significant bit.

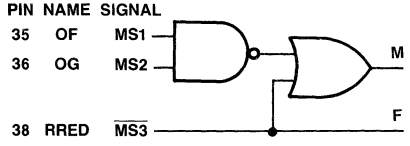
The current synchronization state may be monitored and controlled by various status outputs and control inputs Further information may be derived by logical combinations of the available signals See the referenced paragraph in the R8070 Designer's Guide for additional information

MS1, MS2, MS3 — MASTER STATE SEQUENCE CODE (PARA. 5.3.7.1)

In 193N and 193S modes, MS1 and MS2 are available at pin 35 (OF) and pin 36 (OG), respectively These signals are not available in other modes

In all modes, RRED (Red Alarm) is the same as "Inverse MS3" RRED goes high to indicate a loss of frame sync (in states Wait, Init, Search, and Demons), and goes low to indicate correct frame sync (in states P1, P2, P3 and "In Sync") The "In Sync" state indicates that both the frame and multiframe are aligned (synchronized).

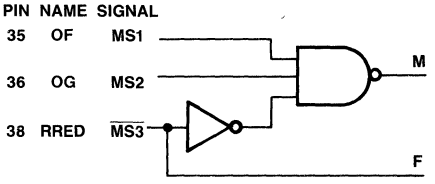
To produce a separate logic function for Multiframe sync, the following circuit may be used.



M = $\overline{MS1 \cdot MS2}$ + $\overline{MS3}$
M = 1 FOR LOSS OF MULTIFRAME SYNC.

F = $\overline{MS3}$
F = 1 FOR LOSS OF FRAME SYNC.

Alternatively, by applying De Morgan's theorem to the logic function for M.



M = $\overline{MS1 \cdot MS2 \cdot MS3}$
M = 1 FOR LOSS OF MULTIFRAME SYNC.

F = $\overline{MS3}$
F = 1 FOR LOSS OF FRAME SYNC.

RSYNC — RECEIVER SYNCHRONIZATION STATE (PARA. 5.3.2.3)

This output may be decoded to provide an indication of the sync state It is useful in modes other than 193N and 193S that do not have MS1 and MS2 available.

RSYNC also provides a useful marker pulse occurring at the first F-bit of each multiframe. This pulse is only valid if the receiver is multiframe aligned (i.e., in the "In Sync" state of the synchronizer sequence).

RMRST — RECEIVER MASTER RESTART (PARA. 5.3.1.3)

This input may be set to a "1" at any time to force the synchronizer back to the "Wait" state and thereby begin the synchronization process again. The "Wait" state is held as long as RMRST is high

RSRCH — RECEIVE SEARCH CONTROL (PARA. 5.3.1.4)

If, while in the "Wait" state, RSRCH goes low, the synchronizer remains in the "Wait" state. RSRCH does **not**, however, force the synchronizer to the "Wait" state, as RMRST does.

The normal use of this input is during correct frame alignment (i.e., when RRED = 0). If RSRCH is set to a "0", bit 5 is skipped in the first channel of the first frame of the next multiframe This bit slipping allows elastic stores to recenter, which is necessary if transmit and receive clock frequencies are marginally different.

D1D = D2 = 1 — SYNCHRONIZATION LOCK (PARA. 5.2.1.1)

When a serial data interface to R8070 is used, RSQ1-RSQ5 (Receive Sequence Code) and TSQ1-TSQ5 (Transmit Sequence Code) indicate which channel has been received or is to be transmitted. These codes equal the five-bit binary value of the channel number. The order in which the codes are produced can be selected by D1D and D2 for compatibility with D1D or D2 channel banks, or to be in normal numerical sequence according to the CCITT convention.

In addition, if D1D = D2 = 1 then the normal CCITT numbering sequence is used, and, once in synchronization, the receiver is locked in that state and will not attempt to resynchronize, even if frame errors occur.

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Bipolar Violation/Loss of Carrier (RVLL) Signal Separation

INTRODUCTION

The signal RVLL is available in all modes and provides a combined indication of "Bipolar Violation" and "Loss of Carrier" for T1 modes. This note describes a method to separate the two signals. (For CEPT PCM 30 modes, RVLL indicates only Bipolar Violation, so no separation is required.)

BIPOLAR VIOLATION

A bipolar violation of the Alternate Mark Inversion (AMI) code, where "1"s are represented alternately as positive and negative pulses, is an occurrence of a pulse of the wrong polarity. To indicate a bipolar violation, RVLL goes high coincident with the emergence of the accused bit at RSER.

LOSS OF CARRIER

A loss of carrier means that no pulses are detected of either polarity; in other words, continuous zeros are received. To indicate loss of carrier, RVLL goes high coincident with the emergence of the 31st zero at RSER. RVLL will return to zero when a "1" is received that is not a bipolar violation.

The term "loss of carrier" is rather confusing since there is no carrier in a T1 system. The channel data at 64 kbps is time-division multiplexed to a higher data rate of 1.544 Mbps but not modulated, hence there is no carrier.

The clock is not actually "recovered" from the data, rather, a local clock is synchronized to the incoming data rate. Hence a loss of pulses on the line does not stop the Receive Clock, although the clock may drift out of synchronization. A lack of data pulses indicates a transmitter or transmission fault and this is indicated by the "Loss of Carrier" signal.

SIGNAL SEPARATION

These two signals may be distinguised by examining the logic value of RSER.

1. A bipolar violation can only be caused by a received pulse (of the wrong polarity). This pulse represents a binary 1, so RSER will be "1".

2. A loss of carrier implies the reception of consecutive zeros, so RSER will be "0".

The circuit shown in Figure 1 separates these two signals on this basis.

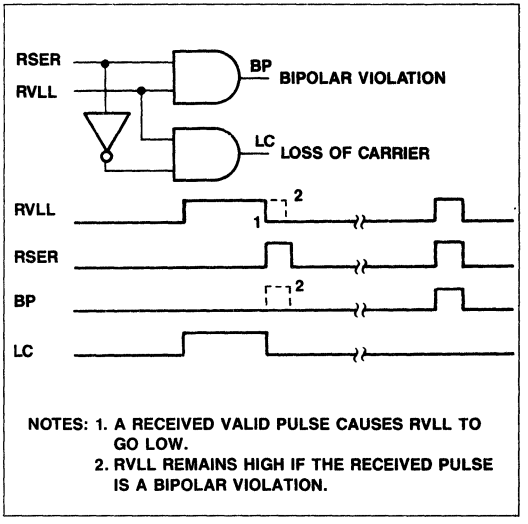

Figure 1. Bipolar Violation/Loss of Carrier Separation Circuit

Nominally, RSER and RVLL transition simultaneously but a slight timing difference could result in a glitch at the outputs of this circuit. To overcome this glitch, the outputs BP and LC should be latched on the falling edge of RCLK to avoid the transitions on the rising edge of RCLK (Figure 2).

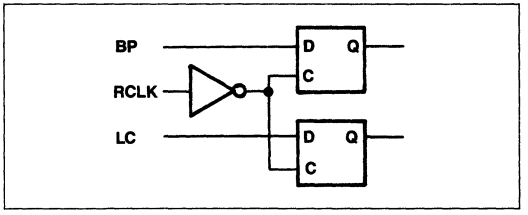

Figure 2. BP and LC Latch Circuit

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Producing AMI Code from TPOS and TNEG

INTRODUCTION

AMI—ALTERNATE MARK INVERSION

AMI is a transmission code where binary zeros are represented by zero volts and binary ones are represented alternately as positive or negative pulses. In the T1 system, the pulses are about 3 volts in amplitude with a pulse shape conforming to the pulse "mask" described in the CCITT Recommendation G.703. A Line Interface Unit (LIU) must be used to convert the R8070 TTL signals to AMI format and provide the required pulse shaping.

AMI code is used for several reasons:

1. It's a bipolar code having an equal number of positive and negative pulses with a resultant D.C. voltage of zero. This A.C. signal allows the use of transformers to couple the LIU to the T1 line, thus facilitating the design of protection devices (e.g., for lightning protection).

2. The signal frequency is effectively halved. The maximum frequency occurs for the transmission of an alternating sequence of zeros and ones. Intuitively, if alternate ones are represented by negative pulses, the period between adjacent positive impulses is twice as long. Hence, the bandwidth required to transmit data in bipolar AMI format is half that required for the original unipolar data.

3. Any noise on the line which is large enough to be mistaken for a data pulse can be rejected as a bipolar violation if it has the same polarity as the previous pulse. AMI therefore allows some error protection to be provided.

NRZ—NON-RETURN-TO-ZERO

A logic level that is maintained for the complete bit time. In the T1 system the clock rate is 1.544 Mbps so the bit time is thus 648 ns.

RZ—RETURN-TO-ZERO

A logic level that is maintained for part (usually half) of a bit time. This is used in the AMI code.

TNRZ—TTL LEVEL NON-RETURN-TO-ZERO

A standard TTL-level, Non-Return-To-Zero, binary output.

TPOS, TNEG

A pair of R8070 outputs both of which are NRZ, positive voltage, TTL-level signals. They assist in producing an AMI coded version of the standard TTL binary output from TNRZ. They are not, themselves, in AMI format.

UNIPOLAR TO BIPOLAR AMI CONVERSION

The circuit in Figure 1 shows a typical method of converting from the paired, unipolar NRZ outputs, TPOS and TNEG, to an RZ AMI code suitable for transmission over a T1 line.

Data outputs TPOS and TNEG are first gated with the inverse of TCLK. This selects the second half of each bit-wide data pulse producing RZ versions, TPOS(RZ) and TNEG(RZ). The second half is chosen because it is stable; the first half includes the transition of the leading edge.

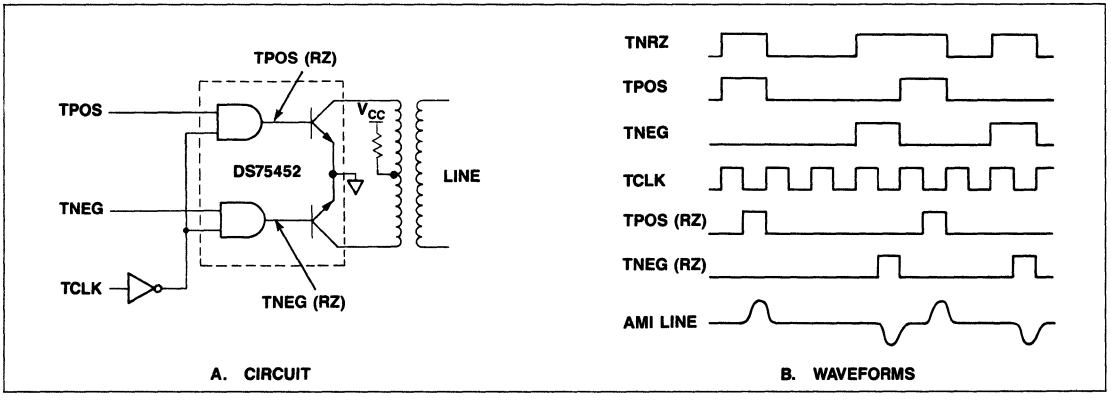

Figure 1. Typical AMI Line Interface and Waveforms

These RZ pulses are applied to a pair of push-pull driver transistors, producing positive pulses from TPOS(RZ) and negative pulses from TNEG(RZ) which are coupled to the line by a pulse transformer.

This is not intended to be a detailed circuit schematic; it describes only the concept of AMI conversion.

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Zero Suppression Methods (B7, B8ZS and HDB3)

INTRODUCTION

This note explains how the B7, B8ZS and HDB3 zero suppression methods are implemented in the R8070 and describes typical waveforms at the R8070 transmitter outputs TNRZ, TPOS and TNEG.

ALTERNATE MARK INVERSION (AMI) CODE

Figure 1 reviews the basic Alternate Mark Inversion (AMI) code. Inverse TCLK is gated with TPOS and TNEG to produce the return-to-zero, alternating bipolar pulse of AMI.

A bipolar violation (BV) is a pulse of the same polarity as that which precedes it. Figure 1 illustrates an example of a bipolar violation caused by noise on the transmission line..

The R8070 will decode a BV to a "1" and present it at RSER with a coincident pulse on RVLL to indicate a violation. The R8070 does not internally suppress bipolar violations; that is left as an option for the user to implement externally, using the RVLL signal. However, if the R8070 detects a zero substitution pattern of BVs, then the received "1"s are replaced by "0"s to recover the original data. In this case RVLL remains low.

Both the North American T1 system and the European CEPT PCM 30 system require AMI line code. Also, they both require a minimum "ones density", so the number of consecutive zeros must be limited using a method of zero suppression. The T1 system uses either B7 or B8ZS; the CEPT PCM 30 system uses HDB3.

ZERO SUPPRESSION METHODS

B7—BIT-7 STUFFING (ZERO CODE SUPPRESSION)

The incoming channel data to the R8070 transmitter is monitored for an all zero condition. If all eight bits are zero, bit-7 is forced to a "1" and the resulting 00000010 pattern is transmitted in place of 00000000, with the "1" correctly output on TPOS or TNEG (i.e., not a bipolar violation). The "1" is also output on TNRZ. An alternative name for this method is Zero Code Suppression.

At the receiver, the "stuffed 1" cannot be distinguished from a normal "1", so the original data cannot be recovered.

Note that zero monitoring is performed on a channel basis and also excludes the F-bit. It is possible for more than eight consecutive zeros to be transmitted. For example, if only bit 1 of channel N is "1" and channel N + 1 is all zero, then channel N + 1 would have have bit 7 forced to "1" and there would be 13 consecutive zeros (bits 2-8 of channel N and bits 1-6 of channel N + 1). The standard requires that no more than 15 consecutive zeros be transmitted.

Figure 2 shows typical B7 waveforms. Channel 23 contains arbitrary data "1"s at bits 6 and 7 which are transmitted normally. Channel 24 is all zero so bit 7 is forced to a "1" on TNRZ and output as a valid "1" on TPOS/TNEG. The F-bit is transmitted normally. Channel 1 is all zero and so bit 7 is forced to "1"

B8ZS—BIPOLAR 8-ZERO SUBSTITUTION

The data stream to be transmitted, including F-bits, is monitored for any group of eight consecutive zeros. These eight zeros do

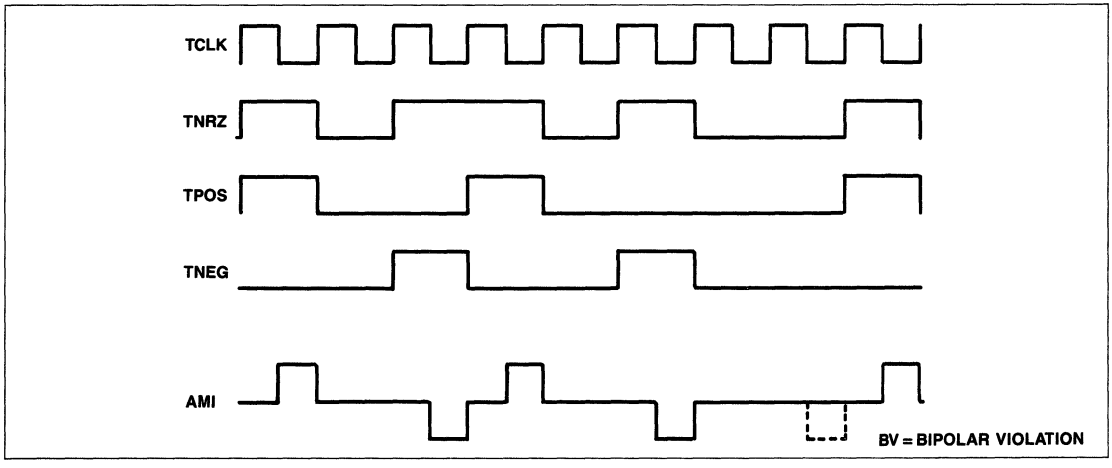

Figure 1. Alternate Mark Inversion (AMI)

Document No. 29300N23

Order No. 323
September 1986

not have to fall in the same channel, they may overlap the channel boundaries or include a zero valued F-bit. An 8-zero group (octet) is replaced with a B8ZS code, shown below.

B8ZS Codes:	1	2	3	4	5	6	7	8	(bit position in octet)
				BV			BV		
Code a	0	0	0	+	−	0	−	+	
Code b	0	0	0	−	+	0	+	−	

Where:

0 = data "0"
\+ = data "1" output on TPOS, to produce a positive AMI pulse
− = data "1" output on TNEG, to produce a negative AMI pulse
BV = bipolar violation

Code a is used if the preceding "1" pulse was positive. Code b is used if the preceding "1" pulse was negative.

This ensures that adjacent BVs alternate in polarity to preserve a D.C. line voltage of zero.

In both codes, bits 4 and 7 are bipolar violations, bits 5 and 8 are normal "1"s and bits 1, 2, 3 and 6 are "0"s. These codes are recognized by the R8070 receiver and the original data is reconstructed.

Figure 3 shows typical B8ZS waveforms. Channel 23 contains arbitrary data "1"s at bits 6 and 7 which are transmitted normally. The next eight bits are zero (bit 8 in channel 23 and bits 1-7 in channel 24) and these eight zeros (not the complete channel 24) are replaced with a B8ZS code. In this case, code a is used because the last pulse was on TPOS.

The search for another 8-zero group begins at bit 8 in Channel 24, and is interrupted by a "1"-valued F-bit, which is transmitted as normal. The search for eight zeros begins again at bit 1, channel 1. Since all eight bits of channel 1 are zero, these are replaced by a B8ZS code. In this case, code b is used because the last pulse was on TNEG.

TNRZ is unaffected by B8ZS coding.

HDB3—HIGH DENSITY BIPOLAR 3-ZERO MAXIMUM

The data stream to be transmitted, including F-bits, is monitored for any group of four consecutive zeros (a maximum of three is allowed). A 4-zero group is replaced with an HDB3 code, shown below.

HDB3 Codes	1	2	3	4	(bit position in 4-zero group)
Code a	0	0	0	BV	
Code b	P	0	0	BV	

Where:

0 = data "0"
BV = data "1" transmitted as a bipolar violation
P = valid "1" pulse (i.e., not a violation)

Two different codes are required to ensure that the BV pulses from adjacent 4-zero groups are of opposite polarity. Code a is used if there is an **odd** number of "1"s after the last BV; code b is used if there is an **even** number.

HDB3 coding is similar to B8ZS and produces similar data patterns, particularly on all-zero channels.

Figure 4 shows typical HDB3 waveforms. The CEPT PCM 30 standard refers to time slots (TS) in the context of the allocated frame space, rather than channels. The data on TNRZ was chosen to illustrate various occurrences of the 4-zero pattern.

Bit 1 of TS1 is a "1" and is transmitted normally. The 4-zero group of bits 2-5 of TS1 are replaced with an HDB3 code. Code a is arbitrarily chosen in this example, as the polarity of the previous BV is not shown. Bits 6 and 7 of TS1 are transmitted as normal "1"s.

The next 4-zero group consists of bit 8 of TS1 and bits 1-3 of TS2 and is replaced by an HDB3 code. In this case, code b is used because an even number of "1"s were transmitted after the last BV. Bits 4 and 5 of TS2 are transmitted as normal "1"s. The search for another 4-zero group begins at bit 6 (TS2) but is interrupted by the "1" in bit 8 of TS2; these bits are all transmitted normally.

Bits 1-4 of TS3 form a 4-zero group and are replaced with HDB3 code a because there was an odd number of "1"s after the last BV. Bits 5-8 of TS3 form another 4-zero group which is replaced by HDB3 code b as there were an even number (zero) of "1"s transmitted after the last BV.

SUMMARY

- B7 — Bit 7 Stuffing
  - — Applicable to T1
  - — Bit 7 is forced in "1" in an all-zero channel
  - — Applied to channel data only — not F bits
  - — Forced errors unrecoverable at receiver
  - — "Stuffed 1" appears on TNRZ
- B8ZS — Bipolar 8-Zero Substitution
  - — Applicable to T1
  - — Any 8-zero group replaced with 00011011
  - — Bipolar violations (BV) allow data recovery
  - — TNRZ not affected
- HDB3 — High Density Bipolar 3-Zero Maximum
  - — Applicable to CEPT PCM 30
  - — Any 4-zero group replaced with 0001
  - — Bipolar violation (BV) allows data recovery
  - — First bit (P) may be "1" to ensure alternate BV polarity
  - — TNRZ not affected

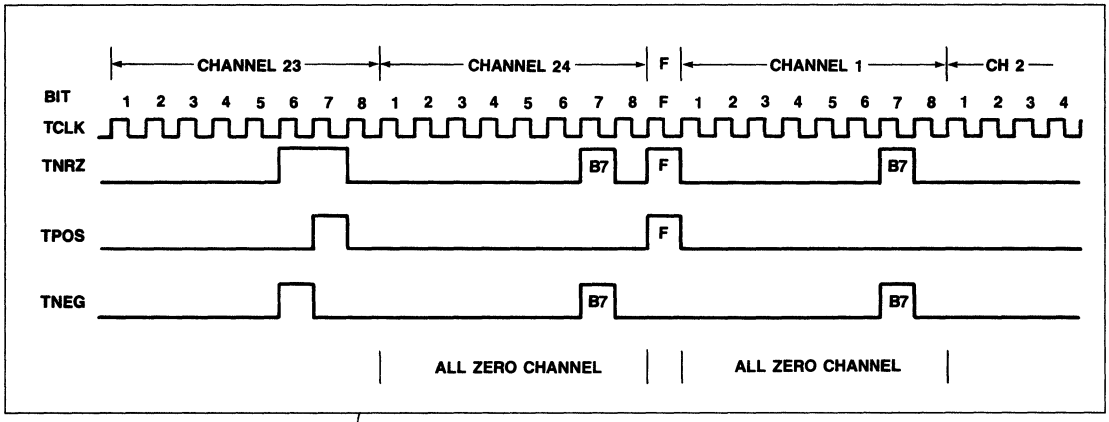

Figure 2. Bit-7 Stuffing (Zero Code Suppression)

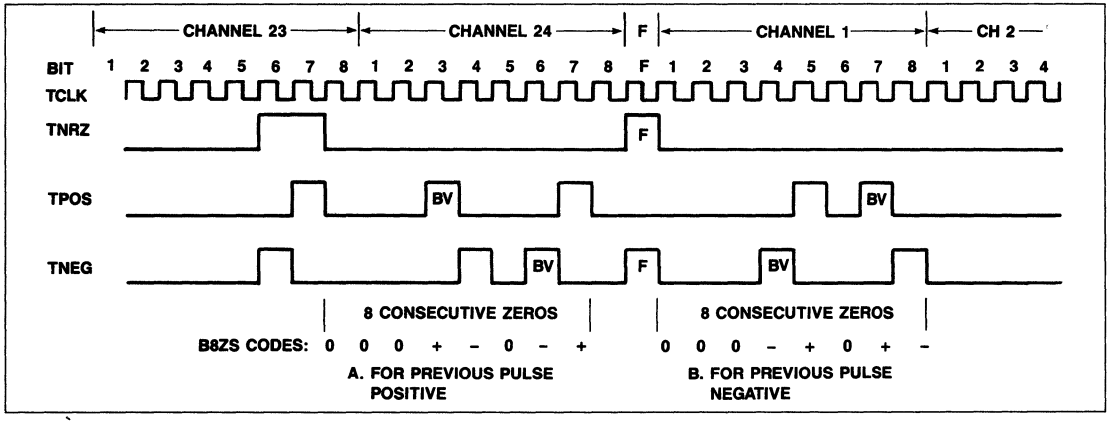

Figure 3. Bipolar 8-Zero Substitution B8ZS

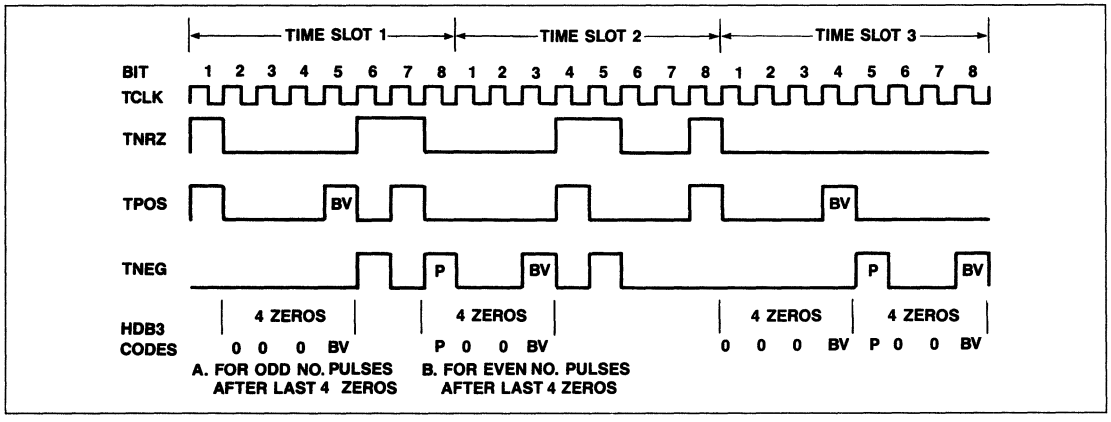

Figure 4. High Density Bipolar 3-Zero Maximum HDB3

Rockwell

Finding the F-Bit

INTRODUCTION

In the North American T1 modes (193 and 197), a framing bit is transmitted at the start of every frame. The sequence of "0"s and "1"s transmitted via this bit position provides frame alignment (Ft), multiframe alignment and identification of signaling frames (Fs), and, in the Extended Superframe Format, a data link and cyclic redundancy check.

The basic framing bits may either be inserted by the user via TFSIG, or generated automatically by the R8070 by connecting TFGEN to TFSIG. In either case, a common requirement is a timing pulse which coincides with the bit interval in which the F-bit is sampled at the transmitter. At the receiver, an equivalent pulse coincident with the F-bit output may also be required.

DERIVING TIMING PULSES

Which signals are available from the R8070 depends on the data interface used; parallel or serial. But the general method of pulse derivation remains the same, as described below and by the Figure 1:

1. Find an R8070 output signal with a pulse repetition frequency (PRF) equal to the frame rate (8 kHz). This may involve decoding several outputs.

2. If necessary, delay the leading edge of the pulse to coincide with the start of the required F-bit time.

3. Stretch or truncate the trailing edge at the end of the required F-bit time. The resulting pulse may then be further gated, stretched or realigned with either a rising or falling clock edge.

Apply this method, or a variation of it, to the R8070 transmitter and receiver for both a parallel and serial data interface.

TRANSMITTER—PARALLEL DATA INTERFACE

The signal TCHSYNC has the required PRF, but the pulse is too wide and occurs too early. Depending on the application, this signal may be used in its present form to load an external F-bit into the R8070.

To produce a one-bit wide pulse that covers the sampling instant of the F-bit, TCHSYNC may be modified as shown in the Figure 2 circuit and the Figure 3 waveforms.

The falling-edge of TCHSYNC clocks a "1" into U1. On the next falling-edge of TCLK, U2 accepts the "1" from U1. The next high level of TCHCLK resets U1, so that on the subsequent falling-edge of TCLK U2 accepts a "0" from U1.

The resulting output is a one-bit wide pulse, aligned on a falling clock edge, that covers the instant of the F-bit sampling.

TRANSMITTER—SERIAL DATA INTERFACE

TCHCLK and TCHSYNC are not available in the serial mode. Instead, TSQ1-TSQ5 may be used. TSQ1-TSQ5 is the binary value of the next channel to be loaded into the R8070. These outputs change two bit-times before the sampling of bit 1 on TSER, thus allowing the user to select the data for the next channel to be sampled. See the Figure 4 circuit and the Figure 3 waveforms.

To indicate the time for F-bit sampling, the TSQ1-TSQ5 outputs are set to 00000 for one bit interval, two bit-times before the F-bit is sampled. The occurrence of all zeros on TSQ1-TSQ5 may be

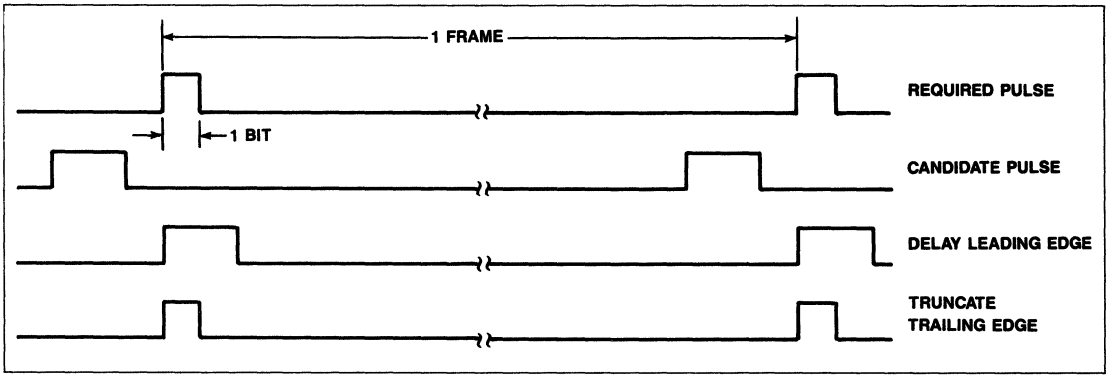

Figure 1. General Method for Deriving Timing Pulses

decoded and then shifted by $1\frac{1}{2}$ bit-times to provide the required F-bit timing pulse. The attached diagrams show the circuit and waveforms.

U1 is a 5-input NOR gate that provides a high level when TSQ1-TSQ5 are all zero. Because the "all zero" condition could momentarily occur during TSQ output changes, the U1 output may contain invalid high levels which do not represent the true "all zero" condition. To remove these glitches, and also to delay the pulse to the required point in time, the U1 output is clocked on the falling-edge of TCLK by two consecutive "D-type" flip-flops.

RECEIVER—PARALLEL DATA INTERFACE

RCHSYNC has the required PRF. RWIHBT and RCHCLK transition at the start and end of the required F-bit time interval. These three signals may be gated to provide the required timing pulse. See the Figure 5 circuit and the Figure 6 waveforms.

RECEIVER—SERIAL DATA INTERFACE

RSQ1-RSQ5 are similar in function to TSQ1-TSQ5. They are 00000 for exactly one bit-time while the F-bit is output at RSER. These outputs may be decoded to produce the required F-bit timing interval. The decoder may contain glitches, but these can be removed by "D-Type" latches which would commonly be used to clock the F-bit from RSER. See the Figure 7 circuit and the Figure 5 waveforms.

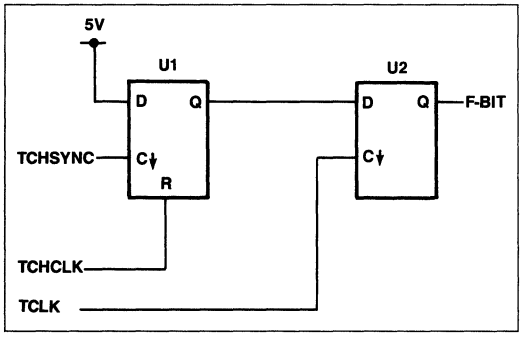

Figure 2. Transmitter—Parallel Data Interface

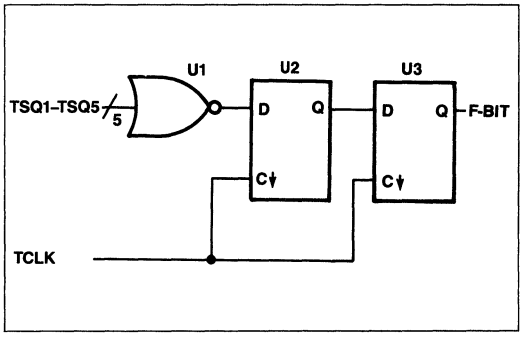

Figure 4. Transmitter—Serial Data Interface

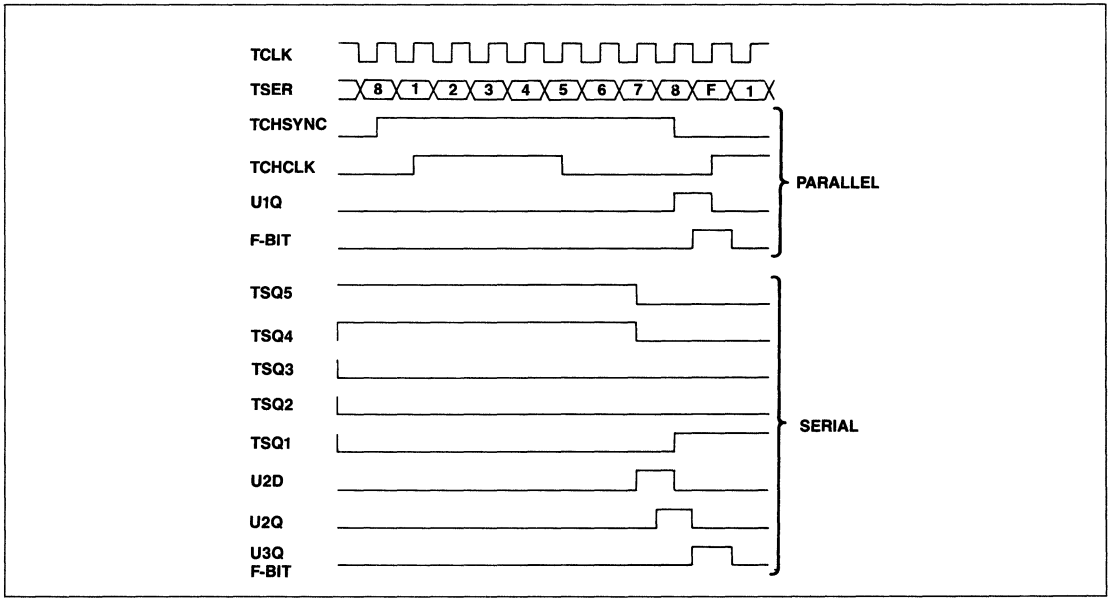

Figure 3. Transmitter—Parallel and Serial Waveforms

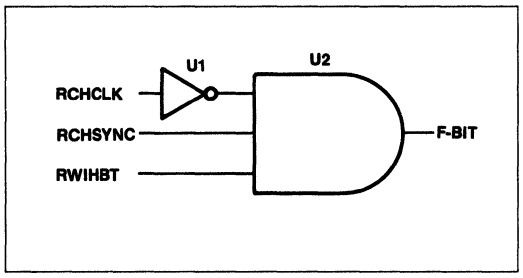

Figure 5. Receiver—Parallel Data Interface

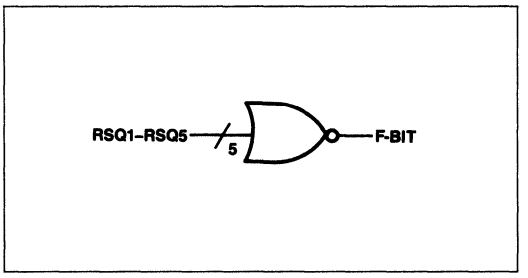

Figure 7. Receiver—Serial Data Interface

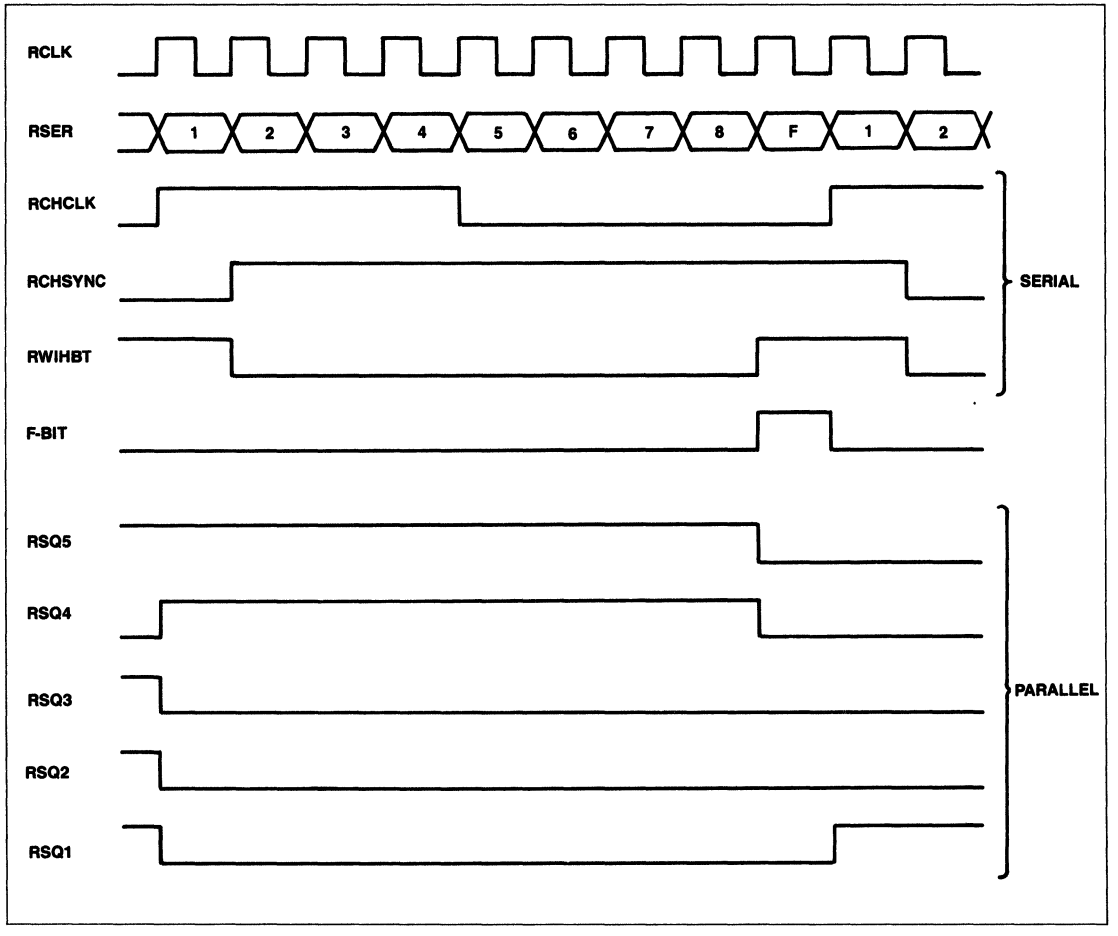

Figure 6. Receiver—Parallel and Serial Waveforms

Rockwell

D4/ESF Conversion Using the R8070

SYSTEM OVERVIEW

D4 is the currently implemented version of T1 in North America, with D3 and D4 being the most common type of channel bank. But the new Extended Superframe Format (ESF) is beginning to replace it. Since the Rockwell R8070 T1/CEPT PCM Transceiver can handle both PCM formats, it is ideally suited to both types of equipment. This application note examines the differences in these two formats and suggests a method for converting between them using the R8070.

DIFFERENCES BETWEEN D4 AND ESF

1. 12/24 FRAMES PER MULTIFRAME

The fundamental difference between D4 and ESF is the number of frames which define a multiframe. D4 has 12 frames; ESF has 24 frames. This larger multiframe provides more signaling bits, and, more importantly, more framing bits (F-bits). It is the definition of these framing bits that characterizes ESF, providing new features and improved performance over the earlier D4.

2. AB/ABCD SIGNALING

Robbed-bit signaling in D4 provides two signaling bits (an A-bit in frame 6, and a B-bit in frame 12) per channel, per multiframe. Since ESF has 24 frames per multiframe, an additional two signaling bits can be provided without robbing more bits from the channel data. These are: a C-bit in frame 18, and a D-bit in frame 24.

The same number of bits are stolen per channel in ESF as in D4, so the rate of signaling remains the same. However, because the robbed-bit signaling method uses simple combinations of the bits (e.g., A = 0, B = 1), rather than a code, to represent on hook/off hook conditions, the four signaling bits of ESF allow an increase in the number of signaling combinations.

3. F-BIT STRUCTURE

The major structural difference between D4 and ESF is in the definition of the F-bits. The larger multiframe of ESF has 24 F-bits, one preceding each frame (as in D4). These 24 bits are allocated to one of three functions:

1. A 6-bit Framing Pattern Sequence (FPS) of 001011 which performs the same frame- and multiframe-defining functions as the Ft and Fs bits of D4.
2. A 6-bit Cyclic Redundancy Checksum (CRC) which provides a block check on the integrity of the previous multiframe.
3. A 12-bit Data Link Facility which gives a 4 kHz link for alarm monitoring, signaling, error reporting, etc. The latest Bellcore specification for ESF allocates certain of these link bits for specific error and alarm purposes.

D4/ESF CONVERSION

Figure 1 illustrates a simplified form of a D4/ESF converter. Looking to the left is a D4 facility, looking to the right, ESF. The elementary requirements of the converter are:

1. To reformat the F-bits, preserving multiframe alignment.
2. To correctly pass data for each of the 24 channels.
3. To convey signaling information.
4. To generate and check CRC bits.

Most of these functions are carried out automatically by the R8070. Two R8070s are required; one is configured for the D4 format, the other for ESF.

MULTIFRAME ALIGNMENT

In order to correctly generate the F-bits for each PCM format, each transmitter must have the same multiframe alignment as the receiver in the other R8070. When dealing with TX/RX

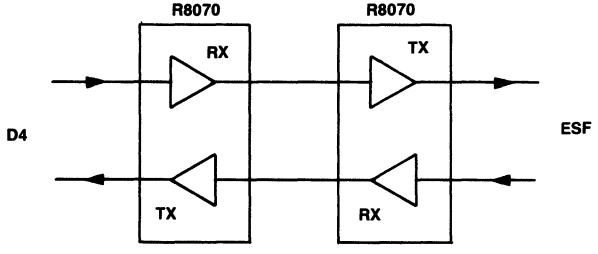

Figure 1. D4/ESF Conversion Using Two R8070s

connections in the same PCM format (e.g., for loopback testing), alignment is achieved by simply connecting RSYNC to TMSYNC and TFSYNC. This is also the case with a D4/ESF converter, but with the added complication of the different multiframe lengths.

Figure 2 compares the multiframe lengths of D4 and ESF. When the R8070 receiver is correctly synchronized, RSYNC produces one pulse per multiframe coincident with the F-bit of frame 1 on RSER. The ESF format will result in one pulse every 24 frames; D4 results in one pulse every 12 frames.

D4 to ESF

Put simply, D4 has twice as many RSYNC pulses as the ESF transmitter needs on TMSYNC. A means of selecting alternate RSYNC pulses is required. TSIGSEL from the ESF transmitter is suitable as a gating signal. TSIGSEL is constantly generated by the transmitter according to the last received alignment or synchronizing signal on TMSYNC. TSIGSEL is low for 12 frames and high for 12 frames (see Figure 2).

Figure 3 shows the gating arrangement. When the transmitter and reciever are correctly aligned, TSIGSEL will allow alternate RSYNC pulses to reach TMSYNC/TFSYNC.

If the receiver loses synchronization with its incoming signal, RSYNC will no longer have the normal multiframe period. For the exact operation of RSYNC, see the R8070 Designer's Guide (Order No. 313). To avoid spurious RSYNC pulses (while the receiver is resynchronizing) from affecting the transmitter, RSYNC may be additionally gated with inverse RRED. If the receiver loses frame alignment, RRED will go high (inverse RRED will go low) and TMSYNC will receive no further pulses until frame alignment is re-established. The transmitter would therefore maintain its previous frame and multiframe alignment during the receiver's resync period.

ESF to D4

In the return direction from ESF to D4 the opposite is true: the ESF receiver produces only half the number of expected pulses at TMSYNC. This is not a problem because TMSYNC/TFSYNC only need one pulse to set the frame and multiframe alignment. If no pulses are applied to these transmitter inputs, the previous alignment is assumed to continue — the internal bit- and frame-counters auto-reset. A direct connection between RSYNC and TMSYNC/TFSYNC can therefore be used (see Figure 3).

To prevent spurious RSYNC pulses (during receiver resynchronization) from affecting the D4 transmitter, RSYNC may be gated with inverse RRED (see D4 to ESF).

THE DATA CONNECTION

The interconnection of channel data between the receiver and the transmitter follows the same pattern as for loopback testing. Figure 4 shows the serial and parallel data connections.

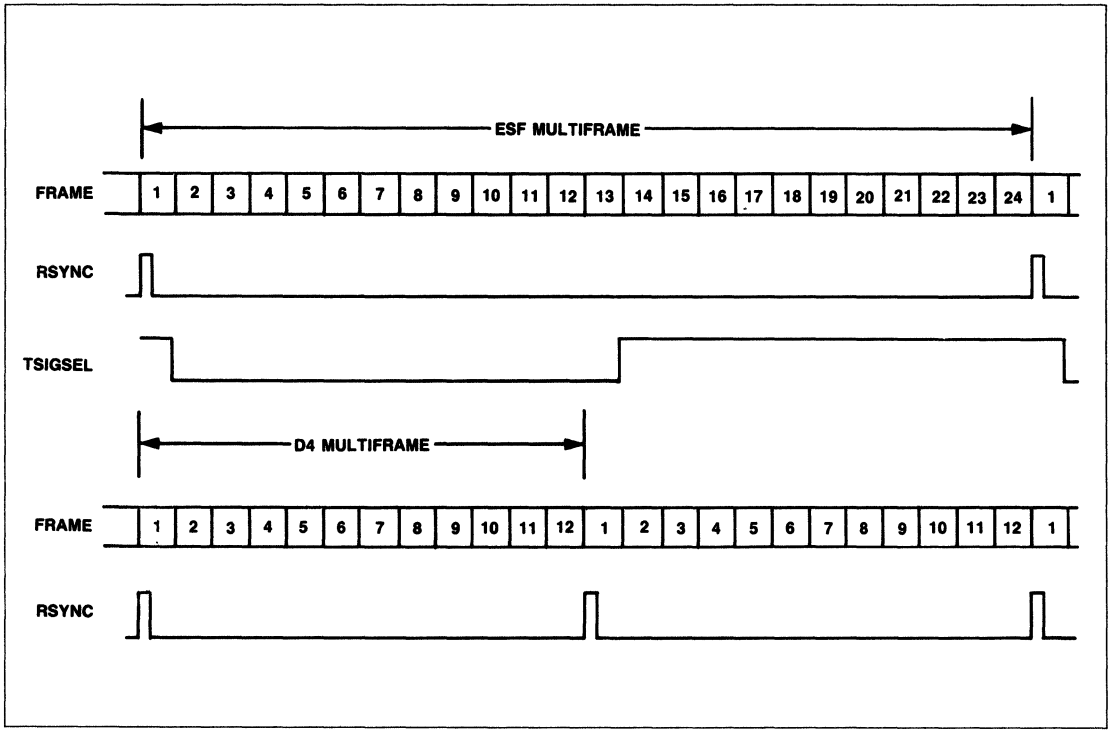

Figure 2. RSYNC Alignment in D4 and ESF

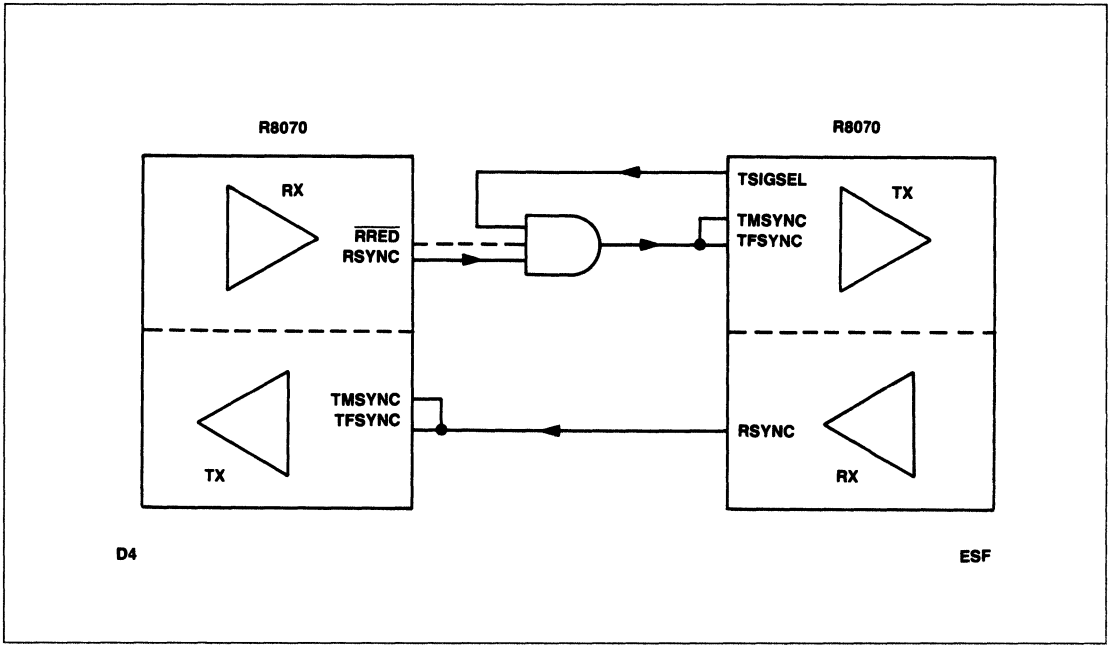

Figure 3. Transmitter and Receiver Alignment

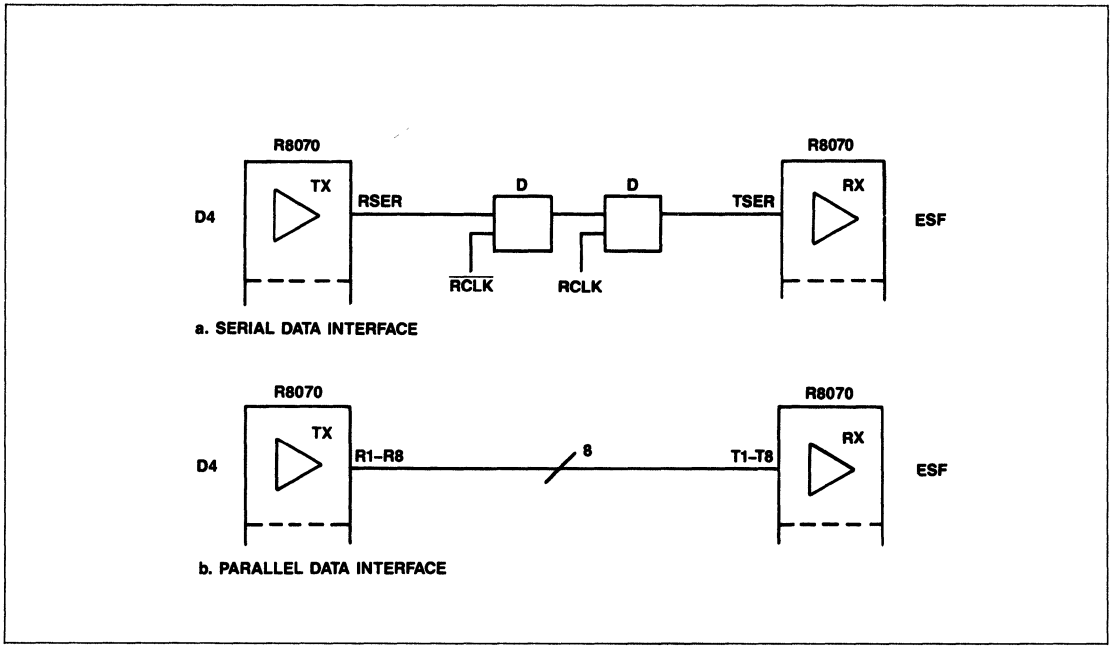

Figure 4. The Data Connection

Serial Path

The serial path requires D-type flip-flops to meet the setup time for TSER and provide one bit delay for correct synchronization between the transmitter and receiver. The serial technique has the advantage that data is always correctly recovered by the receiver even if it loses synchronization, although it would, of course, be subject to failure for a complete data loss. RSER contains the same data as the inputs, RPOS and RNEG. This would be important if the transmitter must maintain its present alignment during periods of resynchronization.

Parallel Path

The parallel path is simply a direct connection between R1–R8 and T1–T8. The parallel technique has the advantage of requiring no external circuits, but its data is subject to correct frame alignment. R1–R8 is gated to zero when frame alignment is lost.

SIGNALING

"Robbed" Bits

Figure 5 compares the different signaling arrangements of D4 and ESF. The basic signaling technique is the same in both formats; the least significant bit from each channel is "robbed" in every sixth frame. The robbed bits are replaced with signaling bits denoted A-bits in frame 6, B-bits in frame 12, and (for ESF) C-bits in frame 18 and D-bits in frame 24.

In the D4 to ESF direction the position of the C- and D-bits would be taken by the A- and B-bits, respectively, as there is no other information to be sent.

The problem arises in the ESF to D4 direction. The capacity of the signaling channels is the same in both formats. But if ABCD signaling was transmitted from the ESF side, it could not be correctly extracted by the D4 receiver at the far end, even though the D4 transmitter in the converter correctly passed all the signaling bits. This is because the shorter D4 multiframe does not permit all four bits to be distinguished; the A and C bits occupy the same frame relative to the RSYNC pulse, so do the B and D bits.

The easiest solution is to permit only A and B signaling on the ESF side. A more ambitious solution might attempt to code the ABCD bits, but this would involve decoding at the final D4 destination in equipment over which there is no control.

Facility Data Link

As with the enhanced signaling capability, the link channel afforded by the extra F-bits of ESF is not available in D4. However, one of the 24 data channels could be assigned for signaling and link data purposes.

HANDLING CRC

CRC is only required on the ESF side and is handled automatically by the R8070. CRC is often used to monitor the performance of the PCM link but in this case CRC will not travel the complete link. However, details such as number of errored multiframes could be computed by the converter and transmitted back on the ESF side using the Facility Data Link.

TRANSMITTER AND RECEIVER CLOCKING

As with any receiver to transmitter connection, care must be taken to observe setup and hold times (see application note entitled, "Loopback Testing with the R8070," Order No. 327). The clock for each receiver would normally be recovered from or synchronized to the line data rate. The transmitters could take the same clock as the receiver from which they get data, but to ensure the specified setup times are met, it is convenient to make the transmitter's clock the inverse of the receiver's. This applies to both directions of the format conversion.

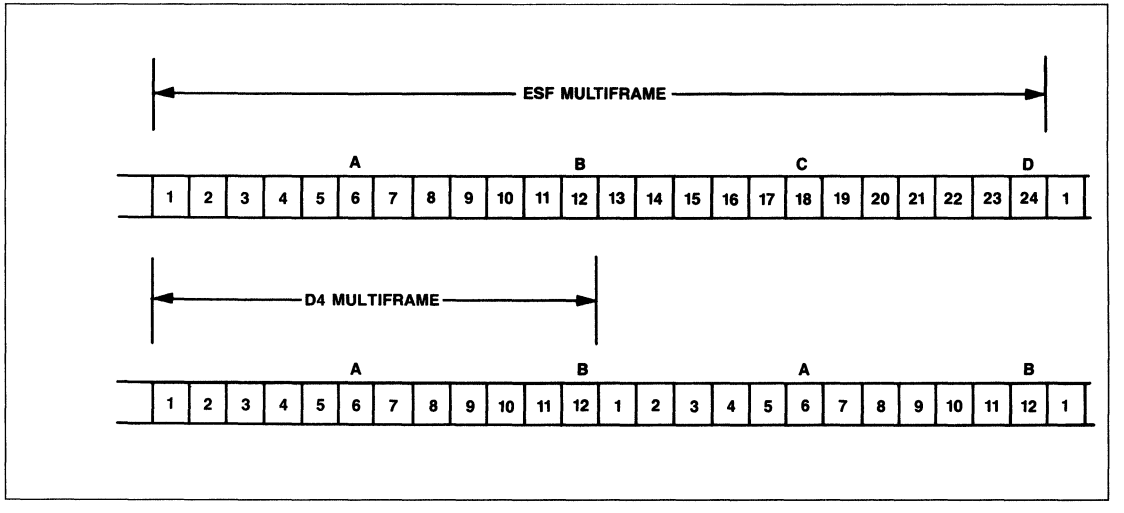

Figure 5. D4 and ESF Signaling

Rockwell

Loopback Testing with the R8070

SYSTEM OVERVIEW

Figure 1 shows a typical T1 link or span between two central offices (COs) which for reference are termed the near-end and far-end offices. The T1 span consists typically of two twisted-pair wires; one pair for transmit, one pair for receive. Digital repeaters are placed at one mile intervals to maintain the quality of the PCM signal. A Rockwell R8070 T1/CEPT PCM Transceiver at each end of the link implements the transmit and receiver functions.

LOOPBACK TESTING

Loopback is a form of testing in which the transmit and receive paths are connected so as to route the signal from the near end (or far end) back to itself. Figure 1 shows four possible positions for the loopback connection. By applying loopback in stages, progressively further from either end of the link, a faulty section can be located. This is termed Failure Sectionalization (Paragraph 6.6, Section A, Bell Publication 43801).

TYPES OF LOOPBACK

1. Loopback is local if the signal is looped at the near end. This is a transmitter-to-receiver loop, shown as Loop 1 in Figure 1. This type of loopback is provided internally by the R8070.
2. Loopback is remote if the signal is looped at the far end. This is a receiver-to-transmitter loop, shown as Loop 4 in Figure 1. This type of loopback is performed by a simple interconnection externally to the R8070.

Loopback can also be made at the line interface, shown as Loop 2 and Loop 3 in Figure 1. This type of loopback is independent of the R8070.

LOCAL LOOPBACK WITH THE R8070

When TLOOP is high, transmitter data on TPOS and TNEG is internally connected to the receiver inputs in place of RPOS and RNEG (Figure 2). When TLOOP is low, the transmitter and receiver signals are independent.

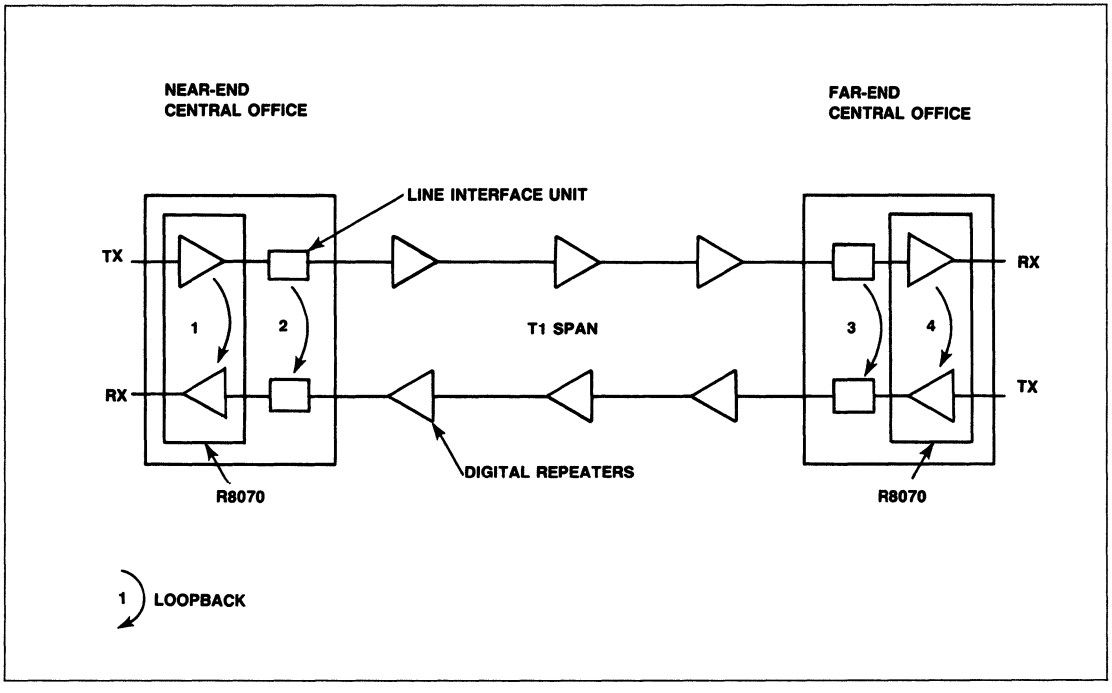

Figure 1. Typical T1 Span and Loopback Configurations

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During loopback, the external TPOS and TNEG pins carry a pattern of continuous 1s, according to Paragraph 6.6.2, Section A, Bell Publication 43801. This continuous 1s pattern includes the F-bits and is referred to as "unframed 1s." The external RPOS and RNEG signals are ignored by the R8070. TNRZ is unaffected by loopback and carries the normal transmit data.

While in loopback, the data received on RSER (serial) or R1–R8 (parallel) is identical (apart from throughput delay) to that data input to the transmitter on TSER (serial) or T1–T8 (parallel). The combined throughput delay of the looped data is one bit time less than the sum of the transmitter (8 bit times) and receiver (14 bit times) throughout delays. This is due to the internal loopback connection.

Clock Switching for Local Loopback

Under normal line operation, the R8070 receiver clock, RCLK, is synchronously recovered from the received data. During loopback, the receiver's clock must be synchronized to the looped transmitter data, which is clocked by TCLK. All R8070 outputs and inputs are clocked on the rising edge of the clock. So, to ensure that setup and hold times are met in loopback, the receiver clock must be offset from the transmitter clock. It is convenient to make RCLK equal to inverse TCLK during loopback. The circuit in Figure 3 shows the standard method of clock selection. When TLOOP is high, inverse TCLK is connected to the receiver clock input. When TLOOP is low, RCLK from the line interface becomes the receiver clock.

REMOTE LOOPBACK WITH THE R8070

Figure 4 shows the external connection for remote (far-end) loopback with the R8070. Data from the line is received as normal on RPOS and RNEG, having been conditioned by the line interface unit (LIU), which also extracts a synchronous clock, RCLK, for the receiver. Serial data is output from the receiver at RSER.

Under loopback conditions, RSER is routed to TSER for retransmission back to the near end. A pair of D-type flip-flops adds a 1-bit delay to this path so that when RSYNC is directly connected to TMSYNC and TFSYNC, the transmitter's framing will coincide with the receiver's. Two flip-flops are used to ensure the setup and hold times are met, both for the D-type and the TSER inputs. Notice that each input (D-type 1, D-type 2, and TSER) is clocked on the opposite edge from the preceding output. This would not be possible with only one flip-flop.

As for local loopback, consideration must be given to the clock sources. The receiver will always clock from the line data rate, the transmitter may have a separate clock or be timed from receive data as well. During remote loopback, the transmitter must be locked to the receiver data rate. Figure 5 shows a simple circuit for switching the source of TCLK. The signal EXLOOP controls the remote loopback function and could be manually applied at the far end or remotely controlled from the near end.

To meet the setup and hold time at the transmitter inputs, inverse RCLK is applied to TCLK.

For clarity, the R8070 is shown in Figure 4 as hardwired for remote loopback. This connection would, or course, normally be switchable using a gating arrangement similar to that of Figure 5.

REMOTE LOOPBACK WITH A PARALLEL DATA INTERFACE

A connection for remote loopback can also be made for a parallel data interface. RSYNC is connected to TMSYNC and TFSYNC as before, and R1–R8 is connected to T1–T8. No delay is required on the data lines. A clock switching circuit similar to Figure 5 should also be used.

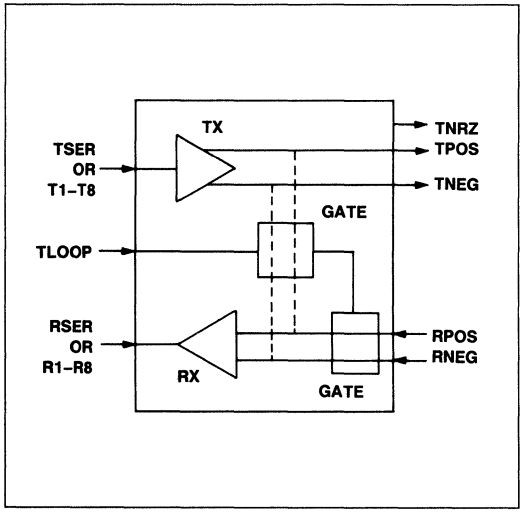

Figure 2. Internal Local Loopback in the R8070

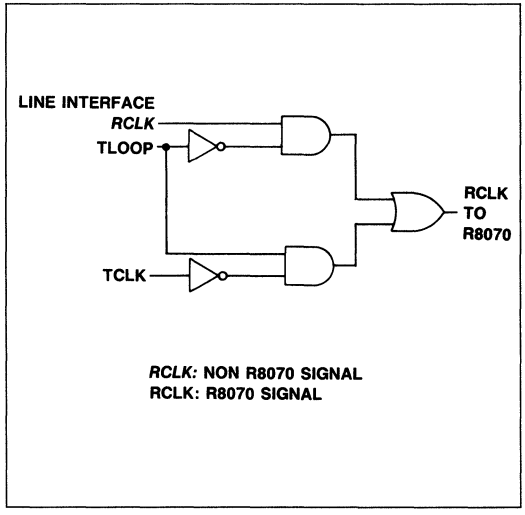

Figure 3. Clock Switching for Local Loopback

TIMING DIAGRAMS

Figure 6 shows the timing diagrams relating to the circuit of Figure 5. Data in RSER is delayed by one-half bit time at Q1, and again at Q2. The RSYNC pulse is clocked into TMSYNC and TFSYNC on the falling edge of RCLK. On the falling edge of this clocked RSYNC pulse, data is acquired at TSER, and this is the F-bit position. Note that although the F-bit is present at this time on RSER, the transmitter does not sample TSER for the F-bit, this is obtained from the TFSIG input. However, it is convenient to describe the synchronization based on the F-bit position because if this is correctly sampled, all the subsequent bits will be correctly sampled too.

Figure 7 shows the equivalent CEPT PCM 30 timing for serial data transfer during remote loopback. This is the same as for T1 except for the F-bit. The same 1-bit delay is required in the serial data line so that on the falling edge of the clocked RSYNC pulse bit 1 of time slot 0 is sampled at TSER.

Figure 8 and Figure 9 describe the remote loopback timing for a parallel interface for T1 and CEPT PCM 30, respectively. No delay is required in the data line because data is valid for longer than a single bit time. Data is sampled by the transmitter on T1–T8 on the rising edge of TCHCLK. Notice in the T1 waveforms that this edge occurs in different places for channel 1 and channel 2 due to the F-bit location. But data is still correctly sampled.

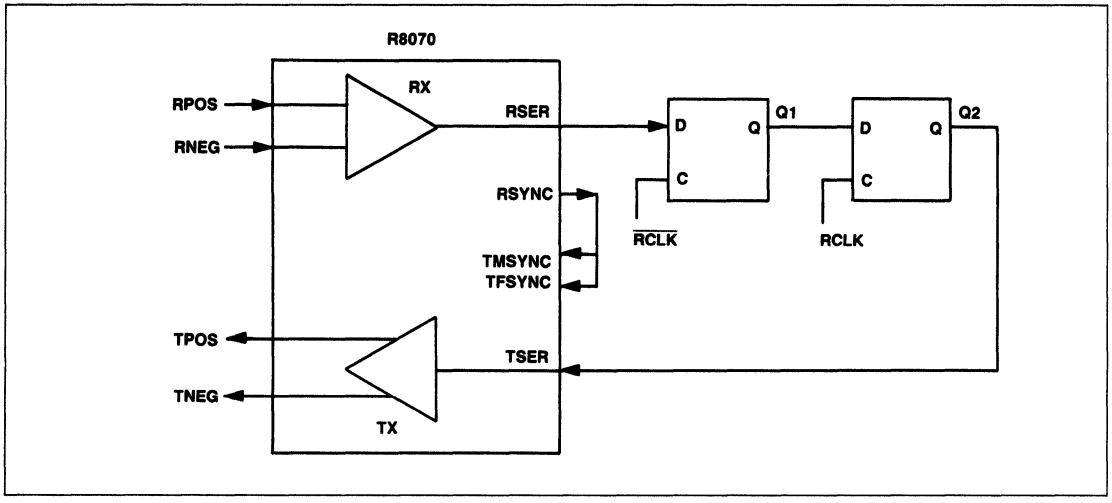

Figure 4. External Remote Loopback in the R8070

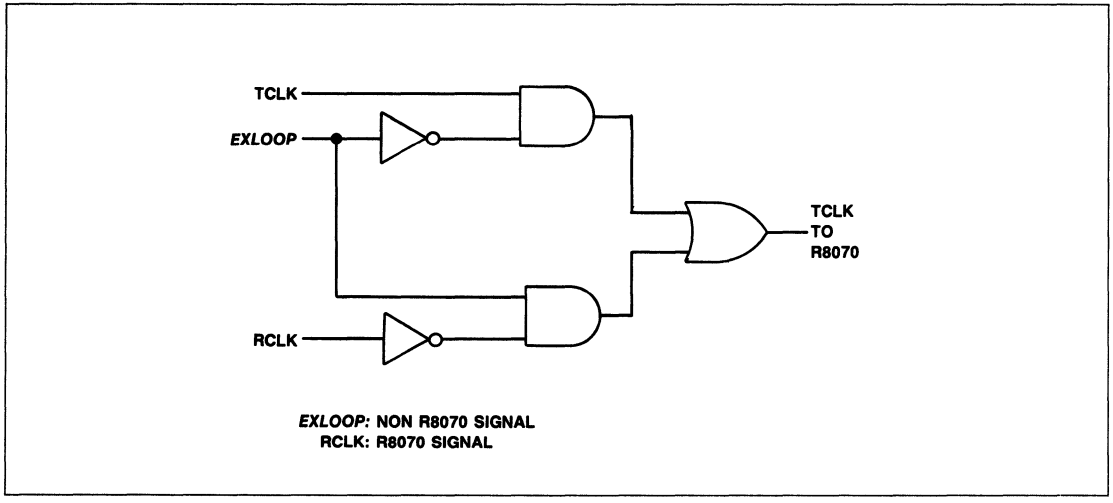

Figure 5. Clock Switching for Remote Loopback

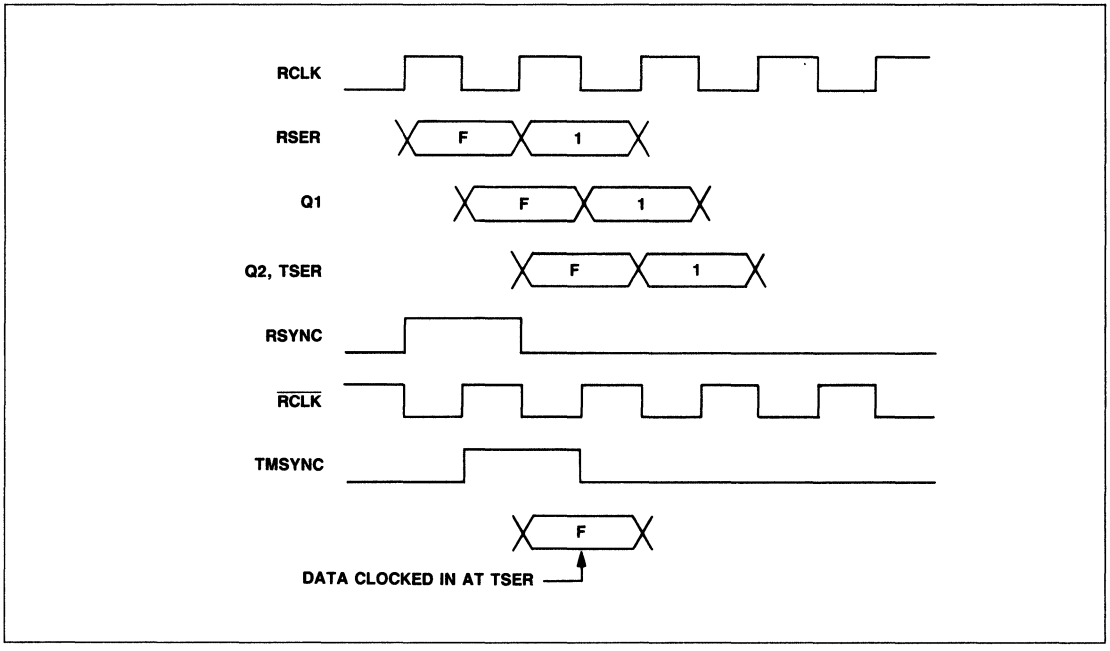

Figure 6. Remote Loopback — Serial Data Timing — T1

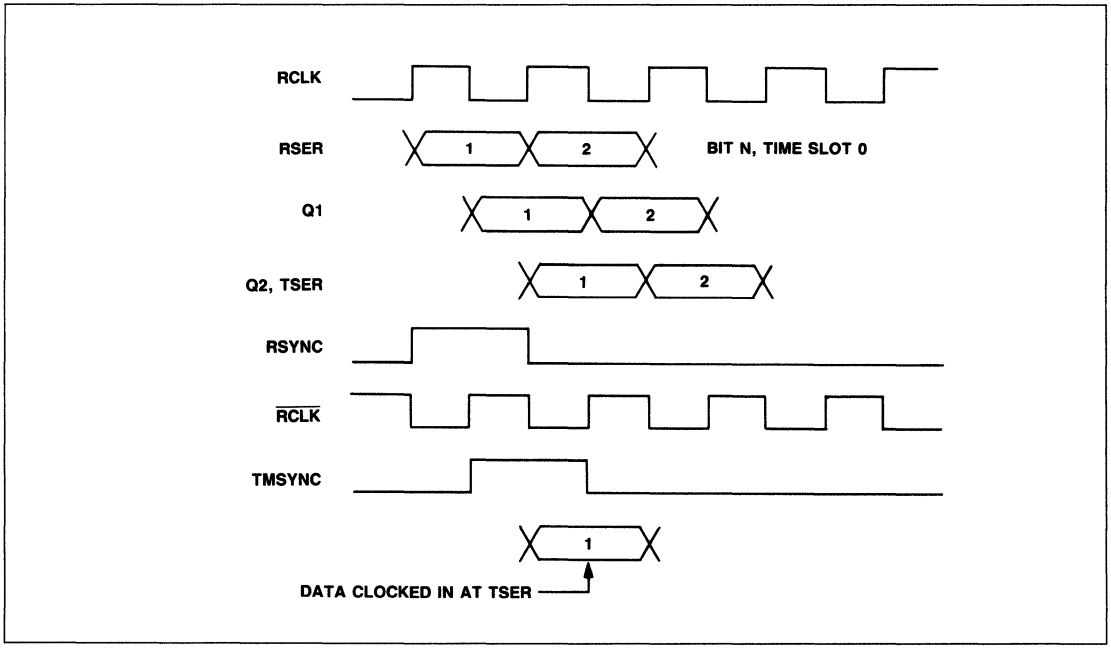

Figure 7. Remote Loopback — Serial Data Timing — CEPT

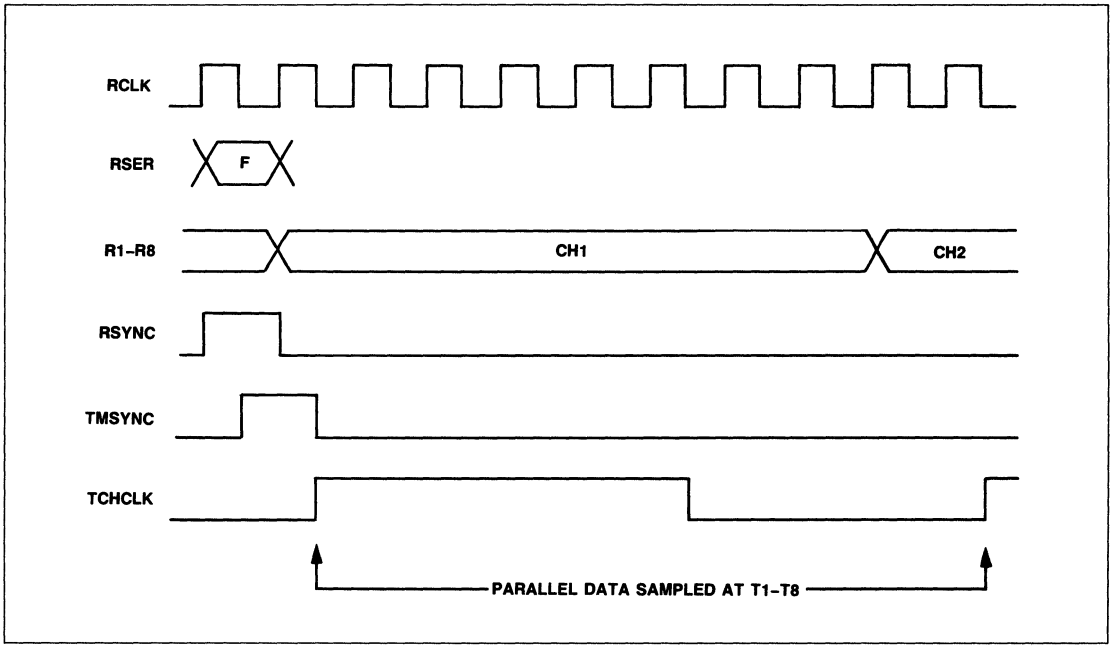

Figure 8. Remote Loopback — Parallel Data Timing — T1

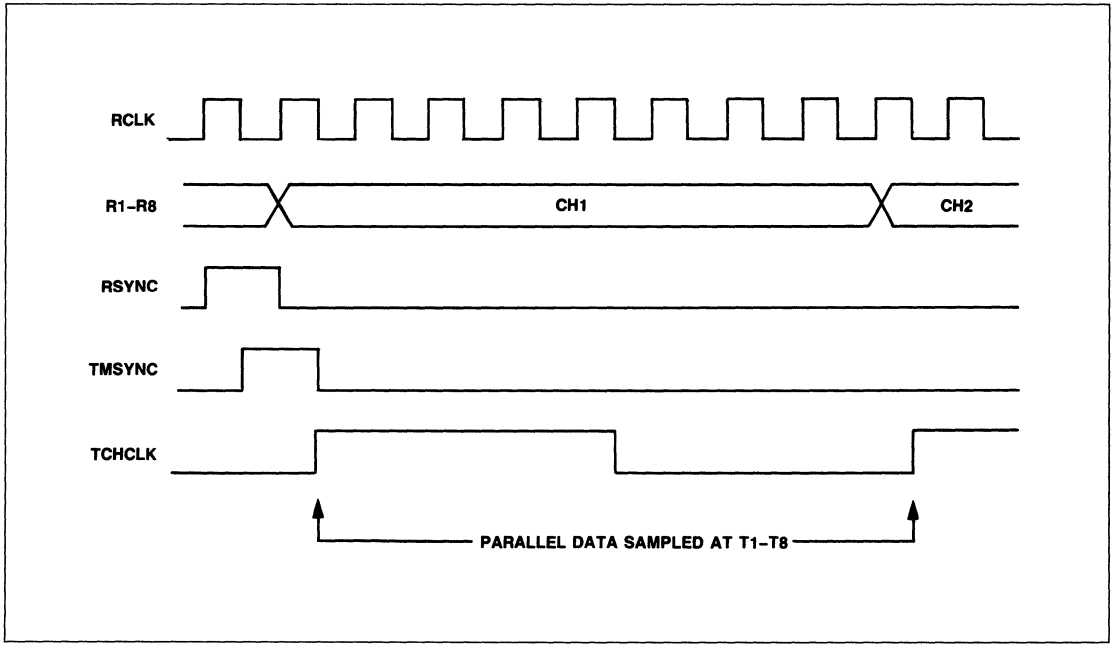

Figure 9. Remote Loopback — Parallel Data Timing — CEPT

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Reporting Error Conditions in the R8070

T1 D4, T1C

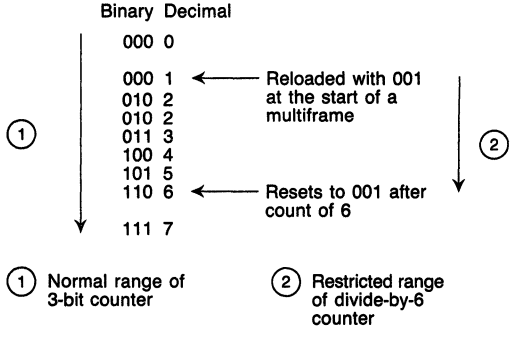
Fs (S-BIT) ERRORS

In the 193S and 197S modes, when the receiver is multiframe aligned, the S-bits are extracted from the incoming F-bit stream and compared with the standard multiframe-defining pattern (001110). Any error in the last received 5 bits of the pattern causes SERR to go high. SERR returns low when the last received 5 bits are correct.

Because of the 5-bit window used for S-bit errors, it is not possible to tell which individual S-bits are in error; except for the first bit, that caused SERR to go high, and the last bit, which allowed SERR to go low (5 S-bits later).

However, the circuit shown in Figure 1 provides an external check on the S-bits. The latest received S-bit, available on RSBIT, is compared with the correct pattern, produced by a divide-by-6 counter on the RSBCLK output. At the start of each multiframe, the counter is reloaded with 001 by RSYNC. This provides the required 001110 pattern from the most significant bit of the counter in synchronization with the multiframe.

Divide-by-6 Counter Sequence



S-Bit Comparator Timing

Figure 2 shows the timing associated with the S-bit comparator. The counter is preloaded with 001 by the RSYNC pulse at the start of the multiframe. The counter is incremented by each rising edge of RSBCLK, giving a sequence of 001110 from the most significant bit. This standard S-bit sequence is compared with the received S-bit on RSBIT by the exclusive OR gate. The comparator output is high for a frame period if the S-bit for that frame is in error.

Ft ERRORS

In modes 193S, 193N, 197S, and 197N, FERR high indicates that the current Ft bit at RSER failed to maintain its alternating pattern (010101).

If two or more Ft errors occur in any five consecutive Ft bits, then a frame alarm is declared, RRED goes high and the receiver attempts to reframe. The "out of frame alignment" condition disables FERR which reports no further errors until multiframe alignment is again achieved.

Example 1.
1 0 1 0 1 0 1 1 0 1 0

A single Ft error causes a single, bit-wide pulse on FERR.

Example 2.
1 0 1 0 1 0 1 1 1 0 1 0 1

Second Ft non-reversal treated as possible continuation of previous pattern. No error pulse on FERR.

First Ft error causes a single, bit-wide pulse on FERR.

Example 3.
1 0 1 0 1 0 1 1 1 1 1 0 1 0 1

Third non-reversal treated as an error. "2 out of 5" criterion is met, RRED goes high and FERR is inhibited.

Second non-reversal is considered a possible continuation of the previous pattern. Ther is no error pulse on FERR.

First non-reversal causes a single, bit-wide pulse on FERR.

Note: In Example 1, the alternating pattern after the error is the reverse of the pattern before the error.

A single error in the Ft pattern, although not sufficient to cause an "out of frame" condition, does have some impact on the framing algorithm. A single Ft error, also known as a slip, causes the framing algorithm to return to the P1 proving period. This does not affect the multiframe alignment.

T1, ESF

FRAMING PATTERN SEQUENCE (FPS) ERRORS

In the 193F mode, and when the receiver is multiframe aligned, the FPS is extracted from the incoming F-bits and compared with the correct pattern (001011). Any single error in the received sequence is indicated by FERR high coincident with the errored F-bit on RSER. The FERR pulse in one bit wide.

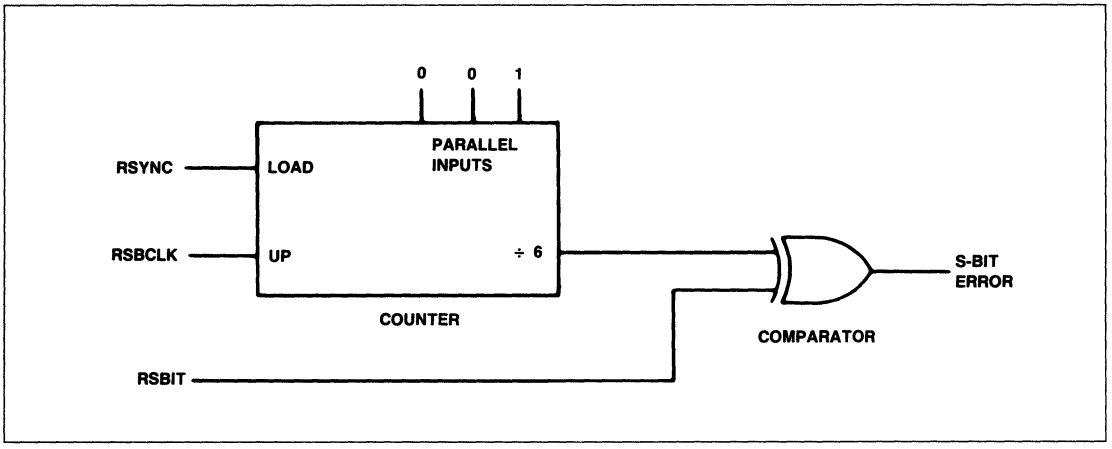


Figure 1. External S-Bit Comparator

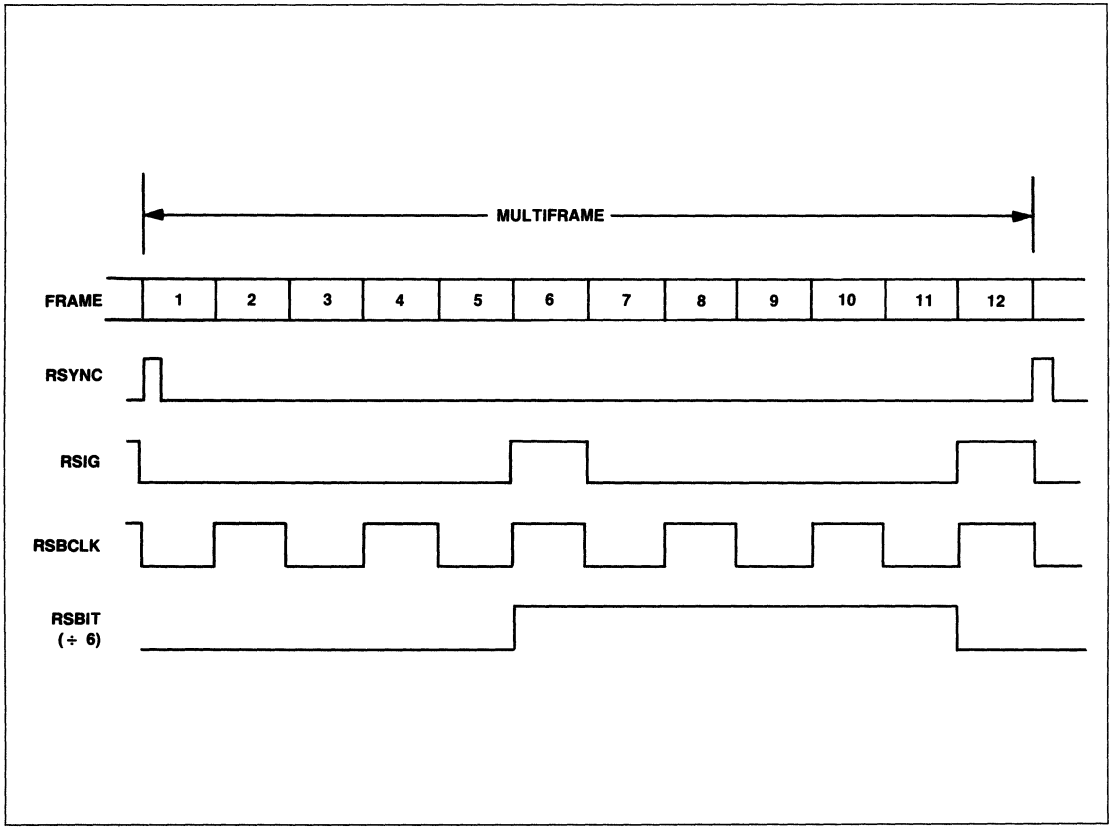


Figure 2. External S-Bit Comparator Timing

CYCLIC REDUNDANCY CHECKSUM (CRC) ERRORS

In the 193F mode, the 6-bit CRC checksum transmitted in the F-bit stream of multiframe N is compared with the locally computed checksum from the received data of multiframe N-1, i.e., the previous multiframe. For the purposes of computing CRC, the F-bits are set to 1. Any discrepancy between the computed and received checksum bits is indicated by CKERR high coincident with the errored CRC bit.

A typical application of ESF requires a signal for an errored multiframe rather than an errored CRC bit. The circuit of Figure 3 provides such a signal. The first occurrence of a CRC error (pulse high on CKERR) clocks a 1 into the D-type flip-flop and the Q output goes high. Q remains high until reset by RSYNC at the start of the next multiframe. CKERR is gated with inverse RCLK to avoid latching any glitches. A counter attached to the output of the flip-flop provides a count of errored multiframes.

Figure 4 shows the timing associated with this circuit. The dotted lines indicate that the Q output (MF Error) may be clocked high by any of the CKERR pulses. Q is reset by RSYNC.

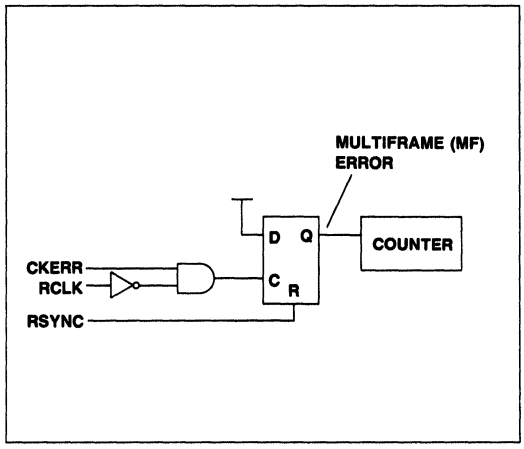


Figure 3. Counting Errored Multiframes from CRC Errors

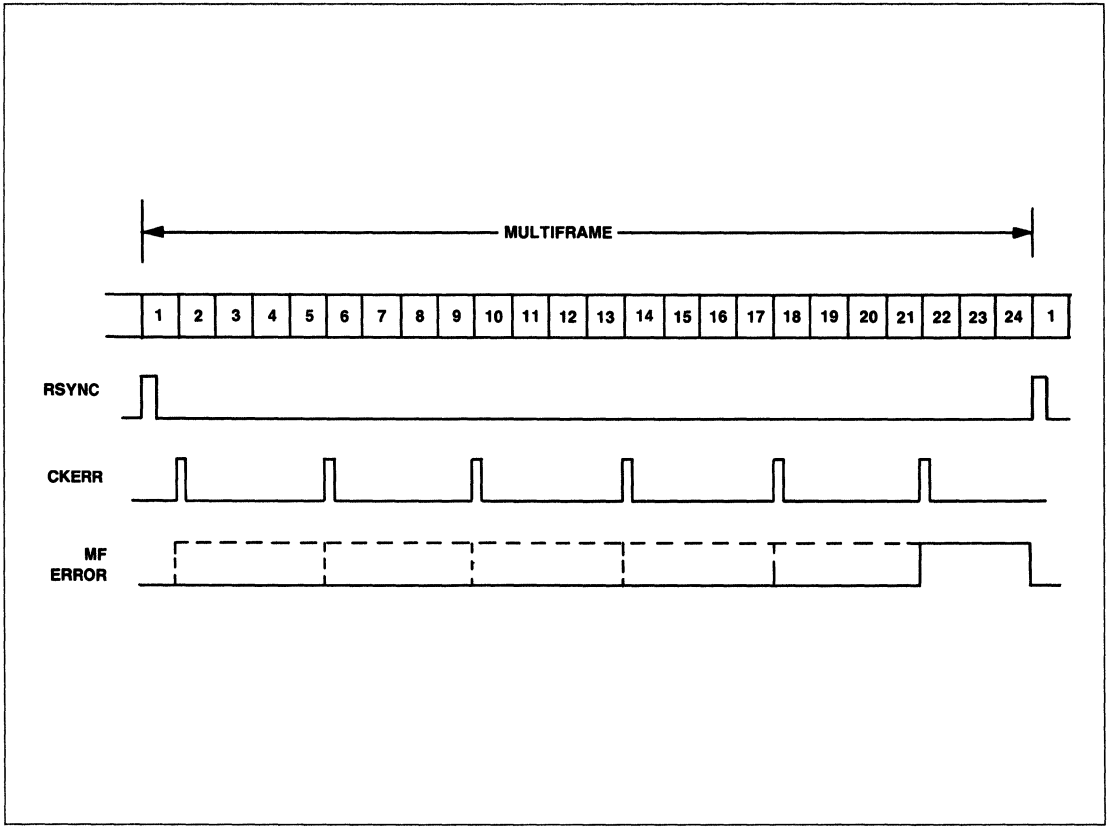


Figure 4. Errored Multiframe Timing

FPS, CRC ERRORS

In 193E mode, the functions of FPS error and CRC error are multiplexed onto a single output, ERR. See the above description of these functions. The circuit of Figure 5 may be used to separate these two signals. The separation is performed on the basis of RSIGBD. If RSIGBD is high, ERR indicates an FPS error. If RSIGBD is low, ERR indicates a CRC error.

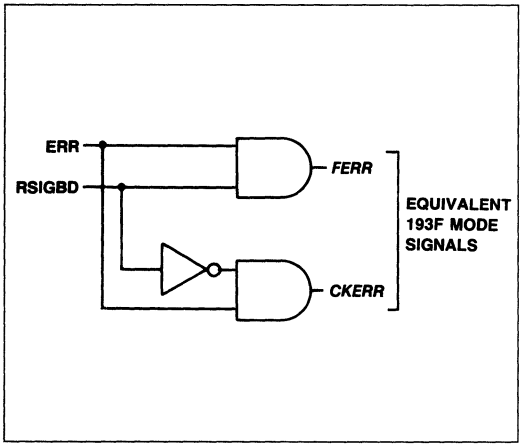


Figure 5. Demultiplexing the 193E Mode ERR Signal

CEPT PCM 30

FRAME ALIGNMENT SIGNAL (FAS) ERRORS (MODE 256N)

The 7-bit Frame Alignment Signal (0011011) is contained in time slot 0 of alternate frames. If any of these received bits is in error, FERR is high for bit 1 of that time slot 0.

FAS AND MULTIFRAME ALIGNMENT SIGNAL (MAS) ERRORS (MODE 256S)

The Multiframe Alignment Signal (0000) is contained in bits 1–4 of time slot 16 of frame 0. An error in this received signal is indicated by FMERR high for bit 1 of time slot 16.

In addition, the FAS error signal (see mode 256N) is multiplexed onto this output.

These two signals may be readily distinguished using the circuit of Figure 6. The separation is performed on the basis of RTS16. A pulse on FMERR during time slot 0 (RTS16 low) indicates a FAS error, while a pulse during time slot 16 (RST16 high) indicates a MAS error.

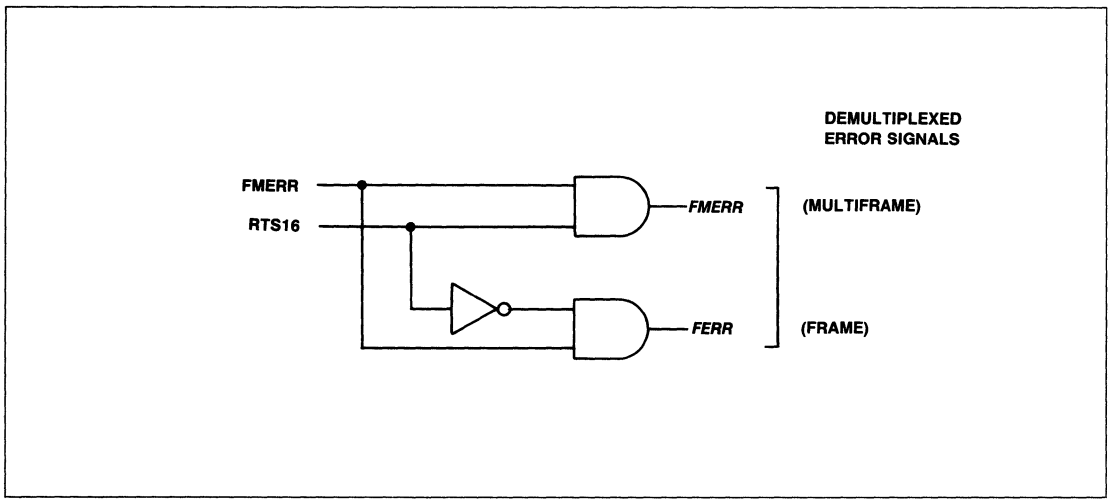


Figure 6. Demultiplexing the 256S Mode FMERR Signal

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Receiver Synchronization in the R8070

INTRODUCTION—THE NEED FOR SYNCHRONIZATION

Synchronization is one of the major functions of the PCM receiver. To enable the correct recovery at the receiver of each telephone channel and its associated signaling, the primary rate PCM signal is given a frame and multiframe structure. This structure is defined by the transmitter, which places framing bits or framing patterns at certain positions within the serial bit stream. The task of the receiver's synchronizer is to locate these patterns, produce a set of timing waveforms from them, and report any errors or deviations from the standard pattern.

Figure 1 represents the concept of alignment. The transmitter inserts the appropriate alignment patterns for the mode (e.g., for T1 an alternating 101010 pattern in the first bit of alternate frames) into the outgoing PCM signal, thereby defining the frame and multiframe structure to which its telephone channels and signaling conform. The transmitter also produces a timing signal, TMAX, at the multiframe rate.

At the receiver, these alignment patterns are recovered from the channel data and used to synchronize frame and multiframe counters, from which all other timing signals are derived. In particular, the receiver produces a timing signal, RSYNC, at the multiframe rate. When the transmitter and receiver are multiframe aligned, TMAX and RSYNC are synchronized and would appear to be coincident on an oscilloscope display. They are not quite coincident because of the transceiver's throughput delay.

These functions appear to be trivially simple, a false impression created, partly, by the simplicity of the standard "data sheet" representation of the bit stream, in which the known framing pattern is clearly recognizable. But the receiver sees only a random stream of 1s and 0s arriving at 1.5 Mbps to 2 Mbps, some of which may be in error or, worse still, may be imitations of the real framing pattern.

The synchronizer is required to frame quickly and reliably on the PCM signal, to be tolerant of bit errors, and to provide sufficient information to the system about framing status, errors and timing.

These notes describe:

1. The frame and multiframe structure of each PCM format.
2. The synchronization process—the framing algorithm.
3. Controlling the synchronizer.
4. Synchronization dependent outputs.
5. The reframe criterion for each R8070 mode.
6. Monitoring the synchronization state.

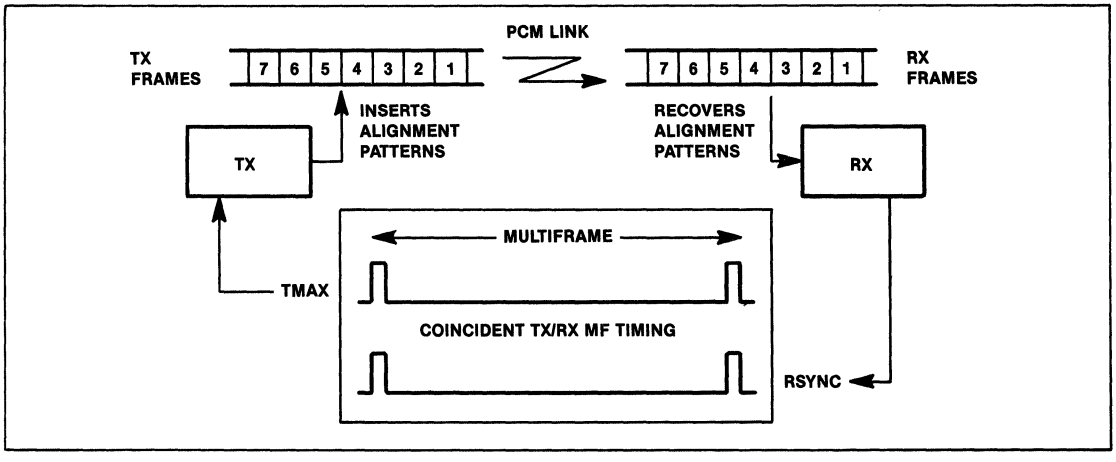

Figure 1. Multiframe Alignment of Receiver and Transmitter

THE FRAME AND MULTIFRAME STRUCTURE

T1 D4

Each of 24 telephone channels is sampled at 8 kHz, with a resolution of 8 bits. The 8-bit samples from each channel are transmitted serially, most significant bit (bit 1) first. The transmission of one sample from each channel produces a group of 192 bits (24 channels × 8 bits), called a **frame.**

In order to identify the frame boundaries, an extra bit, called a framing bit or F-bit, is appended to the start of the frame. This makes a total of 193 bits per frame. The framing bit is sometimes called the 193rd bit, but it always occurs at the start of the frame, not at the end.

The method of "robbed-bit" signaling (where the least significant bit of each channel is replaced by a signaling bit during every sixth frame) requires that signaling frames be identifiable. Since every sixth frame contains one of two signaling bits (A or B), a **multiframe** (or superframe) consisting of 12 frames is defined. The A-bits are contained in frame 6; the B-bits in frame 12.

The F-bit position carries two interleaved patterns; the Ft pattern (101010) and the Fs pattern (001110). These two patterns occupy alternate F-bit positions and define the frame and multiframe boundaries, respectively. See Table 1.

Table 1. F-bit Assignment—D4 Format

Frame Number	Bit Number	F-bit		Signaling Bits
		Fs	Ft	
1	0	—	1	
2	193	0	—	
3	386	—	0	
4	579	0	—	
5	772	—	1	
6	965	1	—	A-bits
7	1158	—	0	
8	1351	1	—	
9	1544	—	1	
10	1737	1	—	
11	1930	—	0	
12	2123	0	—	B-bits

T1 ESF

The Extended Superframe Format (ESF) has the same channel structure and frame structure as D4, but the superframe (or multiframe) is extended from 12 to 24 frames (Table 2). The F-bit position now carries three types of information:

1. Framing Pattern Sequence (FPS) which defines the frame **and** multiframe boundaries.
2. Facility Data Link (FDL) which allows data such as error rates, and alarms to be transmitted over the T1 link.
3. Cyclic Redundancy Check (CRC) which allows the link error rate to be monitored, and enhances the reliability of the receiver's framing algorithm.

Table 2. F-bit Assignment—Extended Superframe Format

ESF Frame Number	ESF Bit Number	F-bit Assignment			Signaling Bits
		FPS	FDL	CRC	
1	0	—	m	—	
2	193	—	—	CB1	
3	386	—	m	—	
4	579	0	—	—	
5	772	—	m	—	
6	965	—	—	CB2	A-bits
7	1158	—	m	—	
8	1351	0	—	—	
9	1544	—	m	—	
10	1737	—	—	CB3	
11	1930	—	m	—	
12	2123	1	—	—	B-bits
13	2316	—	m	—	
14	2509	—	—	CB4	
15	2702	—	m	—	
16	2895	0	—	—	
17	3088	—	m	—	
18	3281	—	—	CB5	C-bits
19	3474	—	m	—	
20	3667	1	—	—	
21	3860	—	m	—	
22	4053	—	—	CB6	
23	4246	—	m	—	
24	4439	1	—	—	D-bits

FPS — Framing Pattern Sequence (...001011...)
FDL — 4 Kbps Facility Data Link (message bits m)
CRC — CRC-6 Cyclic Redundancy Check (check bits CB1–CB6)

CEPT PCM 30

Each of 30 telephone channels is sampled at 8 kHz, with a resolution of 8 bits. The 8-bit samples from each channel are transmitted serially, most significant bit (bit 1) first. A **frame** is defined as 32, 8-bit time slots. Each time slot (TS) contains the 8-bit sample from one of the 30 telephone channels (Table 3). The two spare time slots (0 and 16) contain signaling, alarm, and alignment information.

In order to identify the frame boundaries, a Frame Alignment Signal (FAS), 0011011, is provided in time slot 0 of alternate frames. This allows the receiver to delineate the 8 bits of each channel, as well as determine which is channel 1.

The ABCD signaling method allocates 4 signaling bits per channel, transmitted in time slot 16 (TS16). Since there are 30 channels, each requiring 4 signaling bits, and there are 8 bits in each time slot 16, then 15 "time slot 16s" are required to transmit a set of signaling bits for each channel:

(30 channels × 4 signaling bits = 15 TS16s × 8 bits)

This implies a multiframe grouping of 15 frames which, together with an additional time slot 16 for alarm and alignment, leads to the standard multiframe length of 16 frames. The multiframe boundary is defined by a Multiframe Alignment Signal (MAS), 0000, situated in bits 1–4 of time slot 16, frame 0 (the first frame of the multiframe).

Table 3. CEPT PCM 30 Time Slot and Channel Numbering

Time Slot	Channel Number	Time Slot	Channel Number
0	FAS	16	MAS
1	1	17	16
2	2	18	17
3	3	19	18
4	4	20	19
5	5	21	20
6	6	22	21
7	7	23	22
8	8	24	23
9	9	25	24
10	10	26	25
11	11	27	26
12	12	28	27
13	13	29	28
14	14	30	29
15	15	31	30

Notes: FAS: Frame Alignment Signal, Alarm bits
MAS: Multiframe Alignment Signal, ABCD signaling, alarm

SYNCHRONIZER OPERATION

OVERVIEW

The incoming serial bit stream is first stored in a shift-register and then examined in a serial-parallel fashion to locate first, the framing bit or framing pattern, then the multiframe pattern. When fully multiframe aligned, the synchronizer produces a set of timing waveforms at the channel-, frame-, and multiframe-rate. These allow the extraction of the channel data, its associated signaling bits, and any transmitted alarms. At the same time, the synchronizer monitors the bit stream for errors in the received alignment signals. Single errors are reported in an appropriate format, and multiple errors which exceed a certain criterion cause the present alignment to be abandoned and the synchronization process to be repeated.

SYNCHRONIZER STATES—SUMMARY

The R8070's synchronizer (or framing algorithm) can be viewed as a state machine having eight major states (Figure 2). Each state is referenced by a name and a binary number (Table 4).

In principle, the synchronizer begins at the Wait state and proceeds, in sequence if there are no errors, through each state as it determines and then verifies first, frame alignment, then multiframe alignment; finally reaching the Sync state, where it is fully multiframe aligned. At this point, the framing pattern is continuously monitored for errors.

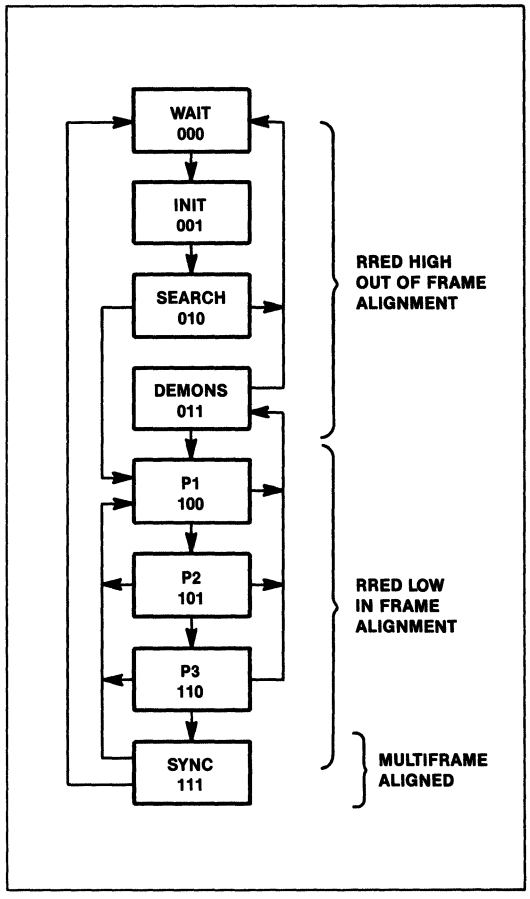

Figure 2. Synchronization States

Table 4. Synchronizer States

Dec	State	Binary MS3	Binary MS2	Binary MS1
0	Wait	0	0	0
1	Init	0	0	1
2	Search	0	1	0
3	Demons	0	1	1
4	P1	1	0	0
5	P2	1	0	1
6	P3	1	1	0
7	Sync	1	1	1

THE PROCESS OF SYNCHRONIZATION—STATE DESCRIPTIONS

0. Wait State

The search for frame alignment begins at the Wait state. There are four means by which the synchronizer might reach, or be held at, the Wait state:

1. Power up reset, PUP.
2. User request for reframe, RMRST.
3. User delay of reframe, RSRCH.
4. Frame errors, causing auto-reframe.

The first three of these are "holding" conditions. If any of them is active, the receiver remains in the Wait state. When none is active, the receiver proceeds to the second state, Init.

The last condition (frame errors) is not invoked by a user input, but is part of the receiver's inherent resynchronization strategy. In this case, the return to the Wait state is followed immediately by an entry into the Init state.

1. Init State

During the Initialization state, a bank of shift registers collects a sample of the incoming serial data—usually about 4 frames, but this is mode-dependent. No checks are made on the data at this stage and so the synchronizer proceeds directly to the Search state.

2. Search State

This is where the basic search for frame alignment takes place. In the T1 modes, this means locating the framing bit; in the CEPT PCM 30 modes, the framing pattern.

A parallel-serial search technique is used for a shorter reframe time. A group of bits, appropriate to the mode, is examined as a candidate for the framing bit or pattern. A failure to follow the prescribed pattern rules out that bit group as a candidate. All possible framing candidates are evaluated repeatedly until all but one is eliminated. If more than one candidate persists, one of them is chosen and further tests on it are made to determine its validity. Random data can mimic the framing pattern for a short period; continuous test tones can imitate it indefinitely. Ultimately, if only one framing candidate remains, it is declared to represent the true frame alignment, and the synchronizer moves on to the next state.

3. Demons State

The Demons state is only entered in modes 193N and 193F. It is a special part of the algorithm which discards false framing candidates (demons). This is particularly valuable in the 193N mode where the Fs pattern is not examined as no multiframe is assumed to exist.

In all other modes, the Demon state is by-passed and the P1 state is entered.

4. P1 State

In the P1 state, the multiframe boundary is determined by examining the multiframe alignment signal as appropriate to the mode. This alignment is verified for a period of two multiframes. The previously established frame alignment is also rechecked.

5. P2 State

In the P2 state, a further two multiframes are checked for correct frame- and multiframe-alignment. In modes 193S and 197S, both the Fs and Ft pattern are monitored for errors, thus providing additional security against imitative data patterns. The error criterion for framing is gradually relaxed as the synchronizer proceeds through the proving states.

6. P3 State

A final check on alignment is made over a further period of two multiframes. Even in the non-signaling (non-multiframed) modes (193N, 197N, and 256N) the proving periods still apply, but only the Ft bits (T1) or the FAS (CEPT) is checked.

In the ESF modes, 193E and 193F, the CRC is also checked during the P3 period. If CRC shows any errors then the present alignment is abandoned and the synchronizer returns to the Wait state.

During the proving periods for modes 193S and 197S (and for the Sync state below), a single Ft error, called a slip, does not cause a complete reframe from the Wait state (two errors are required to cause this). Instead, the synchronizer returns only as far as the P1 state and performs the multiframe alignment process again.

7. Sync State

Finally, the Sync state is achieved, indicating full multiframe alignment. The receiver continues to monitor the alignment patterns and reports any errors.

CONTROLLING SYNCHRONIZATION—THE SYNCHRONIZER INPUTS

The synchronizer is almost entirely controlled internally, based upon the selected mode of operation and the incoming data. The algorithm seeks to maintain full multiframe alignment until forced to abandon it when the criterion for loss of frame alignment, as defined in the relevant CCITT standards, is met. When this occurs, an immediate reframe is automatically implemented.

However, the user does have some external control with the following inputs:

1. RSRCH, receive search control
2. RMRST, receive master restart
3. PUP, power-up reset
4. D1D and D2, synchronization lock

1. RSRCH

When RSRCH is low (this signal is active LOW), the synchronizer is prevented from continuing to the Init state from the Wait state. Note that RSRCH does **not force** a return to the Wait state (compare to RMRST below).

This input may be used to hold off reframe, for example to allow two receivers to be synchronized.

Another function of RSRCH is to slip a bit within the multiframe. If at any time RRED = RSRCH = 0, i.e., RSRCH is active during frame alignment, then bit 5 of the first time slot of the next multiframe is skipped.

2. RMRST

When RMRST is high the synchronizer is forced to return to the Wait state. If RMRST is then held high, the receiver will remain in the Wait state.

This signal may be used to force the receiver to reframe if an error has been detected. Some errors, such as Fs or CRC, are reported by the R8070 but do not cause a reframe. This is left for the user to implement and simply involves feeding back the SERR or CKERR error signal to RMRST.

The signal may also be used to ensure that the receiver reframes after switching from one source of PCM signal to another, such as would occur with protection switching—switching to a spare PCM link if the original fails. When this happens in a T1 D4 link, the new signal may happen to have the same Ft bit alignment but not the same multiframe alignment. The receiver would not automatically reframe because the Ft bits are correct.

3. PUP

When PUP is held low for at least 16 clock cycles, the receiver (and transmitter) are completely reset. This is equivalent to applying a RMRST to the receiver and forces the synchronizer to the Wait state. When PUP is released, the synchronizer proceeds to the Init state and attempts to frame align on the incoming signal in the usual way.

PUP is normally only applied once, at power up, or to restart the transceiver after a system failure. It should also be applied after switching modes unless the user can guarantee that mode switching will not disturb the receiver's timing.

4. D1D and D2

D1D and D2 are normally used in T1 modes with a serial interface. They are used to select the sequence of the binary channel numbers provided at RSQ1-RSQ5 and TSQ1-TSQ5 to match the D1D or D2 channel banks. These inputs are not used for the same purpose in CEPT PCM 30 modes, as the channels are always sequentially numbered: They should normally be set to 0, 0.

D1D and D2 can also be used to control the synchronizer. If D1D and D2 are **both** high, the "synchronization lock" mode is entered. The synchronizer aligns in the normal way but, having achieved multiframe alignment, it remains in the Sync state, regardless of any framing errors.

This feature may be useful if the signal will temporarily be removed or contain errors, and subsequently will recover without affecting the frame alignment.

RMRST will override the application of D1D and D2, forcing the receiver to reframe. If D1D and D2 remain high, the synchronizer will again lock in the Sync state.

SYNCHRONIZATION DEPENDENT OUTPUTS

Almost all outputs from the receiver are dependent on the synchronizer for their timing. Each major function of the receiver: data and signaling recovery, alarm indication, and error reporting, requires knowledge of the location of the channel, frame or multiframe boundaries.

Only two outputs are always available and always valid: RSER and RVLL. These are related directly to the serial bit stream and are not dependent on the channel position.

Tables 5 and 6 describe the effect of the synchronization state on each receiver output for the T1 and PCM 30 modes, respectively.

Table 5. Synchronization State Dependent Signals — T1 Modes

Synchronization State								Signal Name	Signal Type
W	I	S	D	P1	P2	P3	Sy		
H	1	2	2	3	3	3	*	RSYNC	Clocks
L	L	L	L	L	L	L	*	RMFA	
L	L	L	L	*	*	*	*	RCHSYNC	
L	*	L	L	*	*	*	*	RCHCLK	
L	*	L	L	*	*	*	*	RWIHBT	
!	!	!	!	*	*	*	*	RSQ1-RSQ5	
L	L	L	L	L	L	*	*	ERR[1]	Errors
L	L	L	L	L	L	L	*	FERR	
L	L	L	L	L	L	*	*	CKERR	
!	!	!	!	!	!	!	*	SERR	
H	H	H	H	L	L	L	L	RRED	Alarms
L	L	L	L	L	L	L	*	RYEL	
!	!	!	!	!	!	!	*	RSBIT	S-bit, signaling
L	L	L	L	L	L	L	*	RSBCLK	
L	L	L	L	L	L	L	*	RSIG	
!	!	!	!	!	!	!	*	RSIGBD	
!	!	!	!	!	!	!	*	RSIGCD	
!	!	!	!	!	!	!	*	RSIGSQ	
H	H	H	H	H	H	H	*	RLINK	Link bits
L	L	L	L	L	*	*	*	RLCLK	
L	L	L	L	L	L	L	*	R1 - R8	Parallel data
L	H	L	H	L	H	L	H	MS1	Synchronizer state
L	L	H	H	L	L	H	H	MS2	
L	L	L	L	H	H	H	H	RRED/	

Key:

Sync state: W = Wait, I = Init, S = Search, D = Demons
P1, P2, P3 = Proving periods, Sy = Sync

Condition: L = Gated Low
H = Gated High
! = Invalid, indeterminate
* = Valid

RSYNC: 1. Single pulse on the last bit.
2. Single pulse indicates candidate.
3. Single pulse at end of each state, coincident with the F-bit output on RSER.

Notes: 1. ERR is a multiplexed version of FERR and CKERR; its validity is the composite of theirs.

Table 6. Synchronization State Dependent Signals — CEPT Modes

Synchronization State								Signal Name	Signal Type
W	I	S	D	P1	P2	P3	Sy		
H	1	2	—	3	3	3	*	RSYNC[1]	Clocks
L	L	L	L	L	L	L	*	RMFA	
L	L	L	L	*	*	*	*	RCHSYNC	
L	*	L	L	*	*	*	*	RCHCLK	
L	*	L	L	*	*	*	*	RWIHBT	
!	!	!	!	*	*	*	*	RSQ1-RSQ5	
L	L	L	L	L	L	L	*	FERR	Errors
!	!	!	!	*	*	*	*	FMERR[2]	
H	H	H	H	L	L	L	L	RRED	Alarms
L	L	L	L	L	L	L	*	RYEL	
H	H	H	H	H	H	H	L	RMRED	
L	L	L	L	L	L	L	*	RMYEL	
!	!	!	!	*	*	*	*	RIBITS	I, N, X bits
!	!	!	!	*	*	*	*	RNBITS	
!	!	!	!	!	*	*	*	RXBITS	
!	!	!	!	!	!	!	*	RTS16	ABCD signaling
!	!	!	!	!	*	*	*	RABCD	
H	H	H	H	H	H	H	*	RLINK	Link bits
L	L	L	L	L	*	*	*	RLCLK	
L	L	L	L	*	*	*	*	RLINK1	

Key:

Sync state: W = Wait, I = Init, S = Search, D = Demons
P1, P2, P3 = Proving periods, Sy = Sync

Condition: L = Gated Low
H = Gated High
! = Invalid, indeterminate
* = Valid

RSYNC:
1. Single pulse on the first bit.
2. Single pulse indicates candidate.
3. Single pulse at start of each state, coincident with the first bit of multiframe output on RSER.

Notes:
1. FMERR reports frame and multiframe alignment errors. The frame error portion of these is valid only in the Sync state, as FERR.
2. No Demons state in CEPT PCM 30.

REFRAME CRITERION—WHAT THE STANDARDS SAY

The R8070 satisfies the reframe criterion stipulated in Bell Pub 43801 for T1, and in CCITT G.732 for CEPT PCM 30.

Bell Pub 43801

2.2 Out-of Frame Detection

2.2.1 A reframe procedure must start when the fraction of the framing bits in error is in the range 2 out of 5 to 2 out of 4.

CCITT G.732

3. Loss and Recovery of Frame Alignment

Frame alignment will be assumed to have been lost when three or four consecutive frame alignment signals have been received with an error. Frame alignment will be assumed to have been recovered when the following sequence is detected:

— for the first time, the presence of the correct frame alignment signal;

— the absence of the frame alignment signal in the following frame detected by verifying that bit 2 in channel time-slot 0 is a 1;

— for the second time, the presence of the correct frame alignment signal in the next frame.

Note—To avoid the possibility of a state in which no frame alignment can be achieved due to the presence of an imitative frame alignment signal the following procedure may be used:

When a valid frame alignment signal is detected in frame *n*, a check should be made to ensure that a frame alignment signal does not exist in frame $n + 1$, and also that a frame alignment signal exists in frame $n + 2$. Failure to meet one or both of these requirements should cause a new search to be initiated in frame $n + 2$.

REFRAME CRITERION IN THE R8070

The reframe criterion implemented in the R8070 is described below. When the criterion is met, the synchronizer is forced to the Wait state to repeat the framing process.

T1 Modes

All modes: "2 out of 5" errors in the framing bit (Ft for T1 D4, FPS for T1 ESF).

CEPT PCM 30 Modes

256N mode: "4 out of 5" errors in the composite framing pattern (the 7-bit FAS in TS0 of alternate frames **plus** bit 2 of TS0 of frames not containing the FAS).

256S mode: as for 256N but if the Multiframe Alignment Signal is in error then the reframe criterion is reduced to "3 out of 5" errors in the composite framing pattern.

Multiframe Error Criterion — CEPT PCM 30

In addition to the reframe criterion, CEPT PCM 30 also has a multiframe criterion. If this is met, the synchronizer returns to the P1 state to repeat the multiframe alignment process. The "Loss of Multiframe Alignment" bit (bit 6 of time slot 16, frame 0) is automatically set to 1 in the transmitter's output. The frame alignment is not affected.

Multiframe alignment criterion:

256S mode: Two consecutive errors in the Multiframe Alignment Signal.

MONITORING THE SYNCHRONIZER STATE

Figure 2 and Table 4 show the 8 states of the synchronizer. Each state has a three-bit binary number; MS1, MS2, and MS3, where MS3 is the most significant bit. The Red Alarm output, RRED, is the inverse of MS3.

In Modes 193S and 193N, the Master State numbers; MS1, MS2, and MS3 ($\overline{\text{RRED}}$) are readily available on outputs OF, OG, and RRED. In other modes, monitoring the synchronizer involves decoding its various state-dependent signals. In this case, it may not be possible to determine the exact state; all that is normally required is whether the receiver is fully frame- and multiframe-aligned.

The following notes suggest how this basic framing information can be obtained in each mode.

T1 MODES

193S and 193N Modes

All three Master State numbers are available and can be read directly from the R8070 or decoded to indicate a specific state. For example, the circuit of Figure 3 decodes the inverse of the Sync state to give an alarm for "loss of multiframe alignment".

197S and 197N Modes

In Figure 4, RSBCLK activity is used to indicate the Sync state and hence produce a "loss of multiframe alignment" alarm.

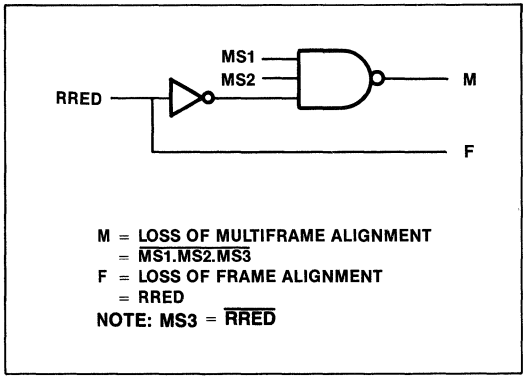

Figure 3. Decoding MS1, MS2, MS3

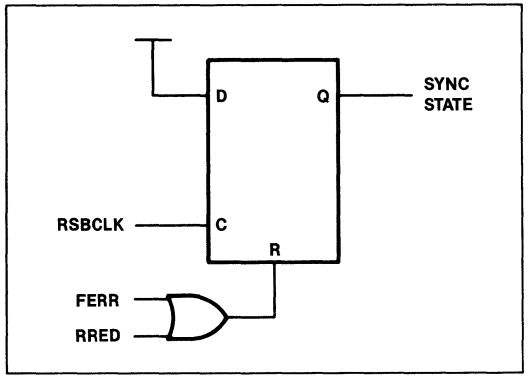

Figure 4. Sync State from RSBCLK

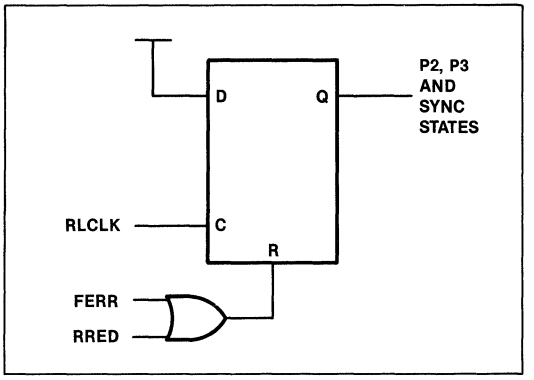

Figure 5. P2, P3, and Sync States

Additionally, in Figure 5 the RLCLK activity in P2, P3 and Sync states produces more information on the intervening states between frame alignment and multiframe alignment.

193E Mode

If RSIG replaces RSBCLK in Figure 4, the circuit produces a similar indication of the Sync state. RSBCLK is not available in 193E mode. The circuit of Figure 5 may also be used.

193F Mode

If RMFA replaces RSBCLK in Figure 4, the Sync state is indicated. RSBCLK is not available in 193F. The circuit of Figure 5 may also be used.

CEPT PCM 30 MODES

256N Mode

There is no convenient signal in 256N mode which is only active in the Sync state. Since there is no multiframe structure in 256N there may be no need to know when the Sync state has been reached, although this is useful for testing.

The circuit of Figure 6 uses the behavior of RSYNC during framing to determine the start of the P1, P2, P3, and Sync states. RSYNC produces a pulse at the start of each of these states. These pulses are counted after the falling edge of RRED.

256S Mode

This mode already has an indicator of multiframe alignment, RMRED, the multiframe equivalent of RRED. However, some of the circuits described above could be used to provide further detail of the synchronization state.

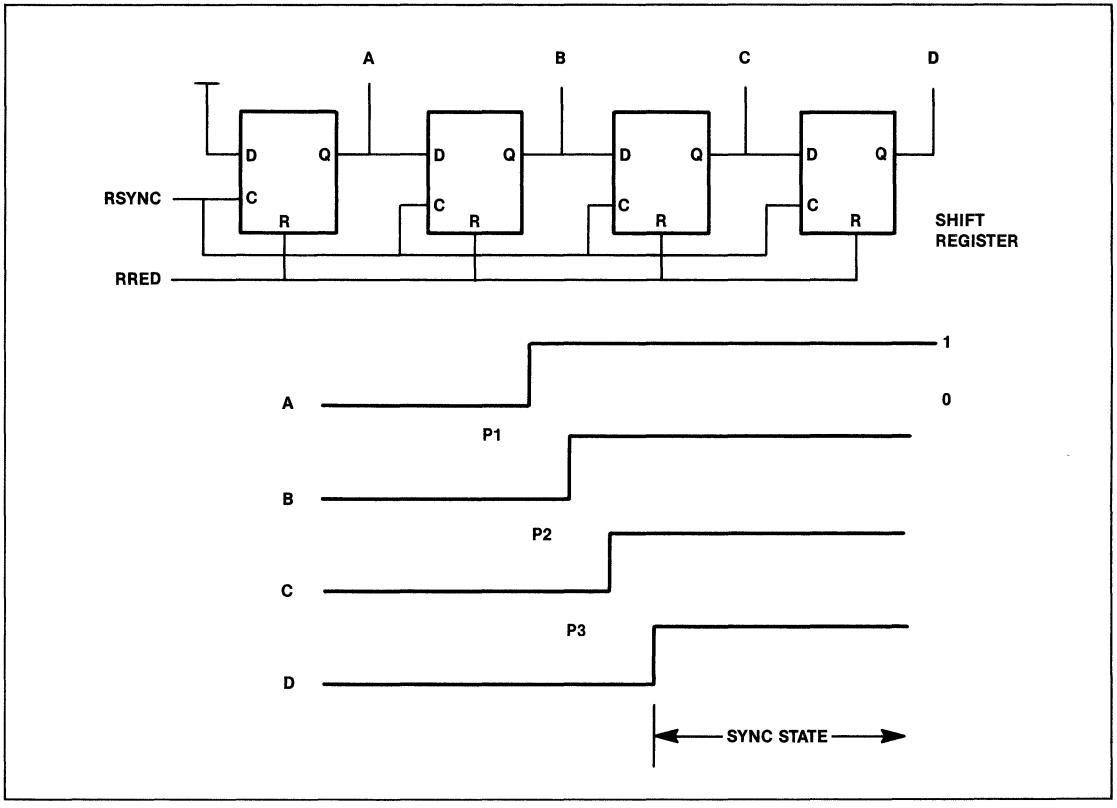

Figure 6. Counting RSYNC Pulses to Find Sync State

Rockwell

Independent Channel Control for the R8070

SYSTEM OVERVIEW

The operation of a PCM link requires that functions such as idle code and digital milliwatt test signals are selectable on a channel-by-channel basis. On the R8070 this is achieved by switching the relevant control signal on and off at the appropriate channel boundaries. This application note examines various methods for deriving such control signals.

CHANNEL CONTROL IN THE R8070

Figure 1 illustrates the principle of channel control in the R8070 T1/CEPT PCM Transceiver. The figure takes TIDLE, the control for transmission of idle code, as an example; RIDLE and RMW work in a similar fashion. The T1 format of 24 channels per frame is shown, but CEPT PCM 30 operation is identical except for the channel numbers.

The schematic at the top of Figure 1 represents the concept of idle code control. Data on either TSER or T1-T8 normally passes through the transmitter (with an 8-bit throughput delay) and, after formatting for the appropriate PCM standard, emerges at TNRZ and at the AMI pair, TPOS and TNEG. When TIDLE is low, the input data is transmitted normally. When TIDLE is high, the data is replaced with idle code.

Channel-by-channel control of idle code insertion is affected by switching the TIDLE signal on and off at the boundaries of the required channels. TIDLE is sampled at the same time as bit 8 of a given channel at TSER for implementation in the next channel. This is shown in the top two traces of Figure 1. For example, if TIDLE is high for channels 3, 7, 8, and 19, then TNRZ replaces the normal data for these channels with idle code.

The detailed timing requirements for TIDLE are shown in the lower traces of Figure 1. An expansion of the time scale at the boundary of channels 2 and 3 shows the point of sampling of TIDLE. TCHCLK may be used to gate the control signal for TIDLE to ensure its stability at sampling.

DERIVING THE CHANNEL CONTROL SIGNAL

The method used to derive the channel control signal depends on the form in which the information is initially represented. This form may range from the hardware extreme of one line (or wire) per channel, where the logic level indicates idle code required, to the software extreme of coded messages indicating idle channel numbers. Between these extremes lies a "bit per channel" representation in memory of channels requiring idle code. It is this form which is assumed for this application note. If the signal is already in a hardware form then it can easily be converted to an appropriate control signal. If the information is in high level software form then it can be translated to the bit-per-channel form.

CHECKING THE TIMING CONSTRAINTS

Could the channel control signal be derived entirely by microprocessor means? This may depend on the type of microprocessor and the other tasks it must simultaneously perform. As a quick check, look at the time scale of a PCM signal:

T1

Clock rate	1.544 MHz
Clock period	648 ns
Channel period	5.2 μs
Frame period	25 μs

CEPT PCM 30

Clock rate	2.048 MHz
Clock period	488 ns
Channel period	3.9 μs
Frame period	125 μs

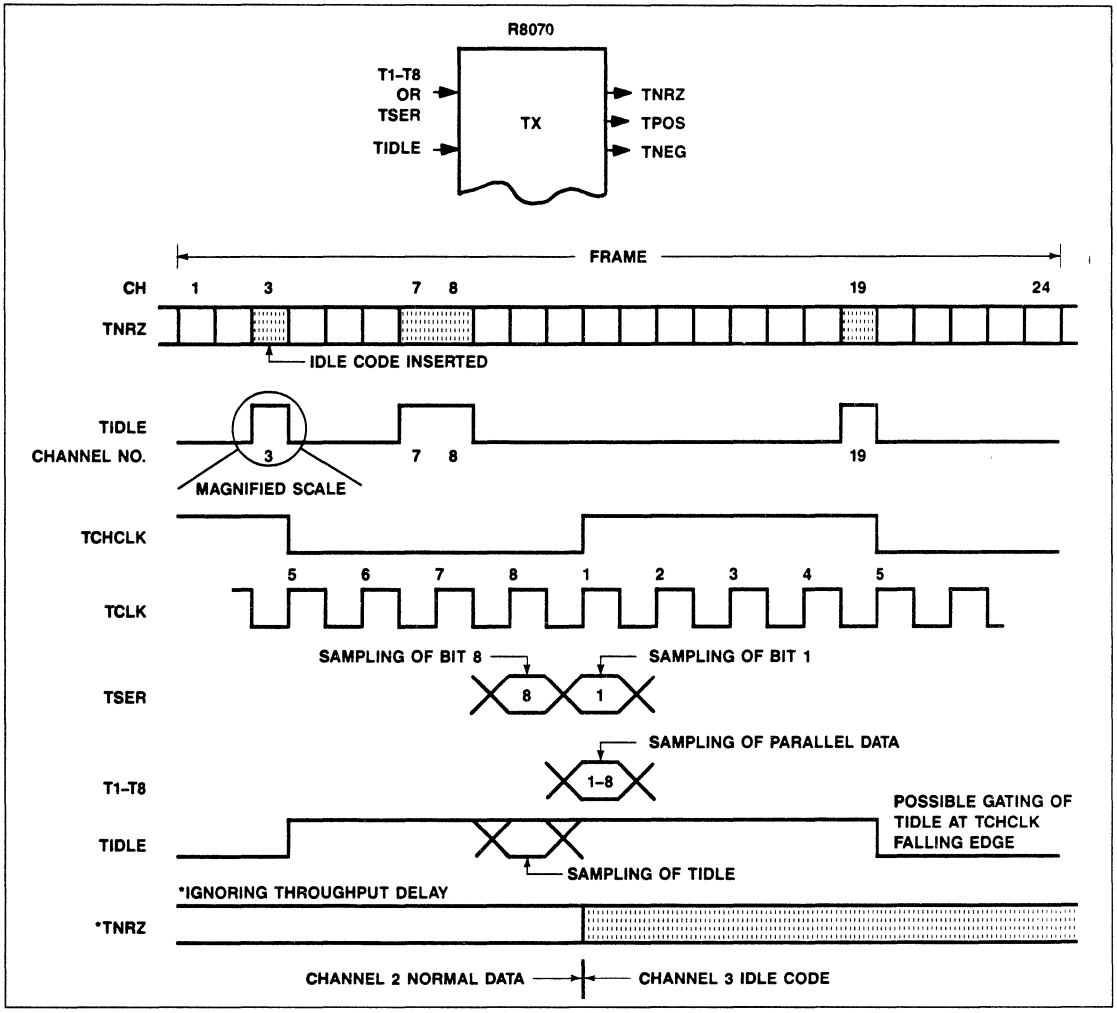

Figure1. Channel-by-Channel Control - TIDLE

A microcontroller could be used to set the appropriate logic levels for TIDLE, RIDLE, and RMW, but it would need to update these values once every 5.2 μs for T1 or every 3.9 μs for CEPT PCM 30. These times are too fast for normal programmed output, even for a fast microcontroller. Special output techniques such as direct memory access (DMA) could be used.

The approach assumed here is that a microprocessor system is used but it does not produce the control signals directly itself. Instead, a suitable hardware interface between the microcontroller and the R8070 provides a correctly timed control signal from the binary numbers downloaded from memory.

8

THE INTERFACE AND ITS REQUIREMENTS

Figure 2 outlines one form that the interface might take. The essential elements are: storage, parallel-to-serial conversion, a microprocessor-compatible bus, timing, and control. These elements are embodied within the shift registers and their associated control logic. Additional buffers might be necessary to avoid timing conflicts when the registers are loaded. The timing logic takes clocks from the microprocessor and from the R8070 and generates the necessary timing and control pulses for the buffers, shift registers and microprocessor. Various versions of a shift register-based interface are examined .

THE SHIFT REGISTER APPROACHES

Various different configurations of shift registers and buffers are possible, each offering its own advantages. The different methods are shown in Figures 3 through 7.

SHIFT REGISTER METHOD 1

Figure 3 shows one method by which shift registers can be used to produce channel-by-channel control signals for, for example, RIDLE. Three 8-bit shift registers (e.g., 74LS166) are required for a 24 channel system (four would be used for a 32 channel system, but see also method 4). The registers are connected end-to-end to form a 24-bit shift register. Each register may be loaded in parallel from the 8-bit microprocessor bus. Under control of the timing circuits, the 24 bits shift in the direction of the arrows towards the final serial output which becomes the control signal. The serial output is recirculated back to the serial input to avoid reloading the registers at the end of every frame. This reduces the load on the microprocessor. Additional control signals are required to handshake with the microprocessor to facilitate the data transfer.

The timing for this circuit is shown in Figure 4 for the T1 format. RCHSYNC, which occurs at the end of every frame, controls the loading of the shift registers. The signal is first gated with RWIHBT so as not to mask a rising edge of RCHCLK, which shifts the registers. RIDLE is sampled as bit 7 emerges from RSER and is implemented in the next channel. At the start of the next channel, on the rising edge of RCHCLK, the shift register is shifted in preparation for the next sampling. Thus the shift register, when parallel loaded, contains a 1 in each bit position for every channel in which idle code, for example, is required. The control bit for channel 1 is loaded into the far right position of register 3 so that it emerges first from the register. On loading, the bit for channel 1 is available at the serial output. The first shift brings the control bit for channel 2 to the serial output.

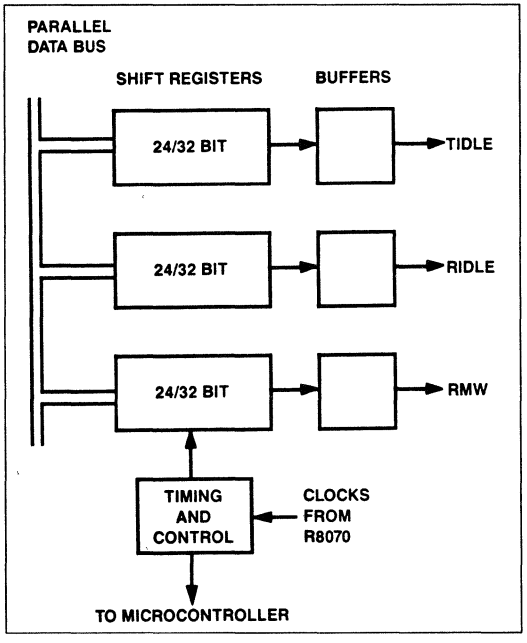

Figure 2. Channel Controller Shift Register (Outline)

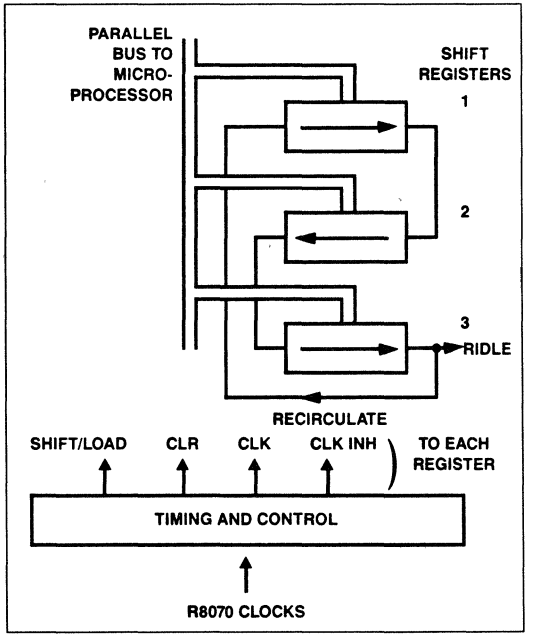

Figure 3. Shift Register Method 1

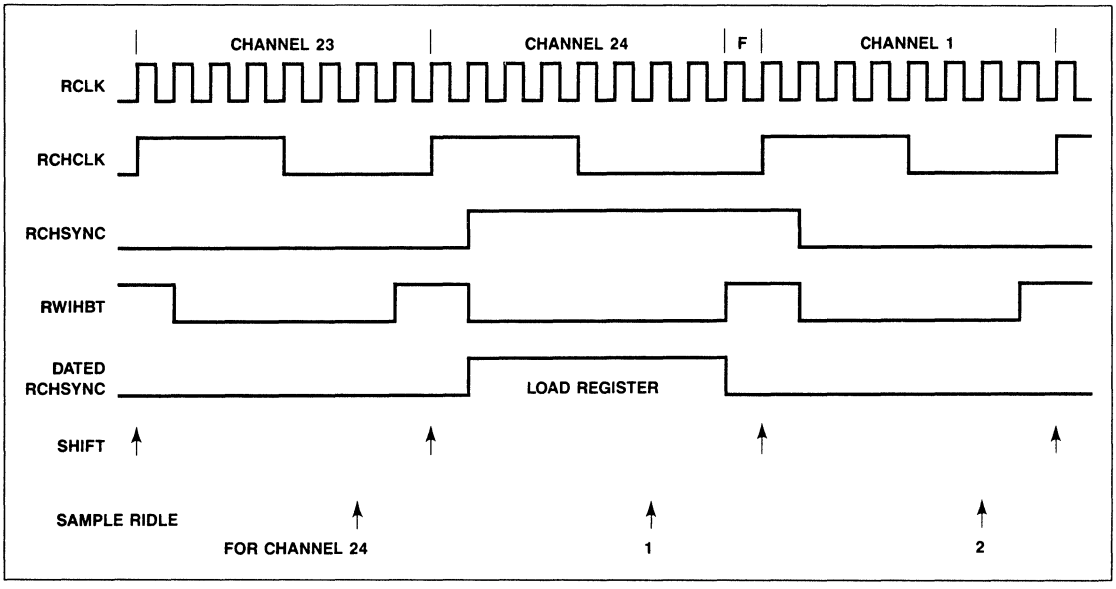

Figure 4. Timing Shift Register Method 1

It would be possible to incorporate a control signal that overrides the register load if the current pattern of idle channels is to be maintained. In which case the 24-bit pattern would continue to recirculate. In addition, it is necessary to set up the handshake signals for the microprocessor. RCHSYNC might be used to interrupt the processor at the end of every frame so that the registers could be loaded. One problem with this scheme is that the processor has very little time to make three loads to the registers (and three more to each of the other control signals).

There are several solutions to the problem of the processor data interface and these are addressed in the other methods discussed below. For this method, though, the problem of data transfer might be alleviated by arranging that only one of the registers is loaded each frame. A coded number system (address) for each register determines which register is to be loaded.

SHIFT REGISTER METHOD 2

An alternative to the first method of shift register implementation is described in Figure 5. The same three 8-bit registers are used but, instead of being loaded directly from the bus, are loaded from buffers which are loaded by the microprocessor. These buffers allow the binary data to be downloaded at any convenient time, although it might be prudent to avoid the moment when the

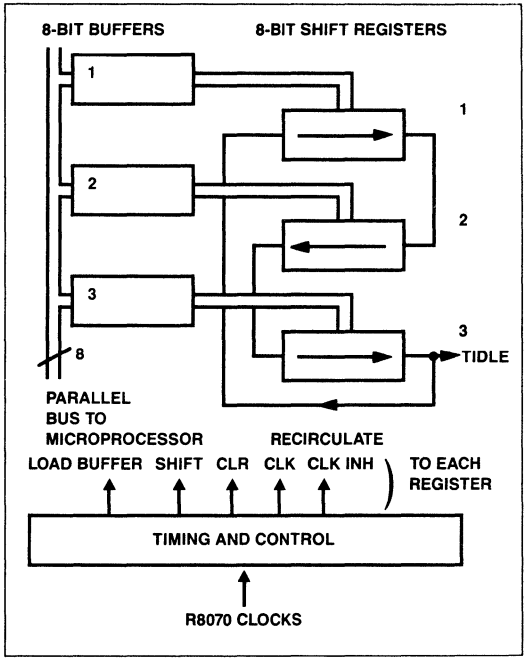

Figure 5. Shift Register Method 2

buffer to register transfer takes place. The 24-bit data could be recirculated as before, or the buffers could be retransferred to the registers at the end of each frame. The timing and control requirements for this version are similar to the previous one.

SHIFT REGISTER METHOD 3

Variation of the above method where only one 8-bit buffer and register is used is shown in Figure 6. This reduces the hardware requirement but increases the burden of data loading on the microprocessor. Recirculation is not possible and it is necessary to make a one-byte data transfer every 8 channels (41 μs for T1, 31 μs for CEPT PCM 30).

SHIFT REGISTER METHOD 4

Figure 7 shows a variation of the first method with 16-bit registers (e.g., 74LS674) instead of 8-bit registers. This reduces the hardware and interconnect requirements but is really only suitable for the CEPT PCM 30 standard because the spare capacity with only 24 channels to be controlled would complicate recirculation. The circuit is illustrated with a 16-bit microprocessor bus which simplifies the parallel loading of the registers. Buffers could be added if required as in method 2. In the CEPT PCM 30 system, idle code cannot be transmitted in time slots 0 or 16, so the control bits related to these time slots would normally be set to 0.

ALTERNATIVE APPROACH

Figure 8 outlines an alternative approach to the implementation of the interface. In this case a single, 32 x 4 random access memory (RAM) contains the binary information on the channels required to contain idle code and digital milliwatt. The RAM locations are sequentially accessed to produce the required logic control signals for TIDLE, etc. The approach is initially attractive because the

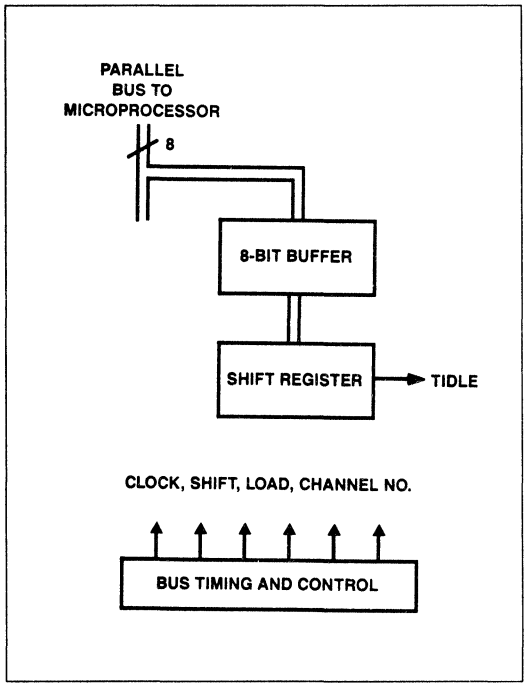

Figure 6. Shift Register Method 3

RAM is a normal microprocessor peripheral and is commonly available in a single package, as opposed to the multiple shift register solution. Indeed, the R8040 triport memory could be used. However, the generation of timing signals to control the RAM is more complex and, more importantly, it would be more difficult to deal with the independent timing requirements of transmit and receive timing (TCLK and RCLK are not always synchronized). This approach is not pursued in this application note.

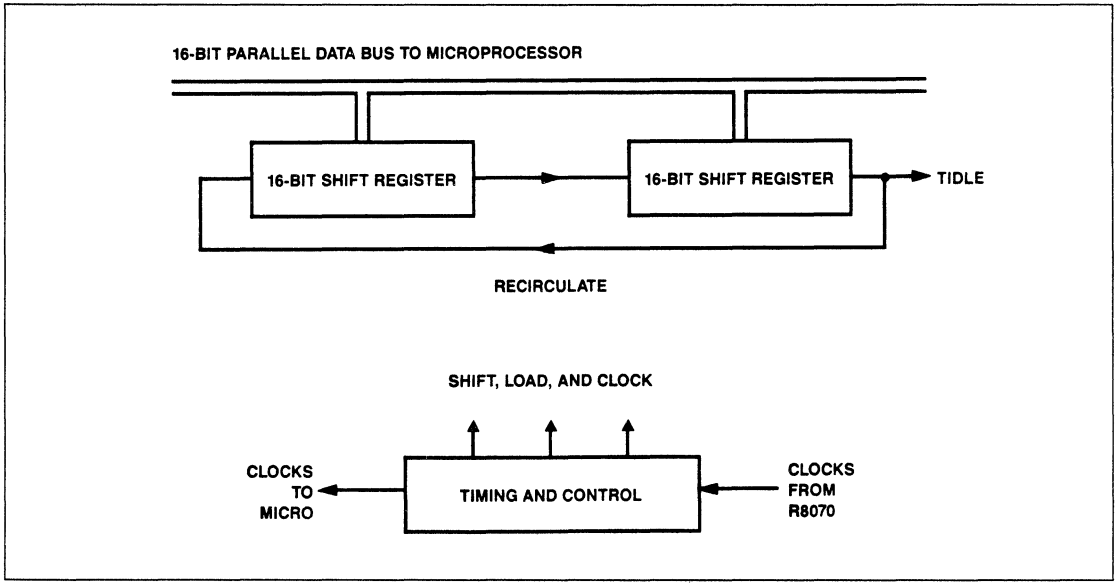

Figure 7. Shift Register Method 4

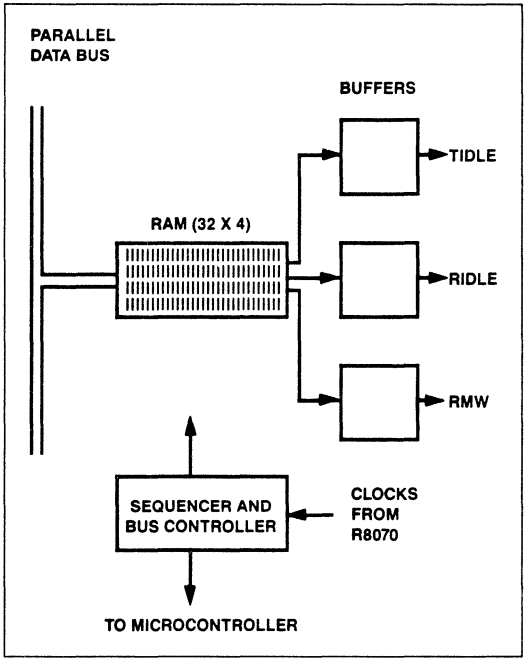

Figure 8. Outline of Channel Controller - RAM

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Idle Code Generation

INTRODUCTION

A fully occupied T1 link contains 24 channels, CEPT PCM 30 has 30 channels. But a PCM link may not be fully occupied, i.e., may have less than 24 or 30 active channels. The unoccupied channels usually contain idle code. Idle code is generally the PCM code word that corresponds to zero or near zero volts as an analog signal.

The R8070 implements idle code insertion both at the transmitter (to be sent over the PCM link) and at the receiver (to be inserted in place of the received channel data).

This note describes how other idle codes – or test patterns – may be inserted into the received or transmitted data channels.

IDLE CODES

The idle code for T1 modes is 01111111. The idle code for CEPT PCM 30 modes is 01010101. The actual PCM codes (after allowing for inversion of all bits in the T1 system, or of even bits in CEPT PCM 30) are 10000000 and 00000000, respectively, which correspond to zero volts or near zero volts analog signal.

INTERNAL GENERATION OF IDLE CODE BY THE R8070

TRANSMITTER - TIDLE

When TIDLE is high, the next channel data to be transmitted is replaced with idle code. TIDLE is sampled at bit 8 of each channel for implementation in the next channel. If TIDLE is modulated (turned on and off) at the appropriate channel boundaries, then channel-by-channel control of idle code insertion is obtained. Idle code appears on all transmitter outputs; TNRZ, TPOS, and TNEG. Idle code does not replace signaling bits in T1 modes, or time slot 0 (framing) and time slot 16 (signaling) in CEPT PCM 30 modes.

Figure 1 illustrates the insertion of idle code at the transmitter. The first two traces represent the insertion of idle code on channels 3, 7, 8, and 19. To achieve this, TIDLE is taken high just prior to the sampling of these channels at the transmitter input, T1-T8.

The exact timing requirements of TIDLE are shown in the lower traces, on an expanded scale, for the case of channel 3. The rising edge of TCHCLK indicates the sampling of data on T1-T8. At this time, bit 1 would be sampled from TSER if a serial data interface were selected (although TCHCLK is not available in serial mode).

Conventionally, cycles of TCLK are numbered as per the currently sampled data bit on TSER. TIDLE is sampled at bit 8. Sampling is shown in the figure by a transition of the signal before and after the sampling instant. Typically, TIDLE might be gated by TCHCLK so as to be stable when sampled. TIDLE is shown transitioning at the falling edge of TCHCLK. Note that TNRZ is shown without the effect of transmitter throughput delay (8 cycles of TCLK). The idle code would normally emerge 8 bit times (1 channel time) after being requested.

RECEIVER - RIDLE

When RIDLE is high, the next channel data to be presented at the receiver output is replaced with idle code. RIDLE is sampled on the rising edge of RCLK at the emergence of bit 7 on RSER. Idle code is inserted in the next channel. If RIDLE is modulated (turned on and off) at the appropriate channel boundaries, then channel-by-channel control of idle code insertion is obtained. Idle code appears on RSER and R1-R8 but not on R8 during a signaling bit. RIDLE is only operative when the receiver is in "Sync" because knowledge of the channel boundaries is required.

Figure 2 illustrates idle code insertion at the receiver. The first two traces show at the frame level how modulation of RIDLE allows insertion of idle code into selected channels.

The lower traces show the timing requirements of RIDLE at the channel 2/3 boundary.

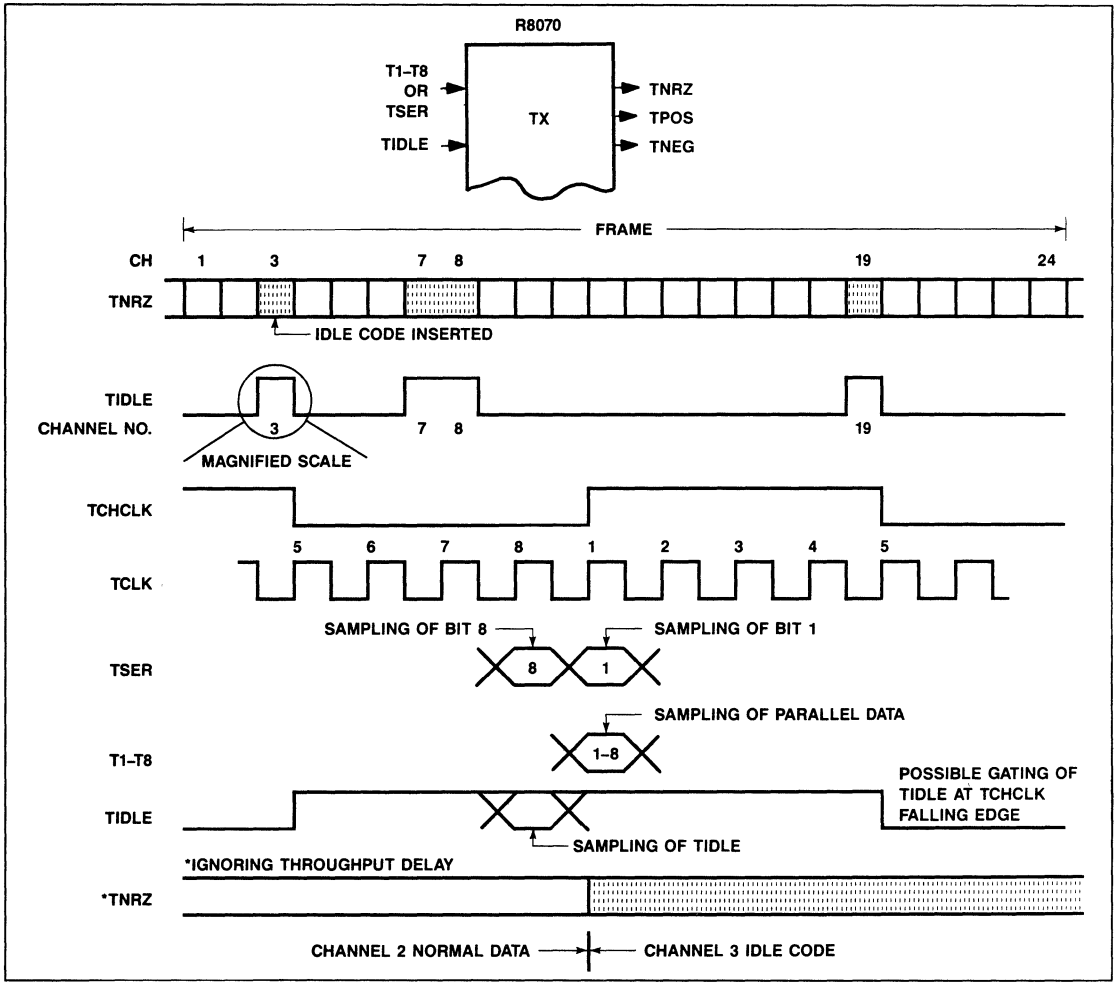

Figure 1. Generation of Idle Code - Transmitter

EXTERNAL GENERATION OF IDLE CODE

TRANSMITTER

If an idle code other than the standard provided by the R8070 is required then this may be applied externally with appropriate timing in the same way as normal channel data. Figures 3 and 4 illustrate how this might be done for a parallel or serial data interface, respectively.

In Figure 3 the external idle code is multiplexed with the normal channel data. A control signal, XTIDLE, selects between normal and idle data. XTIDLE could transition at the falling edge of TCHCLK (as might the channel data itself) to ensure stability during sampling of T1-T8 at the rising edge of TCHCLK.

In Figure 4 the external idle code is first serialized using a shift register before being multiplexed with the normal serial channel data under the control of ZTIDLE. ZTIDLE should be aligned to the channel boundaries for correct switching of the multiplexer. The shift register is clocked by the falling edge of TCLK to avoid shifting data during the sampling of TSER.

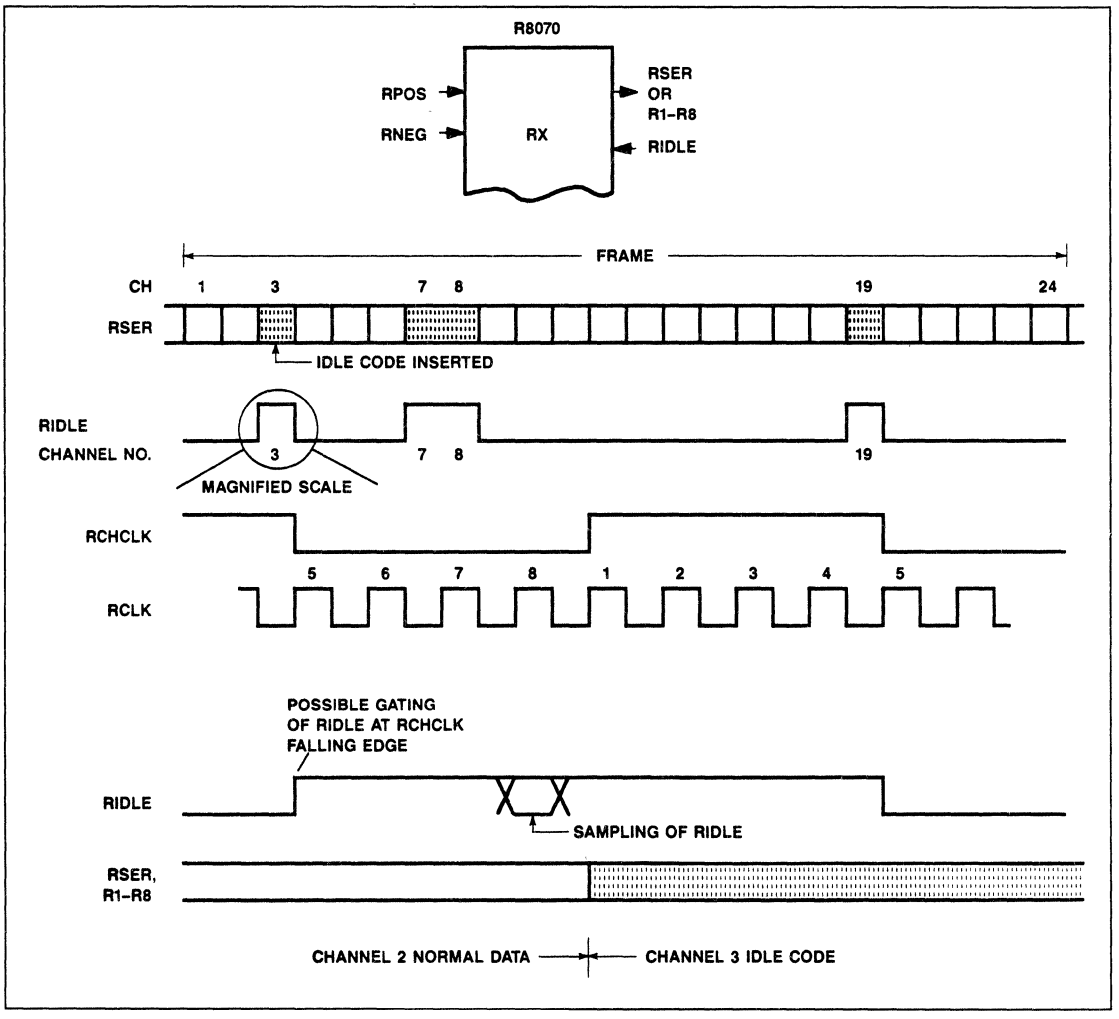

Figure 2. Generation of Idle Code - Receiver

RECEIVER

An alternative idle code may be substituted at the receiver output using a multiplexer. This may be done for either the serial or parallel data interface as shown in Figure 5. Both XRIDLE and ZRIDLE should transition at the rising edge of RCHCLK.

MODULATION OF RIDLE AND TIDLE

The modulated signals for RIDLE and TIDLE may be produced by gating the control signal with an appropriate clock. (See Application Note, "Independent Channel Control" Order No. 331.)

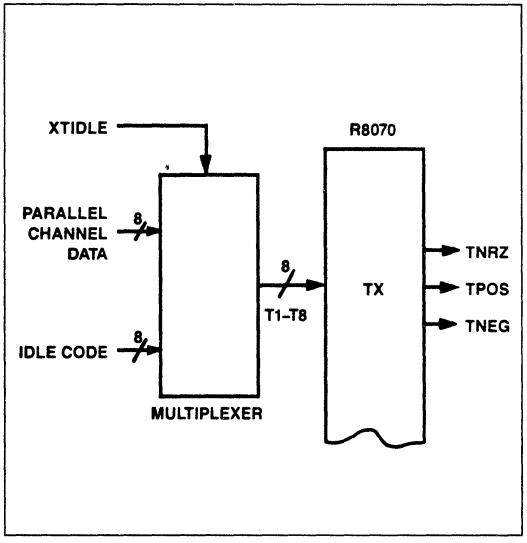

Figure 3. External Idle Code - Parallel

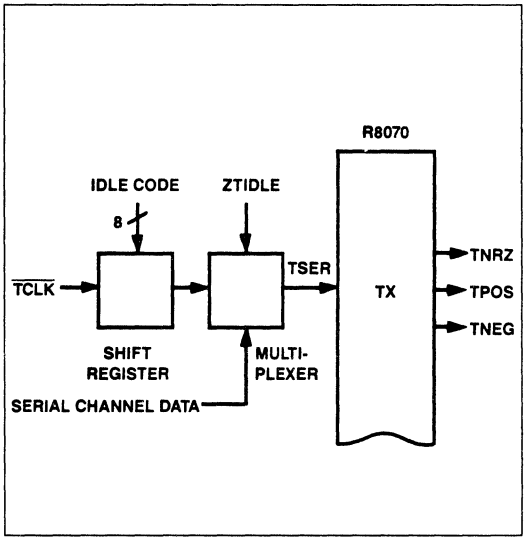

Figure 4. External Idle Code - Serial

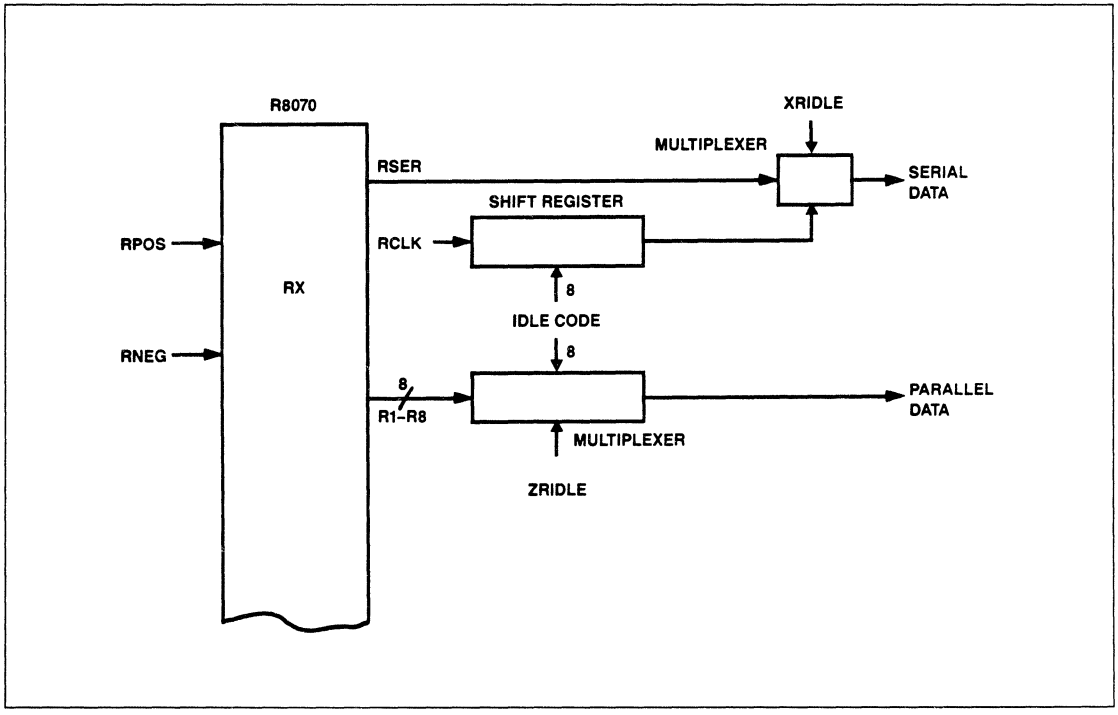

Figure 5. External Idle Code at the Receiver

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Alarm Handling with the R8070

SYSTEM OVERVIEW

Figure 1 shows a typical PCM link between central offices (local exchanges). The central offices (COs) may be up to 100 miles apart and the link may include test monitors or central office repeaters along the route. Digital repeaters spaced at 1-mile intervals regenerate the digital pulses. Under normal operating conditions, 24 time-division multiplexed, PCM encoded channels, each carrying a voice or data signal, are transmitted in each direction (30 channels for CEPT PCM 30).

GENERATION OF ALARMS

Suppose that a line fault causes a loss of signal, or severe errors (see Figure 1). The monitor will lose synchronization and will generate a local Red Alarm. In addition, the monitor will transmit a Blue Alarm onward to the far-end office. The Blue Alarm's "continuous 1s" pattern maintains the clock recovery operation in the subsequent digital repeaters. The monitor will also transmit a Yellow Alarm backwards to the near-end office to indicate the loss of alignment.

In CEPT terminology, the Blue Alarm is analogous to an Alarm Indication Signal (AIS). The Red Alarm is a Service Alarm Indication or Prompt Maintenance Alarm. The Yellow Alarm is an "alarm indication to the remote end".

The alarm requirements for T1 are described in CCITT Recommendation G.733 and in Bell Pub 43801, Section A, Paragraph 6. The alarm requirements for CEPT PCM 30 are described in CCITT G.732.

RED ALARM WITH THE R8070

When the R8070 loses frame alignment (synchronization), Receive Red Alarm (RRED) goes high (following the F-bit on RSER whose error caused "loss of sync"). The R8070 will immediately attempt to reframe. If there are many errors on the line, RRED may be seen to pulse high and low as synchronization is partially recovered and then lost. External circuitry may be used to apply "hysteresis" to RRED so that it conforms to the minimum time requirements for the Red Alarm defined by Bell Pub 43801. If there are no errors on the line, the R8070 will reframe within the specified maximum reframe time.

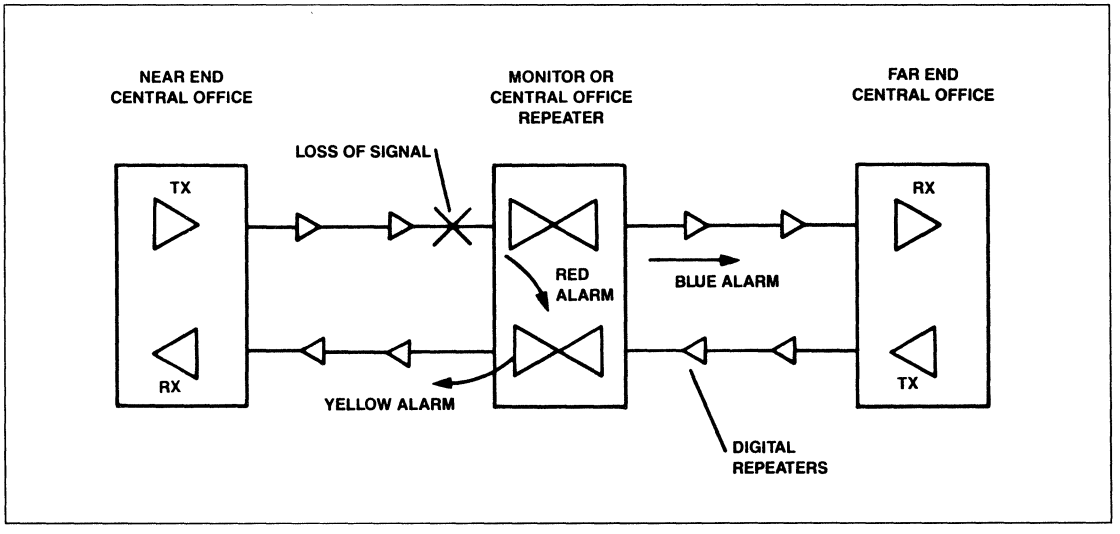

Figure 1. Alarm Signals on a Typical PCM Link

Figures 2 and 3 show the timing of RRED for the T1 modes and CEPT PCM 30 modes, respectively. All transitions of RRED are coincident with bit 1 of the first channel of the frame. RRED goes low to indicate frame alignment is correct, and this always occurs at a multiframe boundary. RRED goes high to indicate loss of frame alignment, and this occurs at the frame boundary associated with the erroneous F-bit (T1) or TS 0 (CEPT PCM 30) which caused the loss of alignment.

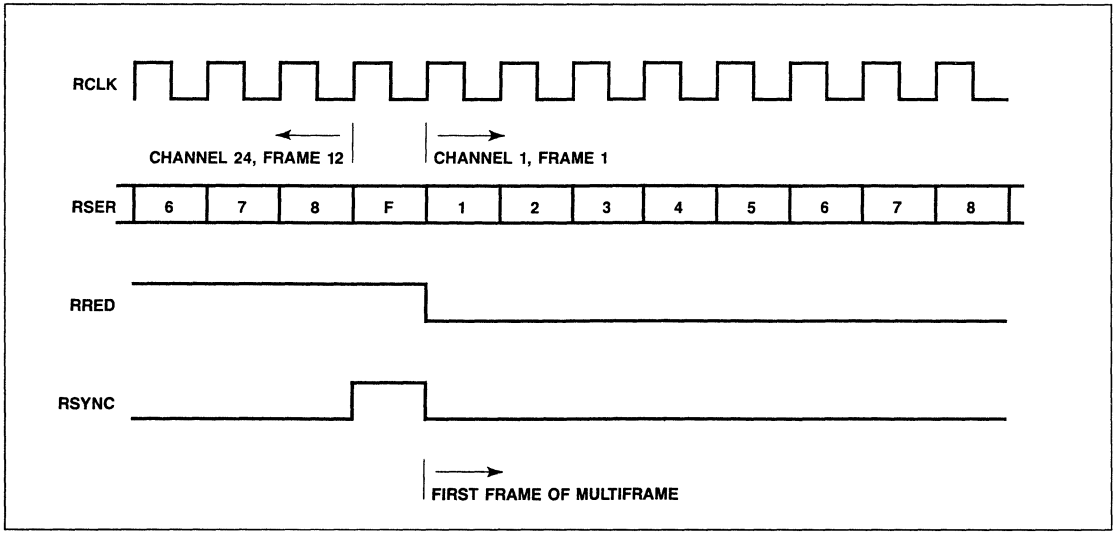

Figure 2. RRED Timing - T1 Modes

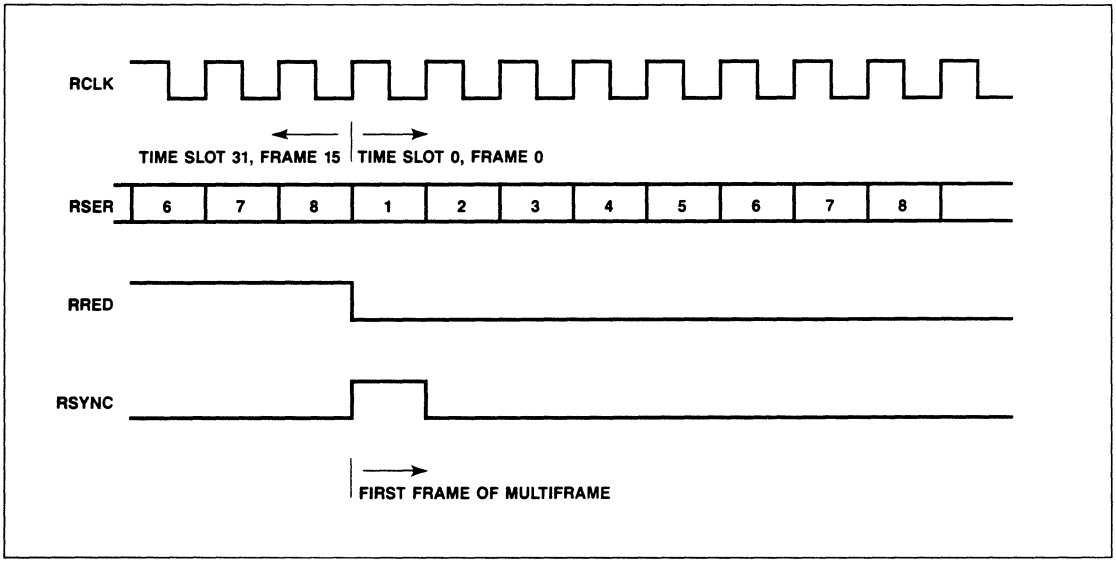

Figure 3. RRED Timing - CEPT PCM 30 Modes

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YELLOW ALARM WITH THE R8070

When TYEL is high, Yellow Alarm is transmitted, with a format dependent on the selected R8070 mode.

Mode	Format
T 1 D4	a. Bit 2 = 0 in all data channels b. Fs = 1 in frame 12 (selected by YELMD)
T1 ESF	Repeated pattern of 8 zeros, 8 ones on data link
CEPT PCM 30	Bit 3 = 1 in TS 0 of non-frame alignment frames

Note: For T1 ESF, the actual number of patterns sent depends on the timing of TYEL:

1. Patterns are sents continuously until TYEL goes low.
2. A minimum of 255 patterns is sent, regardless of TYEL width.
3. Whenever TYEL rises, the 255 count is restarted.
4. If TYEL is toggled at the rate of TCLK, Yellow Alarm patterns are transmitted only for the duration of the toggling, with no minimum count.

YELLOW ALARM AT THE RECEIVER

When configured in the same mode as the far-end transmitter, the receiver will indicate reception of a Yellow Alarm (RYEL high). RYEL is only valid when the receiver is in multiframe alignment. RYEL goes high at the trailing edge of the bit that signifies the Yellow Alarm and which meets the count threshold if a count is involved.

Mode	Format
T1 D4	a. Bit 2 = 0 for 255 consecutive channels b. Fs = 1 in frame 12 (selected by YELMD)
T1 ESF	16 patterns of 8 zeros, 8 ones on data link
CEPT PCM 30	Bit 3 = 1 in time slot 0 of non-frame alignment frames

BLUE ALARM WITH THE R8070

The Blue Alarm is a continuous 1s pattern across all 24 T1 channels; the F-bits remain unchanged. This is referred to as a "framed 1s" pattern. Compare this to the continuous 1s pattern produced by the R8070 during loopback. That signal includes the F-bits, producing an "unframed" pattern.

The circuit of Figure 4 shows how a control signal, TBLUE, causes "all 1s" to be transmitted. This assumes a serial data interface and that signaling is either not used, or used with TSER as the assigned source (TSIGMD high). For a parallel interface, an OR gate is required on each of the T1-T8 parallel inputs and signaling inputs IA and IB (if used).

MULTIFRAME RED AND YELLOW ALARMS - CEPT PCM 30

In 256S mode there is a multiframe (MF) equivalent of the Red and Yellow Alarms. If the receiver loses multiframe alignment due to either:

1. two consecutive errors in the multiframe alignment signal, or
2. time slot 16 contains all zeros for at least one multiframe, then the MF Red Alarm (RMRED) goes high. This signal is automatically coupled to the transmitter and causes a MF Yellow Alarm to be sent (bit 6 = 1 in time slot 16, frame 0).

At the receiver, RMYEL goes high to indicate the reception of a MF Yellow Alarm.

GREEN ALARM

Green Alarm denotes a system failure, and would be generated externally to the R8070.

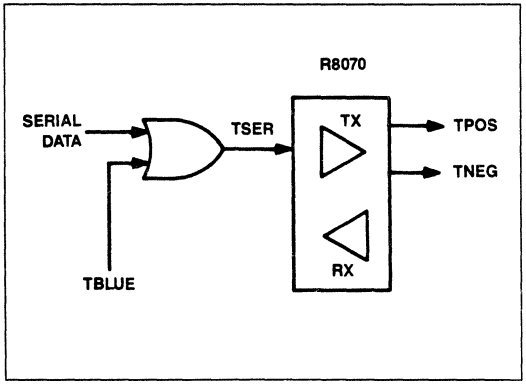

Figure 4. Transmitting Blue Alarm

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An Off-Line Framer for the R8070

SYSTEM OVERVIEW

When a PCM receiver loses frame synchronization it will automatically attempt to regain sync by searching again for the frame and multiframe alignment bits or patterns. During this resynchronization interval, the data is usually discarded and signaling bits frozen at their previous value. However, there may be a requirement to maintain the reception of data and/or signaling, based on the previous frame alignment, until the new alignment is established. At which point, the received channel data and signaling would switch over to the new alignment. This technique is known as off-line framing.

The R8070 turns off (gates to zero) received parallel data until the new alignment is found. This is known as on-line framing. Note that the serial data on RSER remains valid, regardless of the synchronization state. It is exactly the same as the serial input data, delayed by the receiver's throughput delay of 14 clock periods.

This application note describes a method for performing off-line framing with the R8070.

THE PRINCIPLE OF OFF-LINE FRAMING

Figure 1 illustrates the difference between on-line and off-line framing. A serial input to a PCM receiver is represented by a dot pattern within parallel lines. The regular pattern indicates the consistent and repetitive nature of the framing bits or frame alignment pattern. A transient period of errored frames is shown by the broken pattern.

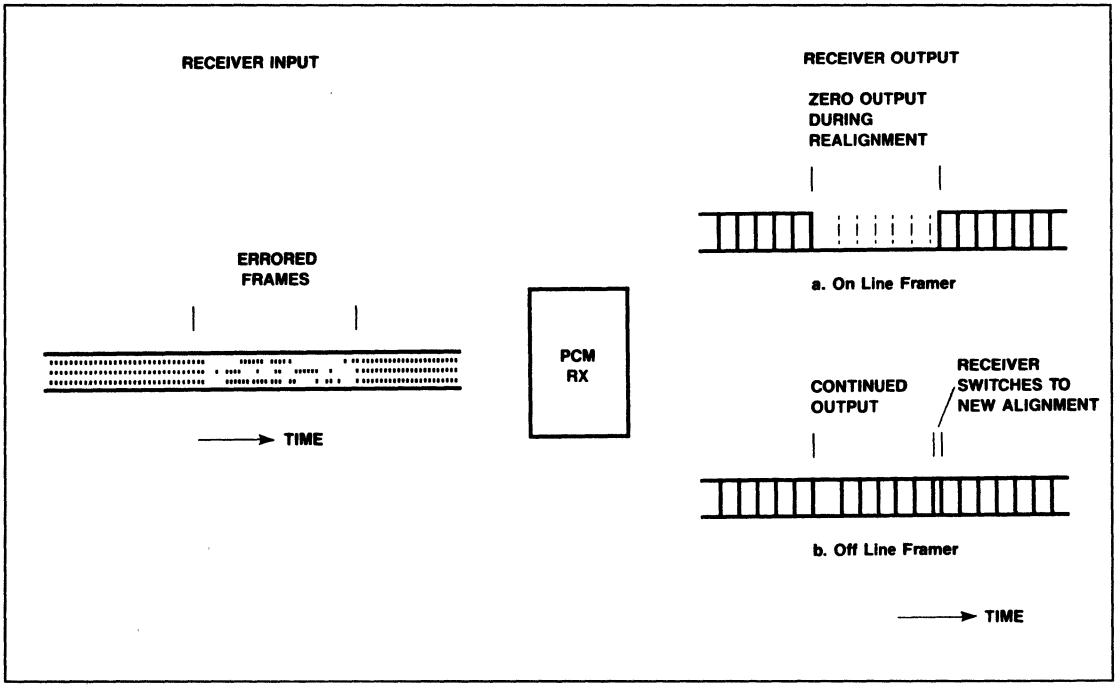

Figure 1. The Principle of Off-Line Framing

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A typical receiver output is shown for:

a. An on-line framer

b. An off-line framer

In both cases the vertical lines indicate the frame boundaries, which appear at regular intervals until the errors are received. When the error criterion is met the receiver will declare loss of alignment and attempt to realign. The effect on the receiver's data output during the reframe period depends on whether the framing is done on or off-line.

On-Line Framer

For the on-line framer, the receive output is inhibited. The frame boundaries, were they visible at the output, might occur as indicated by the dashed vertical lines. During the errors, the receiver's timing may wander so that the actual frame boundaries are not precisely known. After the errors have passed and the receiver is realigned, the frame boundaries are re-established and these may differ from the supposed boundaries of the error period. However, this would not be evident as the output would be zero during the realignment period. Note that the R8070 will declare loss of alignment at a frame boundary and will declare the realignment at the new frame boundary.

Off-Line Framer

For the off-line framer, the receive output continues uninhibited while the receiver realigns. Again the frame boundaries are marked by vertical lines. During the errors, the true alignment may not be accurately known. After the errors have passed, the receiver switches to its new alignment and this may differ from that previously supposed during the error period.

CONVERTING ON-LINE TO OFF-LINE

To convert a receiver from on-line to off-line framing requires a data output that is not inhibited during reframe and a source of timing with the original frame alignment. The data input could be used but might require B8ZS or HDB3 decoding. Fortunately, the R8070 has a serial output, RSER, which is always present, regardless of the synchronization state, and a variety of different clocks and status indicators. A simple logical combination of these signals will provide the necessary timing to extract a parallel data output based on the last known frame alignment.

OFF-LINE FRAMER FOR THE R8070 – T1

Figure 2 shows a typical circuit to perform off-line framing for T1, with the associated timing diagrams in Figure 3.

RSER is clocked into a shift register on the falling edge of RCLK so as to avoid to transitions of RSER which occur on the rising edge of RCLK. When the 8 data bits of a channel are collected in the shift register they are loaded in parallel into the latch by the latch signal. The timing of this latch signal dictates the channel boundaries. The generation of this and related signals is described below.

The central timing element is an 8-bit counter which (Bit Counter) counts the bits in a frame. The Bit Counter is incremented on the rising edge of RCLK. The signal to reset or clear the bit counter determines the frame boundaries. The clear signal is derived in three ways, one or more of which may be active at any time depending on the synchronization state.

1. The AND function of bit 7 and bit 8 of the Bit Counter. This decodes the binary number 11000000 (decimal 192), being the number of bits in a frame excluding the F-bit. In the absence of any other active clear signal, this signal will "auto-reset" the counter to produce 193–bit frames.

2. RSYNC enabled by inverse RRED. During normal operation, when the receiver is correctly frame-aligned and RRED is low, the RSYNC pulse is one bit wide and coincident with the first F-bit of the multiframe. This pulse is used to ensure that the external Bit Counter maintains synchronization with the R8070's internal bit counter. Between RSYNC pulses, the external Bit Counter continues its frame definition based on its own count of 192 bits (see signal 1). When the receiver is out of frame alignment, the RSYNC pulses are absent and the Bit Counter must maintain its frame definition based solely on its internal count of 192 bits.

3. When the receiver returns to frame alignment it is necessary to bring the external Bit Counter back into synchronization as quickly as possible. This could be achieved with signal 2 above. However, because RRED falling edge occurs at the end of the RSYNC pulse, this first RSYNC pulse is missed and synchronization is not affected until the next RSYNC, one multiframe later. For faster resynchronization the falling edge of RRED itself is used to clear the Bit Counter. This is achieved by Exclusive ORing RRED with a 1-bit delayed version of itself, thereby producing a single bit width pulse at the falling edge. Note that a similar pulse is produced at the rising edge of RRED which serves only to emphasize the last known alignment before that alignment is lost.

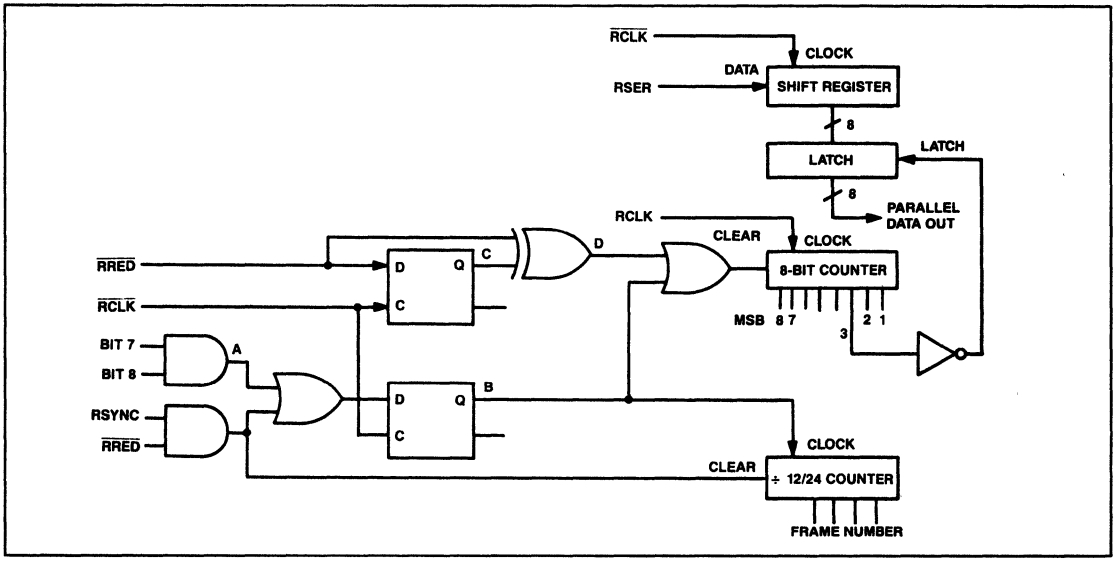

Figure 2. Off-Line Framer for the R8070 - T1

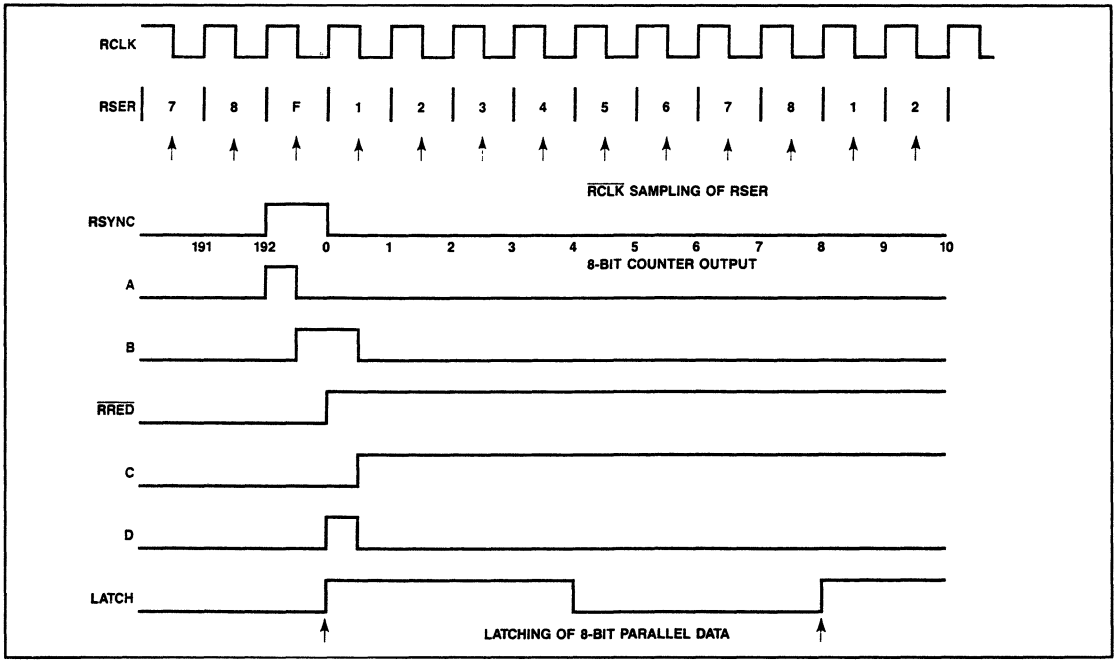

Figure 3. Off-Line Framer Timing - T1

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As an added feature, a divide-by-12 (or divided–by–24 for ESF) counter will produce a frame count from the frame rate clear pulses of the Bit Counter and is synchronized by the RSYNC pulse.

The latch control signal is derived from bit 3 of the Bit Counter which has the required period of 8 bits.

Note that the multiple clear signal is clocked by the falling edge of RCLK to avoid the transients of RRED, RSYNC and the outputs from the Bit Counter which are all aligned to the rising edge of RCLK. The Bit Counter must have an asynchronous clear function.

From the timing diagram of Figure 3 it can be seen that the clear signal not only resets the Bit Counter to zero but holds it at zero so as to miss one RCLK count. This allows for the F-bit which upsets the regular 8-bit pattern of channel data. Notice that the F-bit is actually clocked into the shift register, but because of the 1-bit hold-off of the counter, the latch signal is delayed by one bit and the F-bit is shifted through the register and out the other end, allowing the next 8 bits of channel 1 to be acquired by the latch. The timing signals A, B, C, and D relate to those points of the circuit of Figure 2.

Off-Line Framer for the R8070 - CEPT PCM 30

Figure 4 shows a typical circuit to perform off-line framing for CEPT PCM 30, with the associated timing diagrams in Figure 5.

RSER is clocked into a shift register on the falling edge of RCLK so as to avoid to transitions of RSER which occur on the rising edge of RCLK. When the 8 data bits of a channel are collected in the shift register they are loaded in parallel into the latch by the latch signal. The timing of this latch signal dictates the channel boundaries. The generation of this and related signals is described below.

The central timing element is an 8-bit counter which counts the bits in a frame. The Bit Counter is incremented on the rising edge of RCLK. The signal to reset or clear the Bit Counter determines the frame boundaries. The Bit Counter is reset in one of two ways:

1. The counter will reset itself to zero when it reaches a count of 255. This does not actually produce a clear signal, it is an inherent action of the counter to overflow upon reaching the maximum count. In the absence of any other clear signal the Bit Counter will maintain its own frame alignment by this means.
2. When the receiver is correctly frame aligned, a single width pulse on RSYNC occurs coincident with the first bit of the multiframe (bit 1, time slot 0, frame 0). When gated with RCLK a half-bit pulse results which clears the Bit Counter and thus synchronizes it with the R8070's internal Bit Counter. RSYNC is only valid as a multiframe rate signal when RRED is low, hence the gating with inverse RRED. Note that RRED falling edge occurs at the front of the RSYNC pulse and so the very first valid RSYNC is available to reset the external Bit Counter.

As an added feature, a 4-bit, divide-by-16 counter will produce a frame count from the inverse MSB of the Bit Counter and is synchronized by the RSYNC pulse.

The latch control signal is derived from bit 3 of the Bit Counter which has the required period of 8 bits.

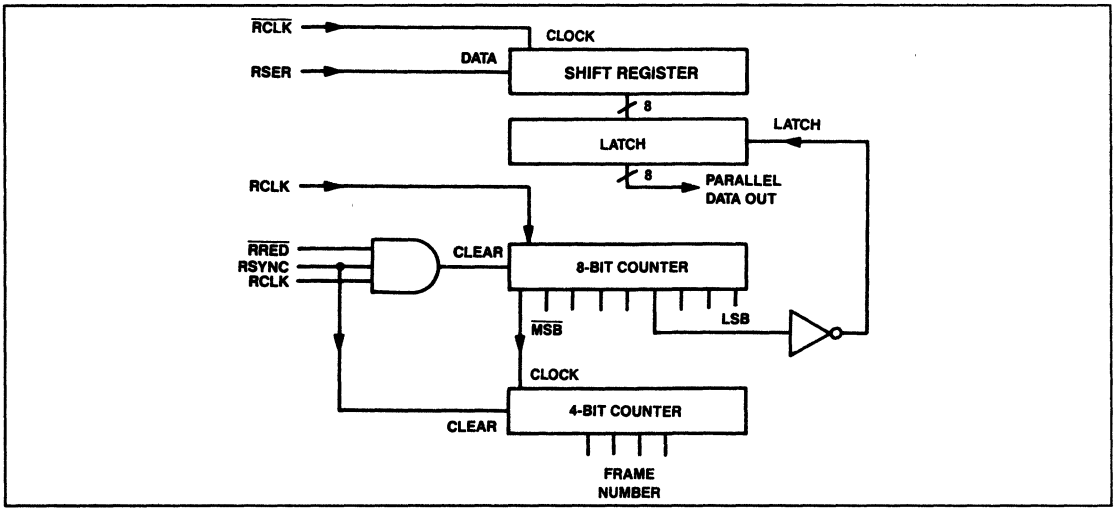

Figure 4. Off-Line Framer for the R8070 - CEPT PCM 30

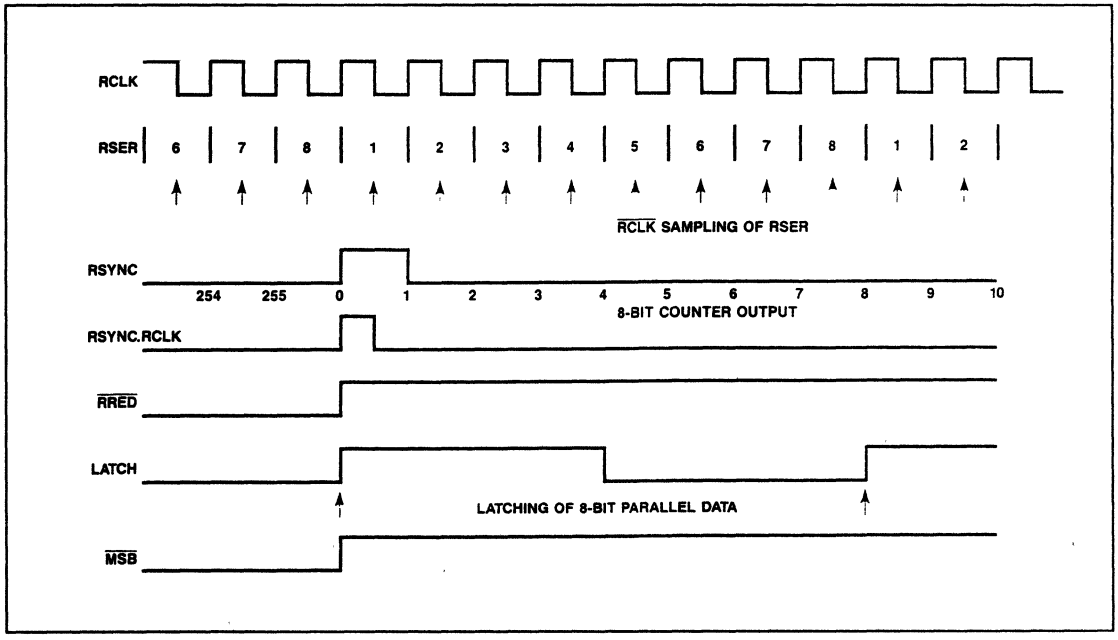

Figure 5. Off-Line Framer Timing - CEPT PCM 30

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Signaling Freeze with the R8070

SYSTEM OVERVIEW

Signaling, on a Pulse Code Modulation (PCM) transmission system, is the transmission of information related to the operation of the network. Signaling data includes the on-hook and off-hook condition of the telephone terminals, dialed digits, call progress states such as busy and ringing, as well as network status and control signals.

This information is passed over the PCM link in a variety of ways depending on the PCM standard; T1 D4, T1 ESF, or CEPT PCM 30.

SIGNALING FORMATS

T1 D4

DC signaling, such as the on/off type of digit pulses, are transmitted as their direct binary equivalent, 0 and 1. Two bits, A and B, are associated with each of the 24 channels on the PCM link. These A and B signaling bits are transmitted in place of the least significant bits of the data for each channel in frame 6 (A bits) and frame 12 (B bits). Because each channel has signaling bits directly associated with it that relate only to that channel, this technique is known as Associated Channel signaling.

The network may also use tone combinations to convey signaling information. These tones lie within the 4-kHz telephone channel (although not necessarily within the voice pass band) and are digitized and transmitted in the same way as the voice signal.

Additional signaling may be conveyed in the Fs part of the F-bit stream after the standard pattern has been used to set up the multiframe alignment.

T1 ESF

Associated Channel signaling is also used in Extended Superframe Format (ESF). In this case, however, there are four signaling bits for each channel, A, B, C, and D, because the multiframe is twice as long as that of D4. These bits replace the LSB of the data for each channel in frames 6, 12, 18, and 24, respectively. These four bits offer more signaling combinations, but for compatibility with existing D4 systems sometimes only two bits are used, with C = A and D = B.

Signaling tones are transmitted in the voice channels as for D4. Additional signaling capacity is afforded by the spare F-bits; only six are required for framing and six for a CRC check. The remaining 12 bits per multiframe carry link data which includes alarm reporting and performance monitoring.

Common Channel signaling is also used in ESF. This technique uses a separate information path for signaling. One or more of the 24 data channels might be dedicated to signaling. Alternatively, the spare F-bits can provide a 4-kHz signaling channel.

The signaling scheme uses an HDLC-like data link which transmits packets of data concerning each of the voice channels to which it relates. Such data includes the address of the called party, routing instructions, call progress, etc. One signaling link can accommodate all the necessary signaling for many voice channels because the transmission bandwidth is used more efficiently than the simple on/off codes of associated signaling. The most recent signaling scheme of this kind is known as CCITT Signaling System No. 7.

Common Channel signaling enables the computers that perform the switching function to communicate more efficiently, allowing faster and more reliable connections to be made and released. This flexibility provides the basis for a multipurpose digital network - ISDN (Integrated Services Digital Network).

CEPT PCM 30

The CEPT version of PCM also has an Associated Channel and a Common Channel form of signaling.

Associated Channel signaling uses 4 bits, A, B, C, and D, to represent the signaling states of each of the 30 channels. These bits are transmitted in time slot 16, together with a signal that defines the multiframe boundaries. The signaling bits convey essentially the same on/off information as the original DC systems , i.e., on-hook and off-hook conditions.

In Common Channel signaling, time slot 16 is treated as a clear 64 kbps data channel. HDLC-coded data according to CCITT No. 7 is passed in this channel and contains signaling data for many voice channels.

SIGNALING FREEZE - T1

In the T1 PCM system there is a new requirement for signaling freeze. This dictates that in the event of loss of frame alignment in an Associated Channel signaling system, the signaling bits should remain (frozen) in their last valid state. The following extracts from Bell Publication 43801 Section A define the requirement.

2.5 SIGNALING FREEZING (NEW REQUIREMENT)

2.5.1 On detection of loss of frame, the on-hook and off-hook signaling states presented to the channel units must be maintained in the state that existed before detection of the out of frame condition. This requires buffering of the signaling information. Specific actions are covered for individual channel units in Section C. The probability of freezing in the wrong signaling state for a 50 percent ones density out of frame condition must be no more than 5 percent. The signaling states must not be changed until the terminal regains synchronization or declares a Carrier Failure Alarm.

6.4 CARRIER FAILURE ALARM

6.4.1 A Carrier Failure Alarm (CFA) is defined as the detection of the beginning and end of a carrier system outage. A "Red Alarm" is defined as a locally detected failure and a "Yellow Alarm" is defined as a remotely detected failure. These color indications are useful in identifying the direction in which a failure has occurred. Either a red or yellow alarm starts a CFA and the CFA controls the trunk conditioning process.

6.5 TRUNK CONDITIONING AND CO-ORDINATION

6.5.1 Under conditions resulting in failure of 24 or more channels in either direction, which would be detected by the Carrier Failure Alarm or by fuse failures, the leads connecting to the central office are to be conditioned to achieve the following:

a. Minimize the chance of a false charge and prevent attempts to use the trunk for the new calls. (i.e., send busy signal).

b. Prevent seizure of terminating end switching equipment by sending on-hook toward the terminating end for the duration of the failure.

c. Automatically restore trunks to service in a co-ordinated manner after the trouble is cleared.

SIGNALING FREEZE - CEPT PCM 30

There is no equivalent requirement in CEPT PCM 30 for signaling freeze. Section 4 of CCITT Recommendation G.732 requires that an Alarm Indication Signal (AIS) be transmitted in place of the channel associated signaling bits under conditions of loss of frame alignment. AIS is an all ones signal.

The remainder of this application note deals with the extraction of channel-associated signaling and the implementation of signaling freeze in the T1 PCM system.

SIGNALING EXTRACTION

There are various different implementations for signaling extraction. These can be categorized as either completely discrete or as microprocessor-based with a discrete interface. Figure 1 illustrates these alternatives forms.

The discrete logic version takes the signaling data from the R8070 output, R8, and stores the A and B bits for each channel in the latch. The latch control is responsible for the acquisition of the correct bits and its timing is derived from various R8070 clocks. The stored A and B bits are passed to the signaling processor.

The microcontroller version reads the channel data in parallel form and, in doing so, acquires the signaling data along with the voice data. The data interface may provide buffering between the R8070 and the microcontroller. The timing interface provides appropriate signals to the microcontroller so that the signaling bits can be distinguished. Status information would also be coupled to this processor so that, for example, loss of frame alignment could be determined.

With the microcontroller approach, the signaling freeze function can easily be implemented as the signaling bits are normally stored in memory. The store is updated only when the receiver is frame aligned.

A discrete form of circuit to implement signaling freeze is described below.

A CIRCUIT FOR SIGNALING FREEZE - MODE 193S

Figure 2 shows a typical circuit that extracts the associated signaling data and incorporates the signaling freeze function. This is based on the block diagram of the discrete interface shown in Figure 1. Figure 3 and Figure 4 show the related timing waveforms at the multiframe level and frame/channel level, respectively.

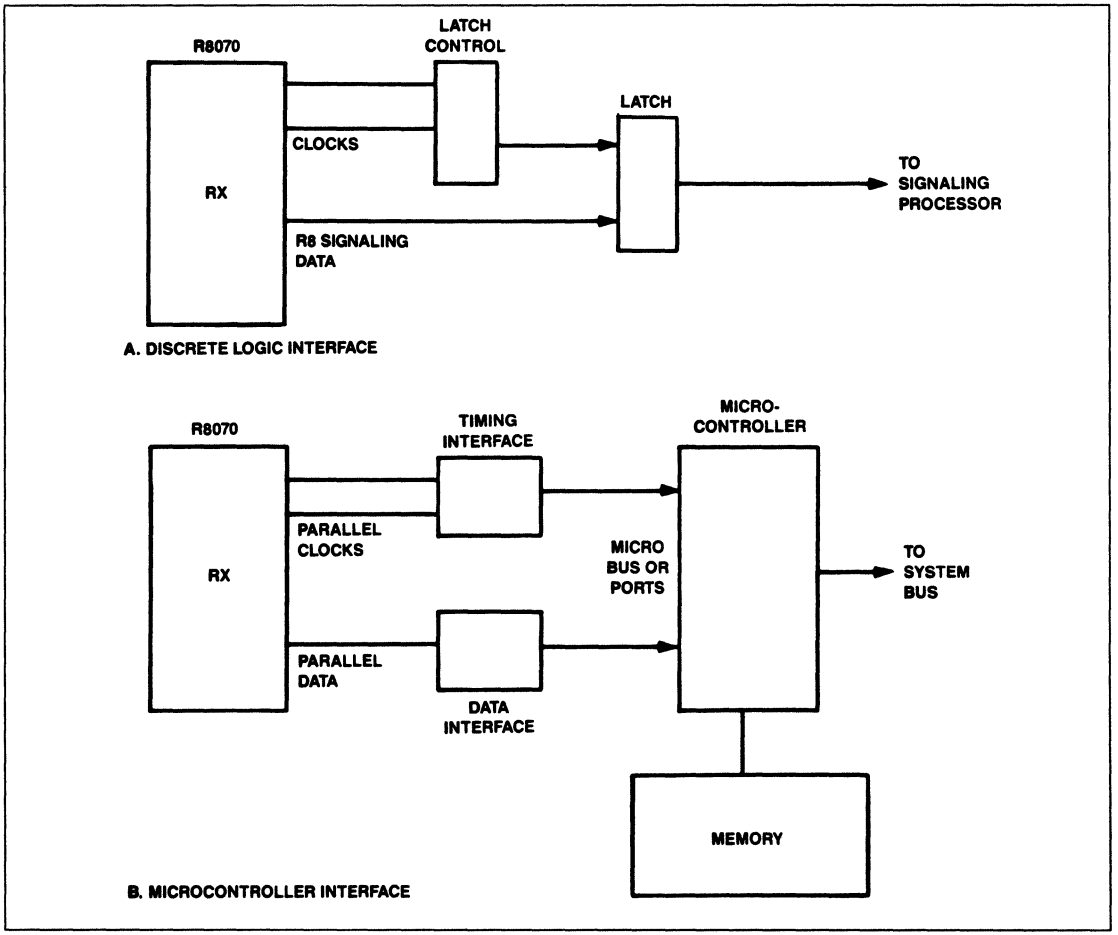

Figure 1. Alternative Interface for Signaling Extraction

The circuit may be used with either a serial or a parallel interface selected for the R8070. The circuit derives all the timing signals required from those available from the R8070 in both modes.

The circuit consists of two parts as indicated in the block diagram of Figure 1: the latches and the latch control. A total of 48 latches are needed to store an A bit and a B bit for each of 24 channels. An expanded view of one of these latches is shown. Signaling data is output from the R8070 on R8 and coupled in parallel to all the latches. A latch control signal is applied to each latch in turn according the channel number being received.

The latch control signals are derived from two decoders, one for the A bits, one for the B bits. The appropriate decoder is selected by RSBIT. If RSBIT is high, the A bit latches are enabled; if RSBIT is low, the B bit latches are enabled. The operation of the decoders is as follows:

A divide-by-8 counter is incremented by RCLK and produces a signal, Rchclk, which is similar to the RCHCLK produced by the R8070 with a parallel interface. Rchclk has a period equal to the channel time and a rising edge near the center of the channel period. The divide-by-8 counter is cleared by RSIG which maintains synchronization with the multiframe and restricts the Rchclk pulses to the 24 channels contained in frame 6, and the 24 contained in frame 12.

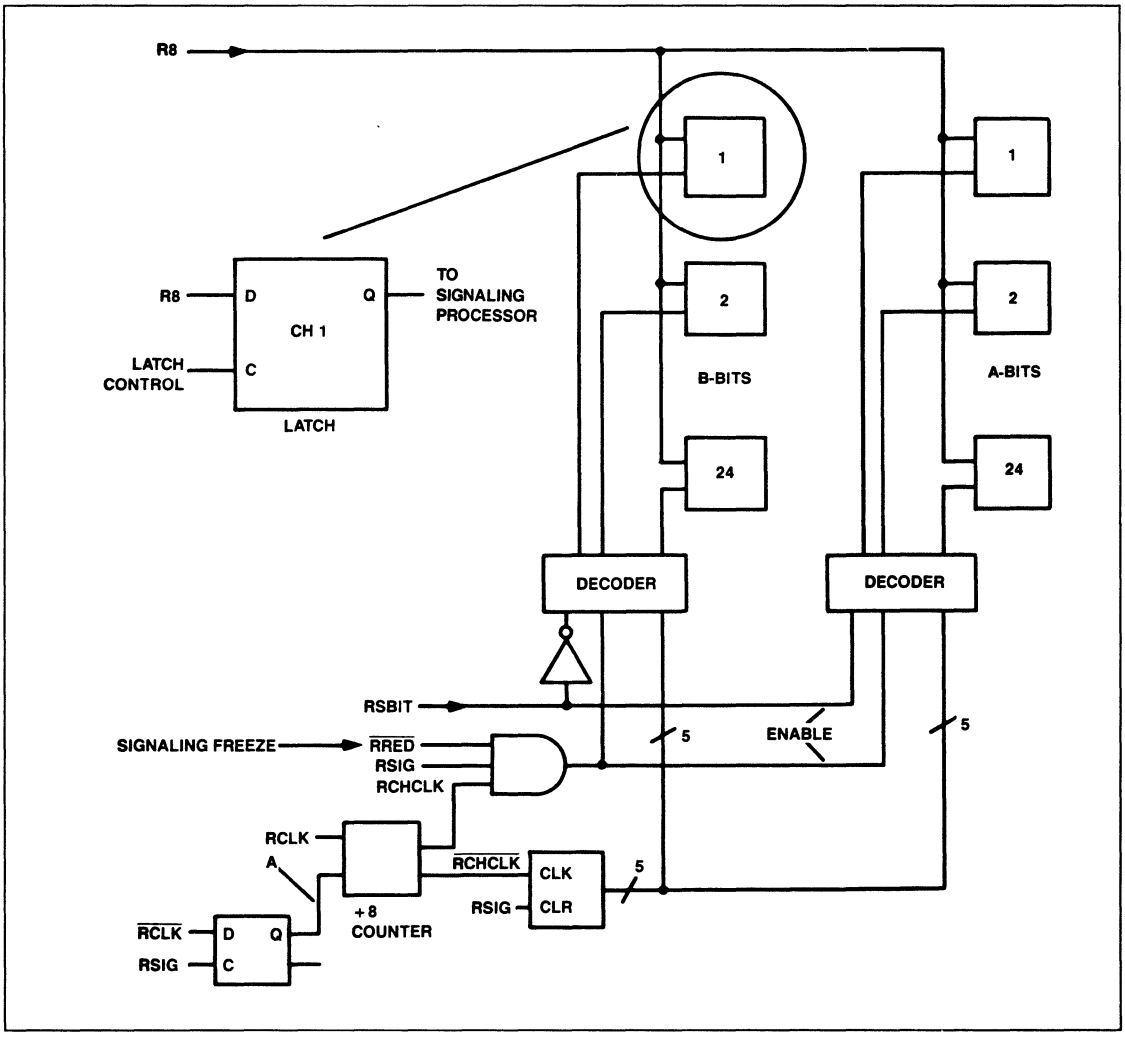

Figure 2. Signaling Freeze for the R8070 - Mode 1985

After additional gating with inverse RRED and RSIG, the Rchclk pulse enables the decoders and clocks the signaling data into the latches (D-type flip–flops).

The RSIG gating limits the Rchclk pulses to the signaling frames. (This could be considered redundant in view of the RSIG function in the clear of the divide-by-8 counter.)

The gating with RRED executes the signaling freeze function. When the receiver is out of frame alignment RRED is high and no further pulses reach the latches so they maintain their previous values until the receiver is again in frame alignment.

RSBIT determines whether the current signaling bits are A or B, and enables the appropriate decoder.

The decoders are sequenced by the 5-bit channel counter. This counter is incremented by $\overline{\text{Rchclk}}$ so as to interleave the channel increments with the data latching. RSIG clears this counter to limit the count to 24 frames and maintain multiframe alignment.

8

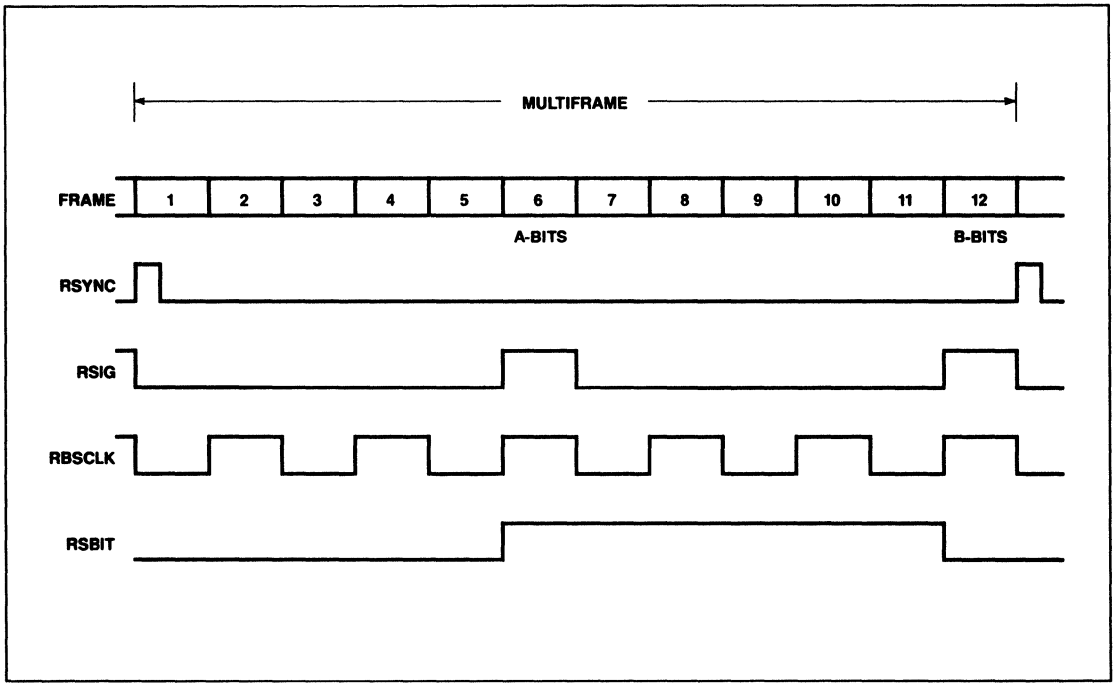

Figure 3. Multiframe View of A, B Signaling - Mode 1985

SIGNALING FREEZE IN OTHER MODES

Signaling freeze is only of interest in the T1 signaling modes:

193S for T1 D4

197S for T1C

193E for ESF

197S

In 197S mode the same circuit can be used. The L bits result in slightly different timing but the signaling data would be latched correctly.

193E

In ESF the same type of circuit could be used but twice as many latches would be required to store the A, B, C, and D bits for each of 24 frames. Four decoders would be required and a suitable control signal to select them. This would be derived from RSIGBD, RSIGCD, and RSIG.

PROCESSOR-BASED SIGNALING FREEZE

The storage or buffer function is assumed to be contained in the signaling processor. It is therefore only necessary to supply the appropriate clock, data, and status information to the processor. The essential signals to pass to the processor are R8, RSBIT, RRED, a signaling clock to indicate valid signaling data, and binary channel number.

The logic required for the signaling clock and the channel number are similar to that of Figure 2. Figure 5 illustrates the interface to the signaling processor.

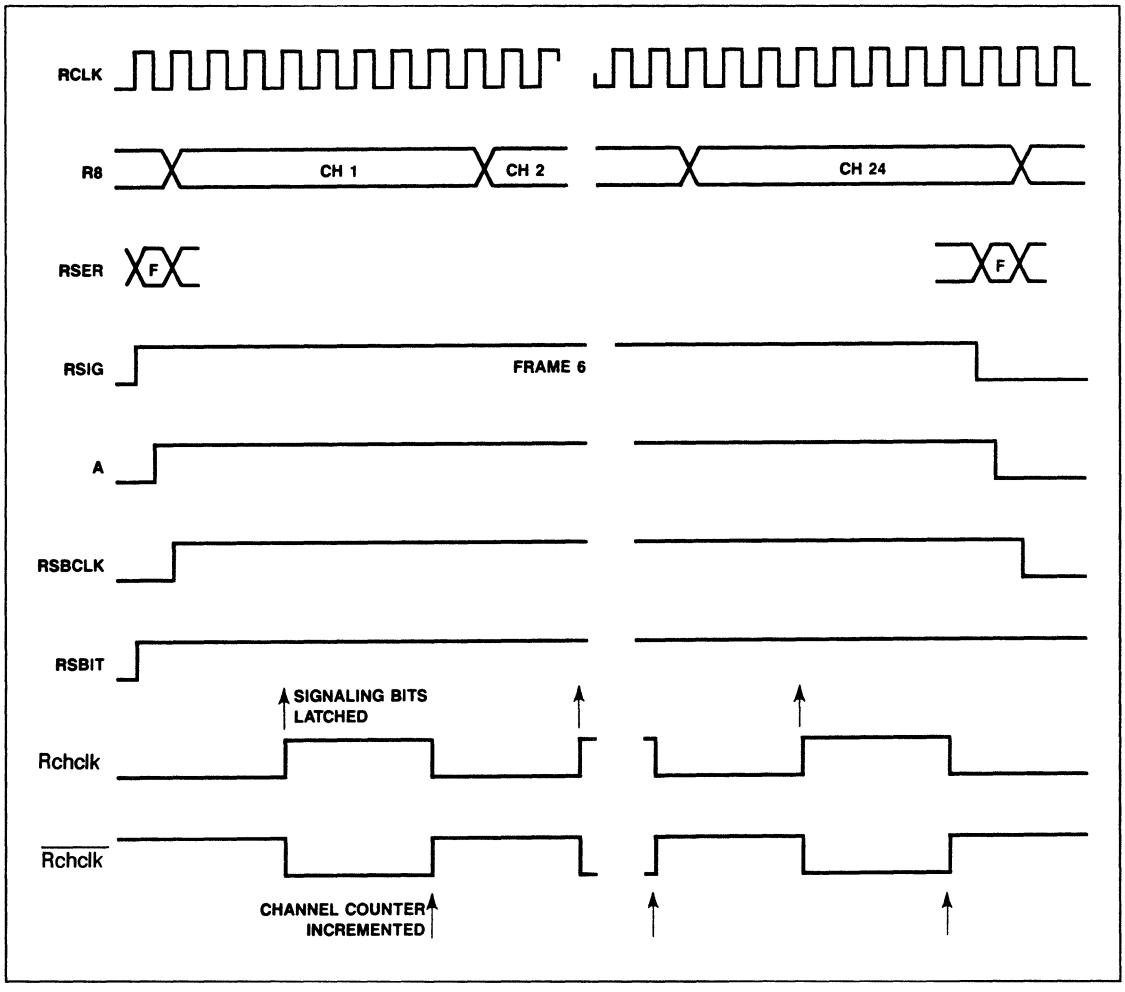

Figure 4. Timing for Signaling Freeze - Mode 1985

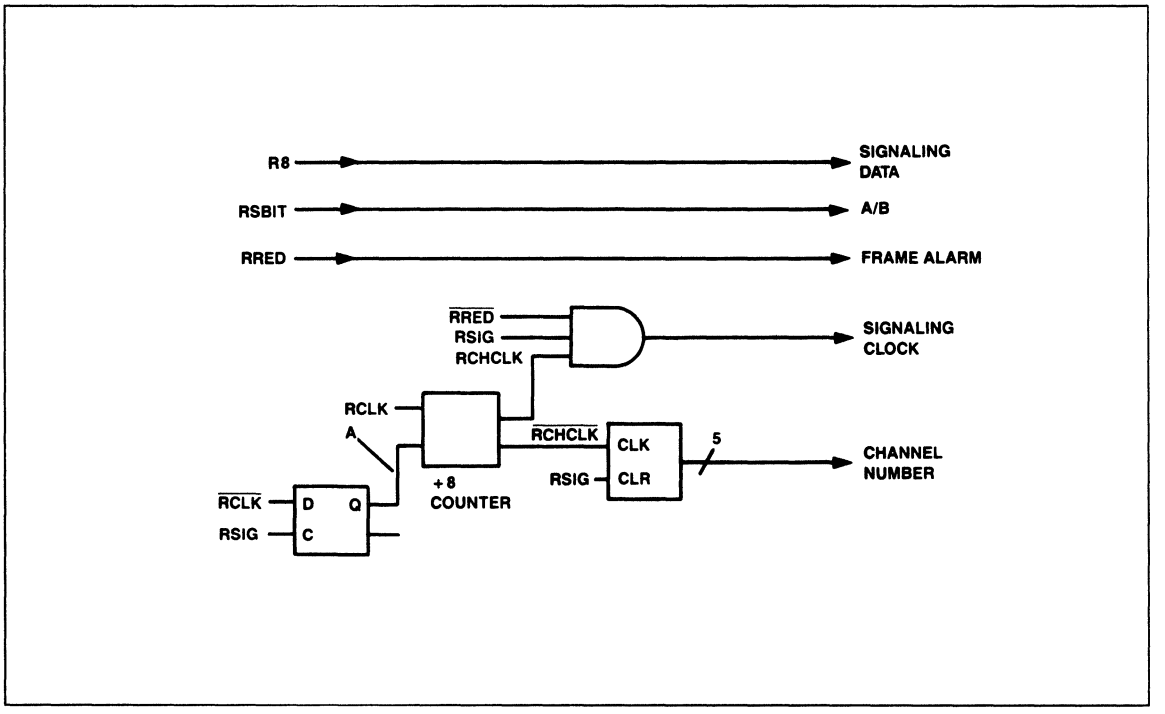

Figure 5. Basic Interface to Signaling Processor

Rockwell

Programming the R8071 ISDN/DMI Link Layer Controller's Buffers

INTRODUCTION

The versatile Rockwell R8071 ISDN/DMI Link Layer Controller finds applications in many diverse areas of telecommunication. The R8071 owes it's versatility to the ease in which it can be programmed to accommodate different applications. This application note, used with the R8071 Data Sheet (Order No. 318), shows the ease in which the R8071 can be initialized and programmed. This application note describes only one of many methods in which the R8071 can be programmed. This application note features:

System Initialization

A synopsis of the overall system initialization including when and how to configure and activate the System Buffer (Activation Byte and Channel Buffer Pointer), Receiver Command Buffer, Receive Data Buffer, Transmit Command Buffer and Transmit Data Buffer.

Configuring System Buffer

An example and explanation of how to program the System Buffer, which consists of the Channel Activation Byte and the Buffer Pointer Addresses.

Configuring Transmit Command Buffer

An explanation of how to program the Transmit command Buffer, and a description of some of the features available in the buffer. These features include: Modes Control, Loop Back options, Data Inversion, Automatic Channel deactivation, Status Bits reporting (UNDR, IVBA, CF/$\overline{P}$, CMND and MPTY bit) and Fill/Mask.

Configuring Transmit Data Buffer

An explanation of how to program the Transmit Data Buffer, and a description of some of the features available in the buffer. Features such as: Buffer Size, Data Length and Status Byte (UNDR, IVBA, CF/$\overline{P}$, CMND and MPTY bit) and Fill/Mask. In addition, different application usages will be discussed briefly.

Configuring Receive Command Buffer

An explanation of how to program the Receive Command Buffer, and a description of some of the features available in the buffer. These features include: Modes Control, Loop Back options, Data Inversion, Automatic Channel deactivation, Status Bits reporting (OVER, IVBA, CF/$\overline{P}$, CMND and MPTY bit) and Fill/Mask.

Configuring Receive Data Buffer

An explanation of how to program the Receive Data Buffer, and a description of some of the features available in the buffer. These features include: Buffer Size control, Status Byte (OVER, IVBA, ABRT, FCER, SHER, CF/$\overline{P}$, CMND and MPTY bit) and Fill/Mask. In addition, different application usages will be discussed briefly.

HARDWARE & SYSTEM OVERVIEW

The R8071 ISDN/DMI Link Layer Controller interfaces to a microprocessor (host) through a Dual Port RAM (DPRAM). The DPRAM, as it's name indicates, allows both the R8071 and the microprocessor (host) to access the same memory location in the DPRAM at the same time without causing a bus contention. In order for the R8071 and host to communicate effectively there must be an agreed upon format in which information is passed back and forth via the DPRAM. The format used by the R8071 to communicate effectively with the host is by setting up buffers in the DPRAM. There are five types of buffers as described in the R8071 data sheet:

1. System Buffer
2. Receive Command Buffer
3. Receive Data Buffer
4. Transmit Command Buffer
5. Transmit Data Buffer

The structure of each buffer is dependent upon the type of microprocessor (host) used to interface with the R8071 via the DPRAM. The MDFS input pin of the R8071 can be strapped to allow the R8071 to interface to either a 68000 or 8086 compatible word addressing microprocessor. (MDFS high [+5 Vdc] selects a 68000 compatible microprocessor system, while MDFS low [0 Vdc or GND] selects an 8086 compatible microprocessor system). The major difference between 68000 and 8086 compatible microprocessors that affects the R8071 is the addressing scheme used by the selected microprocessor. In an Intel 8086 compatible word addressing system, the most significant byte of a two-byte pointer resides at an odd address, while the least significant byte resides at an even address. In a 68000 word addressing system, the most significant byte resides at an even address, while the least significant resides at an odd address.

SYSTEM INITIALIZATION

To begin initializing the SYSTEM BUFFER the user must determine which channel(s) is(are) to be serviced. There are different understandings as to what is a channel. In this application note it is assumed that in a communication link there is a receiver and a transmitter channel. The receiver and transmitter make up the two sides of every channel (also known as time slot). In this application note, a channel refers to only one side of a channel (i.e., the receiver or transmitter only).

Once the channel(s) that is(are) to be serviced has(have) been determined, the System Buffer needs to be programmed. The System buffer contains both the CHANNEL ACTIVATION BYTE and CHANNEL BUFFER POINTERS.

If the first channel to be serviced is a receiver, then the microprocessor would first program the RECEIVE COMMAND BUFFER. The command buffer will determine the operating mode for the channel. The mode configured in the command buffer will determine how the data in the channel is handled. Upon completion of the command buffer, the RECEIVE DATA BUFFER can be programmed.

If the first channel to be serviced is a transmitter, the host should instead program the TRANSMIT COMMAND BUFFER then the TRANSMIT DATA BUFFER.

Data to be received or transmitted need not all be contained in a single data buffer. It can be split up into several data buffers. Splitting up the buffer can maximize the use of the limited memory size. This is accomplished because, if a memory location originally assigned to a different channel is not being used, rather than being unused it can be used by another channel. Splitting a single data buffer into several data buffers also speeds up the ability of the system to process the data (improved throughput). For example, if a single data buffer is used to store the received data, the microprocessor will wait for the data buffer to fill before servicing the contents of the buffer. This means that the microprocessor will not process the data before the total data reception is completed. If the buffers were split up among smaller buffers that were linked together, the microprocessor could be processing part of a data steam while the R8071 is actively receiving other portions of the data stream.

In some applications there is a need to change the configured mode of a channel without deactivating the particular channel. This can be accomplished by linking the last data buffer to another command buffer.

If both the transmitter and receiver of a channel are to be activated, but previously only the address of one side of a channel to be serviced (i.e., Transmit side or Receive side) was programmed into the CHANNEL BUFFER POINTERS, it is necessary to make sure that the CHANNEL BUFFER POINTERS contain both addresses.

To activate or deactivate a channel requires that the ATTN and ATACK handshake be initiated. The host initiates the handshake by pulling ATTN input to the R8071 high. This causes the R8071 to service the SYSTEM BUFFER. Once all the information in the SYSTEM BUFFER has been processed, the R8071 informs the host that the task has been completed by pulling the ATACK line to the host high. The R8071 will continue to assert this line until the host acknowledges the completion of the task by resetting the ATTN line.

In some applications there is a need for minimal time delay between activating the transmit side of a channel and activating the receive side of the same channel. In such a situation, if the CHANNEL BUFFER POINTER has already been programmed with the transmit and receiver side starting address buffer, this can be achieved. This is achieved by initiating the ATTN and ATACK handshake for one side, after which the RX/TX is toggled and the ATTN and ATACK handshake is initiated again for the other side.

Repeat the above process if additional channels are to be serviced.

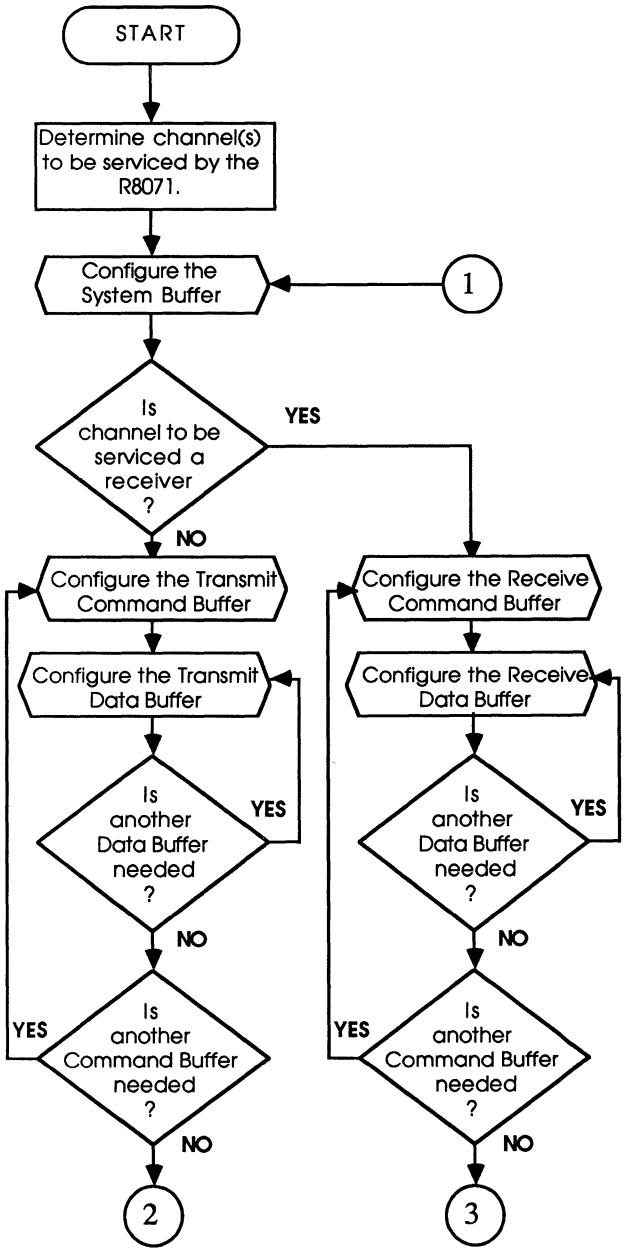

Figure 1. System Initialization Flowchart

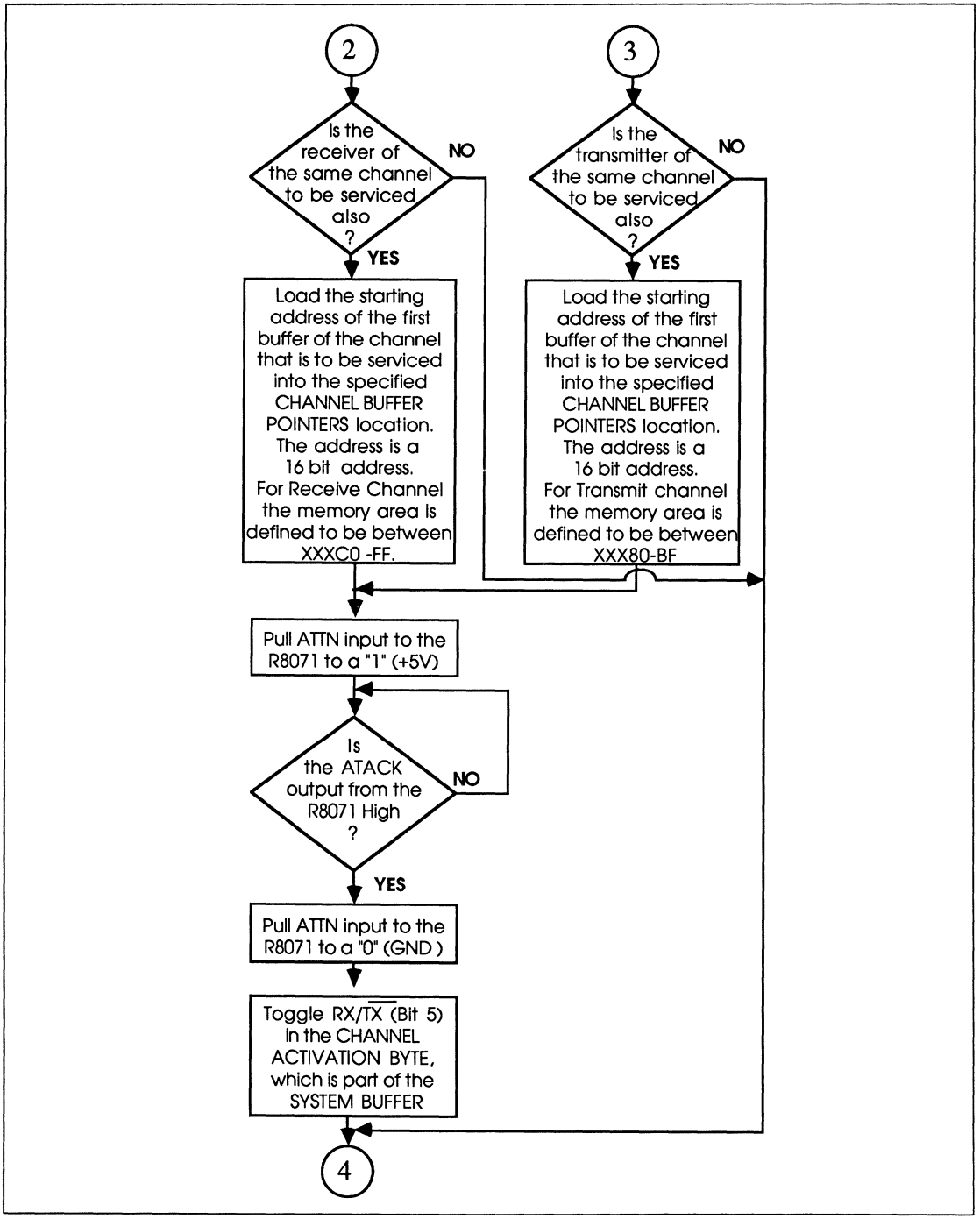

Figure 1. System Initialization Flowchart (Cont'd)

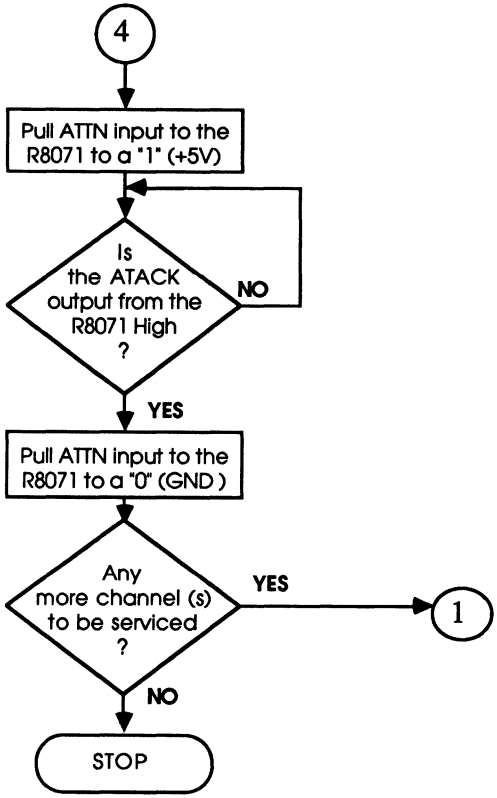

Figure 1. System Initialization Flowchart (Cont'd)

CONFIGURING SYSTEM BUFFER

The SYSTEM BUFFER consists of the CHANNEL ACTIVATION BYTE and the CHANNEL BUFFER POINTERS.

Load Bit 0-4 of the CHANNEL ACTIVATION BYTE (located at address XXX00) with the binary number of the channel that is to be serviced. Bit 4 is the MSB and bit 0 is the LSB. In a T-1 system environment, valid channels are those between 1 - 24, while in a CEPT system the valid channels (time slots) are those between 0 - 31. In an application which is neither a T-1 nor CEPT system application, all 32 channels (0 - 31) are valid.

The R8071 can only activate or deactivate one side of a channel at a time. This requires that the R8071 be told which side of the channel is to be serviced (i.e., the receive or the transmit side). The bit that determines which side of the channel is to be serviced is the $\overline{RX}/TX$ (Bit 5). Setting bit 5 to a "1" selects the receive side as the side of the channel in question to be serviced. Resetting bit 5 to a "0" selects the transmit side as the side of the channel to be serviced.

The CHANNEL BUFFER POINTERS contains 64 2-byte words which are the addresses of the first buffers for each side of the 32 channels. The CHANNEL BUFFER POINTERS are divided between the receive and the transmit sections. The transmit side CHANNEL BUFFER POINTERS are located between memory location XXX80 - XXXBF, with the transmitter channel 0 starting address located at XXX80 and 81, and transmitter channel 1 start address located at XXX82 and 83. Similar to the transmit side portion, the receive side CHANNEL BUFFER POINTERS are located between memory location XXXC0 - XXXFF.

The ACTIVE bit (Bit 7) in the CHANNEL ACTIVATION BYTE determines whether the channel to be serviced is to be activated or deactivated. Setting the ACTIVE bit to "1" would activate the channel, while resetting the bit to "0" would deactivate the channel. Deactivating one side of a channel can also be accomplished by loading the NEXT BUFFER ADDRESS with an invalid buffer address (for more detail see the section entitled, "Configuring Transmit Command Buffer").

The actual activation or deactivation process begins only when the ATTN input line to the R8071 is asserted. The data contained in both the CHANNEL ACTIVATION BYTE and the CHANNEL BUFFER POINTERS at the time the ATTN input is asserted determines the actual channel that is to be serviced. Once a particular channel has been serviced (i.e., activated or deactivated) and the ATTN input to the R8071 is no longer asserted, modifying the data in the CHANNEL ACTIVATION BYTE and the CHANNEL BUFFER POINTER will not change the operating mode of the previous serviced channel. This allows the R8071 to have more than one channel active at a time.

This is accomplished in the R8071 by activating one channel (i.e., initiate the ATTN and $\overline{ATACK}$ handshake). Upon completion of the ATTN and $\overline{ATACK}$ handshake, the information for the next channel to be activated can then be loaded into the ACTIVATION BYTE and the CHANNEL BUFFER POINTER. Upon completion of the next ATTN and ATACK handshake, two channels are now active. To have additional channels activated, the whole process is repeated.

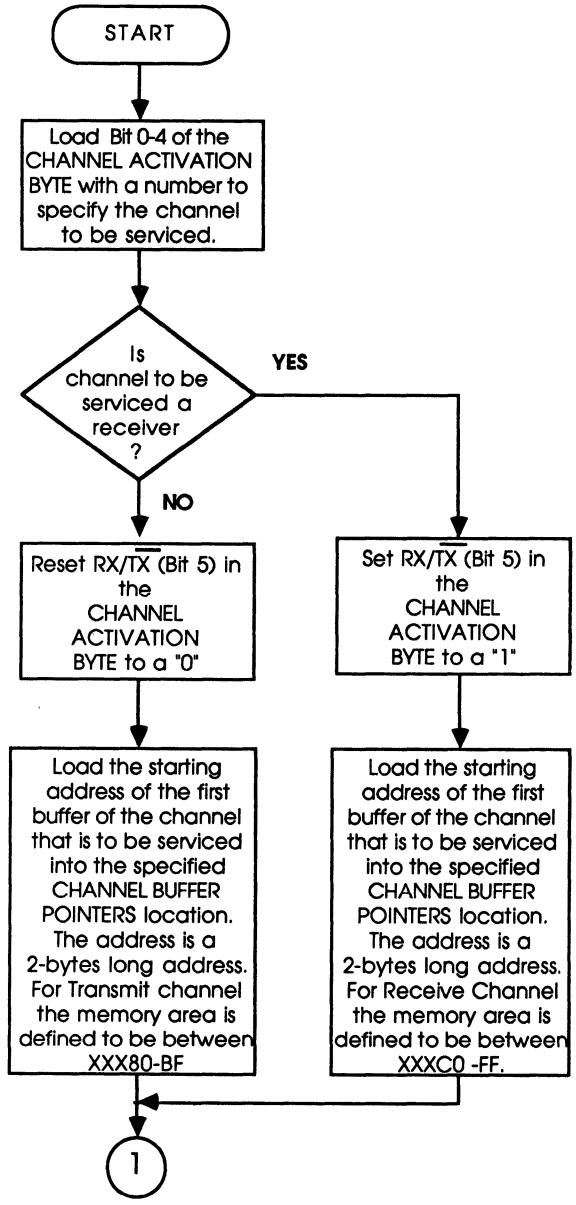

Figure 2. Configuring System Buffer Flowchart

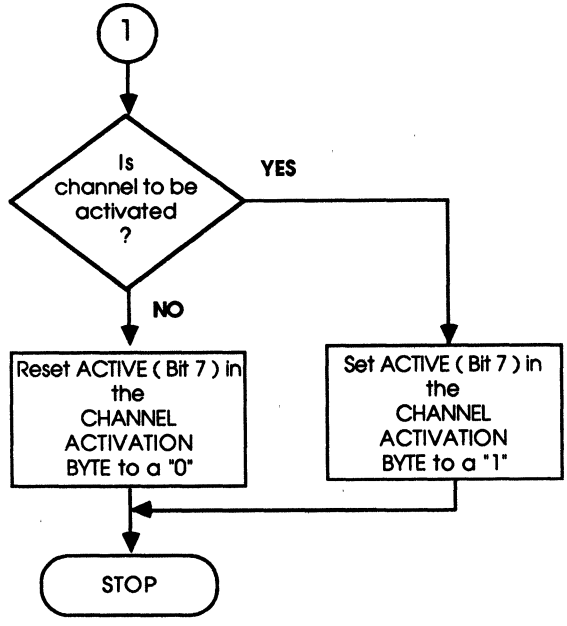

Figure 2. Configuring System Buffer Flowchart (Cont'd)

CONFIGURING TRANSMIT COMMAND BUFFER

Set the CMND bit (Bit 1) in the STATUS BYTE to "1". This will ensure that the R8071 will be able to distinguish the difference between a DATA BUFFER and a COMMAND BUFFER. A DATA BUFFER would have this bit reset to "0".

Load the NEXT BUFFER ADDRESS with the address of the next buffer to be processed upon completion of this buffer. Typically, the next buffer after a COMMAND BUFFER is a DATA BUFFER. However, the NEXT BUFFER ADDRESS could contain the current buffer's address, or an invalid buffer address. Pointing to an invalid buffer address (any address between FFF0 - 0000) will deactivate the channel which the current buffer is part of. The channel will be deactivated only after the completion of the current buffer.

The STATUS byte in the TRANSMIT COMMAND BUFFER contains the UNDR, IVBA, CF/$\overline{P}$, CMND, and MPTY bits. UNDR (underrun) and IVBA (invalid buffer address) are bits normally set by R8071, which the host would read and reset when appropriate. The CF/$\overline{P}$ (complete/partial buffer) in a COMMAND BUFFER is read by the host and set by the R8071 when it reports status for the processed COMMAND BUFFER and CMND (command) bits are only set by the host and read by R8071. In a TRANSMIT COMMAND BUFFER the MPTY (empty) bits is reset by the host and set by R8071.

UNDR (underrun), this bit is set by the R8071 when its transmit channel runs out of data. When this condition occurs the transmit channel sends an all ones pattern until additional data are available to be transmitted. The exception to this occurs when the transmit channel is in HDLC mode. In HDLC mode the specific transmit channel automatically transmit an HDLC abort code (14 consecutive ones) followed by flags.

IVBA (Invalid Buffer Address). This bit is set by the R8071 if it encounters an invalid buffer (all addresses between FFF0 - 0000). When this condition occurs, the specific transmit channel will automatically be deactivated.

The MODES byte specifies the operational mode of the given channel. It is critical that the operational mode specified for the near and far end of a transmission be the same.

Setting LOOP (bit 2) to "1" would select the associated receive channel to retrieve data stored internally in the R8071, and present it to the shared memory. The data stored in the R8071 is provided by the transmitter when it is set up for loop mode (i.e., with LOOP bit set to a "1"). When both the receive and transmit sides are set up for LOOP mode, the R8071 can perform a Local (Near-end) Loop-back. Loop-back can be done only one channel at a time.

SIG (Bit 1) and HDLC (Bit 0) together define operational mode of the specified channel.

SIG	HDLC	MODES
1	0	Non-HDLC Signaling Channel
0	0	Non-HDLC Data Channel
0	1	HDLC Data Channel
1	1	Reserved

Non-HDLC Data Channel

DMI application modes 0 and 1 may be specified by this mode. In this mode, as soon as the channel transmitter is activated and on completion of this buffer, an all ones is transmitted until data from the TRANSMIT DATA BUFFER (location of the first data buffer is determined by the NEXT BUFFER ADDRESS) is transmitted. To ensure that uninterrupted data transmission the CF/$\overline{P}$ bit in the linked data is reset to "0".

Non-HDLC Signalling Channel

When a channel is configured in Non-HDLC Signalling Channel mode, the channel carries bit-oriented signalling data without an HDLC format. Figure 9 of the R8071 Data Sheet specifies the format used to maintain the received data integrity. In this mode the R8071 assumes that there is only a maximum of 2 linked data buffers, with the last data buffer a recirculating buffer (i.e., a buffer with it's NEXT DATA BUFFER pointing to itself). To maintain continuous data transmission, the last data buffer MPTY bit is never set to a "1" by the R8071.

HDLC Data Channel

When a channel is set up to be a HDLC Data Channel it is capable of handling data in either a HDLC data format or a LAPD channel.

The 16 bit CRC-CCITT generator polynomial is:

$$X^{16} + X^{12} + X^5 + 1$$

The FILL/MASK byte is an 8-bit byte which allows the R8071 to perform rate adaption of sub-64 kbps data rates in the form of

$$n \times 8 \text{ Kbps } (n = 1 \text{ to } 8)$$

to the standard 64 Kbps bearer rate. More detailed explanations are available if figure 5 and table 4 of the data sheet.

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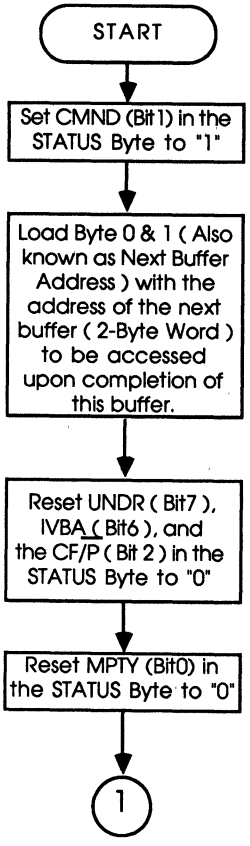

Figure 3. Configuring Transmit Command Buffer

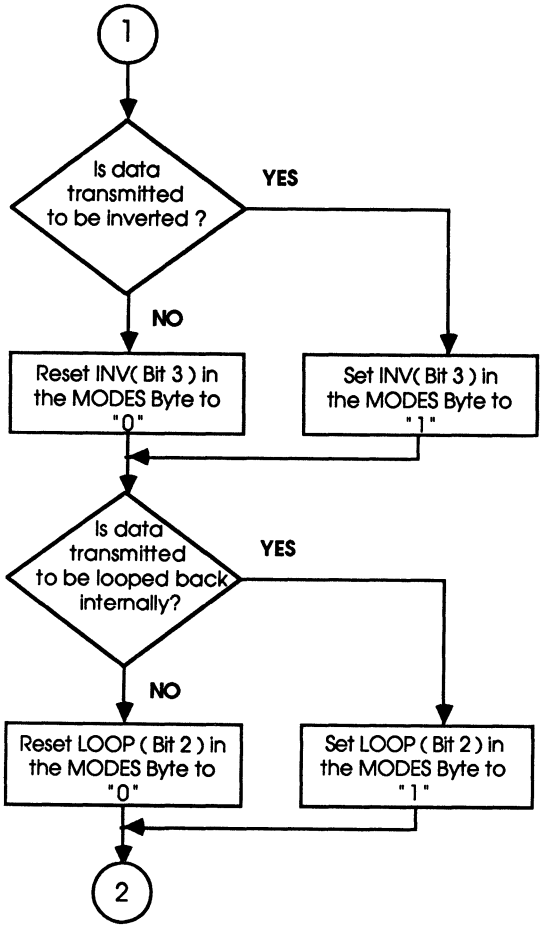

Figure 3. Configuring Transmit Command Buffer (Cont'd)

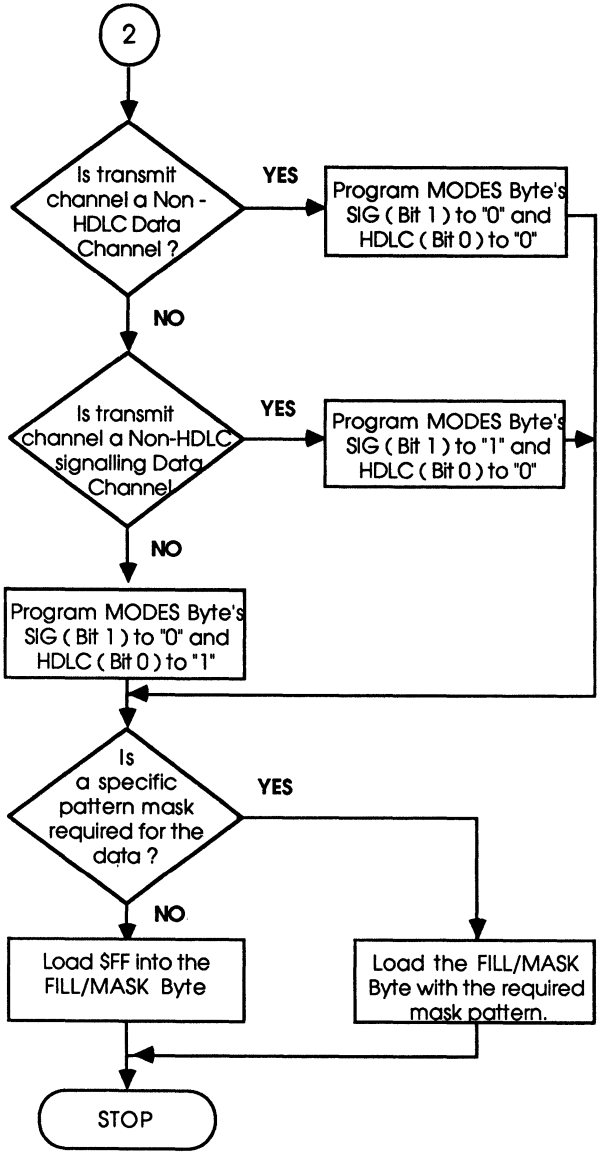

Figure 3. Configuring Transmit Command Buffer (Cont'd)

CONFIGURING TRANSMIT DATA BUFFER

Reset the CMND bit (Bit 1) in the STATUS BYTE to "0". This would ensure that the R8071 will be able to distinguish the difference between a DATA BUFFER and a COMMAND BUFFER. If this buffer was a COMMAND BUFFER the host would have this bit set to "1".

Load the NEXT BUFFER ADDRESS with the address of the next buffer to be processed upon completion of this buffer. The next buffer after a DATA BUFFER could either be a DATA BUFFER or a COMMAND BUFFER. Linking to a COMMAND BUFFER maybe desired if the operating mode of the channel need to be changed. The address contained in the NEXT BUFFER ADDRESS could be pointing to the current buffer's address, or an invalid buffer address. If the NEXT BUFFER ADDRESS contains an invalid buffer address (any address between FFF0 - 0000), the channel which the current buffer is part of will be deactivated. Deactivation will occur only upon the completion of the current buffer.

The CF/$\overline{P}$ bit (Bit 2) in the STATUS BYTE is set by the host to indicate that this buffer contains the last byte of a sequence of bytes to be formatted according the HDLC. With CF/$\overline{P}$ set, the R8071 automatically recognizes that the CRC needs to be calculated and appended at the end of the data. The R8071 performs this task before looking for more data in the next buffer.

In the current data buffer is a partial buffer (CF/$\overline{P}$ = 0) the R8071 will only look at the BUFFER SIZE, but if the data buffer is a complete buffer the R8071 will look at the DATA LENGTH instead. These sizes are used by the R8071 in determining when to start looking for another data buffer or command buffer, and to determine the location of the last data byte in the current buffer.

Setting FC (Flag Control, bit 7) in the Most Significant Byte of the DATA LENGTH (2-Byte word, but actually only 12 bits are for data length information), would select that the Flag Stuffing feature be enabled. FC allows the R8071 to automatically append a certain number of flags to the end of a data string.

The flags that are appended will vary depending on the mode of the transmitting channel. In HDLC mode, HDLC flags ($7E in hexadecimal) are transmitted. In Non-HDLC data mode, the flags are all ones octets. In a Non-HDLC signalling mode this feature is not available.

The FLAG COUNT byte determines the number of flags to be transmitted. This byte is located after the last data byte in the data buffer. The maximum number of additional flags that can be appended after the last valid data byte is 255.

The FO (Flag Offset, bit 6) in the most significant byte of the DATA LENGTH (2-byte word) is meaningful only if FC is set and the channel is in HDLC Data mode. When FO is set by the host, the R8071 will count the total number of HDLC zeros intentionally inserted among the data during the entire duration of transmission. At the end of each HDLC frame, it divides the accumulated number by eight and retains the remainder. The remainder is known as the Flag Count Offset. The R8071 would then subtract the Flag Count Offset (which is available internally to the R8071 only) from the FLAG COUNT byte. The resultant is the additional number of HDLC flags transmitted.

Reset other status bits in the STATUS Byte in preparation for transmission.

The data to be transmitted can now be loaded. Include the FLAG COUNT Byte if additional flags are to be appended after the last valid data byte.

Reset the MPTY (Bit 0) in the STATUS Byte to "0", since the buffer is now full with information that the R8071 has not processed.

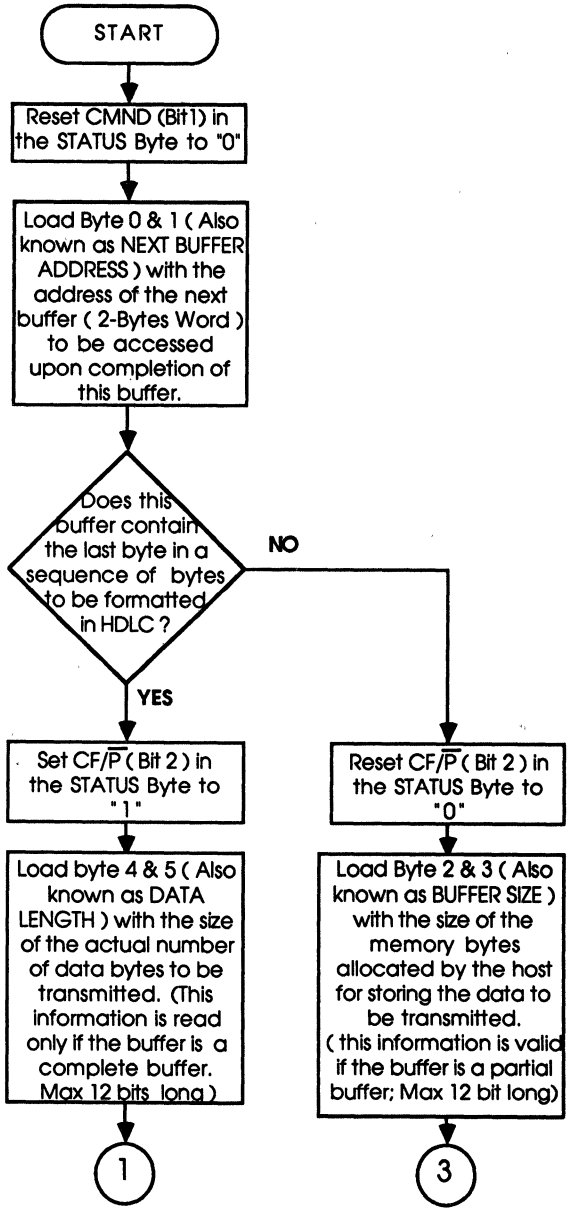

Figure 4. Configuring Transmit Data Buffer

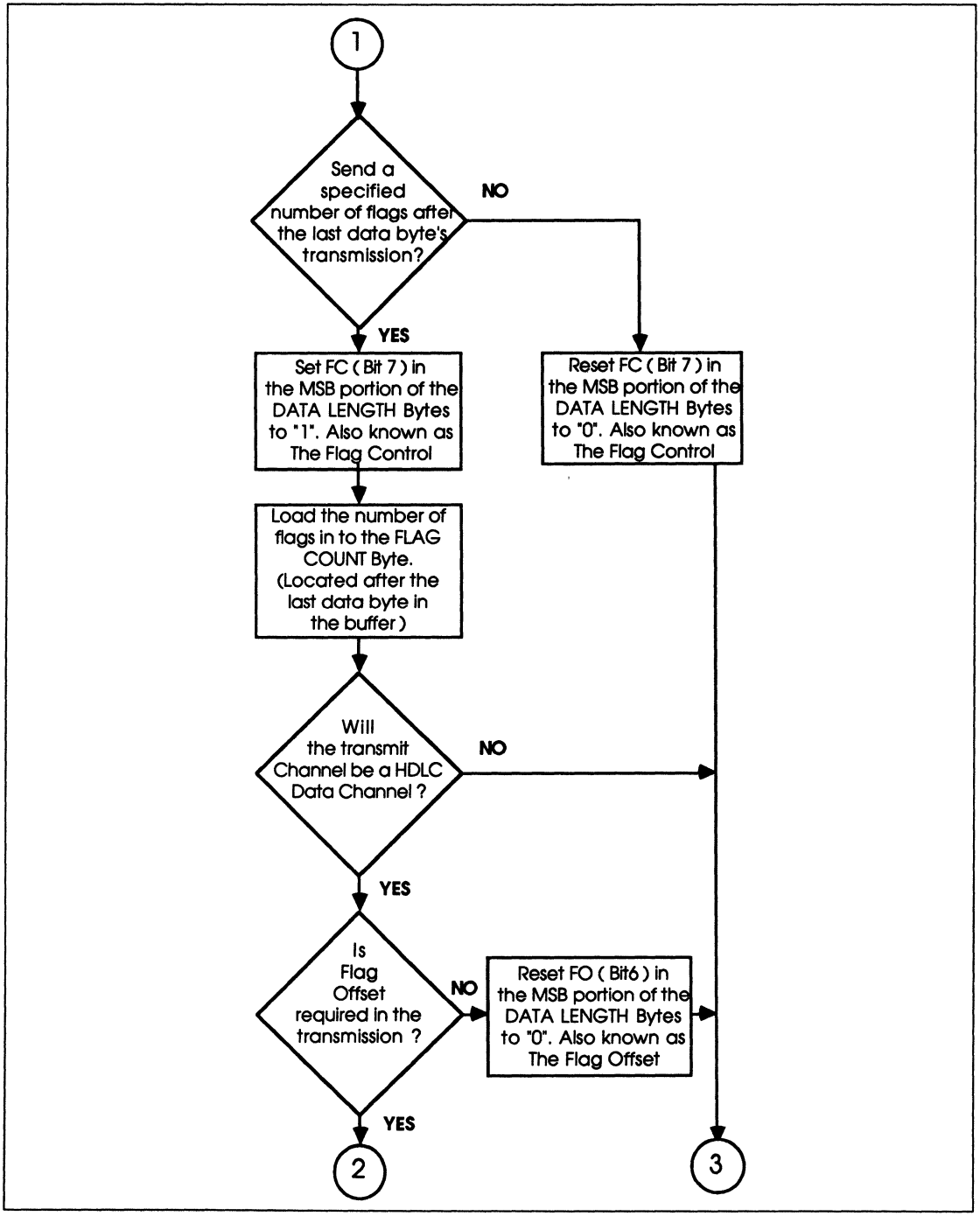

Figure 4. Configuring Transmit Data Buffer (Cont'd)

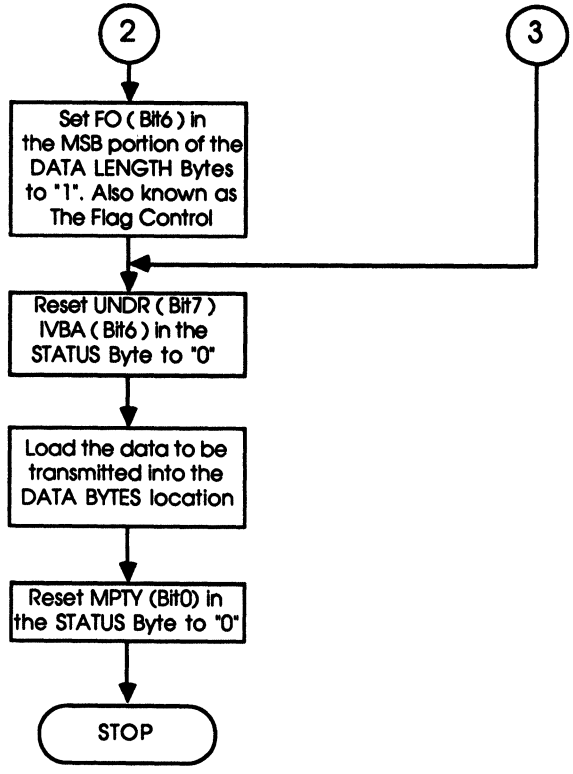

Figure 4. Configuring Transmit Data Buffer (Cont'd)

CONFIGURING RECEIVE COMMAND BUFFER

Set the CMND bit (Bit 1) in the STATUS BYTE to "1". This would ensure that the R8071 will be able to distinguish the difference between a DATA BUFFER and a COMMAND BUFFER. A DATA BUFFER would have this bit reset to "0".

Load the NEXT BUFFER ADDRESS with the address of the next buffer to be processed upon completing this buffer. Typically, the next buffer after a COMMAND BUFFER is a DATA BUFFER. The NEXT BUFFER ADDRESS could be the current buffer's address, or an invalid buffer address. If the contents of the NEXT BUFFER ADDRESS point to an invalid buffer address (any address between FFF0 - 0000), the channel which the current buffer is part of will be deactivated upon completion of the current buffer. If the address was to point to the current buffer's address, it would be called a recirculating buffer.

The STATUS byte in the RECEIVE COMMAND BUFFER contains the OVER, IVBA, CF/P, CMND, and MPTY bits. OVER (overrun) and IVBA (invalid buffer address) are bits normally set by R8071, which the host would read and reset when appropriate. The CF/P (complete/partial buffer) in a COMMAND BUFFER is read by the host and set by the R8071 when it reports status for the processed COMMAND BUFFER and CMND (command) bits are set only by the host and read by the R8071. In a RECEIVE COMMAND BUFFER the MPTY (empty) bit is reset by the host and set by the R8071.

OVER (overrun) bit is set by the R8071 when its receive channel has no next data buffer (all addresses between FF0 - 0000). When this condition occurs, the specific receive channel will automatically be deactivated.

The MODES byte specifies the operational mode of the given channel. It is critical that the operational modes specified for the near and far end of a transmission be the same.

Setting INV (bit 3) to "1" would select all data received are to be inverted prior to writing the information to the shared memory. This would be set only if the data were initially inverted prior to their transmission at the far end. All other non-data information such as HDLC flag, CRC, and ABORT are also inverted after being received.

Setting LOOP (bit 2) to "1" would select that the associated receive channel retrieve data stored internally in the R8071, and present it to the shared memory. The data stored in the R8071 is provided by the transmitter when it is set up for loop mode (i.e., with LOOP bit set to a "1"). When both the receive and transmit sides are set up for LOOP mode, the R8071 can perform a Local (Near-end) Loop-back. Loop back can be done only one channel at a time.

SIG (Bit 1) and HDLC (Bit 0) together define operational mode of the specified channel.

SIG	HDLC	MODES
1	0	Non-HDLC Signaling Channel
0	0	Non-HDLC Data Channel
0	1	HDLC Data Channel
1	1	Reserved

Non-HDLC Data Channel

DMI application modes 0 and 1 may be specified by this mode. In this mode, as soon as the channel receiver is activated it will check the allocated buffer and start placing the received data into the buffer. After filling a buffer, it updates the status of the just completed buffer, simultaneously asserting INTR. It then moves on to the next buffer and repeats the process again until it is interrupted by ATTN or runs out of buffers.

Non-HDLC Signaling Channel

When a channel is configured in Non-HDLC Signaling Channel mode, the channel carries bit-oriented signaling data without an HDLC format. The format used in order to ensure that the receive channel receives the data properly is specified in Figure 19 of the R8071 Data Sheet. In this mode the R8071 assumes that there is only a maximum of 2 linked data buffers, with the last data buffer a recirculating buffer.

HDLC Data Channel

In this mode the R8071 is capable of operating as either an HDLC data channel or a LAPD channel. The 16 bit CRC-CCITT generator polynomial used by the R8071 to generate the CRC-16 is

$$X^{16} + X^{12} + X^5 + 1$$

The FILL/MASK byte is an 8-bit byte which allows the R8071 to perform rate adaption of sub-64 kbps data rates in the form of

n x 8 Kbps (n=1 to 8)

to the standard 64 Kbps bearer rate. A more detailed explanation is available in figure 5 and table 4 of the data sheet.

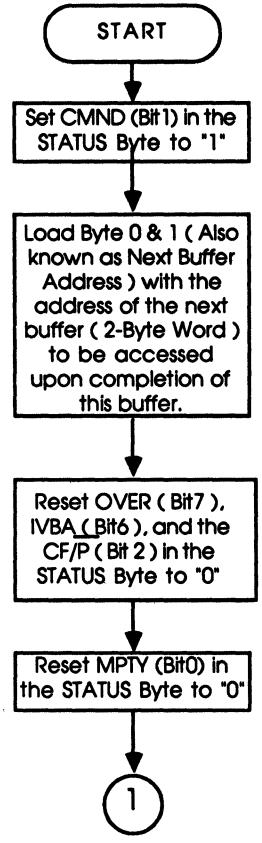

Figure 5. Configuring Receive Command Buffer

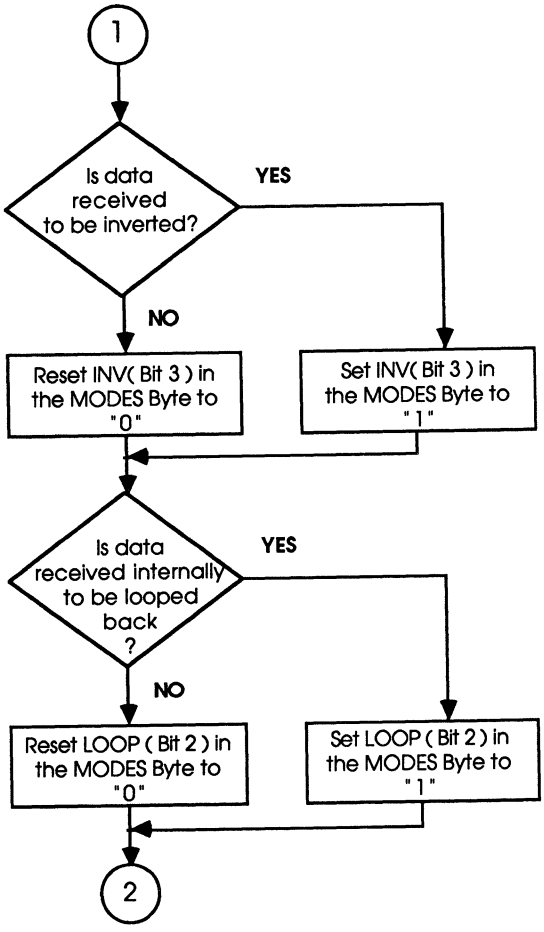

Figure 5. Configuring Receive Command Buffer (Cont'd)

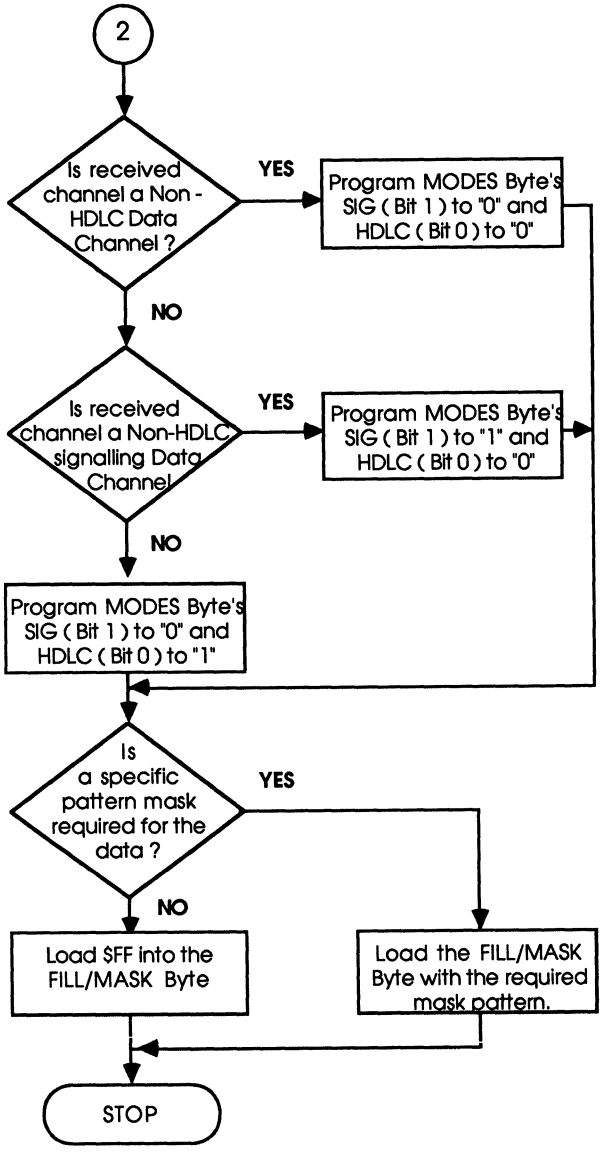

Figure 5. Configuring Receive Command Buffer (Cont'd)

CONFIGURING RECEIVE DATA BUFFER

Reset the CMND bit (Bit 1) in the STATUS BYTE to "0". This would ensure that the R8071 will be able to distinguish the difference between a DATA BUFFER and a COMMAND BUFFER. A COMMAND BUFFER would have this bit set to "1".

Load NEXT BUFFER ADDRESS with the address of the next buffer to be processed upon completion of this buffer. Typically, the next buffer after a COMMAND BUFFER is a DATA BUFFER. However, the NEXT BUFFER ADDRESS need not necessarily point to a DATA buffer, it could point to the current buffer's address, or to an invalid buffer address. If the address was an invalid buffer address (any address between FFF0 - 000), upon completing the current buffer, the channel, which the current buffer is part of will automatically be deactivated.

The BUFFER SIZE determines how much memory is allocated for the received data. The actual received data size will be written by the R8071 into the DATA LENGTH Byte.

In preparation to receive data, initialize all the status bits in the STATUS BYTE. Reset OVER (overrun, bit 7), IVBA (invalid buffer address, bit 6), ABRT (Abort, bit 5), FCER (Frame check error, Bit 4), SHER (Short HDLC Frame Error, bit 3), and CF/$\overline{P}$ (Complete Frame/Partial Frame received, bit 2) to a "0". These bits are reset to ensure that upon completion of the data reception the host will be able to determine if any error conditions may have occurred. The various error conditions that may occur are decoded from the condition of the bits in the STATUS BYTE. (For more information on the different error conditions, please refer to Table 3 in the R8071 Data Sheet). The information that can be derived from the STATUS BYTE would assist the host to determine the validity of the data received.

In preparation for the received data, the host should set the MPTY (Empty, bit 0) bit in the STATUS BYTE to "0". This is to inform the R8071 that this RECEIVED DATA BUFFER is empty and ready to receive data.

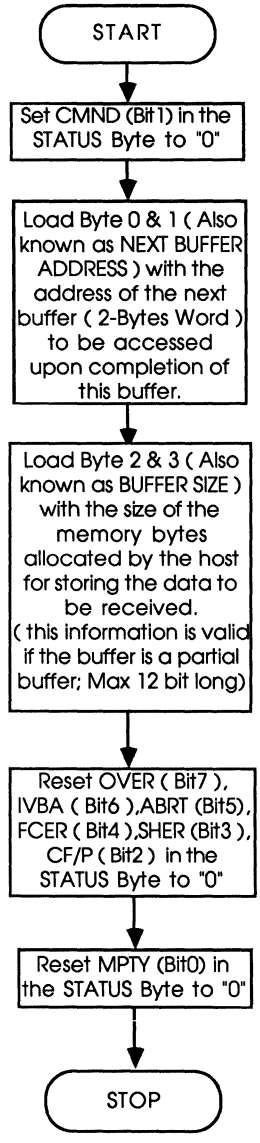

Figure 6. Configuring Receive Data Buffer

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FAX: (317) 359-2091
ESL: 62818996

2009
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(317) 457-9127
FAX: (317) 456-1234

IOWA
2070
Dy-Tronix Inc.
23 Twixt Town Rd. N.E., Ste. 201
Cedar Rapids, IA 52402-3297
(319) 377-8275
FAX: (319) 377-9163

KANSAS
2081
Dy-Tronix Inc.
1999 Amidon, Ste. 322
Wichita, KS 67203-2124
(316) 838-0884
ESL: 62914257

KENTUCKY
2082
Robert O. Whitesell & Associates
313 Lagrange Rd., Ste. 201
P.O. Box 797
Pewee Valley, KY 40056-9998
(502) 241-1441

LOUISIANA
Norcom, Inc.
(See Dallas, TX)

MAINE
Kitchen & Kutchin, Inc.
(See Burlington, Massachusetts)

MARYLAND
Beacon North
(See Sterling, Virginia)

MASSACHUSETTS
2012
Kitchen & Kutchin, Inc.
87 Cambridge St.
Burlington, MA 01803
(617) 229-2660
FAX: (617) 273-5895

MICHIGAN
2011
R.O. Whitesell & Associates
8332 Office Park Dr., Ste. A
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2013
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688 Cascade West Parkway S.E.
Grand Rapids, MI 49506-2187
(616) 942-5420

2014
Robert O. Whitesell & Associates
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FAX: 313-559-9643

2015
R.O. Whitesell & Associates
1822 Hilltop Rd.
St. Joseph, MI 49085-2307
(616) 983-7337

MINNESOTA
2077
Electronic Innovators, Inc.
9727 Valley View Rd.
Eden Prairie, MN 55344
(612) 941-0830
FAX: (612) 941-6193

MISSISSIPPI
Robert O. Whitesell & Associates
(See Huntsville, Alabama)

MISSOURI
2068
Dy-Tronix Inc.
3407 Bridgeland Drive
Bridgeton, MO 63044
(314) 291-4777
FAX: (314) 291-3861

MONTANA
2067
Simpson & Assoc., Inc.
2552 Ridge Rd. #200
Littleton, CO 80120
(303) 466-7777
FAX: 303-460-0626

NEBRASKA
Dy-Tronix Inc.
(See Cedar Rapids, Iowa)
(See Bridgeton, Missouri)

NEVADA
Criterion Sales Inc.
(See Santa Clara, California)

NEW HAMPSHIRE
Kitchen & Kutchin, Inc.
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NEW JERSEY (NORTH)
2043
PAF Associates
508 Main Street
Boonton, NJ 07005
(201) 335-0680

NEW JERSEY (SOUTH)
2017
Naudain Associates
The Pavilions at Greentree
Route 73, Ste. 307
Marlton, NJ 08053
(609) 983-5300
FAX: (609) 596-5367

NEW MEXICO
2018
Rep New Tec
9219 Lagrima De Oro Rd., N.E.
Albuquerque, NM 87111
(505) 293-2582

NEW YORK
2048
Ossman Assoc.
6666 Old Collamer Rd.
East Syracuse, NY 13057
(315) 437-7052
FAX: (315) 437-2332

2020
PAF Associates
120 W. Main Street
Smithtown, NY 11787
(516) 360-0940
FAX: 516-979-8506

NORTH CAROLINA
2021
Quantum Marketing, Inc.
6608 Six Forks Road, Ste. 203
Raleigh, NC 27615
FAX: 919-847-8271
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(See Eden Prairie, Mn)

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FAX: 614-888-8792

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TWX: 510 601-2416
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2079
Westerberg Assoc., Inc.
7165 S.W. Fir Loop
Portland, OR 97223
(503) 620-1931
FAX: (503) 684-5376

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Almo Electronics
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(301) 622-1118

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Jessup, MD 20794
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FAX: 201-575-5839

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Marshall Industries
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FAX: 201-882-0095

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Marshall Industries
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FAX: 609-768-3649

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1250 Scottsville Rd.
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FAX: 716-235-0052

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Syracuse, NY 13206
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954 Senate Dr.
Dayton, OH 45459
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Tulsa, OK 74146
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1113
Quality Components, Inc.
3158 So. 108th East Ave.
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Tulsa, OK 74146
(918) 664-8812

OREGON
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Western Micro Technology
13770 S.W. 24th
Beaverton, Or 97005
(503) 629-2082

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Marshall Industries
9705 SW Gemini Dr.
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(503) 644-5050

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6024 S.W. Jean Rd.
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Lake Oswego, OR 97034
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9815 Roosevelt Blvd.
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Pittsburgh, PA 15222
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8504 Cross Park Dr
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(512) 837-1991

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Quality Components, Inc.
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Austin, TX 78758
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Marshall Industries
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7250 Langtry
Houston, TX 77040
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