SAMSUNG

SRAM Data Book

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1996 DATA BOOK

SRAM

SAMSUNG

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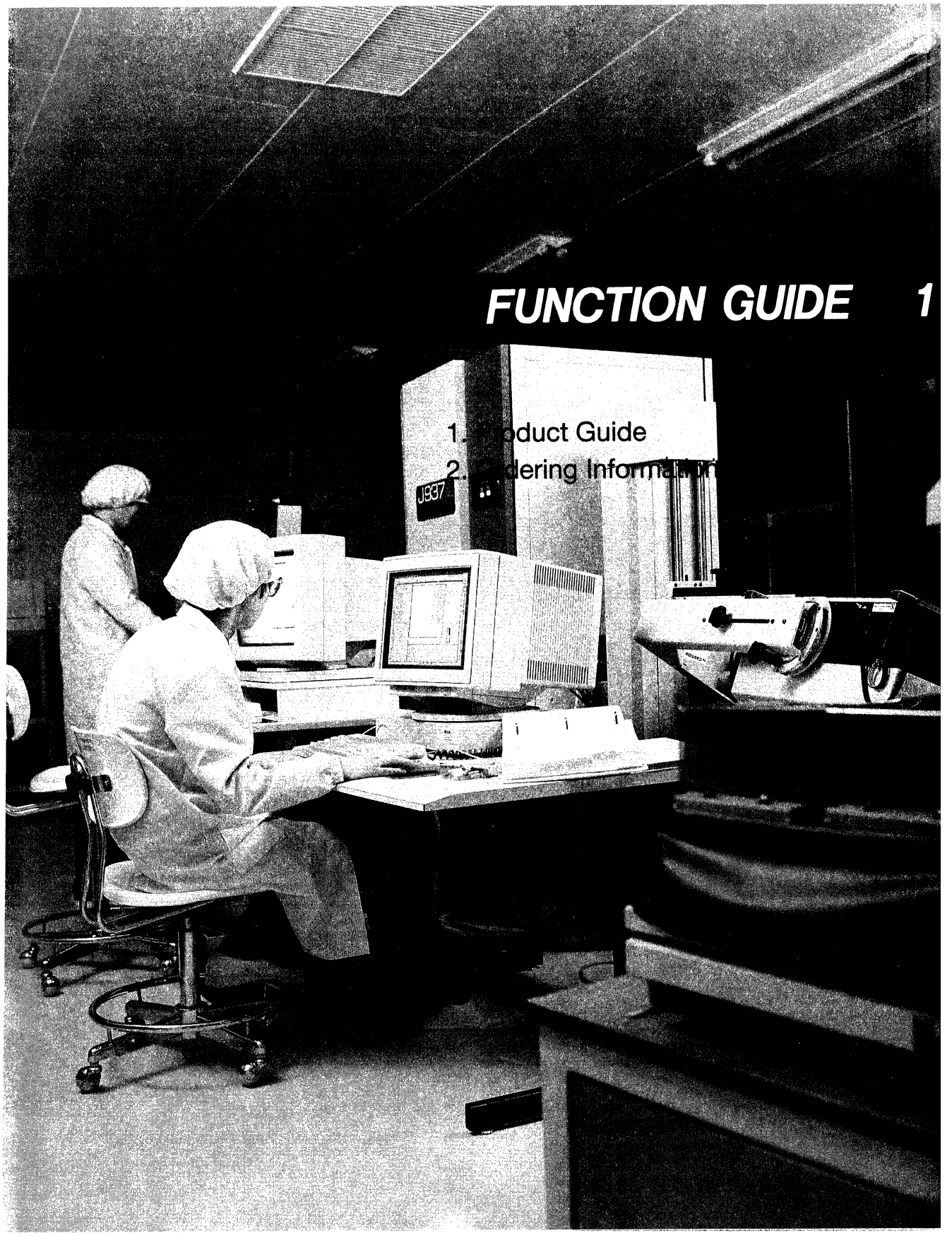


FUNCTION GUIDE 1

1. Product Guide
2. Ordering Information

1. Low Power SRAM (5V Operation)

Den.	Org.	Product No*	Op. Temp	Speed	Icc2/Isb1 (mA/μA)	Package
256K	32K x 8	KM62256CL KM62256CL-L	0~70°C	45/55/70	70/100 70/20	28-TSOP(I) Rev/Forward
		KM62256CLE KM62256CLE-L	-25~85°C	70/100	70/100 70/50	28-DIP
		KM62256CLI KM62256CLI-L	-40~85°C	70/100	70/100 70/50	28-SOP
512K	64K X 8	KM68512CL KM68512CL-L	0~70°C	45/55/70	70/100 70/20	32-TSOP(I) Forward
		KM68512CLI KM68512CLI-L	-40~85°C	70/100	70/100 70/50	32-SOP
1M	128K x 8	KM681000BL KM681000BL-L	0~70°C	55/70	70/100 70/20	
		KM681000BLE KM681000BLE-L	-25~85°C	70/100	70/100 70/50	32-TSOP(I) Rev/Forward
		KM681000BLI KM681000BLI-L	-40~85°C	70/100	70/100 70/50	32-DIP
		***KM681000CL ***KM681000CL-L	0~70°C	45/55	90/5 90/2	32-SOP
		***KM681000CLE ***KM681000CLE-L	-25~85°C	55/70	90/10 90/4	
		***KM681000CLI ***KM681000CLI-L	-40~85°C	55/70	90/10 90/4	
	64K x 16	KM6161000BL KM6161000BL-L KM6161000BLI KM6161000BLI-L	0~70°C -40~85°C	55/70 70/100	70/100 70/20 70/100 70/50	44-TSOP(II) Rev/Forward
4M	512K x 8	KM684000AL KM684000AL-L KM684000ALI KM684000ALI-L	0~70°C -40~85°C	55/70 70/100	70/100 70/20 70/100 70/50	32-TSOP(II) Rev/Forward 32-SOP 32-DIP

* : Refer to the ordering information for more detail description of each product
** : Preliminary
*** : Under development

2. Low Power SRAM (Low Vcc Operation)

Den.	Org. & Op Vcc	Product No*	Op. Temp	Speed	Icc2/Isb1 (mA/μA)	Package
256K	32K x 8 (Vcc=3.0~3.6V)	KM62V256CL-L KM62V256CLE-L KM62V256CLI-L	0~70°C -25~85°C -40~85°C	70/100 70/100 70/100	35/10 35/20 35/20	28-TSOP(I) Reverse 28-TSOP(I) Forward 28-SOP
	32K X 8 (Vcc=2.7~3.3V)	KM62U256CL-L KM62U256CLE-L KM62U256CLI-L	0~70°C -25~85°C -40~85°C	85/100 85/100 85/100	35/10 35/15 35/15	
512K	64K x 8 (Vcc=3.0~3.6V)	KM68V512AL-L** KM68V512ALE-L** KM68V512ALI-L**	0~70°C -25~85°C	70/100 70/100 70/100	40/10 40/20 40/20	32-TSOP(I) Forward 32-SOP
	64K x 8 (Vcc=2.7~3.3V)	KM68U512AL-L** KM68U512ALE-L** KM68U512ALI-L**	-40~85°C	100 100 100	45/10 45/15 45/15	
1M	128K x 8 (Vcc=3.0~3.6V)	KM68V1000BL KM68V1000BL-L KM68V1000BLE KM68V1000BLE-L KM68V1000BLI KM68V1000BLI-L	0~70°C -25~85°C -40~85°C	70/100 70/100 70/100 70/100 70/100 70/100	40/50 40/15 40/100 40/20 40/100 40/20	32-TSOP(I) Rev/Forward 32-SOP
	128K x 8 (Vcc=2.7~3.3V)	KM68U1000BL KM68U1000BL-L KM68U1000BLE KM68U1000BLE-L KM68U1000BLI KM68U1000BLI-L	0~70°C -25~85C -40~85°C	100 100 100 100 100 100	40/50 40/15 40/50 40/15 40/50 40/15	32-TSOP(I) Rev/Forward 32-SOP
	64K x 16 (Vcc=3.0~3.6V)	KM616V1000BL KM616V1000BL-L KM616V1000BLE KM616V1000BLE-L KM616V1000BLI KM616V1000BLI-L	0~70°C -25~85°C -40~85°C	70/100 70/100 85/100 85/100 85/100 85/100	65/50 65/15 65/100 65/20 65/100 65/20	44-TSOP(II) Reverse 44-TSOP(II) Forward
	64K x 16 (Vcc=2.7~3.3V)	KM616U1000BL KM616U1000BL-L KM616U1000BLE KM616U1000BLE-L KM616U1000BLI KM616U1000BLI-L	0~70°C -25~85°C -40~85°C	100 100 100 100 100 100	65/50 65/15 65/100 65/20 65/100 65/20	
4M	512K x 8 (Vcc=3.0~3.6V)	KM68V4000AL KM68V4000AL-L KM68V4000ALI KM68V4000ALI-L	0~70°C -40~85°C	70/100 70/100 70/100 70/100	90/100 90/20 90/100 90/50	32-TSOP(II) Rev/Forward 32-SOP

* : Refer to the ordering information for more detail description of each product

3. 5V CMOS Fast SRAM

Den.		Part Name	Org.	Speed(ns)	Tech.	Power Dissipation		Package
						Active Max(mA)	Standby Max(mA)	
256K		KM64258C	64Kx4	12/15/20	CMOS	150	2	28 DIP/SOJ
		KM68257C	32Kx8	12/15/20	CMOS	165	2	28 DIP/SOJ
1M		KM641001	256Kx4	20/25/35	CMOS	150	2	28 DIP/SOJ
	*	KM641001A	256Kx4	15/17/20	CMOS	190	10	28 SOJ
		KM641003	256Kx4	15/17/20	CMOS	170	10	32 SOJ
	*	KM641003A	256Kx4	12/15/17/20	CMOS	200	10	32 SOJ/TSOP(II)
		KM681001	128Kx8	20/25/35	CMOS	170	2	32 DIP/SOJ
	*	KM681001A	128Kx8	15/17/20	CMOS	190	10	32 SOJ
		KM681002	128Kx8	15/17/20	CMOS	170	10	32 SOJ
	*	KM681002A	128Kx8	12/15/17/20	CMOS	200	10	32 SOJ/TSOP(II)
		KM6161002	64Kx16	15/17/20	CMOS	230	10	44 SOJ
	*	KM6161002A	64Kx16	12/15/17/20	CMOS	220	10	44 SOJ/TSOP(II)
4M		KM644002/L	1Mx4	17/20/25	CMOS	170	10/0.5	32 SOJ
	†	KM644002A	1Mx4	12/15/20	CMOS	170	10/0.5	32 SOJ
		KM684002/L	512Kx8	17/20/25	CMOS	180	10/0.5	36 SOJ
	†	KM684002A	512Kx8	12/15/20	CMOS	200	10	36 SOJ
		KM6164002/L	256Kx16	20/25/35	CMOS	240	10	44 SOJ
	†	KM6164002A	256Kx16	12/15/20	CMOS	260	10	44 SOJ

4. 3.3V CMOS Fast SRAM

Den.		Part Name	Org.	Speed(ns)	Tech.	Power Dissipation		Package
						Active Max(mA)	Standby Max(mA)	
256K		KM68V257C	32Kx8	15/17/20	CMOS	90	0.1	28 DIP/SOJ
1M	*	KM64V1003A	256Kx4	12/15/17/20	CMOS	160	10	32 SOJ/TSOP(II)
	*	KM68V1002A	128Kx8	12/15/17/20	CMOS	170	10	32 SOJ/TSOP(II)
	*	KM616V1002A	64Kx16	12/15/17/20	CMOS	200	10	44 SOJ/TSOP(II)
4M	†	KM64V4002A	1Mx4	12/15/20	CMOS	140	10	32 SOJ
	†	KM68V4002A	512Kx8	12/15/20	CMOS	180	10	36 SOJ
	†	KM616V4002A	256Kx16	12/15/20	CMOS	230	10	44 SOJ

5. 5V BiCMOS Fast SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(mA)	
256K	KM64B261A	64K x 4	6/7/8	BiCMOS	160	20	28SOJ
	KM68B261A	32K x 8	6/7/8	BiCMOS	170	20	32SOJ
1M	KM64B1003	256K x 4	8/10/12/15	BiCMOS	165	10	32SOJ
	KM68B1002	128K x 8	8/10/12/15	BiCMOS	175	10	32SOJ
4M	*KM64B4002	1M x 4	12/13/15	BiCMOS	185	30	32SOJ
	*KM68B4002	512K x 8	12/13/15	BiCMOS	195	30	36SOJ
	*KM616B4002	256K x 16	12/13/15	BiCMOS	270	30	44SOJ

6. 3.3V BiCMOS Fast SRAM

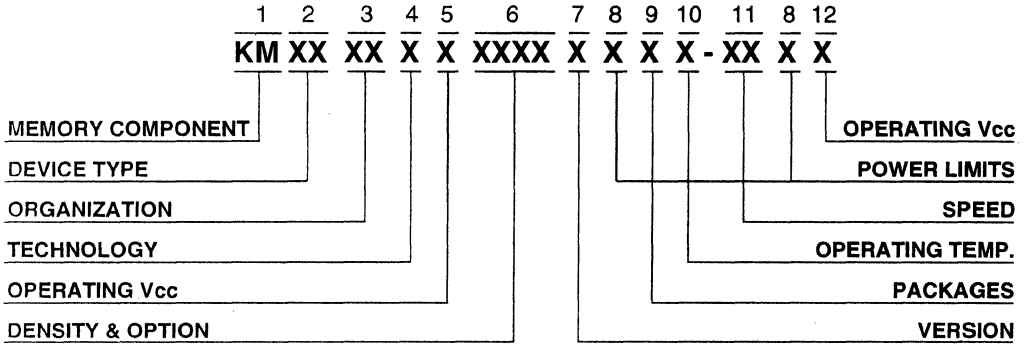
Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(mA)	
4M	*KM64BV4002	1M x 4	12/13/15	BiCMOS	160	30	32SOJ
	*KM68BV4002	512K x 8	12/13/15	BiCMOS	170	30	36SOJ
	*KM616BV4002	256K x 16	12/13/15	BiCMOS	240	30	44SOJ

7. Specialty SRAM

Den.	Org. & Op Vcc	Product No*	Technology	Speed(ns)	Icc2/Isb1 (mA/mA)	Package
1M	64K x 18,5V	KM718B86	BiCMOS	8/9/10/12	290/90	52-PLCC
	64K x 18,3.3V	KM718BV87	BiCMOS	9/10/12	270/80	52-PLCC
	64K x 18,5V	KM718B90	BiCMOS	8/9/10/12	290/90	52-PLCC
	64K x 18,3.3V	KM718BV87AT	BiCMOS	8/9/12	300/100	100-TQFP
	32K x 32,3.3V	KM732V588	CMOS	13/15/17	220/40	100-TQFP/QFP
	32K x 32,3.3V	KM732V589/L	CMOS	13/15/17	200/30	100-TQFP/QFP
	64K x 16,3.3V	KM716V689/L	CMOS	13/15/17	200/30	100-QFP
2M	64K x 36,3.3V	KM736V695/L	CMOS	7.5/8.6/10	TBD/TBD	100-QFP
	64K x 36,3.3V	KM736V687	CMOS	8/9/12	TBD/TBD	100-TQFP

* : Refer to the ordering information for more detail description of each product

1. Asynchronous SRAM Ordering Information



1. MEMORY COMPONENT

2. DEVICE TYPE

- 6 ..... SRAM(Async.)
- 7 ..... SRAM(ASSP)

3. ORGANIZATION

- 1 ..... x1 bit
- 4 ..... x4 bits
- 2 or 8 ..... x8 bits
- 9 ..... x9 bits
- 16 ..... x16 bits
- 32 ..... x32 bits

4. TECHNOLOGY

- BLANK ..... CMOS
- B ..... BiCMOS
- F ..... Full CMOS

5. OPERATING Vcc

- BLANK 5.0V
- V 3.3V
- U 3.0V
- S 2.5V
- T 2.0V

6. DENCITY & OPTION

- 64 ..... 64:64K Slow
- 256 ..... 256:256K Slow
- 257 ..... 257:256K Fast
- 258 ..... 258:256K Fast(with $\overline{OE}$)
- 512 ..... 512:512K Slow
- 1000 ..... 1000:1M Slow
- 1001 ..... 1001:1M Fast
- 1002 ..... 1002:1M Fast(Revolutionary)
- 1003 ..... 1003:1M Fast(Revolutionary, with $\overline{OE}$)
- 4000 ..... 4000:4M Slow
- 4002 ..... 4002:4M Fast(Revolutionary)

7. VERSION

- BLANK ..... First Rev.
- A ..... Second Rev.
- B ..... Third Rev.
- C ..... Forth Rev.

8. POWER LIMITS

- BLANK ..... High Power(Fast)
  In Full CMOS Low Power SRAM(Slow)
- L ..... Low Power
- L-L ..... Low Low Power

9. PACKAGES

- P ..... DIP
- G ..... SOP
- J ..... SOJ or PLCC
- T ..... TSOP(Standard)
- R ..... TSOP(Reverse)

10. OPERATING TEMP.

- BLANK ..... Commercial
- E ..... Extended
- I ..... Industrial

11. SPEED

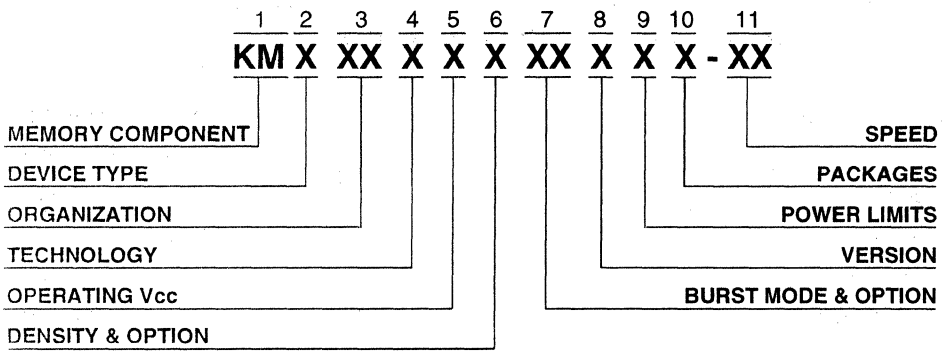
SLOW SRAM

- 4 ..... 45ns
- 5 ..... 55ns
- 7 ..... 70ns
- 8 ..... 85ns
- 10 ..... 100ns
- 12 ..... 120ns
- 15 ..... 150ns

FAST SRAM

- 6 ..... 6ns
- 7 ..... 7ns
- 8 ..... 8ns
- 10 ..... 10ns
- 12 ..... 12ns
- 15 ..... 15ns
- 17 ..... 17ns
- 20 ..... 20ns
- 25 ..... 25ns
- 30 ..... 30ns
- 35 ..... 35ns

2. Synchronous Burst SRAM Ordering Information



1. MEMORY COMPONENT

2. DEVICE TYPE

- 6 ..... SRAM(Async.)
- 7 ..... SRAM(ASSP)

3. ORGANIZATION

- 8 ..... x8 bits
- 9 ..... x9 bits
- 16 ..... x16 bits
- 18 ..... x18 bits
- 32 ..... x32 bits
- 36 ..... x36 bits
- 64 x64 bits

4. TECHNOLOGY

- BLANK ..... CMOS or AMOS
- B ..... BiCMOS

5. OPERATING Vcc

- BLANK 5.0V
- V 3.3V

6. DENSITY & OPTION

- BLANK ..... 32Kx9 or 64Kx18
- 5 ..... 32K Depth
- 6 ..... 64K Depth
- 7 ..... 128K Depth

7. BURST MODE & OPTION

- 86 ..... Binary Count
- 87 ..... Binary Count,Glue Logic
- 88 ..... Binary Count,Pipe Line
- 89 ..... $\overline{GW}$,$\overline{BW}$,Mode,$\overline{FT}$ and ZZ
- 90 ..... Linear Count
- 91 ..... Linear Count,Glue Logic
- 92 ..... Linear Count, Pipe Line
- 95 ..... $\overline{GW}$,$\overline{BW}$,Mode,$\overline{FT}$ and ZZ

8. VERSION

- BLANK ..... None
- A ..... First Rev.
- B ..... Second Rev.
- C ..... Third Rev.

9. POWER LIMITS

- BLANK ..... High Power
- L ..... Low Power

10. PACKAGES

- H ..... BGA
- T ..... TSOP /TQFP
- J ..... PLCC
- G ..... QFP

11. SPEED

Sync Burst (CLOCK ACCESS TIME)

- 8 ..... 8ns
- 9 ..... 9 ns
- 10 ..... 10 ns
- 12 ..... 12 ns
- 15 ..... 15 ns
- 20 ..... 20 ns

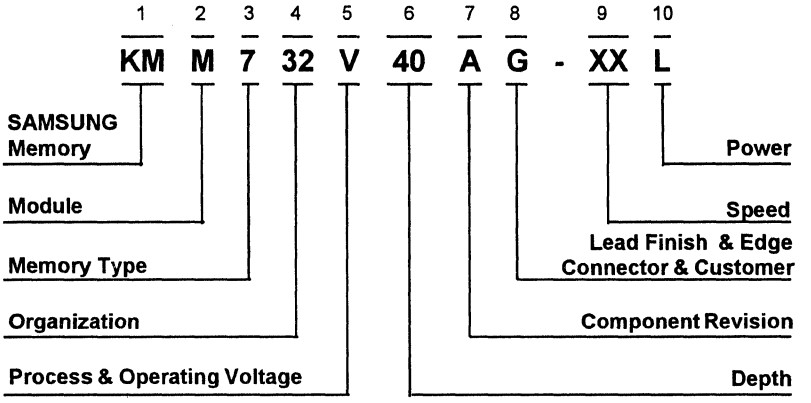
Sync Pipe & Burst (CLOCK CYCLE TIME)

- 7 ..... 133MHz
- 8 ..... 116MHz
- 10 ..... 100MHz
- 13 ..... 75 MHZ
- 15 ..... 66 MHZ
- 17 ..... 60 MHZ
- 20 ..... 50 MHZ

KM732V589 (Pipelined / Non-Pipelined)

- 10 ..... 100MHz,6ns/40MHz,17ns
- 15 ..... 66MHz,8ns/40MHz,17ns
- 20 ..... 66MHz,8ns/50MHz,15ns
- 25 ..... 60MHz,9ns/40MHz,17ns

3. Synchronous SRAM Modul Ordering Information



1. SAMSUNG Memory

2. Module

3. Memory Type
- 1 : FLASH
- 2 : Mask ROM
- 3 : DRAM DIMM
- 4 : DRAM SIP
- 5 : DRAM SIMM
- 6 : Async SRAM
- 7 : Sync SRAM
- 8 : M-ROM and SRAM
- 9 : VRAM

4. Organization
- 8 : x8 bit
- 9 : x9 bit
- 16 : x16 bit
- 18 : x18 bit
- 32 : x32 bit
- 44 : x44 bit
- 64 : x64 bit
- 72 : x72 bit

5. Process & Operating Voltage
- Blank : CMOS 5 V
- V : CMOS 3.3 V
- B : BiCMOS 5 V

6. Depth
- 32.33, 34, 35, 36 ..... : 32K
- 64,65, 66, 67, 68 ..... : 64K
- 128,129, 130, 131 ..... : 128K
- 512,513, 514, 515 ..... : 512K
- 544, 545, 546 ..... : 544K

7. Component Revision
- Blank : Original
- A : First Revision
- B : Second Revision

8. Lead Finish & Edge Connector & Customer
- Blank : Solder DIMM
- G : Gold DIMM

9. Speed
- 10 : 10, 100 ns
- 12 : 12,120ns
- 13 : 13ns
- 15 : 15ns
- 17 : 17ns
- 20 : 20ns
- 25 : 25ns
- 30 : 30ns
- 35 : 35ns
- 55 : 55ns
- 70 : 70ns
- 80 : 80ns
- 90 : 90ns

10. Power Dissipation.
- Blank : Normal Power
- L : Low Power

NOTES

SRAM DATA SHEETS 2

- Low Power SRAMs
- Low Voltage SRAMs
- High Speed SRAM
- Synchronous SRAM

Low Power SRAMs (5.0V)

- KM62256C Family	32K × 8	Commercial, Extended, Industrial Products
- KM68512A Family	64K × 8	Commercial, Industrial Products
- KM681000B Family	128K × 8	Commercial, Extended, Industrial Products
- KM681000C Family	128K × 8	Commercial, Industrial Products
- KM6161000B Family	64K × 16	Commercial, Industrial Products
- KM684000A Family	512K × 8	Commercial, Industrial Products

32Kx8 bit Low Power CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.7 uM CMOS
- Organization : 32K x 8
- Power Supply Voltage : Single 5V +/- 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-DIP, 28-SOP, 28-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

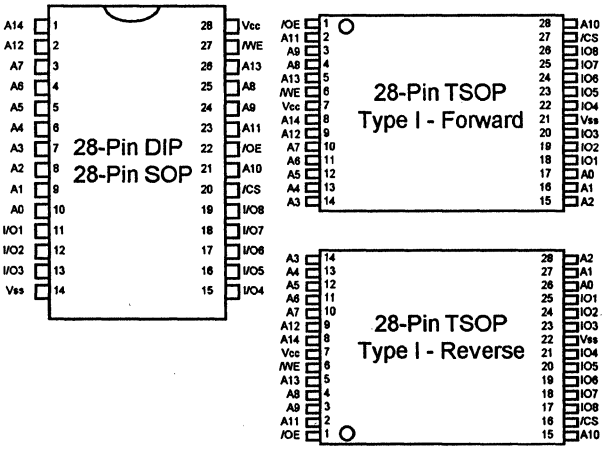
The KM62256C family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operations with low data retention current.

PRODUCT FAMILY

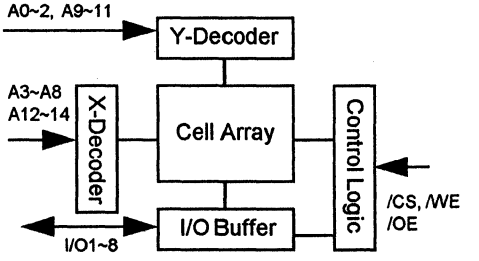
Product Family	Operating Temperature	Speed	PKG Type	Power Dissipation	
				Standby(Isb1, Max)	Operating(Icc2)
KM62256CL	Commercial	45*/55/70ns	28-DIP, 28-SOP	100uA	70mA
KM62256CL-L	(0~70 °C)		28-TSOP(I) R/F	20uA	
KM62256CLE	Extended	70/100ns	28-SOP	100uA	
KM62256CLE-L	(-25~ 85 °C)		28-TSOP(I) R/F	50uA	
KM62256CLI	Industrial	70/100ns	28-SOP	100uA	
KM62256CLI-L	(-40~85 °C)		28-TSOP(I) R/F	50uA	

* measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Pin Name	Function
A0~A14	Address Inputs
/WE	Write Enable Input
/CS	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power
Vss	Groud

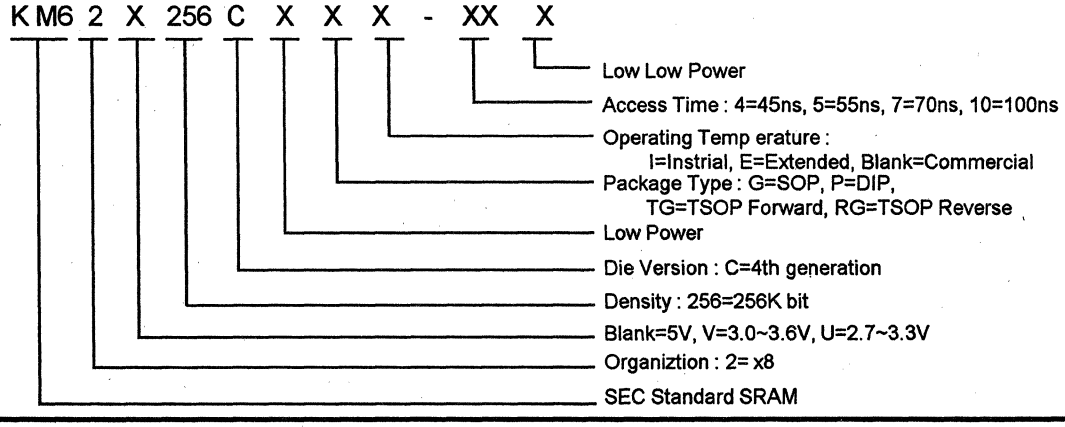
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM62256CLP-4	28-DIP, 45ns, L-pwr	KM62256CLGE-7	28-SOP, 70ns, L-pwr	KM62256CLGI-7	28-SOP, 70ns, L-pwr
KM62256CLP-4L	28-DIP, 45ns, , LL-pwr	KM62256CLGE-7L	28-SOP, 70ns, LL-pwr	KM62256CLGI-7L	28-SOP, 70ns, LL-pwr
KM62256CLP-5	28-DIP, 55ns, , L-pwr	KM62256CLGE-10	28-SOP, 100ns, L-pwr	KM62256CLGI-10	28-SOP, 100ns, L-pwr
KM62256CLP-5L	28-DIP, 55ns, LL-pwr	KM62256CLGE-10L	28-SOP, 100ns, LL-pwr	KM62256CLGI-10L	28-SOP, 100ns, LL-pwr
KM62256CLP-7	28-DIP, 70ns, , L-pwr	KM62256CLTGE-7	28-TSOP F, 70ns, L-pwr	KM62256CLTGI-7	28-TSOP F, 70ns, L-pwr
KM62256CLP-7L	28-DIP, 70ns, LL-pwr	KM62256CLTGE-7L	28-TSOP F, 70ns, LL-pwr	KM62256CLTGI-7L	28-TSOP F, 70ns, LL-pwr
KM62256CLG-4	28-SOP, 45ns, L-pwr	KM62256CLTGE-10	28-TSOP F, 100ns, L-pwr	KM62256CLTGI-10	28-TSOP F, 100ns, L-pwr
KM62256CLG-4L	28-SOP, 45ns, LL-pwr	KM62256CLTGE-10L	28-TSOP F, 100ns, LL-pwr	KM62256CLTGI-10L	28-TSOP F, 100ns, LL-pwr
KM62256CLG-5	28-SOP, 55ns, L-pwr	KM62256CLRGE-7	28-TSOP R, 70ns, L-pwr	KM62256CLRGI-7	28-TSOP R, 70ns, L-pwr
KM62256CLG-5L	28-SOP, 55ns, LL-pwr	KM62256CLRGE-7L	28-TSOP R, 70ns, LL-pwr	KM62256CLRGI-7L	28-TSOP R, 70ns, LL-pwr
KM62256CLG-7	28-SOP, 70ns, L-pwr	KM62256CLRGE-10	28-TSOP R, 100ns, L-pwr	KM62256CLRGI-10	28-TSOP R, 100ns, L-pwr
KM62256CLG-7L	28-SOP, 70ns, LL-pwr	KM62256CLRGE-10L	28-TSOP R, 100ns, LL-pwr	KM62256CLRGI-10L	28-TSOP R, 100ns, LL-pwr
KM62256CLTG -4	28-TSOP F, 45ns, L-pwr				
KM62256CLTG -4L	28-TSOP F, 45ns, LL-pwr				
KM62256CLTG-5	28-TSOP F, 55ns, L-pwr				
KM62256CLTG-5L	28-TSOP F, 55ns, LL-pwr				
KM62256CLTG-7	28-TSOP F, 70ns, L-pwr				
KM62256CLTG-7L	28-TSOP F, 70ns, LL-pwr				
KM62256CLRG-4	28-TSOP R, 45ns, L-pwr				
KM62256CLRG-4L	28-TSOP R, 45ns, LL-pwr				
KM62256CLRG-5	28-TSOP R, 55ns, L-pwr				
KM62256CLRG-5L	28-TSOP R, 55ns, LL-pwr				
KM62256CLRG-7	28-TSOP R, 70ns, L-pwr				
KM62256CLRG-7L	28-TSOP R, 70ns, LL-pwr				

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM62256CL/L-L
		-25 to 85	°C	KM62256CLE/LE-L
		-40 to 85	°C	KM62256CLI/LI-L
Soldering temperature and time	Tsolder	260 °C , 10sec(Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.5	V
Input low voltage	Vil	-0.5***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C , unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤50ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

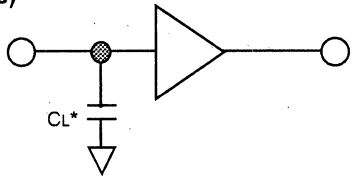
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS=Vih or /WE=Vil Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS=Vil, Vin=Vih or Vil, Iio=0mA		-	7	15***	mA
Average operating current		Icc1	Cycle time=1uS 100% duty /CS≤0.2V, Vil≤0.2V, Vin≥Vcc-0.2V, Iio=0mA		-	-	7****	mA
		Icc2	Min cycle, 100% duty /CS=Vil, Iio=0mA		-	-	70	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	1****	mA
Standby Current (CMOS)	KM62256CL	Isb1	/CS≥Vcc-0.2V Vin≤0.2V or Vin≥Vcc-0.2V	L	-	2	100	uA
	KM62256CL-I			LL	-	1	20	uA
	KM62256CLE			L	-	-	100	uA
	KM62256CLE-L			LL	-	-	50	uA
	KM62256CLI			L	-	-	100	uA
	KM62256CLI-L			LL	-	-	50	uA

* 1) Commercial Product : Ta=0 to 70 °C , Vcc=5V+/-10%, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C , Vcc=5V+/-10%, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C , Vcc=5V+/-10%, unless otherwise specified
** Ta=25 °C
*** 20mA for Extened and Industrial Products
**** 10mA for Extended and Industrial Products
*****2mA for Extended and Industrial Products

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	



* Including scope and jig capacitance

* See test condition of DC and AC Operating characteristics
** Test load for 45ns Commercial Products

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62256CL/L-L	0~70 °C	5V +/- 10%	45*/55/70ns	Commercial
KM62256CLE/LE-L	-25~85 °C	5V +/- 10%	70/100ns	Extended
KM62256CLI/LI-L	-40~85 °C	5V +/- 10%	70/100ns	Industrial

* parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins								Units
			45ns*		55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	100	ns
	Chip select to ouput	tCO	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	30	0	35	ns
	Output disable to high-Z output	tOHZ	0	20	0	20	0	30	0	35	ns
	Output hold from address change	tOH	5	-	5	-	5	-	5	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	50	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	ns

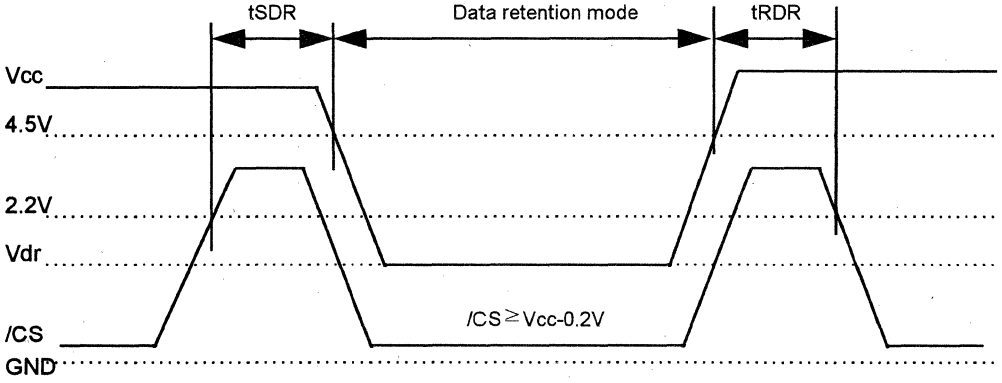
* All the parameters are measured with 30pF test load

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS≥Vcc-0.2V		2.0	-	5.5	V
Data retention current	Idr	KM62256CL	Vcc=3.0V	L-Ver	-	1	50	uA
		KM62256CL-L	/CS≥Vcc-0.2V	LL-Ver	-	0.5	10	
		KM62256CLE		L-Ver	-	-	50	
		KM62256CLE-L		LL-Ver	-	-	25	
		KM62256CLI		L-Ver	-	-	50	
		KM62256CLI-L		LL-Ver	-	-	25	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C

DTA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

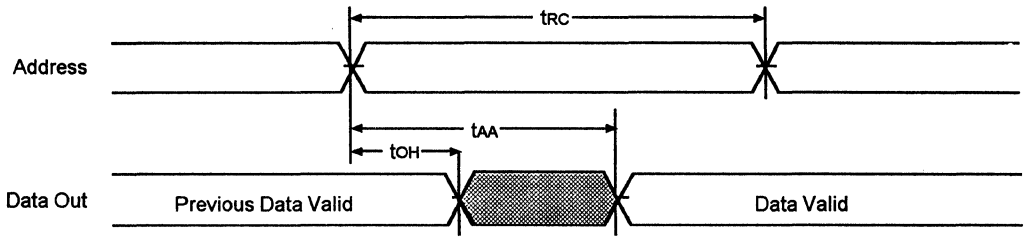
/CS	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	Ouput Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care

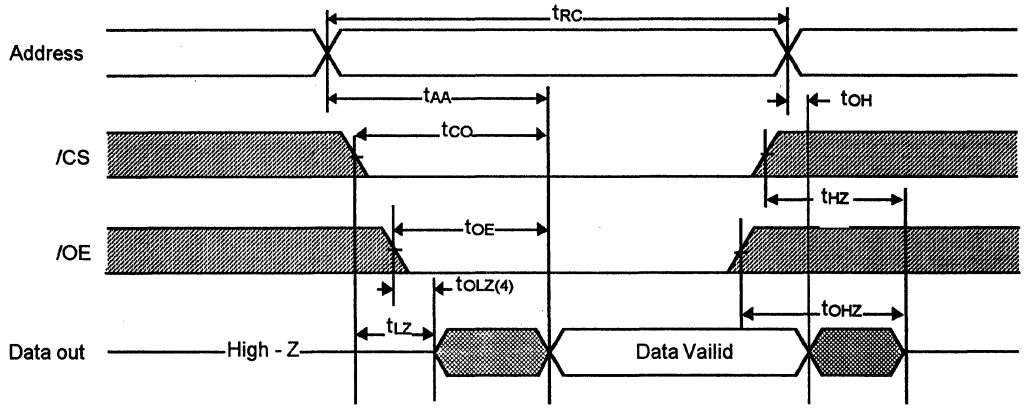
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih)



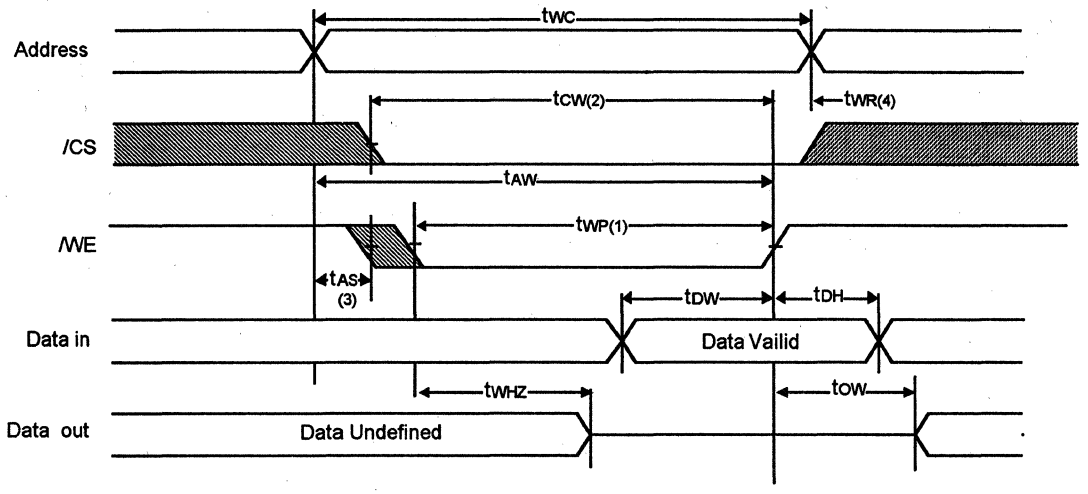
TIMING WAVEFORM OF READ CYCLE (/WE= VIH)



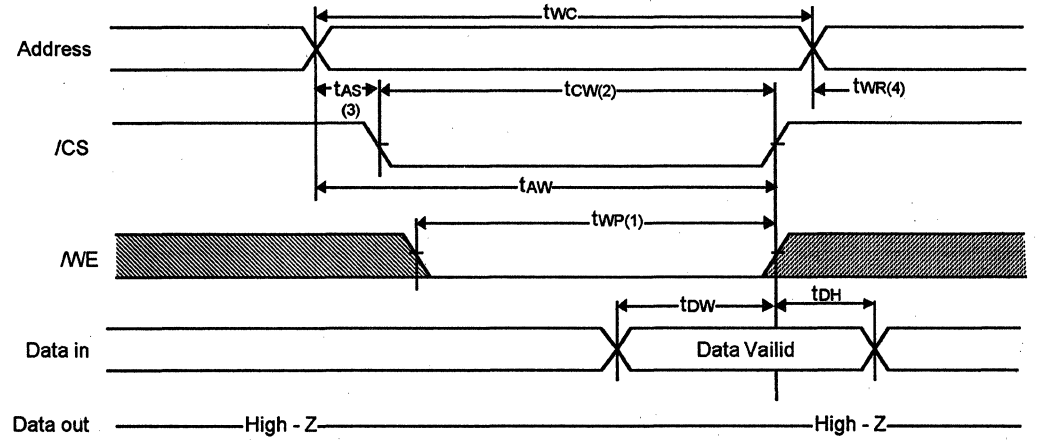
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.)both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



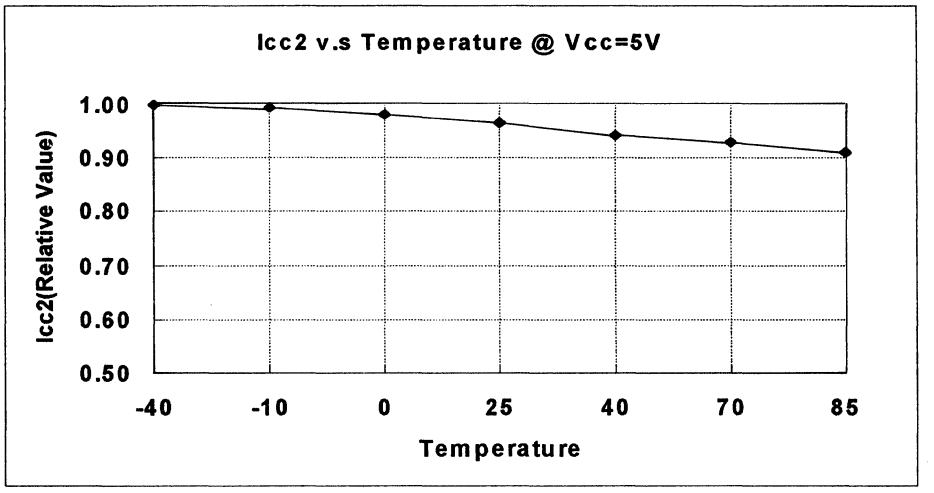
Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CSand low /WE. A write begins at the latest transition among /CS going low and WE going low : A write end at the earliest transition among /CSgoing high and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS,or /WE going high.

TECHNICAL INFORMATION

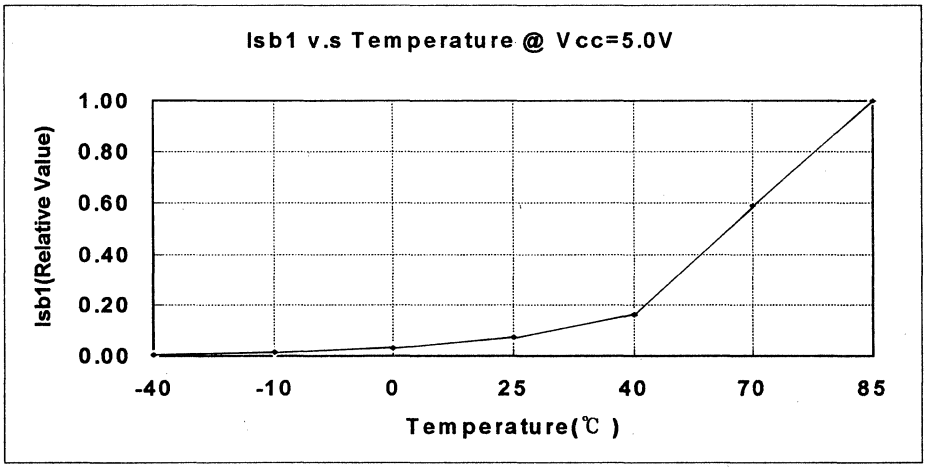
1) Icc2 characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and -40°C temperature. The basic relative value of Icc2 at that condition is set into 1.



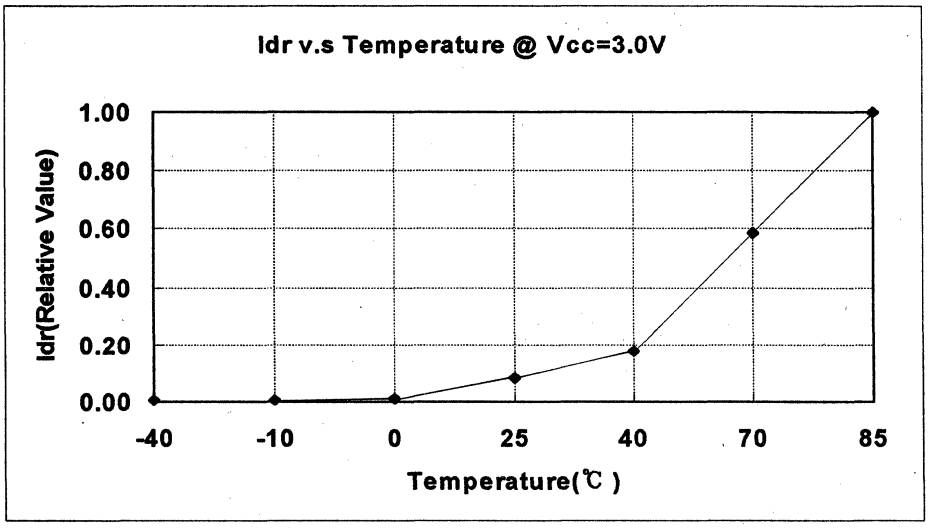
2) Isb1(CMOS Level Stanby Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and 85°C temperature. The basic relative value of Isb1 at that condition is set into 1.



3) Idr(Data Retention Current) characteristics by temperature variation

All the values in this graph is depicted by the relative value with the maximum value measured at Vdr=3.0V and 85°C temperature. The basic relative value of Idr at that condition is set into 1.



64Kx8 bit Low Power CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.6 um CMOS
- Organization : 64K x8
- Power Supply Voltage : Single 5V +/- 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(I)-Forward

GENERAL DESCRIPTION

The KM68512A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ragnges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

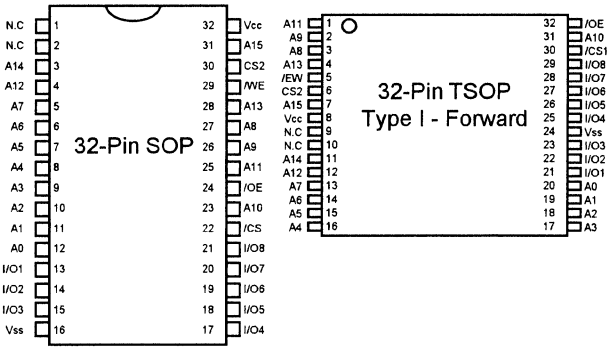
2

PRODUCT FAMILY

Product Family	Operating Temperature	Speed	PKG Type	Power Dissipation	
				Standby(Isb1, Max)	Operating(Icc2)
KM68512AL	Commercial (0~70 °C)	45*/55/70ns	32-SOP	100uA	70mA
KM68512AL-L			32-TSOP(I) F	20uA	
KM68512ALI	Industrial (-40~85 °C)	70/100ns	32-SOP	100uA	
KM68512ALI-L			32-TSOP(I) F	50uA	

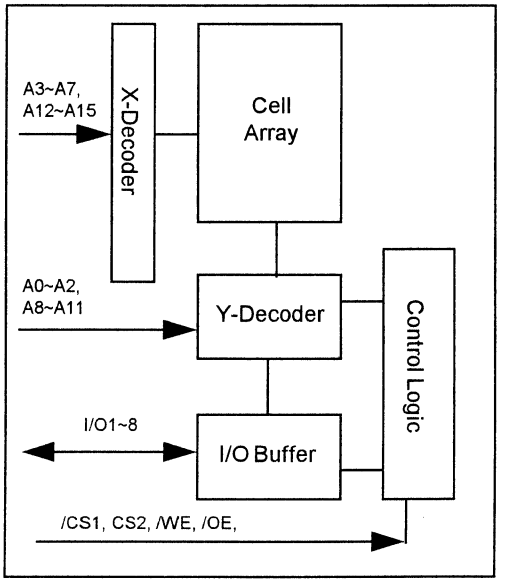
* measured with 30pF test load

PIN DESCRIPTION



Name	Function	Name	Function
A0~A15	Address Inputs	Vcc	Power
/WE	Write Enable Input	Vss	Ground
/CS1, CS2	Chip Select Input	N.C	No Connection
/OE	Output Enable Input		
I/O1~I/O16	Data Input/Output		

FUNCTIONAL BLOCK DIAGRAM

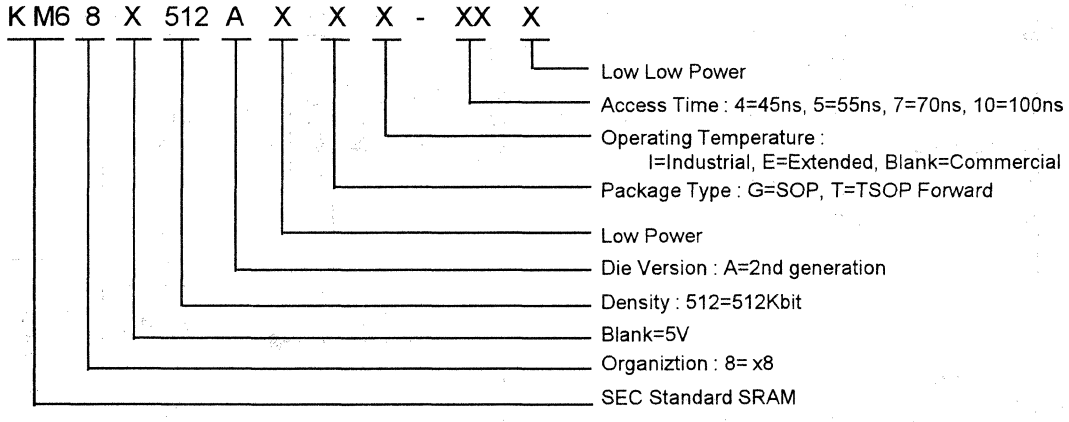


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**
KM68512ALG-4	32-SOP, 45ns, L-pwr	KM68512ALGI-7	32-SOP, 70ns, L-pwr
KM68512ALG-4L	32-SOP, 45ns, LL-pwr	KM68512ALGI-7L	32-SOP, 70ns, LL-pwr
KM68512ALG-5	32-SOP, 55ns, L-pwr	KM68512ALGI-10	32-SOP, 100ns, L-pwr
KM68512ALG-5L	32-SOP, 55ns, LL-pwr	KM68512ALGI-10L	32-SOP, 100ns, LL-pwr
KM68512ALG-7	32-SOP, 70ns, L-pwr	KM68512ALTI-7	32-TSOP F, 70ns, L-pwr
KM68512ALG-7L	32-SOP, 70ns, LL-pwr	KM68512ALTI-7L	32-TSOP F, 70ns, LL-pwr
KM68512ALT-4	32-TSOP F, 45ns, L-pwr	KM68512ALTI-10	32-TSOP F, 100ns, L-pwr
KM68512ALT-4L	32-TSOP F, 45ns, LL-pwr	KM68512ALTI-10L	32-TSOP F, 100ns, LL-pwr
KM68512ALT-5	32-TSOP F, 55ns, L-pwr		
KM68512ALT-5L	32-TSOP F, 55ns, LL-pwr		
KM68512ALT-7	32-TSOP F, 70ns, L-pwr		
KM68512ALT-7L	32-TSOP F, 70ns, LL-pwr		

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM68512AL/L-L
		-40 to 85	°C	KM68512ALI/LI-L
Soldering temperature and time	Tsolder	260 °C,10sec(Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.5	V
Input low voltage	Vil	-0.5***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤50ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

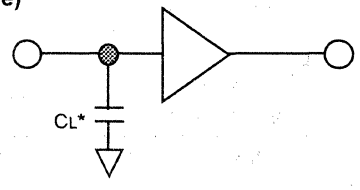
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS1=Vih or CS2=Vil or /WE=Vil, Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current Average operating current		Icc	/CS1=Vil, CS2=Vih, Vin=Vih or Vil, Iio=0mA		-	7	15	mA
		Icc1	Cycle time=1uS 100% duty /CS1≤0.2V, CS2≥Vcc-0.2V Vil≤0.2V, Vih≥Vcc-0.2V, Iio=0mA		-	-	10	mA
		Icc2	Min cycle, 100% duty /CS1=Vil, CS2=Vih, Iio=0mA		-	-	70	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS1=Vih, CS2=Vil		-	-	3	mA
Standby Current (CMOS)	KM68512AL/L-L	Isb1	/CS1≥Vcc-0.2V and CS2≥Vcc-0.2V or CS2≤0.2V Vin≤0.2V or Vin≥Vcc-0.2V	L	-	2	100	uA
				LL	-	1	20	uA
	KM68512ALI/LI-L			L	-	2	100	uA
				LL		1	50	uA

* 1) Commercial Product : Ta=0 to 70 °C , Vcc=5V+/-10%, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , Vcc=5V+/-10%, unless otherwise specified
** Ta=25 °C

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rise and fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics
** Test load for 45ns Commercial Product

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68512AL/L-L	0~70 °C	5V +/- 10%	45*/55/70ns	Commercial
KM68512ALI/LI-L	-40~85 °C	5V +/- 10%	70/100ns	Industrial

* parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins								Units
			45ns*		55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	ns

* All the parameters are measured with 30pF test load

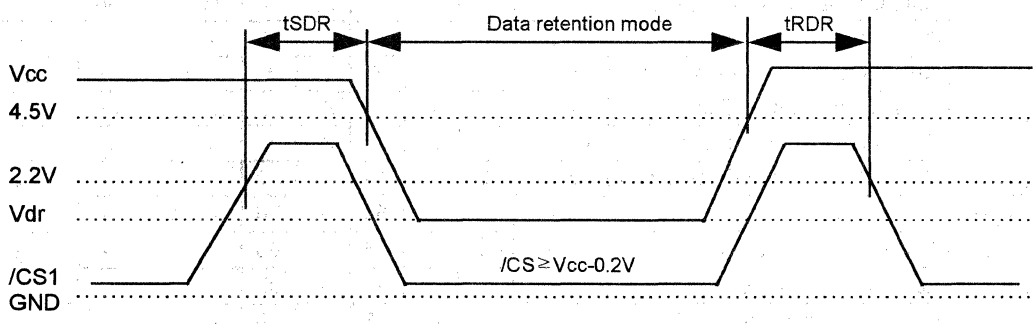
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		***/CS ≥ Vcc-0.2V		2.0	-	5.5	V
Data retention current	Idr	KM68512AL/L-L	Vcc=3.0V /CS ≥ Vcc-0.2V	L-Ver	-	1	50	uA
				LL-Ver	-	0.5	10	
		KM68512ALI/LI-L		L-Ver	-	-	50	
				LL-Ver	-	-	25	
Data retention set-up time	tSDR	See data retention waveform			0	-	-	ms
Recovery time	tRDR				5	-	-	

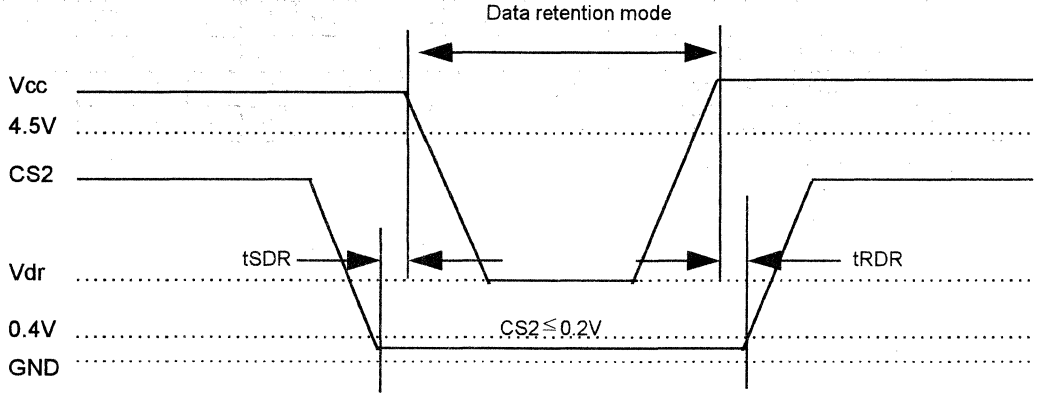
* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C
*** /CS1 ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V(/CS1 controlled) or CS2 ≤ 0.2V(CS2 controlled)

DATA RETENTION TIMING DIAGRAM

1) /CS1 Controlled



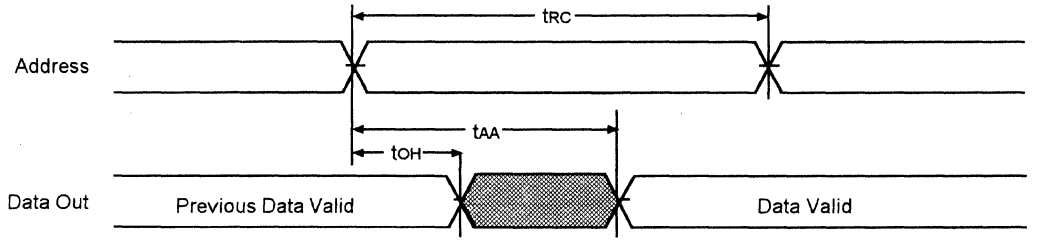
2) CS2 Controlled



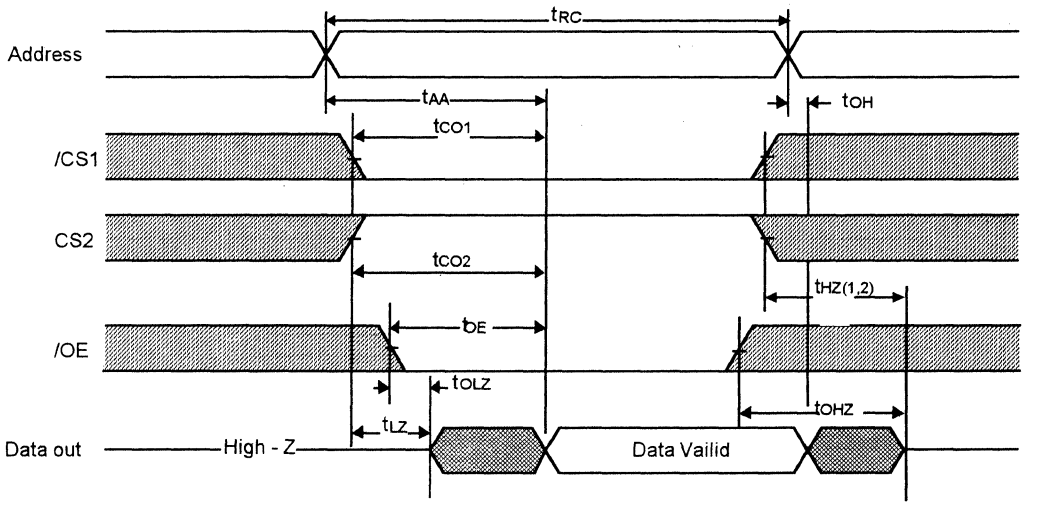
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, CS2=/WE=Vih)



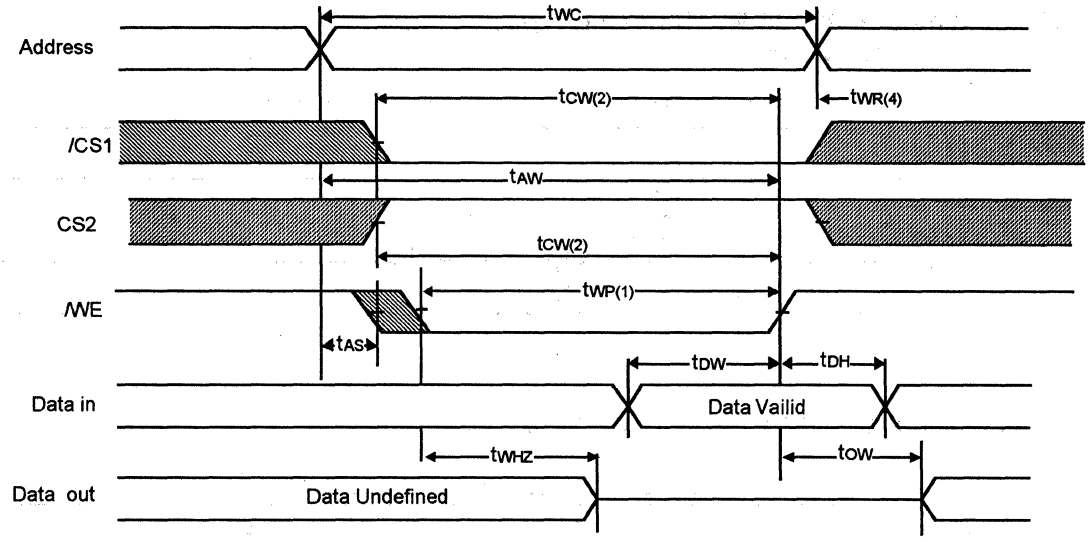
TIMING WAVE FORM OF READ CYCLE(2) (/WE= VIH)



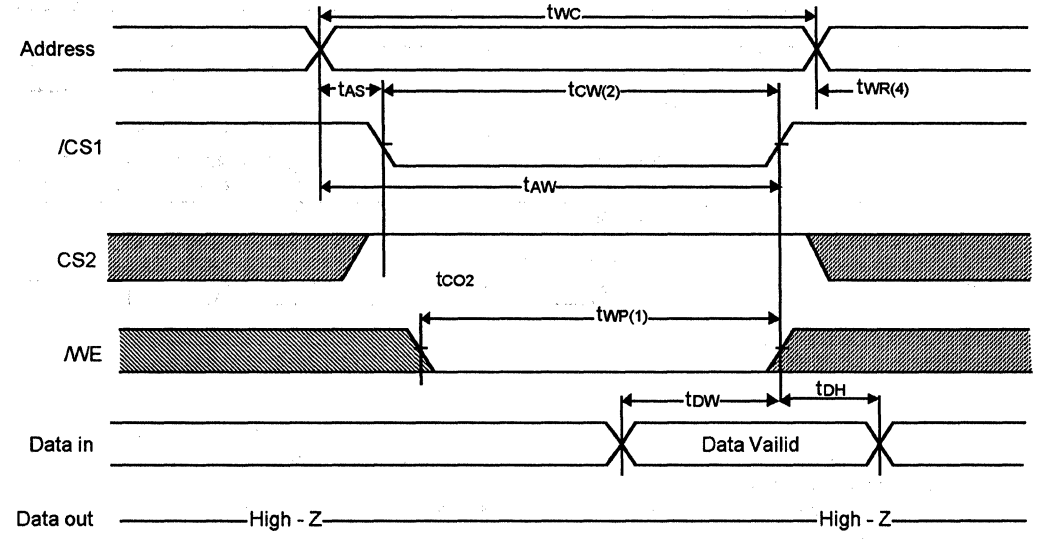
Notes(Read Cycle)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max) is less than tLZ(Min) both for a given device and device to device interconnection.

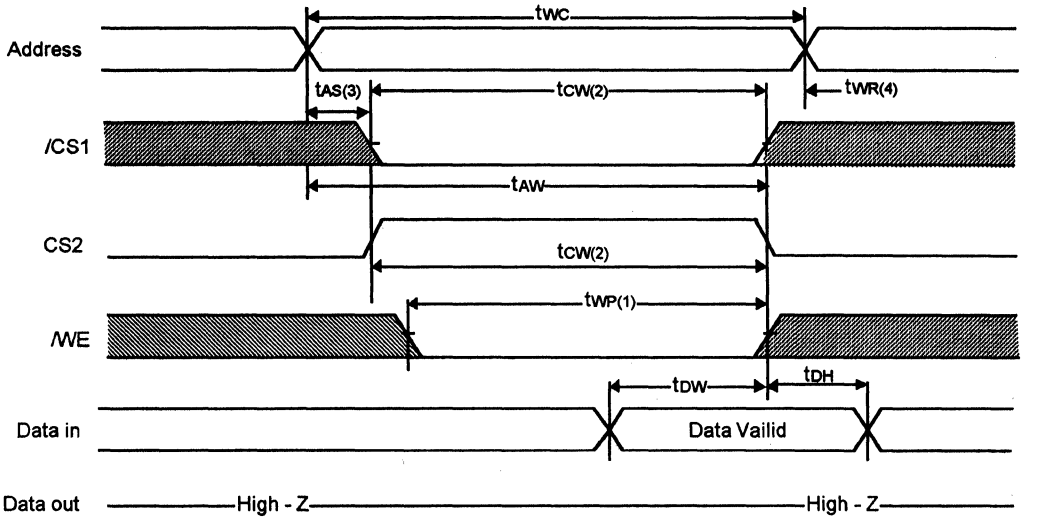
TIMING WAVE FORM OF WRITE CYCLE(1) (/WE Controlled)



TIMING WAVE FORM OF WRITE CYCLE(2) (/CS1 Controlled)



TIMING WAVE FORM OF WRITE CYCLE(3)(CS2 Controlled)



Notes(Write Cycle)

1. A write occurs during the overlap of a low /CS1, a high CS2 and a low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low. A write ends at the earliest transition among /CS1 going high, CS2 going low and /WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends at/CS1, or /WE going high, tWR2 applied in case a write ends at CS2 going to low.

FUNCTIONAL DESCRIPTION

/CS1	CS2	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	Isb, Isb1
X	L	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	H	Ouput Disable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

128Kx8 bit High Speed CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.6 um CMOS
- Organization : 128K x 8
- Power Supply Voltage : Single 5V +/- 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard

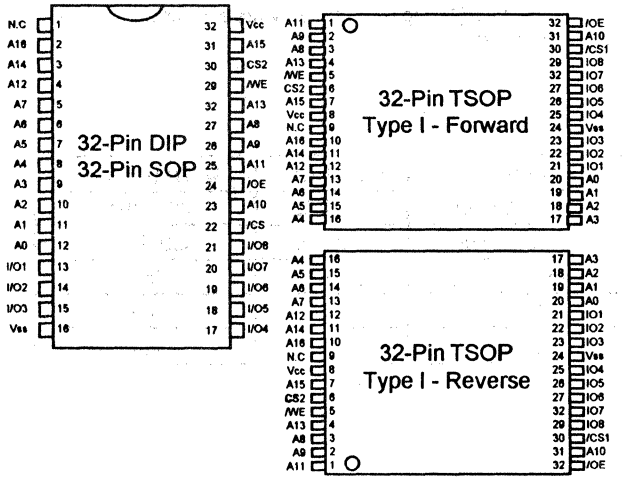
GENERAL DESCRIPTION

The KM681000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operations with low data retention current.

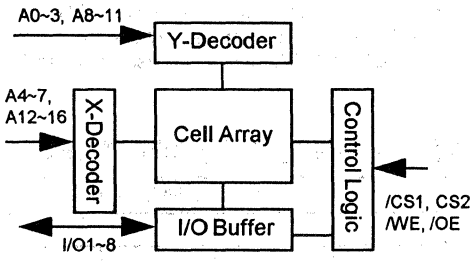
PRODUCT FAMILY

Product Family	Operating Temperature	Speed	PKG Type	Power Dissipation	
				Standby(Isb1, Max)	Operating(Icc2)
KM681000BL	Commercial (0~70 °C)	55/70ns	32-DIP, 32-SOP	100uA	70mA
KM681000BL-L			32-TSOP(I) R/F	20uA	
KM681000BLE	Extended (-25~ 85 °C)	70/100ns	32-SOP	100uA	
KM681000BLE-L			32-TSOP(I) R/F	50uA	
KM681000BLI	Industrial (-40~85 °C)	70/100ns	32-SOP	100uA	
KM681000BLI-L			32-TSOP(I) R/F	50uA	

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



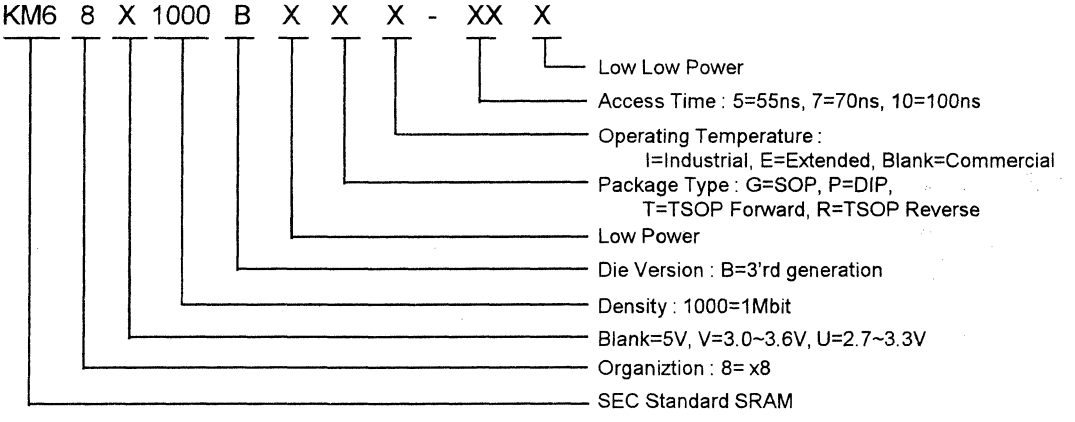
Pin Name	Function
A0~A16	Address Inputs
/WE	Write Enable Input
/CS1,CS2	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power
Vss	Ground
N.C.	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
KM681000BLP-5	32-DIP, 55ns, , L-pwr	KM681000BLGE-7	32-SOP, 70ns, L-pwr	KM681000BLGI-7	32-SOP, 70ns, L-pwr
KM681000BLP-5L	32-DIP, 55ns, LL-pwr	KM681000BLGE-7L	32-SOP, 70ns, LL-pwr	KM681000BLGI-7L	32-SOP, 70ns, LL-pwr
KM681000BLP-7	32-DIP, 70ns, , L-pwr	KM681000BLGE-10	32-SOP, 100ns, L-pwr	KM681000BLGI-10	32-SOP, 100ns, L-pwr
KM681000BLP-7L	32-DIP, 70ns, LL-pwr	KM681000BLGE-10L	32-SOP, 100ns, LL-pwr	KM681000BLGI-10L	32-SOP, 100ns, LL-pwr
KM681000BLG-5	32-SOP, 55ns, L-pwr	KM681000BLTE-7	32-TSOP F, 70ns, L-pwr	KM681000BLTI-7	32-TSOP F, 70ns, L-pwr
KM681000BLG-5L	32-SOP, 55ns, LL-pwr	KM681000BLTE-7L	32-TSOP F, 70ns, LL-pwr	KM681000BLTI-7L	32-TSOP F, 70ns, LL-pwr
KM681000BLG-7	32-SOP, 70ns, L-pwr	KM681000BLTE-10	32-TSOP F, 100ns, L-pwr	KM681000BLTI-10	32-TSOP F, 100ns, L-pwr
KM681000BLG-7L	32-SOP, 70ns, LL-pwr	KM681000BLTE-10L	32-TSOP F, 100ns, LL-pwr	KM681000BLTI-10L	32-TSOP F, 100ns, LL-pwr
KM681000BLT-5	32-TSOP F, 55ns, L-pwr	KM681000BLRE-7	32-TSOP R, 70ns, L-pwr	KM681000BLRI-7	32-TSOP R, 70ns, L-pwr
KM681000BLT-5L	32-TSOP F, 55ns, LL-pwr	KM681000BLRE-7L	32-TSOP R, 70ns, LL-pwr	KM681000BLR-I7L	32-TSOP R, 70ns, LL-pwr
KM681000BLT-7	32-TSOP F, 70ns, L-pwr	KM681000BLRE-10	32-TSOP R, 100ns, L-pwr	KM681000BLRI-10	32-TSOP R, 100ns, L-pwr
KM681000BLT-7L	32-TSOP F, 70ns, LL-pwr	KM681000BLRE-10L	32-TSOP R, 100ns, LL-pwr	KM681000BLRI-10L	32-TSOP R, 100ns, LL-pwr
KM681000BLR-5	32-TSOP R, 55ns, L-pwr				
KM681000BLR-5L	32-TSOP R, 55ns, LL-pwr				
KM681000BLR-7	32-TSOP R, 70ns, L-pwr				
KM681000BLR-7L	32-TSOP R, 70ns, LL-pwr				

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM681000BL/L-L
		-25 to 85	°C	KM681000BLE/LE-L
		-40 to 85	°C	KM681000BLI/LI-L
Soldering temperature and time	Tsolder	260 °C , 10sec(Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.5	V
Input low voltage	Vil	-0.5***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

** Ta=25 °C

*** Vil(min)=-3.0V for ≤50ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

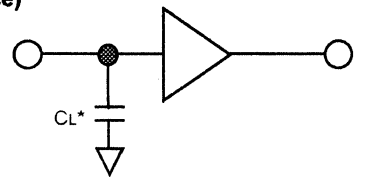
Item		Symbol	Test Conditions*		Min	Typ	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS1=Vih or CS2=Vil or /WE=Vil, Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS1=Vil, CS2=Vih Vin=Vih or Vil, Iio=0mA		-	7	15**	mA
Average operating current		Icc1	Cycle time=1uS 100% duty /CS1≤0.2V, CS2≥Vcc-0.2V		-	-	10***	mA
		Icc2	Iio=0mA,/CS1=Vil, CS2=Vih Min cycle, 100% duty		-	-	70	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS1=Vih, CS2=Vil		-	-	3	mA
Standby Current (CMOS)	KM681000BL	Isb1	/CS1≥Vcc-0.2V CS2≥Vcc-0.2V or CS2≤0.2V	L(Low Power)	-	-	100	uA
	KM681000BL-L			LL(L Low Power)	-	-	20	uA
	KM681000BLE			L(Low Power)	-	-	100	uA
	KM681000BLE-L			LL(L Low Power)	-	-	50	uA
	KM681000BLI			L(Low Power)	-	-	100	uA
	KM681000BLI-L			LL(L Low Power)	-	-	50	uA

* 1) Commercial Product : Ta=0 to 70 °C, Vcc=5V+/-10%, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, Vcc=5V+/-10%, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, Vcc=5V+/-10%, unless otherwise specified
** 20mA for Extened and Industrial Products
***15mA for Extended and Industrial Products

A.C CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rise and fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	CL=100pF+1TTL	-



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics

SAMSUNG ELECTRONICS

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM681000BL/L-L	0~70 °C	5V +/- 10%	55/70ns	Commercial
KM681000BLE/LE-L	-25~85 °C	5V +/- 10%	70/100ns	Extended
KM681000BLI/LI-L	-40~85 °C	5V +/- 10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO1, tCO2	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ1, tLZ2	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ1, tHZ2	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

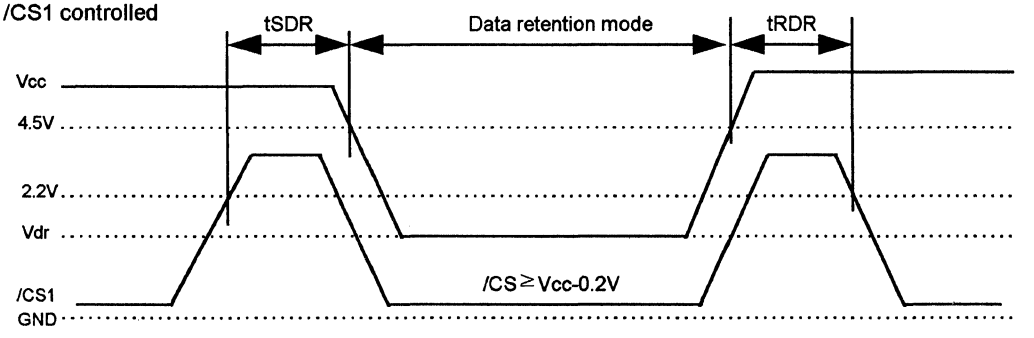
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS*** ≥ Vcc-0.2V		2.0	-	5.5	V
Data retention current	Idr	KM681000BL	Vcc=3.0V	L-Ver	-	1	50	uA
		KM681000BL-L	/CS1 ≥ Vcc-0.2V	LL-Ver	-	0.5	10	
		KM681000BLE		L-Ver	-	-	50	
		KM681000BLE-L		LL-Ver	-	-	25	
		KM681000BLI		L-Ver	-	-	50	
		KM681000BLI-L		LL-Ver	-	-	25	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

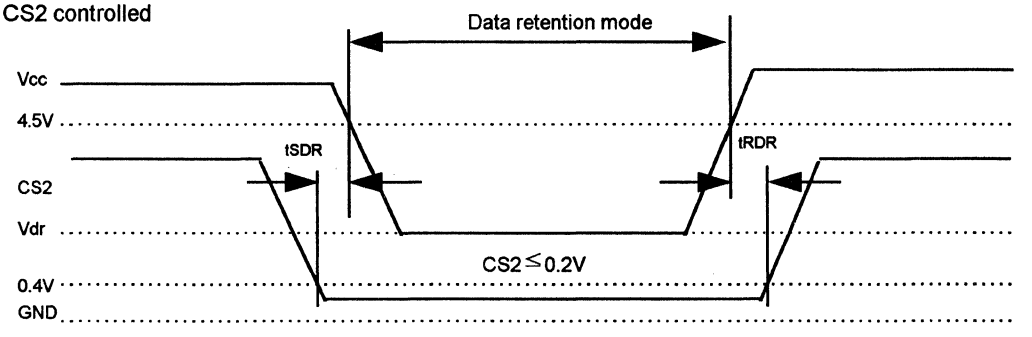
* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C
*** /CS1 ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V(/CS1 controlled) or CS2 ≤ 0.2V(CS2 controlled)

DATA RETENTION TIMING DIAGRAM

1) /CS1 controlled



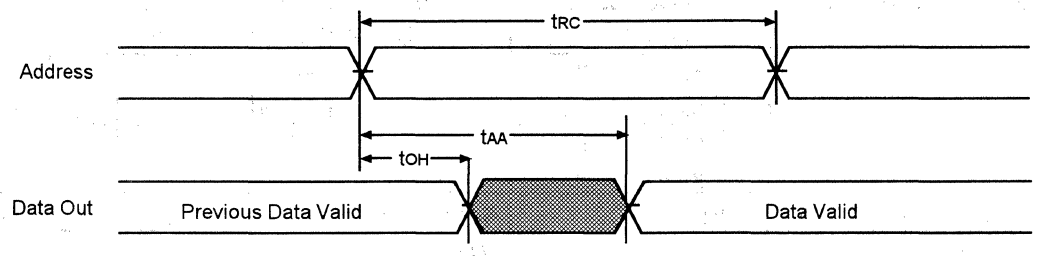
2) CS2 controlled



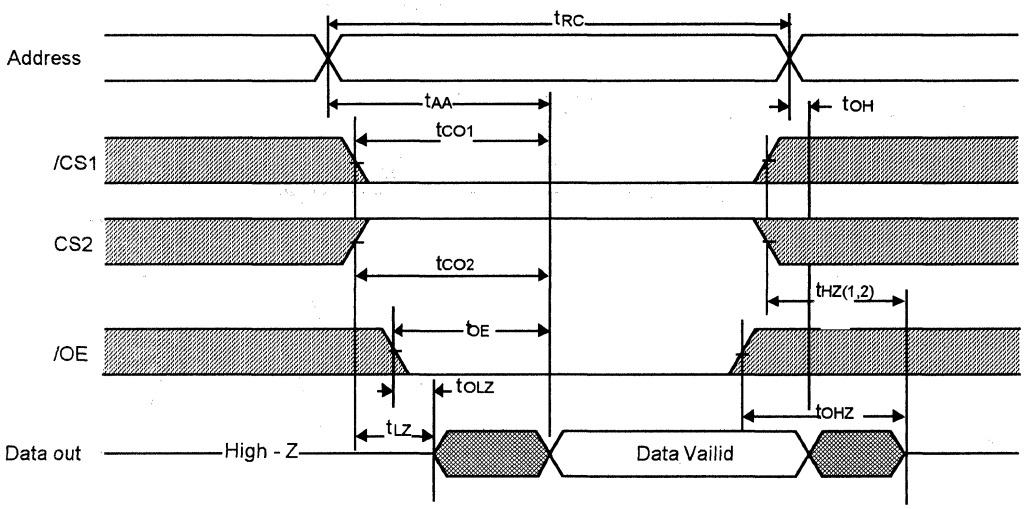
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, CS2=/WE=Vih)



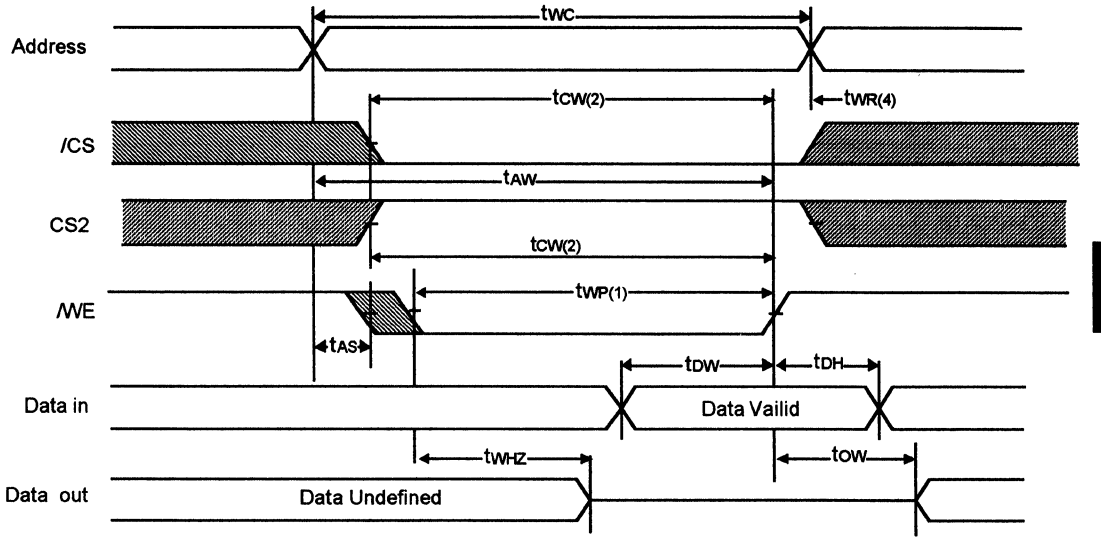
TIMING WAVEFORM OF READ CYCLE(2) (/WE= VIH)



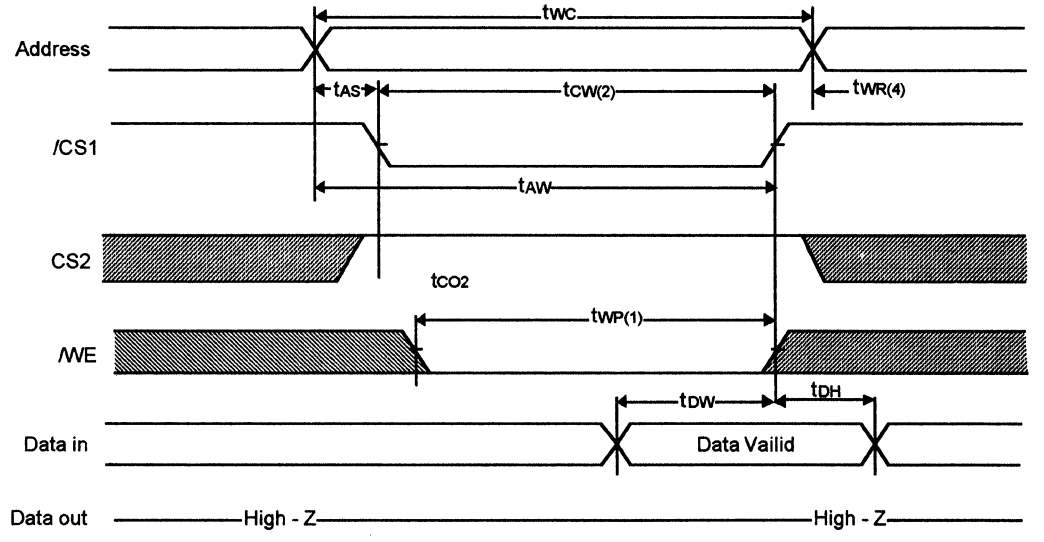
Notes(Read Cycle)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max) is less than tLZ(Min) both for a given device and device to device interconnection.

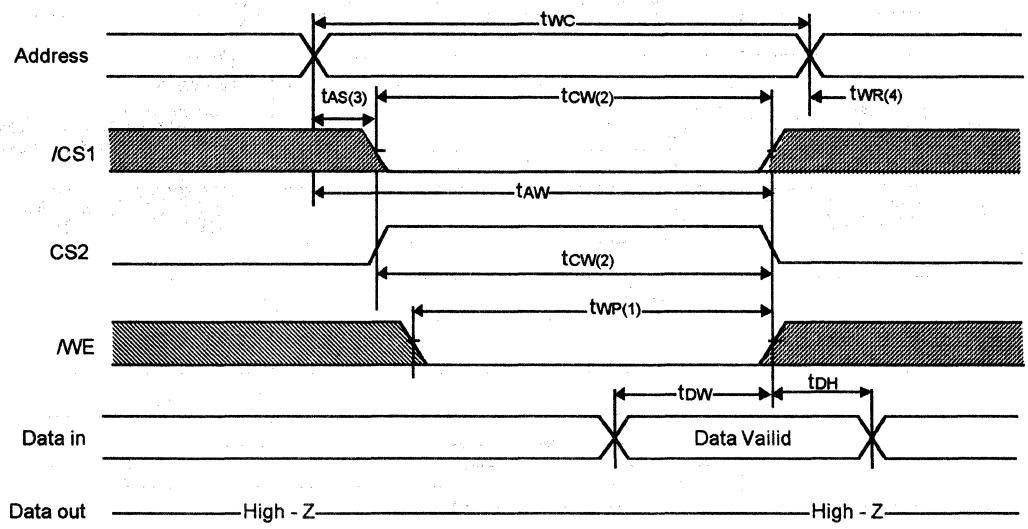
TIMING WAVEFORM OF WRITE CYCLE(1) (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (/CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



Notes(Write Cycle)

1. A write occurs during the overlap of a low /CS1, a high CS2 and a low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low. A write ends at the earliest transition among /CS1 going high, CS2 going low and /WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends at/CS1, or /WE going high, tWR2 applied in case a write ends at CS2 going to low.

FUNCTIONAL DESCRIPTION

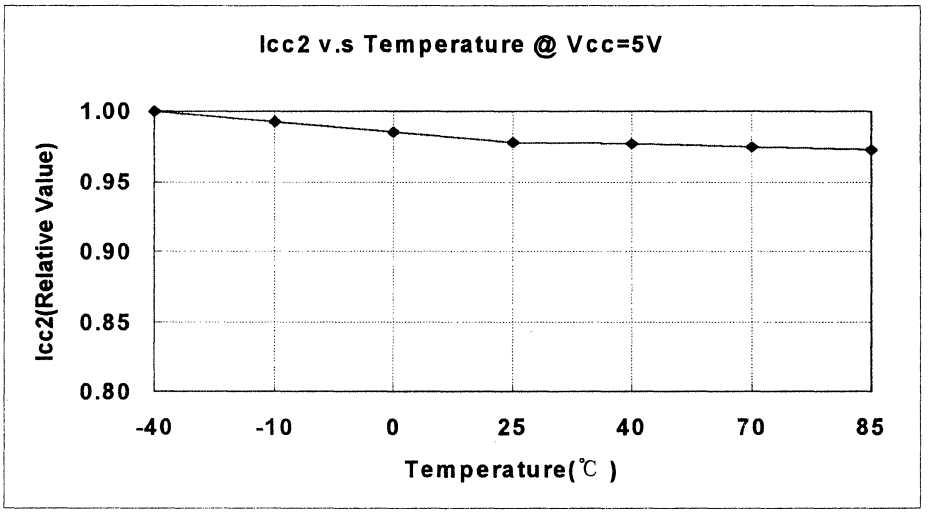
/CS1	CS2	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	Isb, Isb1
X	L	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	H	Ouput Disable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

* X means don't care

TECHNICAL INFORMATION

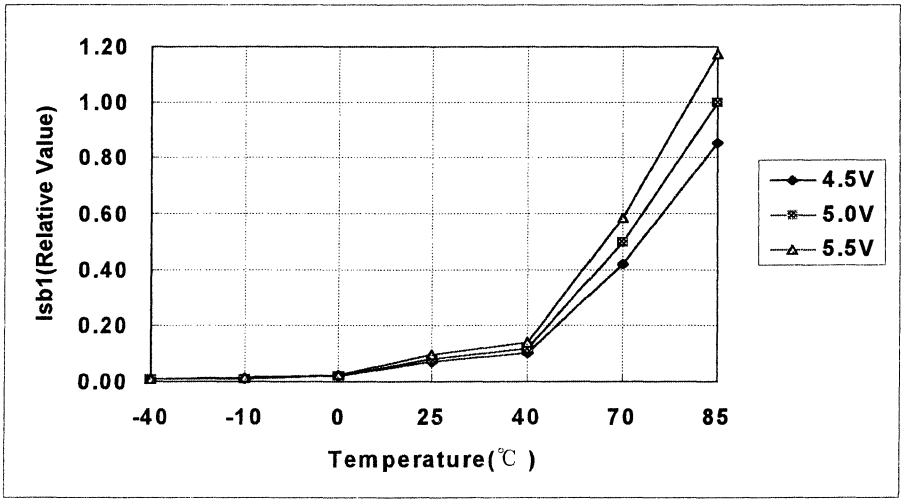
1) Icc2 characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and -40°C temperature. The basic relative value of Icc2 at that condition is set into 1.



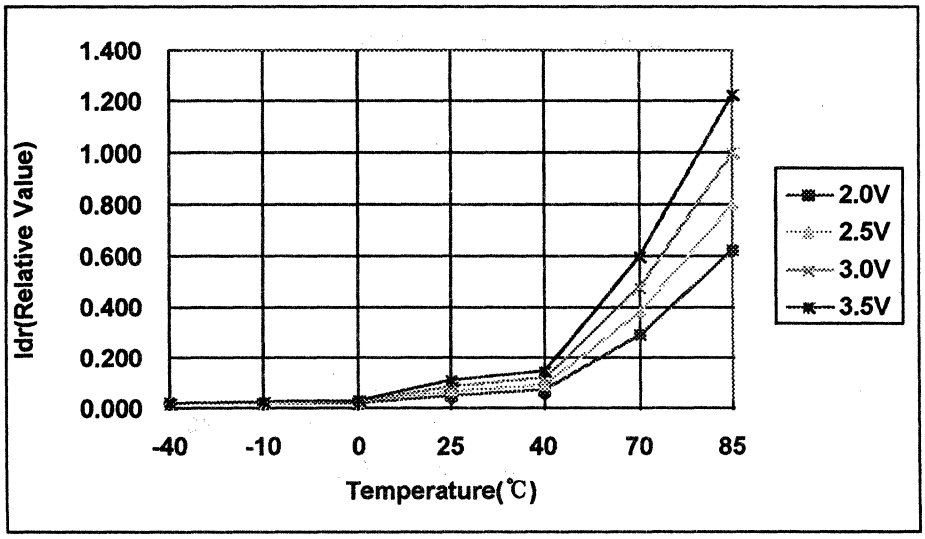
2) Isb1(CMOS Level Stanby Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and 85°C temperature. The basic relative value of Isb1 at that condition is set into 1.



3) Idr(Data Retention Current) characteristics by temperature variation

All the values in this graph is depicted by the relative value with the maximum value measured at Vdr=3.0V and 85°C temperature. The basic relative value of Idr at that condition is set into 1.



128Kx8 bit Low Power CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.4 uM CMOS
- Organization : 128K x 8
- Power Supply Voltage : Single 5V +/- 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-DIP, 32-SOP, 32-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

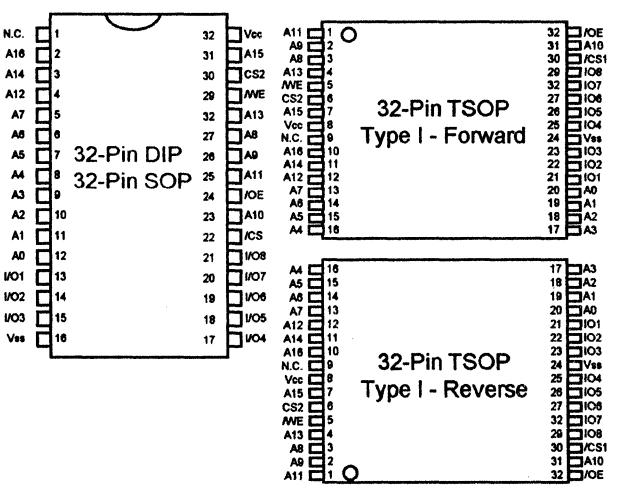
The KM681000C family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operations with low data retention current.

PRODUCT FAMILY

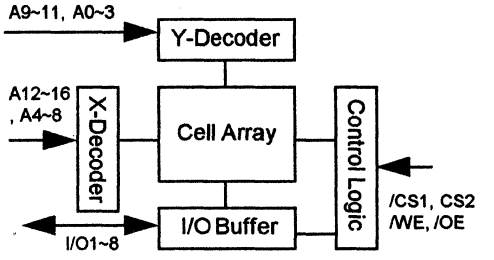
Product Family	Operating Temperature	Vcc Range (V)	Speed	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM681000CL	Commercial	4.5~5.5V	45*/55ns	32-DIP, 32-SOP	5uA	90mA
KM681000CL-L	(0~70 °C)			32-TSOP(I) R/F	2uA	
KM681000CLI	Industrial	4.5~5.5V	55*/70ns	32-SOP	10uA	
KM681000CLI-L	(-40~85 °C)			32-TSOP(I) R/F	4uA	

* measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



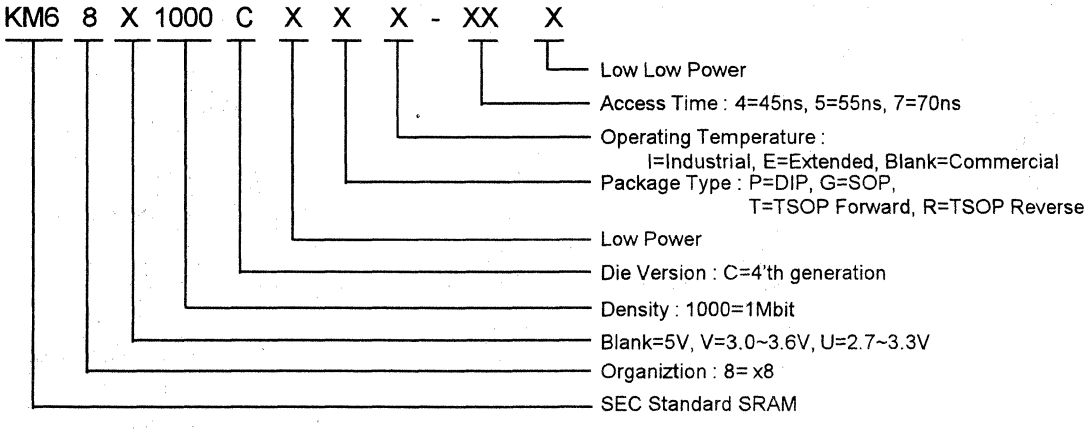
Pin Name	Function
A0~A16	Address Inputs
/WE	Write Enable Input
/CS1,CS2	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power(5V)
Vss	Ground
N.C.	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**
KM681000CLP-4	32-DIP, 45ns, L-pwr	KM681000CLGI-5	32-SOP, 55ns, L-pwr
KM681000CLP-5	32-DIP, 55ns, L-pwr	KM681000CLGI-7	32-SOP, 70ns, L-pwr
KM681000CLP-4L	32-DIP, 45ns, LL-pwr	KM681000CLGI-5L	32-SOP, 55ns, LL-pwr
KM681000CLP-5L	32-DIP, 55ns, LL-pwr	KM681000CLGI-7L	32-SOP, 70ns, LL-pwr
KM681000CLG-4	32-SOP, 45ns, L-pwr	KM681000CLTI-5	32-TSOP (I) F, 55ns, L-pwr
KM681000CLG-5	32-SOP, 55ns, L-pwr	KM681000CLTI-7	32-TSOP (I) F, 70ns, L-pwr
KM681000CLG-4L	32-SOP, 45ns,LL-pwr	KM681000CLTI-5L	32-TSOP (I) F, 55ns, LL-pwr
KM681000CLG-5L	32-SOP, 55ns, LL-pwr	KM681000CLTI-7L	32-TSOP (I) F, 70ns, LL-pwr
KM681000CLT-4	32-TSOP (I) F, 45ns, L-pwr	KM681000CLRI-5	32-TSOP (I) R, 55ns, L-pwr
KM681000CLT-5	32-TSOP (I) F, 55ns, L-pwr	KM681000CLRI-7	32-TSOP (I) R, 70ns, L-pwr
KM681000CLT-4L	32-TSOP (I) F, 45ns, LL-pwr	KM681000CLRI-5L	32-TSOP (I) R, 55ns, LL-pwr
KM681000CLT-5L	32-TSOP (I) F, 55ns, LL-pwr	KM681000CLRI-7L	32-TSOP (I) R, 70ns, LL-pwr
KM681000CLR-4	32-TSOP (I) R, 45ns, L-pwr		
KM681000CLR-5	32-TSOP (I) R, 55ns, L-pwr		
KM681000CLR-4L	32-TSOP (I) R, 45ns, LL-pwr		
KM681000CLR-5L	32-TSOP (I) R, 55ns, LL-pwr		

ORDERING INFORMATION



64Kx16 bit Low Power CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.6 um CMOS
- Organization : 64Kx16
- Data Byte Control : /LB=I/O1~8, /UB=I/O9~16
- Power Supply Voltage : 5.0V +/- 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  44-TSOP(II)-Reverse/Forward

GENERAL DESCRIPTION

The KM6161000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

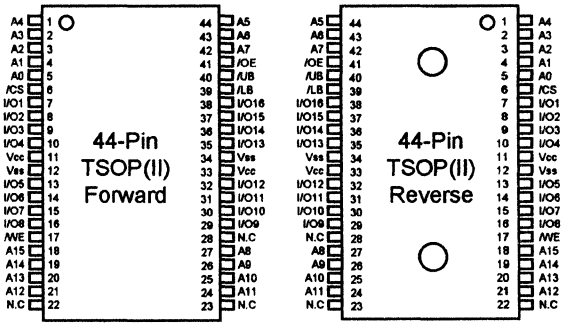
2

PRODUCT FAMILY

Product List	Operating Temp.	Vcc Range (V)	Speed (ns)	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM6161000BLT/LT-L KM6161000BLR/LR-L	Commercial (0~70 °C)	4.5 to 5.5	55*/70	44-TSOP(II) Foward/Reverse	100/20uA	120mA
KM6161000BLTI/LTI-L KM6161000BLRI/LRI-L	Industrial (-40~85 °C)	4.5 to 5.5	70/100	44-TSOP(II) Foward/Reverse	100/50uA	

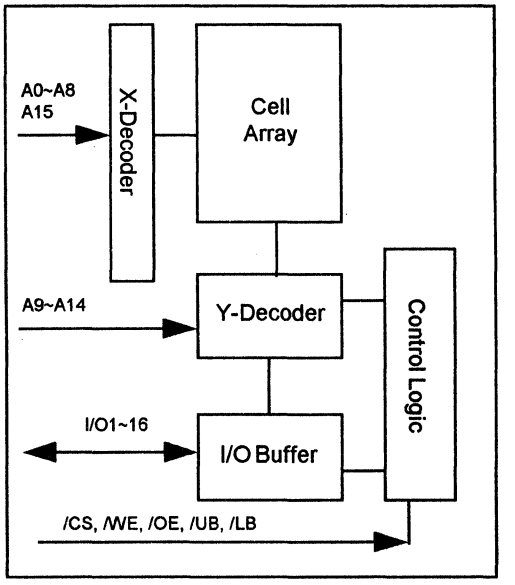
* parameters are measured with 30pF test load

PIN DESCRIPTION



Name	Function	Name	Function
A0~A15	Address Inputs	/LB	Lower Byte(I/O1~8)
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
/CS	Chip Select Input	Vcc	Power
/OE	Output Enable Input	Vss	Ground
I/O1~I/O16	Data Input/Output	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM

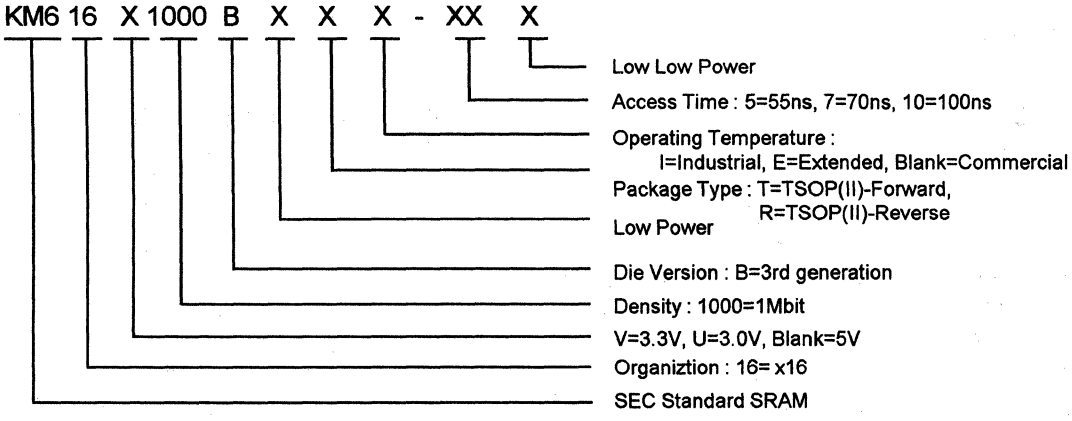


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70°C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**
KM6161000BLT-5	44-TSOP(II), F, 5V, 55ns, L	KM6161000BLTI-7	44-TSOP(II), F, 5V, 70ns, L
KM6161000BLT-5L	44-TSOP(II), F, 5V, 55ns, LL	KM6161000BLTI-7L	44-TSOP(II), F, 5V, 70ns, LL
KM6161000BLT-7	44-TSOP(II), F, 5V, 70ns, L	KM6161000BLTI-10	44-TSOP(II), F, 5V, 100ns, L
KM6161000BLT-7L	44-TSOP(II), F, 5V, 70ns, LL	KM6161000BLTI-10L	44-TSOP(II), F, 5V, 100ns, LL
KM6161000BLR-5	44-TSOP(II), R, 5V, 55ns, L	KM6161000BLRI-7	44-TSOP(II), R, 5V, 70ns, L
KM6161000BLR-5L	44-TSOP(II), R, 5V, 55ns, LL	KM6161000BLRI-7L	44-TSOP(II), R, 5V, 70ns, LL
KM6161000BLR-7	44-TSOP(II), R, 5V, 70ns, L	KM6161000BLRI-10	44-TSOP(II), R, 5V, 100ns, L
KM6161000BLR-7L	44-TSOP(II), R, 5V, 70ns, LL	KM6161000BLRI-10L	44-TSOP(II), R, 5V, 100ns, LL

ORDERING INFORMATION



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	6161000BLT/LT-L, 6161000BLR/LR-L
		-40 to 85	°C	6161000BLTI/LTI-L, 6161000BLRI/LRI-L
Soldering temperature and time	Tsolder	260°C , 10sec (Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.5	V
Input low voltage	Vil	-0.5***	--	0.8	V

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤50ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

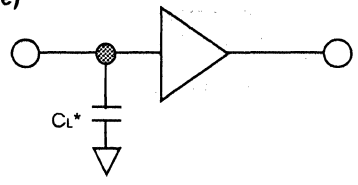
Item		Symbol	Test Conditions*		Min	Typ	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS=Vih or /WE=Vil, /UB=Vih or /LB=Vih, Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS=Vil, Vin=Vih or Vil, Iio=0mA	Read	-	-	10	mA
				Write			20	
Average operating current		Icc1	Cycle time=1uS 100% duty /CS≤0.2V, Iio=0mA	Read	-	-	15	
				Write			25	
		Icc2	Min cycle, 100% duty /CS≤Vil, Iio=0mA		-	-	120	
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Ouput high voltage		Voh	Ioh=-1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	3	mA
Standby Current (CMOS)	6161000BL/L-L	Isb1	/CS≥Vcc-0.2V Vin≥Vcc-0.2V or Vin≤0.2V	L	-	-	100	uA
				LL	-	-	20	uA
	6161000BLI/LI-L			L	-	-	100	uA
				LL	-	-	50	uA

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta= -40 to 85 °C, unless otherwise specified

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4 V	-
Input rise fall time	5 ns	-
Input and output reference voltage	1.5 V	-
Output load(See right)	C_L=100 pF+1TTL	-
	** C_L=30 pF+1TTL	-



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics
** Test load for 55ns product

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM6161000BL/L-L	0~70 °C	5V +/- 10%	55*/70ns	Commercial
KM6161000BLI/LI-L	-40~85 °C	5V +/- 10%	70/100ns	Industrial

* parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			55ns*		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	/UB, /LB Access Time	tBA	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	/UB, /LB enable to low-Z output	tBLZ	5	-	5	-	5	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	/UB, /LB disable to high-Z output	tBHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	/UB, /LB valid to end of write	tBW	45	-	60		80	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

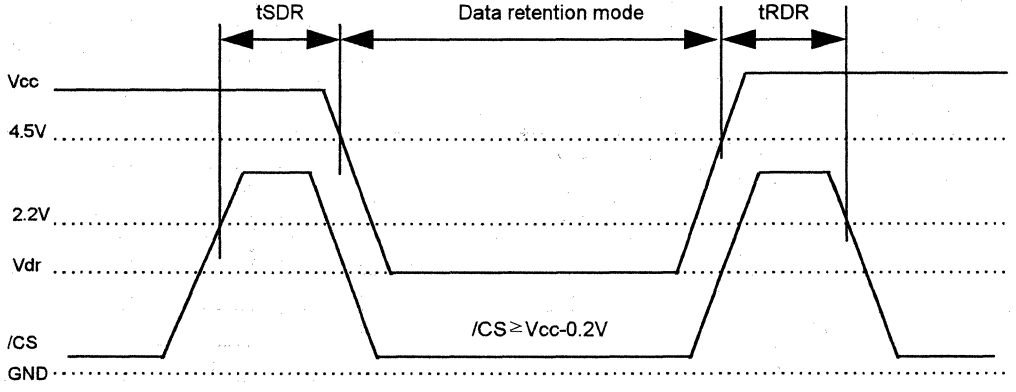
* parameters are measured with 30pF test load

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS≥Vcc-0.2V		2.0	-	5.5	V
Data retention current	Idr	6161000B Family	Vcc=3.0V	L-Ver	-	-	50	uA
		6161000BI Family	/CS≥Vcc-0.2V	LL-Ver	-	-	15	uA
				L-Ver	-	-	50	uA
				LL-Ver	-	-	20	uA
Data retention set-up time	tSDR		See data retention		0	-	-	ms
Recovery time	tRDR		waveform		5	-	-	ms

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C

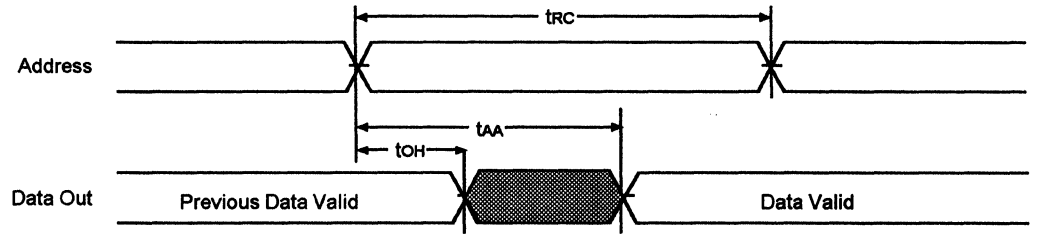
DATA RETENTION TIMING DIAGRAM



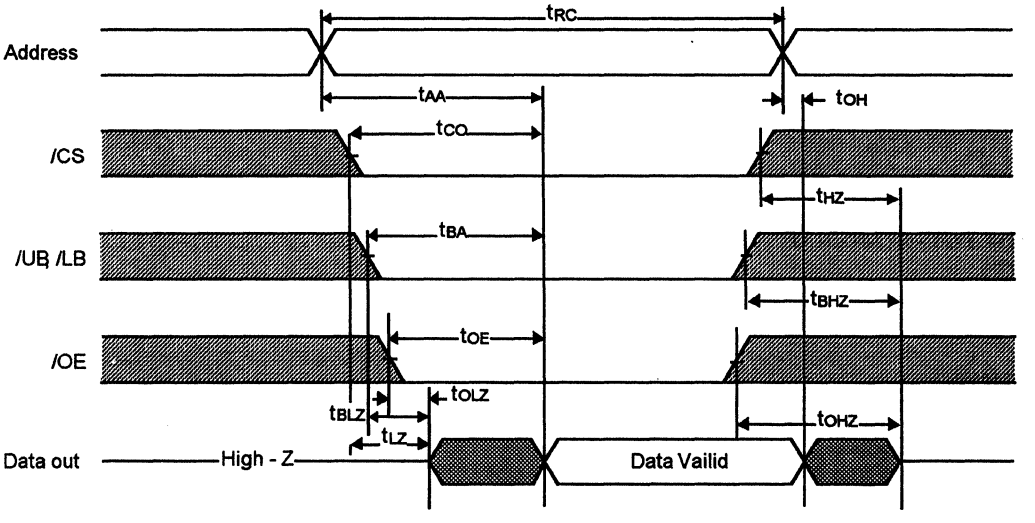
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih, /UB or, and /LB=Vil)



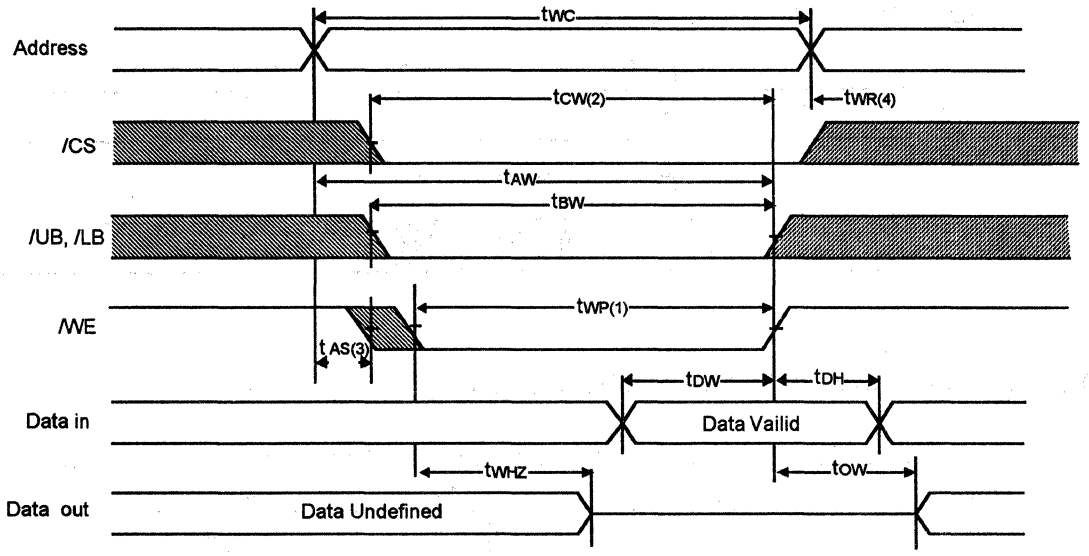
TIMING WAVEFORM OF READ CYCLE (/WE= VIH)



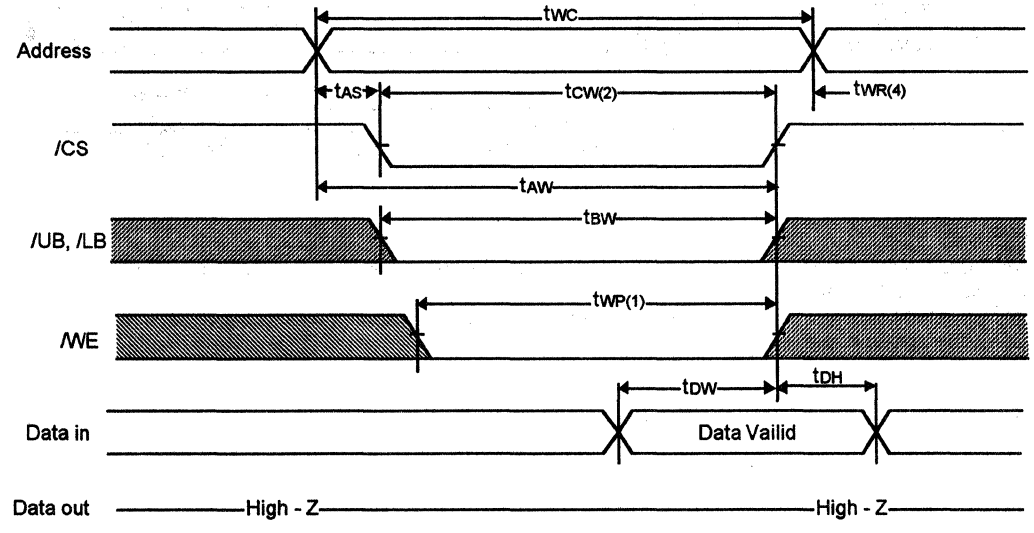
Notes (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than t LZ(min.) both for a given device and from device to device.

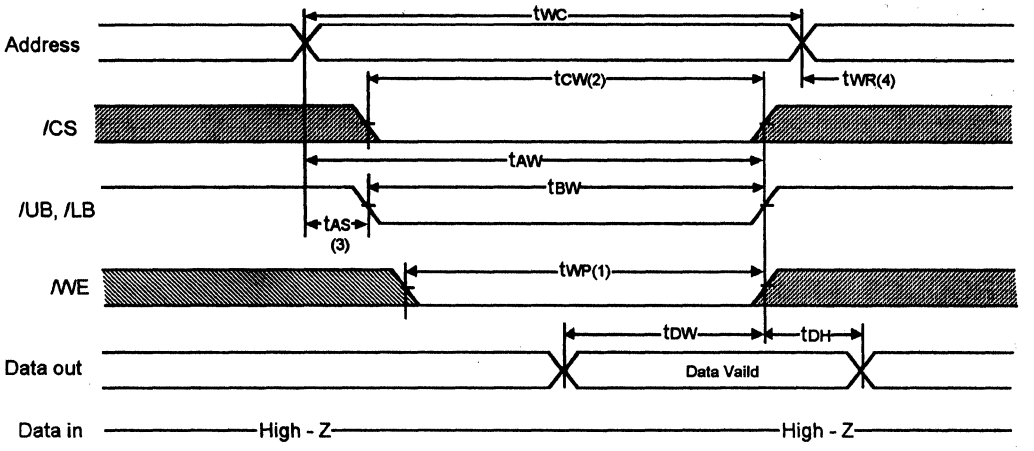
TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/UB,/ LB Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CS and low /WE. A write begins at the latest transition among /CS going low and /WE going low : A write end at the earliest transition among /CS going high and /WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS, or /WE going high.

FUNCTIONAL DESCRIPTION

/CS	/UB	/LB	/WE	/OE	Mode	I/O1~7	I/O 9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	Isb, Isb1
L	X	X	H	H	Ouput	High-Z	High-Z	Icc
L	H	H	X	X	Diable	High-Z	High-Z	
L	L	H	H	L	Read	Dout	High-Z	Icc
	H	L				High-Z	Dout	
	L	L				Dout	Dout	
L	L	H	L	X	Write	Din	High-Z	Icc
	H	L				High-Z	Din	
	L	L				Din	Din	

* X means don't care

SAMSUNG ELECTRONICS

512Kx8 bit High Speed CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.4 um CMOS
- Organization : 512K x8
- Power Supply Voltage : Single 5V +/- 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-DIP, 32-SOP, 32-TSOP(II)-Forward/Reverse

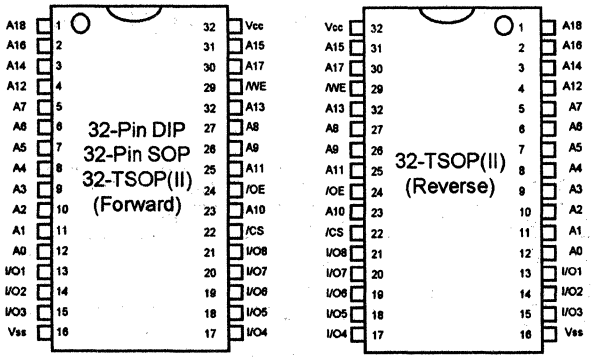
GENERAL DESCRIPTION

The KM684000A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operations with low data retention current.

PRODUCT FAMILY

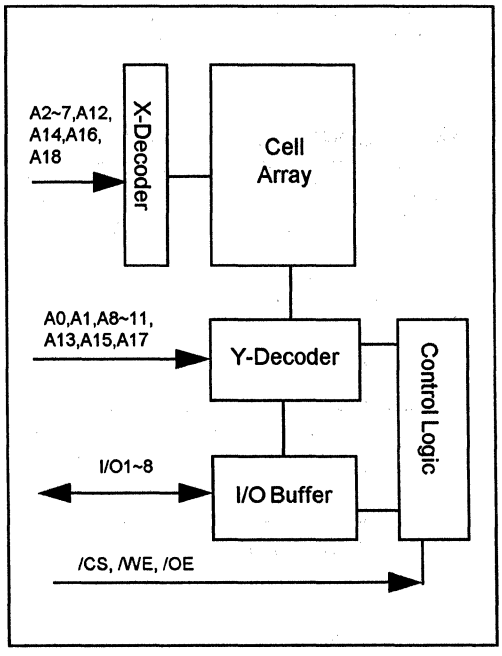
Product Family	Operating Temperature	Vcc Range (V)	Speed	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM684000AL	Commercial	4.5~5.5V	55/70ns	32-DIP, 32-SOP	100uA	90mA
KM684000AL-L	(0~70 °C)			32-TSOP(II) R/F	20uA	
KM684000ALI	Industrial	4.5~5.5V	70/100ns	32-SOP	100uA	
KM684000ALI-L	(-40~85 °C)			32-TSOP(II) R/F	50uA	

PIN DESCRIPTION



Pin Name	Function
A0~A18	Address Inputs
/WE	Write Enable Input
/CS	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power(5V)
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM

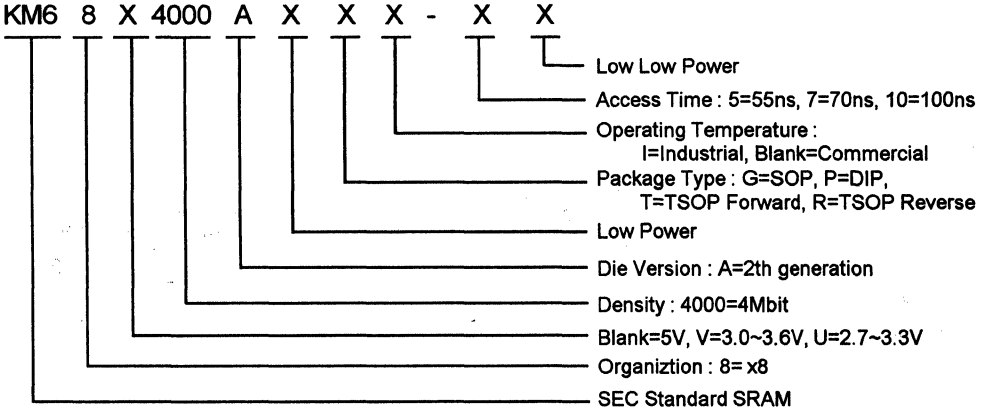


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**
KM684000ALP-5	32-DIP, 55ns, , L-pwr	KM684000ALGI-7	32-SOP, 70ns, L-pwr
KM684000ALP-5L	32-DIP, 55ns, LL-pwr	KM684000ALGI-7L	32-SOP, 70ns, LL-pwr
KM684000ALP-7	32-DIP, 70ns, , L-pwr	KM684000ALGI-10	32-SOP, 100ns, L-pwr
KM684000ALP-7L	32-DIP, 70ns, LL-pwr	KM684000ALGI-10L	32-SOP, 100ns, LL-pwr
KM684000ALG-5	32-SOP, 55ns, L-pwr	KM684000ALTI-7	32-TSOP(II) F, 70ns, L-pwr
KM684000ALG-5L	32-SOP, 55ns, LL-pwr	KM684000ALTI-7L	32-TSOP(II) F, 70ns, LL-pwr
KM684000ALG-7	32-SOP, 70ns, L-pwr	KM684000ALTI-10	32-TSOP(II) F, 100ns, L-pwr
KM684000ALG-7L	32-SOP, 70ns, LL-pwr	KM684000ALTI-10L	32-TSOP(II) F, 100ns, LL-pwr
KM684000ALT-5	32-TSOP(II) F, 55ns, L-pwr	KM684000ALRI-7	32-TSOP(II) R, 70ns, L-pwr
KM684000ALT-5L	32-TSOP(II) F, 55ns, LL-pwr	KM684000ALRI-7L	32-TSOP(II) R, 70ns, LL-pwr
KM684000ALT-7	32-TSOP(II) F, 70ns, L-pwr	KM684000ALRI-10	32-TSOP(II) R, 100ns, L-pwr
KM684000ALT-7L	32-TSOP(II) F, 70ns, LL-pwr	KM684000ALRI-10L	32-TSOP(II) R, 100ns, LL-pwr
KM684000ALR-5	32-TSOP(II) R, 55ns, L-pwr		
KM684000ALR-5L	32-TSOP(II) R, 55ns, LL-pwr		
KM684000ALR-7	32-TSOP(II) R, 70ns, L-pwr		
KM684000ALR-7L	32-TSOP(II) R, 70ns, LL-pwr		

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM684000AL/L-L
		-40 to 85	°C	KM684000ALI/LI-L
Soldering temperature and time	Tsolder	260 °C , 10sec(Lead Only)	-	-

* Stresses greater than those listed under Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilyed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.5	V
Input low voltage	Vil	-0.3***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C
Vil(min)=-3.0V for ≤50ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	V
Output leakage current		Ilo	/CS=Vih or /OE=Vih or /WE=Vil Vio=Vss to Vcc		-1	-	1	V
Operating power supply current		Icc	/CS=Vil, Vin=Vil or Vih Iio=0mA		-	-	20	mA
Average operating current		Icc1	Cycle time=1uS 100% duty /CS≤0.2V, Vih≥Vcc-0.2V Vil≤0.2V, Iio=0mA		-	-	25	mA
		Icc2	Min cycle, 100% duty, /CS=Vil Vin=Vil or Vih, Iio=0mA		-	-	90	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	3	mA
Standby Current (CMOS)	KM684000AL/L-L	Isb1	/CS≥Vcc-0.2V Vin≥Vcc-0.2V or Vin≤0.2V	L	-	-	100	uA
				LL	-	-	20	uA
	KM684000ALI/LI-L			L	-	-	100	uA
				LL	-	-	50	uA

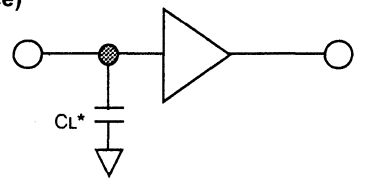
* 1) Commercial Product : Ta=0 to 70 °C , Vcc=5V+/-10%, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C Vcc=5V+/-10%, unless otherwise specified

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL	-

* See test condition of DC and Operating characteristics



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM684000AL/L-L	0~70 °C	5V +/- 10%	55/70ns	Commercial
KM684000ALI/LI-L	-40~85 °C	5V +/- 10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

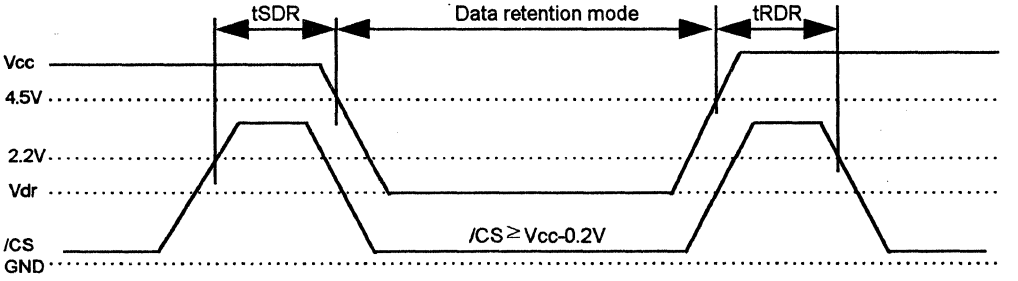
Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to ouput	tCO	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to ouput low-Z	tOW	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS≥Vcc-0.2V		2.0	-	5.5	V
Data retention current	Idr	KM684000AL/L-L	Vcc=3.0V	L-Ver	-		50	uA
			/CS≥Vcc-0.2V	LL-Ver	-	-	15	
		KM684000ALI/LI-L		L-Ver	-	-	50	
				LL-Ver	-	-	20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

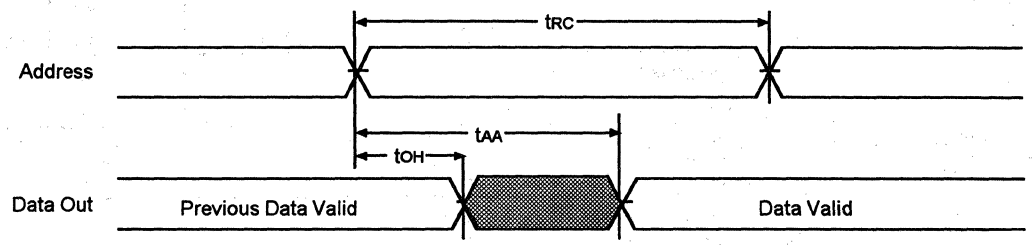
/CS	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	Ouput Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care

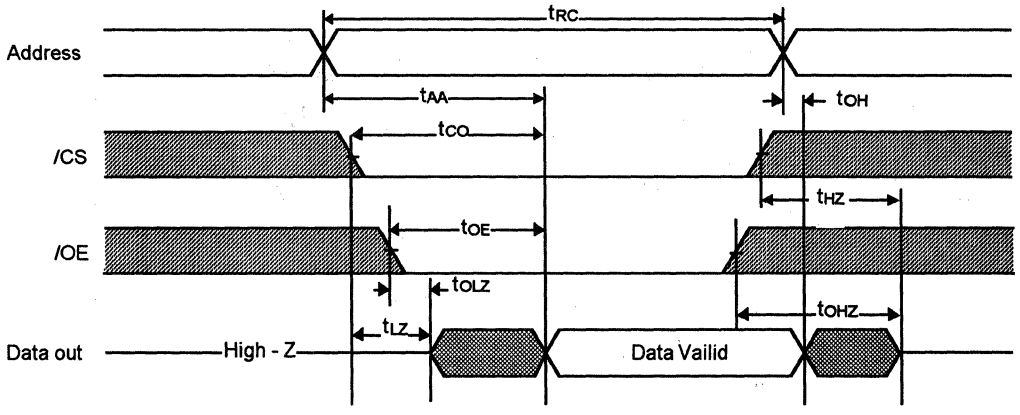
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih)



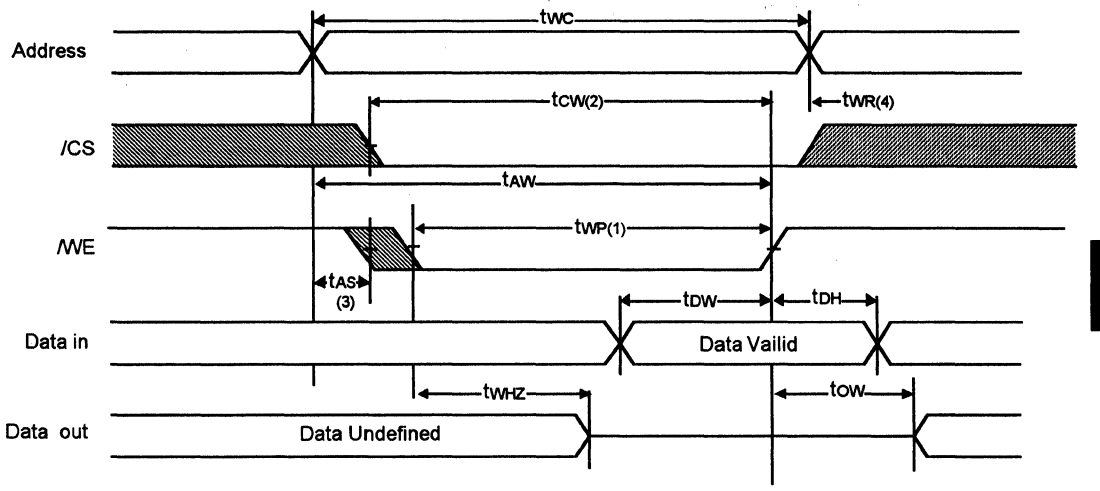
TIMING WAVEFORM OF READ CYCLE (/WE= VIH)



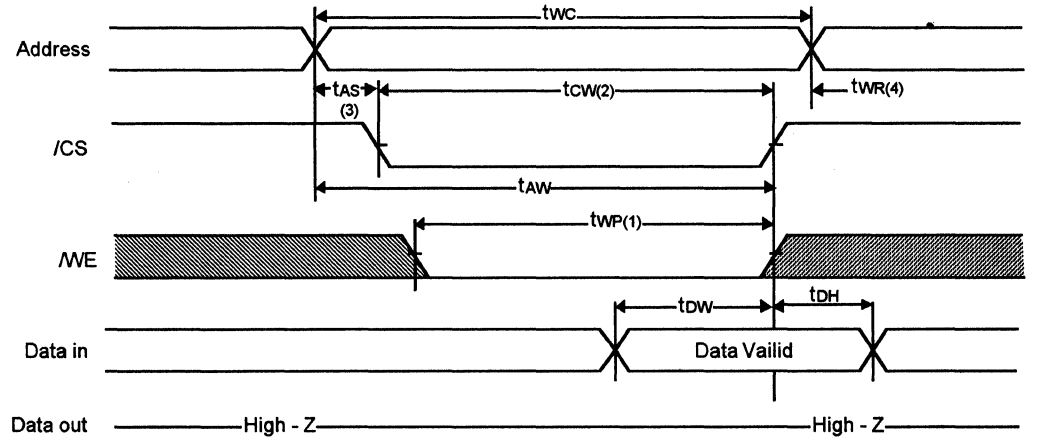
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.)both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



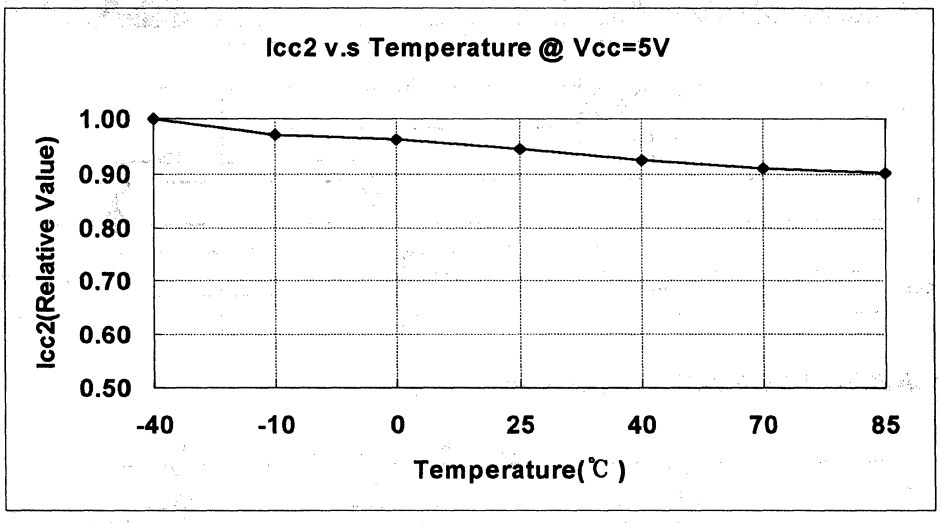
Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CSand low /WE. A write begins at the latest transition among /CS going low and WE going low : A write end at the earliest transition among /CSgoing high and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS,or /WE going high.

TECHNICAL INFORMATION

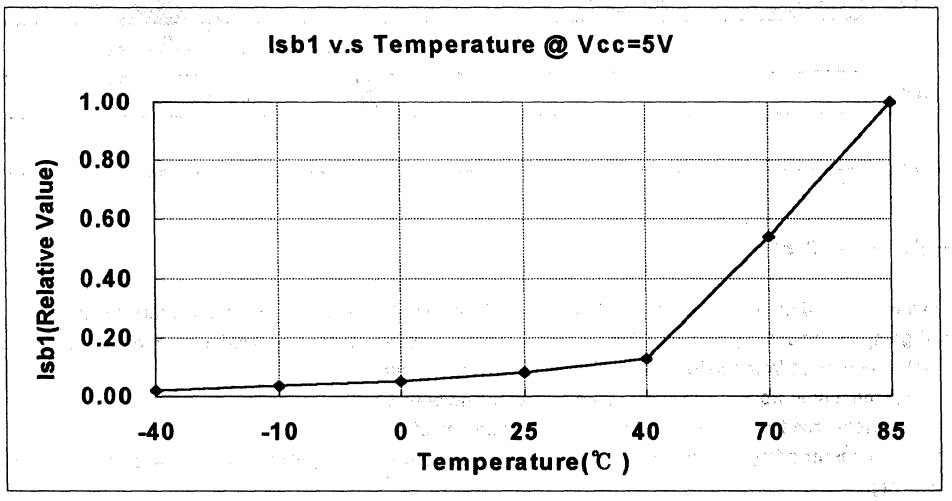
1) Icc2 characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and -40°C temperature. The basic relative value of Icc2 at that condition is set into 1.



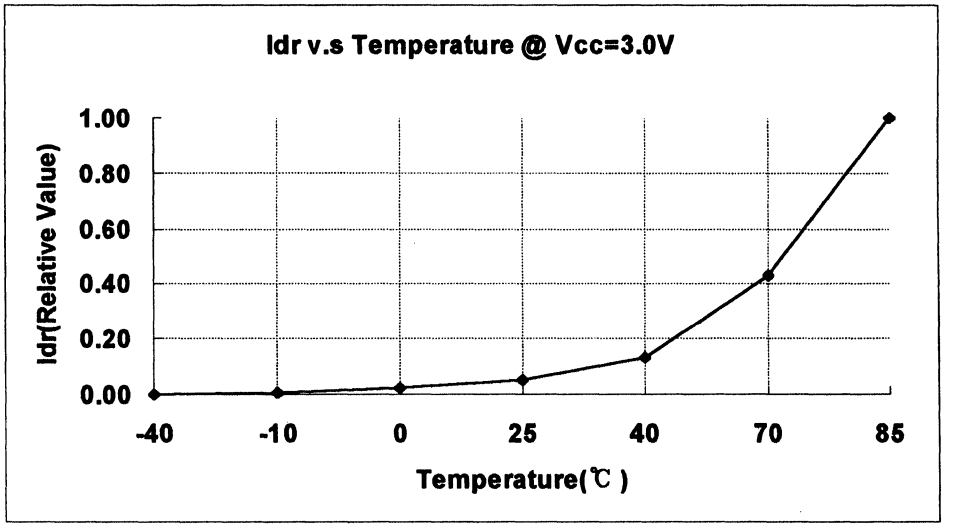
2) Isb1(CMOS Level Stanby Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and 85°C temperature. The basic relative value of Isb1 at that condition is set into 1.



3) Idr(Data Retention Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at Vdr=3.0V and 85°C temperature. The basic relative value of Idr at that condition is set into 1.



Low Voltage SRAMs (3.0V/3.3V)

- KM62V256C, KM62U256C Family	32K × 8	Commercial, Extended, Industrial Products
- KM68V512A, KM68U512A Family	64K × 8	Commercial, Extended, Industrial Products
- KM68V1000B, KM68U1000B Family	128K × 8	Commercial, Extended, Industrial Products
- KM616V1000B, KM616U1000B Family	128K × 8	Commercial, Extended, Industrial Products
- KM68V4000A Family	512K × 8	Commercial, Industrial Products

32Kx8 bit Low Power & Low Vcc CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.7 uM CMOS
- Organization : 32K x 8
- Power Supply Voltage
  KM62V256C family : 3.3V +/- 0.3V
  KM62U256C family : 3.0V +/- 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-SOP, 28-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

The KM62V256C and KM62U256C family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

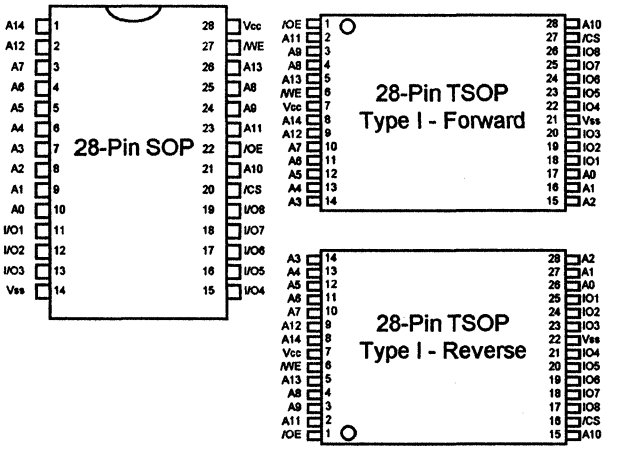
2

PRODUCT FAMILY

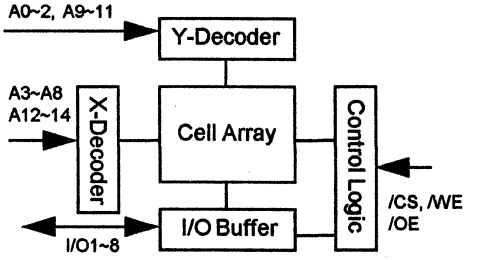
Product List	Operating Temp.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM62V256CL-L	Commercial	3.0~3.6V	70*/100	28-SOP	10uA	35 mA
KM62U256CL-L	(0~70 °C)	2.7~3.3V	85*/100	28-TSOP(I) R/F	10uA	
KM62V256CLE-L	Extended	3.0~3.6V	70*/100	28-SOP	20uA	
KM62U256CLE-L	(-25~ 85 °C)	2.7~3.3V	85*/100	28-TSOP(I) R/F	15uA	
KM62V256CLI-L	Industrial	3.0~3.6V	70*/100	28-SOP	20uA	
KM62U256CLI-L	(-40~85 °C)	2.7~3.3V	85*/100	28-TSOP(I) R/F	15uA	

* measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



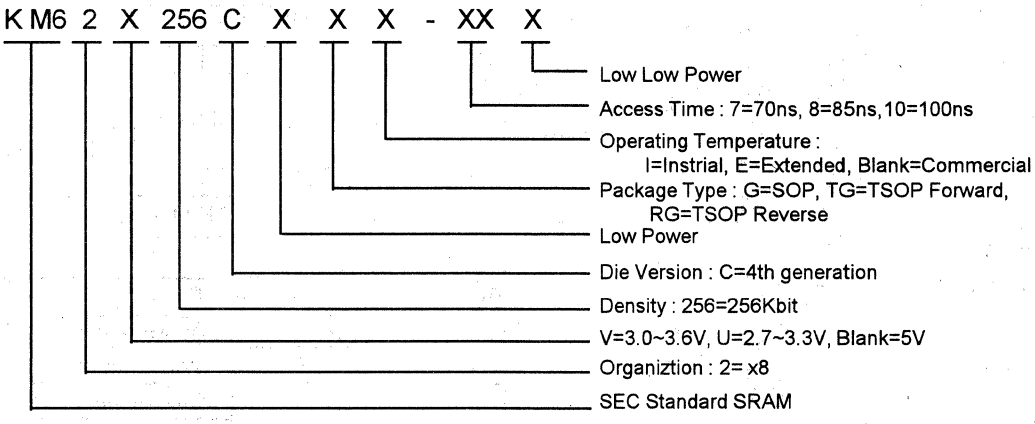
Pin Name	Function
A0~A14	Address Inputs
/WE	Write Enable Input
/CS	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power
Vss	Groud

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
KM62V256CLG-7L	28-SOP, 70ns, 3.3V	KM62V256CLGE-7L	28-SOP, 70ns, 3.3V	KM62V256CLGI-7L	28-SOP, 70ns, 3.3V
KM62V256CLG-10L	28-SOP, 100ns, 3.3V	KM62V256CLGE-10L	28-SOP, 100ns, 3.3V	KM62V256CLGI-10L	28-SOP, 100ns, 3.3V
KM62V256CLTG-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGE-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGI-7L	28-TSOP F, 70ns, 3.3V
KM62V256CLTG-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGE-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGI-10L	28-TSOP F, 100ns, 3.3V
KM62V256CLRG-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGE-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGI-7L	28-TSOP R, 70ns, 3.3V
KM62V256CLRG-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGE-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGI-10L	28-TSOP R, 100ns, 3.3V
KM62U256CLG-8L	28-SOP, 85ns, 3.0V	KM62U256CLGE-8L	28-SOP, 85ns, 3.0V	KM62U256CLGI-8L	28-SOP, 85ns, 3.0V
KM62U256CLTG-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGE-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGI-8L	28-TSOP F, 85ns, 3.0V
KM62U256CLRG-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGE-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGI-8L	28-TSOP R, 85ns, 3.0V
KM62U256CLG-10L	28-SOP, 100ns, 3.0V	KM62U256CLGE-10L	28-SOP, 100ns, 3.0V	KM62U256CLGI-10L	28-SOP, 100ns, 3.0V
KM62U256CLTG-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGE-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGI-10L	28-TSOP F, 100ns, 3.0V
KM62U256CLRG-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGE-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGI-10L	28-TSOP R, 100ns, 3.0V

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Pd	0.7	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM62V256CL-L, KM62U256CL-L
		-25 to 85	°C	KM62V256CLE-L, KM62U256CLE-L
		-40 to 85	°C	KM62V256CLI-L, KM62U256CLI-L
Soldering temperature and time	Tsolder	260 °C , 10sec (Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM62V256C Family	3.0	3.3	3.6	V
		KM62U256C Family	2.7	3.0	3.3	V
Ground	Vss	All	0	0	0	V
Input high voltage	Vih	KM62V256C Family	2.2	-	Vcc+0.3	V
		KM62U256C Family	2.2	-	Vcc+0.3	V
Input low voltage	Vil	KM62V256C Family	-0.3	-	0.4	V
		KM62U256C Family	-0.3***	-	0.4	V

* 1) Commercial Product : Ta=0 to 70 °C unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤30ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

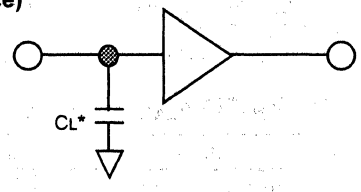
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS=Vih or Vil or /WE=Vil Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS=Vil, Vin=Vih or Vil, Iio=0mA		-	1.0	2.0	mA
Average operating current		Icc1	Cycle time=1uS 100% duty /CS≤0.2V, Vil≤0.2V, Vin≥Vcc-0.2V, Iio=0mA		-	2.5	5	mA
		Icc2	Min cycle, 100% duty /CS=Vil, Iio=0mA		-	20***	35	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Ouput high voltage		Voh	Ioh=-1.0mA		2.2	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	0.3	mA
Standby Current (CMOS)	KM62V256CL-L	Isb1	/CS≥Vcc-0.2V Vin≤0.2V or Vin≥Vcc-0.2V	LL	-	1.5	10	uA
	KM62V256CLE-L			LL	-	1.5	20	uA
	KM62V256CLI-L			LL	-	1.5	20	uA
	KM62U256CL-L			LL	-	1.0	10	uA
	KM62U256CLE-L			LL	-	1.0	15	uA
	KM62U256CLI-L			LL	-	1.0	15	uA

* 1) Commercial Product : Ta=0 to 70 °C, Vcc=3.0 +/- 0.3V(62U256C Family), Vcc=3.3 +/- 0.3V(62V256C Family)
2) Extended Product : Ta=-25 to 85 °C, Vcc=3.0 +/- 0.3V(62U256CE Family), Vcc=3.3 +/- 0.3V(62V256CE Family)
3) Industrial Product : Ta=-40 to 85 °C, Vcc=3.0 +/- 0.3V(62U256CI Family), Vcc=3.3 +/- 0.3V(62V256CI Family)
** Ta=25 °C
*** 25mA for KM62V256C family

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics
** KM62V256CL-7L, KM62V256CLE-7L, KM62V256CLI-7L, KM62U256CL-8L, KM62U256CLE-8L, KM62U256CLI-8L,

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62V256CL/L-L	0~70 °C	3.3V +/- 0.3	70*/100ns	Commercial
KM62V256CLE/LE-L	-25~85 °C	3.3V +/- 0.3	70*/100ns	Extended
KM62V256CLI/LI-L	-40~85 °C	3.3V +/- 0.3	70*/100ns	Industrial
KM62U256CL/L-L	0~70 °C	3.0V +/- 0.3	85*/100ns	Commercial
KM62U256CLE/LE-L	-25~85 °C	3.0V +/- 0.3	85*/100ns	Extended
KM62U256CLI/LI-L	-40~85 °C	3.0V +/- 0.3	85*/100ns	Industrial

* parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			70ns*		85ns*		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to ouput	tCO	-	70	-	85	-	100	ns
	Output enable to valid ouput	tOE	-	35	-	45	-	50	ns
	Chip select to low-Z ouput	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z ouput	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z ouput	tHZ	0	30	0	30	0	35	ns
	Output disable to high-Z ouput	tOHZ	0	30	0	30	0	35	ns
	Ouput hold from address change	tOH	5	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	70	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	70	-	ns
	Write pulse width	tWP	50	-	60	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	50	-	60	-	60	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to ouput low-Z	tOW	5	-	10	-	10	-	ns

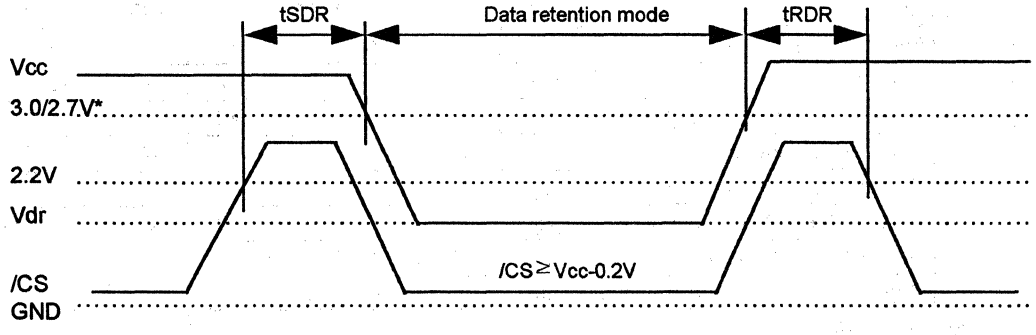
* All the parameters are measured with 30pF test load

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*	Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS≥Vcc-0.2V	2.0	-	3.6	V
Data retention current	Idr	KM62V256CL-L	Vcc=3.0V	-	1	8	uA
		KM62U256CL-L	/CS≥Vcc-0.2V	-	0.6	8	
		KM62V256CLE-L		-	1	10	
		KM62U256CLE-L		-	0.6	10	
		KM62V256CLI-L		-	1	10	
		KM62U256CLI-L		-	0.6	10	
Data retention set-up time	tSDR		See data retention waveform	0	-	-	ms
Recovery time	tRDR			5	-	-	

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C

DTA RETENTION TIMING DIAGRAM



* 3.0V for KM62V256C family, 2.7V for KM62U256C family

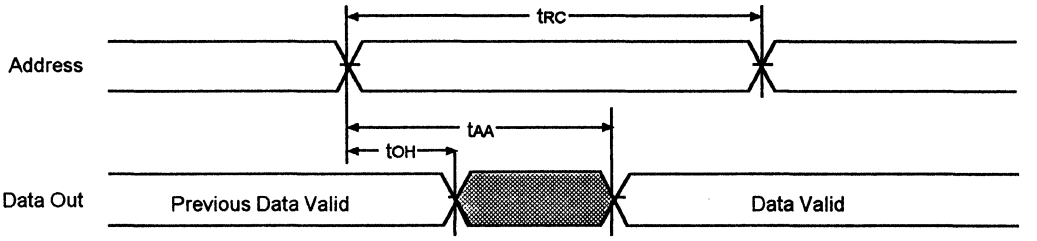
FUNCTIONAL DESCRIPTION

/CS	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	Ouput Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

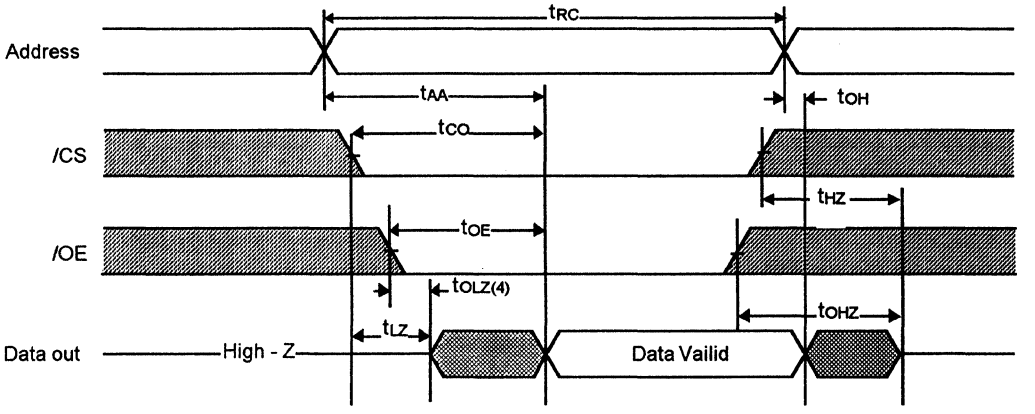
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih)



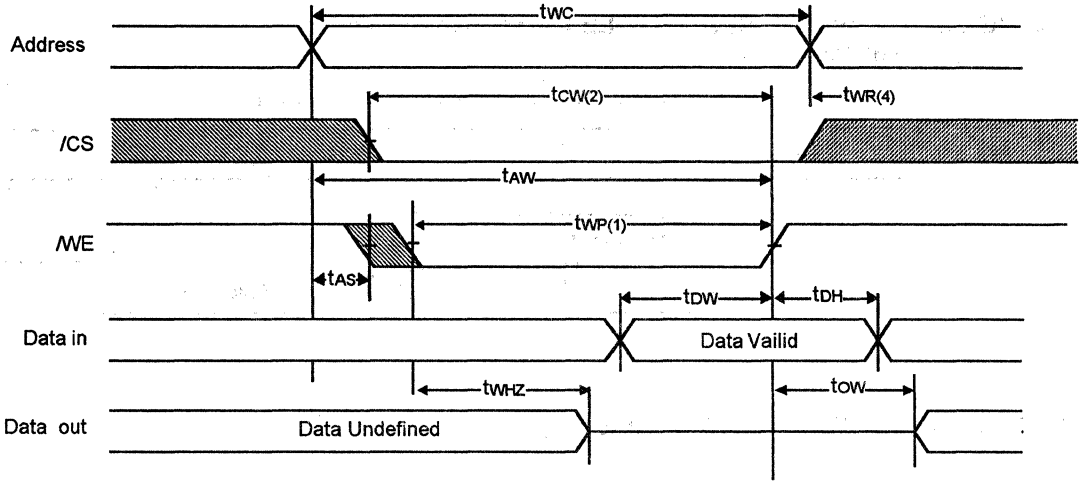
TIMING WAVEFORM OF READ CYCLE (/WE= VIH)



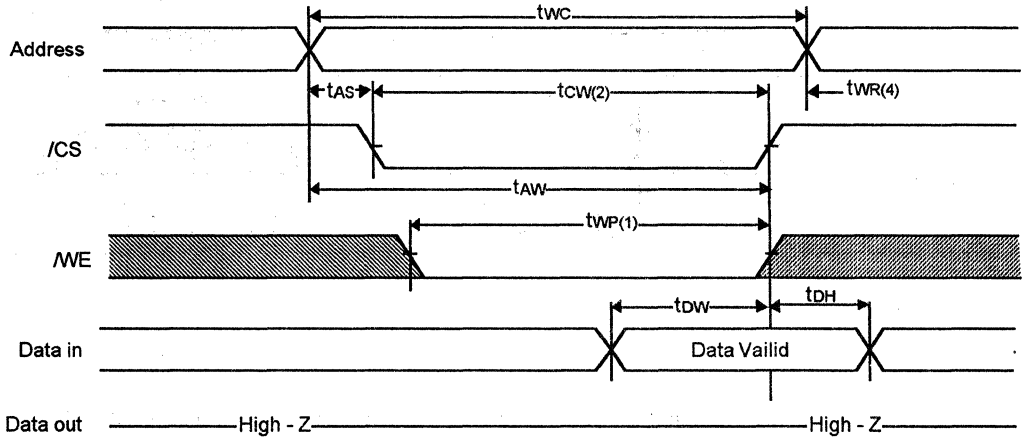
Notes (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ (max.) is less than tLZ (min.)both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



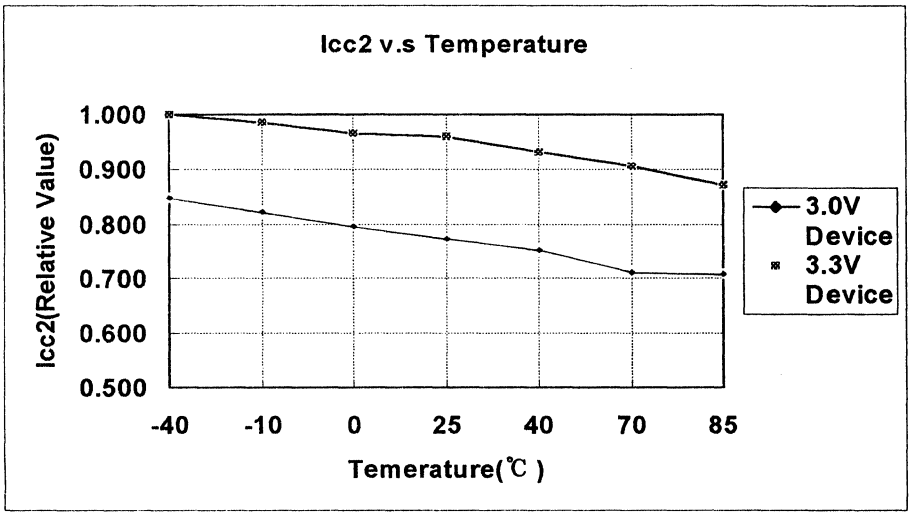
Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CSand low /WE. A write begins at the latest transition among /CS going low and WE going low : A write end at the earliest transition among /CSgoing high and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS,or /WE going high.

TECHNICAL INFORMATION

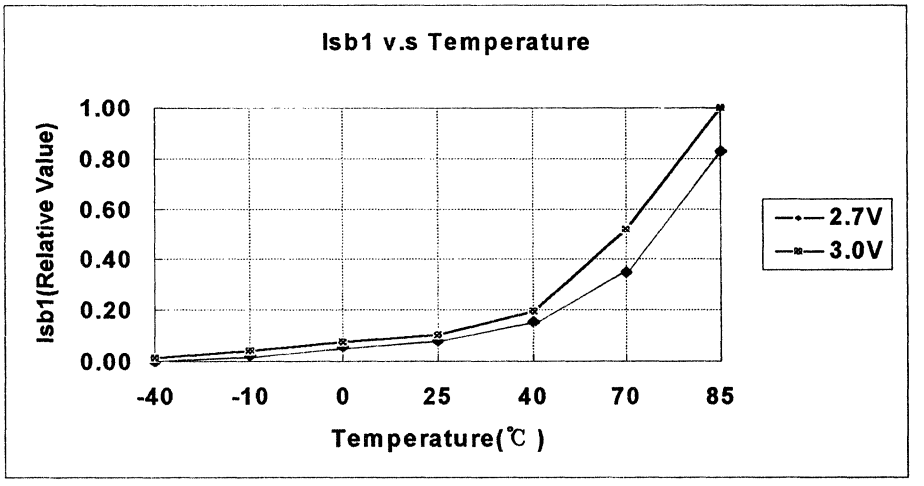
1) Icc2 characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 3.3V Vcc and -40°C temperature. The basic relative value of Icc2 at that condition is set into 1.



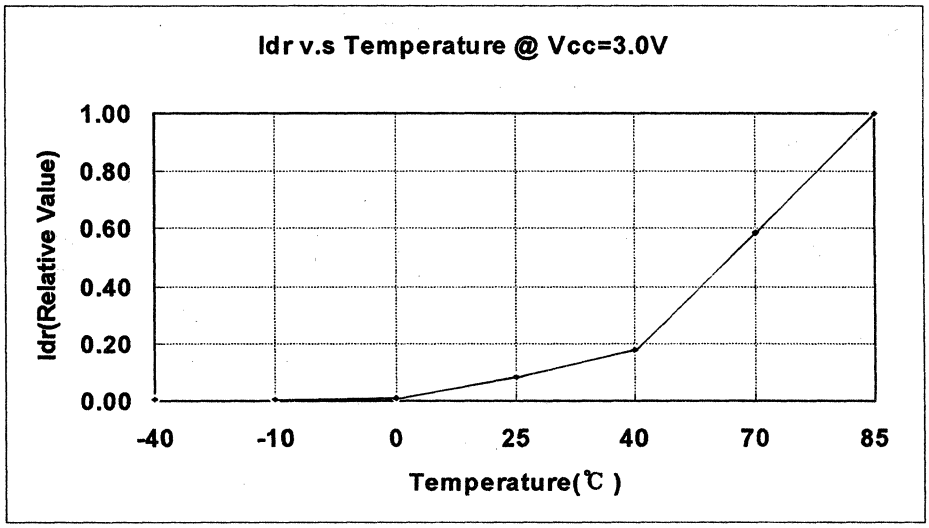
2) Isb1(CMOS Level Stanby Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 3.0V Vcc and 85°C temperature. The basic relative value of Isb1 at that condition is set into 1.



3) Idr(Data Retention Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at Vdr=3.0V and 85°C temperature. The basic relative value of Idr at that condition is set into 1.



64Kx8 bit Low Power & Low Vcc CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.6 um CMOS
- Organization : 64K x 8
- Power Supply Voltage
  KM68V512A family : 3.3V +/- 0.3V
  KM68U512A family : 3.0V +/- 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(I)-Forward

GENERAL DESCRIPTION

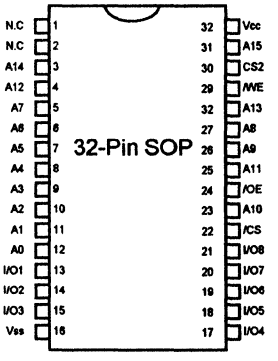
The KM68V512A and KM68U512A family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

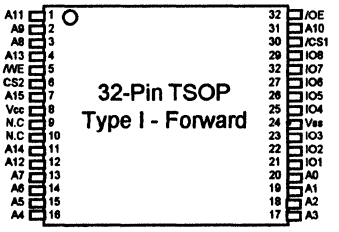
2

PRODUCT FAMILY

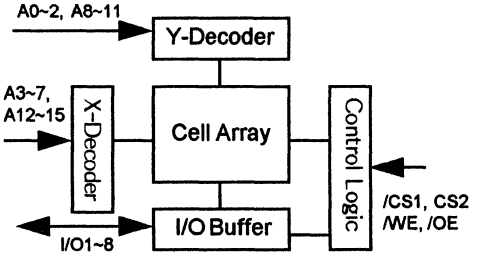
Product List	Operating Temp.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM68V512AL-L	Commercial	3.0~3.6V	70/100	32-SOP	10uA	40mA
KM68U512AL-L	(0~70 °C)	2.7~3.3V	100	32-TSOP(I) F	10uA	
KM68V512ALE-L	Extended	3.0~3.6V	70/100	32-SOP	20uA	
KM68U512ALE-L	(-25~85 °C)	2.7~3.3V	100	32-TSOP(I) F	15uA	
KM68V512ALI-L	Industrial	3.0~3.6V	70/100	32-SOP	20uA	
KM68U512ALI-L	(-40~85 °C)	2.7~3.3V	100	32-TSOP(I) F	15uA	

PIN DESCRIPTION





FUNCTIONAL BLOCK DIAGRAM



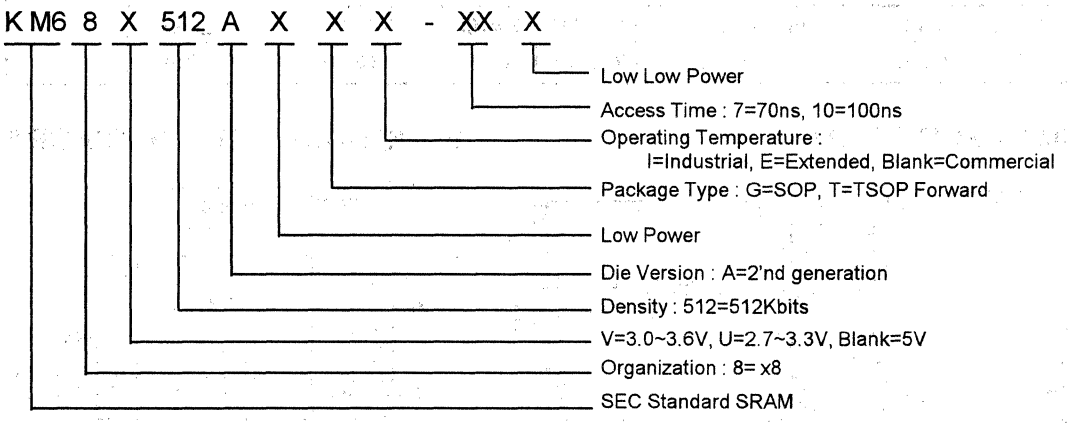
Pin Name	Function
A0~A15	Address Inputs
/WE	Write Enable Input
/CS1, CS2	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power
Vss	Ground
N.C	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
KM68V512ALG-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGE-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGI-7L	32-SOP, 70ns, 3.3V, LL
KM68V512ALG-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGE-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGI-10L	32-SOP, 100ns, 3.3V, LL
KM68V512ALT-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTE-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTI-7L	32-TSOP F, 70ns, 3.3V, LL
KM68V512ALT-10L	32-TSOP F, 100ns, 3.3V, LL	KM68V512ALTE-10L	32-TSOP F, 100ns, 3.3V, LL	KM68V512ALTI-10L	32-TSOP F, 100ns, 3.3V, LL
KM68U512ALG-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGE-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGI-10L	32-SOP, 100ns, 3.0V, LL
KM68U512ALT-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTE-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTI-10L	32-TSOP F, 100ns, 3.0V, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Pd	0.7	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	68V512AL-L, 68U512AL-L
		-25 to 85	°C	68V512ALE-L, 68U512ALE-L
		-40 to 85	°C	68V512ALI-L, 68U512ALI-L
Soldering temperature and time	Tsolder	260 °C , 10sec (Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V512A Family	3.0	3.3	3.6	V
		KM68U512A Family	2.7	3.0	3.3	
Ground	Vss	All Family	0	0	0	V
Input high voltage	Vih	KM68V512A Family	2.2	-	Vcc+0.3	V
		KM68U512A Family	2.2	-	Vcc+0.3	
Input low voltage	Vil	KM68V512A Family	-0.3***	-	0.4	V
		KM68U512A Family	-0.3***	-	0.4	

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

** Ta=25 °C

*** Vil(min)=-3.0V for ≤30ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

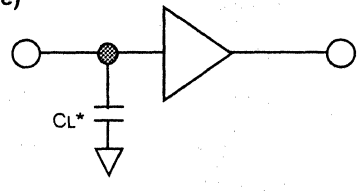
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS1=Vih or CS2=Vil or /WE=Vil, Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS1=Vil, CS2=Vih Vin=Vih or Vil, Iio=0mA		-	-	5	mA
Average operating current		Icc1	1uS Cycle 100% duty, Iio=0mA /CS1≤0.2V, CS2≥Vcc-0.2V		-	-	5	mA
		Icc2	/CS1=Vil, CS2=Vih Min cycle, 100% duty, Iio=0mA		-	-	40	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS1=Vih, CS2=Vil		-	-	0.3	mA
Standby Current (CMOS)	68V512AL-L	Isb1	/CS1≥Vcc-0.2V CS2≥Vcc-0.2V or CS2≤0.2V	LL	- -	- -	10	uA
	68V512ALE-L 68V512ALI-L			LL	- -	- -	20	uA
	68U512AL-L			LL	-	-	10	uA
	68U512ALE-L 68U512ALI-L			LL	-	-	15	uA

* 1) Commercial Product : Ta=0 to 70 °C , Vcc=3.3 +/- 0.3V(68V512A Family), Vcc=3.0 +/- 0.3V(68U512A Family)
2) Extended Product : Ta=-25 to 85 °C , Vcc=3.3 +/- 0.3V(68V512AE Family), Vcc=3.0 +/- 0.3V(68U512AE Family
3) Industrial Product : Ta=-40 to 85 °C , Vcc=3.3 +/- 0.3V(68V512AI Family), Vcc=3.0 +/- 0.3V(68U512AI Family
** Ta=25 °C

A.C CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rise and fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	CL=100pF+1TTL	-



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V512AL-L	0~70 °C	3.3V +/- 0.3	70/100ns	Commercial
KM68V512ALE-L	-25~85 °C	3.3V +/- 0.3	70/100ns	Extended
KM68V512ALI-L	-40~85 °C	3.3V +/- 0.3	70/100ns	Industrial
KM68U512AL-L	0~70 °C	3.0V +/- 0.3	100ns	Commercial
KM68U512ALE-L	-25~85 °C	3.0V +/- 0.3	100ns	Extended
KM68U512ALI-L	-40~85 °C	3.0V +/- 0.3	100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins				Units
			70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	100	-	ns
	Address access time	tAA	-	70	-	100	ns
	Chip select to output	tCO	-	70	-	100	ns
	Output enable to valid output	tOE	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	100	-	ns
	Chip select to end of write	tCW	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	ns
	Write pulse width	tWP	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns

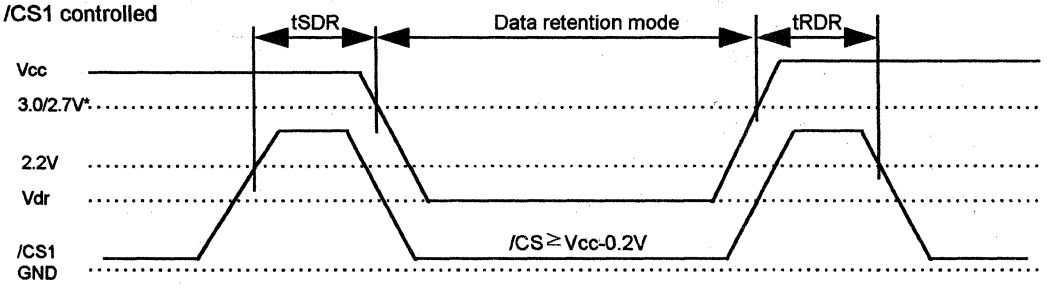
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS*** ≥ Vcc-0.2V		2.0	-	3.6	V
Data retention current	Idr	68V512AL-L	Vcc=3.0V	LL-Ver	-	-	10	uA
		68V512ALE-L	/CS1 ≥ Vcc-0.2V	LL-Ver	-	-	15	
		68V512ALI-L		LL-Ver	-	-	15	
		68U512AL-L		LL-Ver	-	-	10	
		68U512ALE-L		LL-Ver	-	-	15	
		68U512ALI-L		LL-Ver	-	-	15	
Data retention set-up time	tSDR		See data retention		0	-	-	ms
Recovery time	tRDR		wave form		5	-	-	

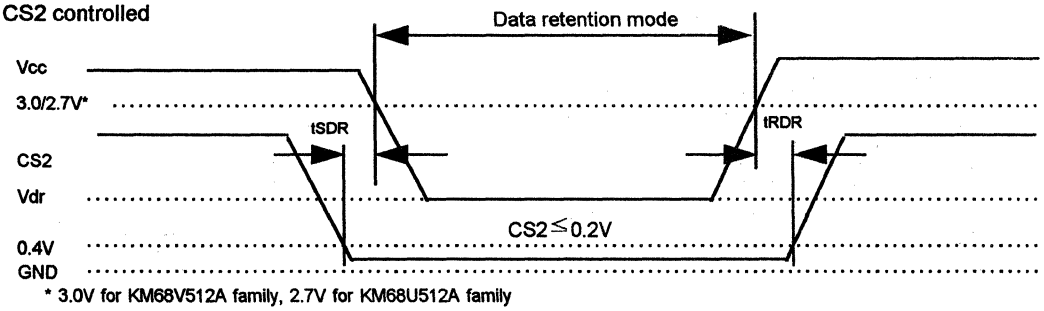
* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C , nless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C
*** /CS1 ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V(/CS1 controlled) or CS2 ≤ 0.2V(CS2 controlled)

DATA RETENTION TIMING DIAGRAM

1) /CS1 controlled



2) CS2 controlled

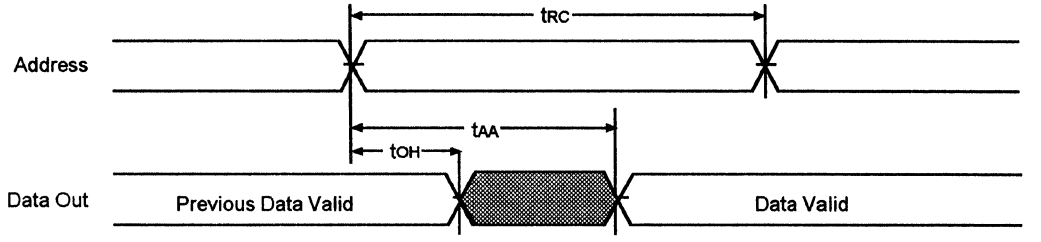


* 3.0V for KM68V512A family, 2.7V for KM68U512A family

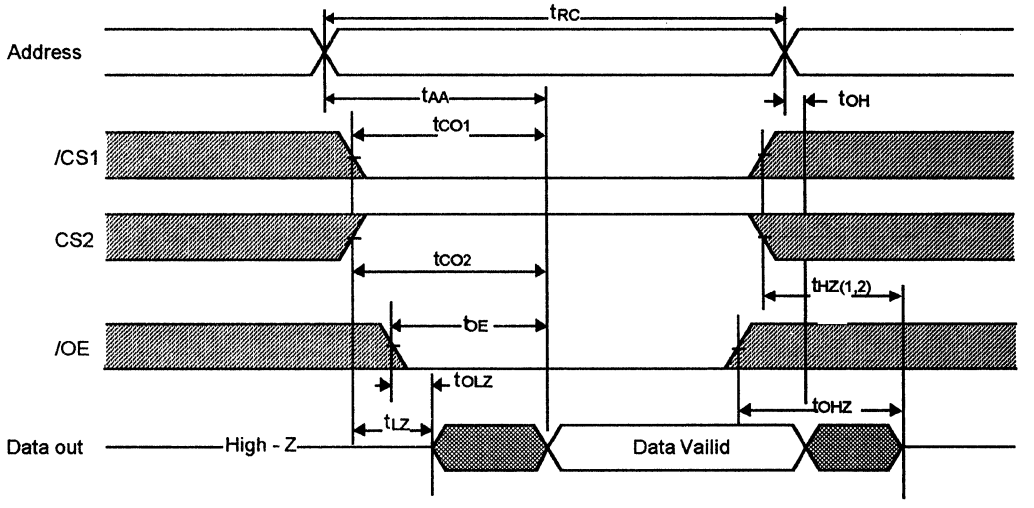
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE (1)(Address Controlled)

(/CS1=/OE=Vil, CS2=/WE=Vih)



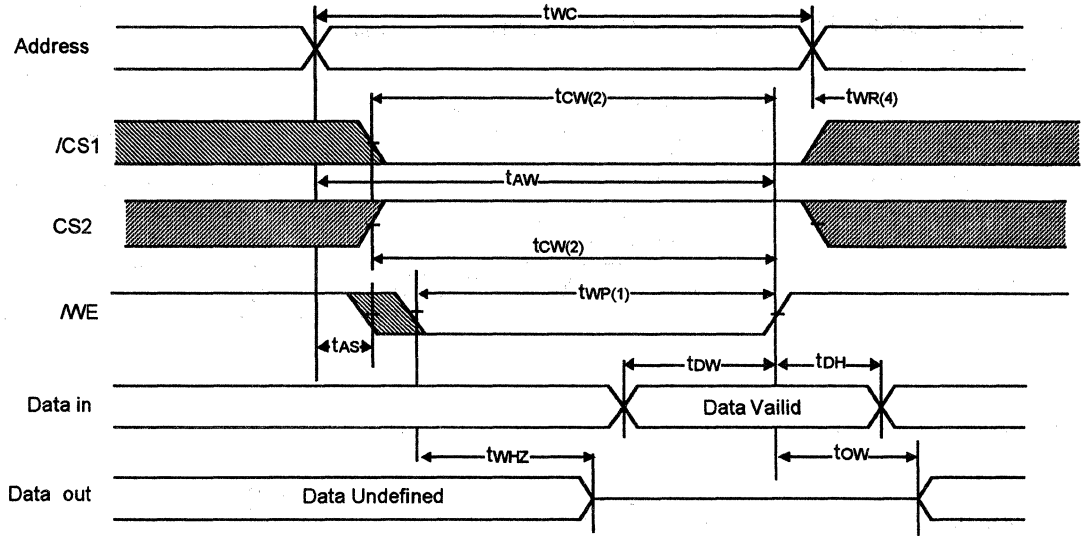
TIMING WAVE FORM OF READ CYCLE(2) (/WE= VIH)



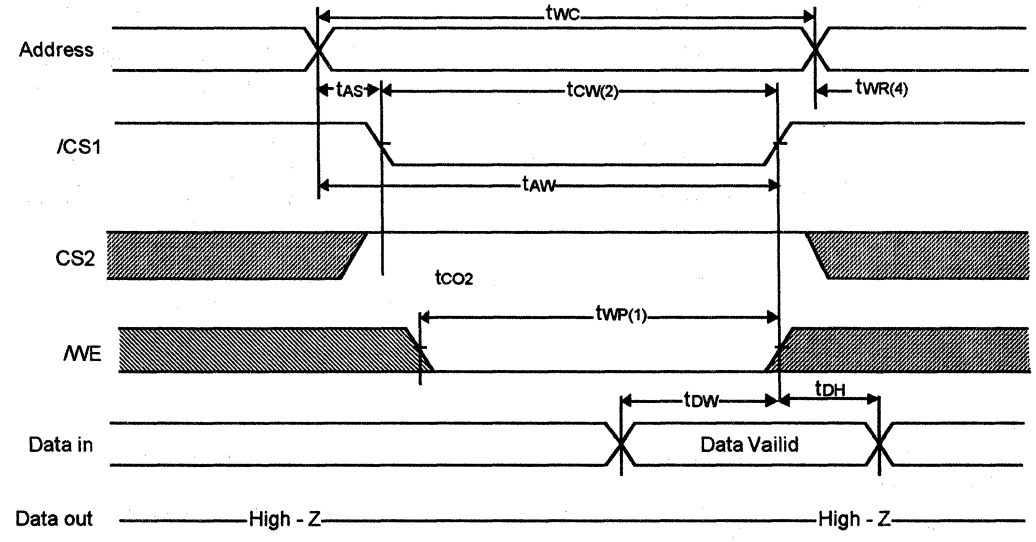
Notes(Read Cycle)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max) is less than tLZ(Min) both for a given device and device to device interconnection.

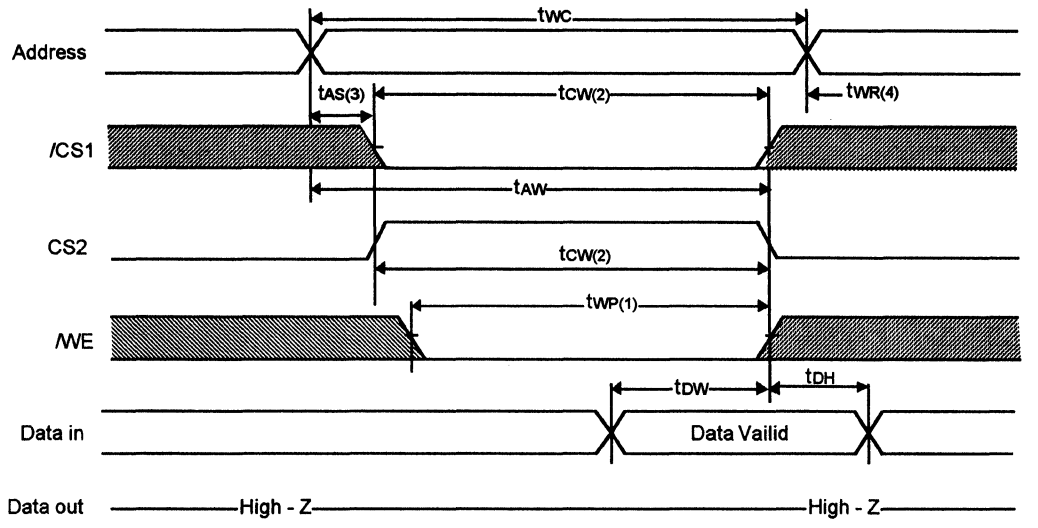
TIMING WAVE FORM OF WRITE CYCLE(1) (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (/CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



Notes(Write Cycle)

1. A write occurs during the overlap of a low /CS1, a high CS2 and a low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low. A write ends at the earliest transition among /CS1 going high, CS2 going low and /WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends at/CS1, or /WE going high, tWR applied in case a write ends at CS2 going to low.

FUNCTIONAL DESCRIPTION

/CS1	CS2	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	Isb, Isb1
X	L	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	H	Ouput Diable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

* X means don't care

128Kx8 bit Low Power & Low Vcc CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.6 um CMOS
- Organization : 128K x8
- Power Supply Voltage
  KM68V1000B family : 3.3V +/- 0.3V
  KM68U1000B family : 3.0V +/- 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

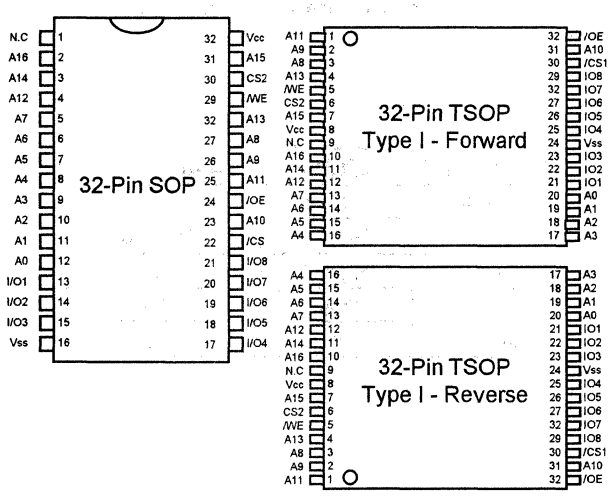
The KM68V1000B and KM68U1000B family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

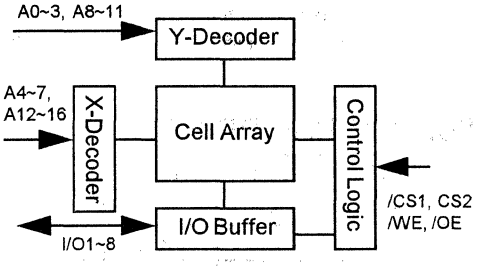
Product List	Operating Temp.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM68V1000BL/L-L	Commercial	3.0~3.6V	70*/100	32-SOP	50/15uA	40mA
KM68U1000BL/L-L	(0~70 °C)	2.7~3.3V	100	32-TSOP(I) R/F	50/15uA	
KM68V1000BLE/LE-L	Extended	3.0~3.6V	70*/100	32-SOP	100/20uA	
KM68U1000BLE/LE-L	(-25~85 °C)	2.7~3.3V	100	32-TSOP(I) R/F	50/15uA	
KM68V1000BLI/LI-L	Industrial	3.0~3.6V	70*/100	32-SOP	100/20uA	
KM68U1000BLI/LI-L	(-40~85 °C)	2.7~3.3V	100	32-TSOP(I) R/F	50/15uA	

* measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



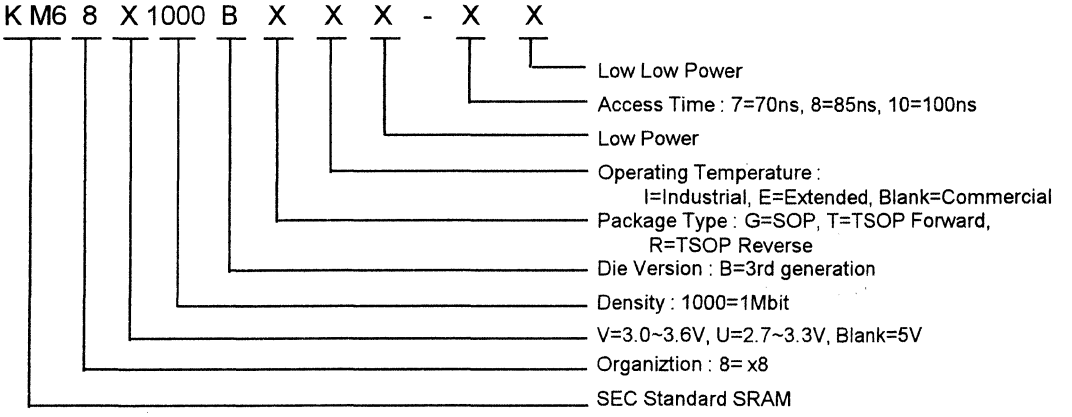
Pin Name	Function
A0~A16	Address Inputs
/WE	Write Enable Input
/CS1, CS2	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power
Vss	Ground
N.C	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
KM68V1000BLG-7	32-SOP, 70ns, 3.3V, L	KM68V1000BLGE-7	32-SOP, 70ns, 3.3V, L	KM68V1000BLGI-7	32-SOP, 70ns, 3.3V, L
KM68V1000BLG-7L	32-SOP, 70ns, 3.3V, LL	KM68V1000BLGE-7L	32-SOP, 70ns, 3.3V, LL	KM68V1000BLGI-7L	32-SOP, 70ns, 3.3V, LL
KM68V1000BLG-10	32-SOP, 100ns, 3.3V, L	KM68V1000BLGE-10	32-SOP, 100ns, 3.3V, L	KM68V1000BLGI-10	32-SOP, 100ns, 3.3V, L
KM68V1000BLG-10L	32-SOP, 100ns, 3.3V, LL	KM68V1000BLGE-10L	32-SOP, 100ns, 3.3V, LL	KM68V1000BLGI-10L	32-SOP, 100ns, 3.3V, LL
KM68V1000BLT-7	32-TSOP F, 70ns, 3.3V, L	KM68V1000BLTE-7	32-TSOP F, 70ns, 3.3V, L	KM68V1000BLTI-7	32-TSOP F, 70ns, 3.3V, L
KM68V1000BLT-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V1000BLTE-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V1000BLTI-7L	32-TSOP F, 70ns, 3.3V, LL
KM68V1000BLT-10	32-TSOP F, 100ns, 3.3V, L	KM68V1000BLTE-10	32-TSOP F, 100ns, 3.3V, L	KM68V1000BLTI-10	32-TSOP F, 100ns, 3.3V, L
KM68V1000BLT-10L	32-TSOP F, 100ns, 3.3V, LL	KM68V1000BLTE-10L	32-TSOP F, 100ns, 3.3V, LL	KM68V1000BLTI-10L	32-TSOP F, 100ns, 3.3V, LL
KM62V1000BLR-7	32-TSOP R, 70ns, 3.3V, L	KM62V1000BLRE-7	32-TSOP R, 70ns, 3.3V, L	KM62V1000BLRI-7	32-TSOP R, 70ns, 3.3V, L
KM62V1000BLR-7L	32-TSOP R, 70ns, 3.3V, LL	KM62V1000BLRE-7L	32-TSOP R, 70ns, 3.3V, LL	KM62V1000BLRI-7L	32-TSOP R, 70ns, 3.3V, LL
KM68V1000BLR-10	32-TSOP R, 100ns, 3.3V, L	KM68V1000BLRE-10	32-TSOP R, 100ns, 3.3V, L	KM68V1000BLRI-10	32-TSOP R, 100ns, 3.3V, L
KM68V1000BLR-10L	32-TSOP R, 100ns, 3.3V, LL	KM68V1000BLRE-10L	32-TSOP R, 100ns, 3.3V, LL	KM68V1000BLRI-10L	32-TSOP R, 100ns, 3.3V, LL
KM68U1000BLG-8	32-SOP, 85ns, 3.0V, L	KM68U1000BLGE-10	32-SOP, 100ns, 3.0V, L	KM68U1000BLGI-10	32-SOP, 100ns, 3.0V, L
KM68U1000BLG-8L	32-SOP, 85ns, 3.0V, LL	KM68U1000BLGE-10L	32-SOP, 100ns, 3.0V, LL	KM68U1000BLGI-10L	32-SOP, 100ns, 3.0V, LL
KM68U1000BLG-10	32-SOP, 100ns, 3.0V, L	KM68U1000BLTE-10	32-TSOP F, 100ns, 3.0V, L	KM68U1000BLTI-10	32-TSOP F, 100ns, 3.0V, L
KM68U1000BLG-10L	32-SOP, 100ns, 3.0V, LL	KM68U1000BLTE-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U1000BLTI-10L	32-TSOP F, 100ns, 3.0V, LL
KM68U1000BLT-8	32-TSOP F, 85ns, 3.0V, L	KM68U1000BLRE-10	32-TSOP R, 100ns, 3.0V, L	KM68U1000BLRI-10	32-TSOP R, 100ns, 3.0V, L
KM68U1000BLT-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U1000BLRE-10L	32-TSOP R, 100ns, 3.0V, LL	KM68U1000BLRI-10L	32-TSOP R, 100ns, 3.0V, LL
KM68U1000BLT-10	32-TSOP F, 100ns, 3.0V, L				
KM68U1000BLT-10L	32-TSOP F, 100ns, 3.0V, LL				
KM68U1000BLR-8	32-TSOP R, 85ns, 3.0V, L				
KM68U1000BLR-8L	32-TSOP R, 85ns, 3.0V, LL				
KM68U1000BLR-10	32-TSOP R, 100ns, 3.0V, L				
KM68U1000BLR-10L	32-TSOP R, 100ns, 3.0V, LL				

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Pd	0.7	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	68V1000BL/L-L, 68U1000BL/L-L
		-25 to 85	°C	68V1000BLE/LE-L, 68U1000BLE/LE-L
		-40 to 85	°C	68V1000BLI/LI-L, 68U1000BLI/LI-L
Soldering temperature and time	Tsolder	260 °C , 10sec (Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V100B Family	3.0	3.3	3.6	V
		KM68U100B Family	2.7	3.0	3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	Vih	KM68V100B Family	2.2	-	Vcc+0.3	V
		KM68U100B Family	2.2	-	Vcc+0.3	V
Input low voltage	Vil	KM68V100B Family	-0.3***	-	0.4	V
		KM68U100B Family	-0.3***	-	0.4	V

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤30ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

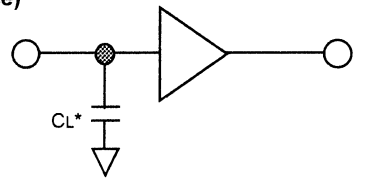
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS1=Vih or CS2=Vil or /WE=Vil, Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS1=Vil, CS2=Vih Vin=Vih or Vil, Iio=0mA		-	2	5	mA
Average operating current		Icc1	1uS Cycle 100% duty, Iio=0mA /CS1≤0.2V, CS2≥Vcc-0.2V		-	3	5	mA
		Icc2	/CS1=Vil, CS2=Vih Min cycle, 100% duty, Iio=0mA		-	30	40	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.2	-	-	V
Standby Current(TTL)		Isb	/CS1=Vih, CS2=Vil		-	-	0.3	mA
Standby Current (CMOS)	68V1000BL/L-L	Isb1	/CS1≥Vcc-0.2V CS2≥Vcc-0.2V or CS2≤0.2V	L	-	1	50	uA
				LL	-	0.5	15	
	68V1000BLE/LE-L 68V1000BLI/LI-L			L	-	1	100	uA
				LL	-	0.5	20	
	68U1000BL/L-L			L	-	1	50	uA
				LL	-	0.5	15	
	68U1000BLE/LE-L 68U1000BLI/LI-L			L	-	1	50	uA
				LL	-	0.5	15	

* 1) Commercial Product : Ta=0 to 70 °C , Vcc=3.3 +/- 0.3V(68V1000B Family), Vcc=3.0 +/- 0.3V(68U1000B Family)
2) Extended Product : Ta=-25 to 85 °C , Vcc=3.3 +/- 0.3V(68V1000BE Family), Vcc=3.0 +/- 0.3V(68U1000BE Family)
3) Industrial Product : Ta=-40 to 85 °C , Vcc=3.3 +/- 0.3V(68V1000BI Family), Vcc=3.0 +/- 0.3V(68U1000BI Family)
** Ta= 25°C

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	CL=100pF+1TTL	-



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V1000BL/L-L	0~70 °C	3.3V +/- 0.3	70*/100ns	Commercial
KM68V1000BLE/LE-L	-25~85 °C	3.3V +/- 0.3	70*/100ns	Extended
KM68V1000BLI/LI-L	-40~85 °C	3.3V +/- 0.3	70*/100ns	Industrial
KM68U1000BL/L-L	0~70 °C	3.0V +/- 0.3	100ns	Commercial
KM68U1000BLE/LE-L	-25~85 °C	3.0V +/- 0.3	100ns	Extended
KM68U1000BLI/LI-L	-40~85 °C	3.0V +/- 0.3	100ns	Industrial

* measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins				Units
			70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	100	-	ns
	Address access time	tAA	-	70	-	100	ns
	Chip select to output	tCO	-	70	-	100	ns
	Output enable to valid output	tOE	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	100	-	ns
	Chip select to end of write	tCW	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	ns
	Write pulse width	tWP	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to ouput low-Z	tOW	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS*** ≥ Vcc-0.2V		2.0	-	3.6	V
Data retention current	Idr	68V1000BL	Vcc=3.0V	L-Ver	-	1	30	uA
		68V1000BL-L	/CS1 ≥ Vcc-0.2V	LL-Ver	-	0.5	15	
		68V1000BLE		L-Ver	-	-	50	
		68V1000BLE-L		LL-Ver	-	-	20	
		68V1000BLI		L-Ver	-	-	50	
		68V1000BLI-L		LL-Ver	-	-	20	
		68U1000BL		L-Ver	-	-	25	
		68U1000BL-L		LL-Ver	-	-	10	
		68U1000BLE		L-Ver	-	-	25	
		68U1000BLE-L		LL-Ver	-	-	15	
		68U1000BLI		L-Ver	-	-	25	
		68U1000BLI-L		LL-Ver	-	-	15	
Data retention set-up time	tSDR		See data retention waveform		0	-		ms
Recovery time	tRDR				5	-		

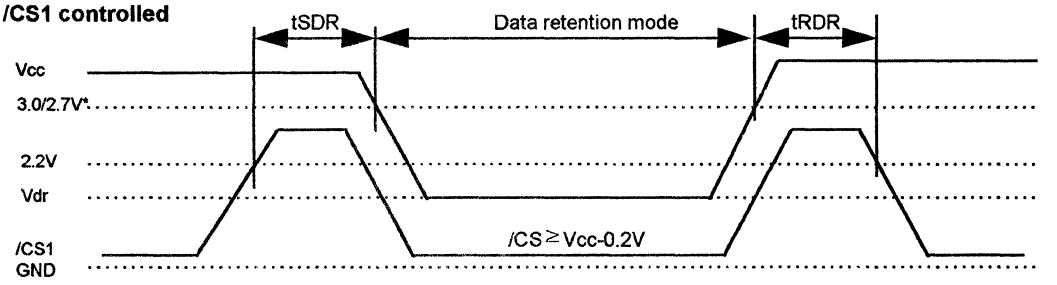
* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C , nless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

** Ta=25 °C

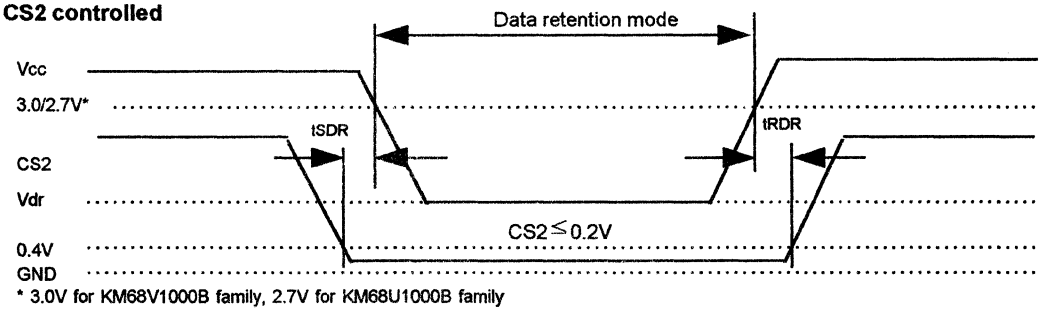
*** /CS1 ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V(/CS1 controlled) or CS2 ≤ 0.2V(CS2 controlled)

DATA RETENTION TIMING DIAGRAM

1) /CS1 controlled



2) CS2 controlled

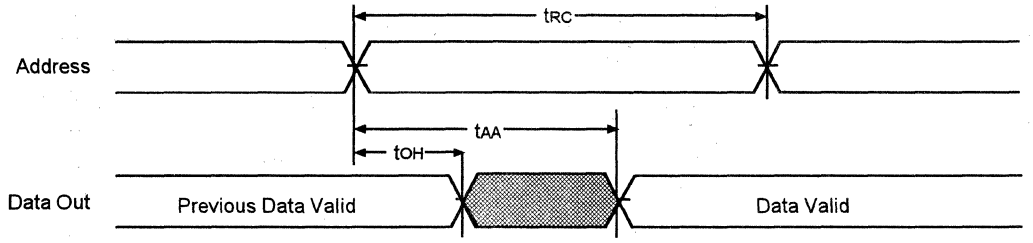


* 3.0V for KM68V1000B family, 2.7V for KM68U1000B family

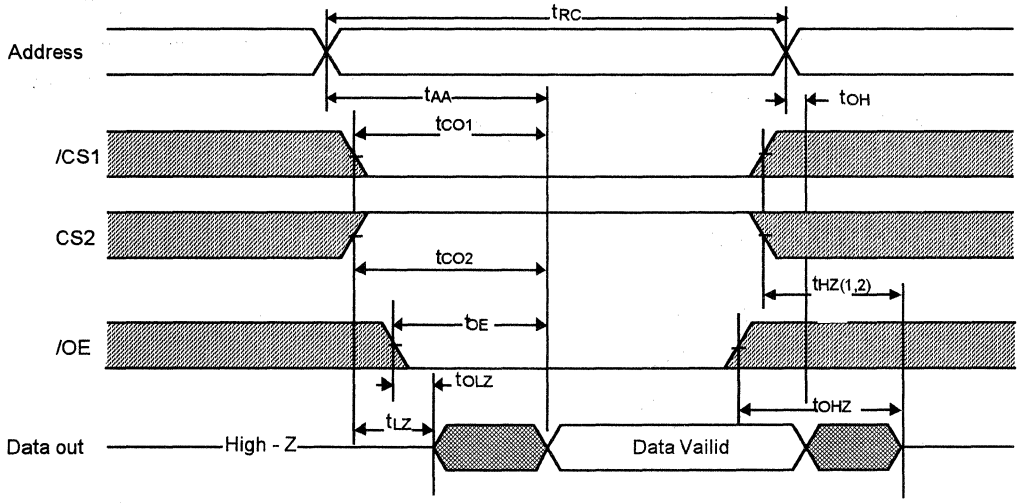
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, CS2=/WE=Vih)



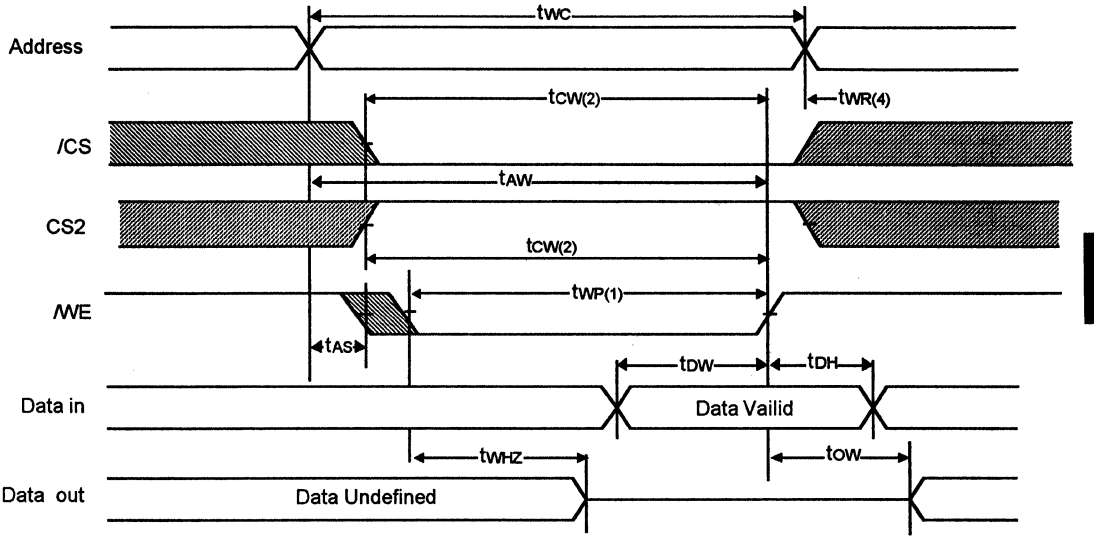
TIMING WAVEFORM OF READ CYCLE(2) (/WE= VIH)



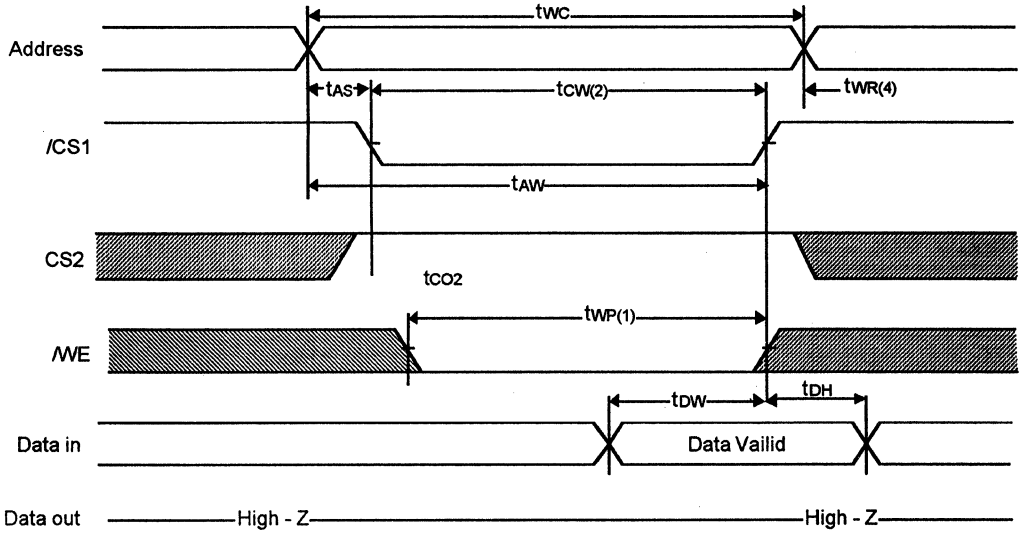
Notes(Read Cycle)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max) is less than tLZ(Min) both for a given device and device to device interconnection.

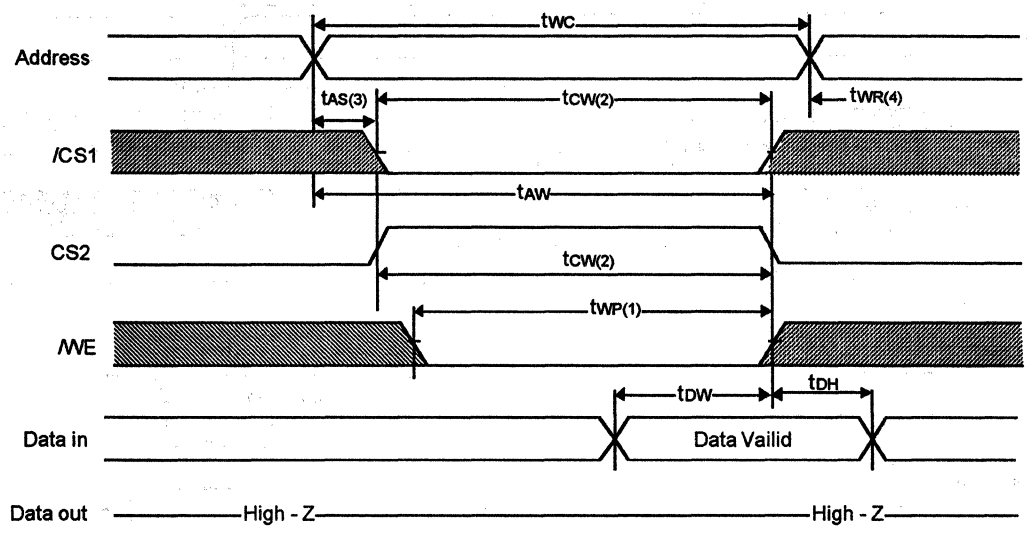
TIMING WAVEFORM OF WRITE CYCLE(1) (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (/CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



Notes(Write Cycle)

1. A write occurs during the overlap of a low /CS1, a high CS2 and a low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low. A write ends at the earliest transition among /CS1 going high, CS2 going low and /WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends at/CS1, or /WE going high, tWR2 applied in case a write ends at CS2 going to low.

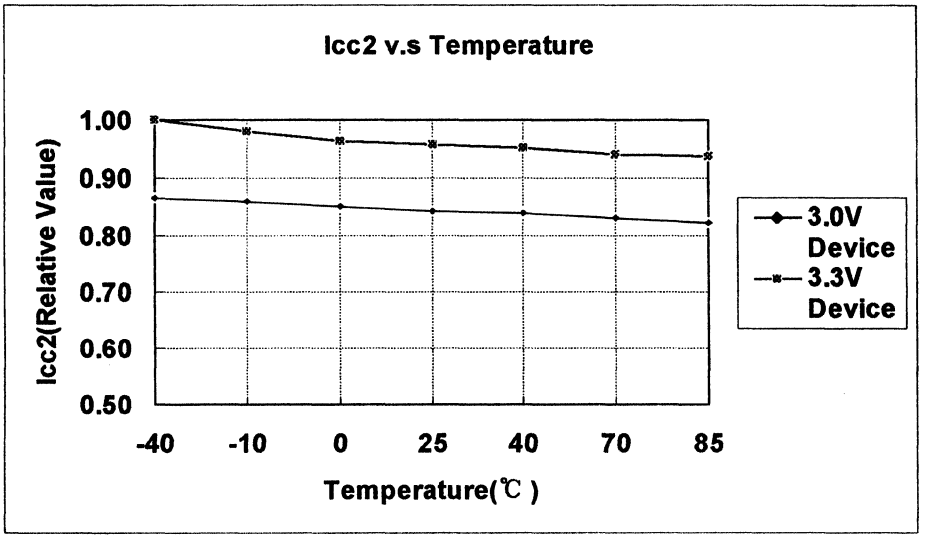
FUNCTIONAL DESCRIPTION

/CS1	CS2	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	Isb, Isb1
X	L	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	H	Ouput Diable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

TECHNICAL INFORMATION

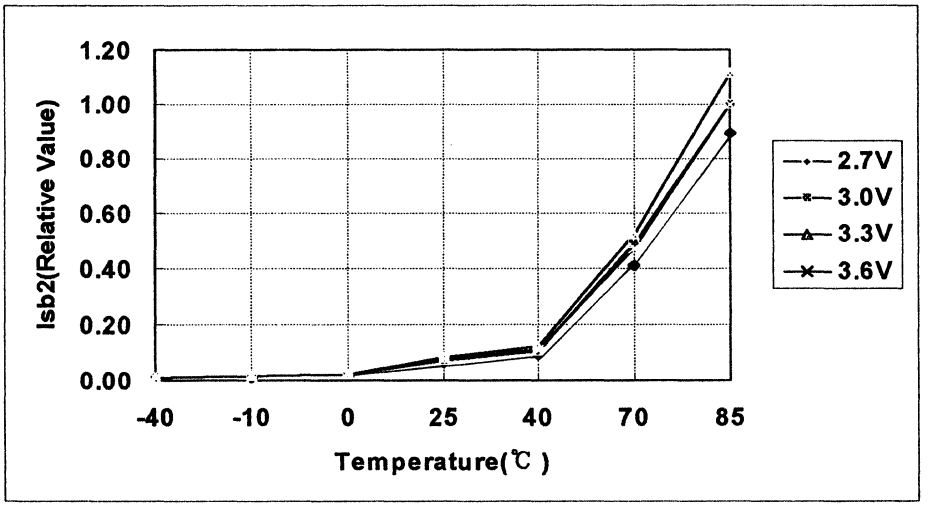
1) Icc2 characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and -40°C temperature. The basic relative value of Icc2 at that condition is set into 1.



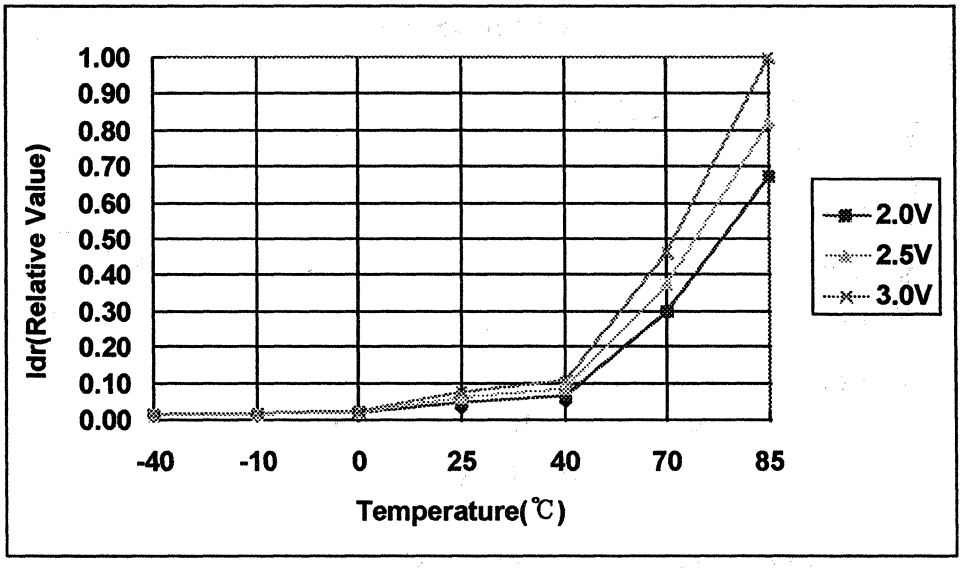
2) Isb1(CMOS Level Stanby Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 3.0V Vcc and 85°C temperature. The basic relative value of Isb1 at that condition is set into 1.



3) Idr(Data Retention Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at Vdr=3.0V and 85°C temperature. The basic relative value of Idr at that condition is set into 1.



64Kx16 bit Low Power & Low Vcc CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.6 um CMOS
- Organization : 64Kx16
- Data Byte Control : /LB=I/O1~8, /UB=I/O9~16
- Power Supply Voltage
  - KM616V1000B family : 3.3V +/- 0.3V
  - KM616U1000B family : 3.0V +/- 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  - 44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

The KM616V1000B and KM616U1000B family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

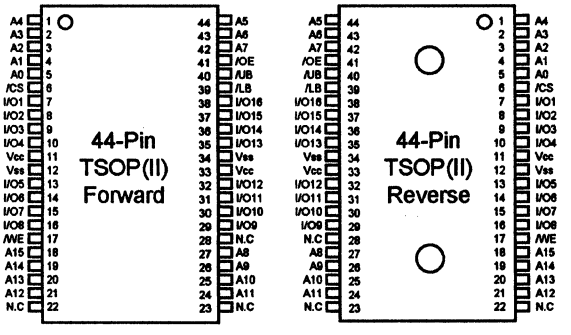
2

PRODUCT FAMILY

Product List	Operating Temp.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM616V1000BL/L-L	Commercial	3.0~3.6V	70*/100	44-TSOP(II)	50/15uA	65mA
KM616U1000BL/L-L	(0~70 °C)	2.7~3.3V	100	Foward/Reverse	50/15uA	
KM616V1000BLE/LE-L	Extended	3.0~3.6V	85*/100	44-TSOP(II)	100/20uA	
KM616U1000BLE/LE-L	(-25 ~85 °C)	2.7~3.3V	100	Foward/Reverse	100/20uA	
KM616V1000BLI/LI-L	Industrial	3.0~3.6V	85*/100	44-TSOP(II)	100/20uA	
KM616U1000BLI/LI-L	(-40~85 °C)	2.7~3.3V	100	Foward/Reverse	100/20uA	

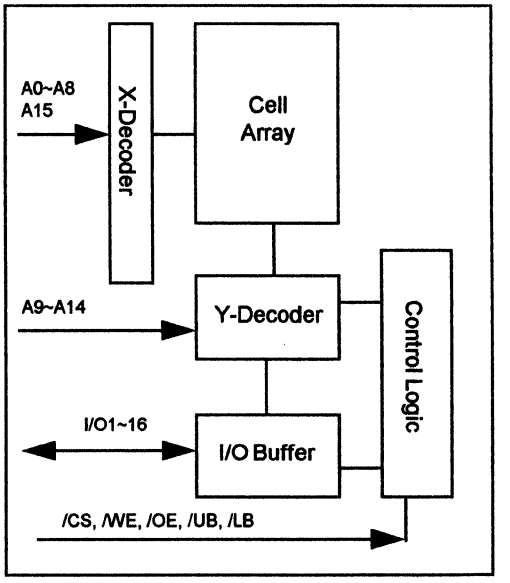
* measured with 30pF test load

PIN DESCRIPTION



Name	Function	Name	Function
A0~A15	Address Inputs	/LB	Lower Byte(I/O1~8)
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
/CS	Chip Select Input	Vcc	Power
/OE	Output Enable Input	Vss	Ground
I/O1~I/O16	Data Input/Output	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM

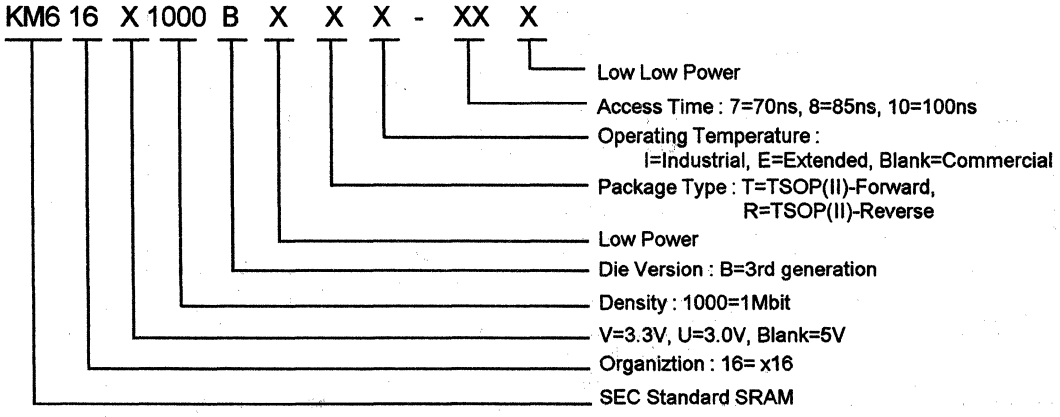


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM616V1000BLT-7	44-TSOP(II), F, 3.3V, 70ns, L	KM616V1000BLTE-8	F, 3.3V, 85ns, L	KM616V1000BLTI-8	44-TSOP(II), F, 3.3V, 85ns, L
KM616V1000BLT-7L	44-TSOP(II), F, 3.3V, 70ns, LL	KM616V1000BLTE-8L	F, 3.3V, 85ns, LL	KM616V1000BLTI-8L	44-TSOP(II), F, 3.3V, 85ns, LL
KM616V1000BLT-10	44-TSOP(II), F, 3.3V, 100ns, L	KM616V1000BLTE-10	F, 3.3V, 100ns, L	KM616V1000BLTI-10	44-TSOP(II), F, 3.3V, 100ns, L
KM616V1000BLT-10L	44-TSOP(II), F, 3.3V, 100ns, LL	KM616V1000BLTE-10L	F, 3.3V, 100ns, LL	KM616V1000BLTI-10L	44-TSOP(II), F, 3.3V, 100ns, LL
KM616U1000BLT-10	44-TSOP(II), F, 3.0V, 100ns, L	KM616U1000BLTE-10	F, 3.0V, 100ns, L	KM616U1000BLTI-10	44-TSOP(II), F, 3.0V, 100ns, L
KM616U1000BLT-10L	44-TSOP(II), F, 3.0V, 100ns, LL	KM616U1000BLTE-10L	F, 3.0V, 100ns, LL	KM616U1000BLTI-10L	44-TSOP(II), F, 3.0V, 100ns, LL
KM616V1000BLR-7	44-TSOP(II), R, 3.3V, 70ns, L	KM616V1000BLRE-8	R, 3.3V, 85ns, L	KM616V1000BLRI-8	44-TSOP(II), R, 3.3V, 85ns, L
KM616V1000BLR-7L	44-TSOP(II), R, 3.3V, 70ns, LL	KM616V1000BLRE-8L	R, 3.3V, 85ns, LL	KM616V1000BLRI-8L	44-TSOP(II), R, 3.3V, 85ns, LL
KM616V1000BLR-10	44-TSOP(II), R, 3.3V, 100ns, L	KM616V1000BLRE-10	R, 3.3V, 100ns, L	KM616V1000BLRI-10	44-TSOP(II), R, 3.3V, 100ns, L
KM616V1000BLR-10L	44-TSOP(II), R, 3.3V, 100ns, LL	KM616V1000BLRE-10L	R, 3.3V, 100ns, LL	KM616V1000BLRI-10L	44-TSOP(II), R, 3.3V, 100ns, LL
KM616U1000BLR-10	44-TSOP(II), R, 3.0V, 100ns, L	KM616U1000BLRE-10	R, 3.0V, 100ns, L	KM616U1000BLRI-10	44-TSOP(II), R, 3.0V, 100ns, L
KM616U1000BLR-10L	44-TSOP(II), R, 3.0V, 100ns, LL	KM616U1000BLRE-10L	R, 3.0V, 100ns, LL	KM616U1000BLRI-10L	44-TSOP(II), R, 3.0V, 100ns, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 4.6	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	616V1000BL/L-L, 616U1000BL/L-L
		-25 to 85	°C	616V1000BLE/LE-L, 616U1000BLE/LE-L
		-40 to 85	°C	616V1000BLI/LI-L, 616U1000BLI/LI-L
Soldering temperature and time	Tsolder	260'C, 10sec (Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616V100B Family	3.0	3.3	3.6	V
		KM616U100B Family	2.7	3.0	3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	Vih	KM616V100B Family	2.2	-	Vcc+0.3	V
		KM616U100B Family	2.2	-	Vcc+0.3	V
Input low voltage	Vil	KM616V100B Family	-0.3***	-	0.4	V
		KM616U100B Family	-0.3***	-	0.4	V

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤30ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS=Vih or /WE=Vil, /UB=Vih or /LB=Vih, Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc***	/CS=Vil, Vin=Vih or Vil, Iio=0mA	Read	-	-	10	mA
				Write			20	
Average operating current		Icc1***	Cycle time=1uS 100% duty /CS≤0.2V, Iio=0mA	Read	-	-	15	
				Write			25	
		Icc2	Min cycle, 100% duty /CS≤Vil, Iio=0mA		-	-	65	
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.2	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	0.5	mA
Standby Current (CMOS)	616V1000BL/L-L	Isb1	/CS≥Vcc-0.2V Vin≥Vcc-0.2V or Vin≤0.2V	L	-	-	50	uA
				LL	-	-	15	uA
	616V1000BLI/LI-L			L	-	-	100	uA
	616V1000BLE/LE-L			LL	-	-	20	uA
	616U1000BL/L-L			L	-	-	50	uA
				LL	-	-	15	uA
	616U1000BLI/LI-L			L	-	-	100	uA
	616U1000BLE/LE-L			LL	-	-	20	uA

* 1) Commercial Product : Ta=0 to 70 °C , Vcc=3.3 +/- 0.3V(616V1000B Family), Vcc=3.0 +/- 0.3V(616U1000B Family)
2) Extended Product : Ta=-25 to 85 °C , Vcc=3.3 +/- 0.3V(616V1000BE Family), Vcc=3.0 +/- 0.3V(616U1000BE Family)
3) Industrial Product : Ta=-40 to 85 °C , Vcc=3.3 +/- 0.3V(616V1000BI Family), Vcc=3.0 +/- 0.3V(616U1000BI Family)

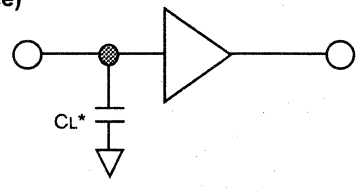
** Typ : Ta=25 °C

*** Industrial Products : Icc(Read/Write)=15mA/25mA, Icc1(Read/Write)=20mA/30mA

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.4V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics
** for 70ns, 85ns products

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM616V1000BL/L-L	0~70 °C	3.3V +/- 0.3	70*/100ns	Commercial
KM616V1000BLE/LE-L	-25~85 °C	3.3V +/- 0.3	85*/100ns	Extended
KM616V1000BLI/LI-L	-40~85 °C	3.3V +/- 0.3	85*/100ns	Industrial
KM616U1000BL/L-L	0~70 °C	3.0V +/- 0.3	100ns	Commercial
KM616U1000BLE/LE-L	-25~85 °C	3.0V +/- 0.3	100ns	Extended
KM616U1000BLI/LI-L	-40~85 °C	3.0V +/- 0.3	100ns	Industrial

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			70ns*		85ns*		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	/UB, /LB Access Time	tBA	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	/UB, /LB enable to low-Z output	tBLZ	5	-	5	-	5	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	/UB, /LB disable to high-Z output	tBHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	/UB, /LB valid to end of write	tBW	60	-	70		80	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

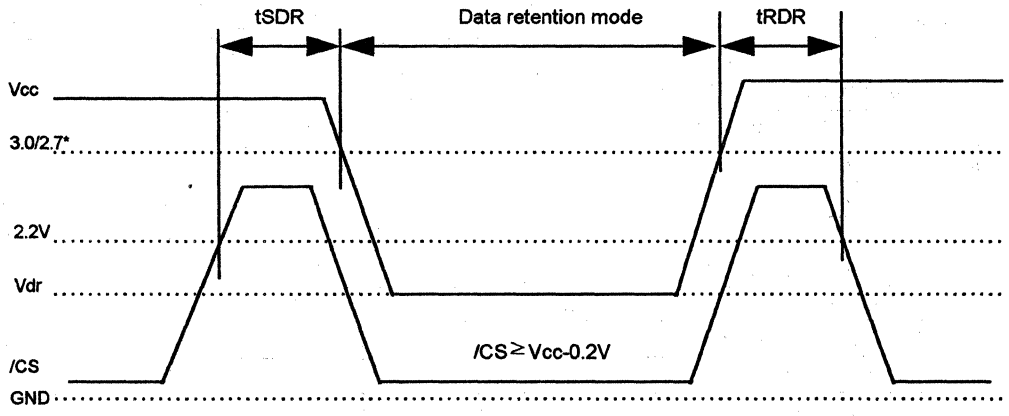
* All the parameters are measured with 30pF test load

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS≥Vcc-0.2V		2.0	-	3.6	V
Data retention current	Idr	616V1000BL/L-L	Vcc=3.0V	L-Ver	-	-	30	uA
			/CS≥Vcc-0.2V	LL-Ver	-	-	15	
		616V1000BLE/LE-L		L-Ver	-	-	50	
		616V1000BLI/LI-L		LL-Ver	-	-	20	
		68U1000BL/L-L		L-Ver	-	-	30	
				LL-Ver	-	-	15	
		616U1000BLE/LE-L		L-Ver	-	-	50	
		616U1000BLI/LI-L		LL-Ver	-	-	20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C , unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C

DATA RETENTION TIMING DIAGRAM

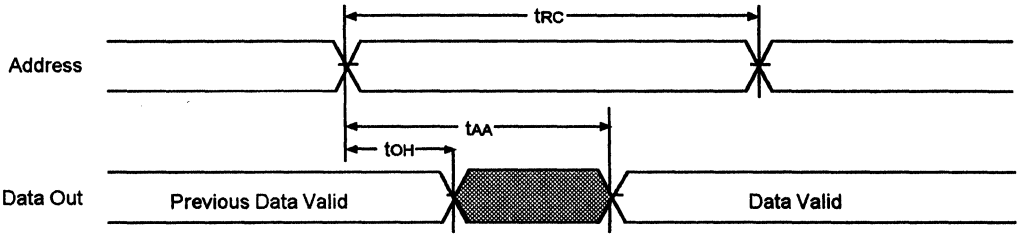


* 2.7V for KM616U1000B family, 3.0V for KM616V1000B family

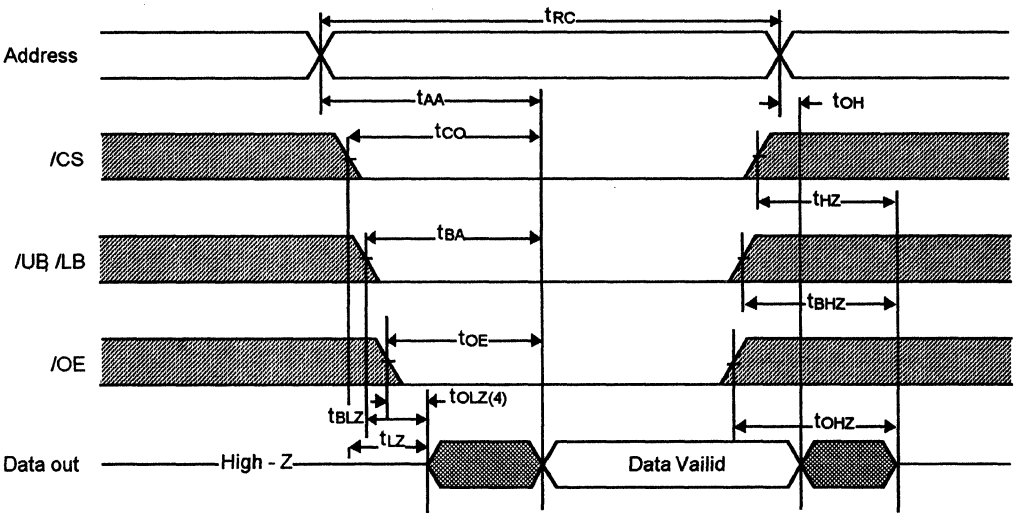
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE (1)(Address Controlled)

(/CS=/OE=Vil, /WE=Vih, /UB or, and /LB=Vil)



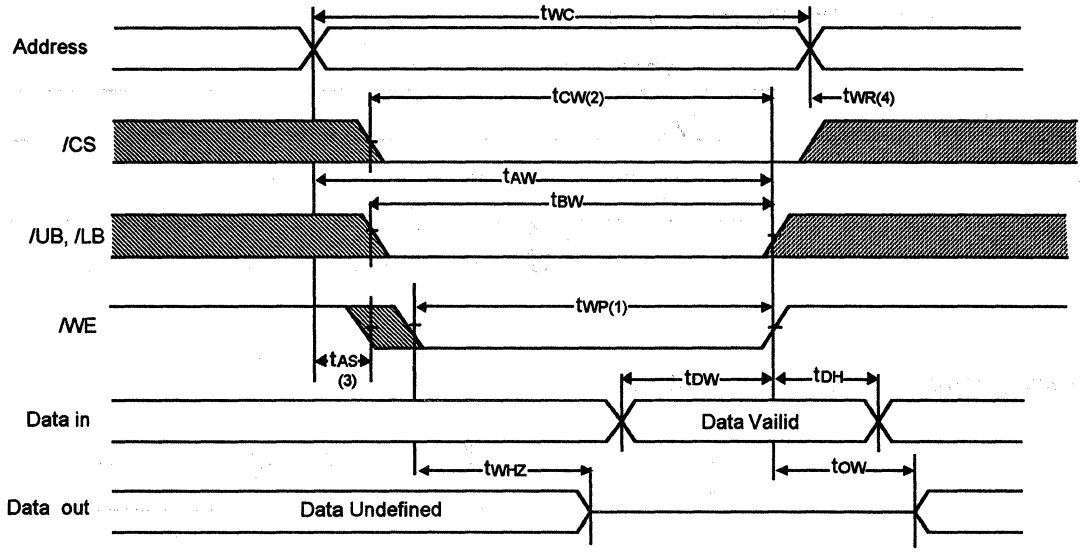
TIMING WAVE FORM OF READ CYCLE (/WE= VIH)



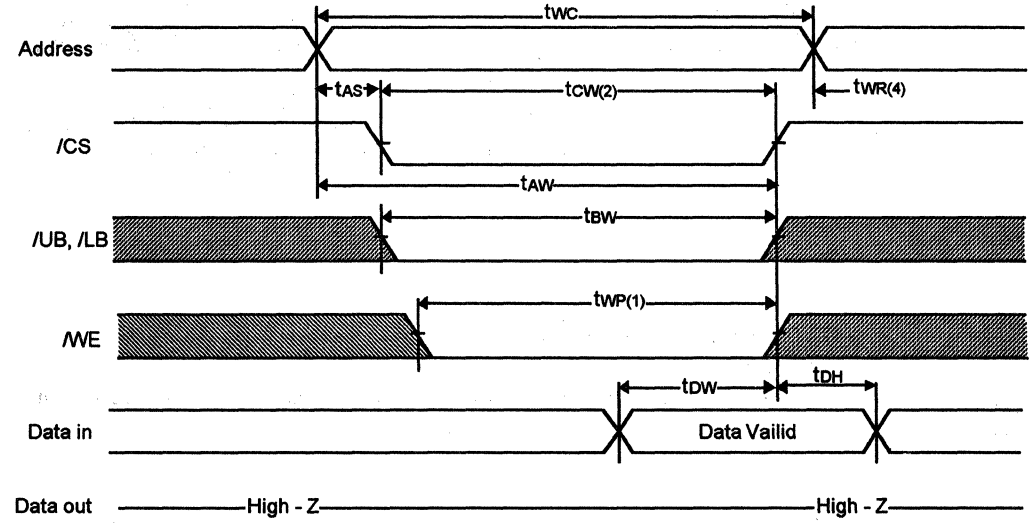
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.)both for a given device and from device to device.

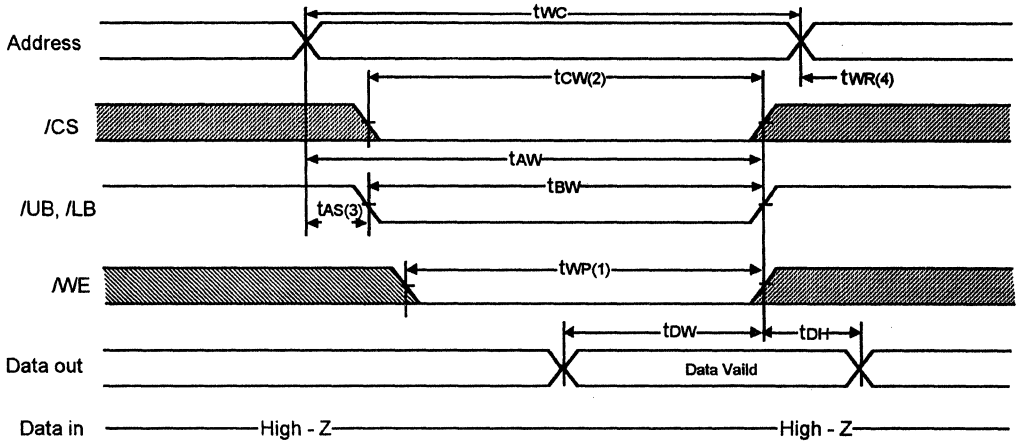
TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/UB,/ LB Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CSand low /WE. A write begins at the latest transition among /CS going low and WE going low : A write end at the earliest transition among /CSgoing high and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS,or /WE going high.

FUNCTIONAL DESCRIPTION

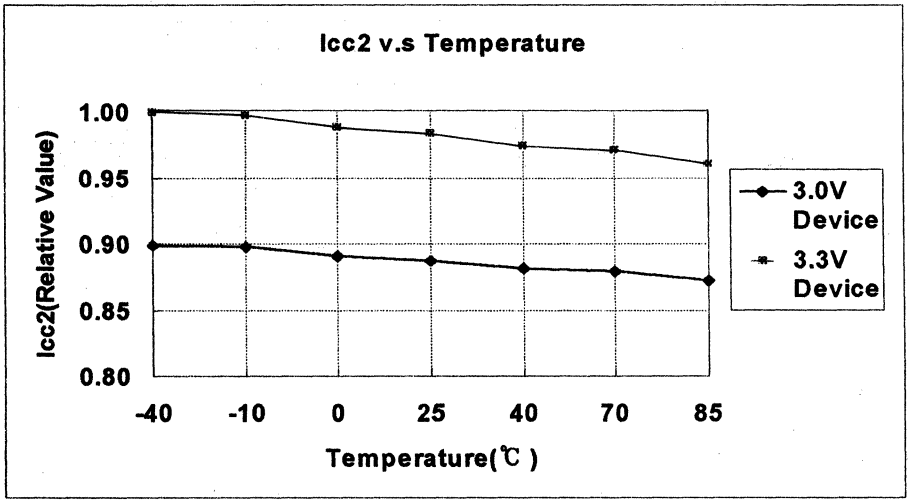
/CS	/UB	/LB	/WE	/OE	Mode	I/O1~8	I/O 9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	Isb, Isb1
L	X	X	H	H	Ouput	High-Z	High-Z	Icc
L	H	H	X	X	Disable	High-Z	High-Z	
L	L	H	H	L	Read	Dout	High-Z	Icc
	H	L				High-Z	Dout	
	L	L				Dout	Dout	
L	L	H	L	X	Write	Din	High-Z	Icc
	H	L				High-Z	Din	
	L	L				Din	Din	

* X means don't care

TECHNICAL INFORMATION

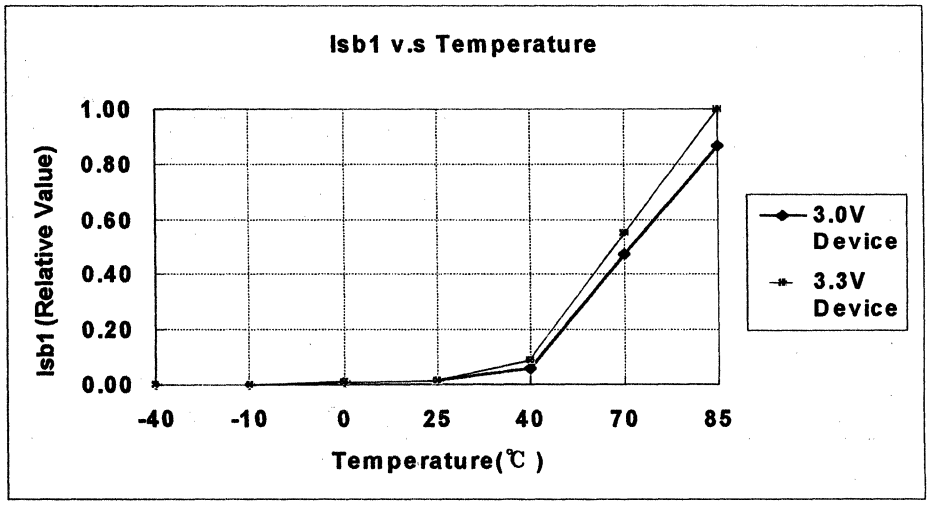
1) Icc2 characteristics by temperature varition

All the values in this graph is depicted by the relative value with the maximum value measured at 3.3V Vcc and -40°C temperature. The basic relative value of Icc2 at that condition is set into 1.



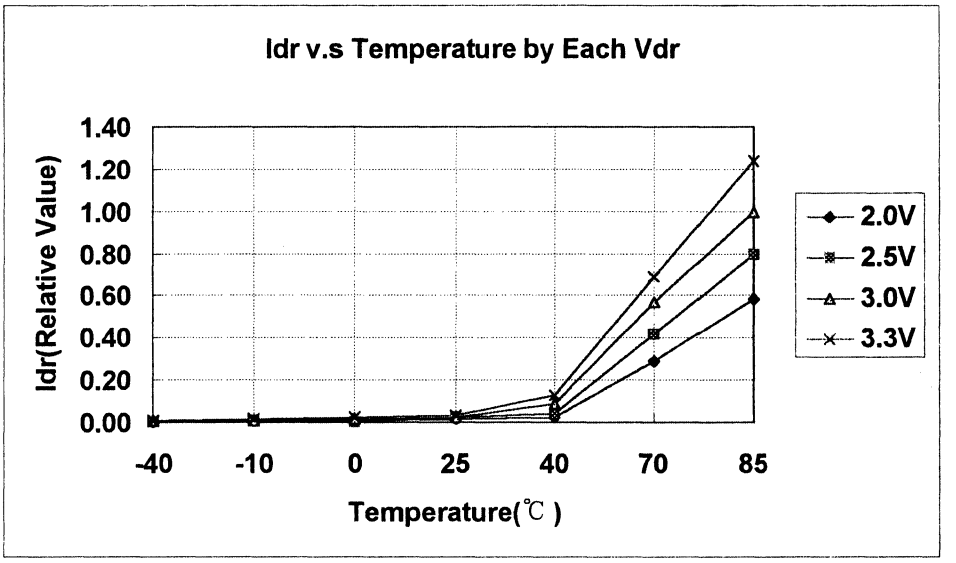
2) Isb1(CMOS Level Stanby Current) characteristics by temperature variation

All the values in this graph is depicted by the relative value with the maximum value measured at 3.3V Vcc and 85°C temperature. The basic relative value of Isb1 at that condition is set into 1.



3) Idr(Data Retention Current) characteristics by temperature variation

All the values in this graph is depicted by the relative value with the maximum value measured at Vdr=3.0V and 85°C temperature. The basic relative value of Idr at that condition is set into 1.



512Kx8 bit Low Power & Low Vcc CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.4 um CMOS
- Organization : 512K x 8
- Power Supply Voltage : 3.3 +/- 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

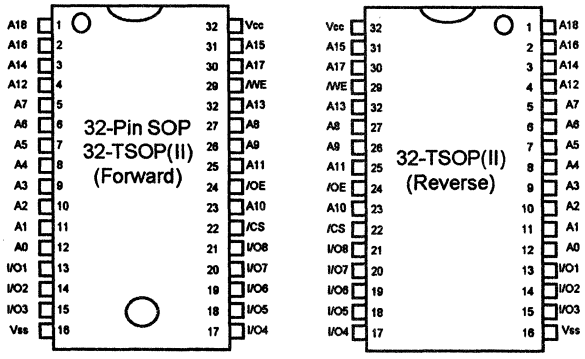
The KM68V4000A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product List	Operating Temp.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM68V4000AL KM68V4000AL-L	Commercial (0~70 °C)	3.0~3.6V	70*/100	32-SOP 32-TSOP(II)-R/F	50/15uA	50mA
KM68V4000ALI KM68V4000ALI-L	Industrial (-40~85 °C)	3.0~3.6V	70*/100	32-SOP 32-TSOP(II)-R/F	50/20uA	

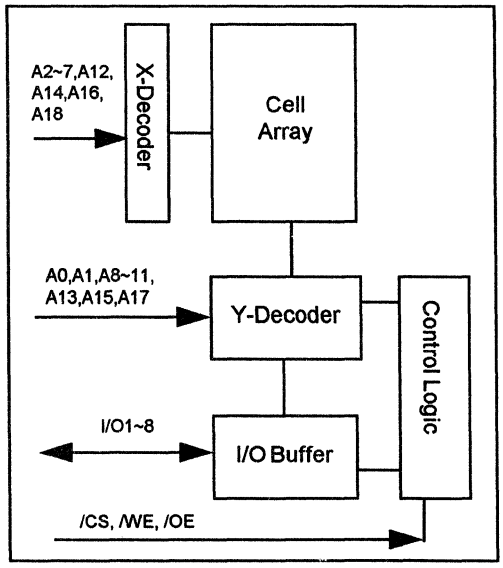
* measured with 30pF test load

PIN DESCRIPTION



Name	Function	Name	Function
A0~A18	Address Inputs	Vcc	Power
/WE	Write Enable Input	Vss	Ground
/CS	Chip Select Input		
/OE	Output Enable Input		
I/O1~I/o8	Data Input/Output		

FUNCTIONAL BLOCK DIAGRAM

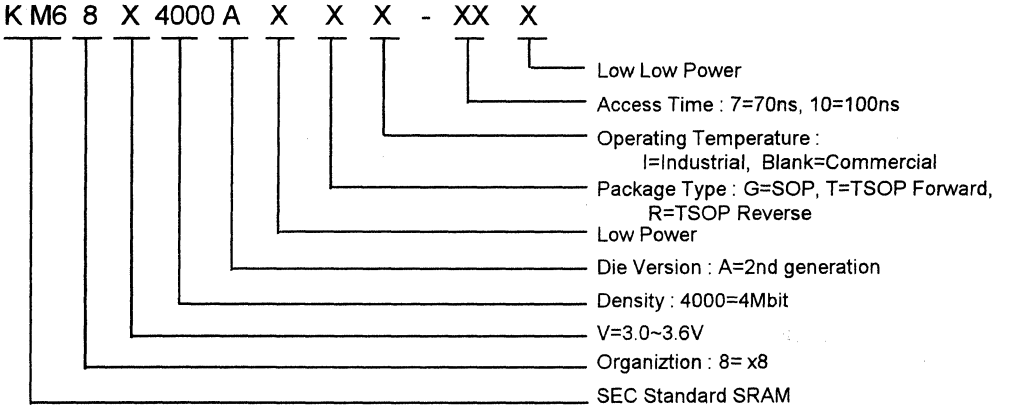


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**
KM68V4000ALG-7	32-SOP, 70ns, 3.3V, L	KM68V4000ALGI-7	32-SOP, 70ns, 3.3V, L
KM68V4000ALG-7L	32-SOP, 70ns, 3.3V, LL	KM68V4000ALGI-7L	32-SOP, 70ns, 3.3V, LL
KM68V4000ALG-10	32-SOP, 100ns, 3.3V, L	KM68V4000ALGI-10	32-SOP, 100ns, 3.3V, L
KM68V4000ALG-10L	32-SOP, 100ns, 3.3V, LL	KM68V4000ALGI-10L	32-SOP, 100ns, 3.3V, LL
KM68V4000ALT-7L	32-TSOP (II) F, 70ns, 3.3V, L	KM68V4000ALTI-7L	32-TSOP(II) F, 70ns, 3.3V, L
KM68V4000ALT-7	32-TSOP (II) F, 70ns, 3.3V, LL	KM68V4000ALTI-7	32-TSOP(II) F, 70ns, 3.3V, LL
KM68V4000ALT-10	32-TSOP (II) F, 100ns, 3.3V, L	KM68V4000ALTI-10	32-TSOP (II) F, 100ns, 3.3V, L
KM68V4000ALT-10L	32-TSOP (II) F, 100ns, 3.3V, LL	KM68V4000ALTI-10L	32-TSOP (II) F, 100ns, 3.3V, LL
KM68V4000ALR-7	32-TSOP (II) R, 70ns, 3.3V, L	KM68V4000ALRI-7	32-TSOP (II) R, 70ns, 3.3V, L
KM68V4000ALR-7L	32-TSOP (II) R, 70ns, 3.3V, LL	KM68V4000ALRI-7L	32-TSOP (II) R, 70ns, 3.3V, LL
KM68V4000ALR-10	32-TSOP (II) R, 100ns, 3.3V, L	KM68V4000ALRI-10	32-TSOP (II) R, 100ns, 3.3V, L
KM68V4000ALR-10L	32-TSOP (II) R, 100ns, 3.3V, LL	KM68V4000ALRI-10L	32-TSOP (II) R, 100ns, 3.3V, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Pd	0.7	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM68V4000AL/L-L
		-40 to 85	°C	KM68V4000ALI/LI-L
Soldering temperature and time	Tsolder	260 °C , 10sec (Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.3	V
Input low voltage	Vil	-0.3***	-	0.4	V

* 1) Commercial Product : Ta=0 to 70 °C unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤30ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

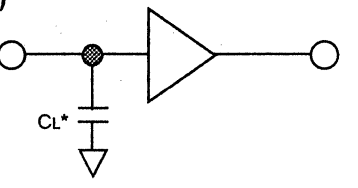
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS=Vih or Vil Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS=Vil, Vin=Vih or Vil, Iio=0mA		-	-	15	mA
Average operating current		Icc1	Cycle time=1uS 100% duty /CS≤0.2V, Vil≤0.2V, Vin≥Vcc-0.2V, Iio=0mA		-	-	15	mA
		Icc2	Min cycle, 100% duty /CS=Vil, Iio=0mA, Vin=Vih or Vil		-	-	50	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.2	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	0.5	mA
Standby Current (CMOS)	KM68V4000AL	Isb1	/CS≥Vcc-0.2V Vin≤0.2V or Vin≥Vcc-0.2V	L	-	-	50	uA
	KM68V4000AL-L			LL	-	-	15	uA
	KM68V4000ALI			L	-	-	50	uA
	KM68V4000ALI-L			LL	-	-	20	uA

* 1) Commercial Product : Ta=0 to 70 °C, Vcc=3.3 +/- 0.3V(68V4000A Family)
2) Industrial Product : Ta=-40 to 85 °C, Vcc=3.3 +/- 0.3V(68V4000AIFamily)
** Ta=25 °C

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics
** Test load for 70ns Industrial product

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V4000AL/L-L	0~70 °C	3.3V +/- 0.3	70*/100ns	Commercial
KM68V4000ALI/LI-L	-40~85 °C	3.3V +/- 0.3	70*/100ns	Industrial

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins				Units
			70ns*		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	100	-	ns
	Address access time	tAA	-	70	-	100	ns
	Chip select to output	tCO	-	70	-	100	ns
	Output enable to valid output	tOE	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	100	-	ns
	Chip select to end of write	tCW	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	ns
	Write pulse width	tWP	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns

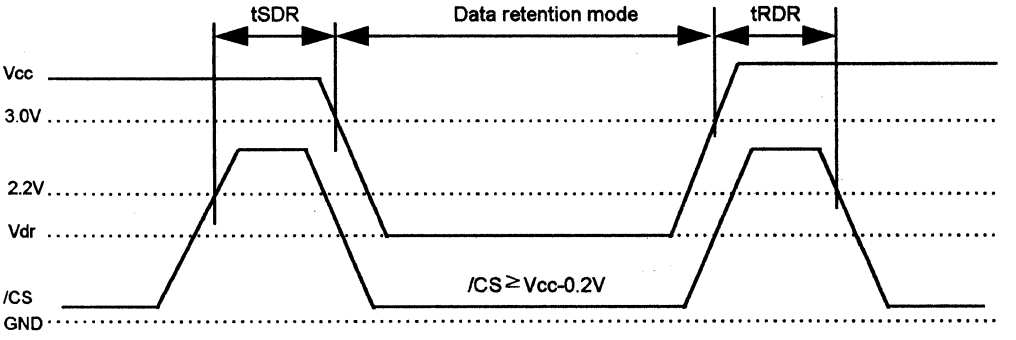
* Test load for measuring parameters : Commercial product-100pF, Industrial product-30pF

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS≥Vcc-0.2V		2.0	-	3.6	V
Data retention current	Idr	KM68V4000AL/L-L	Vcc=3.0V	L-Ver	-	1	30	uA
			/CS≥Vcc-0.2V	LL-Ver	-	0.5	15	
		KM68V4000ALI/LI-L		L-Ver	-	-	30	
				LL-Ver	-	-	20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

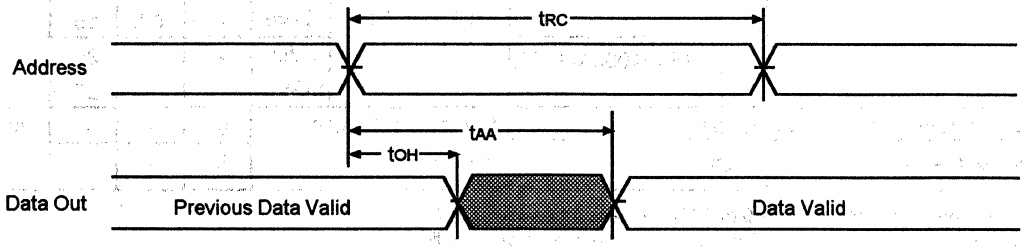
/CS	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	Ouput Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care

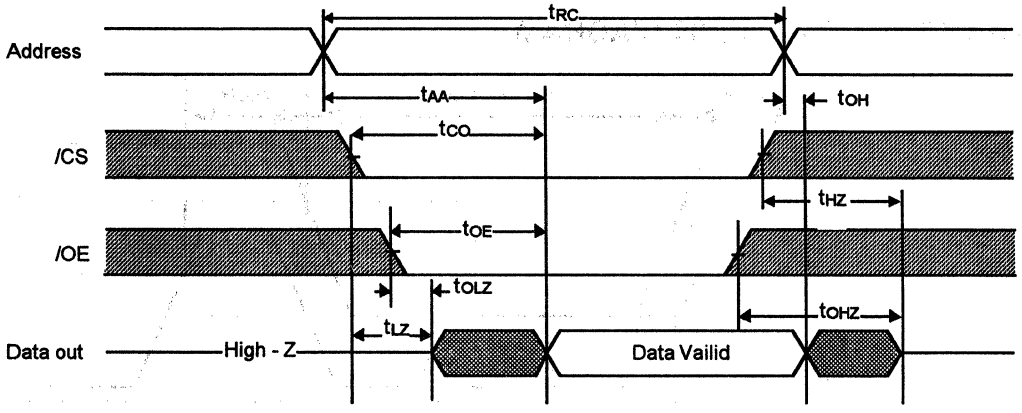
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih)



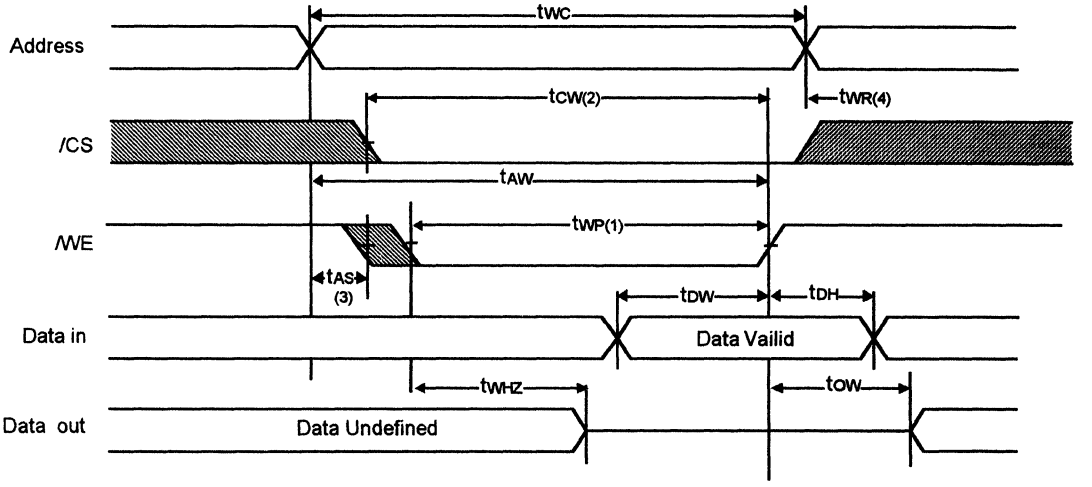
TIMING WAVEFORM OF READ CYCLE (/WE= VIH)



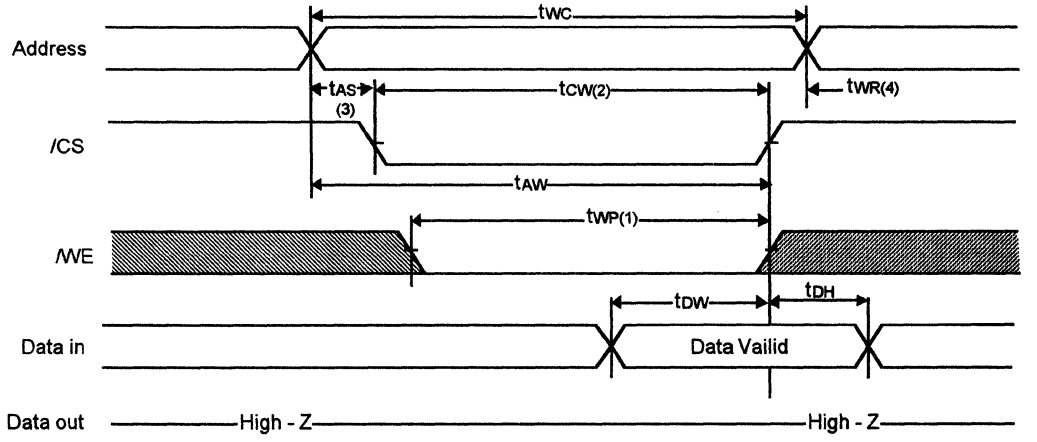
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.)both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CSand low /WE. A write begins at the latest transition among /CS going low and WE going low : A write end at the earliest transition among /CSgoing high and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS,or /WE going high.

High Speed SRAM (5.0V)

- KM64B261A	64K × 4	With OE/BiCMOS Center Power
- KM64258C	64K × 4	With OE/
- KM68B261A	32K × 8	BiCMOS Center Power
- KM68257C	32K × 8	
- KM641001	256K × 4	With OE/
- KM641001A	256K × 4	With OE/
- KM64B1003	256K × 4	With OE/ BiCMOS Center Power
- KM641003	256K × 4	With OE/ Center Power
- KM641003A	256K × 4	With OE/ Center Power
- KM681001	128K × 8	
- KM681001A	128K × 8	
- KM68B1002	128K × 8	BiCMOS Center Power
- KM681002	128K × 8	Center Power
- KM681002A	128K × 8	Center Power
- KM6161002	64K × 16	Center Power
- KM6161002A	64K × 16	Center Power
- KM64B4002	1M × 4	With OE/ BiCMOS Center Power
- KM644002A	1M × 4	Center Power
- KM644002/L	1M × 4	Center Power DTN MODE
- KM68B4002	512K × 8	BiCMOS Center Power
- KM684002A	512K × 8	Center Power
- KM684002/L	512K × 8	Center Power DTN MODE
- KM616B4002	256K × 16	BiCMOS Center Power
- KM6164002A	256K × 16	Center Power
- KM6164002/L	256K × 16	Center Power DTN MODE

64Kx4 Bit (With $\overline{OE}$) High Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 6, 7, 8 ns (Max.)
- Low Power Dissipation
  - Standby (TTL) : 90 mA (Max.)
  - (CMOS) : 20 mA (Max.)
  - Operating Current: 160 mA (f=100MHz)
- Single 5V±5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64B261AJ : 28-SOJ-300

GENERAL DESCRIPTION

The KM64B261A is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

The KM64B261A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

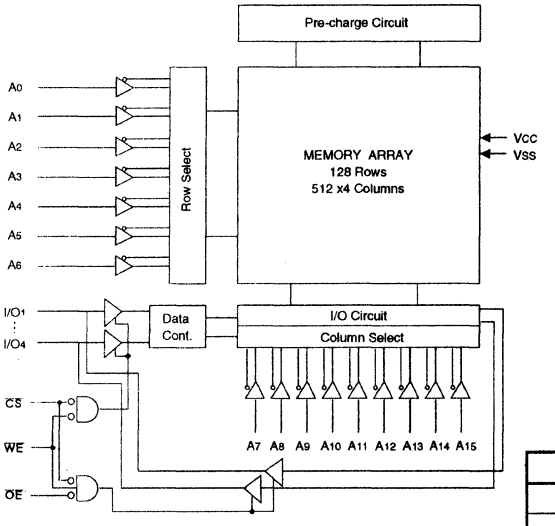
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system applications.

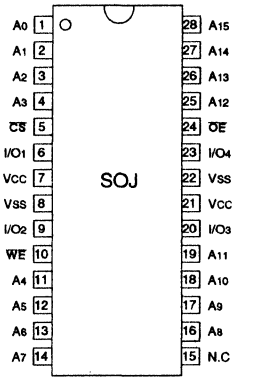
The KM64B261A is packaged in a 300 mil 28-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs/Outputs
Vcc	Power(+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (pulse width ≤3ns) for I≤20 mA

** V_{IH}(Max.)= Vcc+2.0V ac (pulse width ≤8ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±5%, unless otherwise specified)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc	-10	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc	-10	10	μA
Average Operating Current	Icc	f=100MHz,100% Duty,$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0 mA	-	160	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle	-	90	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V	-	20	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA	2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

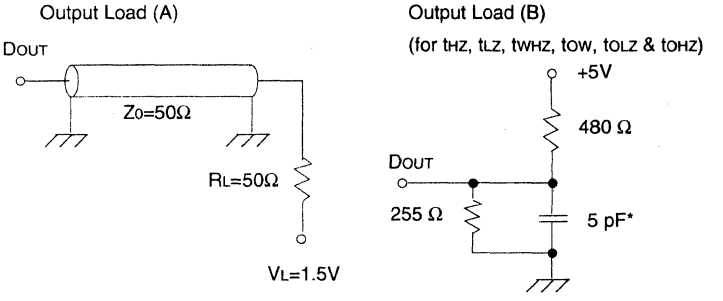
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

(T_A=0 to 70 °C, V_{CC}=5V±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

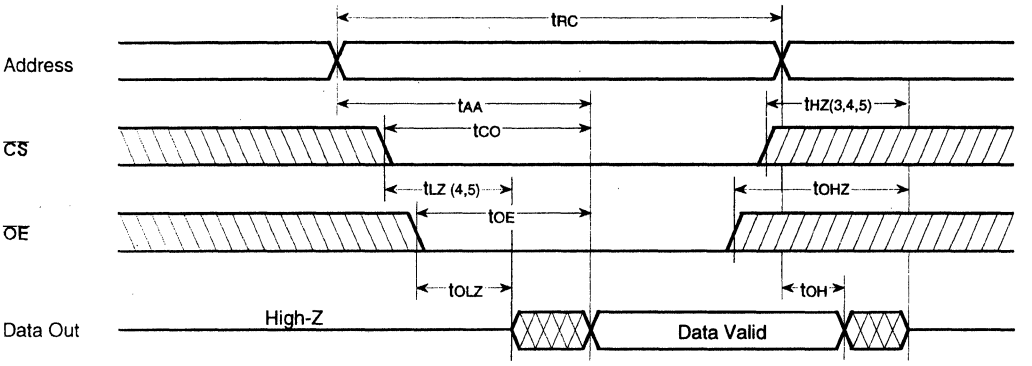
Parameter	Symbol	KM64B261A-6		KM64B261A-7		KM64B261A-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	6	-	7	-	8	-	ns
Address Access Time	t_{AA}	-	6	-	7	-	8	ns
Chip Select to Output	t_{CO}	-	6	-	7	-	8	ns
Output Enable to Valid Output	t_{OE}	-	4	-	4	-	4	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	t_{OHZ}	0	3	0	3.5	0	4	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B261A-6		KM64B261A-7		KM64B261A-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	6	-	7	-	8	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	8	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	3.5	-	4	-	4.5	-	ns
Write Pulse Width($\overline{OE}$ - High)	t_{WP}	3.5	-	4	-	4.5	-	ns
Write Pulse Width($\overline{OE}$ - Low)	t_{WP}	6	-	7	-	8	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WHZ}	0	3	0	3.5	0	4	ns
Data to Write Time Overlap	t_{DW}	3	-	3.5	-	4	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

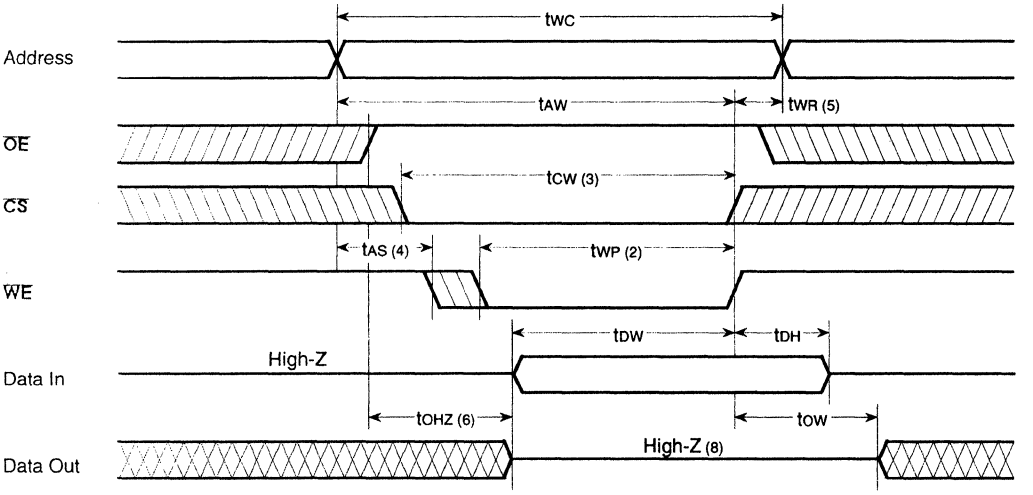
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

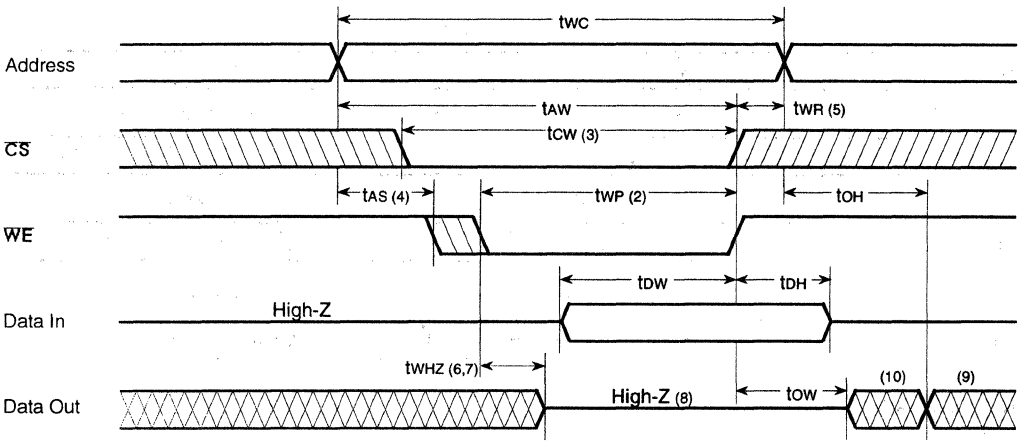
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

64Kx4 Bit (With $\overline{OE}$)High Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 20 ns (Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA (Max.)
  - (CMOS) : 2 mA (Max.)
  - Operating KM64258C-12 : 150 mA (Max.)
  - KM64258C-15 : 140 mA (Max.)
  - KM64258C-20 : 130 mA (Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM64258CP : 28-DIP-300
  - KM64258CJ : 28-SOJ-300

GENERAL DESCRIPTION

The KM64258C is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

The KM64258C uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

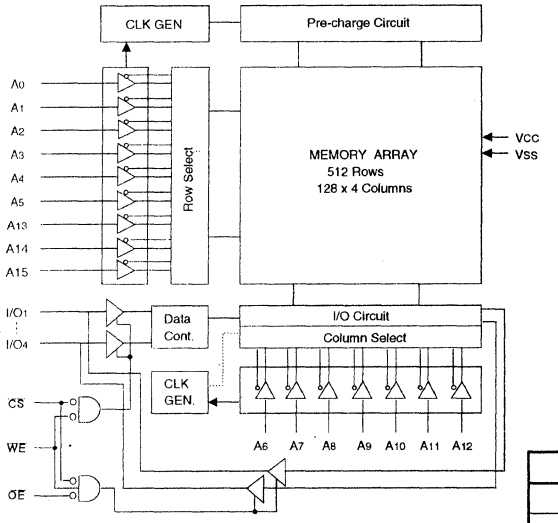
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system applications.

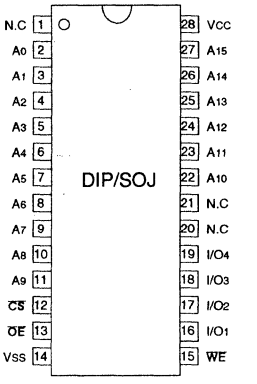
The KM64258C is packaged in a 300 mil 28-pin plastic DIP or SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs/Outputs
VCC	Power(5V)
VSS	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	Tsolder	260°C, 10 sec(Lead Only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	150	mA
		$\overline{CS}$=V_{IL}, I_{VIN} = V_{IH} or V_{IL},	15 ns	-	140	
		I_{OUT}= 0 mA	20 ns	-	130	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0 MHz V_{IN} ≥ V_{CC}-0.2V or V_{IN}≤0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

* Note: Temp. = 25°C, V_{CC}=5V±5%

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

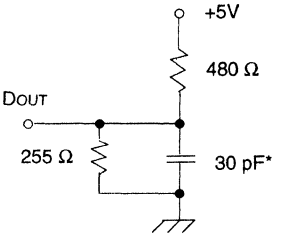
* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

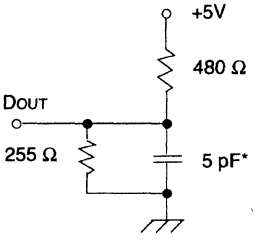
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64258C-12		KM64258C-15		KM64258C-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	20	ns
Output Enable to Valid Output	t_{OE}	-	6	-	7	-	9	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Select to Power up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Select to Power Down Time	t_{PD}	-	12	-	15	-	20	ns

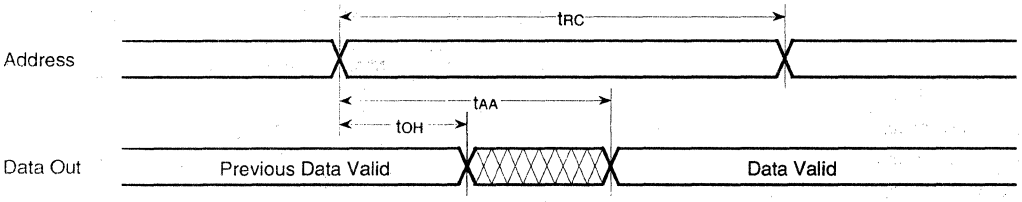
WRITE CYCLE

Parameter	Symbol	KM64258C-12		KM64258C-15		KM64258C-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	9	-	11	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ - High)	tWP	9	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ - Low)	tWP	12	-	15	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	0	-	ns

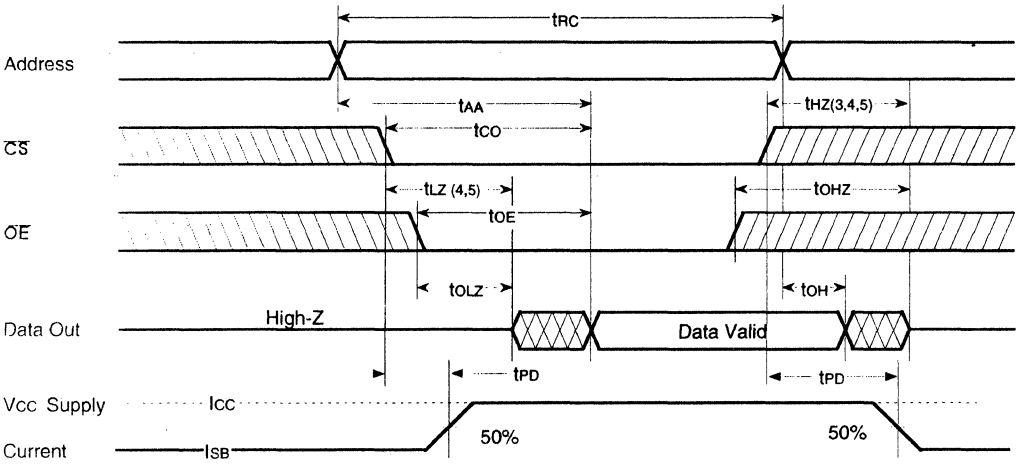
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



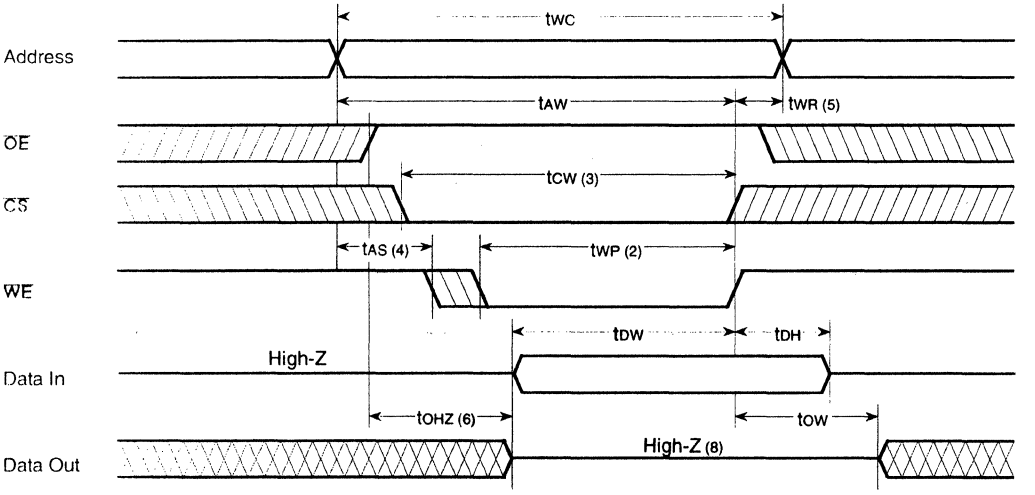
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



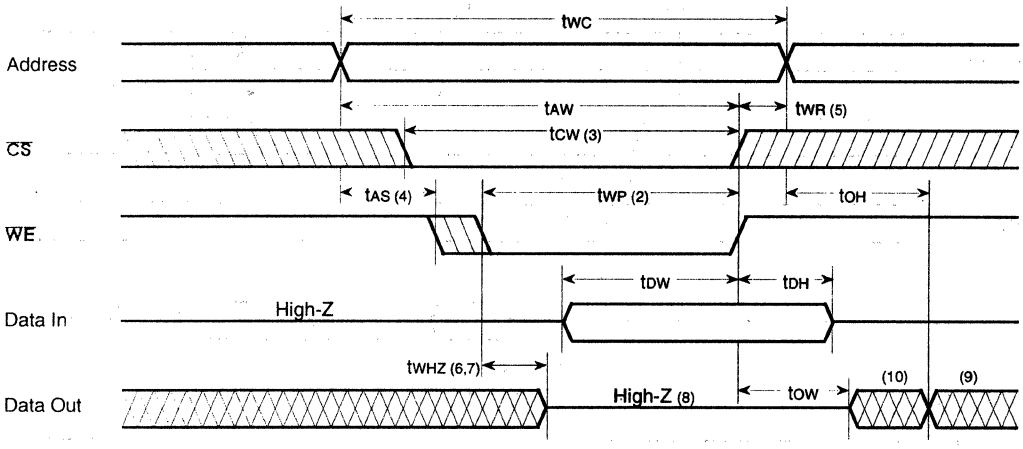
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

32Kx8 Bit High Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 6, 7, 8 ns (Max.)
- Low Power Dissipation
  - Standby (TTL) : 110 mA (Max.)
  - (CMOS) : 20 mA (Max.)
  - Operating Current : 170 mA (f=100MHz)
- Single 5V±5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68B261AJ : 32- SOJ-300

GENERAL DESCRIPTION

The KM68B261A is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68B261A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

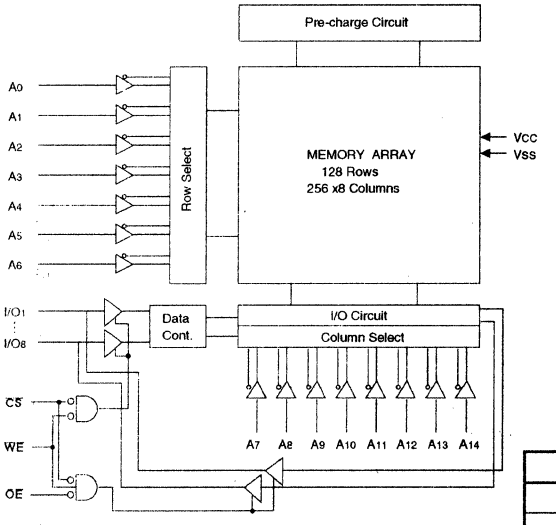
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system applications.

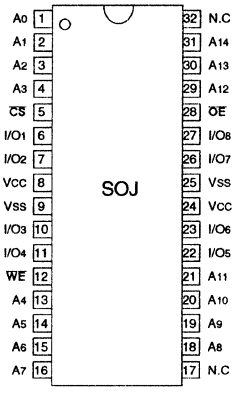
The KM68B261A is packaged in a 300 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A14	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (pulse width ≤3ns) for I≤20 mA

** V_{IH}(Max.)= V_{CC}+2.0V ac (pulse width ≤8ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±5%, unless otherwise specified)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}	-10	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}	-10	10	μA
Average Operating Current	I_{CC}	f=100MHz,100% Duty,$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0 mA	- -	170	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle	-	110	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0 MHz V_{IN} ≥ V_{CC}-0.2V or V_{IN}≤0.2V	-	20	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA	2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

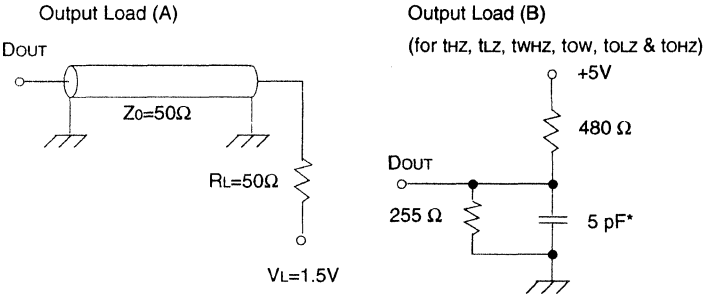
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

(T_A=0 to 70 °C, V_{CC}=5V±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

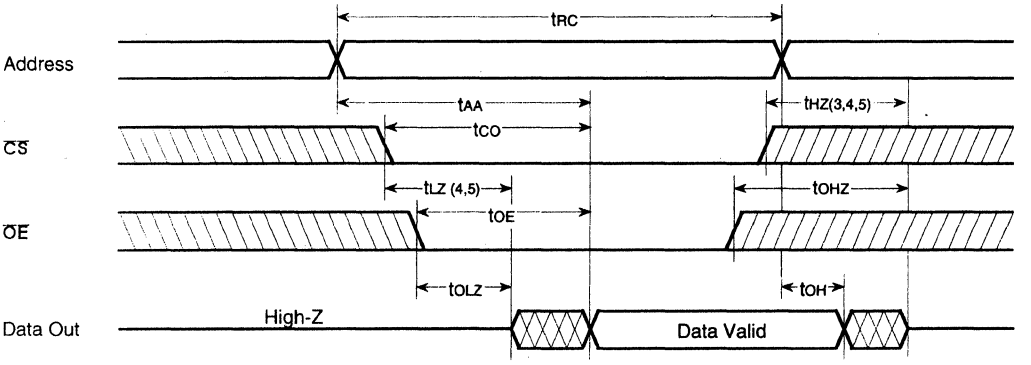
Parameter	Symbol	KM68B261A-6		KM68B261A-7		KM68B261A-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	6	-	7	-	8	-	ns
Address Access Time	t_{AA}	-	6	-	7	-	8	ns
Chip Select to Output	t_{CO}	-	6	-	7	-	8	ns
Output Enable to Valid Output	t_{OE}	-	4	-	4	-	4	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	t_{OHZ}	0	3	0	3.5	0	4	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68B261A-6		KM68B261A-7		KM68B261A-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	6	-	7	-	8	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	3.5	-	4	-	4.5	-	ns
Write Pulse Width($\overline{OE}$ - High)	tWP	3.5	-	4	-	4.5	-	ns
Write Pulse Width($\overline{OE}$ - Low)	tWP	6	-	7	-	8	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	3	0	3.5	0	4	ns
Data to Write Time Overlap	tDW	3	-	3.5	-	4	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

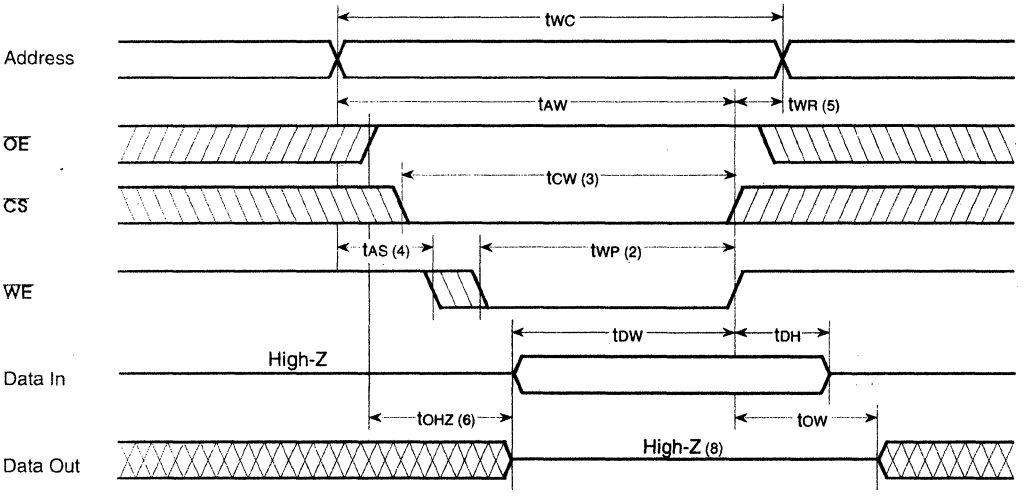
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=VIH)



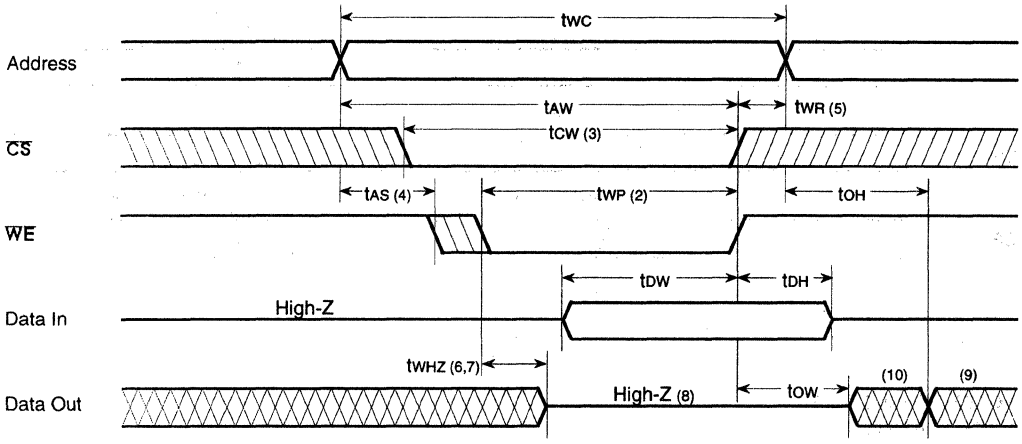
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

32Kx8 Bit High Speed CMOS Static RAM

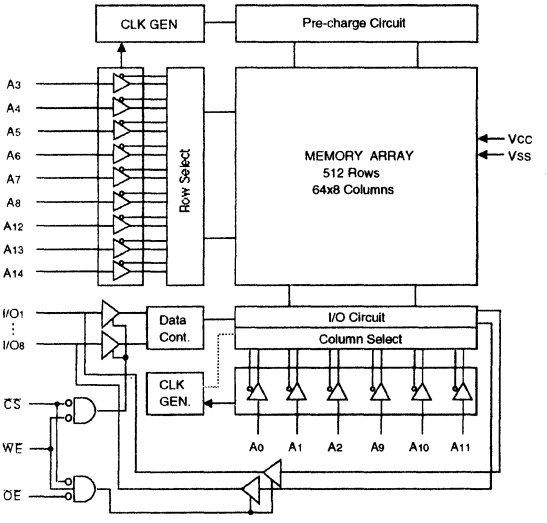
FEATURES

- Fast Access Time 12, 15, 20 ns (Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA (Max.)
  - (CMOS) : 2 mA (Max.)
  - 100 μA(Max.) - L- Ver.
  - Operating KM68257C/CL-12 : 165 mA (Max.)
  - KM68257C/CL-15 : 150 mA (Max.)
  - KM68257C/CL-20 : 140 mA (Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage :2V(Min.) - L- Ver. Only
- Standard Pin Configuration
  - KM68257CP/CLP : 28-DIP-300
  - KM68257CJ/CLJ : 28-SOJ-300
  - KM68257CTG/CLTG : 28-TSOP1-0813.4F

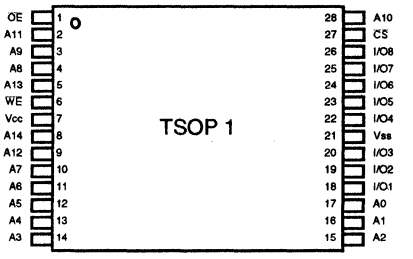
GENERAL DESCRIPTION

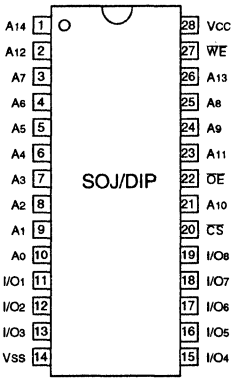
The KM68257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.
The KM68257C uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.
It is particularly well suited for use in high-density high-speed system applications.
The KM68257C is packaged in a 300 mil 28-pin plastic DIP/SOJ and TSOP1 forward.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)





Pin Name	Pin Function
A0-A14	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	Tsolder	260°C, 10 sec(Lead Only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	165	mA
		$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL},	15 ns	-	150	
		I_{OUT}=0 mA	20 ns	-	140	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0 MHz	-	-	2	mA
		V_{IN} ≥ V_{CC}-0.2V or V_{IN}≤0.2V	L-ver.	-	100	μA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

* Note: Temp. = 25°C, V_{CC}=5V±5%

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

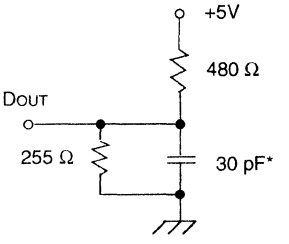
* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

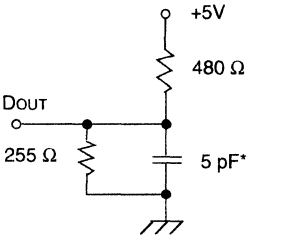
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68257C-12 KM68257CL-12		KM68257C-15 KM68257CL-15		KM68257C-20 KM68257CL-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	20	ns
Output Enable to Valid Output	t_{OE}	-	6	-	7	-	9	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Select to Power up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Select to Power Down Time	t_{PD}	-	12	-	15	-	20	ns

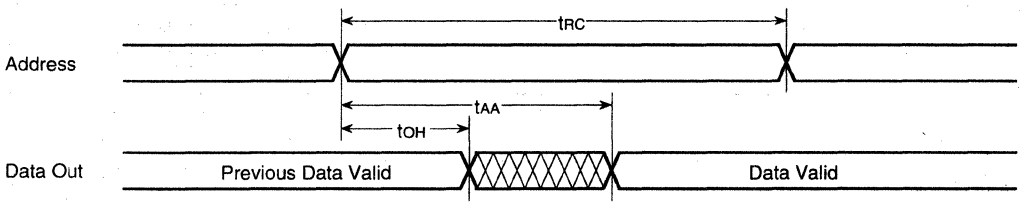
WRITE CYCLE

Parameter	Symbol	KM68257C-12 KM68257CL-12		KM68257C-15 KM68257CL-15		KM68257C-20 KM68257CL-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	15	-	20	-	ns
Chip Select to End of Write	t_{CW}	9	-	11	-	13	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	9	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ - High)	t_{WP}	9	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ - Low)	t_{WP}	12	-	15	-	20	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	6	0	8	0	8	ns
Data to Write Time Overlap	t_{DW}	7	-	8	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	0	-	0	-	0	-	ns

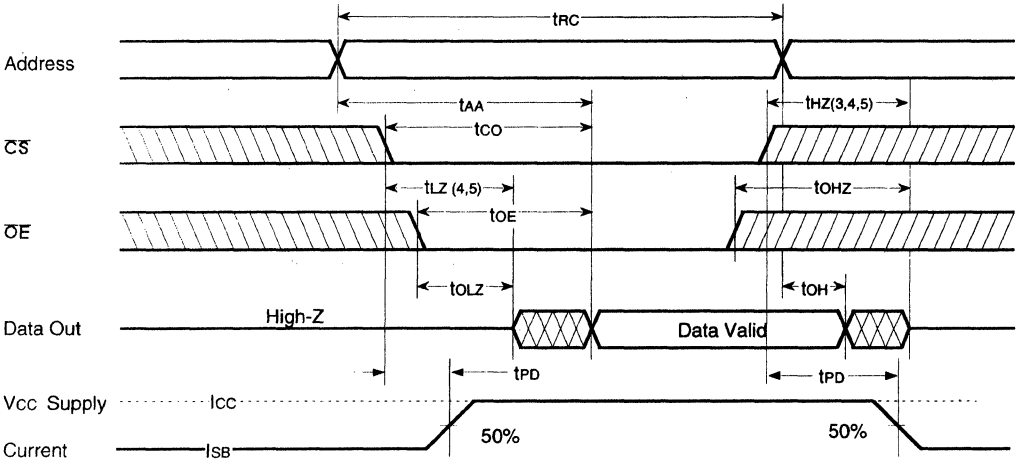
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



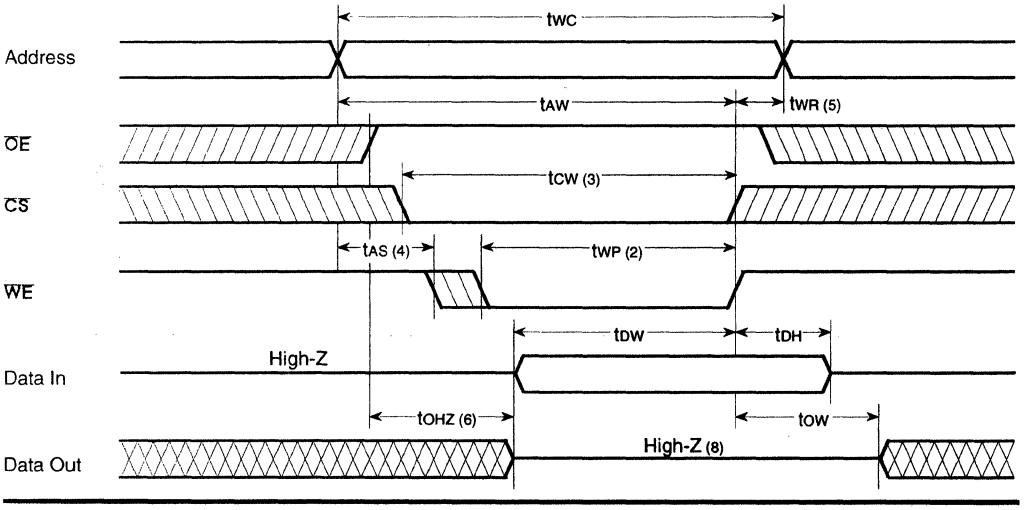
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

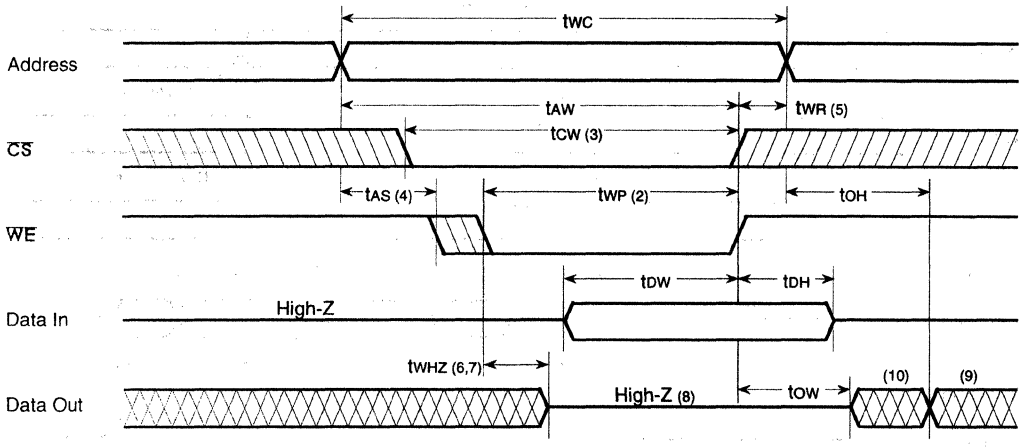
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

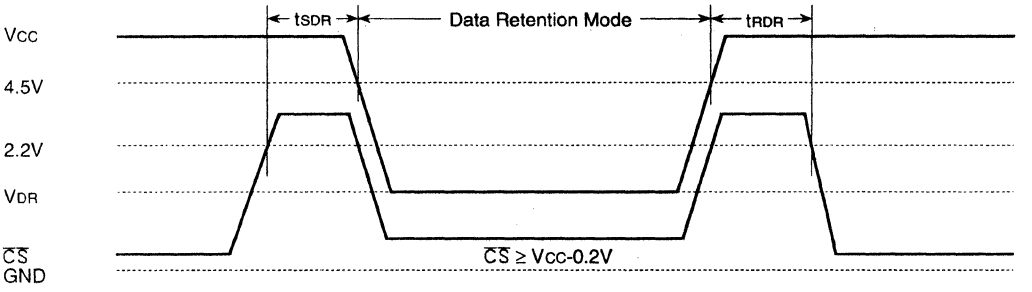
Note : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA=0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Max	Unit
VCC for Data Retention	VDR	$\overline{CS}$≥VCC-0.2V	2	5.5	V
Data Retention Current	IDR	VCC=3.0V, $\overline{CS}$≥VCC-0.2V VIN≥VCC-0.2V or VIN≤0.2V	-	100	μA
Data Retention Set-up Time	tSDR	See Data Retention	0	-	ns
Recovery Time	tRDR	Wave forms(below)	5	-	ms

* L-Version Only.

DATA RETENTION WAVEFORM 1 ($\overline{CS}$ Controlled)



256K x 4 Bit (With $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 20,25,35 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA(Max.)
  - (CMOS): 2 mA(Max.)
  - Operating KM641001-20 : 150 mA(Max.)
  - KM641001-25 : 130 mA(Max.)
  - KM641001-35 : 110 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM641001P: 28-DIP-400
  - KM641001J: 28-SOJ-400B

GENERAL DESCRIPTION

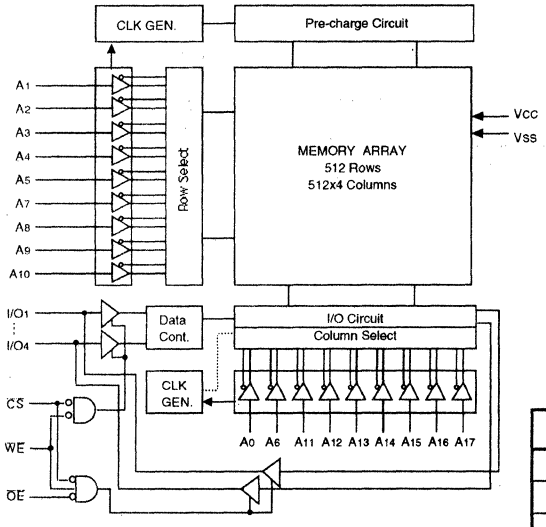
The KM641001 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.

The KM641001 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

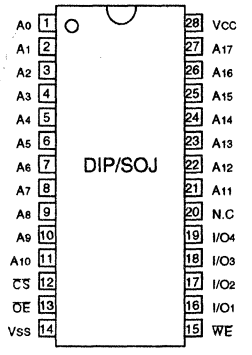
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM641001 is packaged in a 400 mil 28-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
VCC	Power (+5V)
VSS	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	20 ns	-	150	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA,	25 ns	-	130	
		V_{IN} = V_{IH} or V_{IL}	35 ns	-	110	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	40	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

* Note: Capacitance is sampled and not 100% tested.

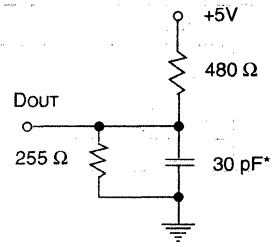
AC CHARACTERISTICS

TEST CONDITIONS

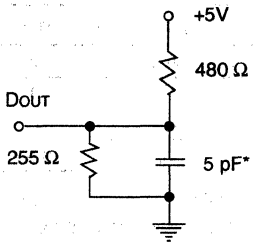
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ} & t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641001-20		KM641001-25		KM641001-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Select to Output	t_{CO}	-	20	-	25	-	35	ns
Output Enable to Output	t_{OE}	-	10	-	13	-	15	ns
Output Enable to Low-Z Output	t_{LZ}	0	-	0	-	0	-	ns
Chip E nable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Output Disable to High-Z Output	t_{HZ}	0	12	0	15	0	15	ns
Chip Disable to High-Z Output	t_{OHZ}	0	8	0	10	0	15	ns
Output Hold from Address Change	t_{OH}	3	-	5	-	5	-	ns
Chip Select to Power Up Time	t_{PU}	0	-	0	25	0	-	ns
Chip Deselect Power Down Time	t_{PD}	-	20	-		-	35	ns

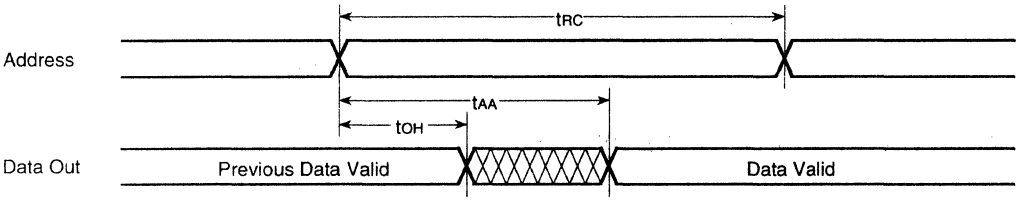
WRITE CYCLE

Parameter	Symbol	KM641001-20		KM641001-25		KM641001-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	20	-	25	-	35	-	ns
Chip Select to End of Write	t_{CW}	17	-	20	-	30	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	17	-	20	-	30	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	15	-	20	-	25	-	ns
Write Recovery Time	t_{WR}	2	-	3	-	3	-	ns
Write to Output High-Z	t_{WHZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12	-	15	-	20	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	0	-	0	-	0	-	ns

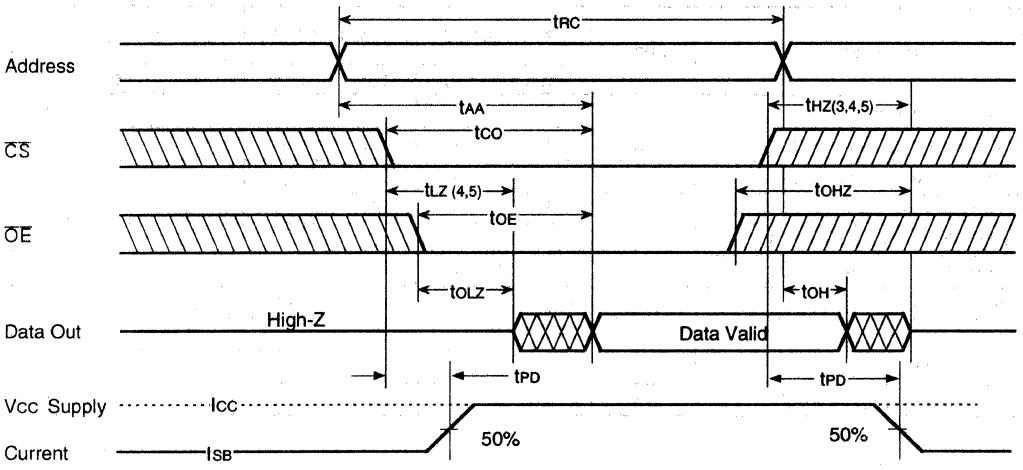
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



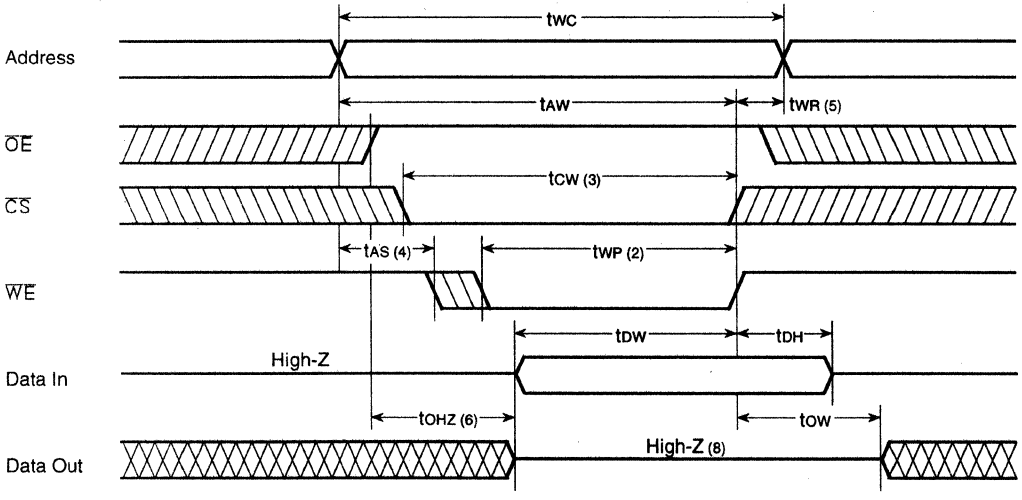
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

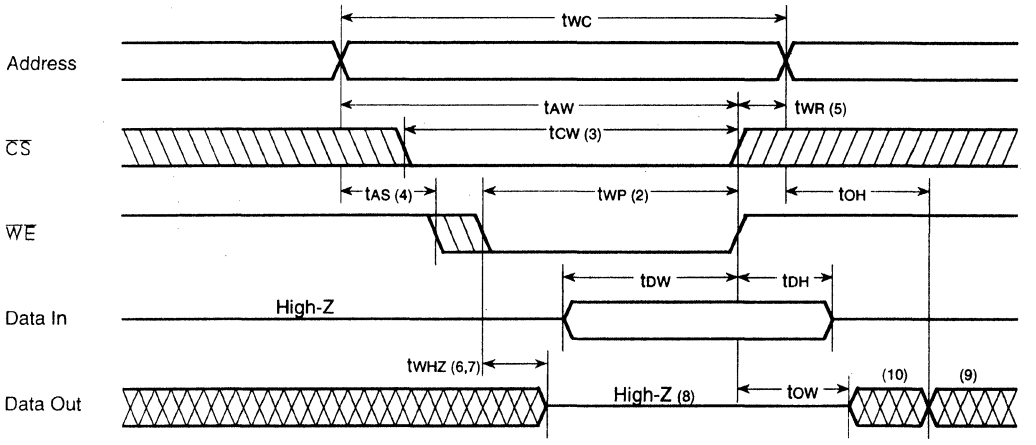
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

256K x 4 Bit (With $\overline{OE}$) High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM641001A-15 : 190 mA (Max.)
  - KM641001A-17 : 180 mA (Max.)
  - KM641001A-20 : 170 mA (Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM641001AJ : 28-SOJ-400

GENERAL DESCRIPTION

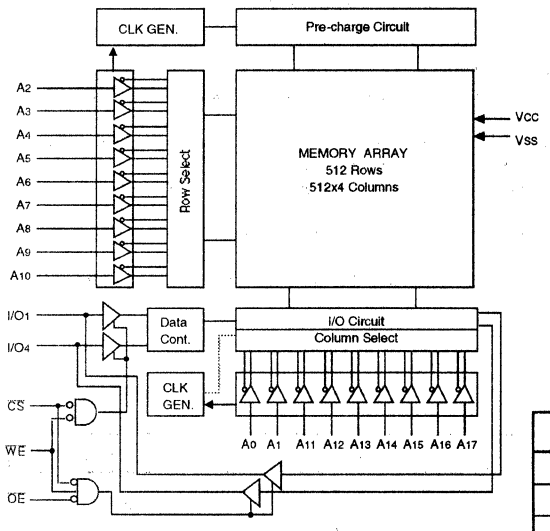
The KM641001A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.

The KM641001A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

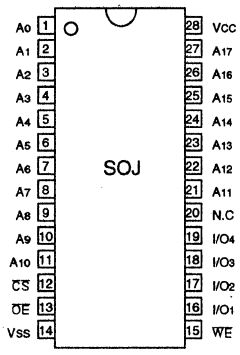
The device is fabricated using Samsung`s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM641001A is packaged in a 400 mil 28-pin plastic SOJ .

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	15 ns	-	190	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	17 ns	-	180	
		V_{IN} = V_{IH} or V_{IL}	20 ns	-	170	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0 MHz		-	10	mA
		V_{IN} ≥ V_{CC}-0.2V or V_{IN}≤0.2V		-		
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

*Note : V_{CC}=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

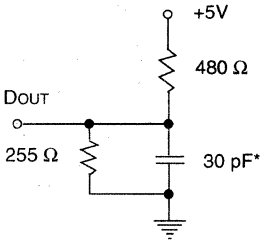
AC CHARACTERISTICS

TEST CONDITIONS

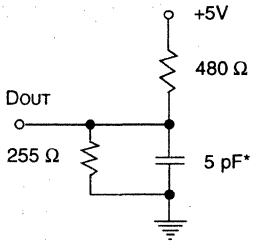
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641001A-15		KM641001A-17		KM641001A-20		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	8	-	9	-	10	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	15	-	17	-	20	ns

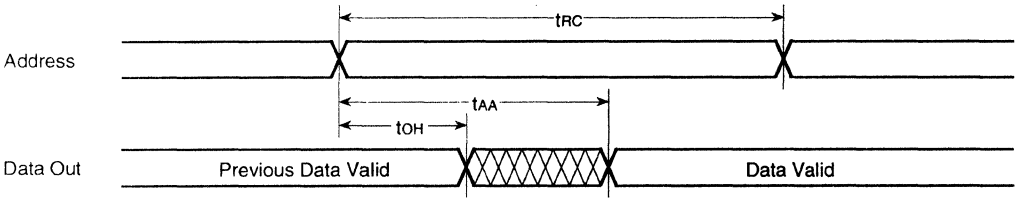
WRITE CYCLE

Parameter	Symbol	KM641001A-15		KM641001A-17		KM641001A-20		Unit
		min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	15	-	17	-	20	-	ns
Chip Select to End of Write	t_{CW}	12	-	12	-	13	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	12	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	12	-	12	-	13	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	8	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	8	-	9	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	4	-	5	-	ns

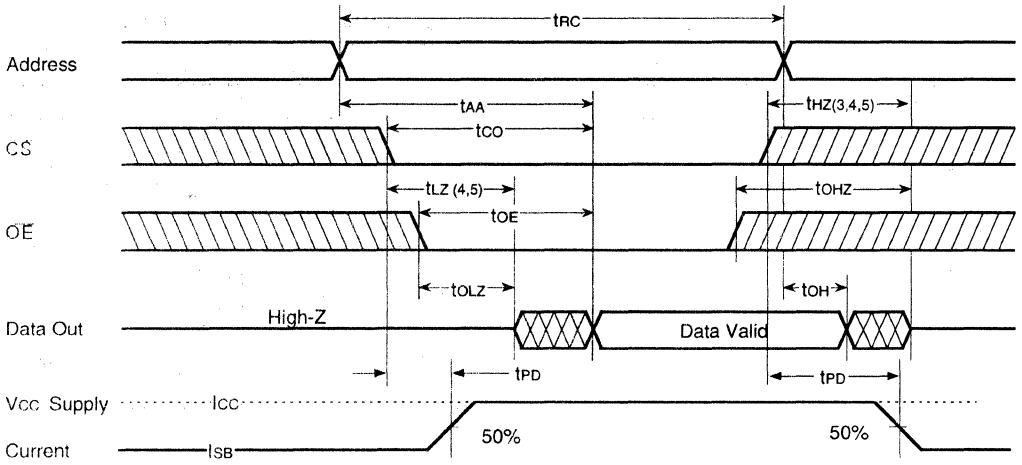
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



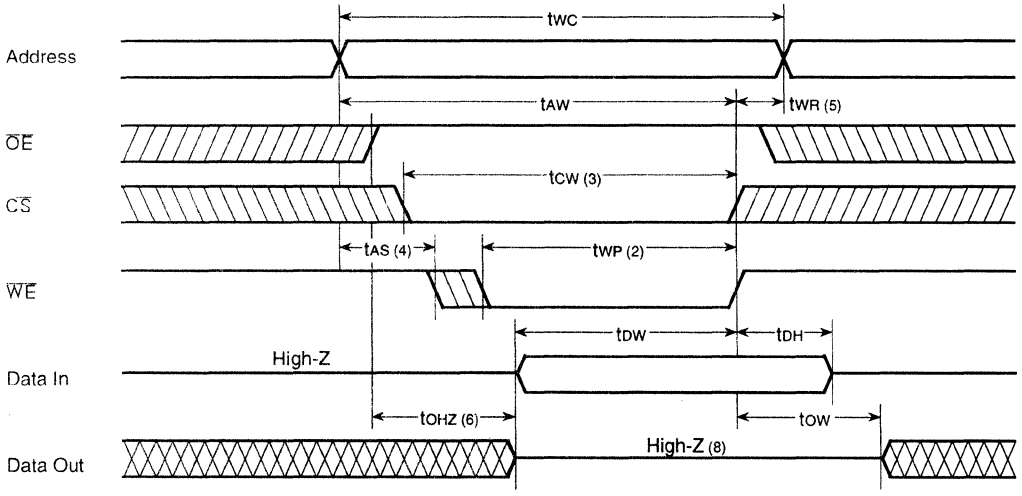
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



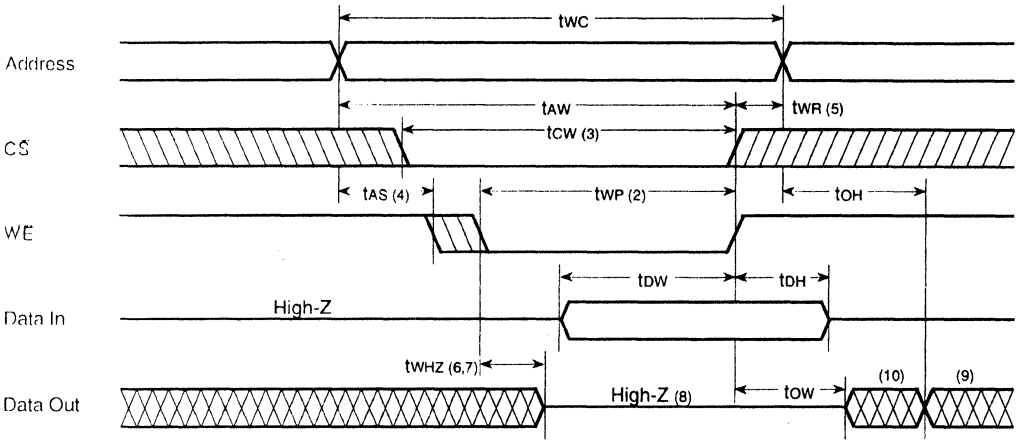
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

256Kx4 Bit(With $\overline{OE}$) High-Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 8,10,12,15 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(max.)
  - (CMOS): 10 mA(max.)
  - Operating KM64B1003J- 8: 165 mA(Max.)
  - KM64B1003J-10: 155 mA(Max.)
  - KM64B1003J-12: 145 mA(Max.)
  - KM64B1003J-15: 135 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64B1003J : 32-SOJ-400

GENERAL DESCRIPTION

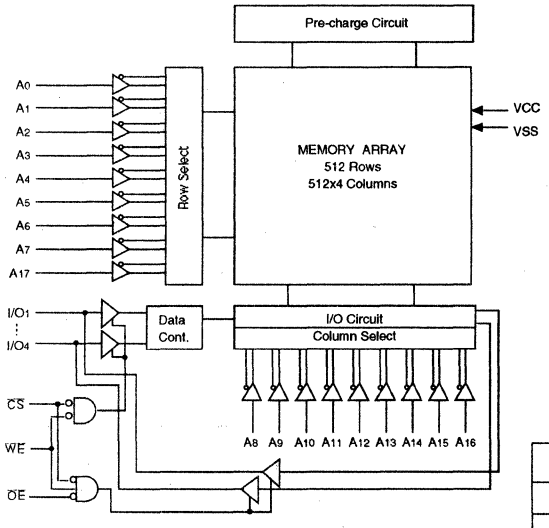
The KM64B1003 is a1,048,576-bit high-speed static random access memory organized as 262,144 words by 4 bits.

The KM64B1003 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

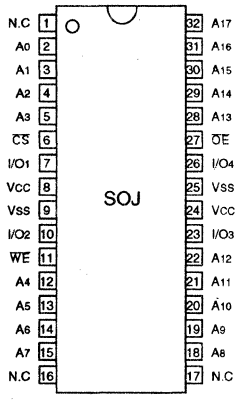
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM64B1003 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
VCC	Power (+5V)
VSS	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-10	10	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	8 ns	-	165	mA
		$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL},	10 ns	-	155	
		I_{OUT}=0 mA	12 ns	-	145	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15 ns	-	135	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

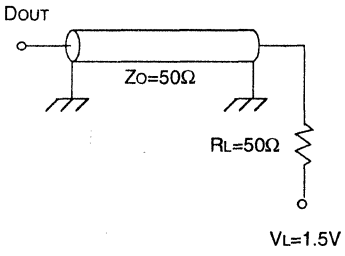
AC CHARACTERISTICS

TEST CONDITIONS

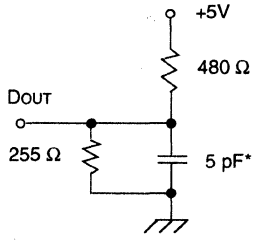
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ)



* Including Scope and Jig Capacitance

READ CYCLE

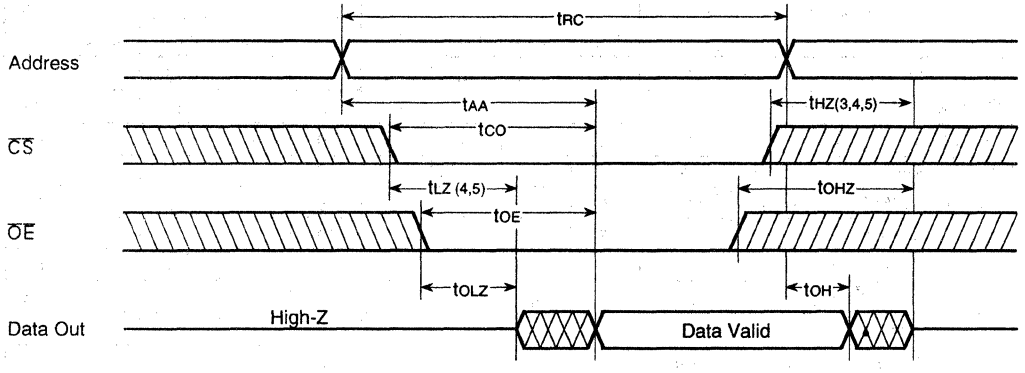
Parameter	Symbol	KM64B1003-8		KM64B1003-10		KM64B1003-12		KM64B1003-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	tRC	8	-	10	-	12	-	15	-	ns
Address Access Time	tAA	-	8	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	8	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	-	6	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B1003-8		KM64B1003-10		KM64B1003-12		KM64B1003-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	6	-	7	-	8	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	8	-	9	-	10	-	10	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WHZ}	0	4	0	5	0	6	-	6	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

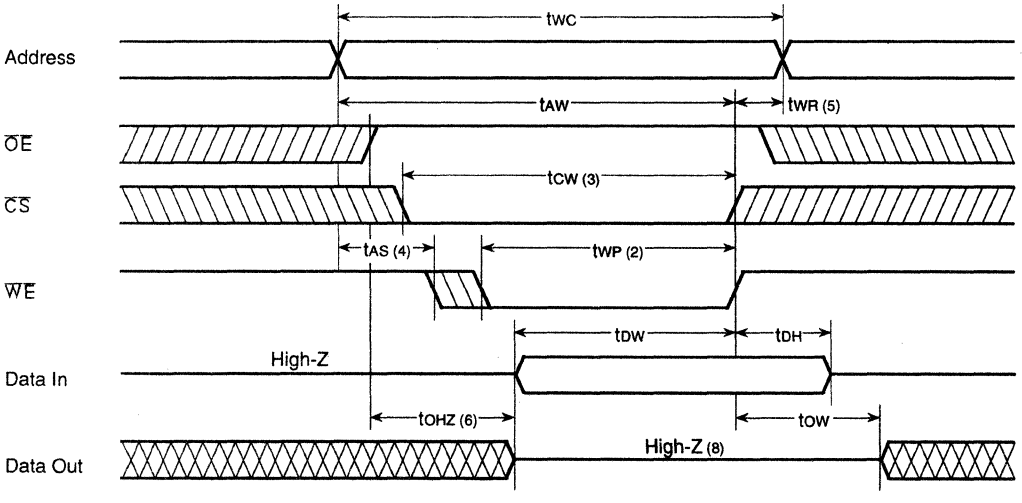
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=V_{IH})



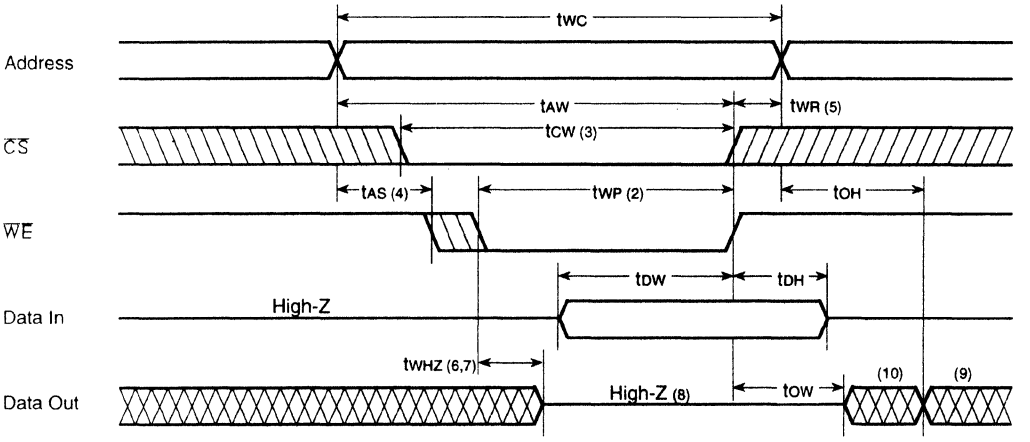
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =V_{IL}
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

256K x 4 Bit (With $\overline{OE}$) High-Speed CMOS Static RAM

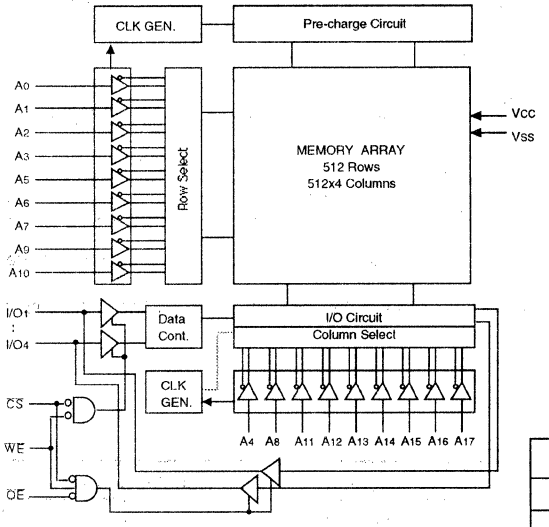
FEATURES

- Fast Access Time 15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA(max.)
  - (CMOS): 10 mA(max.)
  - Operating KM641003-15 : 170 mA(max.)
  - KM641003-17 : 160 mA(max.)
  - KM641003-20 : 150 mA(max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM641003J : 32-SOJ-400

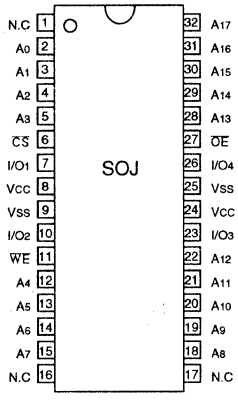
GENERAL DESCRIPTION

The KM641003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.
The KM641003 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.
The KM641003 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	µA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	15 ns	-	170	mA
		$\overline{CS}$=V_{IL}, I_{VIN} = V_{IH} or V_{IL},	17 ns	-	160	
		I_{OUT}=0 mA	20 ns	-	150	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	40	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100µA		-	3.95	V

*Note : Vcc=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

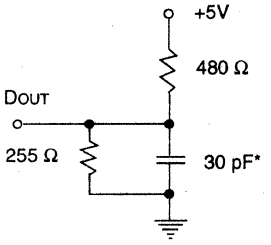
AC CHARACTERISTICS

TEST CONDITIONS

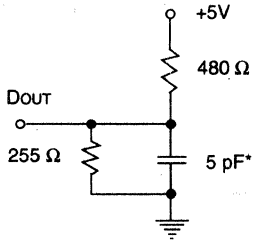
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641003-15		KM641003-17		KM641003-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	8	-	9	-	10	ns
Chip Select to Low-Z Output	t_{LZ}	0	-	0	-	0	-	ns
Output Enable to Low-Z Output	t_{OLZ}	3	-	3	-	3	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	5	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	15	-	17	-	20	ns

WRITE CYCLE

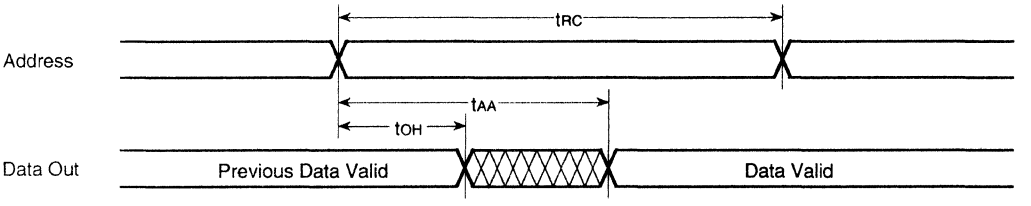
Parameter	Symbol	KM641003-15		KM641003-17		KM641003-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	10	-	11	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

2

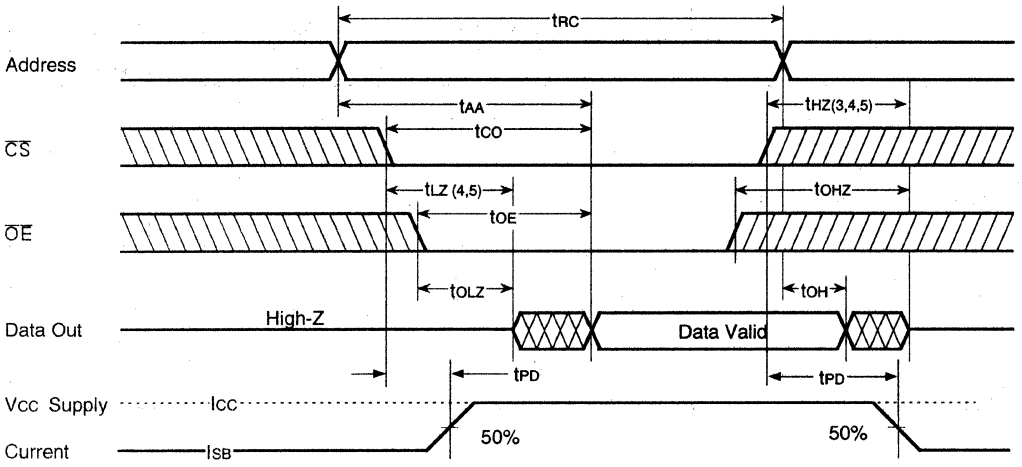
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



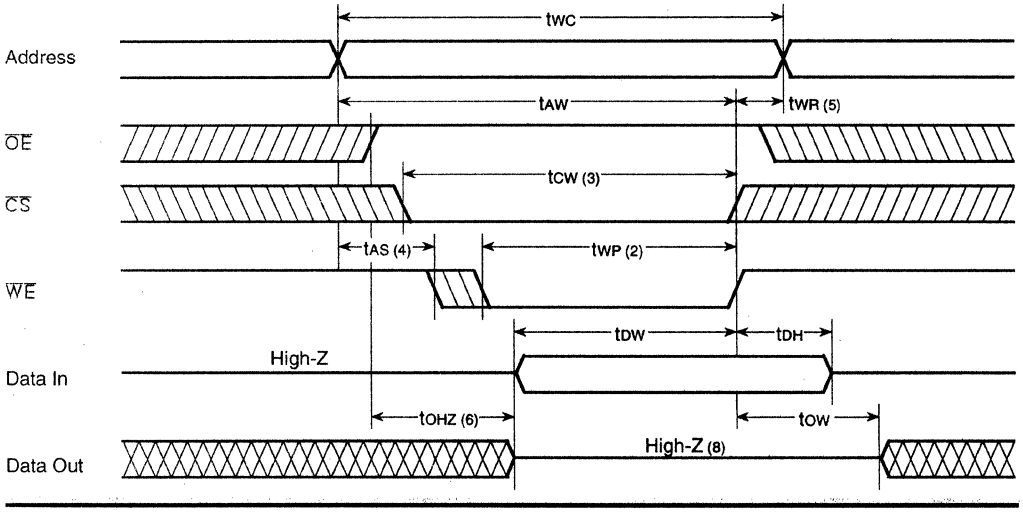
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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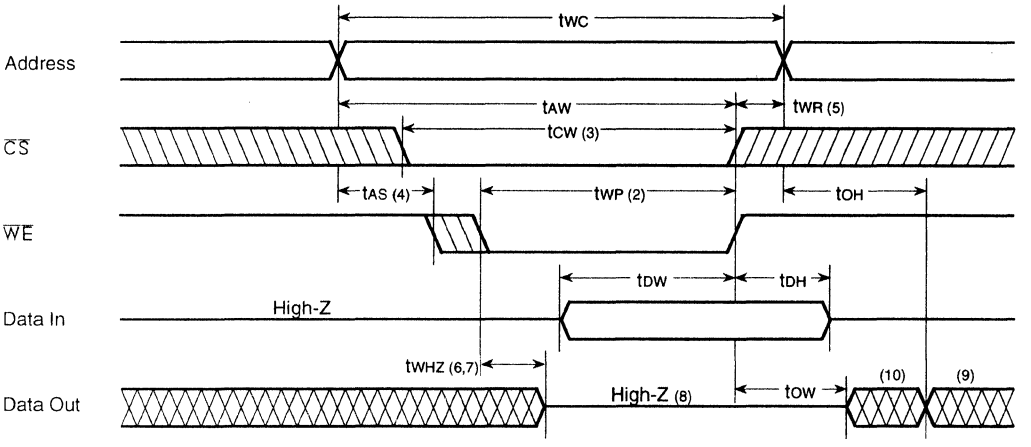
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

256K x 4 Bit (With $\overline{OE}$) High-Speed CMOS Static RAM

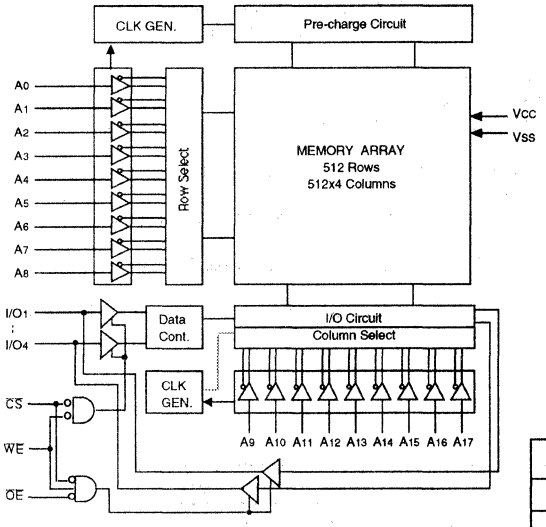
FEATURES

- Fast Access Time 12,15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM641003A-12 : 200 mA(Max.)
  - KM641003A-15 : 190 mA(Max.)
  - KM641003A-17 : 180 mA(Max.)
  - KM641003A-20 : 170 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM641003AJ : 32-SOJ-400
  - KM641003AT : 32-TSOP2-400F

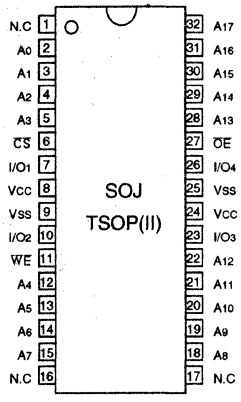
GENERAL DESCRIPTION

The KM641003A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.
The KM641003A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.
The KM641003A is packaged in a 400 mil 32-pin plastic SOJ and TSOP(II) forward.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty, $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0 mA	12 ns	-	200	mA
			15 ns	-	190	
			17 ns	-	180	
			20 ns	-	170	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz, V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

*Note : Vcc=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

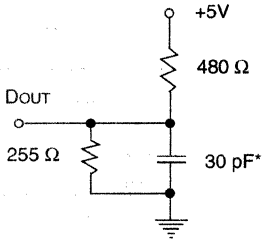
AC CHARACTERISTICS

TEST CONDITIONS

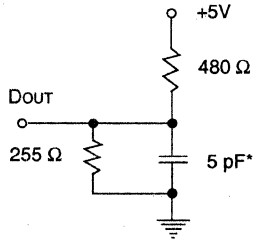
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641003A-12		KM641003A-15		KM641003A-17		KM641003A-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	12	-	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	6	-	7	-	8	-	9	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	12	-	15	-	17	-	20	ns

WRITE CYCLE

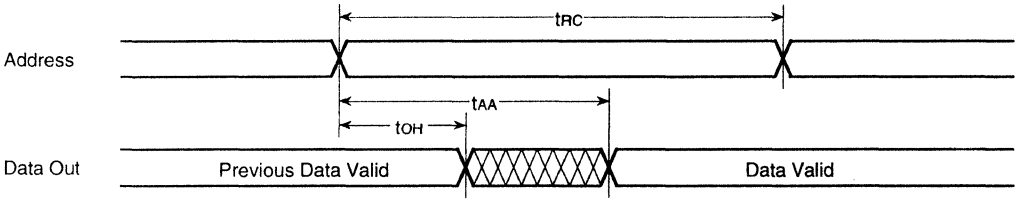
Parameter	Symbol	KM641003A -12		KM641003A -15		KM641003A -17		KM641003A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

2

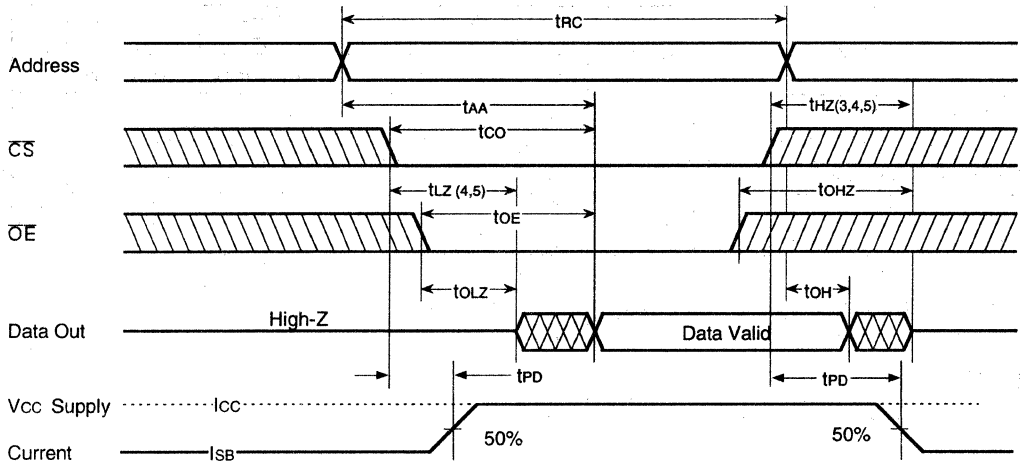
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



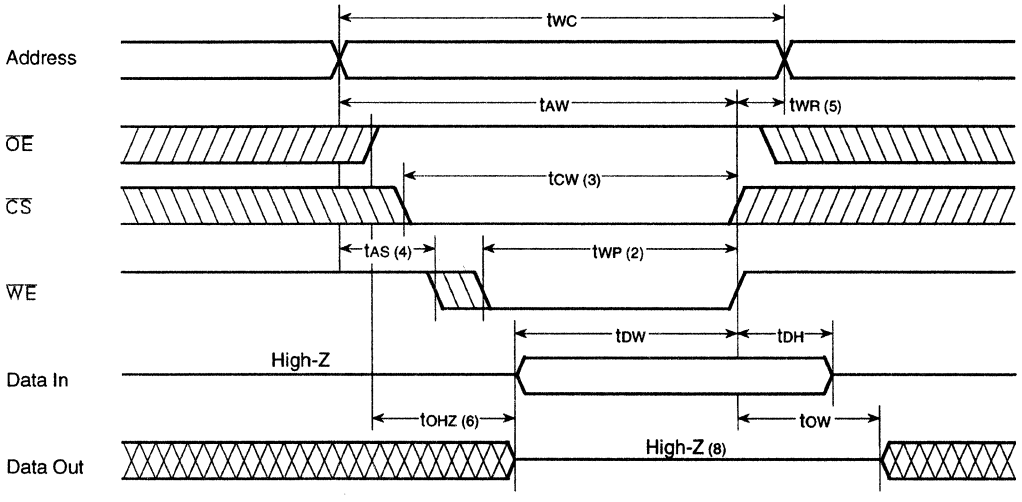
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

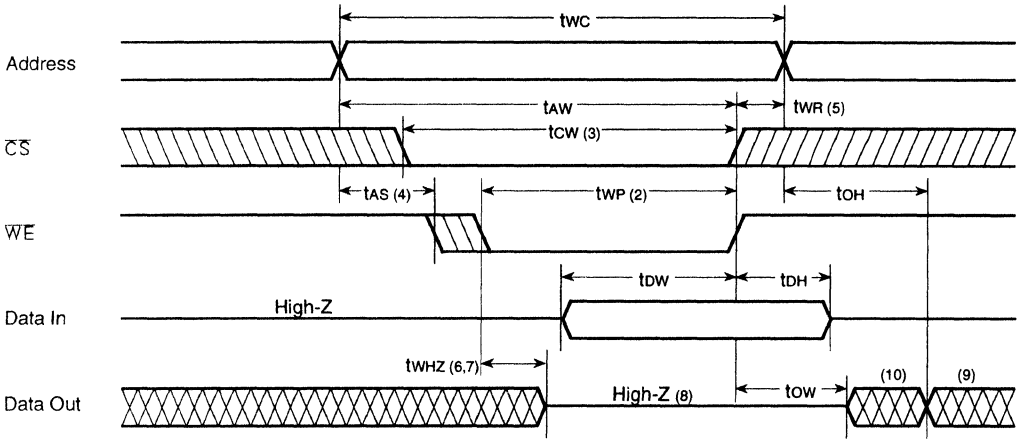
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

SAMSUNG ELECTRONICS

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 20,25,35 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA(Max.)
  - (CMOS): 2 mA(Max.)
  - Operating KM681001-20 : 170 mA(Max.)
  - KM681001-25 : 150 mA(Max.)
  - KM681001-35 : 130 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM681001P: 32-DIP-400
  - KM681001J: 32-SOJ-400

GENERAL DESCRIPTION

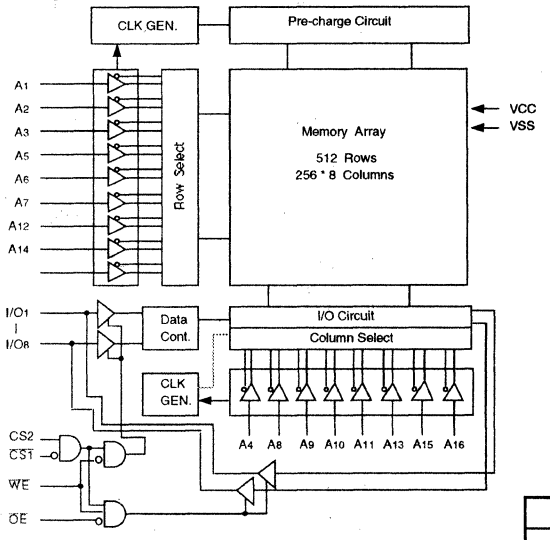
The KM681001 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.

The KM681001 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

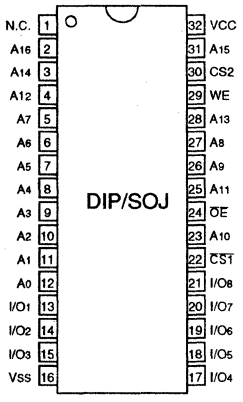
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM681001 is packaged in a 400 mil 32-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$,CS2	Chip Select
$\overline{OE}$	Output E nable
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground
N.C.	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	20 ns	-	170	mA
		$\overline{CS1}$=V_{IL}, CS2=V_{IH},	25 ns	-	150	
		V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0 mA	35 ns	-	130	
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL},Min. Cycle		-	40	mA
	I_{SB1}	$\overline{CS1}$≥Vcc-0.2V or CS2≤0.2V,f=0MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

* Note: Capacitance is sampled and not 100% tested.

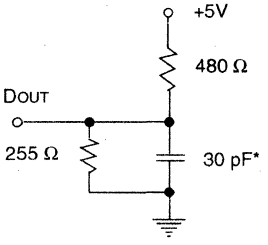
AC CHARACTERISTICS

TEST CONDITIONS

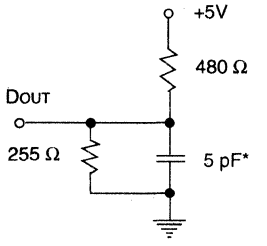
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ} & t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681001-20		KM681001-25		KM681001-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Select to Output	t_{CO1}, t_{CO2}	-	20	-	25	-	35	ns
Output Enable to Output	t_{OE}	-	10	-	13	-	15	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip E nable to Low-Z Output	t_{LZ1}, t_{LZ2}	0	-	0	-	0	-	ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	10	0	15	ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3	-	5	-	5	-	ns
Chip Select to Power Up Time	t_{PU}	0	-	0	-	0	-	
Chip Deselect Power Down Time	t_{PD}	-	20	-	25	-	35	

WRITE CYCLE

Parameter	Symbol	KM681001-20		KM681001-25		KM681001-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	20	-	25	-	35	-	ns
Chip Select to End of Write	t_{CW}	17	-	20	-	30	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	17	-	20	-	30	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	15	-	20	-	25	-	ns
Write Recovery Time	t_{WR}	2	-	3	-	3	-	ns
Write to Output High-Z	t_{WHZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12	-	15	-	20	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	0	-	0	-	0	-	ns

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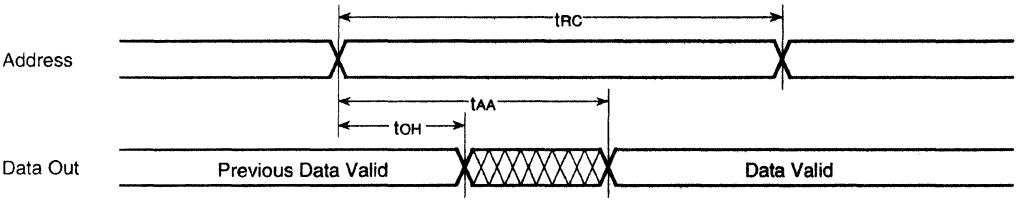
TIMING DIAGRAMS

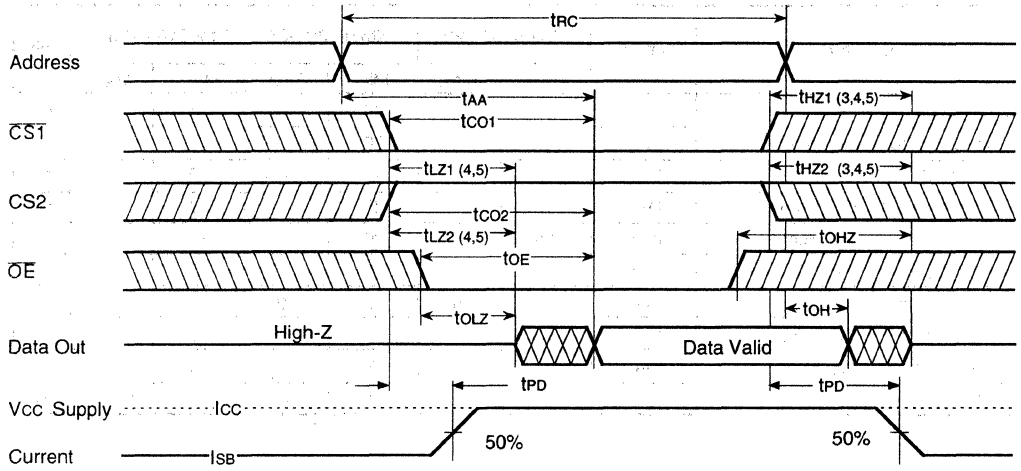
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS1}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=CS2=V_{IH})



SAMSUNG ELECTRONICS

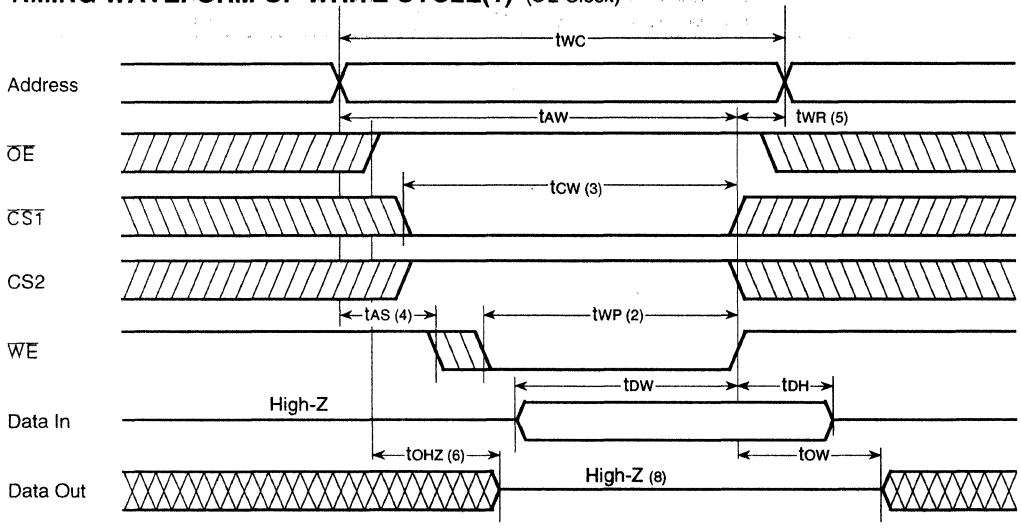
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

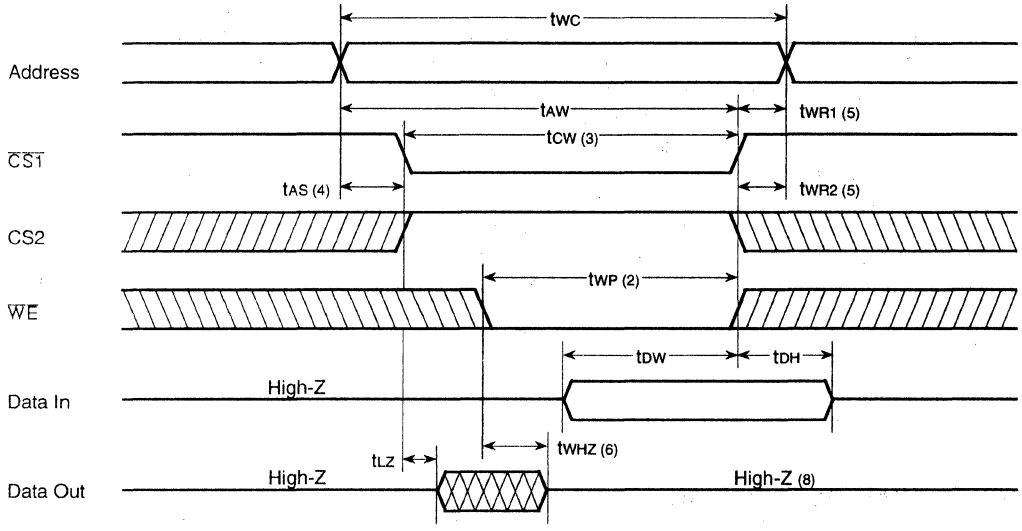
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS1}$ =VIL and CS2 =VIH
7. Address valid prior to coincident with $\overline{CS1}$ transition low and CS2 transition high.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)

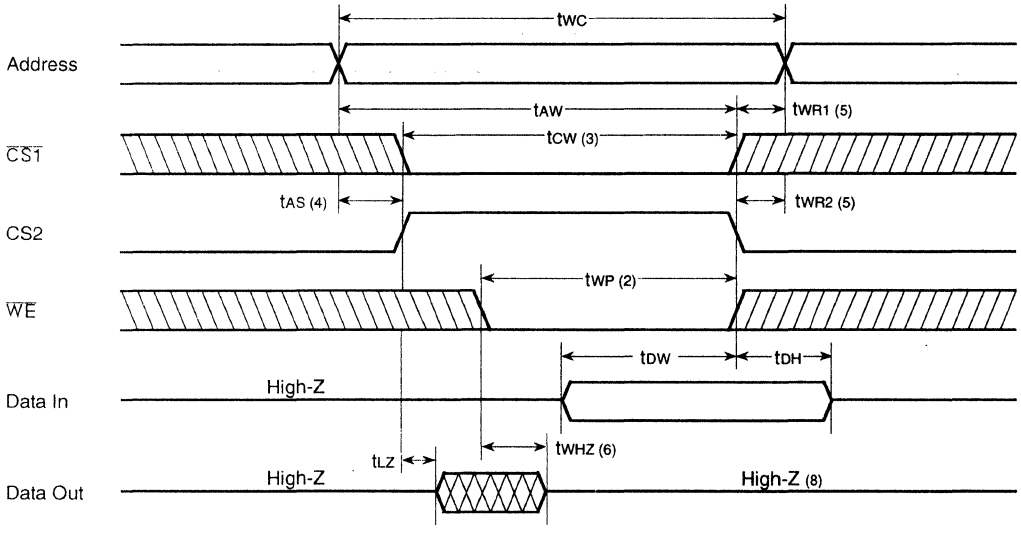


SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS1}$,a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
6. If $\overline{OE}$,$\overline{CS1}$,CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS1}$ goes low and CS2 high simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS1}$ is low and CS2 is high : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	I/O Pin	Supply Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	L	H	Read	D_{OUT}	I_{CC}
L	H	X	L	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM681001A-15 : 190 mA (Max.)
  - KM681001A-17 : 180 mA (Max.)
  - KM681001A-20 : 170 mA (Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM681001AJ : 32-SOJ-400

GENERAL DESCRIPTION

The KM681001A is a 1,048,576-bit high-speed static random access memory organized as 131,072 words by 8 bits.

The KM681001A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM681001A is packaged in a 400 mil 32-pin plastic SOJ.

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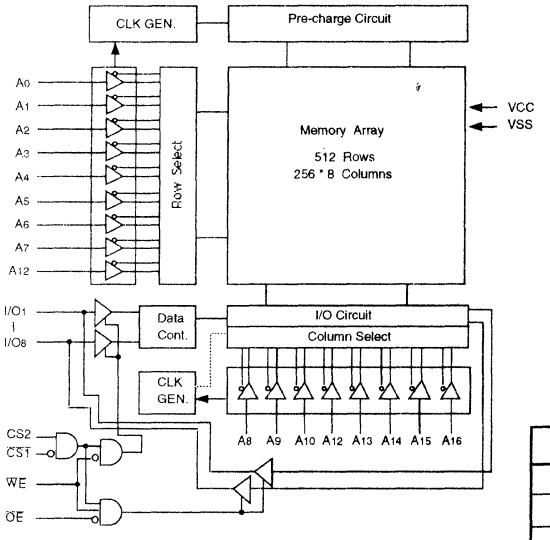
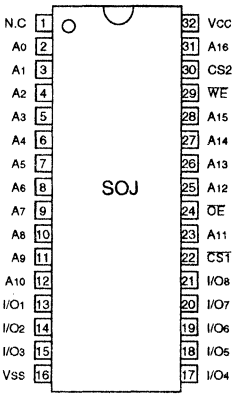
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$, CS2	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs / Outputs
Vcc	Power (+5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc, Vcc=Max		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	15 ns	-	190	mA
		$\overline{CS1}$=V_{IL}, CS2=V_{IH},	17 ns	-	180	
		V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0 mA	20 ns	-	170	
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS1}$≥Vcc-0.2V or CS2≤0.2V,f=0MHz		-	10	mA
		V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-		
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

*Note : Vcc=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

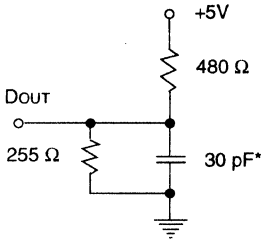
AC CHARACTERISTICS

TEST CONDITIONS

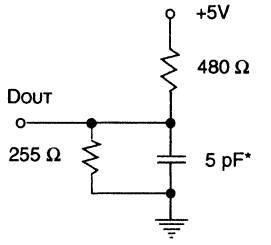
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681001A-15		KM681001A-17		KM681001A-20		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	8	-	9	-	10	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	15	-	17	-	20	ns

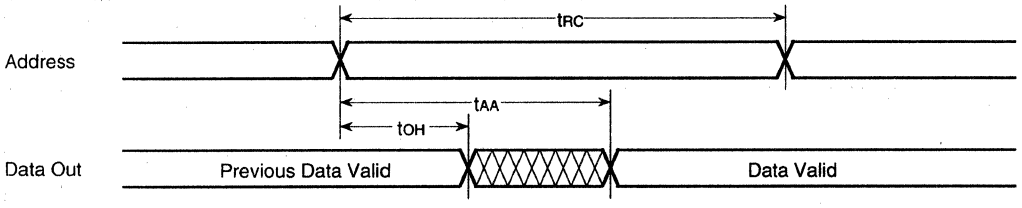
WRITE CYCLE

Parameter	Symbol	KM681001A-15		KM681001A-17		KM681001A-20		Unit
		min.	max.	min.	max.	min.	max.	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	12	-	13	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	9	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

TIMING DIAGRAMS

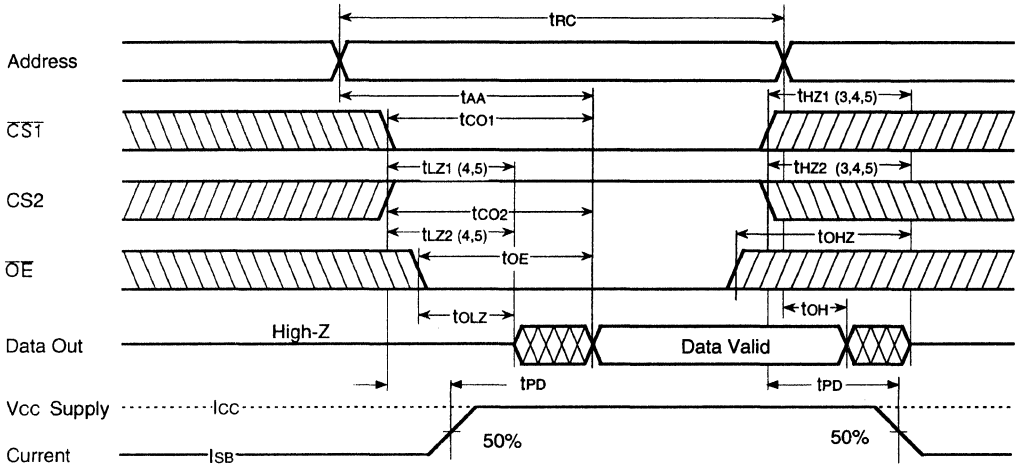
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS1}$=$\overline{OE}$=VIL, $\overline{WE}$=CS2=VIH)



SAMSUNG ELECTRONICS

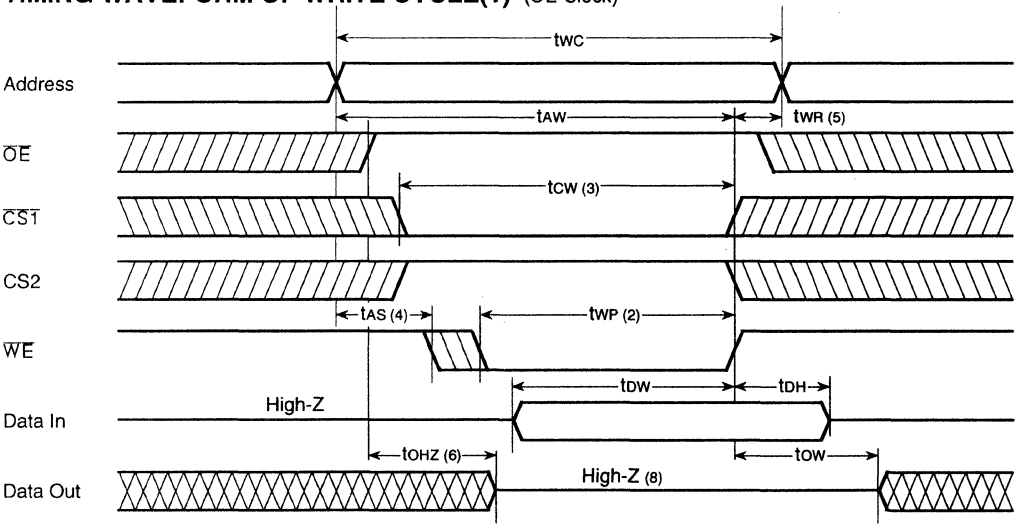
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

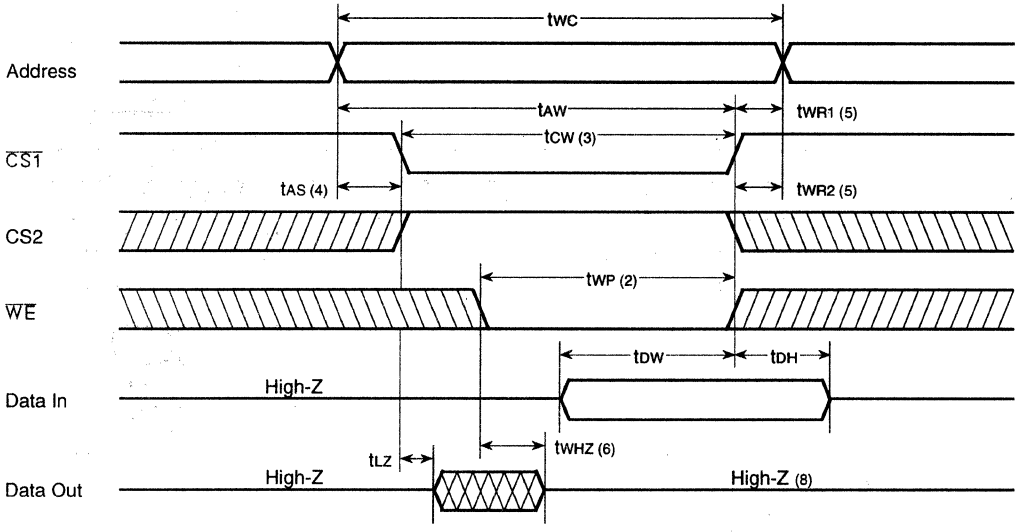
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS1}$ =VIL and CS2 =VIH
7. Address valid prior to coincident with $\overline{CS1}$ transition low and CS2 transition high.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)

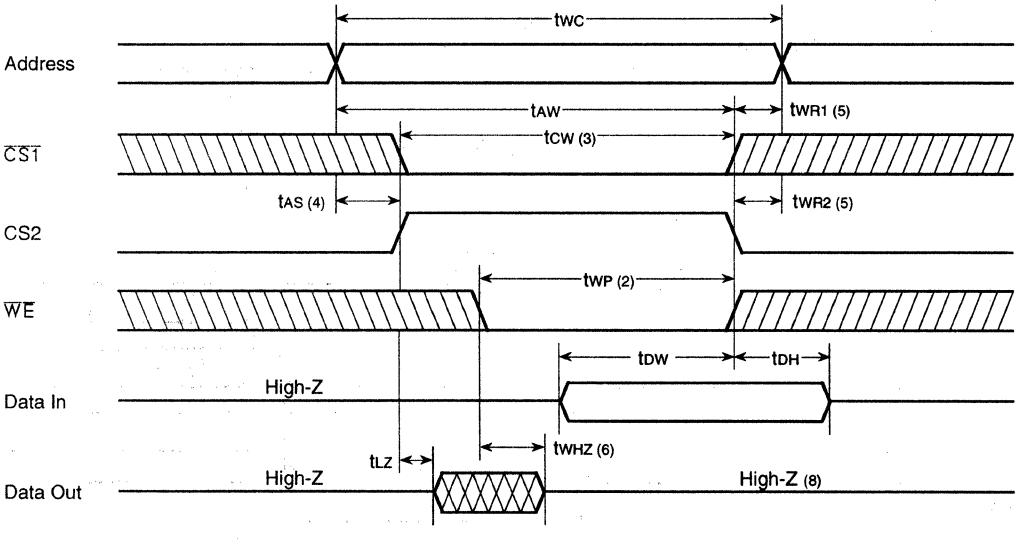


SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS1}$,a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
6. If $\overline{OE}$,$\overline{CS1}$,CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS1}$ goes low and CS2 goes high simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS1}$ is low and CS2 is high : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	I/O Pin	Supply Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	L	H	Read	D_{OUT}	I_{CC}
L	H	X	L	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

128Kx8 Bit High-Speed BiCMOS Static RAM

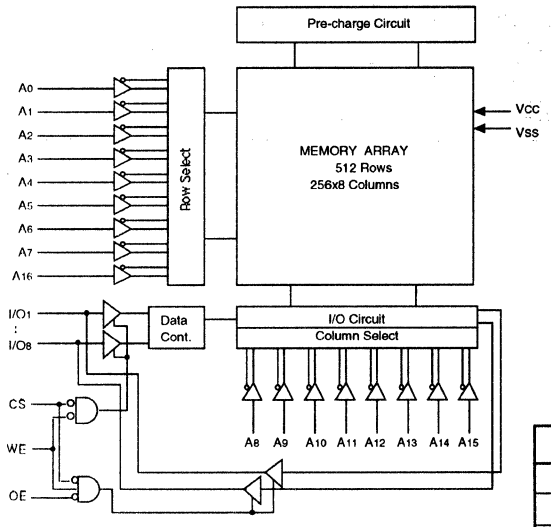
FEATURES

- Fast Access Time 8,10,12,15 ns(Max.)
- Low Power Dissipation
  Standby (TTL) : 60 mA(max.)
  (CMOS): 10 mA(max.)
  Operating KM68B1002J-8 : 175 mA(Max.)
  KM68B1002J-10: 165 mA(Max.)
  KM68B1002J-12: 155 mA(Max.)
  KM68B1002J-15: 145 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  -No Clock or Refresh required
- Three State Output
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  KM68B1002J : 32-SOJ-400

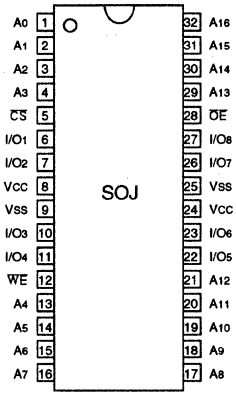
GENERAL DESCRIPTION

The KM68B1002 is a 1,048,576-bit high-speed static random access memory organized as 131,072 words by 8 bits.
The KM68B1002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.
The KM68B1002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs / Outputs
Vcc	Power (+5V)
Vss	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-10	10	μA
Average Operating Current	Icc	Min. Cycle, 100% Duty	8 ns	-	175	mA
		$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL},	10 ns	-	165	
		I_{OUT}=0 mA	12 ns	-	155	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15 ns	-	145	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

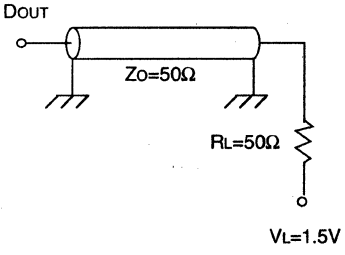
AC CHARACTERISTICS

TEST CONDITIONS

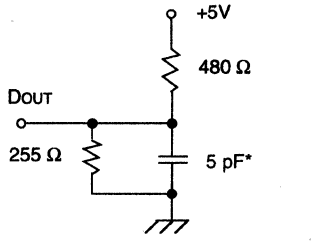
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

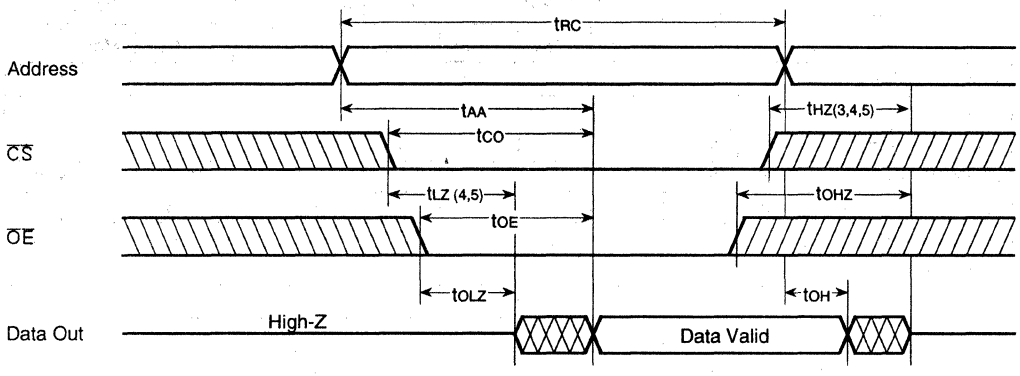
Parameter	Symbol	KM68B1002-8		KM68B1002-10		KM68B1002-12		KM68B1002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	8	-	10	-	12	-	15	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	-	6	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	0	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68B1002-8		KM68B1002-10		KM68B1002-12		KM68B1002-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	6	-	7	-	8	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	8	-	9	-	10	-	10	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WHZ}	0	4	0	5	0	6	-	6	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

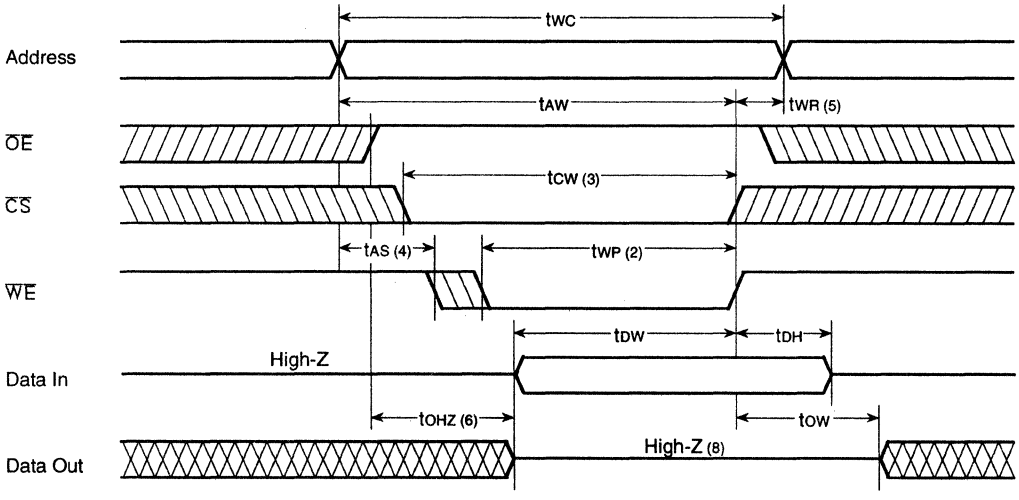
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=VIH)



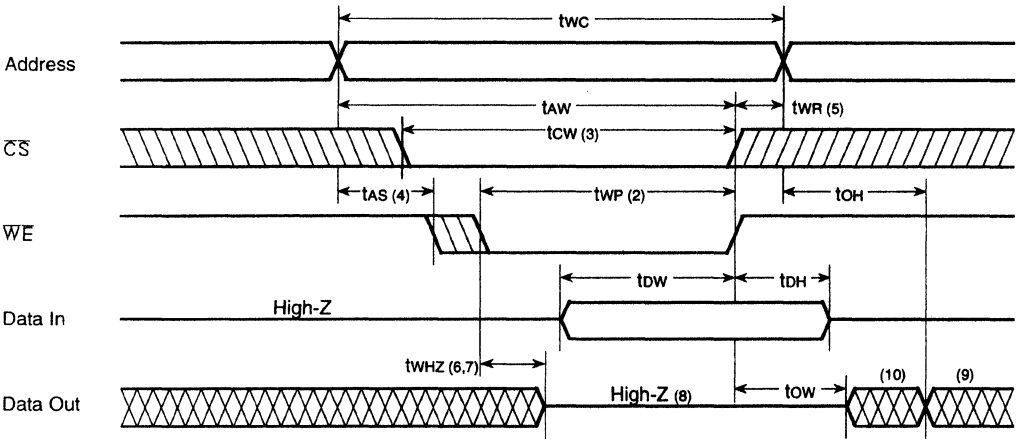
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM681002-15 : 170 mA (Max.)
  - KM681002-17 : 160 mA (Max.)
  - KM681002-20 : 150 mA (Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM681002J : 32-SOJ-400

GENERAL DESCRIPTION

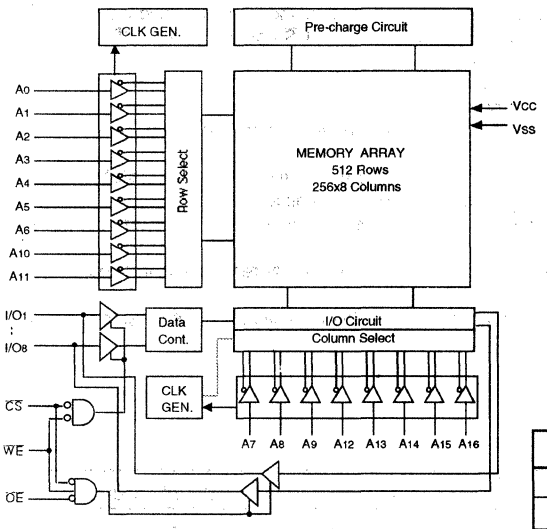
The KM681002 is a 1,048,576-bit high-speed static random access memory organized as 131,072 words by 8 bits.

The KM681002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

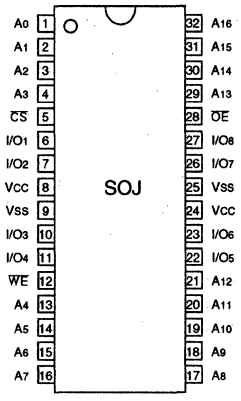
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM681002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs / Outputs
Vcc	Power (+5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	15 ns	-	170	mA
		$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL},	17 ns	-	160	
		I_{OUT}=0 mA	20 ns	-	150	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0 MHz V_{IN} ≥ V_{CC}-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

*Note : V_{CC}=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

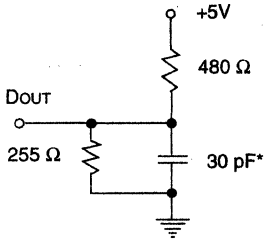
AC CHARACTERISTICS

TEST CONDITIONS

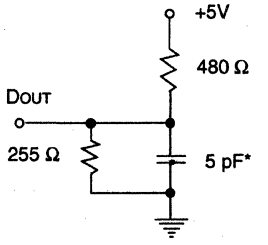
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681002-15		KM681002-17		KM681002-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	8	-	9	-	10	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	4	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	15	-	17	-	20	ns

WRITE CYCLE

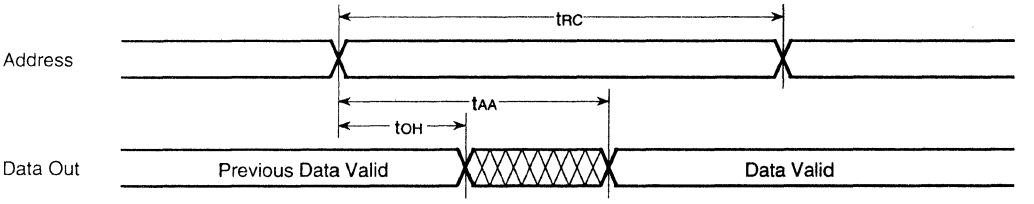
Parameter	Symbol	KM681002-15		KM681002-17		KM681002-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	10	-	11	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

2

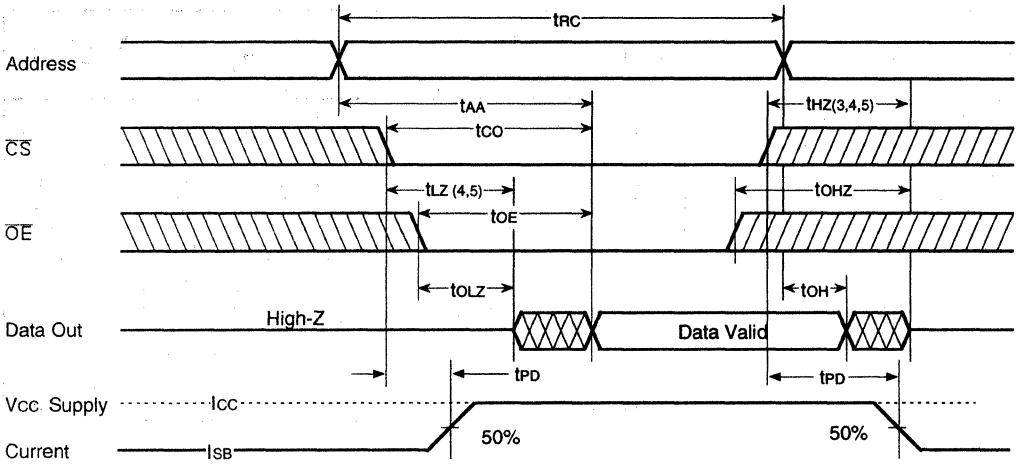
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



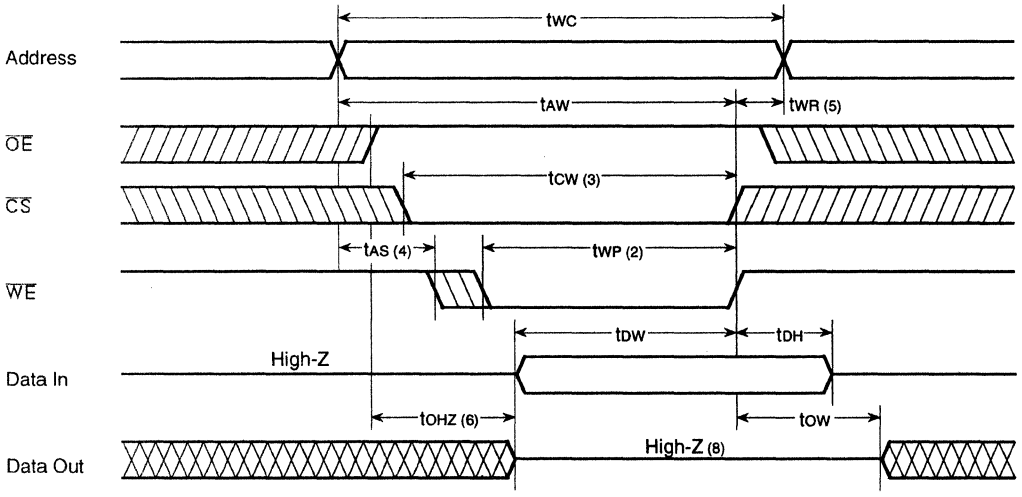
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

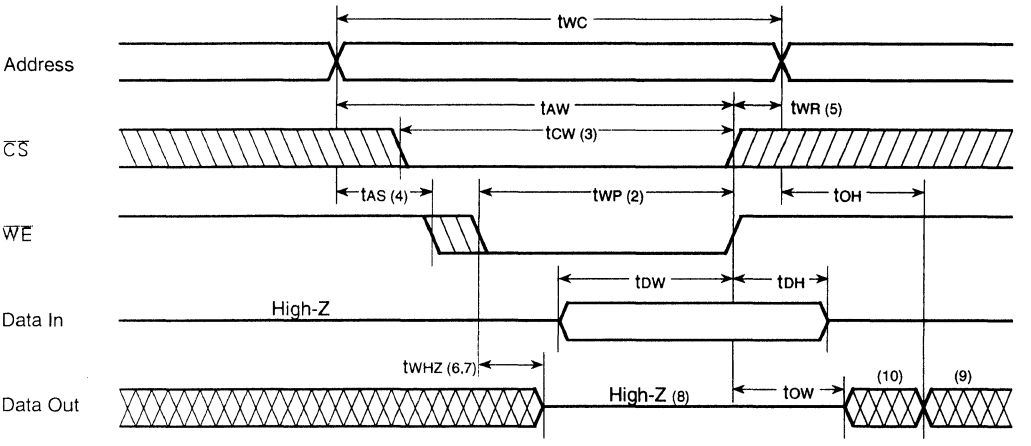
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM681002A-12 : 200 mA (Max.)
  - KM681002A-15 : 190 mA (Max.)
  - KM681002A-17 : 180 mA (Max.)
  - KM681002A-20 : 170 mA (Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM681002AJ : 32-SOJ-400
  - KM681002AT : 32-TSOP2-400F

GENERAL DESCRIPTION

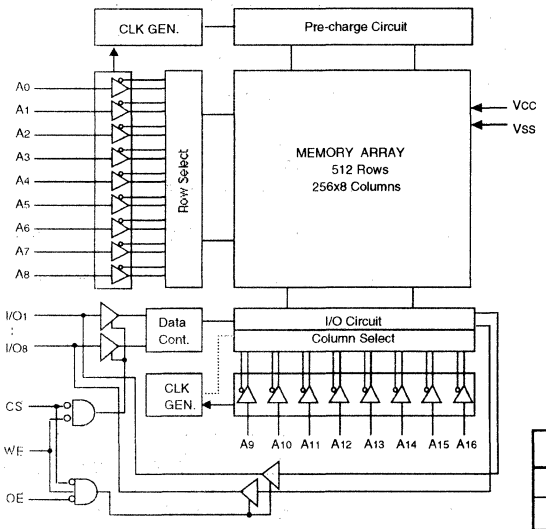
The KM681002A is a 1,048,576-bit high-speed static random access memory organized as 131,072 words by 8 bits.

The KM681002A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

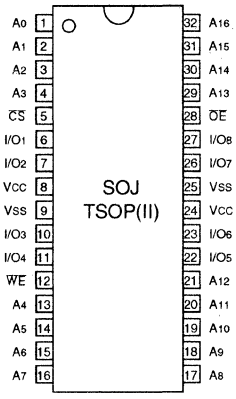
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM681002A is packaged in a 400 mil 32-pin plastic SOJ and TSOP(II) forward.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
VCC	Power (+5V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty, $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0 mA	12 ns	-	200	mA
			15 ns	-	190	
			17 ns	-	180	
			20 ns	-	170	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

*Note : Vcc=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

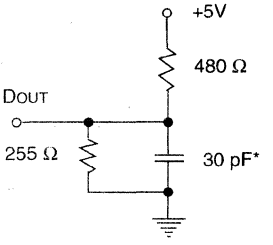
AC CHARACTERISTICS

TEST CONDITIONS

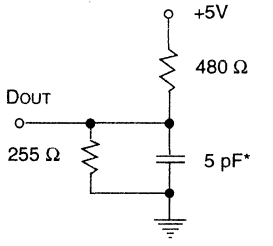
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681002A -12		KM681002A -15		KM681002A -17		KM681002A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	12	-	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	6	-	7	-	8	-	9	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	12	-	15	-	17	-	20	ns

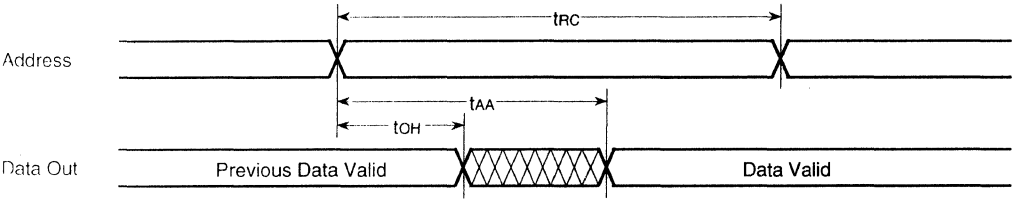
WRITE CYCLE

Parameter	Symbol	KM681002A -12		KM681002A -15		KM681002A -17		KM681002A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

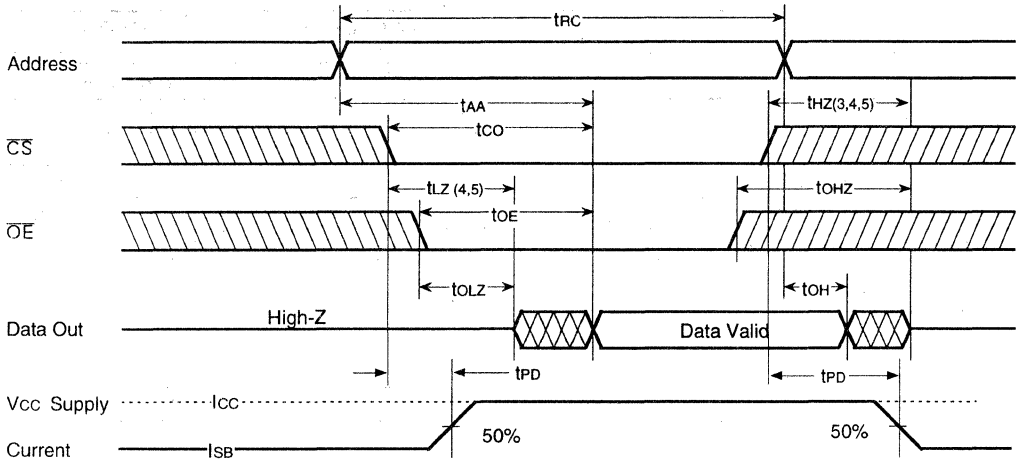
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

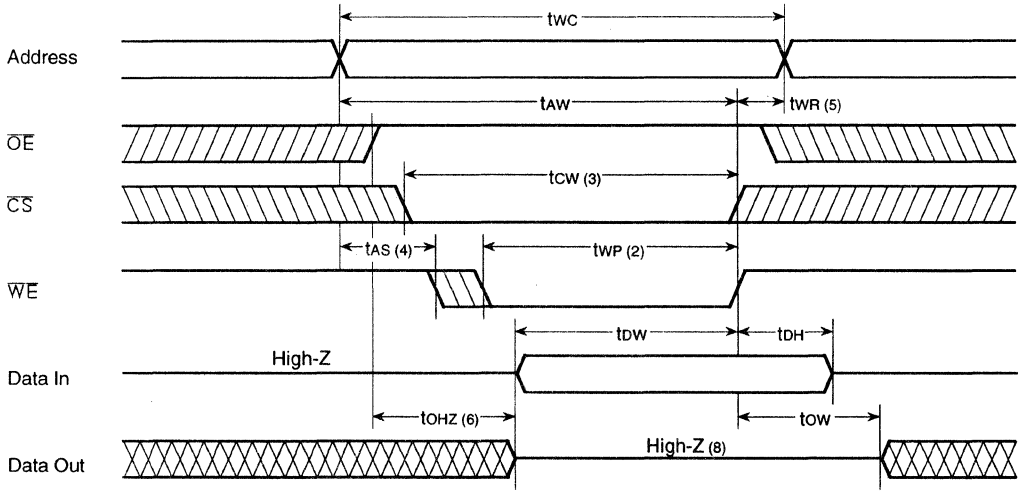
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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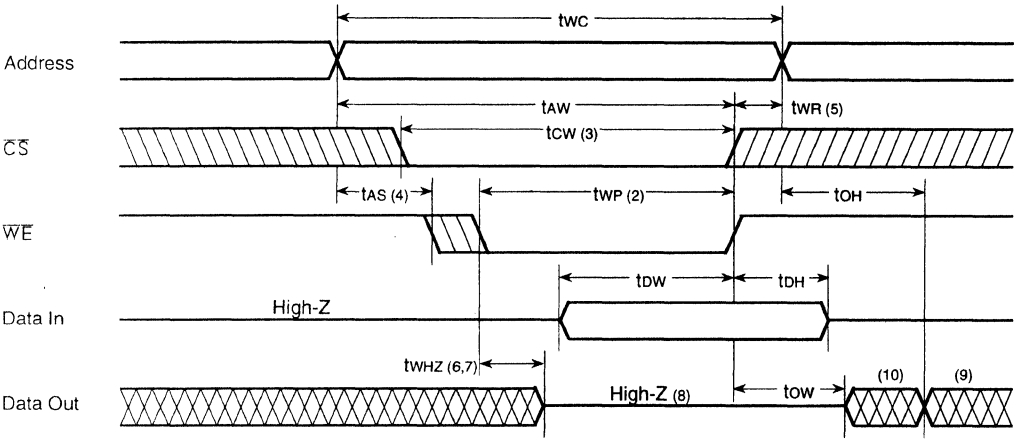
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

SAMSUNG ELECTRONICS

64K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM6161002-15 : 230 mA(Max.)
  - KM6161002-17 : 220 mA(Max.)
  - KM6161002-20 : 210 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Data Byte Control : $\overline{LB}$: I/O_1~I/O_8
  - $\overline{UB}$: I/O_9~I/O_{16}
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM6161002J : 44-SOJ-400

GENERAL DESCRIPTION

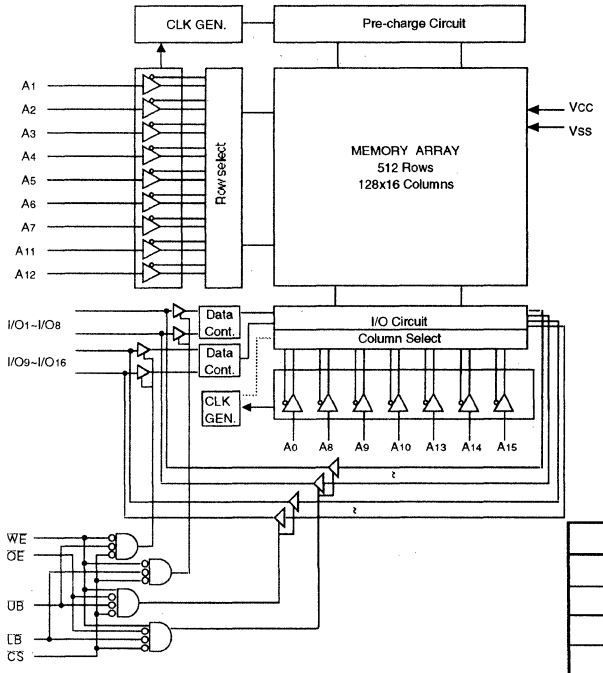
The KM6161002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits.

The KM6161002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{UB}$,$\overline{LB}$).

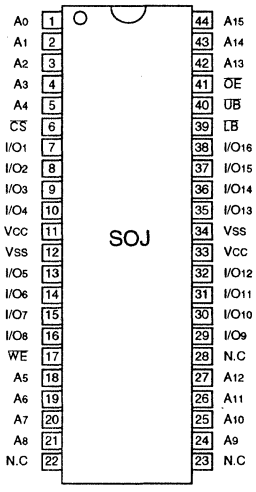
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM6161002 is packaged in a 400 mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O_1~I/O_8)
$\overline{UB}$	Upper-byte Control(I/O_9~I/O_{16})
I/O_1~I/O_{16}	Data Inputs/Outputs
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	15 ns	-	230	mA
		$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL},	17 ns	-	220	
		I_{OUT}=0 mA	20 ns	-	210	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0 MHz V_{IN} ≥ V_{CC}-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

*Note : V_{CC}=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

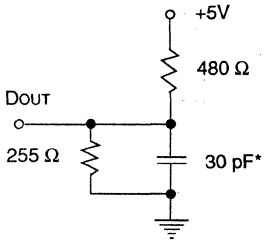
AC CHARACTERISTICS

TEST CONDITIONS

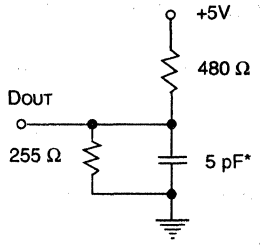
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

PARAMETER	SYMBOL	KM6161002-15		KM6161002-17		KM6161002-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Output	t_{OE}	-	8	-	9	-	10	ns
$\overline{LB}$,$\overline{UB}$ Access Time	t_{BA}	-	8	-	9	-	10	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	4	-	ns

WRITE CYCLE

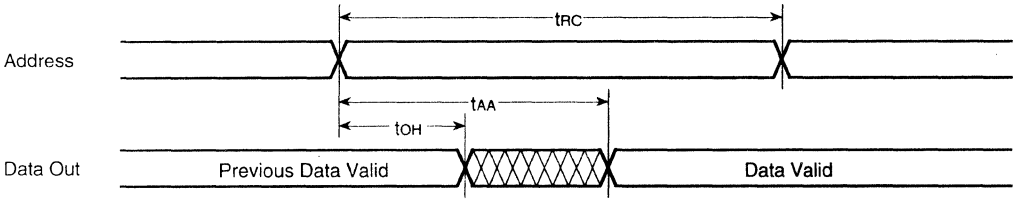
Parameter	Symbol	KM6161002-15		KM6161002-17		KM6161002-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	14	-	ns
$\overline{LB}$,$\overline{UB}$ Valid to End of Write	tBW	12	-	13	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	8	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

2

TIMING DIAGRAMS

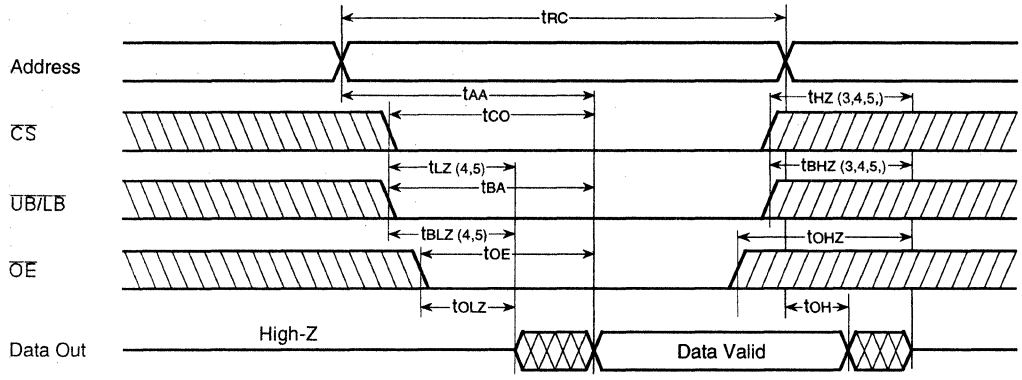
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



TIMING DIAGRAMS

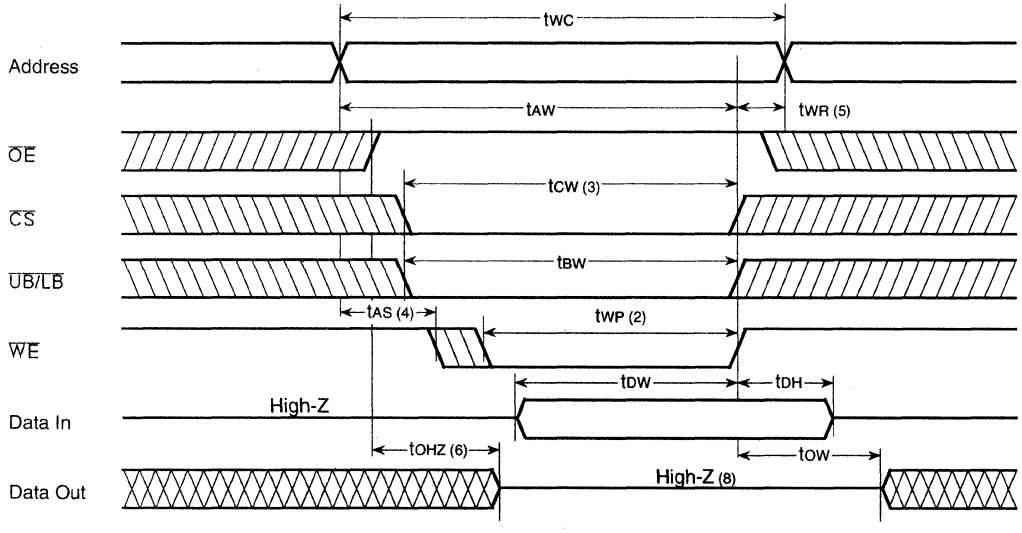
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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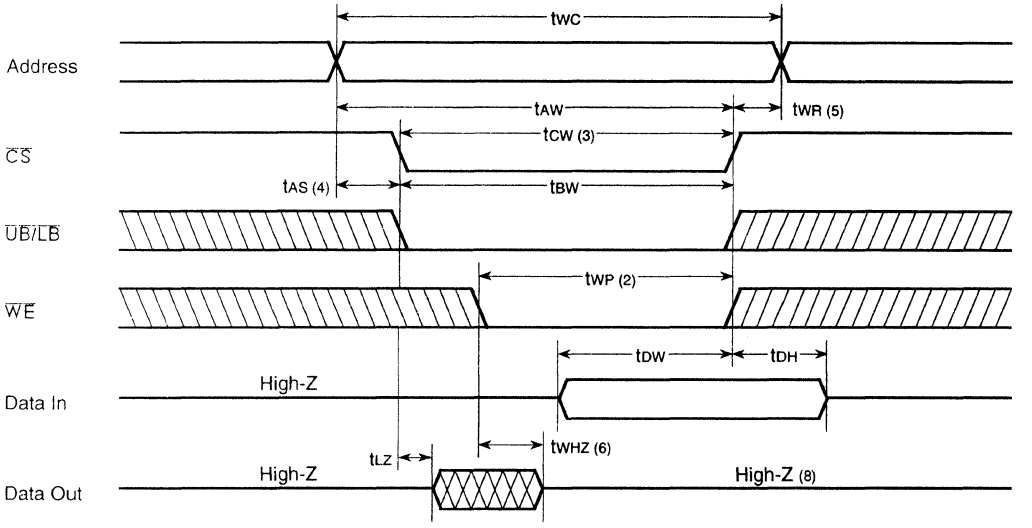
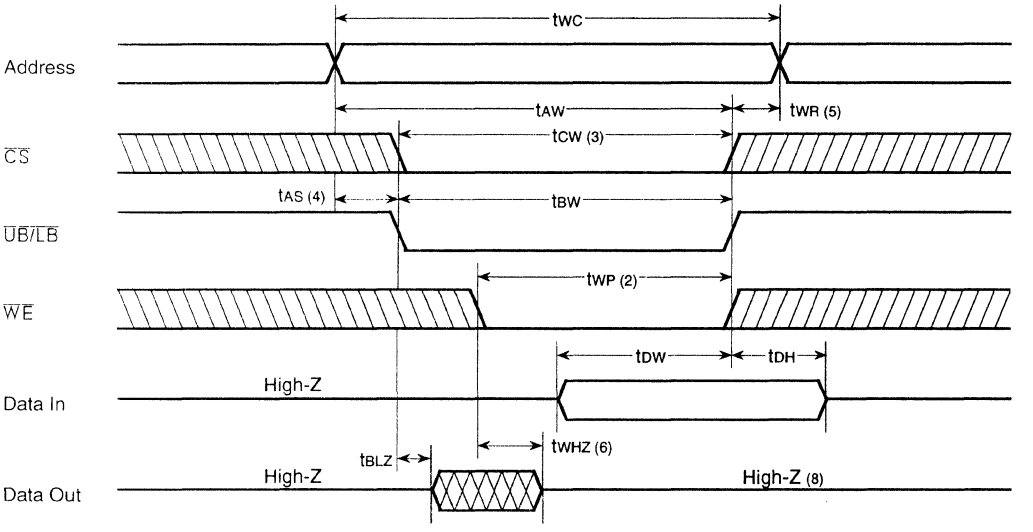
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$/$\overline{LB}$ Controlled)



SAMSUNG ELECTRONICS

NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*Note : X means Don't Care.

64K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM6161002A-12 : 220 mA(Max.)
  - KM6161002A-15 : 210 mA(Max.)
  - KM6161002A-17 : 200 mA(Max.)
  - KM6161002A-20 : 190 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Data Byte Control : $\overline{LB}$: I/O1~I/O8
  - $\overline{UB}$: I/O9~I/O16
- Standard Pin Configuration
  - KM6161002AJ : 44-SOJ-400
  - KM6161002AT : 44-TSOP2-400F

GENERAL DESCRIPTION

The KM6161002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits.

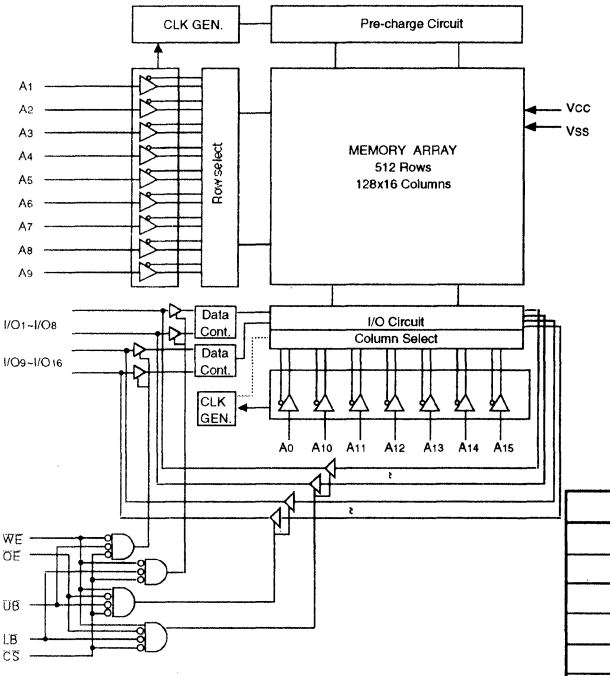
The KM6161002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{UB}$,$\overline{LB}$).

The device is fabricated using Samsung`s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

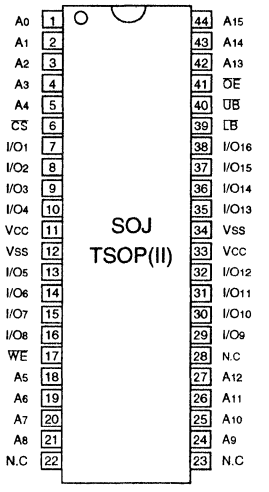
The KM6161002A is packaged in a 400 mil 44-pin plastic SOJ and TSOP(II) forward.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	µA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	220	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	15 ns	-	210	
		V_{IN} = V_{IH} or V_{IL}	17 ns	-	200	
			20 ns	-	190	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100µA		-	3.95	V

*Note : Vcc=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

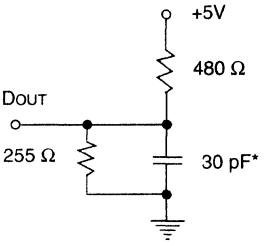
AC CHARACTERISTICS

TEST CONDITIONS

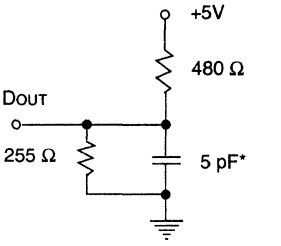
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6161002A -12		KM6161002A -15		KM6161002A -17		KM6161002A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	12	-	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	17	-	20	ns
Output Enable to Output	t_{OE}	-	6	-	7	-	8	-	9	ns
$\overline{LB}$,$\overline{UB}$ Access Time	t_{BA}	-	6	-	7	-	8	-	9	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	0	-	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	0	9	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns

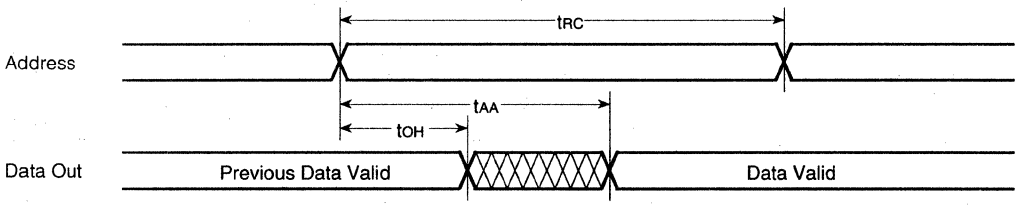
WRITE CYCLE

Parameter	Symbol	KM6161002A -12		KM6161002A -15		KM6161002A -17		KM6161002A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
$\overline{LB}$,$\overline{UB}$ Valid to End of Write	tBW	8	-	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

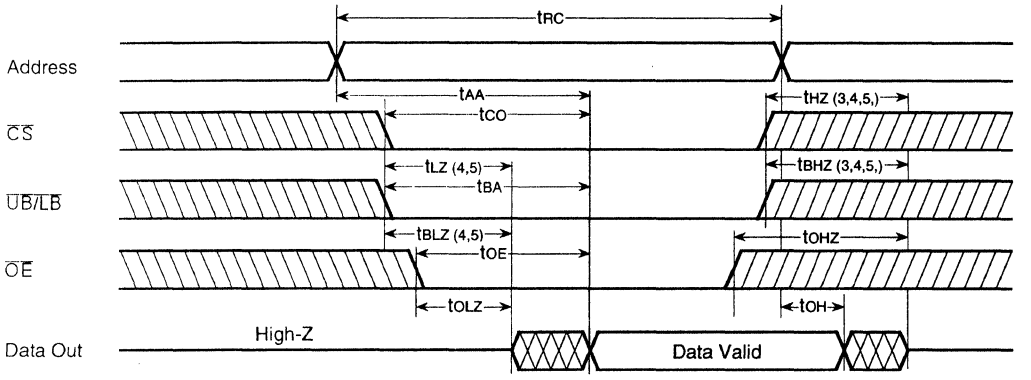
($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS

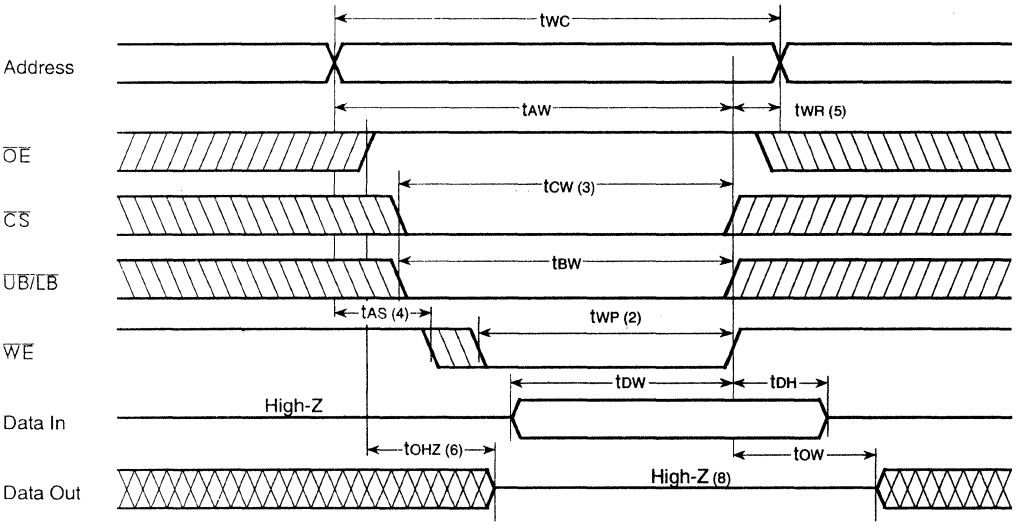
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

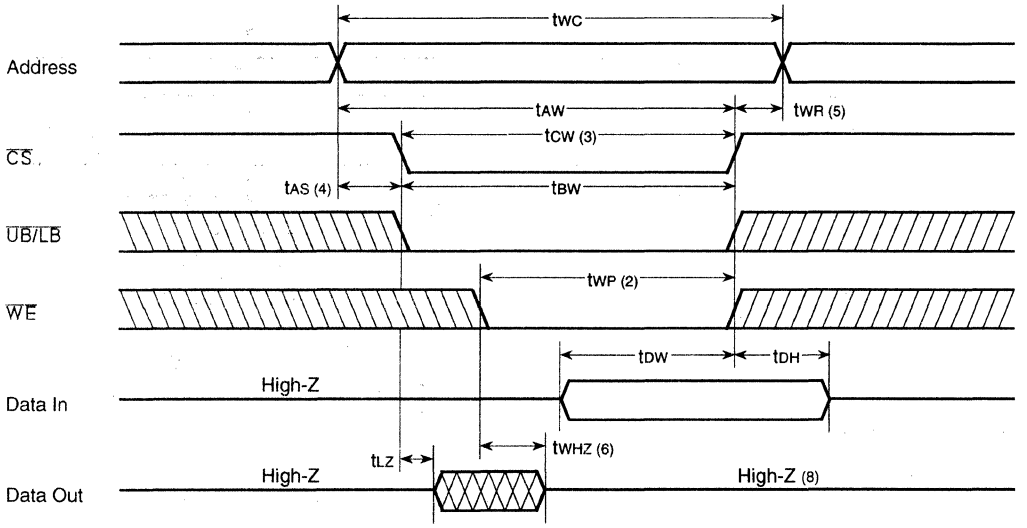
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)

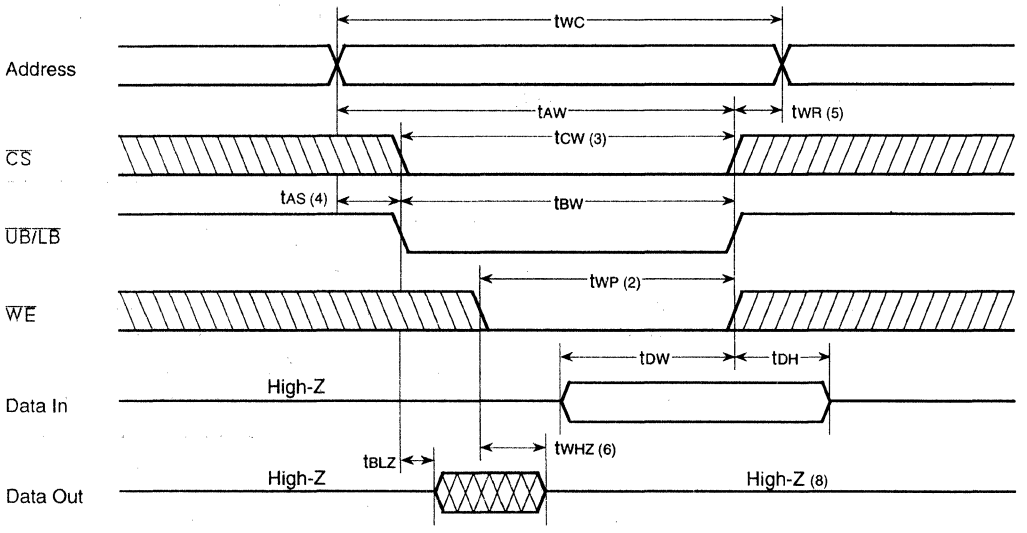


SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$/$\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*Note : X means Don't Care.

1M x 4 Bit (With $\overline{OE}$)High-Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 12,13,15 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS): 30 mA(Max.)
  - Operating KM64B4002-12 : 185 mA(Max.)
  - KM64B4002-13 : 185 mA(Max.)
  - KM64B4002-15 : 180 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM64B4002J: 32-SOJ-400

GENERAL DESCRIPTION

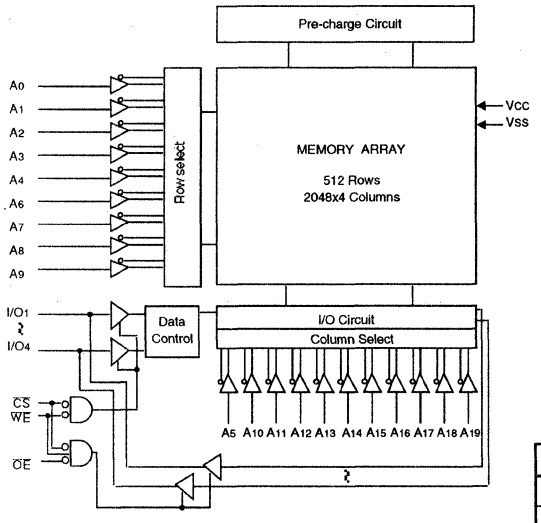
The KM64B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits.

The KM64B4002 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

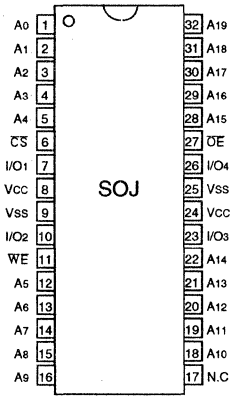
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM64B4002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(TOP VIEW)*



Pin Name	Pin Function
A0-A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs/Outputs
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-10	10	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	185	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	13 ns	-	185	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15 ns	-	180	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	30	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

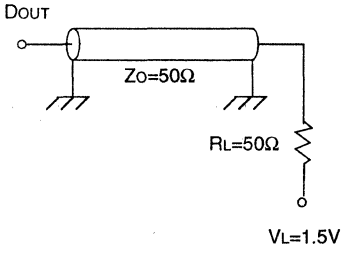
AC CHARACTERISTICS

TEST CONDITIONS

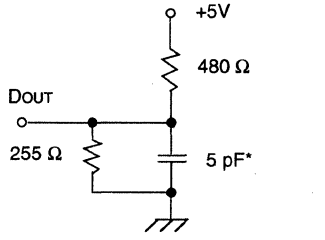
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tHZ, tLZ, twHZ, tow, tOLZ & tOHZ)



* Including Scope and Jig Capacitance

READ CYCLE

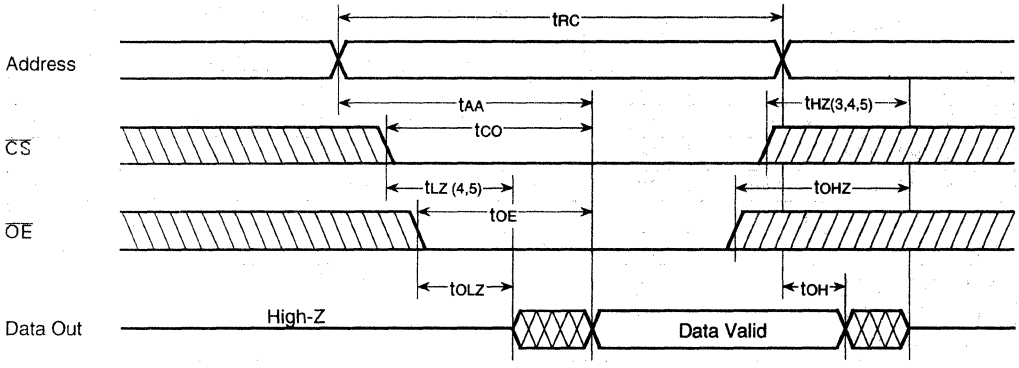
Parameter	Symbol	KM64B4002-12		KM64B4002-13		KM64B4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	6	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	-	6	-	6	-	6	ns
Output Disable to High-Z Output	tOHZ	-	6	-	6	-	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B4002-12		KM64B4002-13		KM64B4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	13	-	15	-	ns
Chip Select to End of Write	t_{CW}	8	-	9	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	10	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	-	6	-	6	-	6	ns
Data to Write Time Overlap	t_{DW}	6	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

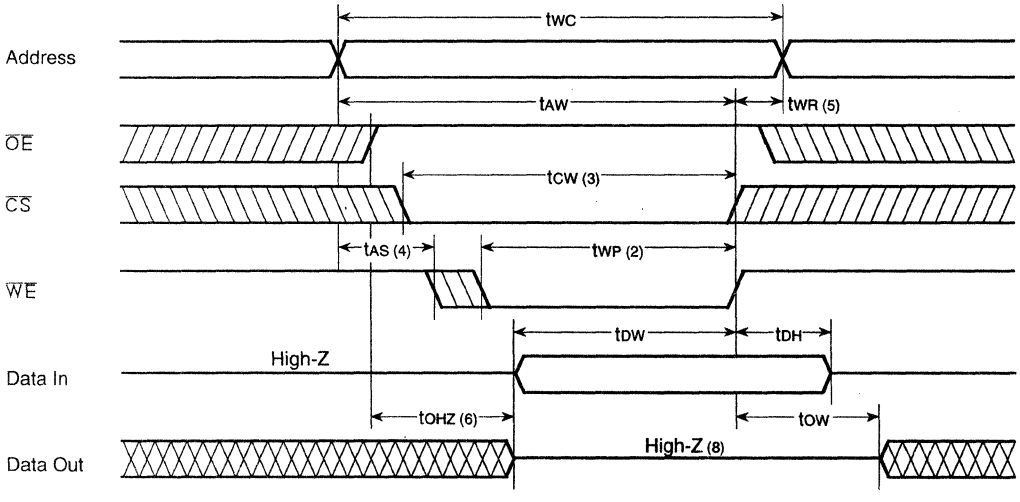
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=VIH)



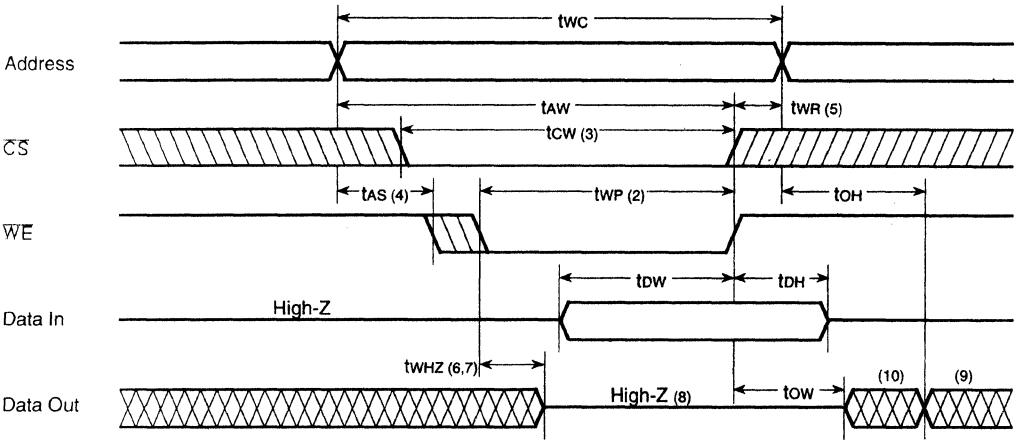
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

1M x 4 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,15,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM644002A-12 : 180 mA(Max.)
  - KM644002A-15 : 170 mA(Max.)
  - KM644002A-20 : 160 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM644002AJ: 32-SOJ-400

GENERAL DESCRIPTION

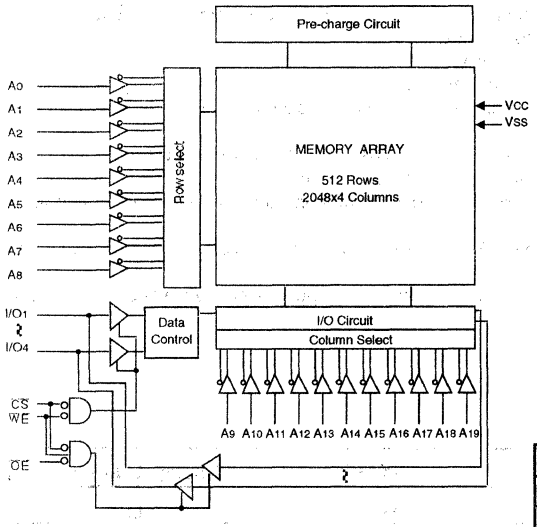
The KM644002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits.

The KM644002A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

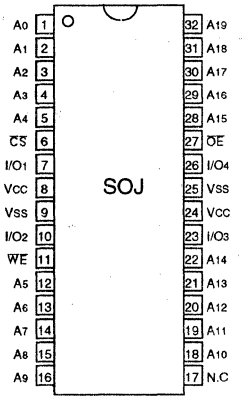
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM644002A is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(TOP VIEWS)*



Pin Name	Pin Function
A0-A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs/Output
Vcc	Power (+5V)
Vss	Ground
N.C	No Connections

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Max.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	Icc	Min. Cycle, 100% Duty	12 ns	-	180	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA,	15 ns	-	170	
		V_{IN} = V_{IH} or V_{IL}	20ns	-	160	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	50	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN}≤0.2V or V_{IN} ≥ Vcc-0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

CAPACITANCE (f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

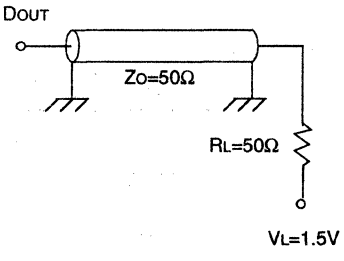
AC CHARACTERISTICS

TEST CONDITIONS

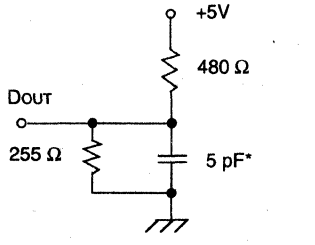
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tOLZ, tOHZ, tHZ, tLZ, tow & twz)



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM644002A-12		KM644002A-15		KM644002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	20	ns
Output Enable to Output	t_{OE}	-	6	-	7	-	9	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	-	6	-	7	-	9	ns
Chip Disable to High-Z Output	t_{HZ}	-	6	-	7	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

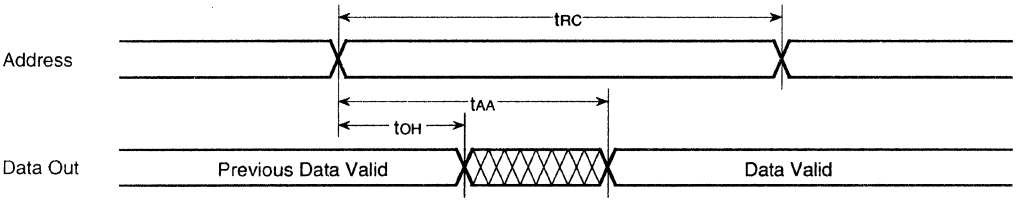
Parameter	Symbol	KM644002A-12		KM644002A-15		KM644002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP	10	-	12	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	-	6	-	7	-	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

2

TIMING DIAGRAMS

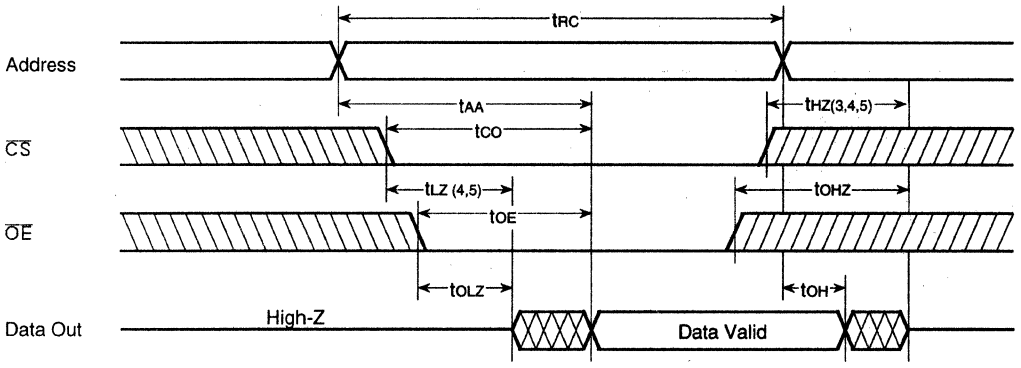
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

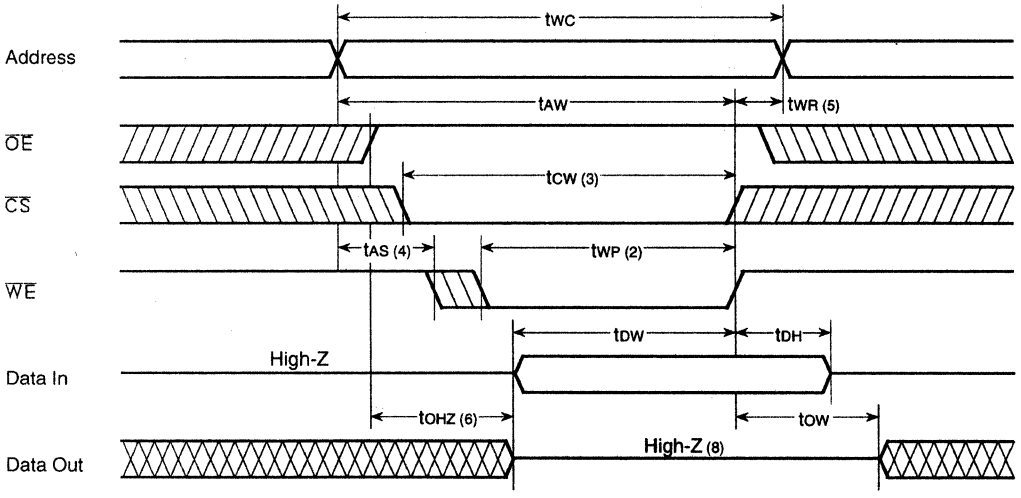
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



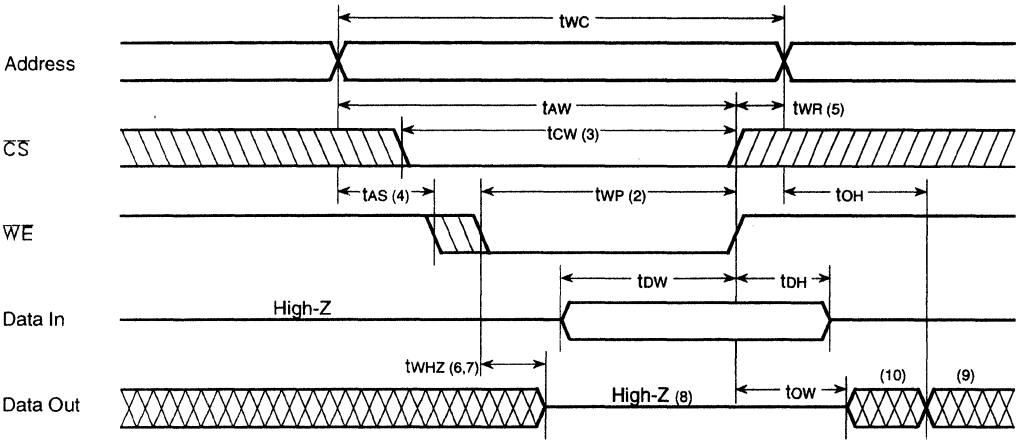
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =V_{IL}
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

1M x 4 Bit (With $\overline{OE}$) High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 17,20,25 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS):10 mA(Max.)
  - 500μA(max.)-L Ver
  - Operating KM644002/L-17 : 170 mA(Max.)
  - KM644002/L-20 : 150 mA(Max.)
  - KM644002/L-25 : 130 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage :2V(Min.)-L Ver. Only
- Standard Pin Configuration
  - KM644002J/LJ : 32- SOJ- 400

GENERAL DESCRIPTION

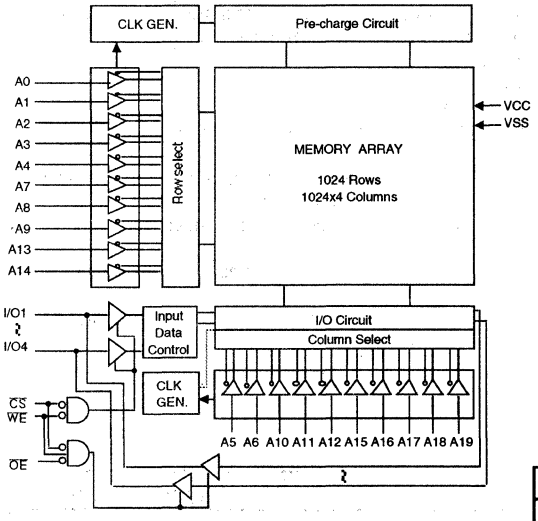
The KM644002/L is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits.

The KM644002/L uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

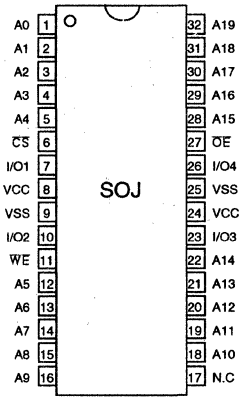
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM644002/L is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	17 ns	-	170	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	20 ns	-	150	
		V_{IN} = V_{IH} or V_{IL}	25 ns	-	130	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz	-	-	10	mA
		V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V	L-Ver	-	500	μA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

Note * : Temp. = 25°C, Vcc=5V±5%

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

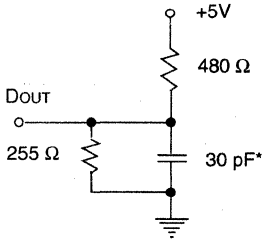
AC CHARACTERISTICS

TEST CONDITIONS

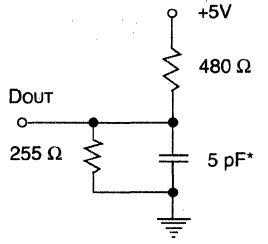
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM644002-17 KM644002L-17		KM644002-20 KM644002L-20		KM644002-25 KM644002L-25		UNIT
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17	-	20	-	25	-	ns
Address Access Time	t_{AA}	-	17	-	20	-	25	ns
Chip Select to Output	t_{CO}	-	17	-	20	-	25	ns
Output Enable to Valid Output	t_{OE}	-	8	-	10	-	12	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3	-	4	-	5	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	17	-	20	-	25	ns

WRITE CYCLE

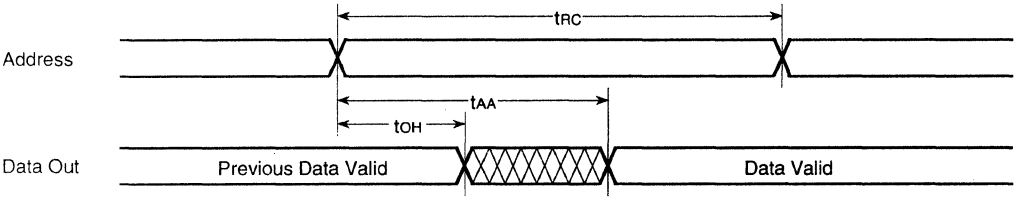
Parameter	Symbol	KM644002-17 KM644002L-17		KM644002-20 KM644002L-20		KM644002-25 KM644002L-25		UNIT
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	17	-	20	-	25	-	ns
Chip Select to End of Write	tCW	12	-	13	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	15	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

2

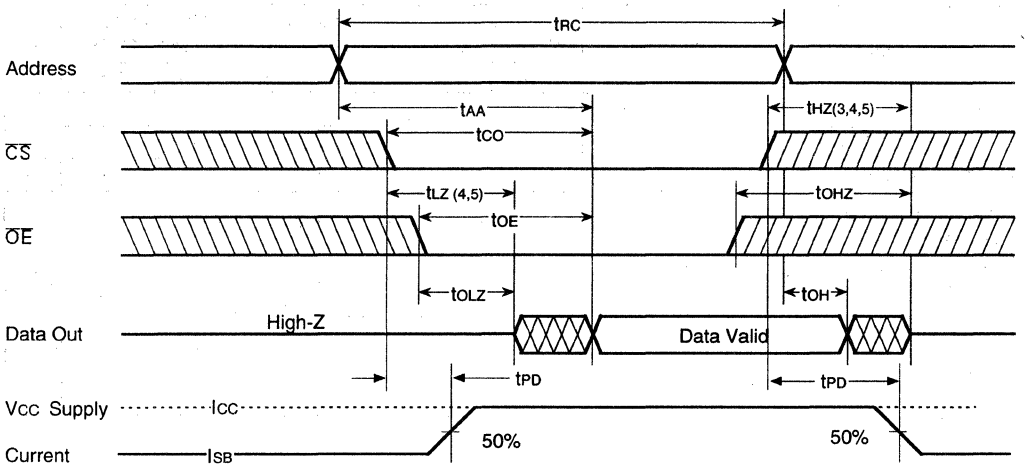
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



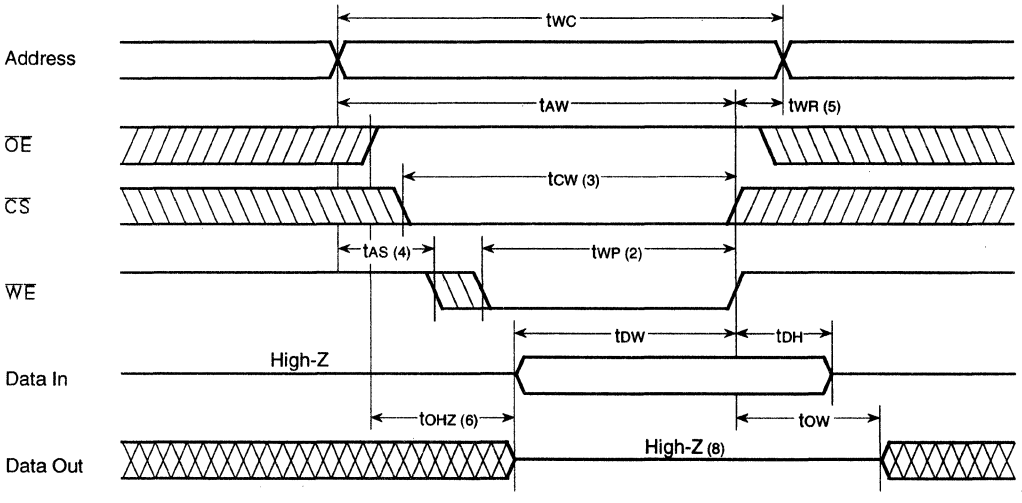
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

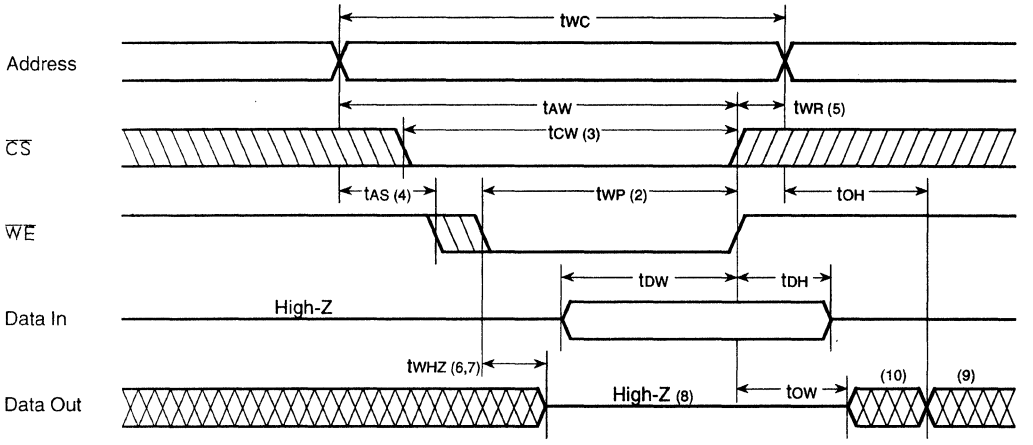
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

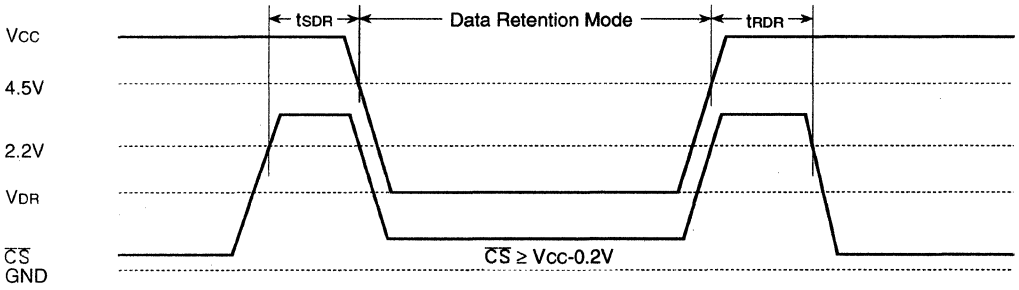
Note : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA=0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Max	Unit
Vcc for Data Retention	VDR	$\overline{CS}$≥Vcc-0.2V	2	5.5	V
Data Retention Current	IDR	Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V VIN≥Vcc-0.2V or VIN≤0.2V	-	200	μA
Data Retention Set-up Time	tSDR	See Data Retention	0	-	ns
Recovery Time	tRDR	Wave forms(below)	5	-	ms

* L-Version Only.

DATA RETENTION WAVEFORM 1 ($\overline{CS}$ Controlled)



512K x 8 Bit High Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 12,13,15 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS): 30 mA(Max.)
  - Operating KM68B4002-12 : 195 mA(Max.)
  - KM68B4002-13 : 195 mA(Max.)
  - KM68B4002-15 : 190 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM68B4002J: 36-SOJ-400

GENERAL DESCRIPTION

The KM68B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits.

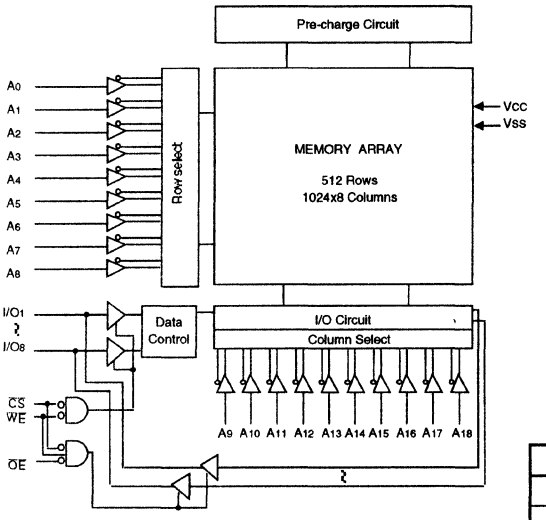
The KM68B4002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

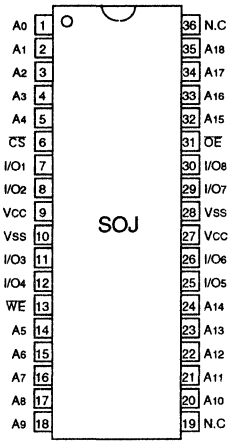
The KM68B4002 is packaged in a 400 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(TOP VIEW)*



Pin Name	Pin Function
A0-A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-10	10	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	195	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	13 ns	-	195	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15 ns	-	190	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	30	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

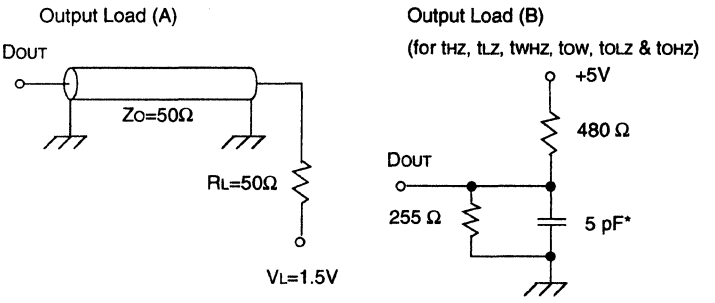
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

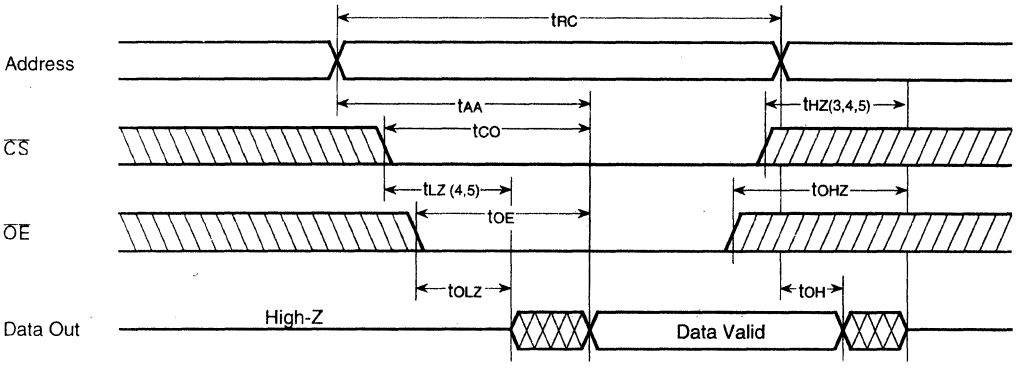
Parameter	Symbol	KM68B4002-12		KM68B4002-13		KM68B4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	12	-	13	-	15	-	ns
Address Access Time	t_{AA}	-	12	-	13	-	15	ns
Chip Select to Output	t_{CO}	-	12	-	13	-	15	ns
Output Enable to Valid Output	t_{OE}	-	6	-	6	-	6	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	-	6	-	6	-	6	ns
Output Disable to High-Z Output	t_{OHZ}	-	6	-	6	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68B4002-12		KM68B4002-13		KM68B4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	13	-	15	-	ns
Chip Select to End of Write	t_{CW}	8	-	9	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	10	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	-	6	-	6	-	6	ns
Data to Write Time Overlap	t_{DW}	6	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

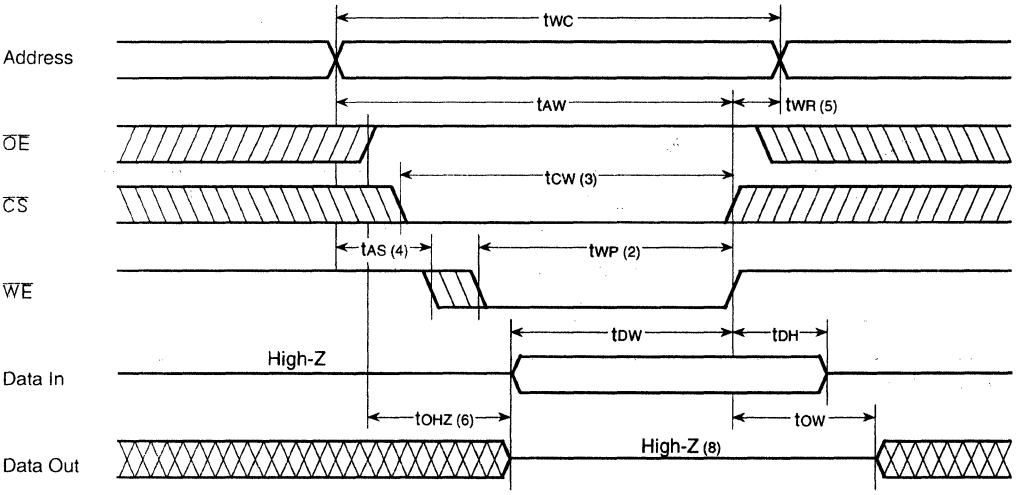
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

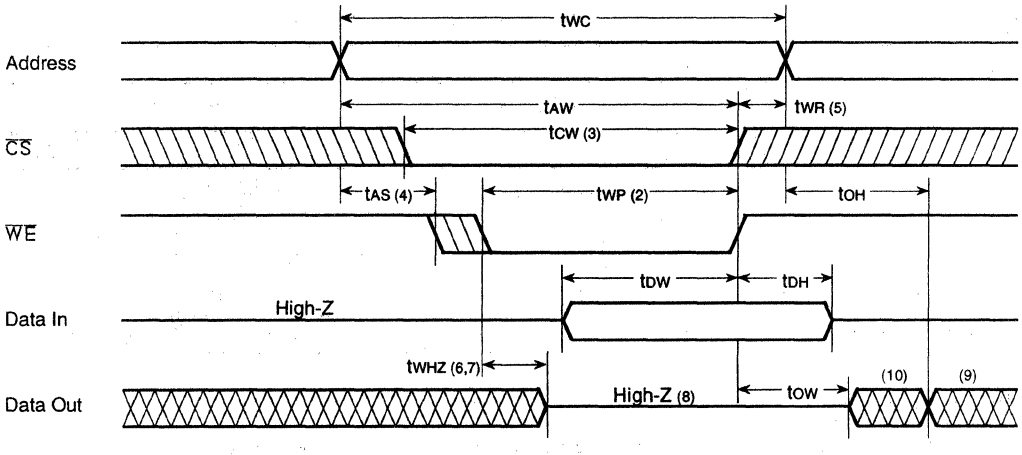
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. twp is measured from the beginning of write to the end of write.
3. tcw is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. twR is measured from the end of write to the address change. twR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

512K x 8 Bit High Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,15,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50 mA
    (CMOS): 10 mA
  - Operating KM684002A-12 : 200 mA(Max.)
    KM684002A-15 : 190 mA(Max.)
    KM684002A-20 : 180 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM684002AJ: 36-SOJ-400

GENERAL DESCRIPTION

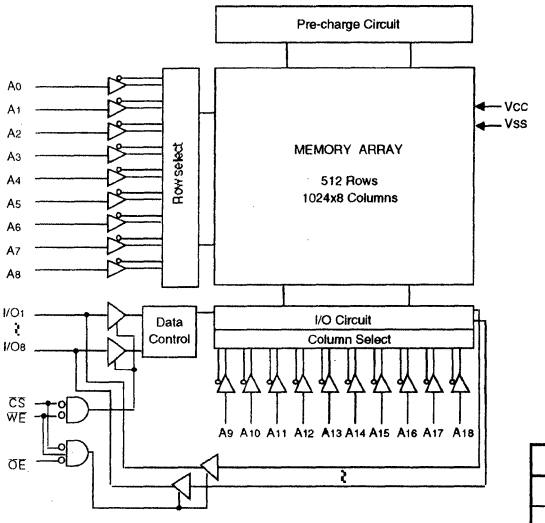
The KM684002A is a 4,194,304-bit high-speed Static Random Access Memory organization as 524,288 words by 8 bits.

The KM684002A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

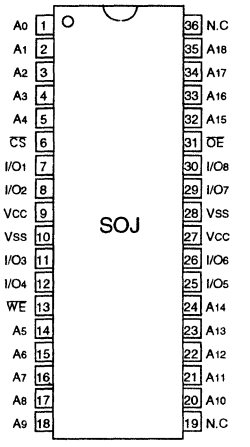
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM684002A is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Input/Output
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	200	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA,	15 ns	-	190	
		V_{IN} = V_{IH} or V_{IL}	20 ns	-	180	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	50	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN}≤0.2V or V_{IN} ≥ Vcc-0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

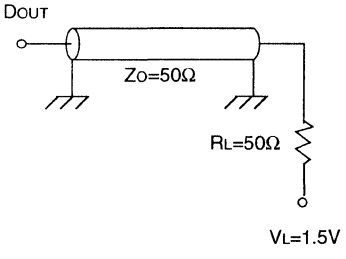
AC CHARACTERISTICS

TEST CONDITIONS

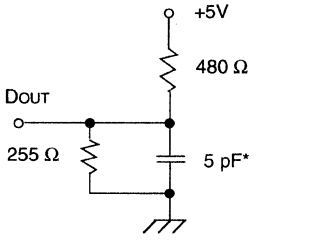
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tOLZ, tOHZ, tHZ, tOW, tLZ & twz)



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM684002A-12		KM684002A-15		KM684002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	20	ns
Output Enable to Output	t_{OE}	-	6	-	7	-	9	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	-	6	-	7	-	9	ns
Chip Disable to High-Z Output	t_{HZ}	-	6	-	7	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

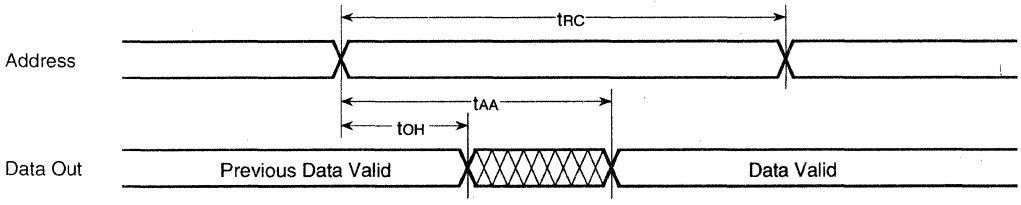
WRITE CYCLE

Parameter	Symbol	KM684002A-12		KM684002A-15		KM684002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	12	-	ns
Write Pulse Width(OE High)	tWP	8	-	10	-	12	-	ns
Write Pulse Width(OE Low)	tWP	10	-	12	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	-	6	-	7	-	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

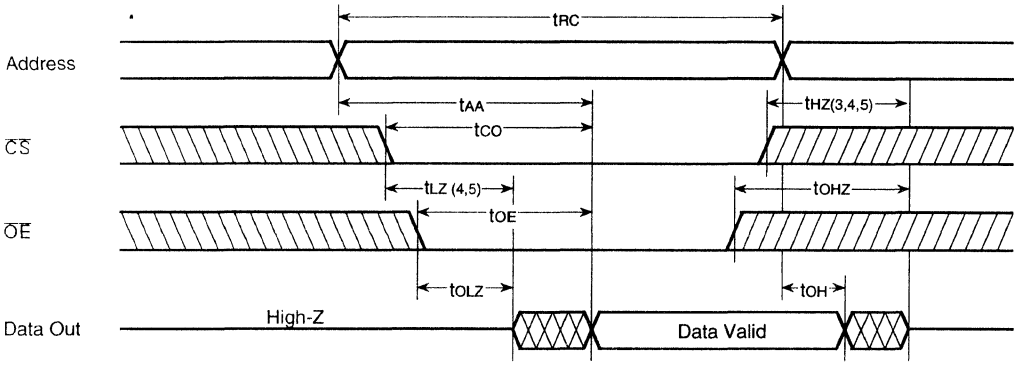
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



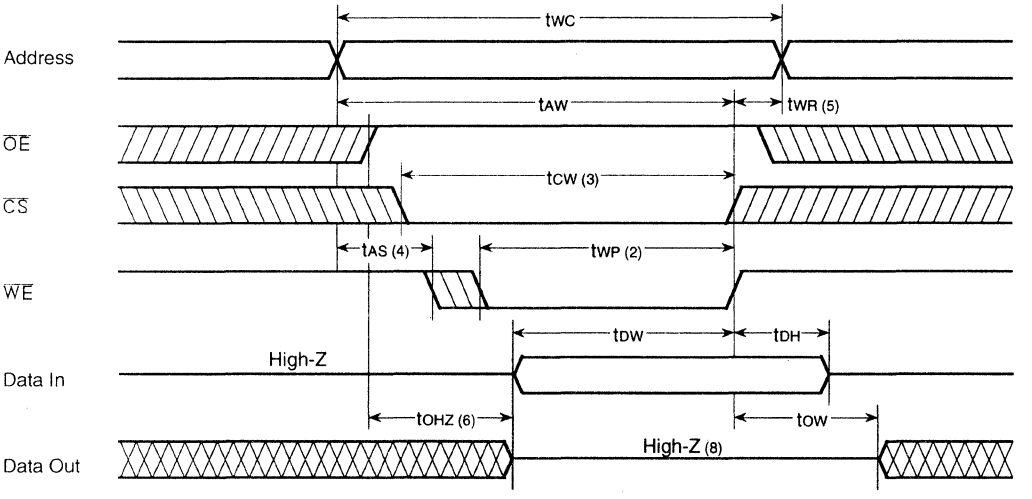
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



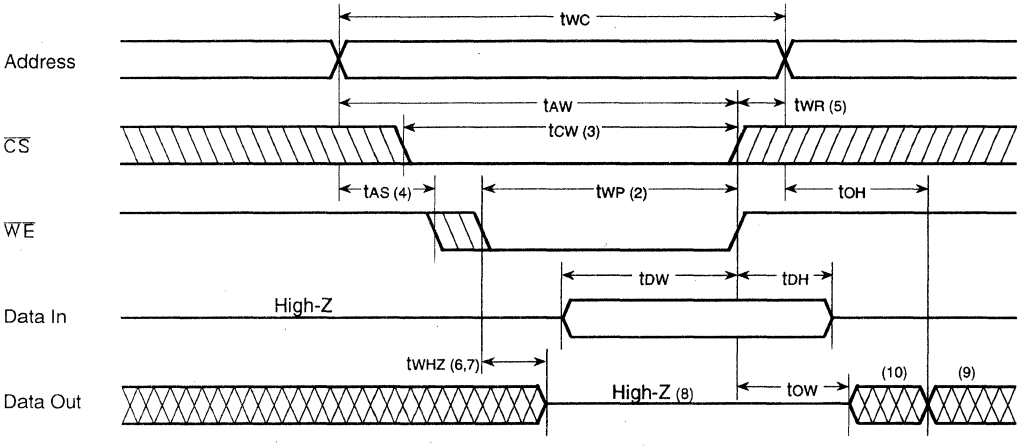
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 17,20,25 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS):10 mA(Max.)
  - 500μA(max.)-L Ver
  - Operating KM684002/L-17 : 180 mA(Max.)
  - KM684002/L-20 : 170 mA(Max.)
  - KM684002/L-25 : 160 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V(Min) - L Ver Only
- Standard Pin Configuration
  - KM684002J/LJ : 36-SOJ-400

GENERAL DESCRIPTION

The KM684002/L is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits.

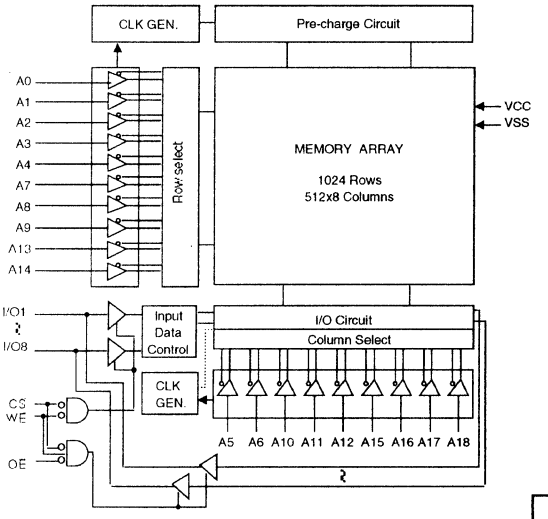
The KM684002/L uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

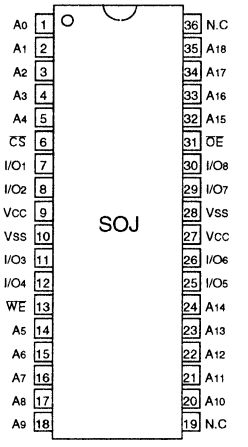
The KM684002/L is packaged in a 400 mil 36-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A0-A18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs/Outputs
VCC	Power (+5V)
VSS	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	µA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	17 ns	-	180	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	20 ns	-	170	
		V_{IN} = V_{IH} or V_{IL}	25 ns	-	160	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz	-	-	10	mA
		V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V	L-Ver		500	µA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100µA		-	3.95	V

Note * : Temp. = 25°C, Vcc=5V±5%

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

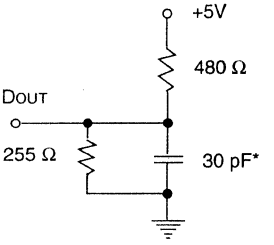
AC CHARACTERISTICS

TEST CONDITIONS

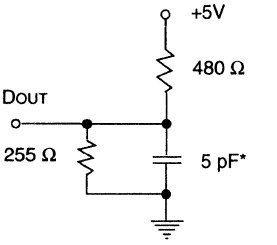
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM644002-17 KM644002L-17		KM644002-20 KM644002L-20		KM644002-25 KM644002L-25		UNIT
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17	-	20	-	25	-	ns
Address Access Time	t_{AA}	-	17	-	20	-	25	ns
Chip Select to Output	t_{CO}	-	17	-	20	-	25	ns
Output Enable to Valid Output	t_{OE}	-	8	-	10	-	12	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3	-	4	-	5	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	17	-	20	-	25	ns

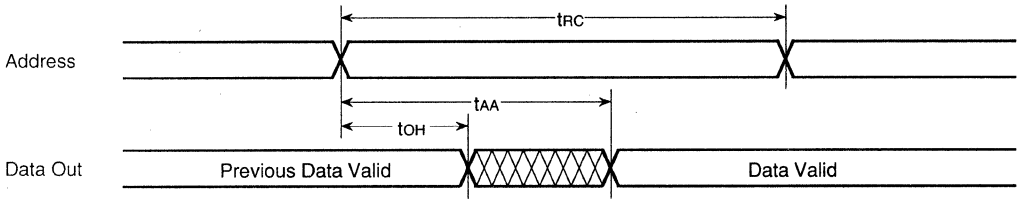
WRITE CYCLE

Parameter	Symbol	KM644002-17 KM644002L-17		KM644002-20 KM644002L-20		KM644002-25 KM644002L-25		UNIT
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	17	-	20	-	25	-	ns
Chip Select to End of Write	tCW	12	-	13	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	15	-	ns
Write Pulse Width ($\overline{OE}$ High)	tWP	12	-	13	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

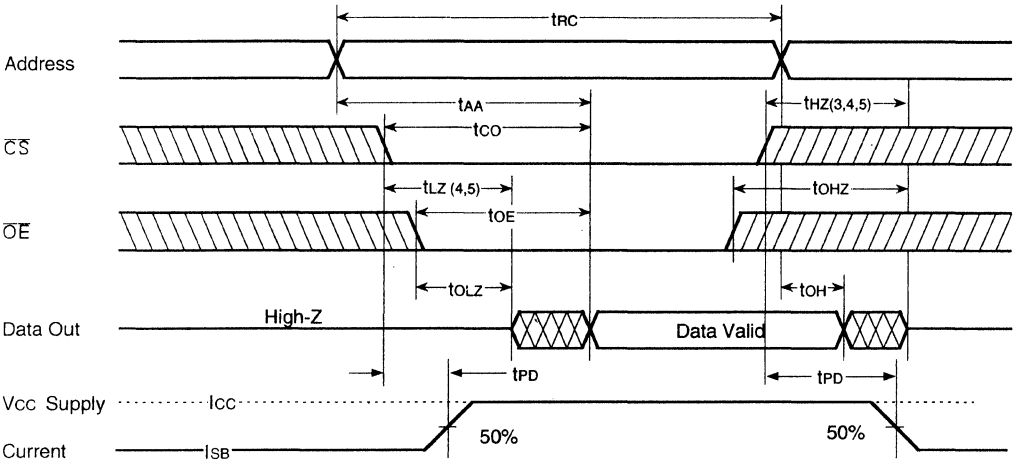
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



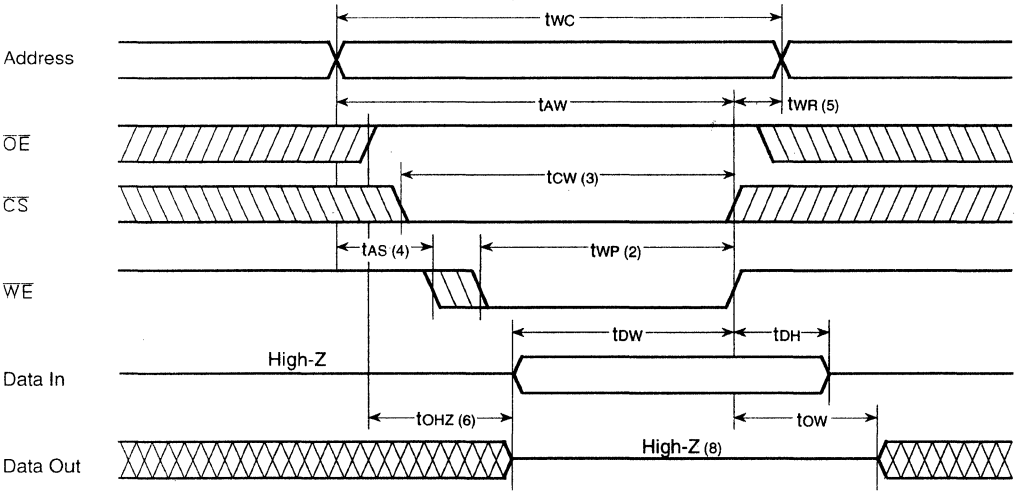
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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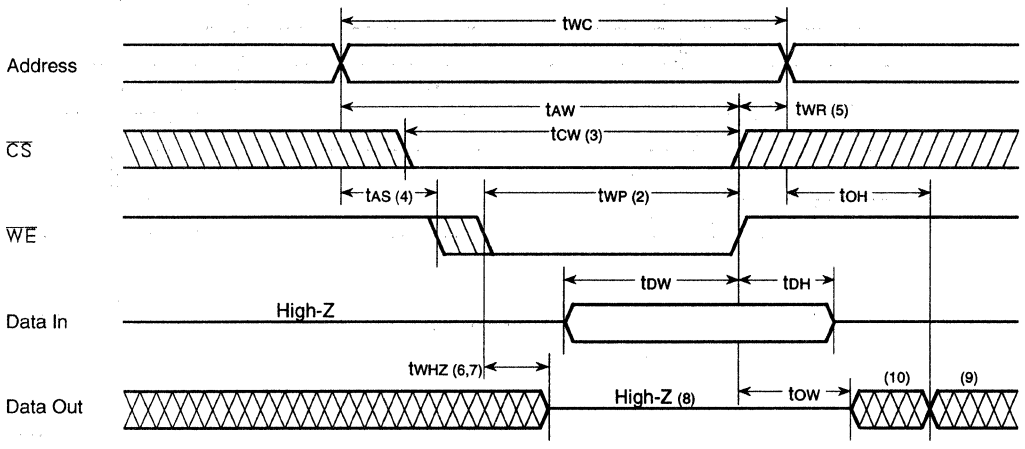
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

DATA RETENTION CHARACTERISTICS* (T_A=0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$	2	5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.0V, $\overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	-	200	µA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0	-	ns
Recovery Time	t_{RDR}	Wave forms(below)	5	-	ms

* L-Version Only.

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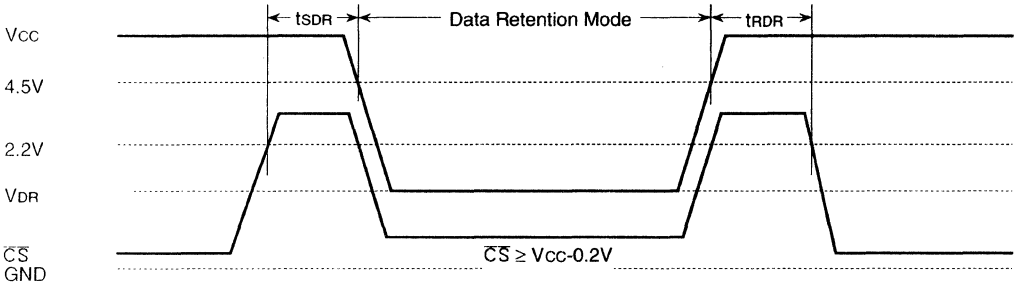
DATA RETENTION WAVEFORM 1 ($\overline{CS}$ Controlled)



SAMSUNG ELECTRONICS

256K x 16 Bit High-Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 12,13,15 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS) : 30 mA(Max.)
  - Operating KM616B4002-12 : 270 mA(Max.)
  - KM616B4002-13 : 265 mA(Max.)
  - KM616B4002-15 : 260 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Data Byte Control : $\overline{LB}$: I/O_1~I/O_8
  - $\overline{UB}$: I/O_9~I/O_{16}
- Standard Pin Configuration
  - KM616B4002J : 44-SOJ-400

GENERAL DESCRIPTION

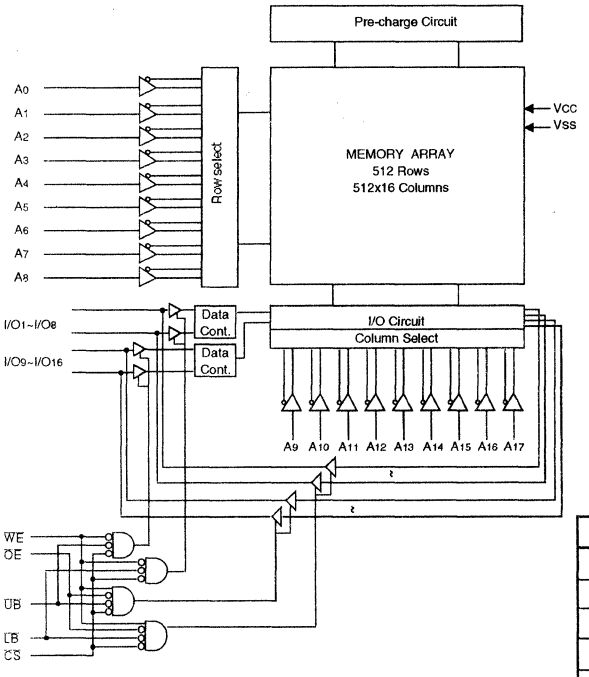
The KM616B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits.

The KM616B4002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{UB}$,$\overline{LB}$).

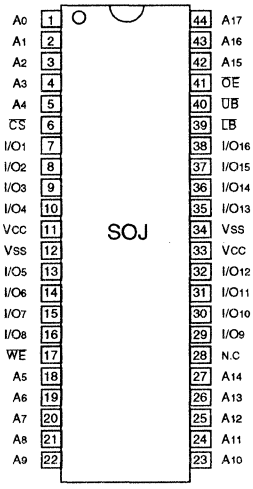
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM616B4002 is packaged in a 400 mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O_1~I/O_8)
$\overline{UB}$	Upper-byte Control(I/O_9~I/O_{16})
I/O_1~I/O_{16}	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-10	10	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty,	12 ns	-	270	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	13 ns	-	265	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15 ns	-	260	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	30	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, TA=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT}=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

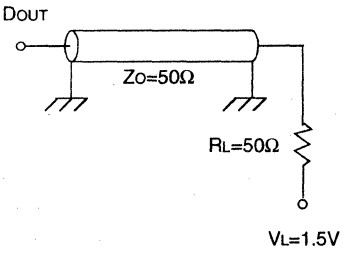
AC CHARACTERISTICS

TEST CONDITIONS

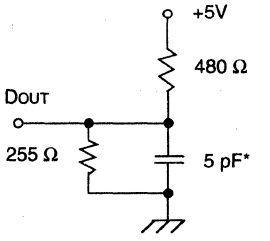
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

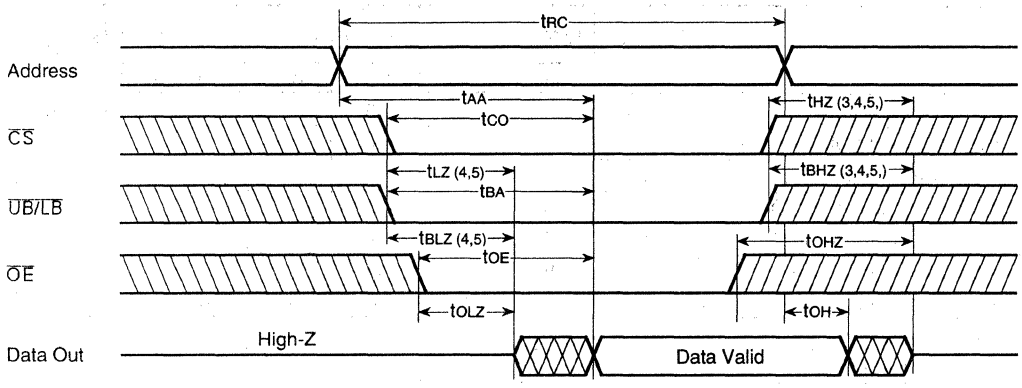
Parameter	Symbol	KM616B4002-12		KM616B4002-13		KM616B4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12	-	13	-	15	-	ns
Address Access Time	t_{AA}	-	12	-	13	-	15	ns
Chip Select to Output	t_{CO}	-	12	-	13	-	15	ns
Output Enable to Output	t_{OE}	-	6	-	6	-	6	ns
$\overline{LB}$,$\overline{UB}$ Access Time	t_{BA}	-	6	-	6	-	6	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	-	6	-	6	-	6	ns
Output Disable to High-Z Output	t_{OHZ}	-	6	-	6	-	6	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	t_{BHZ}	-	6	-	6	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM616B4002-12		KM616B4002-13		KM616B4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	13	-	15	-	ns
Chip Select to End of Write	t_{CW}	8	-	9	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	10	-	11	-	12	-	ns
$\overline{LB}$,$\overline{UB}$ valid to end of write	t_{BW}	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	-	6	-	6	-	6	ns
Data to Write Time Overlap	t_{DW}	6	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

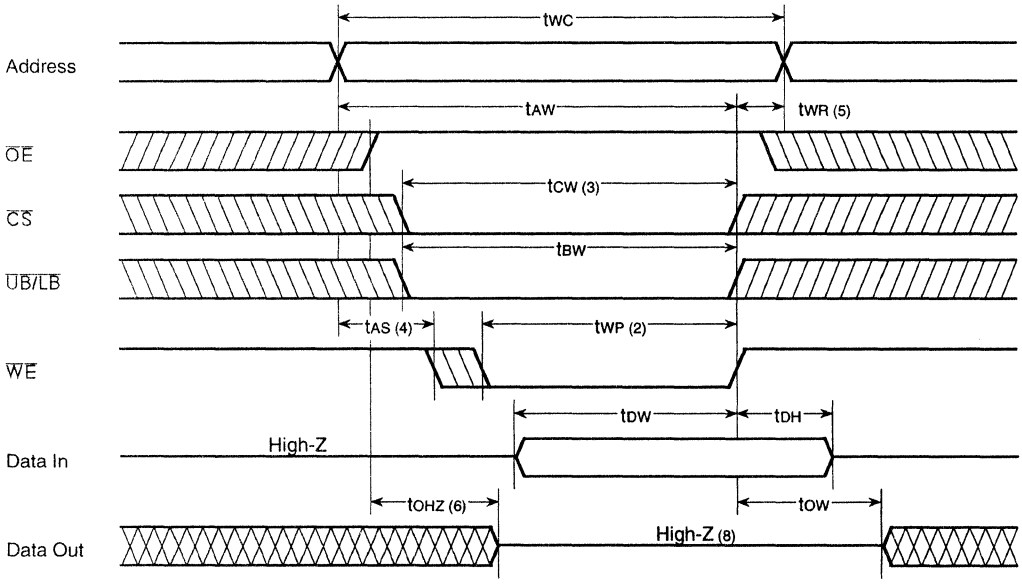
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=V_{IH})



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =V_{IL}
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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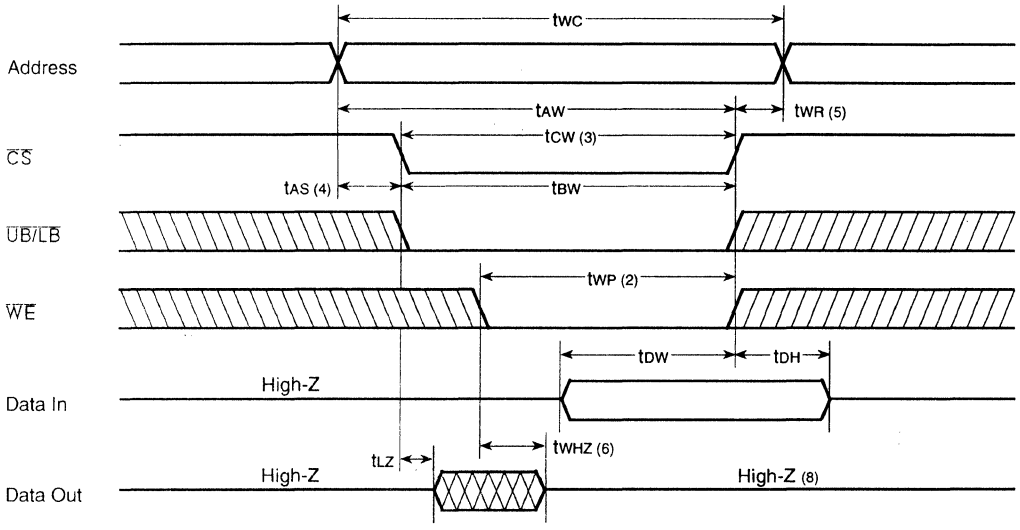
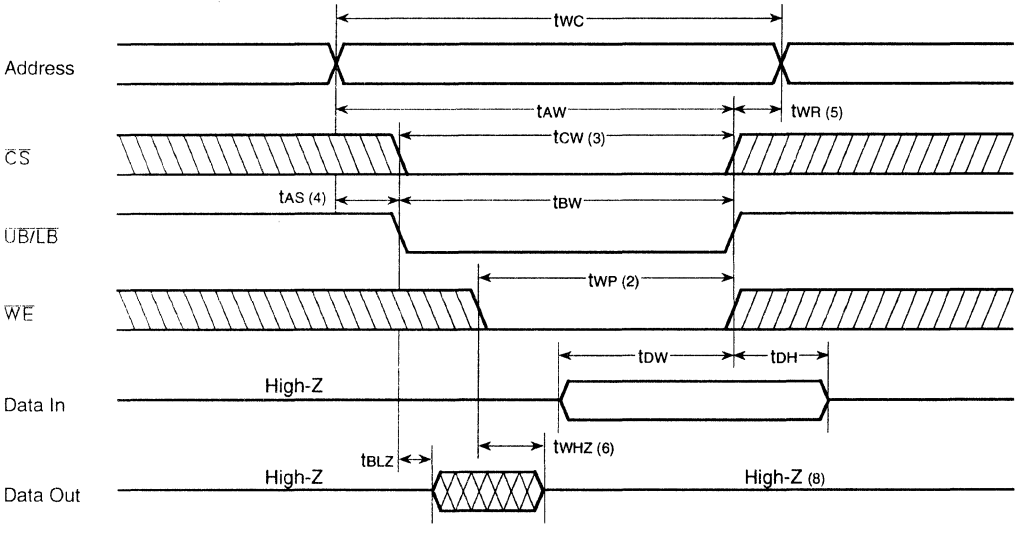
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$/$\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*Note : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,15,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50 mA(Max.)
  - (CMOS) : 10 mA(Max.)
  - Operating KM6164002A-12 : 260 mA(Max.)
  - KM6164002A-15 : 250 mA(Max.)
  - KM6164002A-20 : 240 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Data Byte Control : $\overline{LB}$: I/O_1~I/O_8
  - $\overline{UB}$: I/O_9~I/O_{16}
- Standard Pin Configuration
  - KM6164002AJ : 44-SOJ-400

GENERAL DESCRIPTION

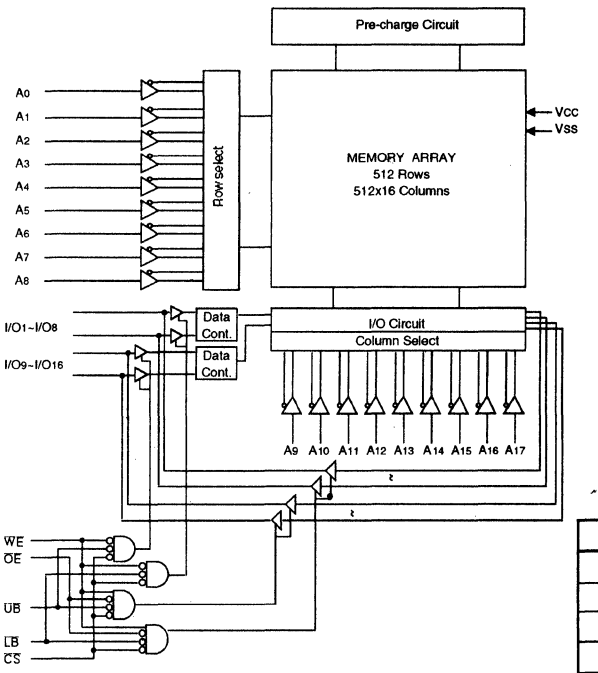
The KM6164002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits.

The KM6164002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{UB}$,$\overline{LB}$).

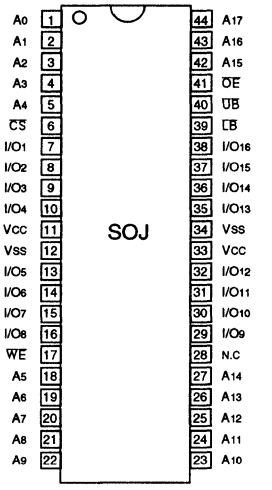
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM6164002A is packaged in a 400 mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O_1~I/O_8)
$\overline{UB}$	Upper-byte Control(I/O_9~I/O_{16})
I/O_1~I/O_{16}	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	260	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	15 ns	-	250	
		V_{IN} = V_{IH} or V_{IL}	20 ns	-	240	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	50	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

CAPACITANCE *(f=1MHz, TA=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT}=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

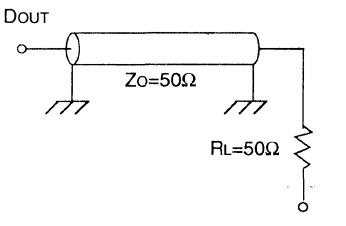
AC CHARACTERISTICS

TEST CONDITIONS

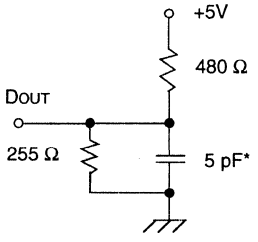
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6164002A-12		KM6164002A-15		KM6164002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	20	ns
Output Enable to Output	t_{OE}	-	6	-	7	-	9	ns
$\overline{LB}$,$\overline{UB}$ Access Time	t_{BA}	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	-	6	-	7	-	9	ns
Output Disable to High-Z Output	t_{OHZ}	-	6	-	7	-	9	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	t_{BHZ}	-	6	-	7	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

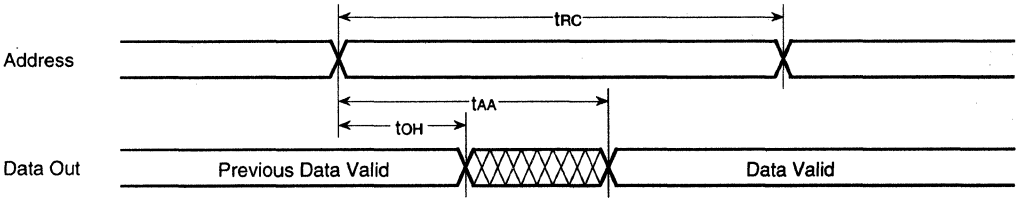
WRITE CYCLE

Parameter	Symbol	KM6164002A-12		KM6164002A-15		KM6164002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	15	-	20	-	ns
Chip Select to End of Write	t_{CW}	8	-	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	10	-	12	-	14	-	ns
$\overline{LB}$,$\overline{UB}$ valid to end of write	t_{BW}	8	-	10	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	-	6	-	7	-	9	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	9	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

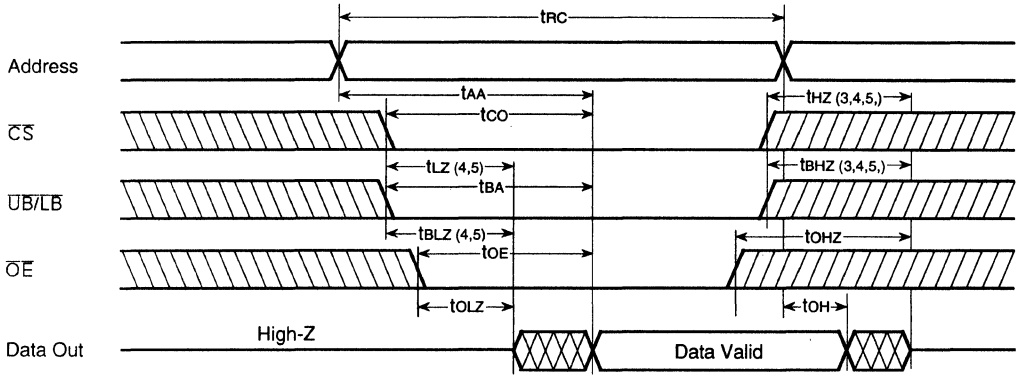
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



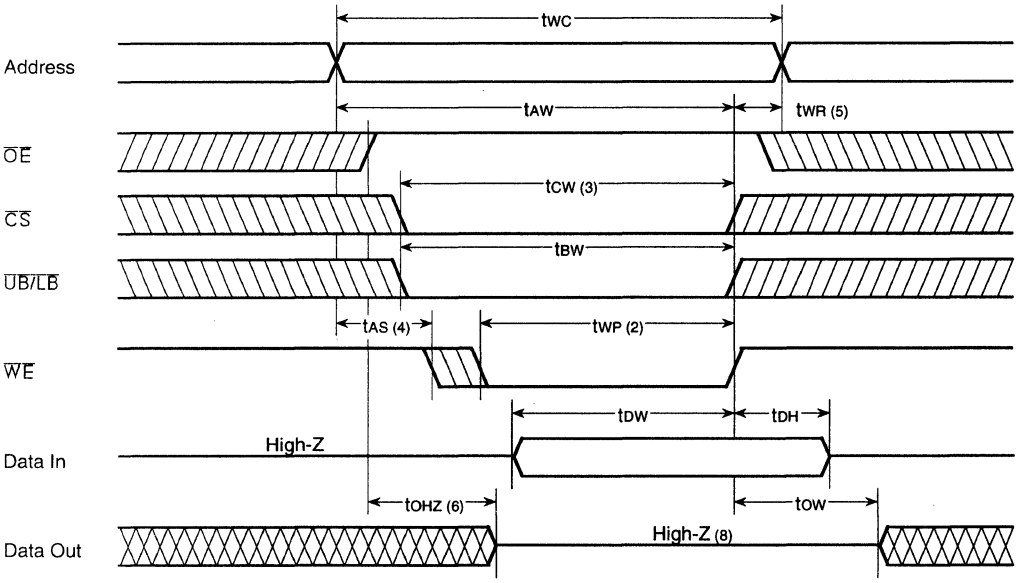
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$=V_{IH})



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =V_{IL}
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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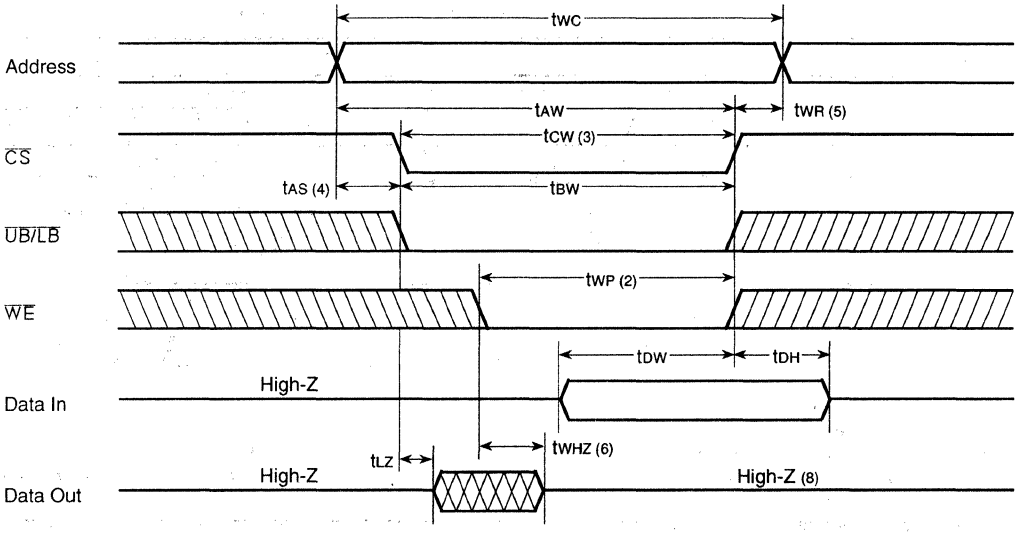
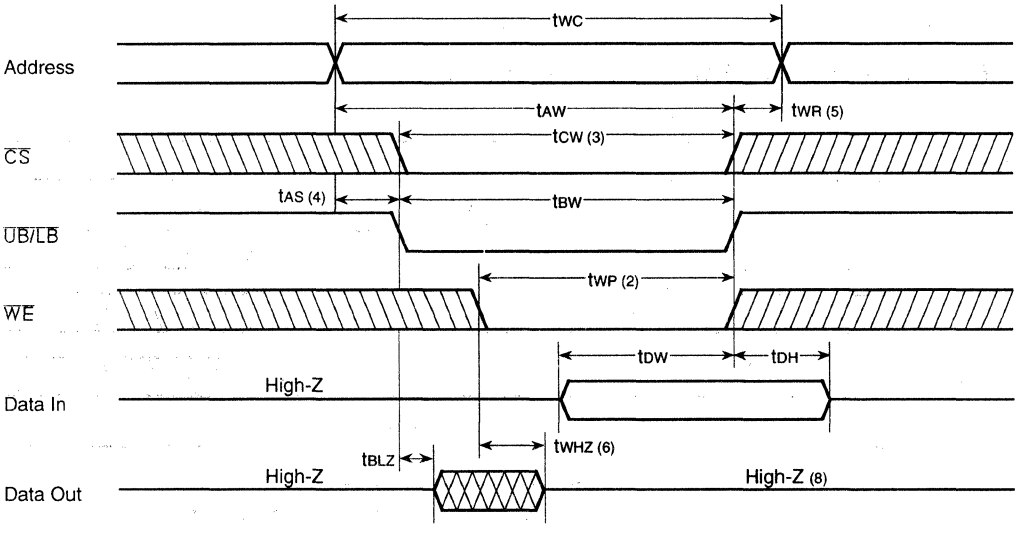
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$/$\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*Note : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 20,25,35 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS):10 mA(Max.)
  - 500μA(Max.) - L-Ver
  - Operating KM6164002/L-20 : 240 mA(Max.)
  - KM6164002/L-25 : 220 mA(Max.)
  - KM6164002/L-35 : 200 mA(Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Devices
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage ; 2V(Min.)- L Ver Only
- Data Byte Control : $\overline{LB}$: I/O1~I/O8
  - $\overline{UB}$: I/O9~I/O16
- Standard Pin Configuration
  - KM6164002J/LJ : 44-SOJ- 400

GENERAL DESCRIPTION

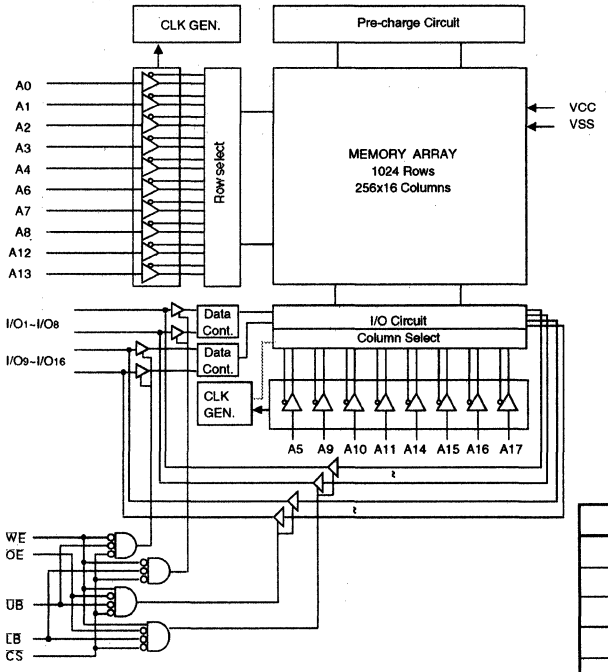
The KM6164002/L is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits.

The KM6164002/L uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{UB}$,$\overline{LB}$).

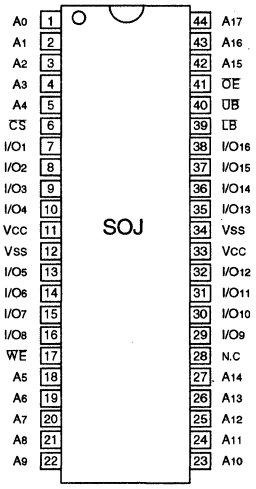
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM6164002/L is packaged in a 400 mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
VCC	Power (+5V)
VSS	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	µA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	20 ns	-	240	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	25 ns	-	220	
		V_{IN} = V_{IH} or V_{IL}	35 ns	-	200	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz	-	-	10	mA
		V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V	L-Ver		500	µA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100µA		-	3.95	V

Note * : Temp. = 25°C, Vcc=5V±5%

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

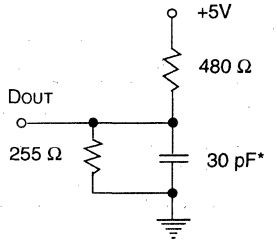
AC CHARACTERISTICS

TEST CONDITIONS

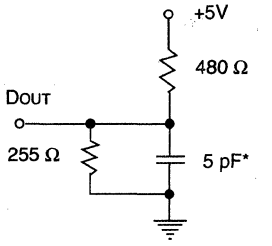
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

PARAMETER	SYMBOL	KM6164002-20 KM6164002L-20		KM6164002-25 KM6164002L-25		KM6164002-35 KM6164002L-35		UNIT
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Select to Output	t_{CO}	-	20	-	25	-	35	ns
Output Enable to Output	t_{OE}	-	10	-	12	-	15	ns
$\overline{LB}$,$\overline{UB}$ Access Time	t_{BA}	-	10	-	12	-	15	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	5	-	5	-	5	-	ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	4	-	5	-	5	-	ns

WRITE CYCLE

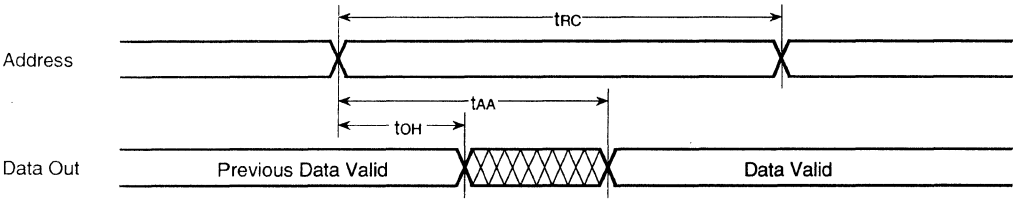
Parameter	Symbol	KM6164002-20 KM6164002L-20		KM6164002-25 KM6164002L-25		KM6164002-35 KM6164002L-35		UNIT
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	20	-	25	-	35	-	ns
Chip Select to End of Write	tCW	15	-	17	-	20	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	15	-	17	-	20	-	ns
Write Pulse Width ($\overline{OE}$ High)	tWP	15	-	17	-	20	-	ns
$\overline{LB}$,$\overline{UB}$ Valid to End of Write	tBW	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	8	ns
Data to Write Time Overlap	tDW	10	-	12	-	15	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

2

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

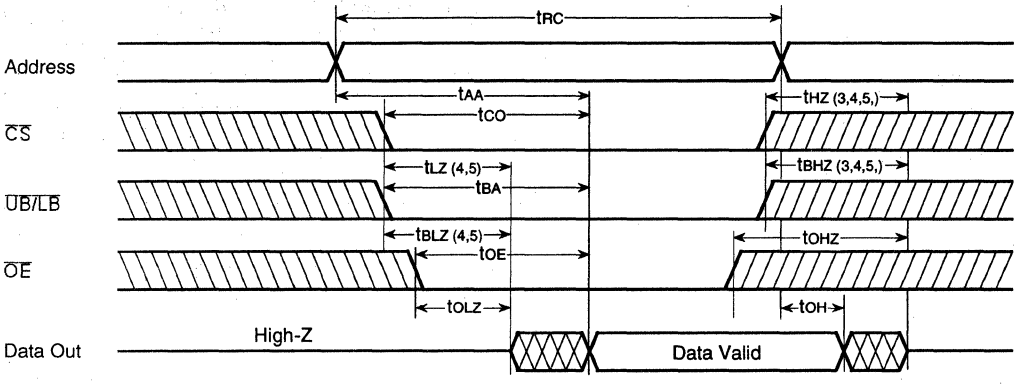
($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS

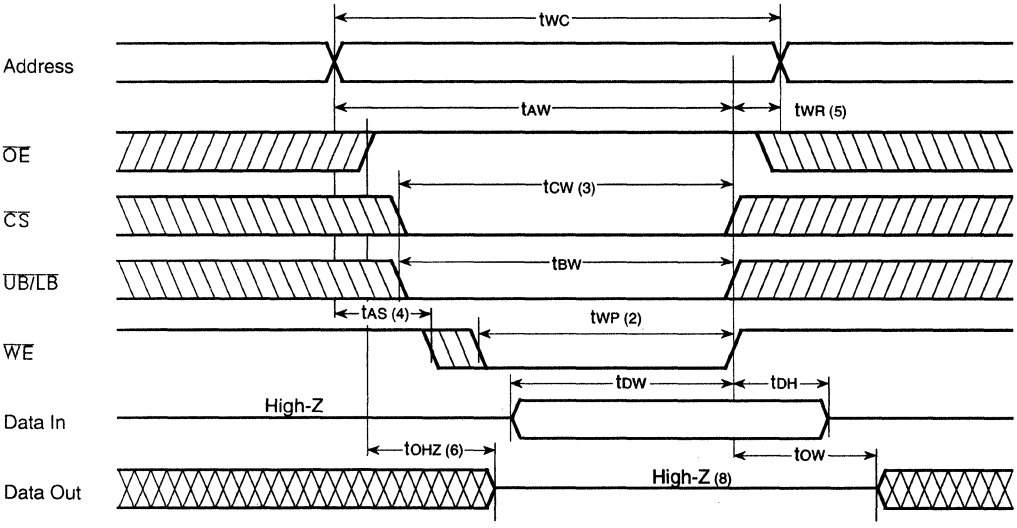
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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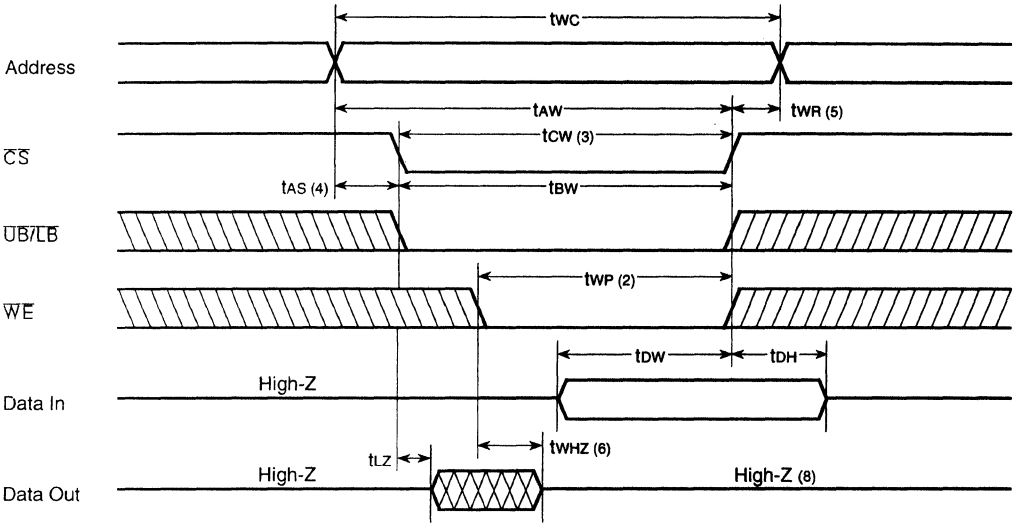
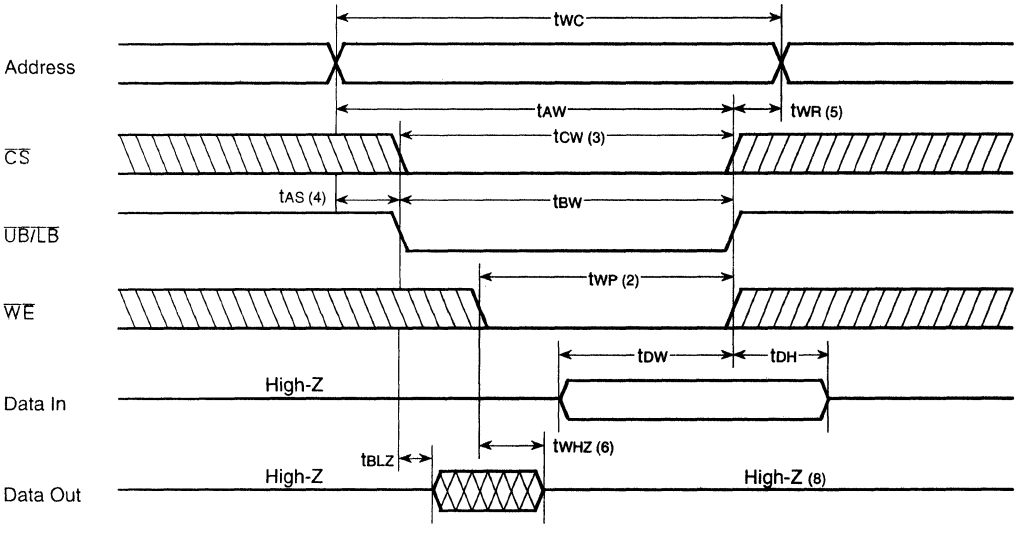
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$/$\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

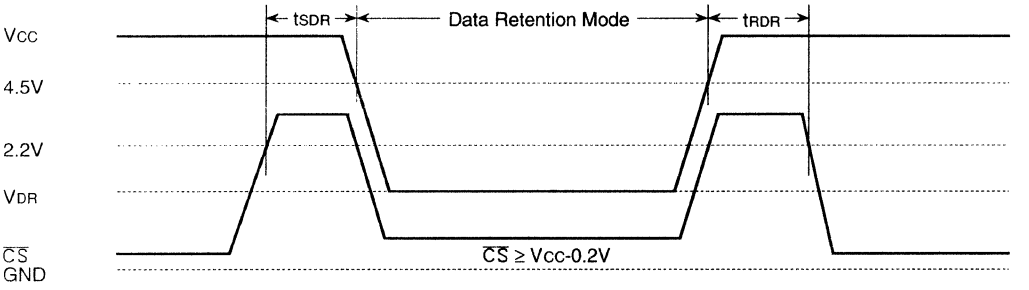
*Note : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A=0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2	5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.0V, $\overline{CS} \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq$0.2V	-	200	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0	-	ns
Recovery Time	t_{RDR}	Wave forms(below)	5	-	ms

* L-Version Only.

DATA RETENTION WAVEFORM 1 ($\overline{CS}$ Controlled)



SAMSUNG ELECTRONICS

High Speed SRAM (3.3V)

- KM68V257	32K × 8	Low Vcc Operation
- KM64V1003A	256K × 4	With OE/ Center Power Low Vcc Operation
- KM68V1002A	128K × 8	Center Power Low Vcc Operation
- KM616V1002A	64K × 16	Center Power Low Vcc Operation
- KM64BV4002	1M × 4	With OE/ BiCMOS Low Vcc Operation
- KM64V4002A	1M × 4	With OE/ Center Power Low Vcc Operation
- KM68BV4002	512K × 8	BiCMOS Low Vcc Operation
- KM68V4002A	512K × 8	Center Power Low Vcc Operation
- KM616BV4002	256K × 16	BiCMOS Low Vcc Operation
- KM616V4002A	256K × 16	Center Power Low Vcc Operation

32Kx8 Bit High Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 15, 17, 20 ns (Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA (Max.)
  - (CMOS) : 100 μA (Max.)
  - Operating KM68V257C-15 : 90 mA (Max.)
  - KM68V257C-17 : 80 mA (Max.)
  - KM68V257C-20 : 70 mA (Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- 2V Minimum Data Retention
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM68V257CP : 28-DIP-300
  - KM68V257CJ : 28-SOJ-300
  - KM68V257CTG : 28-TSOP1-0813.4F

GENERAL DESCRIPTION

The KM68V257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

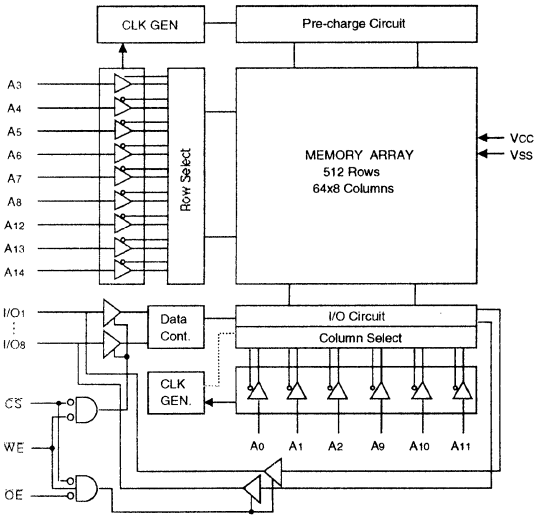
The KM68V257C uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

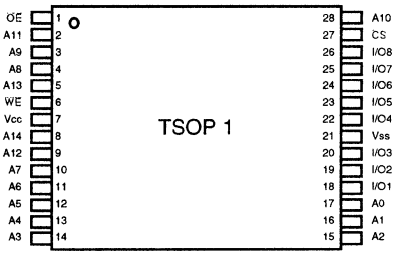
The KM68V257C is designed to operate at 3.3 volts. It is particularly well suited for use in high-density high-speed system applications.

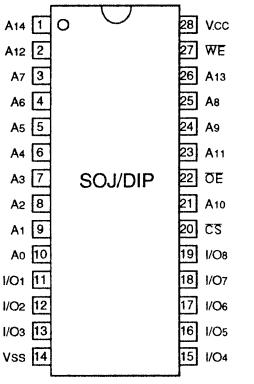
The KM68V257C is packaged in a 300 mil 28-pin plastic DIP/SOJ and TSOP1 forward.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*





Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power(+3.3V)
V_{SS}	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3**	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, Vcc=3.3±0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	Icc	Min. Cycle, 100% Duty	15 ns	-	90	mA
		$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL},	17 ns	-	80	
		I_{OUT}=0 mA	20 ns	-	70	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	100	μA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

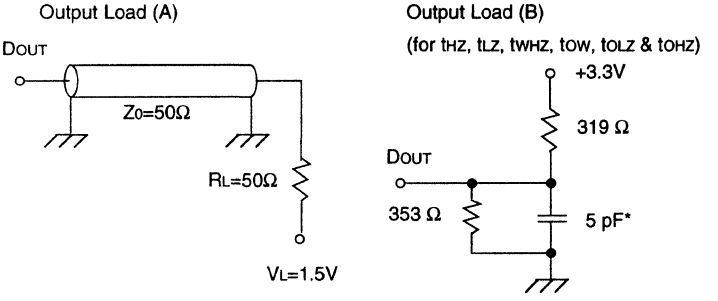
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

(T_A=0 to 70 °C, V_{CC}=3.3±0.3V, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V257C-15		KM68V257C-17		KM68V257C-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	7	-	8	-	10	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Select to Power up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Select to Power Down Time	t_{PD}	-	15	-	17	-	20	ns

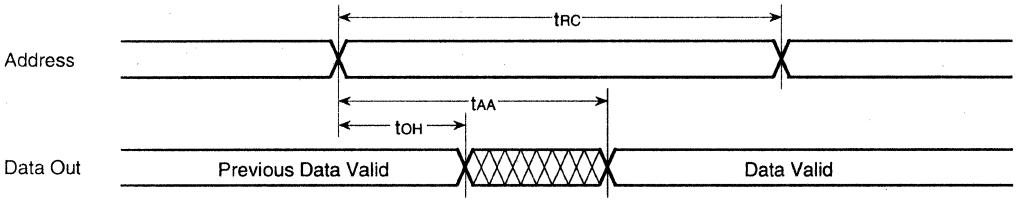
WRITE CYCLE

Parameter	Symbol	KM68V257C-15		KM68V257C-17		KM68V257C-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	11	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	11	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ - High)	tWP	11	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ - Low)	tWP	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	8	ns
Data to Write Time Overlap	tDW	8	-	8	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	0	-	ns

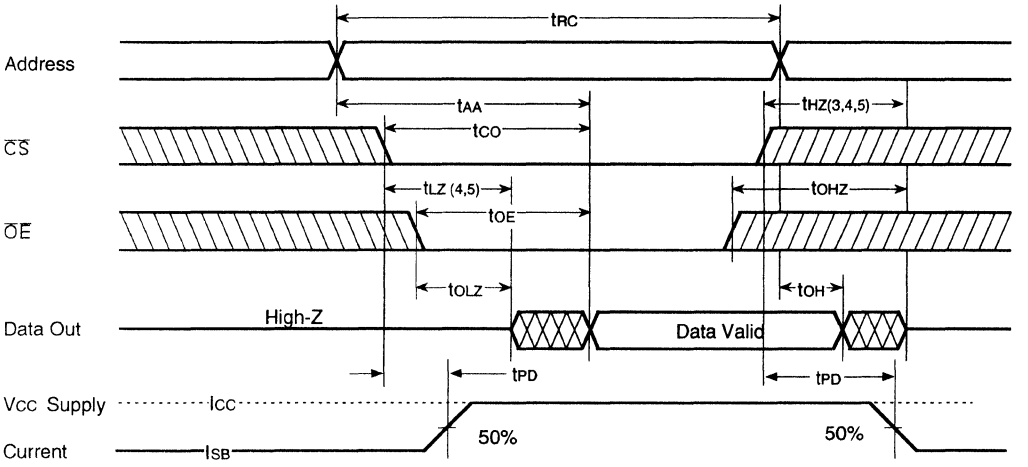
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



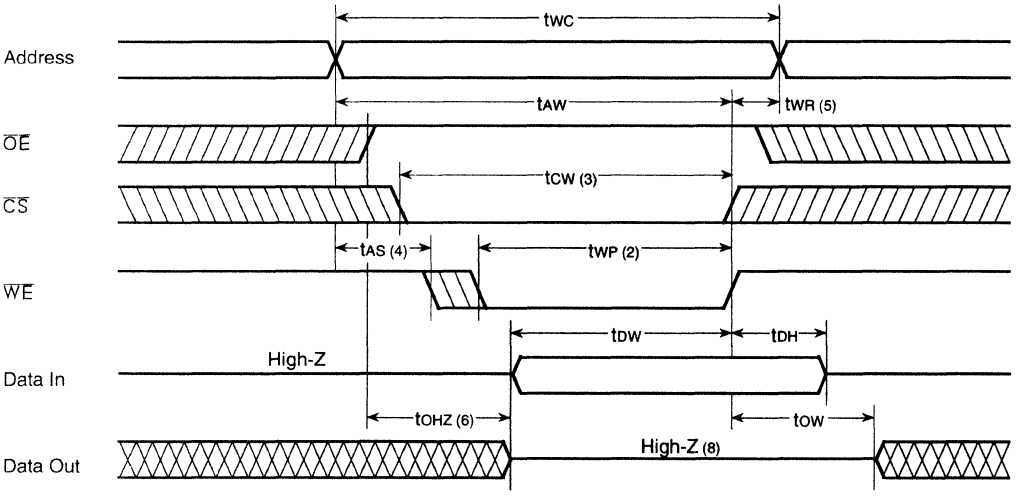
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

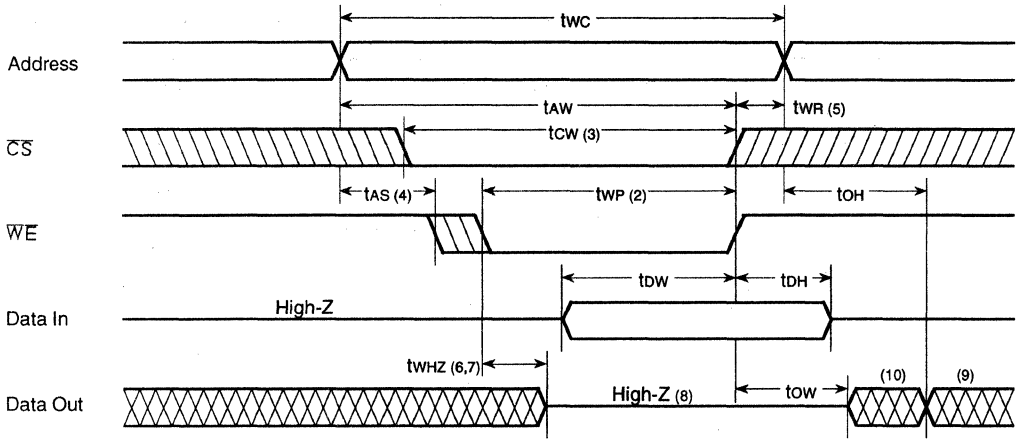
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

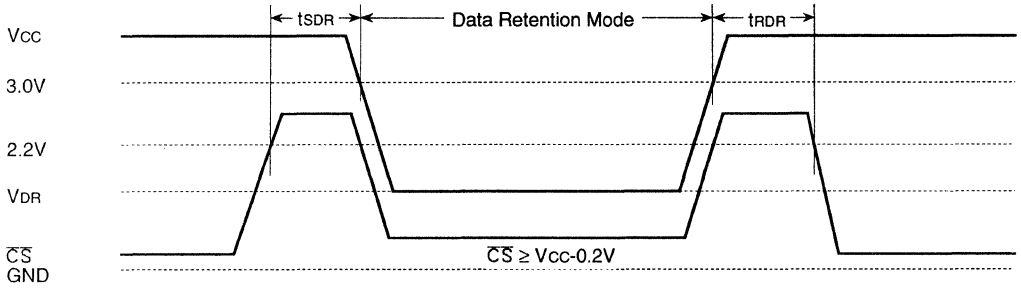
DATA RETENTION CHARACTERISTICS(T_A=0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2	3.6	V
Data Retention Current	I_{DR}	$\overline{CS} \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq$0.2V	-	100	µA
Data Retention Set-up Time	tSDR	See Data Retention	0	-	ns
Recovery Time	t_{RDR}	Wave forms(below)	t_{RC}*	-	ns

* t_{RC}=Read cycle time

2

DATA RETENTION WAVEFORM 1 ($\overline{CS}$ Controlled)



SAMSUNG ELECTRONICS

256K x 4 Bit (With $\overline{OE}$) High-Speed CMOS Static RAM (3.3V Operating)

FEATURES

- Fast Access Time 12,15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM64V1003A-12 : 160 mA(Max.)
  - KM64V1003A-15 : 155 mA(Max.)
  - KM64V1003A-17 : 150 mA(Max.)
  - KM64V1003A-20 : 145 mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64V1003AJ : 32-SOJ-400
  - KM64V1003AT : 32-TSOP2-400F

GENERAL DESCRIPTION

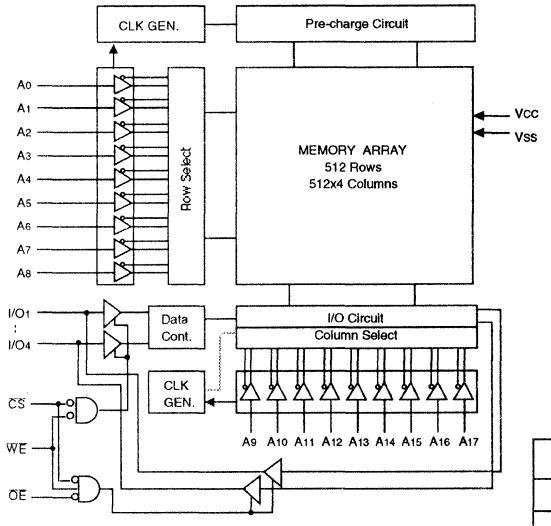
The KM64V1003A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.

The KM64V1003A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

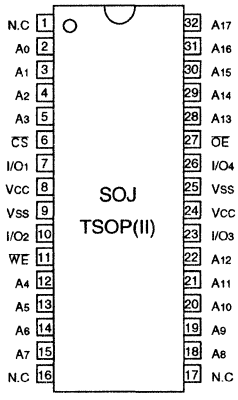
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM64V1003A is packaged in a 400 mil 32-pin plastic SOJ and TSOP(II) forward.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3**	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=3.3±0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty, $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0 mA	12 ns	-	160	mA
			15 ns	-	155	
			17 ns	-	150	
			20 ns	-	145	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz, V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

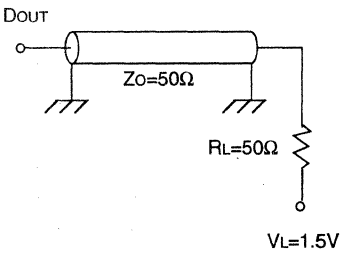
AC CHARACTERISTICS

TEST CONDITIONS

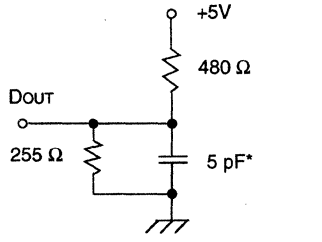
(T_A=0 to 70 °C, V_{CC}=3.3±0.3V, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ)



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64V1003A -12		KM64V1003A -15		KM64V1003A -17		KM64V1003A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	12	-	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	6	-	7	-	8	-	9	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	12	-	15	-	17	-	20	ns

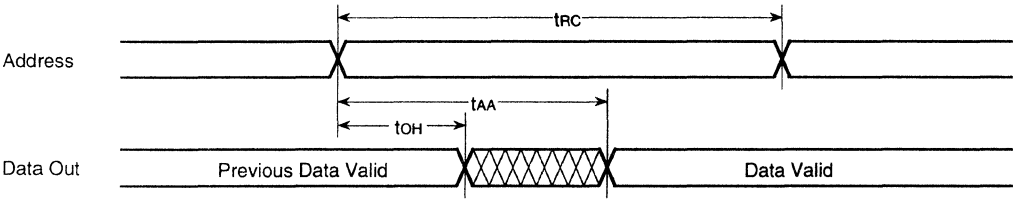
WRITE CYCLE

Parameter	Symbol	KM64V1003A -12		KM64V1003A -15		KM64V1003A -17		KM64V1003A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	t_{CW}	8	-	10	-	11	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	8	-	10	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

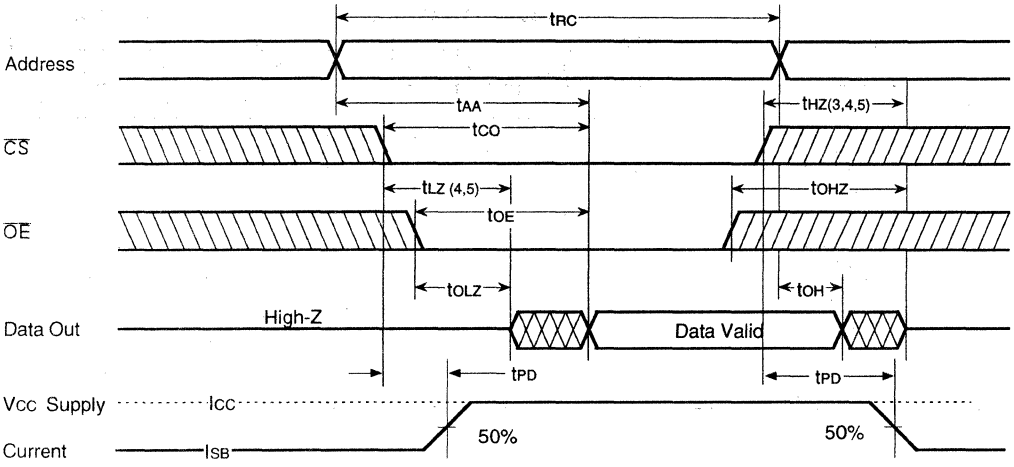
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

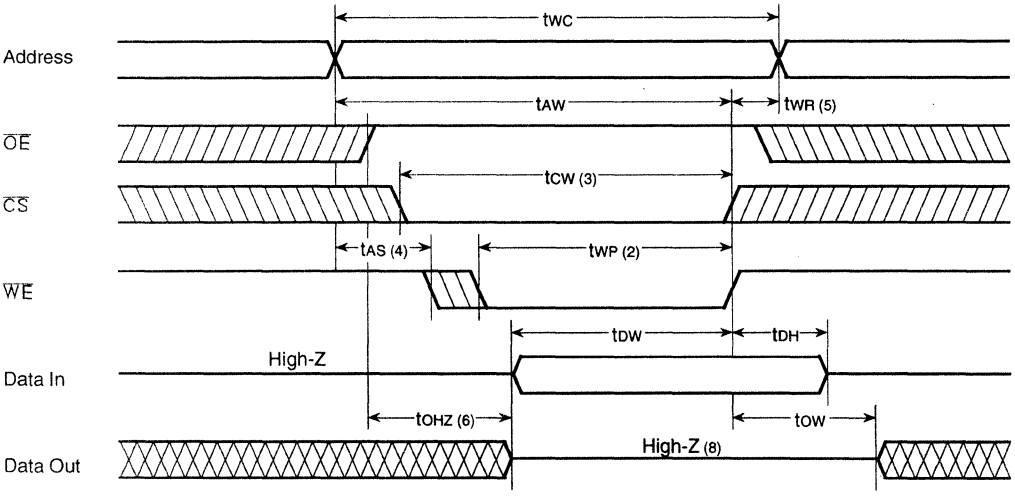
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

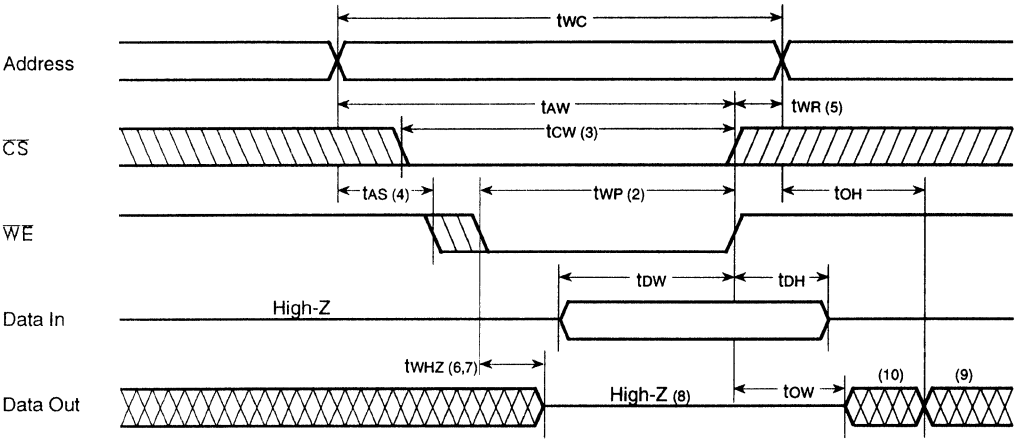
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12,15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM68V1002A-12 : 170 mA (Max.)
  - KM68V1002A-15 : 165 mA (Max.)
  - KM68V1002A-17 : 160 mA (Max.)
  - KM68V1002A-20 : 155 mA (Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68V1002AJ : 32-SOJ-400
  - KM68V1002AT : 32-TSOP2-400F

GENERAL DESCRIPTION

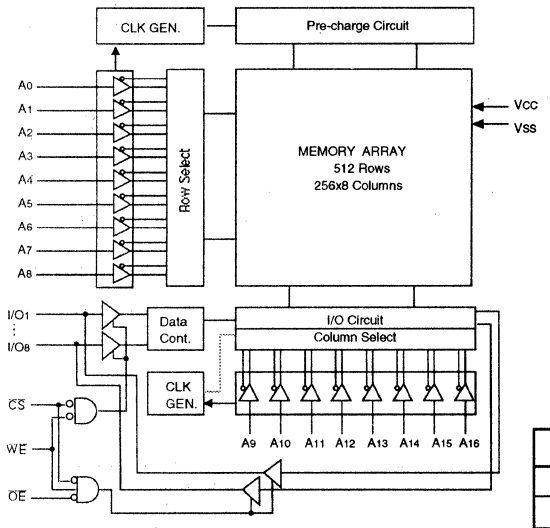
The KM68V1002A is a 1,048,576-bit high-speed static random access memory organized as 131,072 words by 8 bits.

The KM68V1002A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

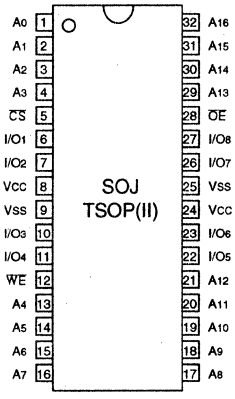
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM68V1002A is packaged in a 400 mil 32-pin plastic SOJ and TSOP(II) forward.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
Vcc	Power (+3.3V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3**	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=3.3±0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	170	mA
		$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL},	15 ns	-	165	
		I_{OUT}=0 mA	17 ns	-	160	
			20 ns	-	155	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

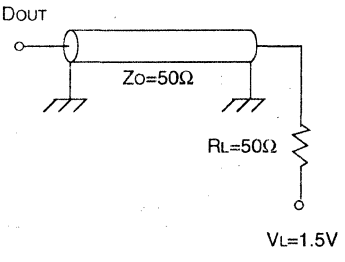
AC CHARACTERISTICS

TEST CONDITIONS

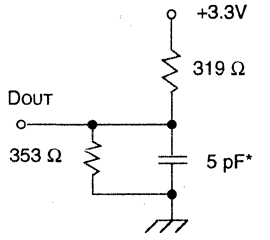
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V1002A -12		KM68V1002A -15		KM68V1002A -17		KM68V1002A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	12	-	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	6	-	7	-	8	-	9	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	12	-	15	-	17	-	20	ns

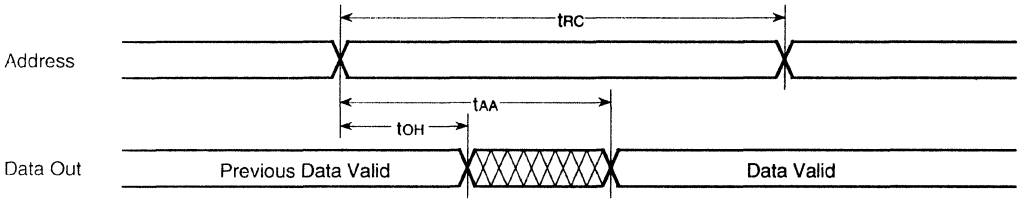
WRITE CYCLE

Parameter	Symbol	KM68V1002A -12		KM68V1002A -15		KM68V1002A -17		KM68V1002A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	t_{CW}	8	-	10	-	11	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	8	-	9	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



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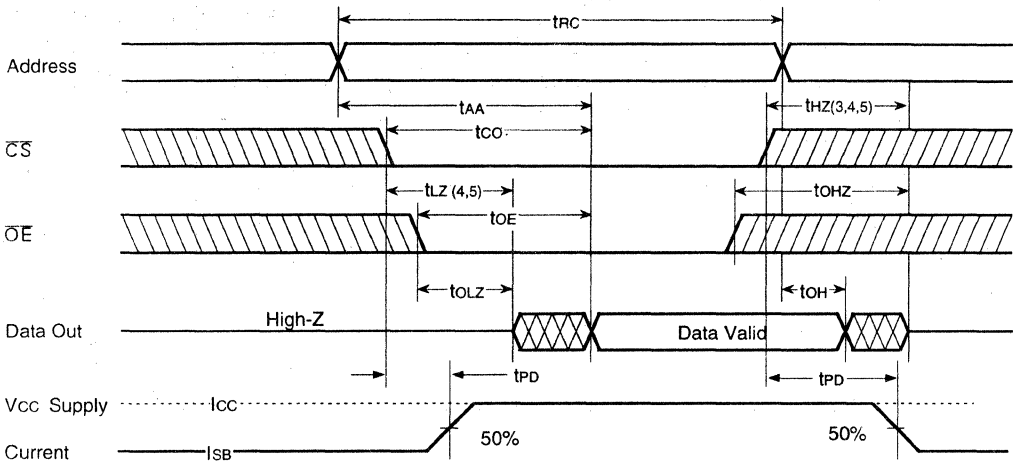
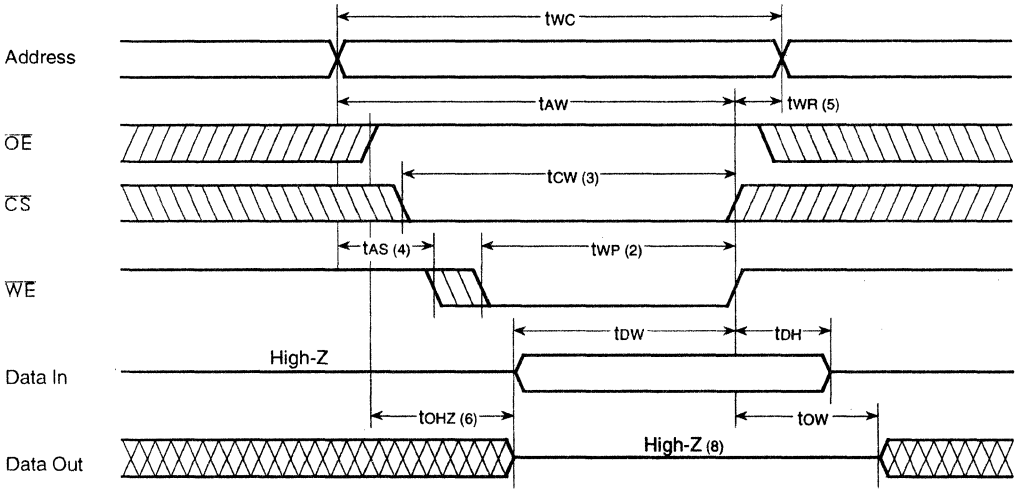
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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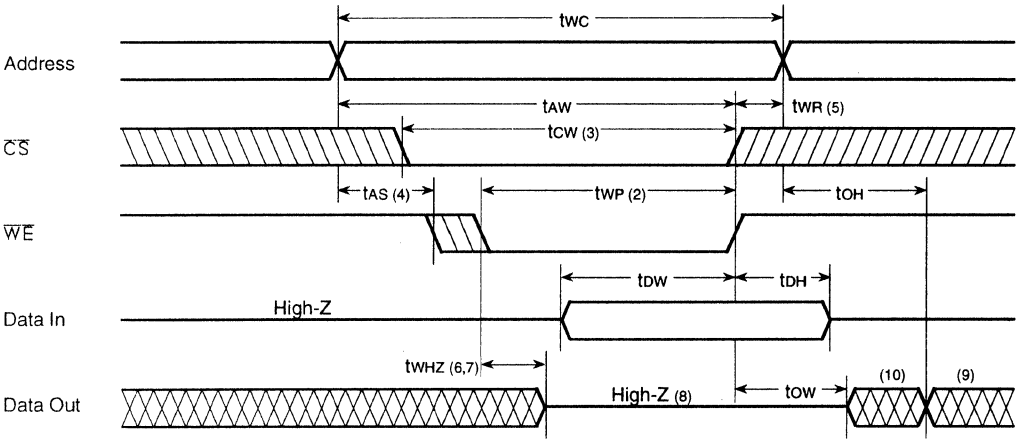
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

64K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12,15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30 mA(Max.)
  - (CMOS): 10 mA(Max.)
  - Operating KM616V1002A-12 : 200 mA(Max.)
  - KM616V1002A-15 : 190 mA(Max.)
  - KM616V1002A-17 : 180 mA(Max.)
  - KM616V1002A-20 : 170 mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Data Byte Control : $\overline{LB}$: I/O1~I/O8
  - $\overline{UB}$: I/O9~I/O16
- Standard Pin Configuration
  - KM616V1002AJ : 44-SOJ-400
  - KM616V1002AT : 44-TSOP2-400F

GENERAL DESCRIPTION

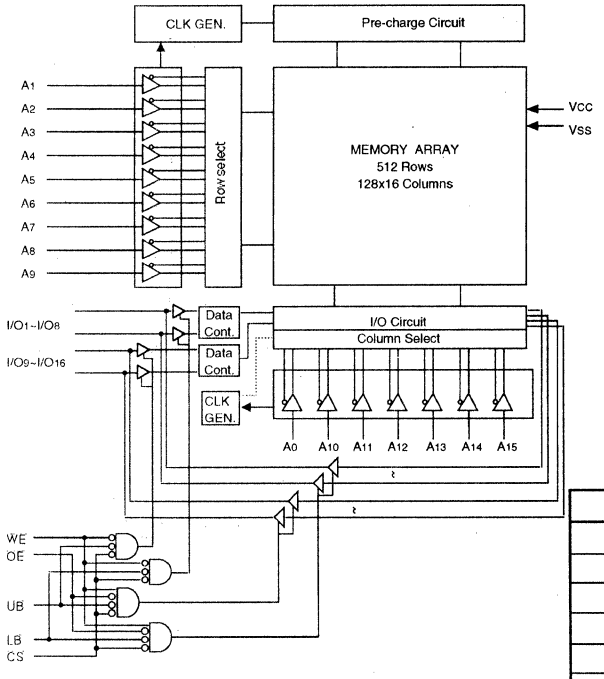
The KM616V1002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits.

The KM616V1002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{UB}$,$\overline{LB}$).

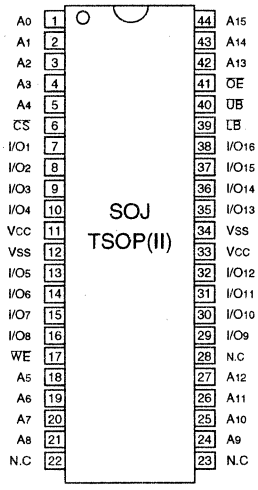
The device is fabricated using Samsung`s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM616V1002A is packaged in a 400 mil 44-pin plastic SOJ and TSOP(II) forward.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3**	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA

** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=3.3±0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	200	mA
		$\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL},	15 ns	-	190	
		I_{OUT}=0 mA	17 ns	-	180	
			20 ns	-	170	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	30	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0 MHz V_{IN} ≥ V_{CC}-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

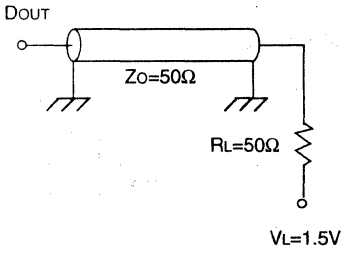
AC CHARACTERISTICS

TEST CONDITIONS

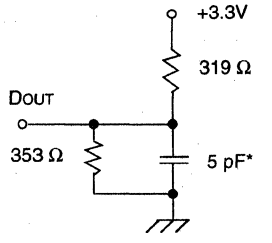
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM616V1002A -12		KM616V1002A -15		KM616V1002A -17		KM616V1002A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	12	-	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	17	-	20	ns
Output Enable to Output	t_{OE}	-	6	-	7	-	8	-	9	ns
$\overline{LB}$,$\overline{UB}$ Access Time	t_{BA}	-	6	-	7	-	8	-	9	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	0	-	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	0	9	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	

WRITE CYCLE

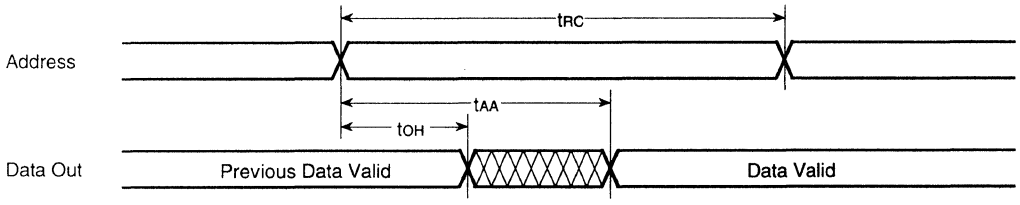
Parameter	Symbol	KM616V1002A -12		KM616V1002A -15		KM616V1002A -17		KM616V1002A -20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
$\overline{LB}$,$\overline{UB}$ Valid to End of Write	tBW	8	-	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

2

TIMING DIAGRAMS

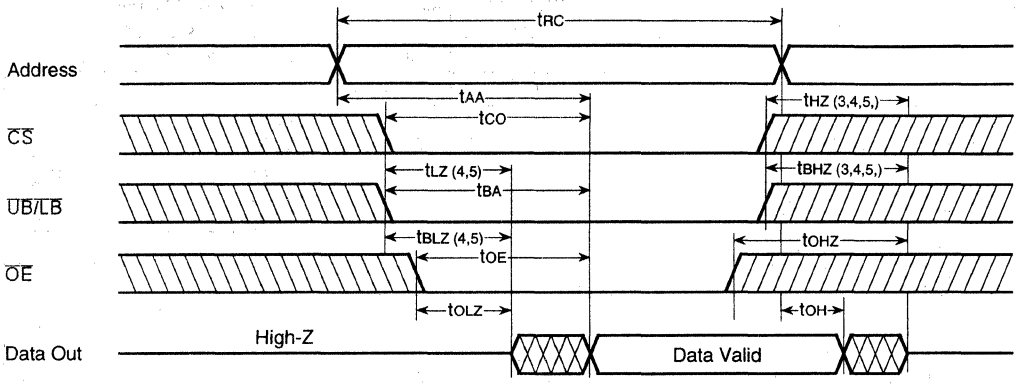
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



TIMING DIAGRAMS

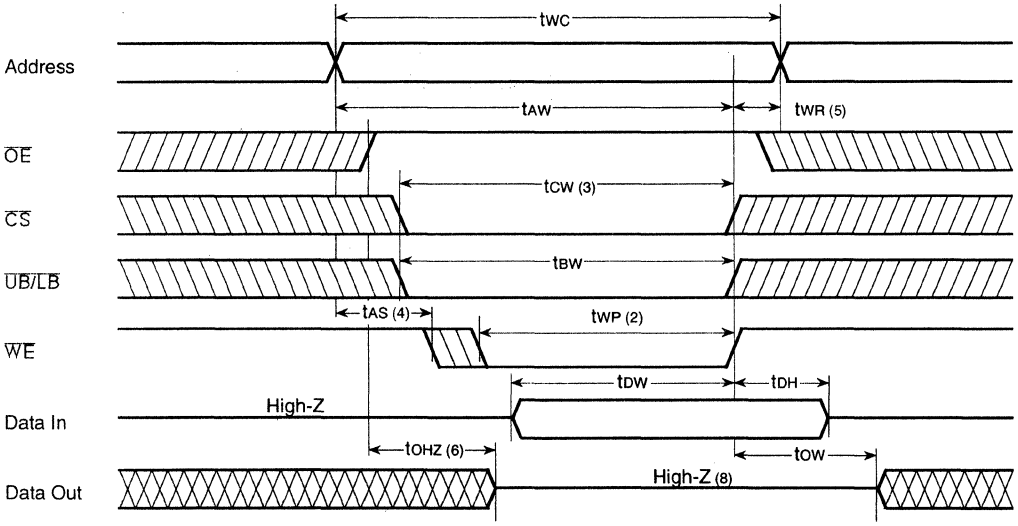
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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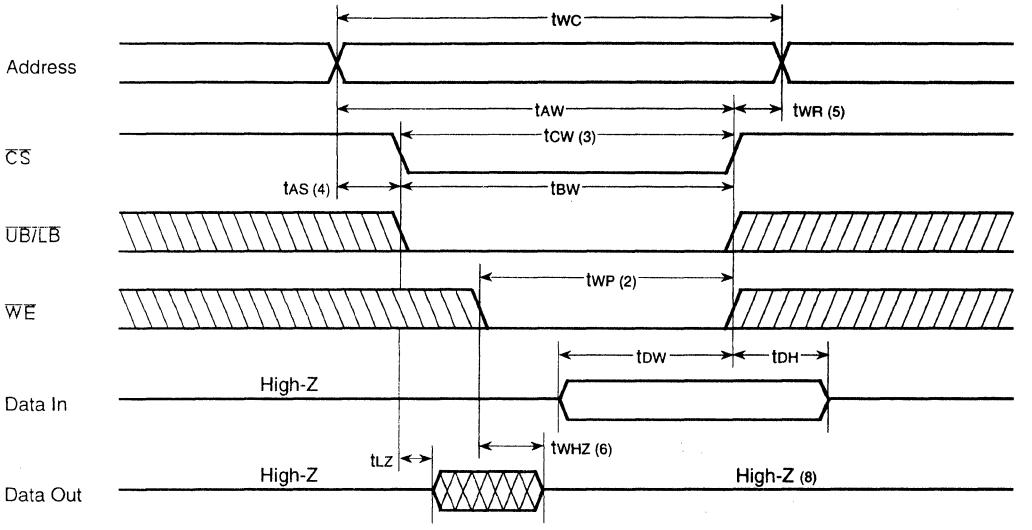
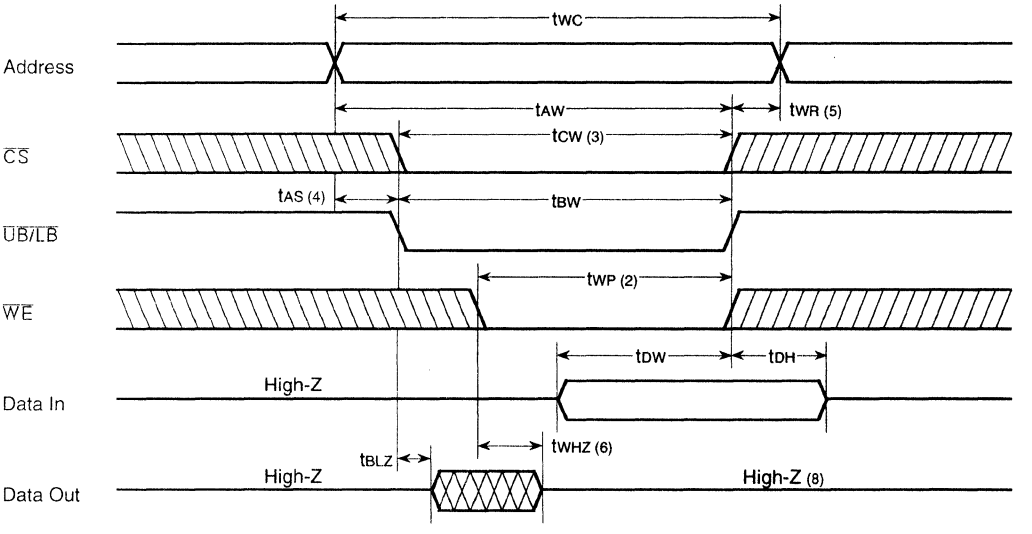
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$/$\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*Note : X means Don't Care.

1M x 4 Bit (With $\overline{OE}$)High-Speed BiCMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12,13,15 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS): 30 mA(Max.)
  - Operating KM64BV4002-12 : 160 mA(Max.)
  - KM64BV4002-13 : 155 mA(Max.)
  - KM64BV4002-15 : 150 mA(Max.)
- Single 3.3V+10% /- 5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM64BV4002J: 32-SOJ-400

GENERAL DESCRIPTION

The KM64BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits.

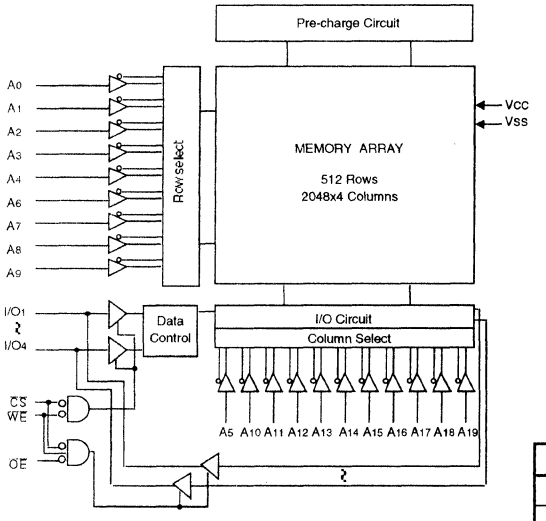
The KM64BV4002 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

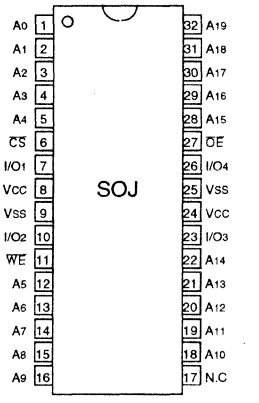
The KM64BV4002 is packaged in a 400 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(TOP VIEW)*



Pin Name	Pin Function
A0-A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs/Outputs
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.60	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3**	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=3.3V+10%/- 5%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-10	10	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	160	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	13 ns	-	155	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15 ns	-	150	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	30	
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

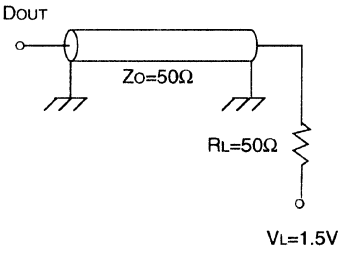
AC CHARACTERISTICS

TEST CONDITIONS

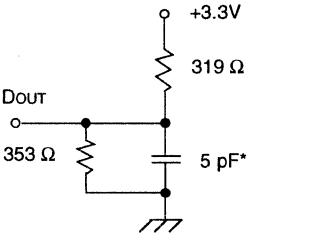
(T_A=0 to 70 °C, V_{CC}=3.3V+10%/- 5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ)



* Including Scope and Jig Capacitance

READ CYCLE

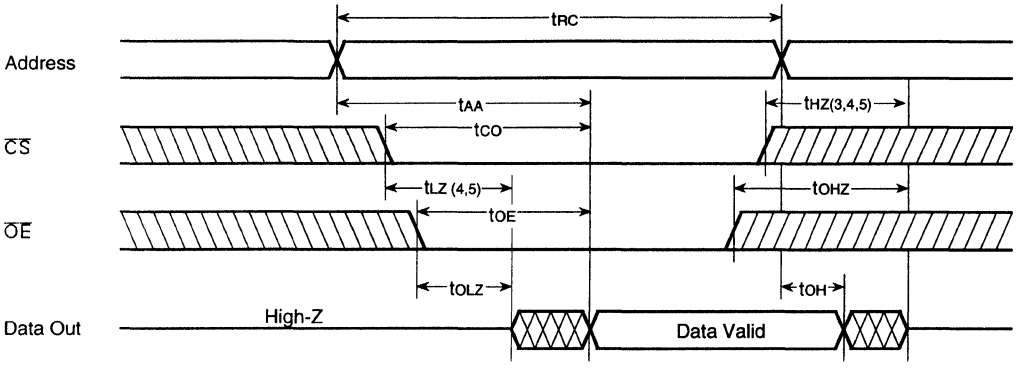
Parameter	Symbol	KM64BV4002-12		KM64BV4002-13		KM64BV4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	-	6	-	6	-	7	ns
Output Disable to High-Z Output	tOHZ	-	6	-	6	-	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64BV4002-12		KM64BV4002-13		KM64BV4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	13	-	15	-	ns
Chip Select to End of Write	t_{CW}	9	-	10	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	10	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	-	6.5	-	7	-	7.5	ns
Data to Write Time Overlap	t_{DW}	7	-	7	-	8	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

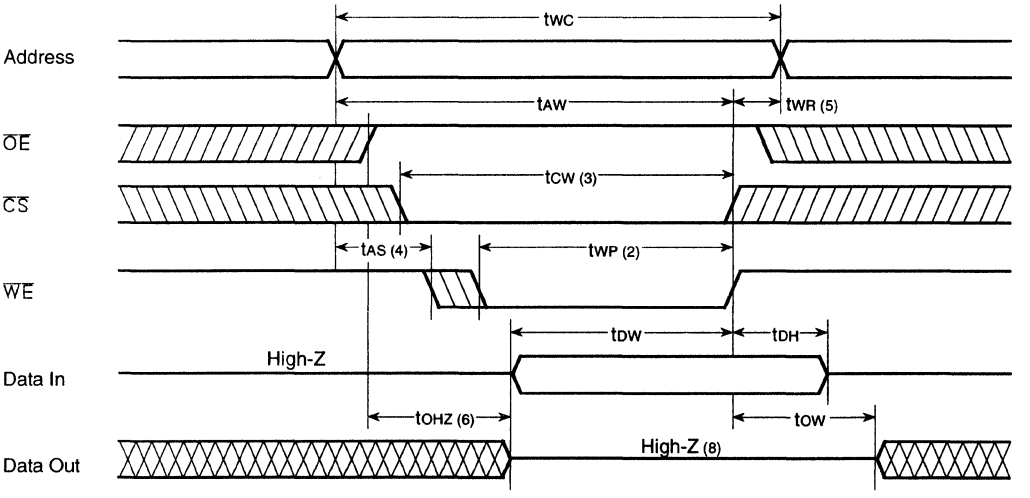
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

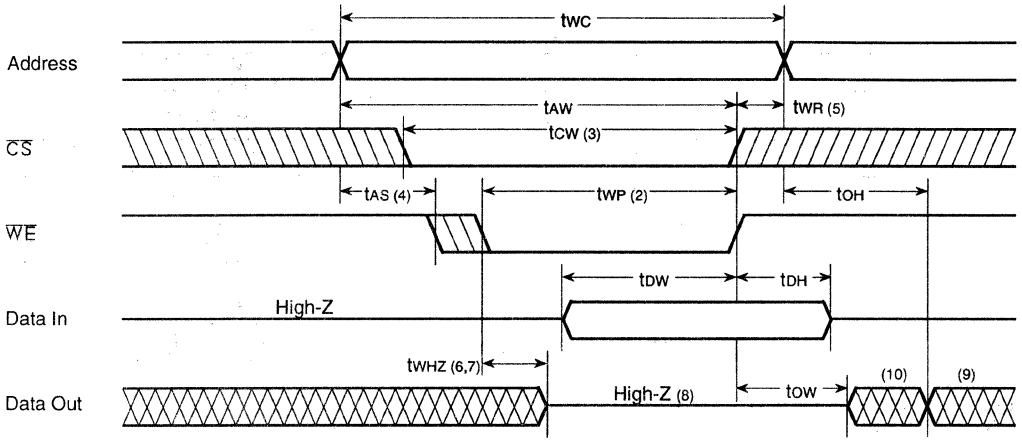
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. twR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

KM64V4002A

CMOS SRAM

1M x 4 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,15,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50 mA(Max.)
    (CMOS): 10 mA(Max.)
  - Operating KM64V4002A-12 : 160 mA(Max.)
    KM64V4002A-15 : 150 mA(Max.)
    KM64V4002A-20 : 140 mA(Max.)
- Single 3.3± 0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM64V4002AJ: 32-SOJ-400

GENERAL DESCRIPTION

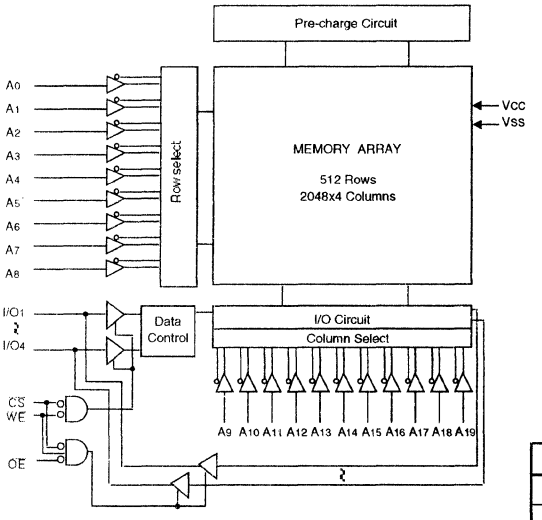
The KM64V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits.

The KM64V4002A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

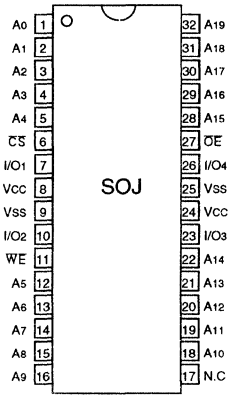
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM64V4002A is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEWS)*



Pin Name	Pin Function
A0-A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs/Output
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connections

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3**	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Max.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=3.3± 0.3V, unless otherwise specified.)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	160	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA,	15 ns	-	150	
		V_{IN} = V_{IH} or V_{IL}	20ns	-	140	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	50	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN}≤0.2V or V_{IN} ≥ Vcc-0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE (f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

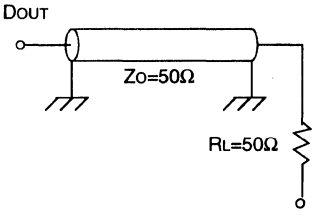
AC CHARACTERISTICS

TEST CONDITIONS

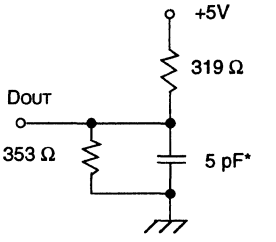
(T_A=0 to 70 °C, V_{CC}=3.3± 0.3V, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tOLZ, tOHZ, tHZ, tLZ, tow & twz)



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64V4002A-12		KM64V4002A-15		KM64V4002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	20	ns
Output Enable to Output	t_{OE}	-	6	-	7	-	9	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	-	6	-	7	-	9	ns
Chip Disable to High-Z Output	t_{HZ}	-	6	-	7	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

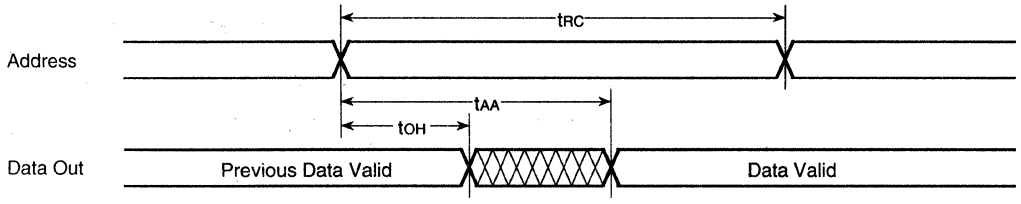
WRITE CYCLE

Parameter	Symbol	KM64V4002A-12		KM64V4002A-15		KM64V4002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP	10	-	12	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	-	6	-	7	-	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

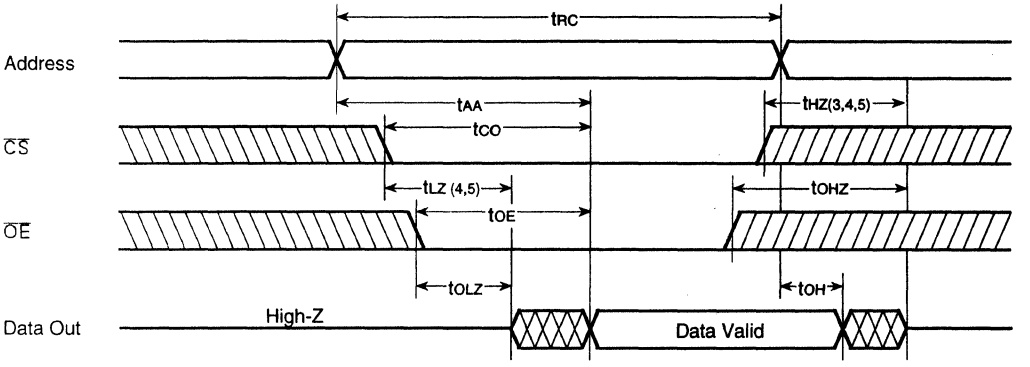
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



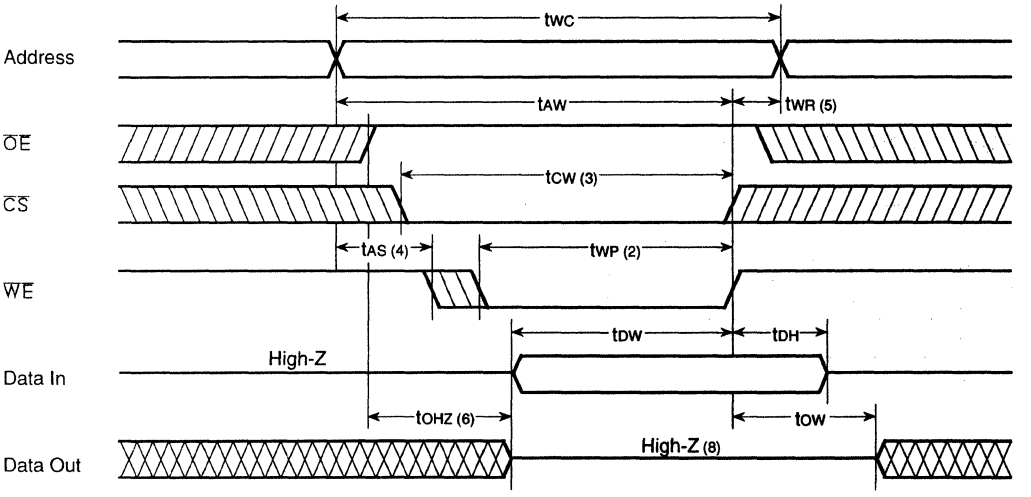
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



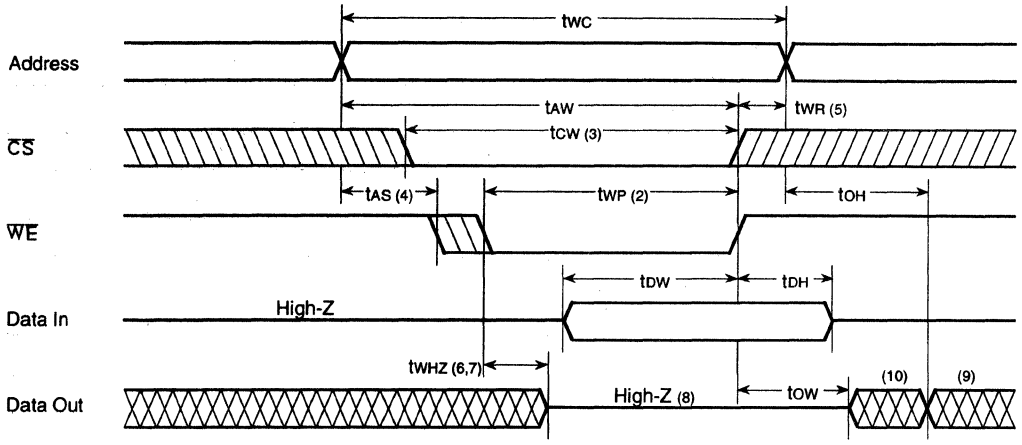
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

512K x 8 Bit High Speed BiCMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12,13,15 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS): 30 mA(Max.)
  - Operating KM68BV4002-12 : 170 mA(Max.)
  - KM68BV4002-13 : 165 mA(Max.)
  - KM68BV4002-15 : 160 mA(Max.)
- Single 3.3V+10%/- 5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM68BV4002J: 36-SOJ-400

GENERAL DESCRIPTION

The KM68BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits.

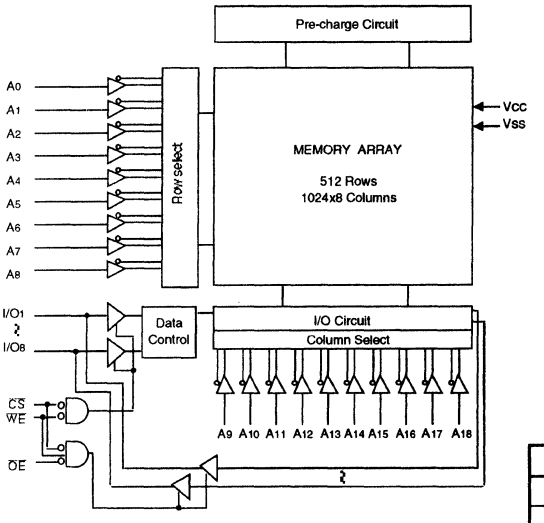
The KM68BV4002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung`s advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

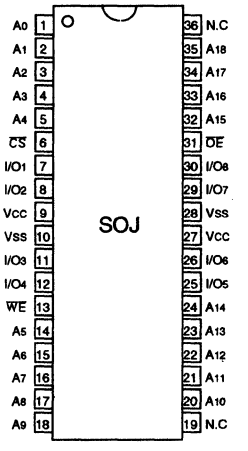
The KM68BV4002 is packaged in a 400 mil 36-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(TOP VIEW)*



Pin Name	Pin Function
A0-A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.60	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3**	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=3.3V+10%/- 5%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-10	10	µA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	170	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	13 ns	-	165	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15 ns	-	160	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	30	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

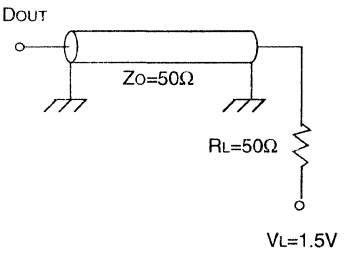
AC CHARACTERISTICS

TEST CONDITIONS

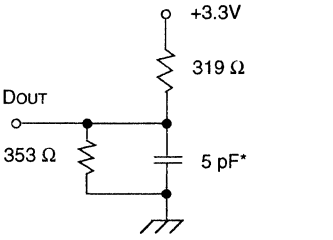
(T_A=0 to 70 °C, V_{CC}=3.3V+10%/- 5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ)



* Including Scope and Jig Capacitance

READ CYCLE

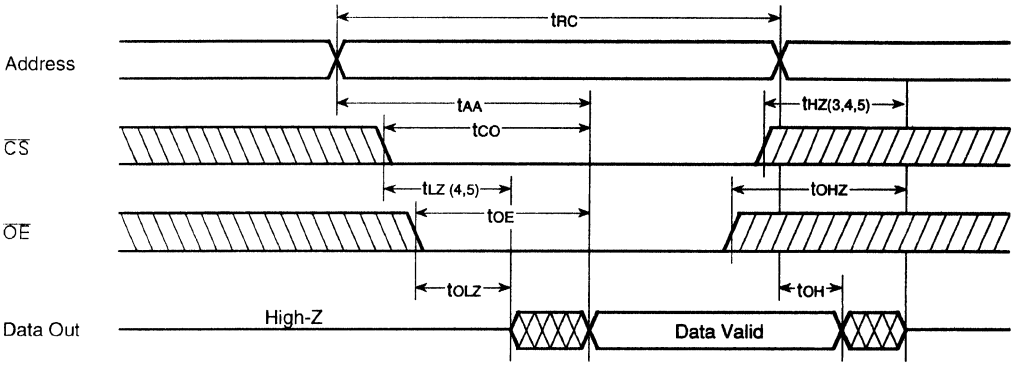
Parameter	Symbol	KM68BV4002-12		KM68BV4002-13		KM68BV4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	-	6	-	6	-	7	ns
Output Disable to High-Z Output	tOHZ	-	6	-	6	-	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68BV4002-12		KM68BV4002-13		KM68BV4002-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	13	-	15	-	ns
Chip Select to End of Write	t_{CW}	9	-	10	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	10	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	-	6.5	-	7	-	7.5	ns
Data to Write Time Overlap	t_{DW}	7	-	7	-	8	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

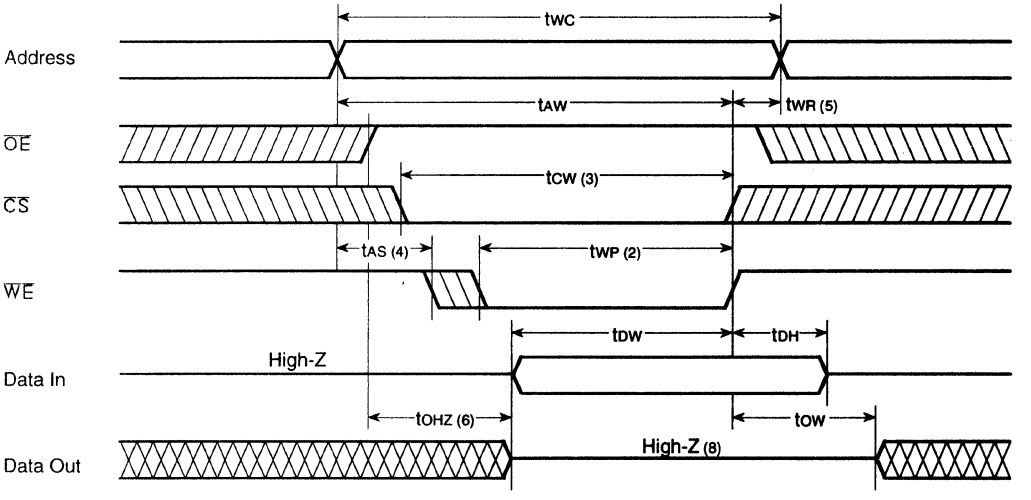
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=V_{IH})



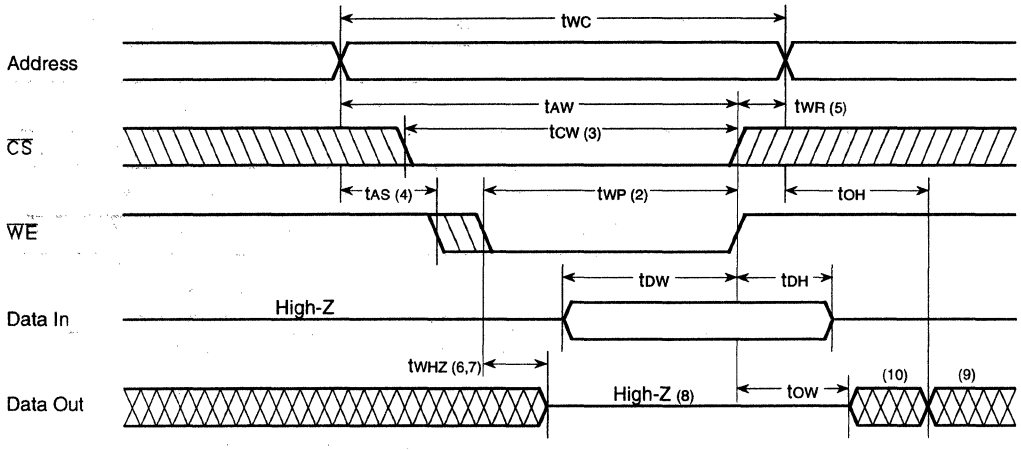
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =V_{IL}
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

512K x 8 Bit High Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,15,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50 mA
    (CMOS): 10 mA
  - Operating KM68V4002A-12 : 180 mA(Max.)
    KM68V4002A-15 : 170 mA(Max.)
    KM68V4002A-20 : 160 mA(Max.)
- Single 3.3± 0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM68V4002AJ: 36-SOJ-400

GENERAL DESCRIPTION

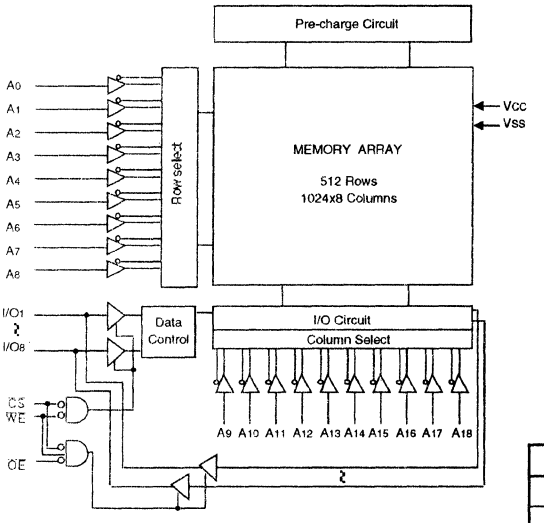
The KM68V4002A is a 4,194,304-bit high-speed Static Random Access Memory organization as 524,288 words by 8 bits.

The KM68V4002A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

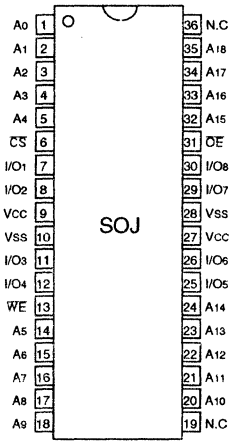
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM68V4002A is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=3.3± 0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} V_{OUT}=Vss to Vcc		-2	2	µA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	180	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA,	15 ns	-	170	
		V_{IN} = V_{IH} or V_{IL}	20 ns	-	160	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	50	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN}≤0.2V or V_{IN} ≥ Vcc-0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

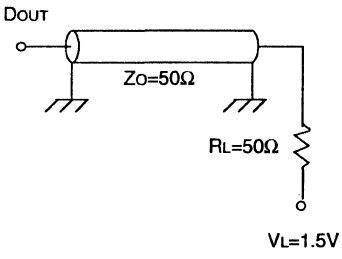
AC CHARACTERISTICS

TEST CONDITIONS

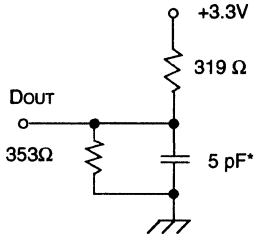
(T_A=0 to 70 °C, V_{CC}=3.3± 0.3V, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tOLZ, tOHZ, tHZ, tOW, tLZ & tWZ)



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V4002A-12		KM68V4002A-15		KM68V4002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	20	ns
Output Enable to Output	t_{OE}	-	6	-	7	-	9	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	-	6	-	7	-	9	ns
Chip Disable to High-Z Output	t_{HZ}	-	6	-	7	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

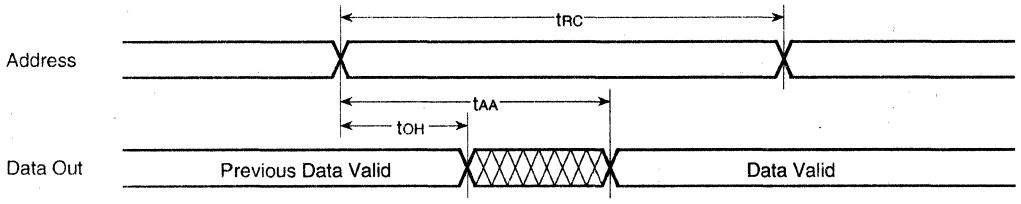
WRITE CYCLE

Parameter	Symbol	KM68V4002A-12		KM68V4002A-15		KM68V4002A-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	12	-	ns
Write Pulse Width(OE High)	tWP	8	-	10	-	12	-	ns
Write Pulse Width(OE Low)	tWP	10	-	12	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	-	6	-	7	-	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

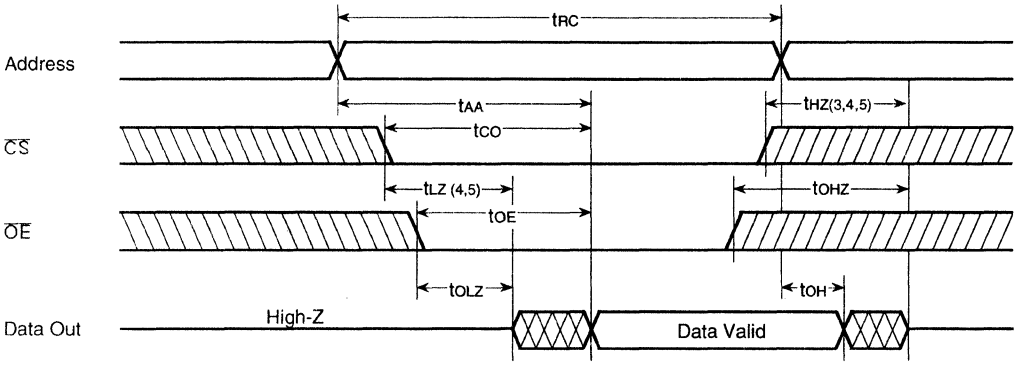
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



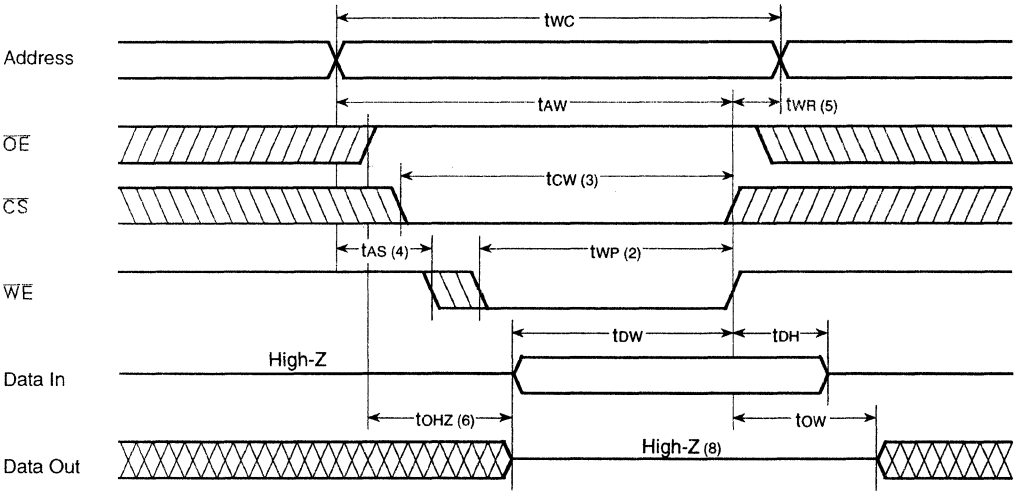
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



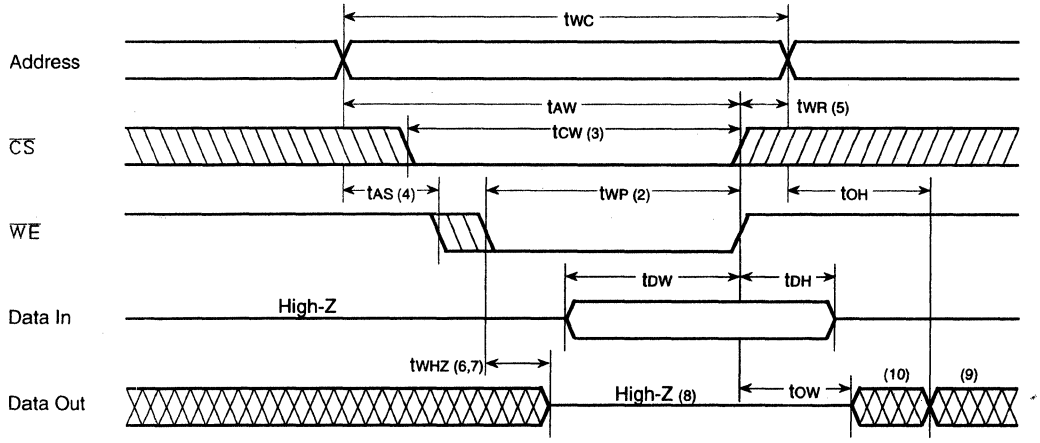
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

256K x 16 Bit High-Speed BiCMOS Static RAM (3.3V Operating)

FEATURES

- Fast Access Time 12,13,15 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS):30 mA(Max.)
  - Operating KM616BV4002-12 : 240 mA(Max.)
  - KM616BV4002-13 : 235 mA(Max.)
  - KM616BV4002-15 : 230 mA(Max.)
- Single 3.3V +10%/- 5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Data Byte Control : $\overline{LB}$: I/O1~I/O8
  - $\overline{UB}$: I/O9~I/O16
- Standard Pin Configuration
  - KM616BV4002J :44-SOJ-400

GENERAL DESCRIPTION

The KM616BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits.

The KM616BV4002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{UB}$,$\overline{LB}$).

The device is fabricated using Samsung`s advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM616BV4002 is packaged in a 400 mil 44-pin plastic SOJ.

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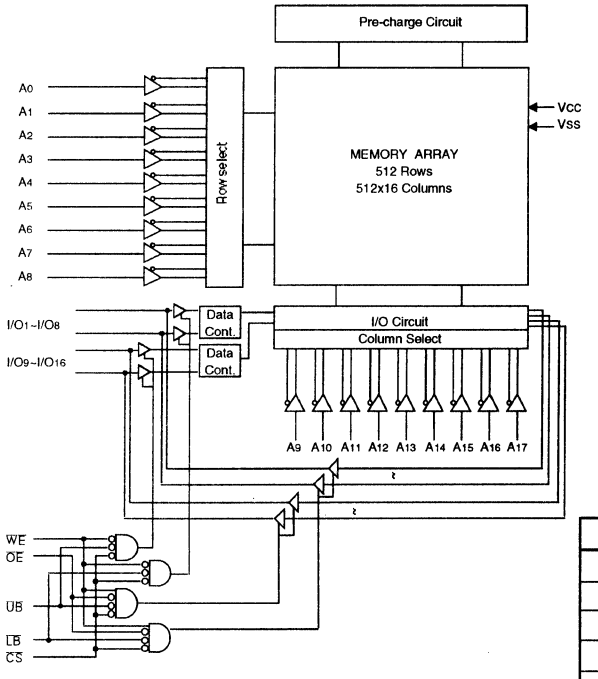
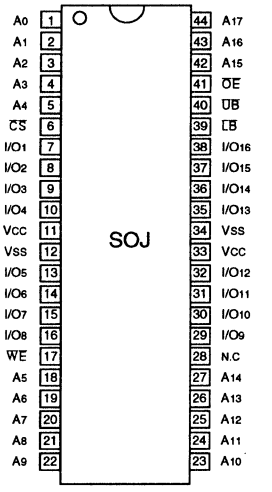
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.60	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= V_{CC}+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=3.3V+10%/- 5%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-10	10	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	240	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	13 ns	-	235	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15 ns	-	230	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	30	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

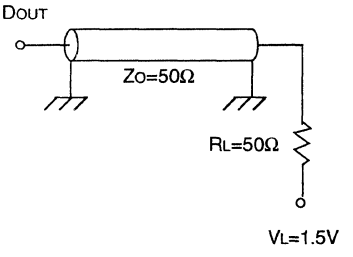
AC CHARACTERISTICS

TEST CONDITIONS

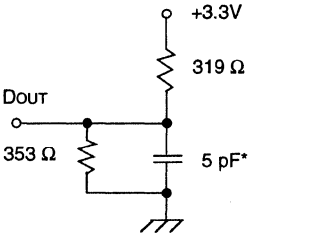
(T_A=0 to 70 °C, V_{CC}=3.3V+10%/- 5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ)



* Including Scope and Jig Capacitance

READ CYCLE

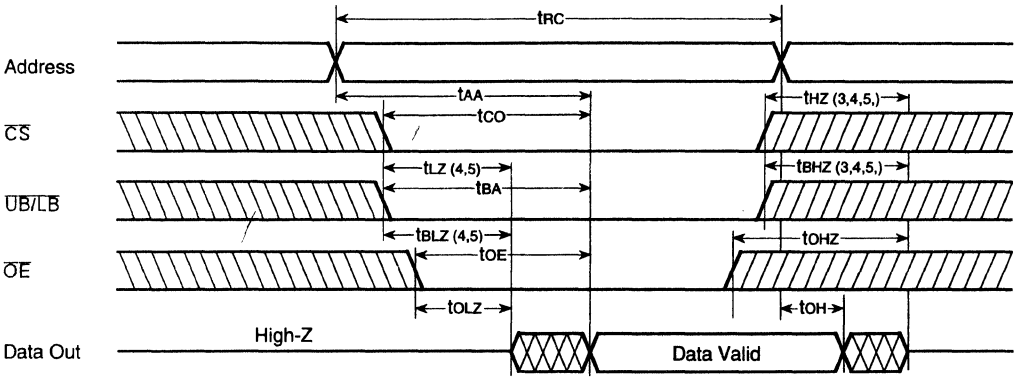
Parameter	Symbol	KM616BV4002-12		KM616BV4002-13		KM616BV4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Output	tOE	-	6	-	6	-	7	ns
$\overline{LB}$,$\overline{UB}$ Access Time	tBA	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	-	6	-	6	-	7	ns
Output Disable to High-Z Output	tOHZ	-	6	-	6	-	7	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	tBHZ	-	6	-	6	-	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM616BV4002-12		KM616BV4002-13		KM616BV4002- 15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	13	-	15	-	ns
Chip Select to End of Write	t_{CW}	9	-	10	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	10	-	11	-	12	-	ns
$\overline{LB}$,$\overline{UB}$ valid to end of write	t_{BW}	9	-	10	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	-	6.5	-	7	-	7.5	ns
Data to Write Time Overlap	t_{DW}	7	-	7	-	8	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	

TIMING DIAGRAMS

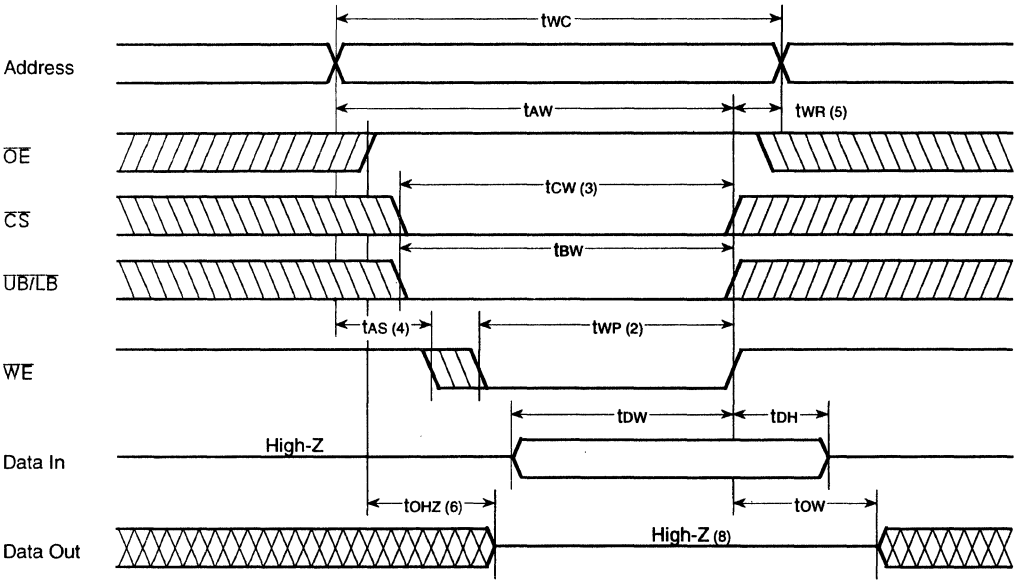
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

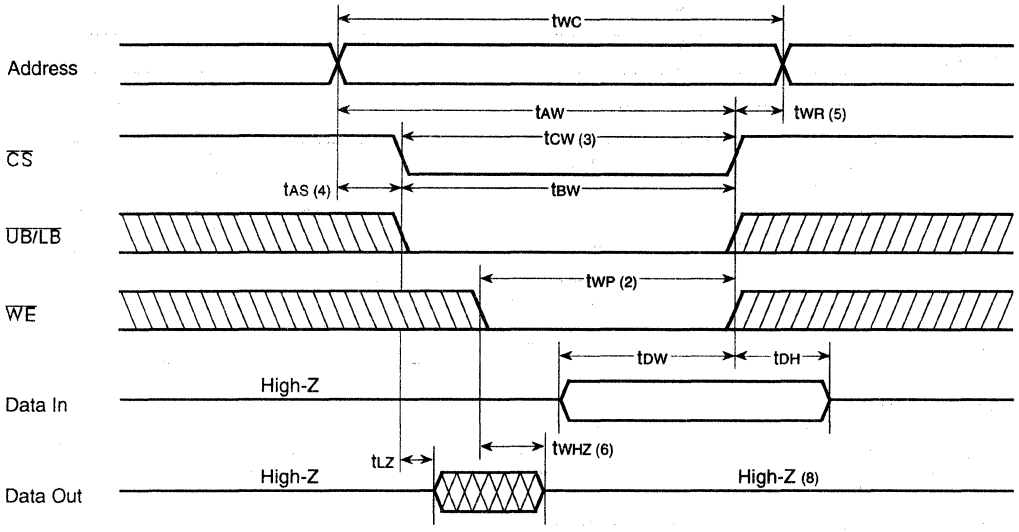
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)

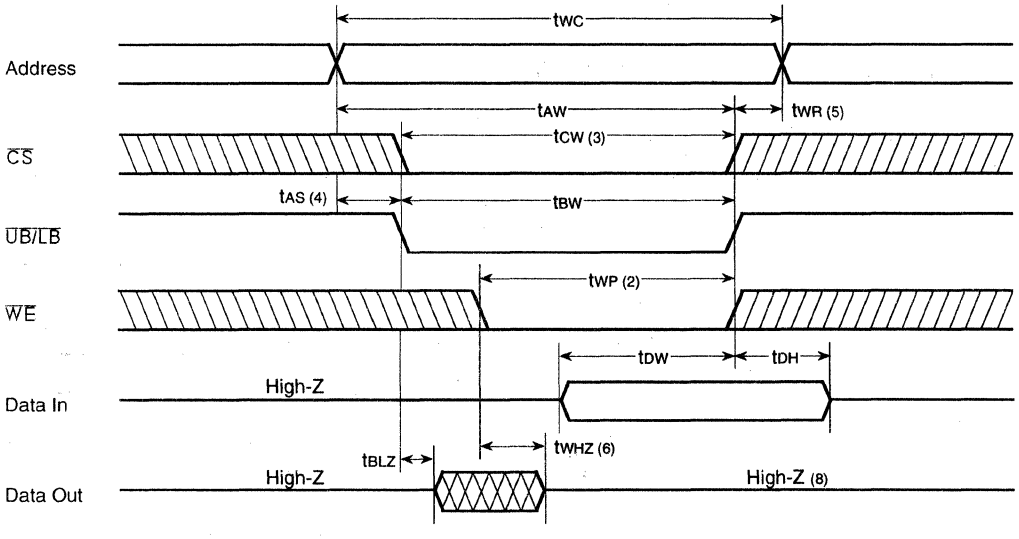


SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$/$\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

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FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*Note : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,15,20 ns (Max.)
- Low Power Dissipation
  - Standby (TTL) : 50 mA (Max.)
  - (CMOS) : 10 mA (Max.)
  - Operating KM616V4002A -12 : 240 mA (Max.)
  - KM616V4002A -15 : 230 mA (Max.)
  - KM616V4002A -20 : 220 mA (Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Data Byte Control : $\overline{LB}$: I/O1~I/O8
  - $\overline{UB}$: I/O9~I/O16
- Standard Pin Configuration
  - KM616V4002AJ : 44-SOJ-400

GENERAL DESCRIPTION

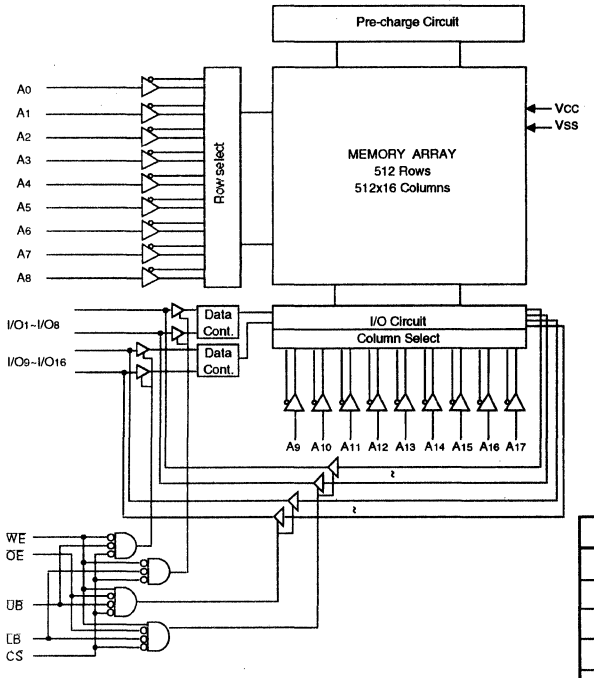
The KM616V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits.

The KM616V4002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$,$\overline{LB}$).

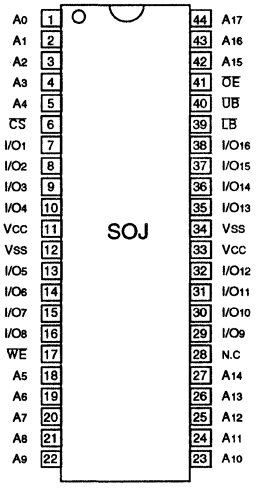
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM616V4002A is packaged in a 400 mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control (I/O1~I/O8)
$\overline{UB}$	Upper-byte Control (I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min.)= -2.0V ac (Pulse Width≤10 ns) for I≤20 mA
** V_{IH}(Min.)= Vcc+2.0V ac (Pulse Width≤10 ns) for I≤20 mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, Vcc=3.3±0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	μA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty	12 ns	-	240	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0 mA,	15 ns	-	230	
		V_{IN} = V_{IH} or V_{IL}	20 ns	-	220	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	50	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V

CAPACITANCE *(f=1MHz, TA=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT}=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

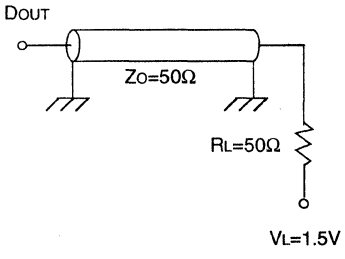
AC CHARACTERISTICS

TEST CONDITIONS

(T_A=0 to 70 °C, V_{CC}=3.3±0.3V, unless otherwise specified)

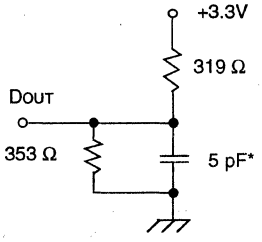
Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)

(for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ)



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM616V4002A -12		KM616V4002A -15		KM616V4002A -20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	20	ns
Output Enable to Output	tOE	-	6	-	7	-	9	ns
$\overline{LB}$,$\overline{UB}$ Access Time	tBA	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	-	6	-	7	-	9	ns
Output Disable to High-Z Output	tOHZ	-	6	-	7	-	9	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	tBHZ	-	6	-	7	-	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

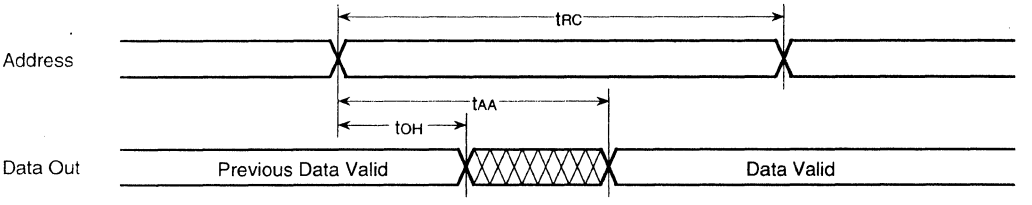
WRITE CYCLE

Parameter	Symbol	KM616V4002A -12		KM616V4002A-15		KM616V4002A -20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	12	-	15	-	20	-	ns
Chip Select to End of Write	t_{CW}	8	-	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	10	-	12	-	14	-	ns
$\overline{LB}$,$\overline{UB}$ valid to end of write	t_{BW}	8	-	10	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	-	6	-	7	-	9	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	9	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

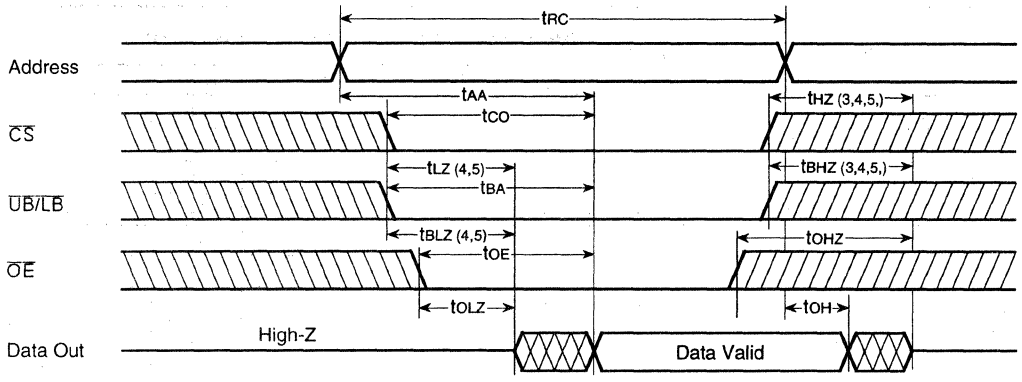
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



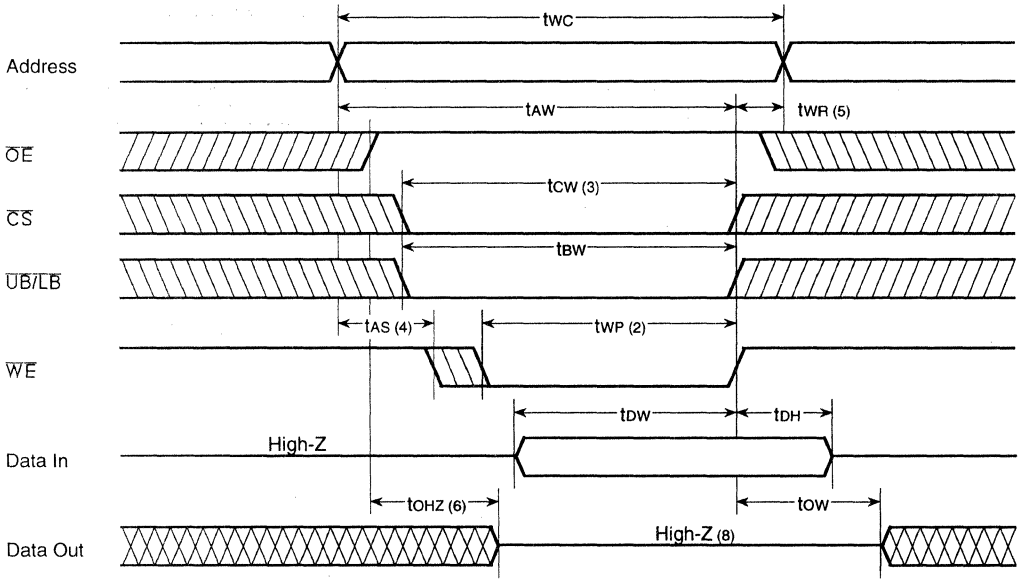
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



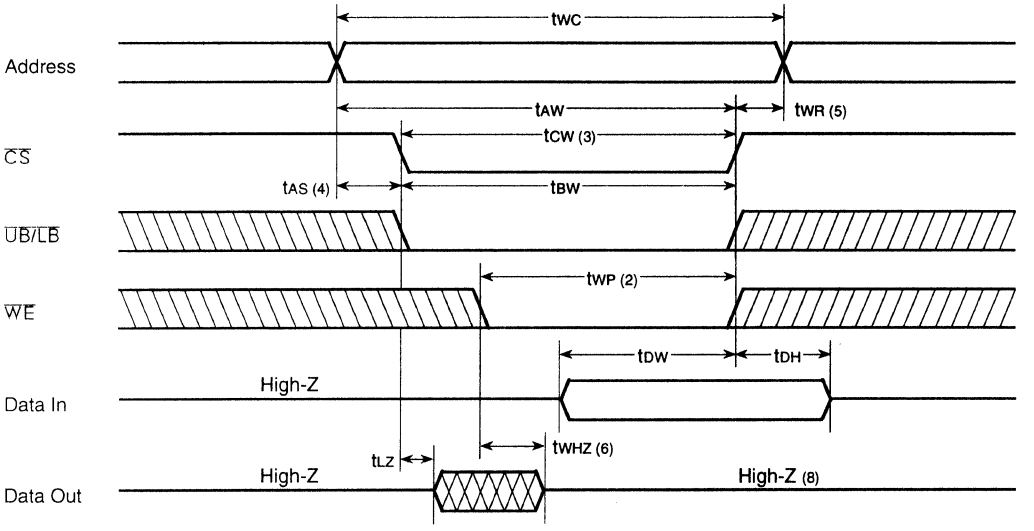
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

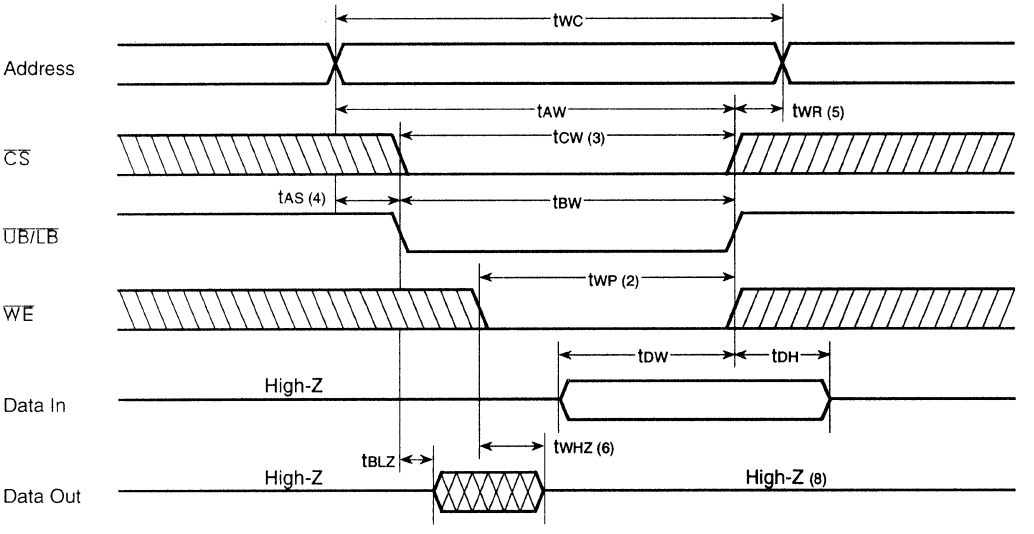
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$/$\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*Note : X means Don't Care.

Synchronous SRAM

- KM718B86	64K × 18	Sync. Burst SRAM with Interleave Burst Order(5V)
- KM718BV87	64K × 18	Sync. Burst SRAM with Interleave Burst Order
- KM718B90	64K × 18	Sync. Burst SRAM with Linear Burst Order(5V)
- KM718BV87AT	64K × 18	Sync. Burst SRAM with Interleave Burst Order
- KM732V588	32K × 32	Sync. Pipe & Burst SRAM with Interleave Burst Order
- KM732V589/L	32K × 32	Sync. Pipe & Burst SRAM with LBO# and ZZ Pin
- KM716V689	64K × 16	Sync. Pipe & Burst SRAM with LBO# and ZZ Pin
- KM736V695/L	64K × 36	Sync. Pipe & Burst SRAM with LBO# and ZZ Pin
- KM736V687	64K × 36	Sync. Burst SRAM with LBO# Pin

64K x 18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 5V±5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 3.3V I/O Compatible.
- 52-Pin PLCC Package.

GENERAL DESCRIPTION

The KM718B86 is a 1,179,648 bit Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches. It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

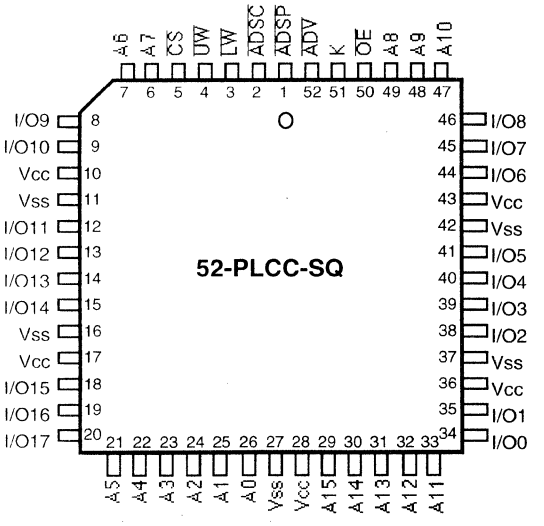
Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM718B86 is implemented in Samsung's high performance BiCMOS technology and is available in a 52 pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	-12	Unit
Cycle Time	tCYC	15	15	17	20	ns
Clock Access Time	tCD	8	9	10	12	ns
Output Enable Access Time	tOE	5	5	5	6	ns

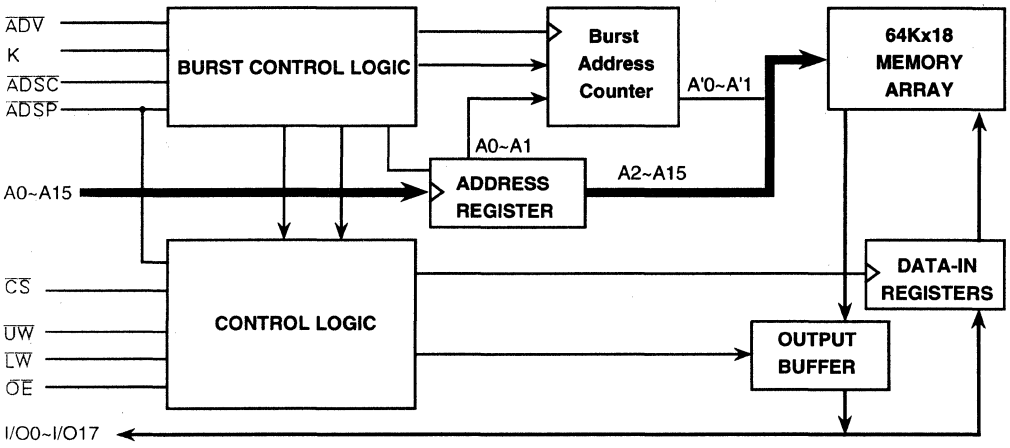
PIN CONFIGURATION(*Top View*)



PIN DESCRIPTION

Pin Name	Pin Function
A0~A15	Address Inputs
K	Clock
$\overline{LW}$,$\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B86 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/586 microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{LW}$,$\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is incremented internally for the next access of the burst when $\overline{LW}$,$\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$,$\overline{UW}$. $\overline{LW}$,$\overline{UW}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$,$\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{LW}$,$\overline{UW}$ is sampled low. The address is incremented internally to the next address of burst if both $\overline{LW}$,$\overline{UW}$ and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by sampling low only one byte write signal ($\overline{LW}$ or $\overline{UW}$), and $\overline{LW}$ controls I/O0 - I/O7 and $\overline{UW}$ controls I/O8 - I/O17.
Read or write cycles (depending on $\overline{LW}$,$\overline{UW}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{LW}$,$\overline{UW}$ is sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Address are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{LW}$/$\overline{UW}$	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE 1 : X means "Don't Care"
NOTE 2 : The rising edge of clock is symbolized by ↑

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Outputs High-Z
X	Not Selected, Outputs High-Z

NOTE 1 : X means "Don't Care"
NOTE 2 : For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.5 to 7.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS (T_A=0°C to 70°C, Vcc=5V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±5%, T_A=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	Vcc=Max; V_{IN}=Vss to Vcc		-2	+2	μA
Output Leakage Current	Iol	Output Disabled		-2	+2	μA
Operating Current	Icc	Vcc=Max				mA
		I_{OUT}=0mA	15ns	-	270	
		Cycle Time ≥ tCYC min	17ns	-	260	
			20ns	-	250	
Standby Current	Isb	Device deselected, I_{OUT}=0mA, Min Cycle All Inputs = V_{IH} and V_{IL}, V_{IH} ≥ 3V and V_{IL}=0V		-	90	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	3.3	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	Vcc+0.5	V

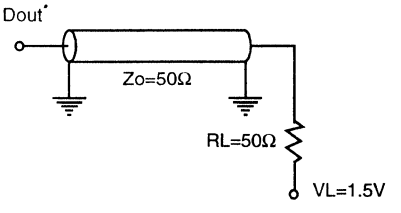
* Vil(min)=-3.0 (Pulse Width ≤20ns)

AC TIMING CHARACTERISTICS (Vcc=5V±5%, TA=0°C to +70°C)

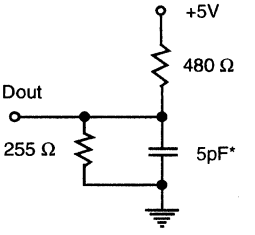
Parameter	Symbol	KM718B86-8		KM718B86-9		KM718B86-10		KM718B86-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15		15		17		20		ns
Clock Access Time	tCD		8		9		10		12	ns
Output Enable to Data Valid	tOE		5		5		5		6	ns
Clock High to Output Low-Z	tLZC	6		6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	0		0		0		0		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC		6		6		6		6	ns
Clock High Pulse Width	tCH	5		5		5		6		ns
Clock Low Pulse Width	tCL	5		5		5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

Output Load (A)

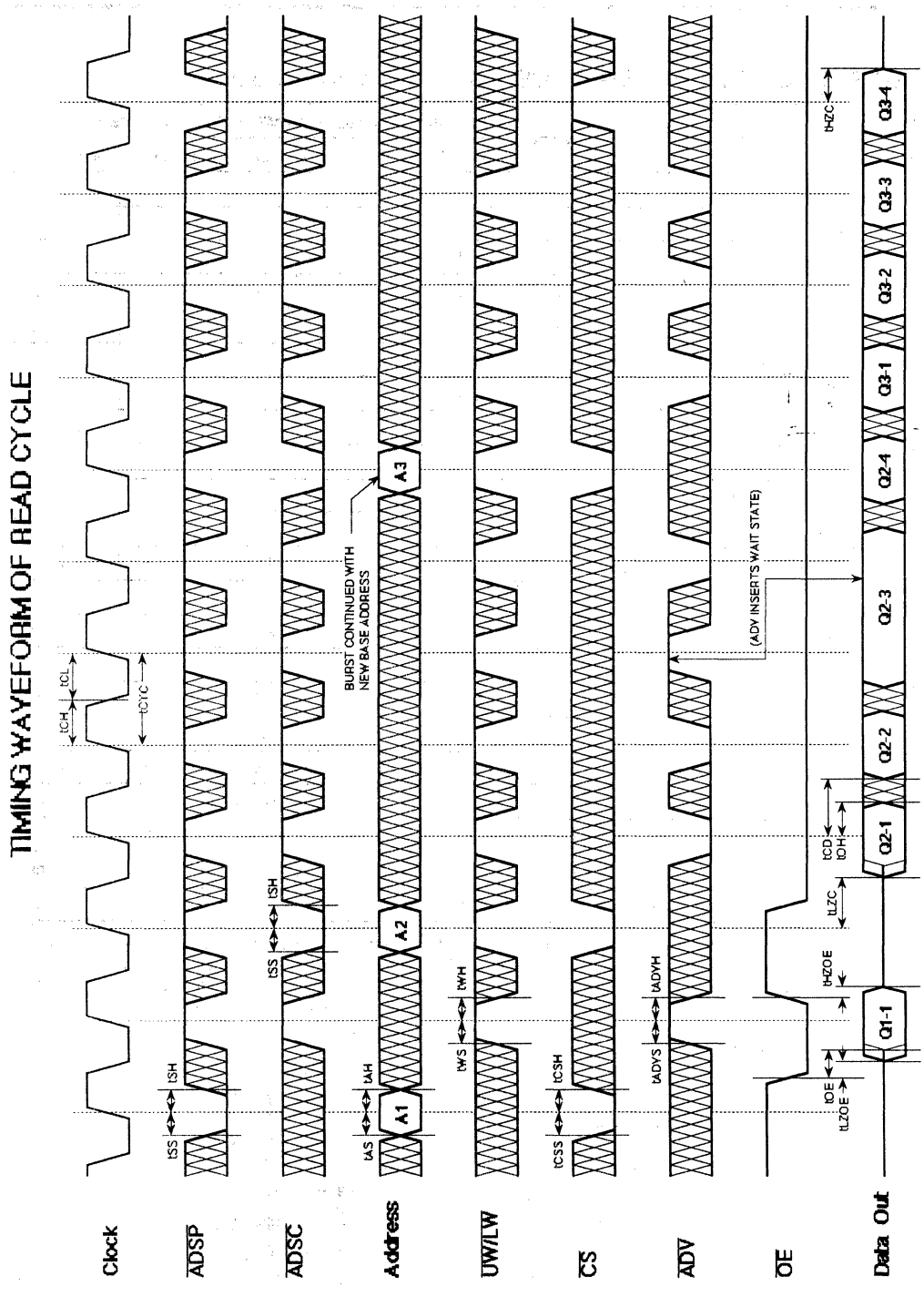


Output Load (B)
(for tLZC, tLZOE, tHZOE & tHZC)

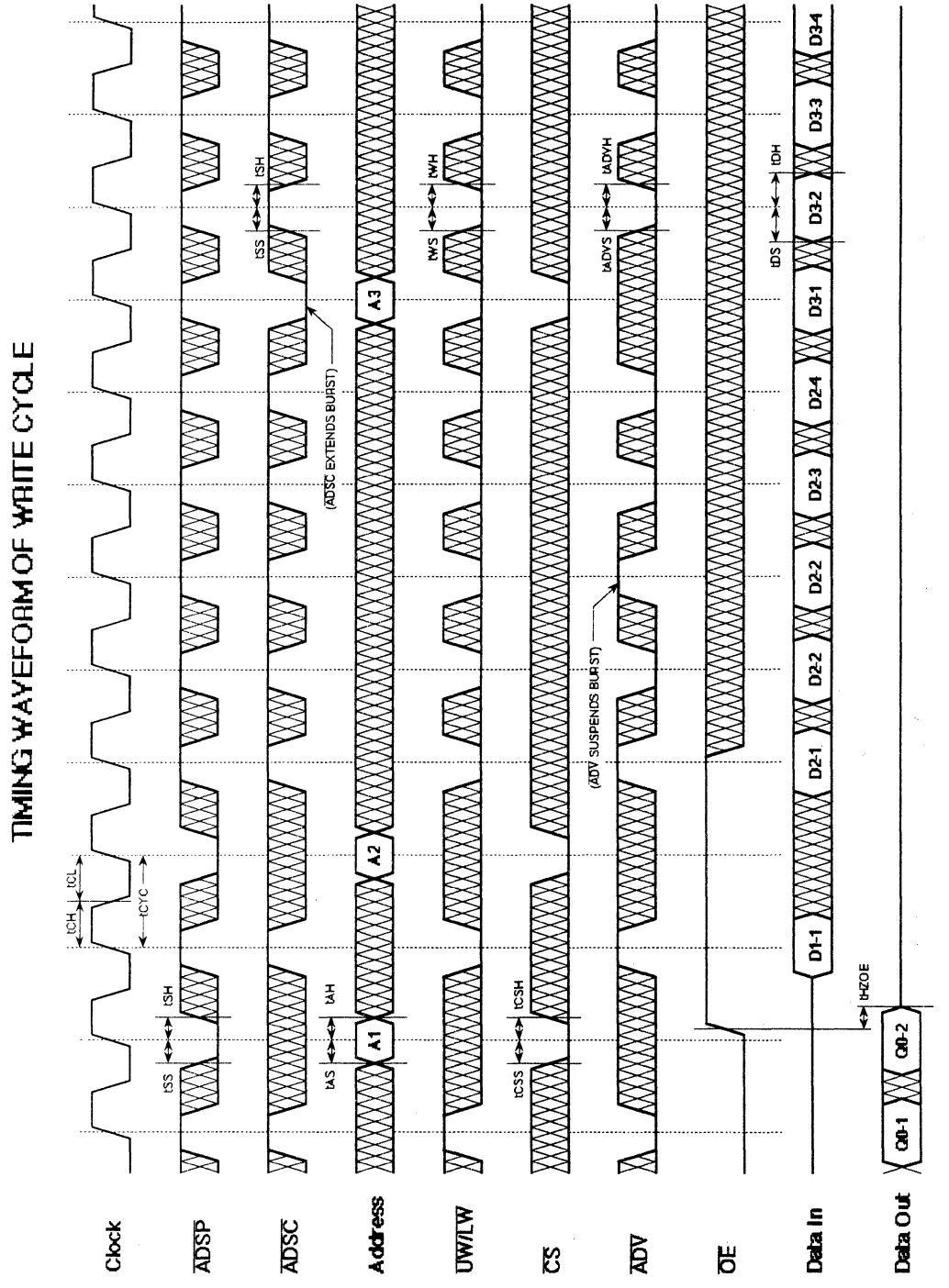


SAMSUNG ELECTRONICS

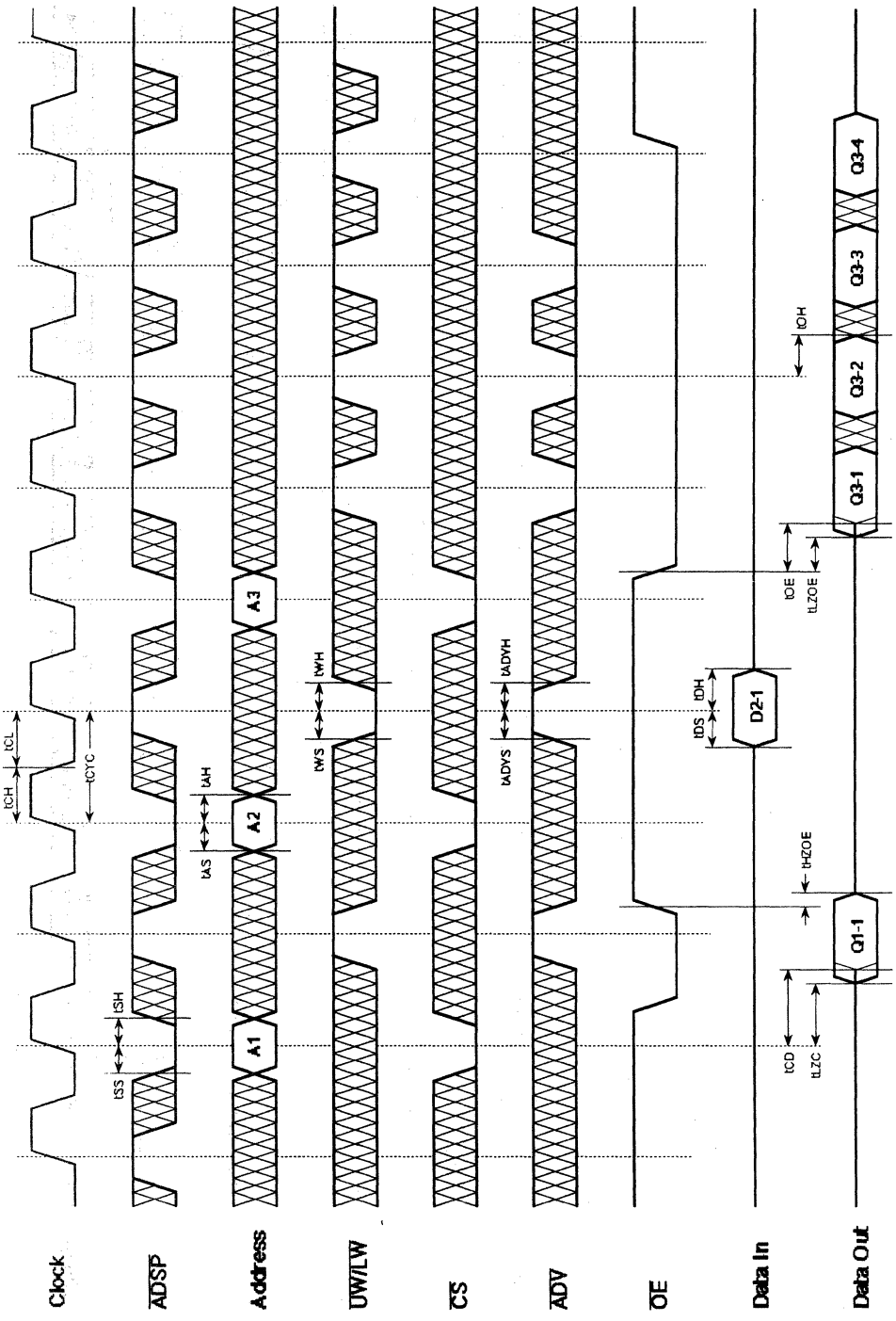
TIMING WAVEFORM OF READ CYCLE



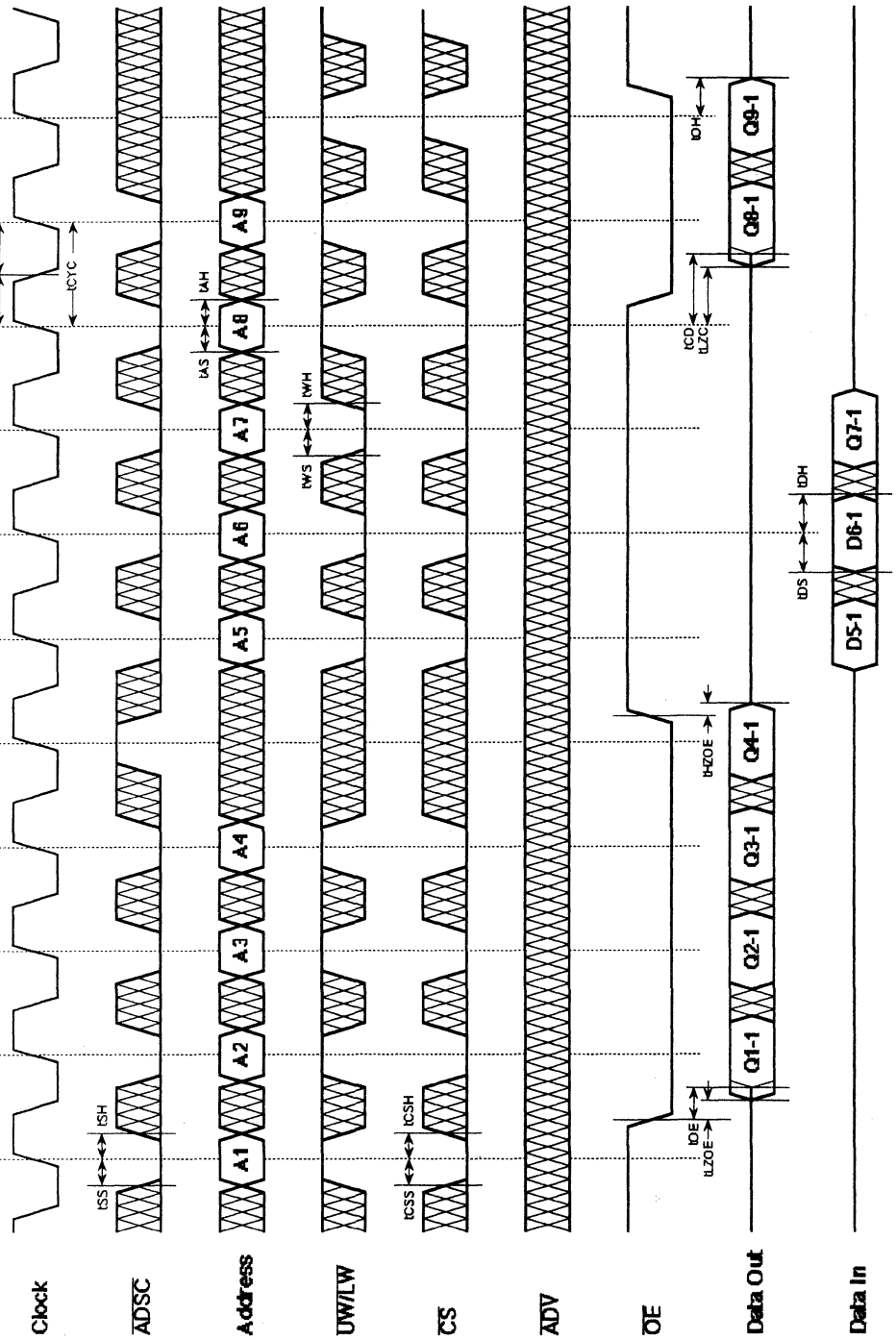
TIMING WAVEFORM OF WRITE CYCLE



TIMING WAYEFORM OF COMBINATION READ/WRITE CYCLE

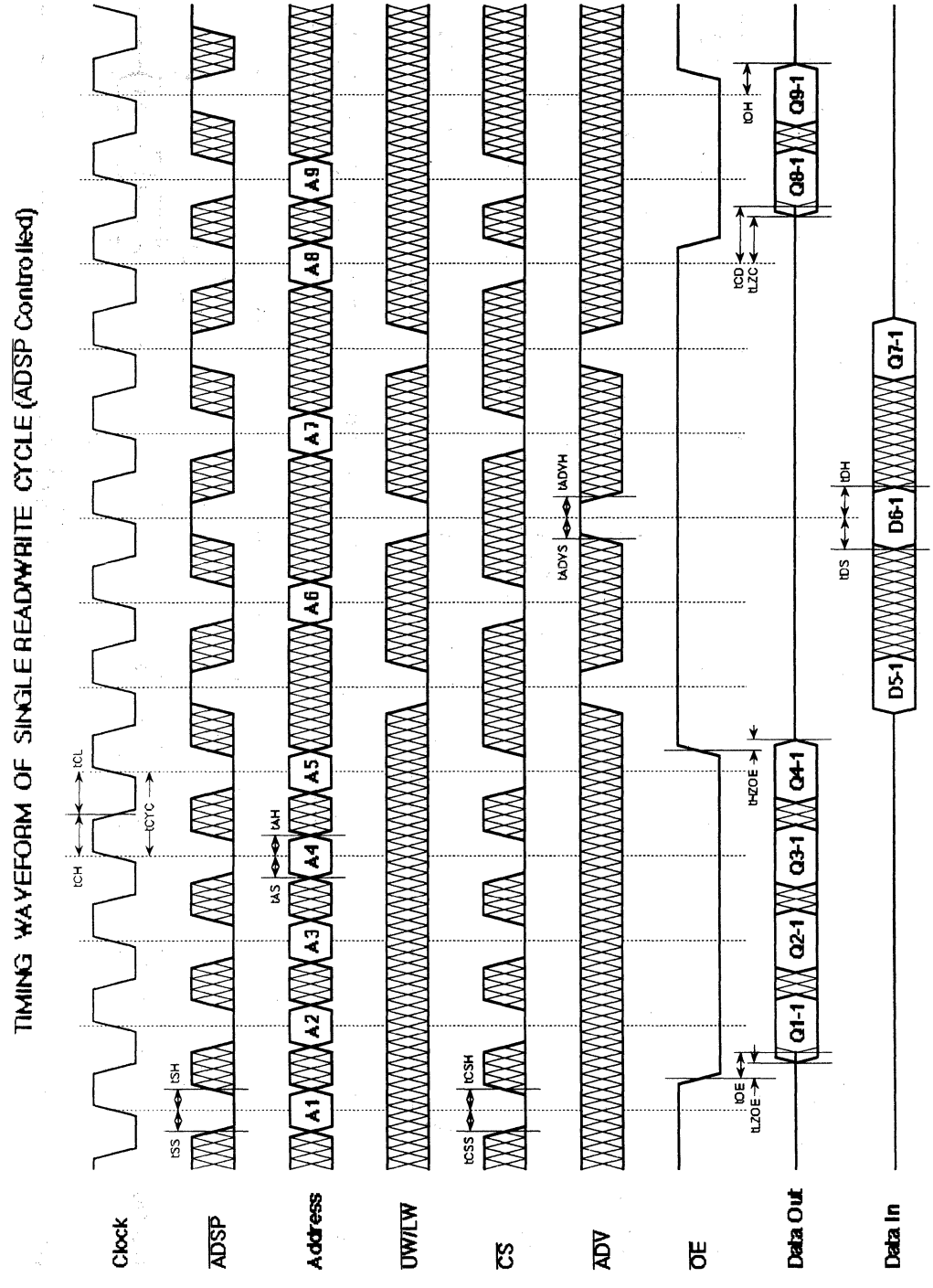


TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE (ADSC Controlled)



2

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE (ADSP Controlled)



64K x 18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V±5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 5V Tolerant I/O.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-9	-10	-12	Unit
Cycle Time	tCYC	15	17	20	ns
Clock Access Time	tCD	9	10	12	ns
Output Enable Access Time	tOE	5	5	6	ns

GENERAL DESCRIPTION

The KM718BV87 is a 1,179,648 bit Synchronous Static Random Access Memory designed to support zero wait state performance with advanced i486/Pentium address pipelining.

When $\overline{CS}$ is high, $\overline{ADSP}$ is blocked to control signals.

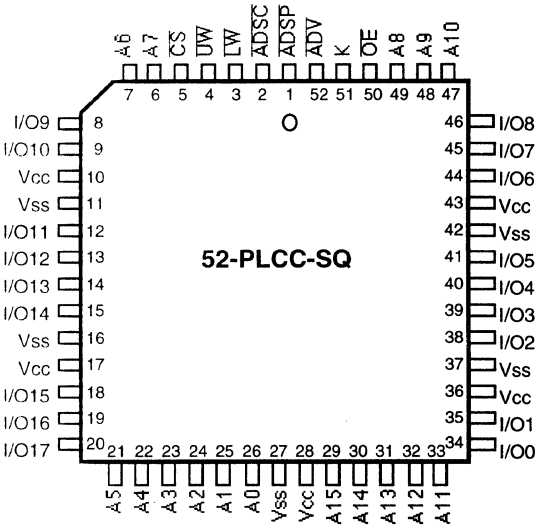
It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM718BV87 is implemented in Samsung's high performance BiCMOS technology and is available in a 52 pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce

PIN CONFIGURATION(*Top View*)

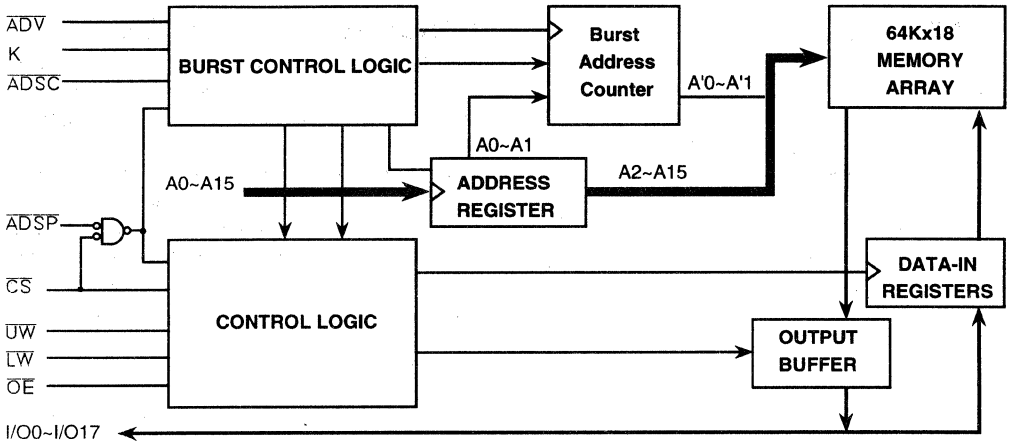


PIN DESCRIPTION

Pin Name	Pin Function
A0~A15	Address Inputs
K	Clock
$\overline{LW}$,$\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+3.3V Power Supply
Vss	Ground

SAMSUNG ELECTRONICS

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718BV87 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/586 microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{LW}$,$\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is incremented internally for the next access of the burst when $\overline{LW}$,$\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS}$.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$,$\overline{UW}$. $\overline{LW}$,$\overline{UW}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$,$\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{LW}$,$\overline{UW}$ is sampled low. The address is incremented internally to the next address of burst if both $\overline{LW}$,$\overline{UW}$ and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by sampling low only one byte write signal ($\overline{LW}$ or $\overline{UW}$), and $\overline{LW}$ controls I/O0 - I/O7 and $\overline{UW}$ controls I/O8 - I/O17.
Read or write cycles (depending on $\overline{LW}$,$\overline{UW}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{LW}$,$\overline{UW}$ is sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Address are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	LW/UW	K	Address Accessed	Operation
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
H	X	L	X	X	↑	N/A	Not Selected
H	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle

NOTE 1 : X means "Don't Care"

NOTE 2 : The rising edge of clock is symbolized by ↑

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Outputs High-Z
X	Not Selected, Outputs High-Z

NOTE 1 : X means "Don't Care"

NOTE 2 : For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

*NOTE : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

*NOTE : Sampled not 100% tested.

TEST CONDITIONS (T_A=0°C to 70°C, Vcc=3.3V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS (Vcc=3.3V±5%, T_A=0°C to +70°C)

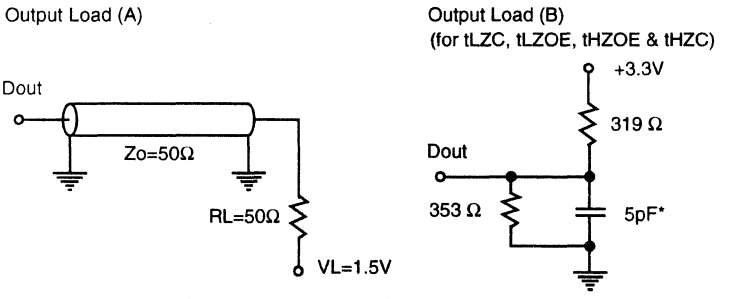
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	Vcc=Max; V_{IN}=Vss to Vcc		-2	+2	μA
Output Leakage Current	Iol	Output Disabled		-2	+2	μA
Operating Current	Icc	Vcc=Max	15ns	-	270	mA
		I_{OUT}=0mA	17ns	-	260	
		Cycle Time ≥ tCYC min	20ns	-	250	
Standby Current	Isb	$\overline{CS}$=V_{IH}, I_{OUT}=0mA, Min Cycle		-	80	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

AC TIMING CHARACTERISTICS (Vcc=3.3V±5%, TA=0°C to +70°C)

Parameter	Symbol	KM718BV87-9		KM718BV87-10		KM718BV87-12		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15		17		20		ns
Clock Access Time	tCD		9		10		12	ns
Output Enable to Data Valid	tOE		5		5		6	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	0		0		0		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC		6		6		6	ns
Clock High Pulse Width	tCH	5		5		6		ns
Clock Low Pulse Width	tCL	5		5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns

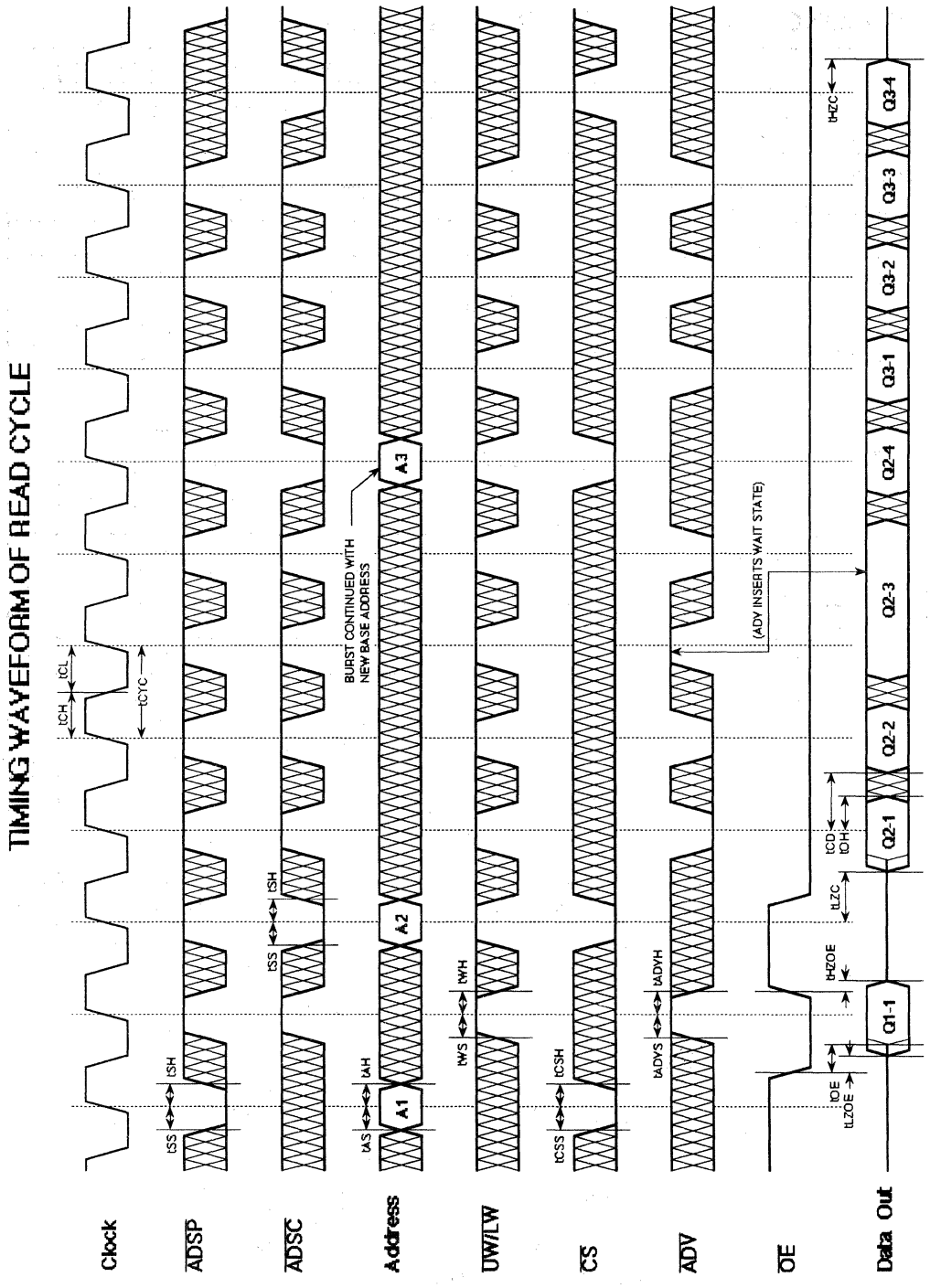
NOTE : All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.



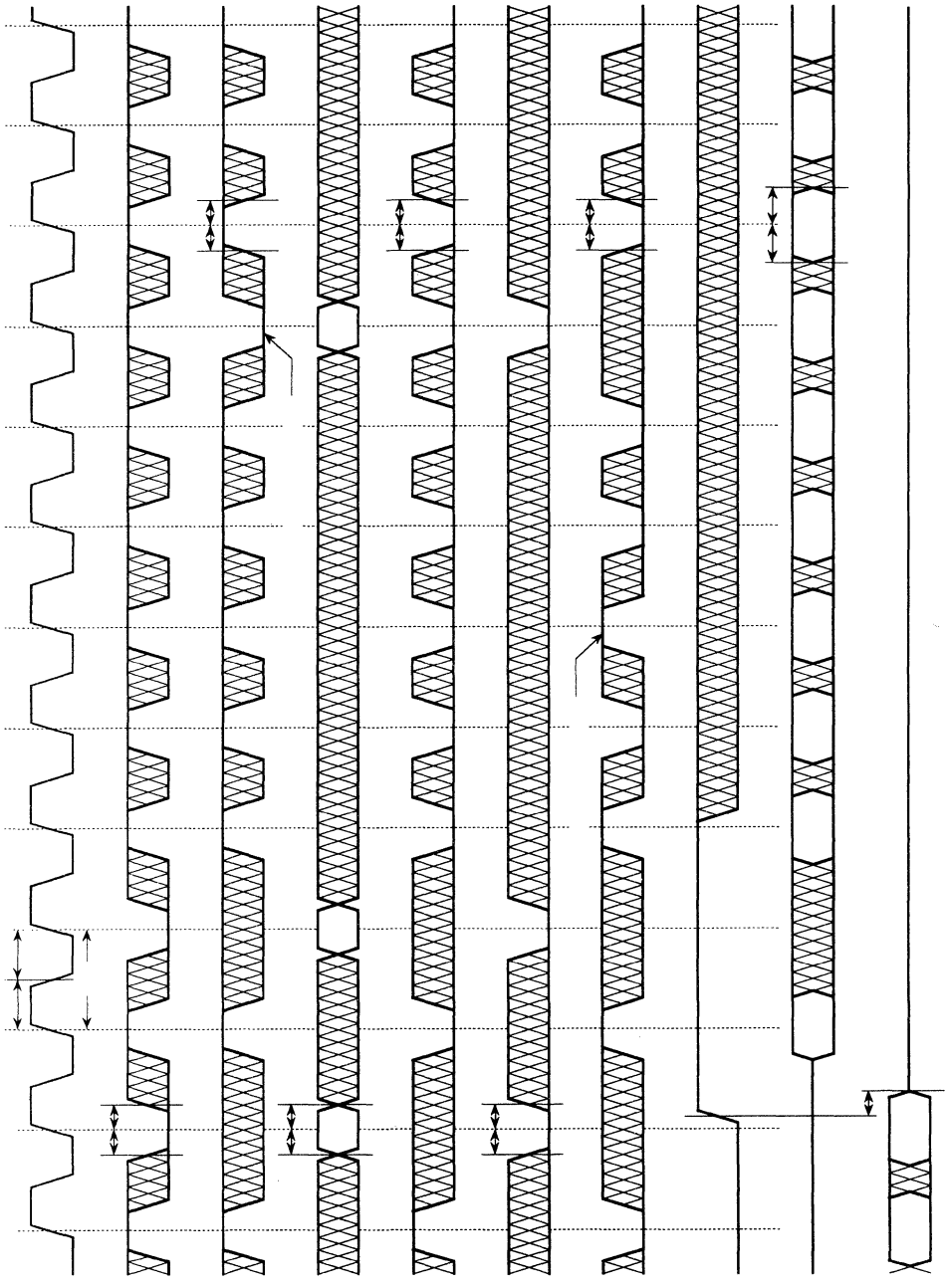
* Including Scope and Jig Capacitance **Fig. 1**

SAMSUNG ELECTRONICS

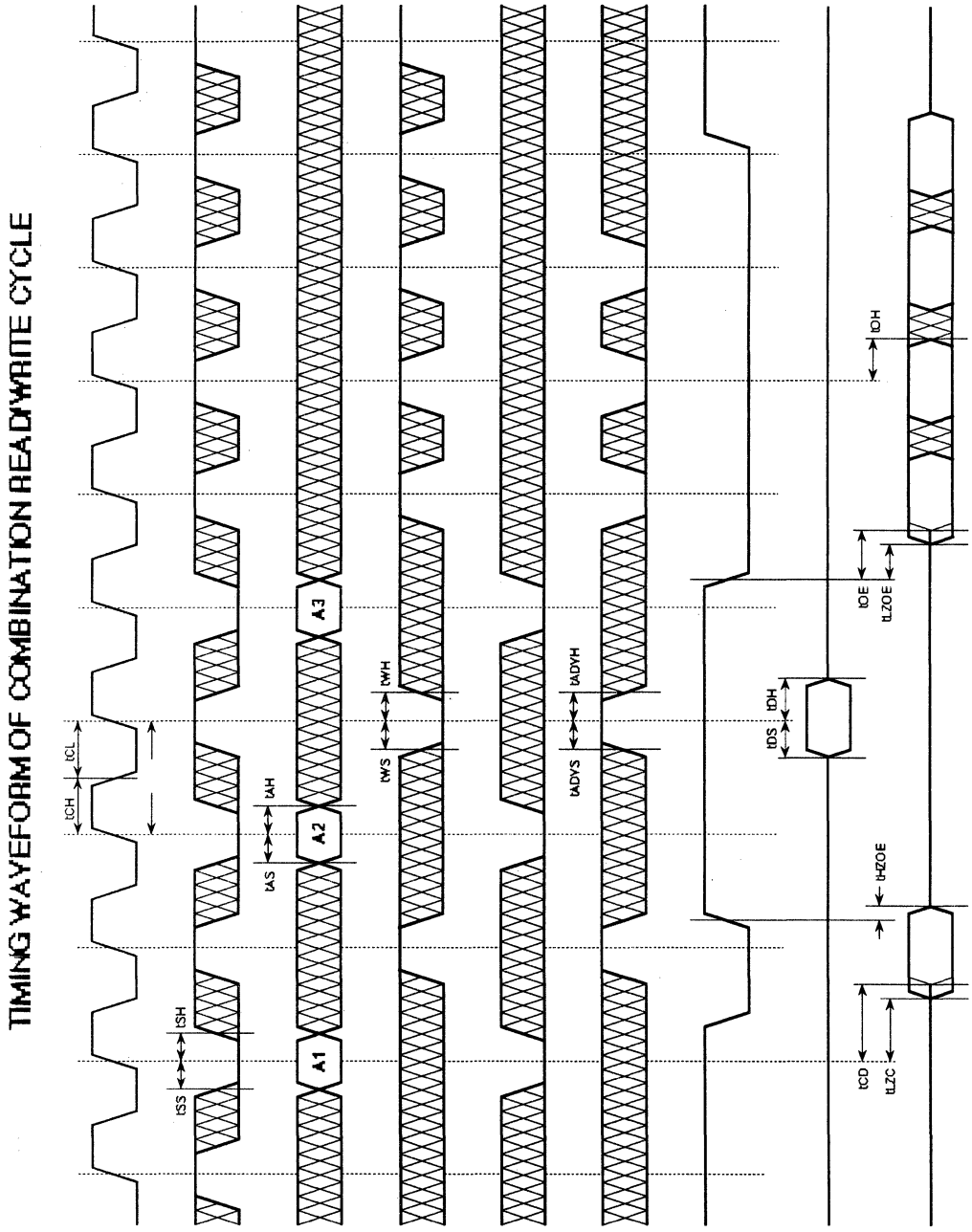
TIMING WAVEFORM OF READ CYCLE



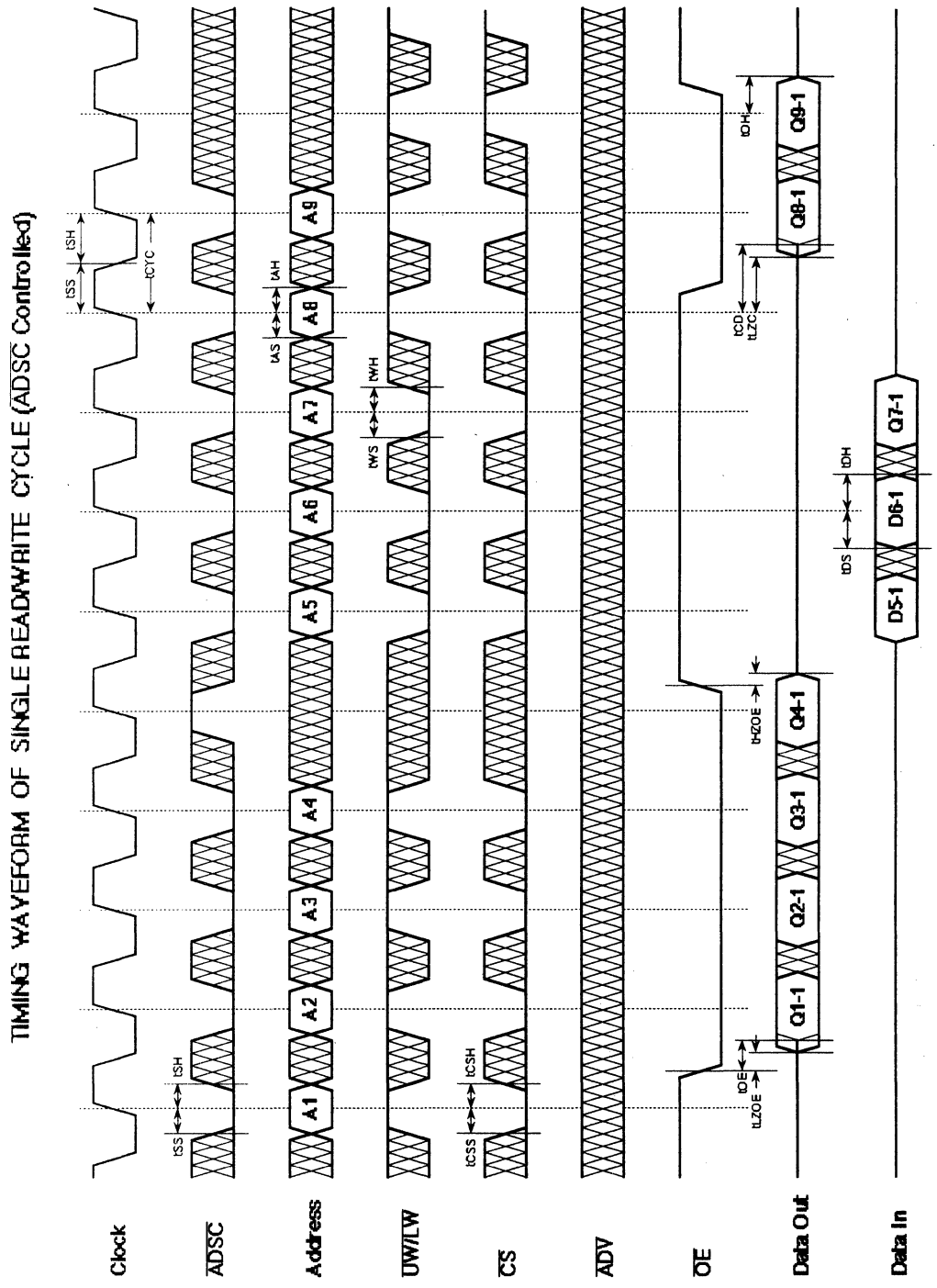
SAMSUNG ELECTRONICS



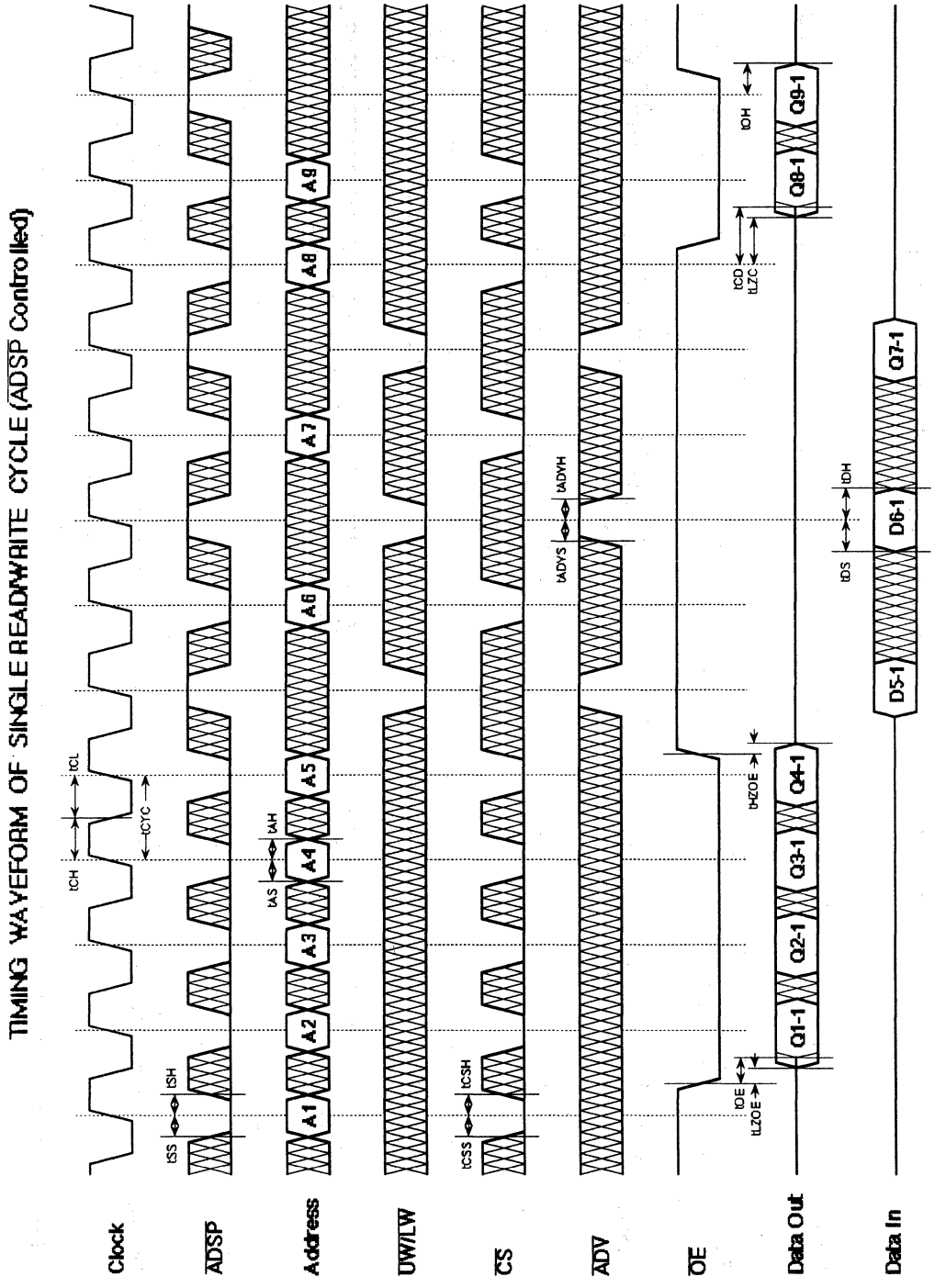
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE (ADSC Controlled)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE (ADSP Controlled)



64K x 18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 5V±5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 3.3V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	-11	Unit
Cycle Time	tCYC	15	15	17	20	ns
Clock Access Time	tCD	8	9	10	11	ns
Output Enable Access Time	tOE	5	5	5	6	ns

GENERAL DESCRIPTION

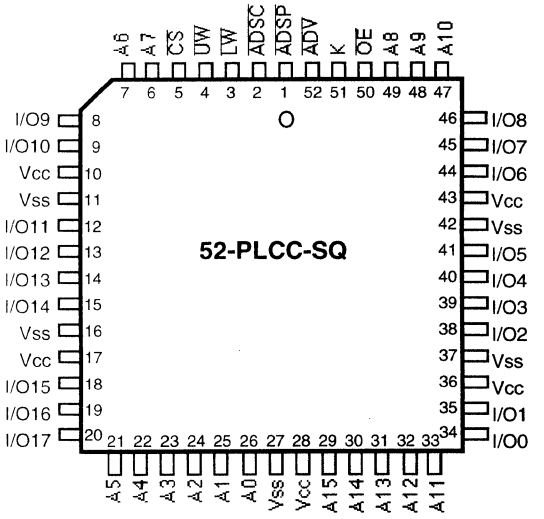
The KM718B90 is a 1,179,648 bit Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches. It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM718B90 is implemented in Samsung's high performance BiCMOS technology and is available in a 52 pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce

PIN CONFIGURATION(*Top View*)

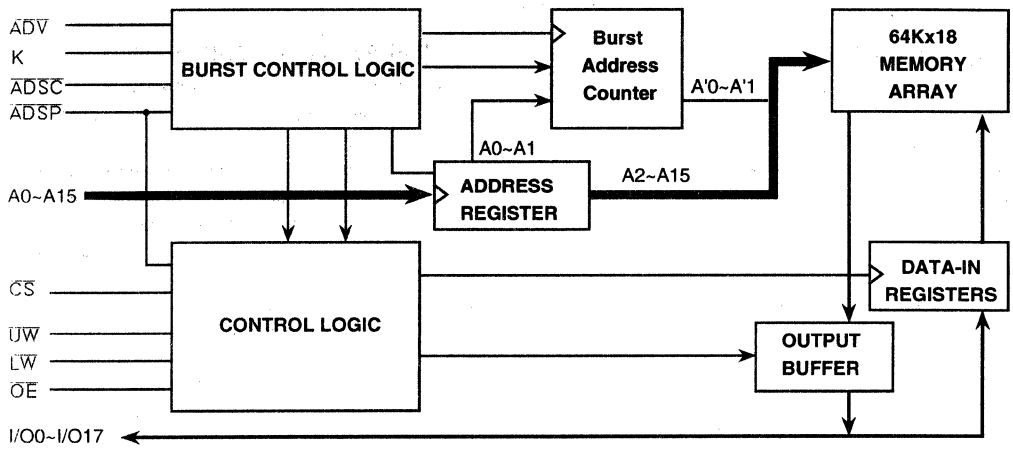


PIN DESCRIPTION

Pin Name	Pin Function
A0~A15	Address Inputs
K	Clock
$\overline{LW}$, $\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground

SAMSUNG ELECTRONICS

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B90 is a synchronous SRAM designed to support the burst address accessing sequence of the POWER microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{LW}$,$\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is incremented internally for the next access of the burst when $\overline{LW}$,$\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$,$\overline{UW}$. $\overline{LW}$,$\overline{UW}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$,$\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{LW}$,$\overline{UW}$ is sampled low. The address is incremented internally to the next address of burst if both $\overline{LW}$,$\overline{UW}$ and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by sampling low only one byte write signal ($\overline{LW}$ or $\overline{UW}$), and $\overline{LW}$ controls I/O0 - I/O7 and $\overline{UW}$ controls I/O8 - I/O17.
Read or write cycles (depending on $\overline{LW}$,$\overline{UW}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{LW}$,$\overline{UW}$ is sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Address are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	LW/UW	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE 1 : X means "Don't Care"
NOTE 2 : The rising edge of clock is symbolized by ↑

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Outputs High-Z
X	Not Selected, Outputs High-Z

NOTE 1 : X means "Don't Care"
NOTE 2 : For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.5 to 7.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS (T_A=0°C to 70°C, Vcc=5V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±5%, T_A=0°C to +70°C)

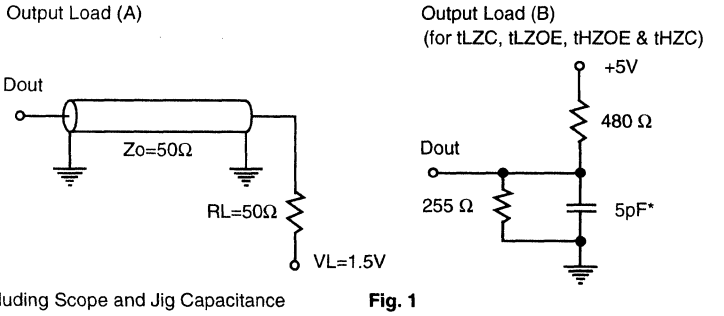
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	Vcc=Max; V_{IN}=Vss to Vcc		-2	+2	μA
Output Leakage Current	Iol	Output Disabled		-2	+2	μA
Operating Current	Icc	Vcc=Max				mA
		I_{OUT}=0mA	15ns	-	270	
		Cycle Time ≥ tCYC min	17ns	-	260	
			20ns	-	250	
Standby Current	Isb	Device deselected, I_{OUT}=0mA, Min Cycle		-	90	mA
		All Inputs = V_{IH} and V_{IL}, V_{IH} ≥ 3V and V_{IL}=0V				
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	3.3	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	Vcc+0.5	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

AC TIMING CHARACTERISTICS (Vcc=5V±5%, TA=0°C to +70°C)

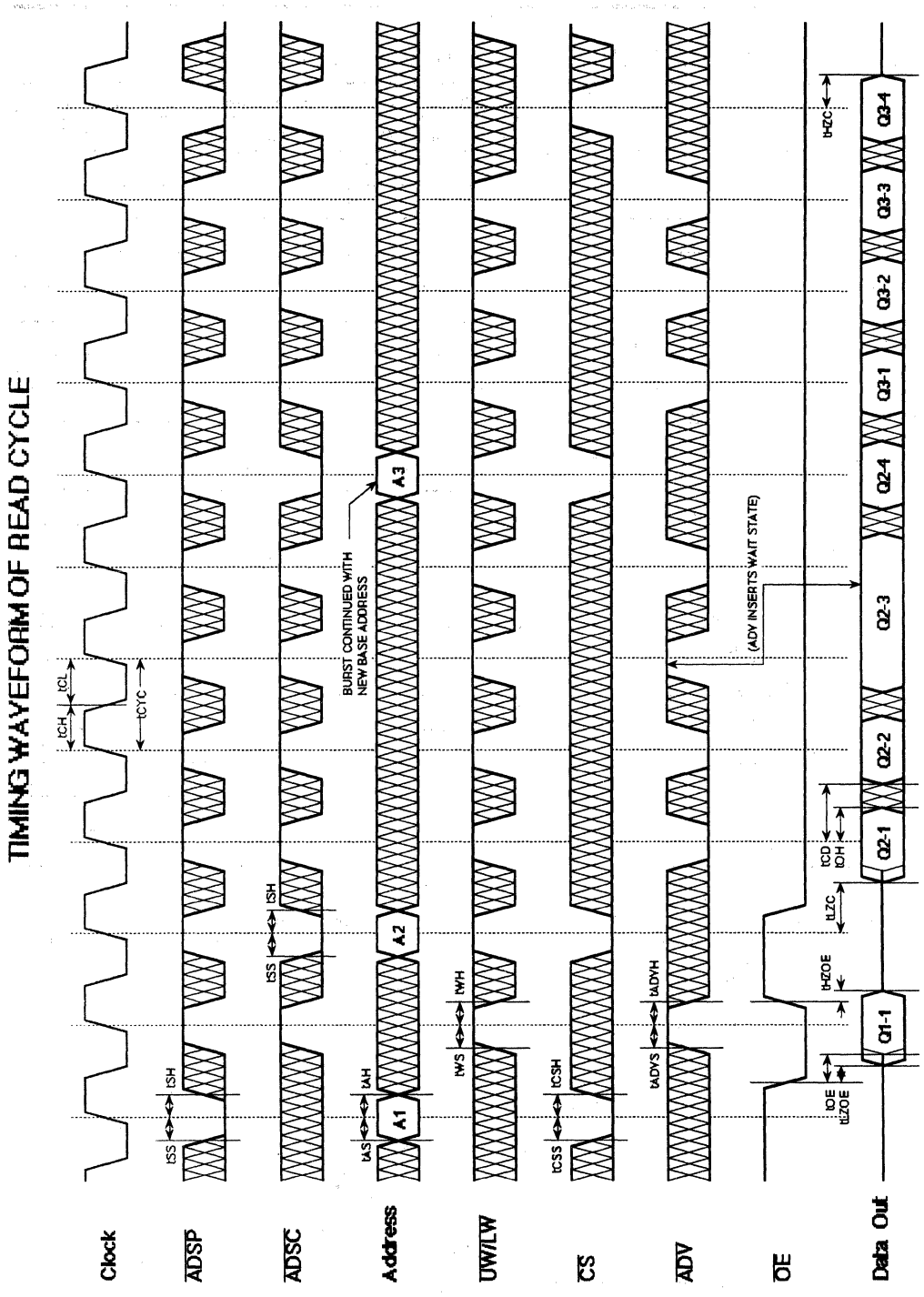
Parameter	Symbol	KM718B90-8		KM718B90-9		KM718B90-10		KM718B90-11		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15		15		17		20		ns
Clock Access Time	tCD		8		9		10		11	ns
Output Enable to Data Valid	tOE		5		5		5		6	ns
Clock High to Output Low-Z	tLZC	6		6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	0		0		0		0		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC		6		6		6		6	ns
Clock High Pulse Width	tCH	5		5		5		6		ns
Clock Low Pulse Width	tCL	5		5		5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

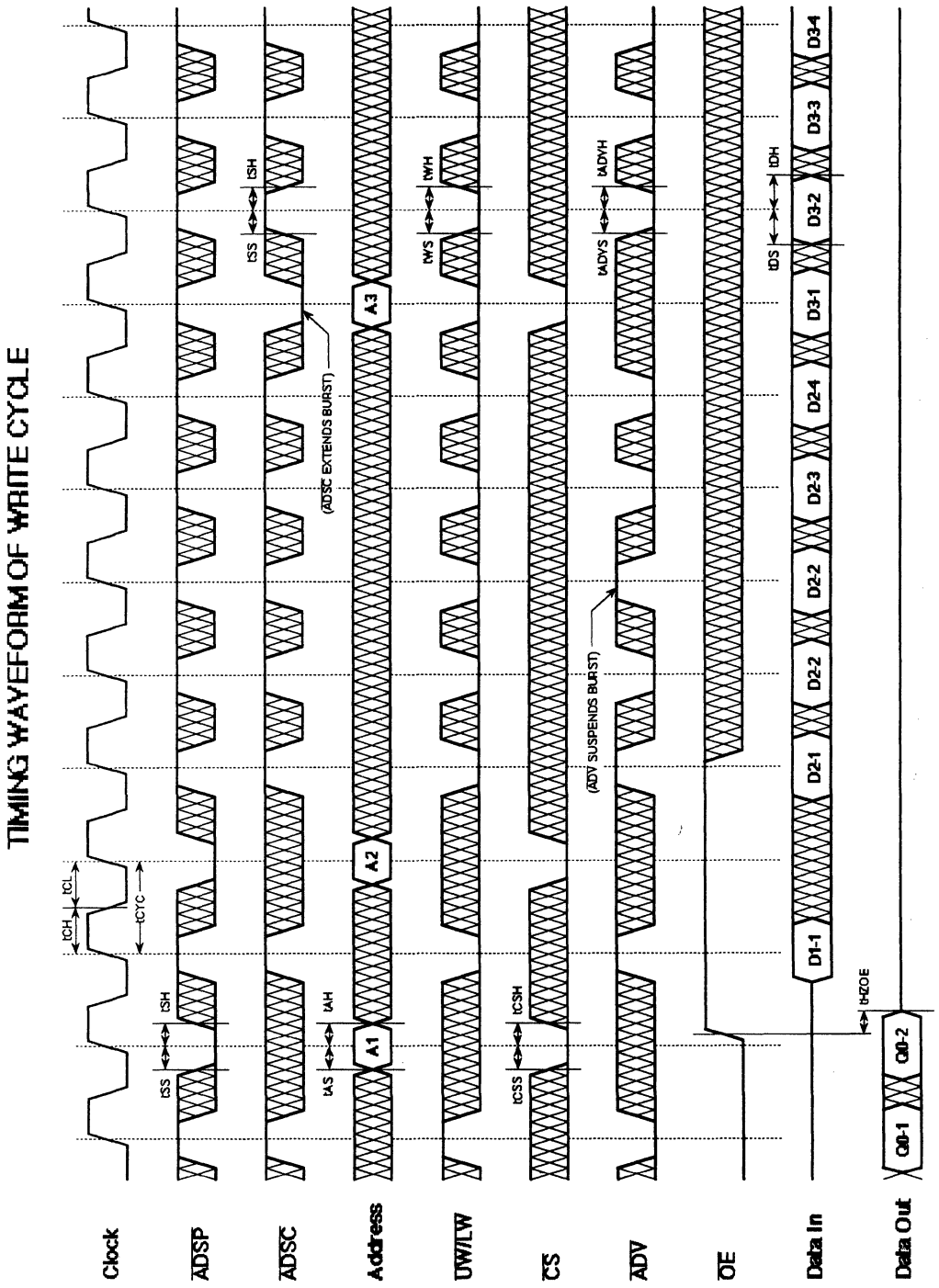


* Including Scope and Jig Capacitance **Fig. 1**

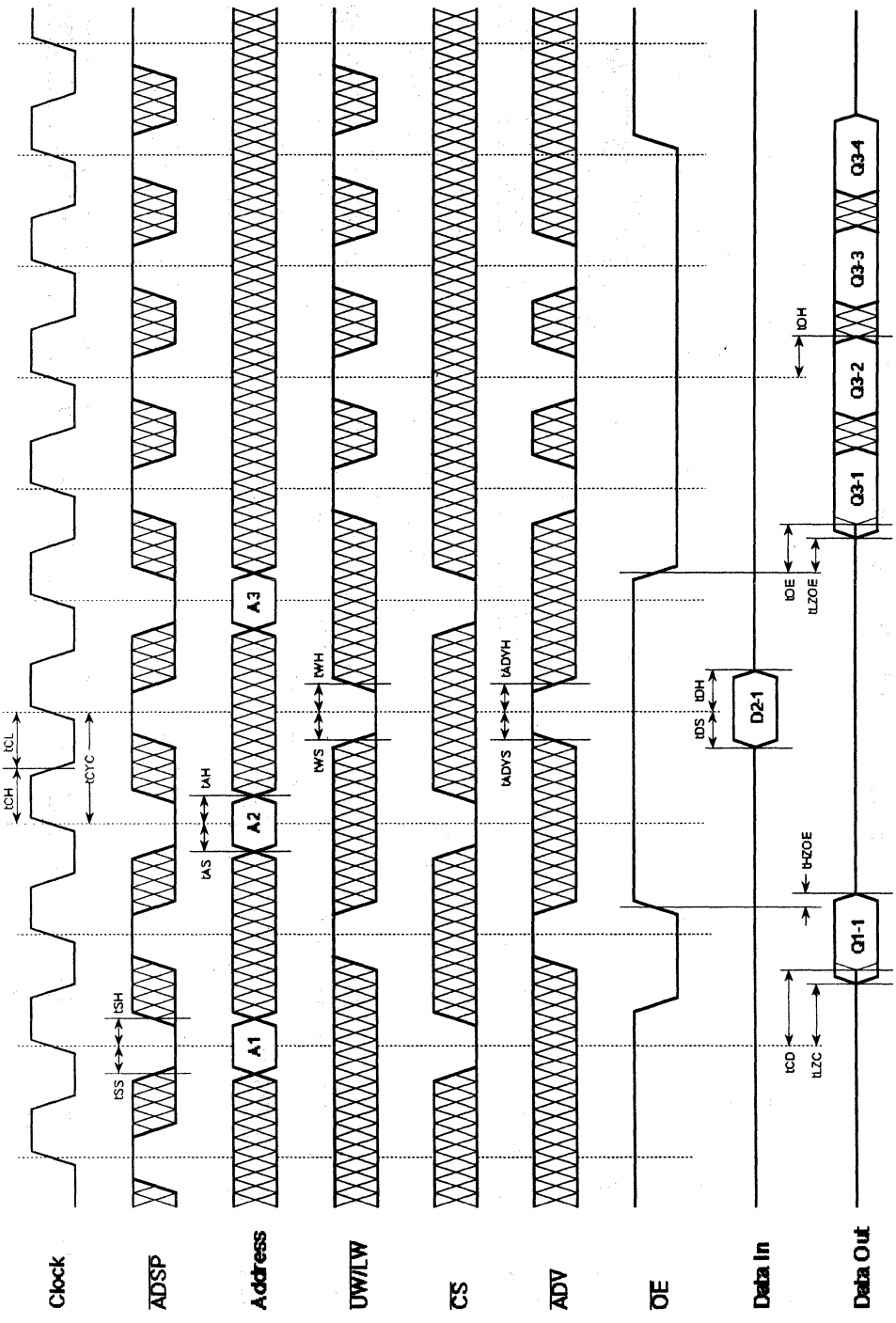
TIMING WAVEFORM OF READ CYCLE



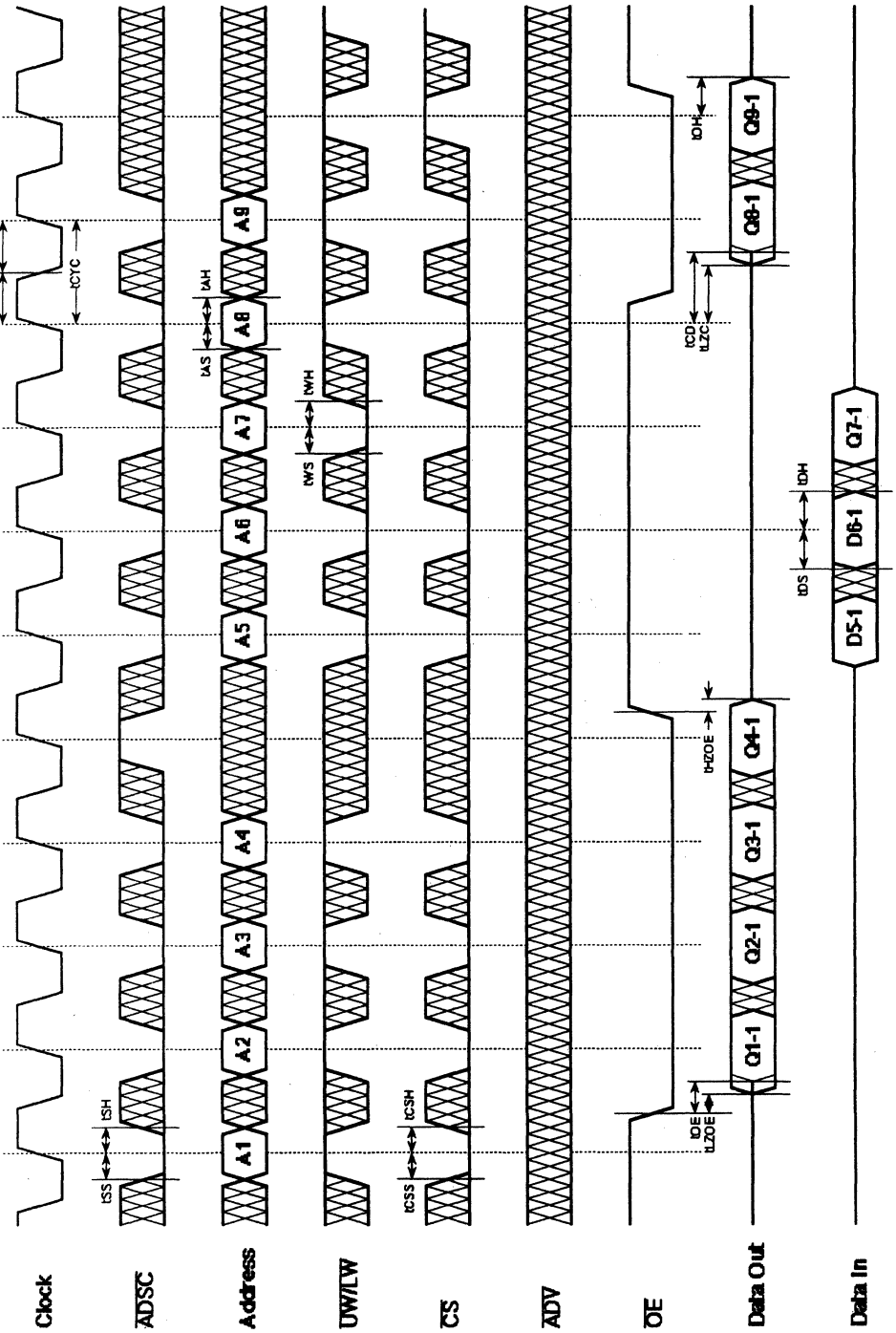
TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE

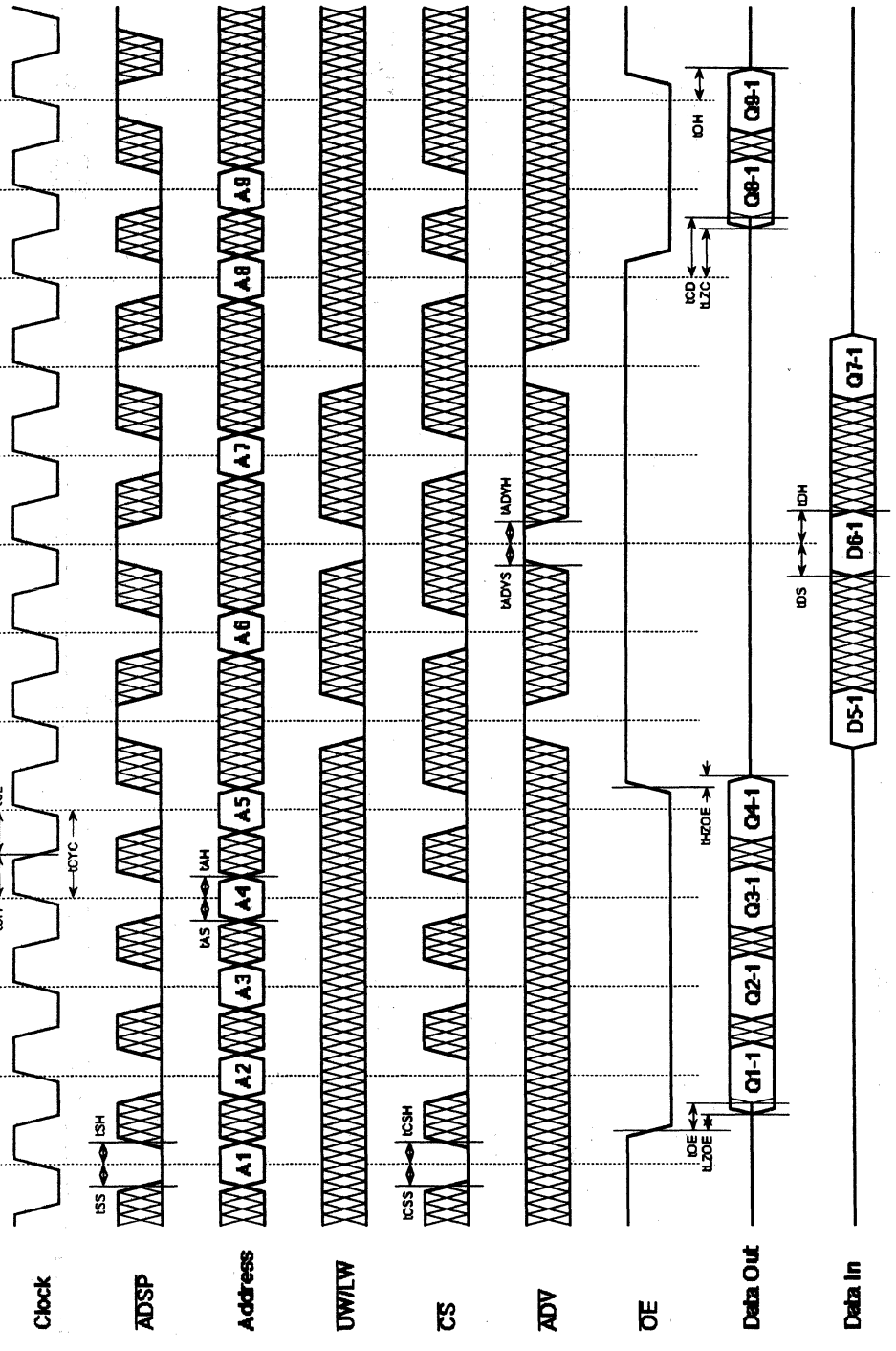


TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE (ADSC Controlled)



2

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE (ADSP Controlled)



64K x 18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V±5% Power Supply.
- 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write
- Asynchronous Output Enable Control.
- /ADSP, /ADSC, /ADV Burst Control Pins.
- /LBO Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention
- TTL-Level Three-State Outputs.
- 100-Pin TQFP Package.

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	11	15	17	ns
Clock Access Time	tCD	8	9	10	ns
Output Enable Access Time	tOE	5	5	5	ns

GENERAL DESCRIPTION.

The KM718BV87AT is a 1,179,648 bit Synchronous Static Random Access Memory designed to support zero wait state performance with advanced Pentium /Power PC address pipelining.

When /CS1 is high, /ADSP is blocked to external signals.

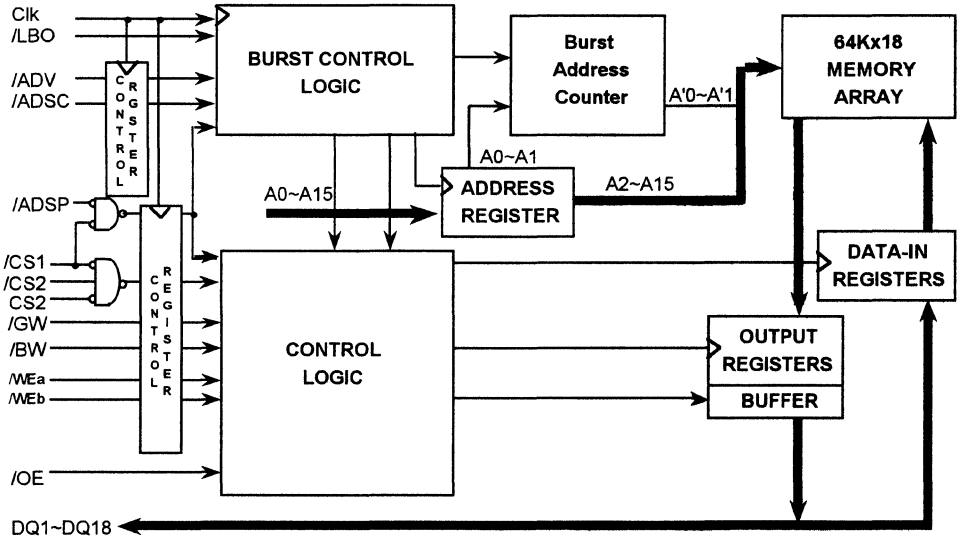
It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

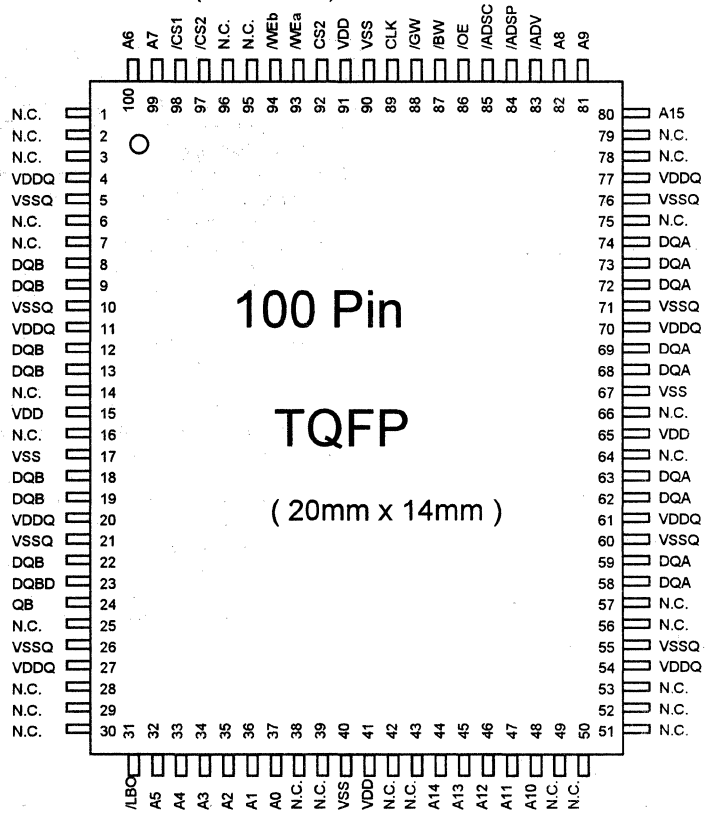
Bursts can be initiated with either the address status processor (/ADSP) or adress status cache controller (/ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance (/ADV) input.

The KM718BV87AT is implemented in Samsung's high performance BiCMOS technology and is available in a 100 pin TQFP package. Multiple Power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	PIN NO.	SYMBOL	PIN NAME	PIN NO.
A0-A15	Address Inputs	32, 33, 34, 35, 36 37, 44, 45, 46, 47 48, 80, 81, 82, 99 100	VDD	PowerSupply (+3.3V)	15, 41, 65, 91
			VSS	Ground	17, 40, 67, 90
			NC	No Connect	1,2,3,6,7,14,16,24 25,28,29,30, 38,39 42,43,49,50,51,52 53,56,57,66,74,75 78, 79,95, 96
/ADV	Burst Address /ADVance	83			
/ADSP	Address Status Processor	84			
/ADSC	Address Status Controller	85			
CLK	Clock	89	DQ1~	Data Inputs/Outputs	8,9,12,13,18,19,22
/CS1	Chip Select	98	DQ18		23,24, 58, 59 62
/CS2	Chip Select	97			63, 68, 69, 72,73,74
CS2	Chip Select	92	VDDQ	Output Po/WEr Supply	4, 11, 20, 27, 54, 61
/BWx	Byte Write inputs	93, 94		(+3.3V)	70, 77
/OE	Output Enable	86	VSSQ	Output Ground	5, 10, 21, 26, 55,60
/GW	Global Write Enable	88			71, 76
/BW	Byte Write Enable	87			
/LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM718BV87AT is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of /OE and /LBO) are sampled on rising clock edges. The start and duration of the burst access is controlled by /ADSP, /ADSC, /ADSP,/ADV and Chip Select pins.

Read cycles are initiated with /ADSP (or /ADSC) using the new external address clocked into the on-chip address register when both /GWE and /BWE are High. When /ADSP is sampled low, the chip selects are sampled active, and the output buffer is enabled with /OE, the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with /ADSP (or /ADSC) and are consisted of two kind of operations ; All byte write operation and individual byte write operation .
All byte write occurres by enabling /GWE (in dependent of /BWE and /BWx.) , and individual byte write is performed onlywhen /GW is High and /BWE is Low. /WEa controls DQ1~DQ9, /WEb controls DQ10~DQ18.

/CS1 is used to enable the device and conditions internal use of /ADSP and is sampled only when a new external address is loaded.

/ADV is ignored at the clock edge when /ADSP is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when /ADV is sampled low.

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the /LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High or N.C, Interleaved burst sequence is selected

BURST SEQUENCE TABLE

(Interleaved Burst , /LBO=High or N.C)

/LBO pin	High or N.C	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Lenear Burst, LBO=Low)

/LBO pin	Low	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

/CS1	CS2	CS2	/ADSP	/ADSC	/ADV	/WRITE	K	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE :

1. X means "Don't Care"

2. The rising edge of clock is symbolized by ↑

3. **/WRITE** =L means Write operation in WRITE TRUTH TABLE
/WRITE =H means Read operation in WRITE TRUTH TABLE

4. Operation finally depends on status of asynchronous input pins (/OE)

WRITE TRUTH TABLE

/GW	/BW	/WEa	/WEb	Operation
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

NOTE :

1. X means "Don't Care"

2. All inputs in this table must meet setup and hold time around the rising edge of CLK (↑)

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Po/WEr Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A =25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} =0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT} =0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS (T_A=0°C to 70°C, Vcc=3.3V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS (Vcc=3.3V±5%, TA=0°C to +70°C)

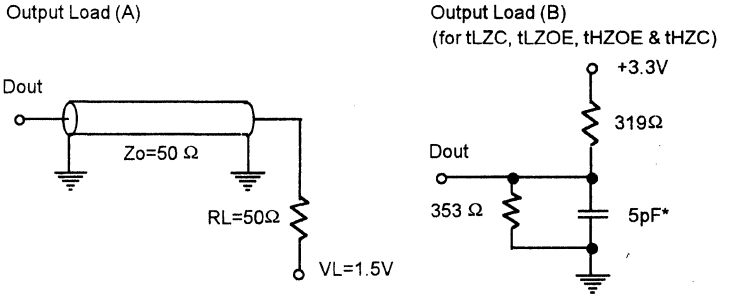
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	Vcc=Max; VIN=Vss to Vcc		-2	+2	μA
Output Leakage Current	Iol	Output Disabled		-2	+2	μA
Operating Current	Icc	Vcc=Max	11ns	-	300	mA
		IOUT=0mA	15ns	-	270	
		Cycle Time ≥ tCYC min	17ns	-	260	
Standby Current	Icc	CS=VIH, IOUT=0mA, Min Cycle		-	100	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5	V

* Vil(min)=-3.0 (Pulse Width ≤ 20ns)

AC TIMING CHARACTERISTICS (Vcc=3.3V±5%, TA=0°C to +70°C)

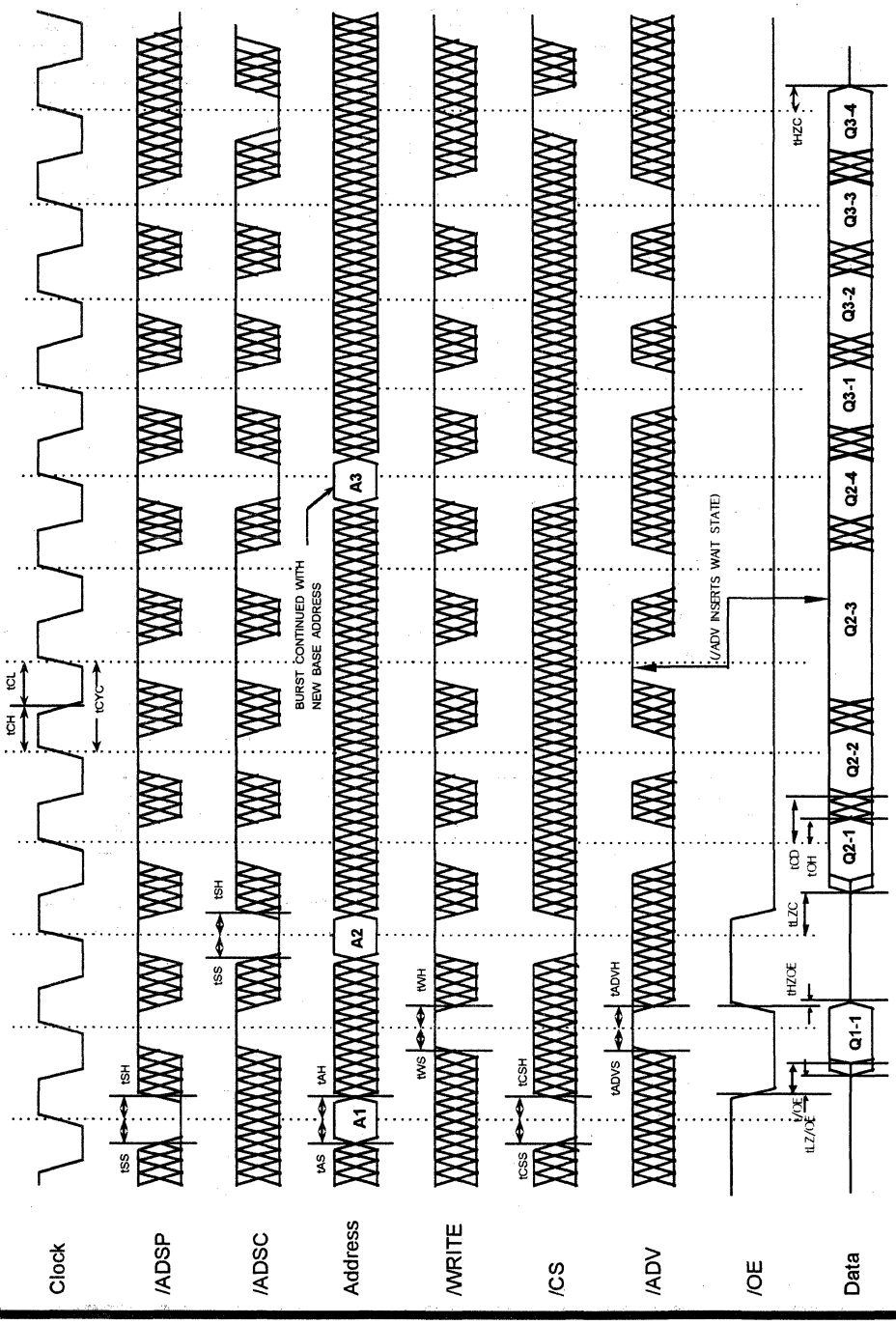
Parameter	Symbol	KM718BV87-8		KM718BV87-9		KM718BV87-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	11		15		17		ns
Clock Access Time	tCD		8		9		10	ns
Output Enable to Data Valid	tOE		5		5		5	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	0		0		0		ns
Output Enable High to Output High-Z	tHZOE	2		2	5	2	5	ns
Clock High to Output High-Z	tHZC		5		6		6	ns
Clock High Pulse Width	tCH	4		5		5		ns
Clock Low Pulse Width	tCL	4		5		5		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		ns
Address /ADVance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		ns
Address /ADVance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever /ADSC and/or /ADSP is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever /ADSC or /ADSP is sampled low in order for the this device to remain enabled.

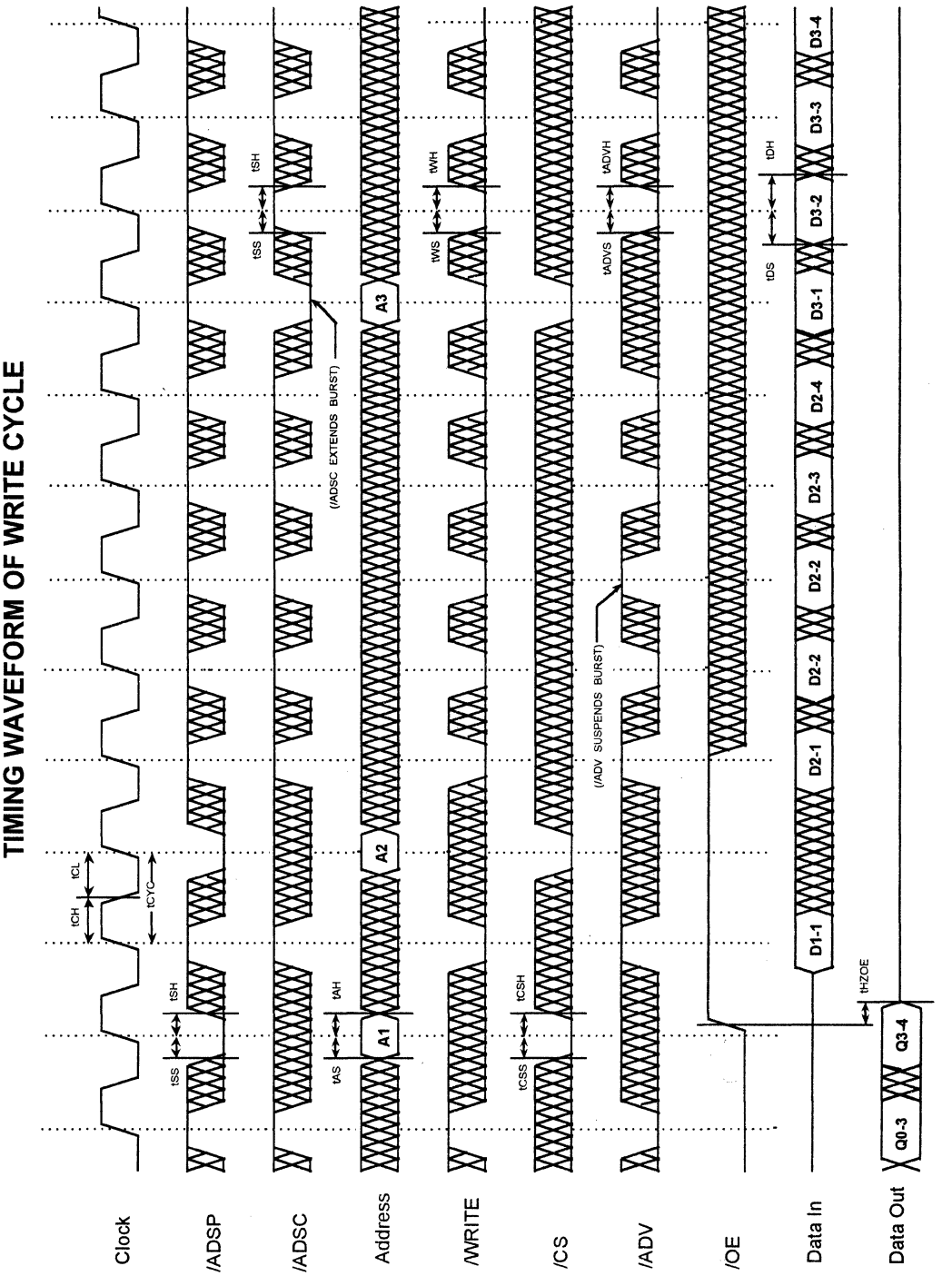


* Including Scope and Jig Capacitance **Fig. 1**

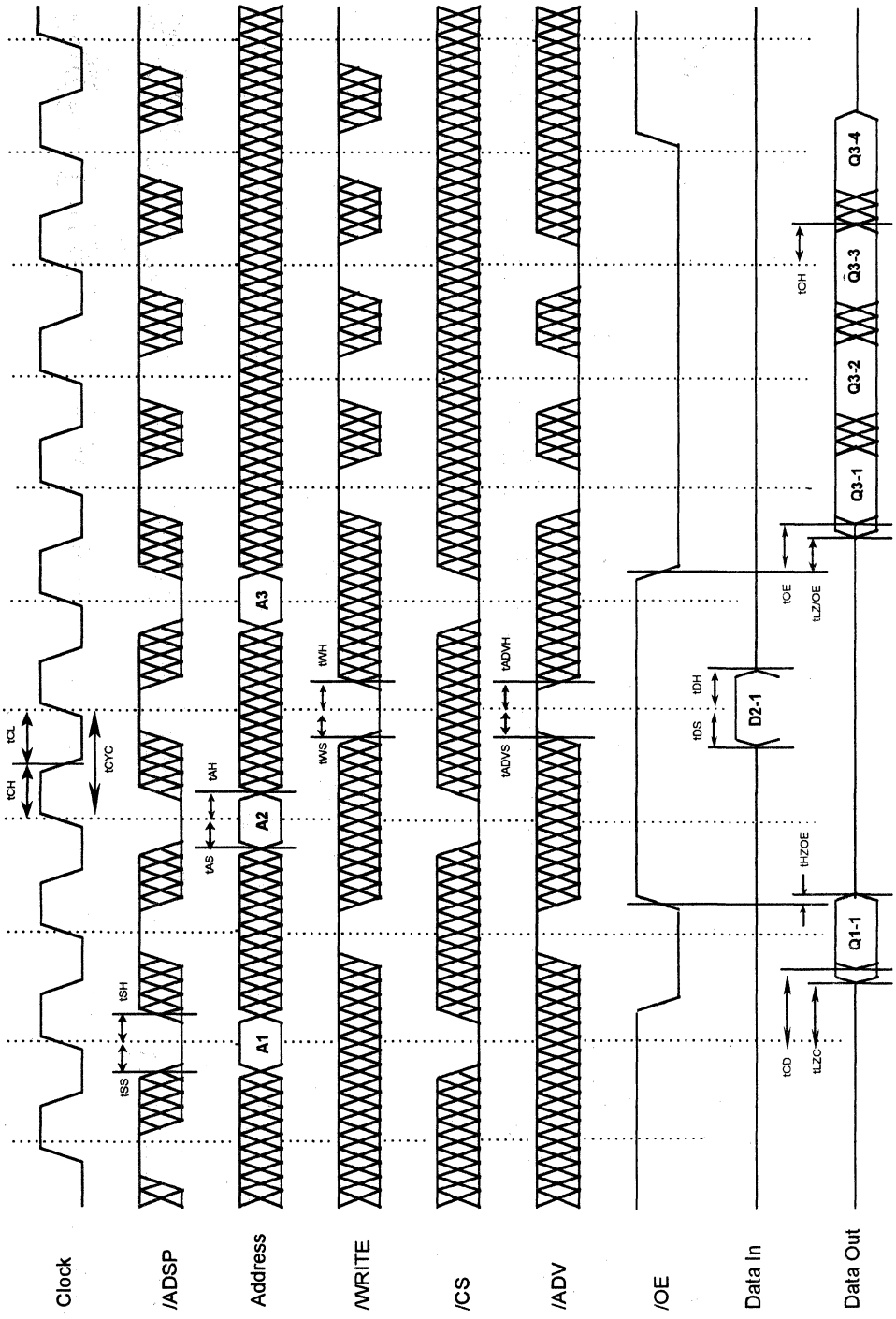
TIMING WAVEFORM OF READ CYCLE



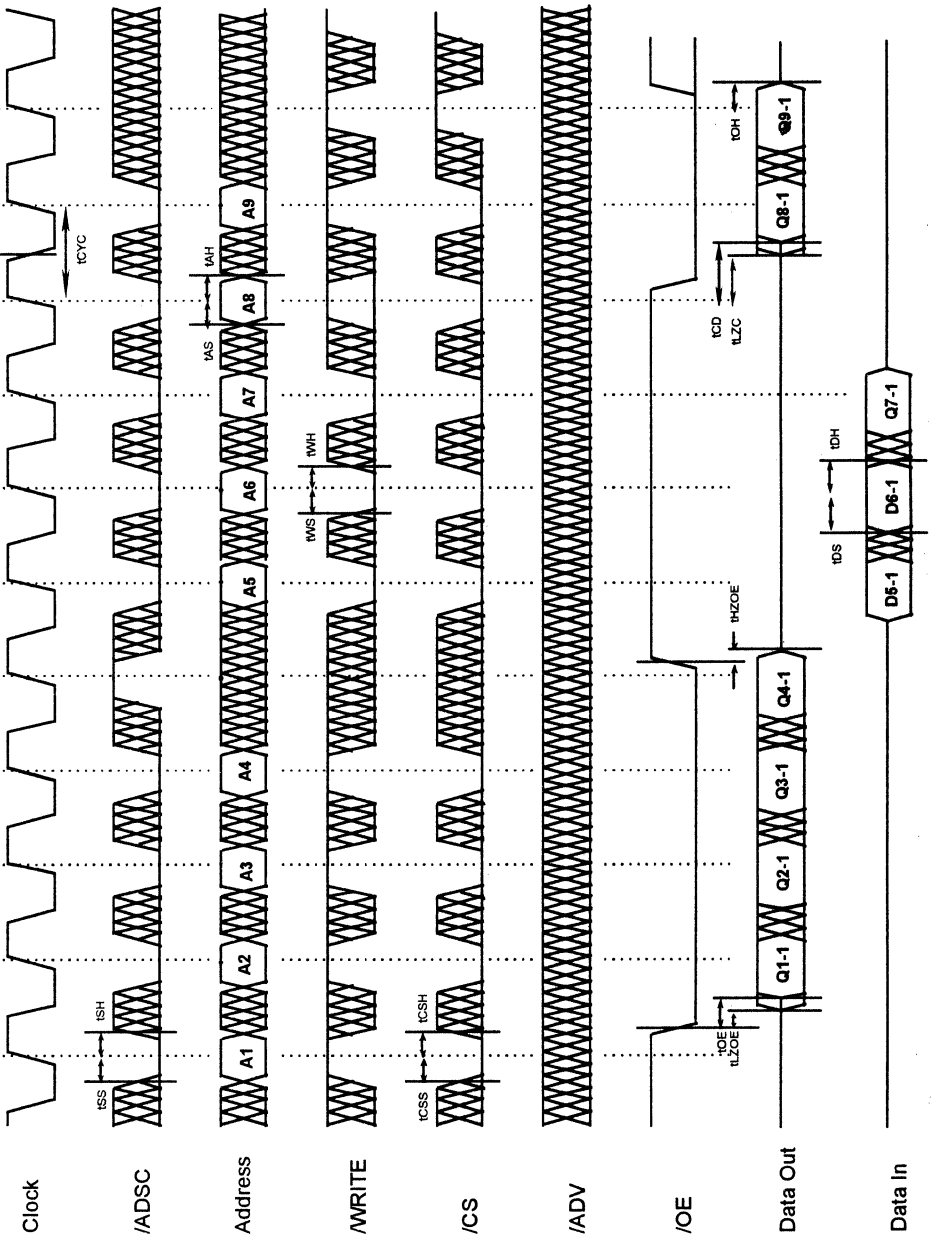
TIMING WAVEFORM OF WRITE CYCLE



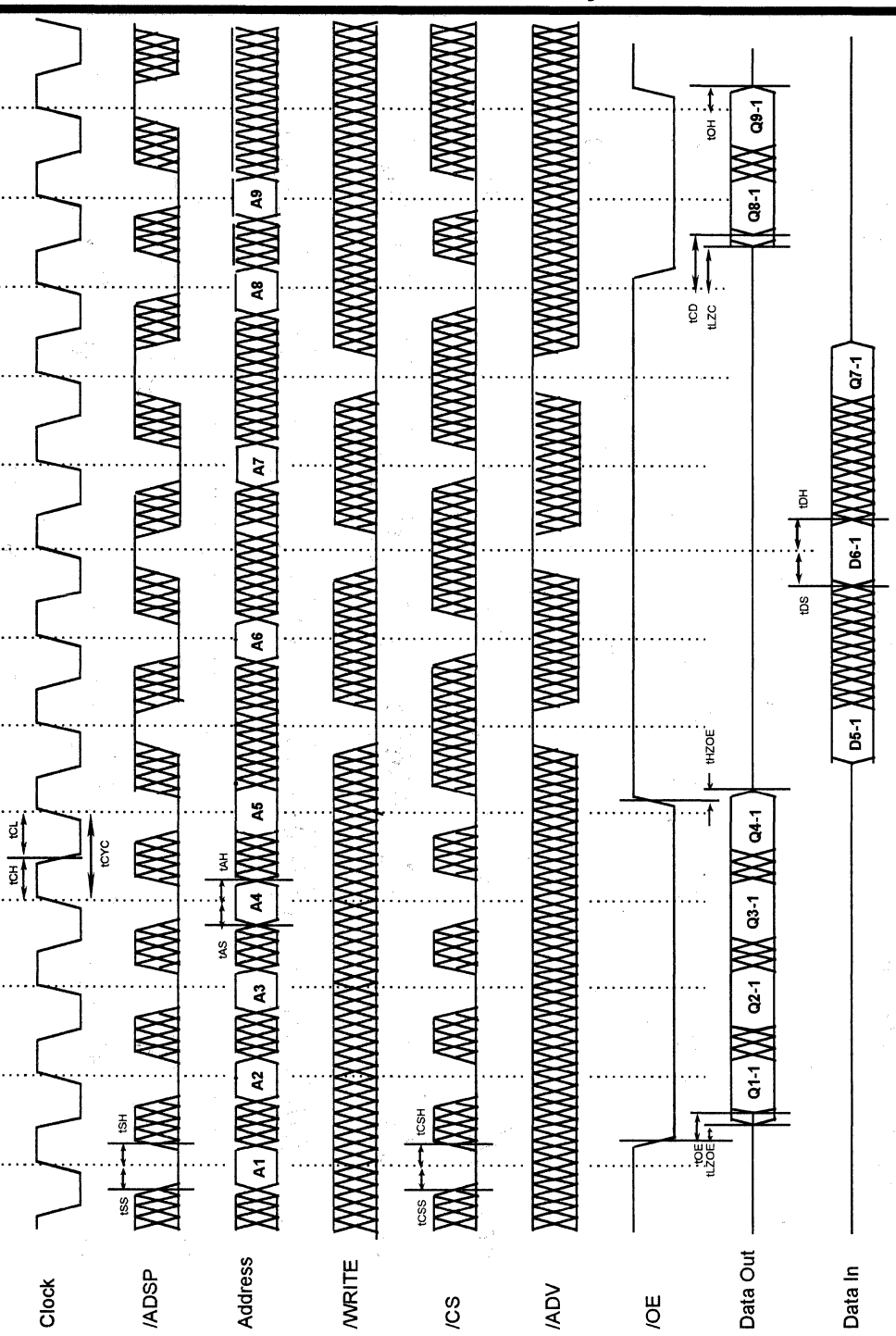
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(/ADSC Controlled)



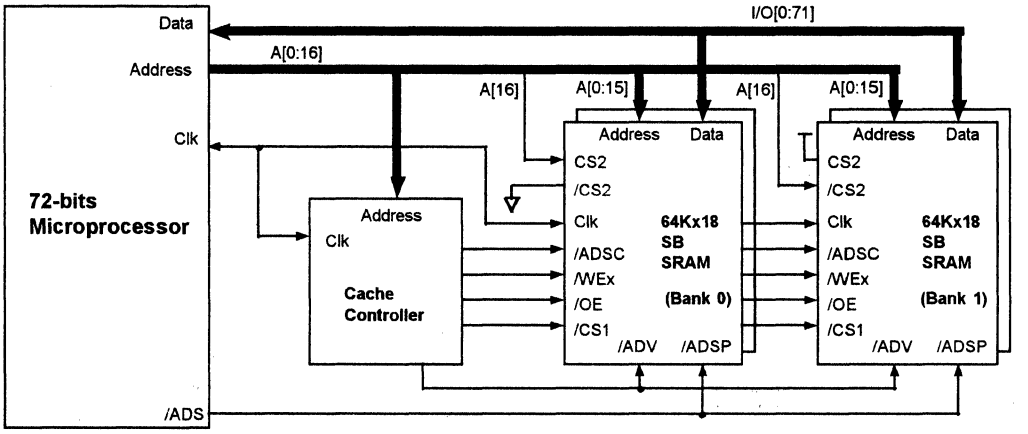
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(/ADSP Controlled)



APPLICATION INFORMATION

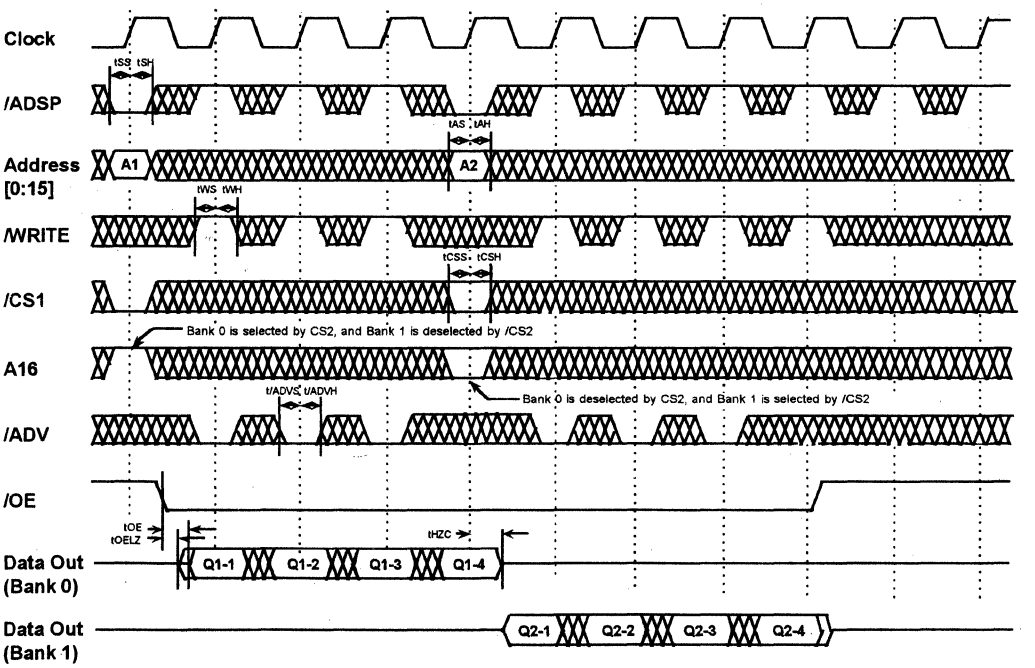
DEPTH EXPANSION

The KM718BV87AT has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING

(Refer to non-interleave write timing for interleave write timing) ;



32K x 32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V-5%/+10% Power Supply.
- 5V tolerant Inputs
- Byte Write Enable Control
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- Transparent Logic Support for 1 or 2 CPU
- TTL-Level Three-State Outputs.
- TTL Compatible Inputs.
- 100-Pin QFP/TQFP Packages .

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	-17	Unit
Cycle Time	tCYC	75	66	60	MHz
Clock Access Time	tCD	7	8	9	ns
Output Enable Access Time	tOE	5	5	5	ns

GENERAL DESCRIPTION

The KM732V588 is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance with advanced i486/Pentium address pipelining. When $\overline{CS1}$ is high, $\overline{ADSP}$ is blocked to control signals.

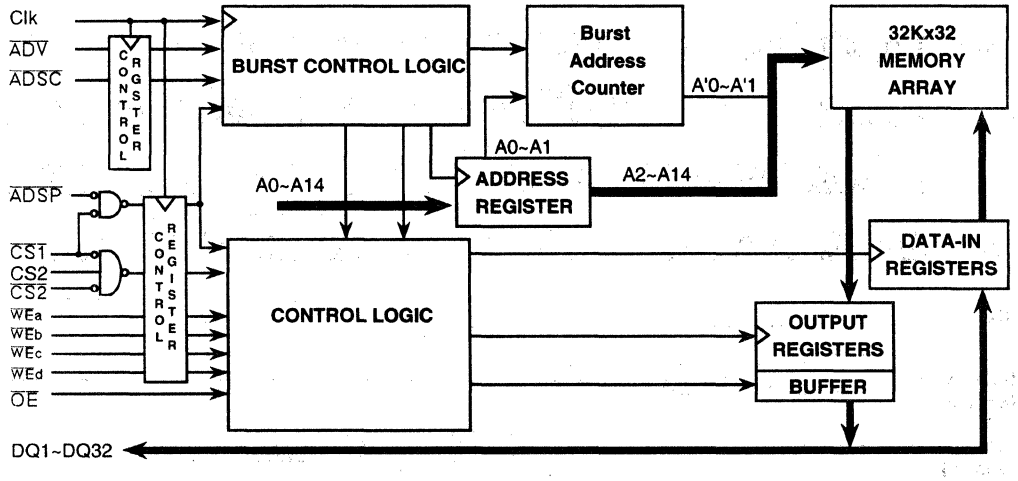
It is organized as 32,768 words of 32 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

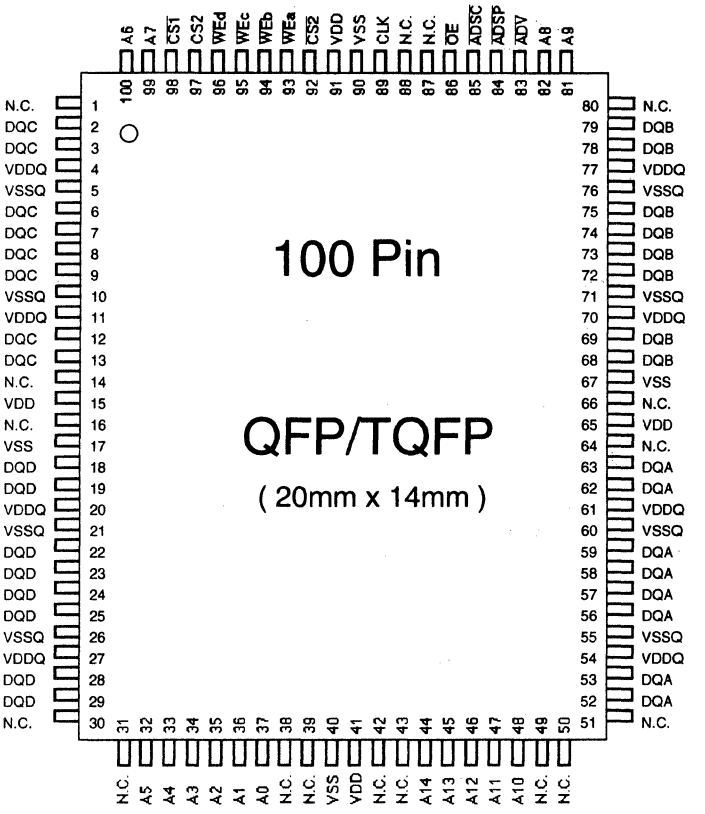
The KM732V588 is fabricated using Samsung's high performance CMOS technology and is available in a 100 pin PQFP package. Multiple power and ground pins are utilized to minimize ground bounce

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	PIN NO.	SYMBOL	PIN NAME	PIN NO.
A0-A14	Address Inputs	32, 33, 34, 35, 36 37, 44, 45, 46, 47 48, 81, 82, 99, 100	NC	No Connect	1, 14, 16, 30, 31, 38 39, 42, 43, 49 ,50 51, 64, 66, 80, 87
$\overline{ADV}$	Burst Address Advance	83			88
$\overline{ADSP}$	Address Status Processor	84	DQ1~	Data Inputs/Outputs	2, 3, 6, 7, 8, 9, 12
$\overline{ADSC}$	Address Status Controller	85	DQ32		13, 18, 19, 22, 23
CLK	Clock	89			24, 25, 28, 29, 52
$\overline{CS1}$	Chip Select	98			53, 56, 57, 58, 59
CS2	Chip Select	97			62, 63, 68, 69, 72
$\overline{CS2}$	Chip Select	92			73, 74, 75, 78, 79
$\overline{WEx}$	Byte Write Enable	93, 94, 95, 96	VDDQ	Output Power Supply	4, 11, 20, 27, 54, 61
$\overline{OE}$	Output Enable	86		(+3.3V)	70, 77
VDD	Power Supply (+3.3V)	15, 41, 65, 91	VSSQ	Output Ground	5, 10, 21, 26, 55,60
VSS	Ground	17, 40, 67, 90			71, 76

FUNCTION DESCRIPTION

The KM732V588 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/Pentium microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of Clk, are carried to the Data-out buffer by the next positive edge of Clk. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled HIGH and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled low. The address increases internally to the next address of burst if both $\overline{WE}$x and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. $\overline{WE}$a controls DQ1~DQ8, $\overline{WE}$b, controls DQ9~DQ16, $\overline{WE}$c controls DQ17~DQ24 and $\overline{WE}$d controls DQ25~DQ32. Read or write cycles (depending on $\overline{WE}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
⬇	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CST}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WEx}$	K	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE 1 : X means "Don't Care"

NOTE 2 : The rising edge of clock is symbolized by ↑

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WEx}$	Operation	$\overline{CST}$	$\overline{WEx}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	L	Initiate Read Cycle Address=An, Data=Qn-1	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	L	No new cycle Data=Qn-1	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, TA=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	V_{DD}=Max; V_{IN}=Vss to V_{DD}		-2	+2	μA
Output Leakage Current	Iol	Output Disabled, V_{OUT}=Vss to V_{DD}		-2	+2	μA
Operating Current	Icc	V_{DD}=Max	75MHz	-	220	mA
		I_{OUT}=0mA	66MHz	-	200	
		Cycle Time ≥ tCYC min	60MHz	-	180	
Standby Current	Isb	Device deselected, I_{OUT}=0mA, Cycle Time ≥ tCYC min All Inputs=Fix (V_{DD}-0.2 or 0.2V)		-	40	mA
	Isb1	Device deselected, I_{OUT}=0mA, Cycle Time =0MHz All Inputs=Fix (V_{DD}-0.2 or 0.2V)		-	20	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5**	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

** In Case of I/O Pins, the Max.Vih=Vcc + 0.5V

CAPACITANCE* (T_A=25°C, f=1Mhz)

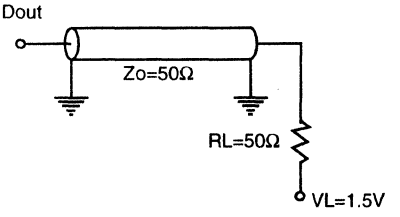
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

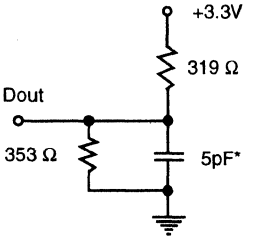
TEST CONDITIONS (T_A=0°C to 70°C, V_{DD}=3.3V-5%/+10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load (A)



Output Load (B)
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, T_A=0°C to +70°C)

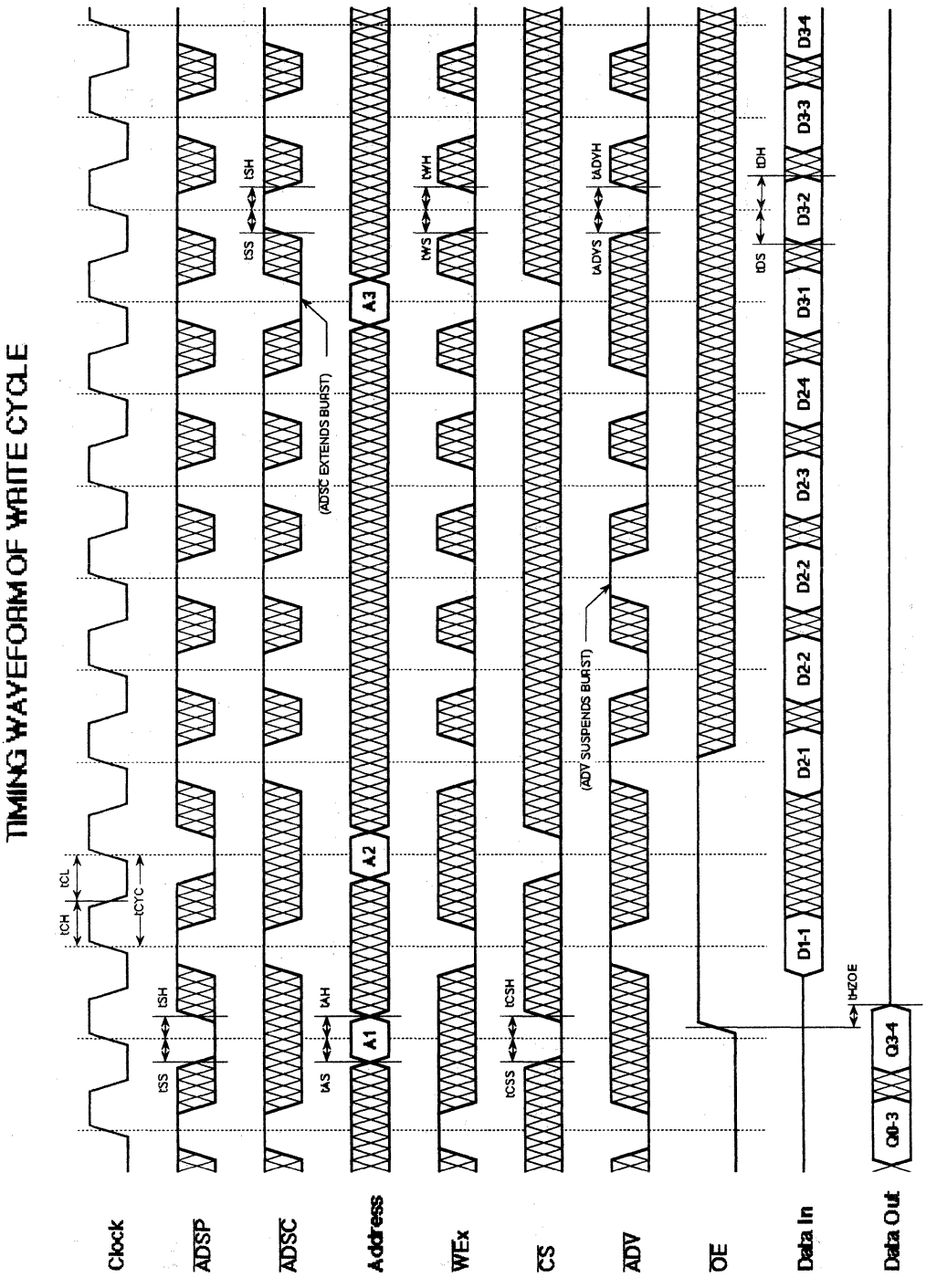
Parameter	Symbol	KM732V588-13		KM732V588-15		KM732V588-17		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	13		15		17		ns
Clock Access Time	tCD		7		8		9	ns
Output Enable to Data Valid	tOE		5		5		5	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	2.5		2.5		2.5		ns
Output Enable Low to Output Low-Z	tLZOE	2		2		2		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	2	6	ns
Clock High to Output High-Z	tHZC		5		6		6	ns
Clock High Pulse Width	tCH	4.5		5.5		6		ns
Clock Low Pulse Width	tCL	4.5		5.5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (Clk) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

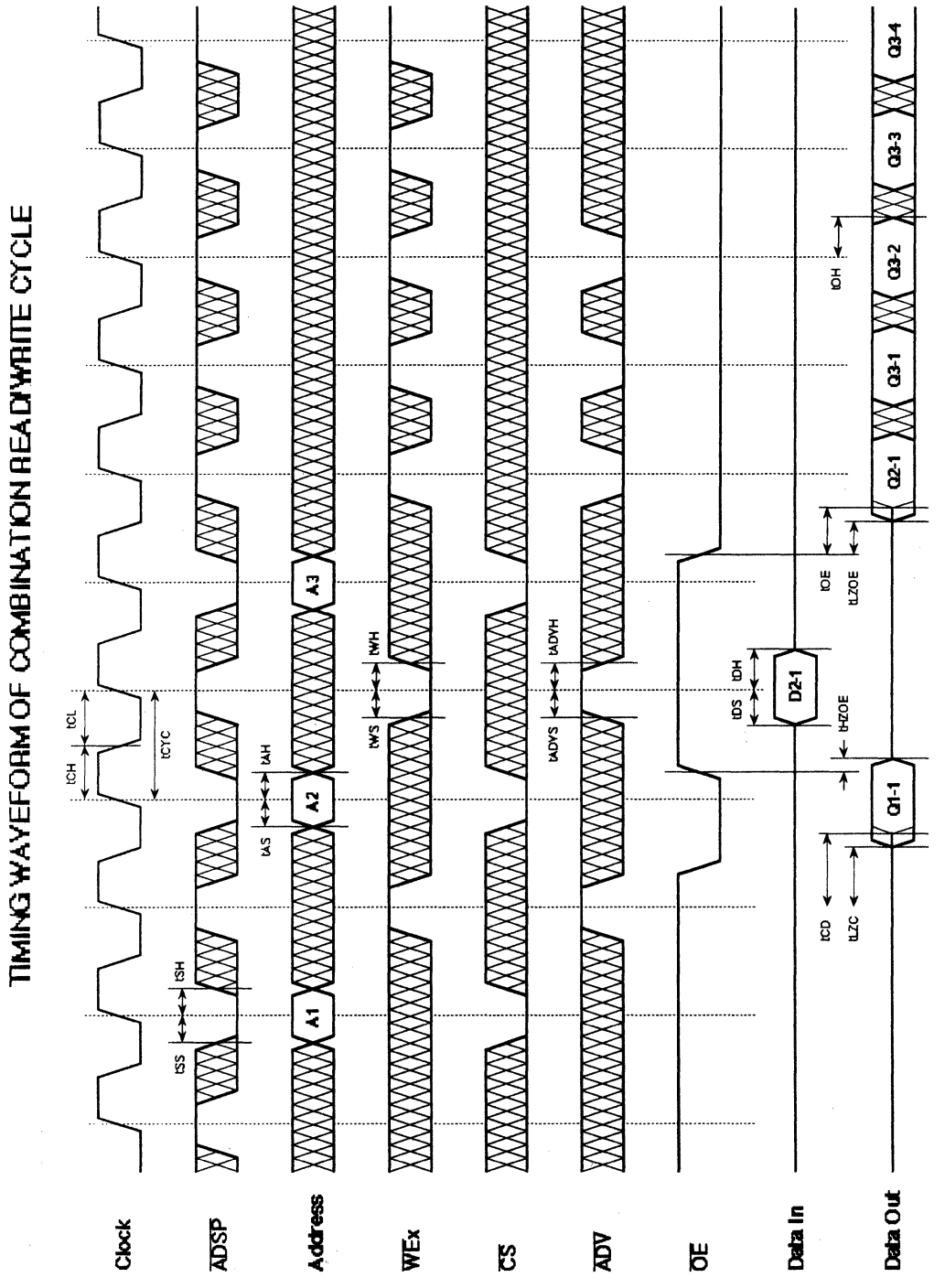
TIMING WAVEFORM OF READ CYCLE

NOTE : The meaning of $\overline{CS}$=Low is $\overline{CS1}$=Low, CS2=High, and $\overline{CS2}$=Low. $\overline{CS}$=High means is $\overline{CS1}$=High or CS2=Low or $\overline{CS2}$=High.

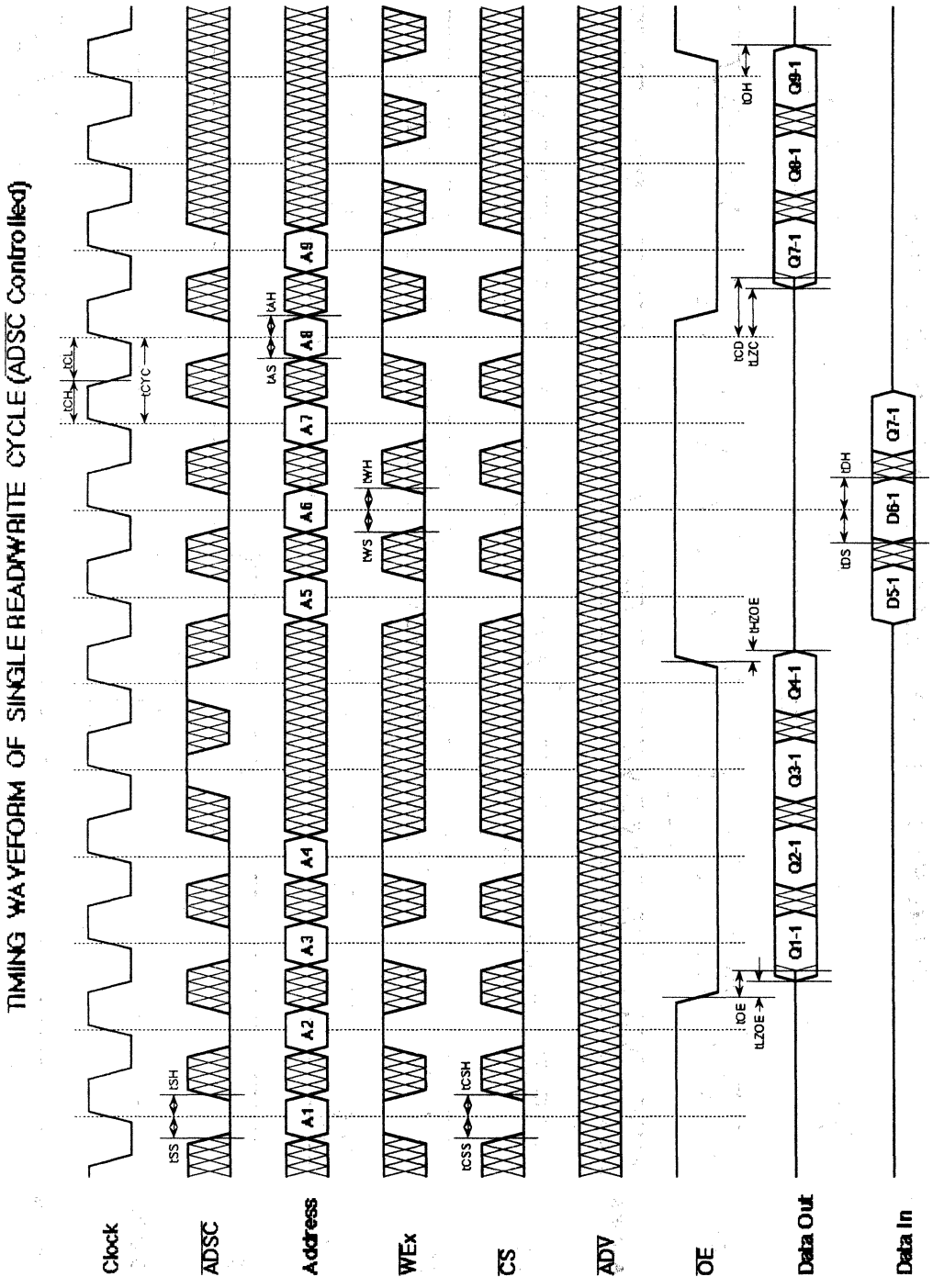
TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE ($\overline{ADSC}$ Controlled)



32K x 32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V-5%/+10% Power Supply.
- 5V Tolerant Inputs except I/O Pins
- Byte Write Enable Control
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable,1 cycle Disable
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 100-Pin QFP /TQFP Package.

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	-17	Unit
Cycle Time	tCYC	75	66	60	MHz
Clock Access Time	tCD	7	8	9	ns
Output Enable Access Time	tOE	6	7	8	ns

GENERAL DESCRIPTION

The KM732V589/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance Second level Cache of i486/Pentium and /Power PC based System.

It is organized as 32,768 words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high perform -ance cache RAM applications; $\overline{GW}$,$\overline{BW}$,$\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous. Full bus-width write is done by $\overline{GW}$,and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is High.

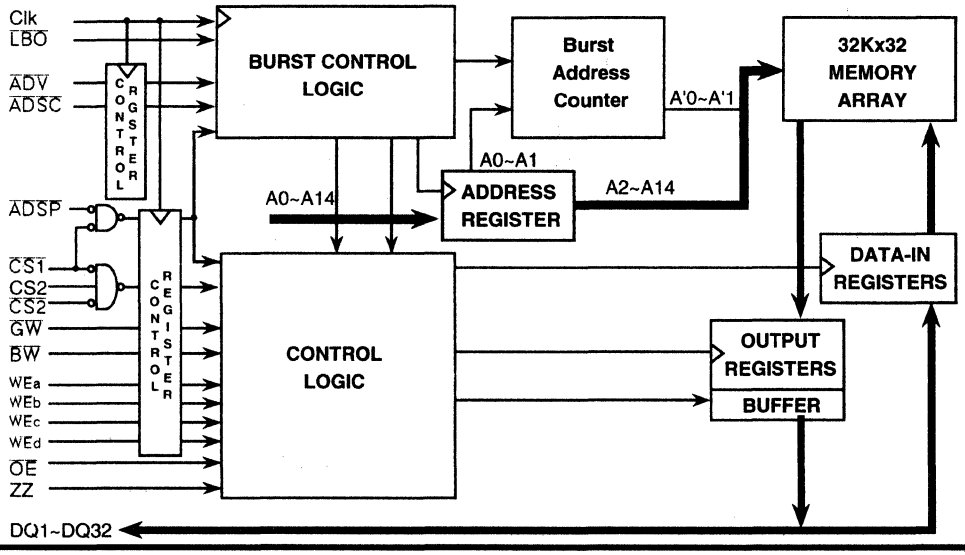
When $\overline{CS1}$ is high, $\overline{ADSP}$ is blocked to control signals. Bursts can be initiate with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

$\overline{LBO}$ Pin is DC operated and determines burst sequence (linear or Interleaved).

ZZ Pin controls Power Down State and reduces Stand by current regardless of CLK.

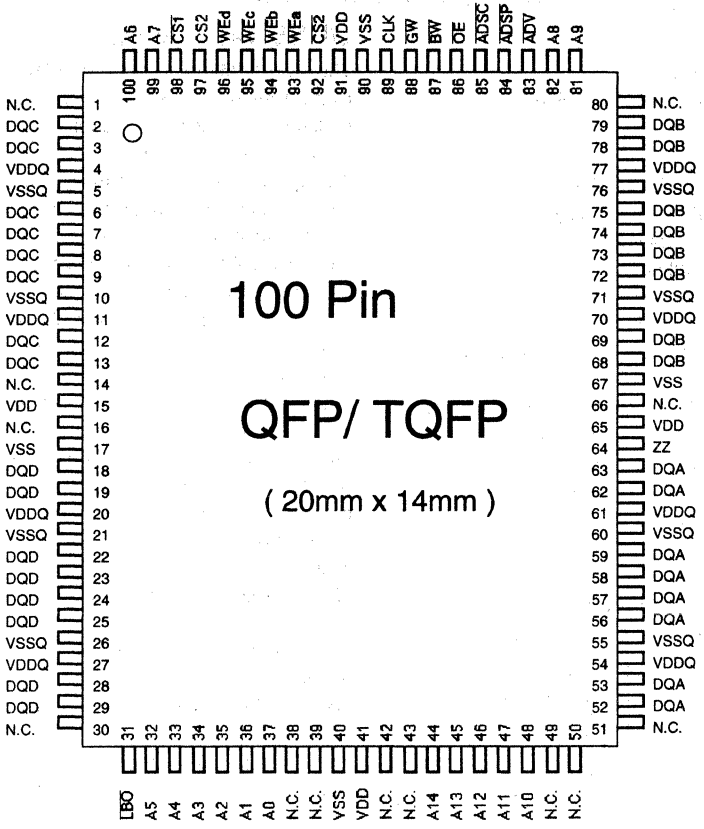
The KM732V589/L is fabricated using Samsung's high performance CMOS technology and is available in 100 pin QFP / TQFP package. Multiple power and ground pins are utilized to minimize ground bounce

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	PIN NO.	SYMBOL	PIN NAME	PIN NO.
A0-A14	Address Inputs	32, 33, 34, 35, 36	VDD	Power Supply (+3.3V)	15, 41, 65, 91
		37, 44, 45, 46, 47	VSS	Ground	17, 40, 67, 90
		48, 81, 82, 99, 100	NC	No Connect	1, 14, 16, 30, 38,39,
$\overline{ADV}$	Burst Address Advance	83			42, 43, 49 ,50, 51,
$\overline{ADSP}$	Address Status Processor	84			66, 80
$\overline{ADSC}$	Address Status Controller	85	DQ1~	Data Inputs/Outputs	2, 3, 6, 7, 8, 9, 12
CLK	Clock	89	DQ32		13, 18, 19, 22, 23
$\overline{CS1}$	Chip Select	98			24, 25, 28, 29, 52
CS2	Chip Select	97			53, 56, 57, 58, 59
$\overline{CS2}$	Chip Select	92			62, 63, 68, 69, 72
$\overline{WE}$x	Byte Write Enable	93, 94, 95, 96			73, 74, 75, 78, 79
$\overline{OE}$	Output Enable	86	VDDQ	Output Power Supply	4, 11, 20, 27, 54, 61
$\overline{GW}$	Global Write Enable	88		(+3.3V)	70, 77
$\overline{BW}$	Byte Write Enable	87	VSSQ	Output Ground	5, 10, 21, 26, 55,60
ZZ	Power Down Input	64			71, 76
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V589/L is a synchronous SRAM designed to support the burst address accessing sequence of the i486/Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ / ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enable signals. Wait states are inserted into the access with $\overline{ADV}$.

During normal operation, ZZ must be pulled LOW. When ZZ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to LOW, the SRAM normally operates after 2 cycles of wake up time.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of Clk, are carried to the Data-out buffer by the next positive edge of Clk. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled HIGH and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$ (regardless of $\overline{BW}$ and $\overline{WE}$x.) ,and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x. when $\overline{GW}$ is High.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled low. The address increases internally to the next address of burst if both $\overline{WE}$x and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. $\overline{WE}$a controls DQ1~DQ8, $\overline{WE}$b, controls DQ9~DQ16, $\overline{WE}$c controls DQ17~DQ24 and $\overline{WE}$d controls DQ25~DQ32. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High , Interleaved burst sequence is selected

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Lenear Burst)

$\overline{LBO}$ pin	Low	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE :
1. $\overline{LBO}$ pin must be tied to High or Low , and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE :

1. X means "Don't Care"
2. The rising edge of clock is symbolized by ↑
3. $\overline{WRITE}$ =L means Write operation in WRITE TRUTH TABLE
   $\overline{WRITE}$ =H means Read operation in WRITE TRUTH TABLE
4. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$)

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE :

1. X means "Don't Care"
2. All inputs in this table must meet setup and hold time around the rising edge of CLK (↑)

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din,High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care"
2. N.C state is Not Allowed.
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An, Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Dn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE

1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2. $\overline{CS2}$ =Low and CS2=High .(Not Deselected)
3. $\overline{ADSC}$ =High when $\overline{CS1}$=High (Not Deselected)
4. $\overline{WRITE}$ = Low means that one or more byte write enable inputs ($\overline{WE}$a, $\overline{WE}$b,$\overline{WE}$c,$\overline{WE}$d) and $\overline{BW}$ are Low or $\overline{GW}$ is High.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, TA=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	V_{IN}=Vss to V_{DD}		-2	+2	μA
Output Leakage Current	Iol	Output Disabled, V_{OUT}=Vss to V_{DD}		-2	+2	μA
Operating Current	Icc	I_{OUT}=0mA , ZZ < VIL	75MHz	-	200	mA
		All Inputs = VIH or VIL	66MHz	-	180	
		Cycle Time ≥ tCYC min	60MHz	-	160	
Standby Current	Isb	Device deselected, I_{OUT}=0mA, ZZ ≤ VIL All Inputs = VIH or VIL, Cycle Time ≥ tCYC min		-	30	mA
	Isb1	Device deselected, ZZ ≤ VIL All Inputs= Fixed(V_{DD}-0.2 or 0.2V)		-	5	mA
		Cycle Time =0 MHz	L-Ver.	-	1	mA
	Isb2	ZZ≥V_{DD}-0.2V All Inputs= V_{DD}-0.2 or 0.2V		-	5	mA
		Cycle Time ≥ tCYC min	L-Ver.	-	200	uA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5 **	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

** In Case of I/O Pins, max. Vih is Vdd +0.5V

CAPACITANCE* (T_A=25°C, f=1Mhz)

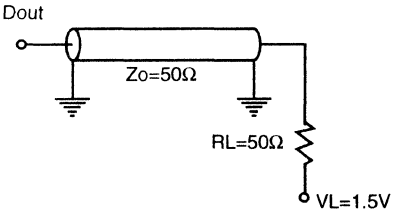
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

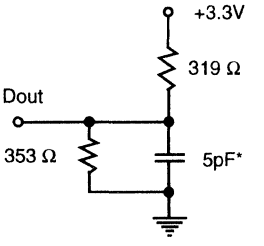
TEST CONDITIONS (T_A=0°C to 70°C, V_{DD}=3.3V-5%/+10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load (A)



Output Load (B)
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, T_A=0°C to +70°C)

Parameter	Symbol	KM732V589-13		KM732V589-15		KM732V589-17		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	13		15		17		ns
Clock Access Time	tCD		7		8		9	ns
Output Enable to Data Valid	tOE		6		7		8	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	2.5		2.5		2.5		ns
Output Enable Low to Output Low-Z	tLZOE	2		2		2		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	2	6	ns
Clock High to Output High-Z	tHZC		7		7		7	ns
Clock High Pulse Width	tCH	4.5		5.5		6		ns
Clock Low Pulse Width	tCL	4.5		5.5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High($\overline{GW}$,$\overline{BW}$,$\overline{WE}$x)	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High($\overline{GW}$,$\overline{BW}$,$\overline{WE}$x)	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns
ZZ High to Power Down	tPDS	2		2		2		cycle
ZZ Low to Power Up	tPUS	2		2		2		cycle

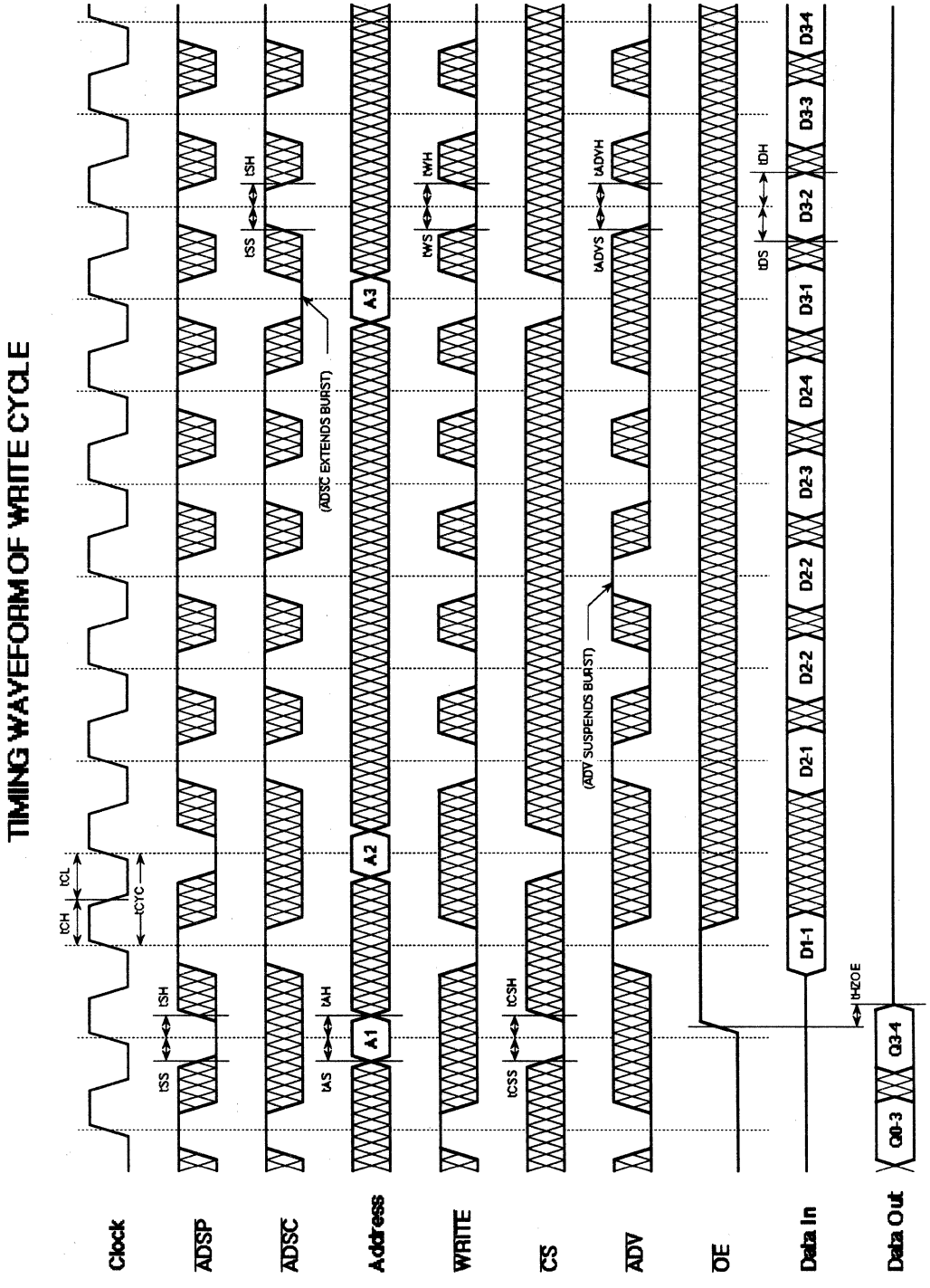
NOTE :

1. All address inputs must meet the specified setup and hold times for all rising clock (Clk) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

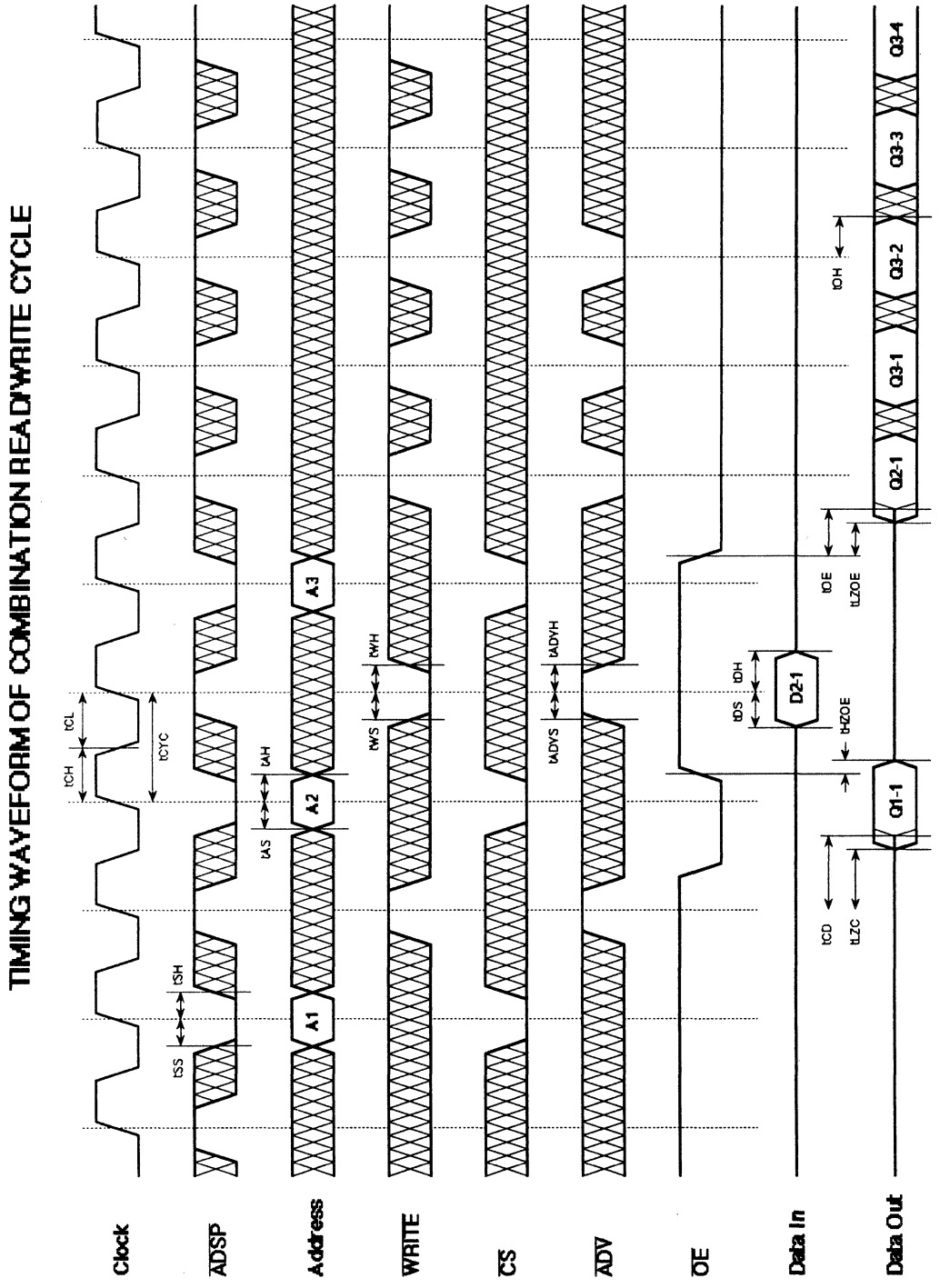
TIMING WAVEFORM OF READ CYCLE

NOTE : The meaning of $\overline{CS}$=Low is $\overline{CS1}$=Low, CS2=High, and $\overline{CS2}$=Low. $\overline{CS}$=High means $\overline{CS1}$=High or CS2=Low or $\overline{CS2}$=High.

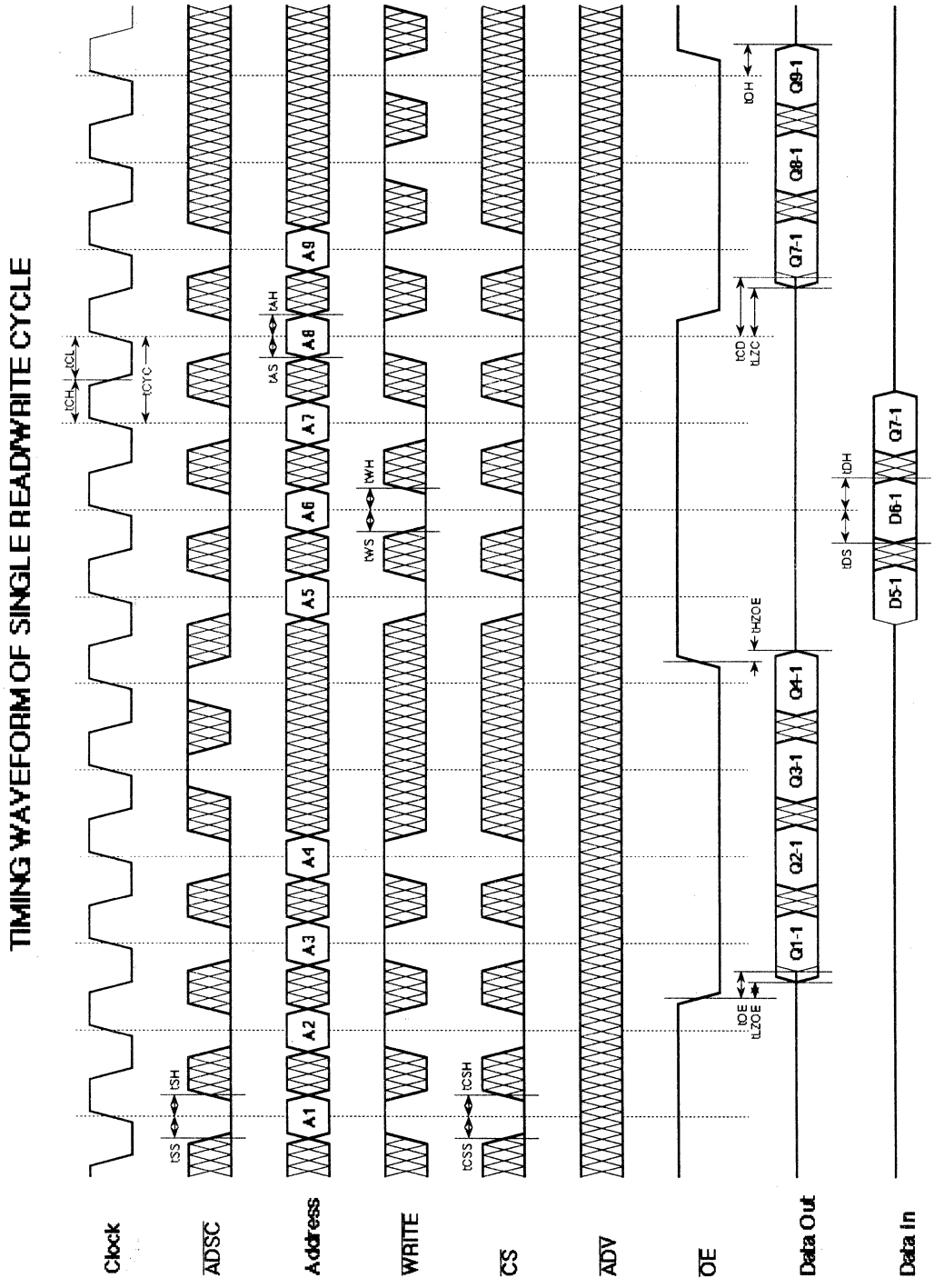
TIMING WAVEFORM OF WRITE CYCLE



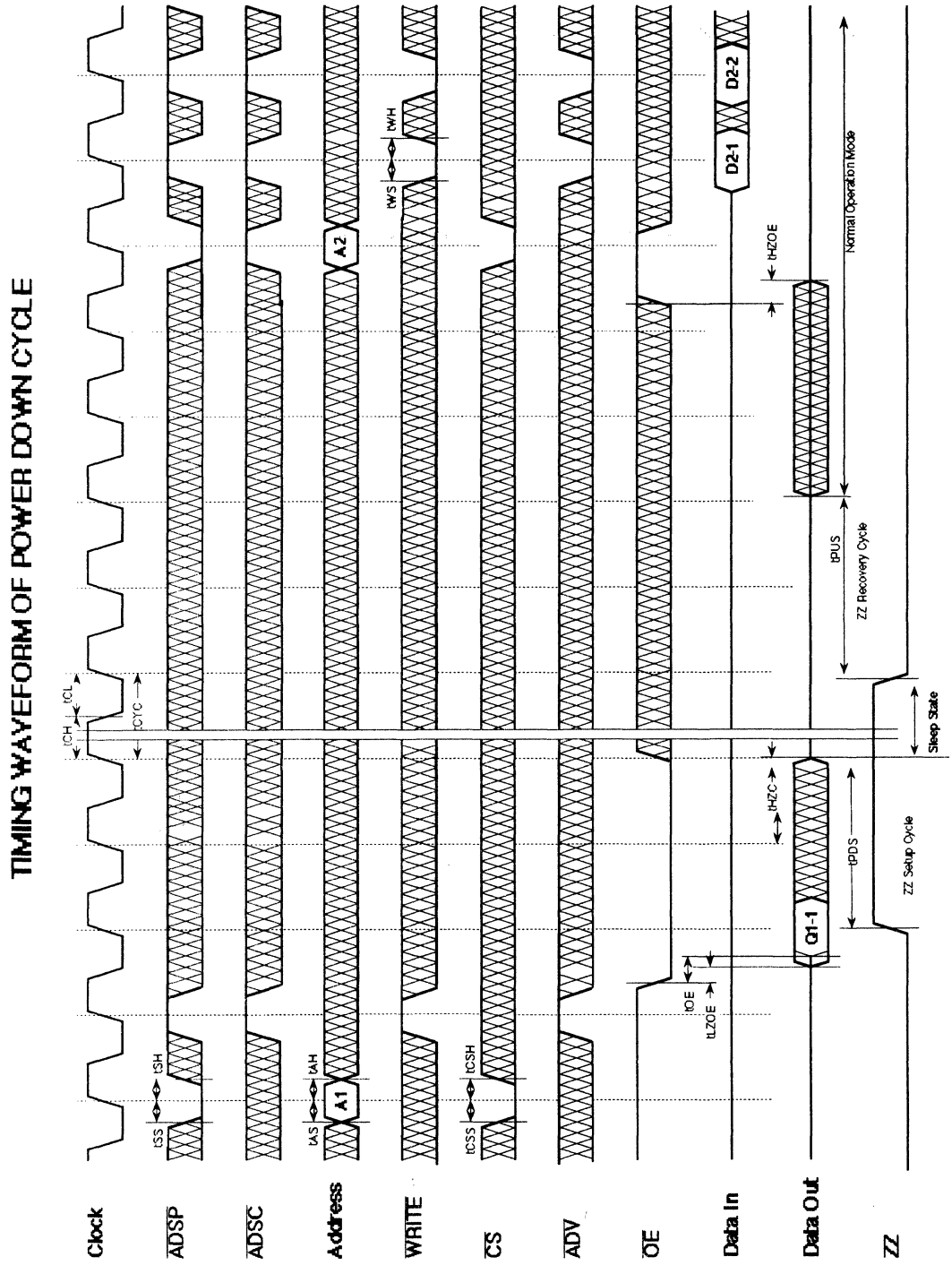
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



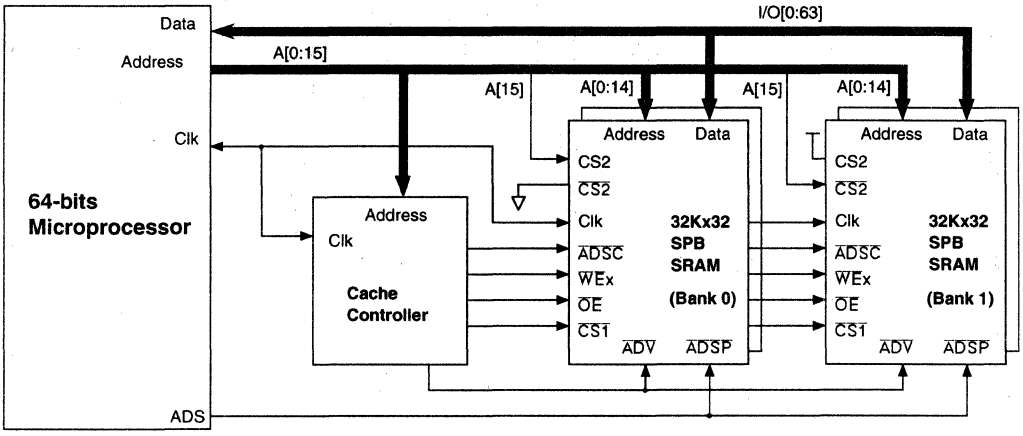
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

DEPTH EXPANSION

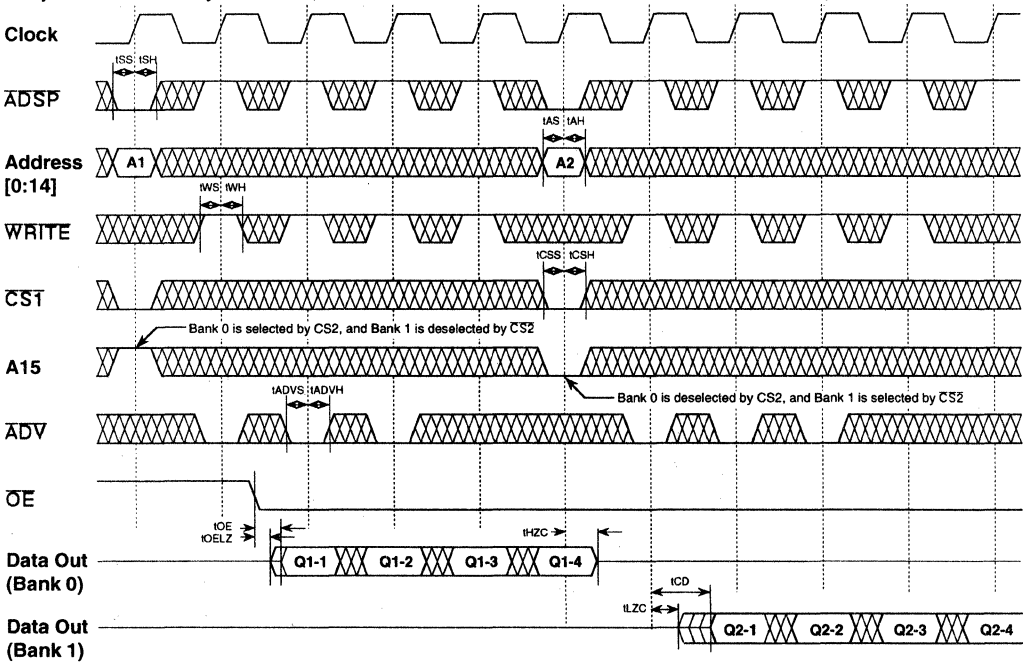
The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING

(Refer to non-interleave write timing for interleave write timing) ;

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



SAMSUNG ELECTRONICS

64K x 16-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V-5%/+10% Power Supply.
- 5V Tolerant Inputs except I/O Pins
- Byte Write Enable Control
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable,1 cycle Disable
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 100-Pin QFP Package.

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	-17	Unit
Cycle Time	tCYC	75	66	60	MHz
Clock Access Time	tCD	7	8	9	ns
Output Enable Access Time	tOE	6	7	8	ns

GENERAL DESCRIPTION

The KM716V689 is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance Second level Cache of i486/Pentium and /Power PC based System.

It is organized as 65,536 words of 16 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high perform -ance cache RAM applications; $\overline{GW}$,$\overline{BW}$,$\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous. Full bus-width write is done by $\overline{GW}$,and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is High.

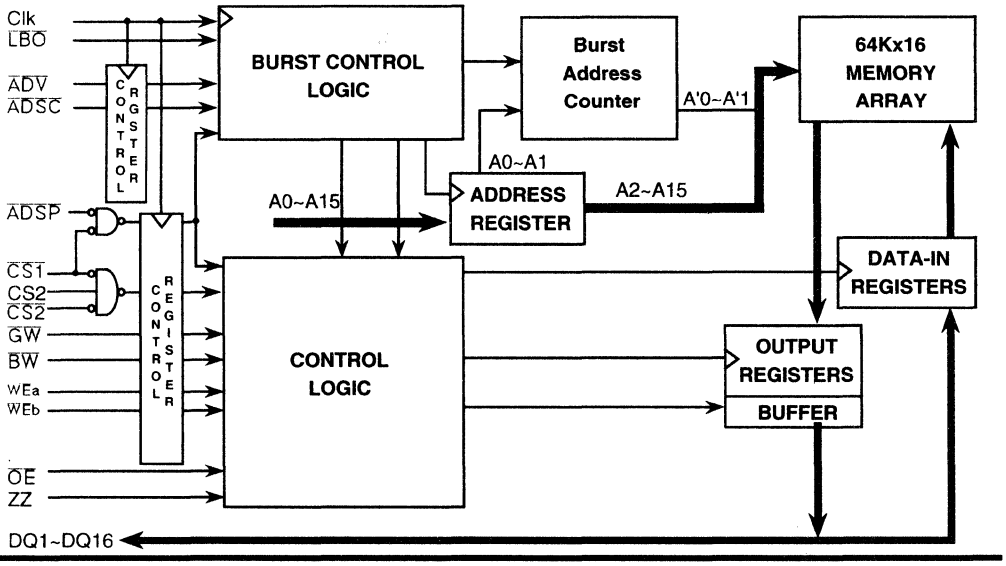
When $\overline{CS1}$ is high, $\overline{ADSP}$ is blocked to control signals. Bursts can be initiate with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

$\overline{LBO}$ Pin is DC operated and determines burst sequence (linear or Interleaved).

ZZ Pin controls Power Down State and reduces Stand by current regardless of CLK.

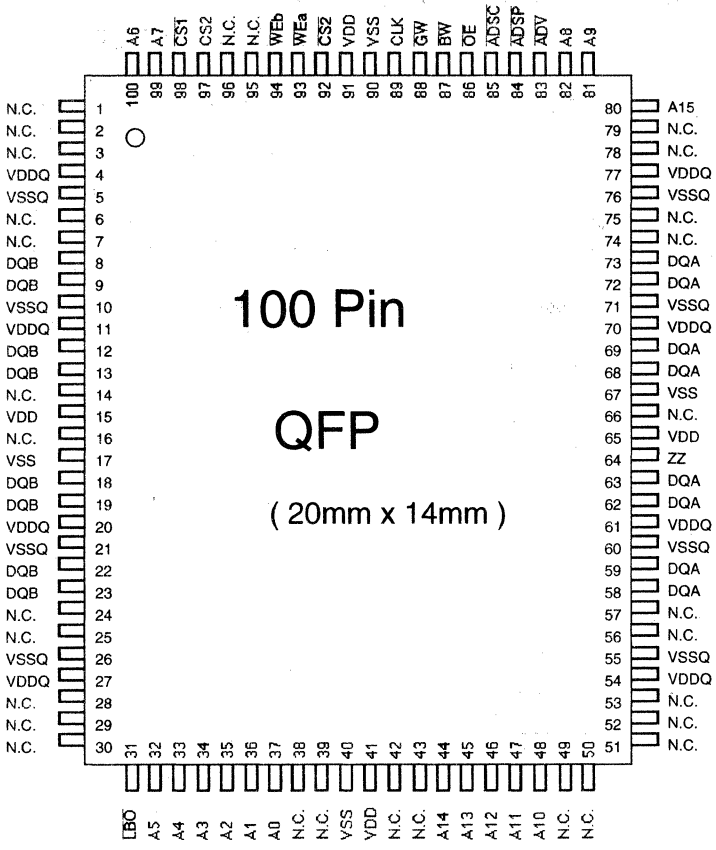
The KM716V689/L is fabricated using Samsung's high performance CMOS technology and is available in 100 pin QFP package. Multiple power and ground pins are utilized to minimize ground bounce

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	PIN NO.	SYMBOL	PIN NAME	PIN NO.
A0-A15	Address Inputs	32, 33, 34, 35, 36 37, 44, 45, 46, 47 48, 80, 81, 82, 99, 100	VDD	Power Supply (+3.3V)	15, 41, 65, 91
			VSS	Ground	17, 40, 67, 90
			NC	No Connect	1,2,3,6,7,14,16,24, 25,28,29,30, 38,39, 42,43,49,50,51,52, 53,56,57,66,74,75, 78, 79,95, 96
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89			
$\overline{CS1}$	Chip Select	98			
CS2	Chip Select	97	DQ1~ DQ16	Data Inputs/Outputs	8,9,12,13,18,19,22, 23, 58, 59 62, 63, 68, 69, 72 ,73
$\overline{CS2}$	Chip Select	92			
$\overline{WEx}$	Byte Write Enable	93, 94,			
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	VDDQ	Output Power Supply (+3.3V)	4, 11, 20, 27, 54, 61 70, 77
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64	VSSQ	Output Ground	5, 10, 21, 26, 55,60 71, 76
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM716V689 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ / ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enable signals. Wait states are inserted into the access with $\overline{ADV}$.

During normal operation, ZZ must be pulled LOW. When ZZ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to LOW, the SRAM normally operates after 2 cycles of wake up time.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of Clk, are carried to the Data-out buffer by the next positive edge of Clk. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled HIGH and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$ (regardless of $\overline{BW}$ and $\overline{WE}$x.) ,and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x. when $\overline{GW}$ is High.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled low. The address increases internally to the next address of burst if both $\overline{WE}$x and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b) sampled low. $\overline{WE}$a controls DQ1~DQ8, $\overline{WE}$b, controls DQ9~DQ16 . Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High , Interleaved burst sequence is selected

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Lenear Burst)

$\overline{LBO}$ pin	Low	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE :
1. $\overline{LBO}$ pin must be tied to High or Low , and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE :

1. X means "Don't Care"
2. The rising edge of clock is symbolized by ↑
3. $\overline{WRITE}$ =L means Write operation in WRITE TRUTH TABLE
   $\overline{WRITE}$ =H means Read operation in WRITE TRUTH TABLE
4. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$)

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	Operation
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

NOTE :

1. X means "Don't Care"
2. All inputs in this table must meet setup and hold time around the rising edge of CLK (↑)

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din,High-Z
Deselected	L	X	High-Z

NOTE

1 . X means "Don't Care"
2 . N.C state is Not Allowed.
3 . For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4 . Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WEx}$	Operation	$\overline{CS1}$	WRITE	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An, Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Dn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE

1 . This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2 . $\overline{CS2}$ =Low and CS2=High .(Not Deselected)
3 . $\overline{ADSC}$ =High when $\overline{CS1}$=High (Not Deselected)
4 . $\overline{WEx}$ = Low means that one or more byte write enable inputs ($\overline{WEa}$, $\overline{WEb}$) and $\overline{BW}$ are Low or $\overline{GW}$ is High.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, TA=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	V_{IN}=Vss to V_{DD}		-2	+2	μA
Output Leakage Current	Iol	Output Disabled, V_{OUT}=Vss to V_{DD}		-2	+2	μA
Operating Current	Icc	I_{OUT}=0mA , ZZ < VIL	75MHz	-	200	mA
		All Inputs = VIH or VIL	66MHz	-	180	
		Cycle Time ≥ tCYC min	60MHz	-	160	
Standby Current	Isb	Device deselected, I_{OUT}=0mA, ZZ ≥ VIL All Inputs = VIH or VIL, Cycle Time ≥ tCYC min		-	30	mA
	Isb1	Device deselected, ZZ ≥ VIL All Inputs= Fixed(V_{DD}-0.2 or 0.2V) Cycle Time =0 MHz		-	5	mA
	Isb2	ZZ≥V_{DD}-0.2V All Inputs= V_{DD}-0.2 or 0.2V Cycle Time ≥ tCYC min		-	5	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5 **	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

** In Case of I/O Pins, max. Vih is Vdd +0.5V

CAPACITANCE* (T_A=25°C, f=1Mhz)

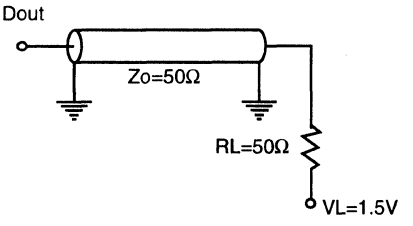
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

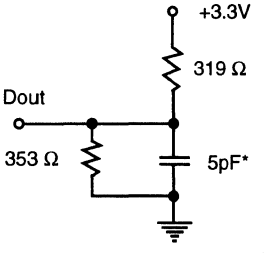
TEST CONDITIONS (T_A=0°C to 70°C, V_{DD}=3.3V-5%/+10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load (A)



Output Load (B)
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Fig. 1

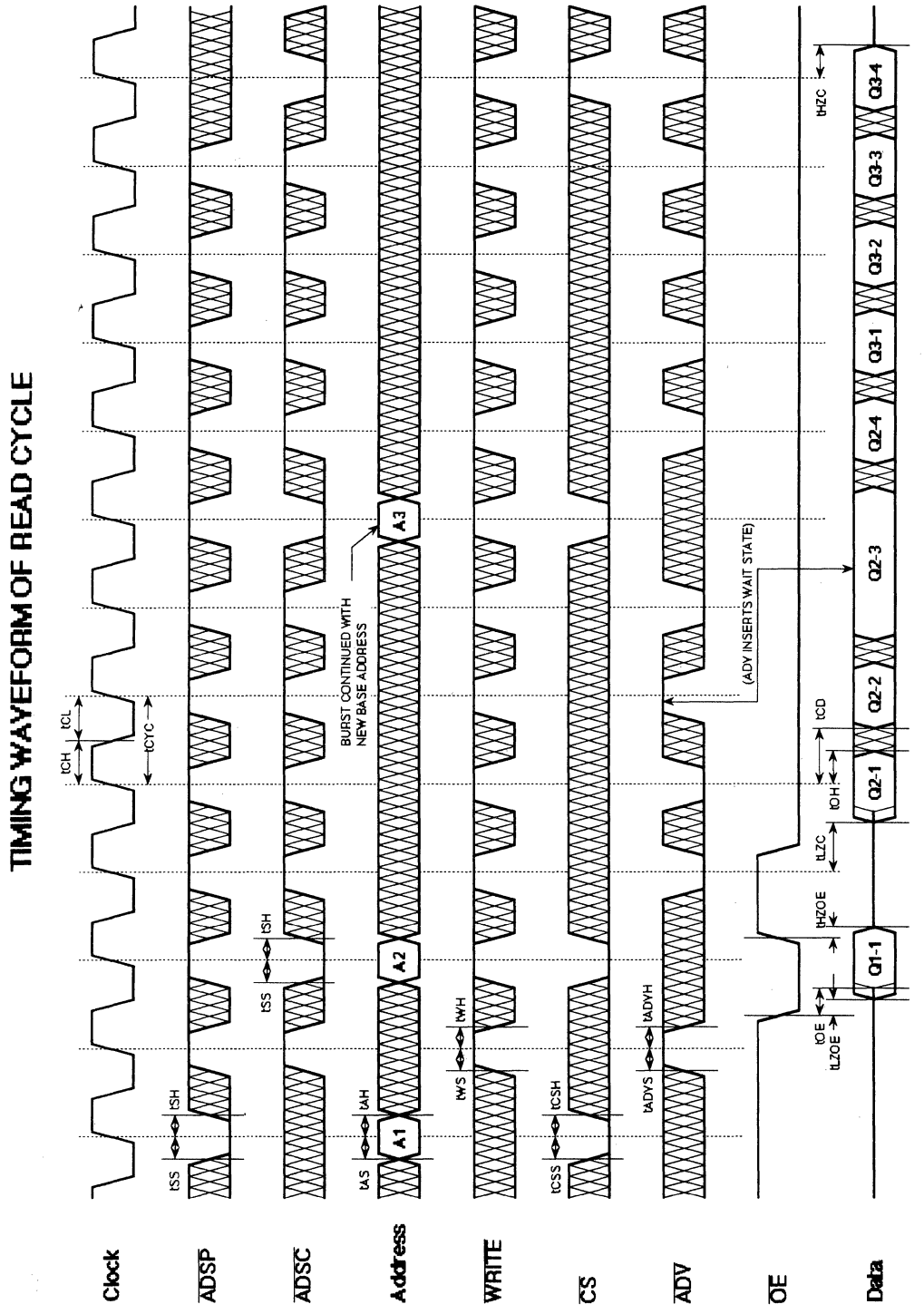
AC TIMING CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, T_A=0°C to +70°C)

Parameter	Symbol	KM716V689-13		KM716V689-15		KM716V689-17		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	13		15		17		ns
Clock Access Time	tCD		7		8		9	ns
Output Enable to Data Valid	tOE		6		7		8	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	2		2		2		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	2	6	ns
Clock High to Output High-Z	tHZC		7		7		7	ns
Clock High Pulse Width	tCH	4.5		5.5		6		ns
Clock Low Pulse Width	tCL	4.5		5.5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High($\overline{GW}$,$\overline{BW}$,$\overline{WE}$x)	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High($\overline{GW}$,$\overline{BW}$,$\overline{WE}$x)	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns
ZZ High to Power Down	tPDS	2		2		2		cycle
ZZ Low to Power Up	tPUS	2		2		2		cycle

NOTE :

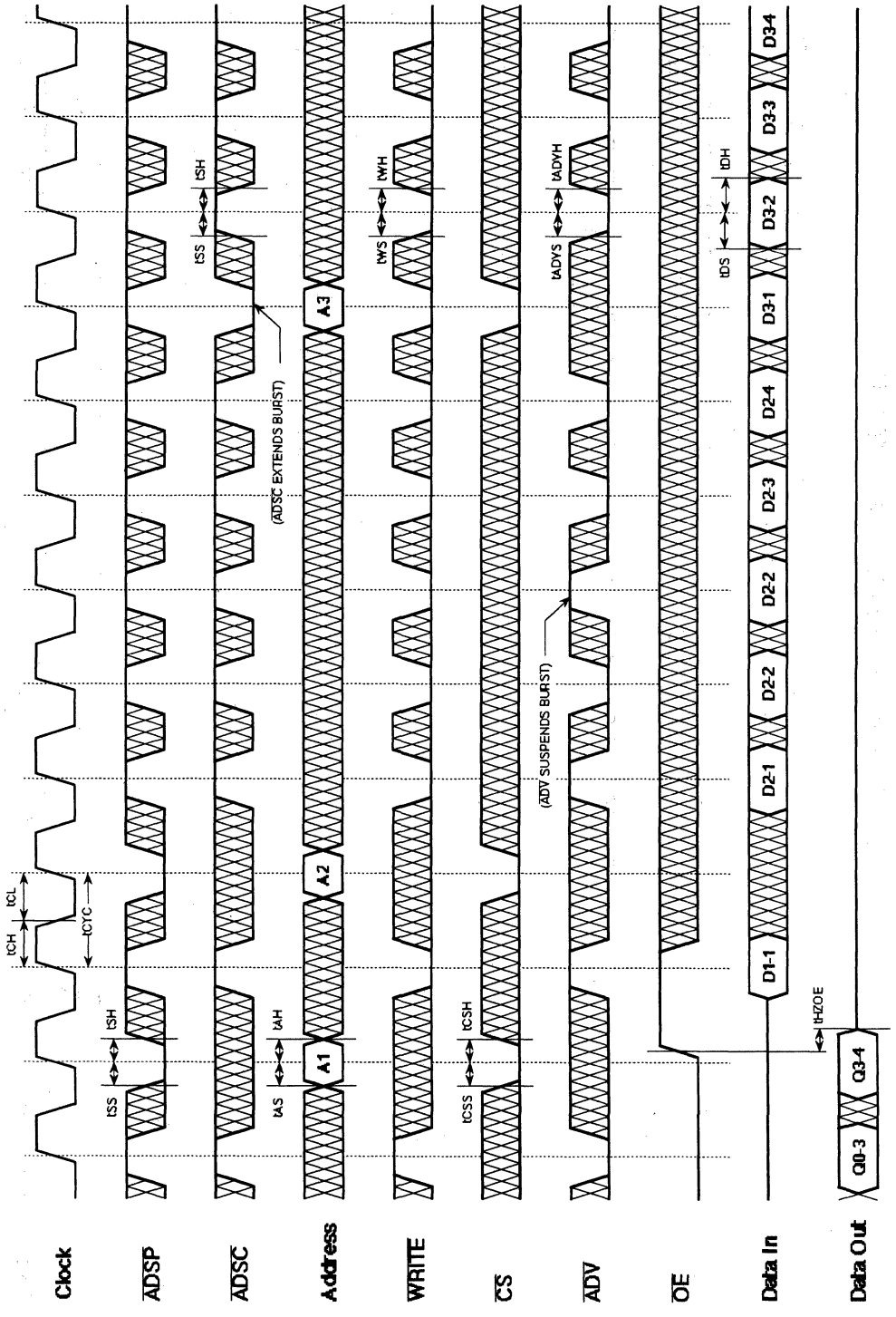
1. All address inputs must meet the specified setup and hold times for all rising clock (Clk) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE

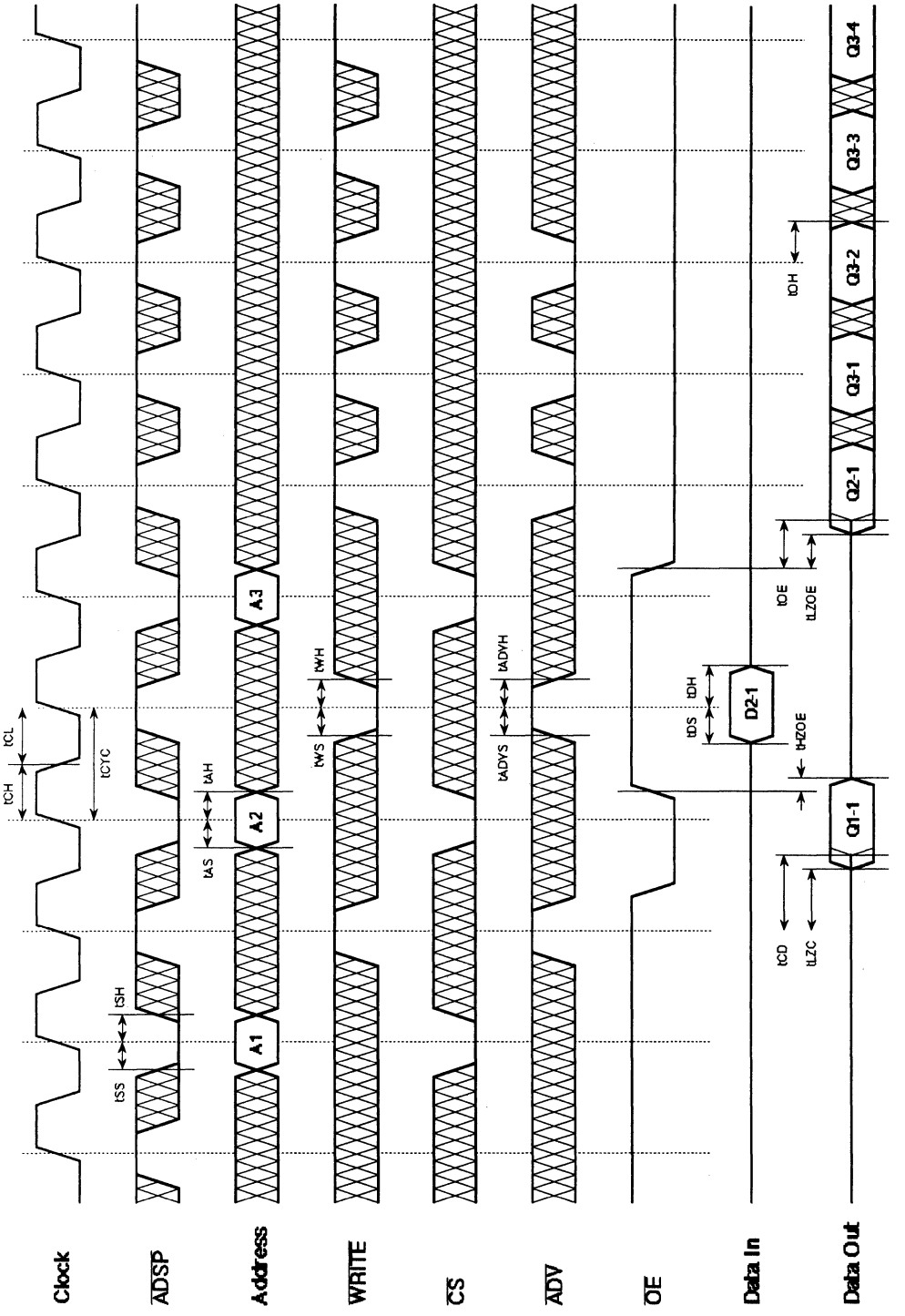


NOTE : The meaning of $\overline{CS}$=Low is $\overline{CS1}$=Low, CS2=High, and $\overline{CS2}$=Low. $\overline{CS}$=High means $\overline{CS1}$=High or CS2=Low or $\overline{CS2}$=High.

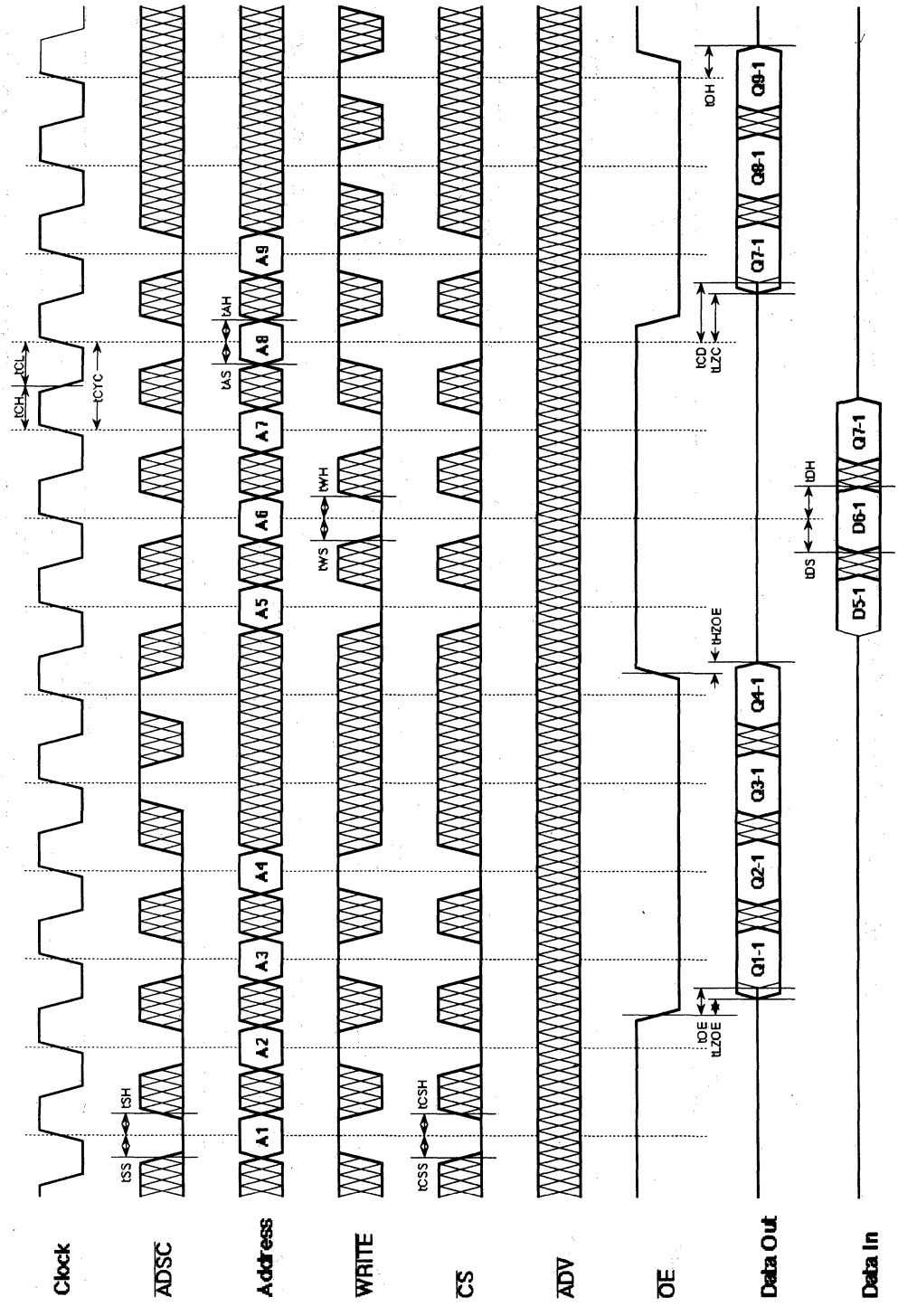
TIMING WAVEFORM OF WRITE CYCLE



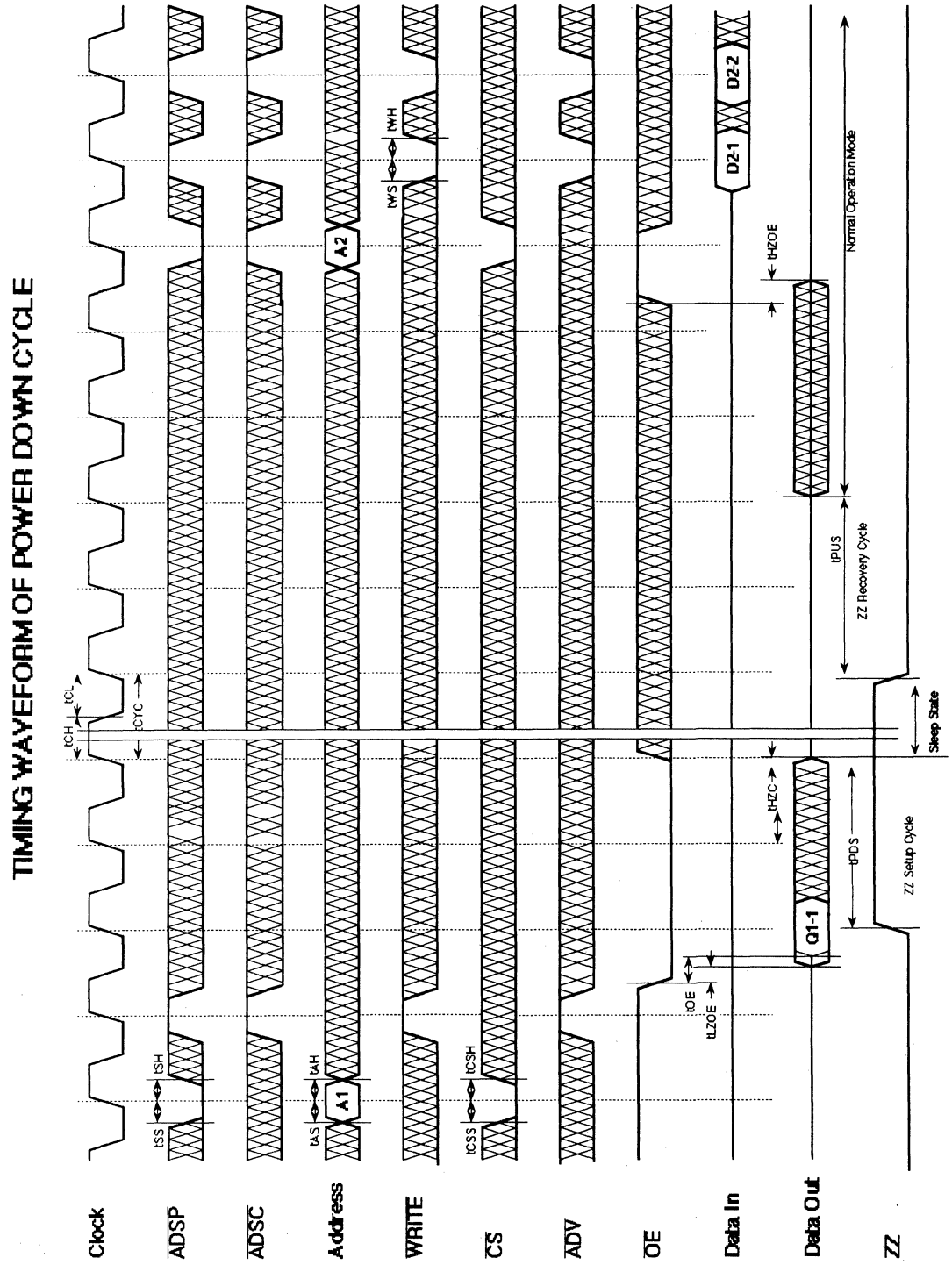
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



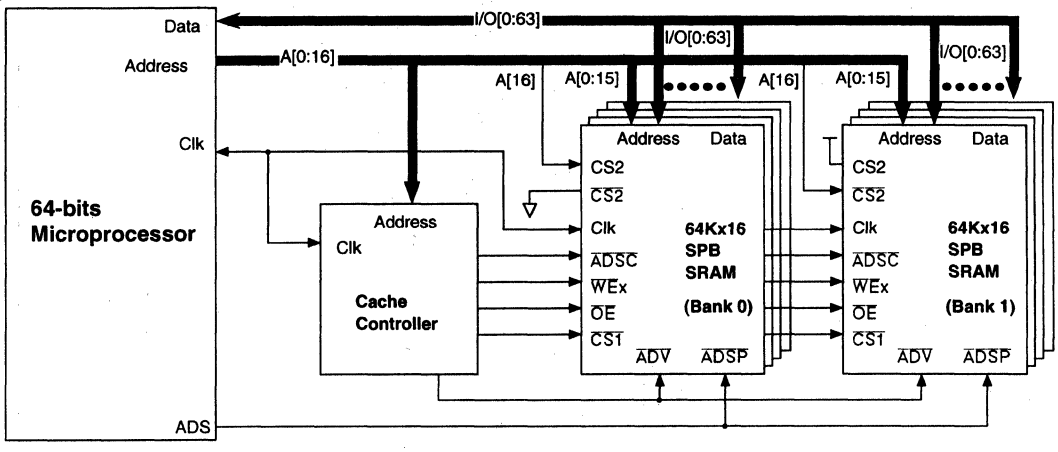
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

DEPTH EXPANSION

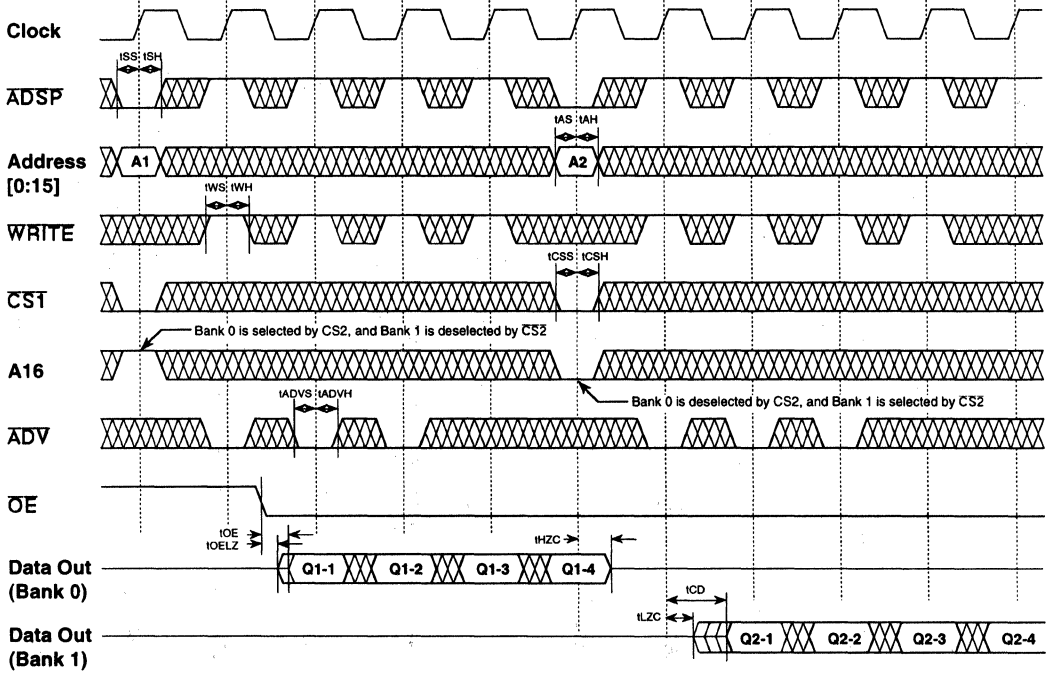
The Samsung 64Kx16 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING

(Refer to non-interleave write timing for interleave write timing) ;

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



64K x 36-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Core Supply Voltage : 3.3V±5%
- I/O Supply Voltage : 2.5V+0.4V/-0.13V
- Byte Write Enable Control
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable,1 cycle Disable
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 100-Pin QFP Package.

FAST ACCESS TIMES

Parameter	Symbol	-7.5	-8.6	-10	Unit
Cycle Time	tCYC	133	117	100	MHz
Clock Access Time	tCD	4.5	5.0	5.5	ns
Output Enable Access Time	tOE	4.5	5.0	5.5	ns

GENERAL DESCRIPTION

The KM732V695/L is a 2,359,296-bit Synchronous Static Random Access Memory designed for high performance Second level Cache of P6 and Power PC based System.

It is organized as 65,536 words of 36 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high perform -ance cache RAM applications; $\overline{GW}$,$\overline{BW}$,$\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous. Full bus-width write is done by $\overline{GW}$,and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is High.

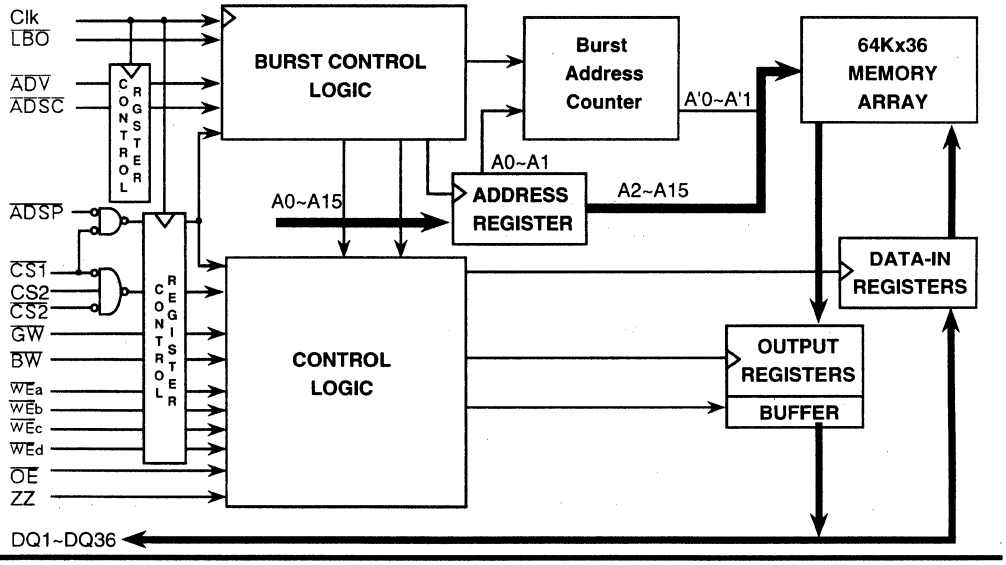
When $\overline{CS1}$ is high, $\overline{ADSP}$ is blocked to control signals. Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

$\overline{LBO}$ Pin is DC operated and determines burst sequence (linear or Interleaved).

ZZ Pin controls Power Down State and reduces Stand by current regardless of CLK.

The KM736V695/L is fabricated using Samsung's high performance CMOS technology and is available in a 100 pin QFP package. Multiple power and ground pins are utilized to minimize ground bounce

LOGIC BLOCK DIAGRAM



64K x 36-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V±5% Power Supply.
- 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention
- TTL-Level Three-State Outputs.
- 100-Pin TQFP Package.

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	10	15	17	ns
Clock Access Time	tCD	8	9	10	ns
Output Enable Access Time	tOE	5	5	5	ns

GENERAL DESCRIPTION

The KM736V687 is a 2,359,296 bit Synchronous Static Random Access Memory designed to support zero wait state performance with advanced i486/Pentium address pipelining.

When $\overline{CS1}$ is high, $\overline{ADSP}$ is blocked to control signals.

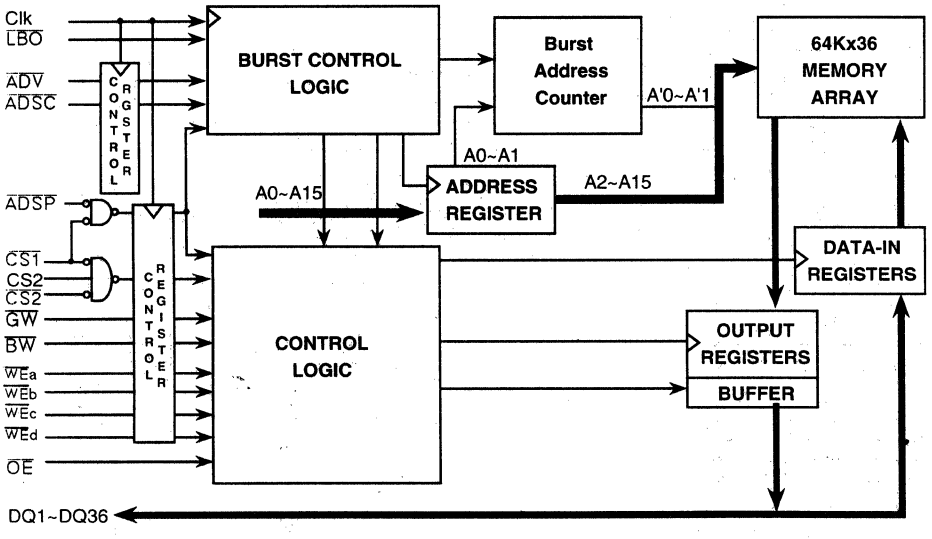
It is organized as 65,536 words of 36 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

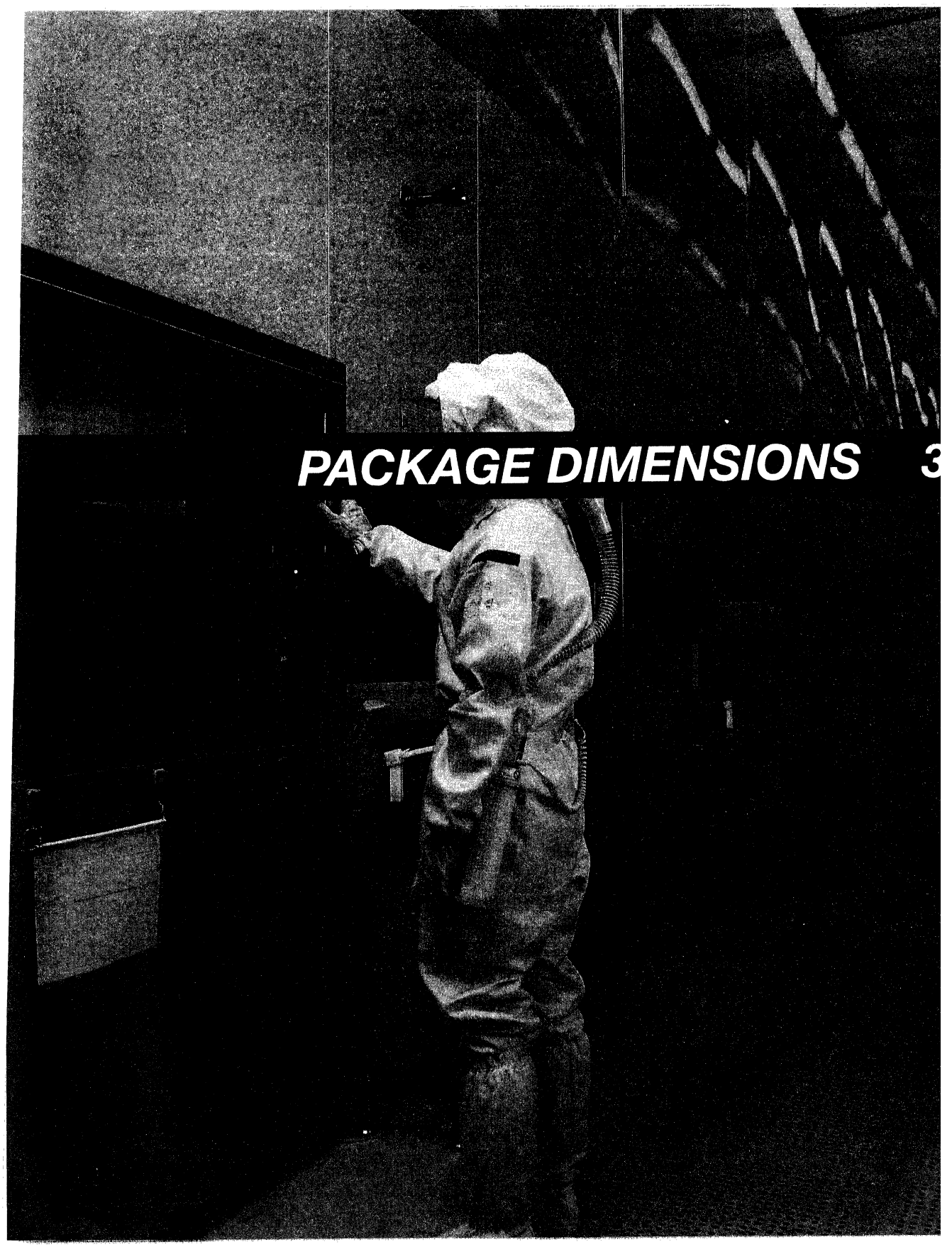
Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM736V687 is implemented in Samsung's high performance CMOS technology and is available in a 100 pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce

LOGIC BLOCK DIAGRAM



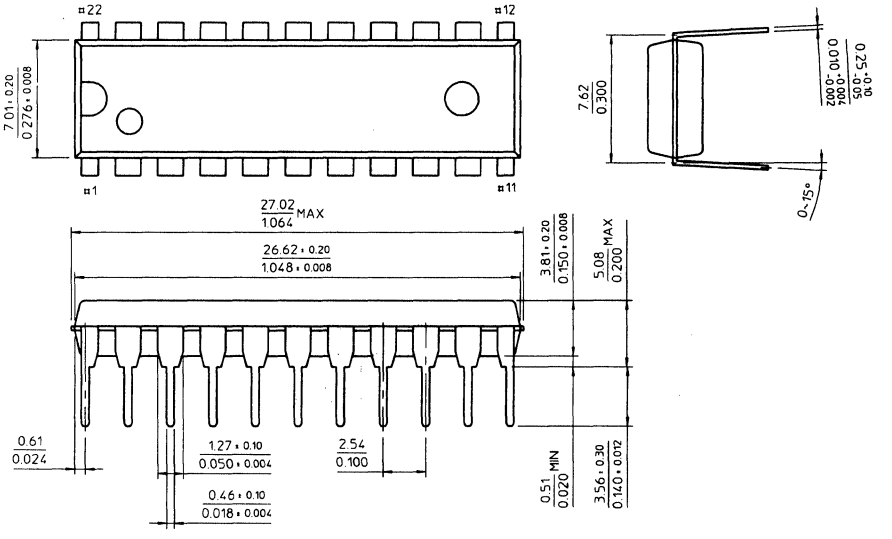


PACKAGE DIMENSIONS 3

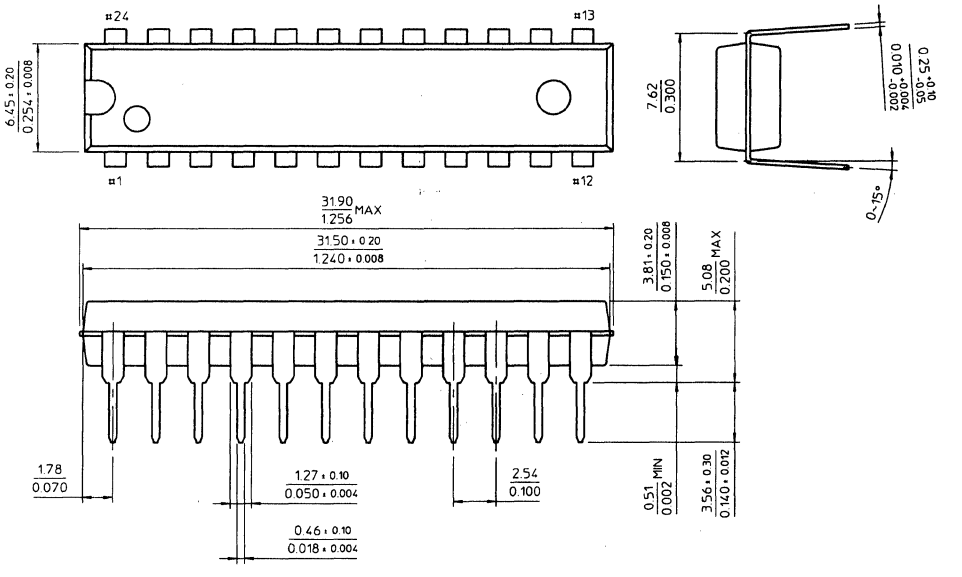
PACKAGE DIMENSIONS

Unit : mm/inch

22-DIP-300B



24-DIP-300



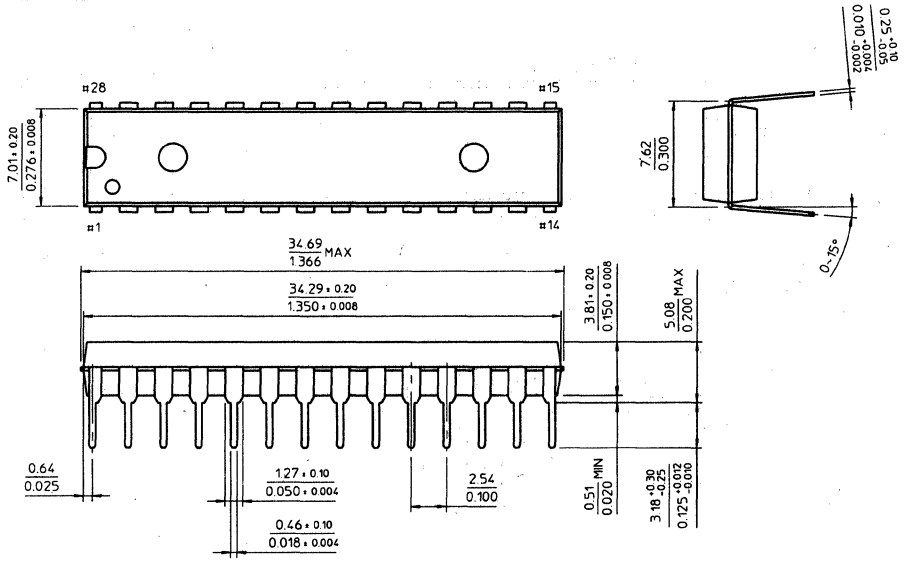
3

SAMSUNG ELECTRONICS

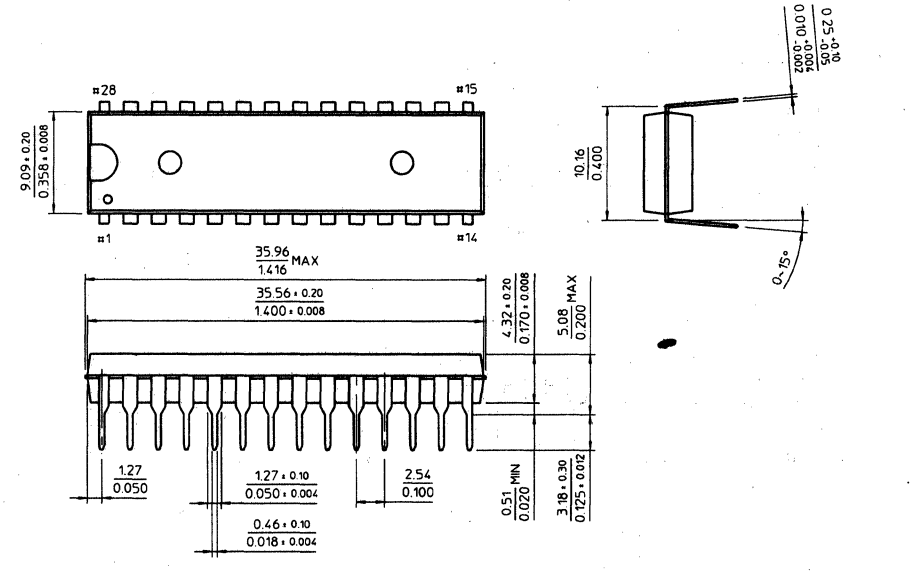
PACKAGE DIMENSIONS

Unit : mm/inch

28-DIP-300



28-DIP-400

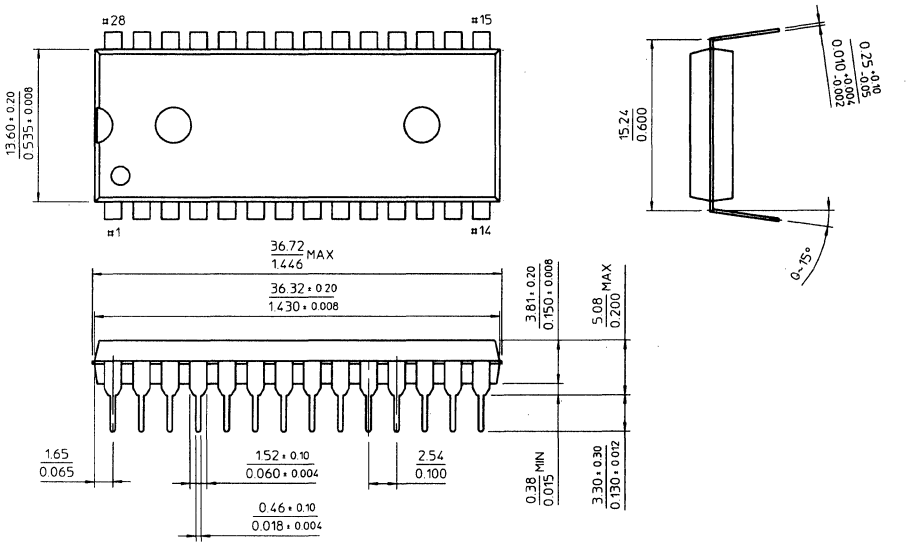


SAMSUNG ELECTRONICS

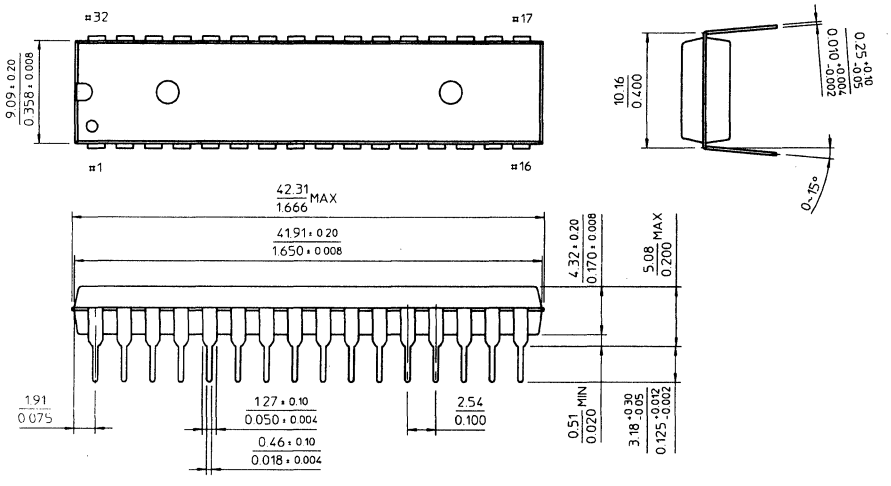
PACKAGE DIMENSIONS

Unit : mm/inch

28-DIP-600B



32-DIP-400

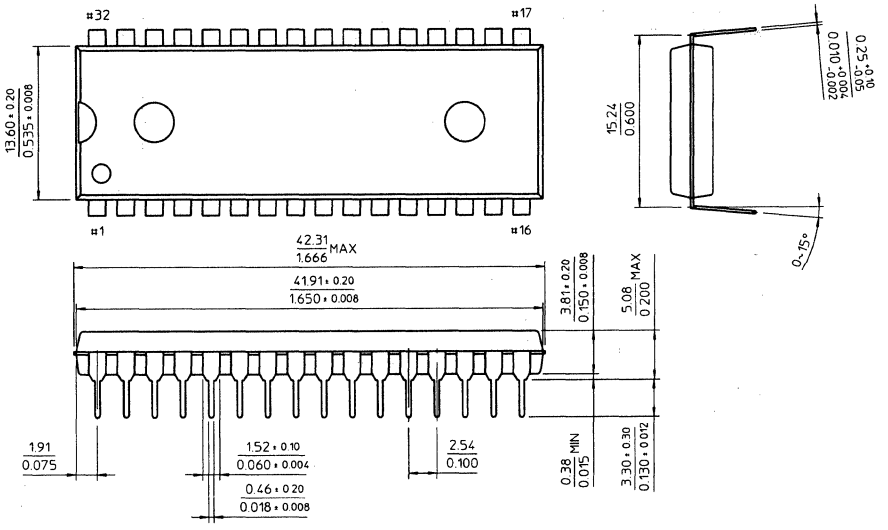


3

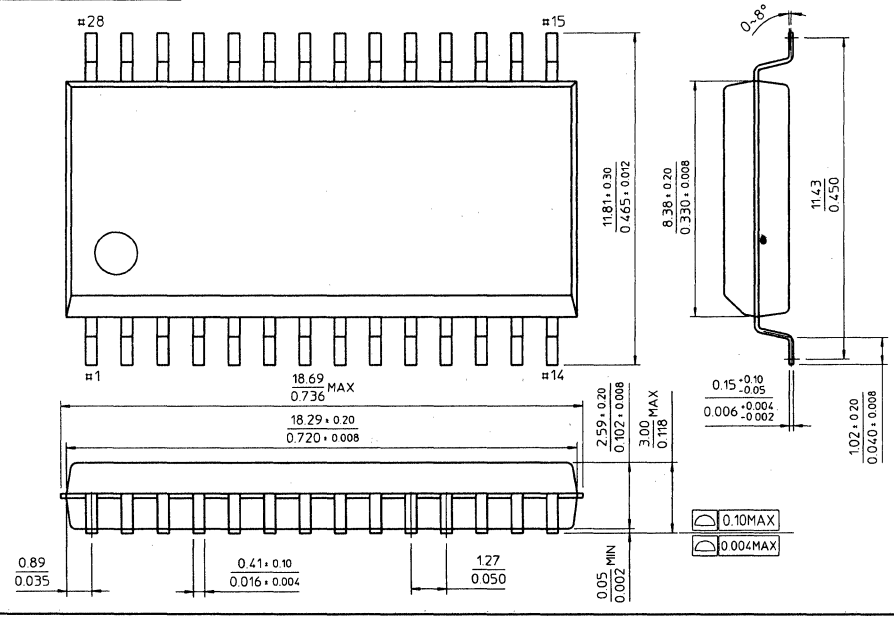
PACKAGE DIMENSIONS

Unit : mm/inch

32-DIP-600



28-SOP-450

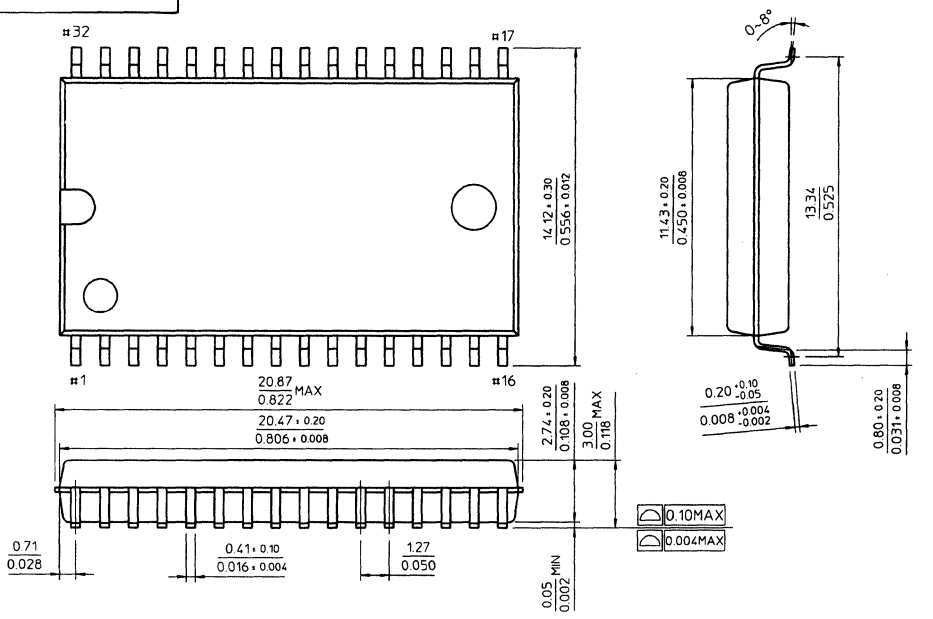


SAMSUNG ELECTRONICS

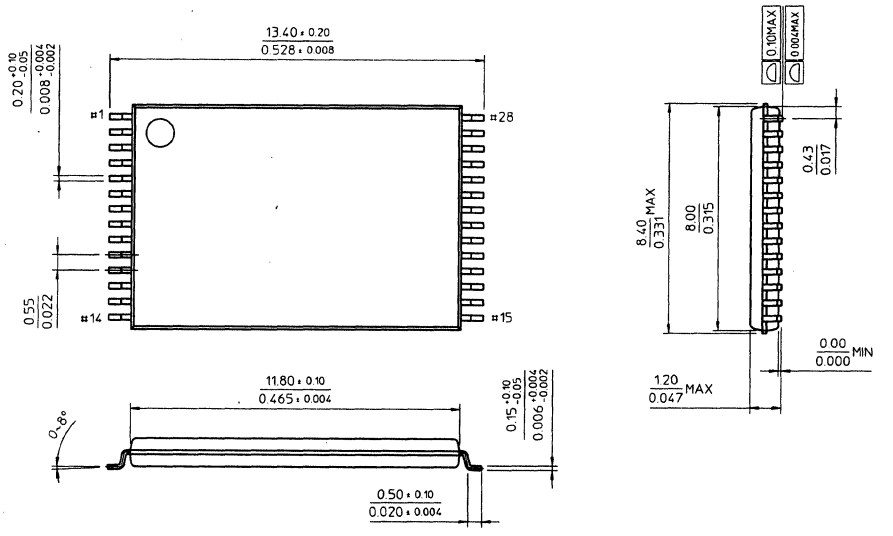
PACKAGE DIMENSIONS

Unit : mm/inch

32-SOP-525



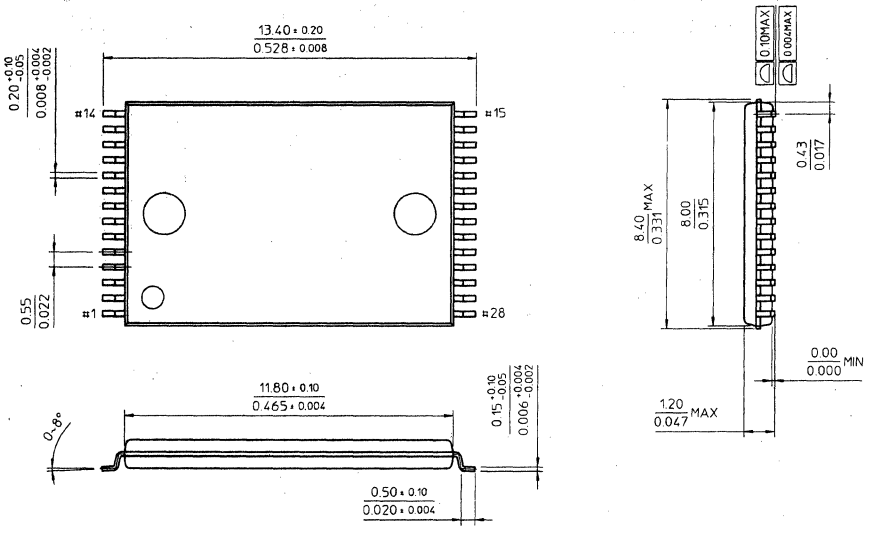
28-TSOP1-0813.4F



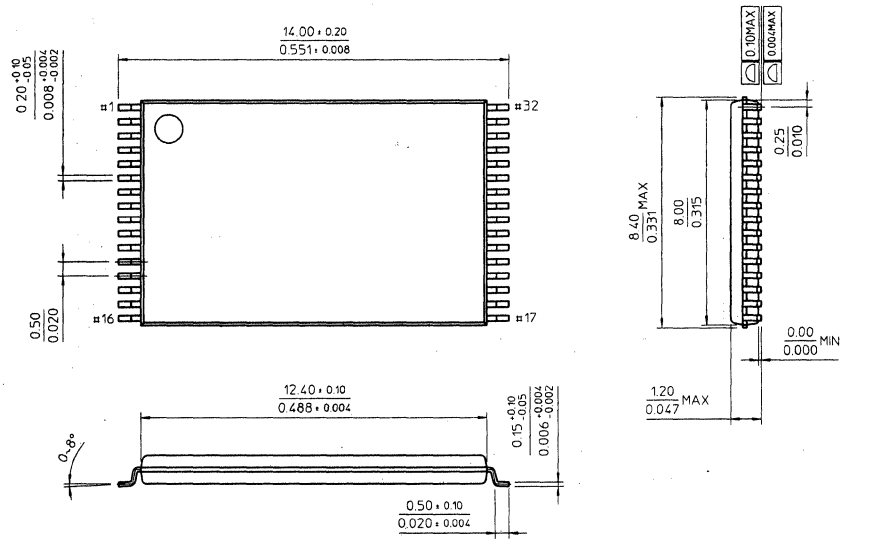
PACKAGE DIMENSIONS

Unit : mm/inch

28-TSOP1-0813.4R



32-TSOP1-0814F

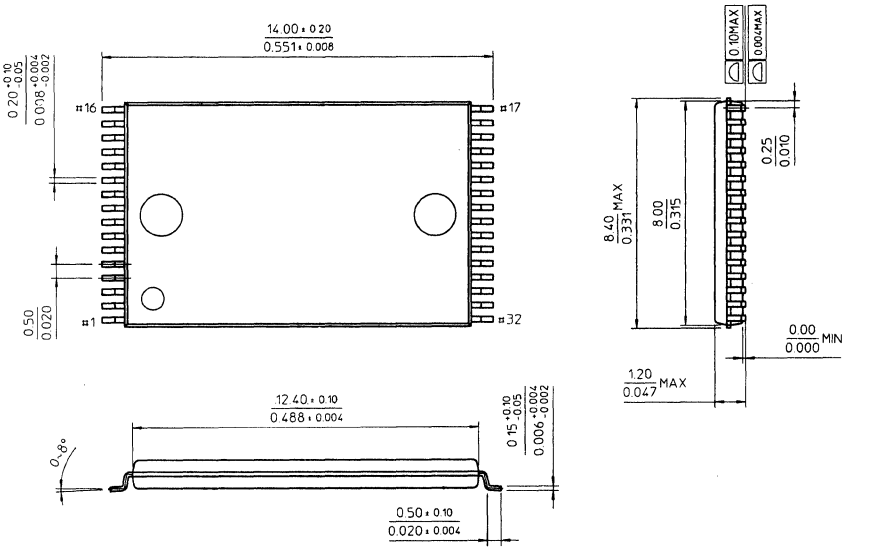


SAMSUNG ELECTRONICS

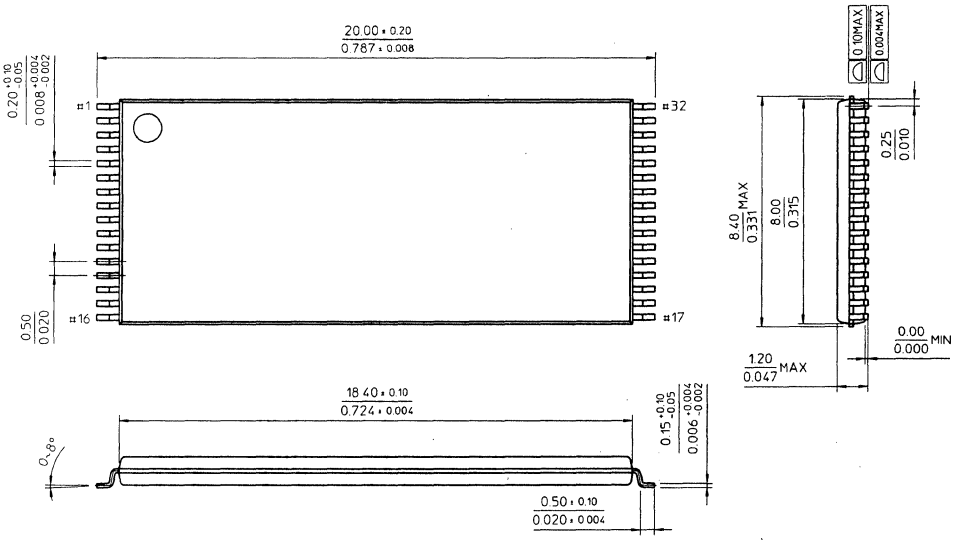
PACKAGE DIMENSIONS

Unit : mm/inch

32-TSOP1-0814R



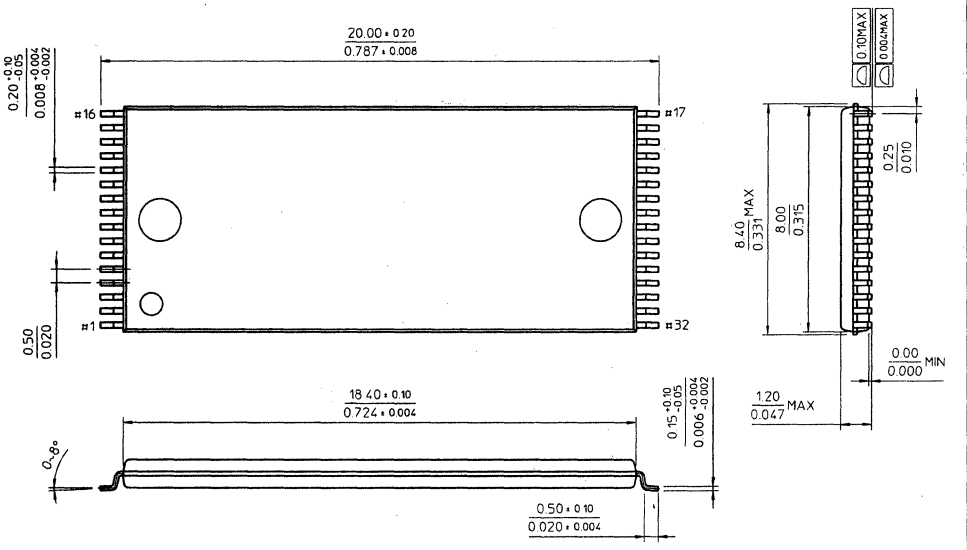
32-TSOP1-0820F



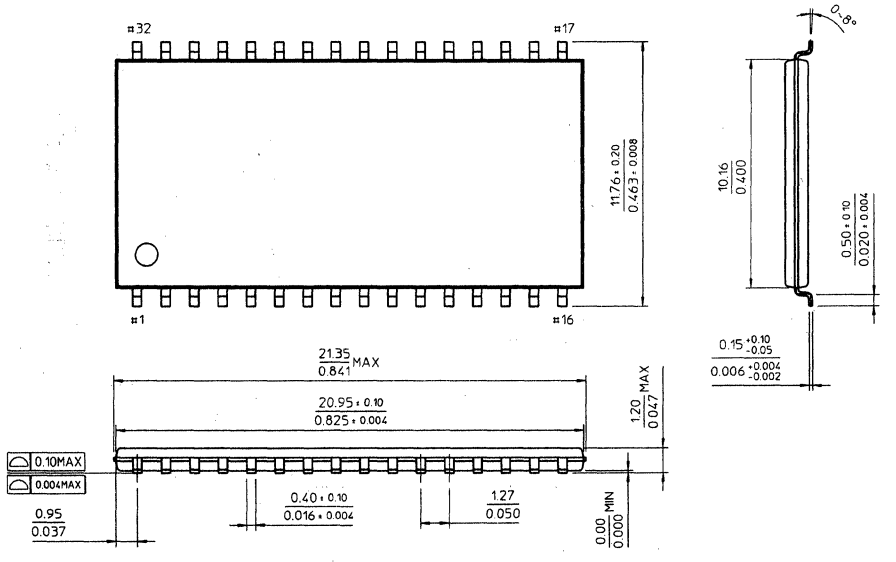
PACKAGE DIMENSIONS

Unit : mm/inch

32-TSOP1-0820R



32-TSOP2-400F

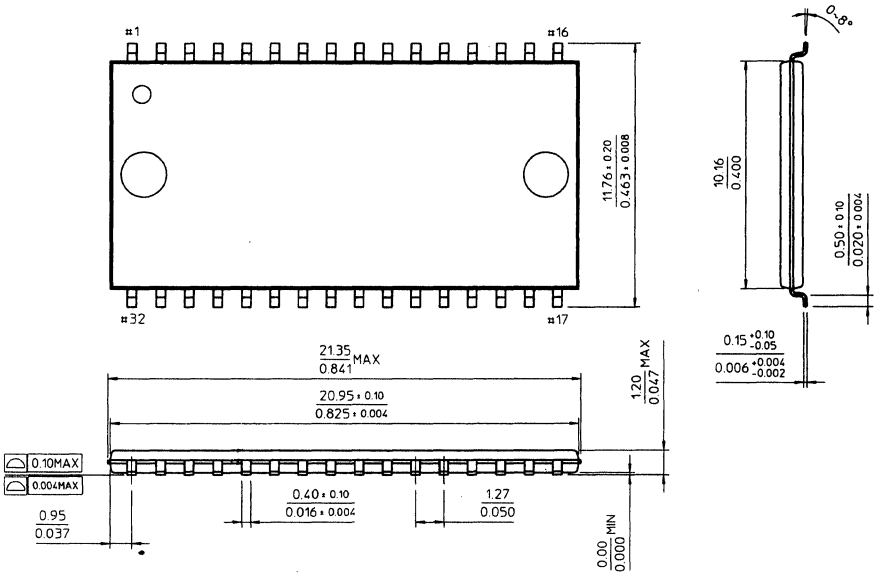


SAMSUNG ELECTRONICS

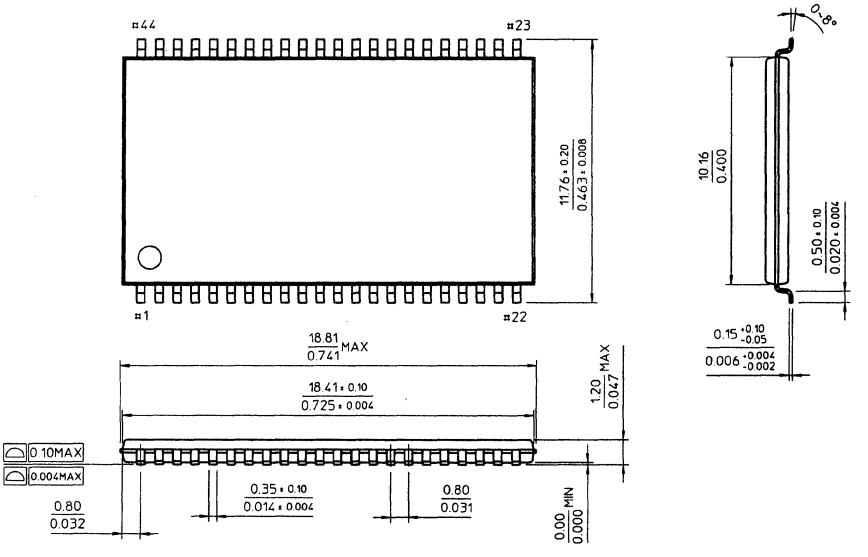
PACKAGE DIMENSIONS

Unit : mm/inch

32-TSOP2-400R



44-TSOP2-400F

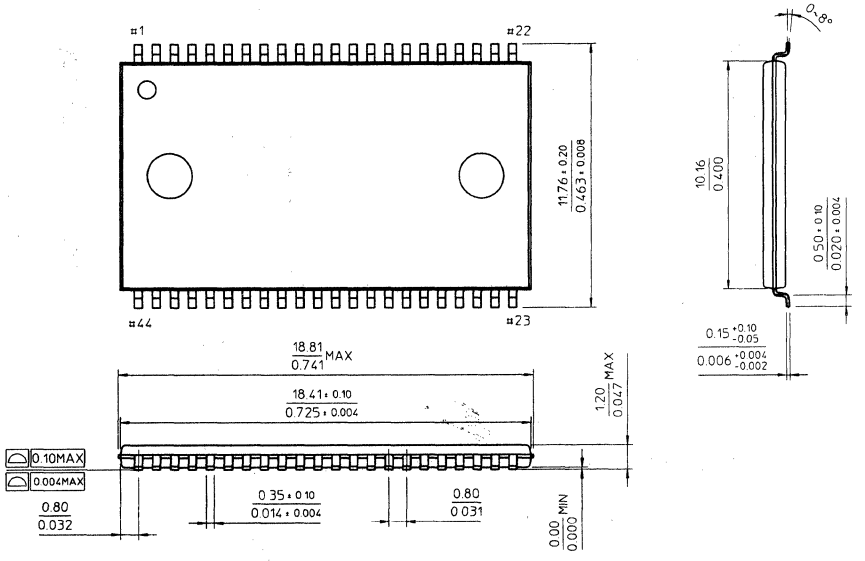


3

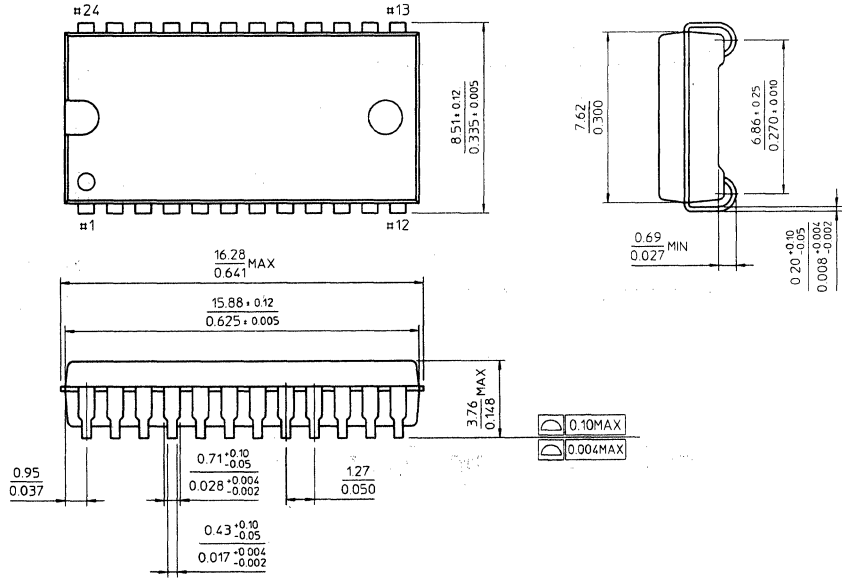
PACKAGE DIMENSIONS

Unit : mm/inch

44-TSOP2-400R



24-SOJ-300

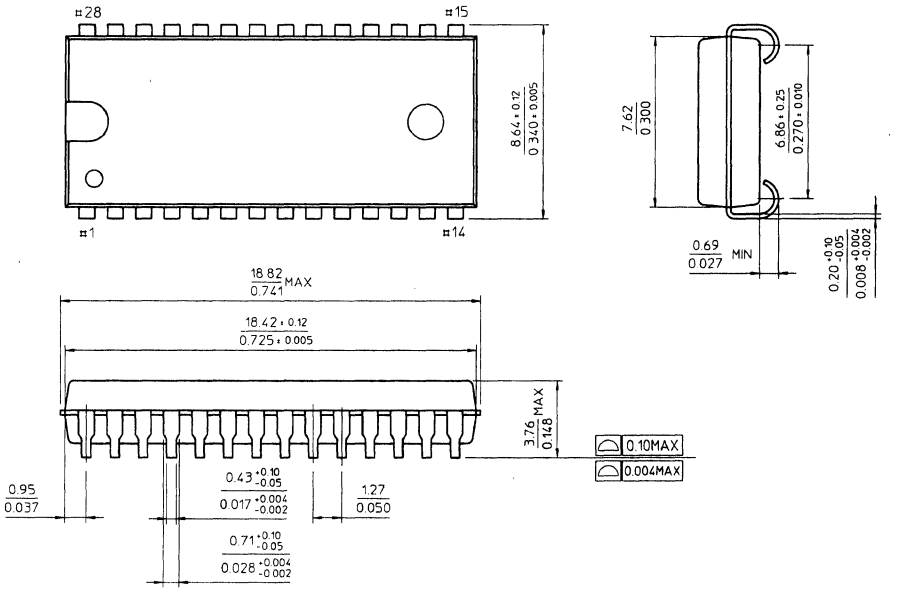


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

Unit : mm/inch

28-SOJ-300



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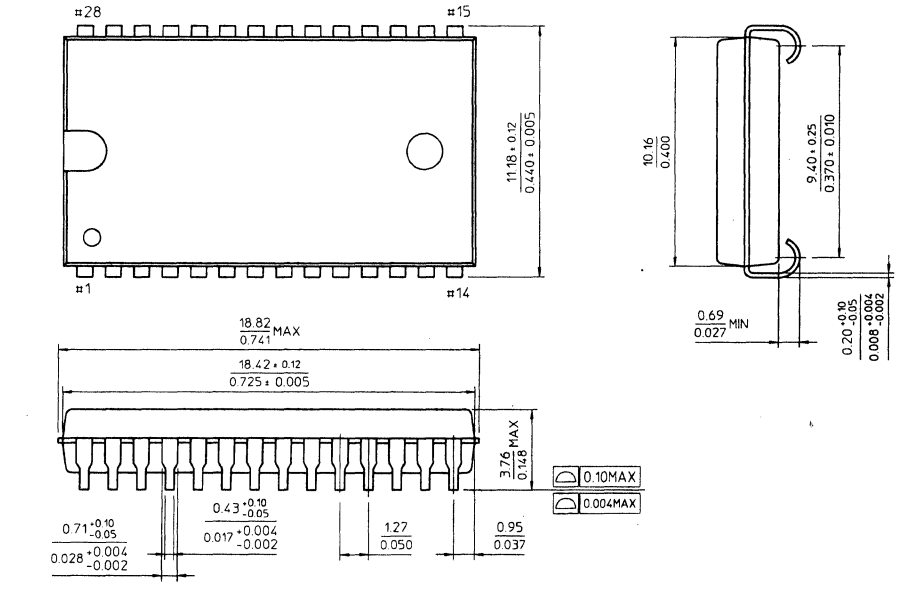
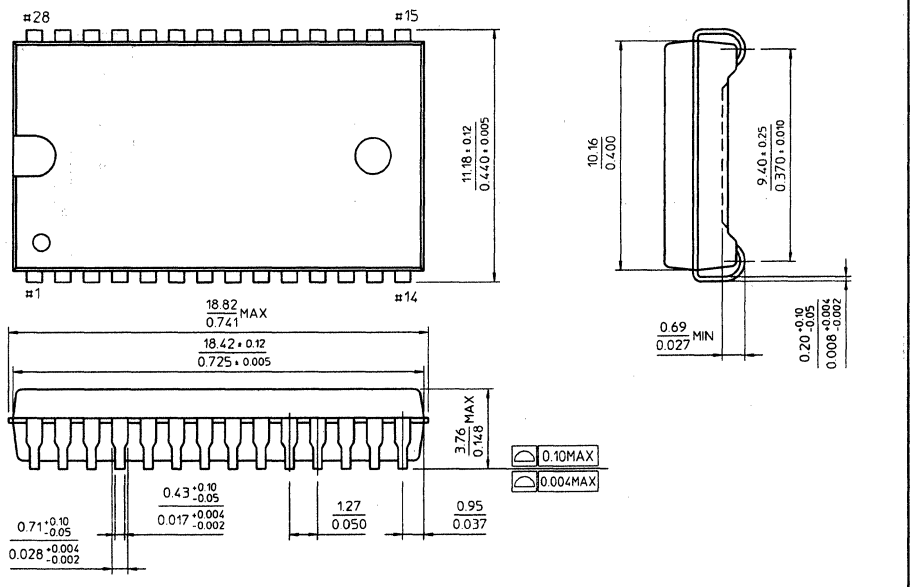


SAMSUNG ELECTRONICS

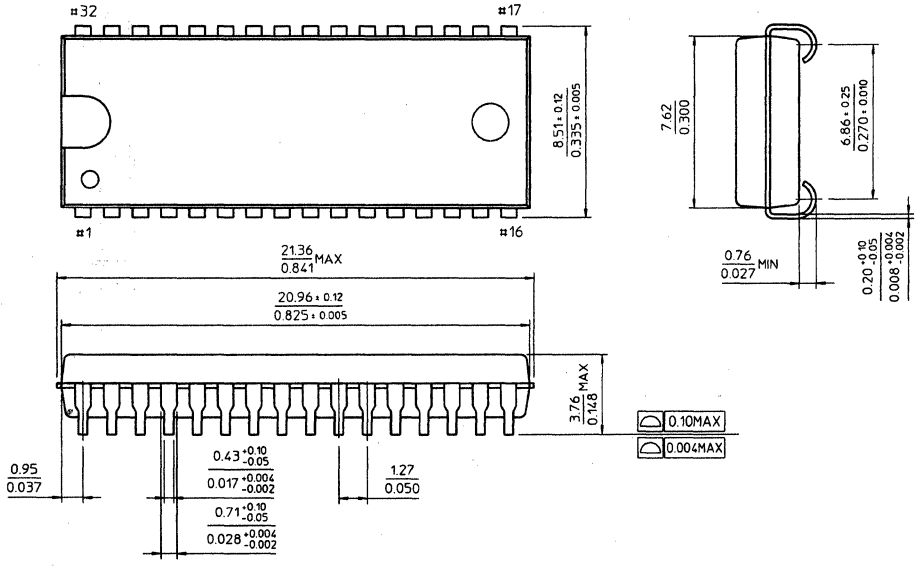
PACKAGE DIMENSIONS

Unit : mm/inch

28-SOJ-400B



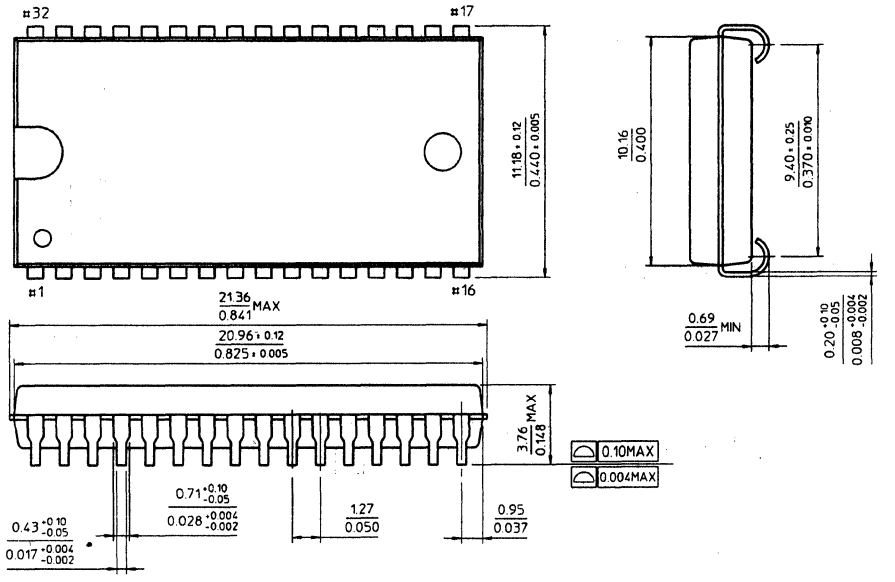
32-SOJ-300



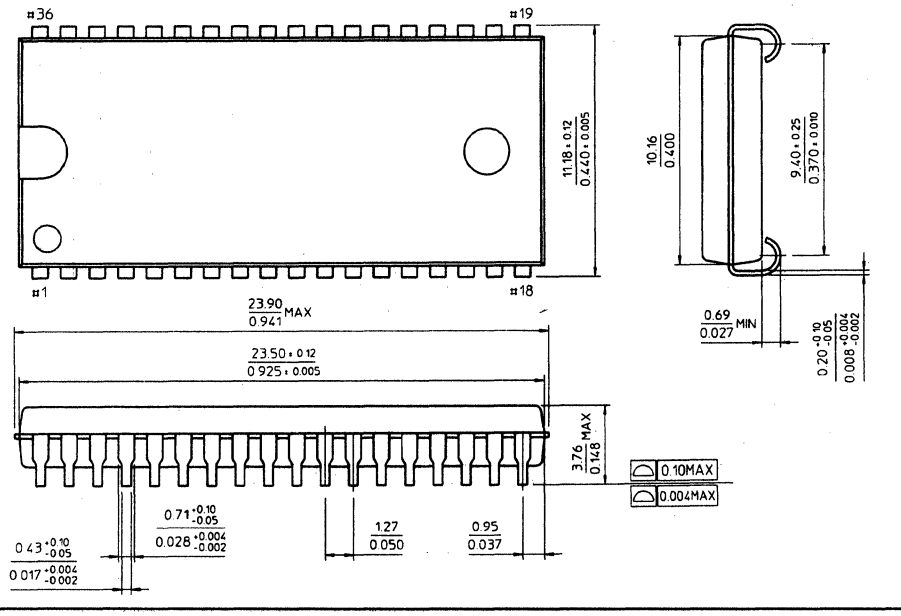
PACKAGE DIMENSIONS

Unit : mm/inch

32-SOJ-400



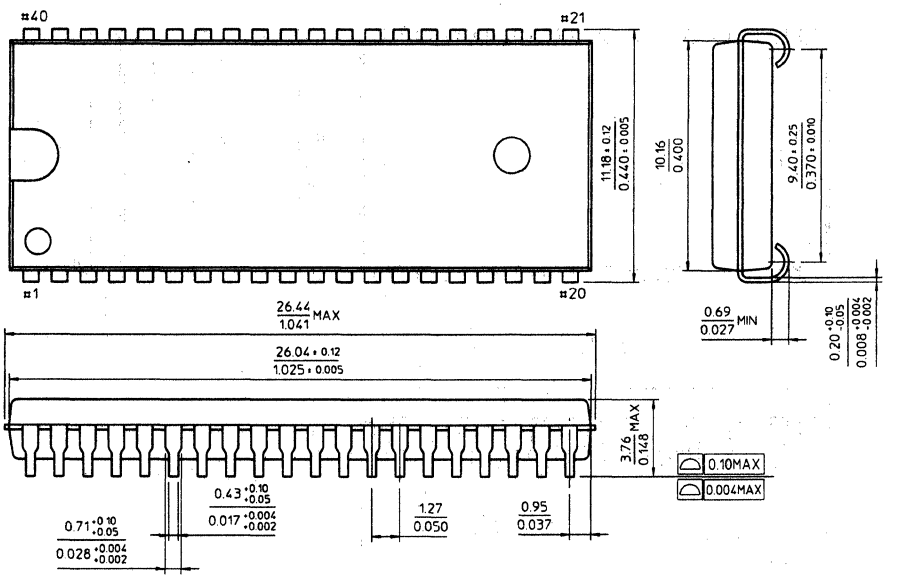
36-SOJ-400



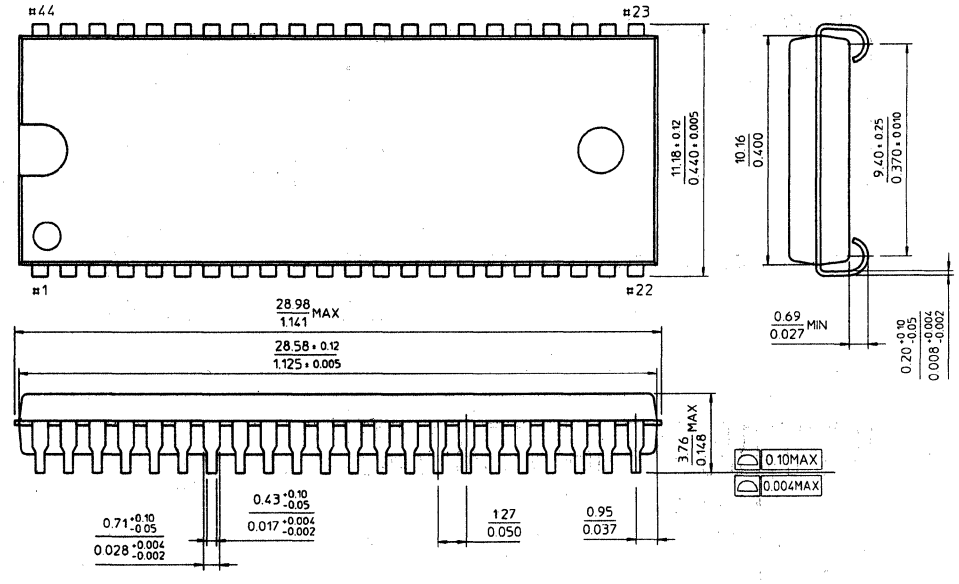
PACKAGE DIMENSIONS

Unit : mm/inch

40-SOJ-400



44-SOJ-400

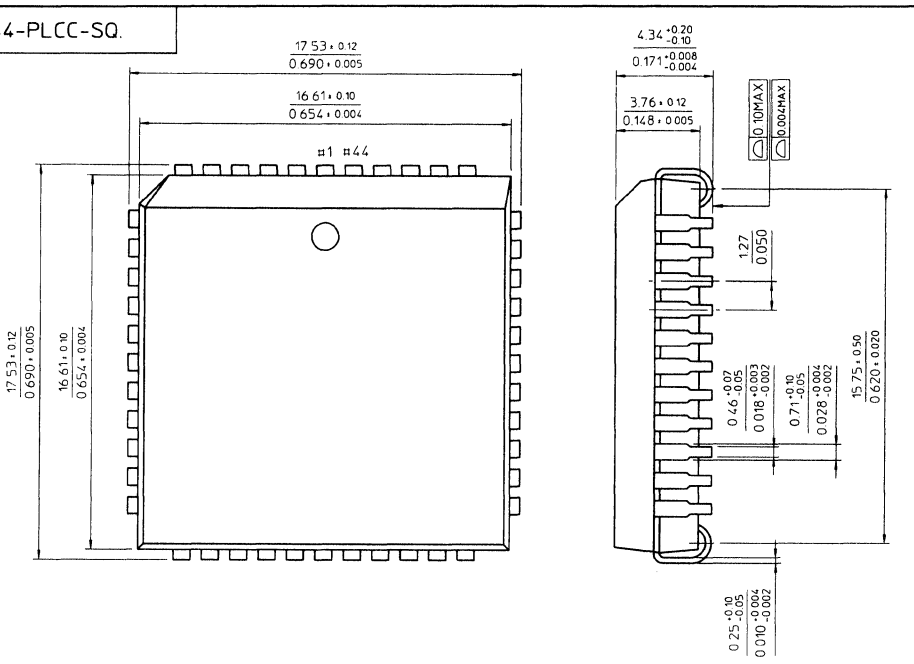


SAMSUNG ELECTRONICS

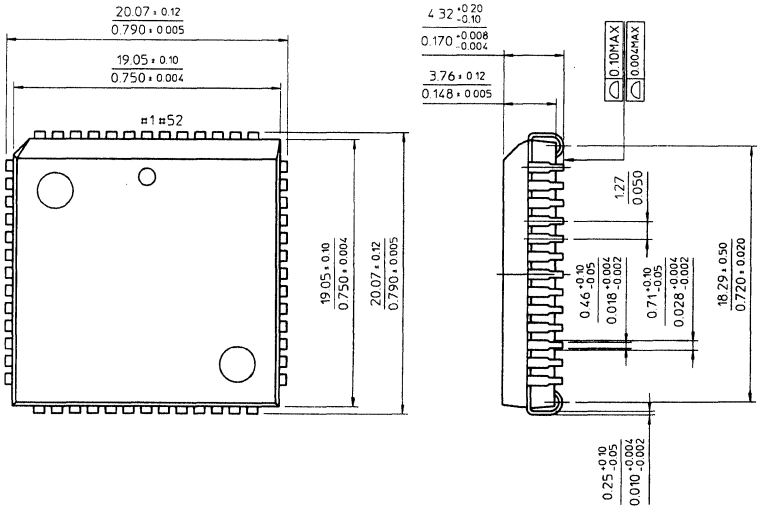
PACKAGE DIMENSIONS

Unit : mm/inch

44-PLCC-SQ.



52-PLCC-SQ.

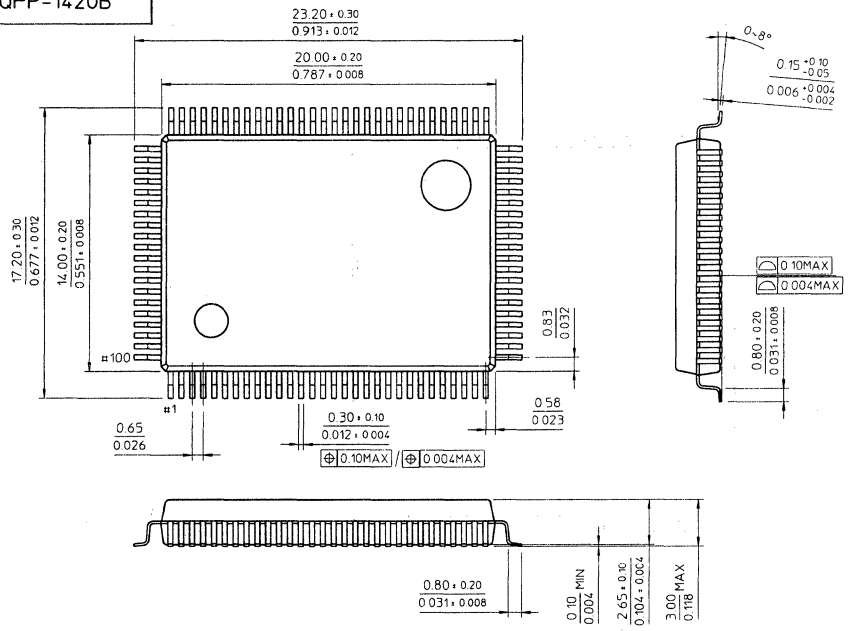


Under Development

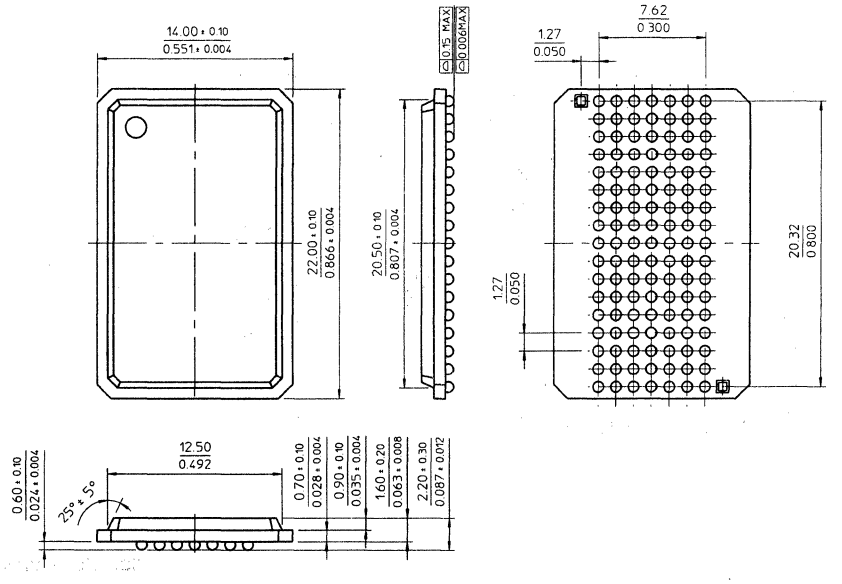
PACKAGE DIMENSIONS

Unit : mm/inch

100-QFP-1420B



119-BGA-1422

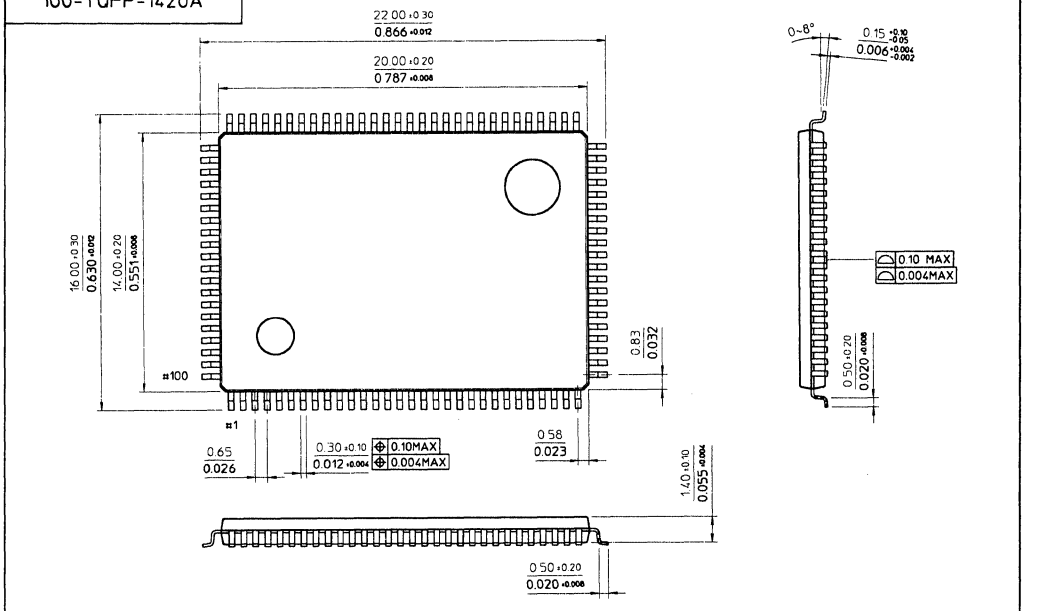


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

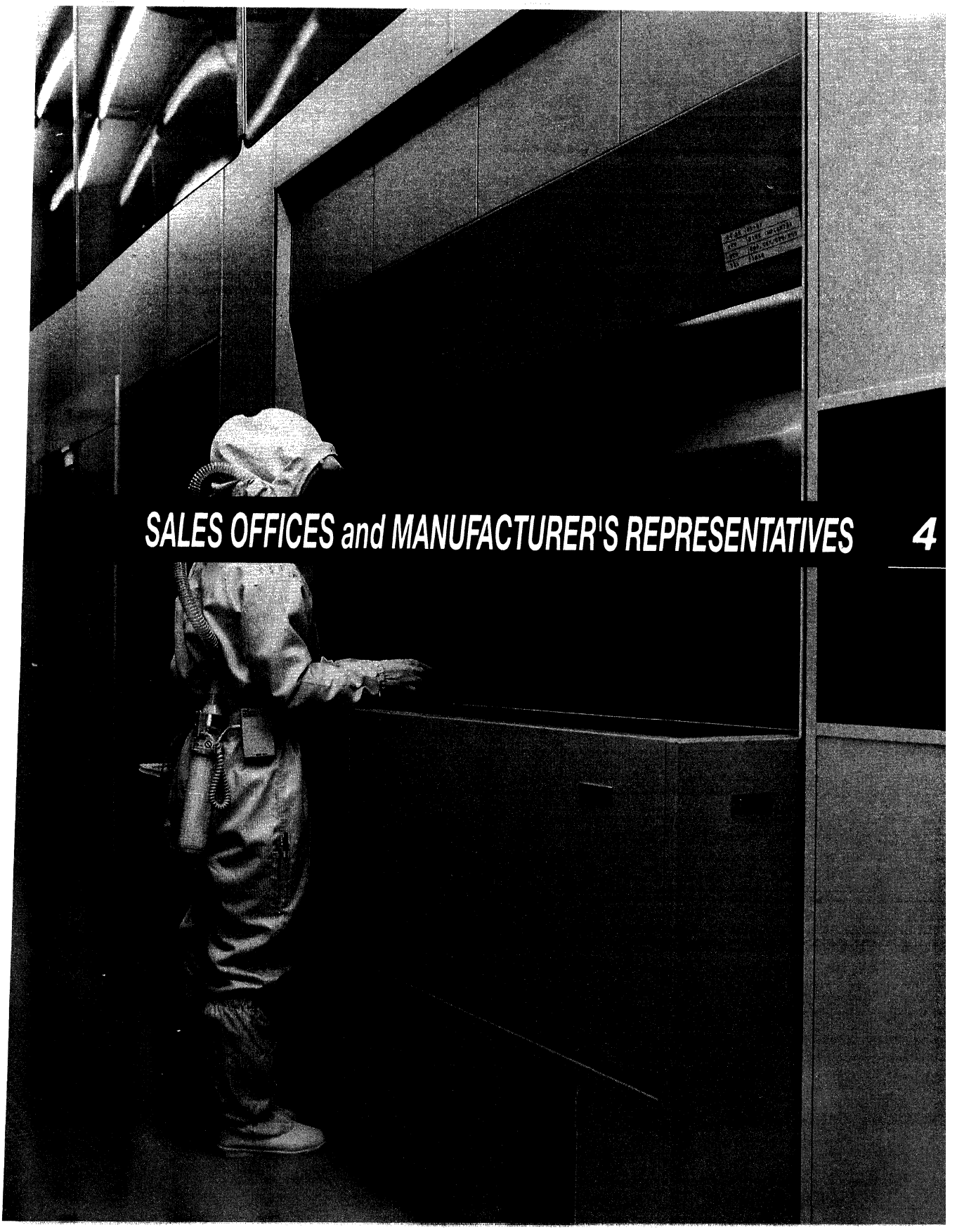
Unit : mm/inch

100-TQFP-1420A

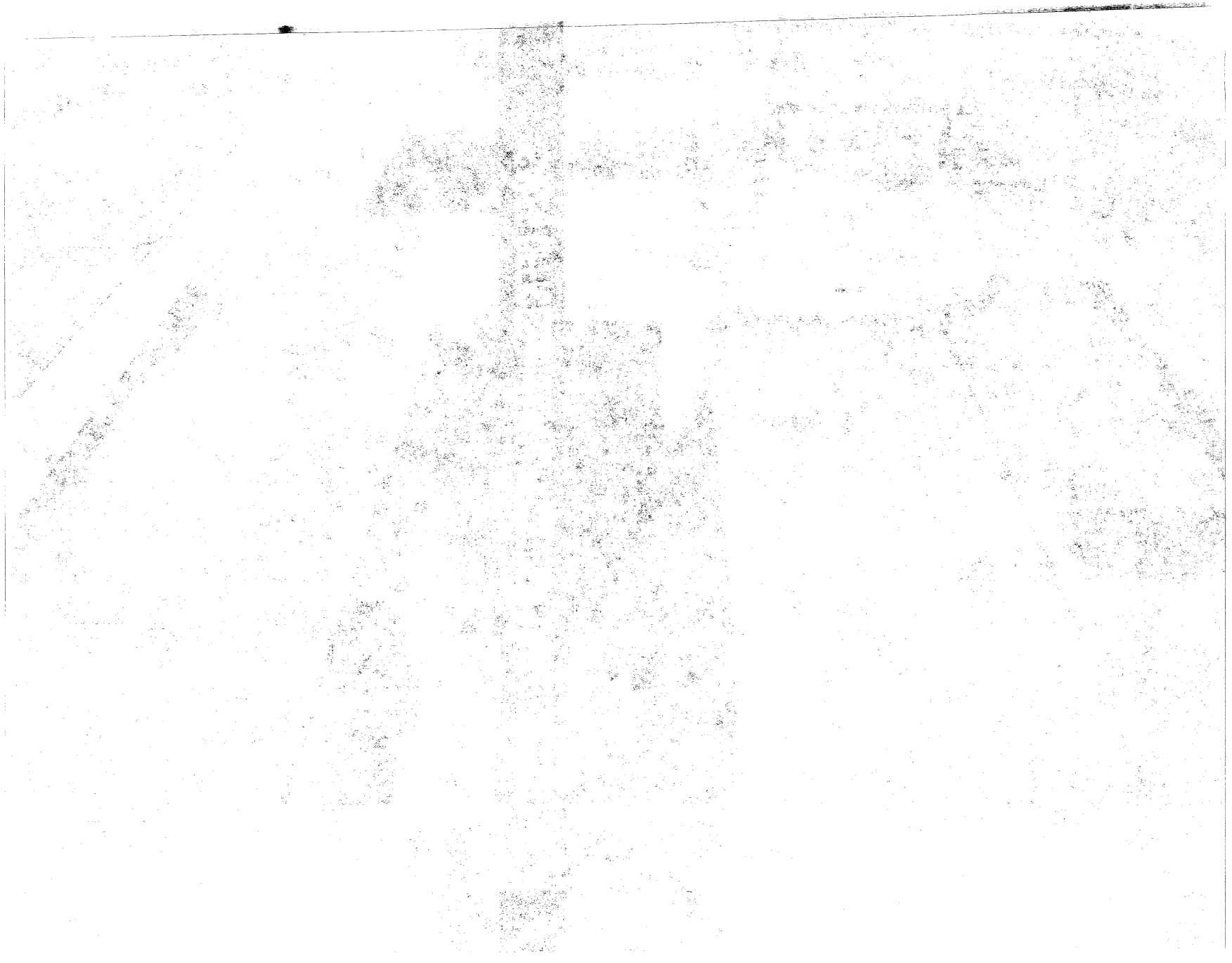


SAMSUNG ELECTRONICS

NOTES



SALES OFFICES and MANUFACTURER'S REPRESENTATIVES 4



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FAX: (408) 954-7883

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Itasca, IL 60143-2636
TEL: (708) 775-1050
FAX: (708) 775-1058

Northeast
119 Russell Street
Littleton, MA 01460
TEL: (508) 486-0700
FAX: (508) 486-8209

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16253 Laguna Canyon Road
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Irvine, CA 92718
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FAX: (714) 753-7544

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Suite 410
Dallas, TX 75248-3307
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FAX: (214) 770-7971

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FAX: (602) 861-2615

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FAX: (602) 797-2047

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FAX: (714) 453-7930

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J.N. BAILEY & ASSOCIATES — TEL: (216) 273-3798
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FAX: 0034-3-4-331944

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B3 B-1140 Brussels
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FAX: 0032-2-2456313

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94523 RUNGIS Cedex
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D-82041 Deisenhofen — FAX : 0049-89-6131668

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D-30539 Hannover Delete — FAX : 0049-551-8764160

MSC VERTRIEBS GmbH
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D-76297 Stutensee 3 — FAX : 0047-7249-7993

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D-41061 Moenchengladbach — FAX : 0049-2161-183313

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I-20090 Assago Mi — FAX : 0039-2-8242631/8242831

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I-40011 Anzola dell' Emilia — FAX : 0039-51-735013

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Fokkerstraat 511-513
Postbus 48
NI-3125 BD Schiedam
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FAX: 0031-10-4154867

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SEMICONDUCTORS S.A.
Ronda General Mitre
240 Bjs
E-08006 Barcelona
TEL: 0034-3-2172340
FAX: 0034-3-2176598

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Segersbyvaegen 3
P.P. Box 2001
S-14502 Norsborg
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FAX : 0046-853-175340

SWITZERLAND

ELBATEX AG
Hard Str. 72
CH-5430 Wettingen Schweiz
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FAX : 0041-56275532

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Leicestershire
LE17 4JB
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FAX : 0044-455-552612

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Cambridgeshire
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FAX : 0044-480-496621

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FAX : 7930811

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FAX : 3636203

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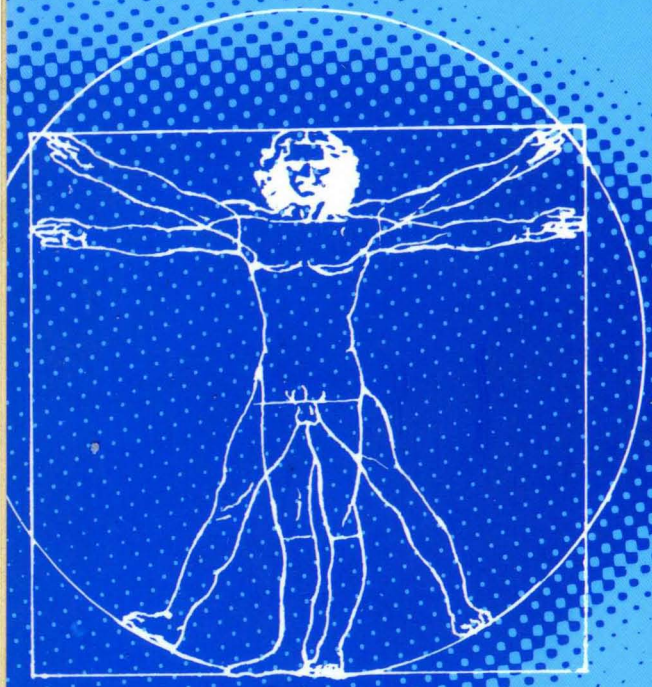

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